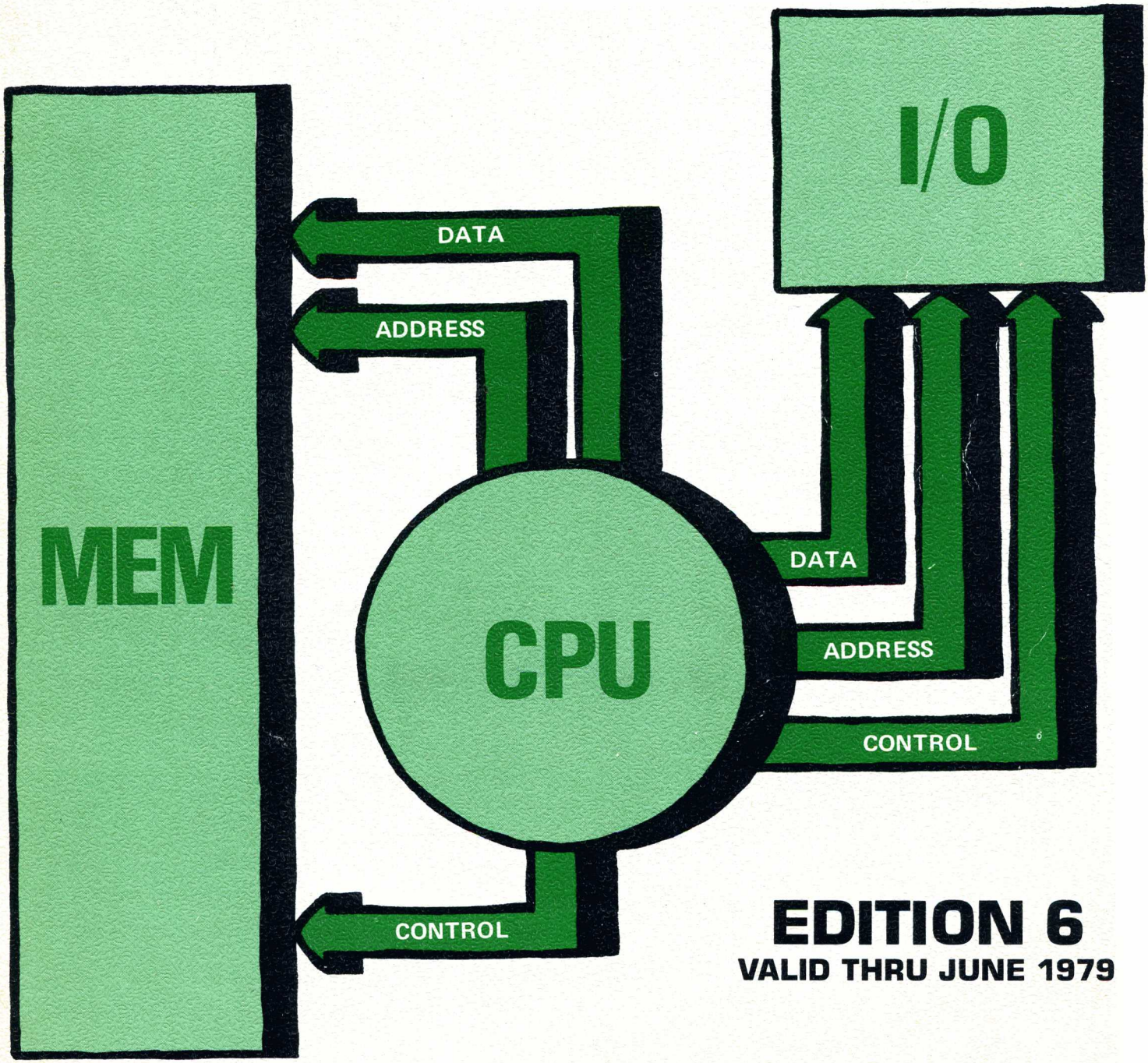
ELECTRONICS INFORMATION SERIES

MICROCOMPUTER D.A.T.A. BOOK®



EDITION 6

VALID THRU JUNE 1979

2. MICROCOMPUTER SYSTEMS

IN ORDER OF: (1)DATA BITS (2)MANUFACT. CODE & (3)SYSTEM TYPE No.

LINE No.	3 SYSTEM TYPE No.	ORGANIZ -ATION 1 DATA BITS	ARCHI -TECT -URE	SYS. CONFIGURATION ADDRESSABLE MEMORY (RAM/ROM) (BYTES)	I/O DEV @PT WIDTH (D/WDTH)	No. BASIC MICRO INSTR	No. ADDR MODE	INTERR -UPT LEVEL No. & TYPE	INSTRUCT TIME-TYP §CLK CYC *-MIN (s)	No. GEN PUR-POSE REG	STACK LEVEL	SYMBOL: PT-PORT V-VECTORED P-PRIORITY M-MULTIPLE OTHER CAPABILITIES	INSTR SET REF. No.	SYSTEM DWG.	2 MFR. CODE
1	MC14500B	1	ChF	256	32/1	16			100n			Industrial Control Unit	IS73	S89	MOTA
2	S2000	4	uCT	8k	1/8	51			4.0u		3	One Chip Microcomputer	IS79	S93	AMI
3	Am2900	4	ChF	4.0k	16/4	512△	4	VP	150n	16	4	Microprogrammable	IS63	S66	AMV
4	ASC40	4	CdF		256/4	45		P	10.8u	7		Uses Intel 4040 MPU	IS22		APS
5	IMC40	4	CdF	8.0k	320/4	60			10.8u	24		Uses C4040CPU	IS56	S58	COM
6▼	SYSTEM4	4	CdF	10k/32k	1024/1	45			12.5u*	24		Uses Intel 4004 CPU	IS14		DSI
7▼	SYSTEM4A	4	CdF	40k/8.0k	1024/1	60			10.8u*	24		Uses Intel 4040 CPU	IS14		DSI
8▼	SYSTEM4B	4	CdF	40k/8.0k	1024/1	60			7.0u*	24		Uses Intel 4040CPU	IS14		DSI
9▼	F2900	4	ChF	16/16	16/4	512△	4		75n*	16	4	Uses 2901CPU;Microprogrm	IS63		FSC
10#	HMCS42	4	uCT	32/512	4/3	74			10u			One Chip Microcomputer			HITJ
11#	HMCS43	4	uCT	80/1k	4/4	74		2P	10u	6	2	One Chip Microcomputer			HITJ
12#	HMCS43C	4	uCT	80/1k	4/4	74		2P	10u	6	2	One Chip Microcomputer			HITJ
13#	HMCS44	4	uCT	160/2k	4/4	69		2P	20u	6	2	One Chip Microcomputer			HITJ
14#	HMCS45	4	uCT	160/2k	6/4	69		2P	20u	6	2	One Chip Microcomputer	IS88	S120	HITJ
15	3000ITL	4	ChF	512	16/8	512△	5			11		MCU And CPE,I/O Expands	IS13	S4	ITL
16	MCS4	4	ChF	32k	128/4	46	4	V	10.8u	16		3 Subroutine Nesting	IS22a	S40	ITL
17	MCS40	4	ChF	64k	128/4	60		V	10.8u		7	Expanded MCS4	IS22		ITL
18#	MN1400	4	uCT	256/8k▼	24/4	75	2		10u		2	One Chip Microcomputer	IS72	S88	MATJ
19♦#	MN1402	4	uCT	128/8k▼	13/4	57	2		10u		2	One Chip Microcomputer	IS72	S147	MATJ
20▼#	MN1403	4	uCT	64/4k▼	12/4	50	2		10u		2	One Chip Microcomputer	IS72	S148	MATJ
21♦#	MN1404	4	uCT	64/4k▼	6/4	48	2		10u		2	One Chip Microcomputer	IS72	S149	MATJ
22♦#	MN1405	4	uCT	512/16k▼	24/4	75	2		10u		2	One Chip Microcomputer	IS72	S150	MATJ
23#	MN1430	4	uCT	256/8k▼	24/4	75	2		10u		2	One Chip Microcomputer	IS72	S88	MATJ
24▼#	MN1432	4	uCT	128/8k▼	13/4	58	2		15u		2	One Chip Microcomputer	IS72	S147	MATJ
25▼#	MN1435	4	uCT	512/16k▼	24/4	75	2		15u		2	One Chip Microcomputer	IS72	S150	MATJ
26▼#	MN1450	4	uCT	256/8k▼	24/4	75	2		10u		2	One Chip Microcomputer	IS72	S88	MATJ
27♦#	MN1498	4	ChF	256/8k▼	13/4	68	2		10u		2	uComp W/Ext Inst Mem	IS72	S151	MATJ
28♦#	MN1499	4	ChF	256/16k▼	21/4	75	2		10u		2	uComp W/Ext Inst Mem	IS72	S152	MATJ
29	5701	4	uCT	512	16/4	36			230n	16		4 Bit Slice Controller	IS18		MMI
30	6701	4	uCT	512	16/4	36			175n	16		4 Bit Slice Controller	IS18		MMI
31	M2900	4	ChF	512/8.0k	16/4	512△	4	VP	150n	16	4	Microprogrammable	IS63	S66	MOTA
32	M10800	4	ChF	256	256/4	16		MP		4		Full Binary And BCD	IS61	S44	MOTA
33	MC141000	4	uCT	256/8k▼	19/1	43			1.4u§			One Chip Microcomputer	IS90	S122	MOTA
34	MC141200	4	uCT	256/8k▼	24/1	43			1.4u§			One Chip Microcomputer	IS90	S122a	MOTA
35#	uCOM-4	4	ChF	16k/64k▼	120/8	55			7.5u		4	Uses NEC uPD751D CPU	IS60		NECJ
36#	uCOM-41	4	ChF	128/2k	16/4	69		8	6.4u*	2	8	Uses NEC uPD541D CPU	IS59		NECJ
37#	uCOM-42	4	uCT	384/19k▼	31/1	72			10u		4	uPD548C Chip Sys	IS80	S109	NECJ
38#	uCOM-43	4	uCT	384/16k▼	35/1	80		1V	10u	6	3	uPD546C Chip Sys	IS81	S110	NECJ
39#	uCOM-44	4	uCT		35/1	80			10u		1	uPD547C Chip Sys	IS81a	S111	NECJ
40#	uCOM-47	4	uCT	32/4k	4/4	103			5.0u		M	uPD766G Chip Sys	IS86	S117	NECJ
41	uCOM-45	4	uCT	128/5k	21/1	58			10u		1	uPD550C,554C Chip Sys	IS81	S112	NECM
42	COP402	4	uCT	128/0	23/1	57	3	2VP	4.0u	1	3	COP420 Without ROM			NSC
43	COP410L	4	uCT	128/4k▼	19/1	43	3	1VP	16u	1	2	5mA,4.5-9.5V Supply			NSC
44	COP411L	4	uCT	128/4k▼	15/1	43	3	1VP	16u	1	2	COP410L In 20 Pin Pkg			NSC
45	COP420	4	uCT	256/8k▼	23/1	57	3	2VP	4.0u	1	3	COP400 Family Software			NSC
46	COP420L	4	uCT	256/8k▼	23/1	57	3	2VP	16u	1	3	7mA,4-9V Supply			NSC
47	FIPS	4	ChF	36k▼	128/4	45	4	V	10.8u	16	3	3 Subroutine Nesting	IS22a	S40	NSC
48	IDM2900	4	ChF	16/16	16/4	512△			75n*	16		Microprogrammable	IS63	S130	NSC
49	MM5781/82	4	ChF	512/16k▼	24/1	52	3	2VP	10u*	2	2	Expandable ROM	IS93		NSC
50	MM5782/129	4	ChF	512/32k▼	24/1	52	3	2V	10u*	2	2	Direct VF/LED Display			NSC
51	MM5799N	4	uCT	384/12k▼	22/1	51	3	1VP	10u*	2	2	LED Drive,Serial I/O	IS92	S124	NSC
52	MM57140N	4	uCT	220/5k▼	24/1	39	3	1VP	15u*	1	2	Direct LED Display Drive	IS91	S123	NSC
53	MM57152N	4	uCT	240/6k▼	24/1	39	3	1VP	15u*	1	2	Direct VF Display Drive	IS91	S123	NSC
54	CM-41	4	SYS	640/2k	14/4	45	4		11.2u*	16	3	4004 KBD/DISP/TTY	IS22a		PRO
55	PLS-401	4	CoC	320/1.0k	9/4	44	4		11.2u*	16	3	One 4x6 Card 4004/1702	IS22a	S70	PRO
56	PLS-411	4	CoC	560/768	9/4	44	4		11.2u	16	3	4004/1702 One Card Sys	IS22a	S70a	PRO
57	PLS-441	4	CoC	640/1280	9/4	60	3	1V	11.2u	24	7	4040/1702 One Card Sys	IS22	S70b	PRO
58	MM75	4	uCT	48/640	22/1	50				4		PPS 4/1 One Chip Comp	IS100		RKW
59	MM76	4	uCT	48/640	31/1	50				4		PPS 4/1 One Chip Comp	IS100		RKW
60	MM77	4	uCT	96/1.3k	31/1	50				6		PPS 4/1 One Chip Comp	IS101		RKW
61	MM78	4	uCT	128/2.0k	31/1	50				6		PPS 4/1 One Chip Comp	IS101		RKW
62	PPS4	4	ChF	4k/4k	16/4	50		2	5.0u	1		Decimal And Binary	IS25	S16	RKW
63	PPS4/1	4	uCT	4k/4k	31/4	50		2	12.5u	1		Decimal And Binary	IS26	S17	RKW
64	PPS4/2	4	ChF	4k/4k	16/4	50		2	5.0u	1		2 Chip System	IS25a	S16	RKW
65	3000SIC	4	ChF	512	16/4	512△	5			11		MCU And CPE	IS13	S4	SIC
66	LS481	4	ChF		2/8	210△		M	100n§		M	Expand,Microprog Slice	IS85	S115	TII
67	S481	4	ChF		2/8	210△		M	60n§		M	Expand,Microprog Slice	IS85	S115	TII
68	SBP0400	4	ChF	512	16/4	76	6		1.0u§	8		Expandable,Microprogram	IS47	S45	TII
69	SBP0400A	4	ChF	512	16/4	76	6		200n§	8		Expandable,Microprogram	IS47	S45	TII
70	TMS1000	4	uCT	256/8.0k▼	23/1	43			15u		1	One Chip Microcomputer	IS7		TII
71	TMS1070	4	uCT	256/8.0k▼	23/1	43			15u		1	One Chip Microcomputer	IS7		TII
72	TMS1100	4	uCT	512/16k▼	23/1	54			15u		1	One Chip Microcomputer	IS8		TII
73	TMS1200	4	uCT	512/16k▼	25/1	43			15u		1	One Chip Microcomputer	IS7		TII
74	TMS1270	4	uCT	256/8.0k▼	27/1	43			15u		1	One Chip Microcomputer	IS7		TII
75	TMS1300	4	uCT	512/16k▼	28/1	54			15u		1	One Chip Microcomputer	IS8		TII
76	CR1872	4	uCT	128/512▼	16/4	20		2Po	10u	5		One Chip Microcontroller	IS89	S53	WDC
77▼	AMC95/4000	8	CoC	4k/12k	48/1	74		8V	250n§	7		Uses Am9080A,A-4 CPU	IS34		AuC
78	S6800	8	ChF	65k	64k/8☑	72	7	V	2.0u	6	M	DMA and Mult Processor	IS11	S1	AMI
79	Am9080A	8	ChF	64k	256/8	74		V	250n§*	7		DMA,TTL Compatible	IS34		AMV
80	70-100	8	CoC	4k/1k	256/8	78	4	8P	2.0u			Expan Options,Intel 8080	IS21		APP
81	EVENT2000	8	CdF	48k		78	4	8P	2.0-8.5u	7	M	Uses 8080A CPU	IS21		APP
82	ASC80	8	CdF	64k	128/8	78	4	8V	2.0u	6		Uses Intel 8080A MPU	IS21		APS
83	ASCZ80	8	CdF	64k	128/8	158	8	256V	1.6u	13		Uses Zilog Z80 CPU	IS64		APS
84▼	CSS-1143	8	CoC	1.0k/16k		158	7	M	500n§	12	M	Uses Z80 CPU	IS65	S144	CLI
85	LSERIES	8	CdF	16k	512/8	48		P	12.5u	6		Intel 8080 3 Card Set	IS29	S21	CLI
86	MM1	8	CdF	64k	8/8	78	4	8VP	500n§	6	16	Uses Intel 8080A	IS29	S90	CLI
87	MSERIES	8	CdF	64k	512/8	78		P	5.5-7.0u	6		Intel 8080 3 Card Set	IS29	S21	CLI
88♦	Z2	8	SYS	64k	256/8	158	10		1.0u*	19		Uses Z80A CPU	IS65		CRO
89	MPS	8	CdF	16k	32/8	48		1M	12u-44u	6	7	Custom System	IS16	S10	DEC
90	TDG6500SYS	8	CdF	64k	512/8	55		1V	1.0u§			Uses 6502CPU;Options	IS1		DIG
91	TDG6800SYS	8	CdF	64k	512/8	72		1V	1.0u§	6		Uses 6800CPU;Options	IS6		DIG
92	TDG8080SYS	8	CdF	64k	512/8	78		8VP	500n§	7		Uses 8080CPU;Options	IS21		DIG
93	TDGZ80SYS1	8	SYS	10k	8/8	78	11	128V	1.0u	16		Packaged Z80 CPU Sys	IS65	S98	DIG
94	TDGZ80SYS2	8	SYS	18k	8/8	78	11	128V	1.0u	16		Z80SYS1 W/Added Mem Bd	IS65	S98	DIG
95	DL8A	8	SYS	64k	256/8	72	4	8P	1.0-2.5u	8		Uses Intel 8080 MPU	IS21	S28	DNI
96	MICROMITE80	8	CoC	64k	256/8	72	4	8P	1.0-2.5u	8		Intel 8080,8.00x8.50 In	IS21		DNI
97▼	CONCEPT80	8	CdF	64k	64/1	78	4	8PrV	2.0-9.0u	6	M	Uses 8080CPU	IS21		DSI
98▼	SYSTEM8	8	CdF	64k	240/8	72	4	8V	500n§	8		Uses M80 CPU MOD	IS21		DSI
99▼	SYSTEM8A	8	CdF	64k	240/8	134	4	7V	250§	8		Uses M8A CPU MOD	IS5		DSI
100▼	DB8/1	8	SYS	32k/4k	3/8	158	10	V			M	Uses Z80 CPU	IS65		DYB
101	DMS	8	SYS	64k	64k/8☑	72	7	MPV	1.0u§	6	M	Uses Motorola 6800 CPU	IS6		DYN
102	uM-65	8	SYS	8.0k	2/8	55	14	16PV	2.5u			Uses MTY6512A CPU	IS84		ECD
103♦	INNOVATOR	8	CoC	64k/512	256/8	158	10	2M	1.0u	16	M	Z80A Based Bd,NOVA Host			EDSI
104	SYSTEM80C	8	CdF	64k	256/8	78		VP	175n§	8		Fast Bipolar CPU,DMA	IS21	S57	EMM
105	SYSTEM80HS	8	CdF	64k	256/8	78		VP	175n§	8		Fast Bipolar CPU,DMA	IS21	S57	EMM
106	SYSTEM80S	8	CdF	64k	256/8	78		VP	175n§	8		Fast Bipolar CPU,DMA	IS21	S57	EMM
107♦	MICRO68	8	SYS	64k	32k/18☑	72	7	MPV	1.0u§	2	M	Uses MOTA6800;Training		S7	EPA
108♦	MICRO68B	8	SYS	64k	32k/18☑	72	7	MPV	1.0u§	2	M	Uses MOTA6800		S7	EPA
109♦	MICRO68K	8	SYS	64k	2/16	72	7	4V	4.0n	2	M	Uses MOTA6800,Kit		S7	EPA
110	ETC1000	8	SYS	64k/8	256/8	55	13	8PV	5.0u		M	Uses 6502 CPU	IS1	S121	ETL

17. INSTRUCTION SETS

IN DRAWING NUMBER SEQUENCE

IS60

	Mnemonic	Instruction code OPR	Instruction code OPA	Description of Operation
Control instruction	NOP	0 0 0 0	0 × × ×	No operation
	STP	0 0 0 0	1 × × ×	Stop
	CFR	0 0 0 1	0 × × ×	reset CTF.
	CFS	0 0 0 1	1 × × ×	set CTF.
Address store instruction	SDR	0 0 1 0	0 r r r	store AC in $WR_{1-3}(n)$. n=rrr
	SDU	0 0 1 0	1 r r r	AC is incremented by one and stored in $WR_{1-3}(n)$. n=rrr
	SDS	0 0 1 0	1 1 1 1	SP is decremented and stores AC in $WR_{1-3}(n)$ with n specified by SP. n=(SP)
Address load instruction	LDR	0 0 1 1	0 r r r	load AC with $WR_{1-3}(n)$. n=rrr
	LDU	0 0 1 1	1 r r r	load AC with $WR_{1-3}(n)$. Then AC is incremented by one. n=rrr
	LDS	0 0 1 1	1 1 1 1	load AC with $WR_{1-3}(n)$ specified by SP. Then SP is incremented by one and the contents of AC and SC are exchanged. n=(SP)
	LDI	0 1 0 0 a_2 a_2 a_2 a_2	a_3 a_3 a_3 a_3 a_1 a_1 a_1 a_1	loads AC_H, AC_M, and AC_L with 12 bits expressed by a_3, a_2, and a_1 respectively.
Branch instruction	JCN	0 1 0 1 a_2 a_2 a_2 a_2	C_3 C_2 C_1 C_0 a_1 a_1 a_1 a_1	If J="1" exchange the contents of AC and SC then jump to SC_H, a_2, a_1. AC becomes SC+2. If J="0" execute SC+2. (Note 1)
Data load instruction	LAR	0 1 1 0	0 r r r	load A_{CC} with $WR_0(n)$. n=rrr
	LAD	0 1 1 0	1 0 0 0	load A_{CC} with the data of the memory location addressed by AC.
	LAM	0 1 1 0	1 m m m	load A_{CC} with the data of the memory location addressed by AC and mmm. (Note 2)
	LAI	0 1 1 1	d d d d	load A_{CC} with dddd.
Data store instruction	SAR	1 0 0 0	0 r r r	Store the A_{CC} content into $WR_0(n)$. n=rrr
	SAD	1 0 0 0	1 0 0 0	Store the A_{CC} content into the memory location addressed by AC.
	SAM	1 0 0 0	1 m m m	Store the A_{CC} content into the memory location addressed by AC and mmm. (Note 2)
Skip instruction	ISU	1 1 0 0	0 r r r	Skips to address SC+2, if $WR_0(n)=0$ n=rrr; Otherwise $WR_0(n)$ is incremented by one.
	ISD	1 1 0 0	1 r r r	Skips to address SC+2, if $WR_0(n)=0$ n=rrr; Otherwise $WR_0(n)$ is decremented by one.
Indirect load instruction	LIN	1 1 0 1	a_3 a_3 a_3 a_3	load TM and A_{CC} with the content of the memory location addressed by a_3 AC_M AC_L.
Arithmetic & Logic Operation	ORL	1 0 0 1	1 0 0 1	OR operation is carried out between the A_{CC} and the content of memory location addressed by AC.
	ANL	1 0 0 1	1 0 1 0	AND operation is carried out between the A_{CC} and the content of the memory location addressed by AC.
	EXL	1 0 0 1	1 1 0 0	Exclusive OR operation is carried out between the A_{CC} and the content of the memory location addressed by AC.
	ADR	1 0 1 0	0 r r r	Addition is carried out between the A_{CC} and the $WR_0(n)$. n=rrr
	ADD	1 0 1 0	1 0 0 0	Addition is carried out between the A_{CC} and the content of the memory location addressed by AC.
	ADM	1 0 1 0	1 m m m	Addition is carried out between the A_{CC} and the content of the memory location addressed by AC and mmm. (Note 2)
	SBR	1 0 1 1	0 r r r	Subtraction is carried out between the A_{CC} and the $WR_0(n)$. n=rrr
	SBD	1 0 1 1	1 0 0 0	Subtraction is carried out between the A_{CC} and the content of the memory location addressed by AC.
	SBM	1 0 1 1	1 m m m	Subtraction is carried out between the A_{CC} and the content of the memory location addressed by AC and mmm. (Note 2)

Note 1 : $J=\overline{C_3}\cdot(C_2\cdot A_{CC}=0+C_1\cdot OVF=1+C_0\cdot CDF=1)+C_3\cdot(\overline{C_2\cdot A_{CC}=0}+\overline{C_1\cdot OVF=1}+\overline{C_0\cdot CDF=1})$

Note 2 : The address for which three bits of AC_M are substituted with mmm.

AC_H AC_M AC_L

(× × × × × m m m × × × ×)

Operations for Registers

(OPR 1 1 1 0 is common to all)

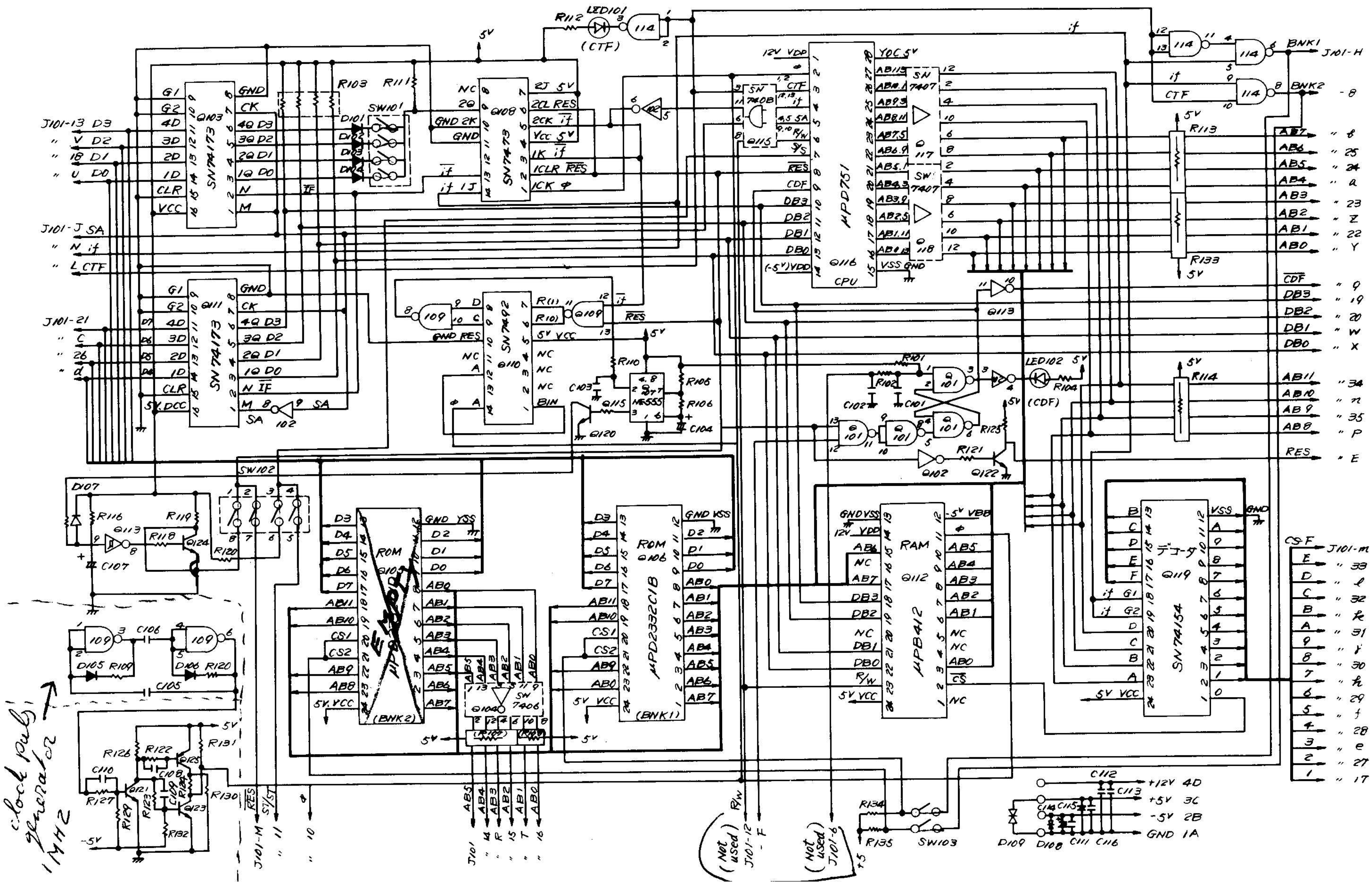
Mnemonic	OPA	Description of Operation
TAS	0 0 0 1	transfers the content of the AC to SC.
TSA	0 0 1 0	transfers the content of the SC to AC.
XSA	0 0 1 1	exchanges the content of the SC with AC.
IAC	0 1 0 0	AC is incremented by one.
DAC	0 1 0 1	AC is decremented by one.
TAL	1 0 0 0	transfers the content of the A_{CC} to AC_L.
TAM	1 0 0 1	transfers the content of the A_{CC} to AC_M.
TAH	1 0 1 0	transfers the content of the A_{CC} to AC_H.
TAT	1 0 1 1	transfers the content of the A_{CC} to TM.
TLA	1 1 0 0	transfers the content of the AC_L to A_{CC}.
TMA	1 1 0 1	transfers the content of the AC_M to A_{CC}.
THA	1 1 1 0	transfers the content of the AC_H to A_{CC}.
TTA	1 1 1 1	transfers the content of the TM to A_{CC}.

Operations for Accumulator

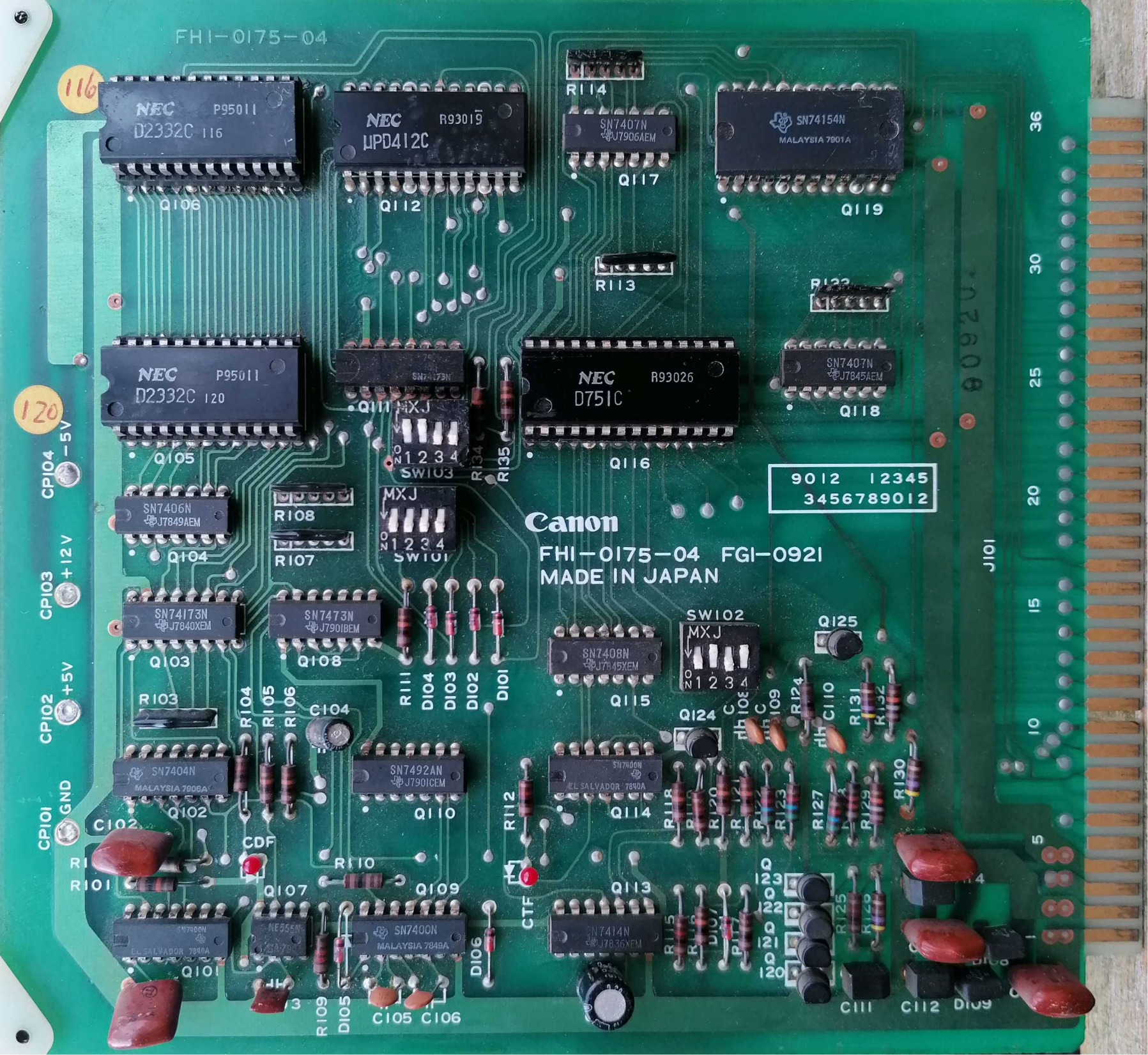
(OPR 1 1 1 1 is common to all)

Mnemonic	OPA	Description of Operation
CLB	0 0 0 0	clear A_{CC} and OVF.
CLC	0 0 0 1	clear OVF.
CLA	0 0 1 0	clear A_{CC}
CMC	0 1 0 0	Complement OVF; $\overline{OVF}\rightarrow OVF$.
CMA	0 1 0 1	Complement A_{CC}; $\overline{A_{CC}}\rightarrow A_{CC}$.
RAL	0 1 1 0	Rotate left. $OVF\rightarrow A_{CC0}$, $A_{CC3}\rightarrow OVF$, $A_{CCi}\rightarrow A_{CCi+1}$.
RAR	0 1 1 1	Rotate right. $A_{CC0}\rightarrow OVF$, $OVF\rightarrow A_{CC3}$, $A_{CCi}\rightarrow A_{CCi-1}$.
INC	1 0 1 0	A_{CC} is incremented by one.
DEC	1 0 1 1	A_{CC} is decremented by one.
DAA	1 1 0 0	Decimal adjust A_{CC} in addition.
DAS	1 1 0 1	Decimal adjust A_{CC} in subtraction.

CPU AND ROM



SN74173
Q103
Q111
R103
R111
SW101
SW102
SW103
SN7473
Q108
SN7492
Q110
LED101
(CTF)
LED102
(CDF)
μPD751
Q116
CPU
SN7407
Q117
Q118
SN7408
Q115
NE555
ROM
Q106
μPD2332C1B
(BNK1)
(BNK2)
EMPTY
RAM
Q112
μPB412
SN74154
Q119
デコーダ
SN7406
Q104
R113
R114
R133
BNK1
BNK2
J101-H
J101-13 D3
J101-J SA
J101-21
J101-M
J101-12
J101-6
CS-F
J101-m
(Not used)
clock pulse generator 1MHz
+12V 4D
+5V 3C
-5V 2B
GND 1A


FHI-0175-04
116
120
NEC P95011 D2332C 116
NEC R93019 μPD412C
NEC P95011 D2332C 120
NEC R93026 D751C
SN74154N MALAYSIA 7901A
SN7407N J7906AEM
SN7407N J7845AEM
SN7406N J7849AEM
SN74173N J7840XEM
SN7473N J7901BEM
SN7408N J7845XEM
SN7404N MALAYSIA 7808A
SN7492AN J7901CEM
SN7400N EL SALVADOR 7840A
SN7400N MALAYSIA 7849A
SN7414N J7836XEM
NE555N
Q101
Q102
Q103
Q104
Q105
Q106
Q107
Q108
Q109
Q110
Q111
Q112
Q113
Q114
Q115
Q116
Q117
Q118
Q119
Q124
Q125
SW101
SW102
SW103
MXJ
ON 1 2 3 4
9012 12345
3456789012
Canon
FHI-0175-04 FGI-0921
MADE IN JAPAN
J101
CP101 GND
CP102 +5V
CP103 +12V
CP104 -5V
CDF
CTF
C102
C104
C105
C106
C109
C110
C111
C112
D101
D102
D103
D104
D105
D106
D109
R101
R103
R104
R105
R106
R107
R108
R109
R110
R111
R112
R113
R114
R123
R124
R127
R129
R130
R131
R132
R134
R135