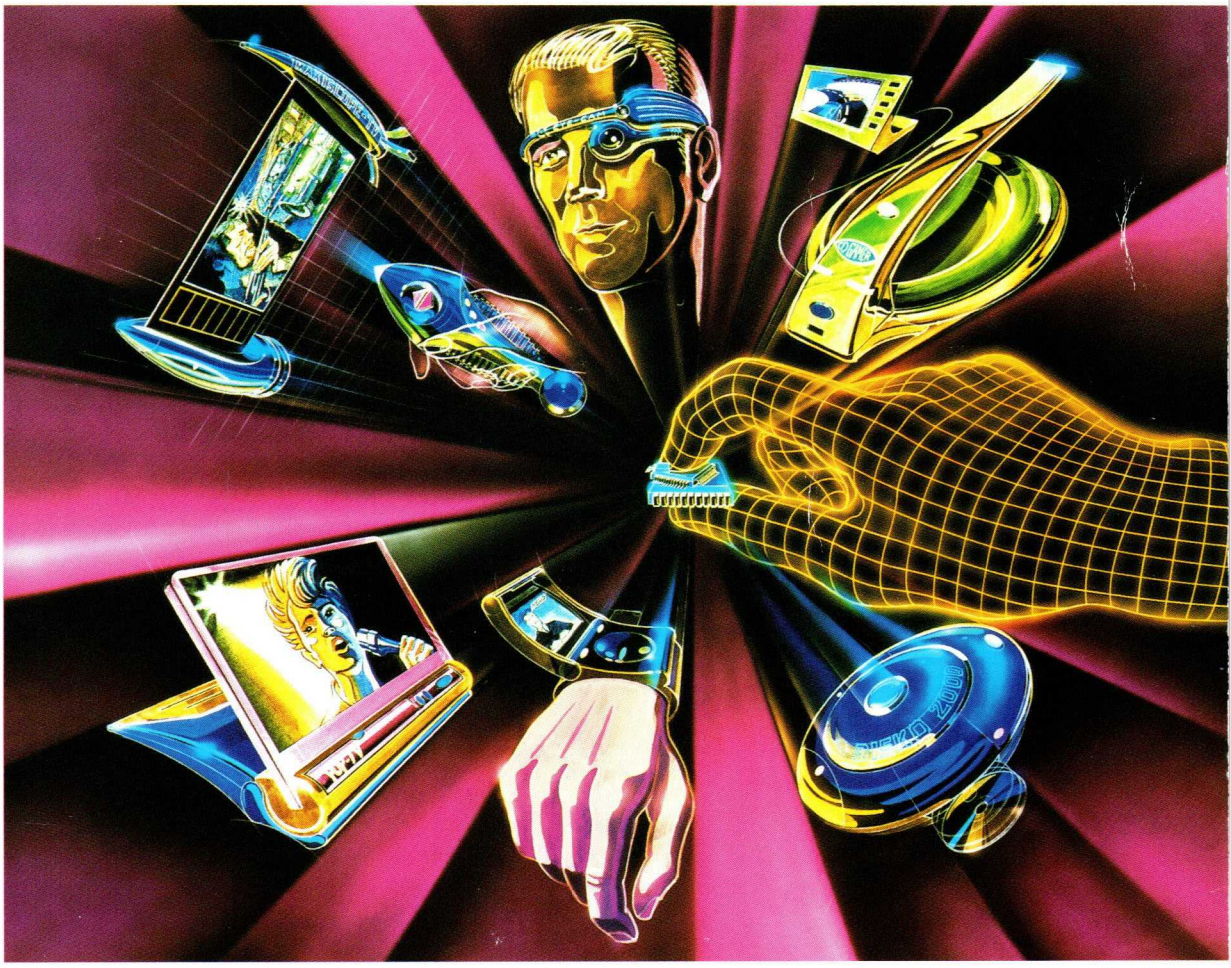
INTEGRATED CIRCUITS

Semiconductors for Television and Video Systems

80/83C528 to TDA2555; TDA2557



1995

DATA HANDBOOK IC02a

Philips Semiconductors

PHILIPS

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Semiconductors for Television and Video Systems

CONTENTS

Page

PART A

SELECTION GUIDE
- Functional index 4
- Alphanumerical index 21

GENERAL
- Quality 36
- Rating systems 37
- Pro electron type numbering system of integrated circuits 39
- Handling MOS devices 41

DEVICE DATA
- 80/83C528 to TDA2555;TDA2557 44

PART B

SELECTION GUIDE
- Functional index 1588
- Alphanumerical index 1605

DEVICE DATA
- TDA2578A to TDA8415 1621

PART C

SELECTION GUIDE
- Functional index 3236
- Alphanumerical index 3253

DEVICE DATA
- TDA8416 to μA733;733C 3269

PACKAGE INFORMATION
- Package outlines 4789
- Soldering 4845

DATA HANDBOOK SYSTEM 4847

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
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SELECTION GUIDE

	Page
Functional index	4
Alphanumerical index	21

		PAGE
TUNING/TUNER		
Tuning		
SAB6456; SAB6456T	Sensitive 1 GHz divide-by-64/divide-by-256 switchable prescaler	1347
SAB8726	Sensitive 2.6 GHz divide-by-2 prescaler	1353
TDA8725T	Antenna signal processor	3785
TSA5511	1.3 GHz bidirectional I²C-bus controlled synthesizer	4685
TSA5512	1.3 GHz bidirectional I²C-bus controlled synthesizer	4697
TSA5514	1.3 GHz bidirectional I²C-bus controlled synthesizer	4709
TSA5515T	1.3 GHz bidirectional I²C-bus controlled synthesizer	4721
TSA5520; TSA5521	1.3 GHz universal bus-controlled TV synthesizer; I²C-bus	4732
TSA5522	1.4 GHz I²C-bus controlled synthesizer	4749
TSA5526; TSA5526A	1.3 GHz universal bus-controlled TV synthesizer; I²C-bus	4762
TSA5527; TSA5527		
Tuner		
BA481	UHF mixer diode	89
BA482; BA483; BA484	Silicon planar diodes	90
BA582	Silicon planar diode	91
BA682; BA683	Band-switching diodes for surface mounting	92
BAT17	Schottky barrier diode	93
BAT18	Silicon planar diode	94
BF547	NPN 1 GHz wideband transistor	128
BF747	NPN 1 GHz wideband transistor	133
BFS17	NPN 1 GHz wideband transistor	153
BFS17A	NPN 3 GHz wideband transistor	154
SAA1300	Tuner switching circuit; I²C-bus	397
TDA5030A	TV VHF mixer/oscillator/UHF preamplifier	2619
TDA5030AT	TV VHF mixer/oscillator/UHF preamplifier	2625
TDA5330T	VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2655
TDA5332T	Double mixer/oscillator for TV and VCR tuners	2669
TDA5630	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2677
TDA5630BT	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 2-band tuners	2690
TDA5630CT	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2701

		PAGE
TDA5631	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2714
TDA5632	Low power VHF and UHF mixer/oscillator for TV and VCR 2-band tuners	2727
TDA5633	Low power VHF and UHF mixer/oscillator for TV and VCR 2-band tuners	2737
TDA5634T	Low power UHF mixer/oscillator for TV and VCR tuners	2747
TDA5636	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2756
TDA5637	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2773
TDA5731M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2790
TDA5732M	Low power VHF, UHF mixer/oscillator for TV and VCR 2-band tuners	2804
TDA5736M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2819
TDA5737M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2837
Varicap		
BB119	Silicon variable capacitance diode	95
BB131	VHF variable capacitance diode	96
BB132	VHF variable capacitance diode	97
BB133	VHF variable capacitance diode	98
BB134	UHF variable capacitance diode	99
BB135	UHF variable capacitance diode	100
BB148	VHF variable capacitance diode	101
BB149	UHF variable capacitance diode	102
BB150	VHF variable capacitance diode	103
BB215	UHF variable capacitance diode	104
BB405B	UHF variable capacitance diode	105
BB417	Variable capacitance diode	106
BB515	UHF variable capacitance diode	107
BB619	VHF variable capacitance diode	108
BB620	VHF variable capacitance diode	109
BB809	Silicon planar variable capacitance diode	110
BB811	UHF variable capacitance diode	111
BB901	Variable capacitance diode	112
BB909A; BB909B	Silicon planar variable capacitance diode	113

		PAGE
BB910	VHF variable capacitance diode	114
BB911A	VHF variable capacitance diode	115
BBY31	Variable capacitance diode	116
BBY39	Double variable capacitance diode	117
BBY40	Variable capacitance diode	118
BBY42	VHF variable capacitance diode	119
BBY62	Double variable capacitance diode	120
BY229 series	Rectifier diodes fast, soft-recovery	156
BY329 series	Rectifier diodes fast, soft-recovery	158
BY359F-1500	Rectifier diode fast, high-voltage	159
BY359X-1500	Rectifier diode fast, high-voltage	160
Dual gate n-channel MOSFET		
BF904; BF904R	Dual-gate MOS-FET	137
BF960	Silicon N-channel dual-gate MOS-FET	138
BF964S	Silicon N-channel dual-gate MOS-FET	139
BF966S	Silicon N-channel dual-gate MOS-FET	140
BF980A	Silicon N-channel dual-gate MOS-FET	141
BF981	Silicon N-channel dual-gate MOS-FET	142
BF982	Silicon N-channel dual-gate MOS-FET	143
BF988	Silicon N-channel dual-gate MOS-FET	144
BF989	Silicon N-channel dual-gate MOS-FET	145
BF990A	Silicon N-channel dual-gate MOS-FET	146
BF991	Silicon N-channel dual-gate MOS-FET	147
BF992	Silicon N-channel dual-gate MOS-FET	148
BF994S	Silicon N-channel dual-gate MOS-FET	149
BF996S	Silicon N-channel dual-gate MOS-FET	150
BF997	Silicon N-channel dual-gate MOS-FET	151
BF998	Silicon N-channel dual-gate MOS-FET	152
IF		
Vision IF		
TDA2549	IF amplifier and demodulator for multistandard TV receivers	1565
TDA3840	TV IF amplifier and demodulator with TV signal identification	1932
TDA3842	Multistandard TV IF amplifier and demodulator with TV signal identification	1944
TDA3853T	TV IF amplifier and demodulator with TV signal identification	1976
TDA8340; TDA8341	Television IF amplifier and demodulator	3061
TDA8349A	Multistandard IF amplifier and demodulator	3072
TDA9800	VIF-PLL demodulator and FM-PLL detector	4301

		PAGE
TDA9802	Multistandard VIF-PLL demodulator and FM-PLL detector	4317
TDA9803	Multistandard VIF-PLL demodulator	4332
TDA9804	VIF-PLL demodulator with internal or external AGC and FM-PLL detector	4345
TDA9808	Single standard VIF-PLL with QSS-IF and FM-PLL demodulator	4360
TDA9812	Multistandard VIF-PLL and FM-PLL/AM demodulator	4378
TDA9814T	Multistandard VIF-PLL with QSS-IF and dual FM-PLL/AM demodulator	4404
TDA9815	Multistandard/MAC VIF-PLL with QSS-IF and dual FM-PLL/AM demodulator	4427
Sound IF		
TDA2545A	Quasi-split-sound circuit	1553
TDA2546A	Quasi-split-sound circuit with 5.5 MHz demodulation	1559
TDA3845; TDA3845T	Quasi-split sound circuit and AM demodulator	1963
TDA3856	Quasi-split sound processor for all standards	1990
TDA3857	Quasi-split sound processor with two FM demodulators	2002
TDA3858	Quasi-split sound processor for all standards	2013
TDA3866	Quasi-split sound processor for all standards	2026
TDA3867T	Quasi-split sound processor with two FM demodulators	2038
TDA3868T	Quasi-split sound processor for all standards	2048
AM demodulator		
TDA9830	TV sound AM demodulator and audio source switch	4463
FM demodulator		
TBA120U	Sound IF amplifier/demodulator for TV	1433
TDA2555; TDA2557	Dual TV-sound demodulator circuits	1571
TDA3825	Single FM TV-sound demodulator circuit with external AF input	1897
TDA3826	Single FM TV-sound demodulator circuit	1907
TDA3827	TV sound demodulator circuit with SCART switches and AF control	1916
TDA9820	Multistandard/dual channel TV FM intercarrier sound demodulator	4450
Nicam demodulator		
TDA8732	NICAM-728 demodulator (NIDEM)	3798

		PAGE
SOUND		
Sound decoding - Stereo decoder/dual language		
TDA3803A	Stereo/dual TV-sound decoder circuit	1885
TDA3833	BTSC-stereo/SAP/DBX decoder and DBX expander	1925
TDA8415	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3212
TDA8416	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3269
TDA8417	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3287
TDA9840	TV and VTR stereo/dual sound processor with digital identification and I²C-bus	4473
TDA9845	TV and VTR stereo/dual sound processor with digital identification	4494
TDA9847	TV and VTR stereo/dual sound processor with digital identification	4508
TDA9854	I²C-bus controlled BTSC stereo/SAP decoder and audio processor	4526
TDA9855	I²C-bus controlled BTSC stereo/SAP decoder and audio processor	4565
TEA5582	Economy PLL stereo decoder (BTSC system)	4647
NICAM		
SAA7282	Terrestrial Digital Sound Decoder (TDSD2); I²C-bus	1196
SOUND		
Sound control		
TDA1029	Signal-sources switch	1461
TDA1524A	Stereo-tone/volume control circuit	1487
TDA1526	Stereo-tone/volume control circuit	1499
TDA3810	Spatial, stereo and pseudo-stereo sound circuit	1893
TDA8421	Hi-fi stereo audio processor; I²C-bus	3305
TDA8424	Hi-fi stereo audio processor; I²C-bus	3326
TDA8425	Hi-fi stereo audio processor; I²C-bus	3345
TDA8426	Hi-fi stereo audio processor; I²C-bus	3367
TDA9860	Universal hi-fi audio processor for TV	4607

		PAGE
Sound ADC		
PCF8591	8-bit A/D and D/A converter; I²C-bus	335
SAD1009	Universal DAC (UDAC)	1395
TDA1541A	Stereo high-performance 16-bit DAC	1509
TDA1543	Dual 16-bit DAC (economy version) I²S input format	1512
TDA1545A	Stereo continuous calibration DAC	1515
TDA1546T	Bitstream continuous calibration DAC with digital sound processing (BCC-DAC)	1519
Sound output		
TDA1013B	4 W audio power amplifier with DC volume control	1439
TDA1015	1 to 4 W audio power amplifier	1441
TDA1015T	0.5 W audio power amplifier	1443
TDA1514A	50 W high-performance hi-fi amplifier	1481
TDA1521; TDA1521Q	2 × 12 W hi-fi audio power amplifier	1483
TDA1521A	2 × 6 W hi-fi audio power amplifier	1485
TDA2611A	5 W audio power amplifier	1687
TDA2613	6 W hi-fi audio power amplifier	1689
TDA2614	6 W hi-fi audio power amplifier	1691
TDA2615	2 × 6 W hi-fi audio power amplifier	1694
TDA2616; TDA2616Q	2 × 12 W hi-fi audio power amplifiers with mute	1697
TDA7050	Low-voltage mono/stereo power amplifier	2897
TDA7050T	Low-voltage mono/stereo power amplifier	2899
TDA7052	1 W BTL mono audio amplifier	2901
TDA7052A; TDA7052AT	1 W BTL mono audio amplifier with DC volume control	2903
TDA7052B; TDA7052BT	Mono BTL audio amplifier with DC volume control	2905
TDA7053	2 × 1 W portable/mains-fed stereo power amplifier	2907
TDA7053A; TDA7053AT	Stereo BTL audio output amplifiers with DC volume control	2909
TDA7056	3 W mono BTL audio output amplifier	2912
TDA7056A	3 W mono BTL audio output amplifier with DC volume control	2914
TDA7056B	5 W mono BTL audio output amplifier with DC volume control	2916
TDA7057AQ	2 × 5 W BTL stereo audio output amplifier with DC volume control	2918
TDA7057Q	2 × 3 W BTL stereo audio output amplifier	2921
VISION		
Colour decoding		
SAA4981	Monolithic integrated 16 : 9 compressor	505
SAA7151B	Digital multistandard colour decoder with SCART interface (DMSD2-SCART); I²C-bus	987
SAA7157	Clock signal generator circuit for digital TV systems (SCGC)	1027

		PAGE
SAA7186	Digital video scaler; I²C-bus	1072
SAA7191B	Digital multistandard colour decoder, square pixel (DMSD-SQP); I²C-bus	1102
SAA7192	Digital colour space converter; I²C-bus	1134
SAA7197	Clock signal generator circuit for Desktop Video systems (SCGC)	1158
SAA7199B	Digital video encoder GENLOCK-capable; I²C-bus	1164
SAA9051	Digital multistandard TV decoder with separate chrominance and luminance inputs; I²C-bus	1242
SAA9056	S-VHS Digital SECAM Decoder (SDSD); I²C-bus	1286
SAA9057B	Clock signal generation circuit for digital TV systems (CGC)	1307
SAA9058	Sample rate converter	1314
TDA3504	Video control combination circuit	1724
TDA3505; TDA3506	Video control combination circuits with automatic cut-off control	1733
TDA3507	Video control combination circuit with automatic cut-off control	1743
TDA3508	Video control combination circuit with automatic cut-off control	1755
TDA3561A	PAL decoder	1765
TDA3565	PAL decoder	1777
TDA3566	PAL/NTSC decoder	1787
TDA3566A	PAL/NTSC decoder	1804
TDA3567	NTSC decoder	1823
TDA3592A	SECAM/PAL transcoder	1835
TDA4510	PAL decoder	2099
TDA4555; TDA4556	Multistandard decoders	2105
TDA4557	Multistandard decoder	2113
TDA4560	Colour transient improvement circuit	2121
TDA4565	Colour transient improvement circuit	2127
TDA4566	Colour transient improvement circuit	2135
TDA4568	Luminance signal delay circuit	2143
TDA4570	NTSC decoder	2151
TDA4580	Video control combination circuit with automatic cut-off control	2157
TDA4632	SECAM colour decoder with negative colour difference output signals	2173
TDA4650	Multistandard colour decoder with negative colour difference output signals	2182
TDA4651	Multistandard colour decoder with negative colour difference output signals	2191
TDA4655	Generic multistandard decoder	2201
TDA4657	Generic multistandard decoder	2212
TDA4661	Baseband delay line	2223
TDA4662	Baseband delay line	2229

		PAGE
TDA4663	Baseband delay line	2234
TDA4665	Baseband delay line	2240
TDA4670	Picture improvement circuit (PSI); I²C-bus	2246
TDA4671	Picture signal improvement (PSI) circuit; I²C-bus	2256
TDA4672	Picture signal improvement (PSI) circuit; I²C-bus with enhanced peaking function	2267
TDA4680	Video processor with automatic cut-off and white-level control; I²C-bus	2277
TDA4685	Video processor with automatic cut-off control; I²C-bus	2293
TDA4686	Video processor with automatic cut-off control; I²C-bus	2309
TDA4688	Video processor with automatic cut-off control; I²C-bus	2325
TDA4780	RGB video processor with automatic cut-off control and gamma adjustment; I²C-bus	2420
TDA8395	SECAM decoder	3206
TDA8440	Switch for CTV receivers; I²C-bus	3411
TDA8443A	I²C-bus controlled YUV/RGB switch	3428
TDA8446	Fast RGB/YC switch for digital decoding	3450
TDA8451A	P²CCD delay line and matrix	3459
TDA8452A	P²CCD filter combination for colour decoders	3469
TDA8453A	P²CCD filter combination for CVBS and S-VHS	3483
TDA8480T	RGB gamma-correction processor; I²C-bus	3495
TDA8490	SECAM decoder	3507
TDA8540	4 × 4 video matrix switch; I²C-bus	3566
TDA8601	RGB/YUV and fast blanking switch	3577
TDA9141	PAL/NTSC/SECAM decoder/sync processor; I²C-bus	4042
TDA9160	PAL/NTSC/SECAM decoder/sync processor; I²C-bus	4124
TDA9170	YUV picture improvement processor based on histogram modification; I²C-bus	4148
TEA7650H	Video signal processor for CD-video/laser vision	4655
Video and high-speed ADC and DAC		
SAA7165	Video enhancement and D/A processor (VEDA2); I²C-bus	1046
SAA7169	35 MHz triple 9-bit D/A converter for high-speed video	1065
SAA9065	Video enhancement and D/A processor (VEDA); I²C-bus	1319
SAA9079	7-bit analog-to-digital converter (ADC 7)	1337
TDA8702	8-bit video digital-to-analog converter	3589
TDA8703	8-bit high-speed analog-to-digital converter	3603
TDA8705	6-bit high-speed dual analog-to-digital converter	3616
TDA8705A	6-bit high-speed dual analog-to-digital converter	3626
TDA8706	6-bit analog-to-digital converter with multiplexer and clamp	3636

		PAGE
TDA8707	Triple RGB 6-bit video analog-to-digital interface	3646
TDA8708A	Video analog input interface	3658
TDA8708B	Video analog input interface	3675
TDA8709A	Video analog input interface	3692
TDA8712; TDF8712	8-bit digital-to-analog converters	3711
TDA8714	8-bit high-speed analog-to-digital converter	3726
TDA8716	8-bit high-speed analog-to-digital converter	3741
TDA8718	8-bit high-speed analog-to-digital converter	3757
TDA8753A	YUV 8-bit analog-to-digital interface	3893
TDA8755	YUV 8-bit video low-power analog-to-digital interface	3908
TDA8758	YC 8-bit low-power analog-to-digital video interface	3923
TDA8760	10-bit high-speed analog-to-digital converter	3939
TDA8761	9-bit analog-to-digital converter for digital video	3960
TDA8762	10-bit high-speed low-power analog-to-digital converter	3974
TDA8766	10-bit high-speed 3 V analog-to-digital converter	3989
TDA8771	Triple 8-bit video digital-to-analog converter	4003
TDA8772; TDA8772A	Triple 8-bit video digital-to-analog converter	4015
TDA8776	10-bit, 500 MSPS digital-to-analog converter	4029
TDF8704	8-bit high-speed analog-to-digital converter	4620
Memory based features		
SAB9075H	Picture-in-Picture (PIP) controller for NTSC; I^2C-bus	1359
Scan conversion		
PCF8570	256 × 8-bit static low-voltage RAM with I^2C-bus interface	308
SAA4940H	NOise reduction IC	490
SAA7158	Back END IC	1033
Video output		
TDA6101BQ	Video output amplifier	2854
TDA6101Q	Video output amplifier	2862
TDA6103Q	Triple video output amplifier	2872
TDA6111Q	Video output amplifier	2882
High voltage transistors		
BF420; BF422	Silicon epitaxial transistors	121
BF421; BF423	Silicon epitaxial transistors	122
BF457 to BF459	Silicon planar transistors for video output stages	123
BF469; BF471	Silicon planar epitaxial transistors	124
BF470; BF472	Silicon planar epitaxial transistors	125
BF483; BF485; BF487	Silicon planar epitaxial transistors	126
BF484; BF486; BF488	Silicon planar epitaxial transistors	127

		PAGE
BF583; BF585; BF587	Silicon planar epitaxial transistors	129
BF584; BF586; BF588	Silicon planar epitaxial transistors	130
BF720; BF722	Silicon epitaxial transistors	131
BF721; BF723	Silicon epitaxial transistors	132
BF857 to BF859	Silicon planar transistors for video output stages	134
BF869; BF871	Silicon planar video output transistors	135
BF870; BF872	Silicon planar video output transistors	136
SYNC/DEFLECTION/SMPS		
Sync and deflection		
BY228	Parallel efficiency diode	155
BY328	32 kHz parallel efficiency diode	157
BY8000 series	High-voltage fast soft-recovery controlled avalanche rectifier diodes	161
BY8100 series	High-voltage very fast soft-recovery controlled avalanche rectifier diodes	162
BY8400 series	High-voltage fast soft-recovery rectifier diodes	163
BYD33 series	Fast soft-recovery controlled avalanche rectifier diodes	164
BYW54 to 56	Controlled avalanche rectifier diodes	166
TDA1082	East-west correction driver circuit	1475
TDA2578A	Synchronization circuit with vertical oscillator and driver stages	1621
TDA2579B	Horizontal/vertical synchronization circuit	1635
TDA2579C	Synchronization circuit with synchronized vertical divider system for 60 Hz	1651
TDA2593	Horizontal combination	1669
TDA2595	Horizontal combination	1677
TDA2653A	Vertical deflection circuit	1701
TDA2654	Vertical deflection circuit	1709
TDA2658	Vertical deflection circuit	1717
TDA3653B; TDA3653C	Vertical deflection and guard circuit (90°)	1849
TDA3654; TDA3654Q	Vertical deflection and guard circuit (110°)	1859
TDA4691	Sync Processor with Clock (SPC)	2341
TDA4800	Vertical deflection circuit for monitor applications	2451
TDA4820T	Sync separation circuit for video applications	2473
TDA8350Q	DC-coupled vertical deflection and East-West output circuit	3085
TDA8351	DC-coupled vertical deflection circuit	3094
TDA8351A	DC-coupled vertical deflection circuit	3103
TDA8356	DC-coupled vertical deflection circuit	3112

		PAGE
TDA8433	Deflection processor for computer controlled TV receivers; I²C-bus	3389
TDA9150B	Programmable deflection controller; I²C-bus	4065
TDA9151B	Programmable deflection controller; I²C-bus	4094
Power supply		
BYV95A to C	Avalanche fast soft-recovery rectifier diodes	165
TDA1023; TDA1023T	Proportional-control triac triggering circuit	1445
TDA8380A	Control circuit for Switched Mode Power Supplies (SMPS)	3189
TEA1039	Control circuit for Switched Mode Power Supplies (SMPS)	4635
Combi		
TDA4504B	Small signal combination for multistandard colour TV	2075
TDA8302	Small signal combination IC for colour TV	2973
TDA8303; TDA8303A	Small signal combination IC for black/white TV	2992
TDA8304	Small signal combination IC for colour TV	3010
TDA8310	PAL/NTSC colour processor for Picture-in-Picture (PIP) applications	3030
TDA8315T	Integrated NTSC decoder and sync processor	3049
TDA8360; TDA8361; TDA8362	Integrated PAL and PAL/NTSC TV processors	3120
TDA8366	I²C-bus controlled PAL/NTSC TV processor	3149
CONTROL		
Clock/calendar		
PCF8573	Clock/calendar with serial I/O; I²C-bus	311
PCF8583	Clock Calendar with 256 × 8-bit Static RAM (SRAM); I²C-bus	329
PCF8593	Low power clock calendar; I²C-bus	338
Display drivers		
PCF1303T	18-element bar graph LCD driver	271
PCF2116 family	LCD controller/drivers; I²C-bus	276
PCF2114X; PCF2116X		
PCF8566	Universal LCD driver for low multiplex rates; I²C-bus	297
PCF8568	LCD row driver for dot matrix displays; I²C-bus	300
PCF8569	LCD column driver for dot matrix graphic displays; I²C-bus	303
PCF8576C	Universal LCD driver for low multiplex rates; I²C-bus	316
PCF8577C	LCD direct/duplex driver with I²C-bus interface	321
PCF8578	LCD row/column driver for dot matrix graphic displays; I²C-bus	323
PCF8579	LCD column driver for dot matrix graphic displays; I²C-bus	326

Selection guide — Functional index

		PAGE
LED driver		
SAA1064	4-digit LED driver with I²C-bus interface	373
On Screen Display (OSD)		
PCA84C646; PCA84C846	Microcontrollers for TV tuning control and OSD application; I²C-bus	250
PCA8515	Stand-alone OSD; I²C-bus	255
PCA8516	Stand-alone OSD; I²C-bus	259
PCE84C886	Microcontroller for monitor OSD and auto-sync applications; I²C-bus	266
SAA5252	Line twenty-one acquisition and display (LITOD); I²C-bus	814
Memories - SRAM		
PCF29F64	8 K × 8-bit static CMOS EEPROM with PAGE-ERASE option	273
PCF8570	256 × 8-bit static low-voltage RAM with I²C-bus interface	308
EEPROM		
PCA8581; PCA8581C	128 × 8-bit EEPROM with I²C-bus interface	263
PCX8582X-2 Family	256 × 8-bit CMOS EEPROMS with I²C-bus interface	360
PCX8594X-2 Family	512 × 8-bit CMOS EEPROMS with I²C-bus interface	364
PCX8598X-2 Family	1024 × 8-bit CMOS EEPROMS with I²C-bus interface	368
MICROCONTROLLERS		
80C528; 83C528	CMOS single-chip 8-bit microcontroller; I²C-bus	44
80C652; 83C652	CMOS single-chip 8-bit microcontroller; I²C-bus	50
83C654	CMOS single-chip 8-bit microcontroller; I²C-bus	56
83CE654	CMOS single-chip 8-bit microcontroller with Electromagnetic Compatibility improvements; I²C-bus	62
84C44X/84C64X/84C84X	8-bit microcontrollers with OSD and VST; I²C-bus	65
87C528	CMOS single-chip 8-bit microcontroller; I²C-bus	71
87C652	CMOS single-chip 8-bit microcontroller; I²C-bus	77
87C654	CMOS single-chip 8-bit microcontroller; I²C-bus	83
P8XCE528	8-bit microcontroller with EMC; I²C-bus	225
P83CL168; P83CL167; P83CL268; P83CL267	Microcontroller for TV OSD, VST and control functions; I²C-bus	233
P90CE201	16-bit microcontroller; I²C-bus	240
PCA84C646; PCA84C846	Microcontrollers for TV tuning control and OSD application; I²C-bus	250
PCA8515	Stand-alone OSD; I²C-bus	255
PCA8516	Stand-alone OSD; I²C-bus	259
PCE84C886	Microcontroller for monitor OSD and auto-sync applications; I²C-bus	266

		PAGE
PCF84C12A; PCF84C22A; PCF84C42A	8-bit microcontroller	281
PCF84C21A; PCF84C41A; PCF84C81A	Telecom microcontroller	284
PCF84CXXXA Family	8-bit microcontrollers; I²C-bus	287
PCF84C85A	Microcontroller with extended I/O; I²C-bus	290
PCF84C430	Single chip 8-bit microcontroller with LCD driver; I²C-bus	293
Remote I/O expanders		
PCF8574	Remote 8-bit I/O expander for I²C-bus	313
PCF8584	I²C-bus controller	331
TDA8722	I²C-bus programmable modulator for negative video modulation and FM sound	3766
Remote control transmitter		
PCA84C122; 222;422; 622; 822	8-bit microcontrollers for remote control transmitters	245
SAA3004	Remote control transmitter	423
SAA3008	Infrared remote control transmitter (RECS 80 low voltage)	433
SAA3009; SAA3049	Infrared remote control decoders	447
SAA3010	Infrared remote control transmitter RC-5	457
TELETEXT		
SAA5191	Teletext video processor	517
SAA5231	Teletext video processor	523
SAA5232	Dual standard VPT decoder and clock calendar; I²C-bus	534
SAA5233	Dual standard PDC decoder; I²C-bus	536
SAA5243 series	Enhanced computer controlled teletext circuits (ECCT); I²C-bus	551
SAA5244A	Integrated VIP and teletext decoder (IVT1.1); I²C-bus	585
SAA5245	Enhanced computer controlled teletext circuit (USECCT); I²C-bus	613
SAA5246A	Integrated VIP and Teletext (IVT1.0); I²C-bus	635
SAA5247	Integrated VIP and Teletext with Background Memory Controller (IVT1.1BMC); I²C-bus	680
SAA5248	Single-chip Teletext and VPS decoder (IVT1.0VPS); I²C-bus	713
SAA5249	Integrated VIP and Teletext with Background Memory Controller (IVT1.1BMCX); I²C-bus	747
SAA5250	Interface for data acquisition and control (for multistandard teletext systems)	783
SAA5252	Line twenty-one acquisition and display (LITOD); I²C-bus	814
SAA5254	Integrated VIP and teletext decoder (IVT1.1X); I²C-bus	828
SAA5260	Integrated VIP and teletext decoder (IVT2.0); I²C-bus	859

		PAGE
SAA5280	Single-chip teletext/VPS and line 23 decoder including 4/8 page memory; I²C-bus	891
SAA5281	Integrated Video input processor and Teletext decoder (IVT1.8*); I²C-bus	896
SAA5290	One-page Economy Teletext/TV microcontroller; I²C-bus	928
SAA5355	Single-chip colour CRT controller (FTFROM)	959
SAA9042	Multistandard Teletext IC for standard and features TV; I²C-bus	1216
SATELLITE TV		
BB811	UHF variable capacitance diode	111
BB901	Variable capacitance diode	112
SAA1760	D2MAC video decompression and descrambling; I²C-bus	409
SAA1770	D2MAC digital MAC packet; I²C-bus	416
SAB8726	Sensitive 2.6 GHz divide-by-2 prescaler	1353
TDA8011T	IF amplifier for satellite TV receivers	2939
TDA8012M	Low power PLL FM demodulator for satellite TV receivers	2945
TDA8040T	Quadrature demodulator	2953
TDA8041H	Quadrature demodulator controller	2963
TDA8730	PLL FM demodulator for DBS signals	3792
TDA8735	PLL frequency synthesizer; I²C-bus	3808
TDA8740; TDA8740H	Satellite sound circuit with noise reduction	3811
TDA8741; TDA 8741H	Satellite sound circuit with noise reduction	3828
TDA8742; TDA8742H	Satellite sound circuit with noise reduction	3844
TDA8745	Satellite sound receiver with I²C-bus control	3860
TDA9821	Dual channel TV FM intercarrier sound demodulator	4457
TSA5055T	2.5 GHz bidirectional I²C-bus controlled synthesizer	4674
PAY TV		
TDA8000	Smart card interface	2924
TDA8001	Smart card interface	2927
TDA8005	Low power smart card coupler	2932
Miscellaneous		
NE592	Video amplifier	167
NE/SA5204A	Wide-band high-frequency amplifier	176
NE/SA/SE5205A	Wide-band high-frequency amplifier	187
NE/SA5209	Wide-band variable gain amplifier	197
NE/SE5539	High frequency operational amplifier	211
NE5592	Video amplifier	219

		PAGE
TDA6800; TDA6800T	Video modulator circuit	2893
TDA8442	I^2C-bus interface for colour decoders	3421
TDA8444	Octuple 6-bit DAC with I^2C-bus	3443
TDA8501	PAL/NTSC encoder	3516
TDA8505	SECAM encoder	3541
µA733; 733C	Differential video amplifier	4782
VCR/Camera/Recorder		
SAA1101	Universal sync generator (USG)	385
SAA1310	Control interface for VHS video recorders	400
SAA4700	VPS data line processor; I^2C-bus	472
SAA4700T	VPS data line processor; I^2C-bus	481
SAD1009	Universal DAC (UDAC)	1395
SAD1019	Multi-norm pulse pattern generator	1407
SAF1135	Data line decoder; I^2C-bus	1421
TDA3755	PAL/NTSC/SECAM synchronization processor for video recorders	1869
TDA3791	Band selector and window detector	1879
TDA4301	Vertical driver	2061
TDA4301T	Vertical driver	2065
TDA4306	Master gain circuit	2069
TDA4710H	VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder	2362
TDA4720	SECAM identification and chrominance correction circuit	2397
TDA4722; TDA4724	SECAM-L chrominance processors for VHS video recorders	2402
TDA4725T	SECAM-L chrominance processor for VHS video recorders	2411
TDA5140A	Brushless DC motor drive circuit	2631
TDA5141	Brushless DC motor drive circuit	2635
TDA5142T	Brushless DC motor drive circuit	2639
TDA5143T	Brushless DC motor drive circuit	2643
TDA5144T; TDA5144AT	Brushless DC motor drive circuit	2647
TDA5145	Brushless DC motor drive circuit	2651
TDA6800; TDA6800T	Video modulator circuit	2893
TDA9610H	Audio FM processor for VHS hi-fi audio; I^2C-bus	4168
TDA9614H	Audio processor for VHS hi-fi and linear audio; I^2C-bus	4205
TDA9715H; TDA9715A	Y/C one-chip processor (VHS standard)	4260
TEA7650H	Video signal processor for CD-video/laser vision	4655

		PAGE
MONITOR CIRCUITS		
Sync		
TDA2593	Horizontal combination	1669
TDA2595	Horizontal combination	1677
TDA4810	Sync processor and horizontal driver for monitors	2459
TDA4820T	Sync separation circuit for video applications	2473
TDA4850	Horizontal and vertical deflection controller for VGA/XGA and multi-frequency monitors	2478
TDA4851	Horizontal and vertical deflection controller for VGA/XGA and autosync monitors	2490
TDA4852	Horizontal and vertical deflection controller for autosync monitors	2503
Deflection		
TDA2653A	Vertical deflection circuit	1701
TDA2654	Vertical deflection circuit	1709
TDA2658	Vertical deflection circuit	1717
TDA4800	Vertical deflection circuit for monitor applications	2451
TDA4860	Vertical deflection power amplifier for monitors	2516
TDA4861	Vertical deflection power amplifier for monitors	2524
TDA4865	Full-bridge current driven vertical deflection booster	2532
TDA4866	Full-bridge current driven vertical deflection booster	2542
SMPS		
TDA8380A	Control circuit for Switched Mode Power Supplies (SMPS)	3189
TEA1039	Control circuit for Switched Mode Power Supplies (SMPS)	4635
Video control		
TDA3507	Video control combination circuit with automatic cut-off control	1743
TDA3508	Video control combination circuit with automatic cut-off control	1755
TDA4880	Advanced monitor video controller	2552
TDA4881	Advanced monitor video controller	2558
TDA4882	Advanced monitor video controller for OSD	2566
TDA4883	Three-gain video preamplifier	2590
TDA4884	Three-gain control video preamplifier for OSD	2598
Miscellaneous		
TDA8442	I^2C-bus interface for colour decoders	3421
TDA8444	Octuple 6-bit DAC with I^2C-bus	3443

ALPHANUMERICAL INDEX		PAGE
80C528; 83C528	CMOS single-chip 8-bit microcontroller; I²C-bus	44
80C652; 83C652	CMOS single-chip 8-bit microcontroller; I²C-bus	50
83C654	CMOS single-chip 8-bit microcontroller; I²C-bus	56
83CE654	CMOS single-chip 8-bit microcontroller with Electromagnetic Compatibility improvements; I²C-bus	62
84C44X; 84C64X; 84C84X	8-bit microcontrollers with OSD and VST; I²C-bus	65
87C528	CMOS single-chip 8-bit microcontroller; I²C-bus	71
87C652	CMOS single-chip 8-bit microcontroller; I²C-bus	77
87C654	CMOS single-chip 8-bit microcontroller; I²C-bus	83
BA481	UHF mixer diode	89
BA482; BA483; BA484	Silicon planar diodes	90
BA582	Silicon planar diode	91
BA682; BA683	Band-switching diodes for surface mounting	92
BAT17	Schottky barrier diode	93
BAT18	Silicon planar diode	94
BB119	Silicon variable capacitance diode	95
BB131	VHF variable capacitance diode	96
BB132	VHF variable capacitance diode	97
BB133	VHF variable capacitance diode	98
BB134	UHF variable capacitance diode	99
BB135	UHF variable capacitance diode	100
BB148	VHF variable capacitance diode	101
BB149	UHF variable capacitance diode	102
BB150	VHF variable capacitance diode	103
BB215	UHF variable capacitance diode	104
BB405B	UHF variable capacitance diode	105
BB417	Variable capacitance diode	106
BB515	UHF variable capacitance diode	107
BB619	VHF variable capacitance diode	108
BB620	VHF variable capacitance diode	109
BB809	Silicon planar variable capacitance diode	110
BB811	UHF variable capacitance diode	111
BB901	Variable capacitance diode	112
BB909A; BB909B	Silicon planar variable capacitance diode	113
BB910	VHF variable capacitance diode	114
BB911A	VHF variable capacitance diode	115
BBY31	Variable capacitance diode	116
BBY39	Double variable capacitance diode	117
BBY40	Variable capacitance diode	118

		PAGE
BBY42	VHF variable capacitance diode	119
BBY62	Double variable capacitance diode	120
BF420; BF422	Silicon epitaxial transistors	121
BF421; BF423	Silicon epitaxial transistors	122
BF457 to BF459	Silicon planar transistors for video output stages	123
BF469; BF471	Silicon planar epitaxial transistors	124
BF470; BF472	Silicon planar epitaxial transistors	125
BF483; BF485; BF487	Silicon planar epitaxial transistors	126
BF484; BF486; BF488	Silicon planar epitaxial transistors	127
BF547	NPN 1 GHz wideband transistor	128
BF583; BF585; BF587	Silicon planar epitaxial transistors	129
BF584; BF586; BF588	Silicon planar epitaxial transistors	130
BF720; BF722	Silicon epitaxial transistors	131
BF721; BF723	Silicon epitaxial transistors	132
BF747	NPN 1 GHz wideband transistor	133
BF857 to BF859	Silicon planar transistors for video output stages	134
BF869; BF871	Silicon planar video output transistors	135
BF870; BF872	Silicon planar video output transistors	136
BF904; BF904R	Dual-gate MOS-FET	137
BF960	Silicon N-channel dual-gate MOS-FET	138
BF964S	Silicon N-channel dual-gate MOS-FET	139
BF966S	Silicon N-channel dual-gate MOS-FET	140
BF980A	Silicon N-channel dual-gate MOS-FET	141
BF981	Silicon N-channel dual-gate MOS-FET	142
BF982	Silicon N-channel dual-gate MOS-FET	143
BF988	Silicon N-channel dual-gate MOS-FET	144
BF989	Silicon N-channel dual-gate MOS-FET	145
BF990A	Silicon N-channel dual-gate MOS-FET	146
BF991	Silicon N-channel dual-gate MOS-FET	147
BF992	Silicon N-channel dual-gate MOS-FET	148
BF994S	Silicon N-channel dual-gate MOS-FET	149
BF996S	Silicon N-channel dual-gate MOS-FET	150
BF997	Silicon N-channel dual-gate MOS-FET	151
BF998	Silicon N-channel dual-gate MOS-FET	152
BFS17	NPN 1 GHz wideband transistor	153
BFS17A	NPN 3 GHz wideband transistor	154
BY228	Parallel efficiency diode	155
BY229 series	Rectifier diodes fast, soft-recovery	156
BY328	32 kHz parallel efficiency diode	157

		PAGE
BY329 series	Rectifier diodes fast, soft-recovery	158
BY359F-1500	Rectifier diode fast, high-voltage	159
BY359X-1500	Rectifier diode fast, high-voltage	160
BY8000 series	High-voltage fast soft-recovery controlled avalanche rectifier diodes	161
BY8100 series	High-voltage very fast soft-recovery controlled avalanche rectifier diodes	162
BY8400 series	High-voltage fast soft-recovery rectifier diodes	163
BYD33 series	Fast soft-recovery controlled avalanche rectifier diodes	164
BYV95A to C	Avalanche fast soft-recovery rectifier diodes	165
BYW54 to 56	Controlled avalanche rectifier diodes	166
NE592	Video amplifier	167
NE/SA5204A	Wide-band high-frequency amplifier	176
NE/SA/SE5205A	Wide-band high-frequency amplifier	187
NE/SA5209	Wide-band variable gain amplifier	197
NE/SE5539	High frequency operational amplifier	211
NE5592	Video amplifier	219
P8XCE528	8-bit microcontroller with EMC; I²C-bus	225
P83CL168; P83CL167; P83CL268; P83CL267	Microcontrollers for TV OSD, VST and control functions; I²C-bus	233
P90CE201	16-bit microcontroller; I²C-bus	240
PCA84C122; 222; 422; 622; 822	8-bit microcontrollers for remote control transmitters	245
PCA84C646; PCA84C846	Microcontrollers for TV tuning control and OSD application; I²C-bus	250
PCA8515	Stand-alone OSD; I²C-bus	255
PCA8516	Stand-alone OSD; I²C-bus	259
PCA8581; PCA8581C	128 × 8-bit EEPROM with I²C-bus interface	263
PCE84C886	Microcontroller for monitor OSD and auto-sync applications; I²C-bus	266
PCF1303T	18-element bar graph LCD driver	271
PCF29F64	8 K × 8-bit static CMOS EEPROM with PAGE-ERASE option	273
PCF2116 family PCF2114X; PCF2116X	LCD controller/drivers; I²C-bus	276
PCF84C12A; PCF84C22A; PCF84C42A	8-bit microcontroller	281
PCF84C21A; PCF84C41A; PCF84C81A	Telecom microcontroller	284
PCF84CXXXA Family	8-bit microcontrollers; I²C-bus	287
PCF84C85A	Microcontroller with extended I/O; I²C-bus	290
PCF84C430	Single chip 8-bit microcontroller with LCD driver; I²C-bus	293
PCF8566	Universal LCD driver for low multiplex rates; I²C-bus	297

		PAGE
PCF8568	LCD row driver for dot matrix displays; I²C-bus	300
PCF8569	LCD column driver for dot matrix graphic displays; I²C-bus	303
PCF8570	256 × 8-bit static low-voltage RAM with I²C-bus interface	308
PCF8573	Clock/calendar with serial I/O; I²C-bus	311
PCF8574	Remote 8-bit I/O expander for I²C-bus	313
PCF8576C	Universal LCD driver for low multiplex rates; I²C-bus	316
PCF8577C	LCD direct/duplex driver with I²C-bus interface	321
PCF8578	LCD row/column driver for dot matrix graphic displays; I²C-bus	323
PCF8579	LCD column driver for dot matrix graphic displays; I²C-bus	326
PCF8583	Clock Calendar with 256 × 8-bit Static RAM (SRAM); I²C-bus	329
PCF8584	I²C-bus controller	331
PCF8591	8-bit A/D and D/A converter; I²C-bus	335
PCF8593	Low power clock calendar	338
PCX8582X-2 Family	256 × 8-bit CMOS EEPROMS with I²C-bus interface	360
PCX8594X-2 Family	512 × 8-bit CMOS EEPROMS with I²C-bus interface	364
PCX8598X-2 Family	1024 × 8-bit CMOS EEPROMS with I²C-bus interface	368
SAA1064	4-digit LED-driver with I²C-bus interface	373
SAA1101	Universal sync generator (USG)	385
SAA1300	Tuner switching circuit; I²C-bus	397
SAA1310	Control interface for VHS video recorders	400
SAA1760	D2MAC video decompression and descrambling; I²C-bus	409
SAA1770	D2MAC digital MAC packet; I²C-bus	416
SAA3004	Remote control transmitter	423
SAA3008	Infrared remote control transmitter (RECS 80 low voltage)	433
SAA3009; SAA3049	Infrared remote control decoders	447
SAA3010	Infrared remote control transmitter RC-5	457
SAA4700	VPS data line processor; I²C-bus	472
SAA4700T	VPS data line processor; I²C-bus	481
SAA4940H	NOise reduction IC	490
SAA4981	Monolithic integrated 16 : 9 compressor	505
SAA5191	Teletext video processor	517
SAA5231	Teletext video processor	523
SAA5232	Dual standard VPT decoder and clock calendar; I²C-bus	534
SAA5233	Dual standard PDC decoder; I²C-bus	536
SAA5243 series	Enhanced computer controlled teletext circuits (ECCT); I²C-bus	551
SAA5244A	Integrated VIP and teletext decoder (IVT1.1); I²C-bus	585
SAA5245	Enhanced computer controlled teletext circuit (USECCT); I²C-bus	613
SAA5246A	Integrated VIP and Teletext (IVT1.0); I²C-bus	635

		PAGE
SAA5247	Integrated VIP and Teletext with Background Memory Controller (IVT1.1BMC); I²C-bus	680
SAA5248	Single-chip Teletext and VPS decoder (IVT1.0VPS); I²C-bus	713
SAA5249	Integrated VIP and Teletext with Background Memory Controller (IVT1.1BMCX); I²C-bus	747
SAA5250	Interface for data acquisition and control (for multistandard teletext systems)	783
SAA5252	Line twenty-one acquisition and display (LITOD); I²C-bus	814
SAA5254	Integrated VIP and teletext decoder (IVT1.1X); I²C-bus	828
SAA5260	Integrated VIP and teletext decoder (IVT2.0); I²C-bus	859
SAA5280	Single-chip teletext/VPS and line 23 decoder including 4/8 page memory; I²C-bus	891
SAA5281	Integrated Video input processor and Teletext decoder (IVT1.8*); I²C-bus	896
SAA5290	One-page Economy Teletext/TV microcontroller; I²C-bus	928
SAA5355	Single-chip colour CRT controller (FTFROM)	959
SAA7151B	Digital multistandard colour decoder with SCART interface (DMSD2-SCART); I²C-bus	987
SAA7157	Clock signal generator circuit for digital TV systems (SCGC)	1027
SAA7158	Back END IC	1033
SAA7165	Video enhancement and D/A processor (VEDA2); I²C-bus	1046
SAA7169	35 MHz triple 9-bit D/A converter for high-speed video	1065
SAA7186	Digital video scaler; I²C-bus	1072
SAA7191B	Digital multistandard colour decoder, square pixel (DMSD-SQP); I²C-bus	1102
SAA7192	Digital colour space converter; I²C-bus	1134
SAA7197	Clock signal generator circuit for Desktop Video systems (SCGC)	1158
SAA7199B	Digital video encoder GENLOCK-capable; I²C-bus	1164
SAA7282	Terrestrial Digital Sound Decoder (TDSD2); I²C-bus	1196
SAA9042	Multistandard Teletext IC for standard and features TV; I²C-bus	1216
SAA9051	Digital multistandard TV decoder with separate chrominance and luminance inputs; I²C-bus	1242
SAA9056	S-VHS Digital SECAM Decoder (SDSD); I²C-bus	1286
SAA9057B	Clock signal generation circuit for digital TV systems (CGC)	1307
SAA9058	Sample rate converter	1314
SAA9065	Video enhancement and D/A processor (VEDA); I²C-bus	1319
SAA9079	7-bit analog-to-digital converter (ADC 7)	1337
SAB6456; SAB6456T	Sensitive 1 GHz divide-by-64/divide-by-256 switchable prescaler	1347
SAB8726	Sensitive 2.6 GHz divide-by-2 prescaler	1353
SAB9075H	Picture-in-Picture (PIP) controller for NTSC; I²C-bus	1359
SAD1009	Universal DAC (UDAC)	1395

		PAGE
SAD1019	Multi-norm pulse pattern generator	1407
SAF1135	Data line decoder; I²C-bus	1421
TBA120U	Sound IF amplifier/demodulator for TV	1433
TDA1013B	4 W audio power amplifier with DC volume control	1439
TDA1015	1 to 4 W audio power amplifier	1441
TDA1015T	0.5 W audio power amplifier	1443
TDA1023; TDA1023T	Proportional-control triac triggering circuit	1445
TDA1029	Signal-sources switch	1461
TDA1082	East-west correction driver circuit	1475
TDA1514A	50 W high-performance hi-fi amplifier	1481
TDA1521; TDA1521Q	2 × 12 W hi-fi audio power amplifier	1483
TDA1521A	2 × 6 W hi-fi audio power amplifier	1485
TDA1524A	Stereo-tone/volume control circuit	1487
TDA1526	Stereo-tone/volume control circuit	1499
TDA1541A	Stereo high-performance 16-bit DAC	1509
TDA1543	Dual 16-bit DAC (economy version) I²S input format	1512
TDA1545A	Stereo continuous calibration DAC	1515
TDA1546T	Bitstream continuous calibration DAC with digital sound processing (BCC-DAC)	1519
TDA2545A	Quasi-split-sound circuit	1553
TDA2546A	Quasi-split-sound circuit with 5.5 MHz demodulation	1559
TDA2549	IF amplifier and demodulator for multistandard TV receivers	1565
TDA2555; TDA2557	Dual TV-sound demodulator circuits	1571
TDA2578A	Synchronization circuit with vertical oscillator and driver stages	1621
TDA2579B	Horizontal/vertical synchronization circuit	1635
TDA2579C	Synchronization circuit with synchronized vertical divider system for 60 Hz	1651
TDA2593	Horizontal combination	1669
TDA2595	Horizontal combination	1677
TDA2611A	5 W audio power amplifier	1687
TDA2613	6 W hi-fi audio power amplifier	1689
TDA2614	6 W hi-fi audio power amplifier	1691
TDA2615	2 × 6 W hi-fi audio power amplifier	1694
TDA2616; TDA2616Q	2 × 12 W hi-fi audio power amplifiers with mute	1697
TDA2653A	Vertical deflection circuit	1701
TDA2654	Vertical deflection circuit	1709
TDA2658	Vertical deflection circuit	1717
TDA3504	Video control combination circuit	1724
TDA3505; TDA3506	Video control combination circuits with automatic cut-off control	1733

		PAGE
TDA3507	Video control combination circuit with automatic cut-off control	1743
TDA3508	Video control combination circuit with automatic cut-off control	1755
TDA3561A	PAL decoder	1765
TDA3565	PAL decoder	1777
TDA3566	PAL/NTSC decoder	1787
TDA3566A	PAL/NTSC decoder	1804
TDA3567	NTSC decoder	1823
TDA3592A	SECAM/PAL transcoder	1835
TDA3653B; TDA3653C	Vertical deflection and guard circuit (90°)	1849
TDA3654; TDA3654Q	Vertical deflection and guard circuit (110°)	1859
TDA3755	PAL/NTSC/SECAM synchronization processor for video recorders	1869
TDA3791	Band selector and window detector	1879
TDA3803A	Stereo/dual TV-sound decoder circuit	1885
TDA3810	Spatial, stereo and pseudo-stereo sound circuit	1893
TDA3825	Single FM TV-sound demodulator circuit with external AF input	1897
TDA3826	Single FM TV-sound demodulator circuit	1907
TDA3827	TV sound demodulator circuit with SCART switches and AF control	1916
TDA3833	BTSC-stereo/SAP/DBX decoder and DBX expander	1925
TDA3840	TV IF amplifier and demodulator with TV signal identification	1932
TDA3842	Multistandard TV IF amplifier and demodulator with TV signal identification	1944
TDA3845; TDA3845T	Quasi-split sound circuit and AM demodulator	1963
TDA3853T	TV IF amplifier and demodulator with TV signal identification	1976
TDA3856	Quasi-split sound processor for all standards	1990
TDA3857	Quasi-split sound processor with two FM demodulators	2002
TDA3858	Quasi-split sound processor for all standards	2013
TDA3866	Quasi-split sound processor for all standards	2026
TDA3867T	Quasi-split sound processor with two FM demodulators	2038
TDA3868T	Quasi-split sound processor for all standards	2048
TDA4301	Vertical driver	2061
TDA4301T	Vertical driver	2065
TDA4306	Master gain circuit	2069
TDA4504B	Small signal combination multistandard colour TV	2075
TDA4510	PAL decoder	2099
TDA4555; TDA4556	Multistandard decoders	2105
TDA4557	Multistandard decoder	2113
TDA4560	Colour transient improvement circuit	2121
TDA4565	Colour transient improvement circuit	2127
TDA4566	Colour transient improvement circuit	2135

		PAGE
TDA4568	Luminance signal delay circuit	2143
TDA4570	NTSC decoder	2151
TDA4580	Video control combination circuit with automatic cut-off control	2157
TDA4632	SECAM colour decoder with negative colour difference output signals	2173
TDA4650	Multistandard colour decoder with negative colour difference output signals	2182
TDA4651	Multistandard colour decoder with negative colour difference output signals	2191
TDA4655	Generic multistandard decoder	2201
TDA4657	Generic multistandard decoder	2212
TDA4661	Baseband delay line	2223
TDA4662	Baseband delay line	2229
TDA4663	Baseband delay line	2234
TDA4665	Baseband delay line	2240
TDA4670	Picture improvement circuit (PSI); I²C-bus	2246
TDA4671	Picture signal improvement (PSI) circuit; I²C-bus	2256
TDA4672	Picture signal improvement (PSI) circuit; I²C-bus with enhanced peaking function	2267
TDA4680	Video processor with automatic cut-off and white-level control; I²C-bus	2277
TDA4685	Video processor with automatic cut-off control; I²C-bus	2293
TDA4686	Video processor with automatic cut-off control; I²C-bus	2309
TDA4688	Video processor with automatic cut-off control; I²C-bus	2325
TDA4691	Sync Processor with Clock (SPC)	2341
TDA4710H	VHS PAL, SECAM BG or chrominance and synchronization circuit for an (S) VHS video cassette recorder	2362
TDA4720	SECAM identification and chrominance correction circuit	2397
TDA4722; TDA4724	SECAM-L chrominance processors for VHS video recorders	2402
TDA4725T	SECAM-L chrominance processor for VHS video recorders	2411
TDA4780	RGB video processor with automatic cut-off control and gamma adjustment; I²C-bus	2420
TDA4800	Vertical deflection circuit for monitor applications	2451
TDA4810	Sync processor and horizontal driver for monitors	2459
TDA4820T	Sync separation circuit for video applications	2473
TDA4850	Horizontal and vertical deflection controller for VGA/XGA and multi-frequency monitors	2478
TDA4851	Horizontal and vertical deflection controller for VGA/XGA and autosync monitors	2490

		PAGE
TDA4852	Horizontal and vertical deflection controller for autosync monitors	2503
TDA4860	Vertical deflection power amplifier for monitors	2516
TDA4861	Vertical deflection power amplifier for monitors	2524
TDA4865	Full-bridge current driven vertical deflection booster	2532
TDA4866	Full-bridge current driven vertical deflection booster	2542
TDA4880	Advanced monitor video controller	2552
TDA4881	Advanced monitor video controller	2558
TDA4882	Advanced monitor video controller for OSD	2566
TDA4883	Three-gain video preamplifier	2590
TDA4884	Three-gain control video preamplifier for OSD	2598
TDA5030A	TV VHF mixer/oscillator/UHF preamplifier	2619
TDA5030AT	TV VHF mixer/oscillator/UHF preamplifier	2625
TDA5140A	Brushless DC motor drive circuit	2631
TDA5141	Brushless DC motor drive circuit	2635
TDA5142T	Brushless DC motor drive circuit	2639
TDA5143T	Brushless DC motor drive circuit	2643
TDA5144T; TDA5144AT	Brushless DC motor drive circuit	2647
TDA5145	Brushless DC motor drive circuit	2651
TDA5330T	VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2655
TDA5332T	Double mixer/oscillator for TV and VCR tuners	2669
TDA5630	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2677
TDA5630BT	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 2-band tuners	2690
TDA5630CT	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2701
TDA5631	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2714
TDA5632	Low power VHF and UHF mixer/ oscillator for TV and VCR 2-band tuners	2727
TDA5633	Low power VHF and UHF mixer/oscillator for TV and VCR 2-band tuners	2737
TDA5634T	Low power UHF mixer/oscillator for TV and VCR tuners	2747
TDA5636	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2756
TDA5637	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2773

		PAGE
TDA5731M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2790
TDA5732M	Low power VHF, UHF mixer/oscillator for TV and VCR 2-band tuners	2804
TDA5736M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2819
TDA5737M	Low power VHF, UHF and hyperband mixer/oscillator for TV and VCR 3-band tuners	2837
TDA6101BQ	Video output amplifier	2854
TDA6101Q	Video output amplifier	2862
TDA6103Q	Triple video output amplifier	2872
TDA6111Q	Video output amplifier	2882
TDA6800; TDA6800T	Video modulator circuit	2893
TDA7050	Low-voltage mono/stereo power amplifier	2897
TDA7050T	Low-voltage mono/stereo power amplifier	2899
TDA7052	1 W BTL mono audio amplifier	2901
TDA7052A; TDA7052AT	1 W BTL mono audio amplifier with DC volume control	2903
TDA7052B; TDA7052BT	Mono BTL audio amplifier with DC volume control	2095
TDA7053	2 × 1 W portable/mains-fed stereo power amplifier	2097
TDA7053A; TDA7053AT	Stereo BTL audio output amplifiers with DC volume control	2909
TDA7056	3 W mono BTL audio output amplifier	2912
TDA7056A	3 W mono BTL audio output amplifier with DC volume control	2914
TDA7056B	5 W mono BTL audio output amplifier with DC volume control	2916
TDA7057AQ	2 × 5 W BTL stereo audio output amplifier with DC volume control	2918
TDA7057Q	2 × 3 W BTL stereo audio output amplifier	2921
TDA8000	Smart card interface	2924
TDA8001	Smart card interface	2927
TDA8005	Low power smart card coupler	2932
TDA8011T	IF amplifier for satellite TV receivers	2939
TDA8012M	Low power PLL FM demodulator for satellite TV receivers	2945
TDA8040T	Quadrature demodulator	2953
TDA8041H	Quadrature demodulator controller	2963
TDA8302	Small signal combination IC for colour TV	2973
TDA8303; TDA8303A	Small signal combination IC for black/white TV	2992
TDA8304	Small signal combination IC for colour TV	3010
TDA8310	PAL/NTSC colour processor for Picture-in-Picture (PIP) applications	3030
TDA8315T	Integrated NTSC decoder and sync processor	3049
TDA8340; TDA8341	Television IF amplifier and demodulator	3061
TDA8349A	Multistandard IF amplifier and demodulator	3072

		PAGE
TDA8350Q	DC-coupled vertical deflection and East-West output circuit	3085
TDA8351	DC-coupled vertical deflection circuit	3094
TDA8351A	DC-coupled vertical deflection circuit	3103
TDA8356	DC-coupled vertical deflection circuit	3112
TDA8360; TDA8361; TDA8362	Integrated PAL and PAL/NTSC TV processors	3120
TDA8366	I²C-bus controlled PAL/NTSC TV processor	3149
TDA8380A	Control circuit for Switched Mode Power Supplies (SMPS)	3189
TDA8395	SECAM decoder	3206
TDA8415	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3212
TDA8416	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3269
TDA8417	TV and VTR stereo/dual sound processor with integrated filters and I²C-bus control	3287
TDA8421	Hi-fi stereo audio processor; I²C-bus	3305
TDA8424	Hi-fi stereo audio processor; I²C-bus	3326
TDA8425	Hi-fi stereo audio processor; I²C-bus	3345
TDA8426	Hi-fi stereo audio processor; I²C-bus	3367
TDA8433	Deflection processor for computer controlled TV receivers; I²C-bus	3389
TDA8440	Switch for CTV receivers; I²C-bus	3411
TDA8442	I²C-bus interface for colour decoders	3421
TDA8443A	I²C-bus controlled YUV/RGB switch	3428
TDA8444	Octuple 6-bit DAC with I²C-bus	3443
TDA8446	Fast RGB/YC switch for digital decoding	3450
TDA8451A	P²CCD delay line and matrix	3459
TDA8452A	P²CCD filter combination for colour decoders	3469
TDA8453A	P²CCD filter combination for CVBS and S-VHS	3483
TDA8480T	RGB gamma-correction processor; I²C-bus	3495
TDA8490	SECAM decoder	3507
TDA8501	PAL/NTSC encoder	3516
TDA8505	SECAM encoder	3541
TDA8540	4 × 4 video matrix switch; I²C-bus	3566
TDA8601	RGB/YUV and fast blanking switch	3577
TDA8702	8-bit video digital-to-analog converter	3589
TDA8703	8-bit high-speed analog-to-digital converter	3603
TDA8705	6-bit high-speed dual analog-to-digital converter	3616
TDA8705A	6-bit high-speed dual analog-to-digital converter	3626
TDA8706	6-bit analog-to-digital converter with multiplexer and clamp	3636
TDA8707	Triple RGB 6-bit video analog-to-digital interface	3646

		PAGE
TDA8708A	Video analog input interface	3658
TDA8708B	Video analog input interface	3675
TDA8709A	Video analog input interface	3692
TDA8712; TDF8712	8-bit digital-to-analog converters	3711
TDA8714	8-bit high-speed analog-to-digital converter	3726
TDA8716	8-bit high-speed analog-to-digital converter	3741
TDA8718	8-bit high-speed analog-to-digital converter	3757
TDA8722	I^2C-bus programmable modulator for negative video modulation and FM sound	3766
TDA8725T	Antenna signal processor	3785
TDA8730	PLL FM demodulator for DBS signals	3792
TDA8732	NICAM-728 demodulator (NIDEM)	3798
TDA8735	PLL frequency synthesizer; I^2C-bus	3808
TDA8740; TDA8740H	Satellite sound circuit with noise reduction	3811
TDA8741; TDA8741H	Satellite sound circuit with noise reduction	3828
TDA8742; TDA8742H	Satellite sound circuit with noise reduction	3844
TDA8745	Satellite sound receiver with I^2C-bus control	3860
TDA8753A	YUV 8-bit analog-to-digital interface	3893
TDA8755	YUV 8-bit video low-power analog-to-digital interface	3908
TDA8758	YC 8-bit low-power analog-to-digital video interface	3923
TDA8760	10-bit high-speed analog-to-digital converter	3939
TDA8761	9-bit analog-to-digital converter for digital video	3960
TDA8762	10-bit high-speed low-power analog-to-digital converter	3974
TDA8766	10-bit high-speed 3 V analog-to-digital converter	3989
TDA8771	Triple 8-bit video digital-to-analog converter	4003
TDA8772; TDA8772A	Triple 8-bit video digital-to-analog converter	4015
TDA8776	10-bit, 500 MSPS digital-to-analog converter	4029
TDA9141	PAL/NTSC/SECAM decoder/sync processor; I^2C-bus	4042
TDA9150B	Programmable deflection controller; I^2C-bus	4065
TDA9151B	Programmable deflection controller; I^2C-bus	4094
TDA9160	PAL/NTSC/SECAM decoder/sync processor; I^2C-bus	4124
TDA9170	YUV picture improvement processor based on histogram modification; I^2C-bus	4148
TDA9610H	Audio FM processor for VHS hi-fi audio; I^2C-bus	4168
TDA9614H	Audio processor for VHS hi-fi and linear audio; I^2C-bus	4205
TDA9715H; TDA9715A	Y/C one-chip processor (VHS standard)	4260
TDA9800	VIF-PLL demodulator and FM-PLL detector	4301
TDA9802	Multistandard VIF-PLL demodulator and FM-PLL detector	4317
TDA9803	Multistandard VIF-PLL demodulator	4332

		PAGE
TDA9804	VIF-PLL demodulator with internal or external AGC and FM-PLL detector	4345
TDA9808	Single standard VIF-PLL with QSS-IF and FM-PLL demodulator	4360
TDA9812	Multistandard VIF-PLL and FM-PLL/AM demodulator	4378
TDA9814T	Multistandard VIF-PLL with QSS-IF and dual FM-PLL/AM demodulator	4404
TDA9815	Multistandard/MAC VIF-PLL with QSS-IF and dual FM-PLL/AM demodulator	4427
TDA9820	Multistandard/dual channel TV FM intercarrier sound demodulator	4450
TDA9821	Dual channel TV FM intercarrier sound demodulator	4457
TDA9830	TV sound AM demodulator and audio source switch	4463
TDA9840	TV and VTR stereo/dual sound processor with digital identification and I²C-bus	4473
TDA9845	TV and VTR stereo/dual sound processor with digital identification	4494
TDA9847	TV and VTR stereo/dual sound processor with digital identification	4508
TDA9854	I²C-bus controlled BTSC stereo/SAP decoder and audio processor	4526
TDA9855	I²C-bus controlled BTSC stereo/SAP decoder and audio processor	4565
TDA9860	Universal hi-fi audio processor for TV	4607
TDF8704	8-bit high-speed analog-to-digital converter	4620
TDF8712	8-bit digital-to-analog converters	3711
TEA1039	Control circuit for Switched Mode Power Supplies (SMPS)	4635
TEA5582	Economy PLL stereo decoder (BTSC system)	4647
TEA7650H	Video signal processor for CD-video/laser vision	4655
TSA5055T	2.5 GHz bidirectional I²C-bus controlled synthesizer	4674
TSA5511	1.3 GHz bidirectional I²C-bus controlled synthesizer	4685
TSA5512	1.3 GHz bidirectional I²C-bus controlled synthesizer	4697
TSA5514	1.3 GHz bidirectional I²C-bus controlled synthesizer	4709
TSA5515T	1.3 GHz bidirectional I²C-bus controlled synthesizer	4721
TSA5520; TSA5521	1.3 GHz universal bus-controlled TV synthesizer; I²C-bus	4732
TSA5522	1.4 GHz I²C-bus controlled synthesizer	4749
TSA5526; TSA5526A; TSA5527; TSA5527A	1.3 GHz universal bus-controlled TV synthesizer; I²C-bus	4762
µA733; 733C	Differential video amplifier	4782

GENERAL

	Page
Quality	36
Rating systems	37
Pro electron type numbering system of integrated circuits	39
Handling MOS devices	41

TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

General

Rating systems

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

BASIC TYPE NUMBER

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

First and second letters

DIGITAL FAMILY CIRCUITS

The first two letters identify the family.(1)

SOLITARY CIRCUITS

The first letter divides solitary circuits into:

S Solitary digital circuits

T Analog circuits

U Mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(2)

MICROPROCESSORS

The first two letters identify microprocessors and related circuits:

MA Microcomputer or central processing unit

MB Slice processor (functional slice of microprocessor)

MD Related memories

ME Other related circuits such as interfaces, clocks, peripheral controllers, etc.

CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

The first two letters identify:

NH Hybrid circuits

NL Logic circuits

NM Memories

NS Analog signal processing using switched capacitors

NT Analog signal processing using charge-transfer devices

NX Imaging devices

NY Other related circuits.

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

(2) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

Third letter

The third letter indicates the operating ambient temperature range:

A temperature range not specified below

B 0 to +70 °C

C −55 to +125 °C

D −25 to +70 °C

E −25 to +85 °C

F −40 to +85 °C

G −55 to +85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

SERIAL NUMBER

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

VERSION LETTER

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C Cylindrical

D Ceramic dual in-line (CERDIL, CERDIP)

F Flat pack (two leads)

G Flat pack (four leads)

H Quad flat pack (QFP)

L Chip on tape (foil)

P Plastic dual in-line (DIL)

Q Quad in-line (QUIL)

T Mini pack (SOL, SO, VSO)

U Uncased chip.

TWO-LETTER SUFFIX

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

First letter (general shape)

C Cylindrical

D Dual in-line (DIL)

E Power DIL (with external heatsink)

F Flat pack (leads on two sides)

G Flat pack (leads on four sides)

H Quad flat pack (QFP)

K Diamond (TO-3 family)

M Multiple in-line (except dual, triple and quad)

Q Quad in-line (QUIL)

R Power QUIL (with external heatsink)

S Single in-line (SIL)

T Triple in-line

W Leaded chip carrier (LCC)

X Leadless chip carrier (LLCC)

Y Pin grid array (PGA).

Second letter (material)

C Metal-ceramic

G Glass-ceramic

M Metal

P Plastic.

EXAMPLES

PCF1105WP: digital IC; PC family; operating temperature range –40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range –55 to +125 °C; serial number 2000.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor.
- All mains-powered electrical equipment should be connected via an earth leakage switch.
- Equipment cases should be earthed.
- Relative humidity should be maintained between 50 and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

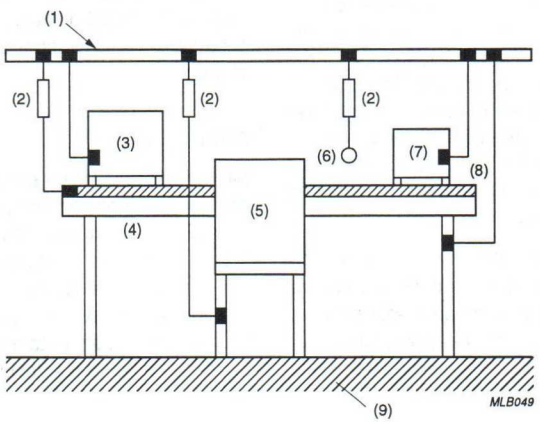
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.
(9) Antistatic floor.

Fig.1 Protected work station.

DEVICE DATA

CMOS single-chip 8-bit microcontroller 80C528/83C528

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

DESCRIPTION

The 8XC528 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 8XC528 has the same instruction set as the 80C51. Three versions of the derivative exist:

- 83C528 — 32k bytes mask programmable ROM
- 80C528 — ROMless version of the 83C528
- 87C528 — 32k bytes EPROM (described in a separate data sheet)

This device provides architectural enhancements that make it applicable in a variety of applications in consumer, telecom and general control systems, especially in those systems which need large ROM and RAM capacity on-chip.

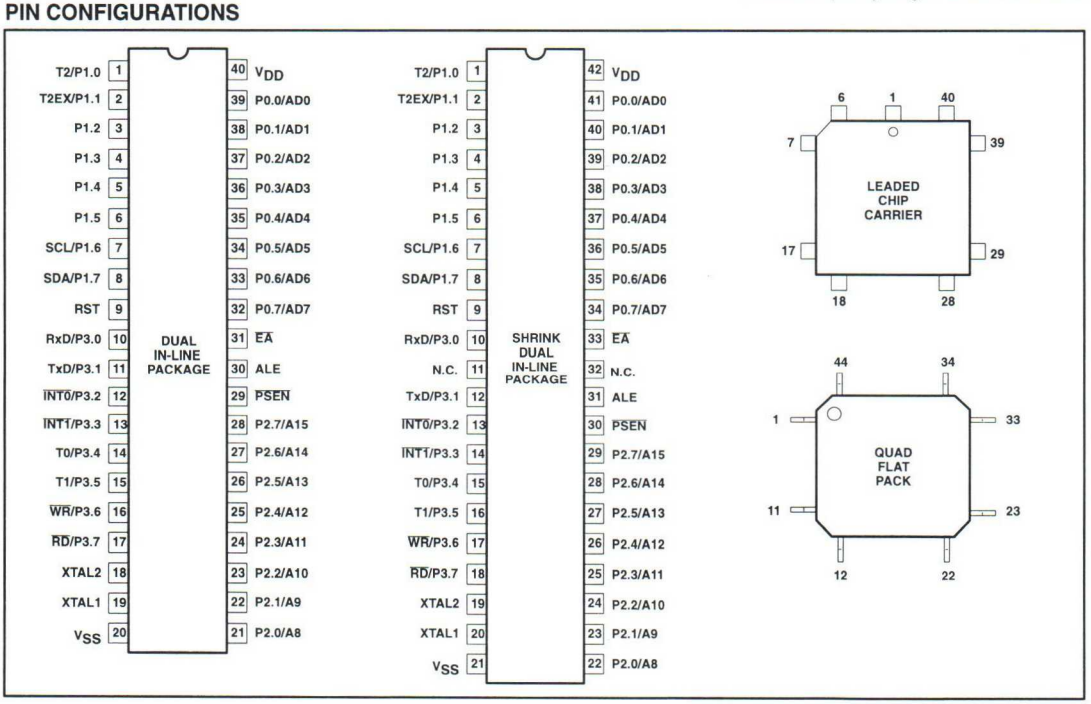
The 8XC528 contains a 32k × 8 ROM (83C528), a 512 × 8 RAM, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a 16-bit timer (identical to the timer 2 of the 80C52), a watchdog timer with a separate oscillator, a multi-source, two-priority-level, nested interrupt structure, two serial interfaces (UART and I²C-bus), and on-chip oscillator and timing circuits.

In addition, the 8XC528 has two software selectable modes of power reduction — idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

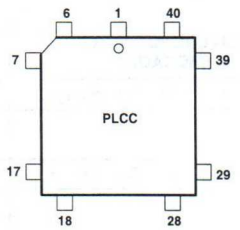
FEATURES

- 80C51 instruction set
  - 32k × 8 ROM (83C528)
  - ROMless (80C528)
  - 512 × 8 RAM
  - Memory addressing capability 64k ROM and 64k RAM
  - Three 16-bit counter/timers
  - On-chip watchdog timer with oscillator
  - Full duplex UART
  - I²C serial interface
  - Four 8-bit I/O ports
- Power control modes:
  - Idle mode
  - Power-down mode
  - Warm start from power-down
- CMOS and TTL compatible
- Extended temperature ranges
- ROM code protection
- 7-source and 7-vector interrupt structure with 2 priority levels
- Up to 3 external interrupt request inputs
- Two programmable power reduction modes (Idle and Power-down)
- Termination of Idle mode by any interrupt, external or WDT (watchdog) reset
- XTAL frequency range: 1.2 MHz to 16 MHz

PIN CONFIGURATIONS

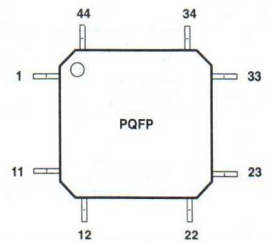


CERAMIC AND PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS



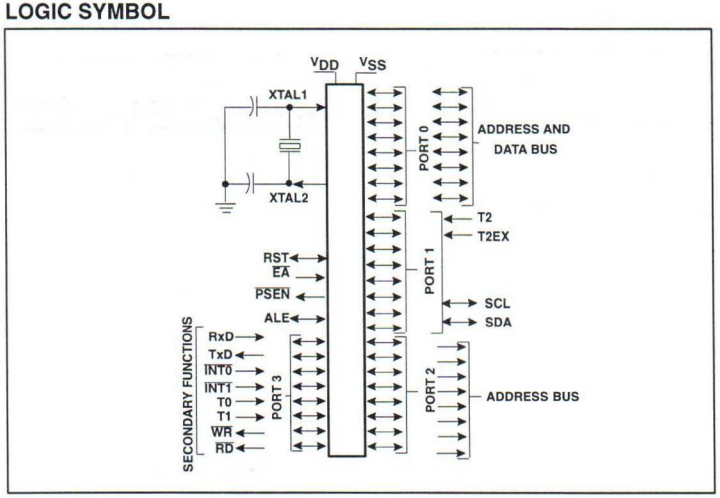
Pin	Function	Pin	Function
1	NC	23	NC
2	P1.0/T2	24	P2.0/A8
3	P1.1/T2EX	25	P2.1/A9
4	P1.2	26	P2.2/A10
5	P1.3	27	P2.3/A11
6	P1.4	28	P2.4/A12
7	P1.5	29	P2.5/A13
8	P1.6/SCL	30	P2.6/A14
9	P1.7/SDA	31	P2.7/A15
10	RST	32	$\overline{PSEN}$
11	P3.0/RxD	33	ALE
12	NC	34	NC
13	P3.1/TxD	35	$\overline{EA}$
14	P3.2/$\overline{INT0}$	36	P0.7/AD7
15	P3.3/$\overline{INT1}$	37	P0.6/AD6
16	P3.4/T0	38	P0.5/AD5
17	P3.5/T1	39	P0.4/AD4
18	P3.6/$\overline{WR}$	40	P0.3/AD3
19	P3.7/$\overline{RD}$	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	V_{SS}	44	V_{DD}

PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function
1	P1.5	23	P2.5/A13
2	P1.6/SCL	24	P2.6/A14
3	P1.7/SDA	25	P2.7/A15
4	RST	26	$\overline{PSEN}$
5	P3.0/RxD	27	ALE
6	NC	28	NC
7	P3.1/TxD	29	$\overline{EA}$
8	P3.2/$\overline{INT0}$	30	P0.7/AD7
9	P3.3/$\overline{INT1}$	31	P0.6/AD6
10	P3.4/T0	32	P0.5/AD5
11	P3.5/T1	33	P0.4/AD4
12	P3.6/$\overline{WR}$	34	P0.3/AD3
13	P3.7/$\overline{RD}$	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	V_{SS}	38	V_{DD}
17	NC	39	NC
18	P2.0/A8	40	P1.0/T2
19	P2.1/A9	41	P1.1/T2EX
20	P2.2/A10	42	P1.2
21	P2.3/A11	43	P1.3
22	P2.4/A12	44	P1.4

LOGIC SYMBOL



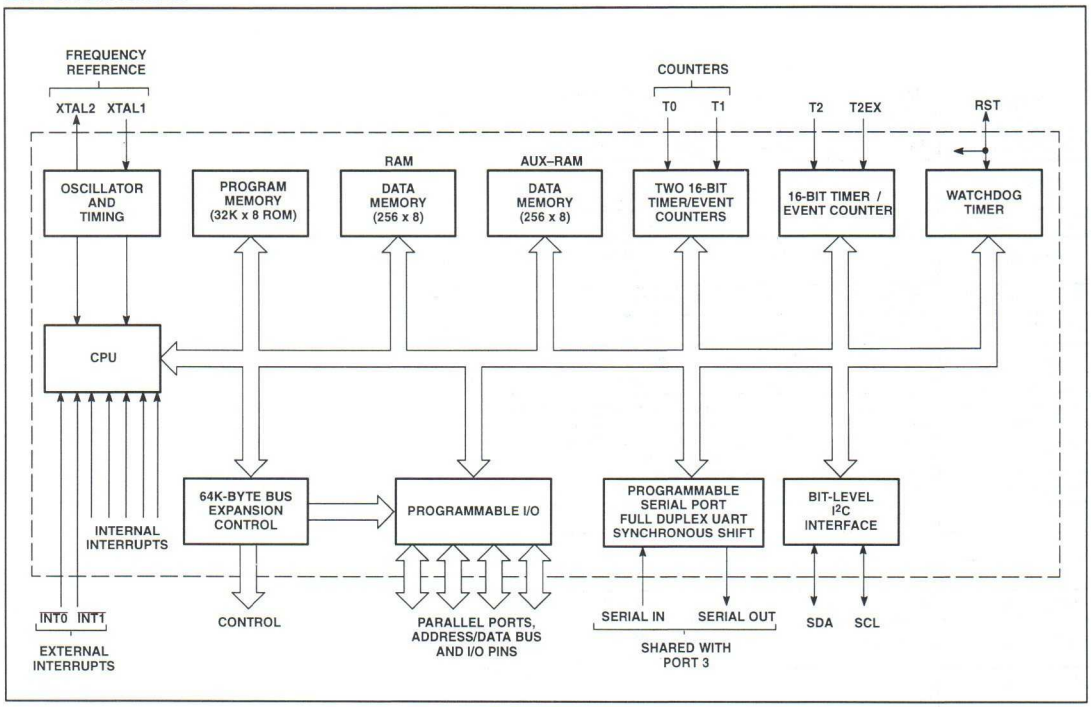
ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA PART ORDER NUMBER				
ROMless	ROM	ROMless	ROM	Drawing Number	TEMPERATURE °C RANGE AND PACKAGE	FREQ MHz
P80C528FBP	P83C528FBP/xxx	P80C528FBP N	P83C528FBP N	SOT129-1	0 to +70, Plastic Dual In-line Package	16
P80C528FBA	P83C528FBA/xxx	P80C528FBA A	P83C528FBA A	SOT187	0 to +70, Plastic Leaded Chip Carrier	16
P80C528FBB	P83C528FBB/xxx	P80C528FBB B	P83C528FBB B	SOT307-2	0 to +70, Plastic Quad Flat Pack	16
P80C528FFP	P83C528FFP/xxx	P80C528FFP N	P83C528FFP N	SOT129-1	–40 to +85, Plastic Dual In-line Package	16
P80C528FFA	P83C528FFA/xxx	P80C528FFA A	P83C528FFA A	SOT187	–40 to +85, Plastic Leaded Chip Carrier	16
P80C528FFB	P83C528FFB/xxx	P80C528FFB B	P83C528FFB B	SOT307-2	–40 to +85, Plastic Quad Flat Pack	16
P80C528FHP	P83C528FHP/xxx	P80C528FHP N	P83C528FHP N	SOT129-1	–40 to +125, Plastic Dual In-line Package	16
P80C528FHA	P83C528FHA/xxx	P80C528FHA A	P83C528FHA A	SOT187	–40 to +125, Plastic Leaded Chip Carrier	16
P80C528FHB	P83C528FHB/xxx	P80C528FHB B	P83C528FHB B	SOT307-2	–40 to +125, Plastic Quad Flat Pack	16
	P83C528FBR/xxx			SOT270	0 to +70, Plastic Shrink Dual In-Linr Package	16

NOTE:
1. xxx denotes the ROM code number.

EPROM	Drawing Number	TEMPERATURE °C RANGE AND PACKAGE	FREQ MHz
P87C528EBP N	SOT129-1	0 to +70, Plastic Dual In-line Package	16
P87C528EBF FA	0590B	0 to +70, Ceramic Dual In-line Package w/Window	16
P87C528EBA AA	0403G	0 to +70, Plastic Leaded Chip Carrier	16
P87C528EBL KA	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	16
P87C528EBB B	SOT307-2	0 to +70, Plastic Quad Flat Pack	16
P87C528EFP N	SOT129-1	–40 to +85, Plastic Dual In-line Package	16
P87C528EFF FA	0590B	–40 to +85, Ceramic Dual In-line Package w/Window	16
P87C528EFF FA	0403G	–40 to +85, Plastic Leaded Chip Carrier	16
P87C528EFL KA	1472A	–40 to +85, Ceramic Leaded Chip Carrier w/Window	16
P87C528EFB B	SOT307-2	–40 to +85, Plastic Quad Flat Pack	16
P87C528GBP N	SOT129-1	0 to +70, Plastic Dual In-line Package	20
P87C528GBF FA	0590B	0 to +70, Ceramic Dual In-line Package w/Window	20
P87C528GBA A	0403G	0 to +70, Plastic Leaded Chip Carrier	20
P87C528GBL KA	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	20
P87C52GFP N	SOT129-1	–40 to +85, Plastic Dual In-line Package	20
P87C52GFF FA	0590B	0 to +70, Ceramic Dual In-line Package w/Window	20
P87C52GFA A	0403G	0 to +70, Plastic Leaded Chip Carrier	20
P87C52GFL KA	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	20

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO. DIP	SDIL	LCC	QFP	TYPE	NAME AND FUNCTION
V_{SS}	20	21	22	16	I	**Ground:** circuit ground potential.
V_{DD}	40	42	44	38	I	**Power Supply:** +5V power supply pin during normal operation, Idle mode and Power-down mode.
P0.0–0.7	39–32	41–34	43–36	37–30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.
P1.0–P1.7	1–8	1–8	2–9	40–44 1–3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7 which have open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 can sink/source one TTL (4 LSTTL) inputs.
	1	1	2	40	I	**T2 (P1.0):** Timer/counter 2 external count input (following edge triggered).
	2	2	3	41	I	**T2EX (P1.1):** Timer/counter 2 trigger input.
	7	7	8	2	I/O	**SCL (P1.6):** I^2C serial port clock line.
	8	8	9	3	I/O	**SDA (P1.7):** I^2C serial port data line.
P2.0–P2.7	21–28	22–29	24–31	18–25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	10–18 (11=NC)	11, 13–19	5, 7–13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the SC80C51 family, as listed below:
	10	10	11	5	I	**RxD (P3.0):** Serial input port
	11	12	13	7	O	**TxD (P3.1):** Serial output port
	12	13	14	8	I	**$\overline{INT0}$ (P3.2):** External interrupt
	13	14	15	9	I	**$\overline{INT1}$ (P3.3):** External interrupt
	14	15	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	16	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	17	18	12	O	**$\overline{WR}$ (P3.6):** External data memory write strobe
	17	18	19	13	O	**$\overline{RD}$ (P3.7):** External data memory read strobe
RST	9	9	10	4	I/O	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{DD}. After a watchdog timer overflow, this pin is pulled high while the internal reset signal is active.
ALE	30	31	33	27	I/O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory.
$\overline{PSEN}$	29	30	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
$\overline{EA}$	31	33	35	29	I	**External Access Enable:** $\overline{EA}$ must be externally held low during RESET to enable the device to fetch code from external program memory locations 0000H to 7FFFH. If $\overline{EA}$ is held high during RESET, the device executes from internal program memory unless the program counter contains an address greater than 7FFFH. $\overline{EA}$ is don't care after RESET.
XTAL1	19	20	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	19	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

CMOS single-chip 8-bit microcontroller — 80C652/83C652

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

DESCRIPTION

The P80C652/83C652 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 80C652/83C652 has the same instruction set as the 80C51. Three versions of the derivative exist:

83C652 — 8k bytes mask programmable ROM

80C652 — ROMless version

87C652 — EPROM version (described in a separate chapter)

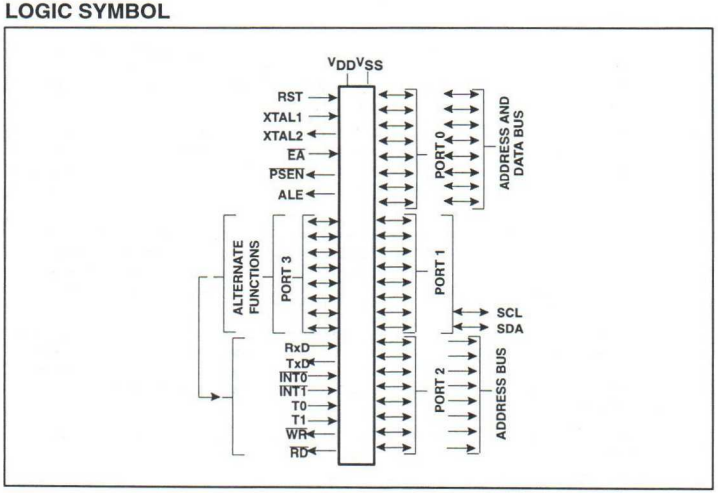
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 8XC652 contains a non-volatile 8k × 8 read-only program memory, a volatile 256 × 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC652 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16(24)MHz crystal, 58% of the instructions are executed in 0.75(0.5)µs and 40% in 1.5(1)µs. Multiply and divide instructions require 3(2)µs.

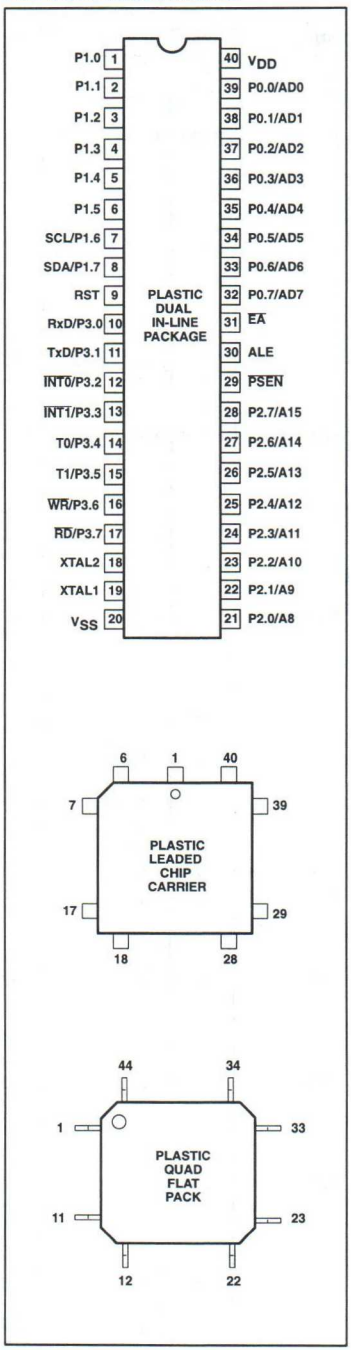
FEATURES

- 80C51 central processing unit
- 8k × 8 ROM expandable externally to 64k bytes
- 256 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- Power control modes
  - Idle mode
  - Power-down mode
- ROM code protection
- Extended frequency range: 1.2 to 24 MHz
- Three operating ambient temperature ranges:
  - 0 to +70°C
  - –40 to +85°C
  - –40 to +125°C

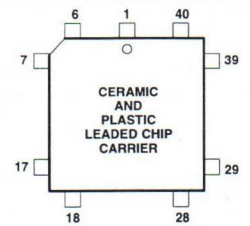
LOGIC SYMBOL



PIN CONFIGURATIONS

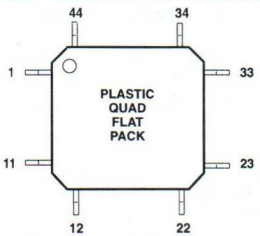


CERAMIC AND PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS



Pin	Function	Pin	Function
1	NC	23	NC
2	P1.0	24	P2.0/A8
3	P1.1	25	P2.1/A9
4	P1.2	26	P2.2/A10
5	P1.3	27	P2.3/A11
6	P1.4	28	P2.4/A12
7	P1.5	29	P2.5/A13
8	P1.6/SCL	30	P2.6/A14
9	P1.7/SDA	31	P2.7/A15
10	RST	32	$\overline{PSEN}$
11	P3.0/RxD	33	ALE
12	NC	34	NC
13	P3.1/TxD	35	$\overline{EA}$
14	P3.2/$\overline{INT0}$	36	P0.7/AD7
15	P3.3/$\overline{INT1}$	37	P0.6/AD6
16	P3.4/T0	38	P0.5/AD5
17	P3.5/T1	39	P0.4/AD4
18	P3.6/$\overline{WR}$	40	P0.3/AD3
19	P3.7/$\overline{RD}$	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	V_{SS}	44	V_{DD}

PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function
1	P1.5	23	P2.5/A13
2	P1.6/SCL	24	P2.6/A14
3	P1.7/SDA	25	P2.7/A15
4	RST	26	$\overline{PSEN}$
5	P3.0/RxD	27	ALE
6	V_{SS4}	28	V_{SS2}
7	P3.1/TxD	29	$\overline{EA}$/V_{PP}
8	P3.2/$\overline{INT0}$	30	P0.7/AD7
9	P3.3/$\overline{INT1}$	31	P0.6/AD6
10	P3.4/T0	32	P0.5/AD5
11	P3.5/T1	33	P0.4/AD4
12	P3.6/$\overline{WR}$	34	P0.3/AD3
13	P3.7/$\overline{RD}$	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	V_{SS1}	38	V_{DD}
17	NC	39	V_{SS3}
18	P2.0/A8	40	P1.0
19	P2.1/A9	41	P1.1
20	P2.2/A10	42	P1.2
21	P2.3/A11	43	P1.3
22	P2.4/A12	44	P1.4

NOTES TO QFP ONLY:

1. Due to EMC improvements, all V_{SS} pins (6, 16, 28, 39) must be connected to V_{SS} on the 80C652/83C652.

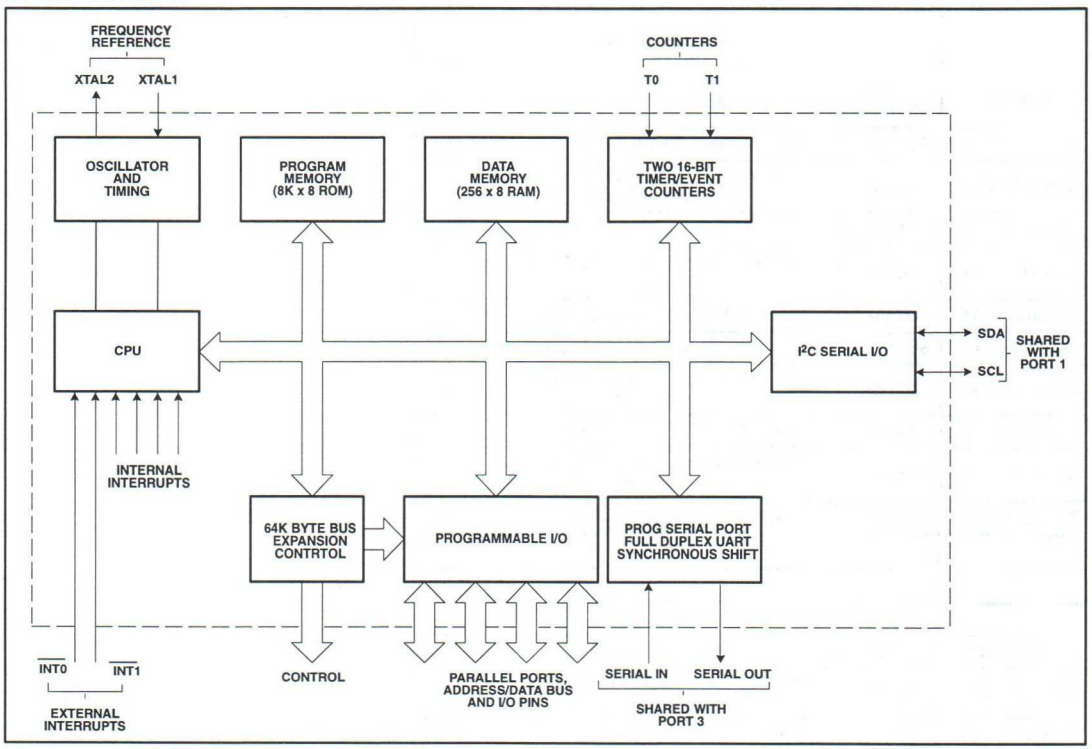
ORDER INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING			PHILIPS NORTH AMERICA PART ORDER NUMBER		TEMPERATURE RANGE (°C) AND PACKAGE	FREQ MHz[1,2]
ROMless	ROM[3]	Drawing Number	ROMless	ROM		
P80C652FBP	P83C652FBP/xxx	SOT129-1	S80C652FBPN	S83C652FBPN	0 to +70, Plastic Dual In-line Package	16
P80C652FBA	P83C652FBA/xxx	SOT187	S80C652FBAA	S83C652FBAA	0 to +70, Plastic Leaded Chip Carrier	16
P80C652FBB	P83C652FBB/xxx	SOT307-2 [4]	S80C652FBBB	S83C652FBBB	0 to +70, Plastic Quad Flat Pack	16
P80C652FFP	P83C652FFP/xxx	SOT129-1	S80C652FFPN	S83C652FFPN	–40 to +85, Plastic Dual In-line Package	16
P80C652FFA	P83C652FFA/xxx	SOT187	S80C652FFAA	S83C652FFAA	–40 to +85, Plastic Leaded Chip Carrier	16
P80C652FFB	P83C652FFB/xxx	SOT307-2 [4]	S80C652FFBB	S83C652FFBB	–40 to +85, Plastic Quad Flat Pack	16
P80C652FHP	P83C652FHP/xxx	SOT129-1	S80C652FHPN	S83C652FHPN	–40 to +125, Plastic Dual In-line Package	16
P80C652FHA	P83C652FHA/xxx	SOT187	S80C652FHAA	S83C652FHAA	–40 to +125, Plastic Leaded Chip Carrier	16
P80C652FHB	P83C652FHB/xxx	SOT307-2 [4]	S80C652FHBB	S83C652FHBB	–40 to +125, Plastic Quad Flat Pack	16
P80C652IBP	P83C652IBP/xxx	SOT129-1	S80C652IBPN	S83C652IBPN	0 to +70, Plastic Dual In-line Package	24
P80C652IBA	P83C652IBA/xxx	SOT187	S80C652IBAA	S83C652IBAA	0 to +70, Plastic Leaded Chip Carrier	24
P80C652IBB	P83C652IBB/xxx	SOT307-2 [4]	S80C652IBBB	S83C652IBBB	0 to +70, Plastic Quad Flat Pack	24
P80C652IFP	P83C652IFP/xxx	SOT129-1	S80C652IFPN	S83C652IFPN	–40 to +85, Plastic Dual In-line Package	24
P80C652IFA	P83C652IFA/xxx	SOT187	S80C652IFAA	S83C652IFAA	–40 to +85, Plastic Leaded Chip Carrier	24
P80C652IFB	P83C652IFB/xxx	SOT307-2 [4]	S80C652IFBB	S83C652IFBB	–40 to +85, Plastic Quad Flat Pack	24

NOTES:
1. 80C652 and 83C652 frequency range is 1.2MHz–16MHz or 1.2 to 24MHz.
2. For specification of the EPROM version, see the 87C652 data sheet.
3. xxx denotes the ROM code number.
4. SOT311 replaced by SOT307-2.

EPROM[2]	Drawing Number	TEMPERATURE RANGE (°C) AND PACKAGE	FREQ MHz[1,2]
S87C652-4N40	SOT129-1	0 to +70, Plastic Dual In-line Package	16
S87C652-4F40	0590B	0 to +70, Ceramic Dual In-line Package w/Window	16
S87C652-4A44	0403G	0 to +70, Plastic Leaded Chip Carrier	16
S87C652-4K44	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	16
S87C652-4B44	SOT307-2	0 to +70, Plastic Quad Flat Pack	16
S87C652-5N40	SOT129-1	–40 to +85, Plastic Dual In-line Package	16
S87C652-5F40	0590B	–40 to +85, Ceramic Dual In-line Package w/Window	16
S87C652-5A44	0403G	–40 to +85, Plastic Leaded Chip Carrier	16
S87C652-5K44	1472A	–40 to +85, Ceramic Leaded Chip Carrier w/Window	16
S87C652-5B44	SOT307-2	–40 to +85, Plastic Quad Flat Pack	16
S87C652-7N40	SOT129-1	0 to +70, Plastic Dual In-line Package	20
S87C652-7F40	0590B	0 to +70, Ceramic Dual In-line Package w/Window	20
S87C652-7A44	0403G	0 to +70, Plastic Leaded Chip Carrier	20
S87C652-7K44	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	20
S87C652-8N40	SOT129-1	–40 to +85, Plastic Dual In-line Package	20
S87C652-8F40	0590B	–40 to +85, Ceramic Dual In-line Package w/Window	20
S87C652-8A44	0403G	–40 to +85, Plastic Leaded Chip Carrier	20
S87C652-8K44	1472A	–40 to +85, Ceramic Leaded Chip Carrier w/Window	20

BLOCK DIAGRAM



PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER DIP	PLCC	QFP	TYPE	NAME AND FUNCTION
V_{SS}	20	22	6, 16, 28, 39	I	**Ground:** 0V reference. With the QFP package all V_{SS} pins (V_{SS1} to V_{SS4}) must be connected.
V_{DD}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	39–32	43–36	37–30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.
P1.0–P1.7	1–8	2–9	40–44, 1–3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7 which are open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Alternate functions include:
P1.6	7	8	2	I/O	**SCL:** I^2C-bus serial port clock line.
P1.7	8	9	3	I/O	**SDA:** I^2C-bus serial port data line.
P2.0–P2.7	21–28	24–31	18–25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port
	11	13	7	O	**TxD (P3.1):** Serial output port
	12	14	8	I	**$\overline{INT0}$ (P3.2):** External interrupt
	13	15	9	I	**$\overline{INT1}$ (P3.3):** External interrupt
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{WR}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{RD}$ (P3.7):** External data memory read strobe
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{DD}.
ALE	30	33	27	I/O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency. Note that one ALE pulse is skipped during each access to external data memory.
$\overline{PSEN}$	29	32	26	O	**Program Store Enable:** Read strobe to external program memory via Port 0 and Port 2. It is activated twice each machine cycle during fetches from the external program memory. When executing out of external program memory two activations of $\overline{PSEN}$ are skipped during each access to external data memory. $\overline{PSEN}$ is not activated (remains HIGH) during no fetches from external program memory. $\overline{PSEN}$ can sink/source 8 LSTTL inputs and can drive CMOS inputs without external pull–ups.
$\overline{EA}$	31	35	29	I	**External Access:** If during a RESET, $\overline{EA}$ is held at TTL, level HIGH, the CPU executes out of the internal program memory ROM provided the Program Counter is less than 8192. If during a RESET, $\overline{EA}$ is held a TTL LOW level, the CPU executes out of external program memory. $\overline{EA}$ is not allowed to float.
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

NOTE:
To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than V_{DD} + 0.5V or V_{SS} – 0.5V, respectively.

CMOS single-chip 8-bit microcontroller 83C654

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

DESCRIPTION

The P83C654 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 83C654 has the same instruction set as the 80C51. Two versions of the derivative exist:

83C654 — 16k bytes mask programmable ROM

87C654 — EPROM version (described in a separate data sheet)

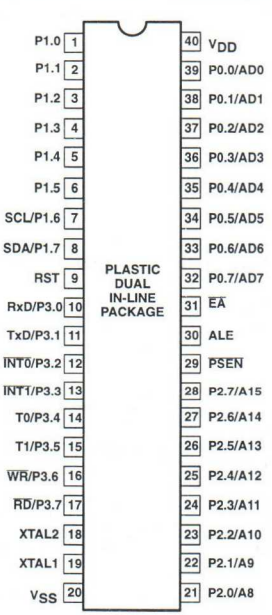
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 83C654 contains a non-volatile 16k × 8 read-only program memory, a volatile 256 × 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I²C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC654 can be expanded using standard TTL compatible memories and logic.

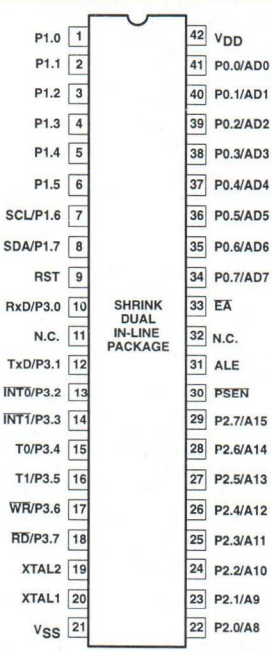
The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16(24)MHz crystal, 58% of the instructions are executed in 0.75(0.5)µs and 40% in 1.5(1)µs. Multiply and divide instructions require 3(2)µs.

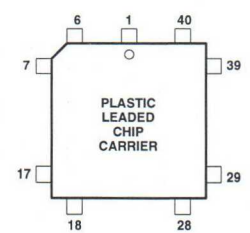
FEATURES

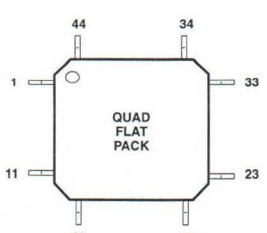
- 80C51 central processing unit
- 16k × 8 ROM expandable externally to 64k bytes
- 256 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I²C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- Power control modes
  - Idle mode
  - Power-down mode
- ROM code protection
- Extended frequency range: 1.2 to 24 MHz
- Three operating ambient temperature ranges:
  - 0 to +70°C
  - –40 to +85°C
  - –40 to +125°C

PIN CONFIGURATIONS



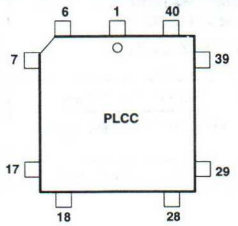






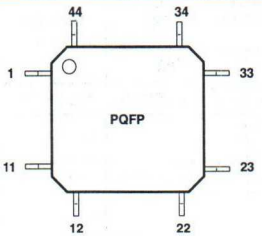
SEE PAGE 3 FOR QFP AND LCC PIN FUNCTIONS.

PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS



Pin	Function	Pin	Function
1	NC	23	NC
2	P1.0	24	P2.0/A8
3	P1.1	25	P2.1/A9
4	P1.2	26	P2.2/A10
5	P1.3	27	P2.3/A11
6	P1.4	28	P2.4/A12
7	P1.5	29	P2.5/A13
8	P1.6/SCL	30	P2.6/A14
9	P1.7/SDA	31	P2.7/A15
10	RST	32	$\overline{PSEN}$
11	P3.0/RxD	33	ALE
12	NC	34	NC
13	P3.1/TxD	35	$\overline{EA}$
14	P3.2/$\overline{INT0}$	36	P0.7/AD7
15	P3.3/$\overline{INT1}$	37	P0.6/AD6
16	P3.4/T0	38	P0.5/AD5
17	P3.5/T1	39	P0.4/AD4
18	P3.6/$\overline{WR}$	40	P0.3/AD3
19	P3.7/$\overline{RD}$	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	V_{SS}	44	V_{DD}

PLASTIC QUAD FLAT PACK PIN FUNCTIONS

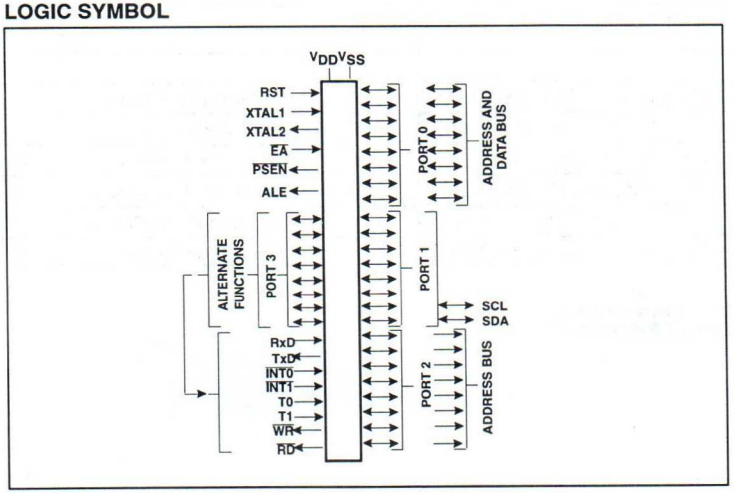


Pin	Function	Pin	Function
1	P1.5	23	P2.5/A13
2	P1.6/SCL	24	P2.6/A14
3	P1.7/SDA	25	P2.7/A15
4	RST	26	$\overline{PSEN}$
5	P3.0/RxD	27	ALE
6	V_{SS4}	28	V_{SS2}
7	P3.1/TxD	29	$\overline{EA}$/V_{PP}
8	P3.2/$\overline{INT0}$	30	P0.7/AD7
9	P3.3/$\overline{INT1}$	31	P0.6/AD6
10	P3.4/T0	32	P0.5/AD5
11	P3.5/T1	33	P0.4/AD4
12	P3.6/$\overline{WR}$	34	P0.3/AD3
13	P3.7/$\overline{RD}$	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	V_{SS1}	38	V_{DD}
17	NC	39	V_{SS3}
18	P2.0/A8	40	P1.0
19	P2.1/A9	41	P1.1
20	P2.2/A10	42	P1.2
21	P2.3/A11	43	P1.3
22	P2.4/A12	44	P1.4

NOTES TO QFP ONLY:

1. Due to EMC improvements, all V_{SS} pins (6, 16, 28, 39) must be connected to V_{SS} on the 80C652/83C654.

LOGIC SYMBOL



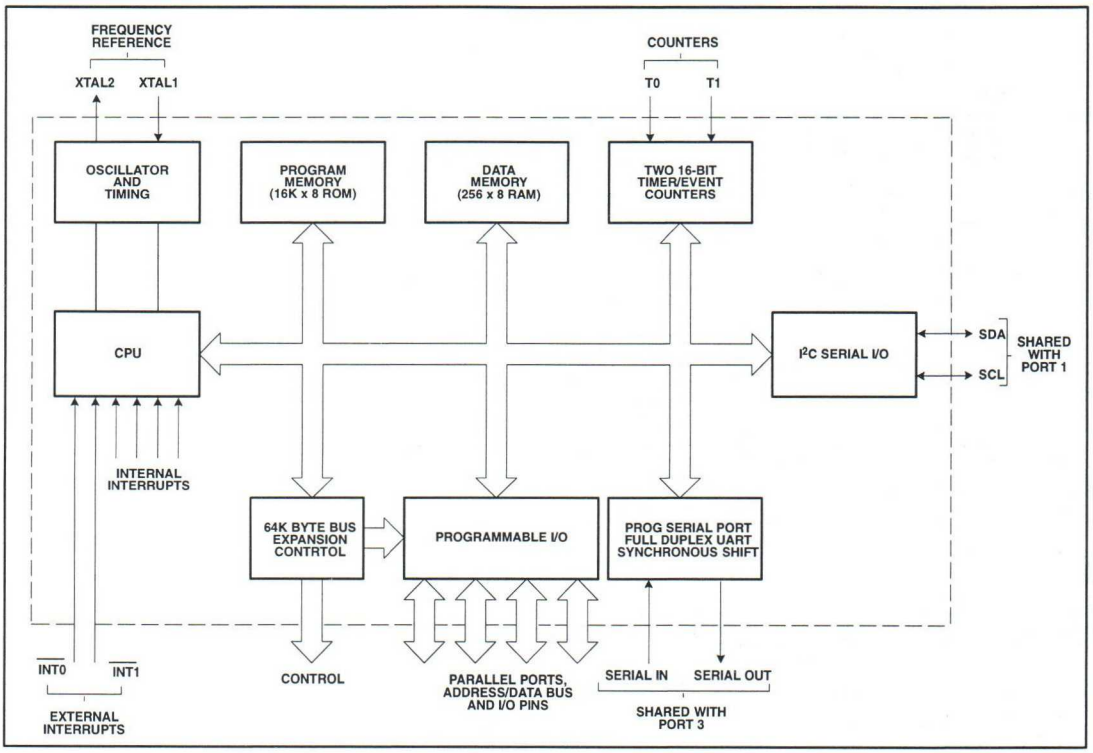
ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA PART ORDER NUMBER		Drawing Number	TEMPERATURE RANGE °C AND PACKAGE	FREQ MHz[2,3]
ROMless[1]	ROM	ROMless[1]	ROM			
P80C652FBP	P83C654FBP/xxx	P80C652FBPN	P83C654FBPN	SOT129-1	0 to +70, Plastic Dual In-line Package	16
					0 to +70, Ceramic Dual In-line Package w/Window	16
P80C652FBA	P83C654FBA/xxx	P80C652FBAA	P83C654FBAA	SOT187	0 to +70, Plastic Leaded Chip Carrier	16
P80C652FBB	P83C654FBB/xxx	P80C652FBBB	P83C654FBBB	SOT307-2[5]	0 to +70, Plastic Quad Flat Pack	16
	P83C654FBR/xxx			SOT270	0 to +70, Plastic Shrink Dual In-Line Package	
P80C652FFP	P83C654FFP/xxx	P80C652FFPN	P83C654FFPN	SOT129-1	–40 to +85, Plastic Dual In-line Package	16
P80C652FFA	P83C654FFA/xxx	P80C652FFAA	P83C654FFAA	SOT187	–40 to +85, Plastic Leaded Chip Carrier	16
P80C652FFB	P83C654FFB/xxx	P80C652FFBB	P83C654FFBB	SOT307-2[5]	–40 to +85, Plastic Quad Flat Pack	16
P80C652FHP	P83C654FHP/xxx	P80C652FHPN	P83C654FHPN	SOT129-1	–40 to +125, Plastic Dual In-line Package	16
P80C652FHA	P83C654FHA/xxx	P80C652FHAA	P83C654FHAA	SOT187	–40 to +125, Plastic Leaded Chip Carrier	16
P80C652FHB	P83C654FHB/xxx	P80C652FHBB	P83C654FHBB	SOT307-2[5]	–40 to +125, Plastic Quad Flat Pack	16
P80C652IBP	P83C654IBP/xxx	P80C652IBPN	P83C654IBPN	SOT129-1	0 to +70, Plastic Dual In-line Package	24
P80C652IBA	P83C654IBA/xxx	P80C652IBAA	P83C654IBAA	SOT187	0 to +70, Plastic Leaded Chip Carrier	24
P80C652IBB	P83C654IBB/xxx	P80C652IBBB	P83C654IBBB	SOT307-2[5]	0 to +70, Plastic Quad Flat Pack	24
P80C652IFP	P83C654IFP/xxx	P80C652IFPN	P83C654IFPN	SOT129-1	–40 to +85, Plastic Dual In-line Package	24
P80C652IFA	P83C654IFA/xxx	P80C652IFAA	P83C654IFAA	SOT187	–40 to +85, Plastic Leaded Chip Carrier	24
P80C652IFB	P83C654IFB/xxx	P80C652IFBB	P83C654IFBB	SOT307-2[5]	–40 to +85, Plastic Quad Flat Pack	24

NOTES:
1. For full specification, see the 80C652/83C652 data sheet.
2. 83C654 frequency range is 1.2MHz – 16MHz or 1.2MHz – 24MHz.
3. For specification of the EPROM version, see the 87C654 data sheet.
4. xxx denotes the ROM code number.
5. SOT311 replaced by SOT307-2.

EPROM[3]	Drawing Number	TEMPERATURE RANGE °C AND PACKAGE	FREQ MHz[2,3]
S87C654-4N40	SOT129-1	0 to +70, Plastic Dual In-line Package	16
S87C654-4F40	0590B	0 to +70, Ceramic Dual In-line Package w/Window	16
S87C654-4A44	0403G	0 to +70, Plastic Leaded Chip Carrier	16
S87C654-4K44	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	16
S87C654–4B44	SOT307-2	0 to +70, PlasticQuad Flat Pack	16
S87C654-5N40	SOT129-1	–40 to +85, Plastic Dual In-line Package	16
S87C654-5F40	0590B	–40 to +85, Ceramic Dual In-line Package w/Window	16
S87C654-5A44	0403G	–40 to +85, Plastic Leaded Chip Carrier	16
S87C654–5K44	1472A	–40 to +85, Ceramic Leaded Chip Carrier w/Window	16
S87C654-5B44	SOT307-2	–40 to +85, Plastic Quad Flat Pack	16
S87C654–7N40	SOT129-1	0 to +70, Plastic Dual In-line Package	20
S87C654–7F40	0590B	0 to +70, Ceramic Dual In-line Package w/Window	20
S87C654–7A44	0403G	0 to +70, Plastic Leaded Chip Carrier	20
S87C654–7K44	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	20
S87C654–8N40	SOT129-1	–40 to +85, Plastic Dual In-line Package	20
S87C654–8F40	0590B	–40 to +85, Ceramic Dual In-line Package w/Window	20
S87C654–8A44	0403G	–40 to +85, Plastic Leaded Chip Carrier	20

BLOCK DIAGRAM



PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER DIP	PLCC	QFP	TYPE	NAME AND FUNCTION
V_{SS}	20	22	6, 16, 28, 39	I	**Ground:** 0V reference. With the QFP package all V_{SS} pins (V_{SS1} to V_{SS4}) must be connected.
V_{DD}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	39–32	43–36	37–30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.
P1.0–P1.7	1–8	2–9	40–44, 1–3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7 which are open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Alternate functions include:
P1.6	7	8	2	I/O	**SCL:** I^2C-bus serial port clock line.
P1.7	8	9	3	I/O	**SDA:** I^2C-bus serial port data line.
P2.0–P2.7	21–28	24–31	18–25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port
	11	13	7	O	**TxD (P3.1):** Serial output port
	12	14	8	I	**$\overline{INT0}$ (P3.2):** External interrupt
	13	15	9	I	**$\overline{INT1}$ (P3.3):** External interrupt
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{WR}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{RD}$ (P3.7):** External data memory read strobe
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{DD}.
ALE	30	33	27	I/O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency. Note that one ALE pulse is skipped during each access to external data memory.
$\overline{PSEN}$	29	32	26	O	**Program Store Enable:** Read strobe to external program memory via Port 0 and Port 2. It is activated twice each machine cycle during fetches from the external program memory. When executing out of external program memory two activations of $\overline{PSEN}$ are skipped during each access to external data memory. $\overline{PSEN}$ is not activated (remains HIGH) during no fetches from external program memory. $\overline{PSEN}$ can sink/source 8 LSTTL inputs and can drive CMOS inputs without external pull–ups.
$\overline{EA}$	31	35	29	I	**External Access:** If during a RESET, $\overline{EA}$ is held at TTL, level HIGH, the CPU executes out of the internal program memory ROM provided the Program Counter is less than 16384. If during a RESET, $\overline{EA}$ is held a TTL LOW level, the CPU executes out of external program memory. $\overline{EA}$ is not allowed to float.
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

NOTE:
To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than V_{DD} + 0.5V or V_{SS} – 0.5V, respectively.

CMOS single-chip 8-bit microcontroller with Electromagnetic Compatibility improvements

83CE654

DESCRIPTION

The 83CE654 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 83CE654 has the same instruction set as the 80C51. The 83CE654 has 16k bytes mask programmable ROM and 256 bytes RAM.

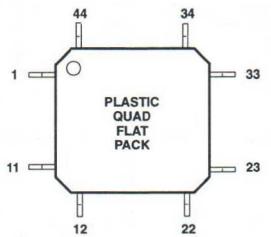
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 83CE654 contains a non-volatile 16k × 8 read-only program memory, a volatile 256 × 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 83CE654 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16MHz crystal, 58% of the instructions are executed in 0.75µs and 40% in 1.5µs. Multiply and divide instructions require 3µs.

FEATURES

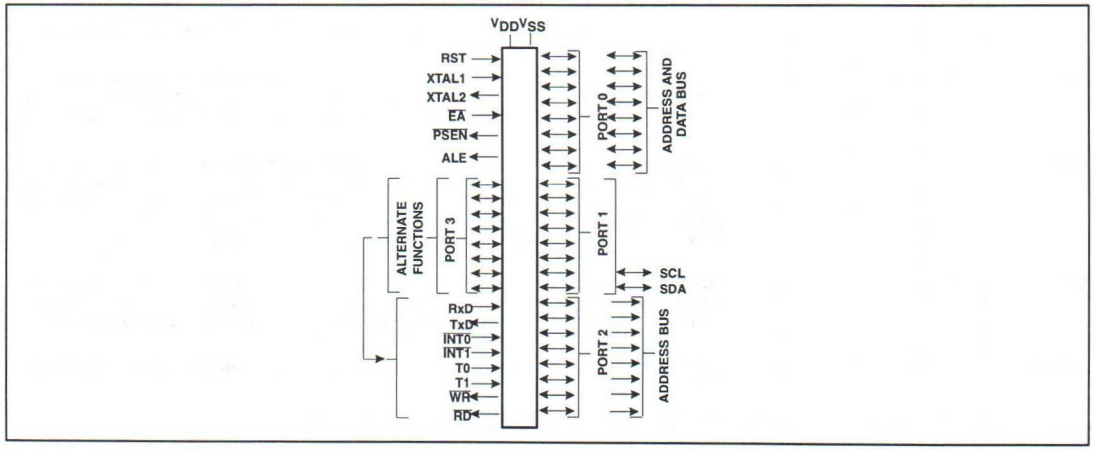
- 80C51 central processing unit
- 16k × 8 ROM expandable externally to 64k bytes
- 256 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- ROM code protection
- XTAL frequency range: 1.2MHz to 16MHz
- Software enable/disable of ALE output pulse
- Electromagnetic compatibility (EMC) improvements
- Operating ambient temperature range:
  - P83CE654 FBB T_{amb} 0°C to +70°C
  - P83CE654 FFB T_{amb} –40°C to +85°C

PIN CONFIGURATION



Pin	Function	Pin	Function
1	P1.5	23	P2.5/A13
2	P1.6/SCL	24	P2.6/A14
3	P1.7/SDA	25	P2.7/A15
4	RST	26	$\overline{PSEN}$
5	P3.0/RxD	27	ALE
6	V_{SS4}	28	V_{SS2}
7	P3.1/TxD	29	$\overline{EA}$
8	P3.2/$\overline{INT0}$	30	P0.7/AD7
9	P3.3/$\overline{INT1}$	31	P0.6/AD6
10	P3.4/T0	32	P0.5/AD5
11	P3.5/T1	33	P0.4/AD4
12	P3.6/$\overline{WR}$	34	P0.3/AD3
13	P3.7/$\overline{RD}$	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	V_{SS1}	38	V_{DD2}
17	V_{DD1}	39	V_{SS3}
18	P2.0/A8	40	P1.0
19	P2.1/A9	41	P1.1
20	P2.2/A10	42	P1.2
21	P2.3/A11	43	P1.3
22	P2.4/A12	44	P1.4

LOGIC SYMBOL



FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

ORDERING INFORMATION

ROM	TEMPERATURE RANGE °C AND PACKAGE	FREQUENCY MHz	DRAWING NUMBER
P83CE654FBB	0 to +70, Plastic Quad Flat Pack	1.2 to 16	SOT307-2[1]
P83CE654FFB	–40 to +85, Plastic Quad Flat Pack	1.2 to 16	SOT307-2[1]

NOTE:
1. SOT311 replaced by SOT307-2.

ELECTROMAGNETIC COMPATIBILITY (EMC) IMPROVEMENTS

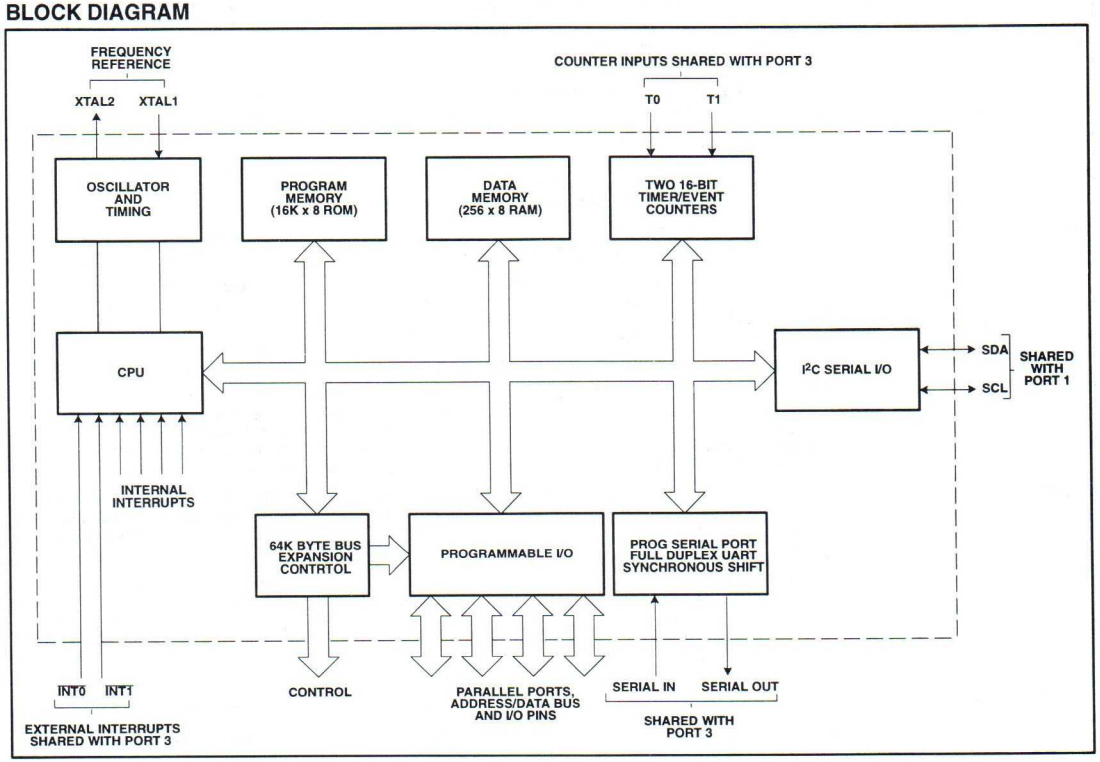
Primary attention is paid on the reduction of electromagnetic emission of the microcontroller P83CE654.

The following features effect in reducing the electromagnetic emission and additionally improve the electromagnetic susceptibility:

- Two supply voltage pins (V_{DD1}, V_{DD2}) and four ground pins (V_{SS1} to V_{SS4})
- Separate V_{DD} pins for the internal logic and the port buffers
- Internal decoupling capacitance improves the EMC radiation behavior and the EMC immunity
- External capacitors are to be located as close as possible between pins V_{DD2} and V_{SS3} as well as V_{DD1} and V_{SS1}; ceramic chip capacitors are recommended (100nF).
- The ALE output signal (pulses at a frequency of $f_{OSC}/6$) can be disabled under software control (bit 5 in the SFR PCON: "RFI"); if disabled, no ALE pulse will occur.

ALE pin will be pulled down internally, switching an external address latch to a quiet state. The MOVX instruction will still toggle ALE as a normal MOVX. ALE will retain its normal high value during Idle mode and a low value during Power-down mode while in the "RFI" reduction mode. Additionally during internal access ($\overline{EA}$ = 1) ALE will toggle normally when the address exceeds the internal program memory size. During external access ($\overline{EA}$ = 0) ALE will always toggle normally, whether the flag "RFI" is set or not.

BLOCK DIAGRAM



PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER	TYPE	NAME AND FUNCTION
V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4}	16, 28, 39, 6	I	**Ground:** 0V reference. All pins must be connected.
V_{DD1}, V_{DD2}	17, 38	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation. Both pins must be connected.
P0.0–0.7	37–30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 can sink/source 8 LSTTL inputs.
P1.0–P1.7	40–44, 1–3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7 which are open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 also receives the low-order address byte during program memory verification. Alternate functions include:
P1.6	2	I/O	**SCL:** I^2C-bus serial port clock line.
P1.7	3	I/O	**SDA:** I^2C-bus serial port data line.
P2.0–P2.7	18–25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	5, 7–13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	5	I	**RxD (P3.0):** Serial input port
	7	O	**TxD (P3.1):** Serial output port
	8	I	**$\overline{INT0}$ (P3.2):** External interrupt 0 or gate control input for timer/event counter 0
	9	I	**$\overline{INT1}$ (P3.3):** External interrupt 1 or gate control input for timer/event counter 1
	10	I	**T0 (P3.4):** Timer 0 external input
	11	I	**T1 (P3.5):** Timer 1 external input
	12	O	**$\overline{WR}$ (P3.6):** External data memory write strobe
	13	O	**$\overline{RD}$ (P3.7):** External data memory read strobe
RST	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal pull-down resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{DD}.
ALE	27	I/O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. ALE can sink/source 8 LSTTL inputs. It can drive CMOS inputs without an external pull-up. To prohibit the toggling of ALE pin (RFI noise reduction) the bit RFI in the PCON Register (PCON.5) must be set by software. This bit is cleared on RESET and can be cleared by software. When set, ALE pin will be pulled down internally, switching an external address latch to a quiet state. The MOVX instruction will still toggle ALE as a normal MOVX. ALE will retain its normal high value during Idle mode and a low value during Power-down mode while in the "RFI" mode. Additionally during internal access ($\overline{EA}$ = 1) ALE will toggle normally when the address exceeds the internal program memory size. During external access ($\overline{EA}$ = 0) ALE will always toggle normally, whether the flag "RFI" is set or not.
$\overline{PSEN}$	26	O	**Program Store Enable:** The read strobe to external program memory. When the 83CE654 is executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory. $\overline{PSEN}$ can sink/source 8 LSTTL inputs.
$\overline{EA}$	29	I	**External Access Enable:** when, during RESET, $\overline{EA}$ is held at a TTL HIGH level the CPU executes out of the internal program ROM, provided the program counter is less than 16384. When $\overline{EA}$ is held at a TTL LOW level during RESET, the CPU executes out of external program memory via Port 0 and Port 2. $\overline{EA}$ is not allowed to float.
XTAL1	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

NOTE:
To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher or lower than V_{DD} + 0.5V or V_{SS} – 0.5V, respectively.

8-bit microcontrollers with OSD and VST 84C44X; 84C64X; 84C84X

FEATURES

PCF84CXXXA kernel

- 8-bit CPU, ROM, RAM, I/O in a single 42 leads shrink DIL package
- Over 80 instructions all of 1 or 2 cycles
- 29 quasi bidirectional standard I/O port lines
- Configuration of I/O lines individually selected by mask
- External interrupt $\overline{INT}$/T0
- 2 direct testable inputs T0, T1
- 8-bit programmable timer/event counter
- 3 single level vectored interrupts (external, timer/counter, I²C-bus)
- Power-on-reset and low voltage detector
- Single power supply
- 2 power reduction modes: Idle and Stop
- Operating temperature range: –20 to +70 °C
- Silicon gate CMOS fabrication process (SAC2).

Derivative features PCA84C640

Although the **PCA84C640** is specifically referred to throughout this data sheet, the information applies to all the devices. The small differences between the 84C640 and the other devices are specified in the text.

The PCA84C640 comprises:

- The PCF84CXXXA processor core
- 6 kbytes mask-programmable program ROM
- 128 bytes RAM
- Multi-master I²C-bus interface
- AFC input for Voltage Synthesized Tuning (VST; with 3-bit DAC and comparator)
- On Screen Display (OSD) facility for two rows of 16-characters
- On Screen Display character set of 64 types
- Four programmable display dot sizes
- Half dot character rounding
- Seven colours for each character
- One 14-bit PWM output for VST
- Five 6-bit PWM outputs for analog controls
- Eight port lines with 10 mA LED drive capability
- 18 general purpose bidirectional I/O lines plus 11 function-combined I/O lines
- 2 direct testable lines
- Programmable VSYNCN and HSYNCN input polarity
- RC oscillator for OSD function.

GENERAL DESCRIPTION

The 84C44X; 84C64X; 84C84X denotes the types:

- PCA84C440; 84C441; 84C443; 84C444
- PCA84C640; 84C641; 84C643; 84C644
- PCA84C840; 84C841; 84C843; 84C844,

which are 8-bit microcontrollers with On Screen Display (OSD) and Voltage Synthesized Tuning (VST) functions. All are members of the 84CXXX microcontroller family.

There are two oscillator types for the OSD function in the various types, i.e.,

- RC oscillator: PCA84C440; 84C443; 84C640; 84C643; 84C840; 84C843
- LC oscillator: PCA84C441; 84C444; 84C641; 84C644; 84C841; 84C844.

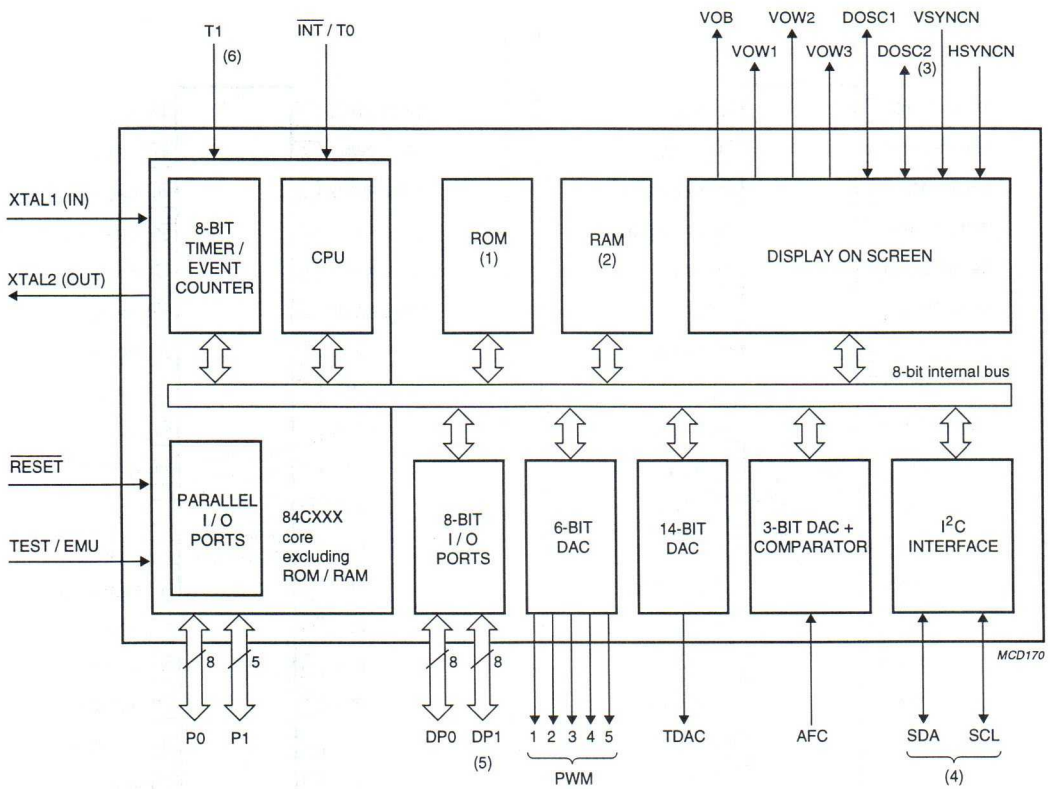
Important note

This data sheet details the specific properties of the PCA84C44X, PCA84C64X and PCA84C84X.
The shared characteristics of the PCA84CXXX family of microcontrollers are described in the PCF84CXXXA Family single-chip 8-bit Microcontroller of *"Data Handbook IC14"*, which should be read in conjunction with this data sheet.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE (°C)
	NAME	DESCRIPTION	VERSION	
PCA84C440; 84C443; 84C640; 84C643; 84C840; 84C843	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1	–20 to +70
PCA84C441; 84C444; 84C641; 84C644; 84C841; 84C844				

BLOCK DIAGRAM



(1) 4K bytes for the PCA84C440; 84C441; 84C443; 84C444.
6K bytes for the PCA84C640; 84C641; 84C643; 84C644.
8K bytes for the PCA84C840; 84C841; 84C843; 84C844.

(2) 128 bytes for the PCA84C440; 84C441; 84C443; 84C444; 84C640; 84C641; 84C643; 84C644.
192 bytes for the PCA84C840; 84C841; 84C843; 84C844.

(3) For use with an LC oscillator, only available with the:
PCA84C441; 84C444; 84C641; 84C644; 84C841; 84C844.

(4) I²C-bus interface not available with the:
PCA84C443; 84C444; 84C643; 84C644; 84C843; 84C844.

(5) DP1.4 only available for PCA84C440; 84C443; 84C640; 84C643; 84C840; 84C843.

(6) T1 = pin 29 for PCA84C440; 84C443; 84C640; 84C643; 84C840; 84C843.
T1 = pin 34 for PCA84C441; 84C444; 84C641; 84C644; 84C841; 84C844.

Fig.1 Block diagram.

PINNING INFORMATION

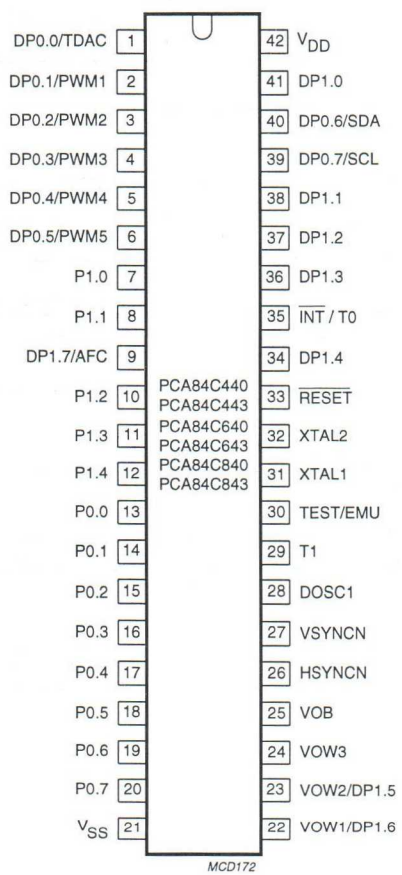


Fig.2 Pinning diagram for PCA84CX40; 84CX43.

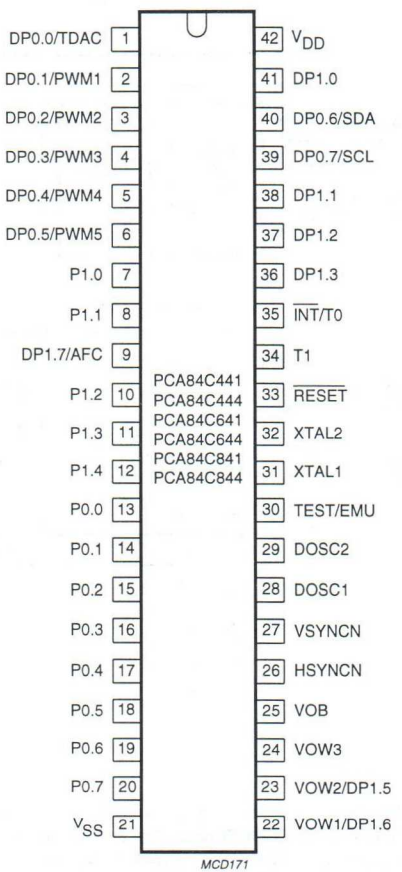


Fig.3 Pinning diagram for PCA84CX41; 84CX44.

Table 1 Pin description

SYMBOL[1]		PIN[1]		DESCRIPTION
84CX40; 84CX43	**84CX41; 84CX44**	**84CX40; 84CX43**	**84CX41; 84CX44**	
Deviating pinning				
DP1.0 to DP1.4	DP1.0 to DP1.3	41, 38, 37, 36, 34	41, 38, 37, 36	Derivative Port 1: quasi-bidirectional I/O lines.
T1	T1	29	34	Direct testable pin and event counter input.
DOSC1	–	28	–	Connection to RC oscillator of OSD clock.
–	DOSC1/DOSC2	–	28, 29	Connections to LC oscillator of OSD clock.
Mutual pinning				
DP0.0/TDAC		1		Derivative Port 0: quasi-bidirectional I/O line or 14-bit DAC PWM.
DP0.1 to DP0.5/PWM1 to PWM5		2 to 6		Derivative Port 1: quasi-bidirectional I/O lines or 6-bit DAC PWM.
P1.0 to P1.4		7, 8, 10, 12		Port 1: quasi-bidirectional I/O lines.
P0.0 to P0.7		13 to 20		Port 0: quasi-bidirectional I/O port.
DP1.7/AFC		9		Derivative Port 1: quasi-bidirectional I/O line or comparator input with 3-bit DAC.
DP0.6/SDA		40		Derivative open drain I/O port or I^2C-bus data line.
DP0.7/SCL		39		Derivative open drain I/O port or I^2C- bus clock line.
$\overline{INT}$/T0		35		External interrupt or direct testable line.
DP1.5 to DP1.6/VOW2 to VOW1		23, 22		Derivative Port 1: quasi-bidirectional I/O lines or character video output.
$\overline{RESET}$		33		Initialize input, active LOW.
XTAL2, XTAL1		32, 31		Oscillator output or input terminal for system clock.
TEST/EMU		30		Control input for testing and emulation mode. Ground for normal operation.
VSYNCN		27		Vertical synchronous signal input.
HSYNCN		26		Horizontal synchronous signal input.
VOB		25		Blanking output.
VOW3		24		Character video output of OSD.
V_{SS}		21		Ground.
V_{DD}		42		Power supply.

Note

1. **84CX40; 84CX43** denotes the types: PCA84C440, PCA84C443, PCA84C640, PCA84C643, PCA84C840 and PCA84C843.
   84CX41; 84CX44 denotes the types: PCA84C441, PCA84C444, PCA84C641, PCA84C644, PCA84C841 and PCA84C844.

DIFFERENCES BETWEEN THE TYPES

Table 2 Differences between the types PCA84C44X, PCA84C64X and PCA84C84X

In this table: yes = available; no = not available.

FEATURE	PCA...											
	84C440	**84C441**	**84C443**	**84C444**	**84C640**	**84C641**	**84C643**	**84C644**	**84C840**	**84C841**	**84C843**	**84C844**
OSD oscillator	RC	LC	RC	LC	RC	LC	RC	LC	RC	LC	RC	LC
General purpose I/O lines	18	17	18	17	18	17	18	17	18	17	18	17
I^2C-bus interface	yes	yes	no	no	yes	yes	no	no	yes	yes	no	no
ROM	4 kbytes				6 kbytes				8 kbytes			
RAM	128 bytes				128 bytes				192 bytes			
Pin assignment												
Pin 29	T1	DOSC2	T1	DOSC2	DP1.4	T1	DP1.4	T1	DP1.4	T1	DP1.4	T1
Pin 34	DP1.4	T1	DP1.4	T1	T1	DOSC2	T1	DOSC2	T1	DOSC2	T1	DOSC2
Register DP1 (bit DP1.4)												
Pin	yes	no	yes	no	yes	no	yes	no	yes	no	yes	no
Latch	yes	no	yes	no	yes	no	yes	no	yes	no	yes	no

CMOS single-chip 8-bit microcontroller 87C528

DESCRIPTION

The 87C528 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 87C528 has the same instruction set as the 80C51. Three versions of the derivative exist:

- 83C528—32k bytes mask programmable ROM
- 80C528—ROMless version of the 83C528
- 87C528—32k bytes EPROM

This device provides architectural enhancements that make it applicable in a variety of applications in consumer, telecom and general control systems, especially in those systems which need large ROM and RAM capacity on-chip.

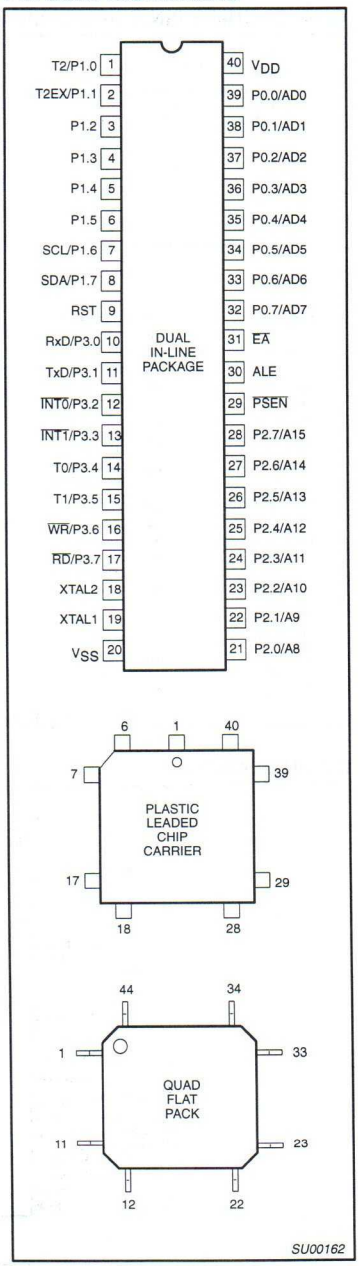
The 87C528 contains a 32k × 8 EPROM, a 512 × 8 RAM, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a 16-bit timer (identical to the timer 2 of the 80C52), a watchdog timer with a separate oscillator, a multi-source, two-priority-level, nested interrupt structure, two serial interfaces (UART and I²C-bus), and on-chip oscillator and timing circuits.

In addition, the 87C528 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

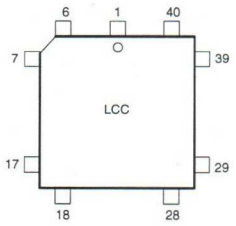
- 80C51 instruction set
  - 32k × 8 EPROM
  - 512 × 8 RAM
  - Memory addressing capability 64k ROM and 64k RAM
  - Three 16-bit counter/timers
  - On-chip watchdog timer with oscillator
  - Full duplex UART
  - I²C serial interface
- Power control modes:
  - Idle mode
  - Power-down mode
  - Warm start from power-down
- CMOS and TTL compatible
- Extended temperature ranges
- EPROM code protection
- OTP package available
- Two speed ranges at V_{CC} = 5V
  - 16MHz
  - 20MHz

PIN CONFIGURATIONS



FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

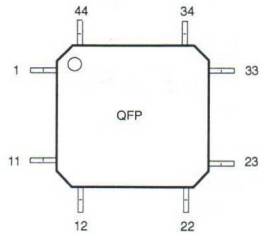
CERAMIC AND PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS



Pin	Function	Pin	Function
1	NC	23	NC
2	P1.0/T2	24	P2.0/A8
3	P1.1/T2EX	25	P2.1/A9
4	P1.2	26	P2.2/A10
5	P1.3	27	P2.3/A11
6	P1.4	28	P2.4/A12
7	P1.5	29	P2.5/A13
8	P1.6/SCL	30	P2.6/A14
9	P1.7/SDA	31	P2.7/A15
10	RST	32	$\overline{PSEN}$
11	P3.0/RxD	33	ALE
12	NC	34	NC
13	P3.1/TxD	35	$\overline{EA}$
14	P3.2/$\overline{INT0}$	36	P0.7/AD7
15	P3.3/$\overline{INT1}$	37	P0.6/AD6
16	P3.4/T0	38	P0.5/AD5
17	P3.5/T1	39	P0.4/AD4
18	P3.6/$\overline{WR}$	40	P0.3/AD3
19	P3.7/$\overline{RD}$	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	V_{SS}	44	V_{DD}

SU00163

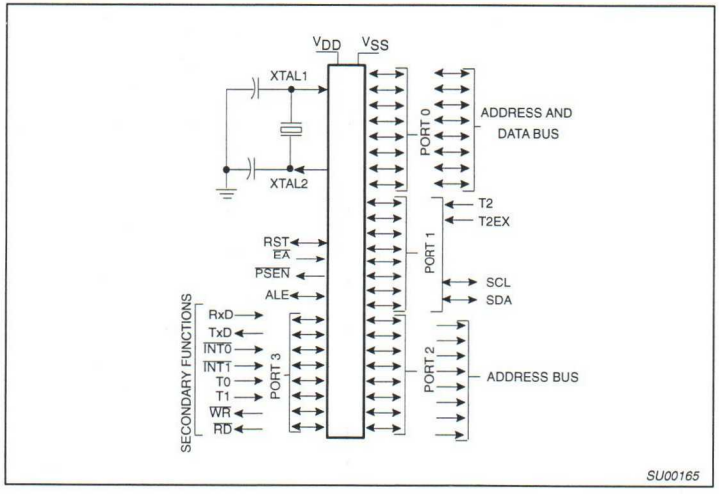
PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function
1	P1.5	23	P2.5/A13
2	P1.6/SCL	24	P2.6/A14
3	P1.7/SDA	25	P2.7/A15
4	RST	26	$\overline{PSEN}$
5	P3.0/RxD	27	ALE
6	NC	28	NC
7	P3.1/TxD	29	$\overline{EA}$
8	P3.2/$\overline{INT0}$	30	P0.7/AD7
9	P3.3/$\overline{INT1}$	31	P0.6/AD6
10	P3.4/T0	32	P0.5/AD5
11	P3.5/T1	33	P0.4/AD4
12	P3.6/$\overline{WR}$	34	P0.3/AD3
13	P3.7/$\overline{RD}$	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	V_{SS}	38	V_{DD}
17	NC	39	NC
18	P2.0/A8	40	P1.0/T2
19	P2.1/A9	41	P1.1/T2EX
20	P2.2/A10	42	P1.2
21	P2.3/A11	43	P1.3
22	P2.4/A12	44	P1.4

SU00164

LOGIC SYMBOL



SU00165

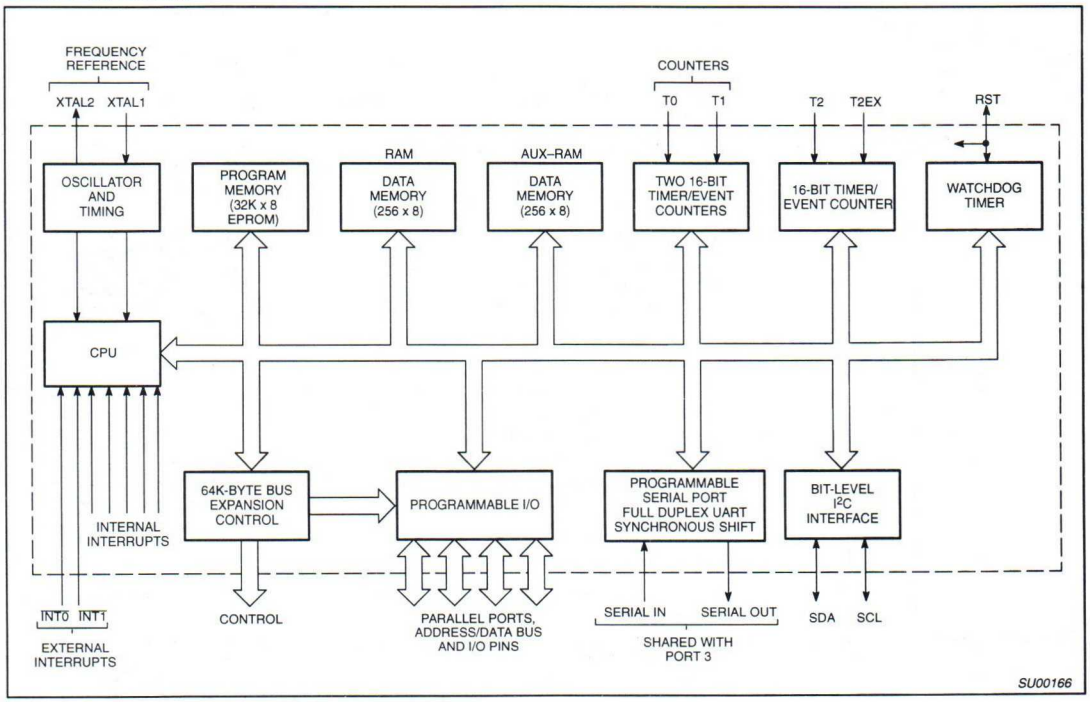
ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA PART ORDER NUMBER				
ROMless	ROM	ROMless	ROM	Drawing Number	TEMPERATURE °C RANGE AND PACKAGE	FREQ MHz
P80C528FBP	P83C528FBP/xxx	P80C528FBP N	P83C528FBP N	SOT129-1	0 to +70, Plastic Dual In-line Package	16
P80C528FBA	P83C528FBA/xxx	P80C528FBA A	P83C528FBA A	SOT187	0 to +70, Plastic Leaded Chip Carrier	16
P80C528FBB	P83C528FBB/xxx	P80C528FBB B	P83C528FBB B	SOT307-2[2]	0 to +70, Plastic Quad Flat Pack	16
P80C528FFP	P83C528FFP/xxx	P80C528FFP N	P83C528FFP N	SOT129-1	–40 to +85, Plastic Dual In-line Package	16
P80C528FFA	P83C528FFA/xxx	P80C528FFA A	P83C528FFA A	SOT187	–40 to +85, Plastic Leaded Chip Carrier	16
P80C528FFB	P83C528FFB/xxx	P80C528FFB B	P83C528FFB B	SOT307-2[2]	–40 to +85, Plastic Quad Flat Pack	16
P80C528FHP	P83C528FHP/xxx	P80C528FHP N	P83C528FHP N	SOT129-1	–40 to +125, Plastic Dual In-line Package	16
P80C528FHA	P83C528FHA/xxx	P80C528FHA A	P83C528FHA A	SOT187	–40 to +125, Plastic Leaded Chip Carrier	16
P80C528FHB	P83C528FHB/xxx	P80C528FHB B	P83C528FHB B	SOT307-2[2]	–40 to +125, Plastic Quad Flat Pack	16

NOTE:
1. xxx denotes the ROM code number.
2. SOT311 replaced by SOT307-2.

EPROM	Drawing Number	TEMPERATURE °C RANGE AND PACKAGE	FREQ MHz
P87C528EBP N	SOT129-1	0 to +70, Plastic Dual In-line Package	16
P87C528EBF FA	0590B	0 to +70, Ceramic Dual In-line Package w/Window	16
P87C528EBA A	0403G	0 to +70, Plastic Leaded Chip Carrier	16
P87C528EBL KA	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	16
P87C528EBB B	SOT307-2[2]	0 to +70, Plastic Quad Flat Pack	16
P87C528EFP N	SOT129-1	–40 to +85, Plastic Dual In-line Package	16
P87C528EFF FA	0590B	–40 to +85, Ceramic Dual In-line Package w/Window	16
P87C528EFA A	0403G	–40 to +85, Plastic Leaded Chip Carrier	16
P87C528EFL KA	1472A	–40 to +85, Ceramic Leaded Chip Carrier w/Window	16
P87C528EFB B	SOT307-2[2]	–40 to +85, Plastic Quad Flat Pack	16
P87C528GBP N	SOT129-1	0 to +70, Plastic Dual In-line Package	20
P87C528GBF FA	0590B	0 to +70, Ceramic Dual In-line Package w/Window	20
P87C528GBA A	0403G	0 to +70, Plastic Leaded Chip Carrier	20
P87C528GBL KA	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	20
P87C52GFP N	SOT129-1	–40 to +85, Plastic Dual In-line Package	20
P87C52GFF FA	0590B	0 to +70, Ceramic Dual In-line Package w/Window	20
P87C52GFA A	0403G	0 to +70, Plastic Leaded Chip Carrier	20
P87C52GFL KA	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	20

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO. DIP	PIN NO. LCC	PIN NO. QFP	TYPE	NAME AND FUNCTION
V_{SS}	20	22	16	I	**Ground:** circuit ground potential.
V_{DD}	40	44	38	I	**Power Supply:** +5V power supply pin during normal operation, Idle mode and Power-down mode.
P0.0–0.7	39–32	43–36	37–30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.
P1.0–P1.7	1–8	2–9	40–44 1–3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7 which have open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 can sink/source one TTL (4 LSTTL) inputs. Port 1 receives the low-order address byte during program memory verification. Port 1 also serves alternate functions for timer 2:
	1	2	40	I	**T2 (P1.0):** Timer/counter 2 external count input (following edge triggered).
	2	3	41	I	**T2EX (P1.1):** Timer/counter 2 trigger input.
	7	8	2	I/O	**SCL (P1.6):** I^2C serial port clock line.
	8	9	3	I/O	**SDA (P1.7):** I^2C serial port data line.
P2.0–P2.7	21–28	24–31	18–25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the SC80C51 family, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port
	11	13	7	O	**TxD (P3.1):** Serial output port
	12	14	8	I	**$\overline{INT0}$ (P3.2):** External interrupt
	13	15	9	I	**$\overline{INT1}$ (P3.3):** External interrupt
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{WR}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{RD}$ (P3.7):** External data memory read strobe
RST	9	10	4	I/O	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{DD}. After a watchdog timer overflow, this pin is pulled high while the internal reset signal is active.
ALE	30	33	27	I/O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory.
$\overline{PSEN}$	29	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
$\overline{EA}$	31	35	29	I	**External Access Enable:** $\overline{EA}$ must be externally held low during RESET to enable the device to fetch code from external program memory locations 0000H to 7FFFH. If $\overline{EA}$ is held high during RESET, the device executes from internal program memory unless the program counter contains an address greater than 7FFFH. $\overline{EA}$ is don't care after RESET.
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

CMOS single-chip 8-bit microcontroller 87C652

DESCRIPTION

The 87C652 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 87C652 has the same instruction set as the 80C51.

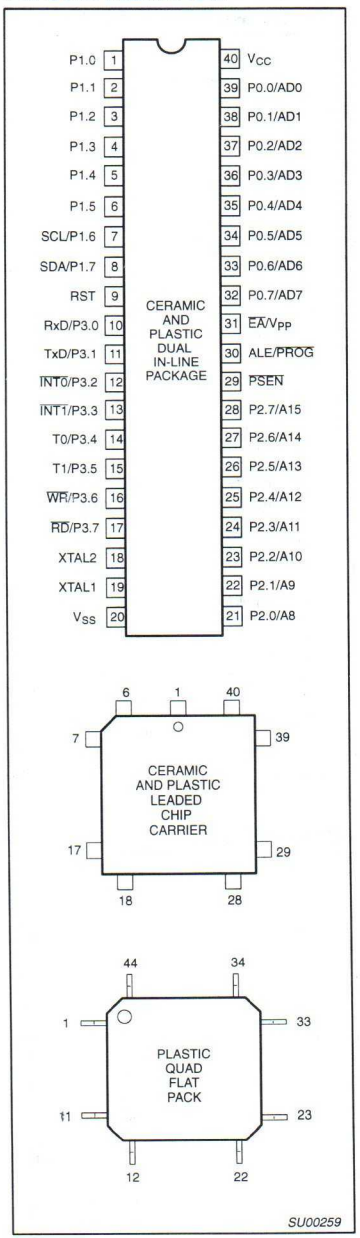
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 87C652 contains a non-volatile 8k × 8 EPROM, a volatile 256 × 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 87C652 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16MHz crystal, 58% of the instructions are executed in 0.75µs and 40% in 1.5µs. Multiply and divide instructions require 3µs.

FEATURES

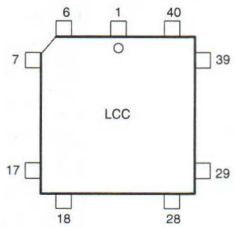
- 80C51 central processing unit
- 8k × 8 EPROM expandable externally to 64k bytes (EPROM is not expandable)
- 256 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- Power control modes
  - Idle mode
  - Power-down mode
- Five package styles
- Extended temperature range
- OTP package available
- Three speed ranges
  - 16MHz
  - 20MHz

PIN CONFIGURATION



FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

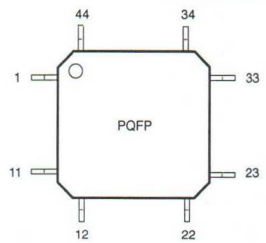
CERAMIC AND PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS



Pin	Function	Pin	Function
1	NC	23	NC
2	P1.0	24	P2.0/A8
3	P1.1	25	P2.1/A9
4	P1.2	26	P2.2/A10
5	P1.3	27	P2.3/A11
6	P1.4	28	P2.4/A12
7	P1.5	29	P2.5/A13
8	P1.6/SCL	30	P2.6/A14
9	P1.7/SDA	31	P2.7/A15
10	RST	32	$\overline{PSEN}$
11	P3.0/RxD	33	ALE/$\overline{PROG}$
12	NC	34	NC
13	P3.1/TxD	35	$\overline{EA}$/V_{PP}
14	P3.2/$\overline{INT0}$	36	P0.7/AD7
15	P3.3/$\overline{INT1}$	37	P0.6/AD6
16	P3.4/T0	38	P0.5/AD5
17	P3.5/T1	39	P0.4/AD4
18	P3.6/$\overline{WR}$	40	P0.3/AD3
19	P3.7/$\overline{RD}$	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	V_{SS}	44	V_{CC}

SU00260

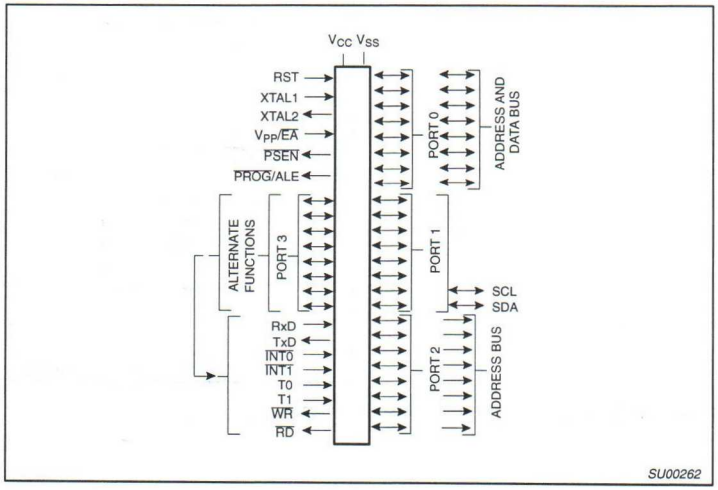
PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function
1	P1.5	23	P2.5/A13
2	P1.6/SCL	24	P2.6/A14
3	P1.7/SDA	25	P2.7/A15
4	RST	26	$\overline{PSEN}$
5	P3.0/RxD	27	ALE/$\overline{PROG}$
6	NC	28	NC
7	P3.1/TxD	29	$\overline{EA}$/V_{PP}
8	P3.2/$\overline{INT0}$	30	P0.7/AD7
9	P3.3/$\overline{INT1}$	31	P0.6/AD6
10	P3.4/T0	32	P0.5/AD5
11	P3.5/T1	33	P0.4/AD4
12	P3.6/$\overline{WR}$	34	P0.3/AD3
13	P3.7/$\overline{RD}$	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	V_{SS}	38	V_{CC}
17	NC	39	NC
18	P2.0/A8	40	P1.0
19	P2.1/A9	41	P1.1
20	P2.2/A10	42	P1.2
21	P2.3/A11	43	P.13
22	P2.4/A12	44	P1.4

SU00261

LOGIC SYMBOL



SU00262

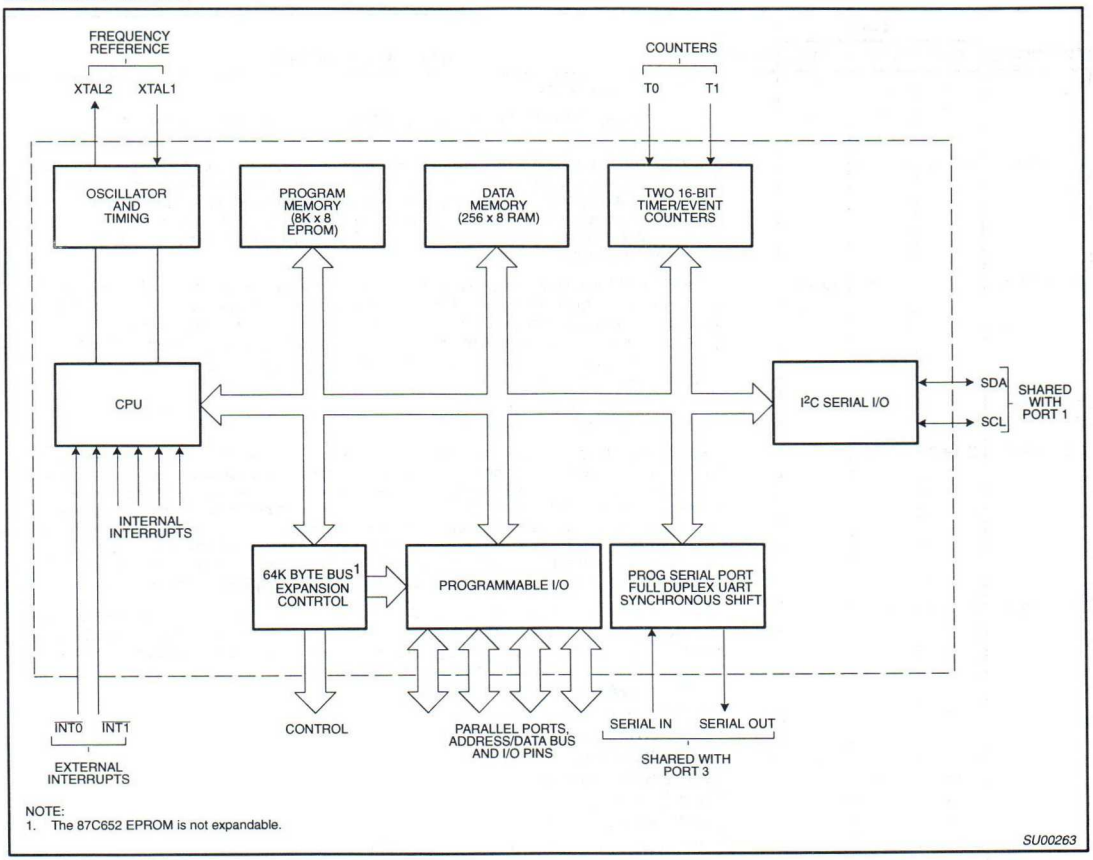
ORDER INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA PART ORDER NUMBER			TEMPERATURE RANGE (°C)	FREQ
ROMless	ROM	ROMless	ROM	Drawing Number	AND PACKAGE	MHz
P80C652FBP	P83C652FBP/xxx	P80C652FBPN	P83C652FBPN	SOT129-1	0 to +70, Plastic Dual In-line Package	16
P80C652FBA	P83C652FBA/xxx	P80C652FBAA	P83C652FBAA	SOT187	0 to +70, Plastic Leaded Chip Carrier	16
P80C652FBB	P83C652FBB/xxx	P80C652FBBB	P83C652FBBA	SOT307-2[5]	0 to +70, Plastic Quad Flat Pack	16
P80C652FFP	P83C652FFP/xxx	P80C652FFPN	P83C652FFPN	SOT129-1	–40 to +85, Plastic Dual In-line Package	16
P80C652FFA	P83C652FFA/xxx	P80C652FFAA	P83C652FFAA	SOT187	–40 to +85, Plastic Leaded Chip Carrier	16
P80C652FFB	P83C652FFB/xxx	P80C652FFBB	P83C652FFBB	SOT307-2[5]	–40 to +85, Plastic Quad Flat Pack	16
P80C652FHP	P83C652FHP/xxx	P80C652FHPN	P83C652FHPN	SOT129-1	–40 to +125, Plastic Dual In-line Package	16
P80C652FHA	P83C652FHA/xxx	P80C652FHAA	P83C652FHAA	SOT187	–40 to +125, Plastic Leaded Chip Carrier	16
P80C652FHB	P83C652FHB/xxx	P80C652FHBB	P83C652FHBB	SOT307-2[5]	–40 to +125, Plastic Quad Flat Pack	16
P80C652IBP	P83C652IBP/xxx	P80C652IBPN	P83C652IBPN	SOT129-1	0 to +70, Plastic Dual In-line Package	24
P80C652IBA	P83C652IBA/xxx	P80C652IBAA	P83C652IBAA	SOT187	0 to +70, Plastic Leaded Chip Carrier	24
P80C652IBB	P83C652IBB/xxx	P80C652IBBB	P83C652IBBB	SOT307-2[5]	0 to +70, Plastic Quad Flat Pack	24
P80C652IFP	P83C652IFP/xxx	P80C652IFPN	P83C652IFPN	SOT129-1	–40 to +85, Plastic Dual In-line Package	24
P80C652IFA	P83C652IFA/xxx	P80C652IFAA	P83C652IFAA	SOT187	–40 to +85, Plastic Leaded Chip Carrier	24
P80C652IFB	P83C652IFB/xxx	P80C652IFBB	P83C652IFBB	SOT307-2[5]	–40 to +85, Plastic Quad Flat Pack	24

NOTES:
1. 80C652 and 83C652 frequency range is 1.2MHz–16MHz or 1.2 to 24MHz.
2. 87C652 frequency range is 3.5MHz–16MHz or 3.5MHz–20MHz.
3. The 87C652 EPROM is not expandable.
4. xxx denotes the ROM code number.
5. SOT311 replaced by SOT307-2.

EPROM	Drawing Number	TEMPERATURE RANGE (°C) AND PACKAGE	FREQ MHz
S87C652-4N40	SOT129-1	0 to +70, Plastic Dual In-line Package	16
S87C652-4F40	0590B	0 to +70, Ceramic Dual In-line Package w/Window	16
S87C652-4A44	0403G	0 to +70, Plastic Leaded Chip Carrier	16
S87C652-4K44	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	16
S87C652-4B44	SOT307-2	0 to +70, Plastic Quad Flat Pack	16
S87C652-5N40	SOT129-1	–40 to +85, Plastic Dual In-line Package	16
S87C652-5F40	0590B	–40 to +85, Ceramic Dual In-line Package w/Window	16
S87C652-5A44	0403G	–40 to +85, Plastic Leaded Chip Carrier	16
S87C652-5K44	1472A	–40 to +85, Ceramic Leaded Chip Carrier w/Window	16
S87C652-5B44	SOT307-2	–40 to +85, Plastic Quad Flat Pack	16
S87C652-7N40	SOT129-1	0 to +70, Plastic Dual In-line Package	20
S87C652-7F40	0590B	0 to +70, Ceramic Dual In-line Package w/Window	20
S87C652-7A44	0403G	0 to +70, Plastic Leaded Chip Carrier	20
S87C652-7K44	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	20
S87C652-8N40	SOT129-1	–40 to +85, Plastic Dual In-line Package	20
S87C652-8F40	0590B	–40 to +85, Ceramic Dual In-line Package w/Window	20
S87C652-8A44	0403G	–40 to +85, Plastic Leaded Chip Carrier	20
S87C652-8K44	1472A	–40 to +85, Ceramic Leaded Chip Carrier w/Window	20

BLOCK DIAGRAM



NOTE:
1. The 87C652 EPROM is not expandable.

SU00263

PIN DESCRIPTION

MNEMONIC	PIN NO. DIP	PIN NO. LCC	PIN NO. QFP	TYPE	NAME AND FUNCTION
V_{SS}	20	22	16	I	**Ground:** 0V reference.
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	39–32	43–36	37–30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the 87C652. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	40–44, 1–3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7 which are open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 also receives the low-order address byte during program memory verification. Alternate functions include:
P1.6	7	8	2	I/O	**SCL:** I^2C-bus serial port clock line.
P1.7	8	9	3	I/O	**SDA:** I^2C-bus serial port data line.
P2.0–P2.7	21–28	24–31	18–25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port
	11	13	7	O	**TxD (P3.1):** Serial output port
	12	14	8	I	**$\overline{INT0}$ (P3.2):** External interrupt
	13	15	9	I	**$\overline{INT1}$ (P3.3):** External interrupt
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{WR}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{RD}$ (P3.7):** External data memory read strobe
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE/$\overline{PROG}$	30	33	27	I/O	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming.
$\overline{PSEN}$	29	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the 87C652 is executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
$\overline{EA}$/V_{PP}	31	35	29	I	**External Access Enable/Programming Supply Voltage:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 1FFFH. If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 1FFFH. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

NOTE:
To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than V_{CC} + 0.5V or V_{SS} – 0.5V, respectively.

CMOS single-chip 8-bit microcontroller — 87C654

DESCRIPTION

The 87C654 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 87C654 has the same instruction set as the 80C51. Two versions of the derivative exist:

83C654—16k bytes mask programmable ROM

87C654—EPROM version

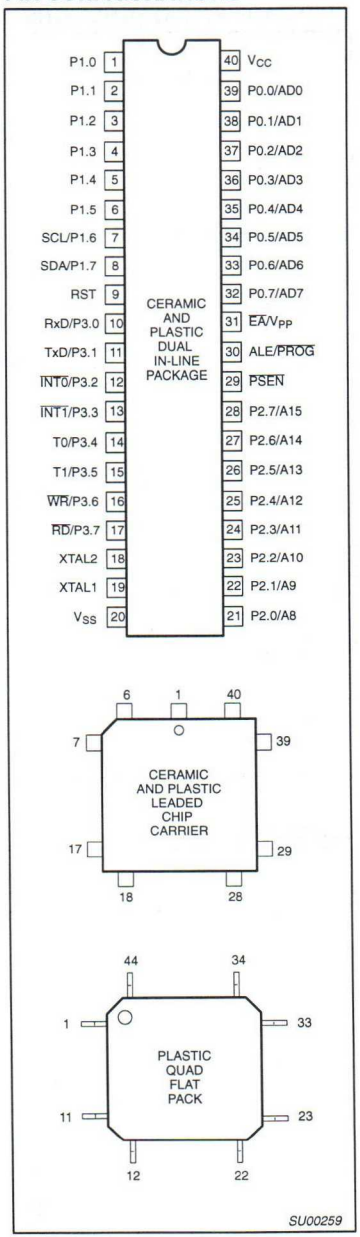
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 87C654 contains a non-volatile 16k × 8 EPROM, a volatile 256 × 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 87C654 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16MHz crystal, 58% of the instructions are executed in 0.75µs and 40% in 1.5µs. Multiply and divide instructions require 3µs.

FEATURES

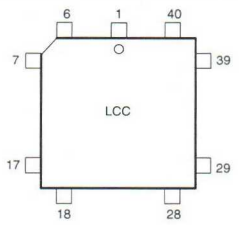
- 80C51 central processing unit
- 16k × 8 EPROM expandable externally to 64k bytes
- 256 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- Power control modes
  - Idle mode
  - Power-down mode
- Five package styles
- Extended temperature range
- OTP package available
- Three speed ranges
  - 16MHz
  - 20MHz

PIN CONFIGURATIONS



FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

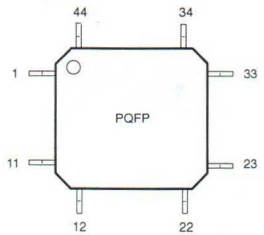
CERAMIC AND PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS



Pin	Function	Pin	Function
1	NC	23	NC
2	P1.0	24	P2.0/A8
3	P1.1	25	P2.1/A9
4	P1.2	26	P2.2/A10
5	P1.3	27	P2.3/A11
6	P1.4	28	P2.4/A12
7	P1.5	29	P2.5/A13
8	P1.6/SCL	30	P2.6/A14
9	P1.7/SDA	31	P2.7/A15
10	RST	32	$\overline{PSEN}$
11	P3.0/RxD	33	ALE/$\overline{PROG}$
12	NC	34	NC
13	P3.1/TxD	35	$\overline{EA}$/V_{PP}
14	P3.2/$\overline{INT0}$	36	P0.7/AD7
15	P3.3/$\overline{INT1}$	37	P0.6/AD6
16	P3.4/T0	38	P0.5/AD5
17	P3.5/T1	39	P0.4/AD4
18	P3.6/$\overline{WR}$	40	P0.3/AD3
19	P3.7/$\overline{RD}$	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	V_{SS}	44	V_{CC}

SU00260

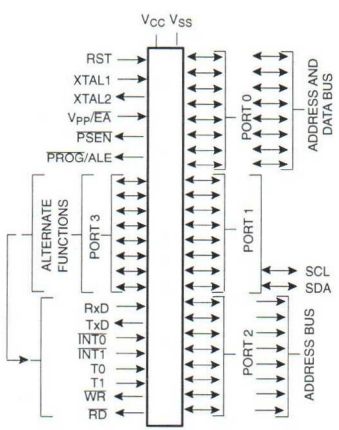
PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function
1	P1.5	23	P2.5/A13
2	P1.6/SCL	24	P2.6/A14
3	P1.7/SDA	25	P2.7/A15
4	RST	26	$\overline{PSEN}$
5	P3.0/RxD	27	ALE/$\overline{PROG}$
6	NC	28	NC
7	P3.1/TxD	29	$\overline{EA}$/V_{PP}
8	P3.2/$\overline{INT0}$	30	P0.7/AD7
9	P3.3/$\overline{INT1}$	31	P0.6/AD6
10	P3.4/T0	32	P0.5/AD5
11	P3.5/T1	33	P0.4/AD4
12	P3.6/$\overline{WR}$	34	P0.3/AD3
13	P3.7/$\overline{RD}$	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	V_{SS}	38	V_{CC}
17	NC	39	NC
18	P2.0/A8	40	P1.0
19	P2.1/A9	41	P1.1
20	P2.2/A10	42	P1.2
21	P2.3/A11	43	P.13
22	P2.4/A12	44	P1.4

SU00261

LOGIC SYMBOL



SU00262

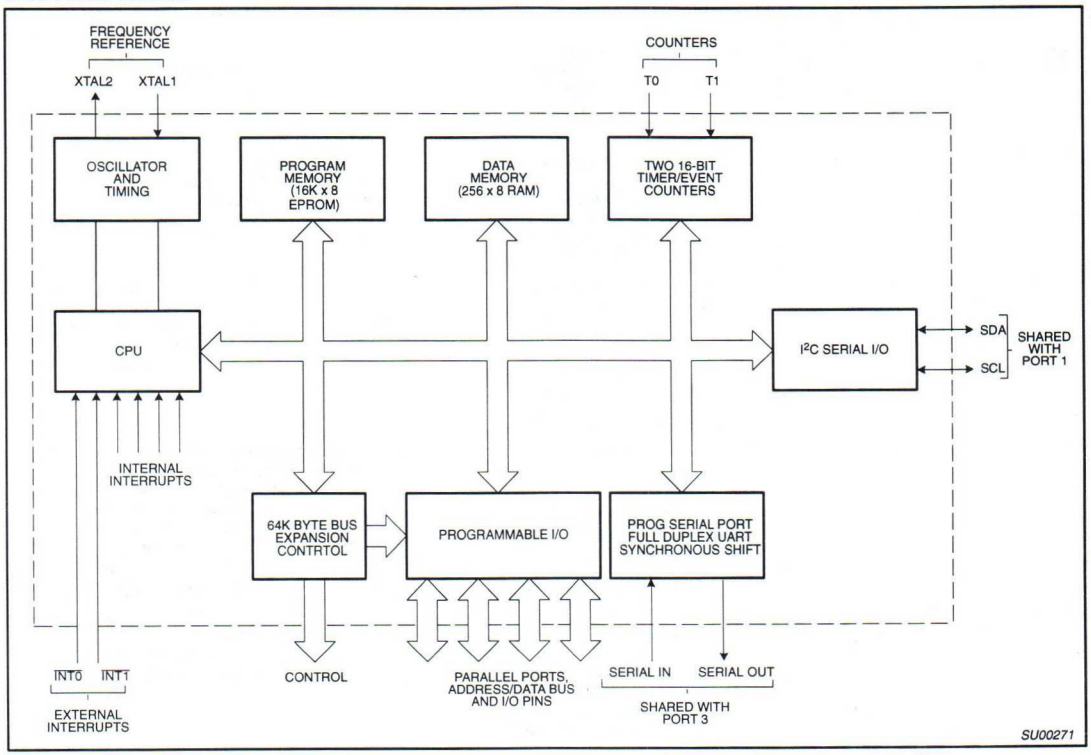
ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA PART ORDER NUMBER			TEMPERATURE RANGE °C AND PACKAGE	FREQ MHz
ROMless	ROM	ROMless	ROM	Drawing Number		
P80C652FBP	P83C654FBP/xxx	S80C652FBPN	S83C654FBPN	SOT129-1	0 to +70, Plastic Dual In-line Package	16
					0 to +70, Ceramic Dual In-line Package w/Window	16
P80C652FBA	P83C654FBA/xxx	S80C652FBAA	S83C654FBAA	SOT187	0 to +70, Plastic Leaded Chip Carrier	16
P80C652FBB	P83C654FBB/xxx	S80C652FBBB	S83C654FBBB	SOT307-2[4]	0 to +70, Plastic Quad Flat Pack	16
P80C652FFP	P83C654FFP/xxx	S80C652FFPN	S83C654FFPN	SOT129-1	–40 to +85, Plastic Dual In-line Package	16
P80C652FFA	P83C654FFA/xxx	S80C652FFAA	S83C654FFAA	SOT187	–40 to +85, Plastic Leaded Chip Carrier	16
P80C652FFB	P83C654FFB/xxx	S80C652FFBB	S83C654FFBB	SOT307-2[4]	–40 to +85, Plastic Quad Flat Pack	16
P80C652FHP	P83C654FHP/xxx	S80C652FHPN	S83C654FHPN	SOT129-1	–40 to +125, Plastic Dual In-line Package	16
P80C652FHA	P83C654FHA/xxx	S80C652FHAA	S83C654FHAA	SOT187	–40 to +125, Plastic Leaded Chip Carrier	16
P80C652FHB	P83C654FHB/xxx	S80C652FHBB	S83C654FHBB	SOT307-2[4]	–40 to +125, Plastic Quad Flat Pack	16
P80C652IBP	P83C654IBP/xxx	S80C652IBPN	S83C654IBPN	SOT129-1	0 to +70, Plastic Dual In-line Package	24
P80C652IBA	P83C654IBA/xxx	S80C652IBAA	S83C654IBAA	SOT187	0 to +70, Plastic Leaded Chip Carrier	24
P80C652IBB	P83C654IBB/xxx	S80C652IBBB	S83C654IBBB	SOT307-2[4]	0 to +70, Plastic Quad Flat Pack	24
P80C652IFP	P83C654IFP/xxx	S80C652IFPN	S83C654IFPN	SOT129-1	–40 to +85, Plastic Dual In-line Package	24
P80C652IFA	P83C654IFA/xxx	S80C652IFAA	S83C654IFAA	SOT187	–40 to +85, Plastic Leaded Chip Carrier	24
P80C652IFB	P83C654IFB/xxx	S80C652IFBB	S83C654IFBB	SOT307-2[4]	–40 to +85, Plastic Quad Flat Pack	24

NOTES:
1. For full specification, see the 87C652 data sheet.
2. 87C654 frequency range is 3.5MHz – 16MHz or 3.5MHz – 24MHz.
3. xxx denotes the ROM code number.
4. SOT311 replaced by SOT307-2.

EPROM	Drawing Number	TEMPERATURE RANGE °C AND PACKAGE	FREQ MHz
S87C654-4N40	SOT129-1	0 to +70, Plastic Dual In-line Package	16
S87C654-4F40	0590B	0 to +70, Ceramic Dual In-line Package w/Window	16
S87C654-4A44	0403G	0 to +70, Plastic Leaded Chip Carrier	16
S87C654-4K44	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	16
S87C654–4B44	SOT307-2	0 to +70, Plastic Quad Flat Pack	16
S87C654-5N40	SOT129-1	–40 to +85, Plastic Dual In-line Package	16
S87C654-5F40	0590B	–40 to +85, Ceramic Dual In-line Package w/Window	16
S87C654-5A44	0403G	–40 to +85, Plastic Leaded Chip Carrier	16
S87C654–5K44	1472A	–40 to +85, Ceramic Leaded Chip Carrier w/Window	16
S87C654-5B44	SOT307-2	–40 to +85, Plastic Quad Flat Pack	16
S87C654–7N40	SOT129-1	0 to +70, Plastic Dual In-line Package	20
S87C654–7F40	0590B	0 to +70, Ceramic Dual In-line Package w/Window	20
S87C654–7A44	0403G	0 to +70, Plastic Leaded Chip Carrier	20
S87C654–7K44	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	20
S87C654–8N40	SOT129-1	–40 to +85, Plastic Dual In-line Package	20
S87C654–8F40	0590B	–40 to +85, Ceramic Dual In-line Package w/Window	20
S87C654–8A44	0403G	–40 to +85, Plastic Leaded Chip Carrier	20

BLOCK DIAGRAM



PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER DIP	LCC	QFP	TYPE	NAME AND FUNCTION
V_{SS}	20	22	16	I	**Ground:** 0V reference.
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	39–32	43–36	37–30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the 87C654. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	40–44, 1–3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7 which are open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 also receives the low-order address byte during program memory verification. Alternate functions include:
P1.6	7	8	2	I/O	**SCL:** I^2C-bus serial port clock line.
P1.7	8	9	3	I/O	**SDA:** I^2C-bus serial port data line.
P2.0–P2.7	21–28	24–31	18–25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port
	11	13	7	O	**TxD (P3.1):** Serial output port
	12	14	8	I	**$\overline{INT0}$ (P3.2):** External interrupt
	13	15	9	I	**$\overline{INT1}$ (P3.3):** External interrupt
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{WR}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{RD}$ (P3.7):** External data memory read strobe
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE/$\overline{PROG}$	30	33	27	I/O	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming.
$\overline{PSEN}$	29	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the 87C654 is executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
$\overline{EA}/V_{PP}$	31	35	29	I	**External Access Enable/Programming Supply Voltage:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH. If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

NOTE:
To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than V_{CC} + 0.5V or V_{SS} – 0.5V, respectively.

UHF mixer diode | BA481

APPLICATIONS

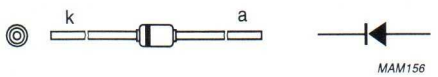
- Mixer applications in:
  - UHF tuners
  - Television modulators
  - RF detectors.

DESCRIPTION

Silicon epitaxial Schottky barrier diode encapsulated in the subminiature DO-34 (SOD68) glass envelope. The diode is suitable for mounting on a 2 E (5.08 mm) pitch.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_R	continuous reverse voltage		4	V
I_F	continuous forward current		30	mA
F	noise figure	f = 900 MHz	8	dB
T_j	junction temperature		100	°C



The BA481 is indicated by a grey band on the cathode side.

Fig.1 Simplified outline (SOD68; DO-34) and symbol.

Silicon planar diodes

BA482; BA483; BA484

FEATURES

- Low diode capacitance.

APPLICATIONS

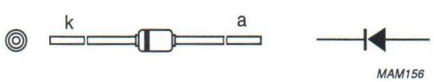
- Intended for band switching in VHF television tuners.

DESCRIPTION

Switching diodes in the subminiature DO-34 glass envelope. The diode is suitable for mounting on a 2 E (5.08 mm) pitch.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_R	continuous reverse voltage		–	35	V
I_F	continuous forward current		–	100	mA
C_d	diode capacitance	V_R = 3 V; f = 1 to 100 MHz			
	BA482		–	1.2	pF
	BA483		–	1	pF
	BA484		–	1.6	pF
r_D	diode series resistance	I_F = 3 mA; f = 200 MHz			
	BA482		–	0.7	Ω
	BA483		–	1.2	Ω
	BA484		–	1.2	Ω
r_D	diode series resistance	I_F = 10 mA; f = 200 MHz			
	BA482		0.4	–	Ω
	BA483		0.5	–	Ω
	BA484		0.5	–	Ω
T_j	junction temperature		–	150	°C



The marking band indicates the cathode.
The diodes are type branded.

Fig.1 Simplified outline (SOD68; DO-34) and symbol.

Silicon planar diode

BA582

FEATURES

- Low diode capacitance
- Low diode series resistance.

APPLICATIONS

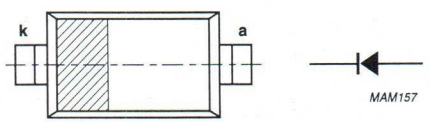
- Intended for low loss band switching in VHF television tuners.

DESCRIPTION

Silicon planar high performance band switching diode encapsulated in a micro-miniature plastic SOD123 package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_R	continuous reverse voltage		35	V
I_F	continuous forward current		100	mA
C_d	diode capacitance	V_R = 3 V; f = 1 to 100 MHz	1.1	pF
r_D	diode series resistance	I_F = 3 mA; f = 200 MHz	0.7	Ω
T_j	junction temperature		150	°C



Cathode indicated by a blue band.
Marking code: P.

Fig.1 Simplified outline (SOD123) and symbol.

Band-switching diodes for surface mounting

BA682; BA683

FEATURES

- Low diode capacitance
- Suitable for Automatic Placement and as such they can withstand immersion soldering.

APPLICATIONS

- Intended for band switching in VHF television tuners.

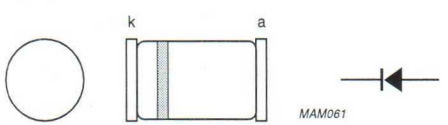
DESCRIPTION

Switching diodes in a SOD80 package. These SM diodes are leadless diodes in a hermetically sealed micro-miniature glass package with tin-plated metal discs at each end.

The diodes are delivered in 'super 8' tape.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_R	continuous reverse voltage		35	V
I_F	continuous forward current		100	mA
C_d	diode capacitance	V_R = 3 V; f = 1 MHz		
	BA682		1.25	pF
	BA683		1.2	pF
r_D	diode series resistance	I_F = 3 mA; f = 200 MHz		
	BA682		0.7	Ω
	BA683		1.2	Ω
r_D	diode series resistance	I_F = 10 mA; f = 200 MHz		
	BA682		0.5	Ω
	BA683		0.9	Ω
T_j	junction temperature		150	°C



The cathode is indicated by a red band.

Fig.1 Simplified outline (SOD80) and symbol.

Schottky barrier diode BAT17

APPLICATIONS

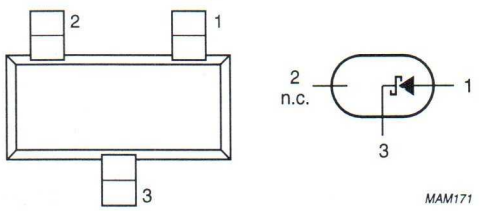
- Mixer and fast switching applications in thick and thin-film circuits.

DESCRIPTION

Silicon epitaxial Schottky barrier diode in a micro-miniature plastic SOT23 package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_R	continuous reverse voltage		4	V
I_F	continuous forward current		30	mA
V_F	forward voltage	I_F = 10 mA	600	mV
C_d	diode capacitance	V_R = 0 V; f = 1 MHz	1	pF
F	noise figure	f = 900 MHz	8	dB
T_j	junction temperature		100	°C



Marking code: A3p.

Fig.1 Simplified outline (SOT23) and symbol.

Silicon planar diode BAT18

APPLICATIONS

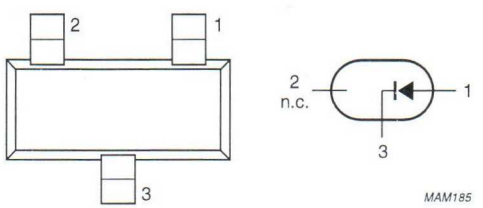
- Intended for thick and thin-film circuits.

DESCRIPTION

Band switching diode in a micro-miniature plastic SOT23 package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_R	continuous reverse voltage		–	35	V
I_F	continuous forward current		–	100	mA
T_j	junction temperature		–	100	°C
C_d	diode capacitance	V_R = 20 V; f = 1 MHz	0.8	1	pF
r_D	series resistance	I_F = 5 mA; f = 200 MHz	0.5	0.7	Ω



Marking code: A2.

Fig.1 Simplified outline (SOT23) and symbol.

Silicon variable capacitance diode BB119

APPLICATIONS

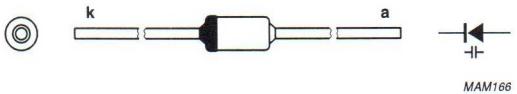
- Automatic frequency control in radio and television receivers.

DESCRIPTION

Planar-diffused diode in a DO-35 envelope.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	15	V
I_R	continuous reverse current	V_R = 15 V; T_j = 150 °C	–	2	μA
C_d	diode capacitance	V_R = 4 V; f = 1 MHz	20	25	pF
$\frac{C_{d(4\,V)}}{C_{d(10\,V)}}$	diode capacitance ratio	f = 300 MHz	1.3	–	
r_D	series resistance	V_R = 4 V; f = 200 MHz;	–	1.5	Ω
T_j	junction temperature		–	200	°C



The coloured band indicates the cathode.

Fig.1 Simplified outline (SOD27; DO-35) and symbol.

VHF variable capacitance diode — BB131

FEATURES

- Ultra small plastic SMD package.

APPLICATIONS

- As coupling diode in VHF tuners.

DESCRIPTION

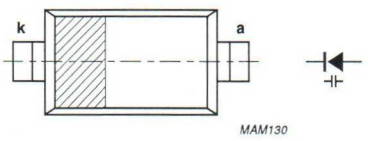
Silicon variable capacitance diode in planar technology, encapsulated in the ultra small SOD323 SMD plastic package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	continuous reverse current	V_R = 30 V	–	10	nA
C_d	diode capacitance	V_R = 0.5 V; f = 1 MHz	8	17	pF
		V_R = 28 V; f = 1 MHz	0.7	1.055	pF
$\frac{C_{d\,(0.5\ V)}}{C_{d\,(28\ V)}}$	diode capacitance ratio	f = 1 MHz	12	16	
r_s	series resistance	f = 470 MHz; note 1	–	3	Ω

Note

1. V_R is the value at which C_d = 9 pF.



Marking code: P1.

Fig.1 Simplified outline (SOD323) and symbol.

VHF variable capacitance diode — BB132

FEATURES

- Very high capacitance ratio
- Excellent matching performance
- Ultra small plastic SMD package.

APPLICATIONS

- In VHF tuners.

DESCRIPTION

Silicon variable capacitance diode in planar technology, encapsulated in the ultra small SOD323 SMD plastic package.

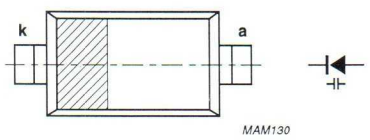
The excellent matching performance is achieved by a direct matching assembly procedure. The diodes are delivered on tape in several matched groups and are also available unmatched upon request.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	continuous reverse current	V_R = 30 V	–	10	nA
C_d	diode capacitance	V_R = 0.5 V; f = 1 MHz	60	75	pF
		V_R = 28 V; f = 1 MHz	2.3	2.75	pF
$\frac{C_{d\,(0.5\ V)}}{C_{d\,(28\ V)}}$	diode capacitance ratio	f = 1 MHz	24	30	
r_s	series resistance	f = 100 MHz; note 1	–	2	Ω

Note

1. V_R is the value at which C_d = 30 pF.



Marking code: P2.

Fig.1 Simplified outline (SOD323) and symbol.

VHF variable capacitance diode — BB133

FEATURES

- Very good linearity
- Excellent matching performance
- Ultra small plastic SMD package.

APPLICATIONS

- In VHF tuners with a CATV range up to 460 MHz.

DESCRIPTION

Silicon double implanted variable capacitance diode in planar technology, encapsulated in the ultra small SOD323 SMD plastic package.

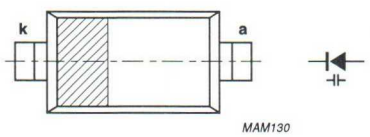
The excellent matching performance is achieved by a direct matching assembly procedure. The diodes are delivered on tape in several matched groups and are also available unmatched upon request.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	continuous reverse current	V_R = 30 V	–	10	nA
C_d	diode capacitance	V_R = 0.5 V; f = 1 MHz	38	46	pF
		V_R = 28 V; f = 1 MHz	2.2	2.6	pF
$\frac{C_{d\,(0.5\ V)}}{C_{d\,(28\ V)}}$	diode capacitance ratio	f = 1 MHz	14	21	
r_s	series resistance	f = 100 MHz; note 1	–	0.9	Ω

Note

1. V_R is the value at which C_d = 30 pF.



Marking code: P3.

Fig.1 Simplified outline (SOD323) and symbol.

UHF variable capacitance diode — BB134

FEATURES

- Very good linearity
- Excellent matching performance
- Ultra small plastic SMD package.

APPLICATIONS

- UHF tuners.

DESCRIPTION

Silicon double implanted variable capacitance diode in planar technology, encapsulated in the ultra small SOD323 plastic SMD package.

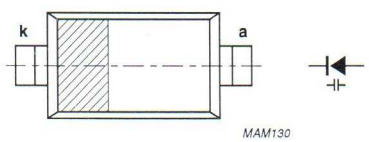
The excellent matching performance is achieved by a direct matching assembly procedure. The diodes are delivered on tape in several matched groups and are also available unmatched upon request.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	continuous reverse current	V_R = 30 V	–	10	nA
C_d	diode capacitance	V_R = 0.5 V; f = 1 MHz	17.5	21	pF
		V_R = 28 V; f = 1 MHz	1.7	2.1	pF
$\frac{C_{d\,(0.5\ V)}}{C_{d\,(28\ V)}}$	diode capacitance ratio	f = 1 MHz	8.9	12	
r_s	series resistance	f = 470 MHz; note 1	–	0.75	Ω

Note

1. V_R is the value at which C_d = 9 pF.



Marking code: P4.

Fig.1 Simplified outline (SOD323) and symbol.

UHF variable capacitance diode — BB135

FEATURES

- Very good linearity
- Ultra small plastic SMD package.

APPLICATIONS

- UHF tuners.

DESCRIPTION

Silicon double implanted variable capacitance diode in planar technology, encapsulated in the ultra small SOD323 SMD plastic package.

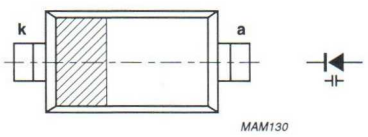
The diodes are delivered on tape (3000 or 10000 pieces), without gaps.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	continuous reverse current	V_R = 30 V	–	10	nA
C_d	diode capacitance	V_R = 0.5 V; f = 1 MHz	17.5	21	pF
		V_R = 28 V; f = 1 MHz	1.7	2.1	pF
$\frac{C_{d\,(0.5\ V)}}{C_{d\,(28\ V)}}$	diode capacitance ratio	f = 1 MHz	8.9	12	
r_s	series resistance	f = 470 MHz; note 1	–	0.75	Ω

Note

1. V_R is the value at which C_d = 9 pF.



Marking code: P5.

Fig.1 Simplified outline (SOD323) and symbol.

VHF variable capacitance diode BB148

FEATURES

- Very good linearity
- Excellent matching performance
- Ultra small plastic SMD package.

APPLICATIONS

- In VHF tuners with a CATV range up to 460 MHz.

DESCRIPTION

Silicon, double implanted variable capacitance diode in planar technology, encapsulated in the ultra small SOD323 SMD plastic package.

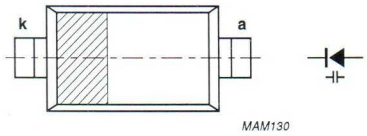
The excellent matching performance is achieved by a direct matching assembly procedure. The diodes are delivered on tape in several matched groups and are also available unmatched upon request.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	continuous reverse current	V_R = 30 V	–	10	nA
C_d	diode capacitance	V_R = 1 V; f = 1 MHz	36.8	41.8	pF
		V_R = 28 V; f = 1 MHz	2.4	2.75	pF
$\frac{C_{d(1\ V)}}{C_{d(28\ V)}}$	diode capacitance ratio	f = 1 MHz	14.5	–	
r_s	series resistance	f = 100 MHz; note 1	–	0.9	Ω

Note

1. V_R is the value at which C_d = 12 pF.



Marking code: P8

Fig.1 Simplified outline (SOD323) and symbol.

UHF variable capacitance diode — BB149

FEATURES

- Very good linearity
- Excellent matching performance
- Ultra small plastic SMD package.

APPLICATIONS

- In UHF tuners.

DESCRIPTION

Silicon, double implanted variable capacitance diode in planar technology, encapsulated in the ultra small SOD323 SMD plastic package.

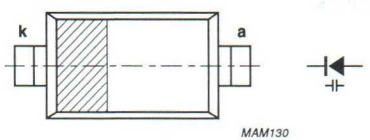
The excellent matching performance is achieved by a direct matching assembly procedure. The diodes are delivered on tape in several matched groups and are also available unmatched upon request.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	continuous reverse current	V_R = 30 V	–	10	nA
C_d	diode capacitance	V_R = 1 V; f = 1 MHz	18	19.5	pF
		V_R = 28 V; f = 1 MHz	1.9	2.25	pF
$\frac{C_{d(1\ V)}}{C_{d(28\ V)}}$	diode capacitance ratio	f = 1 MHz	8.2	10	
r_s	series resistance	f = 470 MHz; note 1	–	0.75	Ω

Note

1. V_R is the value at which C_d = 9 pF.



Marking code: P9.

Fig.1 Simplified outline (SOD323) and symbol.

VHF variable capacitance diode — BB150

FEATURES

- Very good linearity
- Ultra small plastic SMD package.

APPLICATIONS

- In VHF tuners with a CATV range up to 460 MHz.

DESCRIPTION

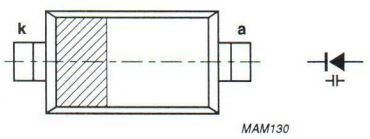
Silicon, double implanted variable capacitance diode in planar technology, encapsulated in the ultra small SOD323 SMD plastic package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	continuous reverse current	V_R = 30 V	–	10	nA
C_d	diode capacitance	V_R = 0.5 V; f = 1 MHz	38	46	pF
		V_R = 28 V; f = 1 MHz	2.2	2.6	pF
$\frac{C_{d\,(0.5\ V)}}{C_{d\,(28\ V)}}$	diode capacitance ratio	f = 1 MHz	14	21	
r_s	series resistance	f = 100 MHz; note 1	–	0.9	Ω

Note

1. V_R is the value at which C_d = 30 pF.



Marking code: P0.

Fig.1 Simplified outline (SOD323) and symbol.

UHF variable capacitance diode BB215

FEATURES

- Capacitance characteristic with a good linearity.

APPLICATIONS

- UHF tuners.

DESCRIPTION

Silicon variable capacitance diode in a hermetically sealed glass envelope (SOD80). The leadless SOD80 encapsulation is intended for surface mounting.

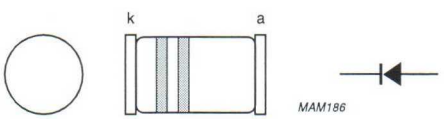
Diodes are supplied in matched sets and the capacitance difference between any two diodes in one set is less than 3% over the voltage range from 0.5 V to 28 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	reverse current	V_R = 28 V	–	10	nA
C_d	diode capacitance	V_R = 28 V; f = 500 kHz	1.8	2.2	pF
$\frac{C_{d\,(1\ V)}}{C_{d\,(28\ V)}}$	diode capacitance ratio	f = 500 kHz	7.6	–	
r_s	series resistance	f = 470 MHz; note 1	–	0.75	Ω

Note

1. V_R is the value at which C_d = 9 pF.



The cathode is indicated by a white band; a second green band indicates the BB215 type.

Fig.1 Simplified outline (SOD80) and symbol.

UHF variable capacitance diode | BB405B

FEATURES

- This miniature diode can be mounted on a 2 E (5.08 mm) pitch.

APPLICATIONS

- UHF tuners.

DESCRIPTION

Silicon variable capacitance diode in a hermetically sealed glass envelope.

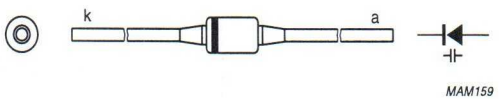
Diodes are supplied in matched sets and the capacitance difference between any two diodes in one set is less than 3% over the voltage range from 0.5 V to 28 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	reverse current	V_R = 28 V	–	10	nA
C_d	diode capacitance	V_R = 28 V; f = 500 kHz	1.8	2.2	pF
$\frac{C_{d(1\ V)}}{C_{d(28\ V)}}$	diode capacitance ratio	f = 500 kHz	7.6	–	
r_s	series resistance	f = 470 MHz; note 1	–	0.75	Ω

Note

1. V_R is the value at which C_d = 9 pF.



MAM159

The cathode is indicated by a white band on a black body.

Fig.1 Simplified outline (SOD68; DO-34) and symbol.

Variable capacitance diode BB417

APPLICATIONS

- Primarily intended for automatic frequency control in television receivers.

DESCRIPTION

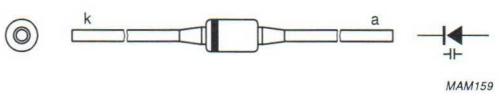
Silicon variable capacitance diode in a hermetically sealed glass DO-34 envelope.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	20	V
I_R	continuous reverse current	V_R = 20 V	–	100	nA
C_d	diode capacitance	f = 500 kHz; V_R = 15 V	2.2	4	pF
$\frac{C_{d(4\ V)}}{C_{d(15\ V)}}$	diode capacitance ratio		2	5	
r_D	series resistance	f = 470 MHz; note 1	–	1.2	Ω

Note

1. V_R is the value at which C_d = 9 pF.



Cathode indicated by a white band.

Fig.1 Simplified outline (SOD68; DO-34) and symbol.

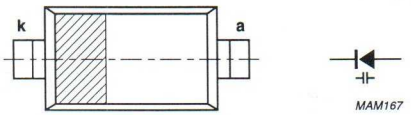
UHF variable capacitance diode BB515

APPLICATIONS

- UHF tuners.

DESCRIPTION

Silicon variable capacitance diode in a hermetically sealed glass envelope.



Marking code: P.
Cathode indicated by a white band.

Fig.1 Simplified outline (SOD123) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_R	continuous reverse voltage		–	–	30	V
I_R	reverse current	V_R = 30 V	–	–	10	nA
C_d	diode capacitance	V_R = 28 V; f = 1 MHz	1.85	–	2.25	pF
$\frac{C_{d\,(1\,V)}}{C_{d\,(28\,V)}}$	diode capacitance ratio	f = 1 MHz	8	–	9.6	
r_s	series resistance	f = 470 MHz; note 1	–	0.5	–	Ω

Note

1. V_R is the value at which C_d = 9 pF.

VHF variable capacitance diode BB619

FEATURES

- A very high capacitance ratio.

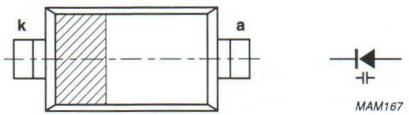
APPLICATIONS

- VHF-band B up to 460 MHz in all-band tuners.

DESCRIPTION

VHF variable capacitance diode in planar technology.

The diode is encapsulated in a hermetically sealed SOD123 plastic package suitable for surface mounting.



Marking code: P.
Cathode indicated by a yellow band.

Fig.1 Simplified outline (SOD123) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_R	continuous reverse voltage		–	–	30	V
I_R	continuous reverse current	V_R = 30 V	–	–	10	nA
C_d	diode capacitance	f = 1 MHz; V_R = 28 V	2.4	–	2.9	pF
$\frac{C_{d(1\ V)}}{C_{d(28\ V)}}$	diode capacitance ratio	f = 1 MHz	12.5	14	–	
r_s	diode series resistance	f = 100 MHz; note 1	–	0.7	–	Ω

Note

1. V_R is the value at which C_d = 30 pF.

VHF variable capacitance diode BB620

FEATURES

- A very high capacitance ratio.

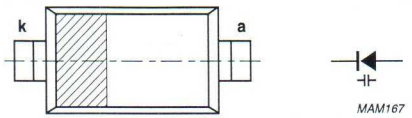
APPLICATIONS

- VHF-band A up to 160 MHz in all-band tuners.

DESCRIPTION

VHF variable capacitance diode in planar technology with a very high capacitance ratio.

The diode is encapsulated in a hermetically sealed SOD123 plastic package suitable for surface mounting.



Marking code: P.
Cathode indicated by a red band.

Fig.1 Simplified outline (SOD123) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_R	continuous reverse voltage		–	–	30	V
I_R	continuous reverse current	V_R = 30 V	–	–	10	nA
C_d	diode capacitance	f = 1 MHz; V_R = 28 V	2.9	–	3.4	pF
$\frac{C_{d(1\,V)}}{C_{d(28\,V)}}$	diode capacitance ratio	f = 1 MHz	19.5	–	25	
r_s	diode series resistance	f = 100 MHz; note 1	–	1.3	–	Ω

Note

1. V_R is the value at which C_d = 30 pF.

Silicon planar variable capacitance diode

BB809

APPLICATIONS

- Electronic tuning in VHF television tuners with extended band I (FCC and OIRT-norm).

DESCRIPTION

Variable capacitance diode in a miniature glass envelope.

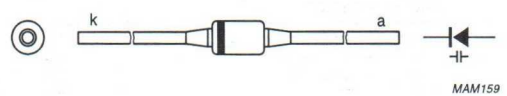
Diodes are supplied in matched sets (minimum 120 pieces and divisible by 12) and the capacitance difference between any two diodes in one set is less than 3% over the voltage range from 0.5 to 28 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	28	V
I_R	continuous reverse current	V_R = 28 V	–	10	nA
C_d	diode capacitance	f = 500 kHz; V_R = 1 V	39	46	pF
		f = 500 kHz; V_R = 28 V	4	5	pF
$\frac{C_{d\,(1\,V)}}{C_{d\,(28\,V)}}$	diode capacitance ratio	f = 500 kHz	8	10	
r_s	diode series resistance	f = 200 MHz; note 1	–	0.6	Ω

Note

1. V_R is the value at which C_d = 25 pF.



MAM159

Cathode indicated by a yellow band.

Fig.1 Simplified outline (SOD68) and symbol.

UHF variable capacitance diode — BB811

APPLICATIONS

- TV-SAT tuners up to 2 GHz.

DESCRIPTION

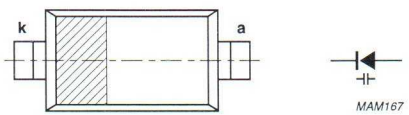
Silicon variable capacitance diode in a hermetically sealed SOD123 envelope.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	continuous reverse current	V_R = 30 V	–	20	nA
C_d	diode capacitance	V_R = 28 V; f = 1 MHz	0.85	1.2	pF
$\frac{C_{d(1\ V)}}{C_{d(28\ V)}}$	diode capacitance ratio	f = 1 MHz	7.8	9.5	
r_s	series resistance	f = 100 MHz; note 1	–	1.45	Ω

Note

1. V_R is the value at which C_d = 9 pF.



Marking code: T.
Cathode indicated by a white band.

Fig.1 Simplified outline (SOD123) and symbol.

Variable capacitance diode BB901

APPLICATIONS

- Intended as a tunable coupling diode in VHF all-band tuners.

DESCRIPTION

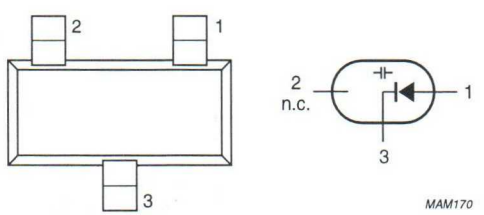
Silicon planar variable capacitance diode in a micro-miniature SOT23 envelope.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	28	V
I_R	continuous reverse current	V_R = 28 V	–	10	nA
C_d	diode capacitance	V_R = 28 V; f = 1 MHz	–	1.055	pF
$\frac{C_{d\,(0.5\ V)}}{C_{d\,(28\ V)}}$	diode capacitance ratio	f = 1 MHz	12	–	
r_s	series resistance	f = 100 MHz; note 1	–	3	Ω

Note

1. V_R is the value at which C_d = 10 pF.



Marking code: S14.

Fig.1 Simplified outline (SOT23) and symbol.

Silicon planar variable capacitance diode

BB909A; BB909B

APPLICATIONS

- Intended for electronic tuning in VHF television tuners for CATV applications.

DESCRIPTION

Silicon variable capacitance diode in planar technology, encapsulated in a DO-34 (SOD68) glass envelope.

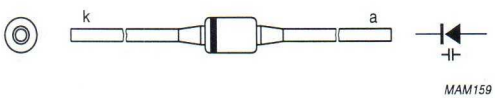
Diodes are supplied in matched sets (minimum 120 pieces and divisible by 12) and the capacitance difference between any two diodes in one set is less than 2.5% over the voltage range from 1 V to 28 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{RM}	peak reverse voltage		–	–	32	V
I_R	continuous reverse current	V_R = 28 V; T_{amb} = 25 °C	–	–	10	nA
C_d	diode capacitance	V_R = 1 V; f = 0.5 MHz				
	BB909A		31	–	–	pF
	BB909B		33.5	–	–	pF
C_d	diode capacitance	V_R = 28 V; f = 0.5 MHz				
	BB909A		2.6	–	3	pF
	BB909B		2.8	–	3.2	pF
$\frac{C_{d(1\,V)}}{C_{d(28\,V)}}$	diode capacitance ratio	f = 0.5 MHz	12	–	15	
r_s	diode series resistance	f = 100 MHz; note 1	–	0.7	0.9	Ω

Note

1. V_R is the value at which C_d = 30 pF.



MAM159

BB909B: green cathode ring; body black coloured.
BB909A: additional red band.

Fig.1 Simplified outline (SOD68; DO34) and symbol.

VHF variable capacitance diode — BB910

FEATURES

- A very high capacitance ratio.

APPLICATIONS

- VHF-band B up to 460 MHz in all-band tuners.

DESCRIPTION

VHF variable capacitance diode in planar technology.

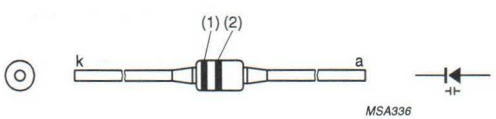
The diode is encapsulated in the whiskerless glass envelope SOD68.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{RM}	peak reverse voltage		–	32	V
I_R	continuous reverse current	V_R = 28 V	–	10	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0.5 V	38	–	pF
		f = 1 MHz; V_R = 28 V	2.3	2.7	pF
$\frac{C_{d\,(0.5\ V)}}{C_{d\,(28\ V)}}$	diode capacitance ratio	f = 1 MHz	14	–	
r_s	diode series resistance	f = 100 MHz; note 1	–	1	Ω

Note

1. V_R is the value at which C_d = 40 pF.



(1) Cathode type taping (on black body).
(2) Additional ring for type taping.

Fig.1 Simplified outline (SOD68) and symbol.

VHF variable capacitance diode BB911A

FEATURES

- Very high capacitance ratio.

APPLICATIONS

- In all-band tuners at VHF up to 160 MHz.

DESCRIPTION

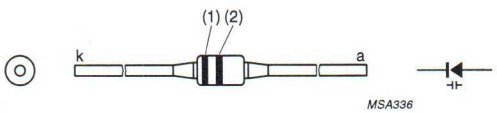
Silicon variable capacitance diode in planar technology, encapsulated in a SOD68 whiskerless glass envelope.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	30	V
I_R	continuous reverse current	V_R = 28 V	–	10	nA
C_d	diode capacitance	V_R = 0.5 V; f = 1 MHz	60	75	pF
		V_R = 28 V; f = 1 MHz	2.4	2.9	pF
$\frac{C_{d\,(0.5\ V)}}{C_{d\,(28\ V)}}$	diode capacitance ratio	f = 1 MHz	28.3	28.4	
r_s	series resistance	f = 100 MHz; note 1	–	2	Ω

Note

1. V_R is the value at which C_d = 40 pF.



(1) Cathode side: red ring on black body.
(2) Additional white ring.

Fig.1 Simplified outline (SOD68) and symbol.

Variable capacitance diode BBY31

APPLICATIONS

- Electronic tuning applications in thick and thin film circuits.

DESCRIPTION

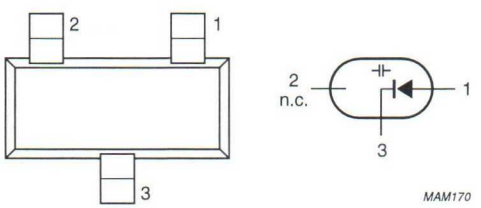
Silicon planar variable capacitance diode in a micro-miniature SOT23 package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_R	continuous reverse voltage		–	–	28	V
I_R	continuous reverse current	V_R = 28 V	–	–	10	nA
C_d	diode capacitance	V_R = 28 V; f = 1 MHz	1.6	–	2	pF
$\frac{C_{d(1\ V)}}{C_{d(28\ V)}}$	diode capacitance ratio	f = 1 MHz	–	8.3	–	
r_s	diode series resistance	f = 470 MHz; note 1	–	–	1.2	Ω

Note

1. V_R is the value at which C_d = 9 pF.



Marking code: S1.

Fig.1 Simplified outline (SOT23) and symbol.

Double variable capacitance diode BBY39

APPLICATIONS

- Electronic tuners in satellite TV systems.

DESCRIPTION

Double variable capacitance diode with a common cathode and mounted in a micro-miniature SOT23 package, suitable for surface mounting.

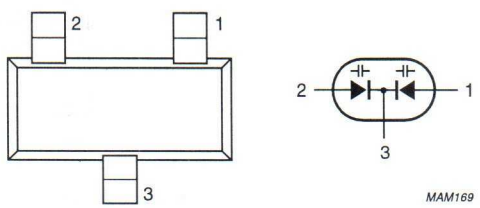
The two diodes in one package are matched.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per diode					
V_R	continuous reverse voltage		–	30	V
T_j	operating junction temperature		–	85	°C
I_R	continuous reverse current	V_R = 28 V	–	10	nA
C_d	diode capacitance	f = 1 MHz; V_R = 28 V	1.6	2	pF
$\frac{C_{d(1\ V)}}{C_{d(28\ V)}}$	diode capacitance ratio	f = 1 MHz	8	–	
r_s	diode series resistance	f = 470 MHz; note 1	–	1.2	Ω

Note

1. V_R is the value at which C_d = 9 pF.



Marking code: S12

Fig.1 Simplified outline (SOT23) and symbol.

Variable capacitance diode — BBY40

APPLICATIONS

- Electronic tuning in VHF television tuners with extended band I (FCC and OIRT norm).

DESCRIPTION

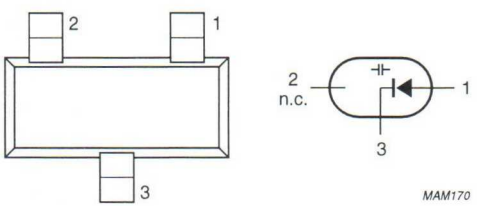
Variable capacitance diode in a plastic SOT23 package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_R	continuous reverse voltage		–	28	V
I_R	continuous reverse current	V_R = 28 V	–	10	nA
C_d	diode capacitance	V_R = 3 V; f = 1 MHz	26	32	pF
		V_R = 25 V; f = 1 MHz	4.3	6	pF
$\frac{C_{d\,(3\,V)}}{C_{d\,(25\,V)}}$	diode capacitance ratio	f = 1 MHz	5	6.5	
r_s	diode series resistance	f = 200 MHz; note 1	–	0.7	Ω

Note

1. V_R is the value at which C_d = 25 pF.



Marking code: S2.

Fig.1 Simplified outline (SOT23) and symbol.

VHF variable capacitance diode BBY42

APPLICATIONS

- VHF tuners and CATV applications using SMD technology.

DESCRIPTION

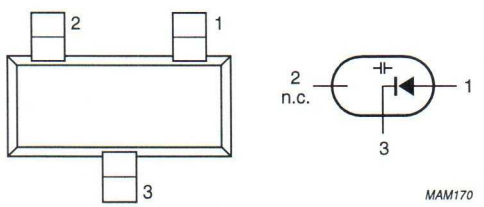
Variable capacitance diode in a micro-miniature plastic SOT23 package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{RM}	peak reverse voltage		–	–	32	V
I_R	continuous reverse current	V_R = 28 V	–	–	10	nA
C_d	diode capacitance	f = 1 MHz; V_R = 28 V	2.4	–	3	pF
$\frac{C_{d(1\ V)}}{C_{d(28\ V)}}$	diode capacitance ratio	f = 1 MHz	12	–	16	
r_s	diode series resistance	f = 100 MHz; note 1	–	0.9	1	Ω

Note

1. V_R is the value at which C_d = 30 pF.



Marking code: S13.

Fig.1 Simplified outline (SOT23) and symbol.

Double variable capacitance diode BBY62

APPLICATIONS

- Electronic tuners using SMD technology.

DESCRIPTION

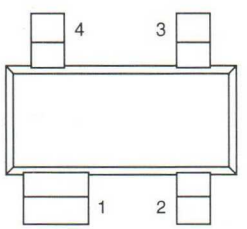
Double variable capacitance diode in a micro-miniature SOT143 package.

QUICK REFERENCE DATA

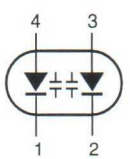
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per diode						
V_R	continuous reverse voltage		–	–	28	V
I_R	continuous reverse current	V_R = 28 V	–	–	10	nA
C_d	diode capacitance	V_R = 28 V; f = 1 MHz	1.6	–	2	pF
$\frac{C_{d(1\ V)}}{C_{d(28\ V)}}$	diode capacitance ratio	f = 1 MHz	–	8.3	–	
r_s	diode series resistance	f = 470 MHz; note 1	–	–	1.2	Ω

Note

1. V_R is the value at which C_d = 9 pF.



Top view



MAM172

Marking code: S4.

Fig.1 Simplified outline (SOT143) and symbol.

Silicon epitaxial transistors — BF420; BF422

APPLICATIONS

- Class-B video output stages in colour television and professional monitor equipment.

DESCRIPTION

NPN transistors in plastic TO-92 package.

PNP complements are BF421 and BF423.

PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BF420		–	300	V
	BF422		–	250	V
V_{CER}	collector-emitter voltage	R_{BE} = 2.7 kΩ			
	BF420		–	300	V
	BF422		–	–	V
V_{CEO}	collector-emitter voltage	open base			
	BF420		–	–	V
	BF422		–	250	V
I_{CM}	peak collector current		–	100	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	830	mW
h_{FE}	DC current gain	T_j = 25 °C; I_C = 25 mA; V_{CE} = 20 V	50	–	
f_T	transition frequency	f = 100 MHz; I_C = 10 mA; V_{CE} = 10 V	60	–	MHz
C_{re}	feedback capacitance	f = 1 MHz; I_C = 0; V_{CE} = 30 V	–	1.6	pF
T_j	junction temperature		–	150	°C

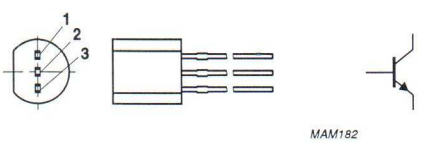


Fig.1 Simplified outline (TO-92) and symbol.

Silicon epitaxial transistors — BF421; BF423

APPLICATIONS

- Class-B video output stages in colour television and professional monitor equipment.

DESCRIPTION

PNP transistors in plastic TO-92 package.

NPN complements are BF420 and BF422.

PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BF421		–	–300	V
	BF423		–	–250	V
V_{CER}	collector-emitter voltage	R_{BE} = 2.7 kΩ			
	BF421		–	–300	V
	BF423		–	–	V
V_{CEO}	collector-emitter voltage	open base			
	BF421		–	–	V
	BF423		–	–250	V
I_{CM}	peak collector current		–	–100	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	830	mW
h_{FE}	DC current gain	T_j = 25 °C; I_C = –25 mA; V_{CE} = –20 V	50	–	
f_T	transition frequency	f = 100 MHz; I_C = –10 mA; V_{CE} = –10 V	60	–	MHz
C_{re}	feedback capacitance	f = 1 MHz; I_C = 0; V_{CE} = –30 V	–	1.6	pF
T_j	junction temperature		–	150	°C

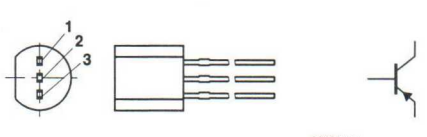


Fig.1 Simplified outline (TO-92) and symbol.

Silicon planar transistors for video output stages

BF457 to BF459

APPLICATIONS

- Video output stages in black-and-white and in colour television receivers.

DESCRIPTION

NPN transistors in a SOT32 plastic package.

PINNING

PIN	DESCRIPTION
1	emitter
2	collector; note 1
3	base

Note

1. Collector connected to mounting base

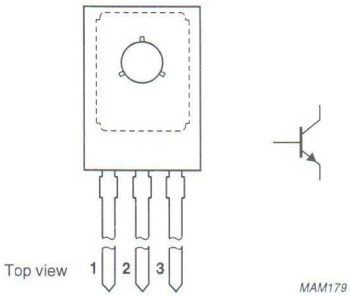


Fig.1 Simplified outline (TO-126; SOT32) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter				
	BF457		–	–	160	V
	BF458		–	–	250	V
	BF459		–	–	300	V
V_{CEO}	collector-emitter voltage	open base				
	BF457		–	–	160	V
	BF458		–	–	250	V
	BF459		–	–	300	V
I_{CM}	peak collector current		–	–	300	mA
P_{tot}	total power dissipation	T_{mb} = 90 °C	–	–	6	W
h_{FE}	DC current gain	T_j = 25 °C; I_C = 30 mA; V_{CE} = 10 V	26	–	–	
f_T	transition frequency	f = 100 MHz; I_C = 15 mA; V_{CE} = 10 V	–	90	–	MHz
C_{re}	feedback capacitance	f = 1 MHz; I_E = 0; V_{CB} = 30 V	–	–	3.5	pF
T_j	junction temperature		–	–	150	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC04 OR DATA SHEET

Silicon planar epitaxial transistors — BF469; BF471

APPLICATIONS

- Class-B video output stages in television receivers and high-voltage i.f. output stages.

DESCRIPTION

NPN transistors in plastic package.

PNP complements are BF470 and BF472 respectively.

PINNING

PIN	DESCRIPTION
1	emitter
2	collector; note 1
3	base

Note

1. Collector connected to mounting base.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BF469		–	250	V
	BF471		–	300	V
V_{CER}	collector-emitter voltage	R_{BE} = 2.7 kΩ			
	BF469		–	–	V
	BF471		–	300	V
V_{CEO}	collector-emitter voltage	open base			
	BF469		–	250	V
	BF471		–	–	V
I_{CM}	peak collector current		–	100	mA
P_{tot}	total power dissipation	$T_{mb} \leq 114$ °C	–	1.8	W
h_{FE}	DC current gain	I_C = 25 mA; V_{CE} = 20 V	50	–	
f_T	transition frequency	f = 100 MHz; I_C = 10 mA; V_{CE} = 10 V	60	–	MHz
C_{re}	feedback capacitance	f = 0.5 MHz; I_E = 0; V_{CB} = 30 V	–	1.8	pF
T_j	junction temperature		–	150	°C

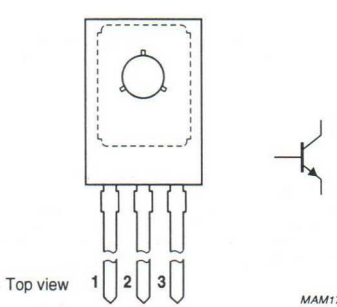


Fig.1 Simplified outline (TO-126; SOT32) and symbol.

Silicon planar epitaxial transistors — BF470; BF472

APPLICATIONS

- Class-B video output stages in television receivers and high-voltage i.f. output stages.

DESCRIPTION

PNP transistors in plastic package.

NPN complements are BF469 and BF471 respectively.

PINNING

PIN	DESCRIPTION
1	emitter
2	collector; note 1
3	base

Note

1. collector connected to mounting base.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BF470		–	–250	V
	BF472		–	–300	V
V_{CER}	collector-emitter voltage	R_{BE} = 2.7 kΩ			
	BF470		–	–	V
	BF472		–	–300	V
V_{CEO}	collector-emitter voltage	open base			
	BF470		–	–250	V
	BF472		–	–	V
I_{CM}	peak collector current		–	–100	mA
P_{tot}	total power dissipation	T_{mb} = 114 °C	–	1.8	W
h_{FE}	DC current gain	I_C = –25 mA; V_{CE} = –20 V	50	–	
f_T	transition frequency	f = 100 MHz; I_C = –10 mA; V_{CE} = –10 V	60	–	MHz
C_{re}	feedback capacitance	f = 0.5 MHz; I_E = 0; V_{CB} = –30 V	–	1.8	pF
T_j	junction temperature		–	150	°C

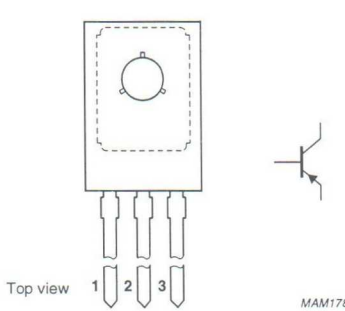


Fig.1 Simplified outline (TO-126; SOT32) and symbol.

Silicon planar epitaxial transistors — BF483; BF485; BF487

APPLICATIONS

- Video output stages in black-and-white and in colour television receivers.

DESCRIPTION

NPN transistors in TO-92 package.

PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BF483		–	300	V
	BF485		–	350	V
	BF487		–	400	V
V_{CEO}	collector-emitter voltage	open base			
	BF483		–	250	V
	BF485		–	300	V
	BF487		–	350	V
I_{CM}	peak collector current		–	100	mA
P_{tot}	total power dissipation	free air	–	830	mW
h_{FE}	DC current gain	I_C = 25 mA; V_{CE} = 20 V	50	–	
f_T	transition frequency	f = 100 MHz; I_E = −10 mA; V_{CB} = 10 V	70	110	MHz
T_j	junction temperature		–	150	°C

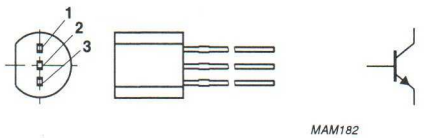


Fig.1 Simplified outline (TO-92) and symbol.

Silicon planar epitaxial transistors BF484; BF486; BF488

APPLICATIONS

- Video output stages of black-and-white and colour television receivers.

DESCRIPTION

PNP transistors in TO-92 package.

PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BF484		–	–250	V
	BF486		–	–300	V
	BF488		–	–350	V
V_{CEO}	collector-emitter voltage	open base			
	BF484		–	–250	V
	BF486		–	–300	V
	BF488		–	–350	V
I_{CM}	peak collector current		–	–100	mA
P_{tot}	total power dissipation	free air	–	830	mW
h_{FE}	DC current gain	I_C = –25 mA; V_{CE} = –20 V	50	–	
f_T	transition frequency	f = 100 MHz; I_C = –10 mA; V_{CE} = –10 V	70	110	MHz
T_j	junction temperature		–	150	°C

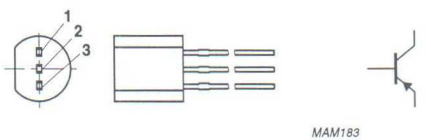


Fig.1 Simplified outline (TO-92) and symbol.

NPN 1 GHz wideband transistor BF547

FEATURES

- Feedback capacitance typ. 1 pF
- Stable oscillator operation
- High current gain
- Good thermal stability.

APPLICATIONS

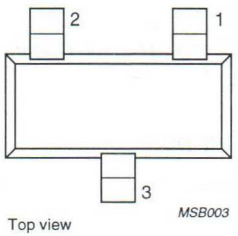
- It is intended for VHF and UHF TV-tuner applications
- Can be used as a mixer and/or oscillator.

DESCRIPTION

Low cost NPN transistor in a plastic SOT23 package.

PINNING

PIN	DESCRIPTION
1	base
2	emitter
3	collector



Top view

Marking code: E16.

Fig.1 SOT23.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{CEO}	collector-emitter voltage	open base	–	20	V
V_{CBO}	collector-base voltage	open emitter	–	30	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_{CM}	peak collector current		–	50	mA
P_{tot}	total power dissipation	up to T_s = 70 °C; note 1	–	300	mW
f_T	transition frequency	I_C = 15 mA; V_{CE} = 10 V; f = 500 MHz	1.2	1.6	GHz
C_{re}	feedback capacitance	$I_E = i_e$ = 0; V_{CB} = 10 V; f = 1 MHz	1	–	pF

Note

1. T_s is the temperature at the soldering point of the collector pin.

Silicon planar epitaxial transistors BF583; BF585; BF587

APPLICATIONS

- Video output stages in black-and-white and in colour television receivers.

DESCRIPTION

NPN transistors in TO-202 plastic package.

PINNING

PIN	DESCRIPTION
1	emitter
2	collector
3	base

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BF583		–	300	V
	BF585		–	350	V
	BF587		–	400	V
V_{CEO}	collector-emitter voltage	open base			
	BF583		–	250	V
	BF585		–	300	V
	BF587		–	350	V
I_{CM}	peak collector current		–	100	mA
P_{tot}	total power dissipation	free air	–	1.6	W
h_{FE}	DC current gain	I_C = 25 mA; V_{CE} = 20 V	50	–	
f_T	transition frequency	f = 100 MHz; I_E = −10 mA; V_{CB} = 10 V	70	110	MHz
T_j	junction temperature		–	150	°C

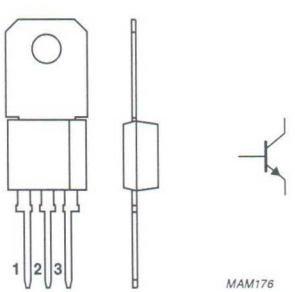


Fig.1 Simplified outline (TO-202) and symbol.

Silicon planar epitaxial transistors — BF584; BF586; BF588

APPLICATIONS

- Video output stages of black-and-white and colour television receivers.

DESCRIPTION

PNP transistors in TO-202 plastic package.

PINNING

PIN	DESCRIPTION
1	emitter
2	collector
3	base

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BF584		–	–250	V
	BF586		–	–300	V
	BF588		–	–350	V
V_{CEO}	collector-emitter voltage	open base			
	BF584		–	–250	V
	BF586		–	–300	V
	BF588		–	–350	V
I_{CM}	peak collector current		–	–100	mA
P_{tot}	total power dissipation	free air	–	1.6	W
h_{FE}	DC current gain	I_C = –25 mA; V_{CE} = –20 V	50	–	
f_T	transition frequency	f = 100 MHz; I_C = –10 mA; V_{CE} = –10 V	70	110	MHz
T_j	junction temperature		–	150	°C

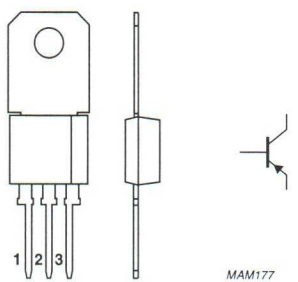


Fig.1 Simplified outline (TO-202) and symbol.

Silicon epitaxial transistors — BF720; BF722

APPLICATIONS

- Class-B video output stages in colour television receivers, and general purpose high voltage circuits.

DESCRIPTION

NPN transistors in a micro-miniature plastic package.

PNP complements are BF721 and BF723 respectively.

PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter
4	collector

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BF720		–	300	V
	BF722		–	250	V
V_{CER}	collector-emitter voltage	R_{BE} = 2.7 kΩ			
	BF720		–	300	V
	BF722		–	–	V
V_{CEO}	collector-emitter voltage	open base			
	BF720		–	–	V
	BF722		–	250	V
I_{CM}	peak collector current		–	100	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	1.5	W
h_{FE}	DC current gain	I_C = 25 mA; V_{CE} = 20 V	50	–	
f_T	transition frequency	f = 100 MHz; I_C = 10 mA; V_{CE} = 10 V	60	–	MHz
C_{re}	feedback capacitance	f = 1 MHz; I_C = 0; V_{CE} = 30 V	–	1.6	pF
T_j	junction temperature		–	150	°C

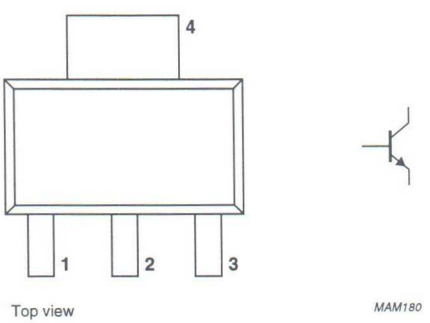


Fig.1 Simplified outline (SOT223) and symbol.

Silicon epitaxial transistors BF721; BF723

APPLICATIONS

- Class-B video output stages in colour television receivers
- General purpose high voltage circuits.

DESCRIPTION

PNP transistors in a micro-miniature plastic package.

NPN complements are BF720 and BF722 respectively.

PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter
4	collector

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BF721		–	–300	V
	BF723		–	–250	V
V_{CER}	collector-emitter voltage	R_{BE} = 2.7 kΩ			
	BF721		–	–300	V
	BF723		–	–	V
V_{CEO}	collector-emitter voltage	open base			
	BF721		–	–	V
	BF723		–	–250	V
I_{CM}	peak collector current		–	–100	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	1.5	W
h_{FE}	DC current gain	I_C = –25 mA; V_{CE} = –20 V	50	–	
f_T	transition frequency	f = 100 MHz; I_C = –10 mA; V_{CE} = –10 V	60	–	MHz
C_{re}	feedback capacitance	f = 1 MHz; I_C = 0; V_{CE} = –30 V	–	1.6	pF
T_j	junction temperature		–	150	°C

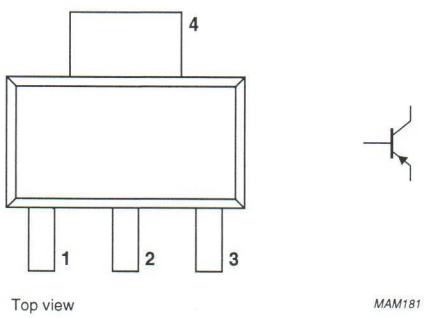


Fig.1 Simplified outline (SOT223) and symbol.

NPN 1 GHz wideband transistor BF747

FEATURES

- Feedback capacitance typ. 0.5 pF
- Stable oscillator operation
- High current gain
- Good thermal stability.

APPLICATIONS

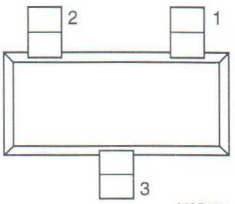
- It is intended for VHF and UHF TV-tuner applications
- Can be used as a mixer and/or oscillator.

DESCRIPTION

Low cost NPN transistor in a plastic SOT23 package.

PINNING

PIN	DESCRIPTION
1	base
2	emitter
3	collector



Top view

Marking code: E15.

Fig.1 SOT23.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{CEO}	collector-emitter voltage	open base	–	20	V
V_{CBO}	collector-base voltage	open emitter	–	30	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_{CM}	peak collector current		–	50	mA
P_{tot}	total power dissipation	up to T_s = 70 °C; note 1	–	300	mW
f_T	transition frequency	I_C = 15 mA; V_{CE} = 10 V; f = 500 MHz	1.2	1.6	GHz
C_{re}	feedback capacitance	$I_E = i_e$ = 0; V_{CB} = 10 V; f = 1 MHz	0.5	–	pF

Note

1. T_s is the temperature at the soldering point of the collector pin.

Silicon planar transistors for video output stages

BF857 to BF859

APPLICATIONS

- Video output stages in black-and-white and in colour television receivers.

DESCRIPTION

NPN transistors in a TO-202 plastic package. An A-version is available on request, it has ebc pinning instead of ecb.

PINNING

PIN	DESCRIPTION
BF857; BF858; BF859	
1	emitter
2	collector; note 1
3	base
BF857A; BF858A; BF859A	
1	emitter
2	base
3	collector; note 1

Note

1. Collector connected to mounting base.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter				
	BF857		–	–	160	V
	BF858		–	–	250	V
	BF859		–	–	300	V
V_{CEO}	collector-emitter voltage	open base				
	BF857		–	–	160	V
	BF858		–	–	250	V
	BF859		–	–	300	V
I_{CM}	peak collector current		–	–	300	mA
P_{tot}	total power dissipation	T_{mb} = 75 °C	–	–	6	W
h_{FE}	DC current gain	I_C = 30 mA; V_{CE} = 10 V	26	–	–	
f_T	transition frequency	f = 100 MHz; I_C = 15 mA; V_{CE} = 10 V	–	90	–	MHz
C_{re}	feedback capacitance	f = 1 MHz; I_E = 0; V_{CB} = 30 V	–	–	3	pF
T_j	junction temperature		–	–	150	°C

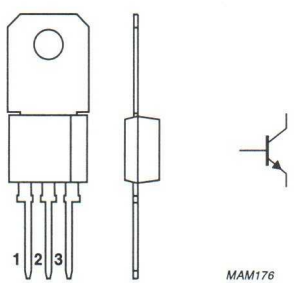


Fig.1 Simplified outline (TO-202) and symbol.

Silicon planar video output transistors

BF869; BF871

APPLICATIONS

- Class-B video output stages in colour television receivers.

DESCRIPTION

NPN transistors in a TO-202 plastic package.

PNP complements are BF870 and BF872.

PINNING

PIN	DESCRIPTION
1	emitter
2	collector; note 1
3	base

Note

1. Collector connected to mounting base.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BF869		–	250	V
	BF871		–	300	V
V_{CER}	collector-emitter voltage	R_{BE} = 2.7 kΩ			
	BF869		–	–	V
	BF871		–	300	V
V_{CEO}	collector-emitter voltage	open base			
	BF869		–	250	V
	BF871		–	–	V
I_{CM}	peak collector current		–	100	mA
P_{tot}	total power dissipation	T_{mb} = 25 °C	–	5	W
h_{FE}	DC current gain	I_C = 25 mA; V_{CE} = 20 V; T_j = 25 °C	50	–	
f_T	transition frequency	f = 100 MHz; I_E = –10 mA; V_{CB} = 10 V	60	–	MHz
C_{re}	feedback capacitance	f = 1 MHz; I_E = 0; V_{CB} = 30 V	–	2	pF
T_j	junction temperature			150	°C

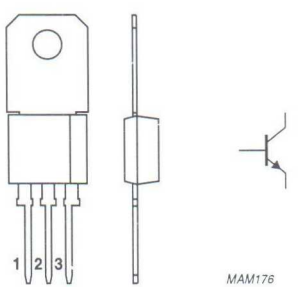


Fig.1 Simplified outline (TO-202) and symbol.

Silicon planar video output transistors

BF870; BF872

APPLICATIONS

- Class-B video output stages in colour television receivers.

DESCRIPTION

PNP transistors in a TO-202 plastic package.

NPN complements are BF869 and BF871.

PINNING

PIN	DESCRIPTION
1	emitter
2	collector; note 1
3	base

Note

1. Collector connected to mounting base.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BF870		–	–250	V
	BF872		–	–300	V
V_{CER}	collector-emitter voltage	R_{BE} = 2.7 kΩ			
	BF870		–	–	V
	BF872		–	–300	V
V_{CEO}	collector-emitter voltage	open base			
	BF870		–	–250	V
	BF872		–	–	V
I_{CM}	peak collector current		–	–100	mA
P_{tot}	total power dissipation	T_{mb} = 25 °C	–	5	W
h_{FE}	DC current gain	I_C = –25 mA; V_{CE} = –20 V; T_j = 25 °C	50	–	
f_T	transition frequency	f = 100 MHz; I_E = 10 mA; V_{CB} = –10 V	60	–	MHz
C_{re}	feedback capacitance	f = 1 MHz; I_E = 0; V_{CB} = –30 V	–	2.2	pF
T_j	junction temperature			150	°C

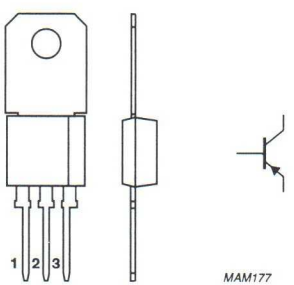


Fig.1 Simplified outline (TO-202) and symbol.

Dual-gate MOS-FET

BF904; BF904R

FEATURES

- Specially designed for use at 5 V supply voltage
- Short channel transistor with high $|Y_{fs}|$: C_{is} ratio
- Low-noise gain-controlled amplifier to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- UHF and VHF applications, such as television tuners and professional communications equipment.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

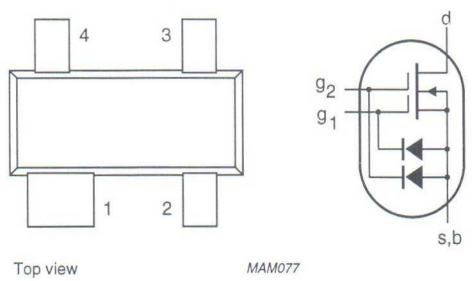
DESCRIPTION

Enhancement type field-effect transistors in plastic micro-miniature SOT143 and SOT143R envelopes.

These transistors consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

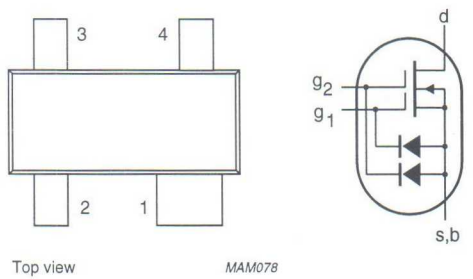
PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source, bias
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MO4.

Fig.1 Simplified outline (SOT143) and symbol.



Marking code: MO6.

Fig.2 Simplified outline (SOT143R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–	7	V
I_D	drain current (DC)		–	–	30	mA
P_{tot}	total power dissipation		–	–	200	mW
$\|Y_{fs}\|$	forward transfer admittance		22	25	30	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1		–	2.2	2.6	pF
C_{rs}	feedback capacitance		–	25	35	pF
F	noise figure	f = 800 MHz	–	2	–	dB
T_j	operating junction temperature		–	–	150	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

Silicon N-channel dual-gate MOS-FET BF960

APPLICATIONS

- UHF applications in television tuners and professional communications equipment.

DESCRIPTION

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source, bias
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

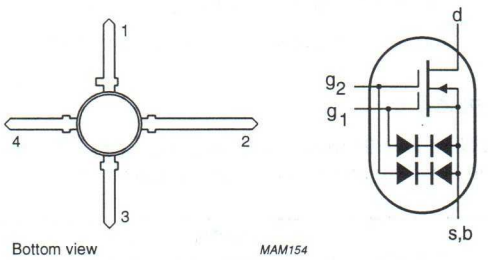


Fig.1 Simplified outline (SOT103) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
I_D	drain current (DC)		–	20	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C	–	225	mW
$\lvert Y_{fs} \rvert$	forward transfer admittance	f = 1 kHz; I_D = 7 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	12	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz; I_D = 7 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	1.8	–	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 7 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	25	–	fF
F	noise figure	G_S = 2 mS; B_S = B_{Sopt}; I_D = 7 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	2.8	–	dB
T_j	operating junction temperature		–	150	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

Silicon N-channel dual-gate MOS-FET BF964S

APPLICATIONS

- VHF applications in television tuners. The device is also suitable for use in professional communications equipment.

DESCRIPTION

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source, bias
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

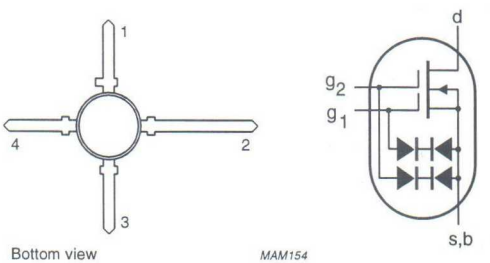


Fig.1 Simplified outline (SOT103) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
I_D	drain current (DC)		–	30	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C	–	225	mW
$\lvert y_{fs} \rvert$	forward transfer admittance	f = 1 kHz; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	18	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	2.5	3	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	25	–	fF
F	noise figure	G_S = 2 mS; $B_S = B_{Sopt}$; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	1	–	dB
T_j	operating junction temperature		–	150	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

Silicon N-channel dual-gate MOS-FET — BF966S

APPLICATIONS

- UHF applications in television tuners and professional communications equipment.

DESCRIPTION

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source, bias
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

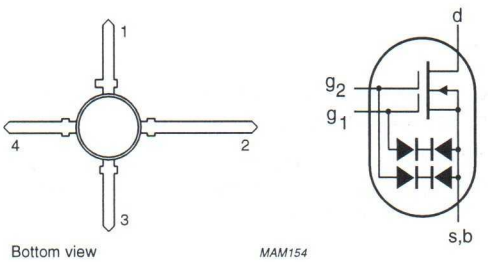


Fig.1 Simplified outline (SOT103) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
I_D	drain current (DC)		–	30	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C	–	225	mW
$\lvert Y_{fs} \rvert$	forward transfer admittance	f = 1 kHz; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	18	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	2.3	2.6	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	25	–	fF
F	noise figure	G_S = 3.3 mS; B_S = B_{Sopt}; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	1.8	–	dB
T_j	operating junction temperature		–	150	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

Silicon N-channel dual-gate MOS-FET BF980A

APPLICATIONS

- UHF applications such as UHF television tuners with 12 V supply voltage and professional communications equipment.

DESCRIPTION

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

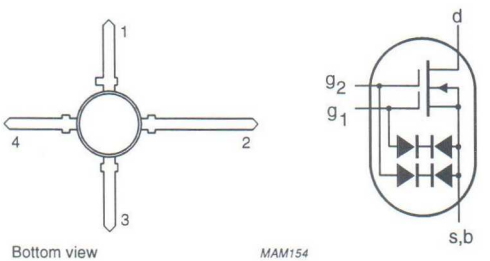


Fig.1 Simplified outline (SOT103) and symbol.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source, bias
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	18	V
I_D	drain current (DC)		–	30	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C	–	225	mW
$\lvert Y_{fs} \rvert$	forward transfer admittance	f = 1 kHz; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	19	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	2.6	3	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	25	–	fF
F	noise figure	G_S = 5 mS; $B_S = B_{Sopt}$; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	2	–	dB
T_j	operating junction temperature		–	150	°C

Silicon N-channel dual-gate MOS-FET BF981

APPLICATIONS

- VHF applications such as VHF television tuners, FM tuners and professional communications equipment.

DESCRIPTION

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source, bias
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

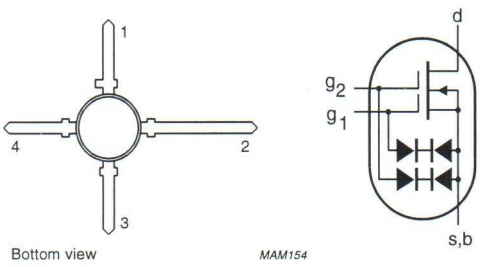


Fig.1 Simplified outline (SOT103) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
I_D	drain current (DC)		–	20	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C	–	225	mW
$\lvert Y_{fs} \rvert$	forward transfer admittance	f = 1 kHz; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	14	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	2.1	–	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	20	–	fF
F	noise figure	G_S = 1 mS; $B_S = B_{Sopt}$; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; f = 100 MHz	0.7	–	dB
T_j	operating junction temperature		–	150	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

Silicon N-channel dual-gate MOS-FET BF982

APPLICATIONS

- VHF applications such as VHF television tuners and FM tuners with 12 V supply voltage.

DESCRIPTION

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source, bias
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

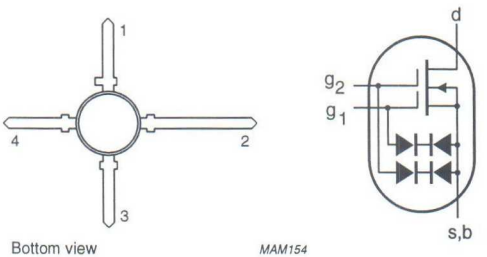


Fig.1 Simplified outline (SOT103) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
I_D	drain current (DC)		–	40	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C	–	225	mW
$\lvert Y_{fs} \rvert$	forward transfer admittance	f = 1 kHz; I_D = 15 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	25	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz; I_D = 15 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	4	–	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 15 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	30	–	fF
F	noise figure	G_S = 2 mS; B_S = B_{Sopt}; I_D = 15 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	1.2	–	dB
T_j	operating junction temperature		–	150	°C

Silicon N-channel dual-gate MOS-FET

BF988

FEATURES

- Short channel transistor with high $|Y_{fs}|$: C_{is} ratio
- Low-noise gain-controlled amplifier to 1 GHz.

APPLICATIONS

- VHF and UHF applications such as television tuners with 12 V supply voltage, and professional communications equipment.

DESCRIPTION

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source, bias
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

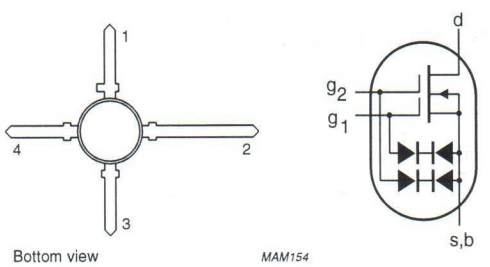


Fig.1 Simplified outline (SOT103) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)	–	12	V
I_D	drain current (DC)	–	30	mA
P_{tot}	total power dissipation	–	225	mW
$\|Y_{fs}\|$	forward transfer admittance	24	–	mS
C_{ig1-s}	input capacitance at gate 1	2.1	–	pF
C_{rs}	feedback capacitance	25	–	fF
F	noise figure	1	–	dB
T_j	operating junction temperature	–	150	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

Silicon N-channel dual-gate MOS-FET BF989

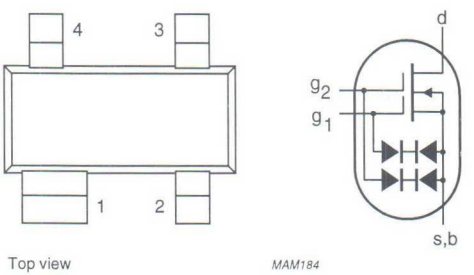
APPLICATIONS

- UHF applications in television tuners. The device is also suitable for use in professional communications equipment.

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 micro-miniature envelope with source and substrate interconnected.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.



Marking code: MAp.

Fig.1 Simplified outline (SOT143) and symbol.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source, bias
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
I_D	drain current (DC)		–	20	mA
P_{tot}	total power dissipation	T_{amb} = 60 °C	–	200	mW
$\lvert Y_{fs} \rvert$	forward transfer admittance	f = 1 kHz; I_D = 7 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	12	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz; I_D = 7 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	1.8	–	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 7 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	25	–	fF
F	noise figure	G_S = 2mS; B_S = B_{Sopt}; I_D = 7 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	2.8	–	dB
T_j	operating junction temperature		–	150	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

Silicon N-channel dual-gate MOS-FET — BF990A

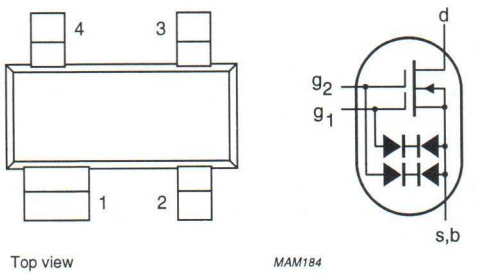
APPLICATIONS

- UHF applications such as television tuners with 12 V supply voltage, and professional communications equipment.

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 micro-miniature envelope with source and substrate interconnected.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.



Marking code: M87.

Fig.1 Simplified outline (SOT143) and symbol.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source, bias
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	18	V
I_D	drain current (DC)		–	30	mA
P_{tot}	total power dissipation	T_{amb} = 60 °C	–	200	mW
$\lvert Y_{fs} \rvert$	forward transfer admittance	f = 1 kHz; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	19	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	2.6	3	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	25	–	fF
F	noise figure	G_S = 5 mS; B_S = B_{Sopt}; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	2	3	dB
T_j	operating junction temperature		–	150	°C

Silicon N-channel dual-gate MOS-FET BF991

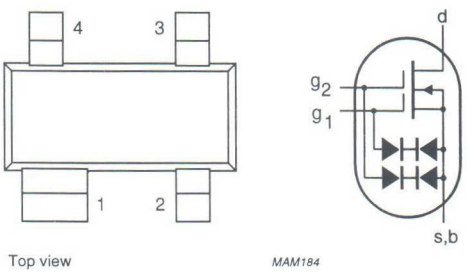
APPLICATIONS

- VHF applications such as VHF television tuners and FM tuners. The device is also suitable for use in professional communications equipment.

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 micro-miniature envelope with source and substrate interconnected.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.



Marking code: M91.

Fig.1 Simplified outline (SOT143) and symbol.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source, bias
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
I_D	drain current (DC)		–	20	mA
P_{tot}	total power dissipation	T_{amb} = 60 °C	–	200	mW
$\lvert Y_{fs} \rvert$	forward transfer admittance	f = 1 kHz; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	14	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	2.1	–	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	20	–	fF
F	noise figure	G_S = 1 mS; B_S = B_{Sopt}; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; f = 100 MHz	0.7	–	dB
T_j	operating junction temperature		–	150	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

Silicon N-channel dual-gate MOS-FET — BF992

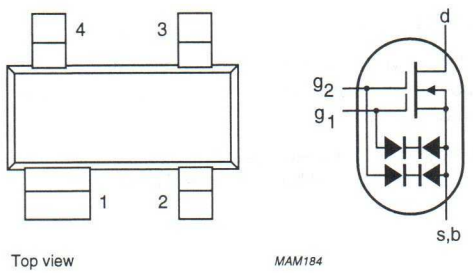
APPLICATIONS

- VHF applications such as VHF television tuners and FM tuners with 12 V supply voltage. The device is also suitable for use in professional communications equipment.

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 micro-miniature envelope with source and substrate interconnected.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.



Marking code: M92.

Fig.1 Simplified outline (SOT143) and symbol.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source, bias
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
I_D	drain current (DC)		–	40	mA
P_{tot}	total power dissipation	T_{amb} = 60 °C	–	200	mW
$\lvert Y_{fs} \rvert$	forward transfer admittance	f = 1 kHz; I_D = 15 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	25	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz; I_D = 15 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	4	–	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 15 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	30	–	fF
F	noise figure	G_S = 2 mS; I_D = 15 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	1.2	–	dB
T_j	operating junction temperature		–	150	°C

Silicon N-channel dual-gate MOS-FET BF994S

APPLICATIONS

- VHF applications in television tuners. The device is also suitable for use in professional communications equipment.

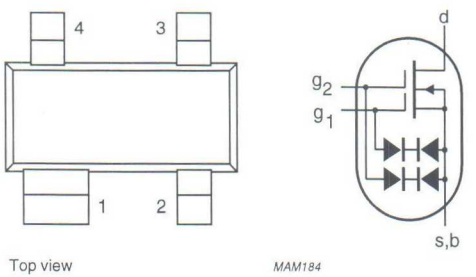
DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected.

The MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source, bias
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MGp.

Fig.1 Simplified outline (SOT143) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
I_D	drain current (DC)		–	30	mA
P_{tot}	total power dissipation	T_{amb} = 60 °C	–	200	mW
$\lvert Y_{fs} \rvert$	forward transfer admittance	f = 1 kHz; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	18	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	2.5	3	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	25	–	fF
F	noise figure	G_S = 2 mS; $B_S = B_{Sopt}$; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	1	–	dB
T_j	operating junction temperature		–	150	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

Silicon N-channel dual-gate MOS-FET BF966S

APPLICATIONS

- UHF applications in television tuners and professional communications equipment.

DESCRIPTION

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source, bias
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

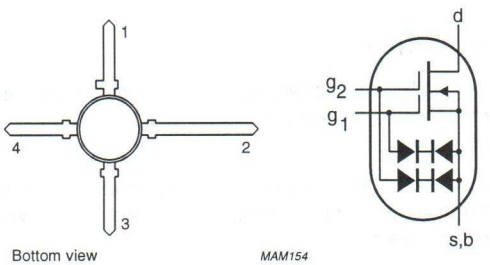


Fig.1 Simplified outline (SOT103) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
I_D	drain current (DC)		–	30	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C	–	225	mW
$\lvert Y_{fs} \rvert$	forward transfer admittance	f = 1 kHz; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	18	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	2.3	2.6	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	25	–	fF
F	noise figure	G_S = 3.3 mS; B_S = B_{Sopt}; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	1.8	–	dB
T_j	operating junction temperature		–	150	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

Silicon N-channel dual-gate MOS-FET — BF997

APPLICATIONS

- UHF and VHF applications such as UHF/ VHF television tuners and professional communications equipment.
- Especially intended for use in pre-amplifiers in CATV tuners with a large tuning range up to 500 MHz.

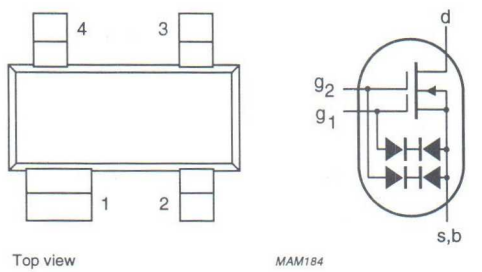
DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source and has an integrated drain resistance to suppress oscillation in the frequency range higher than 1 GHz.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source, bias
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MKp

Fig.1 Simplified outline (SOT143) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
I_D	drain current (DC)		–	30	mA
P_{tot}	total power dissipation	T_{amb} = 60 °C	–	200	mW
$\lvert Y_{fs} \rvert$	forward transfer admittance	f = 1 kHz; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	18	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	2.5	–	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	25	–	fF
F	noise figure	G_S = 2 mS; $B_S = B_{Sopt}$; I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	1	–	dB
T_j	junction temperature		–	150	°C

Silicon N-channel dual-gate MOS-FET — BF998

FEATURES

- Short channel transistor with high ratio $|Y_{fs}| / C_{is}$
- Low noise gain controlled amplifier to 1 GHz.

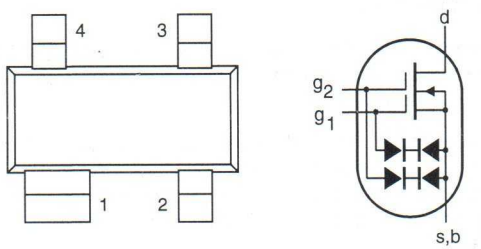
APPLICATIONS

- VHF and UHF applications such as television tuners with 12 V supply voltage and professional communications equipment.

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 micro-miniature envelope with source and substrate interconnected.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.



Marking code: MOp.

Fig.1 Simplified outline (SOT143) and symbol.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source, bias
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	12	V
I_D	drain current (DC)		–	30	mA
P_{tot}	total power dissipation		–	200	mW
$\|Y_{fs}\|$	forward transfer admittance		24	–	mS
C_{ig1-s}	input capacitance at gate 1		2.1	–	pF
C_{rs}	feedback capacitance		25	–	fF
F	noise figure	f = 800 MHz	1	–	dB
T_j	operating junction temperature		–	150	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

NPN 1 GHz wideband transistor — BFS17

APPLICATIONS

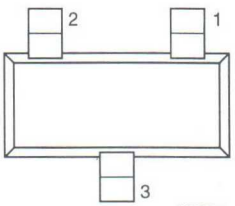
- It is intended for a wide range of RF applications such as mixers and oscillators in TV-tuners and RF communications equipment.

DESCRIPTION

NPN transistor in a plastic SOT23 package.

PINNING

PIN	DESCRIPTION
1	base
2	emitter
3	collector



Top view

Marking code: E1p.

Fig.1 SOT23.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	25	V
V_{CEO}	collector-emitter voltage	open base	–	15	V
I_C	collector current (DC)		–	25	mA
P_{tot}	total power dissipation	up to T_s = 70 °C; note 1	–	300	mW
f_T	transition frequency	I_C = 25 mA; V_{CE} = 5 V; f = 500 MHz; T_j = 25 °C	1	–	GHz
F	noise figure	I_C = 2 mA; V_{CE} = 5 V; R_s = 50 Ω; f = 500 MHz; T_j = 25 °C	4.5	–	dB

Note

1. T_s is the temperature at the soldering point of the collector pin.

NPN 3 GHz wideband transistor — BFS17A

APPLICATIONS

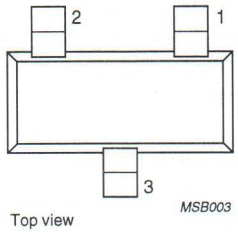
- It is intended for a wide range of RF applications such as TV-tuners.

DESCRIPTION

NPN transistor in a plastic SOT23 package.

PINNING

PIN	DESCRIPTION
1	base
2	emitter
3	collector



Top view

Marking code: E2p.

Fig.1 SOT23.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	25	V
V_{CEO}	collector-emitter voltage	open base	–	15	V
I_C	collector current (DC)		–	25	mA
P_{tot}	total power dissipation	up to T_s = 70 °C; note 1	–	300	mW
f_T	transition frequency	I_C = 25 mA; V_{CE} = 5 V; f = 500 MHz; T_{amb} = 25 °C	2.8	–	GHz
G_{UM}	maximum unilateral power gain	I_C = 14 mA; V_{CE} = 10 V; f = 800 MHz	13.5	–	dB
F	noise figure	I_C = 2 mA; V_{CE} = 5 V; f = 800 MHz; T_{amb} = 25 °C	2.5	–	dB
V_O	output voltage	d_{im} = −60 dB; I_C = 14 mA; V_{CE} = 10 V; R_L = 75 Ω; T_{amb} = 25 °C; $f_{(p+q-r)}$ = 793.25 MHz	150	–	mV

Note

1. T_s is the temperature at the soldering point of the collector pin.

Parallel efficiency diode BY228

FEATURES

- High reverse voltage capability with controlled recovery time.

APPLICATIONS

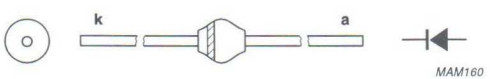
- Efficiency diode in transistorized horizontal deflection circuits of television receivers.

DESCRIPTION

Double-diffused passivated rectifier diode in a hermetically sealed axial-leaded glass envelope.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage	1500	V
I_{FWM}	working peak forward current	5	A
I_{FRM}	repetitive peak forward current	10	A
t_{tot}	total reverse recovery time	20	µs



The marking band indicates the cathode.

Fig.1 Simplified outline (SOD64) and symbol.

Rectifier diodes fast, soft-recovery BY229 series

FEATURES

- Low forward voltage drop
- Fast reverse recovery and soft recovery characteristic.

APPLICATIONS

- Intended for use in:
  - Television receivers
  - Monitors
  - Switched mode power supplies.

DESCRIPTION

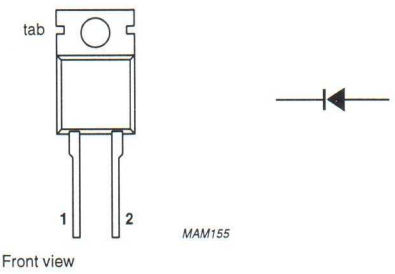
Glass-passivated double diffused rectifier diodes in a plastic TO220AC package.

PINNING

PIN	DESCRIPTION
1	cathode
2	anode
tab	cathode

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage		
	BY229-200	200	V
	BY229-400	400	V
	BY229-600	600	V
	BY229-800	800	V
$I_{F(AV)}$	average forward current	8	A
I_{FSM}	non-repetitive peak forward current	60	A
t_{rr}	reverse recovery time	135	ns



Front view

Fig.1 Simplified outline (TO220AC) and symbol.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC02 OR DATA SHEET

32 kHz parallel efficiency diode BY328

FEATURES

- High reverse voltage capability with controlled recovery time and fast turn-on.

APPLICATIONS

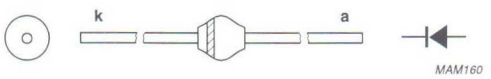
- Efficiency diode in transistorized horizontal deflection circuits of television receivers with line frequency up to 32 kHz.

DESCRIPTION

Double-diffused glass passivated rectifier diode in a hermetically sealed axial-leaded glass envelope.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage	1400	V
I_{FWM}	working peak forward current	6	A
I_{FRM}	repetitive peak forward current	10	A
t_{tot}	total reverse recovery time	13	µs



The marking band indicates the cathode.

Fig.1 Simplified outline (SOD64) and symbol.

Rectifier diodes fast, soft-recovery BY329 series

FEATURES

- Low forward voltage drop
- Fast reverse recovery and soft recovery characteristic.

APPLICATIONS

- Intended for use in:
  - Television receivers
  - Monitors
  - Switched mode power supplies.

DESCRIPTION

Glass-passivated double diffused rectifier diodes in a plastic TO220AC package.

PINNING

PIN	DESCRIPTION
1	cathode
2	anode
tab	cathode

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage		
	BY329-800	800	V
	BY329-1000	1000	V
	BY329-1200	1200	V
$I_{F(AV)}$	average forward current	8	A
I_{FSM}	non-repetitive peak forward current	75	A
t_{rr}	reverse recovery time	135	ns

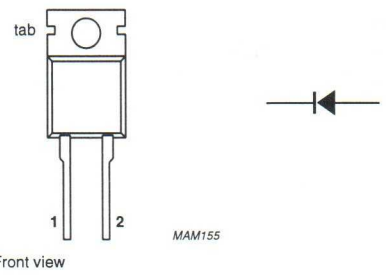


Fig.1 Simplified outline (TO220AC) and symbol.

Rectifier diode fast, high-voltage BY359F-1500

FEATURES

- Low forward voltage drop
- Fast reverse recovery and soft recovery characteristic.

APPLICATIONS

- Television receivers
- Series resonant switched mode power supplies
- High voltage circuits.

DESCRIPTION

Glass-passivated double diffused rectifier diode in a full pack plastic package.

PINNING

PIN	DESCRIPTION
1	cathode
2	anode
case	isolated

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage	1500	V
V_F	forward voltage	1.5	V
I_F	average forward current	10	A
I_{FSM}	non-repetitive peak forward current	60	A
t_{rr}	reverse recovery time	0.6	µs

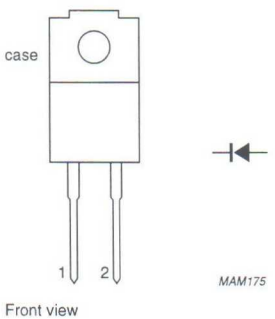


Fig.1 Simplified outline (SOD100) and symbol.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC02 OR DATA SHEET

Rectifier diode fast, high-voltage BY359X-1500

FEATURES

- Low forward voltage drop
- Fast reverse recovery and soft recovery characteristic.

APPLICATIONS

- Television receivers
- Series resonant switched mode power supplies
- High voltage circuits.

DESCRIPTION

Glass-passivated double diffused rectifier diode in a full pack plastic package.

PINNING

PIN	DESCRIPTION
1	cathode
2	anode
case	isolated

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage	1500	V
V_F	forward voltage	1.5	V
I_F	average forward current	10	A
I_{FSM}	non-repetitive peak forward current	60	A
t_{rr}	reverse recovery time	0.6	µs

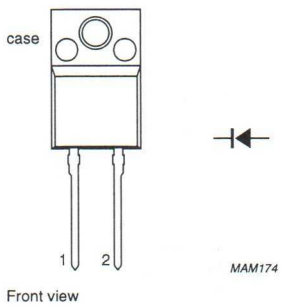


Fig.1 Simplified outline (SOD113) and symbol.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC02 OR DATA SHEET

High-voltage fast soft-recovery controlled avalanche rectifier diodes

BY8000 series

FEATURES

- Non-snap-off (soft-recovery) switching characteristics
- Hermetic seal
- Glass passivation
- Capability of absorbing avalanche energy, e.g. during flash-over in picture tubes and at high-voltage output of a line output transformer
- Withstands peak currents during flash-over in picture tubes.

APPLICATIONS

They are designed for colour television and monitor applications with frequencies up to 25 kHz and suitable for use in high voltage applications such as multipliers and especially in layer-wound diode-split-transformers where controlled avalanche is required.

DESCRIPTION

Glass passivated high-voltage rectifier diodes in hermetically-sealed, axial-leaded glass envelopes. Because of the small envelope, the diode should be used in a suitable insulating medium (resin, oil, or SF6 gas).

CATHODE BAND COLOUR CODES

TYPE NUMBER	INNER BAND	OUTER BAND
BY8004	violet	black
BY8006	violet	green
BY8008	violet	red
BY8010	violet	violet
BY8012	violet	orange
BY8014	violet	lilac
BY8016	violet	grey

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{RW}	working reverse voltage			
	BY8004	–	4	kV
	BY8006	–	6	kV
	BY8008	–	8	kV
	BY8010	–	10	kV
	BY8012	–	12	kV
	BY8014	–	14	kV
	BY8016	–	16	kV
V_{RRM}	repetitive peak reverse voltage			
	BY8004	–	5	kV
	BY8006	–	8	kV
	BY8008	–	10	kV
	BY8010	–	12	kV
	BY8012	–	14	kV
	BY8014	–	17	kV
	BY8016	–	19	kV
$I_{F(AV)}$	average forward current			
	BY8004	–	20	mA
	BY8006	–	10	mA
	BY8008	–	5	mA
	BY8010	–	5	mA
	BY8012	–	5	mA
	BY8014	–	5	mA
	BY8016	–	3	mA
T_j	junction temperature	–65	120	°C
Q_r	recovery charge	–	1	nC
t_{rr}	reverse recovery time	200	–	ns

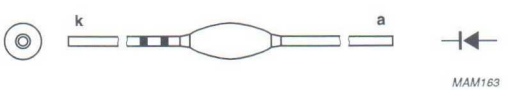


Fig.1 Simplified outline (SOD61).

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATA SHEET

High-voltage very fast soft-recovery controlled avalanche rectifier diodes

BY8100 series

FEATURES

- Non-snap-off (soft-recovery) switching characteristics
- Hermetic seal
- Glass passivation
- Capability of absorbing avalanche energy, e.g. during flash-over in picture tubes and at high-voltage output of a line output transformer
- Withstands peak currents during flash-over in picture tubes.

APPLICATIONS

They are designed for colour television and monitor applications with frequencies up to 128 kHz and suitable for use in high voltage applications such as multipliers and especially in layer-wound diode-split-transformers where controlled avalanche is required.

DESCRIPTION

Glass passivated high-voltage rectifier diodes in hermetically-sealed, axial-leaded glass envelopes. Because of the small envelope, the diode should be used in a suitable insulating medium (resin, oil, or SF6 gas).

CATHODE BAND COLOUR CODES

TYPE NUMBER	INNER BAND	OUTER BAND
BY8104	orange	black
BY8106	orange	green
BY8108	orange	red
BY8110	orange	violet
BY8112	orange	orange
BY8114	orange	lilac
BY8116	orange	grey

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage			
	BY8104	–	5	kV
	BY8106	–	8	kV
	BY8108	–	10	kV
	BY8110	–	12	kV
	BY8112	–	14	kV
	BY8114	–	17	kV
	BY8116	–	19	kV
V_{RW}	working reverse voltage			
	BY8104	–	4	kV
	BY8106	–	6	kV
	BY8108	–	8	kV
	BY8110	–	10	kV
	BY8112	–	12	kV
	BY8114	–	14	kV
	BY8116	–	16	kV
$I_{F(AV)}$	average forward current			
	BY8104	–	20	mA
	BY8106	–	10	mA
	BY8108	–	5	mA
	BY8110	–	5	mA
	BY8112	–	5	mA
	BY8114	–	5	mA
	BY8116	–	3	mA
T_j	junction temperature	–	120	°C
Q_r	recovery charge	–	0.4	nC
t_{rr}	reverse recovery time	100	–	ns

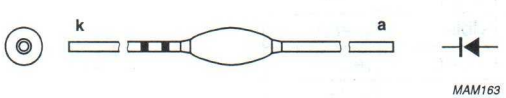


Fig.1 Simplified outline (SOD61).

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATA SHEET

High-voltage fast soft-recovery rectifier diodes

BY8400 series

FEATURES

- Non-snap-off (soft- recovery) switching characteristics
- Hermetic seal
- Glass passivation
- Withstands peak currents during flash-over in picture tubes.

APPLICATIONS

They are designed for colour television and monitor applications with frequencies up to 25 kHz and suitable for use in high voltage applications such as multipliers and especially in layer-wound diode-split-transformers.

DESCRIPTION

Glass passivated high-voltage rectifier diodes in hermetically-sealed, axial-leaded glass envelopes. Because of the small envelope, the diode should be used in a suitable insulating medium (resin, oil, or SF6 gas).

CATHODE BAND COLOUR CODES

TYPE NUMBER	INNER BAND	OUTER BAND
BY8404	black	black
BY8406	black	green
BY8408	black	red
BY8410	black	violet
BY8412	black	orange
BY8414	black	lilac
BY8416	black	grey
BY8418	black	brown
BY8420	black	dark blue
BY8424	black	no band

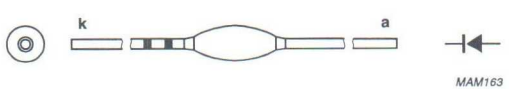


Fig.1 Simplified outline (SOD61).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{RW}	working reverse voltage			
	BY8404	–	4	kV
	BY8406	–	6	kV
	BY8408	–	8	kV
	BY8410	–	10	kV
	BY8412	–	12	kV
	BY8414	–	14	kV
	BY8416	–	16	kV
	BY8418	–	18	kV
	BY8420	–	20	kV
	BY8424	–	24	kV
V_{RRM}	repetitive peak reverse voltage			
	BY8404	–	5	kV
	BY8406	–	8	kV
	BY8408	–	10	kV
	BY8410	–	12	kV
	BY8412	–	14	kV
	BY8414	–	17	kV
	BY8416	–	19	kV
	BY8418	–	22	kV
	BY8420	–	24	kV
	BY8424	–	30	kV
$I_{F(AV)}$	average forward current			
	BY8404	–	20	mA
	BY8406	–	10	mA
	BY8408	–	5	mA
	BY8410	–	5	mA
	BY8412	–	5	mA
	BY8414	–	5	mA
	BY8416	–	3	mA
	BY8418	–	3	mA
	BY8420	–	3	mA
	BY8424	–	3	mA
T_j	junction temperature	–65	120	°C
Q_r	recovery charge	–	1	nC
t_{rr}	reverse recovery time	200	–	ns

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATA SHEET

Fast soft-recovery controlled avalanche rectifier diodes

BYD33 series

FEATURES

- Non-snap-off (soft-recovery) switching characteristics
- Capability of absorbing reverse transient energy (e.g. during flashover in a picture tube).

APPLICATIONS

- Switched-mode power supplies
- Scan rectifiers in television receivers
- Inverter circuits
- Converter circuits.

DESCRIPTION

Glass passivated rectifier diodes in SOD81 hermetically-sealed, axial-leaded implosion diode (ID) glass envelopes.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage		
	BYD33D	200	V
	BYD33G	400	V
	BYD33J	600	V
	BYD33K	800	V
	BYD33M	1000	V
	BYD33U	1200	V
	BYD33V	1400	V
V_R	continuous reverse voltage		
	BYD33D	200	V
	BYD33G	400	V
	BYD33J	600	V
	BYD33K	800	V
	BYD33M	1000	V
	BYD33U	1200	V
	BYD33V	1400	V
$I_{F(AV)}$	average forward current		
	BYD33D to M	1.3	A
	BYD33U and V	1.26	A
I_{FSM}	non-repetitive peak forward current	20	A
E_{RSM}	non-repetitive peak reverse avalanche energy		
	BYD33D to J	10	mJ
	BYD33K to V	7	mJ
t_{rr}	reverse recovery time		
	BYD33D to J	250	ns
	BYD33K and M	300	ns
	BYD33U and V	500	ns

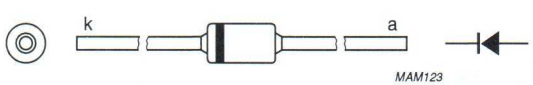


Fig.1 Simplified outline (SOD81) and symbol.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATA SHEET

Avalanche fast soft-recovery rectifier diodes

BYV95A to C

FEATURES

- Non-snap-off (soft-recovery) switching characteristics
- Capable of absorbing reverse transient energy (e.g. during flashover in the picture tube).

APPLICATIONS

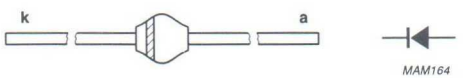
- Television and industrial applications, such as:
  - Switched-mode power supplies
  - Scan rectifiers in TV receivers
  - Inverter and converter applications.

DESCRIPTION

Glass passivated rectifier diodes in hermetically sealed axial-leaded glass envelopes.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage		
	BYV95A	200	V
	BYV95B	400	V
	BYV95C	600	V
V_R	continuous reverse voltage		
	BYV95A	200	V
	BYV95B	400	V
	BYV95C	600	V
$I_{F(AV)}$	average forward current	1.5	A
I_{FSM}	non-repetitive peak forward current	35	A
E_{RSM}	non-repetitive peak reverse energy	10	mJ
t_{rr}	reverse recovery time	250	ns



MAM164

The marking band indicates the cathode.

Fig.1 Simplified outline (SOD57) and symbol.

Controlled avalanche rectifier diodes

BYW54 to 56

FEATURES

- Capability of absorbing reverse transients.

APPLICATIONS

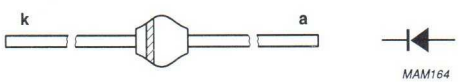
- Rectifier applications in colour television circuits
- General purpose applications in telephony equipment.

DESCRIPTION

Double-diffused glass passivated rectifier diodes in hermetically sealed axial-leaded glass envelopes.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{RWM}	crest working reverse voltage			
	BYW54	–	600	V
	BYW55	–	800	V
	BYW56	–	1000	V
$V_{(BR)R}$	reverse avalanche breakdown voltage			
	BYW54	650	1000	V
	BYW55	900	1300	V
	BYW56	1100	1600	V
$I_{F(AV)}$	average forward current	–	2	A
I_{FSM}	non-repetitive peak forward current	–	50	A
P_{RSM}	non-repetitive peak reverse power dissipation	–	1	kW
T_j	junction temperature	–	175	°C



The marking band indicates the cathode.

Fig.1 Simplified outline (SOD57) and symbol.

Video amplifier

NE592

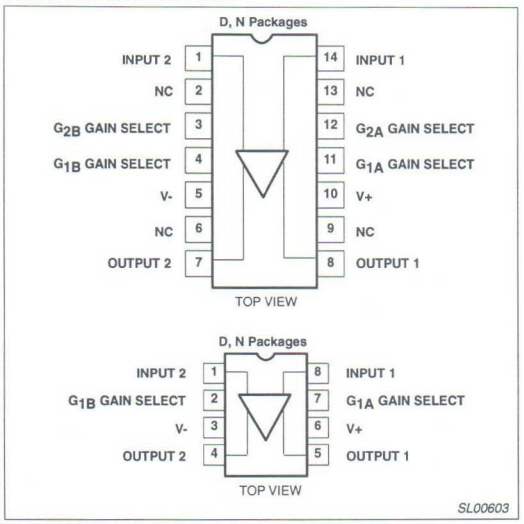
DESCRIPTION

The NE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers. Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor.

FEATURES

- 120MHz unity gain bandwidth
- Adjustable gains from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Wave shaping with minimal external components
- MIL-STD processing available

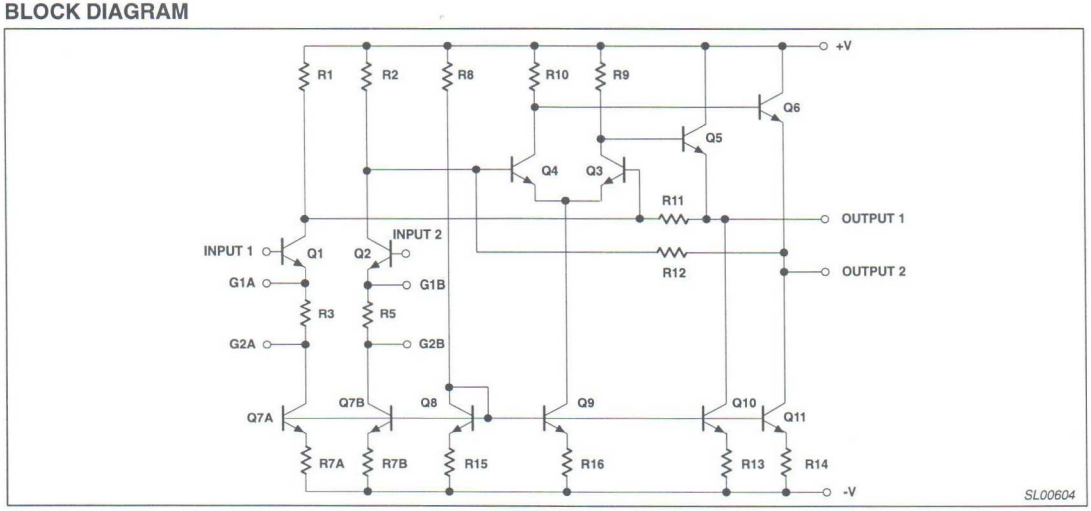
PIN CONFIGURATIONS



APPLICATIONS

- Floppy disk head amplifier
- Video amplifier
- Pulse amplifier in communications
- Magnetic memory
- Video recorder systems

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE592N14	0405B
14-Pin Small Outline (SO) package	0 to +70°C	NE592D14	0175D
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE592N8	0404B
8-Pin Small Outline (SO) package	0 to +70°C	NE592D8	0174C

NOTES:
N8, N14, D8 and D14 package parts also available in "High" gain version by adding "H" before package designation, i.e., NE592HDB

ABSOLUTE MAXIMUM RATINGS

T_A=+25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
$P_{D\ MAX}$	Maximum power dissipation, T_A=25°C (still air)[1]		
	D-14 package	0.98	W
	D-8 package	0.79	W
	N-14 package	1.44	W
	N-8 package	1.17	W

NOTES:
1. Derate above 25°C at the following rates:
   D-14 package at 7.8mW/°C
   D-8 package at 6.3mW/°C
   N-14 package at 11.5mW/°C
   N-8 package at 9.3mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=+25°C V_{SS}=±6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltages V_S=±6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE592			UNIT
			Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part					
	Gain 1[1]	R_L=2kΩ, V_{OUT}=3V_{P-P}	250	400	600	V/V
	Gain 2[2, 4]		80	100	120	V/V
R_{IN}	Input resistance					
	Gain 1[1]			4.0		kΩ
	Gain 2[2, 4]		10	30		kΩ
C_{IN}	Input capacitance[2]	Gain 2[4]		2.0		pF
I_{OS}	Input offset current			0.4	5.0	μA
I_{BIAS}	Input bias current			9.0	30	μA
V_{NOISE}	Input noise voltage	BW 1kHz to 10MHz		12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio					
	Gain 2[4]	V_{CM}±1V, f<100kHz	60	86		dB
	Gain 2[4]	V_{CM}±1V, f=5MHz		60		dB
PSRR	Supply voltage rejection ratio					
	Gain 2[4]	ΔV_S=±0.5V	50	70		dB
V_{OS}	Output offset voltage					
	Gain 1	R_L=∞			1.5	V
	Gain 2[4]	R_L=∞			1.5	V
	Gain 3[3]	R_L=∞		0.35	0.75	V
V_{CM}	Output common-mode voltage	R_L=∞	2.4	2.9	3.4	V
V_{OUT}	Output voltage swing differential	R_L=2kΩ	3.0	4.0		V
R_{OUT}	Output resistance			20		Ω
I_{CC}	Power supply current	R_L=∞		18	24	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 14-pin version only.

DC ELECTRICAL CHARACTERISTICS

DC Electrical Characteristics V_{SS}=±6V, V_{CM}=0, 0°C ≤T_A≤70°C, unless otherwise specified. Recommended operating supply voltages V_S=±6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE592			UNIT
			Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part					
	Gain 1[1]	R_L=2kΩ, V_{OUT}=3V_{P-P}	250		600	V/V
	Gain 2[2, 4]		80		120	V/V
R_{IN}	Input resistance					
	Gain 2[2, 4]		8.0			kΩ
I_{OS}	Input offset current				6.0	μA
I_{BIAS}	Input bias current				40	μA
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio					
	Gain 2[4]	V_{CM}±1V, f<100kHz	50			dB
PSRR	Supply voltage rejection ratio					
	Gain 2[4]	ΔV_S=±0.5V	50			dB
V_{OS}	Output offset voltage					
	Gain 1	R_L=∞			1.5	V
	Gain 2[4]				1.5	
	Gain 3[3]				1.0	
V_{OUT}	Output voltage swing differential	R_L=2kΩ	2.8			V
I_{CC}	Power supply current	R_L=∞			27	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 14-pin versions only.

AC ELECTRICAL CHARACTERISTICS

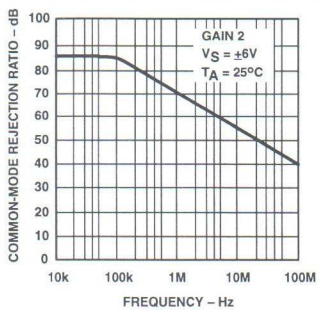
T_A=+25°C V_{SS}=±6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltages V_S=±6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			UNIT
			Min	Typ	Max	
BW	Bandwidth					
	Gain 1[1]			40		MHz
	Gain 2[2, 4]			90		MHz
t_R	Rise time					
	Gain 1[1]	V_{OUT}=1V_{P-P}		10.5	12	ns
	Gain 2[2, 4]			4.5		ns
t_{PD}	Propagation delay					
	Gain 1[1]	V_{OUT}=1V_{P-P}		7.5	10	ns
	Gain 2[2, 4]			6.0		ns

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 14-pin versions only.

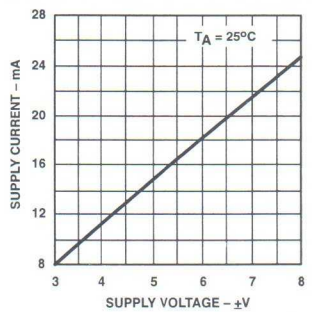
TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Rejection Ratio as a Function of Frequency



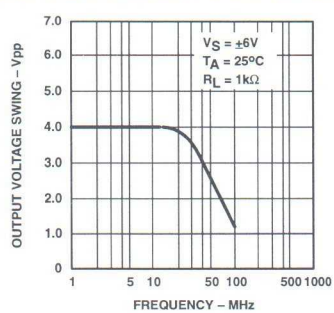
SL00605

Supply Current as a Function of Temperature



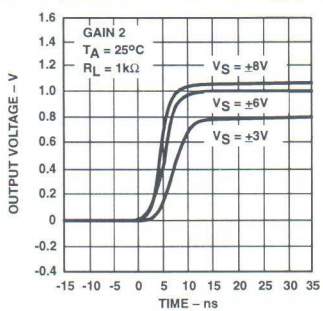
SL00608

Output Voltage Swing as a Function of Frequency



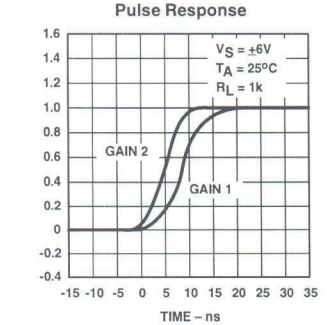
SL00606

Pulse Response as a Function of Supply Voltage



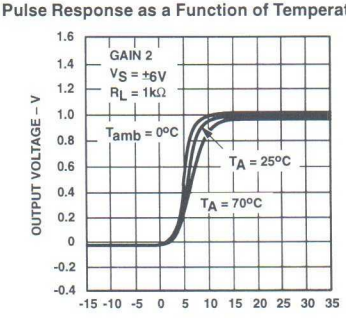
SL00609

Pulse Response



SL00607

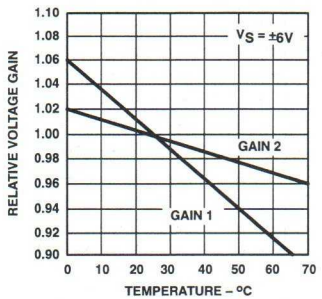
Pulse Response as a Function of Temperature



SL00610

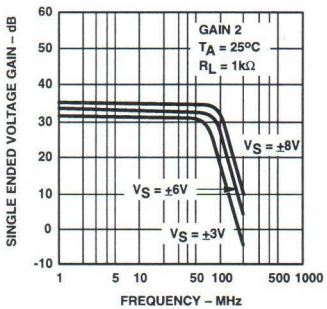
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Voltage Gain as a Function of Temperature



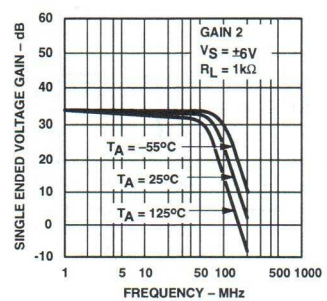
SL00611

Gain vs. Frequency as a Function of Supply Voltage



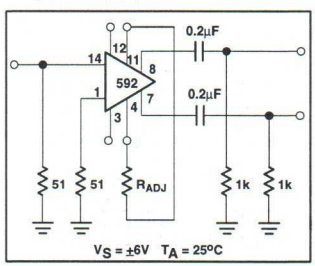
SL00614

Gain vs. Frequency as a Function of Temperature



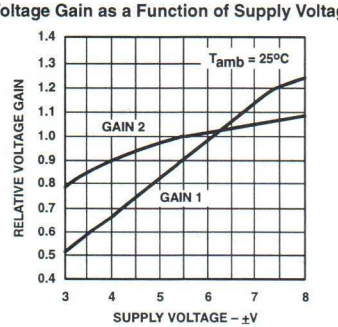
SL00612

Voltage Gain Adjust Circuit



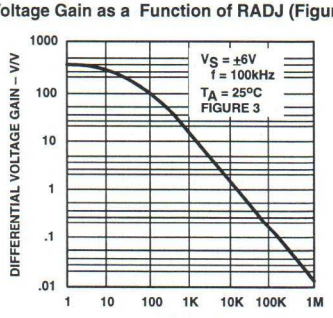
SL00615

Voltage Gain as a Function of Supply Voltage



SL00613

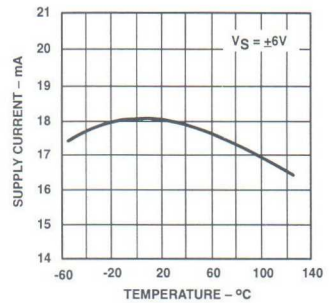
Voltage Gain as a Function of RADJ (Figure 3)



SL00616

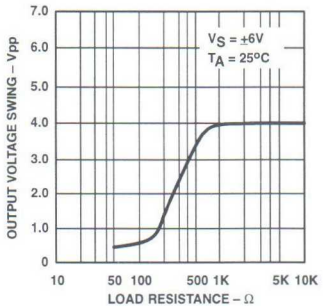
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Supply Current as a Function of Temperature



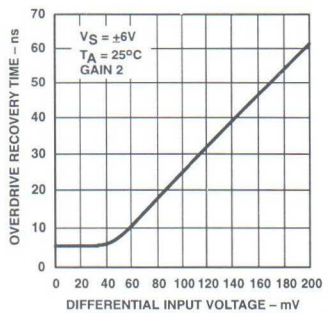
SL00617

Output Voltage Swing as a Function of Load Resistance



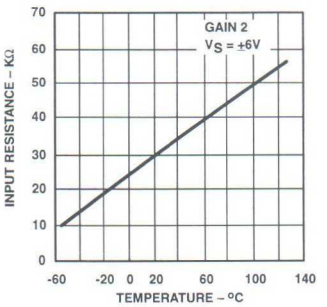
SL00620

Differential Overdrive Recovery Time



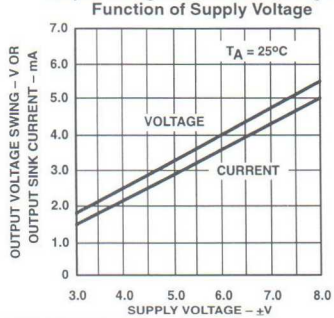
SL00618

Input Resistance as a Function of Temperature



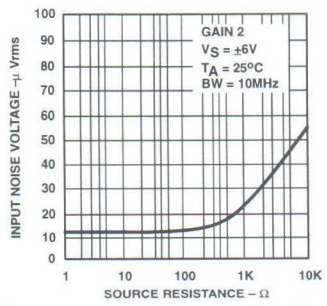
SL00621

Output Voltage and Current Swing as a Function of Supply Voltage



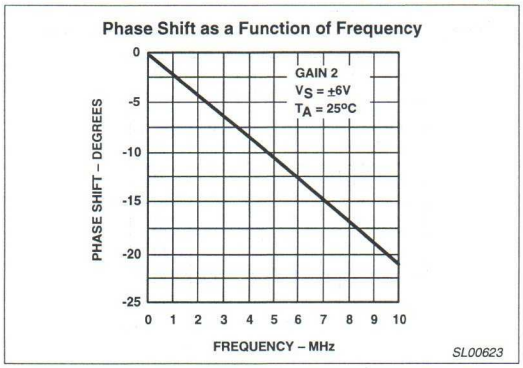
SL00619

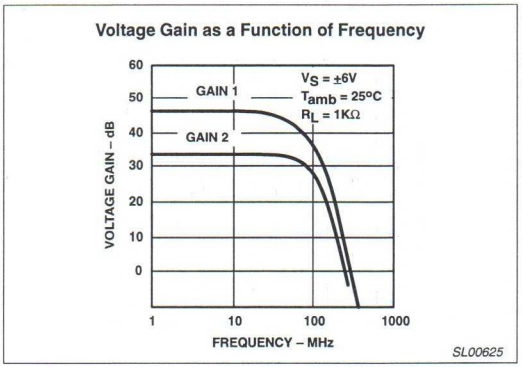
Input Noise Voltage as a Function of Source Resistance

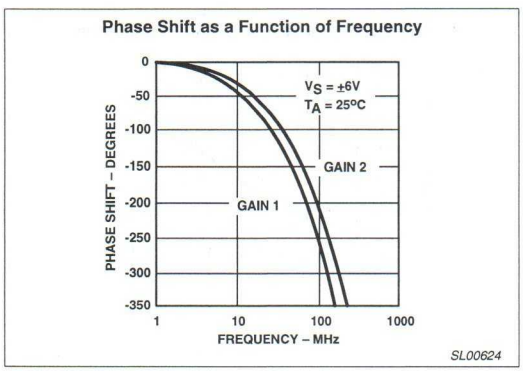


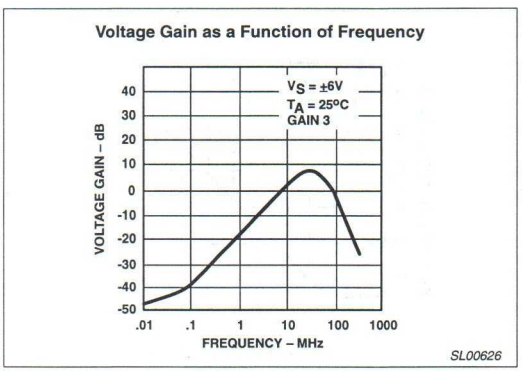
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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

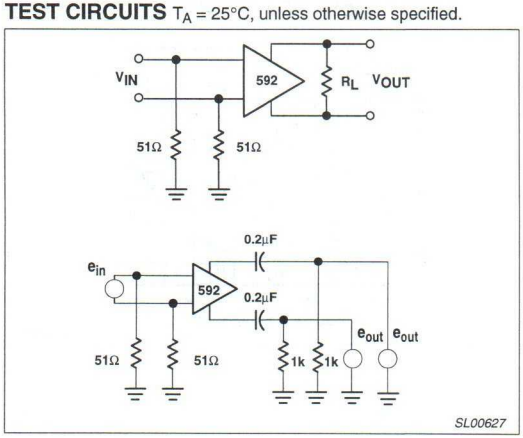








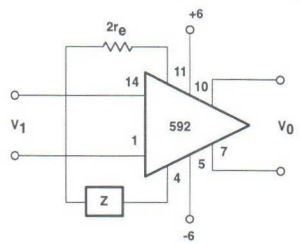
TEST CIRCUITS T_A = 25°C, unless otherwise specified.



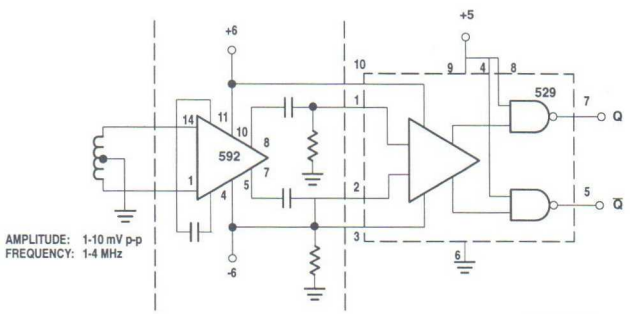
TYPICAL APPLICATIONS

NOTE:

$$\frac{V_0(s)}{v_1(s)} \simeq \frac{1.4 \cdot 10^4}{Z(S) + 2r_e} \simeq \frac{1.4 \cdot 10^4}{Z(S) + 32}$$

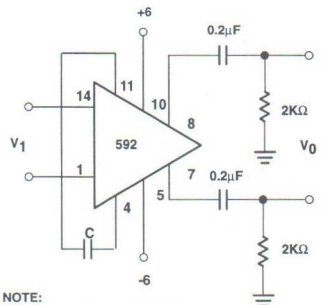


Basic Configuration



READ HEAD | DIFFERENTIATOR/AMPLIFIER | ZERO CROSSING DETECTOR

Disc/Tape Phase-Modulated Readback Systems



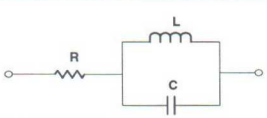
NOTE:
For frequency $F_1 << 1/2\,\pi\,(32)\,C$

$$V_O \simeq 1.4 \times 10^4 C \frac{dVi}{dT}$$

Differentiation with High Common-Mode Noise Rejection

SL00628

FILTER NETWORKS

Z NETWORK	FILTER TYPE	V_0 (s) TRANSFER V_1 (s) FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/Ls + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTES:
In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.
$S = j\omega$
$\omega = 2\pi f$

SL00629

Wide-band high-frequency amplifier NE/SA5204A

DESCRIPTION

The NE/SA5204A family of wideband amplifiers replaces the NE/SA5204 family. The 'A' parts are fabricated on a rugged 2µm bipolar process featuring excellent statistical process control. Electrical performance is nomically identical to the original parts.

The NE/SA5204A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 200MHz. The -3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The NE/SA5204A operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The NE/SA5204A is a relaxed version of the NE5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA5204A solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

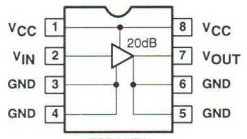
Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

No external components are needed other than AC-coupling capacitors because the NE/SA5204A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA5204As in series as required, without any degradation in amplifier stability.

PIN CONFIGURATION

N, D Packages



TOP VIEW

FEATURES

- Bandwidth (min.)
  200 MHz, ±0.5dB
  350 MHz, -3dB
- 20dB insertion gain
- 4.8dB (6dB) noise figure Z_O=75Ω (Z_O=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface-mount package available
- Cascadable
- 2000V ESD protection

APPLICATIONS

- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broadband LANs
- Networks
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

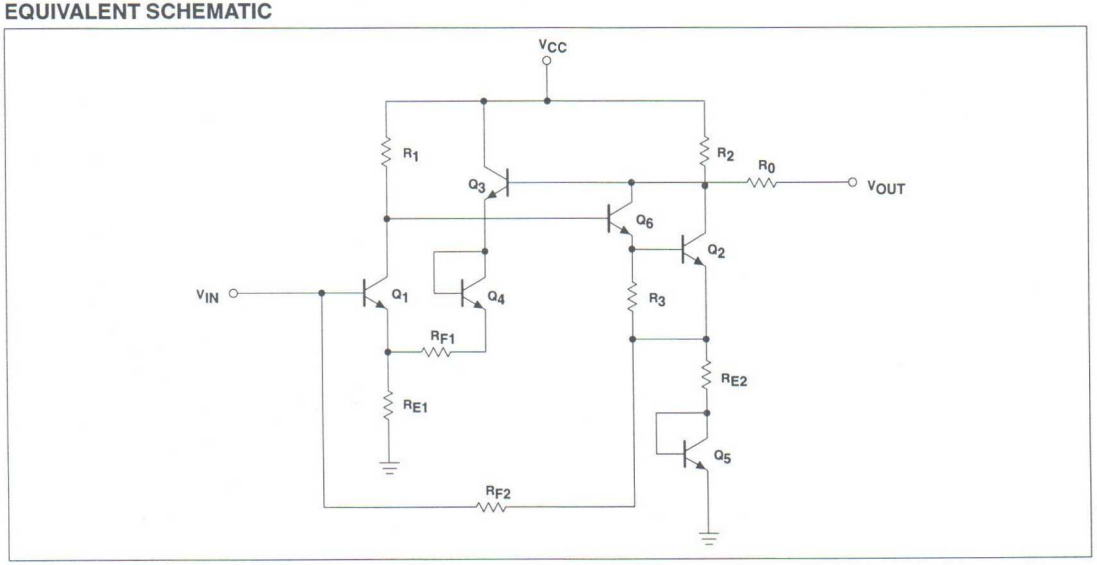
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5204AN	0404B
8-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5204AD	0174C
8-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA5204AN	0404B
8-Pin Plastic Small Outline (SO) package	–40 to +85°C	SA5204AD	0174C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{IN}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	–40 to +85	°C
P_{DMAX}	Maximum power dissipation[1, 2] T_A=25°C(still–air)		
	N package	1160	mW
	D package	780	mW
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	–55 to +150	°C
T_{SOLD}	Lead temperature (soldering 60s)	300	°C

NOTES:
1. Derate above 25°C, at the following rates
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. See "Power Dissipation Considerations" section.

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

V_{CC}=6V, Z_S=Z_L=Z_O=50Ω and T_A=25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5		8	V
I_{CC}	Supply current	Over temperature	19	25	33	mA
S21	Insertion gain	f=100MHz, over temperature	16	19	22	dB
S11	Input return loss	f=100MHz		25		dB
		DC –550MHz		12		
S22	Output return loss	f=100MHz		27		dB
		DC –550MHz		12		
S12	Isolation	f=100MHz		–25		dB
		DC –550MHz		–18		
BW	Bandwidth	±0.5dB	200	350		MHz
BW	Bandwidth	–3dB	350	550		MHz
	Noise figure (75Ω)	f=100MHz		4.8		dB
	Noise figure (50Ω)	f=100MHz		6.0		dB
	Saturated output power	f=100MHz		+7.0		dBm
	1dB gain compression	f=100MHz		+4.0		dBm
	Third–order intermodulation intercept (output)	f=100MHz		+17		dBm
	Second–order intermodulation intercept (output)	f=100MHz		+24		dBm
t_R	Rise time			500		ps
t_P	Propagation delay			500		ps

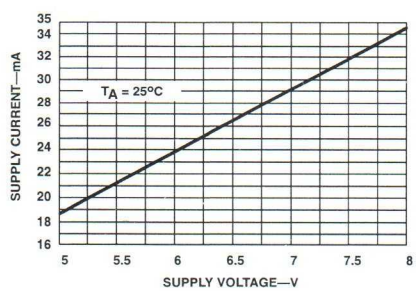


Figure 1. Supply Current vs Supply Voltage

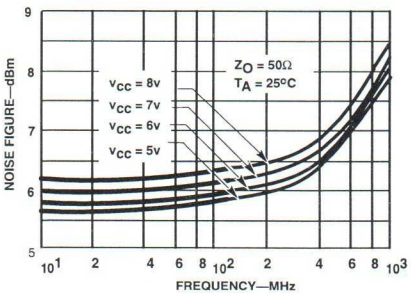


Figure 2. Noise Figure vs Frequency

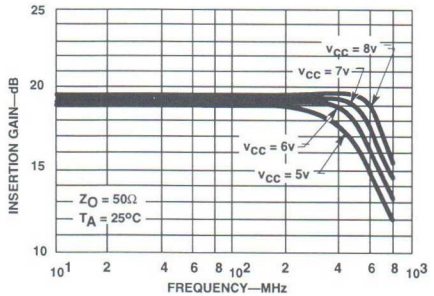


Figure 3. Insertion Gain vs Frequency (S_{21})

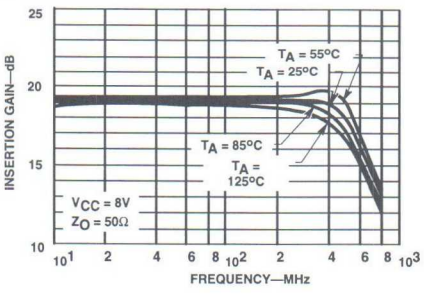


Figure 4. Insertion Gain vs Frequency (S_{21})

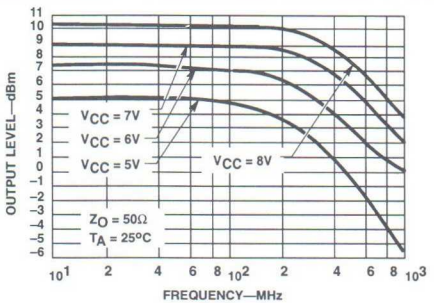


Figure 5. Saturated Output Power vs Frequency

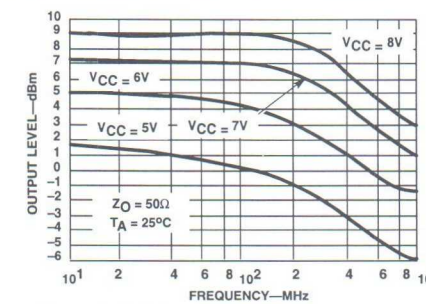


Figure 6. 1dB Gain Compression vs Frequency

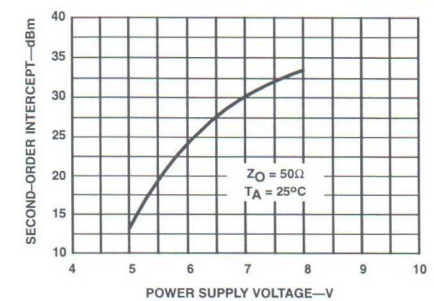


Figure 7. Second-Order Output Intercept vs Supply Voltage

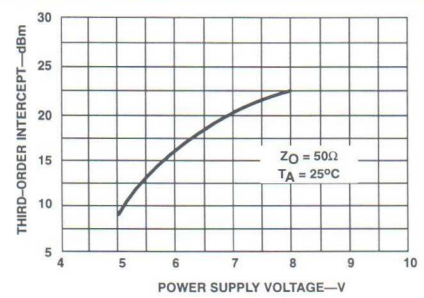


Figure 8. Third-Order Intercept vs Supply Voltage

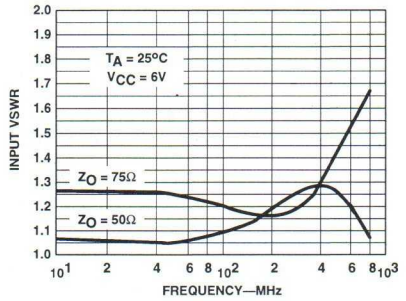


Figure 9. Input VSWR vs Frequency

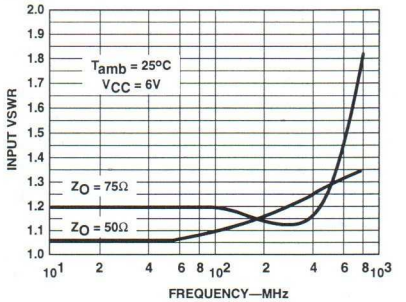


Figure 10. Output VSWR vs Frequency

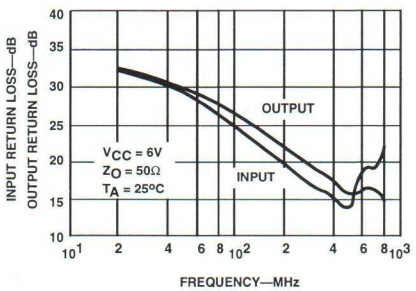


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

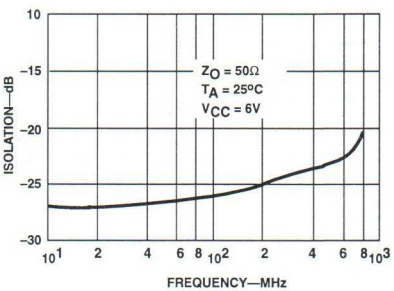


Figure 12. Isolation vs Frequency (S_{12})

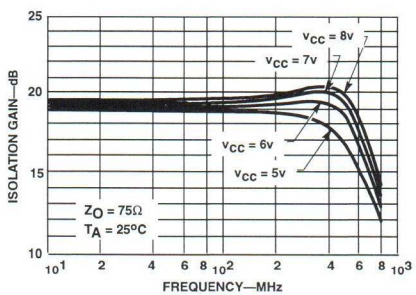


Figure 13. Insertion Gain vs Frequency (S_{21})

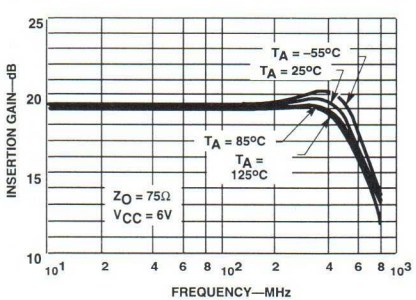


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1}) / R_{E1} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wide-band terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible, while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10\text{Log}\left(1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2q|_{C1}}\right]}{R_O}\right) \text{dB} \quad (2)$$

where I_{C1}=5.5mA, R_{E1}=12Ω, r_b=130Ω, KT/q=26mV at 25°C and R_0=50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN}=V_{BE1}+(I_{C1}+I_{C3})\,R_{E1} \quad (3)$$

where R_{E1}=12Ω, V_{BE}=0.8V, I_{C1}=5mA and I_{C3}=7mA (currents rated at V_{CC}=6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4, which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt-feedback loading on the output. The value of R_{F1}=140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT}=V_{CC}-(I_{C2}+I_{C6})R2, \quad (4)$$

where V_{CC}=6V, R_2=225Ω, I_{C2}=8mA and I_{C6}=5mA.

From here, it can be seen that the output voltage is approximately 3.1V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (32mA max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat-sinking benefits can be realized by mounting the SO and N package bodies against the PC board plane.

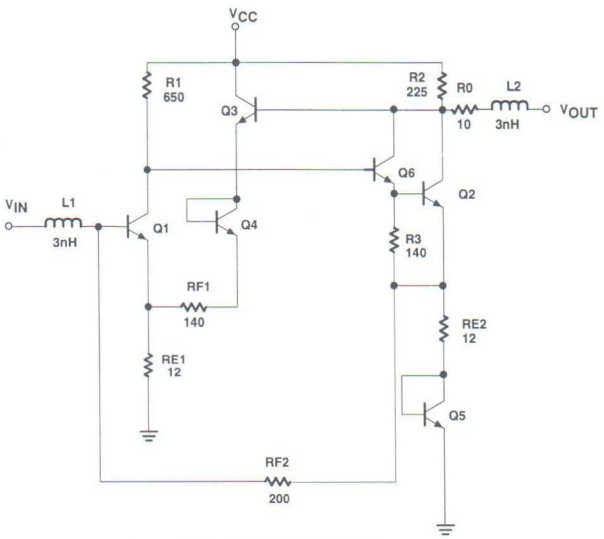


Figure 15. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5204A to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible, and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC-coupled. This is because at V_{CC}=6V, the input is approximately at 1V while the output is at 3.1V. The output must be decoupled into a low-impedance system, or the DC bias on the output of the amplifier will be loaded down, causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high-frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the NE5204A are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier, and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.

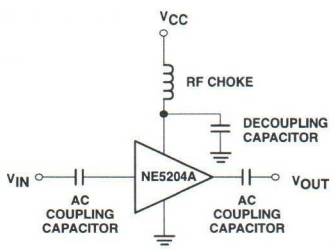


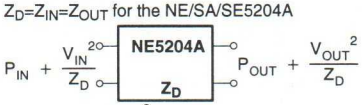
Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5204A to other high-frequency amplifiers.

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D=Z_{IN}=Z_{OUT}$ for the NE/SA/SE5204A



$$P_{IN} + \frac{V_{IN}^2}{Z_D} \qquad P_{OUT} + \frac{V_{OUT}^2}{Z_D}$$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I=V_I{}^2$

P_I=Insertion Power Gain

V_I=Insertion Voltage Gain

Measured value for the NE/SA/SE5204A = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

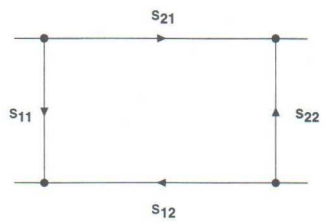
$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20\text{dB}$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:



a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} = \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OSOLATION

$$S_{12} = \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

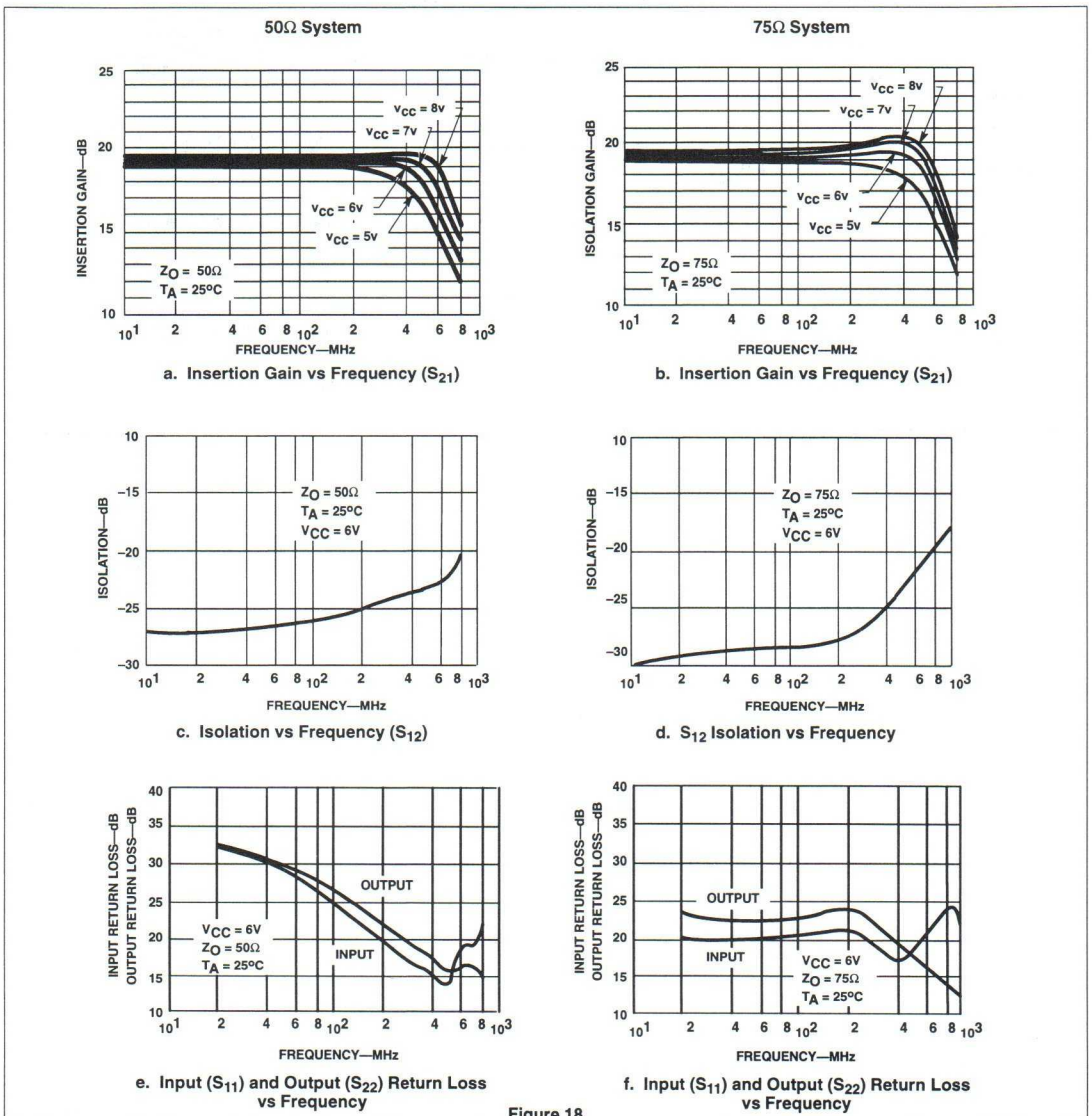
$$S_{21} = \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} = \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

b.

Figure 17.



a. Insertion Gain vs Frequency (S_{21})

b. Insertion Gain vs Frequency (S_{21})

c. Isolation vs Frequency (S_{12})

d. S_{12} Isolation vs Frequency

e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18.

INPUT RETURN LOSS=S_{11}dB
S_{11}dB=20 Log | S_{11} |

OUTPUT RETURN LOSS=S_{22}dB
S_{22}dB=20 Log | S_{22} |

INPUT VSWR=≤1.5

OUTPUT VSWR=≤1.5

1DB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

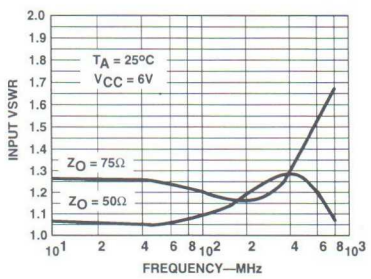
where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA5204A we have chosen an output level of –10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.

ADDITIONAL READING ON SCATTERING PARAMETERS

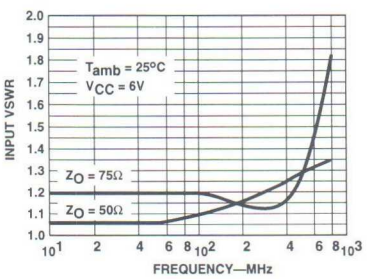
For more information regarding S-parameters, please refer to High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.



a. Input VSWR vs Frequency



b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

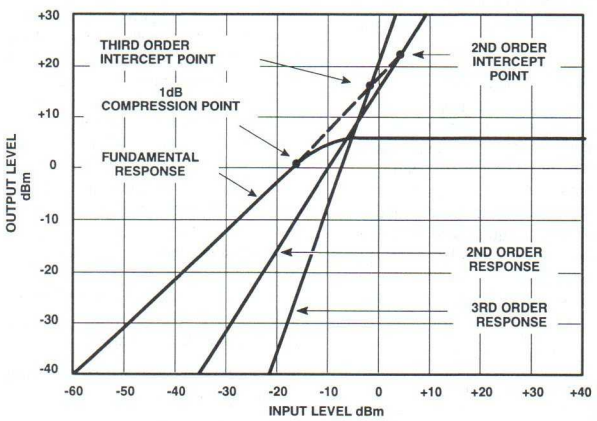

+30
+20
+10
0
-10
-20
-30
-40
OUTPUT LEVEL dBm
THIRD ORDER INTERCEPT POINT
1dB COMPRESSION POINT
FUNDAMENTAL RESPONSE
2ND ORDER INTERCEPT POINT
2ND ORDER RESPONSE
3RD ORDER RESPONSE
-60 -50 -40 -30 -20 -10 0 +10 +20 +30 +40
INPUT LEVEL dBm

Figure 20.

Wide-band high-frequency amplifier

NE/SA/SE5205A

DESCRIPTION

The NE/SA/SE5205A family of wideband amplifiers replace the NE/SA/SE5205 family. The 'A' parts are fabricated on a rugged 2μm bipolar process featuring excellent statistical process control. Electrical performance is nominally identical to the original parts.

The NE/SA/SE5205A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the -3dB bandwidth is greater than 600MHz in the EC package. This performance makes the amplifier ideal for cable TV applications. For lower frequency applications, the part is also available in industrial standard dual in-line and small outline packages. The NE/SA/SE5205A operates with a single supply of 6V, and only draws 24mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA/SE5205A solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the -3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

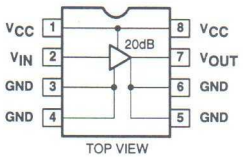
No external components are needed other than AC coupling capacitors because the NE/SA/SE5205A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA/SE5205As in series as required, without any degradation in amplifier stability.

PIN CONFIGURATIONS

N, D Packages



TOP VIEW

FEATURES

- 600MHz bandwidth
- 20dB insertion gain
- 4.8dB (6dB) noise figure ZO=75Ω (ZO=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface mount package available
- MIL-STD processing available
- 2000V ESD protection

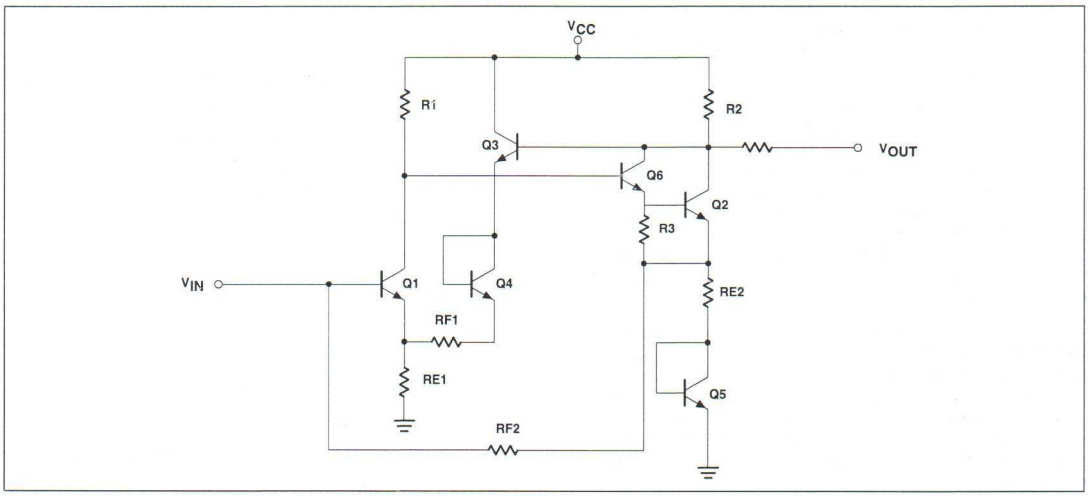
APPLICATIONS

- 75Ω cable TV decoder boxes
- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broad-band LANs
- Fiber-optics
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5205AD	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5205AN	0404B
8-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5205AD	0174C
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5205AN	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-55 to +125°C	SE5205AN	0404B

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{AC}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	-40 to +85	°C
	SE grade	-55 to +125	°C
P_{DMAX}	Maximum power dissipation, T_A=25°C (still-air)[1, 2]		
	N package	1160	mW
	D package	780	mW

NOTES:
1. Derate above 25°C, at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. See "Power Dissipation Considerations" section.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=6V, Z_S=Z_L=Z_O=50Ω and T_A=25°C in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205A			NE/SA5205A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5 5		6.5 6.5	5 5		8 8	V V
I_{CC}	Supply current	Over temperature	20 19	25 25	32 33	20 19	25 25	32 33	mA mA
S21	Insertion gain	f=100MHz Over temperature	17 16.5	19	21 21.5	17 16.5	19	21 21.5	dB
S11	Input return loss	f=100MHz D, N		25			25		dB
		DC - f_{MAX} D, N	12			12			
S22	Output return loss	f=100MHz D, N		27			27		dB
		DC - f_{MAX}	12			12			
S12	Isolation	f=100MHz		-25			-25		dB
		DC - f_{MAX}	-18			-18			
t_R	Rise time			500			500		ps
t_P	Propagation delay			500			500		ps
BW	Bandwidth	±0.5dB D, N		300			450		MHz
f_{MAX}	Bandwidth	-3dB D, N				550			MHz
	Noise figure (75Ω)	f=100MHz		4.8			4.8		dB
	Noise figure (50Ω)	f=100MHz		6.0			6.0		dB
	Saturated output power	f=100MHz		+7.0			+7.0		dBm
	1dB gain compression	f=100MHz		+4.0			+4.0		dBm
	Third-order intermodulation intercept (output)	f=100MHz		+17			+17		dBm
	Second-order intermodulation intercept (output)	f=100MHz		+24			+24		dBm

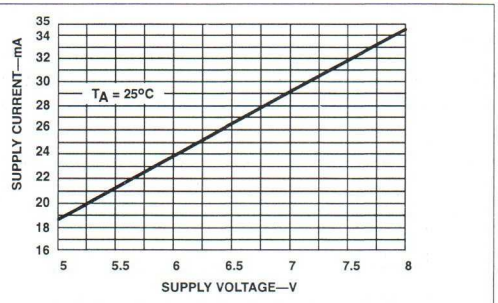


Figure 1. Supply Current vs Supply Voltage

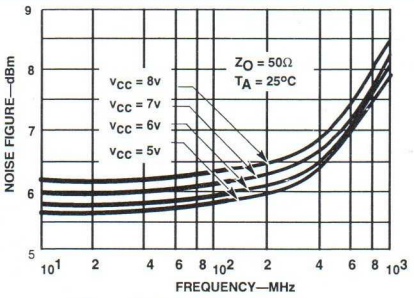


Figure 2. Noise Figure vs Frequency

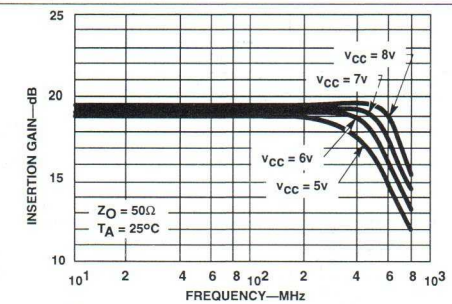


Figure 3. Insertion Gain vs Frequency (S_{21})

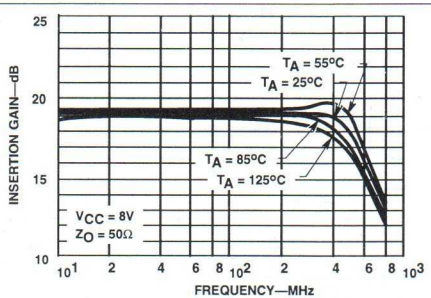


Figure 4. Insertion Gain vs Frequency (S_{21})

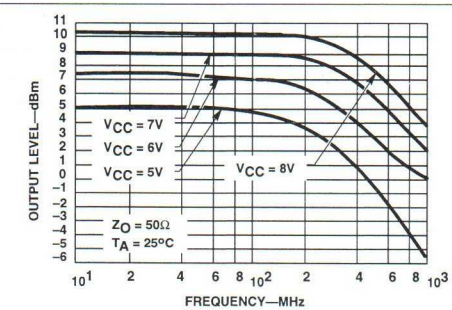


Figure 5. Saturated Output Power vs Frequency

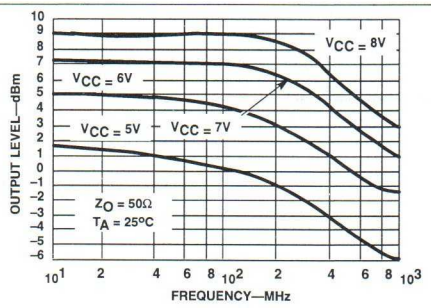


Figure 6. 1dB Gain Compression vs Frequency

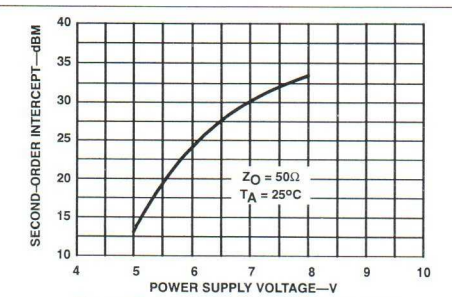


Figure 7. Second-Order Output Intercept vs Supply Voltage

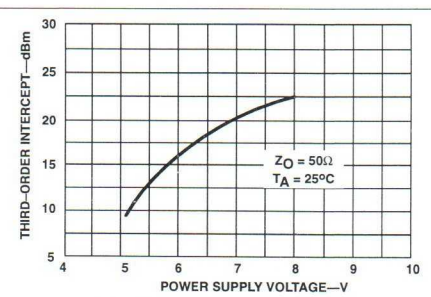


Figure 8. Third-Order Intercept vs Supply Voltage

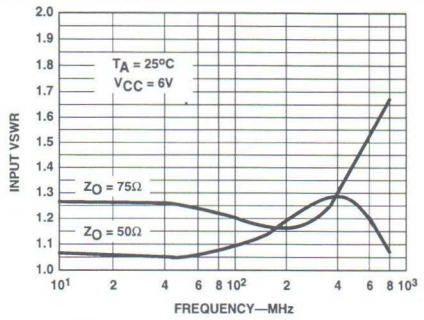


Figure 9. Input VSWR vs Frequency

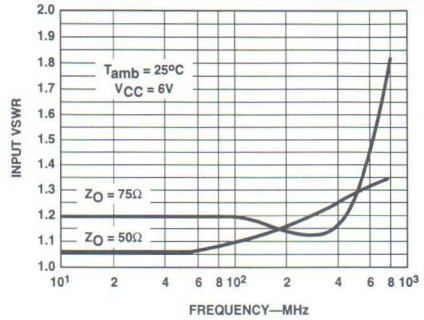


Figure 10. Output VSWR vs Frequency

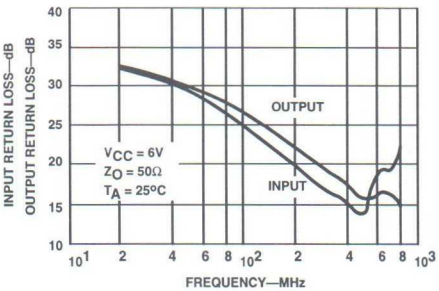


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

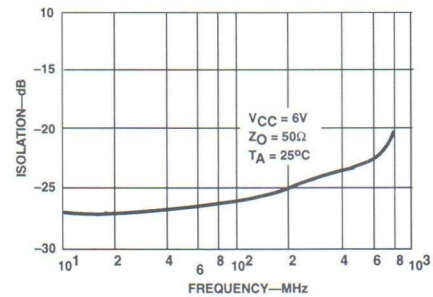


Figure 12. Isolation vs Frequency (S_{12})

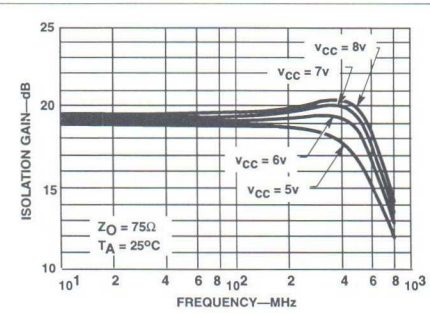


Figure 13. Insertion Gain vs Frequency (S_{21})

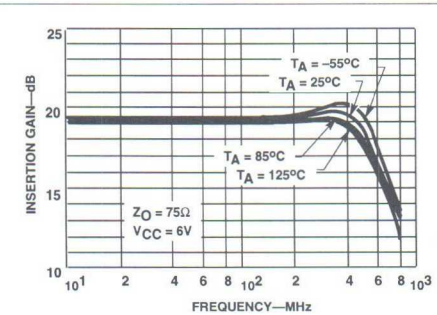


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = \frac{(R_{F1} + R_{E1})}{R_{E1}} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10 \log \left[1 + \left[\frac{r_b + R_{E1} + \frac{KT}{2qI_{C1}}}{R_O} \right] \right] dB \quad (2)$$

where I_{C1}=5.5mA, R_{E1}=12Ω, r_b=130Ω, KT/q=26mV at 25°C and R_0=50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN}=V_{BE1}+(I_{C1}+I_{C3})\ R_{E1}$$

where R_{E1}=12Ω, V_{BE}=0.8V, I_{C1}=5mA and I_{C3}=7mA (currents rated at V_{CC}=6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of R_{F1}=140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT}=V_{CC}-(I_{C2}+I_{C6})R2,(4)$$

where V_{CC}=6V, R_2=225Ω, I_{C2}=8mA and I_{C6}=5mA.

From here it can be seen that the output voltage is approximately 3.1V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

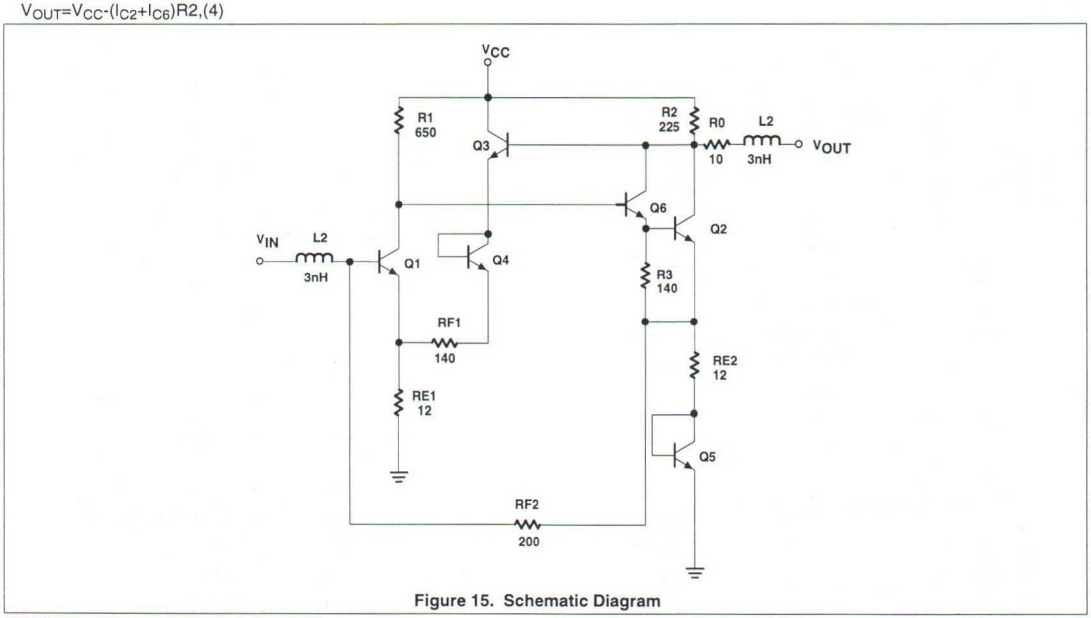


Figure 15. Schematic Diagram

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (32mA Max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the D package body against the PC board plane.

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5205A to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the SO package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection.

Another important consideration is that the input and output should be AC coupled. This is because at V_{CC}=6V, the input is approximately at 1V while the output is at 3.1V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the NE/SA/SE5205A are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5205A to other high-frequency amplifiers.

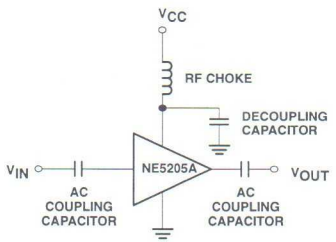
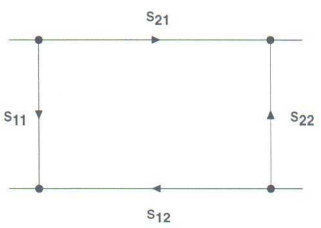


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling



a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} = \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OSOLATION

$$S_{12} = \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} = \sqrt{\text{TRANSDUCER POWER GAIN}}$$

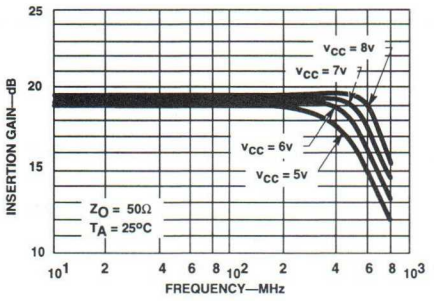
S_{22} — OUTPUT RETURN LOSS

$$S_{22} = \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

b.

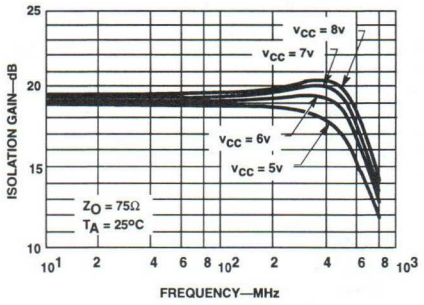
Figure 17.

50Ω System

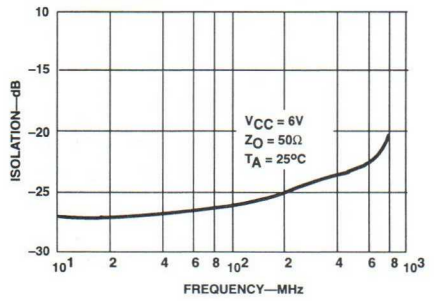


a. Insertion Gain vs Frequency (S_{21})

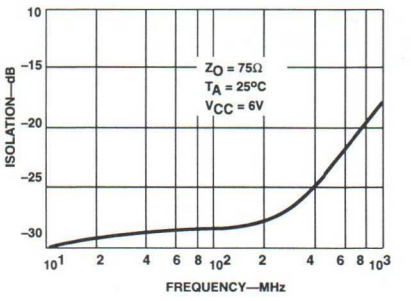
75Ω System



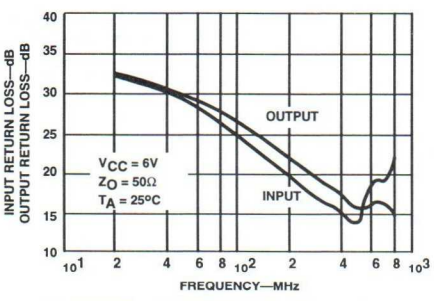
b. Insertion Gain vs Frequency (S_{21})



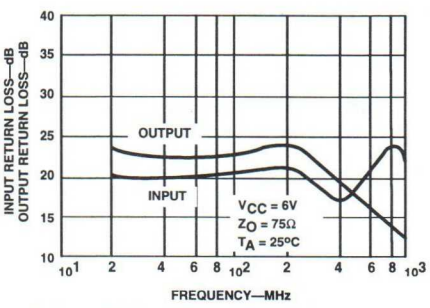
c. Isolation vs Frequency (S_{12})



d. S_{12} Isolation vs Frequency



e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency



f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18.

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D=Z_{IN}=Z_{OUT}$ for the NE/SA/SE5205A



$$P_{IN} + \frac{V_{IN}^2}{Z_D} \qquad P_{OUT} + \frac{V_{OUT}^2}{Z_D}$$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I=V_I^2$

P_I=Insertion Power Gain

V_I=Insertion Voltage Gain

Measured value for the
NE/SA/SE5205A = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20dB$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20dB$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20dB$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS=S_{11}dB
$S_{11}dB=20 \text{ Log } |S_{11}|$

OUTPUT RETURN LOSS=S_{22}dB
$S_{22}dB=20 \text{ Log } |S_{22}|$

INPUT VSWR=≤1.5

OUTPUT VSWR=≤1.5

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

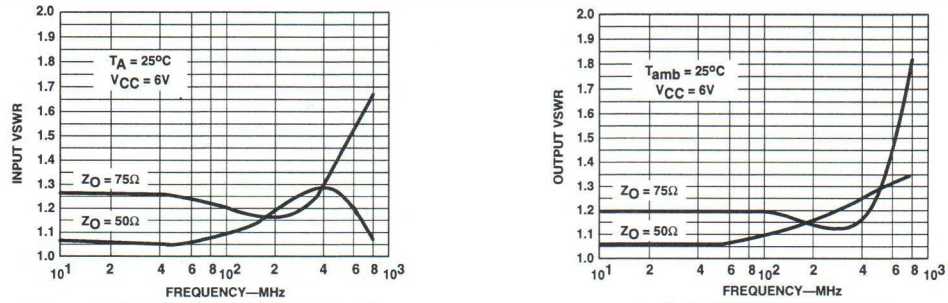
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$IP_2=P_{OUT}+IMR_2$

$IP_3=P_{OUT}+IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA/SE5205A we have chosen an output level of -10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.



a. Input VSWR vs Frequency

b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

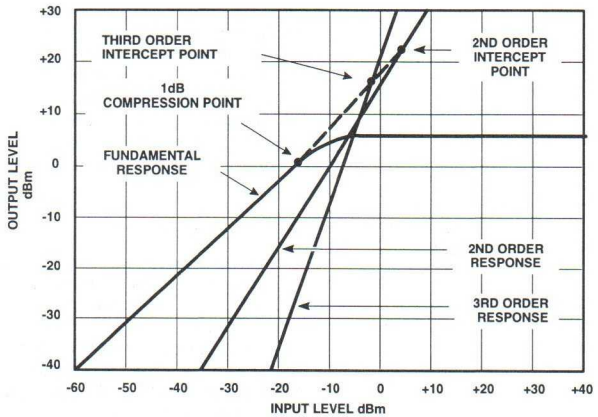


Figure 20.

Wideband variable gain amplifier NE/SA5209

DESCRIPTION

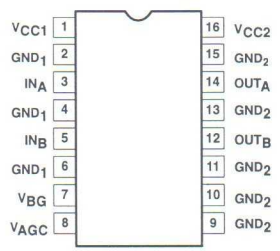
The NE5209 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5209 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5209 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

PIN CONFIGURATION

N, D PACKAGES



FEATURES

- Gain to 1.5GHz
- 850MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

ORDERING INFORMATION

DESCPIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5209D	0005D
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5209N	0406C
16-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5209D	0005D
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5209N	0406C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   16-Pin DIP: θ_{JA} = 85°C/W
   16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	V_{CC1} = V_{CC2} = 4.5 to 7.0V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	38	43	48	mA
		Over temperature[1]	30		55	
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	17	19	21	dB
		Over temperature[1]	16		22	
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	23	25	27	dB
		Over temperature[1]	22		28	
R_{IN}	Input resistance (single-ended)	DC tested at ±50μA	0.9	1.2	1.5	kΩ
		Over temperature[1]	0.8		1.7	
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	40	60	75	Ω
		Over temperature[1]	35		90	
V_{OS}	Output offset voltage (output referred)			±20	±100	mV
		Over temperature[1]			±250	
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
		Over temperature[1]	1.4		2.6	
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
		Over temperature[1]	1.7		3.1	
PSRR	Output offset supply rejection ratio (output referred)		20	45		dB
		Over temperature[1]	15			
V_{BG}	Bandgap reference voltage	4.5V<V_{CC}<7V R_{BG} = 10kΩ	1.2	1.32	1.45	V
		Over temperature[1]	1.1		1.55	

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
R_{BG}	Bandgap loading	Over temperature[1]	2	10		kΩ
V_{AGC}	AGC DC control voltage range	Over temperature[1]		0-1.3		V
I_{BAGC}	AGC pin DC bias current	0V<V_{AGC}<1.3V		-0.7	-6	μA
		Over temperature[1]			-10	

NOTES:

1. "Over Temperature Range" testing is as follows:
   NE is 0 to +70°C
   SA is -40 to +85°C
   At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	-3dB bandwidth		600	850		MHz
		Over temperature[1]	500			
GF	Gain flatness	DC - 500MHz		±0.4		dB
		Over temperature[1]		±0.6		
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[2]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended) for linear operation[2]	R_L = 50Ω		400		mV_{P-P}
		R_L = 1kΩ		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	R_S = 50Ω, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		$nV/\sqrt{Hz}$
S12	Reverse isolation	f = 100MHz		-60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	R_L = 50Ω		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	-3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		-3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		-10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:

1. "Over Temperature Range" testing is as follows:
   NE is 0 to +70°C
   SA is -40 to +85°C
   At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.
2. With R_L > 1kΩ, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With R_L = 50Ω, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

NE5209 APPLICATIONS

The NE5209 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 1. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The NE5209 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 - 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The NE5209 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5209 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The NE5209 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the NE5209. A maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the NE5209 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the NE5209 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the NE5209 is shown in Figure 2. Three NE5209s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An NE5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three NE5209s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three NE5209s will give a dynamic range in excess of 60dB.

The NE5209 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

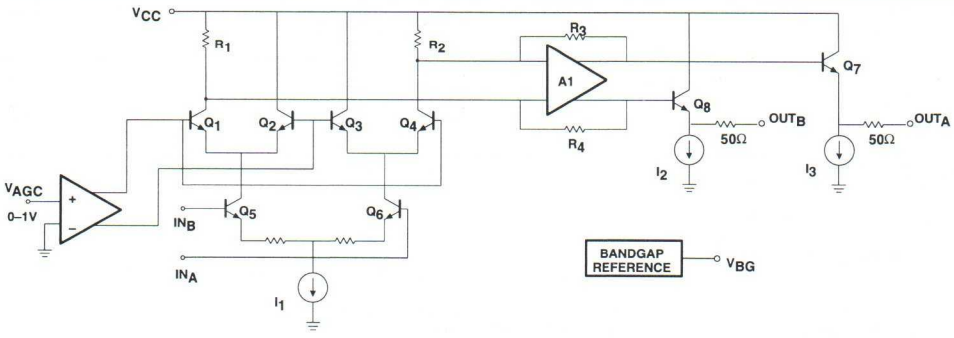


Figure 1. Equivalent Schematic of the VGA

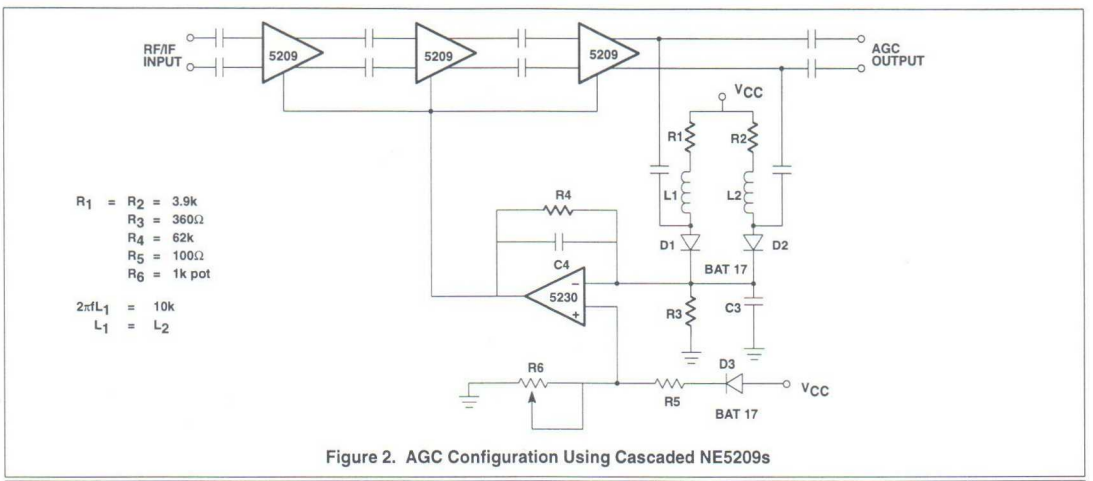


Figure 2. AGC Configuration Using Cascaded NE5209s

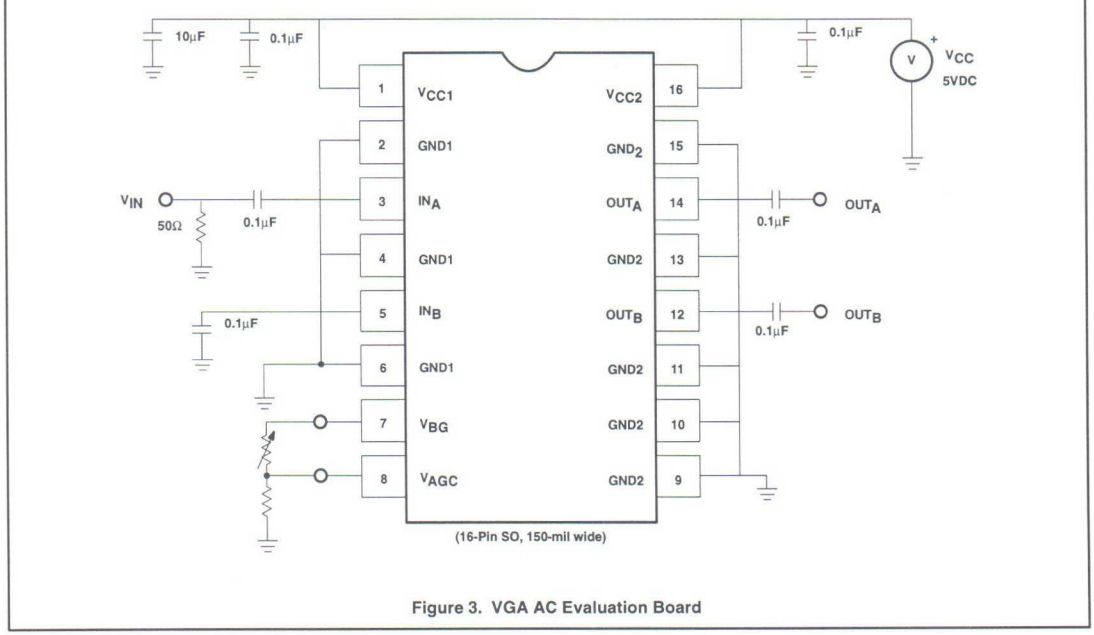
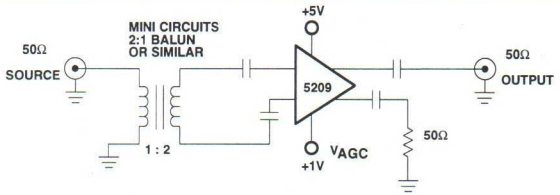
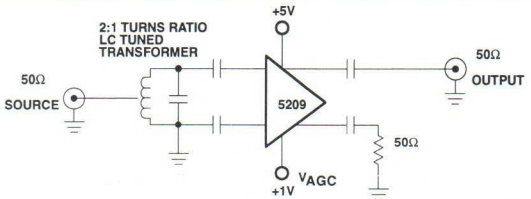


Figure 3. VGA AC Evaluation Board



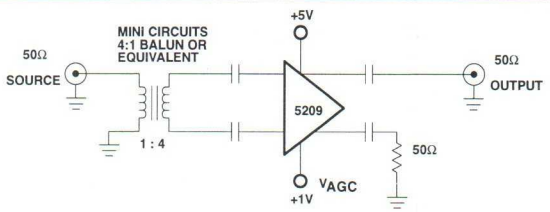
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain.

Figure 4. Broadband Noise Optimization



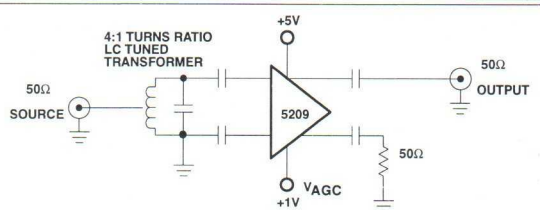
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain. Narrowband circuits have the advantage of greater stability, particularly when multiple devices are cascaded.

Figure 5. Narrowband Noise Optimization



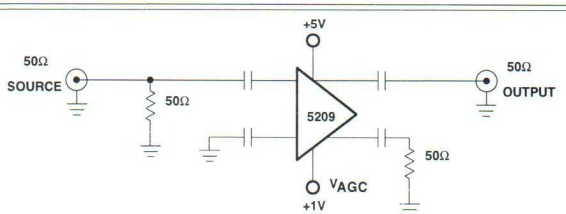
This circuit will exhibit about an 8dB noise figure with 24dB gain.

Figure 6. Broadband Gain Optimization



This circuit will exhibit approximately an 8dB noise figure and 25dB gain.

Figure 7. Narrowband Gain Optimization



The noise figure of this configuration will be approximately 15dB.

Figure 8. Simple Amplifier Configuration

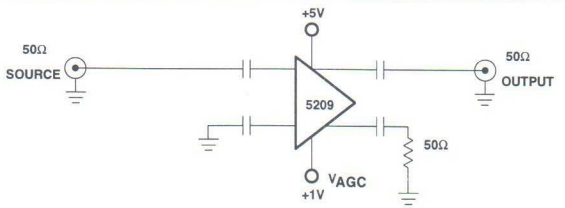


Figure 9. Unterminated Configuration

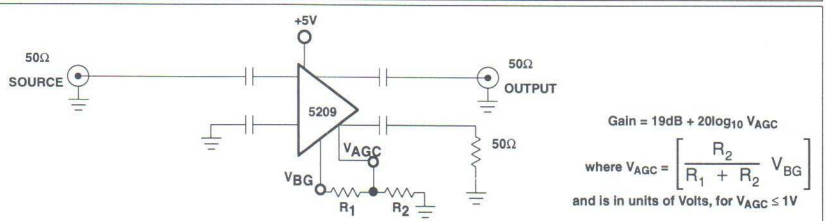


Figure 10. User-Programmable Fixed Gain Block

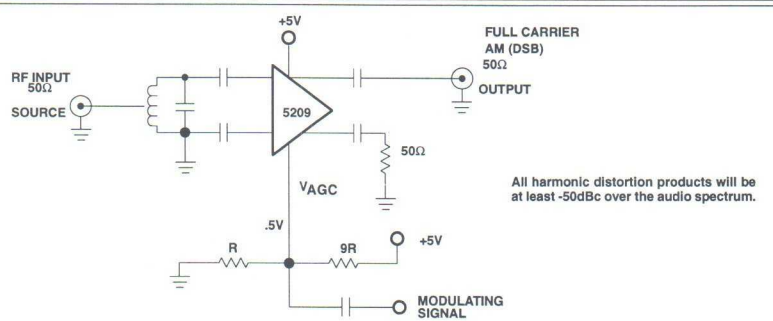


Figure 11. AM Modulator

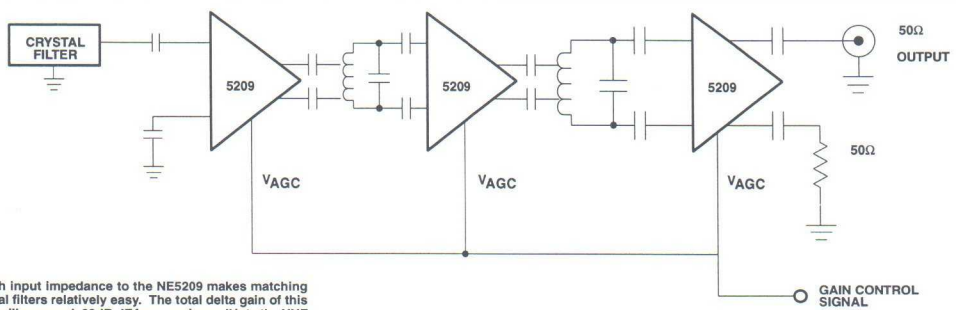


Figure 12. Receiver AGC IF Gain

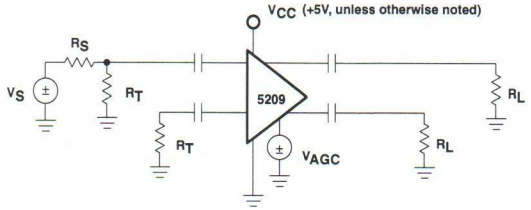


Figure 13. Test Set-up 1 (Used for all Graphs)

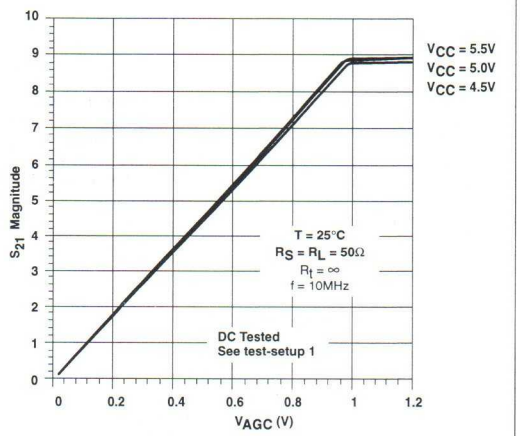


Figure 14. Gain vs V_{AGC} and V_{CC}

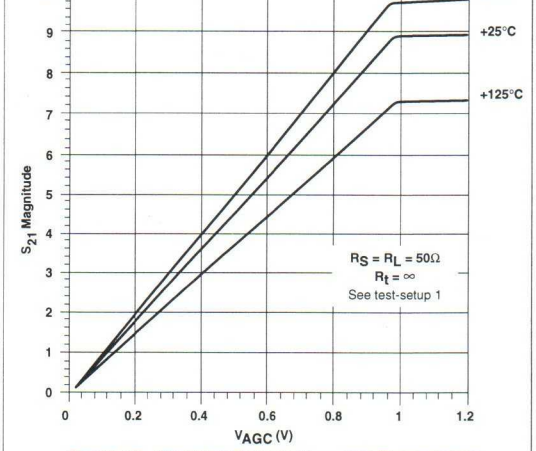


Figure 15. Insertion Gain vs V_{AGC} and Temperature

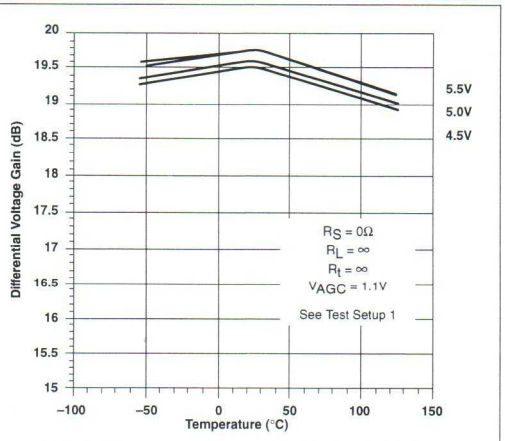


Figure 16. Voltage Gain vs Temperature and V_{CC}

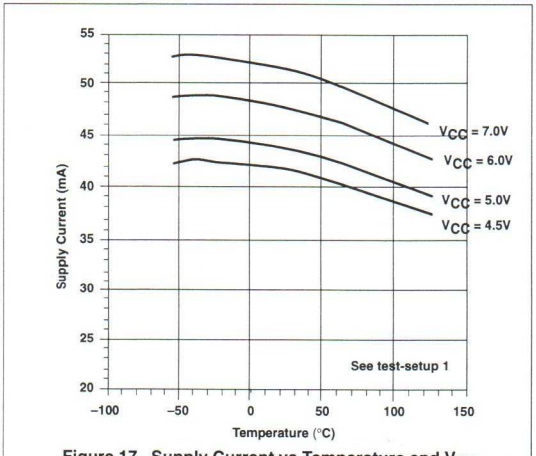


Figure 17. Supply Current vs Temperature and V_{CC}

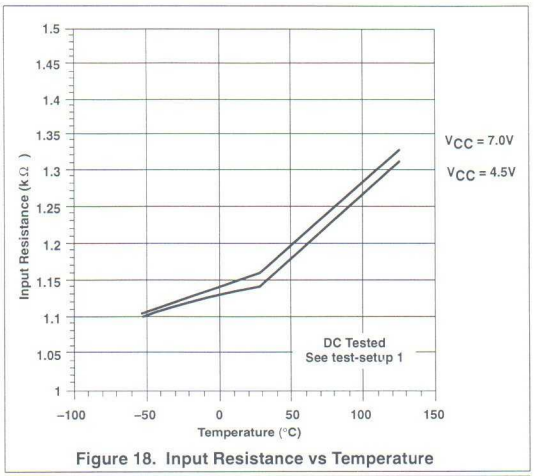


Figure 18. Input Resistance vs Temperature

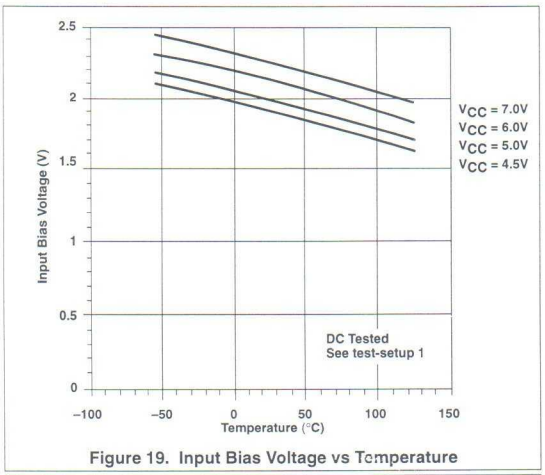


Figure 19. Input Bias Voltage vs Temperature

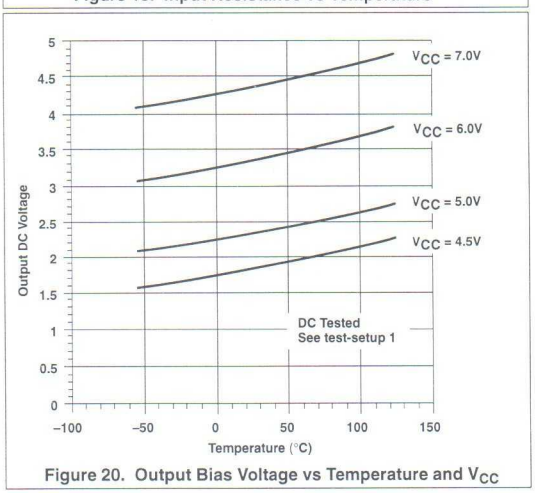


Figure 20. Output Bias Voltage vs Temperature and V_{CC}

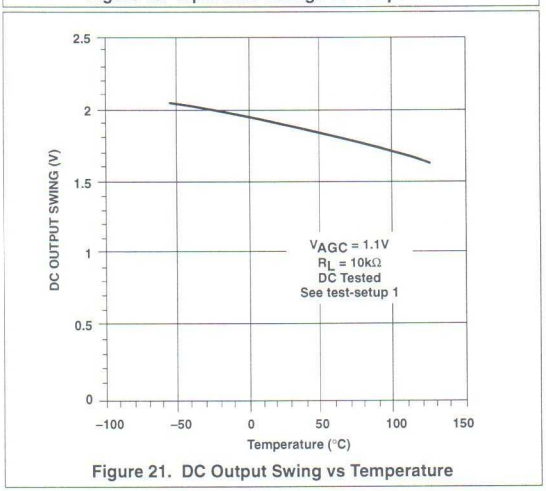


Figure 21. DC Output Swing vs Temperature

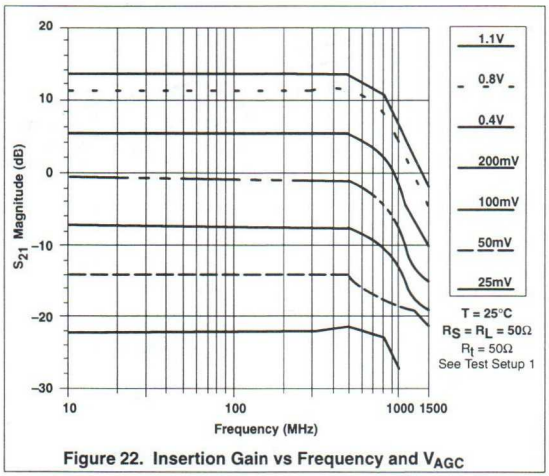


Figure 22. Insertion Gain vs Frequency and V_{AGC}

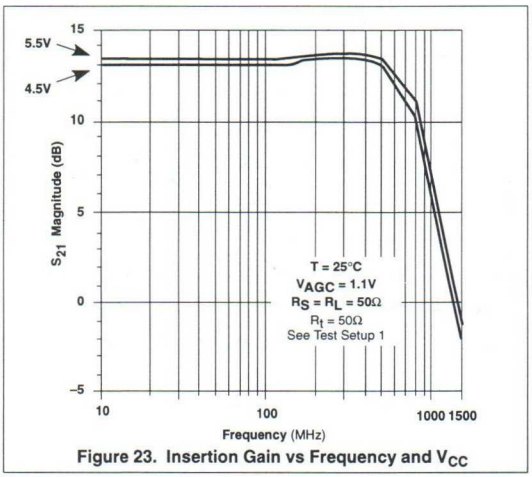


Figure 23. Insertion Gain vs Frequency and V_{CC}

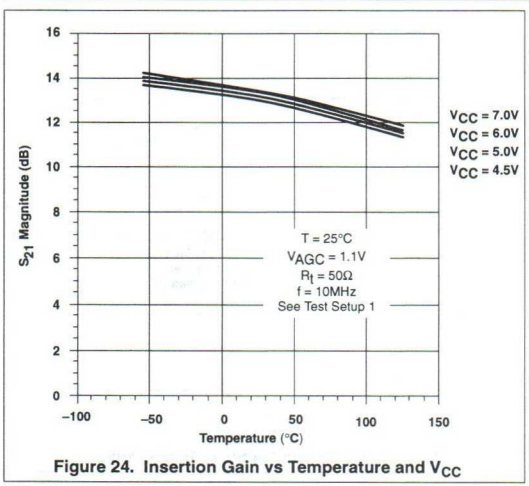


Figure 24. Insertion Gain vs Temperature and V_{CC}

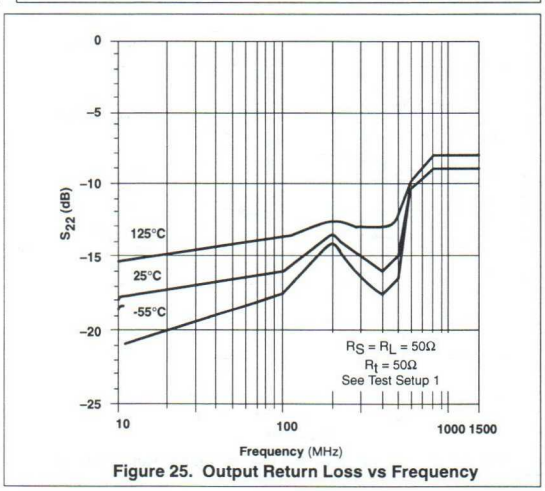


Figure 25. Output Return Loss vs Frequency

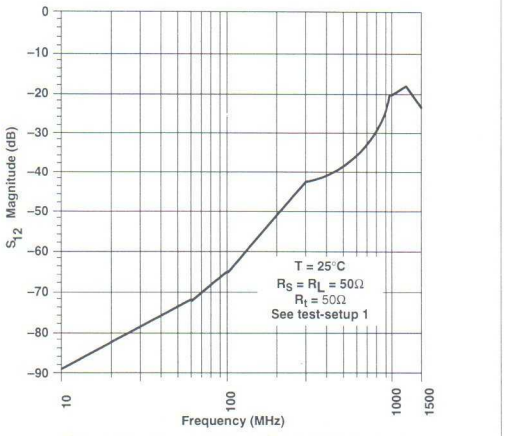


Figure 26. Reverse Isolation vs Frequency

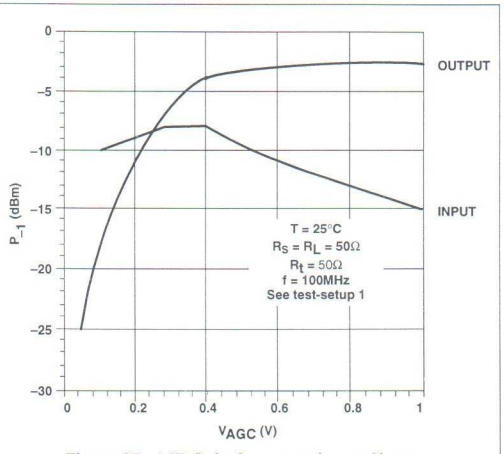


Figure 27. 1dB Gain Compression vs V_{AGC}

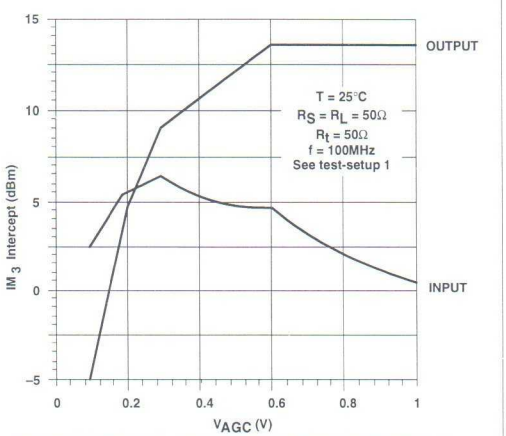


Figure 28. Third-Order Intermodulation Intercept vs V_{AGC}

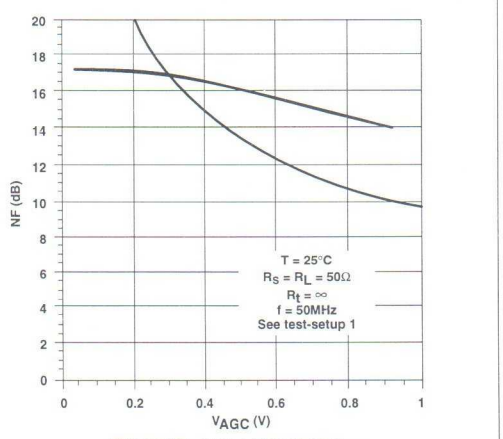


Figure 29. Noise Figure vs V_{AGC}

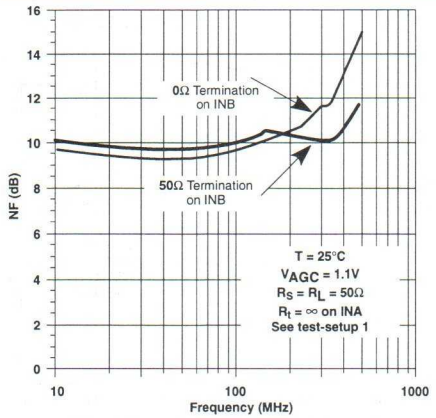


Figure 30. Noise Figure vs Frequency

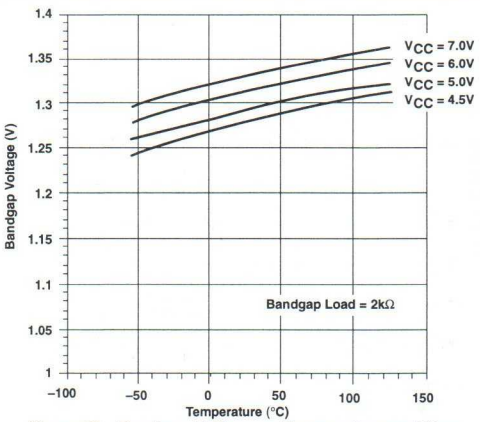


Figure 31. Bandgap Voltage vs Temperature and V_{CC}

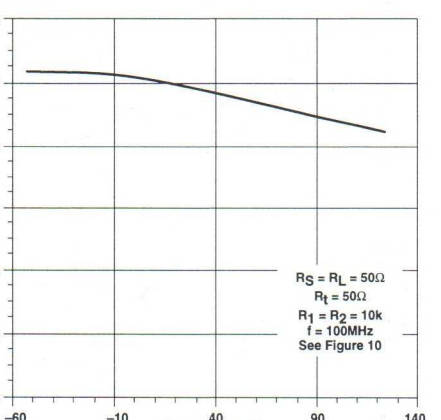
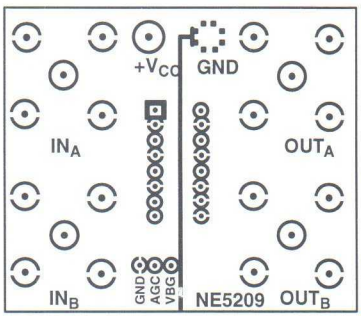
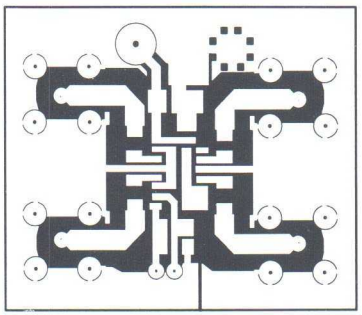


Figure 32. Fixed Gain vs Temperature

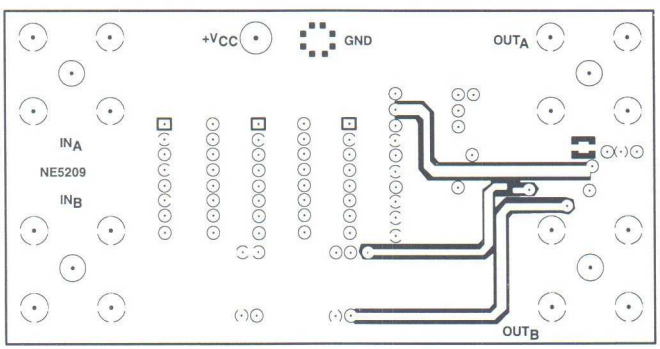


TOP VIEW - COMPONENT SIDE

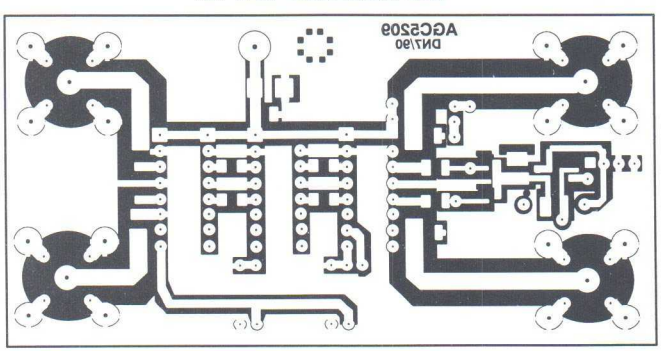


TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout

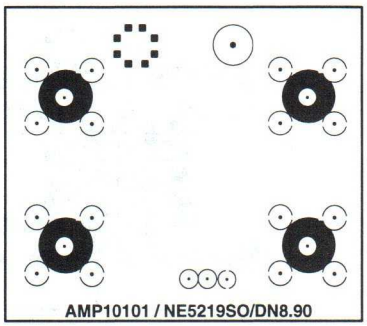


TOP VIEW - COMPONENT SIDE

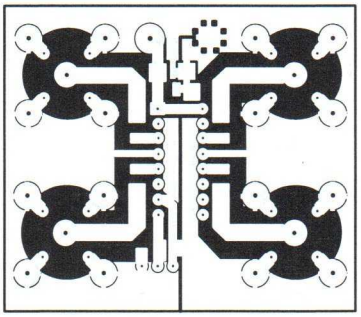


TOP VIEW - SOLDER SIDE

AGC Configuration Using Cascaded NE5209s - Layout



TOP VIEW - COMPONENT SIDE



TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout (DIP Package)

High frequency operational amplifier NE/SE5539

DESCRIPTION

The NE/SE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter-follower inputs provide a true differential input impedance device. Proper external compensation will allow design operation over a wide range of closed-loop gains, both inverting and non-inverting, to meet specific design requirements.

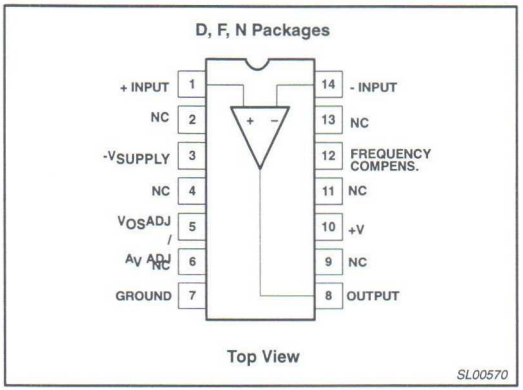
FEATURES

- Bandwidth
  - Unity gain - 350MHz
  - Full power - 48MHz
  - GBW - 1.2GHz at 17dB
- Slew rate: 600/Vμs
- A_{VOL}: 52dB typical
- Low noise - 4nV√Hz typical
- MIL-STD processing available

APPLICATIONS

- High speed datacom
- Video monitors & TV
- Satellite communications
- Image processing
- RF instrumentation & oscillators
- Magnetic storage
- Military communications

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5539N	0405B
14-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5539D	0175D
14-Pin Ceramic Dual In-Line Package	0 to +70°C	NE5539F	0581B
14-Pin Ceramic Dual In-Line Package	-55 to +125°C	SE5539F	0581B

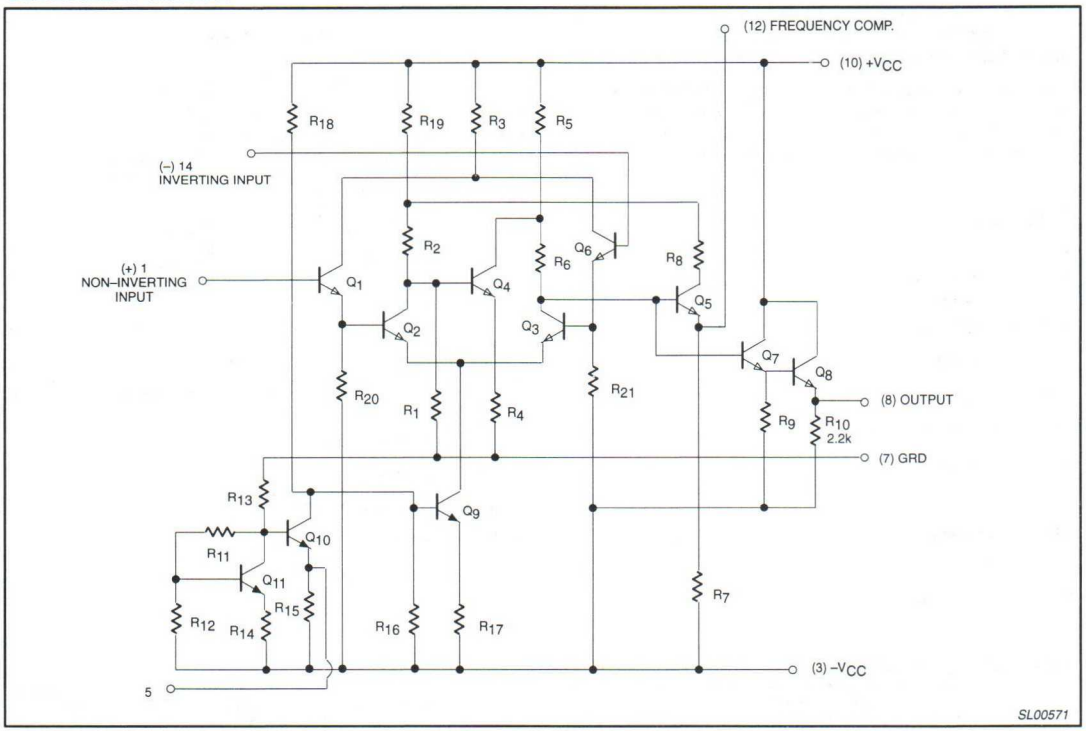
ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	±12	V
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[2]		
	F package	1.17	W
	N package	1.45	W
	D package	0.99	W
T_A	Operating temperature range		
	NE	0 to 70	°C
	SE	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Max junction temperature	150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:

1. Differential input voltage should not exceed 0.25V to prevent excesive input bias current and common-mode voltage 2.5V. These voltage limits may be exceeded if current is limited to less than 10mA.
2. Derate above 25°C, at the following rates:
   F package at 9.3mW/°C
   N package at 11.6mW/°C
   D package at 7.9mW/°C

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

V_{CC} = ±8V, T_A = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			NE5539			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input offset voltage	V_O = 0V, R_S = 100Ω	Over temp		2	5				mV
			T_A = 25°C		2	3		2.5	5	
	$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Input offset current		Over temp		0.1	3				µA
			T_A = 25°C		0.1	1			2	
	$\Delta I_{OS}/\Delta T$				0.5			0.5		nA/°C
I_B	Input bias current		Over temp		6	25				µA
			T_A = 25°C		5	13		5	20	
	$\Delta I_B/\Delta T$				10			10		nA/°C
CMRR	Common mode rejection ratio	F = 1kHz, R_S = 100Ω, V_{CM} ±1.7V		70	80		70	80		dB
			Over temp	70	80					
R_{IN}	Input impedance				100			100		kΩ
R_{OUT}	Output impedance				10			10		Ω

DC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = ±8V, T_A = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			NE5539			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OUT}	Output voltage swing	R_L = 150Ω to GND and 470Ω to -V_{CC}	+Swing -Swing				+2.3 -1.7	+2.7 -2.2		V
V_{OUT}	Output voltage swing	R_L = 25Ω to GND Over temp	+Swing -Swing	+2.3 -1.5	+3.0 -2.1					V
		R_L = 25Ω to GND T_A = 25°C	+Swing -Swing	+2.5 -2.0	+3.1 -2.7					
I_{CC+}	Positive supply current	V_O = 0, R_1 = ∞, Over temp			14	18				mA
		V_O = 0, R_1 = ∞, T_A = 25°C			14	17		14	18	
I_{CC-}	Negative supply current	V_O = 0, R_1 = ∞, Over temp			11	15				mA
		V_O = 0, R_1 = ∞, T_A = 25°C			11	14		11	15	
PSRR	Power supply rejection ratio	ΔV_{CC} = ±1V, Over temp			300	1000				µV/V
		ΔV_{CC} = ±1V, T_A = 25°C						200	1000	
A_{VOL}	Large signal voltage gain	V_O = +2.3V, -1.7V, R_L = 150Ω to GND, 470Ω to -V_{CC}					47	52	57	dB
A_{VOL}	Large signal voltage gain	V_O = +2.3V, -1.7V	Over temp							dB
		R_L = 2Ω to GND	T_A = 25°C				47	52	57	
A_{VOL}	Large signal voltage gain	V_O = +2.5V, -2.0V	Over temp	46		60				dB
		R_L = 2Ω to GND	T_A = 25°C	48	53	58				

DC ELECTRICAL CHARACTERISTICS

V_{CC} = ±6V, T_A = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			UNITS
					MIN	TYP	MAX	
V_{OS}	Input offset voltage			Over temp		2	5	mV
				T_A = 25°C		2	3	
I_{OS}	Input offset current			Over temp		0.1	3	µA
				T_A = 25°C		0.1	1	
I_B	Input bias current			Over temp		5	20	µA
				T_A = 25°C		4	10	
CMRR	Common-mode rejection ratio	V_{CM} = ±1.3V, R_S = 100Ω			70	85		dB
I_{CC+}	Positive supply current			Over temp		11	14	mA
				T_A = 25°C		11	13	
I_{CC-}	Negative supply current			Over temp		8	11	mA
				T_A = 25°CmA		8	10	
PSRR	Power supply rejection ratio	ΔV_{CC} = ±1V		Over temp		300	1000	µV/V
				T_A = 25°C				
V_{OUT}	Output voltage swing	R_L = 150Ω to GND and 390Ω to –V_{CC}	Over temp	+Swing	+1.4	+2.0		V
				–Swing	–1.1	–1.7		
			T_A = 25°C	+Swing	+1.5	+2.0		
				–Swing	–1.4	–1.8		

AC ELECTRICAL CHARACTERISTICS

V_{CC} = ±8V, R_L = 150Ω to GND and 470Ω to -V_{CC}, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
BW	Gain bandwidth product	A_{CL} = 7, V_O = 0.1 V_{P-P}		1200			1200		MHz
	Small signal bandwidth	A_{CL} = 2, R_L = 150Ω[1]		110			110		MHz
t_S	Settling time	A_{CL} = 2, R_L = 150Ω[1]		15			15		ns
SR	Slew rate	A_{CL} = 2, R_L = 150Ω[1]		600			600		V/µs
t_{PD}	Propagation delay	A_{CL} = 2, R_L = 150Ω[1]		7			7		ns
	Full power response	A_{CL} = 2, R_L = 150Ω[1]		48			48		MHz
	Full power response	A_V = 7, R_L = 150Ω[1]		20			20		MHz
	Input noise voltage	R_S = 50Ω, 1MHz		4			4		nV/√Hz
	Input noise current	1MHz		6			6		pA/√Hz

NOTES:
1. External compensation.

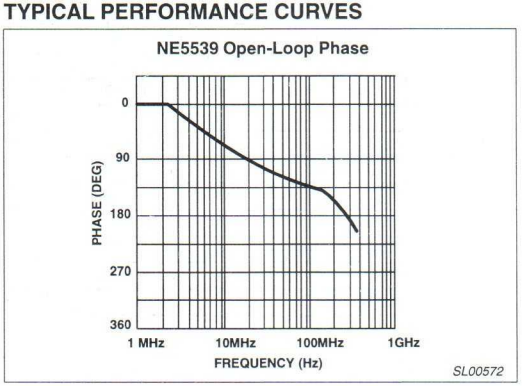
AC ELECTRICAL CHARACTERISTICS

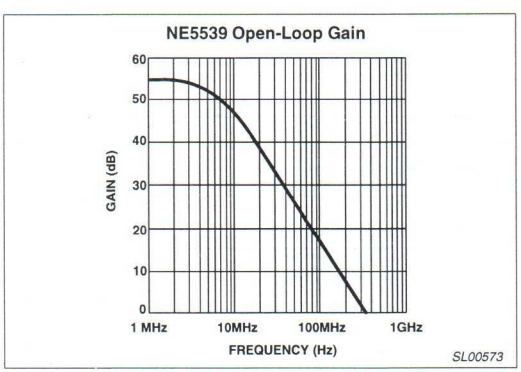
V_{CC} = ±6V, R_L = 150Ω to GND and 390Ω to -V_{CC}, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			UNITS
			MIN	TYP	MAX	
BW	Gain bandwidth product	A_{CL} = 7		700		MHz
	Small signal bandwidth	A_{CL} = 2[1]		120		
t_S	Settling time	A_{CL} = 2[1]		23		ns
SR	Slew rate	A_{CL} = 2[1]		330		V/µs
t_{PD}	Propagation delay	A_{CL} = 2[1]		4.5		ns
	Full power response	A_{CL} = 2[1]		20		MHz

NOTES:
1. External compensation.

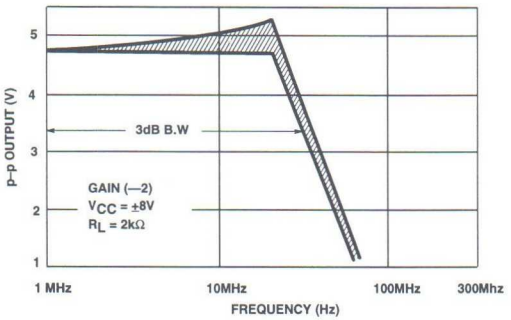
TYPICAL PERFORMANCE CURVES



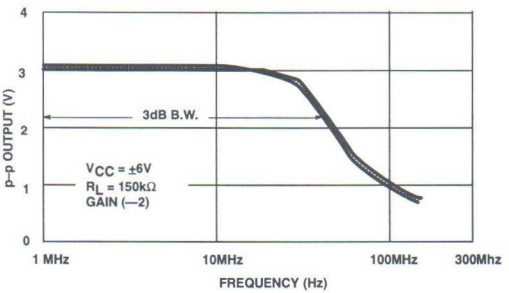


TYPICAL PERFORMANCE CURVES (Continued)

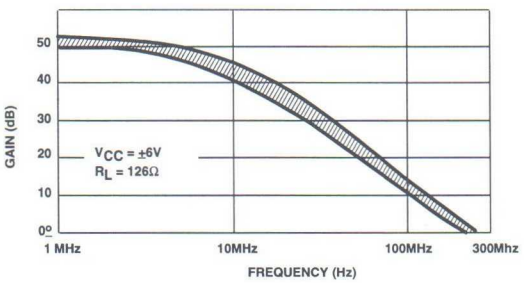
Power Bandwidth (SE)



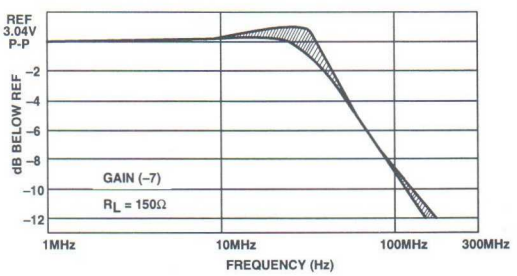
Power Bandwidth (NE)



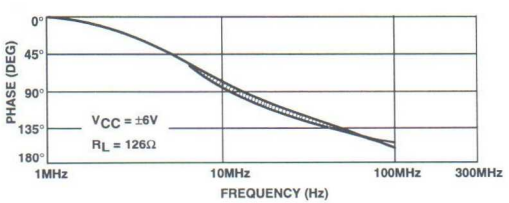
SE5539 Open-Loop Gain vs Frequency



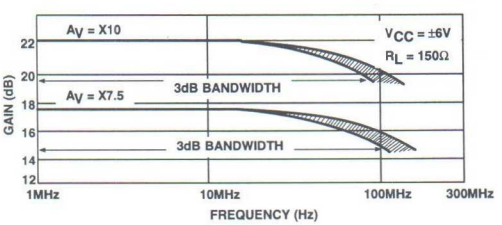
Power Bandwidth



SE5539 Open-Loop Phase vs Frequency



Gain Bandwidth Product vs Frequency



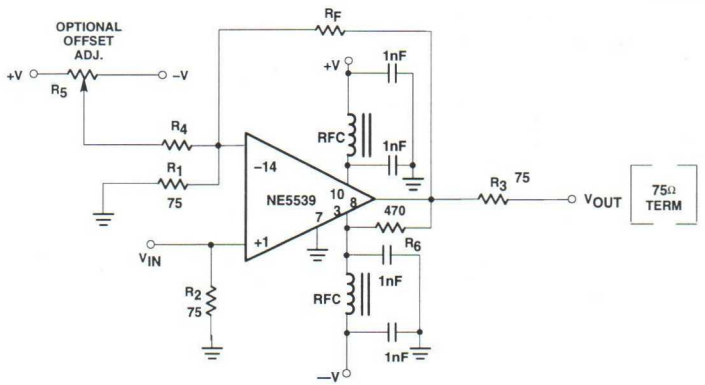
NOTE:

Indicates typical distribution $-55°C \leq T_A \leq 125°C$

SL00574

CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide-gain bandwidth amplifier, the physical circuit is extremely critical. Bread-boarding is not recommended. A double-sided copper-clad printed circuit board will result in more favorable system operation. An example utilizing a 28dB non-inverting amp is shown in Figure 1.

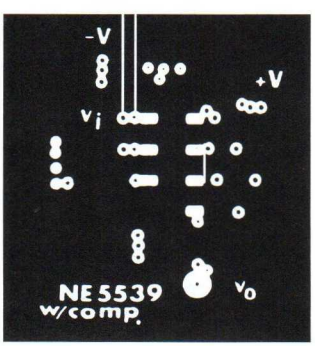


R_1 = 75Ω 5% CARBON
R_2 = 75Ω 5% CARBON
R_3 = 75Ω 5% CARBON
R_4 = 36K 5% CARBON

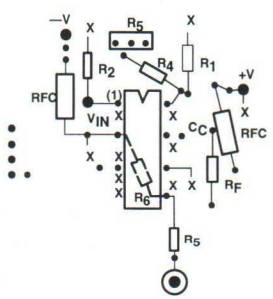
R_5 = 20k TRIMPOT (CERMET)
R_F = 1.5k (28dB GAIN)
R_6 = 470Ω 5% CARBON

RFC 3T # 26 BUSS WIRE ON FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)

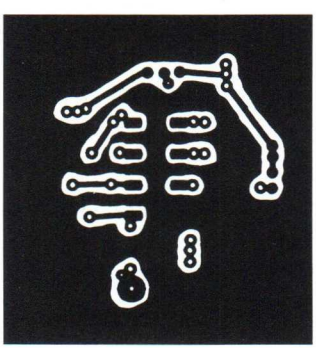
Top Plane Copper[1] (Component Side)



Component Side (Component Layout)



Bottom Plane Copper[1]



SL00575

Figure 1. 28dB Non-Inverting Amp Sample PC Layout

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wideband operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown in Figure 2 along with vector-scope1 photographs showing the amplifier differential gain and phase response to a standard five-step modulated staircase linearity signal (Figures 3, 4 and 5). As can be seen in Figure 4, the gain varies less than 0.5% from the bottom to the top of the staircase. The maximum differential phase shown in Figure 5 is approximately +0.1°.

The amplifier circuit was optimized for a 75Ω input and output termionation impedance with a gain of approximately 10 (20dB).

NOTE:

1. The input signal was 200mV and the output 2V. V_{CC} was ±8V.

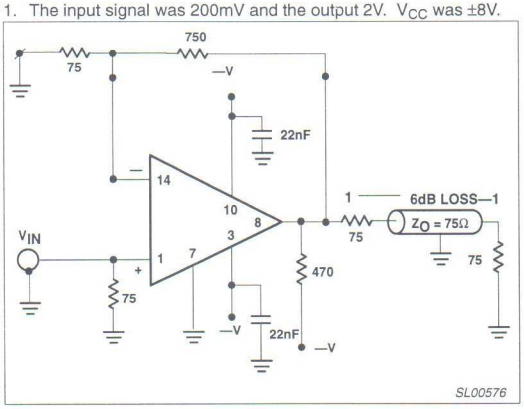


Figure 2. NE5539 Video Amplifier

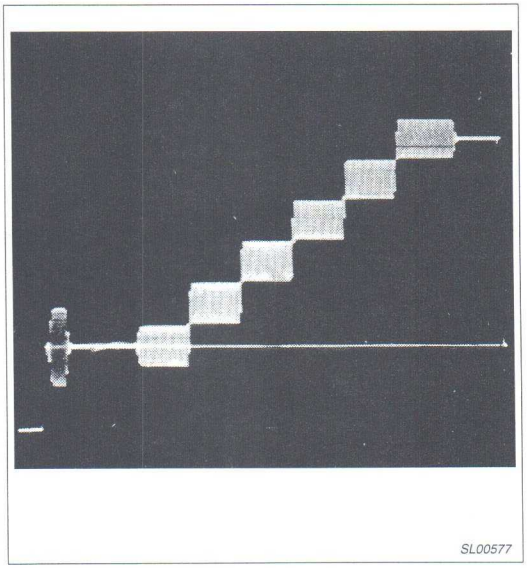


Figure 3. Input Signal

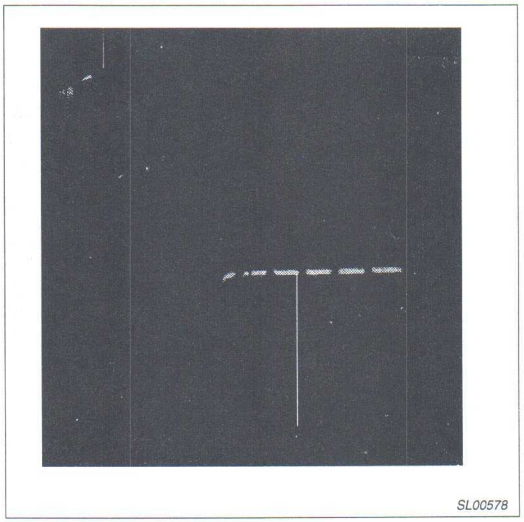


Figure 4. Differential Gain <0.5%

NOTE:

Instruments used for these measurements were Tektronix 146 NTSC test signal generator, 520A NTSC vectorscope, and 1480 waveform monitor.

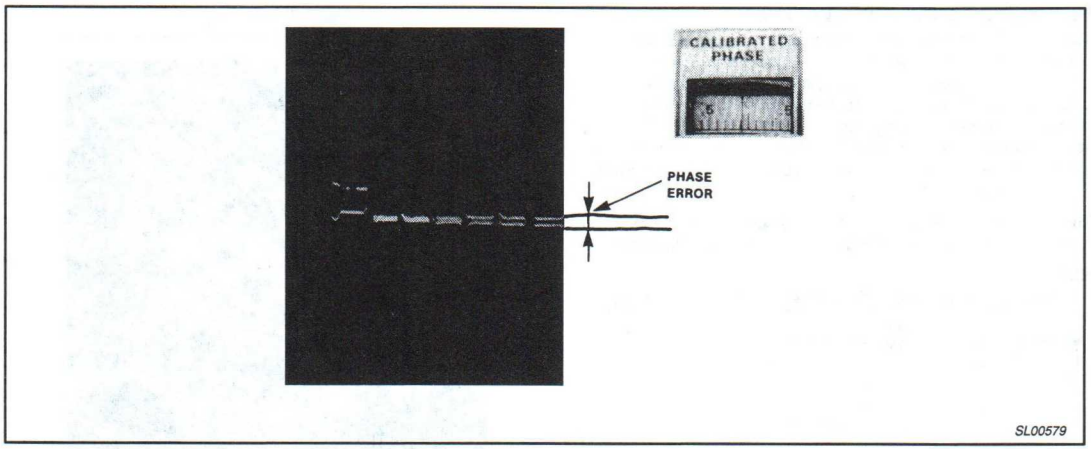


Figure 5. Differential Gain +0.1°

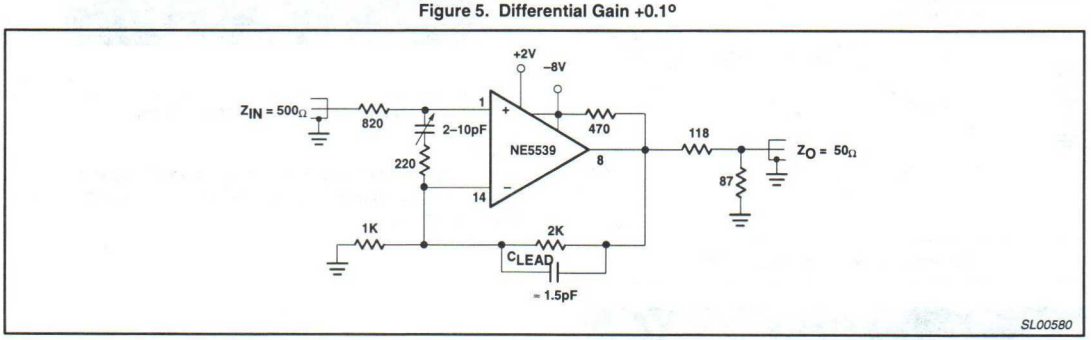


Figure 6. Non-Inverting Follower

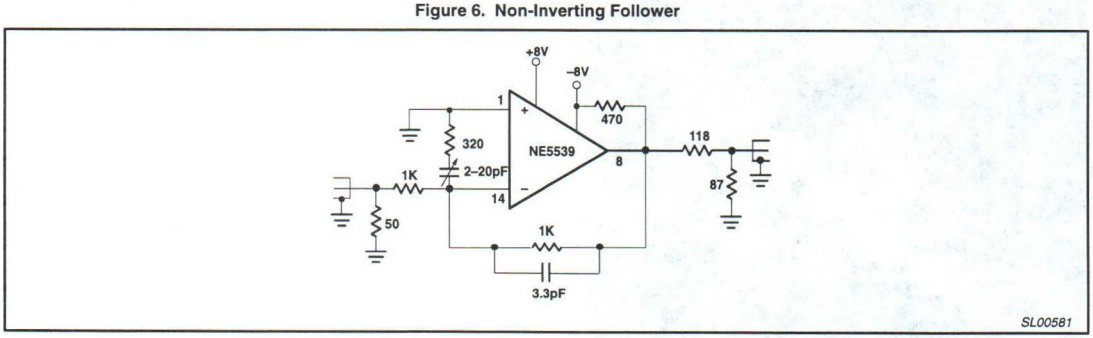


Figure 7. Inverting Follower

Video amplifier NE5592

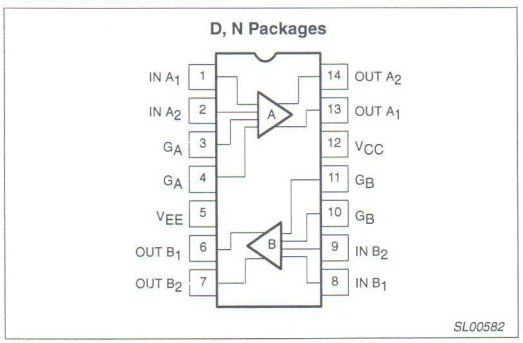
DESCRIPTION

The NE5592 is a dual monolithic, two-stage, differential output, wideband video amplifier. It offers a fixed gain of 400 without external components and an adjustable gain from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.

FEATURES

- 110MHz unity gain bandwidth
- Adjustable gain from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Wave shaping with minimal external component

PIN CONFIGURATION



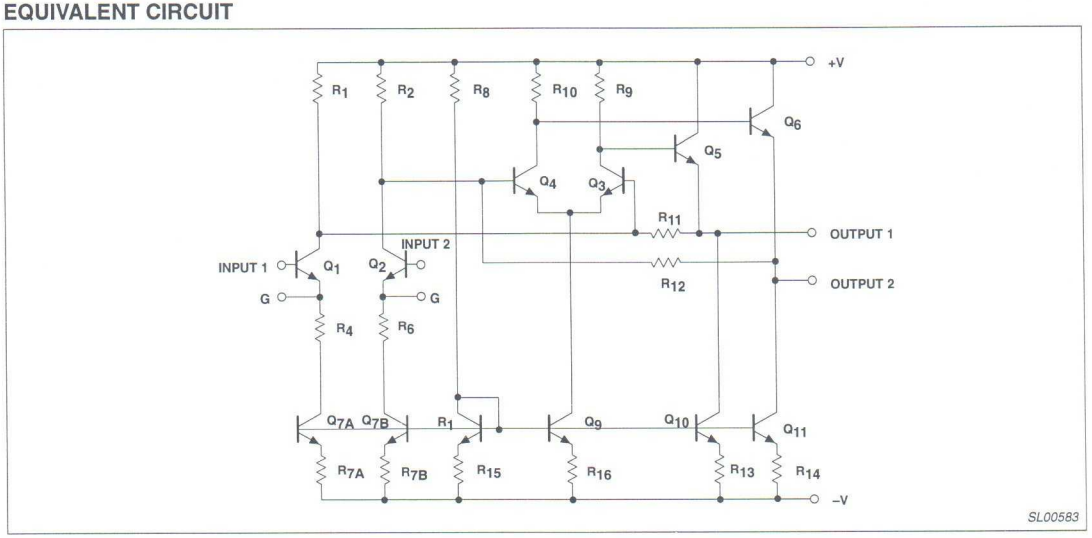
APPLICATIONS

- Floppy disk head amplifier
- Video amplifier
- Pulse amplifier in communications
- Magnetic memory
- Video recorder systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to 70°C	NE5592N	0405B
14-Pin Small Outline (SO) package	0 to 70°C	NE5592D	0175D

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common mode Input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating temperature range NE5592	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
$P_{D\ MAX}$	Maximum power dissipation, T_A=25°C (still air)[1] D package N package	 1.03 1.48	 W W

NOTES:

1. Derate above 25°C at the following rates:
   D package 8.3mW/°C
   N package 11.9mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=+25°C, V_{SS}=±6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltage is V_S = ±6.0V, and gain select pins are connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	R_L=2kΩ, V_{OUT}=3V_{P-P}	400	480	600	V/V
R_{IN}	Input resistance		3	14		kΩ
C_{IN}	Input capacitance			2.5		pF
I_{OS}	Input offset current			0.3	3	µA
I_{BIAS}	Input bias current			5	20	µA
	Input noise voltage	BW 1kHz to 10MHz		4		nV/√Hz
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	V_{CM} ± 1V, f<100kHz V_{CM} ± 1V, f=5MHz	60	93 87		dB dB
PSRR	Supply voltage rejection ratio	ΔV_S= ± 0.5V	50	85		dB
	Channel separation	V_{OUT}=1V_{P-P}; f=100kHz (output referenced) R_L=1kΩ	65	70		dB
V_{OS}	Output offset voltage gain select pins open	R_L=∞ R_L=∞		0.5 0.25	1.5 0.75	V V
V_{CM}	Output common-mode voltage	R_L=∞	2.4	3.1	3.4	V
V_{OUT}	Output differential voltage swing	R_L=2kΩ	3.0	4.0		V
R_{OUT}	Output resistance			20		Ω
I_{CC}	Power supply current (total for both sides)	R_L=∞		35	44	mA

DC ELECTRICAL CHARACTERISTICS

V_{SS}=±6V, V_{CM}=0, 0°C ≤ T_A ≤ 70°C, unless otherwise specified. Recommended operating supply voltage is V_S = ±6.0V, and gain select pins are connected together.

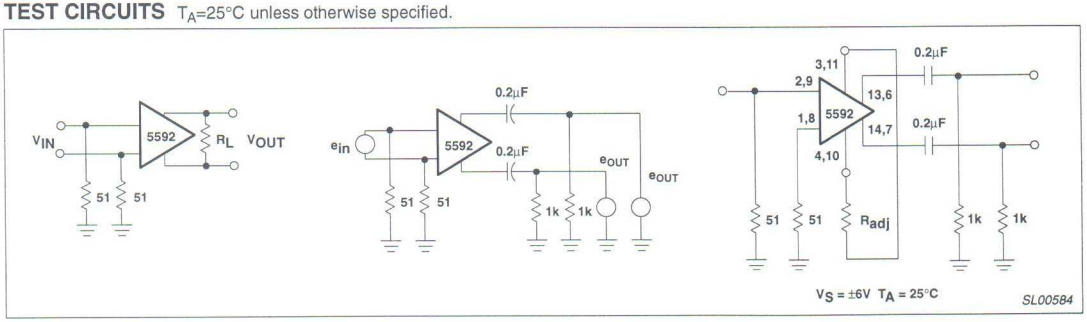
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	R_L=2kΩ, V_{OUT}=3V_{P-P}	350	430	600	V/V
R_{IN}	Input resistance		1	11		kΩ
I_{OS}	Input offset current				5	μA
I_{BIAS}	Input bias current				30	μA
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	V_{CM} ± 1V, f<100kHz R_S=ϕ	55			dB
PSRR	Supply voltage rejection ratio	ΔV_S= ± 0.5V	50			dB
	Channel separation	V_{OUT}=1V_{P-P}; f=100kHz (output referenced) R_L=1kΩ		70		dB
V_{OS}	Output offset voltage gain select pins connected together	R_L=∞			1.5	V
	gain select pins open	R_L=∞			1.0	V
V_{OUT}	Output differential voltage swing	R_L=2kΩ	2.8			V
I_{CC}	Power supply current (total for both sides)	R_L=∞			47	mA

AC ELECTRICAL CHARACTERISTICS

T_A=+25°C V_{SS}=±6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltage V_S=±6.0V. Gain select pins connected together.

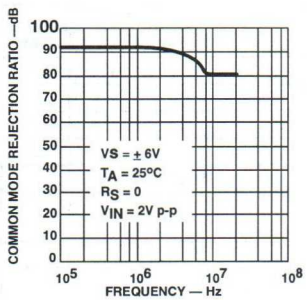
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
BW	Bandwidth	V_{OUT}=1V_{P-P}		25		MHz
t_R	Rise time			15	20	ns
t_{PD}	Propagation delay	V_{OUT}=1V_{P-P}		7.5	12	ns

TEST CIRCUITS T_A=25°C unless otherwise specified.



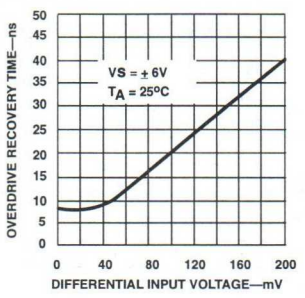
TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Rejection Ratio as a Function of Frequency



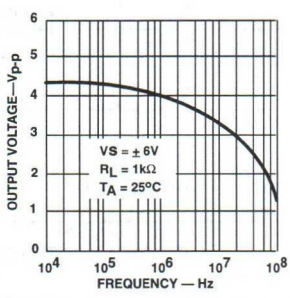
SL00585

Differential Overdrive Recovery Time



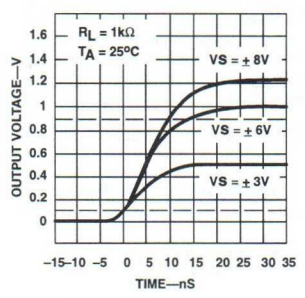
SL00588

Output Voltage Swing as a Function of Frequency



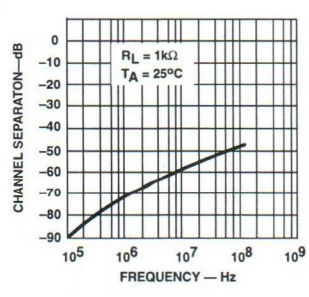
SL00586

Pulse Response as a Function of Supply Voltage



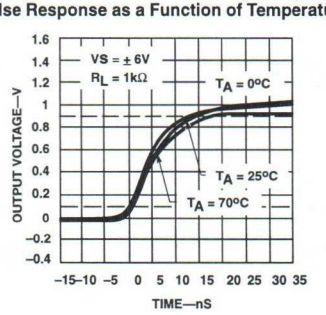
SL00589

Channel Separation as a Function of Frequency



SL00587

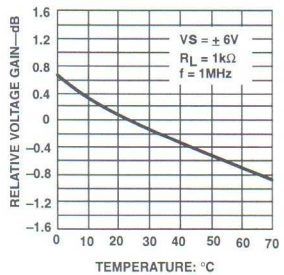
Pulse Response as a Function of Temperature



SL00590

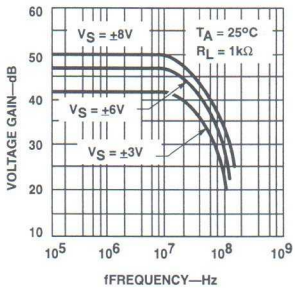
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Voltage Gain as a Function of Temperature



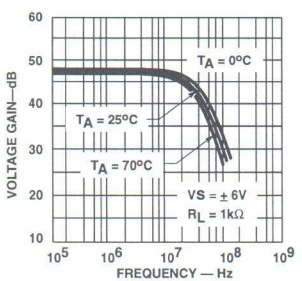
SL00591

Gain vs Frequency as a Function of Supply Voltage



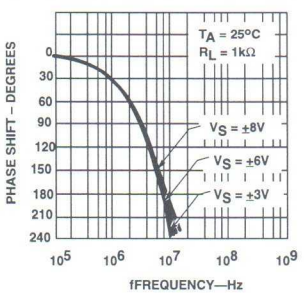
SL00594

Gain vs Frequency as a Function of Temperature



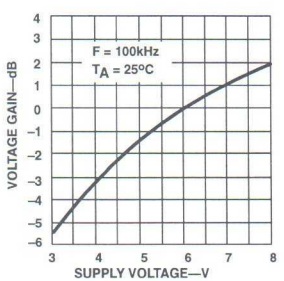
SL00592

Phase vs Frequency as a Function of Supply Voltage



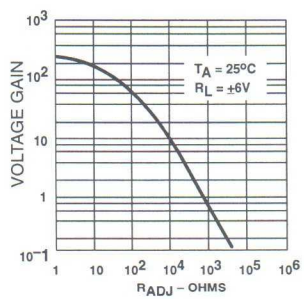
SL00595

Voltage Gain as a Function of Supply Voltage



SL00593

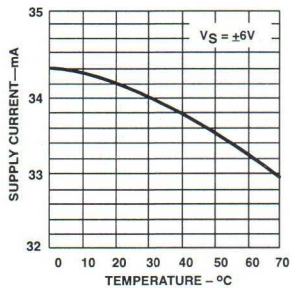
Voltage Gain as a Function of R_{ADJ}



SL00596

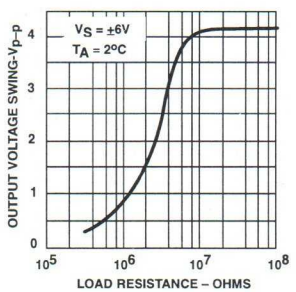
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Supply Current as a Function of Temperature



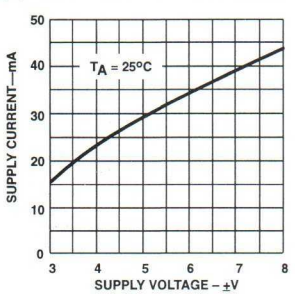
SL00597

Output Voltage Swing as a Function of Load Resistance



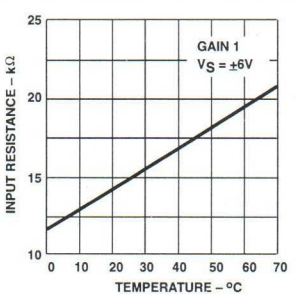
SL00600

Supply Current as a Function of Supply Voltage



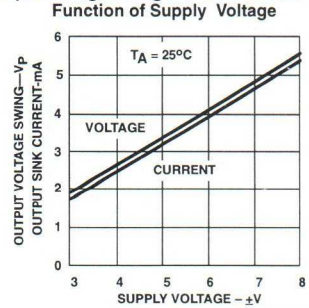
SL00598

Input Resistance as a Function of Temperature



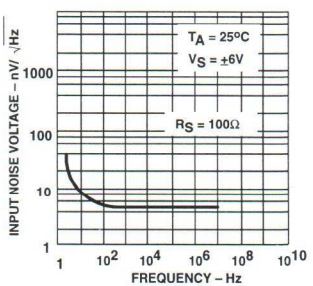
SL00601

Output Voltage Swing and Sink Current as a Function of Supply Voltage



SL00599

Input Noise Voltage as a Function of Frequency



SL00602

8-bit microcontroller with EMC P8xCE528

1 FEATURES

- 80C51 central processing unit
- 32K x 8 ROM, expandable externally to 64 kbytes
- ROM code protection
- 512 x 8 RAM, expandable externally to 63 kbytes
- Four 8-bit I/O ports
- Full-duplex UART compatible with the standard 80C51 and the 8052
- Two standard 16-bit timer/counters
- An additional 16-bit timer (functionally equivalent to the timer 2 of the 8052)
- On-chip Watchdog Timer (WDT) with an on-chip oscillator
- Bit-level I^2C-bus hardware serial I/O Port
- 7-source and 7-vector interrupt structure with 2 priority levels
- Up to 3 external interrupt request inputs
- Two programmable power reduction modes (Idle and Power-down)
- Termination of Idle mode by any interrupt, external or WDT (watchdog) reset
- Wake-up from Power-down by external interrupt, external or WDT reset
- Software enable/disable of ALE output pulse
- Electro-Magnetic Compatibility (EMC) improvements
- XTAL frequency range: 3.5 MHz to 16 MHz
- 4.5 to 5.5 V supply voltage range
- Extended Temperature range (–40 to +85°C)

2 GENERAL DESCRIPTION

The P83CE528, P80CE528 (hereafter generically referred to as P8xCE528) single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family.

The P8xCE528 has the same instruction set as the 80C51. Two versions of the derivative exist:

- P83CE528: 32kbytes mask programmable ROM
- P80CE528: ROMless version of the P83CE528

This device provides architectural enhancements that make it applicable in a variety of applications in general control systems, especially in those systems which need a large ROM and RAM capacity on chip.

The P8xCE528 contains a non-volatile 32K x 8 read-only program memory (P83CE528), a volatile 512 x 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a 16-bit timer (identical to the timer 2 of the 8052), a multi-source, two-priority-level, nested interrupt structure, two serial interfaces (UART and bit-level I^2C-bus), an on-chip oscillator and timing circuits, a watchdog timer (WDT) with a separate on-chip oscillator. For systems that require extra capability, the P8xCE528 can be expanded using standard TTL compatible memories and logic.

In addition, the P8xCE528 has two software selectable modes of power reduction – Idle mode and Power-down mode. The Idle mode freezes the CPU while allowing the RAM, timers, serial ports and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte, and 17 three-byte. With a 16 MHz crystal, 58% of the instructions are executed in 0.75µs and 40% in 1.5µs. Multiply and divide instruction require 3µs.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

3 ELECTROMAGNETIC COMPATIBILITY (EMC)

Primary attention is paid to the reduction of electro-magnetic emission of the microcontroller P8xCE528. The following features reduce the electro-magnetic emission and additionally improve the electromagnetic susceptibility:

- Two supply voltage pins ($V_{DD1;2}$) and four ground pins ($V_{SS1;2;3;4}$) are provided on the package as follows:
  - one V_{DD} and one V_{SS} as a pair of pins placed mid-centre on one side of the package
  - a second pair of V_{DD} and V_{SS} pins placed mid-centre on the opposite side of the package
  - two more V_{SS} pins, one placed on each of the other two sides of the package.
- Separated V_{DD} pins for the internal logic and the port buffers.
- Internal decoupling capacitance improves the EMC radiation behaviour and the EMC immunity.
- External capacitors are to be located as close as possible between pins V_{DD1} and V_{SS1} as well as V_{DD2} and V_{SS3}; ceramic chip capacitors are recommended (100 nF).

3.1 Recommendation on ALE

For applications that require no external memory or temporarily no external memory: the ALE output signal (pulses at a frequency of $f_{osc}/6$) can be disabled under software control (bit 5 in the PCON SFR: "RFI"); if disabled, no ALE pulse will occur. ALE pin will be pulled down internally, switching an external address latch to a quiet state. The MOVX instruction will still toggle ALE as a normal MOVX. ALE will retain its normal HIGH value during Idle mode and a LOW value during Power-down mode while in the "RFI" reduction mode.

Additionally during internal access ($\overline{EA}$ = 1) ALE will toggle normally when the address exceeds the internal program memory size. During external access ($\overline{EA}$ = 0) ALE will always toggle normally, whether the flag "RFI" is set or not.

4 ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE				TEMPERATURE RANGE (°C)	FREQUENCY (MHz)
	PINS	PIN POSITION	MATERIAL	CODE		
ROMless						
P80CE528EBB	44	QFP	plastic	SOT307-2	0 to +70	3.5 to 16
P80CE528EFB	44	QFP	plastic	SOT307-2	−40 to +85	3.5 to 16
P80CE528EBA	44	PLCC	plastic	SOT187	0 to +70	3.5 to 16
P80CE528EFA	44	PLCC	plastic	SOT187	−40 to +85	3.5 to 16
ROM						
P83CE528EBB	44	QFP	plastic	SOT307-2	0 to +70	3.5 to 16
P83CE528EFB	44	QFP	plastic	SOT307-2	−40 to +85	3.5 to 16
P83CE528EBA	44	PLCC	plastic	SOT187	0 to +70	3.5 to 16
P83CE528EFA	44	PLCC	plastic	SOT187	−40 to +85	3.5 to 16

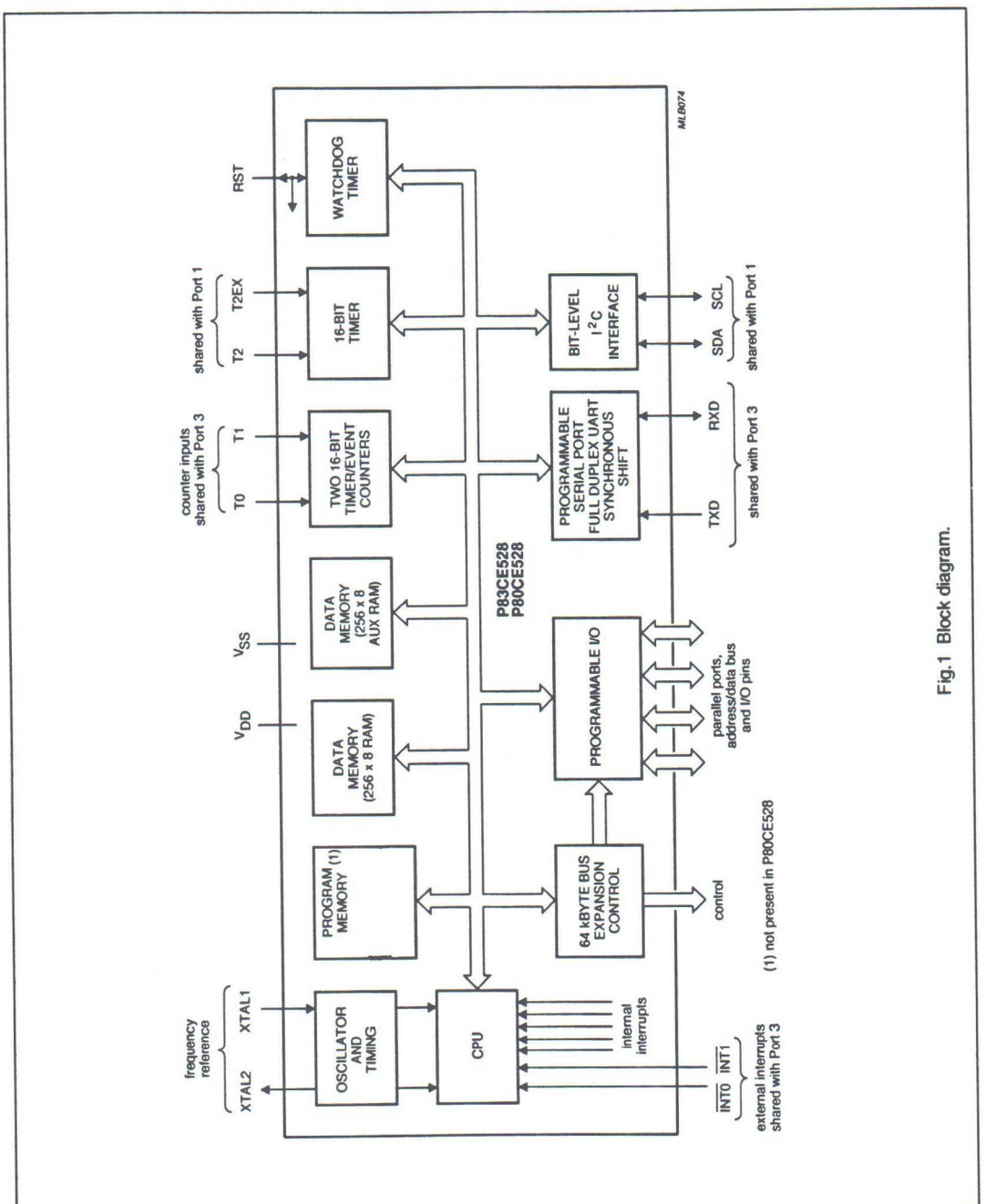


Fig.1 Block diagram.

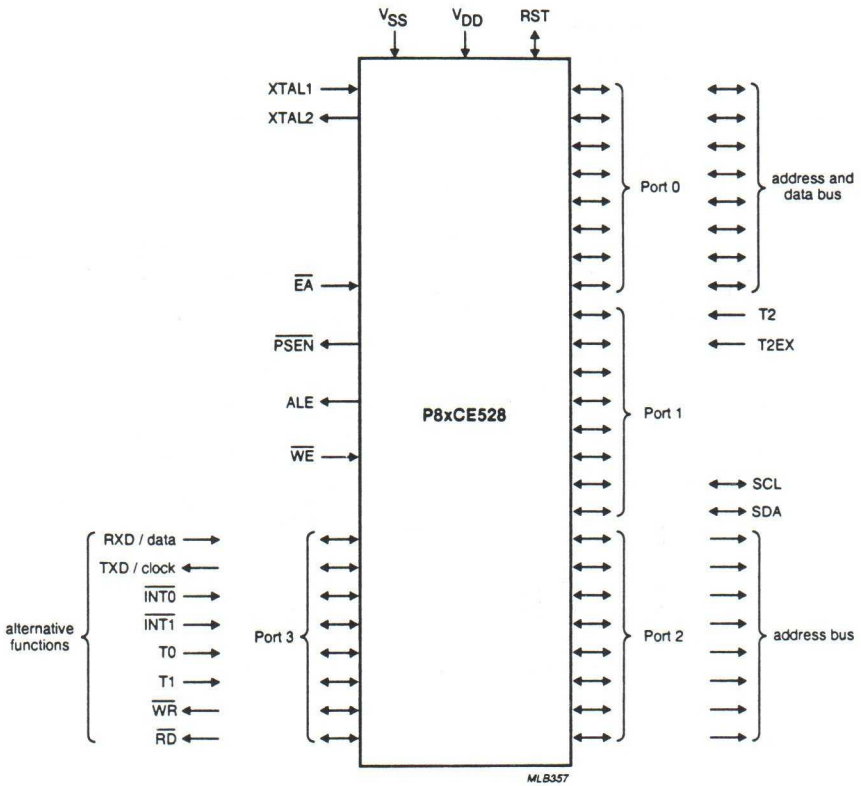


Fig.2 Functional diagram.

5 PINNING INFORMATION

5.1 Pinning

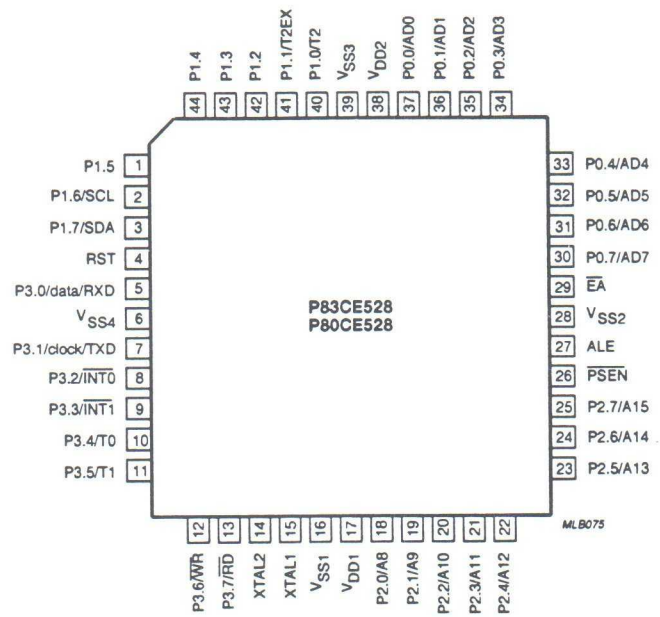


Fig.3 Pin configuration: 44-lead QFP; (SOT307-2).

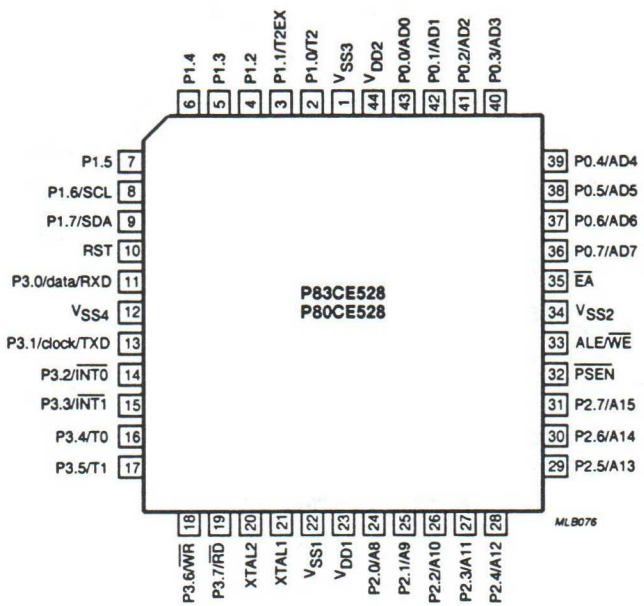


Fig.4 Pin configuration: 44-lead PLCC; (SOT187CG).

Pin description: 44-lead QFP; (SOT307-2).

SYMBOL	PIN	DESCRIPTION
P1.0 to P1.7	40 to 44 1 to 3	**Port 1**: 8-bit quasi-bidirectional I/O Port. Port 1 can sink/source one TTL (= 4 LSTTL) input. It can drive CMOS inputs without external pull-ups, except P1.6 and P1.7 which have open drain outputs.
		Port 1 alternative functions:
P1.0/T2	40	Timer/event counter 2 external event counter input (falling edge triggered).
P1.1/T2EX	41	Timer/event counter 2 capture/reload trigger or external interrupt 2 input (falling edge triggered).
P1.6/SCL	2	I^2C-bus Serial Port clock line.
P1.7/SDA	3	I^2C-bus Serial Port data line.
RST	4	**RESET**: a HIGH level on this pin for two machine cycles while the oscillator is running, resets the device. An internal pull-down resistor permits power-on reset using only a capacitor connected to V_{DD}. After a WDT overflow this pin is pulled HIGH while the internal reset signal is active.
P3.0 to P3.7	5, 7 to 13	**Port 3**: 8-bit quasi-bidirectional I/O Port with internal pull-ups. Port 3 can sink/source one TTL (= 4 LSTTL) input. It can drive CMOS inputs without external pull-ups.
		Port 3 alternative functions:
P3.0/RXD/data	5	Serial Port data input (asynchronous) or data input/output (synchronous).
P3.1/TXD/clock	7	Serial Port data output (asynchronous) or clock output (synchronous).
P3.2/$\overline{INT0}$	8	External interrupt 0 or gate control input for timer/event counter 0.
P3.3/$\overline{INT1}$	9	External interrupt 1 or gate control input for timer/event counter 1.
P3.4/T0	10	External input for timer/event counter 0.
P3.5/T1	11	External input for timer/event counter 1.
P3.6/$\overline{WR}$	12	External data memory write strobe.
P3.7/$\overline{RD}$	13	External data memory read strobe. The generation or use of a Port 3 pin as an alternative function is carried out automatically by the P8xCE528 provided the associated Special Function Register (SFR) bit is set HIGH.
XTAL2	14	**Crystal pin 2**: output of the inverting amplifier that forms the oscillator. This pin left open-circuit when an external oscillator clock is used
XTAL1	15	**Crystal pin 1**: input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external oscillator clock signal when an external oscillator is used.
$V_{SS1;2;3;4}$	16, 28, 39, 6	**Ground**: circuit ground potential. All pins must be connected.

SYMBOL	PIN	DESCRIPTION
P2.0 to P2.7	18 to 25	**Port 2**: 8-bit quasi-bidirectional I/O Port with internal pull-ups. During access to external memories (RAM/ROM) that use 16-bit addresses (MOVX @DPTR) Port 2 emits the high-order address byte (A8 to A15). Port 2 can sink/source one TTL (= 4 LSTTL) input. It can drive CMOS inputs without external pull-ups.
$\overline{PSEN}$	26	**Program Store Enable output**: read strobe to the external program memory via Port 0 and Port 2. It is activated twice each machine cycle during fetches from external program memory. When executing out of external program memory two activations of $\overline{PSEN}$ are skipped during each access to external data memory. $\overline{PSEN}$ is not activated (remains HIGH) during no fetches from external program memory. $\overline{PSEN}$ can sink/source 8 LSTTL inputs. It can drive CMOS inputs without external pull-ups.
ALE/$\overline{WE}$	27	**Address Latch Enable output**: latches the LOW byte of the address during access to external memory in normal operation. It is activated every six oscillator periods except during an external data memory access. ALE/$\overline{WE}$ can sink/source 8 LSTTL inputs. It can drive CMOS inputs without an external pull-up (note 1).
$\overline{EA}$	29	**External Access input**: when during RESET, $\overline{EA}$ is held at a TTL HIGH level, the CPU executes out of the internal program ROM, provided the program counter is less than 32768. When $\overline{EA}$ is held at a TTL LOW level during RESET, the CPU executes out of external program memory via Port 0 and Port 2. $\overline{EA}$ is not allowed to float. $\overline{EA}$ is latched during RESET and don't care after RESET.
P0.0 to P0.7	30 to 37	**Port 0**: 8-bit open drain bidirectional I/O Port. It is also the multiplexed low-order address and data bus during accesses to external memory (AD0 to AD7). During these accesses internal pull-ups are activated. Port 0 can sink/source 8 LSTTL inputs.
$V_{DD1;2}$		**Power supply**: +5 V power supply pin during normal operation and power reduction modes. Both pins must be connected.
V_{DD1}	17	Power supply pin for ports, ALE, $\overline{PSEN}$ and on-chip oscillator.
V_{DD2}	38	Power supply pin for internal logic. To avoid a latch-up effect at power-on, the voltage on any pin (at any time) must not be higher than V_{DD} +0.5 V or lower than V_{SS} –0.5 V respectively.

Note

1. To prohibit the toggling of ALE/$\overline{WE}$ pin (RFI noise reduction) the bit RFI in the PCON register (PCON.5) must be set by software. This bit is cleared on RESET and can be cleared by software. When set, ALE/$\overline{WE}$ pin will be pulled down internally, switching an external address latch to a quiet state. The MOVX instruction will still toggle ALE/$\overline{WE}$ as a normal MOVX. ALE/$\overline{WE}$ will retain its normal HIGH value during Idle mode and a LOW value during Power-down mode while in the "RFI" mode. Additionally during internal access ($\overline{EA}$ = 1) ALE/$\overline{WE}$ will toggle normally when the address exceeds the internal program memory size. During external access ($\overline{EA}$ = 0) ALE/$\overline{WE}$ will always toggle normally, whether the flag "RFI" is set or not.

Microcontroller for TV OSD, VST and control functions

P83CL168; P83CL167 P83CL268; P83CL267

FEATURES

P80CL51 CPU core

- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM and I/O's in a single package
- Maximum memory size: 64 kbytes of ROM plus 64 kbytes of RAM (the P83CL168 has no external memory access capability)
- Two 16-bit timer/event counters
- On-chip oscillator suitable for quartz crystal or ceramic resonator
- Thirteen source, thirteen vector interrupt structure with two priority levels
- Enhanced architecture with:
  - non page orientated instructions
  - direct addressing
  - four 8 byte RAM Register Banks
  - stack depth up to 128 bytes
  - multiply, divide, subtract and compare instructions.

Special

- 16 kbyte system ROM; 256 byte system RAM (no external memory access capability)
- Four 6-bit Pulse Width Modulated outputs
- Four 7-bit Pulse Width Modulated outputs
- One 14-bit Pulse Width Modulated output
- Four 4-bit Analog-to-Digital Converter channels
- LED driver port (Port 0): eight port lines with 10 mA drive capability
- Remote Control Preprocessor:
  - 8-bit counter with pulse width measurement capability and digital filter for noise discrimination
  - programmable resolution of minimal pulse width
  - programmable maximum noise discrimination pulse width
  - interrupt driven or polling by software
- Multimaster I^2C-bus (with two sets of SDA/SCL pins)
- High speed 8-bit 3-wire serial I/O
- Timer/counter T2: suitable for real time clock applications and also HSYNC signal detection
- 8-bit event counter driven by external input. Rising edge Schmitt trigger input.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

On Screen Display

- Display RAM: 160 × 12 bits
- Display character fonts: 126 + 2 reserved codes
- Character matrix: 12 × 18 (no spacing between characters)
- Programmable active level polarities for VSYNC and HSYNC
- 64 horizontal starting positions controlled by software
- 64 vertical starting positions controlled by software
- Character size: 4 different character sizes on a line-by-line basis
- Foreground colours: 8 on a character-by-character basis
- Background/shadowing modes: Two primary modes; TV mode and Monitor mode, on a frame basis. Each primary mode has three sub-modes on a line-by-line basis:
  - Sub-mode 1: Superimpose (no background)
  - Sub-mode 2: North-West shadowing
  - Sub-mode 3: Box shadowing
- Background colours: 8 on a word-by-word basis. Available in North-West shadowing, Box shadowing and Frame shadowing sub-modes
- Starting address in display RAM is programmable. Fast switching between banks of display (RAM) characters is possible through software control
- On-chip PLL oscillator for OSD function; the OSD clock frequency is programmable
- Character blinking ratio: 1 : 1 on a character basis
- Character blinking frequency: programmable using f_{VSYNC} divisors of 32 and 64
- Flexible display format using the Carriage Return Code and the two different Space Codes
- Display character RAM address post increment each time new data is written into RAM
- Vertical jitter cancelling circuit to avoid unstable VSYNC trailing edge mismatch with HSYNC signal
- On-chip Power-on-reset
- Packages: SDIP64 or QFP64
- Operating voltage: 4.5 to 5.5 V
- Operating temperature: –20 to +70 °C
- System clock frequency: 4 to 8 MHz
- OSD clock frequency: 4 to 10 MHz.

GENERAL DESCRIPTION

The P83CL168/167/268/267 family of microcontrollers are designed for medium-high to high-end TV control applications. They feature a Philips 80CL51 CPU which is object code compatible with the industry standard 80C51. They are all manufactured in an advanced CMOS technology featuring low power consumption. Throughout this specification the P83CL168 will be used as the generic term to describe the functions of the entire family. When pin numbers are specified these refer to the SDIP64 package.

The P83CL168 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit handling capabilities. Multiply and divide instructions are implemented by hardware with a cycle time of 6 μs (f_{xtal} = 8 MHz).

The instruction set consists of over 100 instructions; 49 one-byte, 46 two-byte and 16 three-byte. The device contains 16 kbytes of ROM, 256 bytes of RAM, 20 general I/O port lines and 27 function combined I/O lines. The derivative functions dedicated for TV applications are: AFC (Analog-to-Digital Converters), Remote Control Preprocessor, Pulse Width Modulated outputs for analog control and Voltage Synthesized Tuning and an On Screen Display function. There are two serial I/Os available: the I^2C-bus (two sets) and the High-speed 8-bit 3-wire serial I/O. An 8-bit counter (T2) is also provided on-chip and is suitable for AC line frequency measurements and HSYNC pulse counting. The differences between the four devices are specified in Table 1.

Table 1 Differences between the four family members

DIFFERENCES	P83CL168	P83CL167	P83CL268	P83CL267
Features				
ROM	16 kbytes	16 kbytes	12 kbytes	12 kbytes
High-speed 8-bit serial I/O bus (HIO)	Yes	No	Yes	No
Remote Control Preprocessor (RMC)	Yes	No	Yes	No
Pin functions				
Pin 26	P57/RMC	P57	P57/RMC	P57
Pin 27	P40/DOUT	P40	P40/DOUT	P40
Pin 28	P41/CLK	P41	P41/CLK	P41
Pin 29	P42/DIN	P42	P42/DIN	P42

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
P83CL168P	SDIP64	plastic shrink dual in-line package; 64 leads (750 mil)	SOT274-1
P83CL168H	QFP64	plastic quad flat package; 64 leads (lead length 2.35 mm); body 14 × 20 × 2.75 mm	SOT208-1
P83CL167P	SDIP64	plastic shrink dual in-line package; 64 leads (750 mil)	SOT274-1
P83CL167H	QFP64	plastic quad flat package: 64 leads (lead length 2.35 mm); body 14 × 20 × 2.75 mm	SOT208-1
P83CL268P	SDIP64	plastic shrink dual in-line package; 64 leads (750 mil)	SOT274-1
P83CL268H	QFP64	plastic quad flat package; 64 leads (lead length 2.35 mm); body 14 × 20 × 2.75 mm	SOT208-1
P83CL267P	SDIP64	plastic shrink dual in-line package; 64 leads (750 mil)	SOT274-1
P83CL267H	QFP64	plastic quad flat package; 64 leads (lead length 2.35 mm); body 14 × 20 × 2.75 mm	SOT208-1

BLOCK DIAGRAM

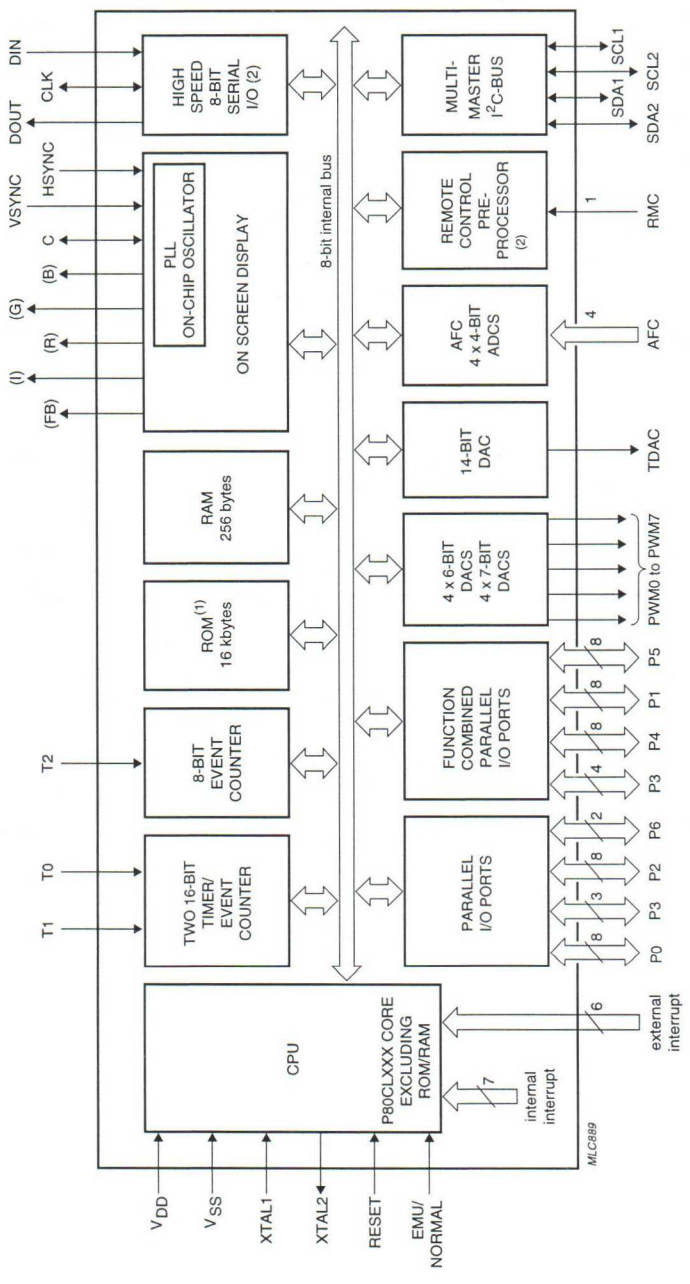
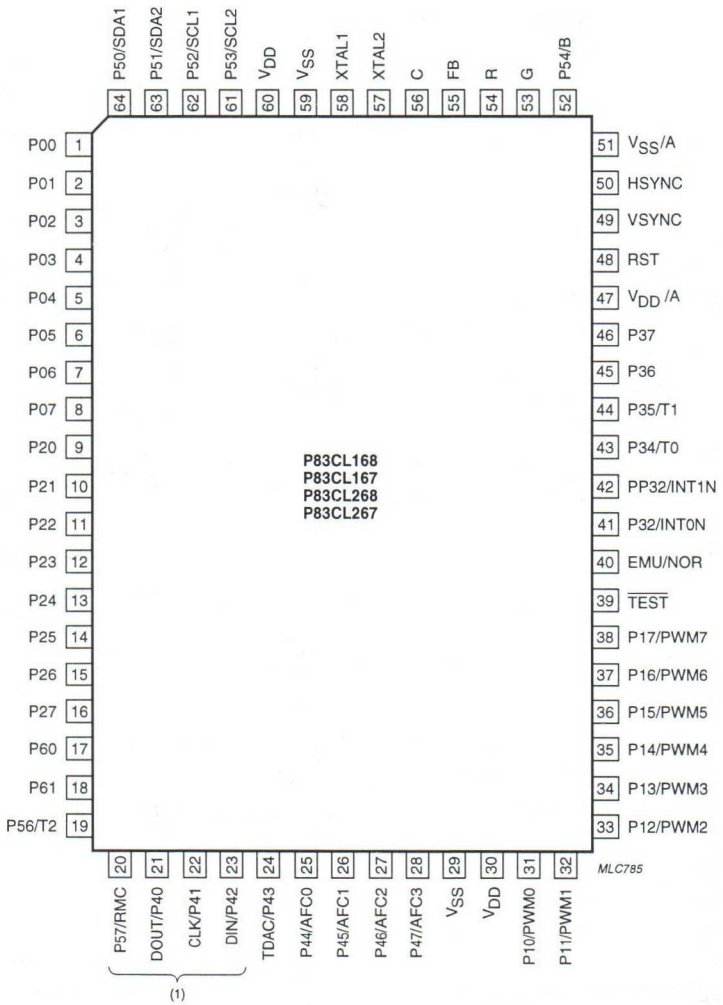


Fig.1 Block diagram.

(1) P83CL168 and P83CL167 have 16 kbytes ROM. The P83CL268 and P83CL267 have 12 kbytes ROM.
(2) The Remote Control Preprocessor is not a feature of the P83CL167 and P83CL267.

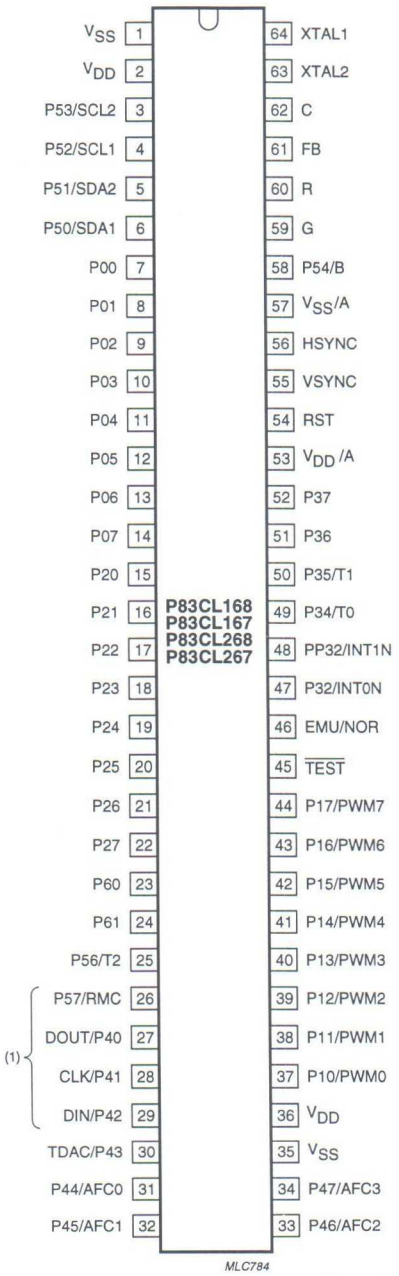
PINNING

SYMBOL	PIN	DESCRIPTION
V_{SS}	1 and 35	Ground; digital
V_{DD}	2 and 36	Power supply; digital
P53/SCL2	3	Port line P53 (quasi-bidirectional) or I^2C2-bus clock (open drain)
P52/SCL1	4	Port line P52 (quasi-bidirectional) or I^2C1-bus clock (open drain)
P51/SDA2	5	Port line P51 (quasi-bidirectional) or I^2C2-bus data line (open drain)
P50/SDA1	6	Port line P50 (quasi-bidirectional) or I^2C1-bus data line (open drain)
P00 to P07	7 to 14	General I/O Port 1 (quasi-bidirectional port), also used in the emulation mode for data transfers in between bondout chip and the derivative.
P20 to P27	15 to 22	General I/O Port 2 (quasi-bidirectional port), also used in the emulation mode for control signal transfers between bondout chip and the derivative.
P60 and P61	23 and 24	Output port lines P60 and P61, (standard option only)
P56/T2	25	I/O Port line P56 (quasi-bidirectional) or 8-bit event counter input
P57/RMC	26	I/O Port line P57 (quasi-bidirectional) or Remote Control Preprocessor input
DOUT/P40	27	High-speed serial data output or port line P40 (quasi-bidirectional)
CLK/P41	28	High-speed serial clock (bidirectional) or port line P41 (quasi-bidirectional)
DIN/P42	29	High-speed serial I/O data input or port line P42 (quasi-bidirectional)
TDAC/P43	30	14-bit PWM (push-pull output) or port line P43 (quasi-bidirectional)
P44/AFC0 to P47/AFC3	31 to 34	I/O Port lines P44 to P47 (quasi-bidirectional port) or 4-bit AFC inputs (standard option)
P10/PWM0 to P17/PWM7	37 to 44	I/O Port lines P10 to P17 (quasi-bidirectional port) or the PWM outputs. PWM0 to PWM3 are the 6-bit PWM outputs; PWM4 to PWM7 are the 7-bit PWM outputs. Port pins P10, P11, P12 and P17 are also used for external interrupt request information and are enabled by software.
TEST	45	Test input (LOW) or normal operation (HIGH)
EMU/NOR	46	Emulation mode (LOW) or Normal mode (HIGH) selection. Set to HIGH in normal operation
P32/INT0N	47	I/O Port line P32 or external interrupt 0 input
P33/INT1N	48	I/O Port line P33 or external interrupt 1 input
P34/T0	49	I/O Port line P34 or 16-bit timer/counter T0 I/O
P35/T1	50	I/O Port line P35 or 16-bit timer/counter T1 I/O
P36 and P37	51 and 52	I/O Port lines P36 and P37
AV_{DD}	53	Power supply; analog
RST	54	Reset input (active HIGH)
VSYNC	55	TV vertical synchronization input
HSYNC	56	TV horizontal synchronization input
P55/I	57	I/O Port line 55 or OSD Intensity (4th colour) output
P54/B	58	I/O Port line P54 or OSD Blue output
G	59	OSD Green output
R	60	OSD Red output
FB	61	OSD Fast Blanking output
C	62	Capacitor connection for OSD on-chip PLL oscillator
XTAL2	63	Crystal oscillator output
XTAL1	64	Crystal oscillator input



(1) For the P83CL167 and P83CL267 devices these pins are port lines only; they have no alternative functions.

Fig.2 Pin configuration (QFP64).



(1) For the P83CL167 and P83CL267 devices these pins are port lines only; they have no alternative functions.

Fig.3 Pin configuration (SDIP64).

1. FEATURES

- CMOS technology
- Full 68000 software compatibility
- 32-bit internal structure
- 16-bit internal data transfer
- 8-bit access to external ROM/RAM
- External addressing range 16 Mbytes for ROM and 16 Mbytes for RAM
- Unused address pins can be used as quasi-bidirectional ports
- On-chip address decoder for ROM/RAM
- 8 edge triggered programmable interrupts that can also be used as quasi-bidirectional ports
- Reset control
- Built-in clock generator
- 2 fully independent fast I²C-bus serial interfaces
- UART serial interface (4 modes)
- 3 fully independent 16-bit timers
- Watchdog timer
- 8-bit quasi-bidirectional port, 4-bits with high drive capability
- EMC optimized layout and pinning
- 64-pin QFP package

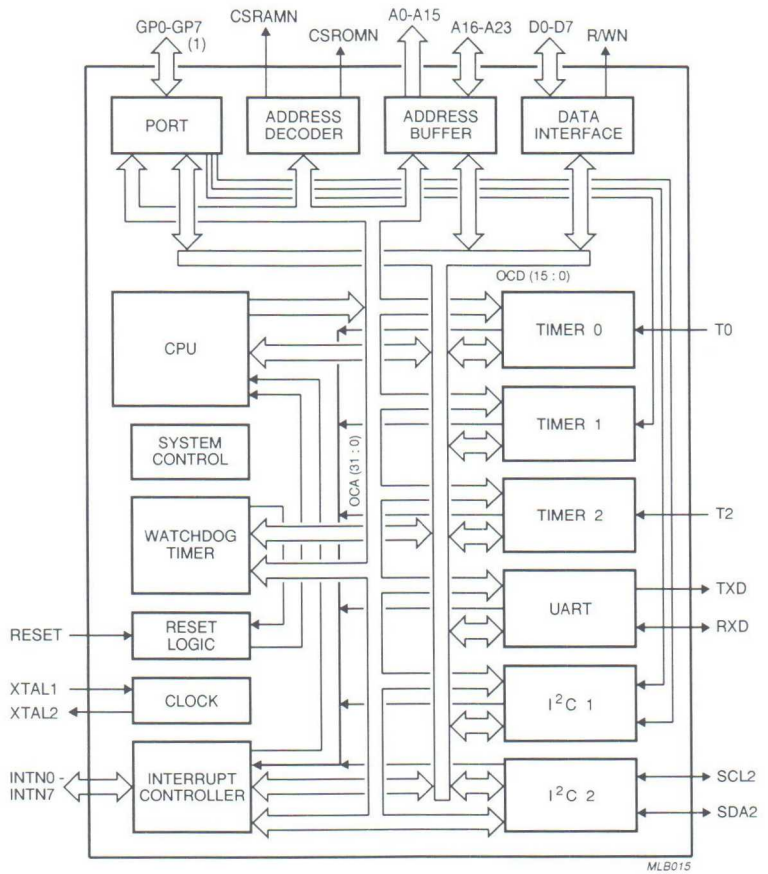
2. GENERAL DESCRIPTION

The P90CE201 is a member of the P9XCXXX family of highly integrated 16-bit microcontrollers for use in a wide variety of applications. It is fully software compatible with the 68070/68000. The complete set of system functions available on the chip results in reduced system cost. Additionally, its modular design concept permits future extension to the family.

3. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE				CLOCK FREQUENCY (MHz)	TEMPERATURE RANGE (°C)
	PINS	PIN POSITION	MATERIAL	CODE		
P90CE201AEB	64	QFP	plastic	SOT319	24.0	−25 to 85

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC21 OR DATA SHEET



1. The General Port lines GP5, GP6 and GP7 have alternate functions for Timer 1, SCL1 and SDA1 respectively; see Table 1.

Fig.1 Block diagram

4. PINNING INFORMATION

4.1 Pinning

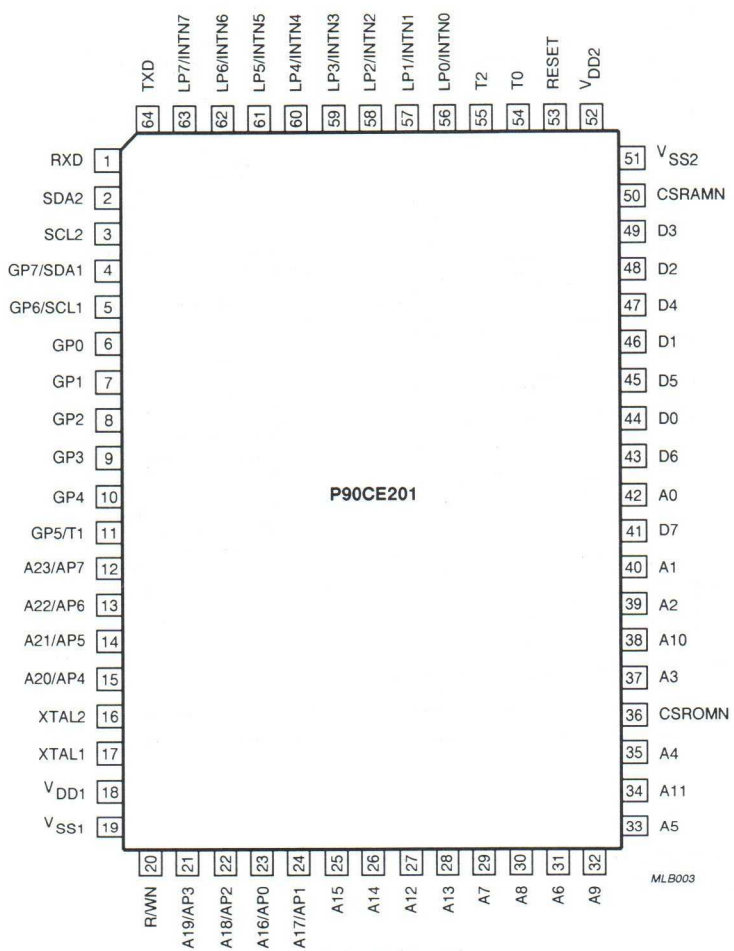


Fig.2 Pin configuration for QFP64.

4.2 Pin description

Table 1 QFP64 package.

MNEMONIC	TYPE	PIN NO.	FUNCTION
RXD	I/O	1	**Receive Data**. RXD is the data input for the UART interface.
SDA2	I/O	2	**Serial Data 2** (open drain). SDA2 is the data signal for the second I²C-bus serial interface.
SCL2	I/O	3	**Serial Clock 2** (open drain). SCL2 is the clock signal for the second I²C-bus serial interface.
GP7/SDA1 GP6/SCL1 GP0 GP1 GP2 GP3 GP4 GP5/T1	I/O	4 5 6 7 8 9 10 11	**General Purpose Port** (active HIGH, 3-state). The alternative functions are as follows. SCL1 is the clock signal for the first I²C-bus serial interface. SDA1 is the data signal for the first I²C-bus serial interface. T1 is the input pin for Timer 1.
A23/AP7 to A16/AP0	I/O	12 to 15, 21, 22, 24, 23	**Address Bus**. Upper 8-bits of the address bus (A23 to A16). The unused address bits can be selected as a quasi-bidirectional port (AP).
A15 to A0	O	25, 26, 28, 27, 34, 38, 32, 30, 29, 31, 33, 35, 37, 39, 40, 42	**Address Bus**. Lower 16-bits of the address bus.
XTAL2	O	16	**Oscillator output**. Not connected if an external clock generator is used.
XTAL1	I	17	**Oscillator input**. XTAL1 can also be used as an external clock input if an external clock generator is used.
V_{DD1}	–	18	**Supply voltage**. For internal logic, address bus, data bus, RWN, CSRAMN, CSROMN, XTAL1 and XTAL2.
V_{SS1}	–	19	**Ground**. For internal logic, address bus, data bus, RWN, CSRAMN, CSROMN, XTAL1 and XTAL2.
R/WN	O	20	**Read** (active HIGH)/**Write** (active LOW). This controls the direction of data flow.
CSROMN	O	36	**Chip Select ROM** (active LOW). This signal selects external ROM.
D0 to D7	O	44, 46, 48, 49, 47, 45, 43, 41	**Data Bus**. 8-bit data bus.
CSRAMN	O	50	**Chip Select RAM** (active LOW). This signal enables external RAM.
V_{SS2}	–	51	**Ground**. For all other periphery pins (quiet port).
V_{DD2}	–	52	**Supply voltage**. For all other periphery pins (quiet port).
RESET	I	53	**Reset** (active HIGH). Input pin for an external reset.
T0	I	54	**Timer 0**. Input pin for cycle and event counting using Timer 0.
T2	I	55	**Timer 2**. Input pin for cycle and event counting using Timer 2.

MNEMONIC	TYPE	PIN NO.	FUNCTION
LP0/INTN0 LP1/INTN1 LP2/INTN2 LP3/INTN3 LP4/INTN4 LP5/INTN5 LP6/INTN6 LP7/INTN7	I/O	56 57 58 59 60 61 62 63	**Latched Interrupt inputs** (active LOW). A LOW level of ≥ 1 clock pulse will be stored as a pending interrupt request. Priority levels are programmable. Unused interrupt inputs can be used as a quasi-bidirectional port (LP).
TXD	O	64	**Transmit Data**. TXD is the data output for the UART serial interface.

8-bit microcontrollers for remote control transmitters

PCA84C122; 222; 422; 622; 822

FEATURES

- 84CXXX CPU
- ROM, RAM and I/O configurations are device dependent
- Two test inputs: T0 (ANDed with Port 1 input lines) and T1
- 3 single-level vectored interrupt sources:
  - external (T0/$\overline{INT}$ and Port 1, for keypad press Wake-up function)
  - timer/counter (TI)
  - hardware modulator interrupt
- 8-bit programmable timer/counter with 5-bit pre-scaler
- Power saving: Idle and Stop modes are provided
- Hardware Modulator providing pulse bursts, with:
  - programmable pulse time and duty factor for each pulse
  - programmable number of pulses
- One output line from the Hardware Modulator to control the driver transistor for the infrared LED (IR-LED). Capable of sinking 27 mA at V_{DD} = 2.0 V, $V_{\overline{OUT}}$ = 1.0 V
- Watchdog Timer to keep the transmitter from being locked or malfunction
- Available packages: SO and DIP types (SO20, SO24, SO28, SDIP24 and DIP20)
- On-chip oscillator: 455 kHz to 6 MHz
- Single supply voltage: 2.0 V to 5.5 V
- Operating temperature: –20 to +50 °C.

GENERAL DESCRIPTION

The PCA84C122 is a stand-alone microcontroller designed for use in remote control transmitters for a wide range of applications.

The PCA84C122 provides a number of dedicated hardware functions for remote controller applications. These functions include the following additional blocks to the 84CXXX core:

- Interrupt Gate
- Hardware Modulator
- Output Driver
- Watchdog Timer.

Although the PCA84C122 is specifically referred to throughout this data sheet, the information applies to all the devices.

Figure 2 shows the general block diagram of the device. The 84CXXX core plus 8 kbytes ROM and 64 bytes RAM has the same function as described in the PCF84CXXX family description (see *"Data Handbook IC14"*).

When the transmitter is not in use the microcontroller is in Stop mode and the oscillator is halted. The AND gate connected to the Port 1 (P10 to P17) lines provides the Wake-up to end the Stop mode.

The Hardware Modulator produces pulse bursts according to the required protocol. The ON-time and OFF-time of each pulse (i.e. duty factor) and the number of pulses are controlled by software.

The purpose of the Watchdog Timer (WDT) is to reset the microcontroller if it enters an erroneous processor state (endless loop, continuous Idle mode, etc.); within a reasonable period of time.

During Stop mode the oscillator is halted, therefore the Watchdog Timer is not running.

The Output Driver can handle sufficient current to drive a single transistor, that provides the required current for the IR-LED.

Important note

This data sheet details the specific properties of the PCA84C122; PCA84C222; PCA84C422; PCA84C622 and PCA84C822. The shared characteristics of the family of microcontrollers are described in the PCF84CXXXA Family single-chip 8-bit Microcontroller of *"Data Handbook IC14"*, which should be read in conjunction with this data sheet.

MEMORY AND I/O CONFIGURATIONS

DEVICE	I/O LINES	ROM	RAM
PCA84C122A	16	1K	32 bytes
PCA84C122B	12		
PCA84C222A	16	2K	
PCA84C222B	12		
PCA84C422A	16	4K	
PCA84C422B	12		
PCA84C622A	16	6K	64 bytes
PCA84C622B	12		
PCA84C622C	20[1]		
PCA84C822A	16	8K	
PCA84C822B	12		
PCA84C822C	20[1]		

Note

1. 4 I/O lines with 10 mA sink capability.

ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA84CX22AP	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1
PCA84CX22AT	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
PCA84CX22BP	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
PCA84CX22BT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
PCA84C622CT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCA84C822CT			

Note

1. 'X' in the type number denotes the numbers: 1, 2, 4, 6 and 8.

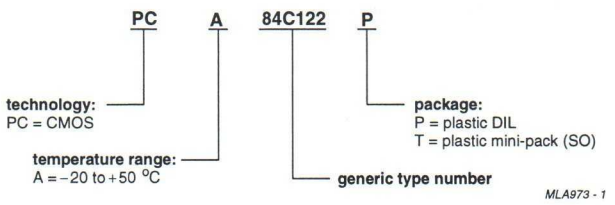


Fig.1 Numbering scheme.

BLOCK DIAGRAM

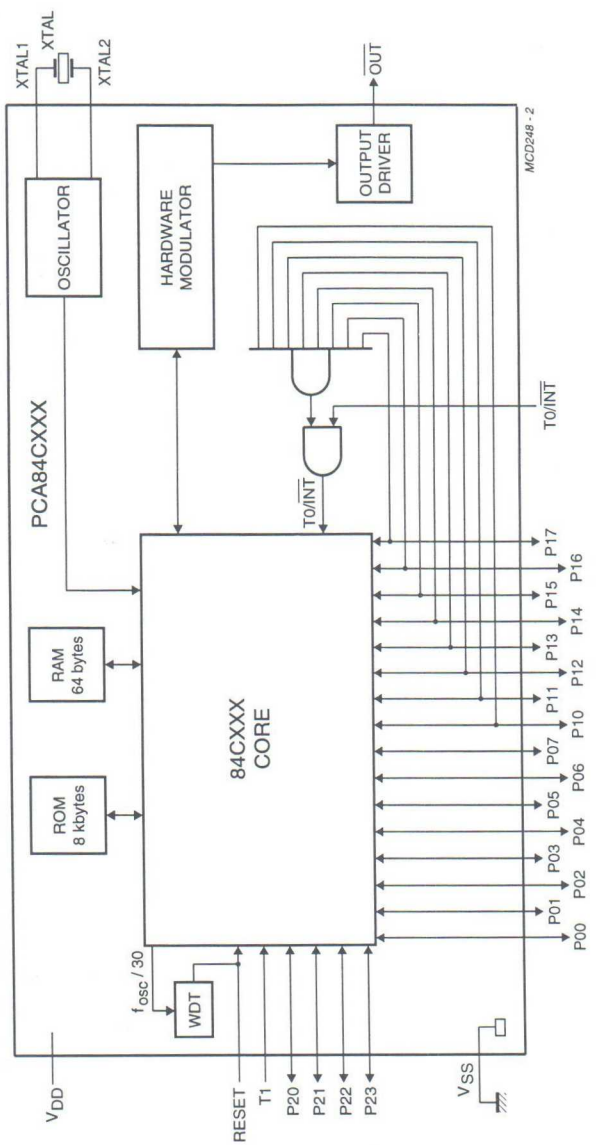


Fig.2 Block diagram.

Port lines: P14, P15, P16 and P17 are **not** available in PCA84CX22BP and PCA84CX22BT.
Port lines: P20, P21, P22 and P23 are **only** available in PCA84C622CT and PCA84C822CT.

PINNING INFORMATION

Pinning

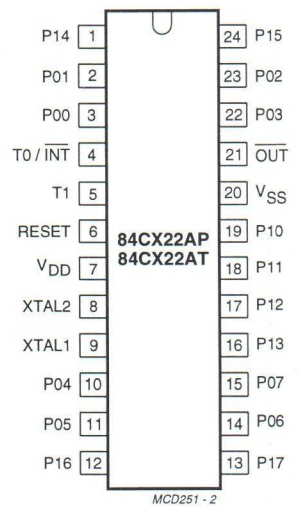


Fig.3 Pin configurations PCA84CX22AP (SDIP24) and PCA84CX22AT(SO24).

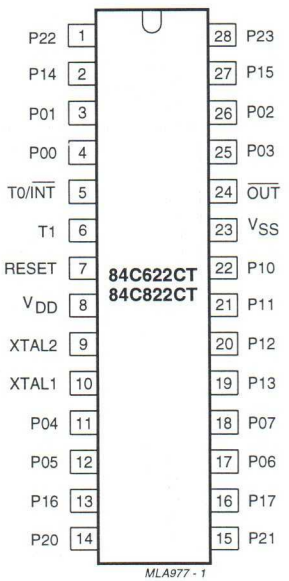


Fig.4 Pin configuration PCA84CX22CT (SO28).

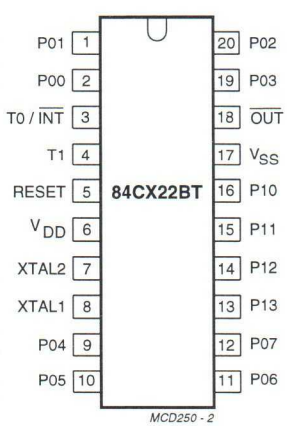


Fig.5 Pin configuration PCA84CX22BT (SO20).

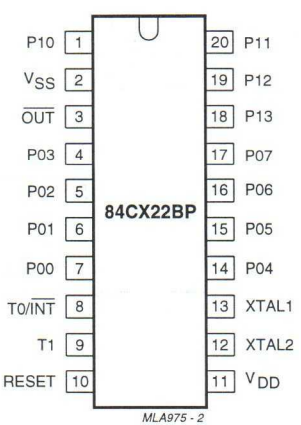


Fig.6 Pin configuration PCA84CX22BP (DIP20).

Pin description

Table 1 Pin description for PCA84CX22AP, PCA84CX22AT, PCA84CX22BP, PCA84CX22BT and PCA84CX22CT

SYMBOL	PIN				DESCRIPTION
	SDIP24/SO24 (see Fig.3)	SO28 (see Fig.4)	SO20 (see Fig.5)	DIP20 (see Fig.6)	
P00 to P07	3, 2, 23, 22, 10, 11, 14, 15	4, 3, 26, 25, 11, 12, 17, 18	2, 1, 20, 19, 9, 10, 11, 12	7, 6, 5, 4, 14, 15, 16, 17	standard I/O Port lines, generally used for keypad scanning (driving)
P10 to P13	19, 18, 17, 16	22, 21, 20,19	16, 15, 14, 13	1, 20,19, 18	standard I/O Port lines, generally used for keypad scanning (sensing)
P14 to P17	1, 24, 12, 13	2, 27, 13, 16	–	–	
P20 to P23	–	14, 15, 1, 28b	–	–	standard I/O Port lines, generally used for visible LED's
T0/$\overline{\text{INT}}$	4	5b	3	8	test T0 and external interrupt input
T1	5	6	4	9	test T1 input
RESET	6	7	5	10	active HIGH reset; normally connected to V_{SS}. For further information see PCF84CXXXA description in *"Data Handbook IC14"*
XTAL1	9	10	8	13	terminals for connecting the crystal or ceramic resonator
XTAL2	8	9	7	12	
$\overline{\text{OUT}}$	21	24	18	3	pulse train output pin, capable of sinking 27 mA
V_{DD}	7	8	6	11	power supply
V_{SS}	20	23	17	2	ground

Microcontrollers for TV tuning control and OSD application

PCA84C646; PCA84C846

FEATURES

PCF84CXXXA kernel

- 8-bit CPU, ROM, RAM, I/O and derivative logic in one package
- Over 80 instructions
- All instructions of 1 or 2 cycles
- Quasi-bidirectional standard I/O port lines (P0, P1)
- Configuration of I/O lines individually selected by mask
- External interrupt $\overline{INT}$/T0
- 2 direct testable inputs T0, T1
- 8-bit timer/event counter
- Single level vectored interrupt: external ($\overline{INT}$), counter/timer, I²C-bus and $\overline{VSYNC}$
- Configuration of optimal on-chip oscillator transconductance by mask
- On-chip oscillator clock frequency: 1 to 10 MHz
- Power-on-reset and low-voltage detector
- Low standby voltage and current in Idle and Stop modes
- Single power supply: 4.5 to 5.5 V
- Operating temperature: –20 to +70 °C.

VST and OSD derivative

- 6 kbytes (PCA84C646) or 8 kbytes (PCA84C846) system ROM, 192 bytes system RAM
- A multi-master I²C-bus interface
- One 14-bit PWM output for VST
- Three AFC inputs with 4-bit DAC and comparator
- Four 6-bit PWM and four 7-bit PWM outputs (DACs for analog controls)
- Eight port lines with 10 mA LED drive (at ≤1.2 V) capability
- Programmable active level polarities of $\overline{VSYNC}$/$\overline{HSYNC}$
- Display RAM: 64 × 10-bit
- Display character fonts: 64 (62 customized + 2 special reserved codes)
- Display starting position: 64 different positions by software control, both vertical and horizontal
- Character size: 4 different character sizes, line-by-line basis, 1 dot = 1H/1V, 2H/2V, 3H/3V, 4H/4V. (H: OSD clock period, V: number of horizontal scan line height)
- Character matrix: 12 × 18 with no spacing between characters
- Foreground colours: 8, character-by-character basis
- Background colours: 8, word-by-word basis. Available when background is either in North-west shadowing, Box shadowing and Frame shadowing mode
- Background/shadowing modes: 4, no background, North-west shadowing, Box shadowing, Frame shadowing (raster blanking), frame basis
- On-chip oscillator for On Screen Display (OSD) function
- Character blinking rate: 1 : 1, 1 : 3, 3 : 1 (frequency: $1/16$, $1/32$, $1/64$ or $1/128$ of f_{VSYNC}, programmable), character basis
- Display format: flexible display format by using CR (carriage return) code
- Spacing between lines: 4 different choices, from 0, 4, 8 or 12 horizontal scan lines
- Auto display character RAM address post increment when writing data
- On-chip Power-on-reset
- $\overline{VSYNC}$ leading edge can generate interrupt (programmable enable/disable by software)
- 8-bit counter triggered by external pulse input.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

Microcontrollers for TV tuning control and OSD application

PCA84C646; PCA84C846

GENERAL DESCRIPTION

The PCA84C646 and PCA84C846 are 8-bit microcontrollers with enhanced OSD and VST functions. The PCA84C646 and PCA84C846 are members of the PCA84C640 CMOS microcontroller family. They include the PCF84CXXXA processor core, 6 or 8 kbytes of ROM, 192 bytes of RAM.

I/O requirements are adequately catered for with 13 general purpose bidirectional I/O lines plus 16 function combined I/O lines. One 14-bit PWM analog control, 3 AFC inputs (4-bit DAC + comparator) for VST and four 6-bit and 7-bit PWM analog control outputs are provided.

In addition to all these features a master-slave I^2C-bus interface, 2 directly testable lines and an enhanced OSD facility for flexible screen format (maximum of 64 character types) are also provided.

The on-chip PLL oscillator for OSD operation considerably reduces the radiation generated by the RC or LC oscillator. An 8-bit timer is integrated on-chip with a 5-bit prescaler. Another 8-bit counter with Schmitt-trigger input is used for clock/timer function application.

Figure 1 shows the block diagram of the PCA84C646 and PCA84C846.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA84C646P	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1
PCA84C846P			

BLOCK DIAGRAM

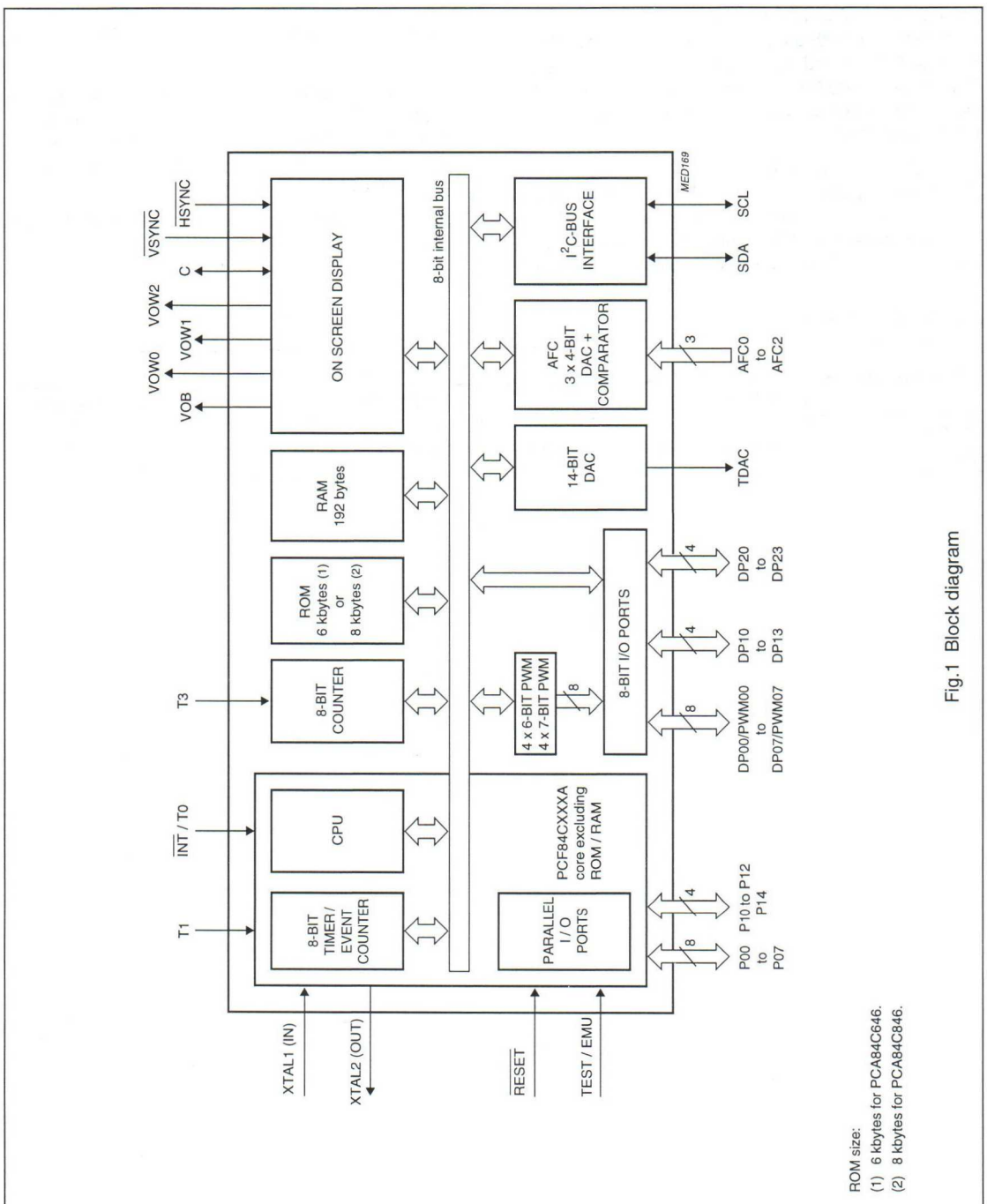


Fig.1 Block diagram

ROM size:
(1) 6 kbytes for PCA84C646.
(2) 8 kbytes for PCA84C846.

PINNING INFORMATION

Pinning

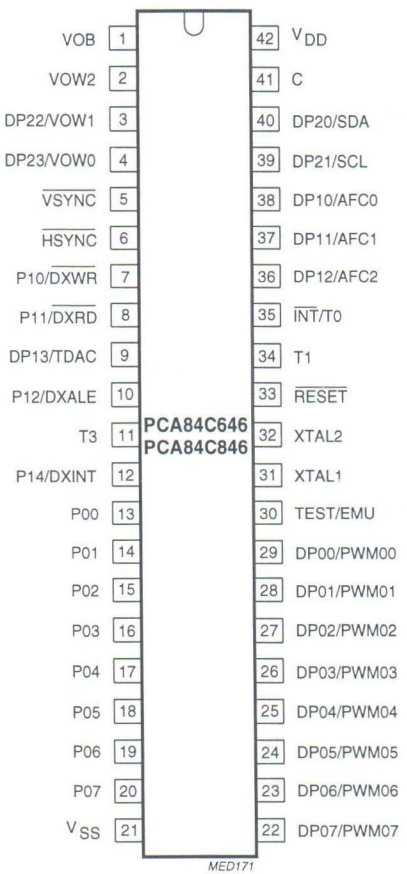


Fig.2 Pin configuration PCA84C646P and PCA84C846P (SDIP42; SOT270-1).

Pin description

Table 1 Pin description for PCA84C646P and PCA84C846P; SDIP42 (see Fig.2)

SYMBOL	PIN	DESCRIPTION
VOB	1	Video fast blanking output signal.
VOW2	2	Video character outputs or derivative port lines.
DP22/VOW1	3	
DP23/VOW0	4	
$\overline{\text{VSYNC}}$	5	Vertical synchronization signal input, active LOW.
$\overline{\text{HSYNC}}$	6	Horizontal synchronization signal input, active LOW.
P10/$\overline{\text{DXWR}}$	7	Port line 10 or emulation $\overline{\text{DXWR}}$ signal input.
P11/$\overline{\text{DXRD}}$	8	Port line 11 or emulation $\overline{\text{DXRD}}$ signal input.
DP13/TDAC	9	Derivative I/O port or 14-bit D/A PWM.
P12/DXALE	10	Port line 12 or emulation DXALE signal input.
T3	11	Secondary 8-bit counter input pin (Schmitt-trigger).
P14/DXINT	12	Port line 14 or emulation DXINT signal input.
P00 to P07	13 to 20	General I/O port lines (10 mA).
V_{SS}	21	Ground.
DP00 to DP07/PWM00 to PWM07	29, 28, 27, 26, 25, 24, 23, 22	Derivative I/O port; 6-bit PWM (PWM04 to 07) or 7-bit PWM (PWM00 to 03).
TEST/EMU	30	Control input of testing and emulation mode, normally LOW.
XTAL1	31	Oscillator input terminal for system clock.
XTAL2	32	Oscillator output terminal for system clock.
$\overline{\text{RESET}}$	33	Initialize input, active LOW.
T1	34	Direct testable pin and event counter input.
$\overline{\text{INT}}$/T0	35	External interrupt/direct testable pin.
DP12/AFC2	36	Derivative I/O port or comparator input with 4-bit D/A.
DP11/AFC1	37	
DP10/AFC0	38	
DP21/SCL	39	Derivative port line or I^2C-bus clock line.
DP20/SDA	40	Derivative port line or I^2C-bus data line.
C	41	External capacitor input for on chip PLL OSD oscillator.
V_{DD}	42	Power supply.

Stand-alone OSD PCA8515

FEATURES

- Display RAM: 256 × 13 bits
- Display character fonts: 253 (fixed in ROM, mask programmable)
- Starting position of the first character displayed: 64 vertical and 64 horizontal starting positions can be selected by software
- Character size: 4 different character sizes on a line-by-line basis (1 dot = 1H/1V; 2H/2V; 3H/3V and 4H/4V)
- Character matrix: 12 × 18 with no spacing between characters and no rounding function
- Foreground colours: 16 combinations of Red, Green, Blue and Intensity on character-by-character basis
- Background/shadowing modes: 4 modes available, No background, Box shadowing, North-West shadowing and Frame shadowing (raster blanking) on frame basis
- Background colours: 1 combinations of Red, Green, Blue and Intensity on word-by-word basis. Available when background mode is in either the Box shadowing, North-West shadowing or Frame shadowing mode
- OSD oscillator: on-chip Phase-Locked Loop (PLL)
- Character blinking ratio: 1 : 1, 1 : 3 and 3 : 1 (programmable frequency of $1/16$, $1/32$, $1/64$ or $1/128$ of f_{VSYNC}) on character basis
- Display format: flexible display format by using the Carriage Return Code, maximum number of characters per line is also flexible and depends on the OSD clock frequency
- Spacing between lines: 4 choices comprising 0, 4, 8 and 12 horizontal scan lines
- Display character RAM address-auto-post increment when writing data
- Fast I²C-bus serial interface (400 kbaud) or High-speed 3-wire serial interface (1 Mbaud) for data/command transfer
- ACM (Active Character Monitor) specifically for use in camrecorder applications on word basis; can also be used as a 5th colour control with R, G, B and I signals
- Programmable active input polarity of HSYNC and VSYNC
- Programmable output polarity of R, G, B, I and FB
- Supply voltage: 5 V ±10%
- Operating temperature: −20 to +70 °C
- Package: DIP24 or SO24.

GENERAL DESCRIPTION

The PCA8515 is a member of the PCA85XX CMOS family and is an on-screen character display generator controlled by a microcontroller via the on-chip fast I²C-bus interface or the on-chip High-speed 3-wire serial interface. It is suitable for use in high-end TV or camrecorder applications and has also been designed for use in conventional mid-end TV with advanced graphic features.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA8515P	DIP24	plastic dual in-line package; 24 leads (300 mil)	SOT222-1
PCA8515T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

BLOCK DIAGRAM

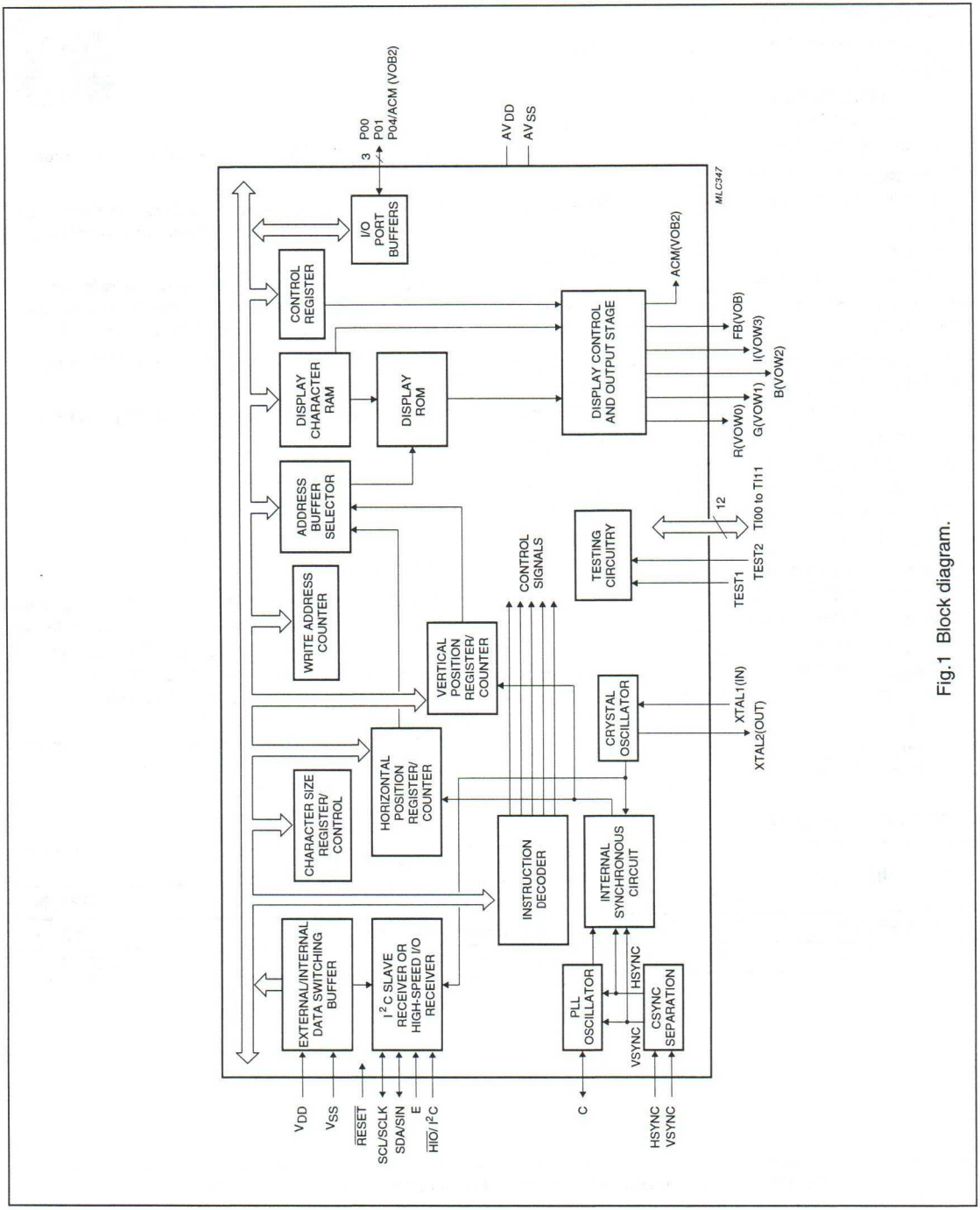


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
I (VOW3)	1	O	Character output signal for intensity control
P04/ACM (VOB2)	2	O	Port 04 output or Active Character Monitor output (VOB2)
TEST2	3	I	Test mode selection; for normal operation TEST2 is connected to V_{SS}.
TEST1	4	I	Test mode selection; for normal operation TEST1 is connected to V_{SS}.
C	5	I/O	Capacitor connection for on-chip OSD PLL oscillator
VSYNC	6	I	Vertical synchronization input, active polarity programmable
HSYNC	7	I	Horizontal synchronization input, active polarity programmable
SDA/SIN	8	I/O	Data line of the I^2C-bus interface or the data line for the High-speed serial interface
SCK/SCLK	9	I/O	Clock line of the I^2C-bus interface or the clock line for the High-speed serial interface
XTAL1 (IN)	10	I	System clock input
XTAL2 (OUT)	11	O	System clock output
V_{SS}	12	I	Ground, digital
$\overline{RESET}$	13	I	Master Reset input (active LOW)
E	14	I	Chip enable (active HIGH) for the High-speed serial interface. When the I^2C-bus interface is selected this pin should be connected to V_{SS}.
$\overline{HIO}/I^2C$	15	I	Serial interface selection. When this pin is LOW the High-speed serial interface is selected; when this pin is HIGH the I^2C-bus interface is selected.
R (VOW0)	16	O	Character output signal: VOW0 for Red
P00	17	I/O	General purpose I/O Port 00
G (VOW1)	18	O	Character output signal: VOW1 for Green
P01	19	I/O	General purpose I/O Port 01
B (VOW2)	20	O	Character output signal: VOW2 for Blue
V_{DD}	21	I	Power supply, digital
FB (VOB)	22	O	Fast Blanking output (VOB)
AV_{SS}	23	I	Ground, analog
AV_{DD}	24	I	Power supply, analog

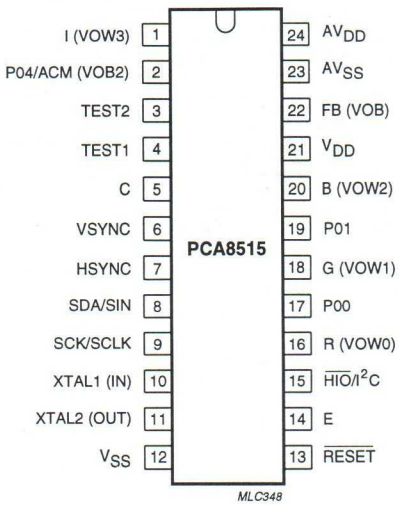


Fig.2 Pin configuration for DIP24.

Stand-alone OSD PCA8516

FEATURES



- Display RAM: 256 × 13 bits
- Display character fonts: 253 (fixed in ROM, mask programmable)
- Starting position of the first character displayed: 64 vertical and 64 horizontal starting positions can be selected by software
- Character size: 4 different character sizes on a line-by-line basis (1 dot = 1H/1V; 2H/2V; 3H/3V and 4H/4V)
- Character matrix: 12 × 18 with no spacing between characters and no rounding function
- Foreground colours: 16 combinations of Red, Green, Blue and Intensity on character-by-character basis
- Background/shadowing modes: 4 modes available, No background, Box shadowing, North-West shadowing and Frame shadowing (raster blanking) on frame basis
- Background colours: 16 combinations of Red, Green, Blue and Intensity on word-by-word basis. Available when background mode is in either the Box shadowing, North-West shadowing or Frame shadowing mode
- OSD oscillator: on-chip Phase-Locked Loop (PLL)
- Character blinking ratio: 1 : 1, 1 : 3 and 3 : 1 (programmable frequency of $1/16$, $1/32$, $1/64$ or $1/128$ of f_{VSYNC}) on character basis
- Display format: flexible display format by using the Carriage Return Code, maximum number of characters per line is also flexible and depends upon the OSD clock frequency
- Spacing between lines: 4 choices comprising 0, 4, 8 and 12 horizontal scan lines
- Display character RAM address auto-post-increment when writing data
- Fast I²C-bus serial interface (400 kbaud) or High-speed 3-wire serial interface (1 Mbaud) for data/command transfer
- ACM (Active Character Monitor) specifically for use in camcorder applications on word basis; can also be used as a 5th colour control with R, G, B and I signals
- Programmable active input polarity of HSYNC and VSYNC
- Programmable output polarity of R, G, B, I and FB
- Supply voltage: 5 V ±10%
- Operating temperature: –20 to +70 °C
- Package: DIP24 or SO24.

GENERAL DESCRIPTION

The PCA8516 is a member of the PCA85XX CMOS family and is an on-screen character display generator controlled by a microcontroller via the on-chip fast I²C-bus interface or the on-chip High-speed 3-wire serial interface. It is suitable for use in high-end TV or camrecorder applications and has also been designed for use in conventional mid-end TV with advanced graphic features.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA8516P	DIP24	plastic dual in-line package; 24 leads (300 mil)	SOT222-1
PCA8516T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

BLOCK DIAGRAM

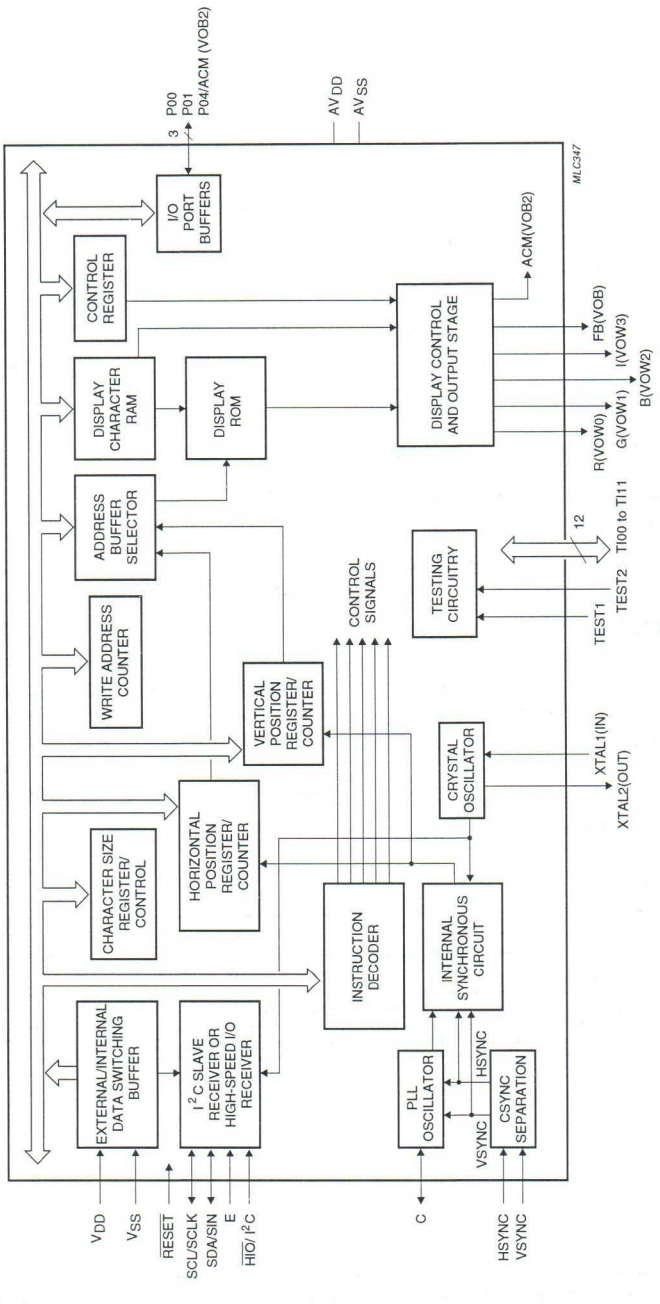


Fig.1 Block diagram.

PINNING

Table 1 DIP24 and SO24 packages

SYMBOL	PIN	I/O	DESCRIPTION
I (VOW3)	1	O	Character output signal for intensity control.
P04/ACM (VOB2)	2	O	Port 04 output or Active Character Monitor output (VOB2).
TEST2	3	I	Test mode selection; for normal operation TEST2 is connected to V_{SS}.
TEST1	4	I	Test mode selection; for normal operation TEST1 is connected to V_{SS}.
C	5	I/O	Capacitor connection for on-chip OSD PLL oscillator.
VSYNC	6	I	Vertical synchronization input, active polarity programmable.
HSYNC	7	I	Horizontal synchronization input, active polarity programmable.
SDA/SIN	8	I/O	Data line of the I^2C-bus interface or the data line for the High-speed serial interface.
SCL/SCLK	9	I/O	Clock line of the I^2C-bus interface or the clock line for the High-speed serial interface.
XTAL1 (IN)	10	I	System clock input.
XTAL2 (OUT)	11	O	System clock output.
V_{SS}	12	I	Ground, digital.
$\overline{RESET}$	13	I	Master Reset input (active LOW).
E	14	I	Chip enable (active HIGH) for the High-speed serial interface. When the I^2C-bus interface is selected this pin should be connected to V_{SS}.
$\overline{HIO}/I^2C$	15	I	Serial interface selection. When this pin is LOW the High-speed serial interface is selected; when this pin is HIGH the I^2C-bus interface is selected.
R (VOW0)	16	O	Character output signal: VOW0 for Red.
P00	17	I/O	General purpose I/O Port 00.
G (VOW1)	18	O	Character output signal: VOW1 for Green.
P01	19	I/O	General purpose I/O Port 01.
B (VOW2)	20	O	Character output signal: VOW2 for Blue.
V_{DD}	21	I	Power supply, digital.
FB (VOB)	22	O	Fast Blanking output (VOB).
AV_{SS}	23	I	Ground, analog.
AV_{DD}	24	I	Power supply, analog.

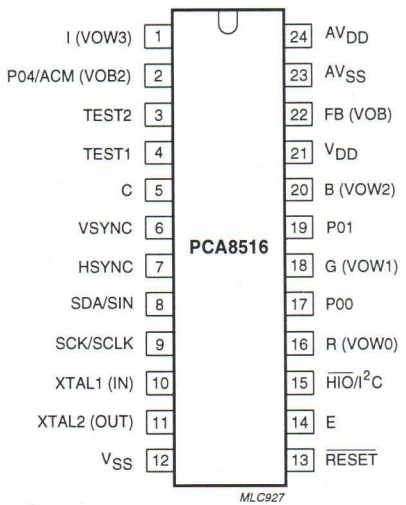


Fig.2 Pin configuration for DIP24.

128 × 8-bit EEPROM with I²C-bus interface PCA8581; PCA8581C

FEATURES

- Operating supply voltage:
  - 4.5 to 5.5 V (PCA8581)
  - 2.5 to 6.0 V (PCA8581C)
- Integrated voltage multiplier and timer for writing (no external components required)
- Automatic erase before write
- Low standby current; maximum 10 µA
- 8-byte page write mode
- Serial input/output bus (I²C-bus)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Designed for minimum 10000 write cycles per byte
- 10 years minimum non-volatile data retention
- Infinite number of read cycles
- Pin and address compatibility to PCF8570, PCF8571 and PCF8582
- Operating temperature: –25 to +85 °C.

GENERAL DESCRIPTION

The PCA8581 and PCA8581C are low power CMOS EEPROMs with standard and wide operating voltages:

4.5 to 5.5 V (PCA8581)

2.5 to 6.0 V (PCA8581C).

In the following text, the generic term 'PCA8581' is used to refer to both types in all packages except when otherwise specified.

The PCA8581 is organized as 128 words of 8-bytes.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. All bytes can be read in a single operation. Up to 8 bytes can be written in one operation, reducing the total write time per byte. Three address pins, A0, A1 and A2 are used to define the hardware address, allowing the use of up to 8 devices connected to the bus without additional hardware.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage				
	PCA8581		4.5	5.5	V
	PCA8581C		2.5	6.0	V
I_{DD}	supply current (standby)	f_{SCL} = 0 Hz	–	10	µA
T_{amb}	operating ambient temperature		–25	+85	°C
T_{stg}	storage temperature	without EEPROM retention	–65	+150	°C
		with EEPROM retention	–65	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA8581P	8	DIP	plastic	SOT97-1
PCA8581CP	8	DIP	plastic	SOT97-1
PCA8581T	8	SO8	plastic	SOT96-1
PCA8581CT	8	SO8	plastic	SOT96-1

BLOCK DIAGRAM

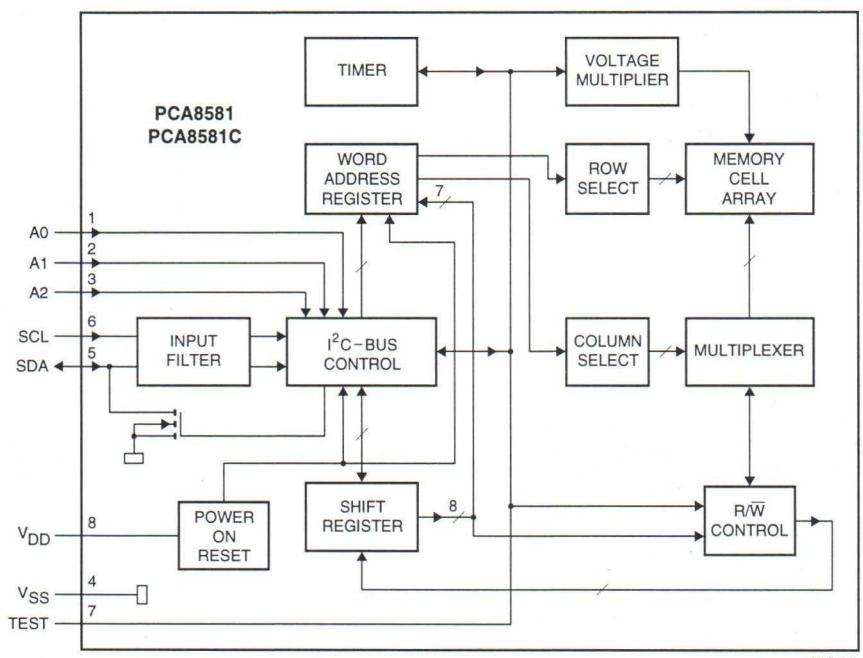


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	hardware address input 0
A1	2	hardware address input 1
A2	3	hardware address input 2
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
TEST	7	test output can be connected to V_{SS}, V_{DD} or left open-circuit
V_{DD}	8	supply

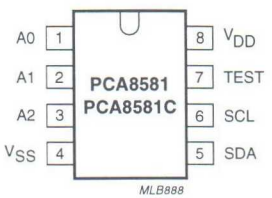


Fig.2 Pin configuration.

Microcontroller for monitor OSD and auto-sync applications

PCE84C886

FEATURES

General

- CMOS 8-bit CPU (enhanced 8048 CPU) with 8 kbytes system ROM and 192 bytes system RAM
- One 8-bit timer/event counter (T1) and one 8-bit counter triggered by external input (T3)
- Four single level vectored interrupt sources: external (INTN), counter/timer, I²C-bus and VSYNCN
- 2 directly testable inputs T0 and T1
- On-chip oscillator clock frequency: 1 to 10 MHz
- On-chip Power-on-reset with low power detector
- Twelve quasi-bidirectional I/O lines, configuration individually selected by mask option
- Idle and Stop modes for reduced power consumption
- Operating temperature: –25 to +85 °C
- Operating voltage: 4.5 to 5.5 V
- Package: SDIP42.

Special

- Master-slave I²C-bus interface
- Four 6-bit Pulse Width Modulated outputs (PWM4 to PWM7)
- Four 7-bit Pulse Width Modulated outputs (PWM0 to PWM3)
- One 14-bit Pulse Width Modulated output (PWM8)
- Three 4-bit ADC channels
- 16 derivative I/O ports.

OSD

- Maximum dot frequency (f_{OSD}): 14 MHz
- Display RAM: 64 × 10 bits
- Display character fonts: 62 + 2 special reserved codes
- Character matrix: 12 × 18 (no spacing between characters)
- 4 character sizes: 1H/1V, 1H/2V, 1H/3V and 1H/4V
- 64 Horizontal starting positions (4 dots for each step)
- 64 Vertical starting positions (4 scan lines for each step)
- Spacing between character rows: 0, 4, 8 and 12 scan lines
- Foreground colours: 8 on a character-by-character basis
- Background colours: 8 on a word-by-word basis
- Background/shadowing modes: 4 modes available, No background, North shadowing, Box shadowing and Frame shadowing (raster blanking) on a frame basis
- On-chip Phase-Locked Loop (PLL) oscillator (auto-sync with HSYNCN) with programmable oscillator for On Screen Display (OSD) function
- Character blinking frequency: programmable using f_{VSYNC} divisors of 16, 32, 64 and 128; on a frame basis
- Character blinking ratios: 1 : 1, 1 : 3 and 3 : 1
- Programmable active level polarities of VSYNCN, HSYNCN, R, G, B and FB
- Flexible display format by using Carriage Return Code
- Auto display RAM address (DCRAR) incremented after write operation to the Character Data Register (DCRCR)
- VSYNCN generates an interrupt (enabled by software) when VIEN is active.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCE84C886	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

Microcontroller for monitor OSD and auto-sync applications

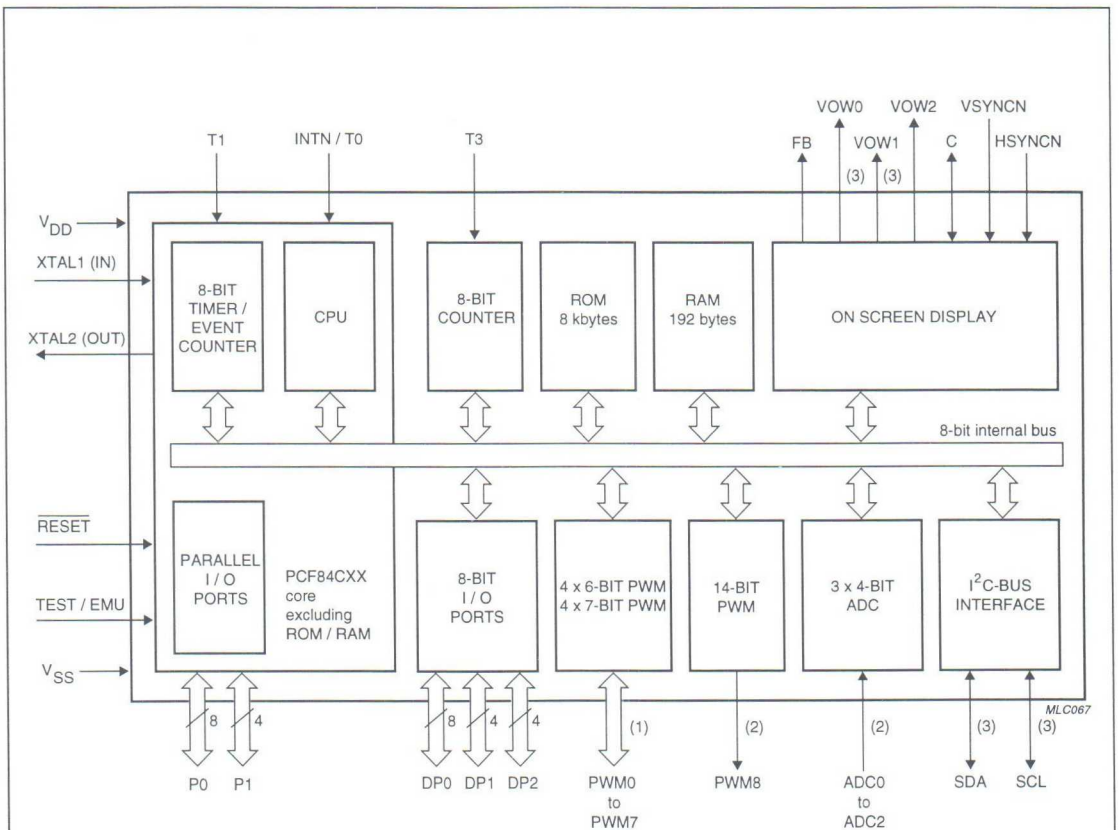
PCE84C886

GENERAL DESCRIPTION

The PCE84C886 is a member of the 84CXXX CMOS microcontroller family. It is suitable for use in 14", 15" and 17" auto-sync monitors for OSD and auto-sync applications. The device uses the PCE84CXX processor core and has 8 kbytes of ROM and 192 bytes of RAM. I/O requirements are adequately catered for with 12 general purpose bidirectional I/O lines plus 16 function combined I/O lines. 9 PWM analog outputs are provided specifically for analog control purposes and also three 4-bit ADCs. The device has an 8-bit counter, suitable for use in pulse counting applications; an 8-bit timer/counter with programmable clock and an on-chip programmable PLL oscillator that generates the OSD clock. In addition to all these features a master-slave I²C-bus interface, 2 directly testable lines and an enhanced OSD facility for flexible screen format (64 character types) are also provided.

The block diagram of the PCE84C886 is shown in Fig.1.

BLOCK DIAGRAM



(1) Alternative function of DP0.
(2) Alternative function of DP1.
(3) Alternative function of DP2.

Fig.1 Block diagram.

PINNING INFORMATION

Pinning

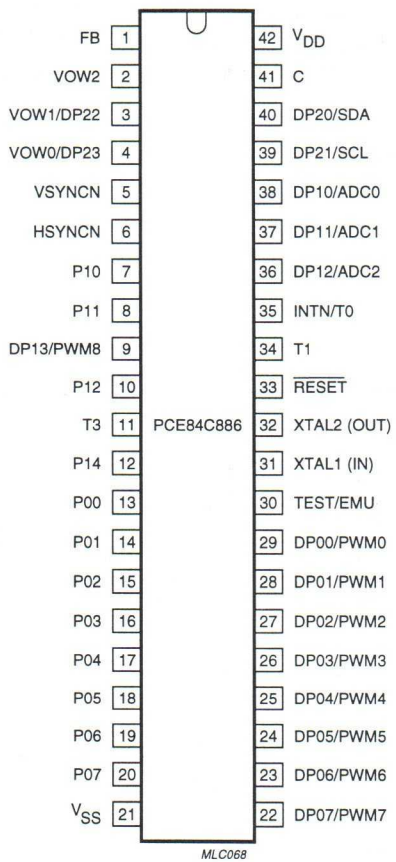


Fig.2 Pin configuration.

Pin description

Table 1 SDIP42 package

SYMBOL	PIN	DESCRIPTION
FB	1	Video Fast Blanking output.
VOW2	2	Video character output VOW2.
VOW1/DP22	3	Video character output VOW1 or Derivative Port line DP22.
VOW0/DP23	4	Video character output VOW0 or Derivative Port line DP23.
VSYNCN	5	Vertical synchronization input.
HSYNCN	6	Horizontal synchronization input.
P10	7	Port line 10 or emulation input $\overline{\text{DXWR}}$.
P11	8	Port line 11 or emulation input $\overline{\text{DXRD}}$.
DP13/PWM8	9	Derivative I/O port or PWM8 output.
P12	10	Port line 12 or emulation input DXALE.
T3	11	Secondary 8-bit counter input (Schmitt trigger).
P14	12	Port line 14 or emulation output DXINT.
P00 to P07	13 to 20	General I/O port lines.
V_{SS}	21	Ground.
DP00/PWM0 to DP07/PWM7	29, 28, 27, 26 25, 24, 23, 22	Derivative I/O ports or PWM outputs.
TEST/EMU	30	Control input for testing and emulation mode, normally LOW.
XTAL1 (IN)	31	Oscillator input pin for system clock.
XTAL2 (OUT)	32	Oscillator output pin for system clock.
$\overline{\text{RESET}}$	33	Reset input; active LOW input initializes device.
T1	34	Direct testable pin or event counter input.
INTN/T0	35	External interrupt or direct testable pin.
DP10/ADC0	38	Derivative I/O port or ADC Channel 0 input.
DP11/ADC1	37	Derivative I/O port or ADC Channel 1 input.
DP12/ADC2	36	Derivative I/O port or ADC Channel 2 input.
DP21/SCL	39	Derivative port line or I^2C-bus clock input.
DP20/SDA	40	Derivative port line or I^2C-bus data input.
C	41	External capacitor input for on-chip oscillator.
V_{DD}	42	Power supply.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

18-ELEMENT BAR GRAPH LCD DRIVER

GENERAL DESCRIPTION

The PCF1303T is an 18-element bar graph LCD driver with linear relation to control voltage (V_C) when in pointer or thermometer mode.

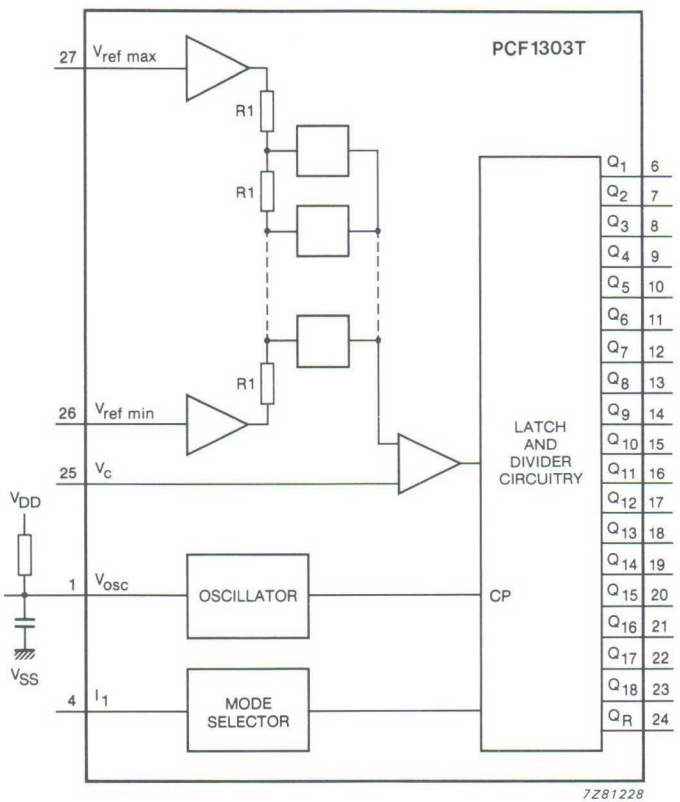
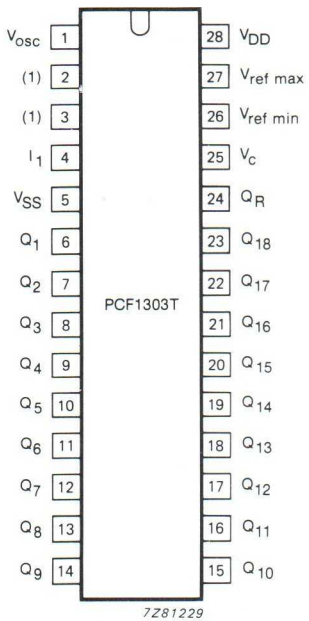


Fig. 1 Block diagram.

PACKAGE OUTLINE

PCF1303T: 28-lead mini-pack; plastic (SO28; SOT136A).



(1) Pins 2 and 3 should be connected to V_{SS}.

Fig. 2 Pin configuration.

PIN DESCRIPTION

pin no.	symbol	name and function
1	V_{osc}	oscillator pin
4	I_1	mode select input
5	V_{SS}	ground (0 V)
6 to 23	Q_1 to Q_{18}	segment outputs
24	Q_R	back-plane output
25	V_c	control voltage
26 27	$V_{ref\ min}$ $V_{ref\ max}$	reference voltage inputs
28	V_{DD}	positive supply voltage

FUNCTION TABLE

I_1	mode
L	pointer
H	thermometer

H = HIGH voltage level
L = LOW voltage level

8 K x 8-bit static CMOS EEPROM with PAGE-ERASE option

PCF29F64

FEATURES

- Low Power CMOS
  - maximum active current 10 mA
  - maximum standby current 200 µA
- Access time 200 ns
- Fast Erase cycle time
  - 32-byte Erase operation (PAGE-Erase) 5 ms
  - 256-byte Erase operation (BLOCK-Erase) 5 ms
  - complete Memory Erase operation 5 ms
- Fast Write cycle time 2.5 ms
- $\overline{\text{Data}}$ Polling allows user to minimize Write cycle time
- Simple Write operation
  - single TTL-level $\overline{\text{WE}}$ signal
  - internally latched address and data
  - automatic Write timing
- Endurance 10 000; T_{amb} = 85 °C
- 10 years non-volatile data retention time.

GENERAL DESCRIPTION

The PCF29F64 is an 8 K x 8-bit floating gate electrically erasable programmable read only memory (EEPROM), fabricated in a 1.2 micron n-channel floating gate CMOS technology.

Power consumption is very low and reliability is high due to the full CMOS technology used, as that for the PCX8582 family.

Three different Erase-operation modes are offered by the PCF29F64:

- 32-byte Erase operation (PAGE)
- 256-byte Erase operation (BLOCK)
- Complete Memory Erase operation

A write operation is performed in approximately 2.5 ms, which allows the entire memory to be written in less than 21 s.

The PCF29F64 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

Philips EPROMs and PAGE-EEPROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	–	5.5	V
I_{DDR}	supply current READ				
	CMOS inputs	–	–	5	mA
I_{DDW}	supply current WRITE/ERASE				
	CMOS inputs	–	–	10	mA
I_{DDO}	standby supply current				
	CMOS input level	–	–	200	µA
	TTL input level	–	–	2	mA

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF29F64P	28	DIL	plastic	SOT117
PCF29F64T	28	SO28	plastic	SOT136

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC10 OR DATA SHEET

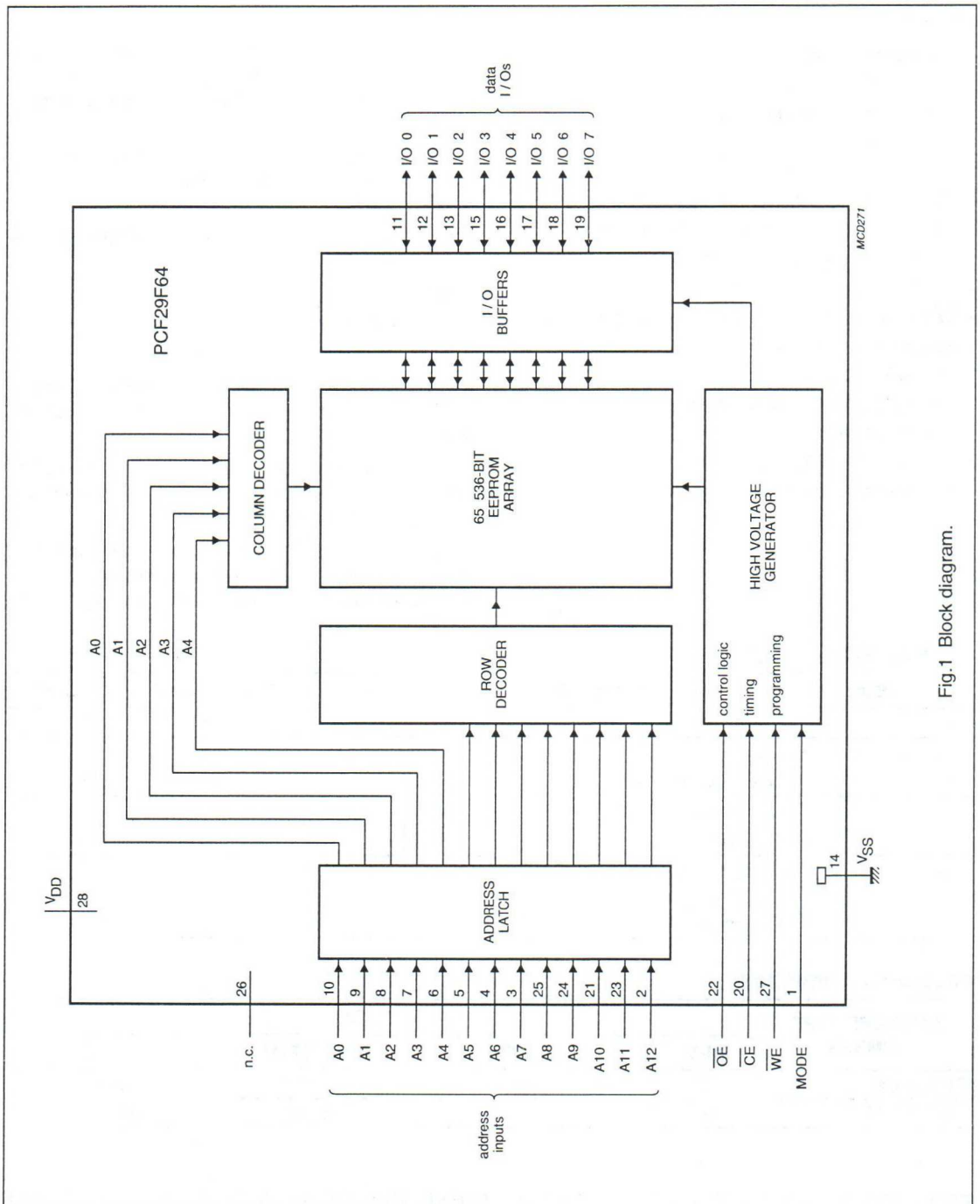


Fig.1 Block diagram.

8 K x 8-bit static CMOS EEPROM with PAGE-ERASE option

PCF29F64

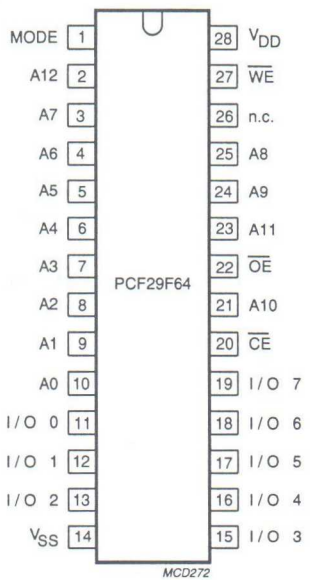


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
MODE	1	selection of Erase mode is achieved by a HIGH at this input, LOW selects the Write mode
A0 to A7 A8, A9 A10, A11, A12	10 to 3 25, 24 21, 23, 2	address inputs which select an 8-bit memory location during a read or write operation
I/O 0 to I/O 7	11 to 13, 15 to 19	data is written to or read from the PCF29F64 via the I/O pins
V_{SS}	14	negative supply voltage
$\overline{CE}$	20	Chip Enable input which must be LOW to enable all read/write operations, when HIGH power consumption is reduced
$\overline{OE}$	22	Output Enable input which controls the data output buffers and is used to initiate read operations
n.c.	26	not connected
$\overline{WE}$	27	Write Enable input which controls the writing of data to the PCF29F64
V_{DD}	28	positive supply voltage

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.3	+7.0	V
V_I	voltage on any input pin	$\lvert Z_I \rvert > 500\ \Omega$	V_{SS} −0.8	V_{DD} +0.8	V
I_I	current on any input pin		–	1	mA
I_O	output current		–	5	mA
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C

LCD controller/drivers

PCF2116 family (PCF2114X; PCF2116X)

FEATURES

- Single chip LCD controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- On-chip:
  - generation of LCD supply voltage (external supply also possible)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

GENERAL DESCRIPTION

The PCF2116 family of LCD controller/drivers consists of 2 similar members: PCF2116X and PCF2114X, later referred to as PCF2116. The letter X in PCF2116X or PCF2114X specifies the character set in the character generator ROM (CGROM). The different character sets currently available are specified by the letters A, C, G and J. Set 'A' in PCF2116A characterises the built-in standard character set. Other character sets are available on request.

The PCF2116 is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system power consumption. The chip contains a character generator and displays alphanumeric and kana characters. The PCF2116 interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus.

Packages

- PCF2116XU/10; chip on FFC
- PCF2114XU/10; chip on FFC
- PCF2116XU/12; chip with bumps on FFC
- PCF2114XU/12; chip with bumps on FFC
- PCF2116XH; SQFP128 (14 × 20 mm)
- Pin grid array PGA144 (samples only).

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF2114XH	128	SQFP128	plastic	SOT387-1
PCF2116XH	128	SQFP128	plastic	SOT387-1
PCF2114XU	116	FFC116	–	–
PCF2116XU	116	FFC116	–	–

BLOCK DIAGRAM

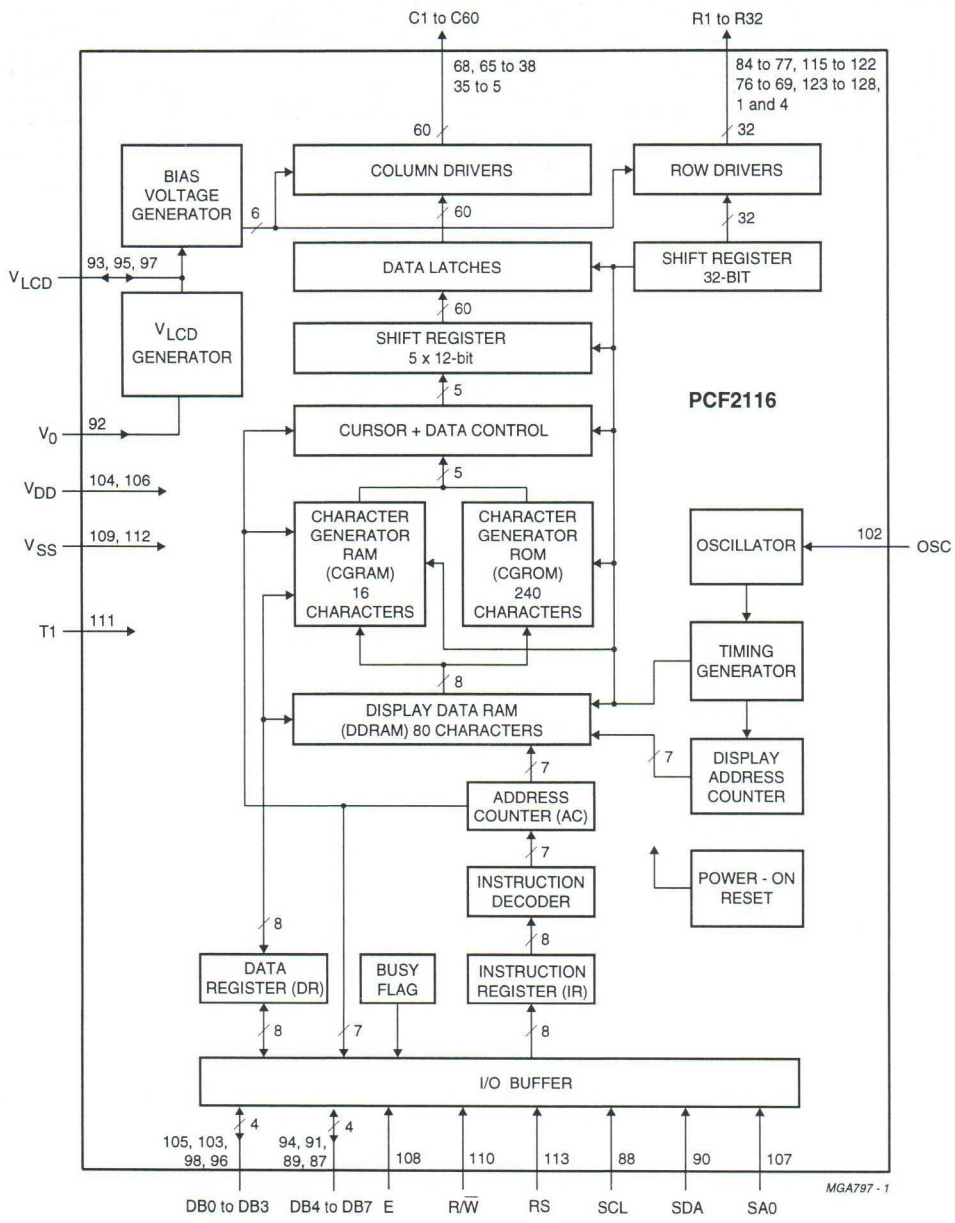


Fig.1 Block diagram (SQFP128).

PINNING

SYMBOL	SQFP128 PIN	FFC PAD	DESCRIPTION
R31	1	27	LCD row driver output
n.c.	2 and 3	–	not connected
R32	4	28	LCD row driver output
C60 to C30	5 to 35	29 to 59	LCD column driver outputs 60 to 30
n.c.	36 and 37	–	not connected
C29 to C2	38 to 65	60 to 87	LCD column driver outputs 29 to 2
n.c.	66 and 67	–	not connected
C1	68	88	LCD column driver output 1
R24 to R17	69 to 76	89 to 96	LCD row driver outputs
R8 to R1	77 to 84	97 to 104	LCD row driver outputs
n.c.	85 and 86	–	not connected
DB7	87	105	bidirectional data bus
SCL	88	106	I^2C serial clock input
DB6	89	107	bidirectional data bus
SDA	90	108	I^2C serial data input/output
DB5	91	109	bidirectional data bus
V_0	92	110	control input for V_{LCD}
V_{LCD1}	93	111	LCD supply voltage
DB4	94	112	bidirectional data bus
V_{LCD2}	95	113	LCD supply voltage
DB3	96	114	bidirectional data bus
V_{LCD3}	97	115	LCD supply voltage
DB2	98	116	bidirectional data bus
n.c.	99 to 101	–	not connected
OSC	102	1	oscillator/external clock input
DB1	103	2	bidirectional data bus
V_{DD2}	104	3	supply voltage
DB0	105	4	bidirectional data bus
V_{DD1}	106	5	supply voltage
SA0	107	6	I^2C address pin
E	108	7	data bus clock
V_{SS1}	109	8	ground (logic)
$R/\overline{W}$	110	9	read/write
T1	111	10	test pad (connect to V_{SS})
V_{SS2}	112	11	ground (logic)
RS	113	12	register select
n.c.	114	–	not connected
R9 to R16	115 to 122	13 to 20	LCD row driver outputs
R25 to R30	123 to 128	21 to 26	LCD row driver outputs

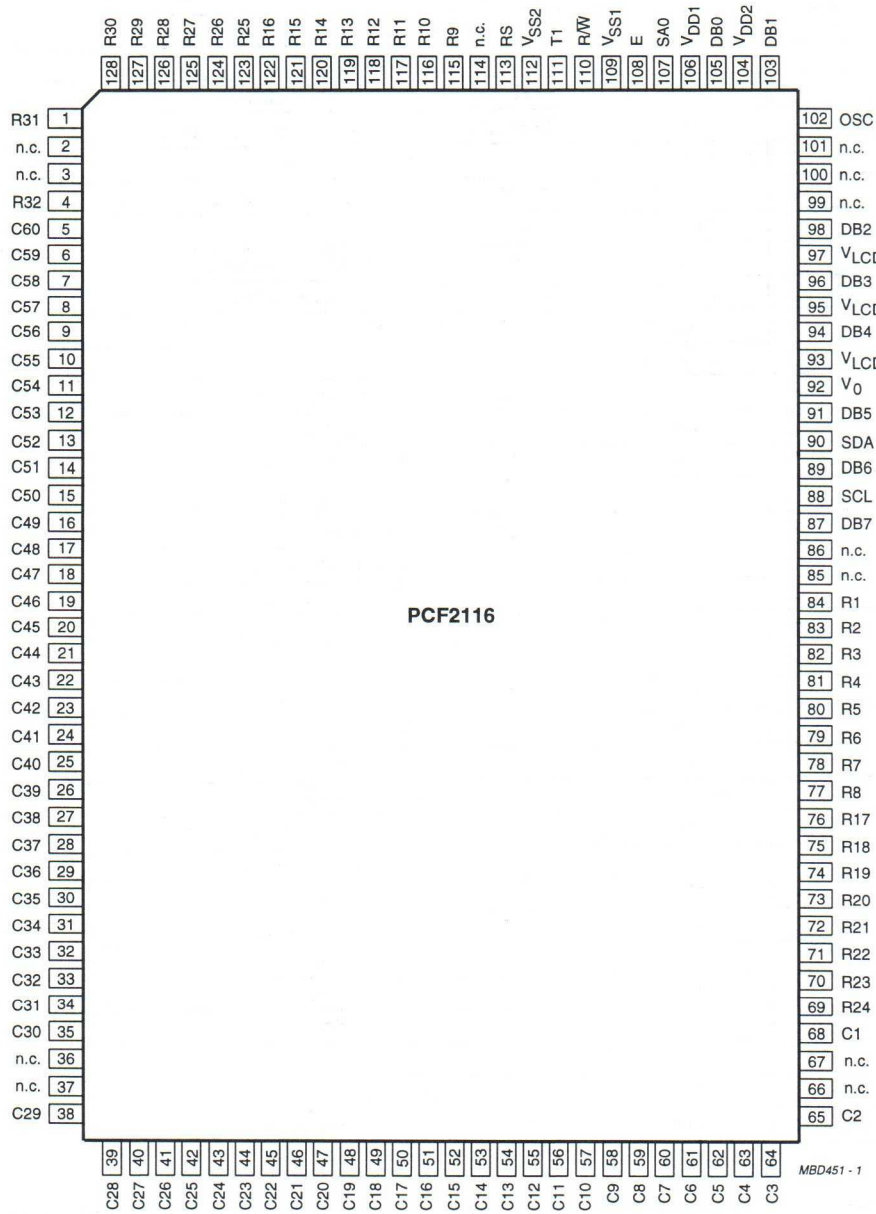


Fig.2 Pin configuration (SQFP128).

8-Bit Microcontroller

PCF84C12A, PCF84C22A, PCF84C42A

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 20-lead package
- 1k ROM bytes (PCF84C12A)
- 2k ROM bytes (PCF84C22A)
- 4k ROM bytes (PCF84C42A)
- 64 RAM bytes
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 13 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- Two single-level vectored interrupts: external, 8-bit programmable timer/event counter 1
- Two test inputs, one of which also serves as the external interrupt input
- Stop and idle modes
- Logic supply V_{DD}: 2.5 V to 5.5 V
- Clock frequency: 1 MHz to 16 MHz - Operating temperature range: –40 °C to 85 °C
- Manufactured in silicon gate CMOS process

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCF84C12A, PCF84C22A and PCF84C42A. The shared characteristics of the PCF84CXXXA family of microcontrollers are described in the PCF84CXXXA family data sheet, which should be read in conjunction with this publication.

The PCF84C12A, PCF84C22A and PCF84C42A are general purpose CMOS microcontrollers with 1k, 2k and 4k bytes of program memory, respectively. They include 64 bytes of RAM and 13 I/O port lines. The instruction set is based on that of the MAB8048 and is software compatible with the PCF84CXXXA family.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF84C12AP/22AP/42AP	20	DIL	plastic	SOT146
PCF84C12AT/22AT/42AT	20	mini-pack	plastic	SOT163A

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

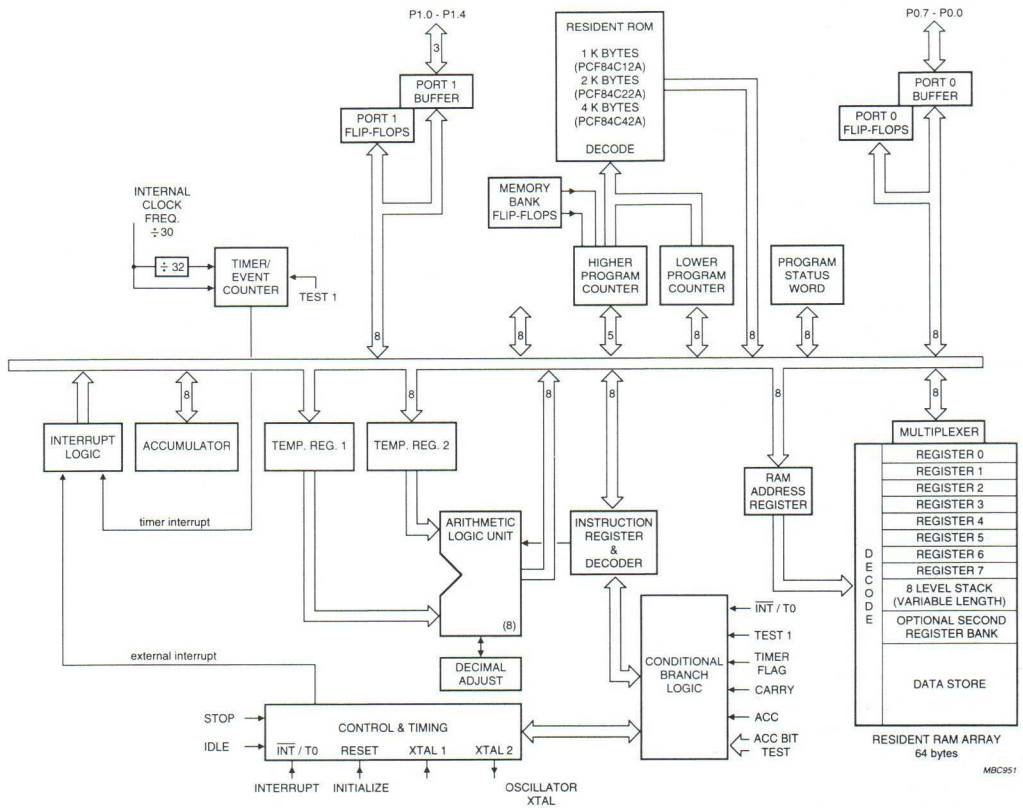


Fig.1 PCF84C12A/22A/42A Block diagram.

PINNING

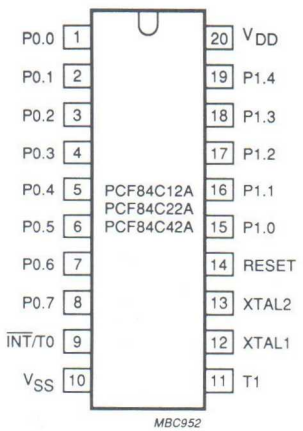


Fig.2 Pinning diagram.

Table 1 Pin description

SYMBOL	PIN	TYPE	FUNCTION
P0.0-P0.7	1-8	I/O	Port 0: quasi-bidirectional I/O lines
INT/T0	9	I	interrupt / test 0
V_{SS}	10	P	ground
T1	11	I	test 1/count input of 8-bit timer/event counter 1
XTAL1	12	I	crystal oscillator / external clock
XTAL2	13	O	crystal oscillator output
RESET	14	I	reset input
P1.0-P1.4	15-19	I/O	Port 1:quasi-bidirectional I/O lines
V_{DD}	20	P	positive supply

Telecom Microcontroller

PCF84C21A, PCF84C41A, PCF84C81A

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead package
- 2k ROM bytes, 64 RAM bytes (PCF84C21A)
- 4k ROM bytes, 128 RAM bytes (PCF84C41A)
- 8k ROM bytes, 256 RAM bytes (PCF84C81A)
- Serial I/O interface with multi-master capability
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O Port lines
- High sink current capability on the 8 lines of Port 1
- 8-bit programmable timer/event counter 1
- 3 single-level vectored interrupts: external, 8-bit programmable timer/event counter 1, SIO
- Two test inputs, one of which also serves as the external interrupt input
- Stop and Idle modes
- Positive supply V_{DD}: 2.5 V to 5.5 V
- Clock frequency: 1 MHz to 16 MHz - Operating temperature range: –40 °C to 85 °C
- Manufactured in silicon gate CMOS process

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCF84C21A, PCF84C41A and PCF84C81A. The shared characteristics of the PCF84CXXXA family of microcontrollers are described in the PCF84CXXXA family data sheet, which should be read in conjunction with this publication.

The PCF84C21A, PCF84C41A and PCF84C81A are general purpose CMOS microcontrollers with 2k, 4k and 8k bytes of program memory and 64, 128 and 256 bytes of RAM, respectively. In addition to 20 I/O port lines, the microcontrollers provide an on-chip serial I/O interface. This two-line serial bus extends the microcontroller capabilities when implemented with the powerful I²C bus devices of the PCF85XX, PCD33XX and "Clips" peripheral families. These include liquid crystal display drivers, telecom circuits, AD/DA converters, clock/calendar circuits, EEPROM and RAM. The instruction set is based on that of the MAB8048 and is software compatible with the PCF84CXXXA family.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF84C21AP	28	DIL	plastic	SOT117
PCF84C41AP	28	DIL	plastic	SOT117
PCF84C81AP	28	DIL	plastic	SOT117
PCF84C21AT	28	mini-pack	plastic	SOT136A
PCF84C41AT	28	mini-pack	plastic	SOT136A
PCF84C81AT	28	mini-pack	plastic	SOT136A

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

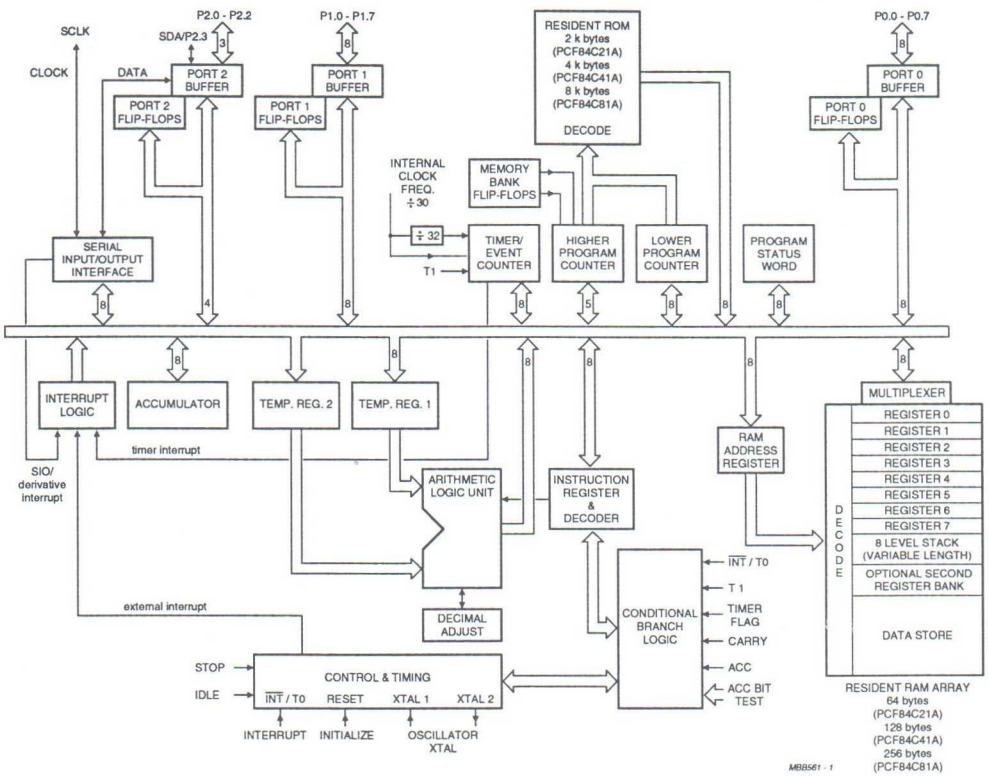


Fig.1 PCF84C21A/41A/81A block diagram.

PINNING



Fig.2 Pin configuration

PIN DESCRIPTION

SYMBOL	PIN	FUNCTION
P2.2	1	Port 2: quasi-bidirectional I/O line
SDA/P2.3	2	bidirectional data line of the serial I/O interface Port 2: quasi-bidirectional I/O line
SCLK	3	bidirectional clock line of the serial I/O interface
P0.0-P0.7	4-11	Port 0: quasi-bidirectional I/O lines
$\overline{INT}$/T0	12	interrupt/test 0
T1	13	test 1/count input of 8-bit timer/event counter 1
V_{SS}	14	ground
XTAL1	15	crystal oscillator/external clock
XTAL2	16	crystal oscillator output
RESET	17	reset input
P1.0-P1.7	18-25	Port 1: quasi-bidirectional I/O lines
P2.0-P2.1	26-27	Port 2: quasi-bidirectional I/O lines
V_{DD}	28	positive supply

8-bit microcontrollers PCF84CXXXA Family

INTRODUCTION

This data sheet describes the shared properties of the PCF84CXXXA family of microcontrollers and its quickly growing number of derivative microcontrollers. For a particular microcontroller, this data sheet should be read in conjunction with the individual data sheet of the specific device.

FEATURES

- 8-bit CPU, ROM, RAM, I/O all in one package
- Up to 8 kbytes ROM
- Up to 256 bytes RAM
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 8 or more quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- 3 single-level vectored interrupts: external, timer/event counter, SIO/derivative
- Two test inputs, one of which also serves as the external interrupt input
- Serial I/O interface (some devices only)
- Power-on-reset, Stop and Idle modes
- Supply voltage range: 2.5 to 6 V
- Clock frequency: 1 to 16 MHz
- Operating temperature: –40 to +85 °C
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The PCF84CXXXA family of microcontrollers provide up to 8 kbytes of program memory and up to 256 bytes of RAM. All devices include flexible I/O ports, an 8-bit programmable timer/event counter and a choice of single-level vectored interrupts. The instruction set is based on that of the well-known MAB8048. Being similar to the MAB8400 family of NMOS controllers, some devices can serve as CMOS replacements, especially where the lower power consumption and higher speed provide advantages.

A range of prototyping devices with external program memory and 'Piggy-backs', as well as emulation probes and prototyping systems are available.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

BLOCK DIAGRAM

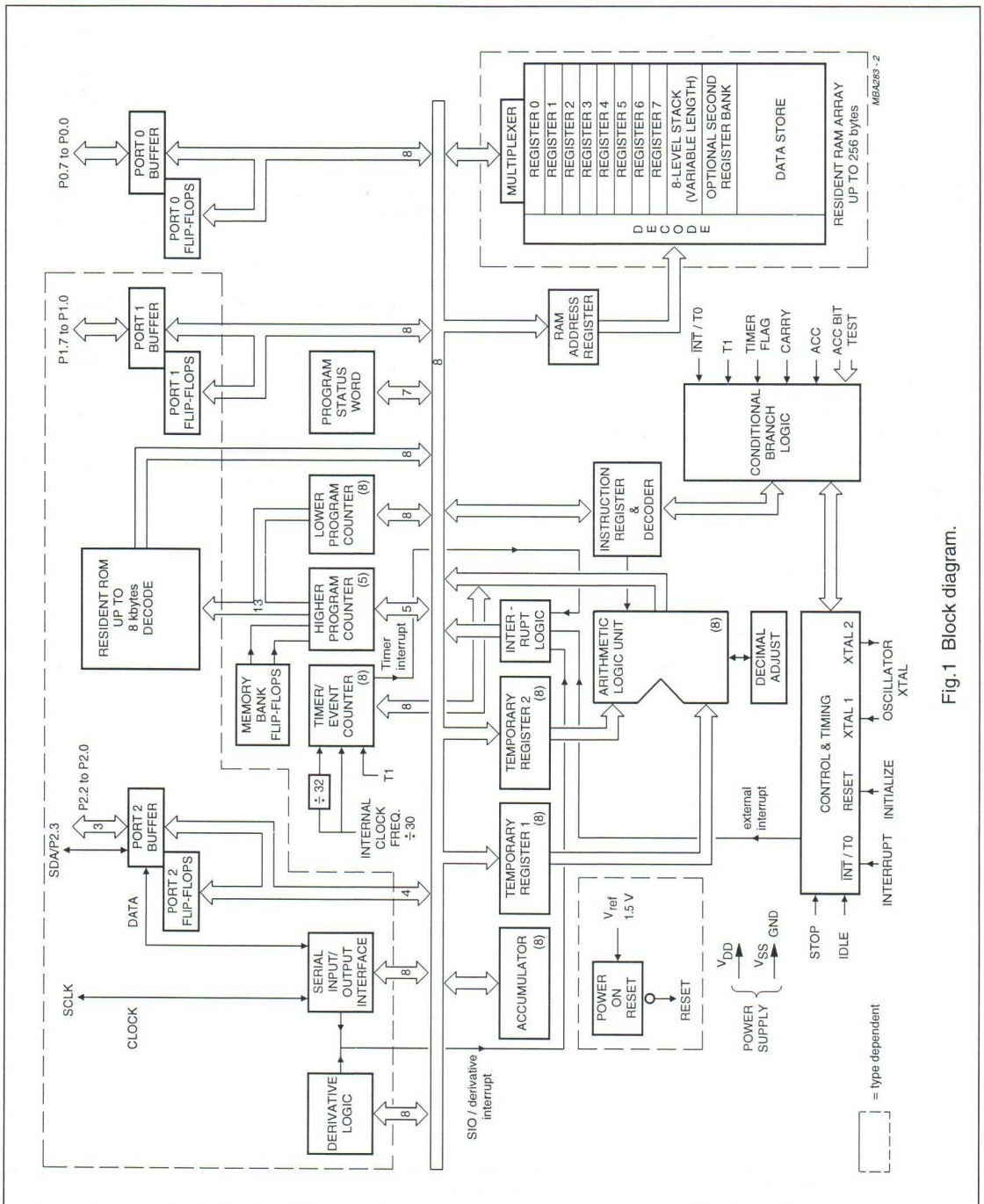


Fig.1 Block diagram.

PINNING

For individual pinning configurations consult the data sheet of the specific device.

Table 1 describes the common functions of the devices. For full details of pin descriptions consult the data sheet of the specific device.

Table 1 Common functions.

SYMBOL	TYPE	DESCRIPTION
V_{SS}	P	Ground
V_{DD}	P	Positive supply voltage
XTAL1	I	Crystal oscillator/external clock input
XTAL2	O	Crystal oscillator output
RESET	I	Reset input
$\overline{INT}$/T0	I	Interrupt/Test 0
T1	I	Test 1/count input of 8-bit timer/event counter 1
P0.0 to P0.7	I/O	Port 0: quasi-bidirectional I/O lines
P1.0 to P1.7	I/O	Port 1: quasi-bidirectional I/O lines
P2.0 to P2.2	I/O	Port 2: quasi-bidirectional I/O lines
SDA/P2.3	I/O	bidirectional data line of the serial I/O interface/Port 2: quasi-bidirectional I/O line
SCLK	I/O	bidirectional clock line of the serial I/O interface

Microcontroller with extended I/O PCF84C85A

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead package
- 8 kbytes ROM
- 256 bytes RAM
- Serial I²C-bus interface with multi-master capability
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 32 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- 3 single-level vectored interrupts:
  - external
  - 8-bit programmable timer/event counter 1
  - SIO
- Two test inputs, one of which also serves as the external interrupt input
- Stop and Idle modes
- Logic supply voltage: V_{DD} = 2.5 to 5.5 V
- Clock frequency: 1 to 16 MHz
- Operating temperature: –40 to +85 °C
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCF84C85A. The shared characteristics of the PCF84CXXXA family of microcontrollers are described in the *"PCD84XXXA family data sheet"* which should be read in conjunction with this publication.

The PCF84C85A is a general purpose CMOS microcontroller with emphasis on input/output. It provides 32 I/O port lines, 8 kbytes of program memory and 256 bytes of RAM. In addition to 20 I/O port lines, the microcontroller provides an on-chip serial I/O interface. This two-line serial bus extends the microcontroller's capabilities when implemented with the powerful I²C-bus devices of the PCF85XX, PCD33XX and 'Clips' peripheral families.These include liquid crystal display drivers, telecom circuits, AD/DA converters, clock/calendar circuits, EEPROM and RAM.

The instruction set is based on that of the MAB8048 and is software compatible with the PCF84CXXXA family.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF84C85AP	40	DIP	plastic	SOT129-1
PCF84C85AT	40	VSO40	plastic	SOT158-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

BLOCK DIAGRAM

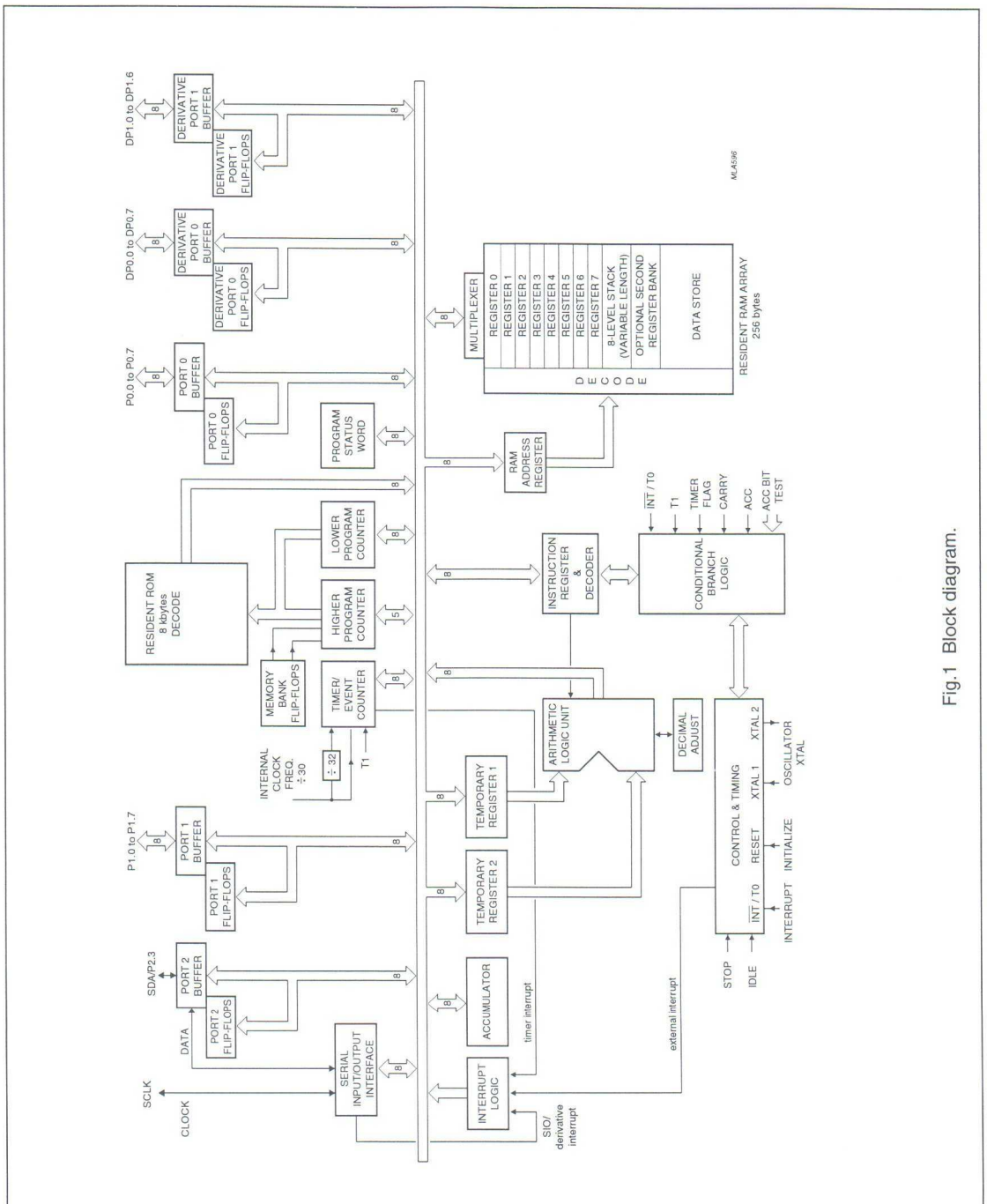


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
$\overline{INT}$/T0	1	I	Interrupt/Test 0
P0.0 to P0.7	2 to 9	I/O	Port 0: quasi-bidirectional I/O lines
P1.0 to P1.7	10 to 17	I/O	Port 1: quasi-bidirectional I/O lines
XTAL1	18	I	XTAL input: crystal oscillator/external clock input
XTAL2	19	O	XTAL output: crystal oscillator output
V_{SS}	20	P	ground
RESET	21	I	Reset input
DP0.0 to DP0.7	22 to 29	I/O	Derivative Port 0: quasi-bidirectional I/O lines
DP1.0 to DP1.6	30 to 36	I/O	Derivative Port 1: quasi-bidirectional I/O lines
SDA/P2.3	37	I/O	Port 2: bidirectional data line of the serial I/O interface/ quasi-bidirectional I/O line
SCLK	38	I/O	bidirectional clock line of the serial I/O interface
T1	39	I	Test 1: count input of 8-bit timer/event counter 1
V_{DD}	40	P	positive supply

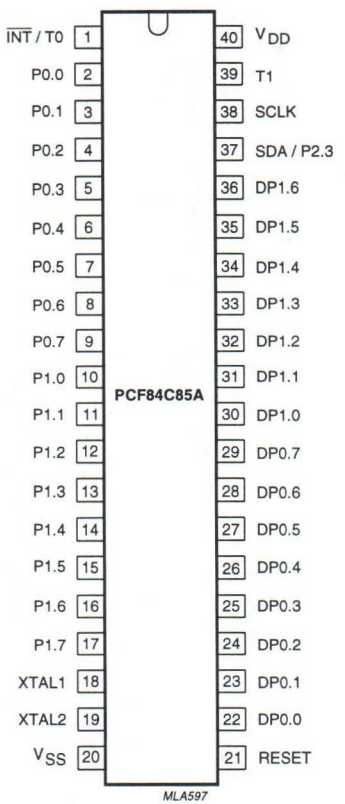


Fig.2 Pin configuration.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH LCD DRIVER

DESCRIPTION

The PCF84C430 microcontroller is a derivative of the 84CXXX family of microcontrollers and is manufactured in CMOS technology. For detailed information see the 84CXXX family specification.

The PCF84C430 contains a PCF84CXX core CPU and is completely software compatible. In addition, the PCF84C430 contains an LCD driver supporting four back planes and a maximum driving capacity of up to 96 segments.

The PCF84C430 has 16 quasi-bidirectional I/O port lines, plus a derivative 8-bit port, a serial I/O interface, a single-level vectored interrupt circuit, an 8-bit timer/event counter and on-board clock oscillator and clock circuits.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 64-lead QFP package
- 4 K ROM bytes
- 128 RAM bytes
- On-chip LCD driver with 24 outputs (max. 96 segments)
- LCD multiplexing rates at 1:1 (static), 1:2, 1:3 and 1:4
- Low-power oscillator for LCD driver during STOP mode
- 25 quasi-bidirectional I/O port lines are configured as two 8-bit ports, a 1-bit port (shared with SDA) and an 8-bit derivative port
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C-bus hardware interface for serial data transfer on two separate lines
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V ($V_{SS} \leqslant V_{LCD} < V_{DD}$)
- STOP and IDLE mode
- Power-on-reset circuit
- Operating temperature range: −40 to + 85 °C

PACKAGE OUTLINE

PCF84C430H: 64-lead quad flat-pack; plastic (SOT208).

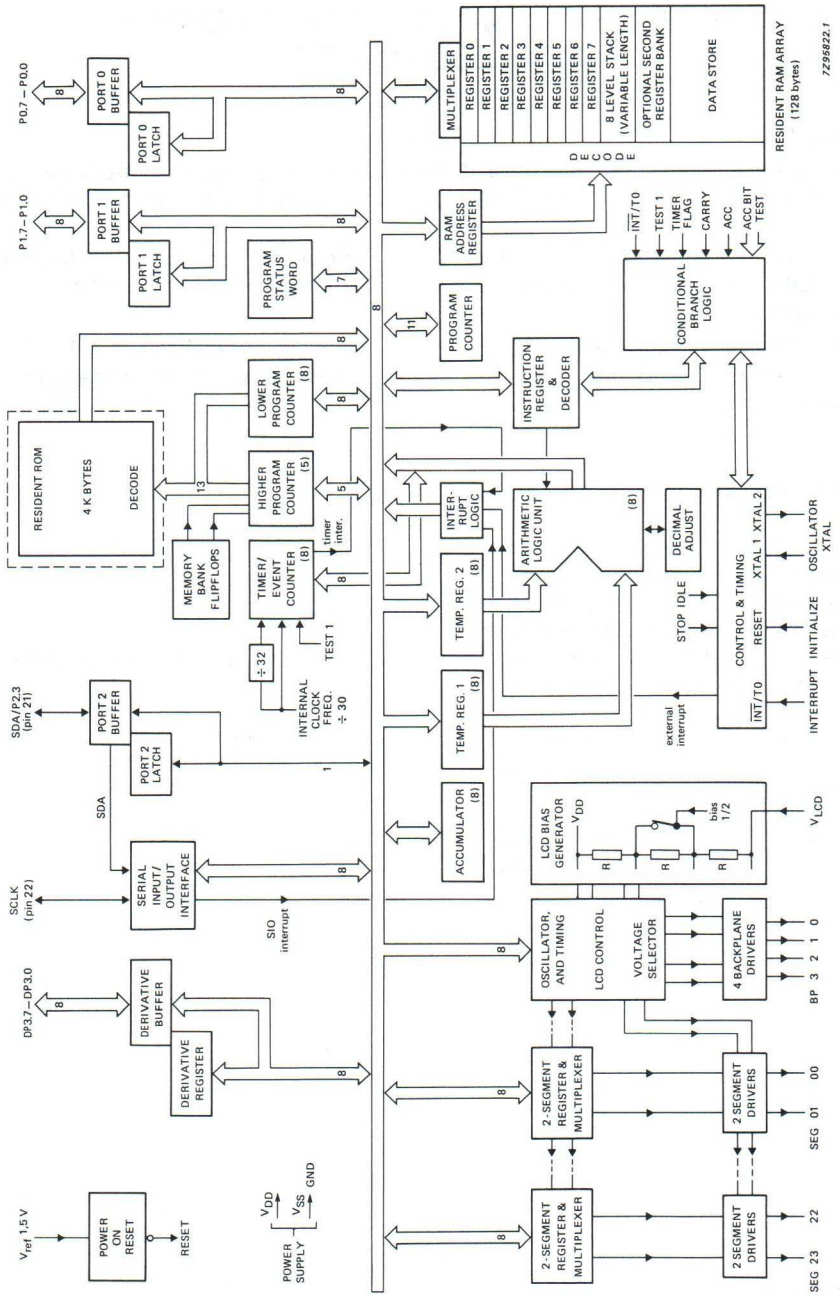


Fig. 1 Block diagram; PCF84C430.

PINNING

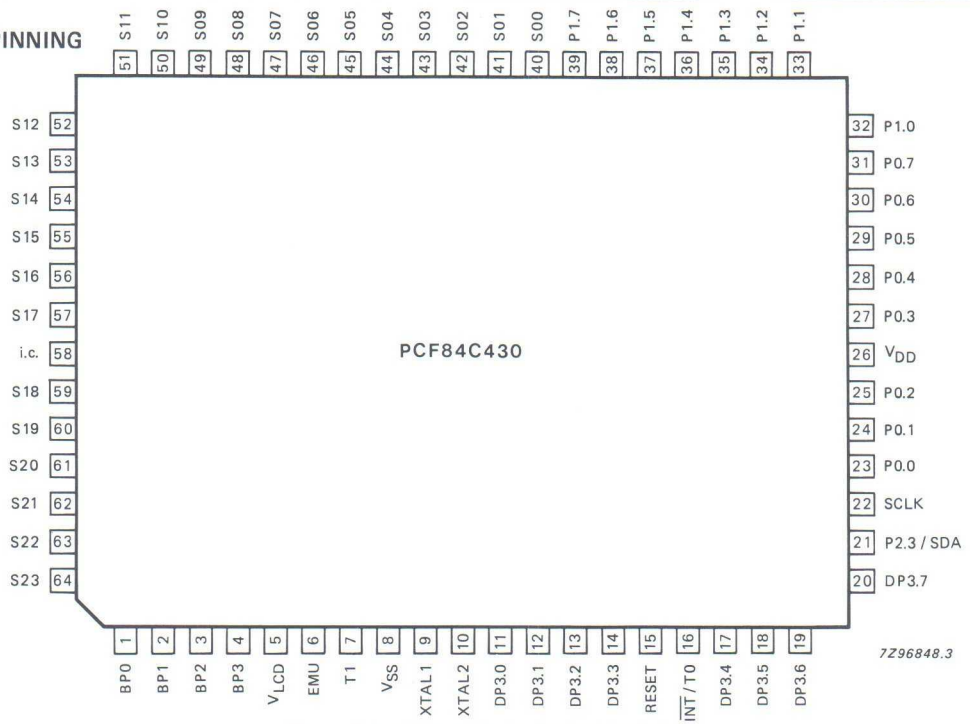


Fig. 2 Pin designation of the PCF84C430.

PIN DESIGNATION

pin	symbol	type	function
1-4	BP0-BP3	O	**LCD**: backplane outputs.
5	V_{LCD}		**LCD**: supply ground level.
6	EMU	I	**EMU pin:** to be grounded for normal operation.
7	T1	I	**Test 1:** test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
8	V_{SS}		**Ground:** circuit earth potential.
9	XTAL1	I	**Oscillator input:** crystal which determines the internal oscillator frequency or the external clock generator.
10	XTAL2	I/O	Connection to other side of oscillator.
11-14	DP3.0-DP3.3	I/O	**Derivative port 3:** 8-bit parallel port LSBs.
15	RESET	I/O	**Reset input:** used to initialize the processor (active HIGH), or output of power-on-reset circuit.
16	$\overline{INT}$/T0	I	**Interrupt/Test 0:** external interrupt input (sensitive to negative going edge)/test input; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
17-20	DP3.4-DP3.7	I/O	**Derivative port 3:** 8-bit parallel port MSBs.
21	SDA/P23	I/O	**Serial data:** input/output in serial I/O mode. If not selected as serial data pin, P23 functions as a quasi-bidirectional I/O line.
22	SCLK	I/O	**Serial clock:** bidirectional clock for serial I/O.
23-25 27-31	P0.0-P0.7	I/O	**Port 0:** 8-bit quasi-bidirectional I/O port.
26	V_{DD}		**Power supply:** 2,5 V to 5,5 V.
32-39	P1.0-P1,7	I/O	**Port 1:** 8-bit quasi-bidirectional I/O port.
40-57 59-64	S00-S23	O	**LCD** segment driver outputs.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT129).
PCF8566T: 40-lead mini-pack (VSO40; SOT158A).

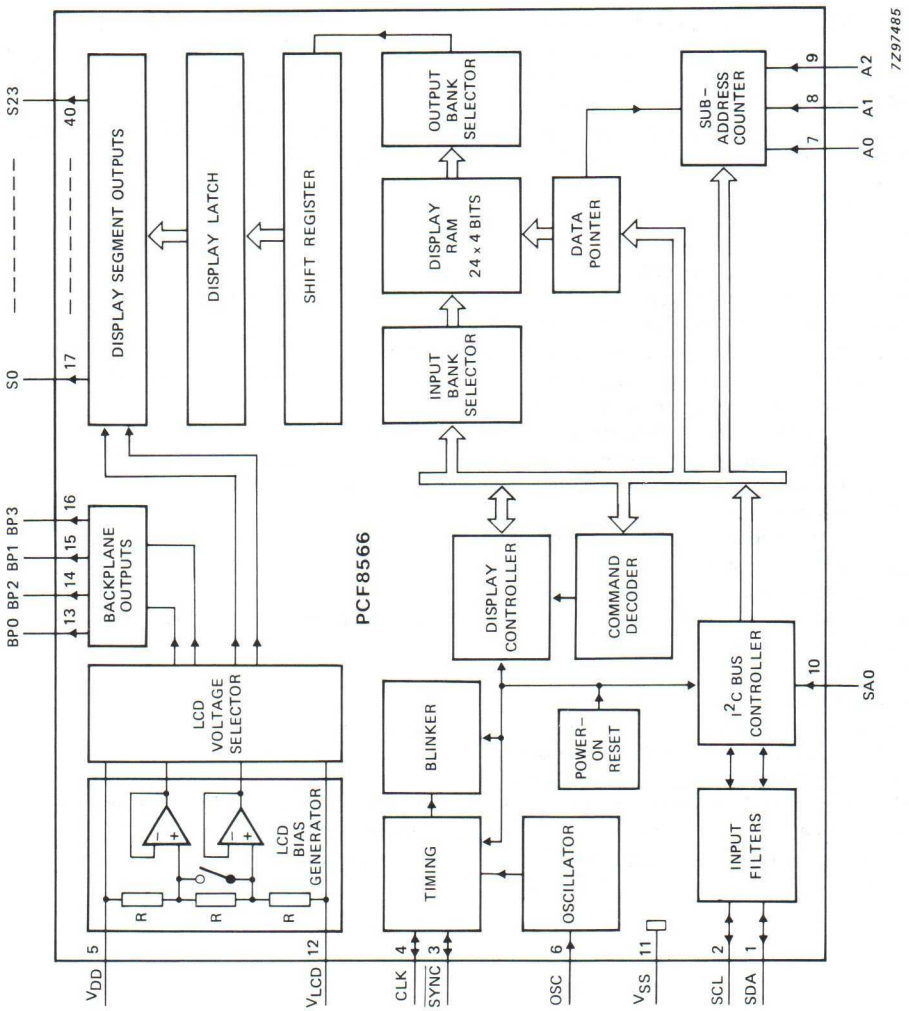


Fig. 1 Block diagram.

DEVELOPMENT DATA

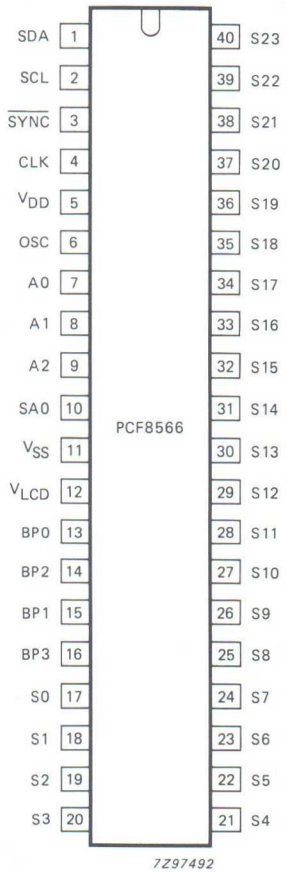


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17 to 40	S0 to S23	LCD segment outputs

LCD row driver for dot matrix displays

PCF8568

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

FEATURES

- Single chip LCD row driver with 16 outputs
- Low power consumption
- Selectable multiplex rate 1:8, 1:16, 1:24, 1:32
- Cascadable to 1:24 or 1:32 multiplex rates
- Internally generated intermediate LCD bias voltages
- LCD column bias voltages available at pins VO3 and VO4
- Minimizes display system power requirements
- On-chip oscillator, requires only one external resistor
- Power-on reset blanks display
- Logic voltage range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9.0 V
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring
- Available in 28-lead plastic DIL or space saving mini-pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- General instrumentation
- Consumer products.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range	+2.5	-	+6.0	V
V_{LCD}	LCD supply voltage range voltage	V_{DD} −9	-	V_{DD} −3.5	V
I_{DD2}	supply current with internal clock (R_{OSC} = 330 kΩ)	-	67	150	µA
T_{amb}	operating ambient temperature range	−40	-	+85	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8568P	28	DIL	plastic	SOT117
PCF8568T	28	SO28	plastic	SOT136A
PCF8568U/7	(28 pads)	die: bumped chip on tape	-	-

GENERAL DESCRIPTION

The PCF8568 is a low power LCD row driver, designed to drive dot matrix graphic displays with multiplex rates of 1:8 or 1:16. The device has 16 row outputs. Two devices may be cascaded to drive displays with multiplex rates of 1:24 or 1:32. The PCF8568 is optimised for use with the PCF8569 and PCF8579 LCD dot matrix column drivers. Intermediate LCD bias voltages are internally generated. LCD column bias voltages are available at pins VO3 and VO4 for connection to the column drivers. The PCF8568 is compatible with most microcontrollers and communicates via a two- line bidirectional bus (I²C).

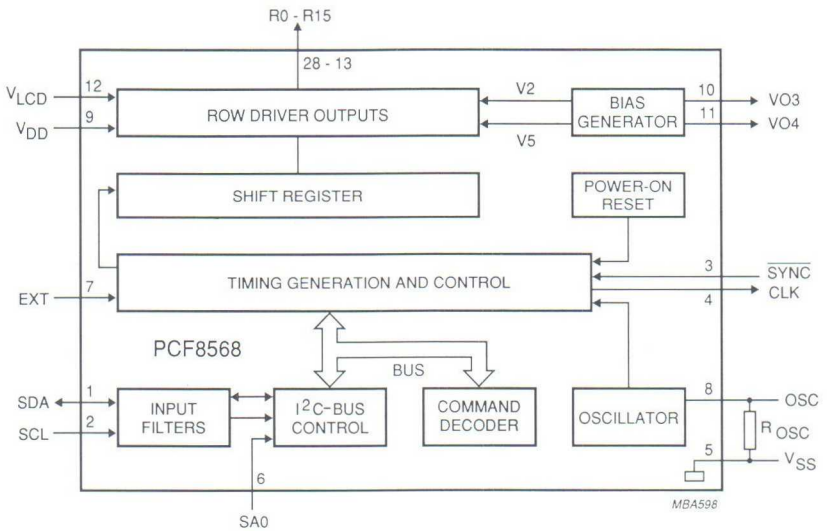


Fig.1 Block diagram.

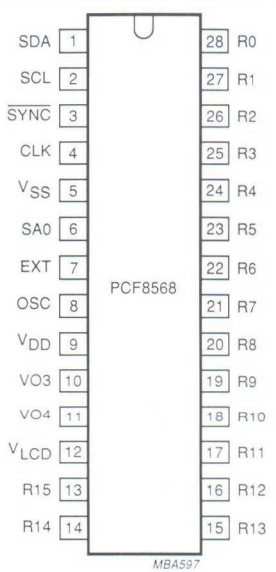


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus serial data line
SCL	2	I²C-bus serial clock line
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	clock output
V_{SS}	5	ground (logic)
SA0	6	I²C-bus slave address input (bit 0)
EXT	7	external clock select pin
OSC	8	oscillator or external clock input pin
V_{DD}	9	positive supply voltage
VO3	10	LCD bias voltage output (V3)
VO4	11	LCD bias voltage output (V4)
V_{LCD}	12	LCD supply voltage
R15 to R0	13 to 28	LCD row driver outputs

LCD row driver for dot matrix displays

PCF8568

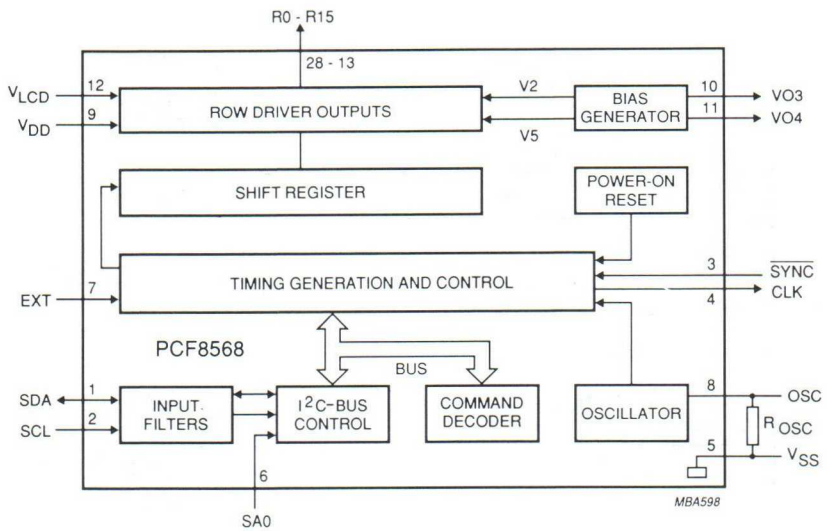


Fig.1 Block diagram.

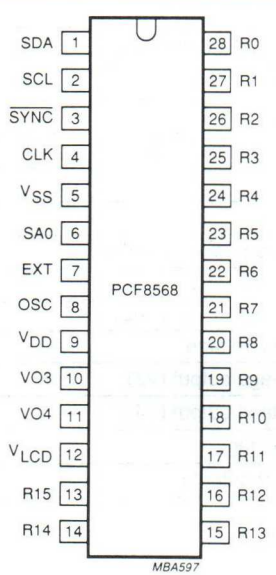


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus serial data line
SCL	2	I²C-bus serial clock line
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	clock output
V_{SS}	5	ground (logic)
SA0	6	I²C-bus slave address input (bit 0)
EXT	7	external clock select pin
OSC	8	oscillator or external clock input pin
V_{DD}	9	positive supply voltage
VO3	10	LCD bias voltage output (V3)
VO4	11	LCD bias voltage output (V4)
V_{LCD}	12	LCD supply voltage
R15 to R0	13 to 28	LCD row driver outputs

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8569 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8 or 1:16. The device has 40 outputs and can drive 16 x 40 dots in a 16 row multiplexed LCD. Up to 16 PCF8569s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8568/78/79 family of LCD row/column drivers. Together the PCF8568, PCF8578 and PCF8569 form a general LCD dot matrix driver chip set, capable of driving displays of up to 20 480 dots. The PCF8569 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

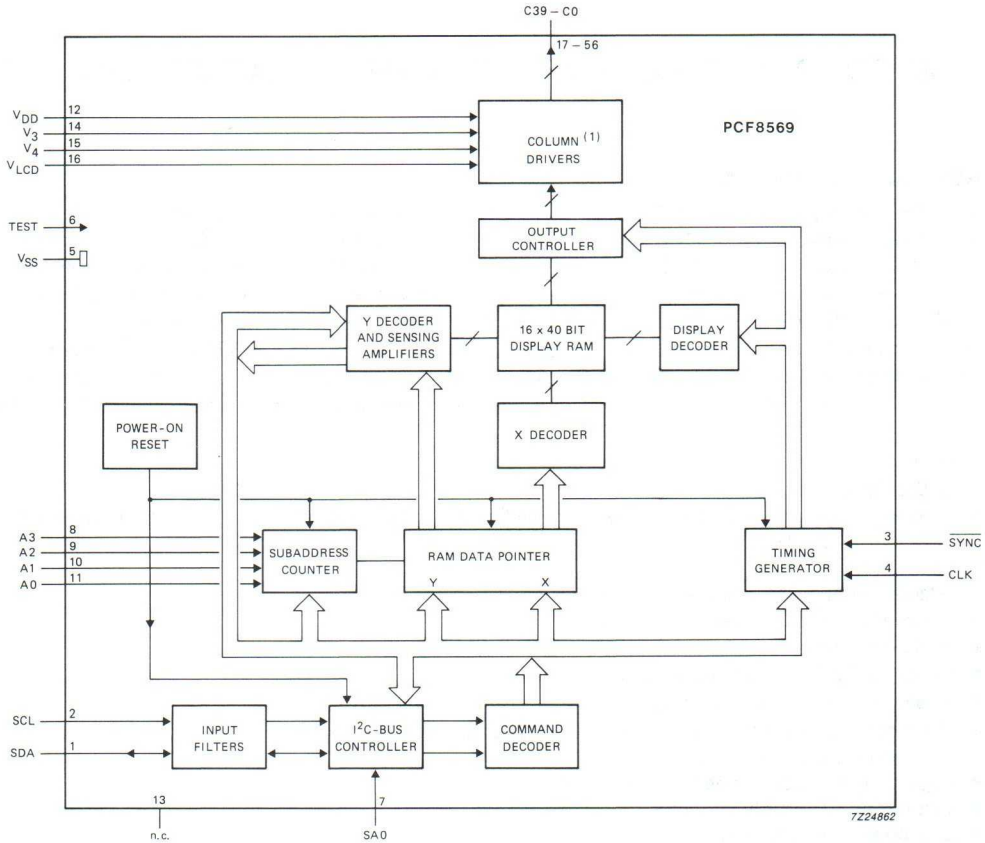
- LCD column driver
- Used in conjunction with the PCF8568 or PCF8578, this device forms part of a chip set capable of driving up to 20 480 dots.
- 40 column outputs
- Selectable multiplex rates; 1:8 or 1:16
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications
- 640-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack or 64-lead tab module

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8569T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8569V: 64-lead tape-automated-bonding (tab) module (SOT267).



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram (pin numbers shown for VSO56; SOT190).

PINNING

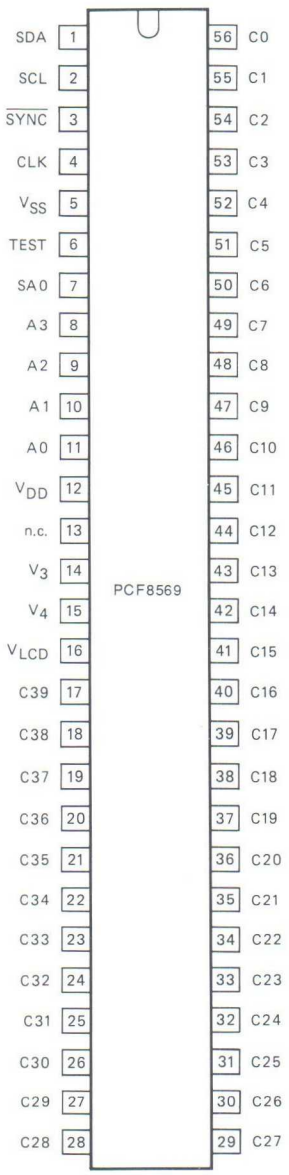
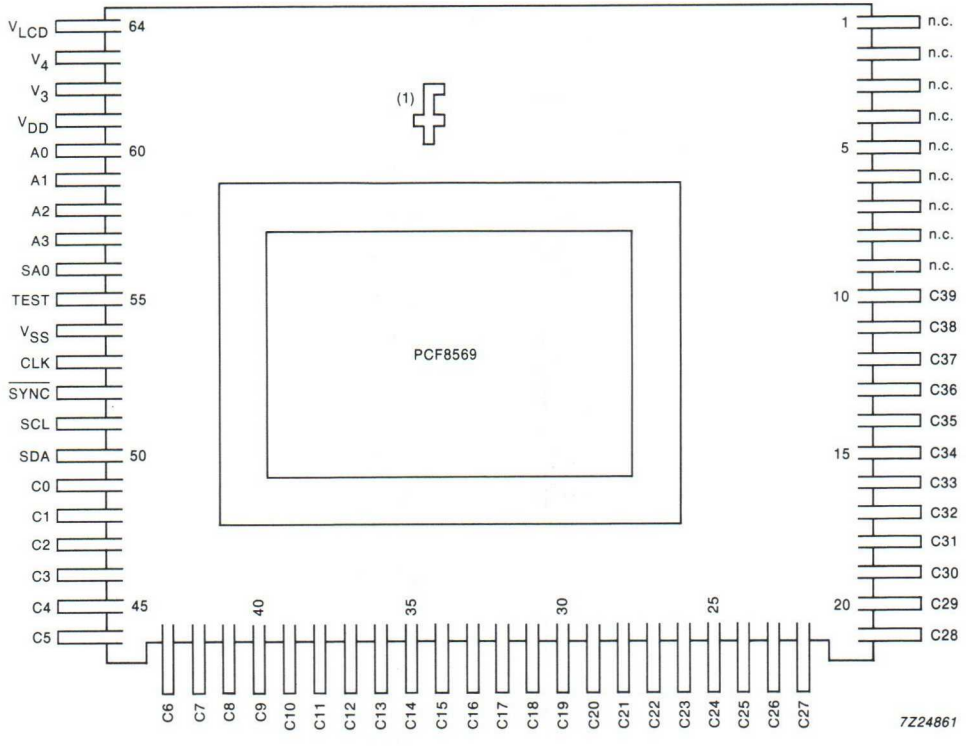


Fig.2 (a) Pinning diagram: VSO56; SOT190.

DEVELOPMENT DATA

PINNING (continued)



(1) Orientation mark.

Fig.2 (b) Pinning diagram: SOT267.

mnemonic	pin number		description
	SOT190	SOT267	
SDA	1	50	I^2C-bus serial data line
SCL	2	51	I^2C-bus serial clock line
$\overline{SYNC}$	3	52	cascade synchronization input
CLK	4	53	external clock input
V_{SS}	5	54	ground (logic)
TEST	6	55	test pin (connect to V_{SS})
SA0	7	56	I^2C-bus slave address input (bit 0)
A3 to A0	8 to 11	57 to 60	I^2C-bus subaddress inputs
V_{DD}	12	61	positive supply voltage
n.c.	13 *	1 - 9	not connected
V_3 to V_4	14 to 15	62 to 63	LCD bias voltage inputs
V_{LCD}	16	64	LCD supply voltage
C39 to C0	17 to 56	10 to 49	LCD column driver outputs

DEVELOPMENT DATA

* Do not connect, this pin is reserved.

256 × 8-bit static low-voltage RAM with I²C-bus interface

PCF8570

FEATURES

- Operating supply voltage 2.5 to 6.0 V
- Low data retention voltage; minimum 1.0 V
- Low standby current; maximum 15 μA
- Power saving mode; typical 50 nA
- Serial input/output bus (I²C-bus)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Available in DIP8 and SO8L packages.

APPLICATIONS

- Telephony:
  - RAM expansion for stored numbers in repertory dialling (e.g. PCD33XX applications)
- General purpose RAM for applications requiring extremely low current and low-voltage RAM retention (i.e. battery or capacitor backed)
- Radio, television and video cassette recorder:
  - channel presets
- General purpose:
  - RAM expansion for the microcontroller families PCD33XX, PCF84CXX, P80CLXXX and most other microcontrollers.

GENERAL DESCRIPTION

The PCF8570 is a low power static CMOS RAM.

The PCF8570 is organized as 256 words by 8-bits.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. Three address pins, A0, A1 and A2 are used to define the hardware address, allowing the use of up to 8 devices connected to the bus without additional hardware.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	6.0	
I_{DD}	supply current (standby)	f_{SCL} = 0 Hz	–	15	μA
I_{DDR}	supply current (power-saving mode)	T_{amb} = 25 °C	–	400	nA
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8570P	8	DIP8	plastic	SOT97-1
PCF8570T	8	SO8L	plastic	SOT176-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

BLOCK DIAGRAM

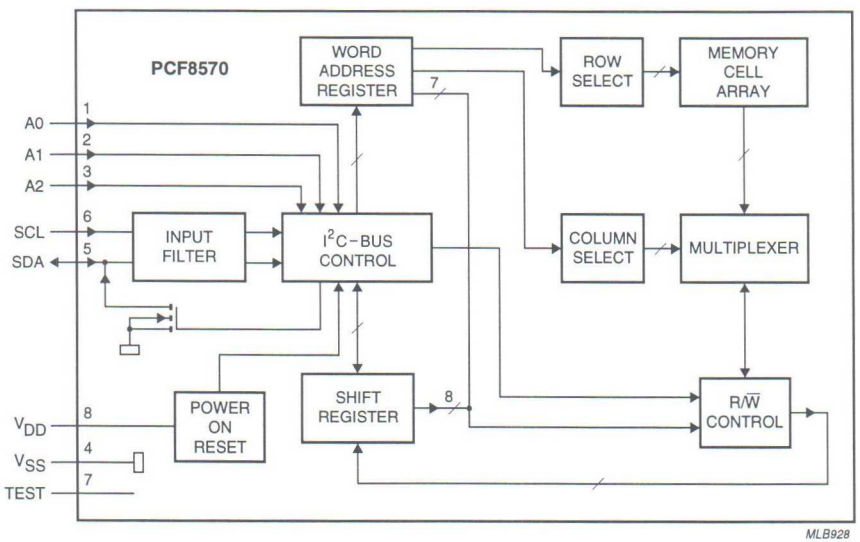


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	hardware address input 0
A1	2	hardware address input 1
A2	3	hardware address input 2
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
TEST	7	test output for test speed-up; must be connected to V_{SS} when not in use (power-saving mode)
V_{DD}	8	positive supply

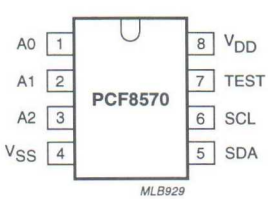


Fig.2 Pin configuration.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, CMOS circuit that functions as a real time clock/calendar with an I^2C-bus interface.
The IC incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred via a serial two-line bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1.2 V nickel cadium battery. The time base is generated from a 32.768 kHz crystal-controlled oscillator.

Features

- Serial input/output I^2C-bus interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32.768 kHz)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range					
clock (pin 16 to pin 15)	$V_{DD}-V_{SS1}$	1.1	–	6.0	V
I^2C interface (pin 16 to pin 8)	$V_{DD}-V_{SS2}$	2.5	–	6.0	V
Crystal oscillator frequency	f_{osc}	–	32.768	–	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT38).
PCF8573T: 16-lead mini-pack; plastic (SO16L; SOT162A).

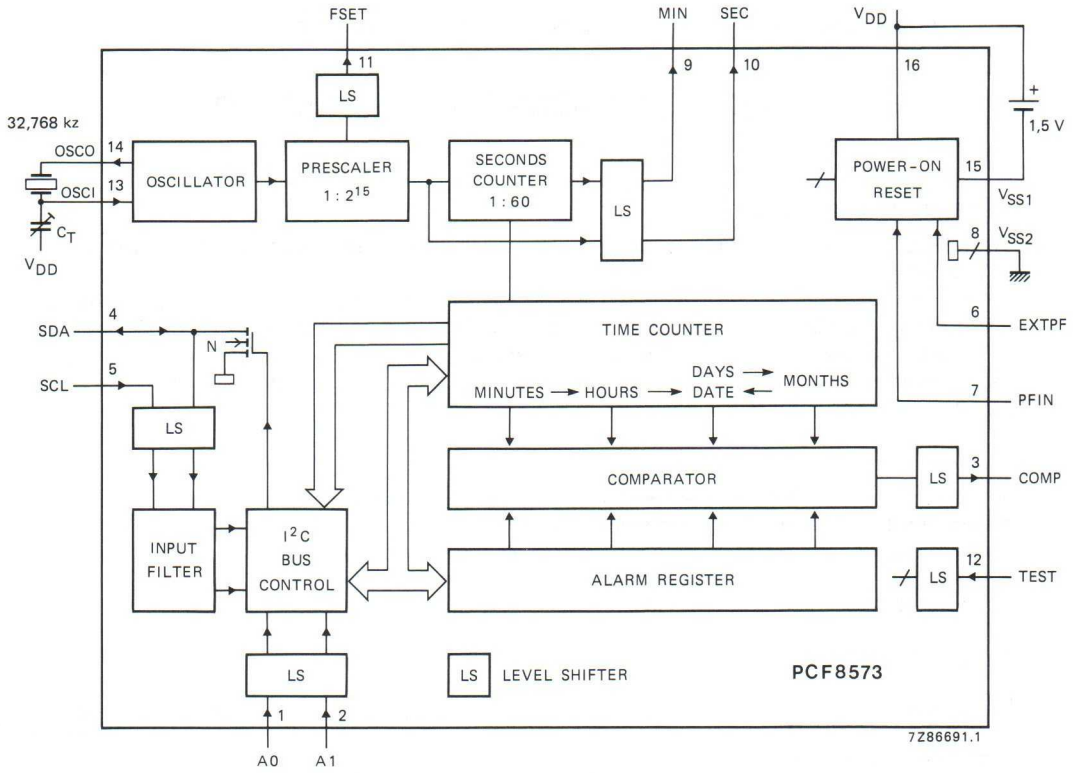


Fig.1 Block diagram.

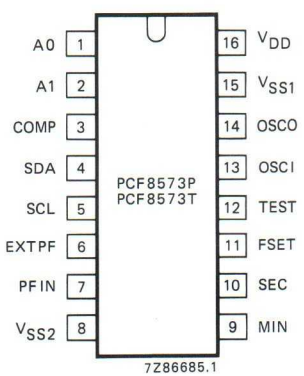


Fig.2 Pinning diagram.

PINNING

1	A0	address input	
2	A1	address input	
3	COMP	comparator output	
4	SDA	serial data line	I^2C-bus
5	SCL	serial clock line	I^2C-bus
6	EXTPF	enable power fail flag input	
7	PFIN	power fail flag input	
8	V_{SS2}	negative supply 2 (I^2C interface)	
9	MIN	one pulse per minute output	
10	SEC	one pulse per second output	
11	FSET	oscillator tuning output	
12	TEST	test input; must be connected to V_{SS2} when not in use	
13	OSCI	oscillator input	
14	OSCO	oscillator input/output	
15	V_{SS1}	negative supply 1 (clock)	
16	V_{DD}	common positive supply	

Remote 8-bit I/O expander for I²C-bus PCF8574

FEATURES

- Operating supply voltage 2.5 to 6 V
- Low standby current consumption of 10 μA maximum
- I²C to parallel port expander
- Open-drain interrupt output
- 8-bit remote I/O Port for the I²C-bus
- Compatible with most microcontrollers
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)
- DIP16, space-saving SO16 or SSOP20 package.

GENERAL DESCRIPTION

The PCF8574 is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I²C).

The device consists of an 8-bit quasi-bidirectional Port and an I²C interface. The PCF8574 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line ($\overline{INT}$) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and PCF8574A versions differ only in their slave address.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8574P; PCF8574AP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
PCF8574T; PCF8574AT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCF8574TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

BLOCK DIAGRAM

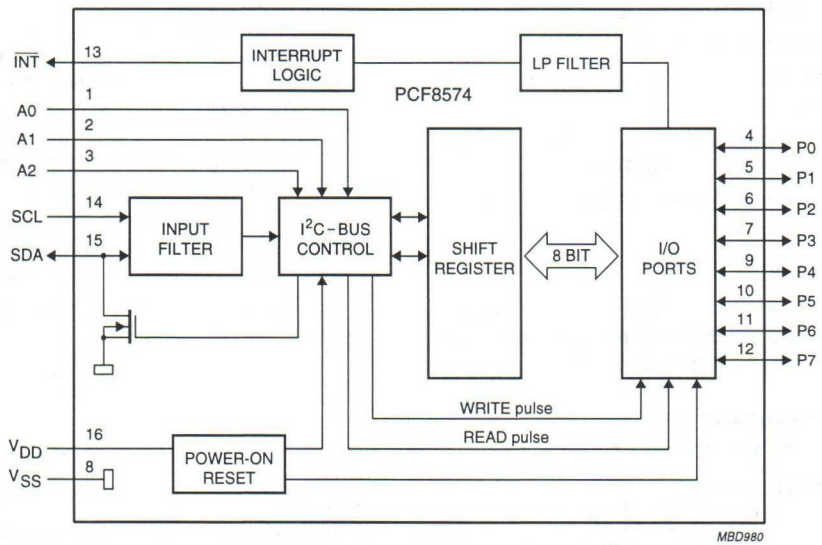


Fig.1 Block diagram (SOT38-1 and SOT162-1).

PINNING

SYMBOL	PIN		DESCRIPTION
	DIP16; SO16	SSOP20	
A0	1	6	address input 0
A1	2	7	address input 1
A2	3	9	address input 2
P0	4	10	quasi-bidirectional I/O Port 0
P1	5	11	quasi-bidirectional I/O Port 1
P2	6	12	quasi-bidirectional I/O Port 2
P3	7	14	quasi-bidirectional I/O Port 3
V_{SS}	8	15	supply ground
P4	9	16	quasi-bidirectional I/O Port 4
P5	10	17	quasi-bidirectional I/O Port 5
P6	11	19	quasi-bidirectional I/O Port 6
P7	12	20	quasi-bidirectional I/O Port 7
$\overline{INT}$	13	1	interrupt output (active LOW)
SCL	14	2	serial clock line
SDA	15	4	serial data line
V_{DD}	16	5	supply voltage
n.c.	–	3	not connected
n.c.	–	8	not connected
n.c.	–	13	not connected
n.c.	–	18	not connected

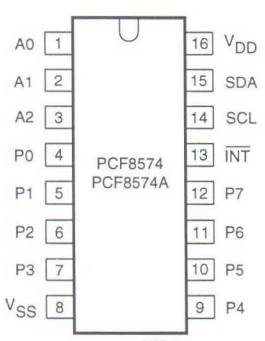


Fig.2 Pin configuration (DIP16; SO16).

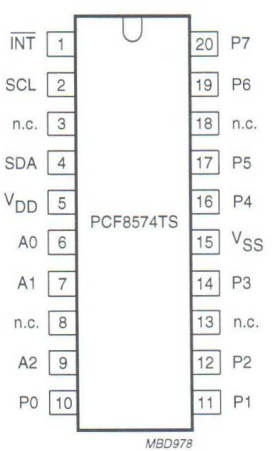


Fig.3 Pin configuration (SSOP20).

Universal LCD driver for low multiplex rates

PCF8576C

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 6 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with 24-segment LCD driver PCF8566
- Optimized pinning for plane wiring in both and multiple PCF8576C applications
- Space-saving 56-lead plastic very small outline package (VSO56) or 64-lead low profile quad flat package (LQFP64)
- Very low external component count (maximum of one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The PCF8576C is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576C is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8576CT	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8576CU	–	uncased chip in tray	–
PCF8576CU/10	FFC	chip-on-film frame carrier	–
PCF8576CH	LQFP64	plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm	SOT314-2

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

BLOCK DIAGRAM

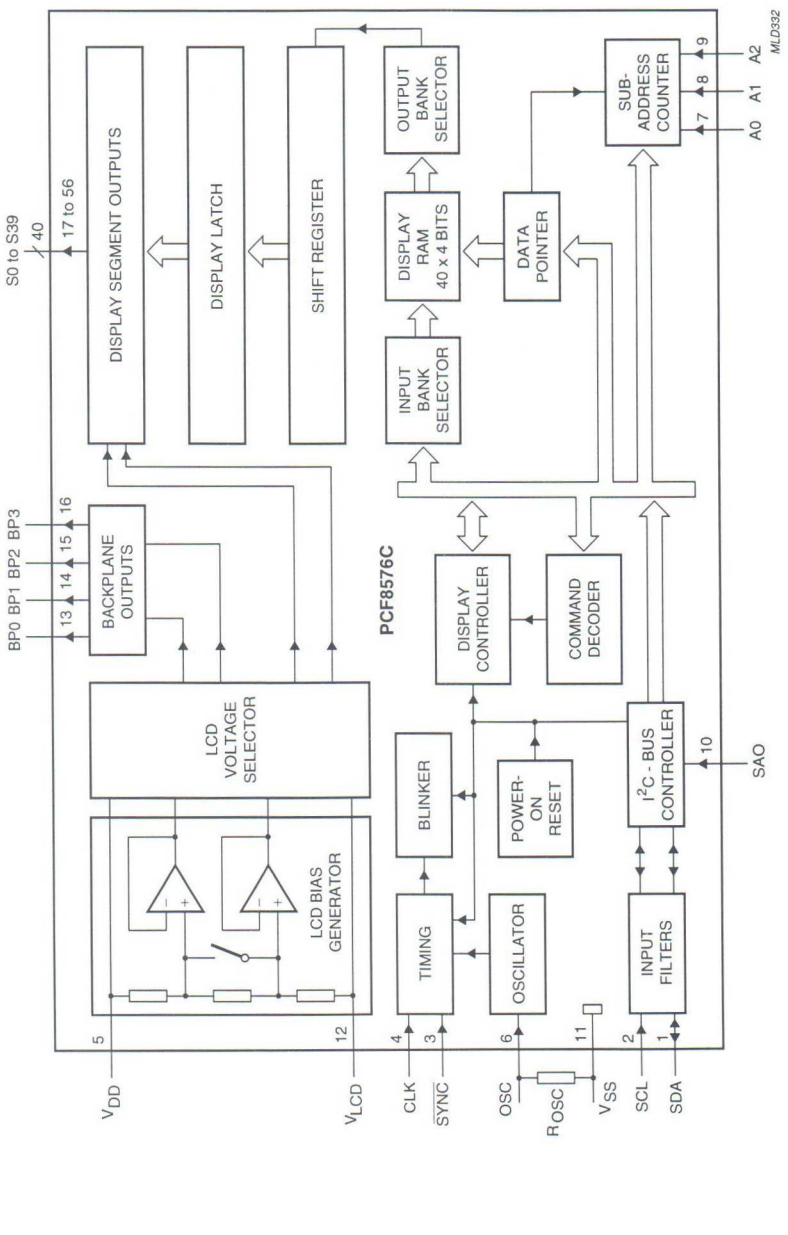


Fig.1 Block diagram; VSO56.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT190	SOT314	
SDA	1	10	I²C-bus serial data input/output
SCL	2	11	I²C-bus serial clock input
$\overline{SYNC}$	3	12	cascade synchronization input
CLK	4	13	external clock input
V_{DD}	5	14	supply voltage
OSC	6	15	oscillator input
A0 to A2	7 to 9	16 to 18	I²C-bus subaddress inputs
SA0	10	19	I²C-bus slave address input; bit 0
V_{SS}	11	20	logic ground
V_{LCD}	12	21	LCD supply voltage
BP0 to BP3	13 to 16	25 to 28	LCD backplane outputs
S0 to S39	17 to 56	29 to 32, 34 to 47, 49 to 64, 2 to 7	LCD segment outputs
n.c.	–	1, 8, 9, 22 to 24, 33 and 48	not connected

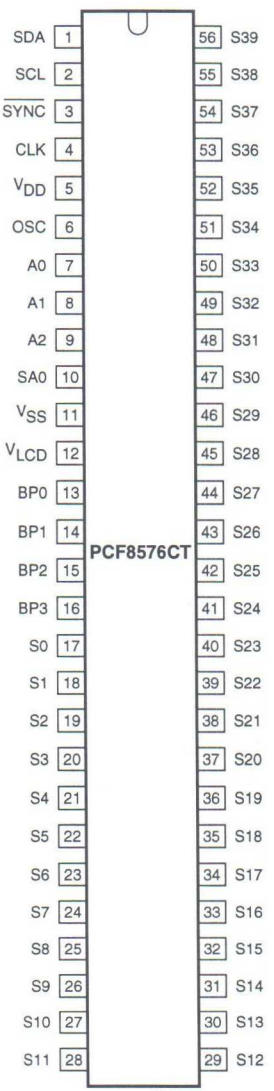


Fig.2 Pin configuration; VSO56.

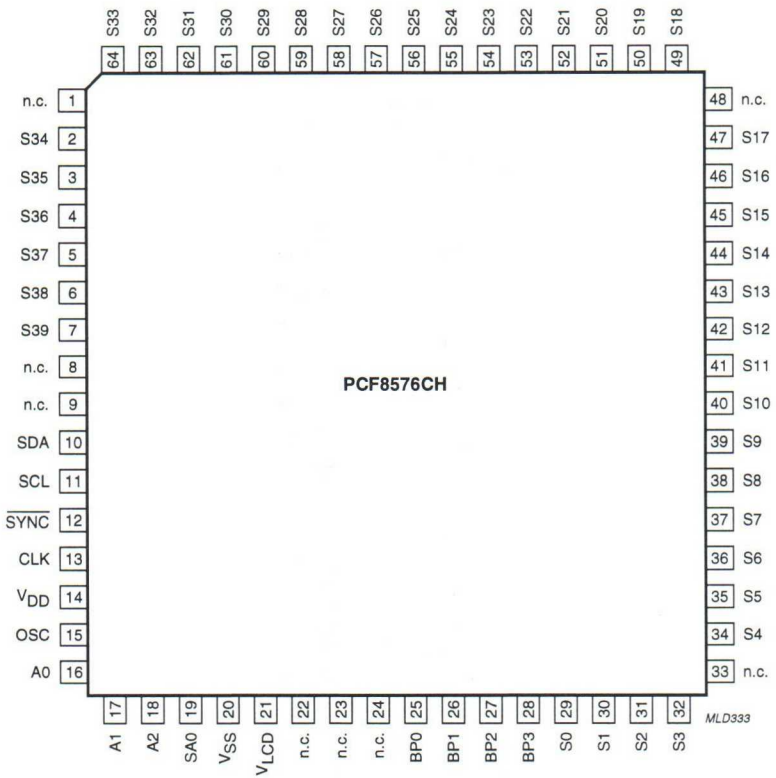


Fig.3 Pin configuration; LQFP64.

LCD direct/duplex driver with I²C-bus interface

PCF8577C

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

FEATURES

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments
- Power-on reset blanks display.

GENERAL DESCRIPTION

The PCF8577C is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware subaddressing and display memory switching (direct drive mode).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8577CP	40	DIL	plastic	SOT129
PCF8577CT	40	VSO40	plastic	SOT158A
PCF8577CT	–	in blister tape	–	–
PCF8577CU/5	–	wafer unsawn	–	–
PCF8577CU/10	–	chip on film-frame-carrier (FFC)	–	–

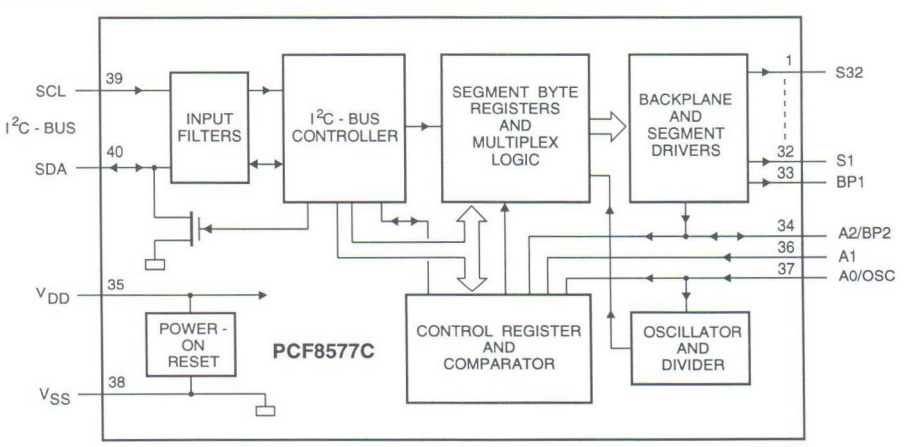


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
Supply		
V_{DD}	35	positive supply
V_{SS}	38	negative supply
I²C-bus		
SDA	40	I²C-bus data line
SCL	39	I²C-bus clock line
Inputs		
A1	36	hardware address line
A0/OSC	37	hardware address line/oscillator pin
Outputs		
S32 to S1	1 to 32	segments outputs
Input/Output		
A2/BP2	34	hardware address line/cascade sync input/backplane output
BP1	33	cascade sync input/backplane output

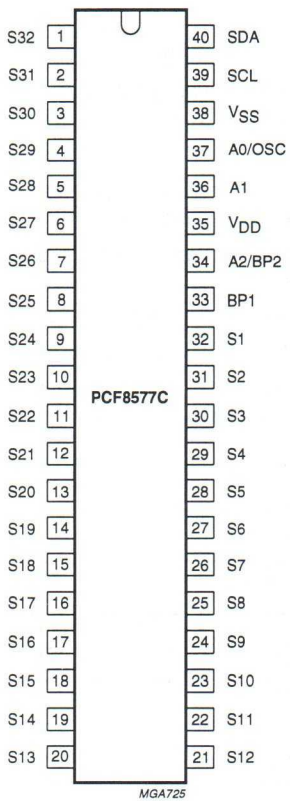


Fig.2 Pinning diagram.

LCD row/column driver for dot matrix graphic displays

PCF8578

FEATURES

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40960 dots possible)
- 40 driver outputs, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology.

GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs, of which 24 are programmable, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

APPLICATIONS

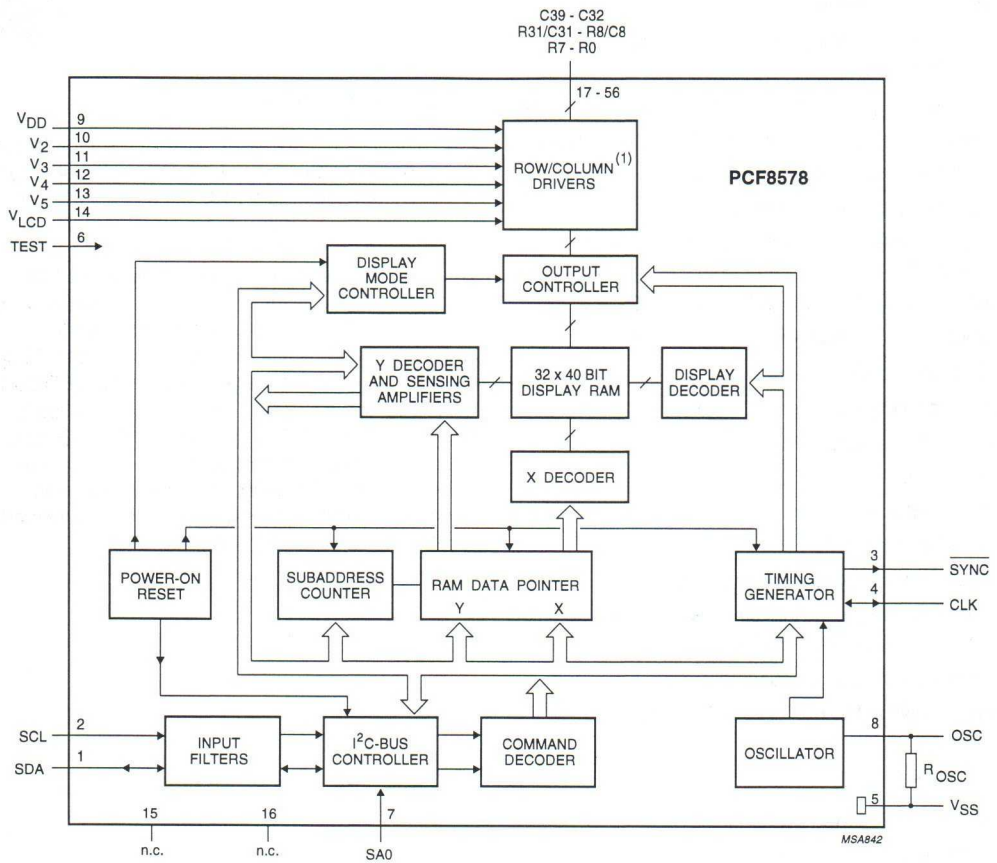
- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8578T	56	VSO56	plastic	SOT190
PCF8578U7	–	chip with bumps on-tape	–	–

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

BLOCK DIAGRAM



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus serial data line
SCL	2	I²C-bus serial clock line
$\overline{SYNC}$	3	cascade synchronization output
CLK	4	external clock input/output
V_{SS}	5	ground (logic)
TEST	6	test pin (connect to V_{SS})
SA0	7	I²C-bus slave address input (bit 0)
OSC	8	oscillator input
V_{DD}	9	positive supply voltage
V_2 to V_5	10 to 13	LCD bias voltage inputs
V_{LCD}	14	LCD supply voltage
n.c.	15, 16	not connected
C39 to C32	17 to 24	LCD column driver outputs
R31/C31 to R8/C8	25 to 48	LCD row/column driver outputs
R7 to R0	49 to 56	LCD row driver outputs

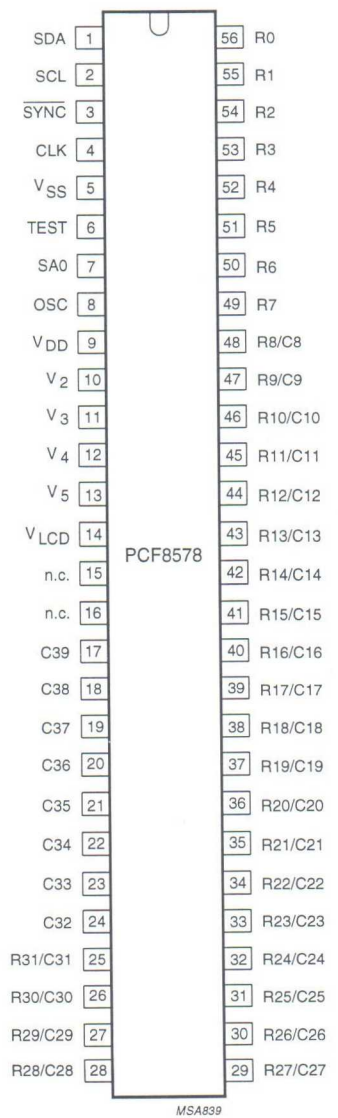


Fig.2 Pin configuration.

LCD column driver for dot matrix graphic displays

PCF8579

FEATURES

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40960 dots
- 40 column outputs
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8578)
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8578)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

GENERAL DESCRIPTION

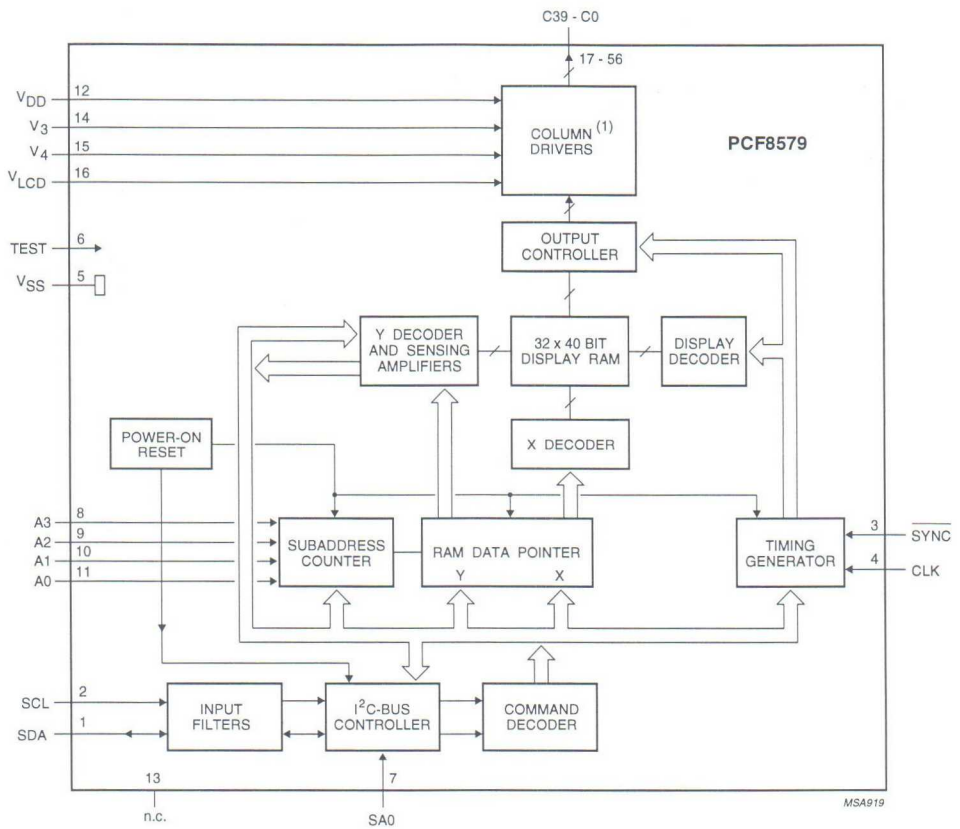
The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs and can drive 32 × 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I²C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8579T	56	VSO56	plastic	SOT190
PCF8579U7	–	chip with bumps on-tape	–	–

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

BLOCK DIAGRAM



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus serial data line
SCL	2	I²C-bus serial clock line
$\overline{SYNC}$	3	cascade synchronization input
CLK	4	external clock input
V_{SS}	5	ground (logic)
TEST	6	test pin (connect to V_{SS})
SA0	7	I²C-bus slave address input (bit 0)
A3 to A0	8 to 11	I²C-bus subaddress inputs
V_{DD}	12	supply voltage
n.c.	13(1)	not connected
V_3, V_4	14, 15	LCD bias voltage inputs
V_{LCD}	16	LCD supply voltage
C39 to C0	17 to 56	LCD column driver outputs

Note

1. Do not connect, this pin is reserved.

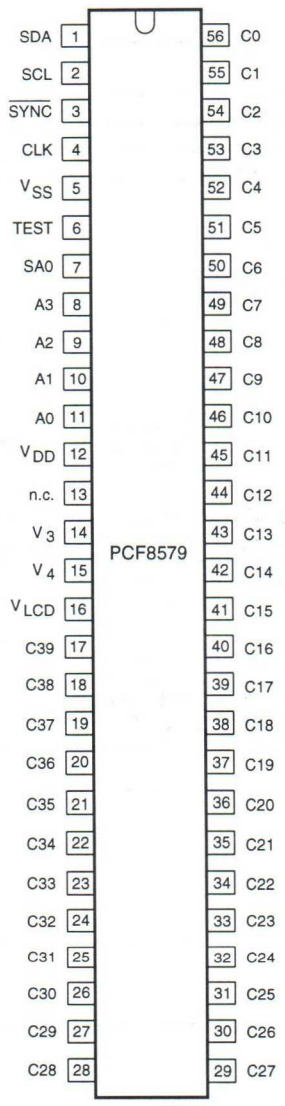


Fig.2 Pin configuration.

Clock Calendar with 256 x 8-bit Static RAM

PCF8583

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

FEATURES



- I²C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage (0 to +70 °C): 1.0 V to 6.0 V
- Data retention voltage: 1.0 V to 6 V
- Operating current (f_{scl} = 0 Hz): max. 50 A
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Slave address, READ: A1 or A3, WRITE: A0 or A2.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_{DD}	supply voltage operating range	I²C-bus active	2.5	6.0	V
V_{DD}	supply voltage operating range	I²C-bus inactive	1.0	6.0	V
I_{DD}	supply current operating mode	f_{scl} =100 kHz	-	200	µA
I_{DDO}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V f_{scl} = 0 Hz; V_{DD} = 1 V	- -	50 10	µA µA
T_{amb}	operating ambient temperature range		–40	+85	°C
T_{stg}	storage temperature range		–65	+150	°C

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8 bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8583P	8	DIL	plastic	SOT97
PCF8583T	8	mini-pack	plastic	SO8L; SOT176C

Clock Calendar with 256 x 8-bit Static RAM

PCF8583

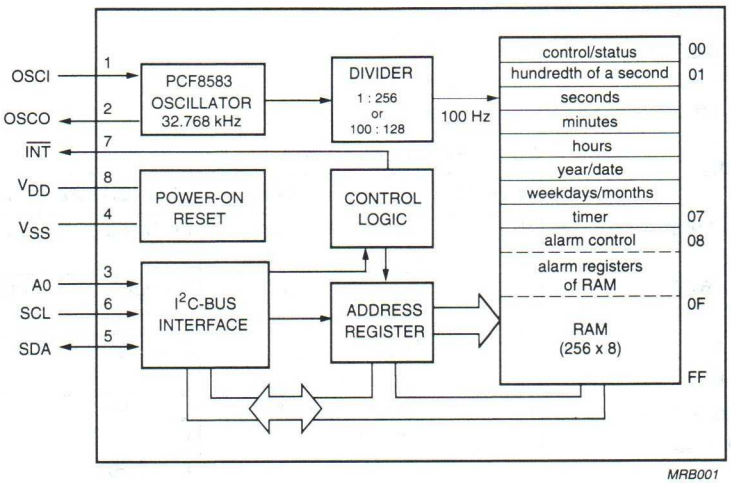


Fig.1 Block diagram.

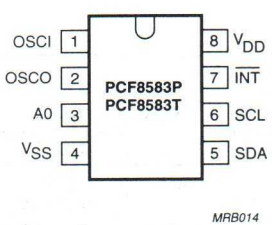


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
A0	3	address input
V_{SS}	4	negative supply
SDA	5	serial data line
SCL	6	serial clock line
$\overline{INT}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

I²C-bus controller PCF8584

FEATURES

- Parallel-bus to I²C-bus protocol converter and interface
- Compatible with most parallel-bus microcontrollers/microprocessors including 8049, 8051, 6800, 68000, and Z80
- Both master and slave functions
- Automatic detection and adaption to bus interface type
- Programmable interrupt vector
- Multi-master capability
- I²C-bus monitor mode
- Long-distance mode (4-wire)
- Operating supply voltage 4.5 to 5.5 V
- Operating temperature range: –40 to +85 °C.

GENERAL DESCRIPTION

The PCF8584 is an integrated circuit designed in CMOS technology which serves as an interface between most standard parallel-bus microcontrollers/microprocessors and the serial I²C-bus. The PCF8584 provides both master and slave functions.

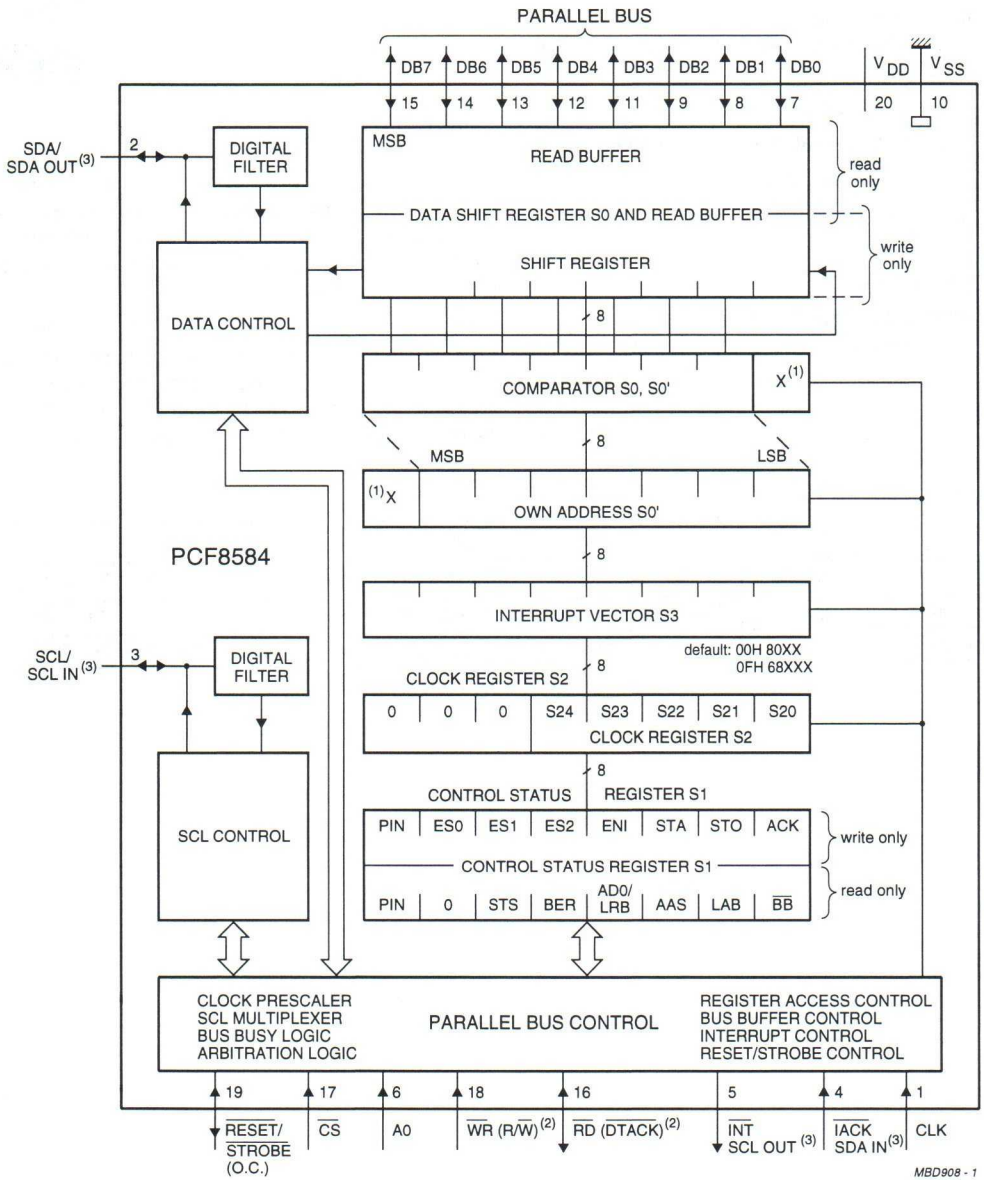
Communication with the I²C-bus is carried out on a byte-wise basis using interrupt or polled handshake. It controls all the I²C-bus specific sequences, protocol, arbitration and timing. The PCF8584 allows parallel-bus systems to communicate bidirectionally with the I²C-bus.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8584P	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
PCF8584T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

BLOCK DIAGRAM



(1) X = don't care.

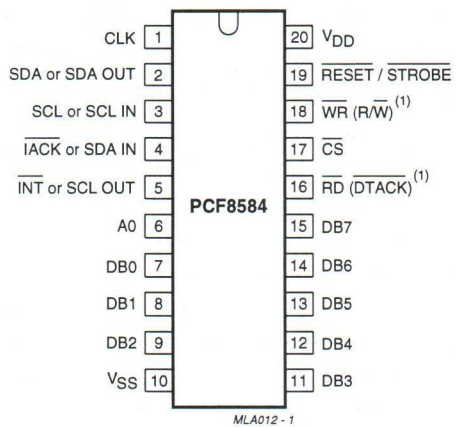
(2) Pin mnemonics between brackets indicate the 68000 mode pin designations.

(3) These pin mnemonics represent the long-distance mode pin designations.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
CLK	1	I	clock input from microcontroller clock generator (internal pull-up)
SDA or SDA OUT	2	I/O	I²C-bus serial data input/output (open-drain). Serial data output in long-distance mode.
SCL or SCL IN	3	I/O	I²C-serial clock input/output (open-drain). Serial clock input in long-distance mode.
$\overline{\text{IACK}}$ or SDA IN	4	I	interrupt acknowledge input (internal pull-up); when this signal is asserted the interrupt vector in register S3 will be available at the bus Port if the ENI flag is set. Serial data input in long-distance mode.
$\overline{\text{INT}}$ or SCL OUT	5	O	interrupt output (open-drain); this signal is enabled by the ENI flag in register S1. It is asserted when the PIN flag is reset. (PIN is reset after 1 bye is transmitted or received over the I²C-bus). Serial clock output in long-distance mode.
A0	6	I	register select input (internal pull-up); this input selects between the control/status register and the other registers. Logic 1 selects register S1, logic 0 selects one of the other registers depending on bits loaded in ES0, ES1, and ES2 of register S1.
DB0	7	I/O	bidirectional 8-bit bus Port 0
DB1	8	I/O	bidirectional 8-bit bus Port 1
DB2	9	I/O	bidirectional 8-bit bus Port 2
V_{SS}	10	–	ground
DB3	11	I/O	bidirectional 8-bit bus Port 3
DB4	12	I/O	bidirectional 8-bit bus Port 4
DB5	13	I/O	bidirectional 8-bit bus Port 5
DB6	14	I/O	bidirectional 8-bit bus Port 6
DB7	15	I/O	bidirectional 8-bit bus Port 7
$\overline{\text{RD}}$ ($\overline{\text{DTACK}}$)	16	I/O	$\overline{\text{RD}}$ is the read control input for MAB8049, MAB8051 or Z80-types. $\overline{\text{DTACK}}$ is the data transfer control output for 68000-types (open-drain).
$\overline{\text{CS}}$	17	I	chip select input (internal pull-up)
$\overline{\text{WR}}$ (R/$\overline{\text{W}}$)	18	I	$\overline{\text{WR}}$ is the write control input for MAB8048, MAB8051, or Z80-types (internal pull-up). R/$\overline{\text{W}}$ control input for 68000-types.
$\overline{\text{RESET}}$/ $\overline{\text{STROBE}}$	19	I/O	reset input (open-drain); this input forces the I²C-bus controller into a predefined state; all flags are reset, except PIN, which is set. Also functions as strobe output.
V_{DD}	20	–	supply voltage



(1) Pin mnemonics between brackets indicate the 68000 mode pin designations.

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The PCF8584 acts as an interface device between standard high-speed parallel buses and the serial I²C-bus. On the I²C-bus, it can act either as master or slave. Bidirectional data transfer between the I²C-bus and the parallel-bus microcontroller is carried out on a byte-wise basis, using either an interrupt or polled handshake. Interface to either 80XX-type (e.g. MAB8048, MAB8051, Z80) or 68000-type buses is possible. Selection of bus type is automatically performed.

Table 1 Control signals utilized by the PCF8584 for microcontroller/microprocessor interfacing

TYPE	R/$\overline{W}$	$\overline{WR}$	$\overline{R}$	$\overline{DTACK}$	$\overline{IACK}$
8048/ 8051	no	yes	yes	no	no
68000	yes	no	no	yes	yes
Z80	no	yes	yes	no	yes

The structure of the PCF8584 is similar to that of the I²C-bus interface section of the MABXXXX/PCF84(C)XX-series of microcontrollers, but with a modified control structure. The PCF8584 has five internal register locations. Three of these (own address register S0', clock register S2 and interrupt vector S3) are used for initialization of the PCF8584. Normally they are only written once directly after resetting of the PCF8584. The remaining two registers function as double registers (data buffer/shift register S0, and control/status register S1) which are used during actual data transmission/reception. By using these double registers, which are separately write and read accessible, overhead for register access is reduced. Register S0 is a combination of a shift register and data buffer. Register S0 performs all serial-to-parallel interfacing with the I²C-bus. Register S1 contains I²C-bus status information required for bus access and/or monitoring.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

Features

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT38).
PCF8591T:16-lead mini-pack; plastic (SO16L; SOT162A).

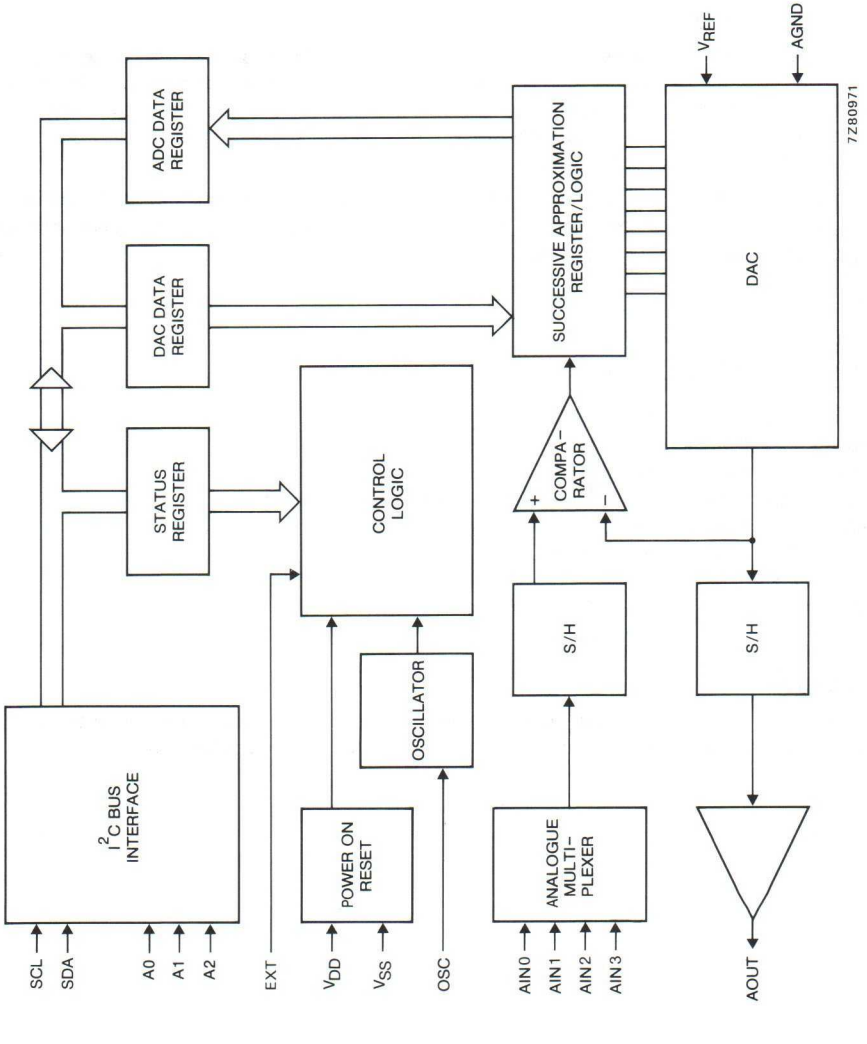


Fig. 1 Block diagram.

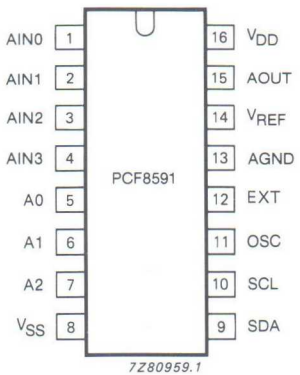


Fig. 2 Pinning diagram.

PINNING

1.	AIN0	analogue inputs (A/D converter)
2.	AIN1	
3.	AIN2	
4.	AIN3	
5.	A0	hardware address
6.	A1	
7.	A2	
8.	V_{SS}	negative supply voltage
9.	SDA	I^2C bus data input/output
10.	SCL	I^2C bus clock input/output
11.	OSC	oscillator input/output
12.	EXT	external/internal switch for oscillator input
13.	AGND	analogue ground
14.	V_{REF}	voltage reference input
15.	AOUT	analogue output (D/A converter)
16	V_{DD}	positive supply voltage

DEVELOPMENT DATA

Low power clock calendar PCF8593

FEATURES

- I²C-bus interface operating supply voltage: 2.5 to 6.0 V
- Clock operating supply voltage (T_{amb} = 0 to +70 °C): 1.0 to 6.0 V
- Data retention voltage: 1.0 to 6.0 V
- External $\overline{\text{RESET}}$ input pin
- Operating current (f_{scl} = 0 Hz, 32 kHz time base, V_{DD} = 2.0 V): typ. 1 µA
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C-bus)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Space-saving SO8 package
- Slave address:
  - READ A3H
  - WRITE A2H.

GENERAL DESCRIPTION

The PCF8593 is a CMOS Real-time clock/calendar optimized for low power consumption. Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. The built-in 32.768 kHz oscillator circuit and the first 8 registers are used for the clock/calendar and counter functions. The next 8 registers may be programmed as alarm registers or used as free RAM space.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage operating mode	I²C-bus active	2.5	6.0	V
		I²C-bus inactive	1.0	6.0	V
I_{DD}	supply current operating mode	f_{scl} = 100 kHz	–	200	µA
I_{DD}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V	4.0	15.0	µA
		f_{scl} = 0 Hz; V_{DD} = 2 V	1.0	8.0	µA
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8593P	8	DIL	plastic	SOT97-1
PCF8593T	8	SO8	plastic	SOT96-1

BLOCK DIAGRAM

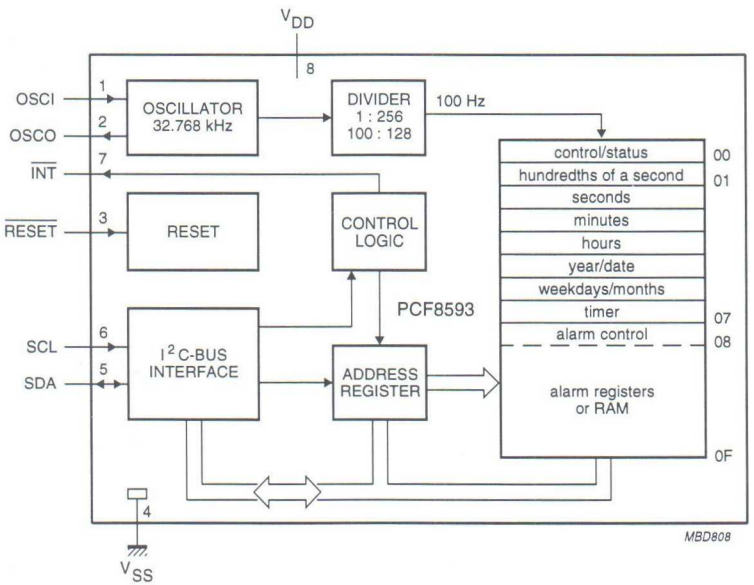


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
$\overline{\text{RESET}}$	3	reset input (active LOW)
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
$\overline{\text{INT}}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

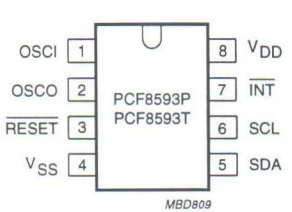


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The PCF8593 contains sixteen 8-bit registers with an 8-bit auto-incrementing address register, an on-chip 32.768 kHz oscillator circuit, a frequency divider and a serial two-line bidirectional I^2C-bus interface.

The first 8 registers (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F may be programmed as alarm registers or used as free RAM locations.

Counter function modes

When the control/status register is programmed, a 32.768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and week day are stored in a BCD format. The timer register stores up to 99 days. The event counter mode is used to count pulses applied to the oscillator input (OSCO left open-circuit). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore, faulty reading of the count during a carry condition is prevented.

When a counter is written, other counters are not affected.

Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a week day alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open-drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled). The flags remain set until directly reset by a write operation.

When a timer function without any function is programmed the remaining alarm registers (addresses 09 to 0F) may be used as free RAM space.

Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I^2C-bus. All functions and options are controlled by the contents of the control/status register (see Fig.3).

Counter registers

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig.5.

The year and date are packed into memory location 05 (see Fig 6). The weekdays and months are packed into memory location 06 (see Fig.7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

In the different modes the counter registers are programmed and arranged as shown in Fig.4. Counter cycles are listed in Table 1.

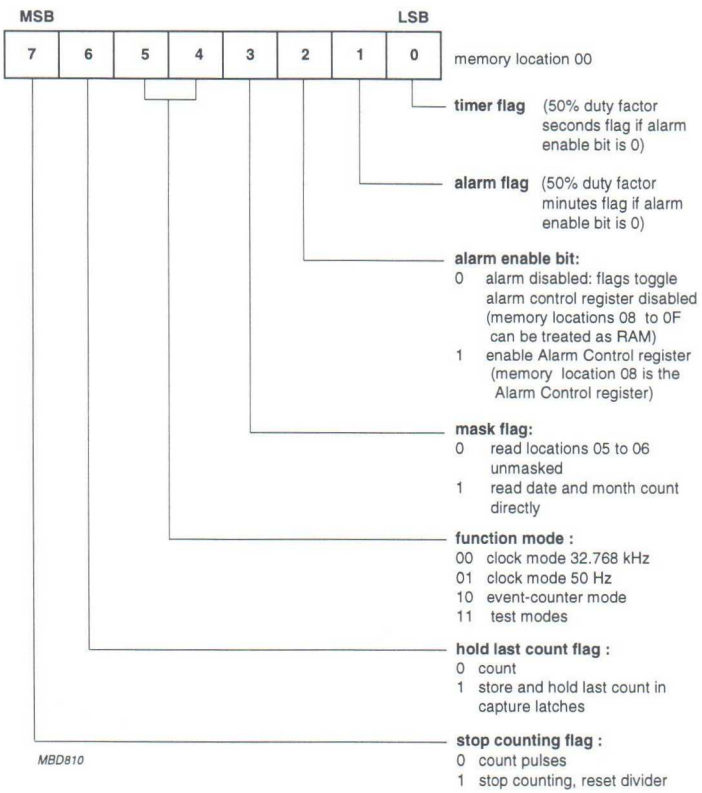


Fig.3 Control/status register.

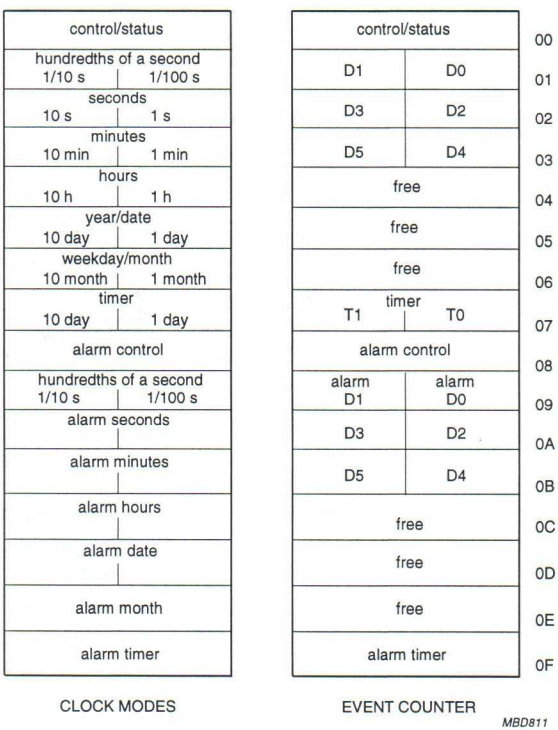


Fig.4 Register arrangement.

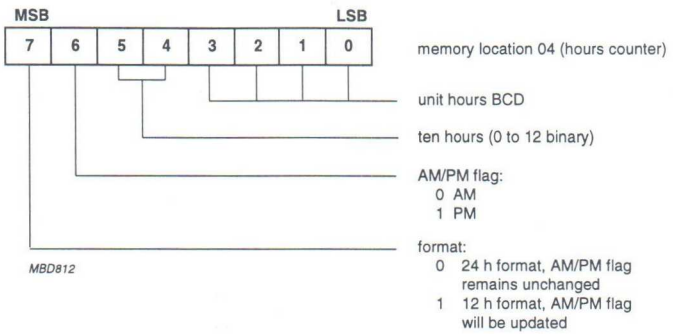


Fig.5 Format of the hours counter.

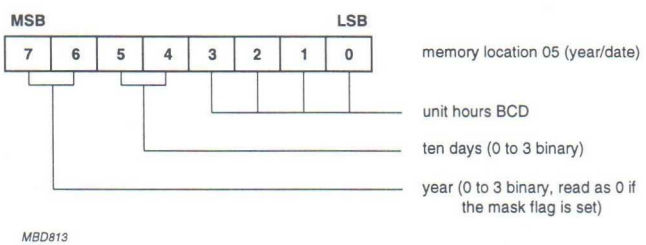


Fig.6 Format of the year/date counter.

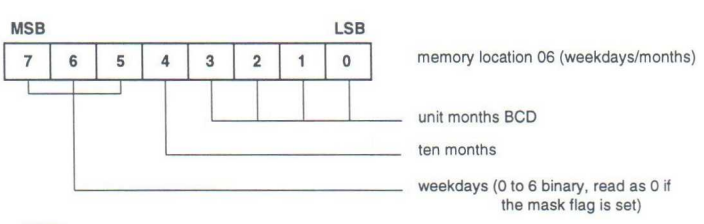


Fig.7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes.

UNIT	COUNTING CYCLE	CARRY TO NEXT UNIT	CONTENTS OF THE MONTH COUNTER
Hundredths of a second	00 to 99	99 to 00	–
Seconds	00 to 59	59 to 00	–
Minutes	00 to 59	59 to 00	–
Hours (24 h)	00 to 23	23 to 00	–
Hours (12 h)	12 AM	–	–
	01 AM to 11 AM	–	–
	12 PM	–	–
	01 PM to 11 PM	11 PM to 12 AM	–
Date	01 to 31	31 to 01	1, 3, 5, 7, 8, 10 and 12
	01 to 30	30 to 01	4, 6, 9 and 11
	01 to 29	29 to 01	2, year = 0
	01 to 28	28 to 01	2, year = 1, 2 and 3
Months	01 to 12	12 to 01	–
Year	0 to 3	–	–
Weekdays	0 to 6	6 to 0	–
Timer	00 to 99	no carry	–

Alarm control register

When the alarm enable bit of the control/status register is set (address 00, bit 2) the alarm control register (address 08) is activated. All alarm, timer, and interrupt output functions are controlled by the contents of the alarm control register (see Fig.8).

Alarm registers

All alarm registers are allocated with a constant address offset of hexadecimal 08 to the corresponding counter registers (see Fig.4; Register arrangement).

An alarm signal is generated when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig.9).

Remark: in the 12 h mode, bits 6 and 7 of the alarm hours register must be the same as the hours counter.

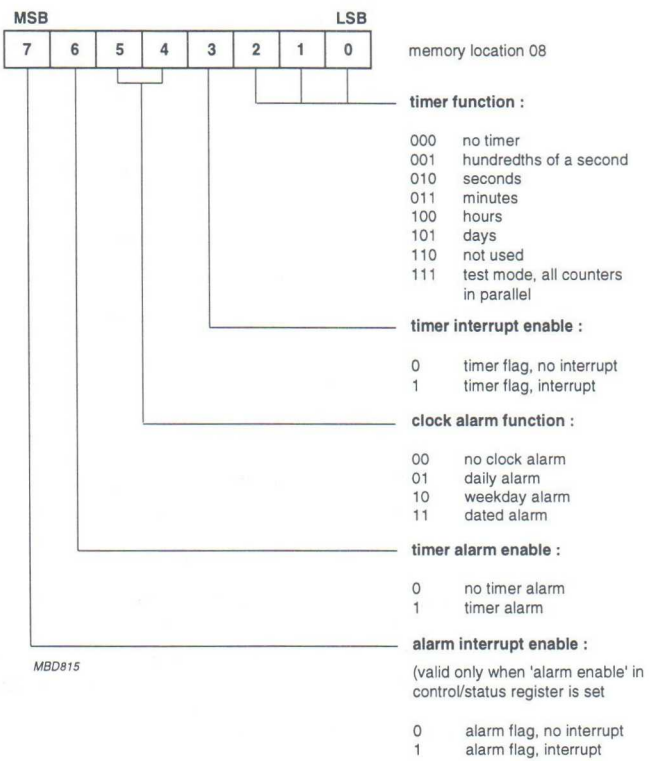


Fig.8 Alarm control register; clock mode.

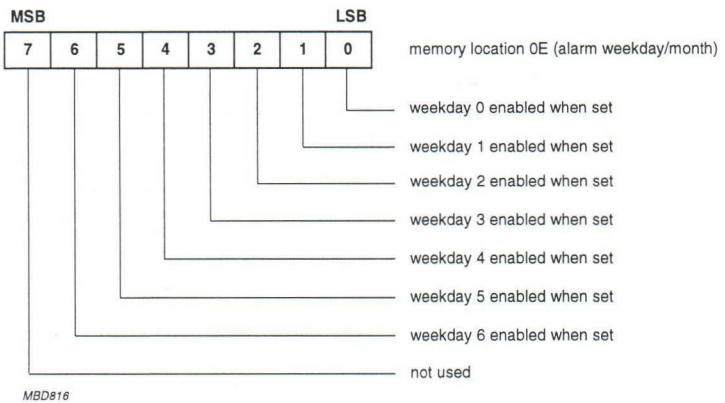


Fig.9 Selection of alarm weekdays.

Timer

The timer (location 07) is enabled by setting the control/status register = XX0X X1XX. The timer counts up from 0 (or a programmed value) to 99. On overflow, the timer resets to 0. The timer flag (LSB of control/status register) is set on overflow of the timer. This flag must be reset by software. The inverted value of this flag can be transferred to the external interrupt by setting bit 3 of the alarm control register.

Additionally, a timer alarm can be programmed by setting the timer alarm enable (bit 6 of the alarm control register). When the value of the timer equals a pre-programmed value in the alarm timer register (location 0F), the alarm flag is set (bit 1 of the control/status register). The inverted value of the alarm flag can be transferred to the external interrupt by enabling the alarm interrupt (bit 6 of the alarm control register).

Resolution of the timer is programmed via the 3 LSBs of the alarm control register (see Fig.11; Alarm and timer Interrupt logic diagram).

Event counter mode

Event counter mode is selected by bits 4 and 5 which are logic 1, 0 in the control/status register. The event counter mode is used to count pulses externally applied to the oscillator input (OSCO left open-circuit). The event counter stores up to 6 digits of data, which are stored as 6 hexadecimal values located in locations 1, 2, and 3. Thus, up to 1 million events may be recorded.

An event counter alarm occurs when the event counter registers match the value programmed in locations 9, A, and B, and the event alarm is enabled (bits 4 and 5 which are logic 0, 1 in the alarm control register). In this event, the alarm flag (bit 1 of the control/status register) is set. The inverted value of this flag can be transferred to the interrupt pin (pin 7) by setting the alarm interrupt enable in the alarm control register. In this mode, the timer (location 07) increments once for every one, one-hundred, ten thousand, or 1 million events, depending on the value programmed in bits 0,1 and 2 of the alarm control register. In all other events, the timer functions are as in the clock mode.

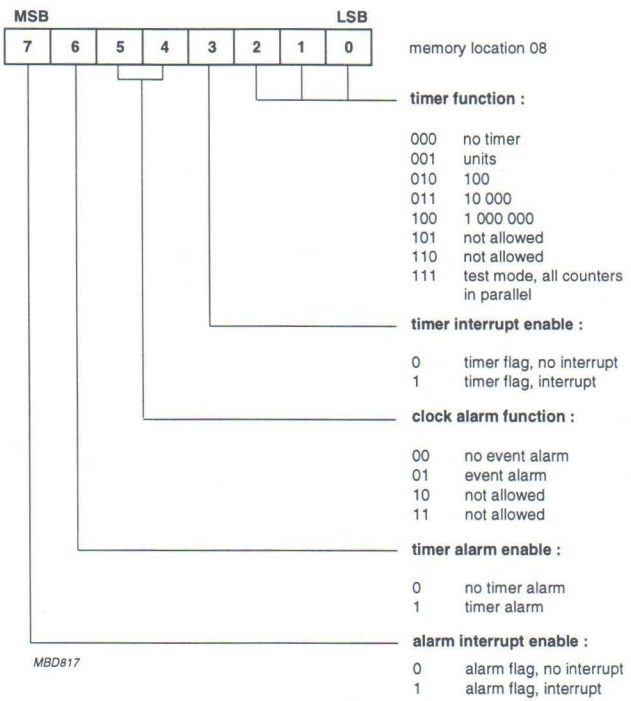
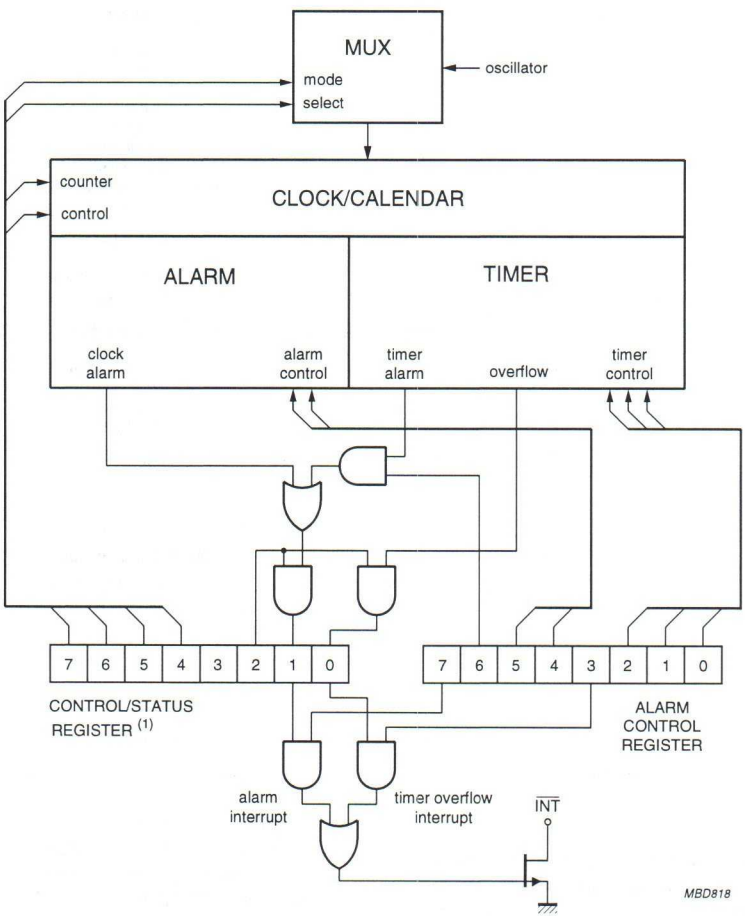


Fig.10 Alarm control register; event-counter mode.

Interrupt output

The conditions for activating the open-drain n-channel interrupt output $\overline{INT}$ (active LOW) are determined by appropriate programming of the alarm control register. These conditions are clock alarm, timer alarm, timer overflow, and event counter alarm. An interrupt occurs when the alarm flag or the timer flag is set, and the corresponding interrupt is enabled. In all events, the interrupt is cleared only by software resetting of the flag which initiated the interrupt.

In the clock mode, if the alarm enable is not activated (alarm enable bit of control/status register is logic 0), the interrupt output toggles at 1 Hz with a 50% duty cycle (may be used for calibration). The OFF voltage of the interrupt output may exceed the supply voltage, up to a maximum of 6.0 V. A logic diagram of the interrupt output is shown in Fig.11.



(1) If the alarm enable bit of the control/status register is reset (logic 0), a 1 Hz signal can be observed on the interrupt pin $\overline{INT}$.

Fig.11 Alarm and timer interrupt logic diagram.

Oscillator and divider

A 32.768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator (see Chapter "Application information" ; Section "Quartz frequency adjustment"). A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high-impedance state. This allows the user to feed the 50 Hz reference frequency or an external high-speed event signal into the input OSCI.

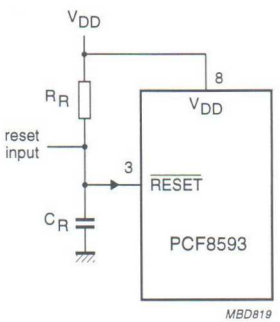
DESIGNING

When designing the printed-circuit board layout, keep the oscillator components as close to the IC package as possible, and keep all other signal lines as far away as possible. In applications involving tight packing of components, shielding of the oscillator may be necessary. AC coupling of extraneous signals can introduce oscillator inaccuracy.

Initialization (see Fig.12)

Note that immediately following power-on, all internal registers are undefined and, following a $\overline{\text{RESET}}$ pulse on pin 3, must be defined via software. Attention should be paid to the possibility that the device may be initially in event-counter mode, in which event the oscillator will not operate. Over-ride can be achieved via software.

Reset is accomplished by applying an external $\overline{\text{RESET}}$ pulse (active LOW) at pin 3. When reset occurs the I^2C-bus interface is reset. The control/status register and all clock counters are not affected by $\overline{\text{RESET}}$. $\overline{\text{RESET}}$ must return HIGH during device operation.



To avoid overload of the internal diode by falling V_{DD}, an external diode should be added in parallel to R_R if $C_R \geq 0.2\ \mu F$. Note that RC must be evaluated with the actual V_{DD} of the application, as their value will be V_{DD} rise-time dependent.

Fig.12 RC reset.

An RC combination can also be utilized to provide a power-on $\overline{\text{RESET}}$ signal at pin 3. In this event, the values of the RC must fulfil the following relationship to guarantee power-on reset (see Fig.12).

$\overline{\text{RESET}}$ input must be $\leq 0.3V_{DD}$ when V_{DD} reaches V_{DDmin} (or higher).

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states may lead to a temporary clock malfunction.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

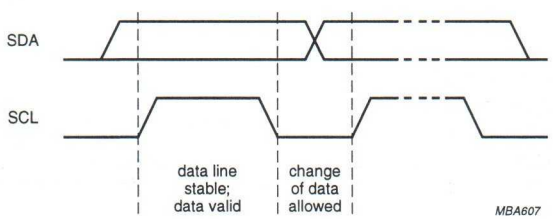


Fig.13 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

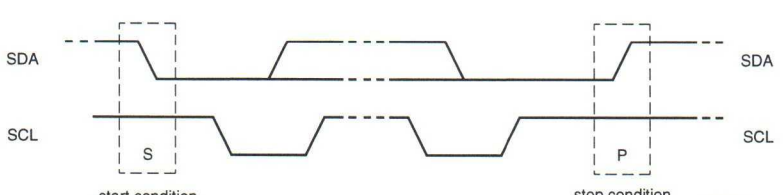


Fig.14 Definition of start and stop conditions.

System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

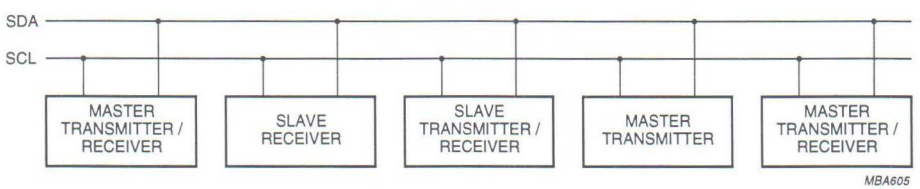


Fig.15 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

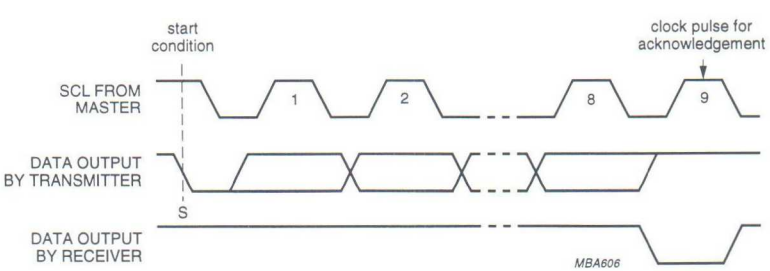


Fig.16 Acknowledgement on the I^2C-bus.

I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF8593 READ and WRITE cycles is shown in Figs 17, 18 and 19.

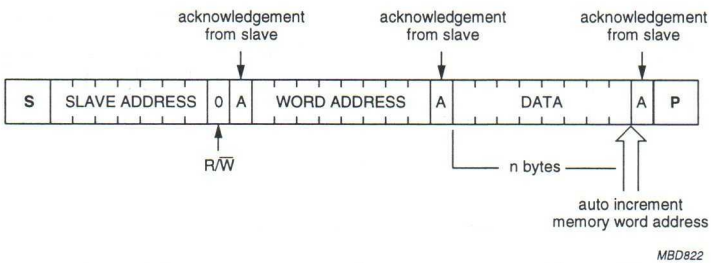


Fig.17 Master transmits to slave receiver (WRITE) mode.

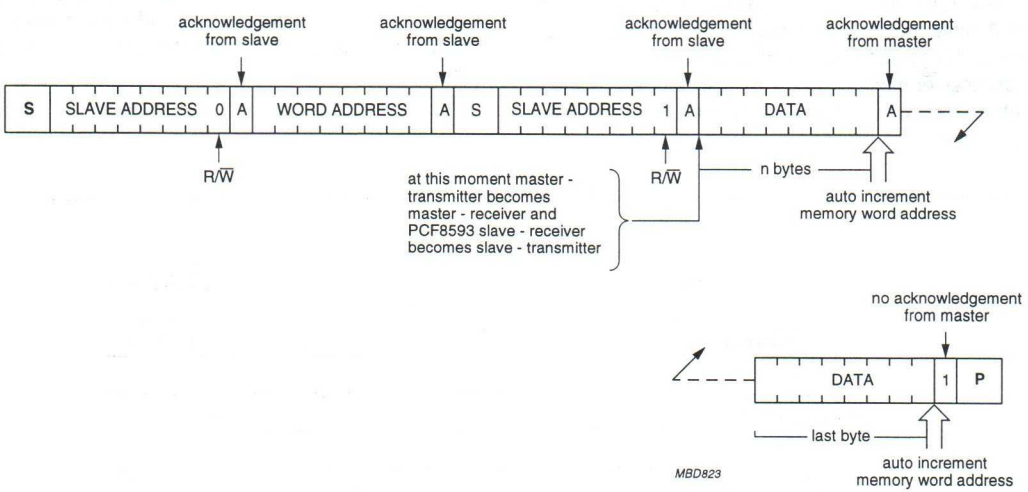


Fig.18 Master reads after setting word address (write word address; READ data).

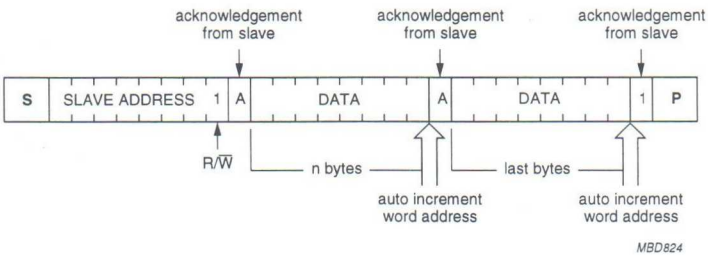


Fig.19 Master reads slave immediately after first byte (READ mode).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 8)	−0.8	+7.0	V
I_{DD}	supply current (pin 8)	–	50	mA
I_{SS}	supply current (pin 4)	–	50	mA
V_I	input voltage	−0.8	V_{DD} + 0.8	V
I_I	DC input current	–	10	mA
I_O	DC output current	–	10	mA
P_{tot}	total power dissipation per package	–	300	mW
P_O	power dissipation per output	–	50	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

DC CHARACTERISTICS

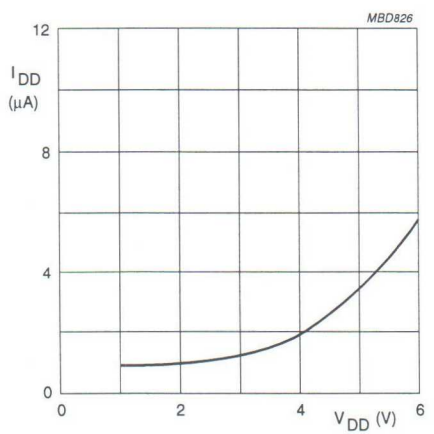
V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; f_{osc} = 32 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
Supply						
V_{DD}	supply voltage operating mode	I²C-bus active	2.5	–	6.0	V
		I²C-bus inactive	1.0	–	6.0	V
V_{DDosc}	quartz oscillator supply voltage	T_{amb} = 0 to 70 °C; note 2	1.0	–	6.0	V
		T_{amb} = −40 to 85 °C; note 2	1.2	–	6.0	V
I_{DD}	supply current operating mode	f_{scl} = 100 kHz; clock mode; note 3	–	–	200	µA
I_{DD}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 2 V; inputs at V_{DD} or V_{SS}	–	1.0	8.0	µA
		f_{scl} = 0 Hz; V_{DD} = 5 V; inputs at V_{DD} or V_{SS}	–	4.0	15	µA
SDA, SCL, $\overline{INT}$ and RESET						
V_{IL}	LOW level input voltage		0	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD}	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	–	–	mA
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	−1	–	+1	µA
C_I	input capacitance	note 4	–	–	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
OSCI and $\overline{\text{RESET}}$						
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−250	–	+250	nA
$\overline{\text{INT}}$						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1	–	–	mA
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA
SCL						
C_I	input capacitance	note 4	–	–	7	pF
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA

Notes

1. Typical values measured at 25 °C.
2. When powering up the device, V_{DD} must exceed the specified minimum value by 300 mV to guarantee correct start-up of the oscillator.
3. Event counter mode; supply current dependent upon input frequency.
4. Tested on sample basis.



f_{SCL} = 32 kHz; T_{amb} = 25 °C.

Fig.20 Typical supply current in clock mode as a function of supply voltage.

AC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
C_{osc}	integrated oscillator capacitance		20	25	30	pF
Δf_{osc}	oscillator stability	for ΔV_{DD} = 100 mV; T_{amb} = 25 °C; V_{DD} = 1.5 V	–	2×10^{-7}	–	
f_i	input frequency	note 1	–	–	1	MHz
Quartz crystal parameters (f = 32.768 kHz)						
R_s	series resistance		–	–	40	kΩ
C_L	parallel load capacitance		–	10	–	pF
C_T	trimmer capacitance		5	–	25	pF
I²C-bus timing (see Fig.21; notes 2 and 3)						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SP}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	start condition set-up time		4.7	–	–	µs
$t_{HD;STA}$	start condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1.0	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid		–	–	3.4	µs
$t_{SU;STO}$	stop condition set-up time		4.0	–	–	µs

Notes

1. Event counter mode only.
2. All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
3. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

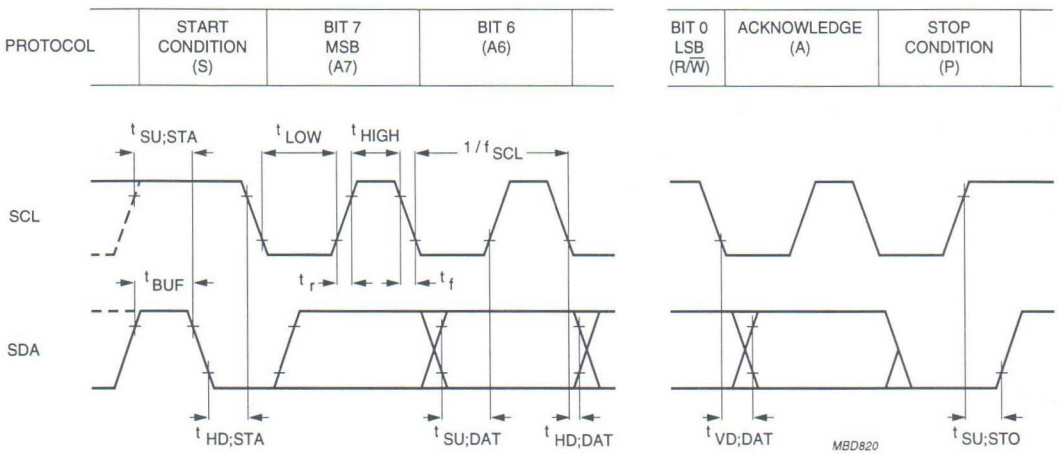


Fig.21 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

APPLICATION INFORMATION

Quartz frequency adjustment

METHOD 1: FIXED OSCI CAPACITOR

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 1 Hz signal which can be programmed to occur at the interrupt output (pin 7). The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$). Average deviations of ±5 minutes per year can be achieved.

METHOD 2: OSCI TRIMMER

Using the alarm function (via the I²C-bus) a signal faster than 1 Hz can be generated at the interrupt output for fast setting of a trimmer.

Procedure:

- Power-on
- Apply $\overline{\text{RESET}}$
- Initialization (alarm functions).

Routine:

- Set clock to time T and set alarm to time T + ΔT
- At time T + ΔT (interrupt) repeat routine.

METHOD 3: DIRECT OUTPUT

Direct measurement of oscillator output (accounting for test probe capacitance).

Slave address

The PCF8593 has an internally fixed I²C-bus slave address.

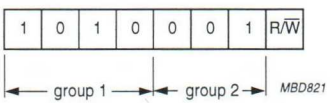
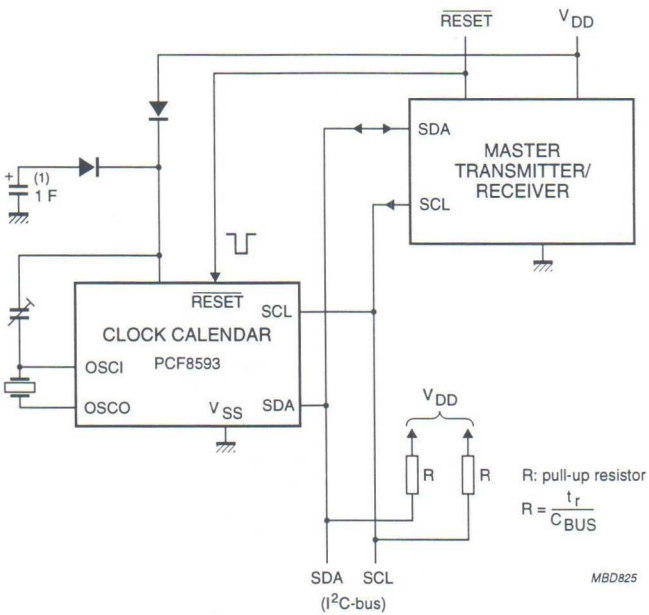


Fig.22 Slave address.



(1) Example Philips DLC 196 Double-Layer Capacitor family.

Fig.23 Application diagram.

256 × 8-bit CMOS EEPROMS with I²C-bus interface

PCX8582X-2 Family

FEATURES

- Low power CMOS
  - maximum active current 2.0 mA
  - maximum standby current 10 μA (at 6.0 V), typical 4 μA
- Non-volatile storage of 2-Kbits organized as 256 × 8-bits
- Single supply with full operation down to 2.5 V
- On-chip voltage multiplier
- Serial input/output I²C-bus
- Write operations
  - byte write mode
  - 8-byte page write mode (minimizes total write time per byte)
- Read operations
  - sequential read
  - random read
- Internal timer for writing (no external components)
- Power-on reset
- High reliability by using a redundant storage code
- Endurance
  - >500 k E/W-cycles at T_{amb} = 22 °C
- 40 years non-volatile data retention time (typ.)
- Pin and address compatible to
  - PCX8570, PCF8571, PCF8572 and PCF8581
  - PCX8494X-2, PCX8598X-2 -Family.

DESCRIPTION

The PCX8582X-2 is a 2-Kbit (256 × 8-bit) floating gate electrically erasable programmable read only memory (EEPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to eight PCX8582X-2 devices may be connected to the I²C-bus. Chip select is accomplished by three address inputs (A0, A1, A2).

Timing of the ERASE/WRITE cycle is carried out internally, thus no external components are required. Pin 7 (PTC) must be connected to either V_{DD} or left open-circuit.

There is an option of using an external clock for timing the length of an ERASE/WRITE cycle.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	6.0	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	–	60	μA
		V_{DD} = 6 V	–	200	μA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	–	0.6	mA
		V_{DD} = 6 V	–	2.0	mA
I_{DDSB}	supply current STANDBY	V_{DD} = 3 V	–	3.5	μA
		V_{DD} = 6 V	–	10	μA

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE (°C)		SUPPLY (V)	
	NAME	DESCRIPTION	VERSION	MIN.	MAX.	MIN.	MAX.
PCF8582C-2P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1	−40	+85	2.5	6.0
PCD8582D-2P				−25	+70	3.0	6.0
PCF8582E-2P				−40	+85	4.5	5.5
PCA8582F-2P				−40	+125	4.5	5.5
PCF8582C-2T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1	−40	+85	2.5	6.0
PCD8582D-2T				−25	+70	3.0	6.0
PCF8582E-2T				−40	+85	4.5	5.5
PCA8582F-2T				−40	+125	4.5	5.5

DEVICE SELECTION

Table 1 Device selection code

SELECTION	DEVICE CODE				CHIP ENABLE			R/$\overline{W}$
Bit	b7[1]	b6	b5	b4	b3	b2	b1	b0
Device	1	0	1	0	A2	A1	A0	R/$\overline{W}$

Note

1. The MSB b7 is sent first.

Table 2 Endurance and data retention guarantees

DEVICE	ENDURANCE E/W CYCLES	DATA RETENTION YEARS
PCF8582C-2; PCA8582F-2	500000[1]	40

Note

1. At the time of publication of this data sheet the statistical history was not yet sufficient to guarantee 1000000000 E/W cycle performance for these types.

BLOCK DIAGRAM

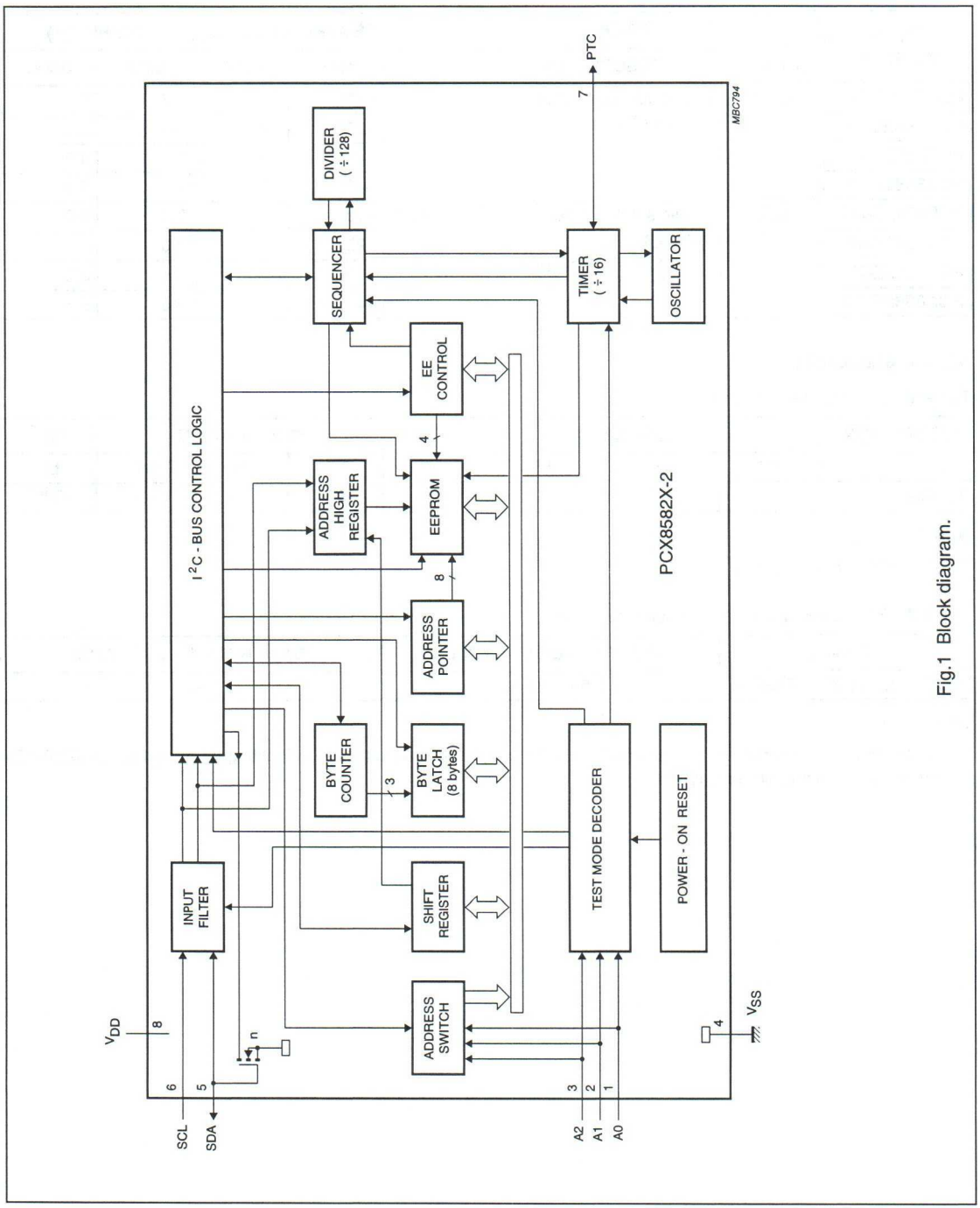


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	address input 0
A1	2	address input 1
A2	3	address input 2
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I²C-bus)
SCL	6	serial clock input (I²C-bus)
PTC	7	programming time control output
V_{DD}	8	positive supply voltage

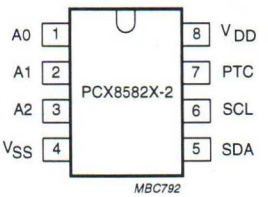


Fig.2 Pin configuration.

512 x 8-bit CMOS EEPROMS with I²C-bus interface

PCX8594X-2 Family

FEATURES

- Low power CMOS
  - maximum active current 2.5 mA
  - maximum standby current 10 µA (at 6.0 V), typical 4 µA
- Non-volatile storage of 4-Kbits organized as two pages of 256 × 8-bits each
- Single supply with full operation down to 2.5 V
- On-chip voltage multiplier
- Serial input/output I²C-bus
- Write operations
  - byte write mode
  - 8-byte page write mode (minimizes total write time per byte)
- Write-protection input
- Read operations
  - sequential read
  - random read
- Internal timer for writing (no external components)
- Power-on reset
- High reliability by using a redundant storage code (single bit error correction)
- Endurance
  - >500 k E/W-cycles at T_{amb} = 22 °C
- 40 years non-volatile data retention time (typ.)
- Pin and address compatible to
  - PCX8582X-2 Family and PCX8598X-2 Family.

DESCRIPTION

The PCX8594X-2 is a 4-Kbit (512 × 8-bit) floating gate electrically erasable programmable read only memory (EEPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to four PCX8594X-2 devices may be connected to the I²C-bus. Chip select is accomplished by two address inputs (A1 and A2).

Timing of the ERASE/WRITE cycle is carried out internally, thus no external components are required. Pin 7 (PTC) must be connected to either V_{DD} or left open-circuit.

There is an option of using an external clock for timing the length of an ERASE/WRITE cycle.

A write-protection input at pin 1 (WP) allows disable of write-commands from the master by a hardware signal. When pin 1 is HIGH and one of the upper 256 EEPROM cells is addressed, then the data bytes will not be acknowledged by the PCX8594X-2 and the EEPROM contents are not changed.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC 12 OR DATA SHEET

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	6.0	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	–	60	µA
		V_{DD} = 6 V	–	200	µA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	–	0.8	mA
		V_{DD} = 6 V	–	2.5	mA
I_{DDSB}	supply current STANDBY	V_{DD} = 3 V	–	3.5	µA
		V_{DD} = 6 V	–	10	µA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE (°C)		SUPPLY (V)	
	NAME	DESCRIPTION	VERSION	MIN.	MAX.	MIN.	MAX.
PCF8594C-2P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1	–40	+85	2.5	6.0
PCD8594D-2P				–25	+70	3.0	6.0
PCF8594E-2P				–40	+85	4.5	5.5
PCA8594F-2P				–40	+125	4.5	5.5
PCF8594C-2T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1	–40	+85	2.5	6.0
PCD8594D-2T				–25	+70	3.0	6.0
PCF8594E-2T				–40	+85	4.5	5.5
PCA8594F-2T				–40	+125	4.5	5.5

DEVICE SELECTION

Table 1 Device selection code

SELECTION	DEVICE CODE				CHIP ENABLE			R/$\overline{W}$
Bit	b7[1]	b6	b5	b4	b3	b2	b1	b0
Device	1	0	1	0	A2	A1	MEM SEL	R/$\overline{W}$

Note

1. The MSB b7 is sent first.

Table 2 Endurance and data retention guarantees

DEVICE	ENDURANCE E/W CYCLES	DATA RETENTION YEARS
PCF8594C-2; PCA8594F-2	500000[1]	40

Note

1. At the time of publication of this data sheet the statistical history was not yet sufficient to guarantee 1000000000 E/W cycle performance for these types.

BLOCK DIAGRAM

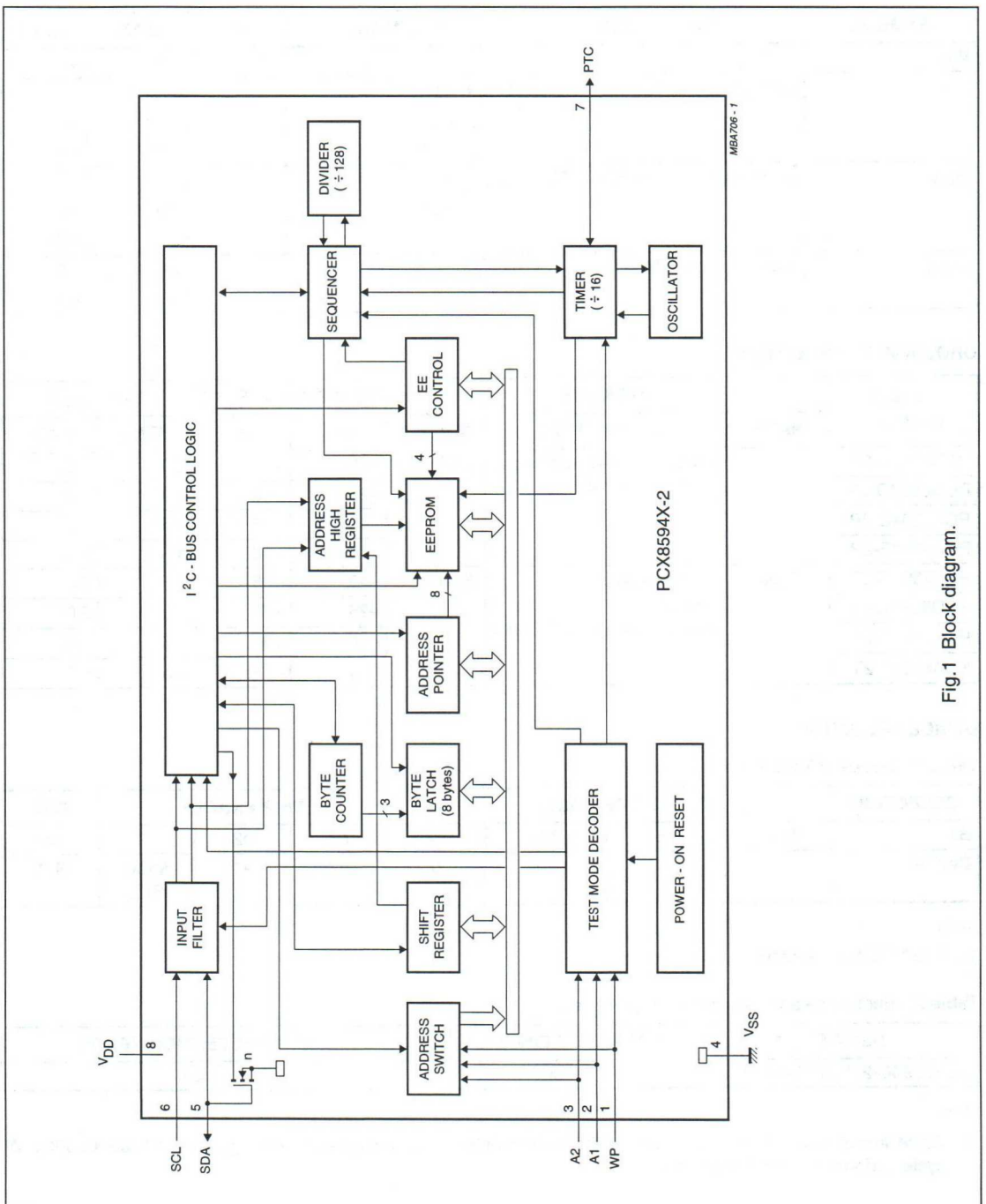


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
WP	1	write-protection input
A1	2	address input 1
A2	3	address input 2
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I^2C-bus)
SCL	6	serial clock input (I^2C-bus)
PTC	7	programming time control output
V_{DD}	8	positive supply voltage

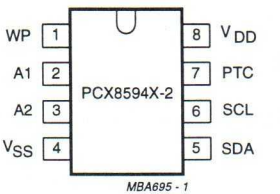


Fig.2 Pin configuration.

1024 × 8-bit CMOS EEPROMS with I²C-bus interface

PCX8598X-2 Family

FEATURES

- Low power CMOS
  - maximum active current 4.0 mA
  - maximum standby current 10 μA (at 6.0 V), typical 4 μA
- Non-volatile storage of 8-Kbits organized as four pages of 256 × 8-bits each
- Single supply with full operation down to 2.5 V
- On-chip voltage multiplier
- Serial input/output I²C-bus
- Write operations
  - byte write mode
  - 8-byte page write mode (minimizes total write time per byte)
- Write-protection input
- Read operations
  - sequential read
  - random read
- Internal timer for writing (no external components)
- Power-on reset
- High reliability by using a redundant storage code (single bit error correction)
- Endurance
  - >500 k E/W-cycles at T_{amb} = 22 °C
- 40 years non-volatile data retention time (typ.)
- Pin and address compatible to
  - PCX8582X-2 Family and PCX8594X-2 Family.

DESCRIPTION

The PCX8598X-2 is an 8-Kbit (1024 × 8-bit) floating gate electrically erasable programmable read only memory (EEPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to two PCX8598X-2 devices may be connected to the I²C-bus. Chip select is accomplished by one address input (A2).

Timing of the ERASE/WRITE cycle is carried out internally, thus no external components are required. Pin 7 (PTC) must be connected to either V_{DD} or left open-circuit.

There is an option of using an external clock for timing the length of an ERASE/WRITE cycle.

A write-protection input at pin 1 (WP) allows disable of write-commands from the master by a hardware signal. When pin 1 is HIGH and one of the upper 512 EEPROM cells is addressed, then the data bytes will not be acknowledged by the PCX8598X-2 and the EEPROM contents are not changed.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	6.0	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	–	60	μA
		V_{DD} = 6 V	–	200	μA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz			
		V_{DD} = 3 V	–	1.0	mA
		V_{DD} = 6 V	–	4.0	mA
I_{DDSB}	supply current STANDBY	V_{DD} = 3 V	–	3.5	μA
		V_{DD} = 6 V	–	10	μA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE (°C)		SUPPLY (V)	
	NAME	DESCRIPTION	VERSION	MIN.	MAX.	MIN.	MAX.
PCF8598C-2P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1	–40	+85	2.5	6.0
PCD8598D-2P				–25	+70	3.0	6.0
PCF8598E-2P				–40	+85	4.5	5.5
PCA8598F-2P				–40	+125	4.5	5.5
PCF8598C-2T	SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT176-1	–40	+85	2.5	6.0
PCD8598D-2T				–25	+70	3.0	6.0
PCF8598E-2T				–40	+85	4.5	5.5
PCA8598F-2T				–40	+125	4.5	5.5

DEVICE SELECTION

Table 1 Device selection code

SELECTION	DEVICE CODE				CHIP ENABLE			R/$\overline{W}$
Bit	b7[1]	b6	b5	b4	b3	b2	b1	b0
Device	1	0	1	0	A2	MEM SEL	MEM SEL	R/$\overline{W}$

Note

1. The MSB b7 is sent first.

Table 2 Endurance and data retention guarantees

DEVICE	ENDURANCE E/W CYCLES	DATA RETENTION YEARS
PCF8598C-2; PCA8598F-2	500000[1]	40

Note

1. At the time of publication of this data sheet the statistical history was not yet sufficient to guarantee 1 000 000 000 E/W cycle performance for these types.

BLOCK DIAGRAM

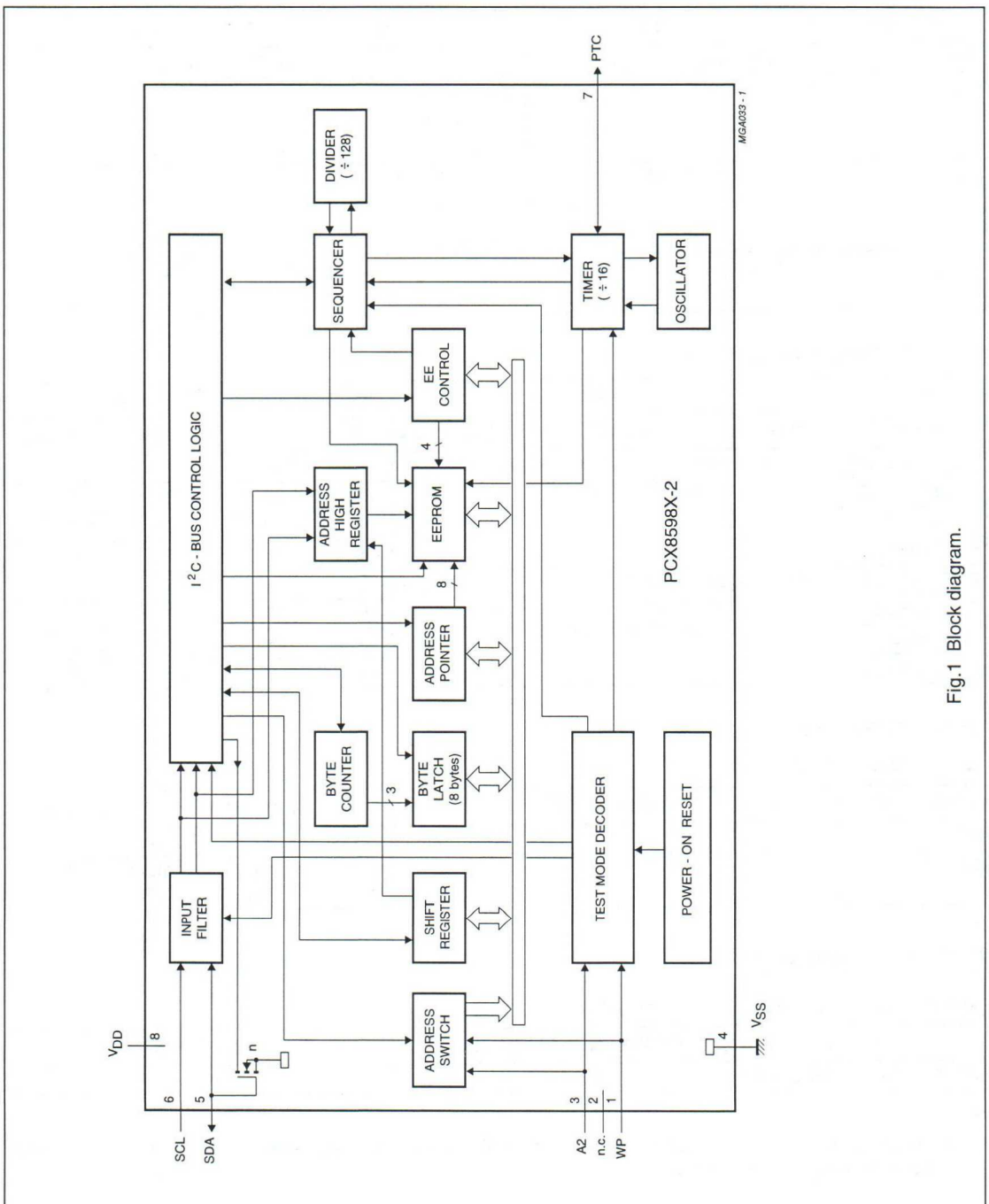


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
WP	1	write-protection input
n.c.	2	not connected
A2	3	address input 2
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I²C-bus)
SCL	6	serial clock input (I²C-bus)
PTC	7	programming time control output
V_{DD}	8	positive supply voltage

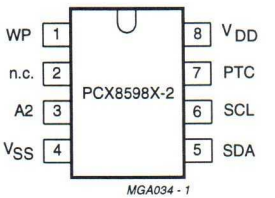


Fig.2 Pin configuration.

4-DIGIT LED-DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The LED-driver is a bipolar integrated circuit made in an I²L compatible 18 volts process. The circuit is especially designed to drive four 7-segment LED displays with decimal point by means of multiplexing between two pairs of digits. It features an I²C-Bus slave transceiver interface with the possibility to program four different SLAVE ADDRESSES, a POWER RESET flag, 16 current sink OUTPUTS, controllable by software up to 21 mA, two multiplex drive outputs for common anode segments, an on-chip multiplex oscillator, control bits to select static, dynamic and blank mode, and one bit for segment test.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	V_{EE} = 0 V	V_{CC}	4.5	5	15	V
Supply current all outputs OFF	V_{CC} = 5 V	I_{CC}*	7	9.5	14	mA
Total power dissipation						
24-lead DIL (SOT101B)		P_{tot}	–	–	1000	mW
24-lead DIL SO (SOT137A)		P_{tot}	–	–	500	mW
Operating ambient temperature range		T_{amb}	–40	–	+85	°C

* The positive current is defined as the conventional current flow into a device (sink current).

PACKAGE OUTLINE

SAA1064: 24-lead DIL; plastic with internal heat spreader (SOT101B).
SAA1064T: 24-lead mini-pack; plastic (SO-24; SOT137A).

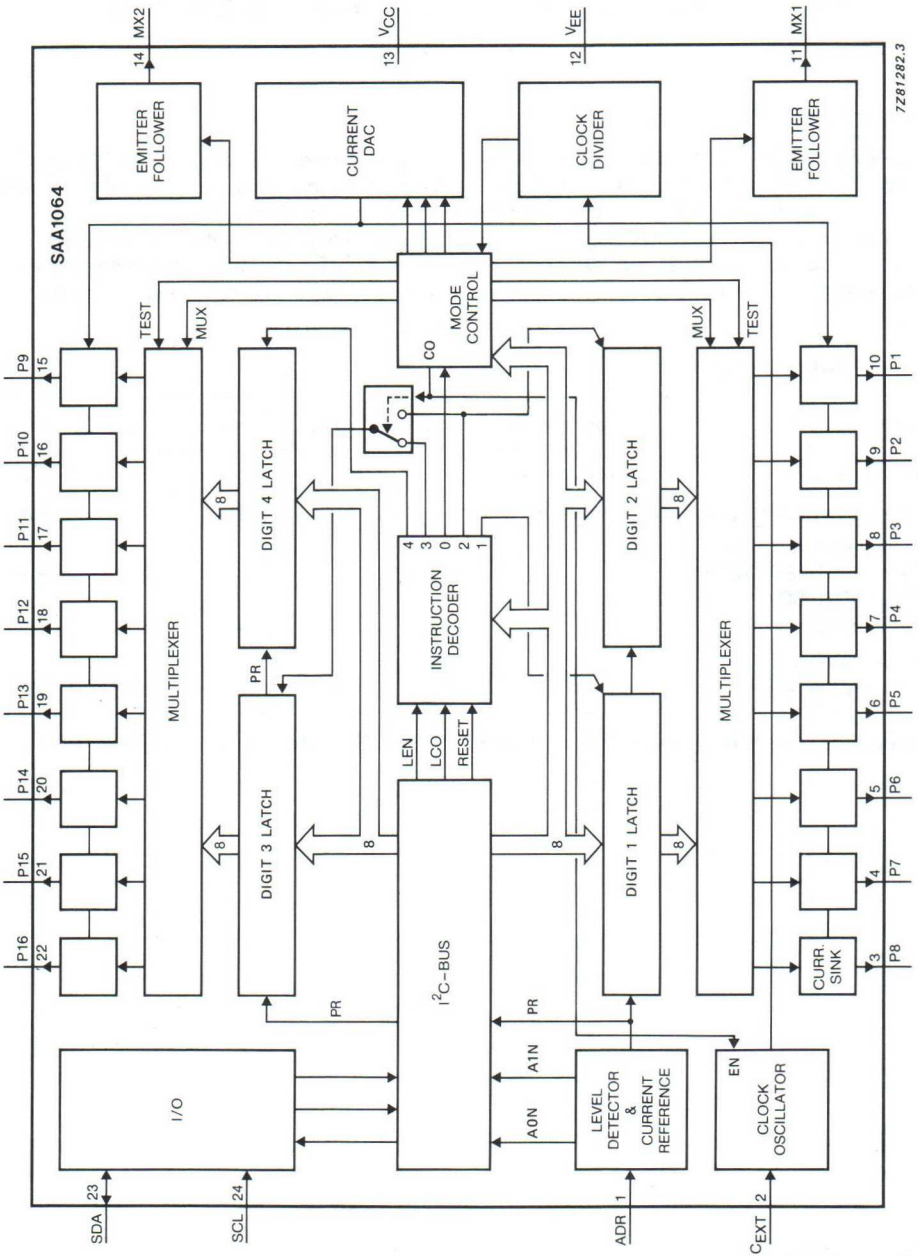


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
ADR	1	I²C-Bus slave address input
C_{EXT}	2	external control
P8 to P1	3-10	segment output
MX1	11	multiplex output
V_{EE}	12	ground
V_{CC}	13	positive supply
MX2	14	multiplex output
P9 to P16	15-22	segment output
SDA	23	I²C-Bus serial data line
SCL	24	I²C-Bus serial clock line

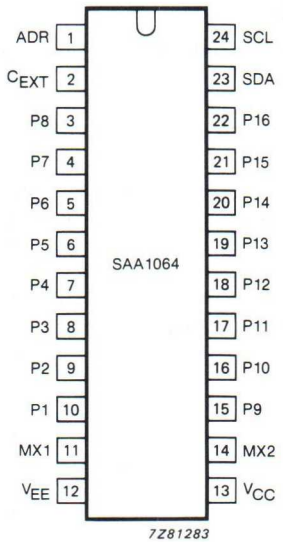


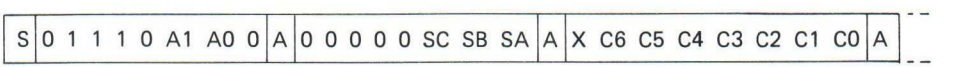
Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

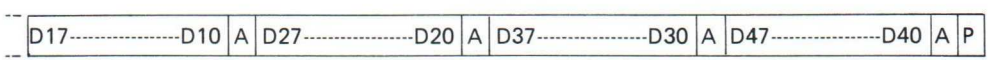


slave address status byte

Fig. 3a I²C-Bus format; READ mode.



slave address instruction byte control byte



data digit 1 data digit 2 data digit 3 data digit 4

Fig. 3b I²C-Bus format; WRITE mode.

S = start condition
P = stop condition
A = acknowledge
X = don't care

A1, A0 = programmable address bits
SC SB SA = subaddress bits
C6 to C0 = control bits
PR = POWER RESET flag

Address pin ADR

Four different slave addresses can be chosen by connecting ADR either to V_{EE}, 3/8 V_{CC}, 5/8 V_{CC} or V_{CC}. This results in the corresponding valid addresses HEX 70, 72, 74 and 76 for writing and 71, 73, 75 and 77 for reading. All other addresses cannot be acknowledged by the circuit.

Status byte

Only one bit is present in the status byte, the POWER RESET flag. A logic 1 indicates the occurence of a power failure since the last time it was read out. After completion of the READ action this flag will be set to logic 0.

Subaddressing

The bits SC, SB and SA form a pointer and determine to which register the data byte following the instruction byte will be written. All other bytes will then be stored in the registers with consecutive subaddresses. This feature is called Auto-Increment (AI) of the subaddress and enables a quick initialization by the master.
The subaddress pointer will wrap around from 7 to 0.
The subaddresses are given as follows:

SC	SB	SA	sub-address	function
0	0	0	00	control register
0	0	1	01	digit 1
0	1	0	02	digit 2
0	1	1	03	digit 3
1	0	0	04	digit 4
1	0	1	05	reserved, not used
1	1	0	06	
1	1	1	07	

Control bits (see Fig. 4)

The control bits C0 to C6 have the following meaning:

C0 = 0	static mode, i.e. continuous display of digits 1 and 2
C0 = 1	dynamic mode, i.e. alternating display of digit 1 + 3 and 2 + 4
C1 = 0/1	digits 1 + 3 are blanked/not blanked
C2 = 0/1	digits 2 + 4 are blanked/not blanked
C3 = 1	all segment outputs are switched-on for segment test*
C4 = 1	adds 3 mA to segment output current
C5 = 1	adds 6 mA to segment output current
C6 = 1	adds 12 mA to segment output current

Data

A segment is switched ON if the corresponding data bit is logic 1. Data bits D17 to D10 correspond with digit 1, D27 to D20 with digit 2, D37 to D30 with digit 3 and D47 to D40 with digit 4.
The MSBs correspond with outputs P8 and P16, the LSBs with P1 and P9. Digit numbers 1 to 4 are equal to their subaddresses (hex) 1 to 4.

* At a current determined by C4, C5 and C6.

SDA, SCL

The SDA and SCL I/O meet the I²C-Bus specification. For protection against positive voltage pulses on these inputs voltage regulator diodes are connected to V_{EE}. This means that normal line voltage should not exceed 5,5 volt. Data will be latched on the positive-going edge of the acknowledge related clock pulse.

Power-on reset

The power-on reset signal is generated internally and sets all bits to zero, resulting in a completely blanked display. Only the POWER RESET flag is set.

External Control (C_{EXT})

With a capacitor connected to pin 2 the multiplex frequency can be set (see Fig. 5). When static this pin can be connected to V_{EE} or V_{CC} or left floating since the oscillator will be switched off.

Segment outputs

The segment outputs P1 to P16 are controllable current-sink sources. They are switched on by the corresponding data bits and their current is adjusted by control bits C4, C5 and C6.

Multiplex outputs

The multiplex outputs MX1 and MX2 are switched alternately in dynamic mode with a frequency derived from the clock-oscillator. In static mode MX1 is switched on. The outputs consist of an emitter-follower, which can be used to drive the common anodes of two displays directly provided that the total power dissipation of the circuit is not exceeded. If this occurs external transistors should be connected to pins 11 and 14 as shown in Fig. 5.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 13)	$V_{EE} = 0$ V	V_{CC}	−0.5	18	V
Supply current (pin 13)		I_{CC}	−50	200	mA
Total power dissipation					
24-lead DIL (SOT101B)		P_{tot}		1000	mW
24-lead SO (SO137A)		P_{tot}		500	mW
SDA, SCL voltages	$V_{EE} = 0$ V	$V_{23,24}$	−0.5	5.9	V
Voltages ADR-MX1 and MX2-P16	$V_{EE} = 0$ V	$V_{1\text{-}11}$, $V_{14\text{-}22}$	−0.5	$V_{CC}+0.5$	V
Input/output current all pins	outputs OFF	$\pm I_{I/O}$	–	10	mA
Operating ambient temperature range		T_{amb}	−40	+85	°C
Storage temperature range		T_{stg}	−55	+150	°C

THERMAL RESISTANCE

From crystal to ambient

24-lead DIL	$R_{th\,j\text{-}a}$	35 K/W
24-lead SO (on ceramic substrate)	$R_{th\,j\text{-}a}$	75 K/W
24-lead SO (on printed circuit board)	$R_{th\,j\text{-}a}$	105 K/W

CHARACTERISTICS

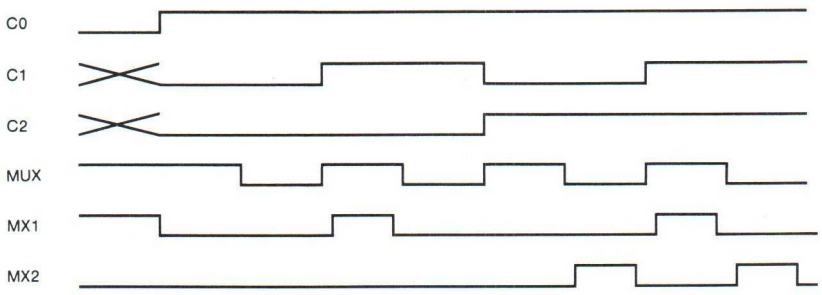
V_{CC} = 5 V; T_{amb} = 25 °C; voltages are referenced to ground (V_{EE} = 0 V); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 13)		V_{CC}	4,5	5,0	15	V
Supply current	all outputs OFF V_{CC} = 5 V	I_{CC}	7,0	9,5	14,0	mA
Power dissipation	all outputs OFF	P_d	–	50	–	mW
SDA; SCL (pins 23 and 24)						
Input voltages		$V_{23,24}$	0	–	5,5	V
Logic input voltage LOW		$V_{IL(L)}$	–	–	1,5	V
Logic input voltage HIGH		$V_{IH(L)}$	3,0	–	–	V
Input current LOW	$V_{23,24} = V_{EE}$	$-I_{IL}$	–	–	10	μA
Input current HIGH	$V_{23,24} = V_{CC}$	I_{IH}	–	–	10	μA
SDA						
Logic output voltage LOW	I_O = 3 mA	$V_{OL(L)}$	–	–	0,4	V
Output sink current		I_{SDA}	3	–	–	mA
Address input (pin 1)						
Input voltage programmable address bits:						
A0 = 0; A1 = 0		V_1	V_{EE}	–	$3/16V_{CC}$	V
A0 = 1; A1 = 0		V_1	$5/16V_{CC}$	$3/8V_{CC}$	$7/16V_{CC}$	V
A0 = 0; A1 = 1		V_1	$9/16V_{CC}$	$5/8V_{CC}$	$11/16V_{CC}$	V
A0 = 1; A1 = 1		V_1	$13/16V_{CC}$	–	V_{CC}	V
Input current LOW	$V_1 = V_{EE}$	$-I_1$	–	–	10	μA
Input current HIGH	$V_1 = V_{CC}$	I_1	–	–	10	μA
External control (C_{EXT}) pin 2						
Switching level input						
Input voltage LOW		V_{IL}	–	–	$V_{CC}-3,3$	V
Input voltage HIGH		V_{IH}	$V_{CC}-1,5$	–	–	V
Input current	V_2 = 2 V	I_2	−140	−160	−180	μA
	V_2 = 4 V	I_2	140	160	180	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Segment outputs (P8 to P1; pins 3 to 10) P9 to P16; pins 15 to 22)						
Output voltages	I_O = 15 mA	V_O	–	–	0.5	V
Output leakage current HIGH	$V_O = V_{CC}$ = 15 V	I_{LO}	–	–	± 10	μA
Output current LOW						
All control bits (C4, C5 and C6) are HIGH	V_{OL} = 5 V	I_{OL}	17.85	21	25.2	mA
Contribution of:						
control bit C4		I_O	2.55	3.0	3.6	mA
control bit C5		I_O	5.1	6.0	7.2	mA
control bit C6		I_O	10.2	12.0	14.4	mA
Relative segment output current accuracy						
with respect to highest value		ΔI_O	–	–	7.5	%
Multiplex 1 and 2 (pins 11 and 14)						
Maximum output voltage (when ON)	$-I_{MPX}$ = 50 mA	V_{MPX}	V_{CC}–1.5	–	–	V
Maximum output current HIGH (when ON)	V_{MPX} = 2 V	$-I_{MPX}$	50	–	110	mA
Maximum output current LOW (when OFF)	V_O = 2 V	$+ I_{MPX}$	50	70	110	μA
Multiplex output period	C_{EXT} = 2.7 nF	T_{MPX}	5	–	10	ms
Multiplexed duty factor			–	48.4	–	%

* Value to be fixed.



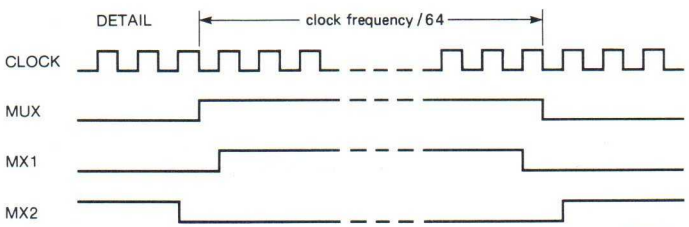


Fig. 4 Timing diagram.

APPLICATION INFORMATION

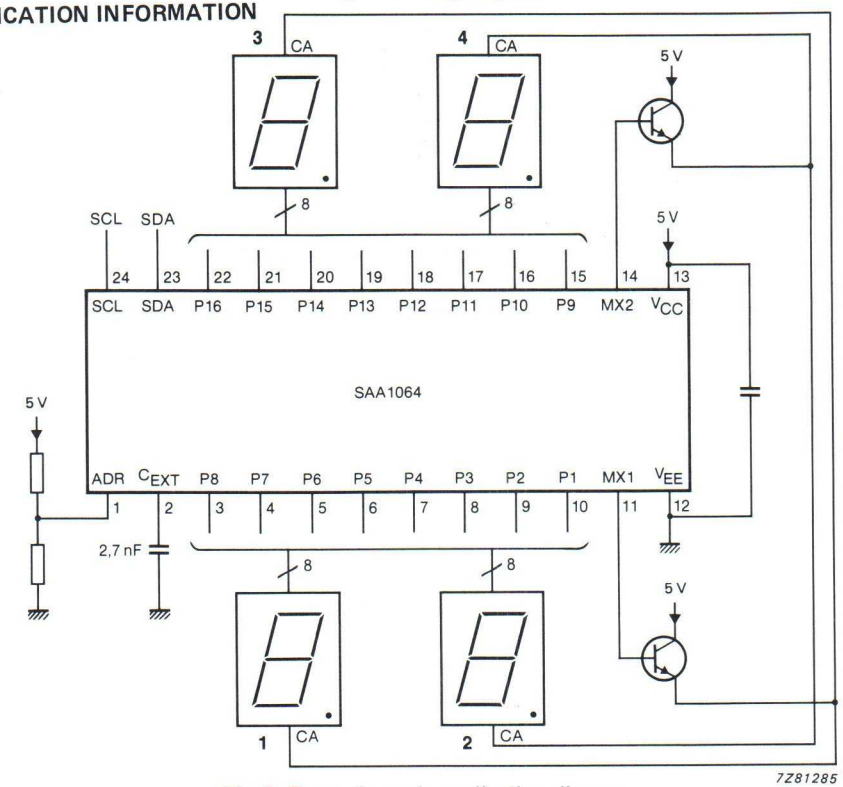


Fig. 5 Dynamic mode application diagram.

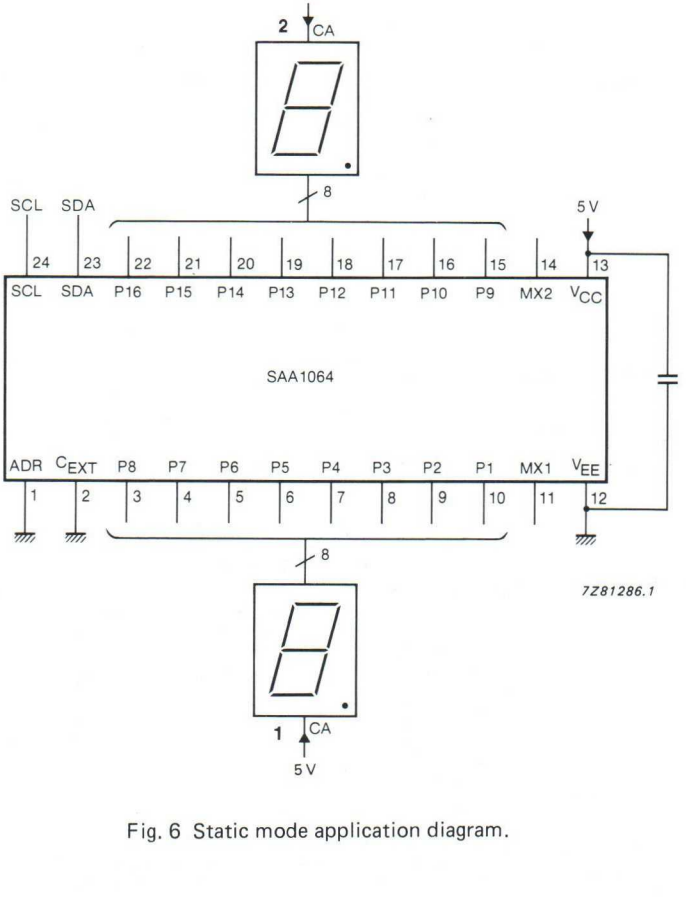


Fig. 6 Static mode application diagram.

POWER DISSIPATION

The total maximum power dissipation of the SAA1064 is made up by the following parts:

1. Maximum dissipation when none of the outputs are programmed (continuous line in Fig.7).
2. Maximum dissipation of each programmed output. The dashed line in Fig.7 visualises the dissipation when **all** the segments are programmed (max. 16 in the static, and max. 32 in the dynamic mode). When less segments are programmed one should take a proportional part of the maximum value.
3. Maximum dissipation of the programmed segment drivers which can be expressed as: $P_{add} = V_o \times I_o \times N$.

Where: P_{add} = The additional power dissipation of the segment drivers

V_o = The low state segment driver output voltage

I_o = The programmed segment output current

N = The number of programmed segments in the static mode, or half the number of programmed segment drivers in the dynamic mode.

Under no conditions the total maximum dissipation (500 mW for the SO and 1000 mW for the DIL package) should be exceeded.

Example: V_{cc} = 5 V

V_o = 0.25 V

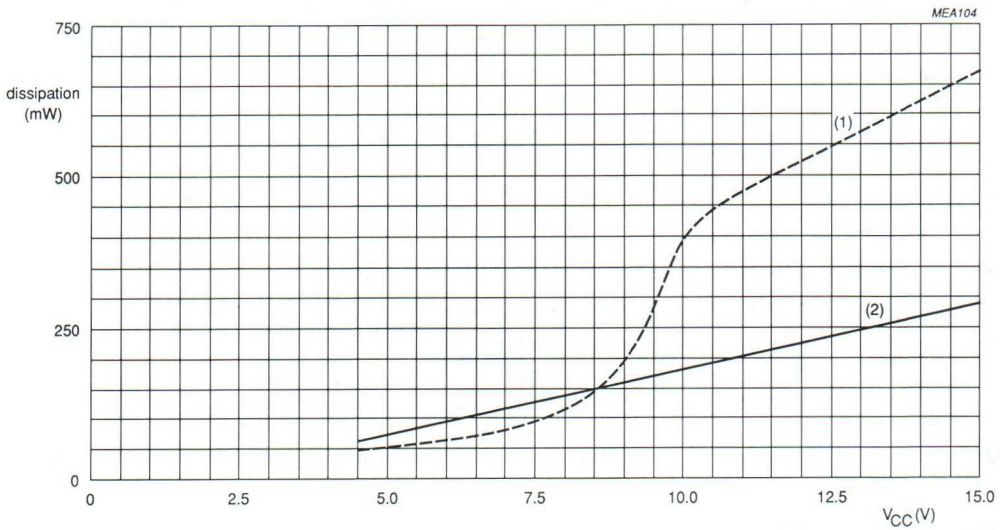
I_o = 12 mA

24 programmed segments in dynamic mode

$P_{tot} = P_1 + P_2 + P_3$

$= 75\ mW + (50 * 24/32)\ mW + (0.25 * 12.10^{-3} * 12)\ mW$

$= 148.5\ mW$



(1) All outputs programmed (no segment current sink).

(2) Outputs not programmed.

Fig.7 SAA1064 power dissipation as a function of supply voltage.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Philips Semiconductors

Data sheet	
status	Product specification
code	
date of issue	January 1990

SAA1101
Universal sync generator (USG)

FEATURES

- Programmable to seven standards
- Additional outputs to simplify signal processing
- Can be synchronized to an external sync. signal
- Option to select the 524/624 line mode instead of the 525/625 line mode
- Lock from subcarrier to line frequency

GENERAL DESCRIPTION

The SAA1101 is a Universal Sync Generator (USG) and is designed for application in video sources such as cameras, film scanners, video generators and associated apparatus. The circuit can be considered as a successor to the SAA1043 sync generator and the SAA1044 subcarrier coupling IC.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range (pin 28)	4.5	5.5	V
I_{DD}	quiescent supply current	–	10	μA
f_{OSC}	clock oscillator frequency	–	24	MHz

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA1101P	28	DIL	plastic	SOT117
SAA1101T	28	SO28	plastic	SOT136A

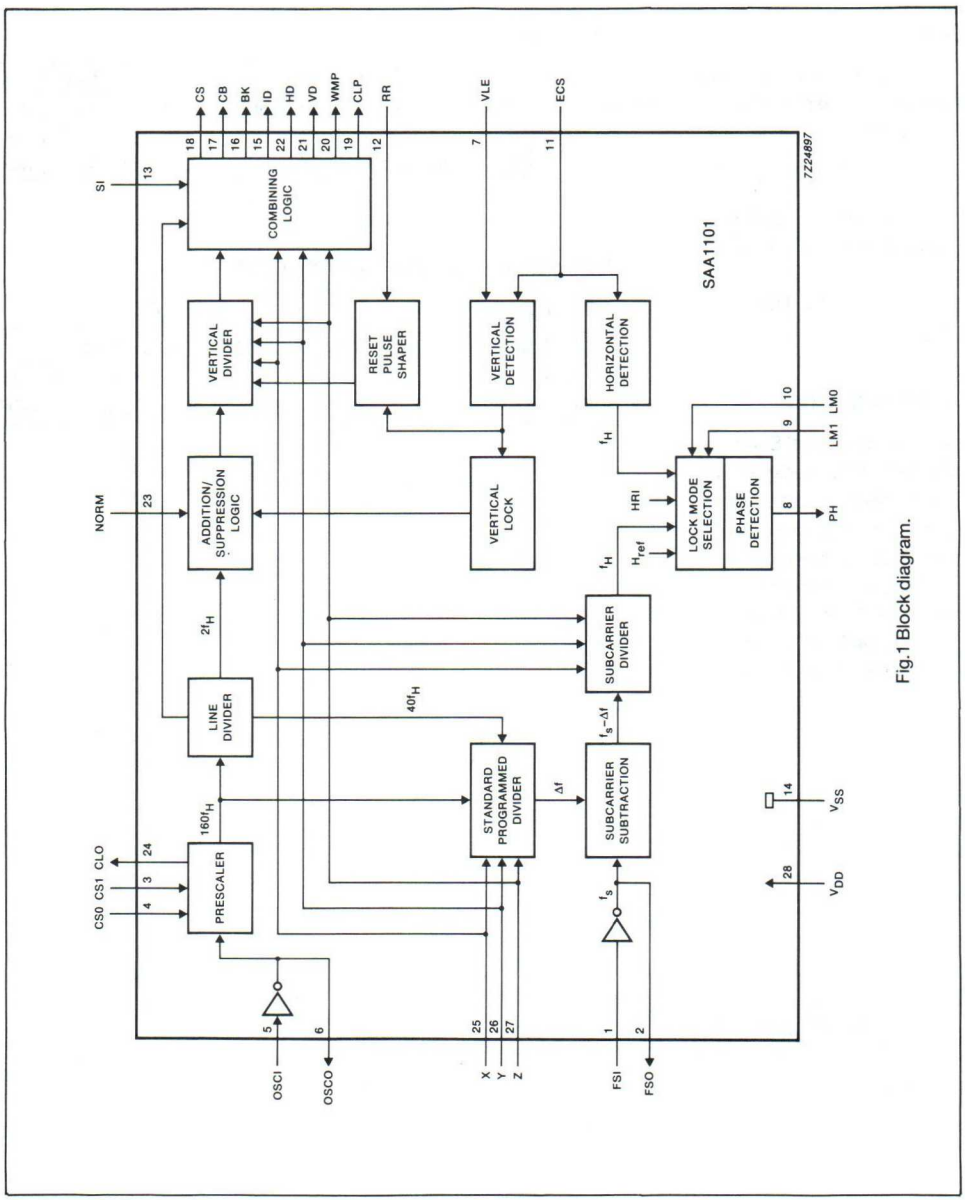


Fig.1 Block diagram.

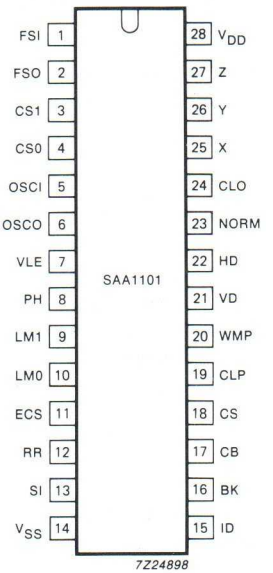


Fig.2 Pinning configuration; SOT117.

PINNING

SYMBOL	PIN	DESCRIPTION
FSI	1	subcarrier oscillator input, where f_{max} = 5 MHz
FSO	2	subcarrier oscillator output
CS1	3	clock frequency selection – CMOS input
CS0	4	clock frequency selection – CMOS input
OSCI	5	clock oscillator input, where f_{max} = 24 MHz
OSCO	6	clock oscillator output
VLE	7	vertical in-lock enable – CMOS input
PH	8	phase detector output – 3-state output
LM1	9	lock mode selection – CMOS input
LM0	10	lock mode selection – CMOS input
ECS	11	external composite sync. signal – CMOS Schmitt-trigger input
RR	12	frame reset – CMOS Schmitt-trigger input
SI	13	set identification, used to set the correct field sequence in PAL-mode. The correction (inversion of fH2) is done at the left-hand slope of the SI-pulse. Minimum pulse width is 800 ns. CMOS Schmitt-trigger input.
V_{SS}	14	ground
ID	15	identification – push-pull output
BK	16	burst key (PAL/NTSC), chroma-blanking (SECAM) – push-pull output
CB	17	composite blanking – push-pull output
CS	18	composite sync. – push-pull output
CLP	19	clamp pulse – push-pull output
WMP	20	white measurement pulse – 3-state output
VD	21	vertical drive pulse – push-pull output
HD	22	horizontal drive pulse – push-pull output
NORM	23	used with X, Y and Z to select TV system; NORM = 0, 625/525 line mode (standard); NORM = 1, 624/524 line mode – CMOS input
CLO	24	clock output – push-pull output
X	25	TV system selection input – CMOS input
Y	26	TV system selection input – CMOS input
Z	27	TV system selection input – CMOS input
V_{DD}	28	voltage supply

FUNCTIONAL DESCRIPTION

Generation of pulses

Generation of standard pulses such as sync, blanking and burst for TV systems: PAL B/G, PALN, PALM, SECAM and NTSC. In addition a number of non-standard pulses have been supplied to simplify signal processing. These signals include – horizontal drive, vertical drive, clamp pulse, identification etc. It is possible to select the 524/624 line mode instead of the 525/625 line mode for all the above TV systems for applications such as robotics, games and computers.

Lock modes

The USG offers four lock modes:

- Lock from the subcarrier
- Slow sync. lock, external H_{ref}
- Slow sync. lock, internal H_{ref}
- Fast sync. lock, internal H_{ref}

LOCK FROM SUBCARRIER

Lock from subcarrier to the line frequency for the above mentioned TV systems is given below; the horizontal frequency (f_H) = 15.625 kHz for 625 line systems and 15.734264 kHz for 525 line systems.

SECAM (1 and 2)	$282f_H$
PALN	$229.2516f_H$
NTSC (1 and 2)	$227.5f_H$
PALM	$227.25f_H$
PAL B/G	$283.7516f_H$

These relationships are obtained by the use of a phase locked loop and the internal programmed divider chain, see Fig. 3(a).

LOCK TO AN EXTERNAL SIGNAL SOURCE

The following methods can be used to lock to an external signal source:

1. Sync. lock slow; the line frequency is locked to an external signal. The line and frame information are extracted from the external sync. signal and used separately in the lock system. The line information is used in a phase-locked loop where external and internal line frequencies are compared by the same phase detector as is used for the subcarrier lock. The external frame information is compared with the internal frame in a slow lock system; mismatch of internal and external frames will result in the addition or suppression of one line depending on the direction of the fault. The maximum lock time for frame lock is 6.25 s, see Fig. 3(b).
2. Sync. lock fast. A fast lock of frames is possible with a frame reset which is extracted out of the incoming external sync. signal, see Fig. 3(c).
3. Sync. lock with external reference. Lock of an external sync. signal to the line frequency with an external line reference to make possible a shifted lock. The subcarrier input is, in this case, used as an external input for the horizontal reference, see Fig. 3(d).

SELECTION OF LOCK MODE

Lock mode is selected using the inputs LM0 and LM1 as illustrated in the Table below.

LM0	LM1	SELECTION
0	0	lock to subcarrier
0	1	slow sync. lock external H_{ref}
1	0	slow sync. lock internal H_{ref}
1	1	fast sync. lock internal H_{ref}

The different lock modes are illustrated by the following figures:

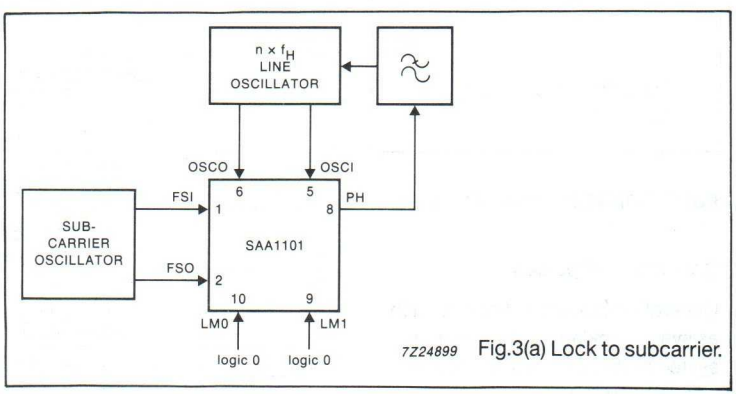


Fig.3(a) Lock to subcarrier.

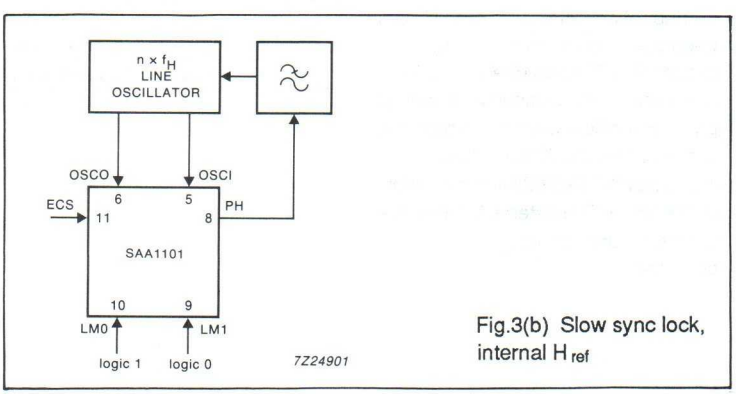


Fig.3(b) Slow sync lock, internal H_{ref}

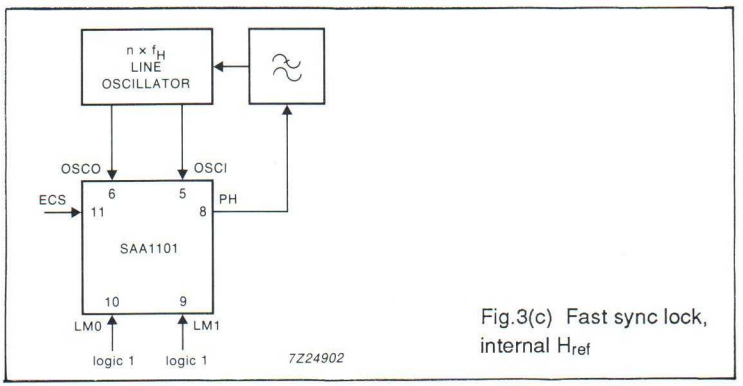


Fig.3(c) Fast sync lock, internal H_{ref}

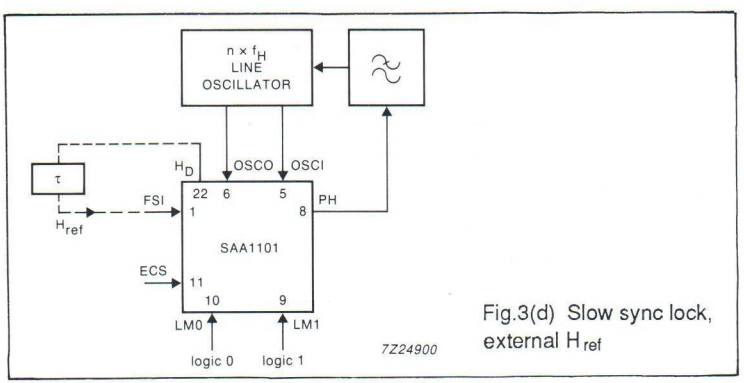


Fig.3(d) Slow sync lock, external H_{ref}

LOCK WITH HORIZONTAL AND VERTICAL SIGNALS

(slow lock modes only)

It is possible to use horizontal and vertical signals instead of composite sync signals. The connections in this situation are: the external horizontal signal is connected to the ECS input (pin 11) and the vertical signal to the RR input (pin 12). The HIGH time of the horizontal pulse must be less than 14.4 μs, otherwise it will be detected as being a vertical pulse and will corrupt the vertical slow lock system.

Selection of Clock Frequency

The clock frequency is selected using the CS0 and CS1 inputs as illustrated below.

CS0	CS1	FREQUENCY	625 LINES	525 LINES	UNITS
0	0	$160f_H$	2.5	2.517482	MHz
0	1	$320f_H$	5	5.034964	MHz
1	0	$960f_H$	15	15.104893	MHz
1	1	$1440f_H$	22.5	22.657340	MHz

Where the horizontal frequency, f_H = 15.625 kHz for 625 lines and 15.734264 kHz for 525 lines.

Oscillators

The subcarrier oscillator has FSI as its input and FSO as its output. It is always used as a crystal oscillator with a series resonance crystal with parallel load capacitor. The maximum frequency, f_{max} = 5 MHz and the load capacitor, $C_L = 10 < C_L < 35$ pF.

The clock oscillator has OSCI as its input and OSCO as its output. It can be used with an LC oscillator or a series resonance crystal with parallel load capacitor (Fig.4). The maximum frequency, f_{max} = 24 MHz and the load capacitor, $C_L = 10 < C_L < 35$ pF.

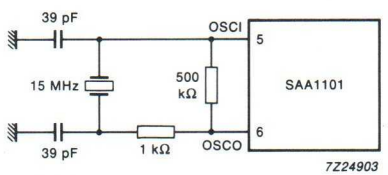


Fig.4 Crystal oscillator circuit.

Selection of TV System

Selection of the required TV system is achieved by the X, Y and Z inputs as illustrated by the following Table.

SYSTEM	X	Y	Z
SECAM1	0	0	0
PALN	0	0	1
NTSC1	0	1	0
PALM	0	1	1
SECAM2	1	0	0 (with identifier)
PAL B/G	1	0	1
NTSC2	1	1	0 (short blanking)

Selection of 625/525 (standard; interlaced mode) or 624/524 lines (non-interlaced mode)

Selection is achieved using the NORM input. When NORM = 0, 625/525 (standard) lines are selected; when NORM = 1, 624/524 line are selected.

Output Dimensions

All push-pull outputs: standard output 2 mA.

White measurement pulse, WMP: 3-state output 2 mA.

Phase detector, PH: 3-state output 2 mA.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7	V
V_I	input voltage	−0.5	V_{DD} + 0.5 *	V
I_I	maximum input current	–	±10	mA
I_O	maximum output current	–	±10	mA
I_{DD}	maximum supply current in V_{DD}	–	25	mA
P_{tot}	maximum power dissipation	–	400	mW
T_{stg}	storage temperature range	−55	+150	°C

* Input voltage should not exceed 7 V.

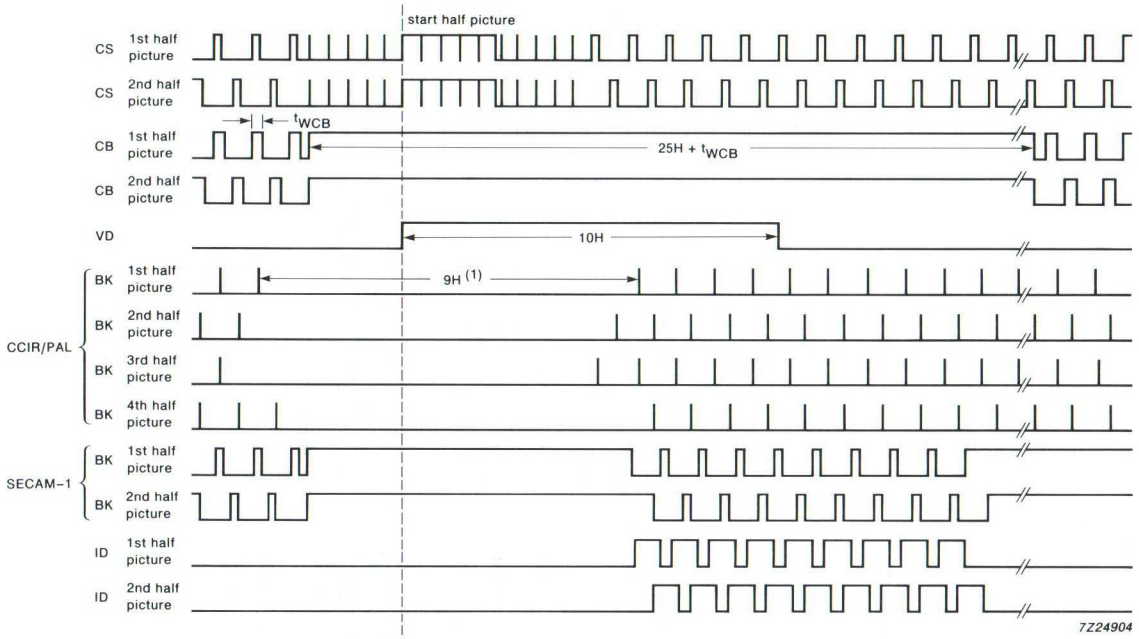
CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = -25 to +70 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	–	5.5	V
I_{DD}	supply current (quiescent)	T_{amb} = 25 °C	–	–	10	µA
Inputs						
$\pm I_I$	input leakage current	T_{amb} = 25 °C	–	–	100	nA
CMOS COMPATIBLE; X, Y, Z, NORM, CS0, CS1, LM0, LM1 AND VLE						
V_{IH}	input voltage HIGH		$0.7V_{DD}$	–	–	V
V_{IL}	input voltage LOW		–	–	$0.3V_{DD}$	V
SCHMITT TRIGGER INPUTS; ECS, RR AND SI						
V_{T+}	positive-going threshold		–	2.5	4	V
V_{T-}	negative-going threshold		1	1.5	–	V
V_H	hysteresis		0.4	1	–	V
OSCILLATOR INPUTS; OSCI AND FSI						
V_{IH}	input voltage HIGH		$0.7V_{DD}$	-	–	V
V_{IL}	input voltage LOW		–	–	$0.3V_{DD}$	V
Outputs PUSH-PULL OUTPUTS; CB, CS, BK, ID, HD, VD, CLP AND CLO						
V_{OH}	output voltage HIGH	$-I_O$ = 2 mA; V_{DD} = 5 V	4.5	–	–	V
V_{OL}	output voltage LOW	I_O = 2 mA; V_{DD} = 5 V	–	–	0.5	V
OSCILLATOR OUTPUTS; OSCO AND FSO						
V_{OH}	output voltage HIGH	$-I_O$ = 0.75 mA; V_{DD} = 5 V	4.5	–	–	V
V_{OL}	output voltage LOW	I_O = 0.75 mA; V_{DD} = 5 V	–	–	0.5	V
3-STATE OUTPUTS; WMP AND PH						
V_{OH}	output voltage HIGH	$-I_O$ = 2 mA; V_{DD} = 5 V	4.5	–	–	V
V_{OL}	output voltage LOW	I_O = 2 mA; V_{DD} = 5 V	–	–	0.5	V
$\pm I_{OZ}$	OFF-state current	T_{amb} = 25 °C	–	–	50	nA

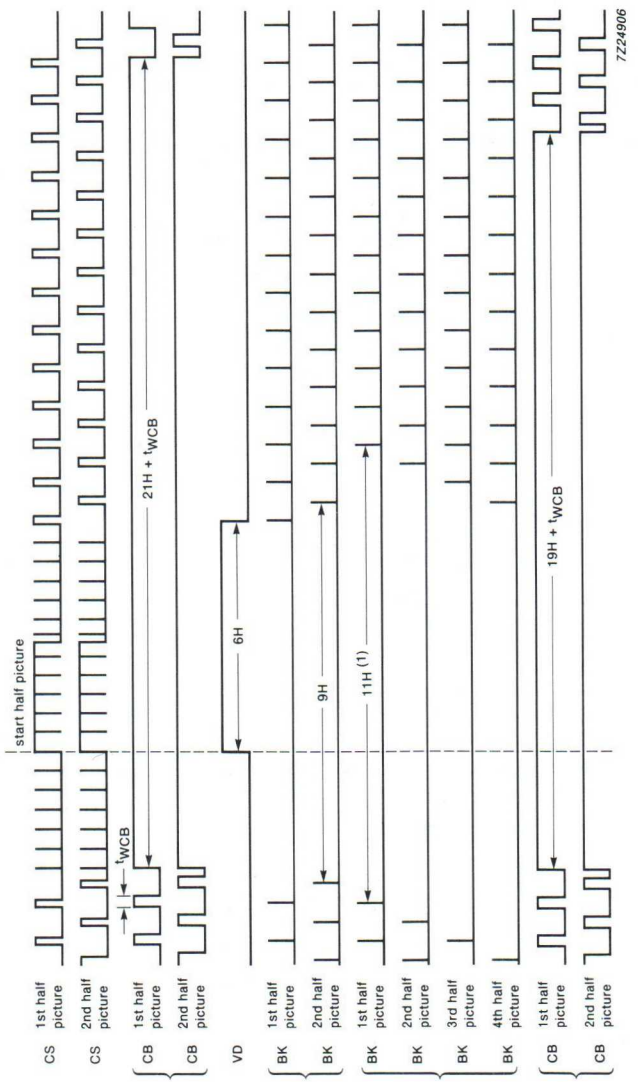
OUTPUT WAVEFORMS

The output waveforms for the different modes of operation are illustrated by Figs 5 and 6.



(1) H = 1 horizontal scan.

Fig.5 Typical output waveforms for PAL/CCIR and SECAM. In the 624-line mode the output waveforms are identical to the first half picture of PAL/CCIR and are not interlaced.



(1) H = 1 horizontal scan.
(2) NTSC mode reset; the fourth half picture is identical to the second half picture for NTSC.

Fig.6 Typical output waveforms for NTSC and PAL-M. In the 524-line mode the output waveforms are identical to the first half picture of NTSC and are not interlaced.

WAVEFORM TIMING

The waveform timing depends on the frequency of the oscillator input (f_{OSCI}). This is illustrated in the table below as the number (N) of oscillations at OSCI. The timings are derived from N x t_{OSCI} ± 100 ns.

One horizontal scan (H) = 320 x t_{OSCI} = $1/f_H$.

Where t_{OSCI} = 200 ns for PAL/SECAM and 198.6 ns for NTSC/PAL-M

SYMBOL	PARAMETER	PAL	NTSC	PAL-M	SECAM	UNIT	N
Composite sync (CS)							
t_{WSC1}	horizontal sync pulse width	4.8	4.77	4.77	4.8	µs	24
t_{WSC2}	equalizing pulse width	2.4	2.38	2.38	2.4	µs	12
t_{WSC3}	serration pulse width	4.8	4.77	4.77	4.8	µs	24
-	duration of pre-equalizing pulses	2.5	3	3	2.5	H	-
-	duration of post-equalizing pulses	2.5	3	3	2.5	H	-
-	duration of serration pulses	2.5	3	3.5	2.5	H	-
Composite blanking (CB) HORIZONTAL BLANKING PULSE WIDTH							
t_{WCB}	PAL/SECAM/PAL-M	12	–	11.12	12	µs	60
t_{WCB}	NTSC1	–	11.12	–	–	µs	56
t_{WCB}	NTSC2	–	10.53 *	–	–	µs	53
FRONT PORCH							
t_{PCBCS}	front porch	1.6	1.59	1.59	1.6	µs	8
DURATION OF VERTICAL BLANKING							
-	PAL/SECAM/PAL-M	25H + t_{WCB}	–	21H + t_{WCB}	25H + t_{WCB}	–	-
-	NTSC1	–	21H + t_{WCB}	–	–	–	-
-	NTSC2	–	19H + t_{WCB}	–	–	–	-
Burst key (BK) (not SECAM)							
t_{WBK}	burst key pulse width	2.4	2.38	2.38	–	µs	12
t_{PCSBK}	CS to burst key delay	5.6	5.56	5.76	–	µs	28
-	burst suppression	9	9	11	–	H	-

* Horizontal blanking pulse width for NTSC2 can be 11.12 µs maximum

SYMBOL	PARAMETER	PAL	NTSC	PAL-M	SECAM	UNIT	N
Burst key (BK) (not SECAM) (continued) POSITION OF BURST SUPPRESSION							
-	first half picture	H623 to H6	H523 to H6	H523 to H8	–	–	-
-	second half picture	H310 to H318	H261 to H269	H260 to H270	–	–	-
-	third half picture	H622 to H5	H523 to H6	H522 to H7	–	–	-
-	fourth half picture	H311 to H319	H261 to H269	H259 to H269	–	–	-
Burst key (BK) (SECAM)							
t_{WBK}	chroma pulse width	–	–	–	7.2	µs	36
t_{PBKCS}	CS to chroma delay	–	–	–	1.6	µs	8
DURATION OF VERTICAL BLANKING							
-	SECAM1	–	–	–	note 1	–	-
-	SECAM2	–	–	–	note 2	–	-
Clamp pulse (CLP)							
t_{WCLP}	clamp pulse width	2.4	2.38	2.38	2.4	µs	12
t_{PCSCLP}	CS to CLP delay	1.6	1.59	1.59	1.6	µs	8
Horizontal drive (HD)							
t_{WHD}	pulse width	7.2	7.15	7.15	7.2	µs	36
t_{PHDCS}	CS to HD delay	0.8	0.79	0.79	0.8	µs	4
-	repetition period	64	63.56	63.56	64	µs	-
Vertical drive (VD)							
-	VD duration	10	6	6	10	H	-
t_{PVDCS}	CS to VD delay	1.6	1.59	1.59	1.6	µs	8
White measurement pulse (WMP)							
-	pulse width	2.4	2.38	2.38	2.4	µs	12
-	CS to WMP delay	34.4	34.16	34.16	34.4	µs	172
-	duration of WMP	10	9	9	10	H	-

WAVEFORM TIMING (CONTINUED)

SYMBOL	PARAMETER	PAL	NTSC	PAL-M	SECAM	UNIT	N
White measurement pulse (WMP) (continued)							
POSITION OF WMP							
-	first half picture	H163 to H173	H134 to H143	H134 to H143	H163 to H173	–	-
-	second half picture	H475 to H485	H396 to H405	H396 to H405	H475 to H485	–	-
Identification (ID)							
t_{WID}	pulse width	12	11.12	11.12	12	µs	60
t_{PIDCS}	CS to ID delay	1.6	1.59	1.59	1.6	µs	8
POSITION OF ID							
-	first half picture	H7 to H15	H8 to H22	H8 to H22	H7 to H15	–	-
-	second half picture	H320 to H328	H271 to H285	H271 to H285	H320 to H328	–	-

Notes to the characteristics

1. SECAM1, first half picture: 25H + t_{WBK} except H320 to H328. Second half picture: 24.5H + t_{WBK} except H7 to H15.

2. SECAM2, first half picture: 25H + t_{WBK}. Second half picture: 24.5H + t_{WBK}.

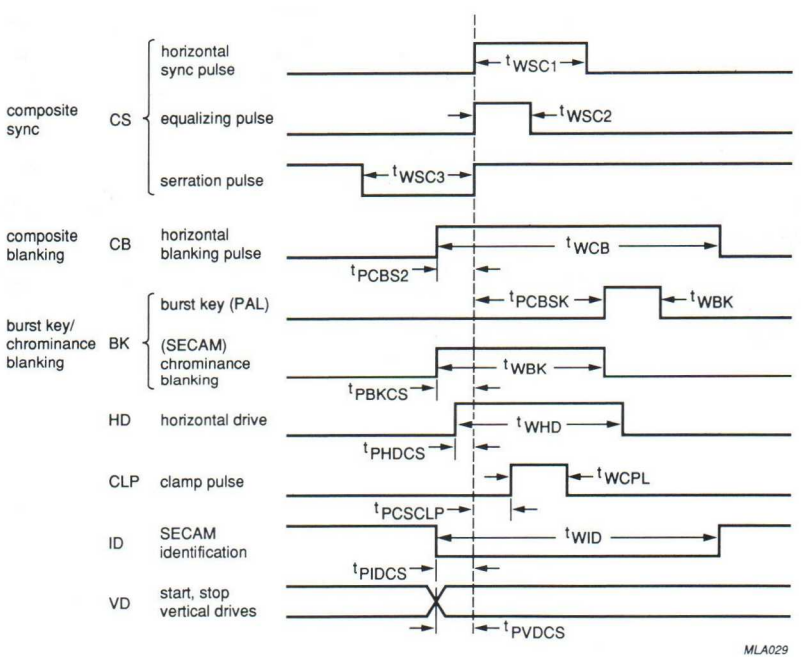


Fig.7 Waveform timing.

TUNER SWITCHING CIRCUIT

The SAA1300 is for switching on and off the supply lines of various circuit parts via an I²C bus signal. Furthermore, it can be used to supply current for switching diodes in radio and television tuners. It contains 5 output stages, which are capable of supplying up to 85 mA in the ON state or sinking up to −100 μA in the OFF state.

Current limiting and short-circuit protection are included. The output stages are driven by a shift register/latch combination which is loaded via data from the I²C bus. A power-on reset of the latches ensures the OFF state of the output stages (OUT 2 to OUT 5) without data reception from the I²C bus. A subaddressing system allows the connection of up to three circuits on the same I²C bus lines; one of the outputs (OUT 1, pin 7) can also be used as an input to select the device via a simple internal A/D converter.

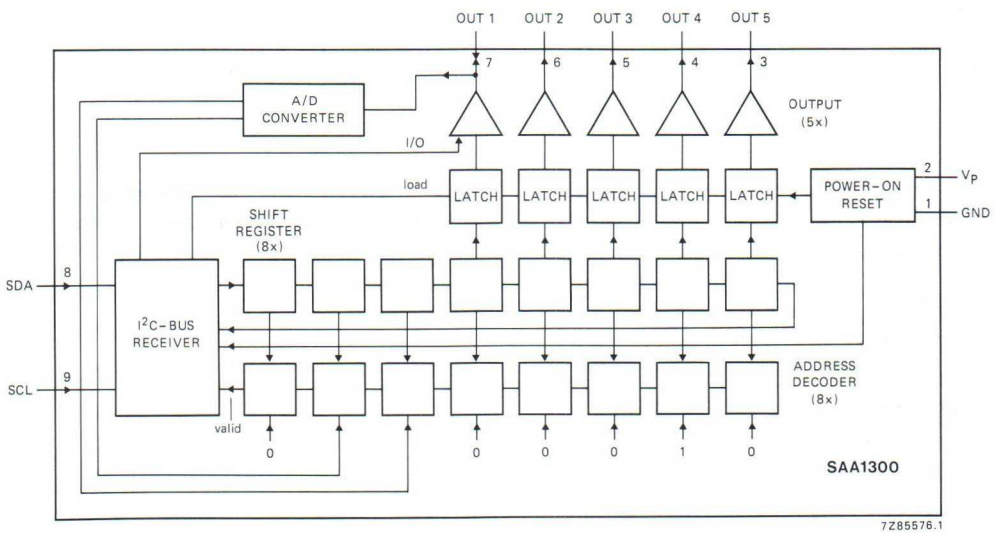


Fig. 1 Block diagram.

PACKAGE OUTLINE

9-lead SIL; plastic (SOT142).

PINNING

pin no.	symbol	function
1	GND	ground
2	V_P	positive supply
3	OUT 5	outputs
4	OUT 4	
5	OUT 3	
6	OUT 2	
7	OUT 1	output and subaddressing input
8	SDA	serial data line (I^2C bus)
9	SCL	serial clock line (I^2C bus)

I^2C BUS INFORMATION

Address, first byte

0 1 0 0 0 A B 0 where,

A	B	function	condition
0	0	general address	OUT 1 = output
0	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,L}$ (LOW)
1	0	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,H}$ (HIGH)
1	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,M}$ (MEDIUM)

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max. 13,2	V
Input voltage range at SDA, SCL	V_I	−0,5 to + 6,0	V
Input voltage range at OUT 1	V_I	−0,5 to + 12,5	V
Output voltage range at OUT 1 to OUT 5	V_O	−0,5 to + 12,5	V
Input current at SDA, SCL	I_I	max. 20	mA
Input current at OUT 1	I_I	max. 20	mA
Total power dissipation	P_{tot}	max. 825	mW
Storage temperature range	T_{stg}	−40 to + 125	°C
Operating ambient temperature range	T_{amb}	−20 to + 80	°C

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 2)					
Supply voltage range	V_P	4	8	12	V
Supply current					
5 outputs LOW	I_{PL}	5	10	15	mA
5 outputs HIGH	I_{PH}	30	50	70	mA
Power-on reset level output stage in "OFF' condition	V_{PR}	–	3,5	3,8	V
Maximum power dissipation*	P_{max}	–	650	–	mW
Inputs SDA, SCL (pins 8 and 9)					
Input voltage HIGH	V_{IH}	3,0	–	5,5	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current HIGH	$-I_{IH}$	–	–	10	μA
Input current LOW	I_{IH}	–	–	0,4	μA
Acknowledge sink current	I_{ACK}	2,5	–	–	mA
Maximum input frequency	$f_{i\,max}$	100	–	–	kHz
Outputs OUT 1 to OUT 5 (pins 3 to 7)					
Maximum output current; source: "ON"	I_{Oso}	+ 85	–	+ 150	mA
Maximum output current; source: "ON" T_{amb} = 80 °C	I_{Oso}	60	–	–	mA
Output voltage HIGH at I_{Oso} = 85 mA	V_{OH}	V_P–2	–	–	V
Output current; sink "OFF"	I_{Osi}	–100	–300	–	μA
Output voltage LOW at I_{Osi} = –100 μA	V_{OL}	–	–	100	mV
Output voltage MEDIUM at I_O = 10 mA	V_{OM}	V_P–0,5	–	–	V
OUT 1 used as subaddressing input					
Input voltage HIGH (code 1 0)	$V_{OUT\,1H}$	0,72 V_P	–	V_P	V
Input voltage MEDIUM (code 1 1)	$V_{OUT\,1M}$	0,39 V_P	–	0,61 V_P	V
Input voltage LOW (code 0 1)	$V_{OUT\,1L}$	0	–	0,28 V_P	V



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

* Outputs must not be driven simultaneously at maximum source current.

Data sheet	
status	Product specification
date of issue	April 1995

SAA1310

Control interface for VHS video recorders

FEATURES

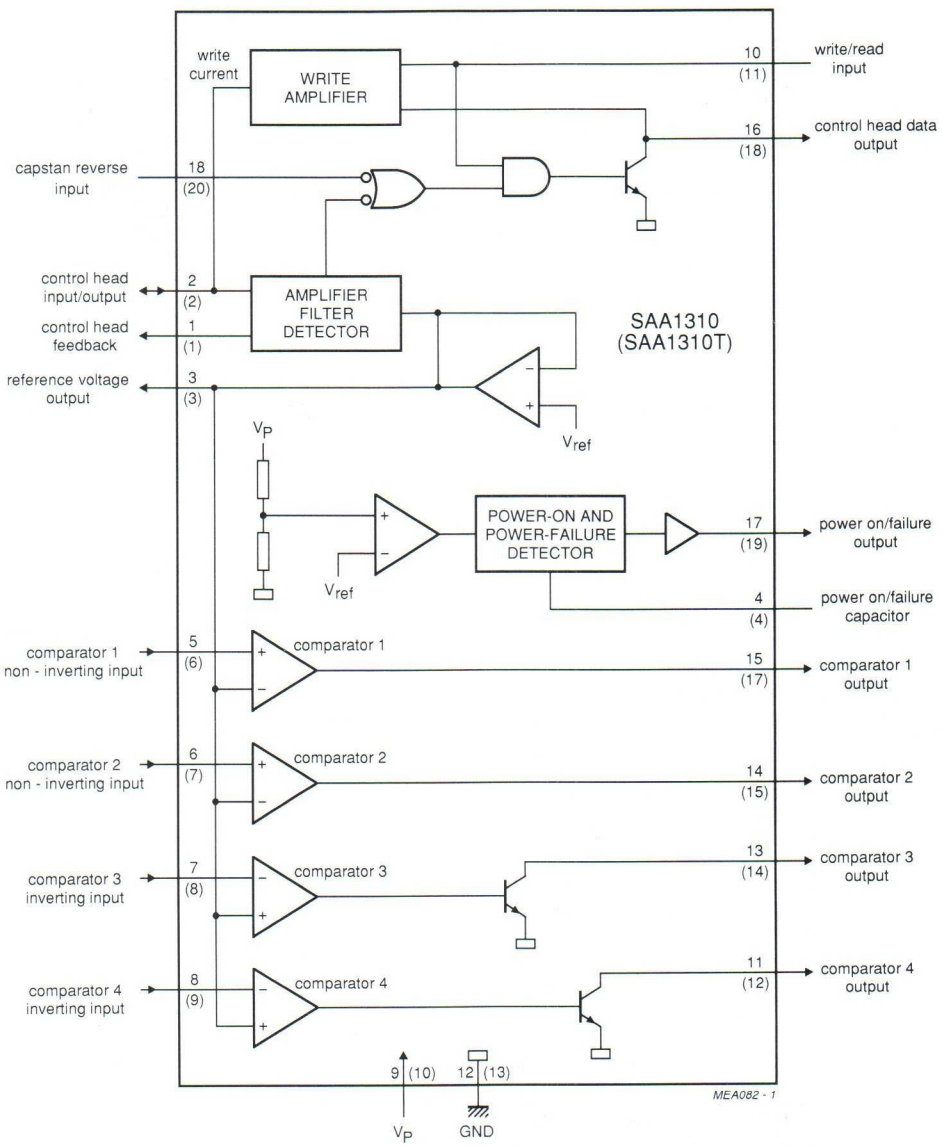
- Full support of VISS and VASS mode (VHS Index/Address Search System
- Read, write and overwrite of Tape Control/head signal (CTL)
- Power-ON and power-failure indicator
- 4 general purpose comparators for interface between sensors and microprocessor
- 2 comparators have a 100 mA output driver
- PAL and NTSC compatible

GENERAL DESCRIPTION

The SAA1310 provides an interface between the tape control head in the VHS deck-electronics.
The circuit also includes an interface between sensors in the deck mechanics and the microprocessor.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA1310	18	DIL	plastic	SOT102
SAA1310T	20	SO	plastic	SOT163A



Pin numbers in parenthesis refer to the SAA1310T.

Fig.1 Block diagram.

PIN CONFIGURATION

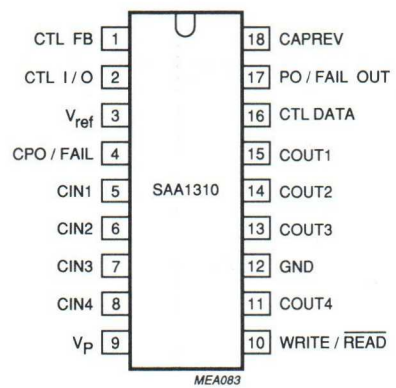


Fig.2 (a) Pin configuration for SAA1310.

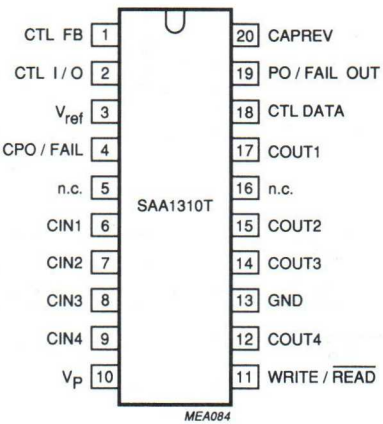


Fig.2 (b) Pin configuration for SAA1310T.

PINNING (pins in parenthesis refer to SAA1310T)

SYMBOL	PIN	DESCRIPTION
CTL FB	1 (1)	control head feedback
CTL I/O	2 (2)	control head input/output
V_{ref}	3 (3)	reference voltage output
CPO/FAIL	4 (4)	power on/failure capacitor
CIN1	5 (6)	comparator 1 input
CIN2	6 (7)	comparator 2 input
CIN3	7 (8)	comparator 3 input
CIN4	8 (9)	comparator 4 input
V_P	9 (10)	supply voltage
WRITE/$\overline{READ}$	10 (11)	write/read input
COUT4	11 (12)	comparator 4 output
GND	12 (13)	ground
COUT3	13 (14)	comparator 3 output
COUT2	14 (15)	comparator 2 output
COUT1	15 (17)	comparator 1 output
CTL DATA	16 (18)	control head data output
PO/FAIL OUT	17 (19)	power on/failure output
CAPREV	18 (20)	capstan reverse input

LIMITING VALUES (pin numbers in parenthesis refer to SAA1310T)

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage range		0	6.0	V
V_I/V_O	voltage on all pins	except pins 11 (12) and 13 (14)	0	V_P	V
V_O	output voltage on pins 11 (12) and 13 (14)		0	18	V
T_{stg}	storage temperature range		–65	+150	°C
T_{amb}	ambient temperature range		0	+70	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
R_{th}	thermal resistance (SAA1310)	75	-	K/W
R_{th}	thermal resistance (SAA1310T)	90	-	K/W

CHARACTERISTICS (pin numbers in parenthesis refer to SAA1310T)

V_P = 5 V; T_{amb} = 25 °C; all voltage referenced to pin 12 (13); according to the test set-up (see Fig.4); unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
P_d	power dissipation	note 1	-	85	-	mW
Supply pin 9 (10)						
V_P	supply voltage		4.5	5.0	5.5	V
I_P	supply current	read mode	10	15	20	mA
		write mode; duty factor = 50%	13	18	24	mA
CTL I/O pin 2 (2)						
READ MODE PIN 10 (11) < 0.5 V						
V_I	input voltage (peak-to-peak value)	f = 500 Hz	0.35	-	-	mV
		f = 30 kHz; non-linear operation	-	-	200	mV
B	bandwidth low-pass filter		-	3	-	kHz
I_b	input bias current	read mode	-	0.1	-	µA
WRITE MODE PIN 10 (11) > 3.5 V						
V_O	output voltage LOW	$I_{CTL\ I/O}$ = 3 mA; pin CTL DATA = HIGH	-	-	0.4	V
V_O	output voltage HIGH	$I_{CTL\ I/O}$ = −3 mA; pin CTL DATA = LOW	4.6	-	-	V
WRITE/READ pin 10 (11)						
V_I	input voltage	read mode	-	-	0.5	V
		write mode; analog	1.6	-	3.3	V
I_I	input current	read mode	-	-1.5	-	µA
		write mode	-	0.1	-	µA
V_{ref} pin 3 (3); note 2						
V_O	output voltage		2.4	2.5	2.6	V
I_{tot}	total current	including write current	−4	-	+4	mA
R_O	output resistance		-	0.4	0.6	Ω
CAPREV pin 18 (20)						
V_{IH}	input voltage HIGH		2.0	-	-	V
V_{IL}	input voltage LOW		-	-	0.8	V
I_{IH}	input current HIGH	V_{CAPREV} = 5 V	-	-	10	µA
I_{IH}	input current LOW	V_{CAPREV} = 0 V	−10	-	-	µA
CTL DATA pin 16 (18)						
WRITE MODE						
V_{IH}	input voltage HIGH		2.0	-	-	V
V_{IL}	input voltage LOW		-	-	0.8	V
I_{IH}	input current HIGH	$V_{CTL\ DATA}$ = 5 V	-	-	10	µA
I_{IL}	input current LOW	$V_{CTL\ DATA}$ = 0 V	−10	-	-	µA
READ MODE						
V_{OL}	output voltage LOW	I_{OL} = 0.5 mA	-	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −50 µA	2.4	-	-	V

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
CPO/FAIL and PO/FAIL OUT pin 4 (4) and 17 (19); see Fig.3						
V_O	operating voltage range	at decreasing V_P	1.5	-	5.5	V
V_{OL}	output voltage LOW	I_{OL} = 1 mA	-	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −1 mA	V_P−0.9	-	-	V
t_d	delay time	C_{CAPREV} = 68 nF	-	50	-	ms
V_{TL1}	threshold level 1		4.5	-	4.8	V
V_{TL2}	threshold level 2		-	3.5	-	V
I_O	source current pin 4		-	−3	-	μA
I_O	sink current pin 4		-	300	-	μA
$V_{O(min.)}$	minimum output voltage		-	20	-	mV
$V_{O(max.)}$	maximum output voltage		-	2.1	-	V
High output current type comparators						
CIN3 and CIN4 pins 7 (8) and 8 (9)						
V_{hys}	input hysteresis		-	10	-	mV
V_{IL}	input voltage LOW		-	-	V_{ref} −10 mV	V
V_{IH}	input voltage HIGH		V_{ref} +10 mV	-	-	V
I_{IL}	input current LOW	CIN3 = CIN4 = 0 V	−1	-	-	μA
I_{IH}	input current HIGH	CIN3 = CIN4 = V_P	-	-	+1	μA
COUT3 and COUT4 pins 13 (14) and 11 (12)						
V_{OL}	output voltage LOW	I_{OL} = 100 mA I_{OL} = 2 mA	- -	- -	1.0 0.4	V V
$\pm I_{OL}$	leakage current	output voltage HIGH; COUT3 = COUT4 = 17 V	-	-	1	μA
t_{tr}	transient time	note 3	-	0.5	-	μs
T_j	thermal protection		-	130	-	°C
Low output current type comparators						
CIN1 AND CIN2 pins 5 (6) and 6 (7)						
V_{hys}	input hysteresis		-	10	-	mV
V_{IL}	input voltage LOW		-	-	V_{ref} −10 mV	V
V_{IH}	input voltage HIGH		V_{ref} +10 mV	-	-	V
I_I	input current	CIN1 = CIN2 = 0 V CIN1 = CIN2 = V_P	−1 -	- -	- +1	μA μA
COUT1 AND COUT2 pins 15 (17) and 14 (15)						
V_{OL}	output voltage HIGH	I_{OH} = −100 μA	4.5	-	-	V
V_{OH}	output voltage LOW	I_{OL} = 2 mA	-	-	1	V
t_{tr}	transient time	note 4	-	0.5	-	μs

Notes to the characteristics

1. Without the sink current of the comparators; in write mode.
2. Minimum value of capacitor connected to this pin is 4.7 μF.
3. V_i = 100 mV p-p. Inputs connected to V_{ref} via a 10 kΩ resistor; outputs connected to V_P via a 250 Ω resistor.
4. V_i = 100 mV p-p. Inputs connected to V_{ref} via a 10 kΩ resistor; outputs connected to V_P via a 2.5 kΩ resistor.

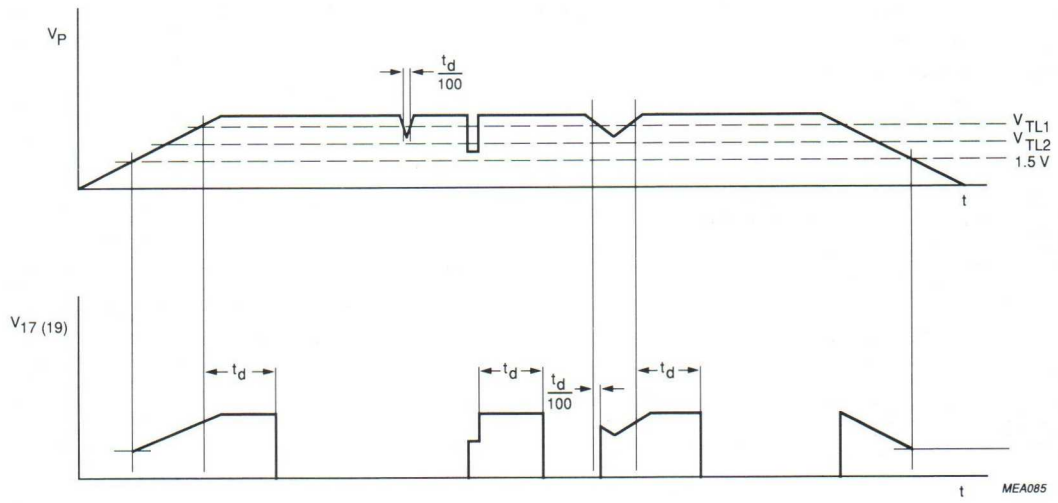


Fig.3 Power-ON and power-failure detector.

APPLICATION INFORMATION

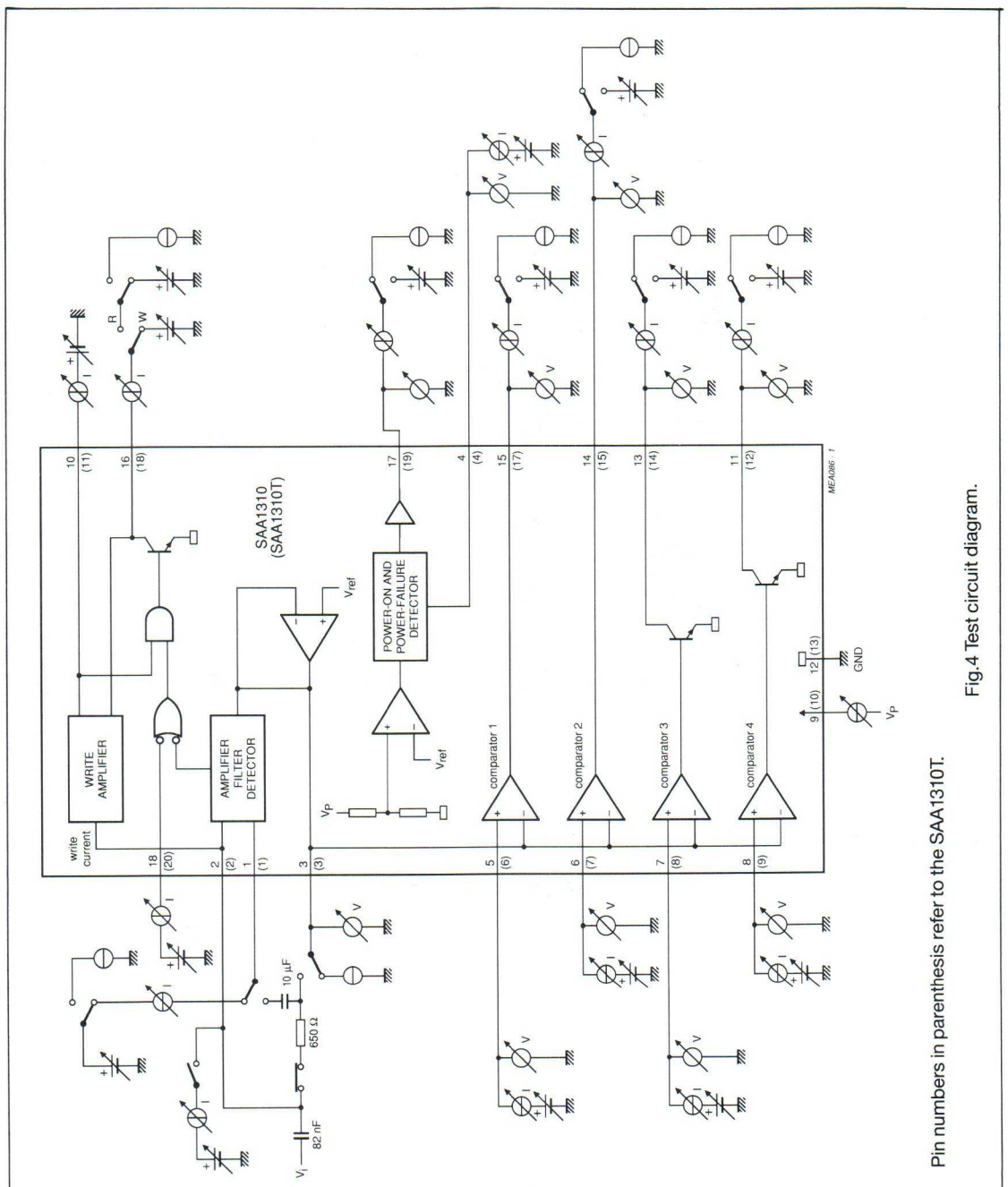
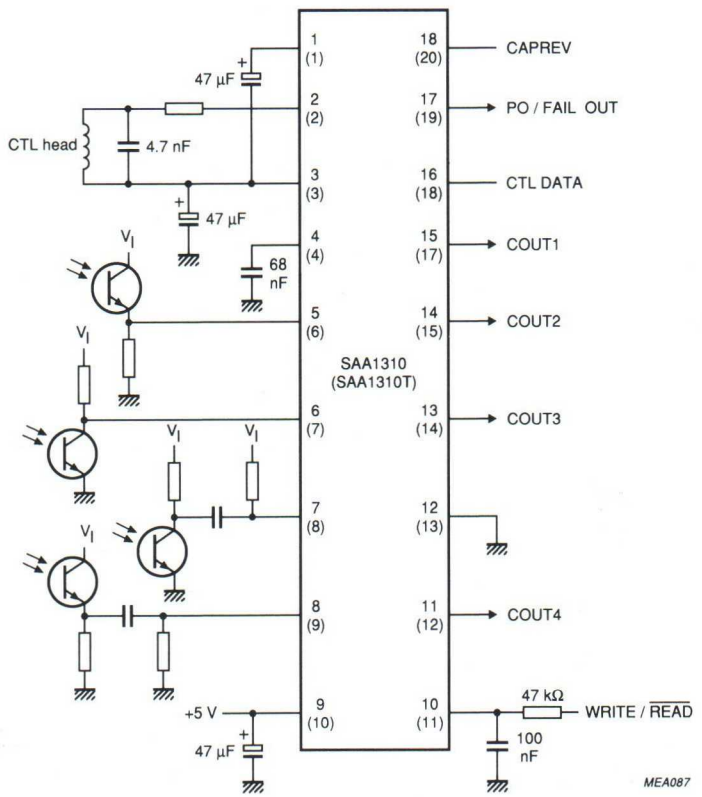


Fig.4 Test circuit diagram.

Pin numbers in parenthesis refer to the SAA1310T.

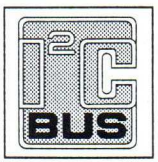


Pin numbers in parenthesis refer to the SAA1310T.

Fig.5 Application diagram.

D2MAC video decompression and descrambling

SAA1760



FEATURES

- Dual energy dispersal cancellation and video clamping for MAC satellite and Cable application
- On-chip video analog-to-digital converter
- 4 : 3 or 16 : 9 aspect ratio modes with panning
- Single or double cut rotation descrambling
- Digital YUV filters and DACs. Filter bandwidths selectable. Compatible with 100% saturated colours
- External YUV input with analog switching for "daisy chaining"
- On-chip MAC clock/data recovery with minimum external components
- Programmable delays for external filter compensation
- Sync outputs for YUV matrix, PAL/SECAM encoders and teletext decoders
- Output port (6-bits) for peripheral chip control
- PLCC68 package

GENERAL DESCRIPTION

The SAA1760 provides video decompression/descrambling and clock/data recovery functions of the Philips 2-chip MAC decoder. It provides two YUV outputs (analog luminance and chrominance) derived by decompressing and, if required, descrambling a baseband D2MAC signal. An analog YUV input is provided for multiplexing MAC and another YUV source on one of the two YUV outputs. These YUV outputs are intended for direct connection to YUV/RGB matrix chips or PAL/SECAM encoders.

The SAA1760 has an on-chip clock and data recovery sub-system implementing all functions of an analog gated phase-locked loop except for (external) loop filter and 20.25 MHz crystal components. D2MAC clock and data pins are provided for connection to the SAA1770 chip which extracts line and field synchronizing data for the chip set.

The SAA1760 is programmed (configured) by CDATA input which is supplied from the SAA1770 chip. This input specifies, for example, the video aspect ratio (4 : 3; 16 : 9), descrambling mode, descrambler control word, filter set-up and programmable delay compensation for external filters. The device also outputs bit error rate data on the CDATA pin.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5	5.5	V
I_{DD}	supply current	–	–	200	mA
f_{xtal}	oscillator frequency	20.248	20.25	20.252	MHz
T_{amb}	operating ambient temperature	0	–	70	°C
Vbw	video bandwidth (±3 dB)	–	5.5	–	MHz

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA1760	68	PLCC	plastic	SOT188CG

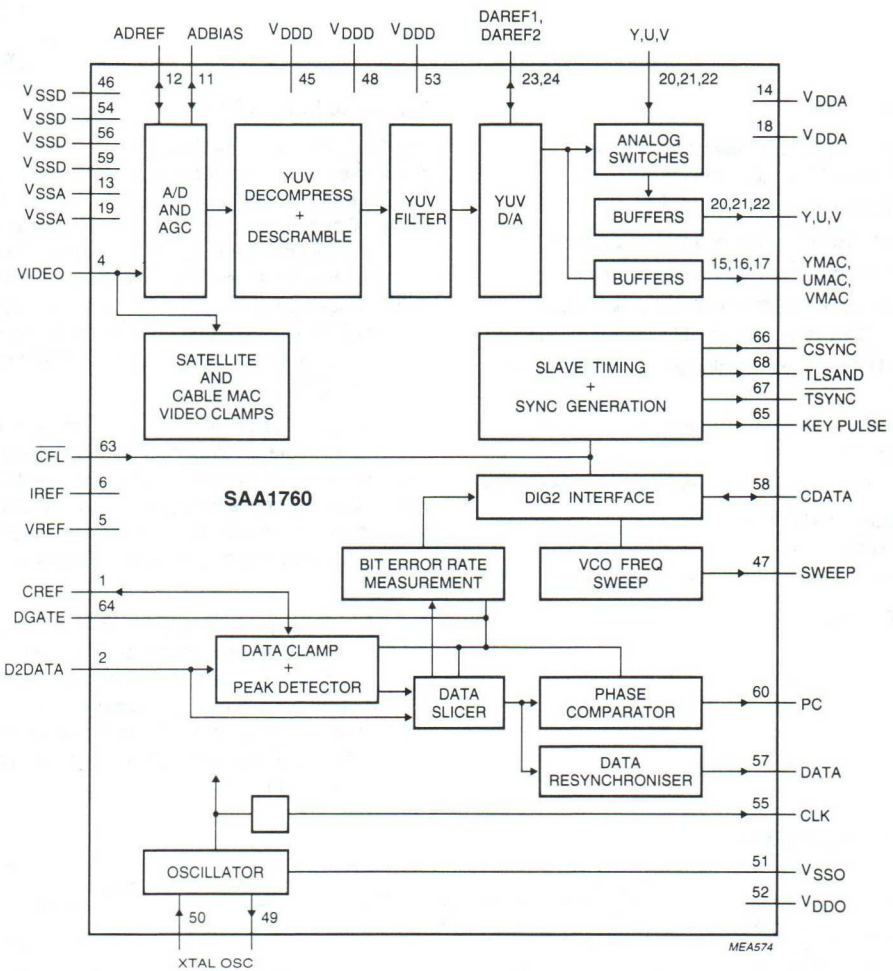


Fig.1 Block diagram.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

PINNING

SYMBOL	PIN	DESCRIPTION
CREF	1	data burst positive peak voltage storage pin. Connected to V_{SSA} via a capacitor
D2DATA	2	analog D2MAC data input. Nominal baseband signal with 800 mV peak-to-peak data burst. Input AC coupled for clamping/energy dispersal cancellation
i.c.	3	internally connected. Connect to ground for normal use
VIDEO	4	analog D2MAC baseband video input. 1 V black-to-white. Input must be AC coupled for clamping and energy dispersal cancellation
VREF	5	connection for external capacitor decoupling internal master reference voltage
IREF	6	connection for resistor defining master reference current
n.c.	7-10	not connected
ADBIAS	11	connection for ADC bias voltage decoupling capacitor
ADREF	12	connection for ADC reference voltage decoupling capacitor
V_{SSA}	13	0 V analog ground
V_{DDA}	14	+5 V supply to analog parts of chip
YMAC	15	analog luminance output. Nominally 1 V black-to-white always derived from MAC video input. Output impedance <300 Ω
VMAC	16	analog chrominance output –(R–Y). Nominally 1.05 V peak-to-peak. Output can be inverted to give (R–Y). Output impedance <300 Ω
UMAC	17	analog chrominance output –(B–Y). Nominally 1.33 V peak-to-peak. Output can be inverted to give (B–Y). Output impedance <300 Ω
V_{DDA}	18	+5 V supply to analog parts of chip
V_{SSA}	19	0 V analog ground
Y	20	analog luminance output. Nominally 1 V or 0.315 V black-to-white when Y output is derived from a MAC video input. Output level is programmable from the SAA1770. Alternatively this output corresponds to the signal on the YIN pin. Output impedance <300 Ω
V	21	analog chrominance output –(R–Y). Nominally 1.05 V peak-to-peak. Output can be inverted to give (R–Y) if derived from the MAC video input of this chip. Alternatively this output corresponds to the signal on the VIN pin. Output impedance <300 Ω
U	22	analog chrominance output –(B–Y). Nominally 1.33 V peak-to-peak. Output can be inverted to give (B–Y) if derived from the MAC video input of this chip. Alternatively this output corresponds to the signal on the UIN pin. Output impedance <300 Ω
DAREF2	23	connection for external capacitor used to store lower reference voltage for the YUV digital-to-analog converters
DAREF1	24	connection for external capacitor used to store upper reference voltage for the YUV digital-to-analog converters
YIN	25	analog luminance input. For (AC coupled) connection of external Y signal to on-chip analog switch
n.c.	26-29	not connected

SYMBOL	PIN	DESCRIPTION
UIN	30	analog chrominance input. For (AC coupled) connection of external U (B–Y) signal to on-chip analog switch. Signals on this pin cannot be inverted before output on pin U
VIN	31	analog chrominance input. For (AC coupled) connection of external V (R–Y) signal to on-chip analog switch. Signals on this pin cannot be inverted before output on pin V
P5, P4	32, 33	digital output port pins. These pins are programmable via the CDATA input
F	34	digital field rate timing signal. HIGH for odd-numbered fields. Changes state near the start of the video input line 1
L	35	digital line rate timing signal. HIGH for odd-numbered lines. Changes state near the start of every video input line
P3, P2, P1, P0	36-39	digital output port pins. These pins are programmable via the CDATA input
i.c.	40	internally connected. Connect to ground for normal operation
i.c.	41	internally connected. Connect to ground for normal operation
n.c.	42-44	not connected
V_{DDD}	45	+5 V supply to the digital parts of the chip
V_{SSD}	46	0 V digital ground
SWEEP	47	3-state digital output. A low frequency square wave can be output on this pin. Intended for assisting the clock/data recovery PLL to lock
V_{DDD}	48	+5 V supply to digital parts of chip
OSC	49	20.25 MHz oscillator output. Connection for external component network
XTAL	50	connection for 20.25 MHz crystal
V_{SSO}	51	0 V oscillator ground
V_{DDO}	52	+5 V supply for oscillator
V_{DDD}	53	+5 V supply to digital parts of chip
V_{SSD}	54	0 V digital ground
CLK	55	20.25 MHz clock. Waveform and amplitude chosen for EMC compatibility
V_{SSD}	56	0 V digital ground
DATA	57	digital binary output recovered from duo-binary D2DATA MAC data input; 10.125 Mbits/s.
CDATA	58	digital configuration data input/output. Open drain in output mode. Used by SAA1770 to control programmable features and provide video descrambler information (control words and frame-count). Also used to transmit bit error rate and AGC information from SAA1760 to SAA1770.
V_{SSD}	59	0 V digital ground
PC	60	3-state digital phase comparator output. When the chip set is locked to a MAC signal this pin is active only during data bursts on each line. Always active if chip set is out of lock.

SYMBOL	PIN	DESCRIPTION
n.c.	61	not connected
i.c.	62	internally connected. Connect to +5 V for normal operation
$\overline{CFL}$	63	digital combined field and line rate synchronizing signal from SAA1770
DGATE	64	digital MAC data burst gating signal from SAA1770. Used for data peak detector gating and phase-locked-loop gating. Active HIGH during data burst or when chip set is out of lock
KEYPULSE	65	active HIGH/LOW programmable line rate pulse output. Can be programmed to start or stop on any sample number. Intended for additional video clamping or as data burst marker for AFC gating
$\overline{CSYNC}$	66	digital negative-going composite sync. The line start time relative to the MAC YUV outputs is programmable for PAL/SECAM encoder/decoder delay compensation
$\overline{TSYNC}$	67	digital composite sync with reduced number of broad pulses and no equalizing pulses. Intended for use with teletext decoders capable of acquiring text on lines 2 to 5 and 315 to 317; i.e. lines normally containing broad or equalizing pulses
TLSAND	68	digital 3-state output. Used with external resistor network to obtain two-level sandcastle pulse for YUV/RGB matrix chips

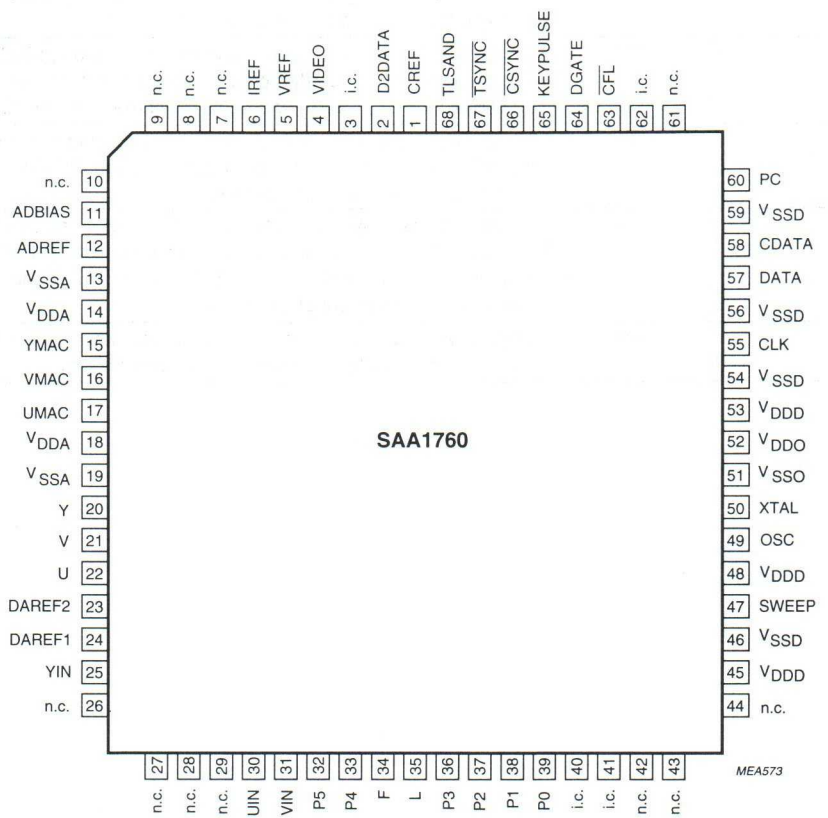


Fig.2 Pin configuration

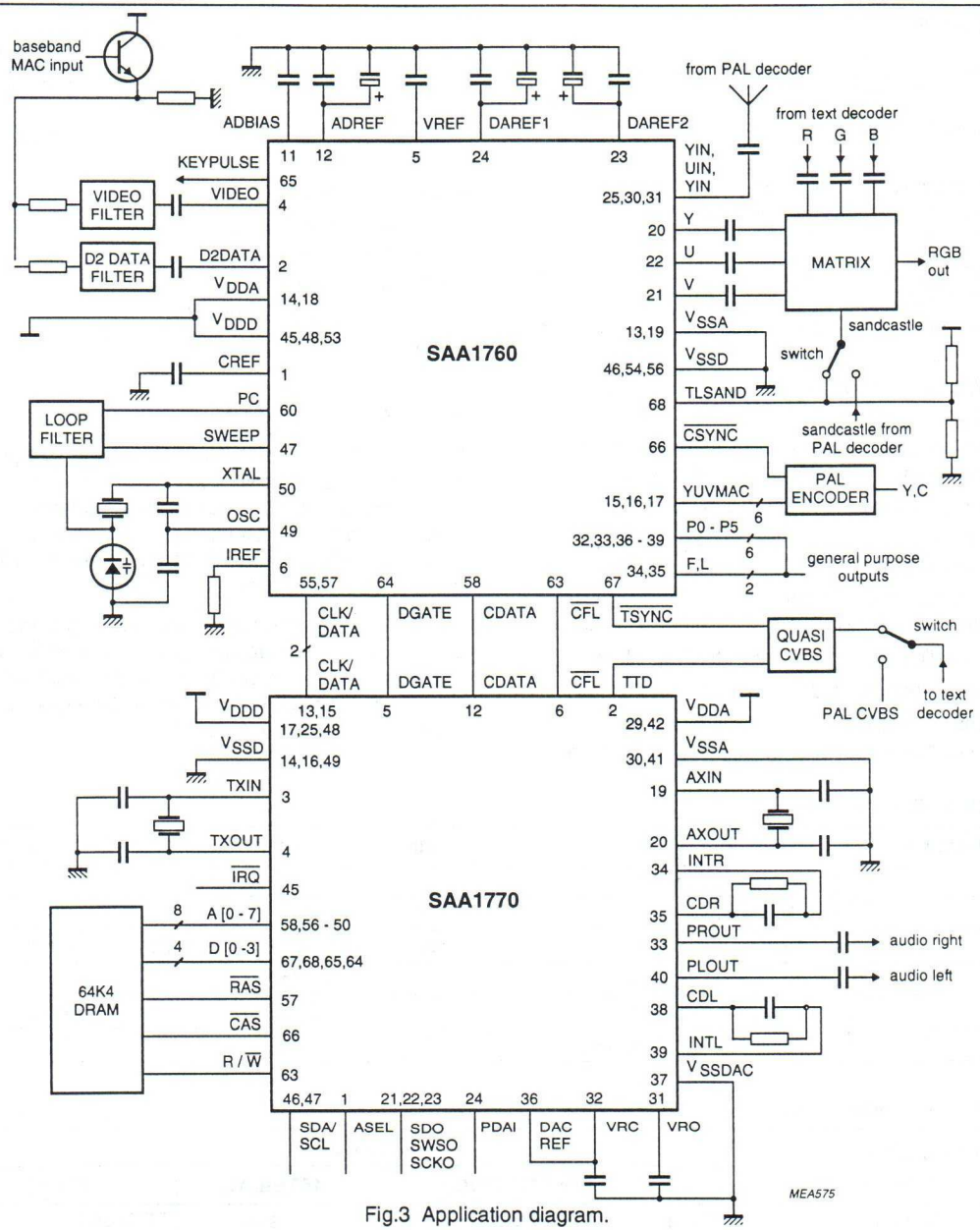


Fig.3 Application diagram.

D2MAC digital MAC packet SAA1770

FEATURES

- Spectrum descrambling and de-interleaving of one 99-bit wide sub-frame
- Full field capability, sub-frame can start anywhere on line 1
- VBI and packet teletext acquisition, frequency converted to output compatible with WST teletext decoders
- Processing of line 625 SDF and RDF with automatic pan vector extraction
- De-scrambling of packets. Four independent packet de-scramblers
- Golay decoding of packet headers and contents where required
- Two independent packet '0' data group acquisition "buffers" with automatic 3-way majority voting
- Four, 8-packet buffers for EMM acquisition
- Four, 16-packet buffers for general purpose (ECM, EMM, data) acquisition
- Three sound acquisition channels decoding any coding schemes in the EBU MAC/packet specification.
- Automatic sound configuration by B1 packets
- Two programmable digital sound mixers
- Primary analog sound output - one bit DACs and J17 de-emphasis on-chip. Also available in DAI format
- Secondary sound output in I²S-format
- Error concealment plus interpolation of sound samples
- Buffering of all received packets using a single external 64K4 DRAM
- I²C-bus control up to 400 kHz
- PLCC68 package

GENERAL DESCRIPTION

The SAA1770 is a D2MAC digital component acquisition and processing device which forms part of the Philips Semiconductors 2nd generation MAC decoder chip set. It accepts clock and data from a D2MAC source and performs all line 625 and sub-frame processing required for normal tv applications.

The SAA1770 synchronizes to the incoming data stream using the line sync words and provides timing for the chip set. It is programmed (configured) by an I²C-bus. The I²C-bus also used to program the SAA1760 via the CDATA output from the SAA1770.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5	5.5	V
I_{DD}	supply current	–	–	200	mA
f_{xtal}	oscillator frequency	20.248	20.25	20.252	MHz
f_{TXT}	teletext crystal frequency	–	6.3975	–	MHz
f_{SND}	sound crystal frequency	–	8.192	–	MHz
T_{amb}	operating ambient temperature	0	–	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA1770	68	PLCC	plastic	SOT188CG

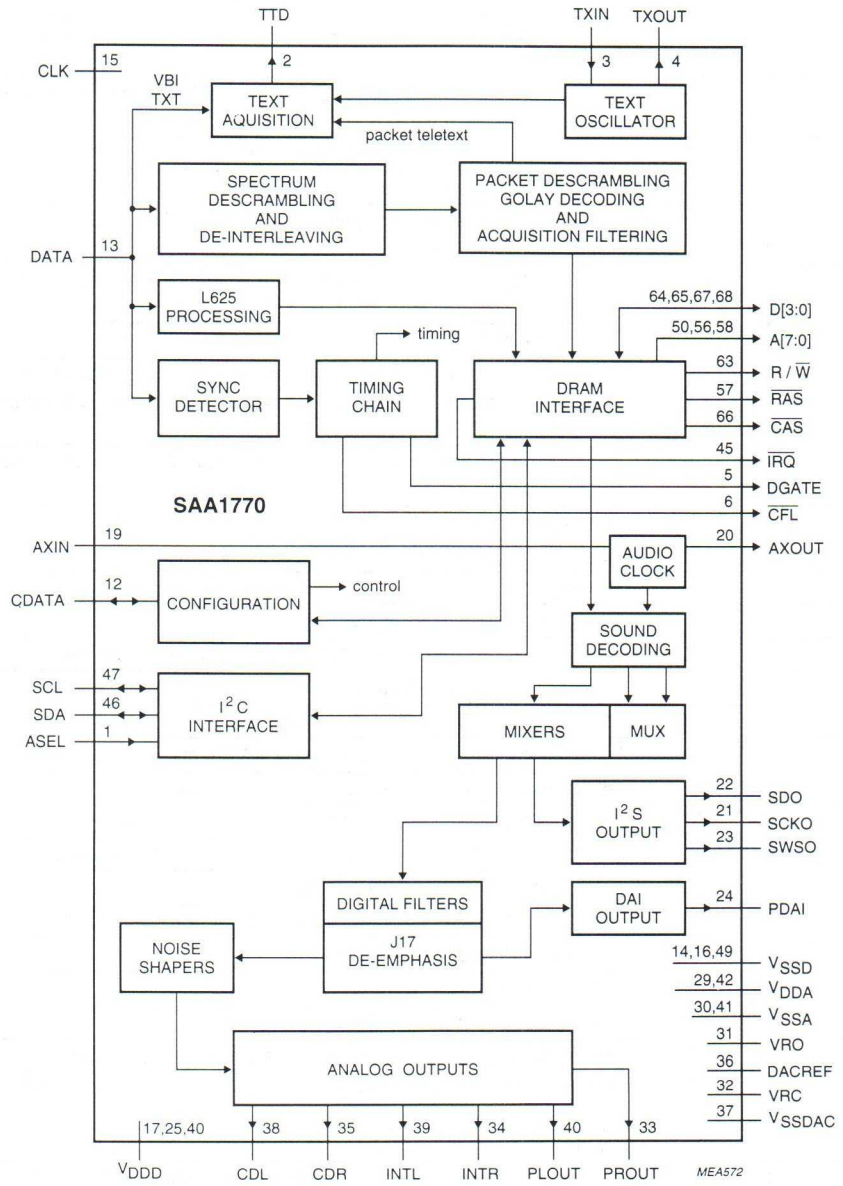


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
ASEL	1	digital input. I²C-bus address select. Selects one of two possible I²C-bus addresses
TTD	2	digital output. Teletext data output at 6.9375 Mb/s rate from VBI or packet teletext with clock run-in and framing code added
TXIN	3	connection for 6.9375 MHz teletext crystal
TXOUT	4	connection for 6.9375 MHz teletext crystal
DGATE	5	digital output. Data gate signal to SAA1760 marks data burst for PLL and data slicer gating etc.
$\overline{CFL}$	6	digital output. Composite field and line timing for synchronizing the SAA1760. Also synchronizes CDATA pin transfers
n.c.	7-11	not connected
CDATA	12	digital input/output. Configuration data to SAA1760 strobed by field timing events on the $\overline{CFL}$ signal. Also used to receive bit error rate information from SAA1760
DATA	13	digital input. Sliced and re-synchronized D2MAC data input from SAA1760 (10.125 Mb/s)
V_{SSD}	14	0 V digital ground
CLK	15	digital input. 20.25 MHz input clock from SAA1760
V_{SSD}	16	0 V digital ground
V_{DDD}	17	+5 V supply to digital parts of chip
i.c.	18	internally connected. Connect to ground for normal operation
AXIN	19	connection for 8.192 MHz sound crystal
AXOUT	20	connection for 8.192 MHz sound crystal
SCKO	21	digital output. Secondary sound output I²S-clock
SDO	22	digital output. Secondary sound output I²S-data
SWSO	23	digital output. Secondary sound output I²S-word select
PDAI	24	DAI output. Primary sound output in DAI format, J17 de-emphasized
V_{DDD}	25	+5 V supply to digital parts of chip
i.c.	26-28	internally connected. Connect to ground for normal operation
V_{DDA}	29	+ 5 V supply to analog parts of chip
V_{SSA}	30	0 V analog ground
VRO	31	voltage reference output for DACs
VRC	32	connection for DAC voltage reference decoupling capacitor
PROUT	33	analog output. Primary sound output right channel, J17 de-emphasized analog bit stream
INTR	34	connection to filter/integrator for right primary sound output
CDR	35	connection to external damping network for right sound output
DACREF	36	voltage reference input for DACs
V_{SSDAC}	37	ground for audio DACs
CDL	38	connection to external damping network for left sound output

SYMBOL	PIN	DESCRIPTION
INTL	39	connection to filter/integrator for left primary sound channel
PLOUT	40	analog output. Primary sound output left channel, J17 de-emphasized analog bit stream
V_{SSA}	41	0 V analogue ground
V_{DDA}	42	+5 V supply to analog parts of chip
n.c.	43	not connected
i.c.	44	internal connection. Connect to ground for normal operation
$\overline{IRQ}$	45	digital output. Open drain interrupt request. Active LOW signal indicating service request. Data available e.g. in packet buffers
SDA	46	digital input/output. I²C-400 kHz serial interface data. Slave receiver for controlling chip set and reading data
SCL	47	digital input/output. I²C-400 kHz serial interface clock. This pin is an output when SAA1760 "stretches" the clock
V_{DDD}	48	+5 V supply to digital parts of chip
V_{SSD}	49	0 V digital ground
A7	50	digital output. Address bus for external 64K4 DRAM
A4	51	digital output. Address bus for external 64K4 DRAM
A3	52	digital output. Address bus for external 64K4 DRAM
A5	53	digital output. Address bus for external 64K4 DRAM
A2	54	digital output. Address bus for external 64K4 DRAM
A6	55	digital output. Address bus for external 64K4 DRAM
A1	56	digital output. Address bus for external 64K4 DRAM
$\overline{RAS}$	57	digital output. Row address strobe for external 64K4 DDRAM
A0	58	digital output. Address bus for external 64K4 DRAM
n.c.	59-62	not connected
R/$\overline{W}$	63	digital output. Read/Write signal for external 64K4 DRAM
D2	64	digital input/output. Data bus for external 64K4 DRAM
D1	65	digital input/output. Data bus for external 64K4 DRAM
$\overline{CAS}$	66	digital output. Column address strobe for external 64K4 DRAM
D0	67	digital input/output. Data bus for external 64K4 DRAM
D3	68	digital input/output. Data bus for external 64K4 DRAM

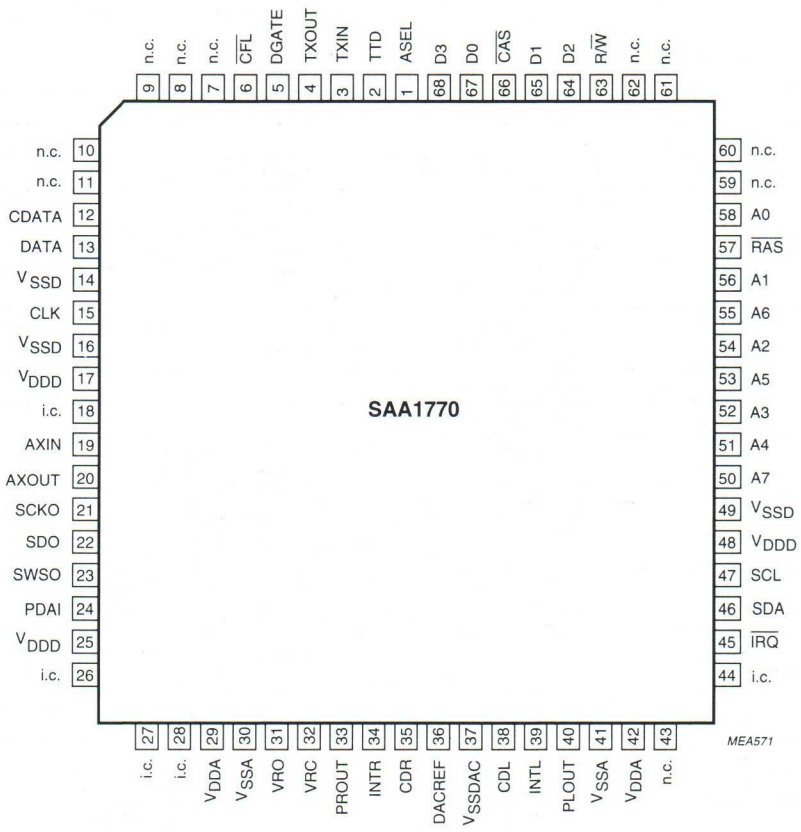


Fig.2 Pin configuration

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

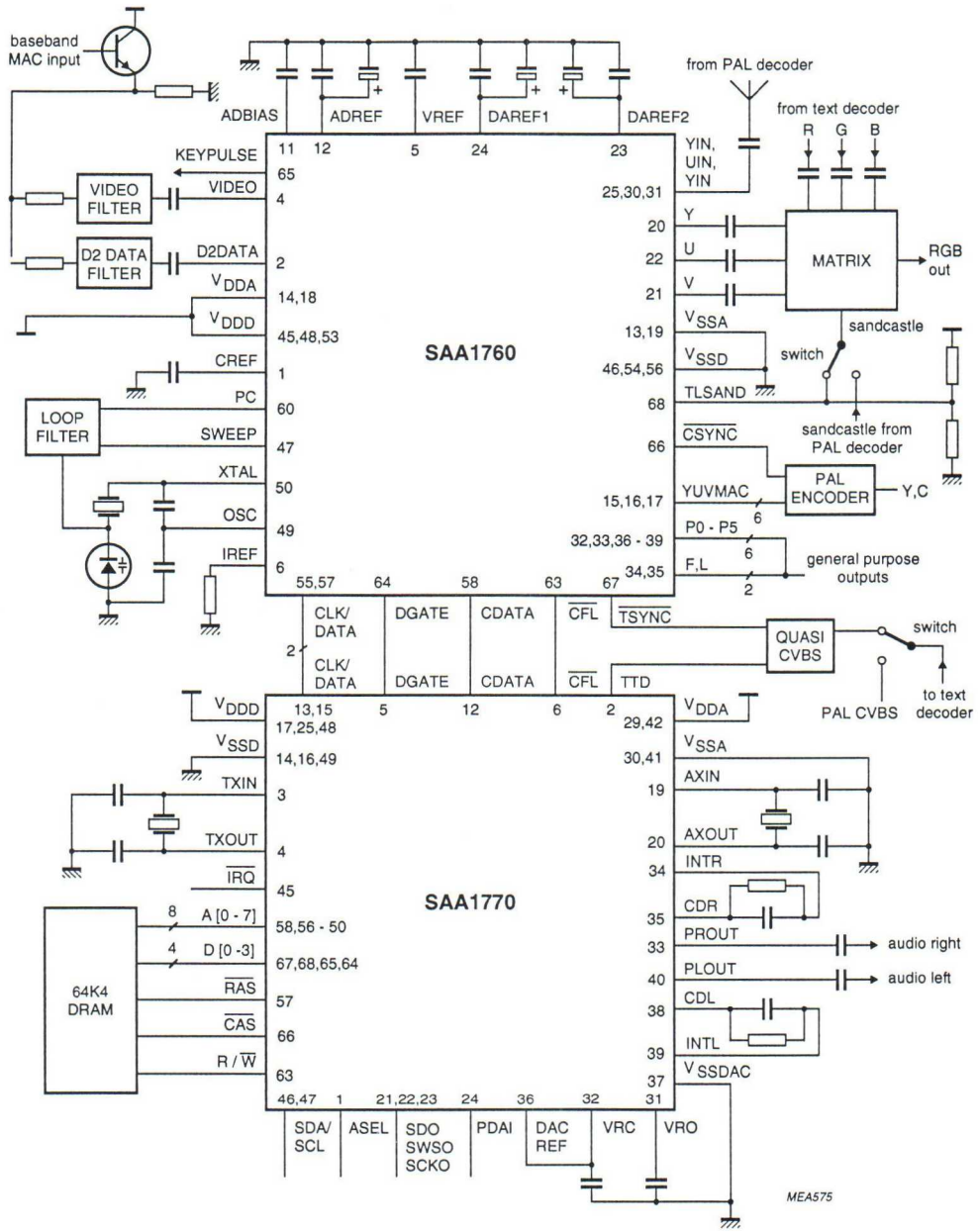


Fig.3 Application diagram.

REMOTE CONTROL TRANSMITTER

GENERAL DESCRIPTION

The SAA3004 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The SAA3004 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

The SAA3004 has the following features:

- Flashed or modulated transmission
- 7 sub-system addresses
- Up to 64 commands per sub-system address
- High-current remote output at V_{DD} = 6 V ($-I_{OH}$ = 40 mA)
- Low number of additional components
- Key release detection by toggle bits
- Very low stand-by current ($< 2\ \mu A$)
- Operational current < 2 mA at 6 V supply
- Wide supply voltage range (4 to 11 V)
- Ceramic resonator controlled frequency (typ. 450 kHz)
- Encapsulation: 20-lead plastic DIL or 20-lead plastic mini-pack (SO-20)

PACKAGE OUTLINES

SAA3004P: 20-lead DIL; plastic (SOT146).
SAA3004T: 20-lead mini-pack; plastic (SO20; SOT163A).

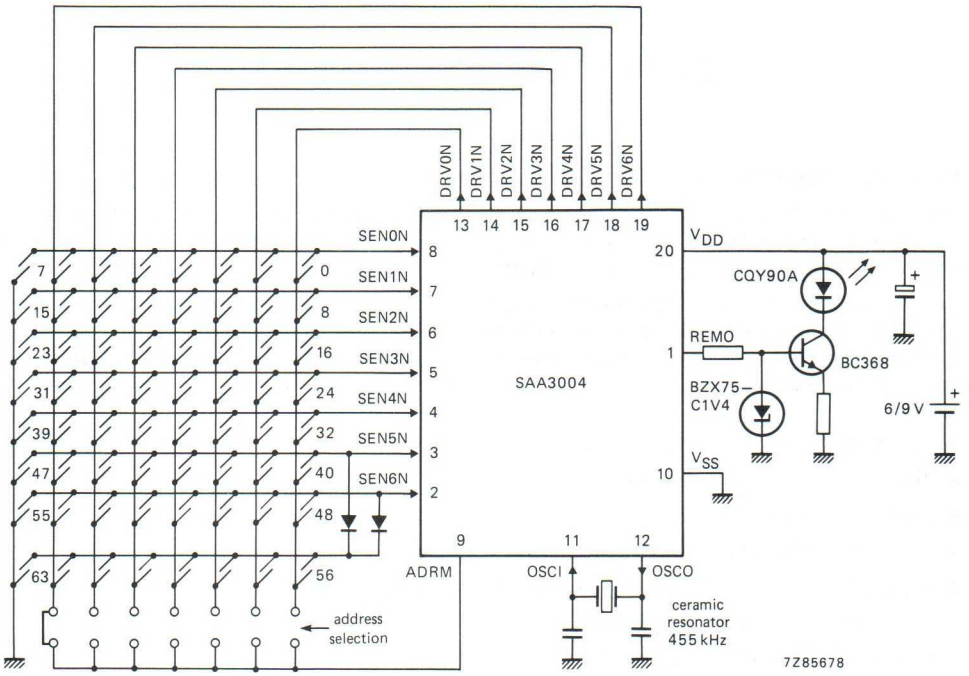


Fig. 1 Transmitter with SAA3004.

INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N)

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in Fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable.The sense inputs have P-channel pull-up transistors, so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

Address mode input (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode. This allows the definition of seven sub-system addresses as shown in Table 3. If driver DRV6N is connected to ADRM the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by presssing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnN with the highest number (n) defines the sub-system address, e.g. if driver DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in transmitters for more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4.

A change of the sub-system address will not start a transmission.

Remote control signal output (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in Tables 1 and 2.

The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see Fig. 3).

The format of the output data is given in Figs 2 and 3. In the flashed transmission mode the data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A, which are defined by the selected key.

In the modulated transmission mode the first toggle bit T1 is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence.

The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command.

The codes for the sub-system address and the selected key are given in Tables 3 and 4.

Oscillator input/output (OSCI and OSCO)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 400 kHz and 500 kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation

In the stand-by mode all drivers (DRV0N to DRV6N) are on. Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see Fig. 4) the output drivers (DRV0N to DRV6N) become active successively.

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch. In contradiction to the command code the sub-system address is sensed only within the *first* scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key-stroke sequence (see Fig. 5) the command code is always altered in accordance with the sensed key.

Multiple key-stroke protection

The keyboard is protected against multiple key-strokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see Fig. 5). In case of a multiple key-stroke the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix:

FUNCTIONAL DESCRIPTION (continued)

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored.
- SEN5N and SEN6N are not protected against multiple key-stroke on the same driver line, because this condition has been used for the definition of additional codes (code numbers 56 to 63).

Output sequence (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in Figs 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see Fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

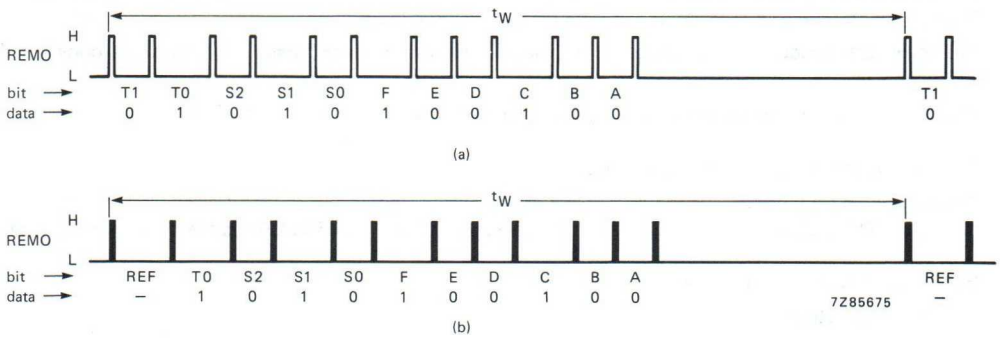
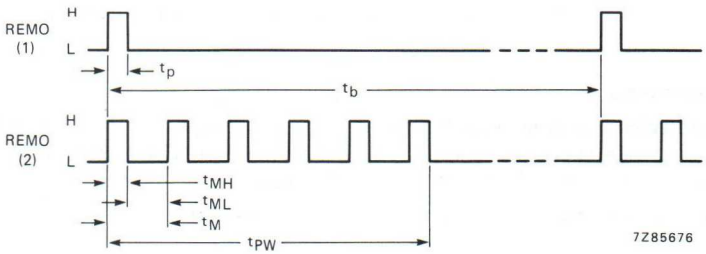


Fig. 2 Data format of REMO output; REF = reference time; T0 and T1 = toggle bits; S0, S1 and S2 = system address; A, B, C, D, E and F = command bits.
(a) flashed mode: transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed).
(b) modulated mode: transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).



(1) Flashed pulse.
(2) Modulated pulse ($t_{PW} = (5 \times t_M) + t_{MH}$.

Fig. 3 REMO output waveform.

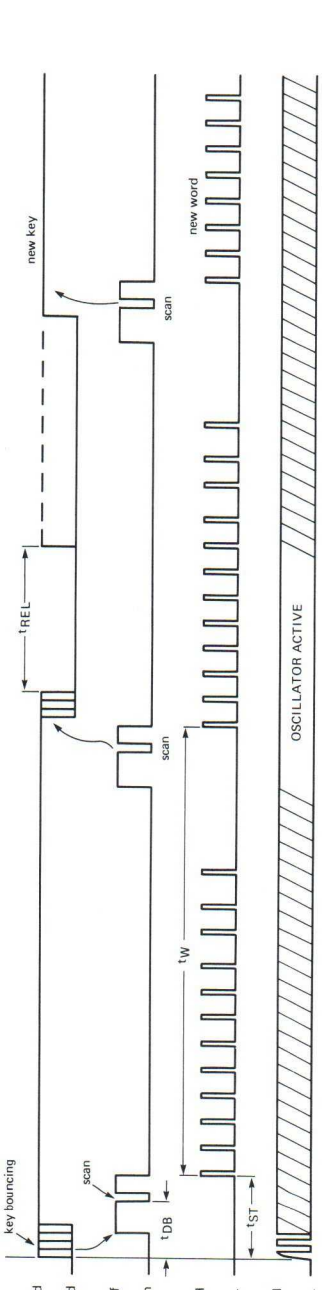


Fig. 4 Single key-stroke sequence.
Debounce time: t_{DB} = 4 to 9 x T_O.
Start time: t_{ST} = 5 to 10 x T_O.
Minimum release time: t_{REL} = T_O.
Word distance: t_W.

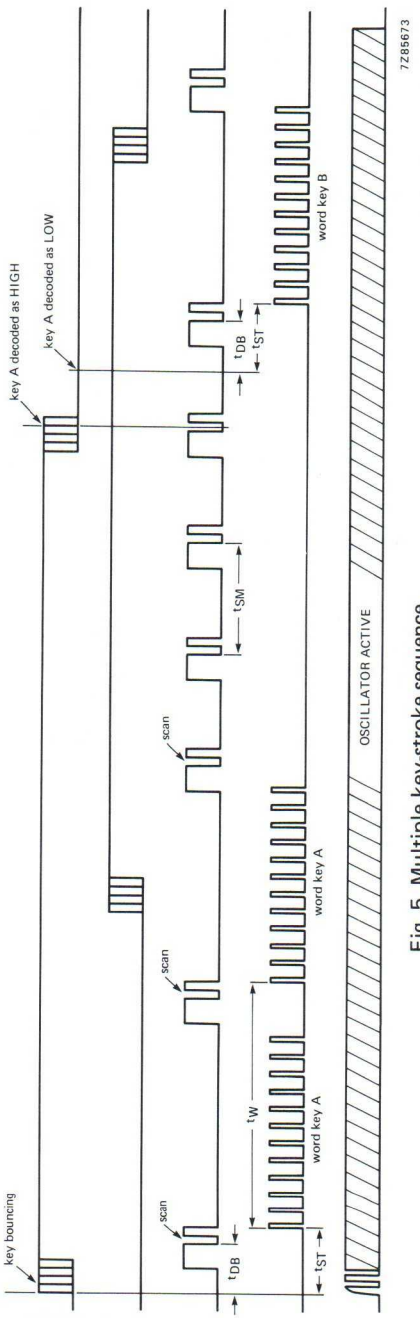


Fig. 5 Multiple key-stroke sequence.
Scan rate multiple key-stroke: t_{SM} = 6 to 10 x T_O.
For t_{DB}, t_{ST} and t_W see Fig. 4.

Table 1 Pulse train timing

mode	T_o ms	t_p μs	t_M μs	t_{ML} μs	t_{MH} μs	t_W ms
flashed	2,53	8,8	–	–	–	121
modulated	2,53	–	26,4	17,6	8,8	121

f_{osc}	455 kHz	$t_{osc} = 2{,}2\ \mu s$
t_p	$4 \times t_{osc}$	flashed pulse width
t_M	$12 \times t_{osc}$	modulation period
t_{ML}	$8 \times t_{osc}$	modulation period LOW
t_{MH}	$4 \times t_{osc}$	modulation period HIGH
T_o	$1152 \times t_{osc}$	basic unit of pulse distance
t_W	$55\,296 \times t_{osc}$	word distance

Table 2 Pulse train separation (t_b)

code	t_b
logic "0"	$2 \times T_o$
logic "1"	$3 \times T_o$
reference time	$3 \times T_o$
toggle bit time	$2 \times T_o$ or $3 \times T_o$

Table 3 Transmission mode and sub-system address selection

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode.

mode	sub-system address				driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
F	0	1	1	1							
L	1	0	0	0	o						
A	2	0	0	1	X	o					
S	3	0	1	0	X	X	o				
H	4	0	1	1	X	X	X	o			
E	5	1	0	0	X	X	X	X	o		
D	6	1	0	1	X	X	X	X	X	o	
M											
O	0	1	1	1							o
D	1	0	0	0	o						o
U	2	0	0	1	X	o					o
L	3	0	1	0	X	X	o				o
A	4	0	1	1	X	X	X	o			o
T	5	1	0	0	X	X	X	X	o		o
E	6	1	0	1	X	X	X	X	X	o	o
D											

o = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 Key codes

matrix drive	matrix sense	code F	E	D	C	B	A	matrix position
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
*	SEN1N	0	0	1		**		8 to 15
*	SEN2N	0	1	0		**		16 to 23
*	SEN3N	0	1	1		**		24 to 31
*	SEN4N	1	0	0		**		32 to 39
*	SEN5N	1	0	1		**		40 to 47
*	SEN6N	1	1	0		**		48 to 55
*	SEN5N and SEN6N	1	1	1		**		56 to 63

* The complete matrix drive as shown above for SEN0N is also applicable for the matrix sense inputs SEN1N to SEN6N and the combined SEN5N/SEN6N.

** The C, B and A codes are identical to SEN0N as given above.

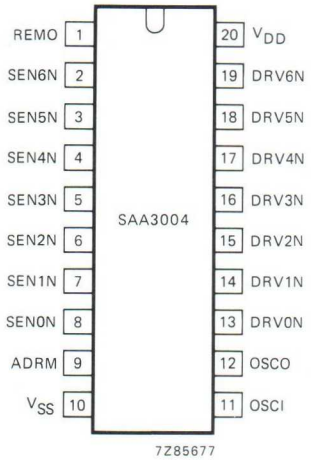


Fig. 6 Pinning diagram.

PINNING

1	REMO	remote data output
2	SEN6N	key matrix sense inputs
3	SEN5N	
4	SEN4N	
5	SEN3N	
6	SEN2N	
7	SEN1N	
8	SEN0N	
9	ADRM	address mode control input
10	V_{SS}	ground
11	OSCI	oscillator input
12	OSCO	oscillator output
13	DRV0N	key matrix drive outputs
14	DRV1N	
15	DRV2N	
16	DRV3N	
17	DRV4N	
18	DRV5N	
19	DRV6N	
20	V_{DD}	positive supply

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to +15		V
Input voltage range	V_I	−0,5 to V_{DD} +0,5		V
Output voltage range	V_O	−0,5 to V_{DD} +0,5		V
D.C. current into any input or output	±I	max.	10	mA
Peak REMO output current during 10 μs; duty factor = 1%	$-I_{(REMO)M}$	max.	300	mA
Power dissipation per package for T_{amb} = −20 to +70 °C	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}	−55 to +150		°C
Operating ambient temperature range	T_{amb}	−20 to +70		°C

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage T_{amb} = 0 to +70 °C	–	V_{DD}	4	–	11	V
Supply current; active f_{osc} = 455 kHz; REMO output unloaded	6 9	I_{DD} I_{DD}	– –	1 3	– –	mA mA
Supply current; inactive (stand-by mode) T_{amb} = 25 °C	6 9	I_{DD} I_{DD}	– –	– –	2 2	μA μA
Oscillator frequency (ceramic resonator)	4 to 11	f_{osc}	400	–	500	kHz
Keyboard matrix						
Inputs SEN0N to SEN6N						
Input voltage LOW	4 to 11	V_{IL}	–	–	0,2 x V_{DD}	V
Input voltage HIGH	4 to 11	V_{IH}	0,8 x V_{DD}	–	–	V
Input current V_I = 0 V	4 11	$-I_I$ $-I_I$	10 30	– –	100 300	μA μA
Input leakage current V_I = V_{DD}	11	I_I	–	–	1	μA
Outputs DRV0N to DRV6N						
Output voltage "ON" I_O = 0,1 mA I_O = 1,0 mA	4 11	V_{OL} V_{OL}	– –	– –	0,3 0,5	V V
Output current "OFF" V_O = 11 V	11	I_O	–	–	10	μA
Control input ADRM						
Input voltage LOW	–	V_{IL}	–	–	0,8 x V_{DD}	V
Input voltage HIGH	–	V_{IH}	0,2 x V_{DD}	–	–	V
Input current (switched P- and N-channel pull-up/ pull-down)						
Pull-up active stand-by voltage: 0 V	4 11	I_{IL} I_{IL}	10 30	– –	100 300	μA μA
Pull-down active stand-by voltage: V_{DD}	4 11	I_{IH} I_{IH}	10 30	– –	100 300	μA μA

CHARACTERISTICS (continued)

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Data output REMO						
Output voltage HIGH	6	V_{OH}	3	–	–	V
$-I_{OH}$ = 40 mA	9	V_{OH}	6	–	–	V
Output voltage LOW	6	V_{OL}	–	–	0,2	V
I_{OL} = 0,3 mA	9	V_{OL}	–	–	0,1	V
Oscillator						
Input current OSCI at V_{DD}	6	I_I	0,8	–	2,7	μA
Output voltage HIGH $-I_{OL}$ = 0,1 mA	6	V_{OH}	–	–	$V_{DD}-0,6$	V
Output voltage LOW I_{OH} = 0,1 mA	6	V_{OL}	–	–	0,6	V

INFRARED REMOTE CONTROL TRANSMITTER (RECS 80 LOW VOLTAGE)

GENERAL DESCRIPTION

The SAA3008 transmitter IC is designed for infrared remote control systems. It has a capacity for 1280 commands arranged in 20 sub-system address groups of 64 commands each. The subsystem address may be selected by press-button, slider switches or be hard-wired.

Commands are transmitted in patterns which are pulse distance coded. Modulated pulse transmissions allow a narrow-band receiver to be used for improved noise rejection. The modulation frequency of the SAA3008 is 38 kHz which is 1/12 of the oscillator frequency of 455 kHz (typical).

Features

- Modulated transmission
- Ceramic resonator controlled frequency
- Data-word-start with reference time of unique start pattern
- Supply voltage range 2 V to 6.5 V
- 40 mA output current capability
- Very low standby current ($< 4\ \mu A$ at $V_{DD} = 6$ V)
- Up to 20 subsystem address groups
- Up to 64 commands per subsystem address

  } up to 1280 commands

- Requires few additional components

PACKAGE OUTLINES

SAA3008P: 20-lead DIL; plastic (SOT146).
SAA3008T: 20-lead mini-pack; plastic (SO20; SOT163A).

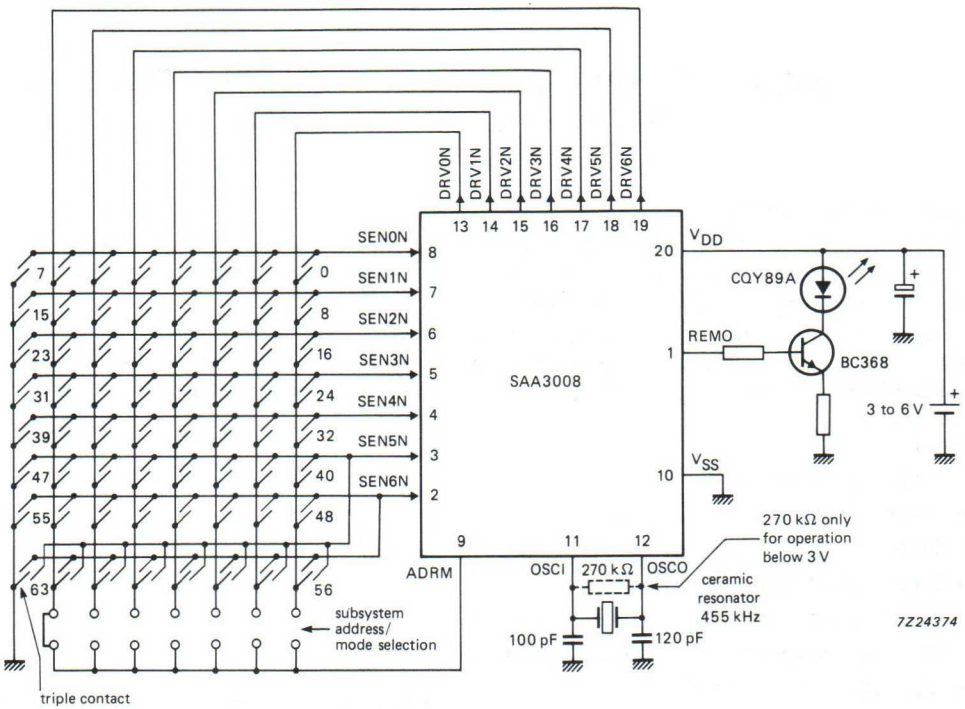


Fig.1 SAA3008 application example.

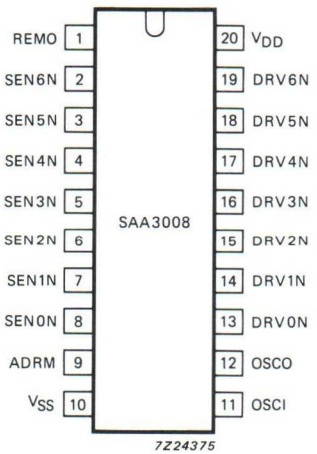


Fig.2 Pinning diagram.

PINNING

1	REMO	remote data output
2	SEN6N	sense inputs from key matrix
3	SEN5N	
4	SEN4N	
5	SEN3N	
6	SEN2N	
7	SEN1N	
8	SEN0N	
9	ADRM	address/mode control input
10	V_{SS}	ground (0 V)
11	OSCI	oscillator input
12	OSCO	oscillator output
13	DRV0N	drive outputs to key matrix
14	DRV1N	
15	DRV2N	
16	DRV3N	
17	DRV4N	
18	DRV5N	
19	DRV6N	
20	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Key matrix (DRV0N - DRV6N and SEN0N - SEN6N)

The transmitter keyboard is arranged as a scanned matrix with seven driver outputs (DRV0N to DRV6N) and seven sensing inputs (SEN0N to SEN6N) as shown in Fig.1. The driver outputs are open-drain n-channel transistors which are conductive in the stand-by mode. The sensing inputs enable the generation of 56 command codes. With two external diodes connected (or triple contact), as in Fig.1, all 64 commands are addressable. The sense lines have p-channel pull-up transistors, so that they are HIGH until pulled LOW by connecting them to an output via a key depression to initiate a code transmission.
The maximum allowable value of contact series resistance for keyboard switches in the ON-state is 7 kΩ.

Address/mode input (ADRM)

Subsystem addresses are defined by connecting one or two of the key matrix driver lines (DRV0N to DRV6N) to the ADRM input. This allows up to 20 subsystem addresses to be generated for the REMO output (bits S3, S2, S1 and S0) as shown in Table 1 and Fig.3.

The transmission mode is defined by the DRV6N to ADRM connection as follows:

- Mode 1 DRV6N not connected to ADRM
- Mode 2 DRV6N connected to ADRM

In Mode 1 the reference time REF equals 3To, this may be used as a reference time for the decoding sequence. In Mode 2 an additional modulated pulse has been inserted into the middle of the reference time, therefore, these pulses are now separated by 1.5To. This unique start pattern START uses the detection of a beginning word (see Fig.3).
When more than one connection is made to ADRM then all connections should be decoupled using diodes.

The ADRM input has switched pull-up and pull-down loads. In the standby mode only pull-down load is active and ADRM input is held LOW (this condition is independent of the ADRM circuit configuration and minimizes power loss in the standby mode). When a key is pressed the transmitter becomes active (pull-down is switched OFF, pull-up is switched ON) and the driver line signals are sensed for the subsystem address coding.

The subsystem address is sensed only within the first scan cycle, whereas the command code is sensed in every scan. The transmitted subsystem address remains unchanged if the subsystem address selection is changed while the command key is pressed. A change of the subsystem address does not start a transmission.

In a multiple keystroke sequence (Fig.6) the second word B might be transmitted with subsystem address 18 or 19 instead of the preselected subsystem address (Table 1). This is only relevant for systems decoding subsystem address 18 or 19.

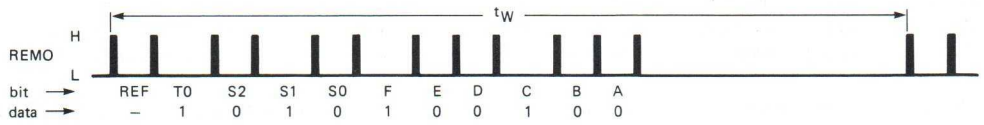
Remote control signal output (REMO)

The REMO output driver stage incorporates a bipolar emitter-follower which allows a high output current in the output active (HIGH) state (Fig.7).
The information is defined by the distance 't_b' between the leading edges of the modulated pulses (Fig.4). The distance t_b is a multiple of the basic unit T_o (Table 3) which equals 1152 periods of the oscillator frequency f_{osc} (Table 3). The pulses are modulated with 6 periods of 1/12 of the oscillator frequency (38 kHz).
The format of the output data is illustrated in Figs 3 and 4.
A data word starts with the reference time and toggle bit T0 and is followed by the definition bits for the subsystem address S3, S2, S1 and S0 (bit S3 is transmitted only for subsystem addresses 8 to 20). The selected command key is defined by bits F, E, D, C, B and A as shown in Table 2.

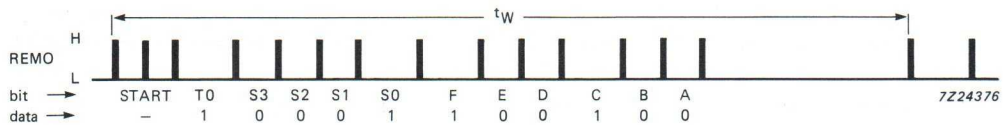
DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

The toggle bit T0 acts as an indication for the decoder whether the next instruction should be considered as a new command or not. The codes for the subsystem address and the selected key are given in Table 3.



(a) Transmission with reference time and subsystem addresses 1 to 7.



(b) Transmission with start-pattern and subsystem addresses 8 to 20.

Where:

Reference time	
start pattern	T0 toggle bit
S3, S2, S1, S0	subsystem address
A to F	command bits
t_W	word length
binary values	determined by pulse spacing

Fig.3 Data format of remote control signal (REMO).

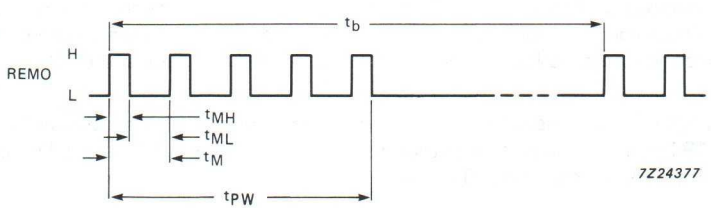


Fig.4 Waveform for one pulse period at REMO output; for timing values see Table 3.

Oscillator (OSCI, OSCO)

The external components for the oscillator circuit are connected to OSCI and OSCO. The oscillator operates with a ceramic resonator in the frequency range 350 kHz to 500 kHz, as defined by the resonator. When operating at a supply voltage of below 3 V a 270 kHz resistor should be connected in parallel with the resonator.

DEVELOPMENT DATA

Table 1 Definition of subsystem addresses

address number	driver line(s) connected to ADRM	subsystem address S3	S2	S1	S0
1	no connection	–	1	1	1
2	DRV0N	–	0	0	0
3	DRV1N	–	0	0	1
4	DRV2N	–	0	1	0
5	DRV3N	–	0	1	1
6	DRV4N	–	1	0	0
7	DRV5N	–	1	0	1
8	DRV0N and DRV2N	0	0	0	0
9	DRV0N and DRV3N	1	0	0	0
10	DRV0N and DRV4N	0	1	0	0
11	DRV0N and DRV5N	1	1	0	0
12	DRV1N and DRV2N	0	0	0	1
13	DRV1N and DRV3N	1	0	0	1
14	DRV1N and DRV4N	0	1	0	1
15	DRV1N and DRV5N	1	1	0	1
16	DRV2N and DRV3N	1	0	1	0
17	DRV2N and DRV4N	0	1	1	0
18	DRV2N and DRV5N	1	1	1	0
19	DRV3N and DRV4N	0	1	1	1
20	DRV3N and DRV5N	1	1	1	1

Table 2 Definition of command codes

key pressed	drive-to-sense connection made	command code generated F	EE	D	C	B	A
0	DRV0N to SEN0N	0	0	0	0	0	0
1	DRV1N to SEN0N	0	0	0	0	0	1
2	DRV2N to SEN0N	0	0	0	0	1	0
3	DRV3N to SEN0N	0	0	0	0	1	1
4	DRV4N to SEN0N	0	0	0	1	0	0
5	DRV5N to SEN0N	0	0	0	1	0	1
6	DRV6N to SEN0N	0	0	0	1	1	0
7	DRV7N to SEN0N	0	0	0	1	1	1
8	DRV0N to SEN1N	0	0	1	0	0	0
9	DRV1N to SEN1N	0	0	1	0	0	1
10	DRV2N to SEN1N	0	0	1	0	1	0
11	DRV3N to SEN1N	0	0	1	0	1	1
12	DRV4N to SEN1N	0	0	1	1	0	0
13	DRV5N to SEN1N	0	0	1	1	0	1
14	DRV6N to SEN1N	0	0	1	1	1	0
15	DRV7N to SEN1N	0	0	1	1	1	1
16	DRV0N to SEN2N	0	1	0	0	0	0
17	DRV1N to SEN2N	0	1	0	0	0	1
18	DRV2N to SEN2N	0	1	0	0	1	0
19	DRV3N to SEN2N	0	1	0	0	1	1
20	DRV4N to SEN2N	0	1	0	1	0	0

Table 2 Definition of command codes (continued)

key pressed	drive-to-sense connection made	command code generated					
		F	E	D	C	B	A
21	DRV5N to SEN2N	0	1	0	1	0	1
22	DRV6N to SEN2N	0	1	0	1	1	0
23	DRV7N to SEN2N	0	1	0	1	1	1
24	DRV0N to SEN3N	0	1	1	0	0	0
25	DRV1N to SEN3N	0	1	1	0	0	1
26	DRV2N to SEN3N	0	1	1	0	1	0
27	DRV3N to SEN3N	0	1	1	0	1	1
28	DRV4N to SEN3N	0	1	1	1	0	0
29	DRV5N to SEN3N	0	1	1	1	0	1
30	DRV6N to SEN3N	0	1	1	1	1	0
31	DRV7N to SEN3N	0	1	1	1	1	1
32	DRV0N to SEN4N	1	0	0	0	0	0
33	DRV1N to SEN4N	1	0	0	0	0	1
34	DRV2N to SEN4N	1	0	0	0	1	0
35	DRV3N to SEN4N	1	0	0	0	1	1
36	DRV4N to SEN4N	1	0	0	1	0	0
37	DRV5N to SEN4N	1	0	0	1	0	1
38	DRV6N to SEN4N	1	0	0	1	1	0
39	DRV7N to SEN4N	1	0	0	1	1	1
40	DRV0N to SEN5N	1	0	1	0	0	0
41	DRV1N to SEN5N	1	0	1	0	0	1
42	DRV2N to SEN5N	1	0	1	0	1	0
43	DRV3N to SEN5N	1	0	1	0	1	1
44	DRV4N to SEN5N	1	0	1	1	0	0
45	DRV5N to SEN5N	1	0	1	1	0	1
46	DRV6N to SEN5N	1	0	1	1	1	0
47	DRV7N to SEN5N	1	0	1	1	1	1
48	DRV0N to SEN6N	1	1	0	0	0	0
49	DRV1N to SEN6N	1	1	0	0	0	1
50	DRV2N to SEN6N	1	1	0	0	1	0
51	DRV3N to SEN6N	1	1	0	0	1	1
52	DRV4N to SEN6N	1	1	0	1	0	0
53	DRV5N to SEN6N	1	1	0	1	0	1
54	DRV6N to SEN6N	1	1	0	1	1	0
55	DRV7N to SEN6N	1	1	0	1	1	1
56	DRV0N to SEN5N and SEN6N	1	1	1	0	0	0
57	DRV1N to SEN5N and SEN6N	1	1	1	0	0	1
58	DRV2N to SEN5N and SEN6N	1	1	1	0	1	0
59	DRV3N to SEN5N and SEN6N	1	1	1	0	1	1
60	DRV4N to SEN5N and SEN6N	1	1	1	1	0	0
61	DRV5N to SEN5N and SEN6N	1	1	1	1	0	1
62	DRV6N to SEN5N and SEN6N	1	1	1	1	1	0
63	DRV7N to SEN5N and SEN6N	1	1	1	1	1	1

Table 3 Pulse timing

parameter	symbol	duration	duration at f_{osc} = 455 kHz; t_{osc} = 2.2 μs
Modulation period	t_M	$12t_{osc}$	26.4 μs
Modulation LOW time	t_{ML}	$8t_{osc}$	17.6 μs
Modulation HIGH time	t_{MH}	$4t_{osc}$	8.8 μs
Modulation pulse width	t_{PW}	$5t_M + t_{MH}$	140.8 μs
Basic unit of pulse spacing	t_o	$1152t_{osc}$	2.53 ms
Word length for subsystem addresses			
0 to 7	t_W	$55296t_{osc}$	121.44 ms
8 to 20	t_W	$59904t_{osc}$	132.56 ms
Pulse separation for			
logic 0	t_b	$2t_o$	5.06 ms
logic 1	t_b	$3t_o$	7.59 ms
reference time	t_b	$3t_o$	7.59 ms
toggle bit	t_b	$2t_o$	5.06 ms
		$3t_o$	7.59 ms
Start pattern	t_b	$2 \times 1.5t_o$	2 x 3.79 ms

DEVELOPMENT DATA

OPERATION

Keyboard

In the standby mode all drivers DRV0N-DRV6N are ON but are non-conducting due to their open drain configuration. When a key is pressed, a completed drain connection pulls down one or more of the sense lines to ground. Referring to Fig.5, the power-up sequence for the IC commences as a key is pressed. The oscillator becomes active and then, following the debounce time (t_{DB}), the output drivers become active successively.

Within the first scan cycle the transmission mode, subsystem address and the selected command code are sensed and loaded into an internal data latch. In a multiple keystroke sequence (Fig.6) the command code is always altered according to the sensed key.

Multiple keystroke protection

The keyborad is protected against multiple keystrokes. If more than one key is pressed the circuit will not generate a new REMO sequence (Fig.6).
In a multiple keystroke sequence the scan repetition rate is increased to detect the release of the key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix:

- The keys switching directly to ground (codes 7, 15, 23, 31, 39, 47, 55, 63) are not completely covered by multiple keystroke protection. If one sense input is switched to ground, other keys on that sense line are ignored.
- The sense lines SEN5N and SEN6N are not protected against multiple keystrokes on the same driver line because this has been used to define codes 56 to 63.

OPERATION (continued)

Output sequence

The output operation starts when the code of the selected key has been loaded into the internal command register. A burst of pulses, including the latched address and command codes, is generated at the output REMO for as long as the key is pressed. The format of the output pulse train is as shown in Figs 3 and 4. The operation is terminated by releasing the key, or by pressing more than one key at the same time. Once a sequence has been started, the transmitted words will always be completed after the key has been released.

The toggle bit T0 is incremented if the key is released for a minimum time t_{REL} (Fig.5). In a multiple keystroke sequence the toggle bit remains unchanged.

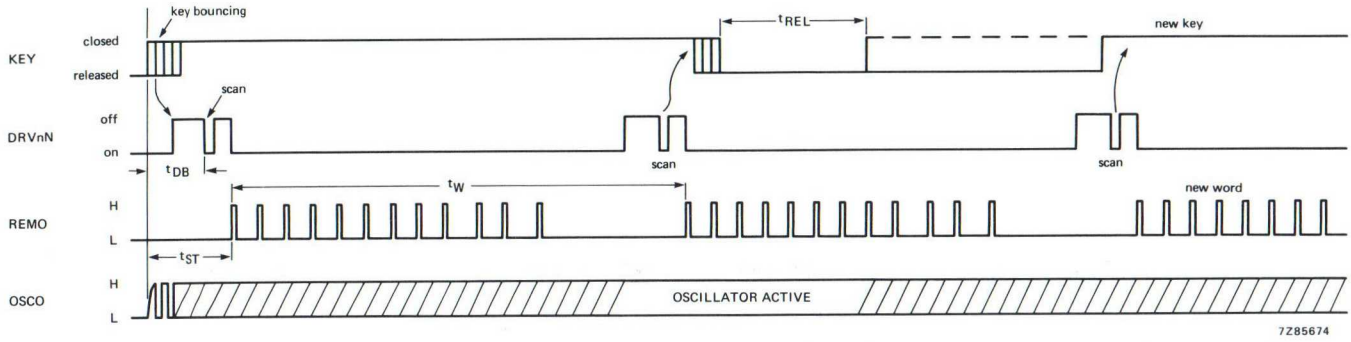


Fig.5 Single keystroke sequence; t_{DB} = debounce time = $4T_o$ to $9T_o$; t_{ST} = start time = $5T_o$ to $10T_o$; t_{REL} = minimum release time = T_o; t_W = word length.

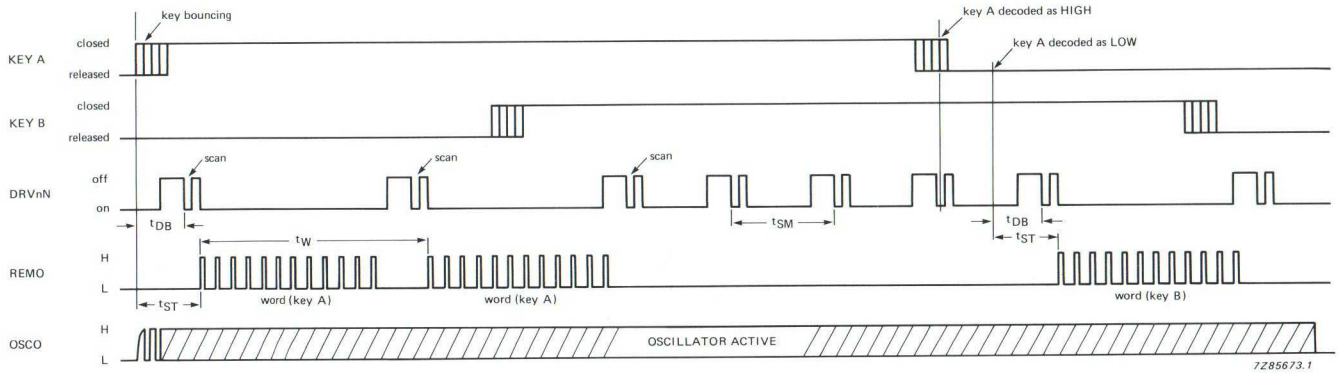


Fig.6 Scan rate multiple keystroke sequence: t_{SM} = scan rate (multiple keystroke) = $6T_O$ to $10T_O$; t_{DB}, t_{ST}, and t_W are as per Fig.5.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0.3	+7	V
Input voltage range		V_I	−0.3	V_{DD} + 0.3	V
Output voltage range		V_O	−0.3	V_{DD} + 0.3	V
Total power dissipation					
DIL package (SOT146)		P_{tot}	–	300	mW
mini-pack (SO20; SOT163A)		P_{tot}	–	200	mW
Power dissipation					
matrix outputs DRV0N to DRV6N		P_O	–	50	mW
remote data output REMO		P_O	–	200	mW
Operating ambient temperature range		T_{amb}	−20	+70	°C
Storage temperature range		T_{stg}	−20	+125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 0 to +70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2.0	–	6.5	V
Supply current active	f_{osc} = 455 kHz;					
	V_{DD} = 3 V	I_{DD}	–	0.25	–	mA
	V_{DD} = 4.5 V	I_{DD}	–	0.5	–	mA
	V_{DD} = 6 V	I_{DD}	–	1	–	mA
Standby mode	T_{amb} = 25 °C;					
	V_{DD} = 6 V	I_{DD}	–	–	4	μA
Oscillator frequency (ceramic resonator)	V_{DD} = 2 to 6.5 V	f_{osc}	350	–	500	kHz
Inputs SEN0N to SEN6N						
Input voltage LOW	V_{DD} = 2 to 6.5 V	V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH	V_{DD} = 2 to 6.5 V	V_{IH}	0.7 V_{DD}	–	–	V
Input current (p-channel pull-up)	V_{IL} = 0 V					
	V_{DD} = 2 V	I_I	−10	–	−100	μA
	V_{DD} = 6.5 V	I_I	−100	–	−600	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Outputs DRV0N to DRV6N (open drain 1)						
Output voltage ON	I_O = 0.25 mA; V_{DD} = 2 V	V_{OL}	–	–	0.3	V
	I_O = 2.5 mA; V_{DD} = 6.5 V	V_{OL}	–	–	0.6	V
Output current OFF	V_{DD} = 6.5 V	I_O	–	–	10	μA
Input ADRM						
Input voltage LOW		V_{IL}	–	–	0.4 V_{DD}	V
Input voltage HIGH		V_{IH}	0.85 V_{DD}	–	–	V
Input current (switched p and n channel pull-up and pull-down)						
pull-up active	V_I = 0 V					
	V_{DD} = 2 V	I_{IL}	−10	–	−100	μA
	V_{DD} = 6.5 V	I_{IL}	−100	–	−600	μA
pull-down active	V_I = V_{DD}					
	V_{DD} = 2 V	I_{IH}	10	–	100	μA
	V_{DD} = 6.5 V	I_{IH}	100	–	600	μA
Output REMO						
Output voltage HIGH	I_{OH} = −40 mA; T_{amb} = 25 °C					
	V_{DD} = 2 V	V_{OH}	0.8	–	–	V
	V_{DD} = 6.5 V	V_{OH}	5.0	–	–	V
	I_{OH} = 0.5 mA; V_{DD} = 2 V	V_{OH}	0.8 V_{DD}	–	–	V
Output voltage LOW	I_{OL} = 0.5 mA; V_{DD} = 2 V	V_{OL}	–	–	0.4	V
	I_{OL} = 2.0 mA; V_{DD} = 6.5 V	V_{OL}	–	–	0.4	V
Input OSCI						
Input current HIGH	V_{DD} = 6.5 V	I_{IH}	3.0	–	7.0	μA
Output OSCO						
Output voltage HIGH	I_{OH} = 100 μA; V_{DD} = 6.5 V	V_{OH}	V_{DD}−0.8	–	–	V
Output voltage LOW	I_{OL} = 100 μA; V_{DD} = 6.5 V	V_{OL}	–	–	0.7	V

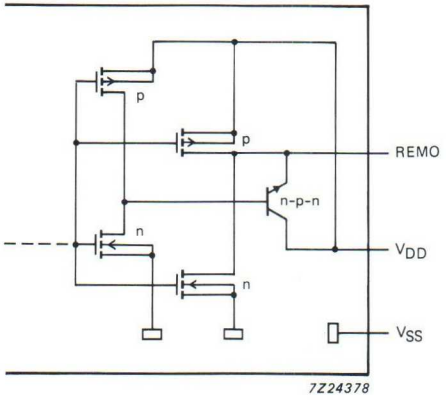


Fig.7 REMO output stage.

DEVELOPMENT DATA

INFRARED REMOTE CONTROL DECODERS

GENERAL DESCRIPTION

The main function of the SAA3009 and SAA3049 ICs is to check and convert the received coded data (RECS80/RC5) into latched binary outputs. The device address can be hard-wired for a particular address allowing several devices in one location. Alternatively, received data with any address can be accepted, the received data and address are then outputs.

Features

- Decodes 64 remote control commands with a maximum of 32 subaddresses
- Accepts RECS80 codes with pulse position modulation (SAA3004, SAA3007, SAA3008) or RC5 codes with biphase transmission (SAA3006, SAA3010)
- Available at SAA3009 with 8 high current (10 mA) open-drain outputs and internal pull-ups for direct LED drive via resistors or as SAA3049 for low supply current applications
- Adding circuitry for binary decoding allows a maximum of 2048 commands to be used, for example 1-of-16 decoder (HEF4515)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
SAA3009	note 1	V_{CC}	4.5	5.0	5.5	V
SAA3049	note 2	V_{CC}	2.5	–	5.5	V
Supply current						
SAA3009	note 1	I_{CC}	–	–	70	mA
SAA3049	note 2	I_{CC}	–	1.0	2.0	mA
Oscillator frequency		f_{osc}	–	4	–	MHz
Output sink current LOW (pins 1 to 8)						
SAA3009	note 3	I_{OL}	–	–	10	mA
SAA3049	note 4	I_{OL}	1.6	3.0	–	mA

Notes to the QUICK REFERENCE DATA

1. T_{amb} = 0 to + 70 °C.
2. T_{amb} = −40 to + 85 °C.
3. Open-drain with 20 to 50 kΩ internal pull-up resistor.
4. Open-drain without internal pull-up resistor at V_{CC} = 5 V ± 10%; V_O = 0.4 V.

PACKAGE OUTLINES

SAA3009P; SAA3049P: 20 lead DIL; plastic (SOT146).
SAA3049T: 20 lead mini-pack; plastic (SO20; SOT163A).

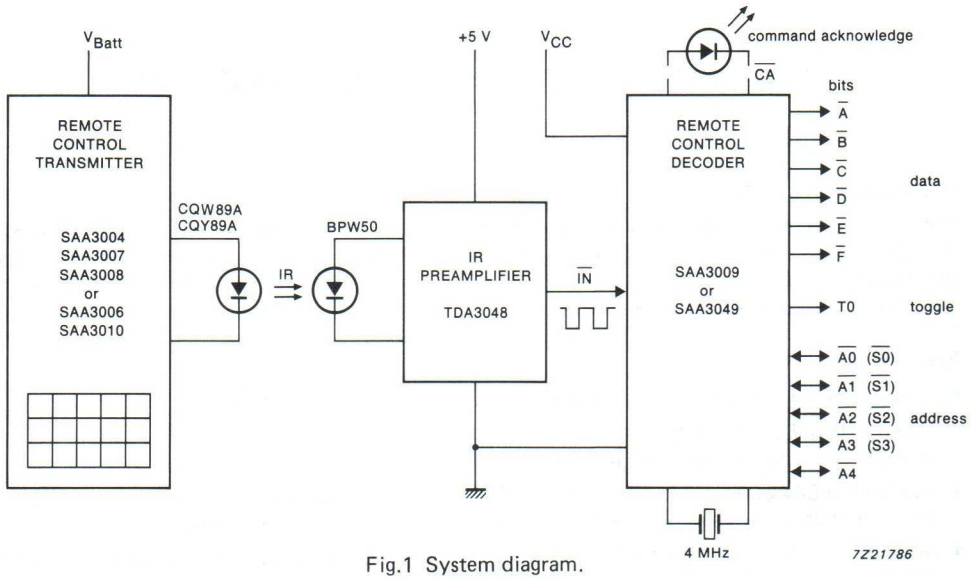


Fig.1 System diagram.

TRANSMITTERS (see individual data sheets for full specifications)

SAA3004 V_{Batt} = 4 to 11 V (max.); 7 x 64 = 448 commands (RECS80 code)

SAA3007 V_{Batt} = 2 to 6.5 V (max.); 20 x 64 = 1280 commands (RECS80 code)

SAA3008 V_{Batt} = 2 to 6.5 V (max.); 20 x 64 = 1280 commands (RECS80 code)

SAA3006 V_{Batt} = 2 to 7.0 V (max.); 32 x 64 = 2048 commands (RC5 code)

SAA3010 V_{Batt} = 2 to 7.0 V (max.); 32 x 64 = 2048 commands (RC5 code)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage				
SAA3009	V_{CC}	−0.5	7.0	V
SAA3049	V_{CC}	−0.8	8.0	V
Input voltage (any pin)				
SAA3009	V_I	−0.5	7.0	V
SAA3049	V_I	−0.8	V_{CC} + 0.8	V
DC input/output current				
SAA3009 (pins 1 to 8)	$\pm I_I, \pm I_O$	–	20	mA
SAA3009 (all other pins)	$\pm I_I, \pm I_O$	–	10	mA
SAA3049 (any pin)	$\pm I_I, \pm I_O$	–	10	mA
Total power dissipation				
SAA3009	P_{tot}	–	1	W
SAA3049	P_{tot}	–	0.5	W
Operating ambient temperature range				
SAA3009	T_{amb}	0	+ 70	°C
SAA3049	T_{amb}	−40	+ 85	°C
Storage temperature range				
SAA3009	T_{stg}	−65	+ 150	°C
SAA3049	T_{stg}	−65	+ 150	°C

DEVELOPMENT DATA

CHARACTERISTICS

All voltages measured with respect to ground (V_{EE} = 0 V).

SAA3009: V_{CC} = 4.5 to 5.5 V; T_{amb} = 0 to + 70 °C unless otherwise specified
SAA3049: V_{CC} = 2.5 to 5.5 V; T_{amb} = −40 to + 85 unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
SAA3009		V_{CC}	4.5	5.0	5.5	V
SAA3049		V_{CC}	2.5	–	5.5	V
Supply current						
SAA3009		I_{CC}	–	–	70	mA
SAA3049		I_{CC}	–	0.8	2.0	mA
Input signals (pin 9)						
Input voltage HIGH						
SAA3009		V_{IH}	2.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW	active					
SAA3009		V_{IL}	0.5	–	0.8	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Mode selection (pin 11)						
Input voltage HIGH	note 1					
SAA3009		V_{IH}	2.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW	note 2					
SAA3009		V_{IL}	−0.5	–	0.8	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Command received indicator and mode control (pin 19)	note 3					
Input voltage HIGH						
SAA3009		V_{IH}	3.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW						
SAA3009		V_{IL}	−0.5	–	1.5	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Crystal oscillator						
Oscillator frequency	note 4	f_{osc}	–	4	–	MHz

parameter	conditions	symbol	min.	typ.	max.	unit
SAA3009 OUTPUTS						
10 mA open-drain with internal pull-up resistor						
(pins 1 to 8)						
Output voltage HIGH	$I_{OH} = -50\ \mu A$	V_{OH}	2.4	–	V_{CC}	V
Output voltage LOW	$I_{OL} = 10$ mA	V_{OL}	–	–	1.0	V
Output sink current LOW		I_{OL}	–	–	10	mA
5 mA open-drain without internal pull-up resistor						
(pins 18 and 19)						
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW	$I_{OL} = 5$ mA	V_{OL}	–	–	0.45	V
Output sink current LOW		I_{OL}	–	–	5	mA
1.6 mA open-drain with internal pull-up resistor						
(pins 15, 16 and 17)						
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW	$I_{OL} = 1.6$ mA	V_{OL}	–	–	0.45	V
Output sink current LOW		I_{OL}	–	–	1.6	mA
SAA3049 OUTPUTS						
Open-drain without internal pull-up resistor	note 5					
Output sink current LOW	$V_{CC} = 5\ V \pm 10\%$; $V_{OL} = 0.4$ V	I_{OL}	1.6	3.0	–	mA

Notes to the characteristics

1. RECS80 decoder for transmitters SAA3004, SAA3007 or SAA3008; SAA3009 has an internal pull-up resistor.
2. RC5 decoder for transmitters SAA3006 or SAA3010.
3. With pin 19 = HIGH, then pins 7, 8, 15, 16 and 17 are address inputs.
   With pin 19 = LOW, then pins 7, 8, 15, 16 and 17 are 4 or 5 address received outputs.

   In Figs 4, 5 and 6 this HIGH/LOW switching is dependent on whether the transistor on pin 19 is fed via a series resistor or not. In both applications pin 19, which toggles several times (see Fig.3) while a valid command is acknowledged, can be used to activate (flash) an LED indicator.
4. A quartz crystal with a frequency of 4 MHz is recommended for the standard transmitter application.
4. Application as output requires connection of an external pull-up resistor.

DEVELOPMENT DATA

CHARACTERISTICS (continued)

Reset (pin 14)

The simple circuit is shown in Figs 4, 5 and 6. The alternative reset circuit shown in Fig.2 protects against short term power supply transients by generating a reset.

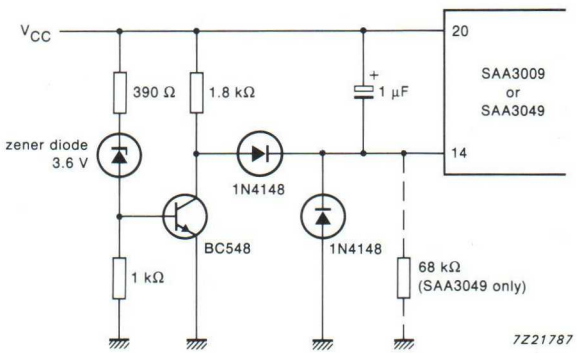


Fig.2 Proposed improved reset circuit.

Infrared signal input (pin 9)

This pin is sensitive to a negative-going edge.

Command received indicator (pin 19)

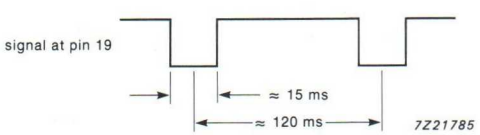
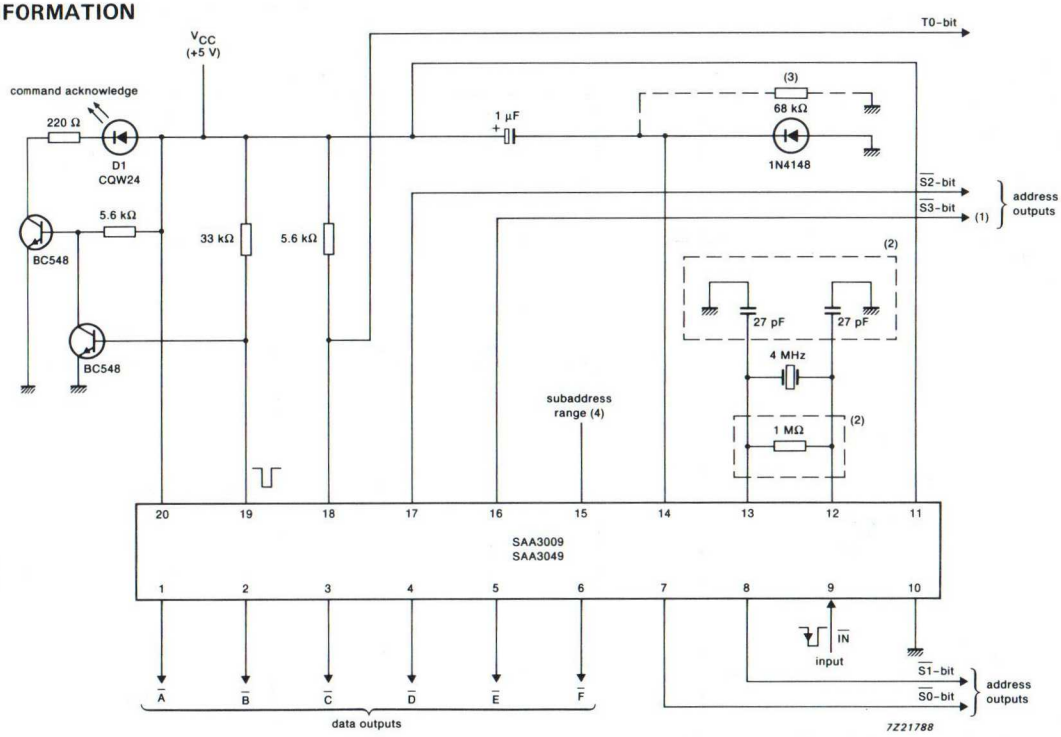


Fig.3 Output diagram of command acknowledge.

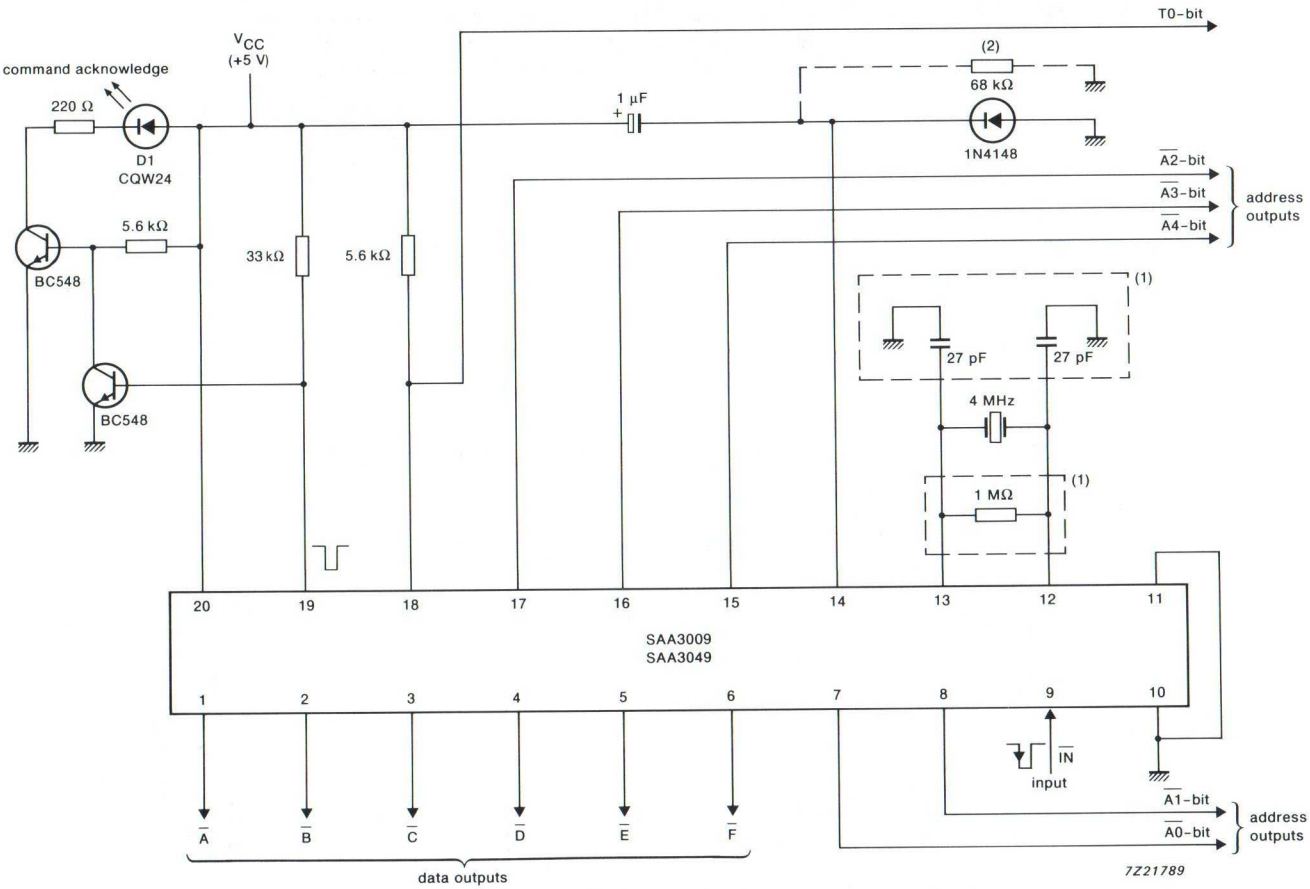
APPLICATION INFORMATION



(1) only for subaddress 8 to 20.
(2) only for SAA3009.
(3) only for SAA3049.
(4) subaddress range:
when LOW (subaddress 8 to 20) pin 15 is connected to ground
when HIGH (subaddress 1 to 7) pin 15 is open (SAA3009)
when HIGH (subaddress 1 to 7) pin 15 is connected via pull-up resistor to V_{CC} (SAA3049)

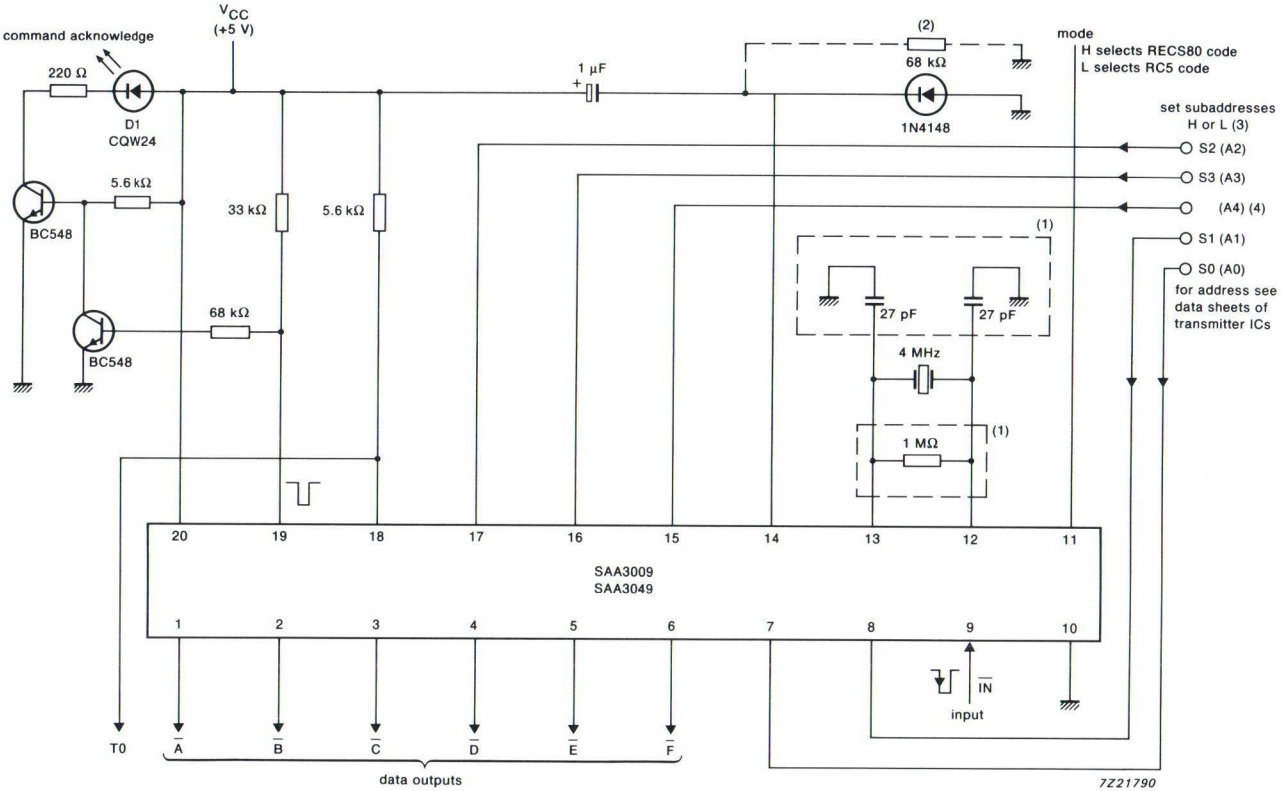
Fig.4 Remote control decoder with latched 11 (10) -bit parallel outputs (10 (9) -bits inverted) for use with transmitter types SAA3004, SAA3007 or SAA3008; pin 11 is HIGH for RECS80 code.

APPLICATION INFORMATION (continued)



(1) only for SAA3009.
(2) only for SAA3049.

Fig.5 Remote control decoder with latched 12-bit parallel outputs (11 bits inverted) for use with transmitter types SAA3006 or SAA3010; pin 11 is LOW for RC5 code.



(1) only for SAA3009.
(2) only for SAA3049.
(3) address inputs:
when LOW address input pin is connected to ground
when HIGH address input pin is open (SAA3009)
when HIGH address input pin is connected via pull-up resistor to V_{CC} (SAA3049)
(4) subaddress range RECS80 code:
when LOW (subaddress 8 to 20) pin 15 is connected to ground
when HIGH (subaddress 1 to 7) pin 15 is open (SAA3009)
when HIGH (subaddress 1 to 7) pin 15 is connected via pull-up resistor to V_{CC} (SAA3049)

Fig.6 Remote control decoder for up to 20 subaddresses with 6 + 1-bit parallel outputs (RECS80 code). Decoder is set for required subaddress by holding address pins HIGH or LOW. Pin 11 is HIGH for use with transmitter types SAA3004, SAA3007 or SAA3008 (RECS80 code). Pin 11 is LOW for use with transmitter types SAA3006 or SAA3010 (RC5 code). Remote control decoder for up to 32 subaddresses with 6 + 1-bit parallel outputs (RC5 code).

INFRARED REMOTE CONTROL TRANSMITTER RC-5

GENERAL DESCRIPTION

The SAA3010 is intended as a general purpose (RC-5) infrared remote control system for use where a low voltage supply and a large debounce time are expected. The device can generate 2048 different commands and utilizes a keyboard with a single pole switch for each key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands. The keyboard interconnection is illustrated by Fig.3.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified in the section **"KEYBOARD OPERATION"**.

Features

- Low voltage requirement
- Biphase transmission technique
- Single pin oscillator
- Test mode facility

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{DD}	2	–	7	V
Input voltage range*	V_I	−0.5	–	V_{DD}+0.5	V
Input current	I_I	–	–	±10	mA
Output voltage range*	V_O	−0.5	–	V_{DD}+0.5	V
Output current	I_O	–	–	±10	mA
Operating ambient temperature range	T_{amb}	−25	–	85	°C

* V_{DD}+0.5 V must not exceed 9 V.

The use of this device must conform with the Philips Standard number URT-0421.

PACKAGE OUTLINES

28-lead DIL plastic; (SOT117).
28-lead mini-pack; plastic (SO28; SOT136A).

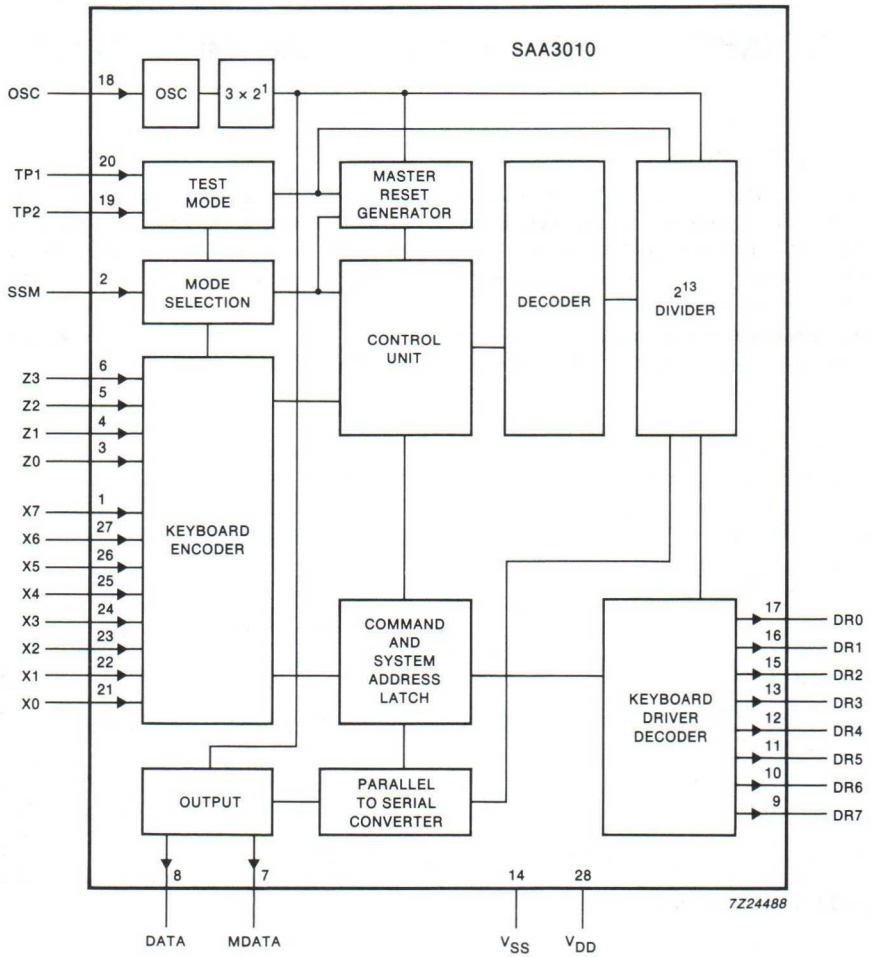


Fig.1 Block diagram.

PINNING

pin	mnemonic	function
1	X7 (IPU)	sense input from key matrix
2	SSM (I)	system mode selection input
3-6	Z0-Z3 (IPU)	sense inputs from key matrix
7	MDATA (OP3)	generated output data modulated with 1/12 the oscillator frequency at a 25% duty factor
8	DATA (OP3)	generated output information
9-13	DR7-DR3 (ODN)	scan drivers
14	V_{SS}	ground (0 V)
15-17	DR2-DR0 (ODN)	scan drivers
18	OSC (I)	oscillator input
19	TP2 (I)	test point 2
20	TP1 (I)	test point 1
21-27	X0-X6 (IPU)	sense inputs from key matrix
28	V_{DD} (I)	voltage supply

(I) = input
(IPU) = input with p-channel pull-up transistor
(ODN) = output with open drain n-channel transistor
(OP3) = output 3-state

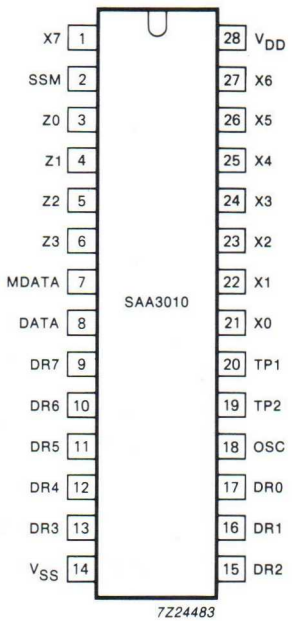


Fig.2 Pinning diagram.

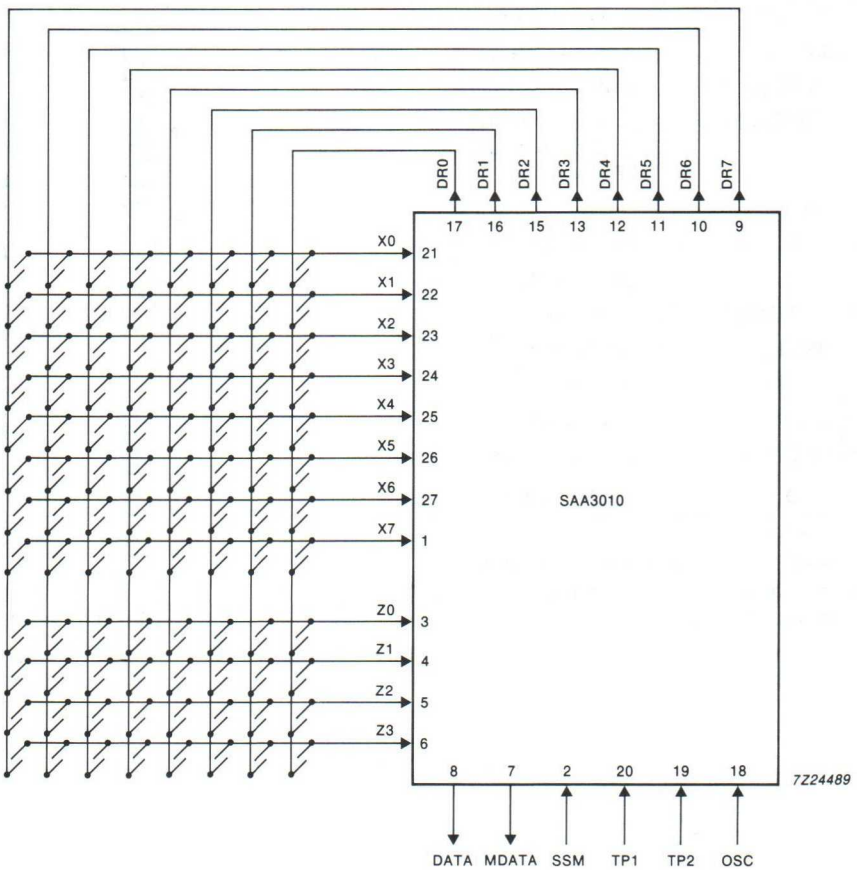


Fig.3 Keyboard interconnection.

FUNCTIONAL DESCRIPTION

Keyboard operation

Every connection of one X-input and one DR-output will be recognized as a legal key operation and will cause the device to generate the corresponding code. The same applies to every connection of one Z-input to one DR-output with the proviso that SSM must be LOW. When SSM is HIGH a wired connection must exist between a Z-input and a DR-output. If no connection is present the system number will not be generated. Activating two or more X-inputs, Z-inputs or Z-inputs and X-inputs at the same time is an illegal action and inhibits further activity (oscillator will not start).

When one X- or Z-input is connected to more than one DR-output, the last scan signal will be considered as legal.

The maximum value of the contact series resistance of the switched keyboard is 7 kΩ.

Inputs

In the quiescent state the command inputs X0 to X7 are held HIGH by an internal pull-up transistor. When the system mode selection (SSM) input is LOW and the system is quiescent, the system inputs Z0 to Z3 are also held HIGH by an internal pull-up transistor. When SSM is HIGH the pull-up transistor for the Z-inputs is switched off, in order to prevent current flow, and a wired connection in the Z-DR matrix provides the system number.

Outputs

The output signal DATA transmits the generated information in accordance with the format illustrated by Fig.4 and Tables 1 and 2. The code is transmitted using a biphase technique as illustrated by Fig.5. The code consists of four parts:

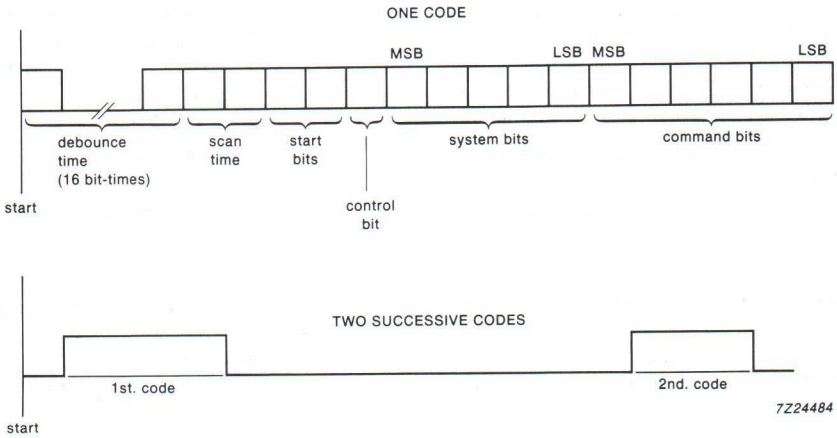
- Start part – 1.5 bits (2 x logic 1)
- Control part – 1 bit
- System part – 5 bits
- Command part – 6 bits

The output signal MDATA transmits the generated information modulated by 1/12 of the oscillator frequency with a 50% duty factor.

In the quiescent state both DATA and MDATA are non-conducting (3-state outputs).

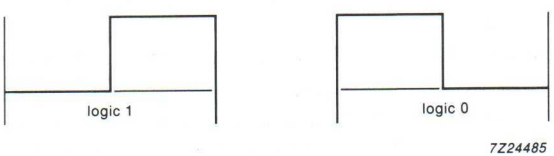
The scan driver outputs DR0 to DR7 are open drain n-channel transistors and conduct when the circuit is quiescent. After a legal key operation the scanning cycle is started and the outputs switched to the conductive state one by one. The DR-outputs were switched off at the end of the preceding debounce cycle.

FUNCTIONAL DESCRIPTION (continued)



Where: debounce time + scan time = 18 bit-times
repetition time = 4 x 16 bit-times

Fig.4 Data output format.



Where: 1 bit-time = $3.2^8 \times T_{OSC}$ = 1.778 ms (typ.)

Fig.5 Biphase transmission technique.

Table 1 Command matrix (X-DR)

code no.	X-lines 0 1 2 3 4 5 6 7	DR-lines 0 1 2 3 4 5 6 7	command bits 5 4 3 2 1 0
0	●	●	0 0 0 0 0 0
1	●	●	0 0 0 0 0 1
2	●	●	0 0 0 0 1 0
3	●	●	0 0 0 0 1 1
4	●	●	0 0 0 1 0 0
5	●	●	0 0 0 1 0 1
6	●	●	0 0 0 1 1 0
7	●	●	0 0 0 1 1 1
8	●	●	0 0 1 0 0 0
9	●	●	0 0 1 0 0 1
10	●	●	0 0 1 0 1 0
11	●	●	0 0 1 0 1 1
12	●	●	0 0 1 1 0 0
13	●	●	0 0 1 1 0 1
14	●	●	0 0 1 1 1 0
15	●	●	0 0 1 1 1 1
16	●	●	0 1 0 0 0 0
17	●	●	0 1 0 0 0 1
18	●	●	0 1 0 0 1 0
19	●	●	0 1 0 0 1 1
20	●	●	0 1 0 1 0 0
21	●	●	0 1 0 1 0 1
22	●	●	0 1 0 1 1 0
23	●	●	0 1 0 1 1 1
24	●	●	0 1 1 0 0 0
25	●	●	0 1 1 0 0 1
26	●	●	0 1 1 0 1 0
27	●	●	0 1 1 0 1 1
28	●	●	0 1 1 1 0 0
29	●	●	0 1 1 1 0 1
30	●	●	0 1 1 1 1 0
31	●	●	0 1 1 1 1 1

FUNCTIONAL DESCRIPTION (continued)

Table 1 Command matrix (X-DR) (continued)

code no.	X-lines 0 1 2 3 4 5 6 7	DR-lines 0 1 2 3 4 5 6 7	command bits 5 4 3 2 1 0
32	●	●	1 0 0 0 0 0
33	●	●	1 0 0 0 0 1
34	●	●	1 0 0 0 1 0
35	●	●	1 0 0 0 1 1
36	●	●	1 0 0 1 0 0
37	●	●	1 0 0 1 0 1
38	●	●	1 0 0 1 1 0
39	●	●	1 0 0 1 1 1
40	●	●	1 0 1 0 0 0
41	●	●	1 0 1 0 0 1
42	●	●	1 0 1 0 1 0
43	●	●	1 0 1 0 1 1
44	●	●	1 0 1 1 0 0
45	●	●	1 0 1 1 0 1
46	●	●	1 0 1 1 1 0
47	●	●	1 0 1 1 1 1
48	●	●	1 1 0 0 0 0
49	●	●	1 1 0 0 0 1
50	●	●	1 1 0 0 1 0
51	●	●	1 1 0 0 1 1
52	●	●	1 1 0 1 0 0
53	●	●	1 1 0 1 0 1
54	●	●	1 1 0 1 1 0
55	●	●	1 1 0 1 1 1
56	●	●	1 1 1 0 0 0
57	●	●	1 1 1 0 0 1
58	●	●	1 1 1 0 1 0
59	●	●	1 1 1 0 1 1
60	●	●	1 1 1 1 0 0
61	●	●	1 1 1 1 0 1
62	●	●	1 1 1 1 1 0
63	●	●	1 1 1 1 1 1

Table 2 System matrix (Z-DR)

syst. no.	Z-lines 0 1 2 3 4 5 6 7	DR-lines 0 1 2 3 4 5 6 7	system bits 4 3 2 1 0
0	●	●	0 0 0 0 0
1	●	●	0 0 0 0 1
2	●	●	0 0 0 1 0
3	●	●	0 0 0 1 1
4	●	●	0 0 1 0 0
5	●	●	0 0 1 0 1
6	●	●	0 0 1 1 0
7	●	●	0 0 1 1 1
8	●	●	0 1 0 0 0
9	●	●	0 1 0 0 1
10	●	●	0 1 0 1 0
11	●	●	0 1 0 1 1
12	●	●	0 1 1 0 0
13	●	●	0 1 1 0 1
14	●	●	0 1 1 1 0
15	●	●	0 1 1 1 1
16	●	●	1 0 0 0 0
17	●	●	1 0 0 0 1
18	●	●	1 0 0 1 0
19	●	●	1 0 0 1 1
20	●	●	1 0 1 0 0
21	●	●	1 0 1 0 1
22	●	●	1 0 1 1 0
23	●	●	1 0 1 1 1
24	●	●	1 1 0 0 0
25	●	●	1 1 0 0 1
26	●	●	1 1 0 1 0
27	●	●	1 1 0 1 1
28	●	●	1 1 1 0 0
29	●	●	1 1 1 0 1
30	●	●	1 1 1 1 0
31	●	●	1 1 1 1 1

FUNCTIONAL DESCRIPTION (continued)

Combined system mode (SSM is LOW)

The X and Z sense inputs have p-channel pull-up transistors, so that they are HIGH, until pulled LOW by connecting them to an output as the result of a key operation. Legal operation of a key in the X-DR or Z-DR matrix will start the debounce cycle, once key contact has been established for 18 bit-times without interruption, the oscillator enable signal is latched and the key may be released. An interruption within the 18 bit-time period resets the device.

At the end of the debounce cycle the DR-outputs are switched off and two scan cycles are started, that switch on the DR-lines one by one. When a Z- or X-input senses a low level, a latch enable signal is fed to the system (Z-input) or command (X-input) latches.

After latching a system number the device will generate the last command (i.e. all command bits logic 1) in the chosen system for as long as the key is operated. Latching of a command number causes the chip to generate this command together with the system number memorized in the system latch. Releasing the key will reset the device if no data is to be transmitted at the time. Once transmission has started the code will complete to the end.

Single system mode (SSM is HIGH)

In the single system mode, the X-inputs will be HIGH as in the combined system mode. The Z-inputs will be disabled by having their pull-up transistors switched off; a wired connection in the Z-DR matrix provides the system code. Only legal key operation in the X-DR matrix will start the debounce cycle, once key contact has been established for 18 bit-times without interruption the oscillator enable signal is latched and the key may be released. An interruption within the 18 bit-time period resets the internal action.

At the end of the debounce cycle the pull-up transistors in the X-lines are switched off and those in the Z-lines are switched on for the first scan cycle. The wired connection in the Z-matrix is then translated into a system number and memorized in the system latch. At the end of the first scan cycle the pull-up transistors in the Z-lines are switched off and the inputs are disabled again; the pull-up transistors in the X-lines are switched on. The second scan cycle produces the command number which, after being latched, is transmitted together with the system number.

Key release detection

An extra control bit is added which will be complemented after key release; this indicates to the decoder that the next code is a new command. This is important in the case where more digits need to be entered (channel numbers of Teletext or Viewdata pages). The control bit will only be complemented after the completion of at least one code transmission. The scan cycles are repeated before every code transmission, so that even with "take over" of key operation during code transmission the right system and command numbers are generated.

Reset action

The device will be reset immediately a key is released during:

- debounce time
- between two codes.

When a key is released during matrix scanning, a reset will occur if:

- a key is released while one of the driver outputs is in the low ohmic state (logic 0)
- a key is released before that key has been detected
- there is no wired connection in the Z-DR matrix when SSM is HIGH.

Oscillator

The OSC is the input/output for a 1-pin oscillator. The oscillator is formed by a ceramic resonator, TOKO CRK429, order code, 2422 540 98069 or equivalent. A resistor of 6.8 kΩ must be placed in series with the resonator. The resistor and resonator are grounded at one side.

Test

Initialization of the circuit is performed when TP1, TP2 and OSC are HIGH. All internal nodes are defined except for the LATCH. The latch is defined when a scan cycle is started by pulling down an X- or Z-input while the oscillator is running.

If the debounce cycle has been completed, the scan cycle can be completed 3×2^3 faster, by setting TP1 HIGH.

If the scan cycle has been completed, the contents of the latch can be read 3×2^7 faster by setting TP2 HIGH.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	8.5	V
Input voltage range *	V_I	−0.5	V_{DD}+0.5	V
Output voltage range *	V_O	−0.5	V_{DD}+0.5	V
Input current	I_I	–	±10	mA
Output current	I_O	–	±10	mA
Maximum power dissipation				
OSC output	P_O	–	50	mW
other outputs	P_O	–	100	mW
Total power dissipation	P_{tot}	–	200	mW
Operating ambient temperature range	T_{amb}	−25	+ 85	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

* V_{DD}+0.5 V must not exceed 9.0 V.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling, however, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DC CHARACTERISTICS

T_{amb} = −25 °C to + 70 °C; V_{DD} = 2.0 to 7.0 V unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2.0	–	7.0	V
Quiescent supply current	note 1 T_{amb} = 25 °C; I_O = 0 mA at all outputs. X0 to X7 and Z0 to Z3 at V_{DD} TP1, TP2, OSC at V_{SS} SSM at V_{SS} or V_{DD}	I_{DD}	–	–	10	μA
INPUTS						
Keyboard inputs X and Z with p-channel pull-up transistor						
Input current at each input	V_I = 0 V; TP1 = TP2 = SSM = LOW	$-I_I$	10	–	600	μA
Input voltage HIGH	note 2	V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input voltage LOW	note 2	V_{IL}	0	–	$0.3V_{DD}$	V
Input leakage current	T_{amb} = 25 °C; V_I = 7 V; TP1 = TP2 = HIGH	I_{LI}	–	–	1	μA
Input leakage current	T_{amb} = 25 °C; V_I = 0 V; TP1 = TP2 = HIGH	$-I_{LI}$	–	–	1	μA
OSC						
Input leakage current	T_{amb} = 25 °C; V_I = 0 V; TP1 = TP2 = HIGH	$-I_{LI}$	–	–	2	μA
Input current	T_{amb} = 25 °C; V_I = V_{DD}	I_{OSC}	4.5	–	30	μA
SSM, TP1, TP2						
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input voltage LOW		V_{IL}	0	–	$0.3V_{DD}$	V
Input leakage current	T_{amb} = 25 °C; V_I = 7.0 V	I_{LI}	–	–	1	μA
Input leakage current	T_{amb} = 25 °C; V_I = 0 V	$-I_{LI}$	–	–	1	μA

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
OUTPUTS						
DATA, MDATA						
Output voltage HIGH	$I_{OH} = -0.4$ mA	V_{OH}	$V_{DD}-0.3$	–	–	V
Output voltage LOW	$I_{OL} = 0.6$ mA	V_{OL}	–	–	0.3	V
Output leakage current	$V_O = 7.0$ V	$+I_{LO}$	–	–	10	μA
	$V_O = 7.0$ V; $T_{amb} = 25$ °C	$+I_{LO}$	–	–	1	μA
	$V_O = 0$ V	$-I_{LO}$	–	–	20	μA
	$V_O = 0$ V; $T_{amb} = 25$ °C	$-I_{LO}$	–	–	2	μA
DR0 to DR7						
Output voltage LOW	$I_{OL} = 0.3$ mA	V_{OL}	–	–	0.3	V
Output leakage current	$V_O = 7.0$ V	$+I_{LO}$	–	–	10	μA
	$V_O = 7.0$ V; $T_{amb} = 25$ °C	$+I_{LO}$	–	–	1	μA

Notes to the DC characteristics

1. Quiescent supply current measurement must be preceded by the initialization procedure described in the **TEST** section.
2. This DC test condition protects the AC performance of the output. The DC current requirements in the actual application are lower.

AC CHARACTERISTICS

T_{amb} = −25 to + 85 °C; V_{DD} = 2.0 to 7.0 V unless otherwise stated

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator frequency	C_L = 160 pF; Figs 6 and 7					
operational		f_{OSC}	–	–	450	kHz
free-running		f_{OSC}	10	–	120	kHz

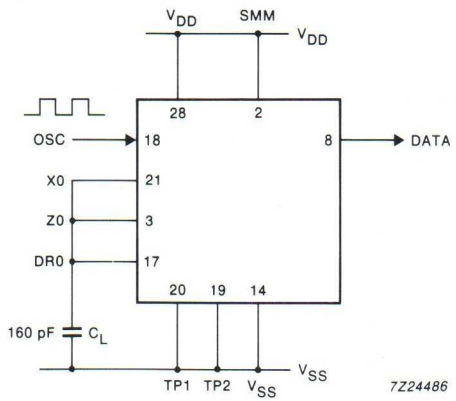


Fig.6 Test set-up for maximum f_{OSC} measurement.

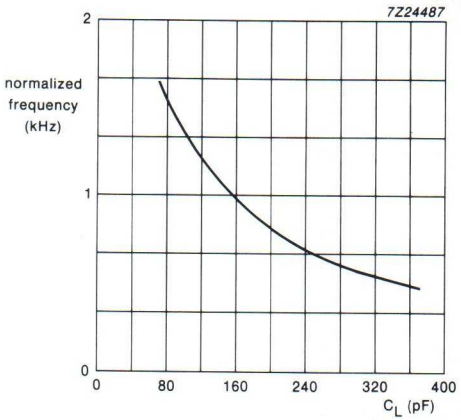


Fig.7 Typical normalized frequency as a function of keyboard load capacitance.

Philips Semiconductors

Data sheet	
status	Preliminary specification
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SAA4700
VPS dataline processor



FEATURES

- Adaptive sync slicer with buffered composite sync output VCS
- Adaptive data slicer
- Data rate clock regenerator
- Field selection and line 16 decoding
- Startcode and biphase check
- Data valid output
- Storage of data line information in a 40 bit register bank
- I²C-bus transmission

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 15 and 16)	4.5	5	5.5	V
I_P	total supply current	-	18	23	mA
$V_{i\ CVBS}$	CVBS input signal sync-to-white (peak-to-peak value)	0.5	1	1.4	V
T_{amb}	operating ambient temperature	0	-	+70	°C

GENERAL DESCRIPTION

The SAA4700 is a bipolar integrated circuit designed for use in dataline receivers and incorporates a dataline slicer and decoder. The slicer extracts the dataline signal from the video signal and regenerates the data clock. It also provides signals for the decoder in order to decode the binary data that is transmitted in line 16 of every first field of the composite video signal (video programming signal and video recording programming by Teletext, VPS and VPT systems). The decoded information out of words 5 and 11 to 14 is accessed via the built-in I²C-bus interface. This information then can be used for programming a video cassette recorder in order to start and stop a recording of a television program at the correct aligned time, regardless of a delay or extension in the transmission time of the required program.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA4700	18	DIL	plastic	SOT102

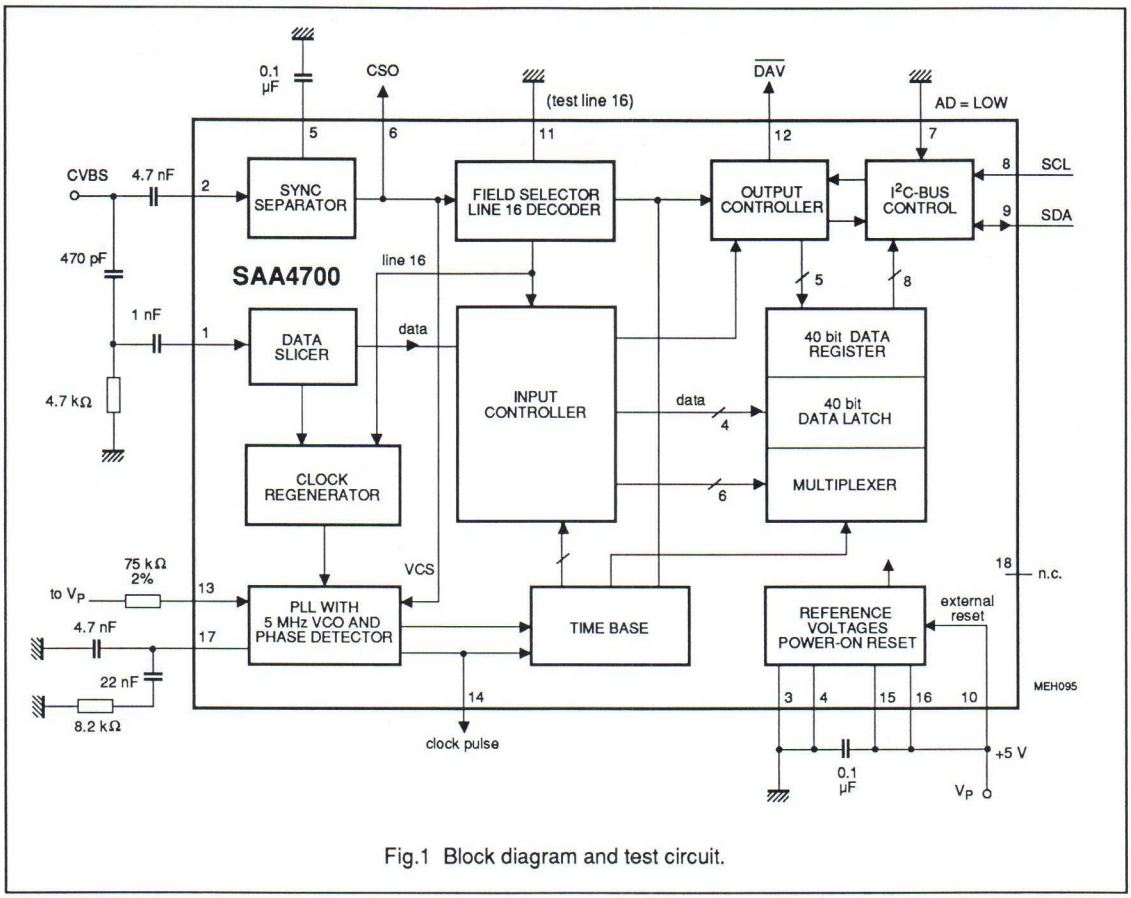


Fig.1 Block diagram and test circuit.

FUNCTIONAL DESCRIPTION

Dataline 16

The information in dataline 16 consists of fifteen 8-bit words; the total information content is shown in Table 1; and the organization of transmitted bytes is shown in Table 2.

Out of the fifteen possible 8-bit words the SAA4700 extracts words 5 and 11 to 14. The contents of these words can be read via the built-in I²C-bus interface. The circuit is fully transparent, thus each bit is transferred without modification with only the sequence of words being changed. Words 11 to 14 are transmitted first followed by word 5.

By evaluating the sliced sync signal the circuit can identify the beginning of dataline 16 in the first field. The dataline decoder stage releases the start code detector. When a correct start code is detected (for timing of start code detection see Fig.3) words 5 and 11 to 14 are decoded, checked for biphase errors and stored in a register bank. If no biphase error has occured, the contents of the register bank are transferred to a second register bank by the data valid control signal. If the system has been addressed, this transfer will be delayed until the next start or stop condition of the I²C-bus has been received.

The last bit of correct information on the dataline remains available until it is read via the I²C-bus. Once the stored information has been read it is considered to be no longer valid and the internal new data flag is reset. Subsequently, if the circuit is addressed, the only VPS data that will be sent back is "FFF to F". The same conditions apply after power-up when no data can be read out. New data is available after reception of another error-free dataline 16.

PINNING

SYMBOL	PIN	DESCRIPTION
CVBS	1	video signal input (CVBS from TV)
SYNC	2	sync amplitude input (CVBS from TV)
GND1	3	analog ground (0 V)
GND2	4	digital ground (0 V)
C_{black}	5	capacitor for black level
CSO	6	composite sync output
AD	7	address set input
SCL	8	I²C-bus clock line
SDA	9	I²C-bus data line
$\overline{RS}$	10	reset input active LOW
TP	11	test point for line 16 decoder
$\overline{DAV}$	12	data available output active LOW
R_{osc}	13	oscillator resistor for frequency adjustment
CP	14	test point clock pulse
V_{P1}	15	+5 V supply voltage (digital part)
V_{P2}	16	+5 V supply voltage (analog part)
C_{ph}	17	capacitor of phase detector
n.c.	18	not connected

PIN CONFIGURATION

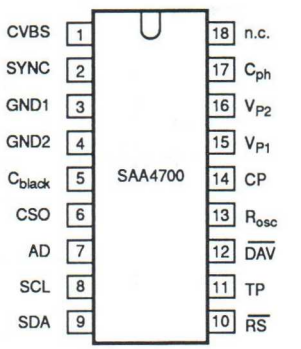


Fig.2 Pin configuration.

External reset
The circuit provides an internal power-on reset. When using this facility pin 10 should be connected to V_P or, if external reset (RESET = LOW) is to be used pin 10 should be prepared by connecting pin 10 via a 10 kΩ pull-up resistor to V_P.

Reset forces the following:

- I²C-bus not to acknowledge
- $\overline{DAV}$ output to go HIGH (pin 12)
- I²C-bus transfer register to "FFF"

CVBS input
The CVBS signal is applied to the sync separator (pin 2) via a decoupling capacitor and to the data slicer (pin1) via an RC high-pass filter. To enable proper storage of the sync value in the decoupling capacitor, the sync generator output resistance should not exceed 1 kΩ.

Black level
The capacitor connected to pin 5 stores the black level value for the adaptive sync slicer.

Composite sync output (CSO)
A composite sync output signal for customer application is provided (pin 6).

$\overline{DAV}$ output
The data available output pin 12 is set LOW after an error free dataline 16 is received. $\overline{DAV}$ returnes to HIGH after the beginning of the next first field. If no valid data is available $\overline{DAV}$ remains HIGH. A short duration pulse of 1 µs (Fig.5) is inserted at the beginning of dataline 16; it will ensure that a HIGH-to-LOW transmission occurs which can then be used for triggering.

5 MHz VCO and phase detector
The resistor connected between pin 13 and V_{P2} determines the current into the voltage controlled oscillator. The RC network connected to pin 17 acts as a low-pass filter for the phase detector.

Power supply
To prevent crosscoupling the circuit is provided with separate ground and supply pins for analog and digital parts (pins 3, 4, 15 and 16).

Table 1 Information per word in dataline 16

word number	content
1	run in
2	start code
3	program source identification (binary coded)
4	program source identification (ASCII sequential)
5	sound and VTR control information
6	program/test picture identification
7	internal information exchange
8	) address assignment of signal distribution
9	)
10	messages/commands
11	)
12	)
13	) VTR control / information
14	)
15	reserve

Table 2 VTR control information of dataline 16

| | VTR control information | | |

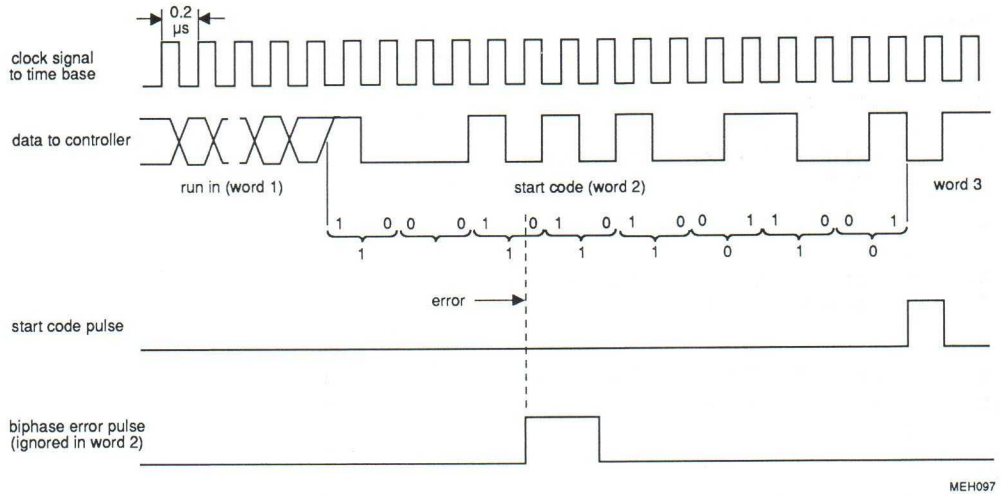


Fig.3 Timing diagram of start code detection.

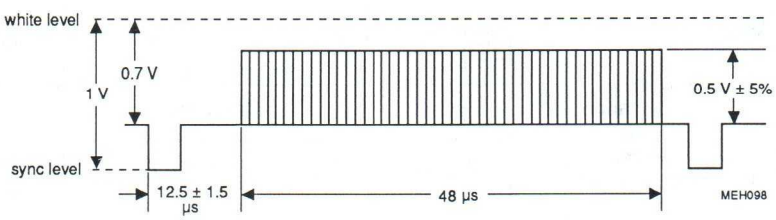


Fig.4 Timing diagram of dataline 16; modulation depth 71.4%.

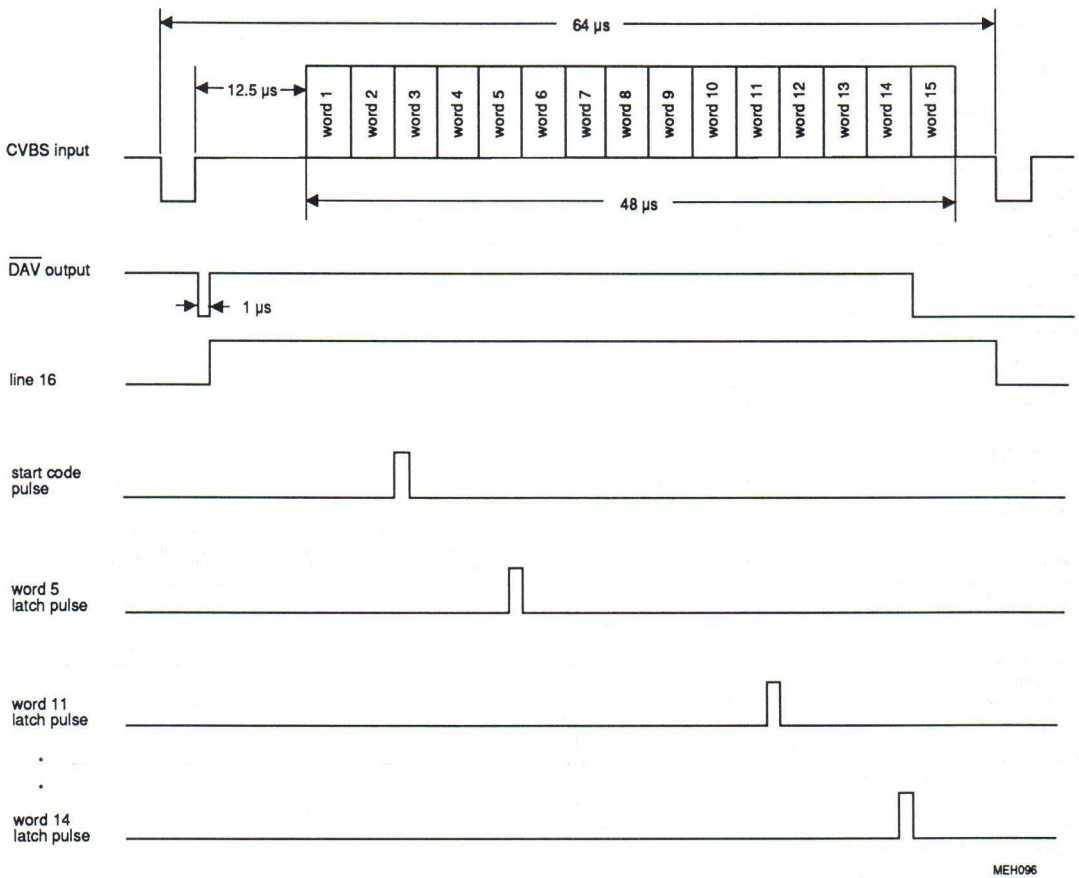


Fig.5 Timing diagram of the data available output and word latch pulses.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Ground pins 3 and 4 as well as supply pins 15 and 16 tied together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 15)	–0.5	6.0	V
V_{P2}	supply voltage (pin 16)	–0.5	6.0	V
T_{stg}	storage temperature range	–20	125	°C
T_{amb}	operating ambient temperature range	0	+70	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	78	K/W

CHARACTERISTICS

$V_{P1} = V_{P2} = 5$ V; $T_{amb} = 25$ °C; CVBS signal according to VPS and VPT standard and measurements taken in Fig.1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}, V_{P2}	supply voltages (pins 15 and 16)		4.5	5	5.5	V
I_P	total supply current	$I_{15} + I_{16}$	-	18	23	mA
CVBS and sync inputs (pins 1 and 2)						
$V_{i\ CVBS}$	CVBS input signal (peak-to-peak value)	sync-to-white note 1; Fig.4	0.5	1	1.4	V
$V_{i\ data}$	data input signal (peak-to-peak value, pin 1)	line 16; Fig.4	250	500	700	mV
$V_{i\ sync}$	sync input signal (peak-to-peak value, pin 2)		100	-	600	mV
R_S	source resistance		-	-	1	kΩ
Composite sync output (pin 6)						
V_{OL}	output voltage LOW		-	-	0.4	V
V_{OH}	output voltage HIGH		2.4	-	-	V
I_{OL}	output current LOW		-	-	200	µA
I_{OH}	output current HIGH		-	-	–500	µA
t_d	sync separator delay time		-	0.3	-	µs
$\overline{\text{DAV}}$ **output** (pin 12)		note 2				
V_{OL}	output voltage LOW		-	-	0.4	V
V_{OH}	output voltage HIGH		2.4	-	-	V
I_{OL}	output current LOW		-	-	500	µA
I_{OH}	output current HIGH		-	0.01	1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCL and SDA (pins 8 and 9)						
V_{IL}	input voltage LOW		-	-	1.5	V
V_{IH}	input voltage HIGH		3	-	-	V
I_I	input current	$0.9V_P$	-	-	±10	μA
C_I	input capacitance		-	-	10	pF
$V_{O\ ACK}$	output voltage during acknowledge on pin 9	I_{OL} = 3 mA	-	-	0.4	V
t_r	rise time		-	-	1	μs
t_f	fall time		-	-	0.3	μs
$t_{p\,L}$	pulse duration LOW		4.7	-	-	μs
$t_{p\,H}$	pulse duration HIGH		4.0	-	-	μs
SCL	clock frequency		-	-	100	kHz
AD set input (pin 7)		note 2				
V_{IL}	input voltage LOW	address 23H	0	-	0.4	V
V_{IH}	input voltage HIGH	address 21H	2.4	-	V_P	V
RESET input (pin 10)		note 2				
V_{IL}	input voltage LOW	reset active	-	-	0.4	V
V_{IH}	input voltage HIGH	reset non-active	2.4	-	-	V
I_{IL}	input current LOW		-	-	−10	μA
I_{IH}	input current HIGH		-	0.01	1	μA

Notes to the characteristics

1. With standard sync and data amplitude of 68% to 75% black-white.
2. If the open collector output $\overline{DAV}$ is used, a pull-up resistor to V_{P1} is necessary.

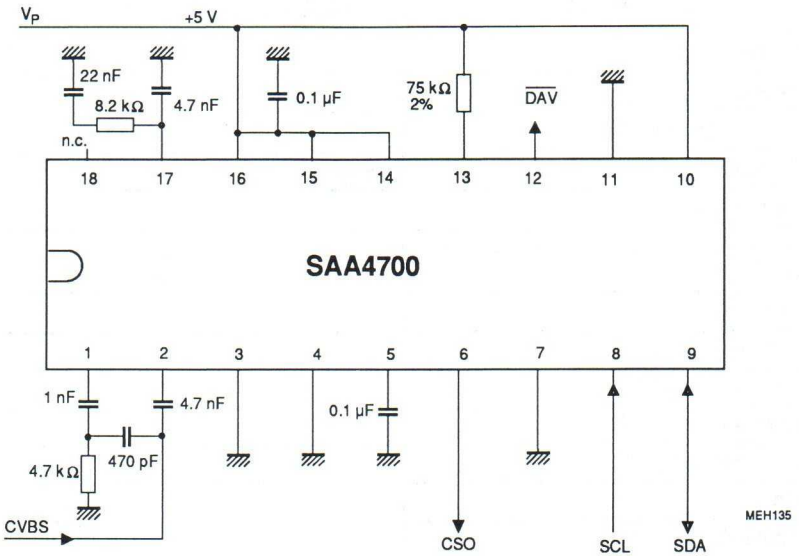


Fig.6 Application circuit.

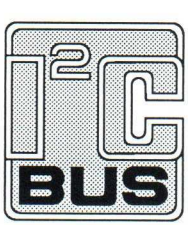
I²C-BUS FORMAT

S	SLAVE ADDRESS	A	DATA	A	DATA	A	DATA	A	DATA	A	DATA	P

S	=	start condition
SLAVE ADDRESS	=	**0010 0001 or 0010 0011** for set input AD = HIGH respectively LOW on pin 7 (the circuit is only a slave transmitter)
A	=	acknowledge, generated by the slave or the master
DATA	=	five data bytes, see words in Table 1
P	=	stop condition respectivily non-acknowledge by the microcontroller

Remarks to I²C-bus transmission

- the MSB of each word is transmitted first
- there is no restriction on the number of words to be transmitted, but if more than five words are requested, the following content will be "FF" continuously.
- Normally every dataline transmission has to be ended with STOP condition by non-acknowledge of the controller.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1991

SAA4700T
VPS dataline processor

FEATURES

- Adaptive sync slicer with buffered composite sync output VCS
- Adaptive data slicer
- Data rate clock regenerator
- Field selection and line 16 decoding
- Startcode and biphase check
- Data valid output
- Storage of data line information in a 40 bit register bank
- I²C-bus transmission

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 17 and 18)	4.5	5	5.5	V
I_P	total supply current	-	18	23	mA
$V_{i\ CVBS}$	CVBS input signal sync-to-white (peak-to-peak value)	0.5	1	1.4	V
T_{amb}	operating ambient temperature	0	-	+70	°C

GENERAL DESCRIPTION

The SAA4700T is a bipolar integrated circuit designed for use in dataline receivers and incorporates a dataline slicer and decoder. The slicer extracts the dataline signal from the video signal and regenerates the data clock. It also provides signals for the decoder in order to decode the binary data that is transmitted in line 16 of every first field of the composite video signal (video programming signal and video recording programming by Teletext, VPS and VPT systems). The decoded information out of words 5 and 11 to 14 is accessed via the built-in I²C-bus interface. This information then can be used for programming a video cassette recorder in order to start and stop a recording of a television program at the correct aligned time, regardless of a delay or extension in the transmission time of the required program.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA4700T	20	mini-pack	plastic	SOT163A

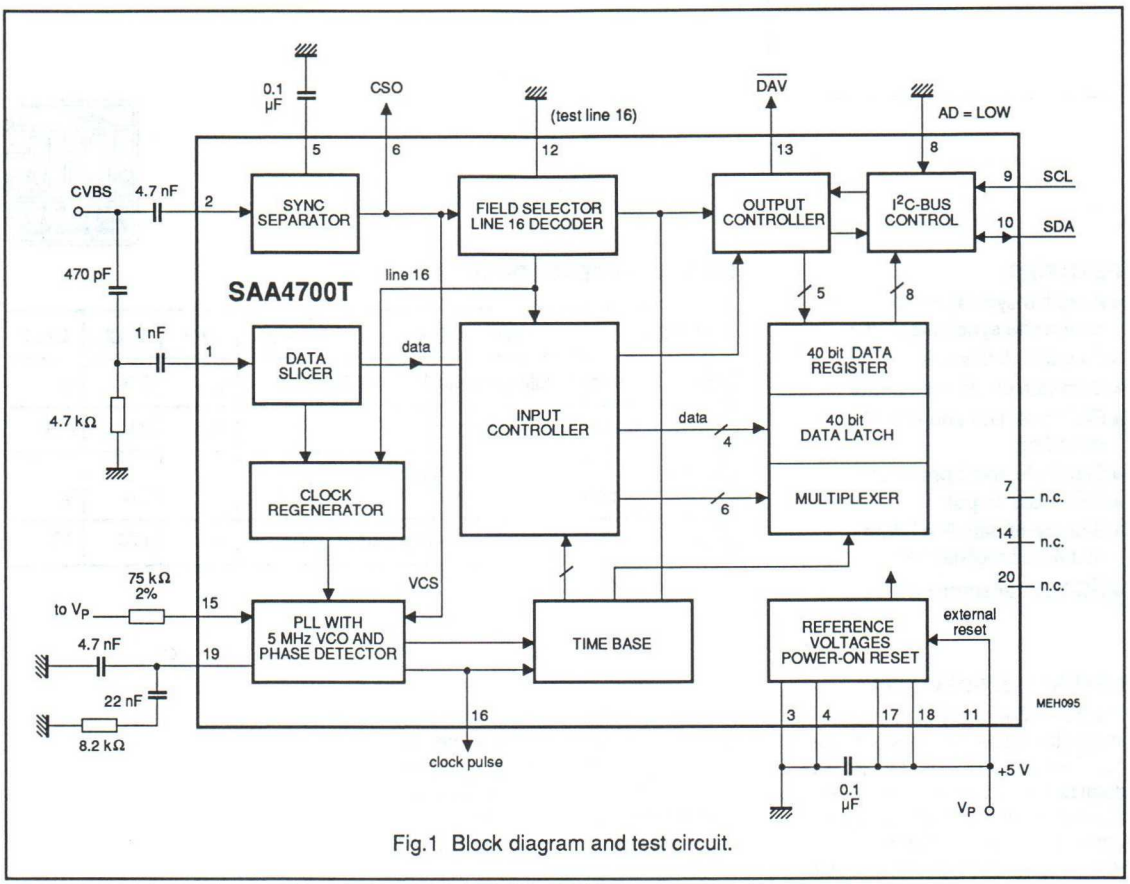


Fig.1 Block diagram and test circuit.

FUNCTIONAL DESCRIPTION

Dataline 16

The information in dataline 16 consists of fifteen 8-bit words; the total information content is shown in Table 1; and the organization of transmitted bytes is shown in Table 2.

Out of the fifteen possible 8-bit words the SAA4700T extracts words 5 and 11 to 14. The contents of these words can be read via the built-in I²C-bus interface. The circuit is fully transparent, thus each bit is transferred without modification with only the sequence of words being changed. Words 11 to 14 are transmitted first followed by word 5.

By evaluating the sliced sync signal the circuit can identify the beginning of dataline 16 in the first field. The dataline decoder stage releases the start code detector. When a correct start code is detected (for timing of start code detection see Fig.3) words 5 and 11 to 14 are decoded, checked for biphase errors and stored in a register bank. If no biphase error has occured, the contents of the register bank are transferred to a second register bank by the data valid control signal. If the system has been addressed, this transfer will be delayed until the next start or stop condition of the I²C-bus has been received.

The last bit of correct information on the dataline remains available until it is read via the I²C-bus. Once the stored information has been read it is considered to be no longer valid and the internal new data flag is reset. Subsequently, if the circuit is addressed, the only VPS data that will be sent back is "FFF to F". The same conditions apply after power-up when no data can be read out. New data is available after reception of another error-free dataline 16.

PINNING

SYMBOL	PIN	DESCRIPTION
CVBS	1	video signal input (CVBS from TV)
SYNC	2	sync amplitude input (CVBS from TV)
GND1	3	analog ground (0 V)
GND2	4	digital ground (0 V)
C_{black}	5	capacitor for black level
CSO	6	composite sync output
n.c.	7	not connected
AD	8	address set input
SCL	9	I²C-bus clock line
SDA	10	I²C-bus data line
$\overline{RS}$	11	reset input active LOW
TP	12	test point for line 16 decoder
$\overline{DAV}$	13	data available output active LOW
n.c.	14	not connected
R_{osc}	15	oscillator resistor for frequency adjustment
CP	16	test point clock pulse
V_{P1}	17	+5 V supply voltage (digital part)
V_{P2}	18	+5 V supply voltage (analog part)
C_{ph}	19	capacitor of phase detector
n.c.	20	not connected

PIN CONFIGURATION

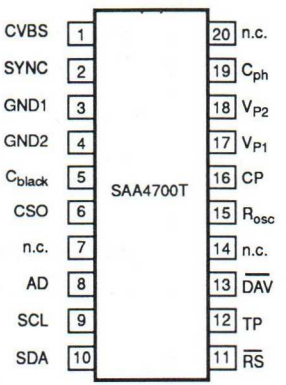


Fig.2 Pin configuration.

External reset
The circuit provides an internal power-on reset. When using this facility pin 11 should be connected to V_P or, if external reset (RESET = LOW) is to be used pin 11 should be prepared by connecting pin 11 via a 10 kΩ pull-up resistor to V_P.

Reset forces the following:

- I²C-bus not to acknowledge
- $\overline{DAV}$ output to go HIGH (pin 13)
- I²C-bus transfer register to "FFF"

CVBS input
The CVBS signal is applied to the sync separator (pin 2) via a decoupling capacitor and to the data slicer (pin1) via an RC high-pass filter. To enable proper storage of the sync value in the decoupling capacitor, the sync generator output resistance should not exceed 1 kΩ.

Black level
The capacitor connected to pin 5 stores the black level value for the adaptive sync slicer.

Composite sync output (CSO)
A composite sync output signal for customer application is provided (pin 6).

$\overline{DAV}$ output
The data available output pin 13 is set LOW after an error free data line 16 is received. $\overline{DAV}$ returnes to HIGH after the beginning of the next first field. If no valid data is available $\overline{DAV}$ remains HIGH.
A short duration pulse of 1 µs (Fig.5) is inserted at the beginning of dataline 16; it will ensure that a HIGH-to-LOW transmission occurs which can then be used for triggering.

5 MHz VCO and phase detector
The resistor connected between pin 15 and V_{P2} determines the current into the voltage controlled oscillator. The RC network connected to pin 19 acts as a low-pass filter for the phase detector.

Power supply
To prevent crosscoupling the circuit is provided with separate ground and supply pins for analog and digital parts (pins 3, 4, 17 and 18).

Table 1 Information per word in dataline 16

word number	content
1	run in
2	start code
3	program source identification (binary coded)
4	program source identification (ASCII sequential)
5	sound and VTR control information
6	program/test picture identification
7	internal information exchange
8	) address assignment of signal distribution
9	)
10	messages/commands
11	)
12	)
13	) VTR control / information
14	)
15	reserve

Table 2 VTR control information of dataline 16

| | VTR control information | | |

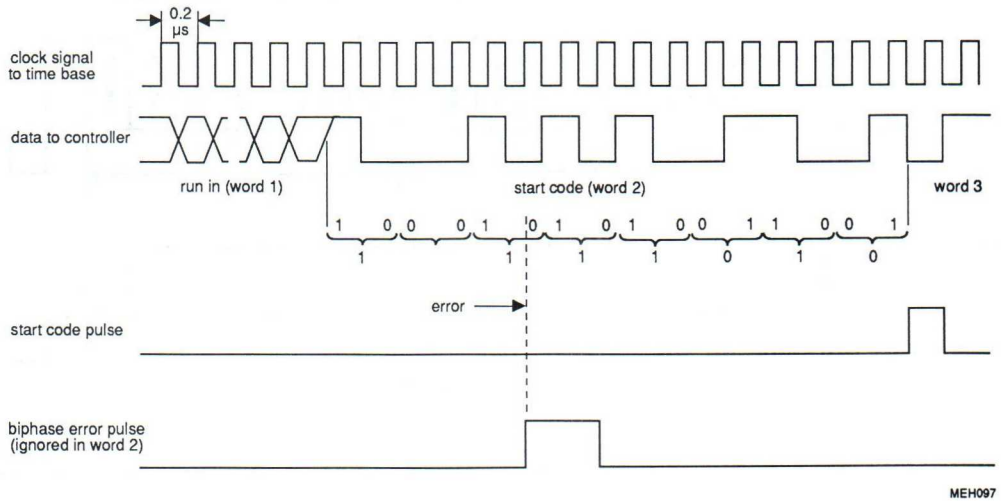


Fig.3 Timing diagram of start code detection.

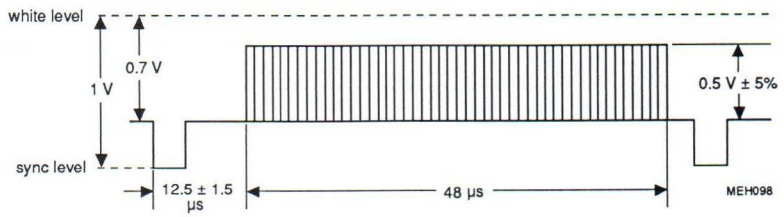


Fig.4 Timing diagram of dataline 16; modulation depth 71.4%.

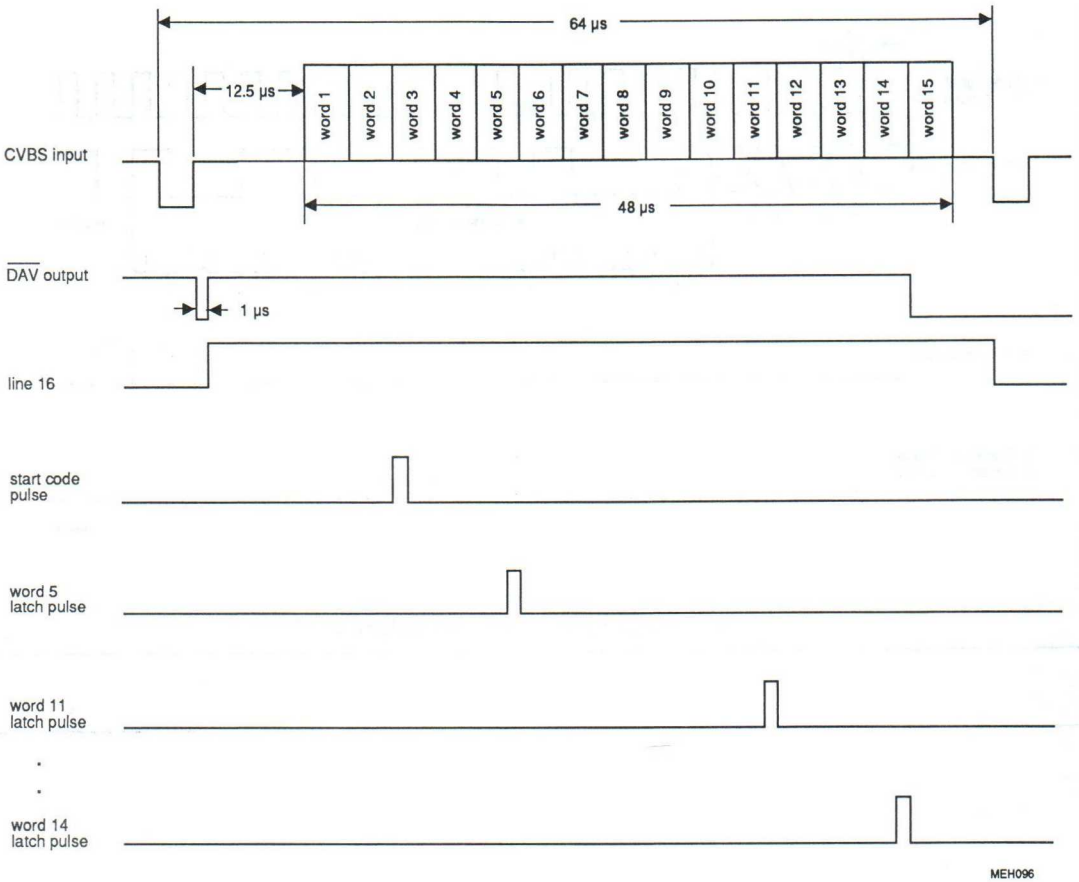


Fig.5 Timing diagram of the data available output and word latch pulses.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Ground pins 3 and 4 as well as supply pins 17 and 18 tied together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 17)	–0.5	6.0	V
V_{P2}	supply voltage (pin 18)	–0.5	6.0	V
T_{stg}	storage temperature range	–20	125	°C
T_{amb}	operating ambient temperature range	0	+70	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	130	K/W

CHARACTERISTICS

$V_{P1} = V_{P2} = 5$ V; $T_{amb} = 25$ °C; CVBS signal according to VPS and VPT standard and measurements taken in Fig.1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}, V_{P2}	supply voltages (pins 17 and 18)		4.5	5	5.5	V
I_P	total supply current	$I_{17} + I_{18}$	-	18	23	mA
CVBS and sync inputs (pins 1 and 2)						
$V_{i\ CVBS}$	CVBS input signal (peak-to-peak value)	sync-to-white note 1; Fig.4	0.5	1	1.4	V
$V_{i\ data}$	data input signal (peak-to-peak value, pin 1)	line 16; Fig.4	250	500	700	mV
$V_{i\ sync}$	sync input signal (peak-to-peak value, pin 2)		100	-	600	mV
R_S	source resistance		-	-	1	kΩ
Composite sync output (pin 6)						
V_{OL}	output voltage LOW		-	-	0.4	V
V_{OH}	output voltage HIGH		2.4	-	-	V
I_{OL}	output current LOW		-	-	200	µA
I_{OH}	output current HIGH		-	-	–500	µA
t_d	sync separator delay time		-	0.3	-	µs
$\overline{\text{DAV}}$ **output** (pin 13)		note 2				
V_{OL}	output voltage LOW		-	-	0.4	V
V_{OH}	output voltage HIGH		2.4	-	-	V
I_{OL}	output current LOW		-	-	500	µA
I_{OH}	output current HIGH		-	0.01	1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCL and SDA (pins 9 and 10)						
V_{IL}	input voltage LOW		-	-	1.5	V
V_{IH}	input voltage HIGH		3	-	-	V
I_I	input current	$0.9V_P$	-	-	±10	μA
C_I	input capacitance		-	-	10	pF
$V_{O\ ACK}$	output voltage during acknowledge on pin 10	I_{OL} = 3 mA	-	-	0.4	V
t_r	rise time		-	-	1	μs
t_f	fall time		-	-	0.3	μs
$t_{p\,L}$	pulse duration LOW		4.7	-	-	μs
$t_{p\,H}$	pulse duration HIGH		4.0	-	-	μs
SCL	clock frequency		-	-	100	kHz
AD set input (pin 8)		note 2				
V_{IL}	input voltage LOW	address 23H	0	-	0.4	V
V_{IH}	input voltage HIGH	address 21H	2.4	-	V_P	V
RESET input (pin 11)		note 2				
V_{IL}	input voltage LOW	reset active	-	-	0.4	V
V_{IH}	input voltage HIGH	reset non-active	2.4	-	-	V
I_{IL}	input current LOW		-	-	−10	μA
I_{IH}	input current HIGH		-	0.01	1	μA

Notes to the characteristics

1. With standard sync and data amplitude of 68% to 75% black-white.
2. If the open collector output $\overline{DAV}$ is used, a pull-up resistor to V_{P1} is necessary.

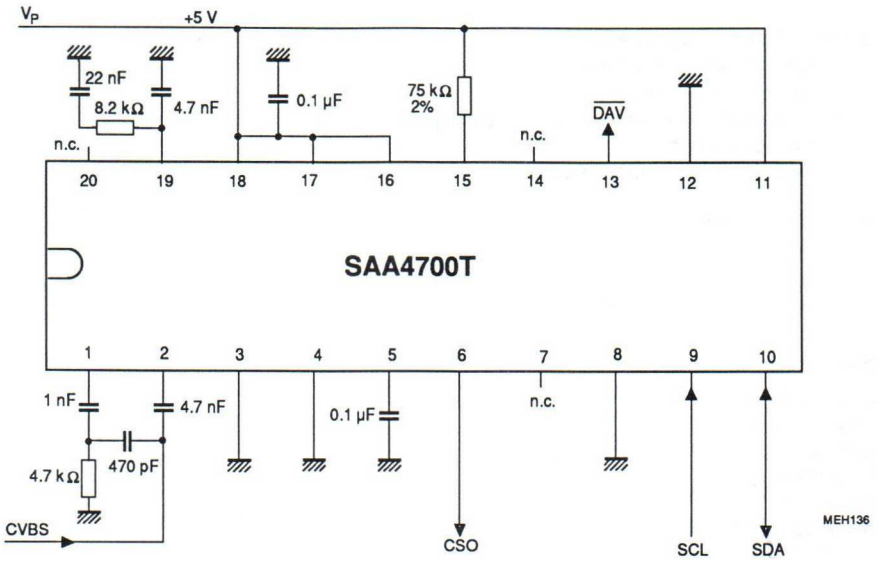


Fig.6 Application circuit.

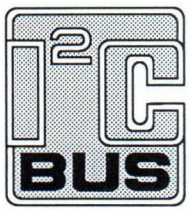
I²C-BUS FORMAT

S	SLAVE ADDRESS	A	DATA	A	DATA	A	DATA	A	DATA	A	DATA	P

S	=	start condition
SLAVE ADDRESS	=	**0010 0001 or 0010 0011** for set input AD = HIGH respectively LOW on pin 8 (the circuit is only a slave transmitter)
A	=	acknowledge, generated by the slave or the master
DATA	=	five data bytes, see words in Table 1
P	=	stop condition respectivily non-acknowledge by the microcontroller

Remarks to I²C-bus transmission

- the MSB of each word is transmitted first
- there is no restriction on the number of words to be transmitted, but if more than five words are requested, the following content will be "FF" continuously.
- Normally every dataline transmission has to be ended with STOP condition by non-acknowledge of the controller.



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NOise Reduction IC SAA4940H

FEATURES

- Constant and motion adaptive noise reduction
- Cross colour and cross luminance reduction
- Colour generation for side panels, box or border
- Possibility for cross-fade between two synchronized video inputs
- Prepared for Multi-PIP applications
- Split screen noise reduction inside or outside box
- Solarization
- Internal bypass for 4:4:4 format

GENERAL DESCRIPTION

The NOise Reduction IC (NORIC) is intended for noise reduction purposes. Together with the BENDIC (SAA7158WP) it is designed to operate in an 100/120 Hz environment. However, an application with 50/60 Hz environment is possible. The NORIC is designed to co-operate with an 8051 type of microprocessor, the BENDIC and Texas Instruments field memories plus memory/sync controller, but other configurations may be applicable.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage range	4.75	5.25	V
V_{OH}	output voltage	2.6	3.4	V
T_{amb}	operating ambient temperature range	0	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA4940H	80	QFP80	plastic	SOT318-2

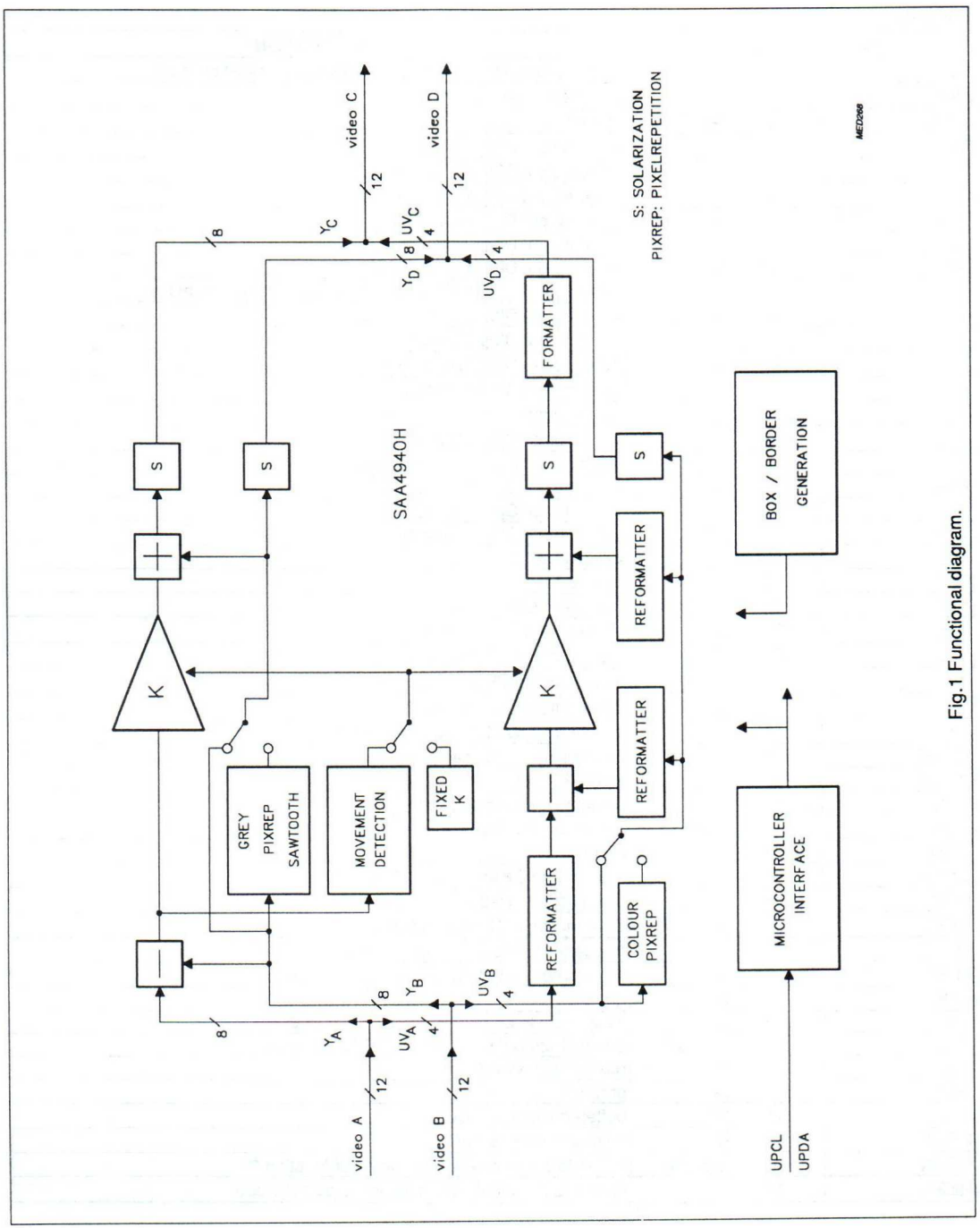


Fig.1 Functional diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
Y_{D0}	1	O	video output D[0], Y data, bit 0 (LSB = least significant bit)
V_{DD}	2	–	positive supply voltage
GND	3	–	ground
Y_{D1}	4	O	video output D[1], Y data, bit 1
Y_{D2}	5	O	video output D[2], Y data, bit 2
Y_{D3}	6	O	video output D[3], Y data, bit 3
Y_{D4}	7	O	video output D[4], Y data, bit 4
Y_{D5}	8	O	video output D[5], Y data, bit 5
Y_{D6}	9	O	video output D[6], Y data, bit 6
Y_{D7}	10	O	video output D[7], Y data, bit 7 (MSB = most significant bit)
UV_{D0}	11	O	video output D[8], UV data, bit 0
UV_{D1}	12	O	video output D[9], UV data, bit 1
UV_{D2}	13	O	video output D[10], UV data, bit 2
UV_{D3}	14	O	video output D[11], UV data, bit 3
UV_{C0}	15	O	video output C[8], UV data, bit 0
UV_{C1}	16	O	video output C[9], UV data, bit 1
UV_{C2}	17	O	video output C[10], UV data, bit 2
UV_{C3}	18	O	video output C[11], UV data, bit 3
Y_{C0}	19	O	video output C[0], Y data, bit 0 (LSB)
Y_{C1}	20	O	video output C[1], Y data, bit 1
Y_{C2}	21	O	video output C[2], Y data, bit 2
GND	22	–	ground
V_{DD}	23	–	positive supply voltage
Y_{C3}	24	O	video output C[3], Y data, bit 3
Y_{C4}	25	O	video output C[4], Y data, bit 4
Y_{C5}	26	O	video output C[5], Y data, bit 5
Y_{C6}	27	O	video output C[6], Y data, bit 6
Y_{C7}	28	O	video output C[7], Y data, bit 7 (MSB)
BOXE	29	O	external boxing signal
INVO	30	O	inverted version of INVI
INVI	31	I	signal to be inverted to INVO
SAWN	32	I(p-up)	control pin for sawtooth at video C and D *
GND	33	–	ground
ORIB	34	I	signal to be ORed with ORIA to ORO
ORIA	35	I	signal to be ORed with ORIB to ORO
ORO	36	O	OR-function of ORIA and ORIB
FLOP	37	O	frequency divide by 2 output of FLIP
FLIP	38	I	signal to be frequency divided by 2 to FLIP
GND	39	–	ground
CL	40	I	clock input to be buffered to CIO and CLO
CIO	41	O(3-st)	3-state buffered version of CL (FBWN control)
V_{DD}	42	–	positive supply voltage
GND	43	–	ground
CLO	44	O	buffered version of CL
FBWN	45	I	3-state control for CIO
RECN	46	I(p-up)	recirculate-not for external control of function **
RE2	47	I	read-enable signal indicating active part of video

SYMBOL	PIN	TYPE	DESCRIPTION
BLN	48	I	blanking-not used for colour format phase reference
RSTR	49	I	reset-read signal for reset of communication phase
UPCL	50	I	microprocessor communication clock
UPDA	51	I	microprocessor communication data
GND	52	–	ground
CLK	53	I	system clock
GND	54	–	ground
Y_{A7}	55	I	video input A[7], Y data, bit 7 (MSB)
Y_{A6}	56	I	video input A[6], Y data, bit 6
Y_{A5}	57	I	video input A[5], Y data, bit 5
Y_{A4}	58	I	video input A[4], Y data, bit 4
Y_{A3}	59	I	video input A[3], Y data, bit 3
Y_{A2}	60	I	video input A[2], Y data, bit 2
Y_{A1}	61	I	video input A[1], Y data, bit 1
GND	62	–	ground
V_{DD}	63	–	positive supply voltage
Y_{A0}	64	I	video input A[0], Y data, bit 0 (LSB)
UV_{A3}	65	I	video input A[11], UV data, bit 3
UV_{A2}	66	I	video input A[10], UV data, bit 2
UV_{A1}	67	I	video input A[9], UV data, bit 1
UV_{A0}	68	I	video input A[8], UV data, bit 0
UV_{B3}	69	I	video input B[11], UV data, bit 3
UV_{B2}	70	I	video input B[10], UV data, bit 2
UV_{B1}	71	I	video input B[9], UV data, bit 1
UV_{B0}	72	I	video input B[8], UV data, bit 0
Y_{B7}	73	I	video input B[7], Y data, bit 7 (MSB)
Y_{B6}	74	I	video input B[6], Y data, bit 6
Y_{B5}	75	I	video input B[5], Y data, bit 5
Y_{B4}	76	I	video input B[4], Y data, bit 4
Y_{B3}	77	I	video input B[3], Y data, bit 3
Y_{B2}	78	I	video input B[2], Y data, bit 2
Y_{B1}	79	I	video input B[1], Y data, bit 1
Y_{B0}	80	I	video input B[0], Y data, bit 0 (LSB)

* SAWN pull up resistor internal 5 kΩ

** RECN pull up resistor internal 50 kΩ

I = Input

O = Output

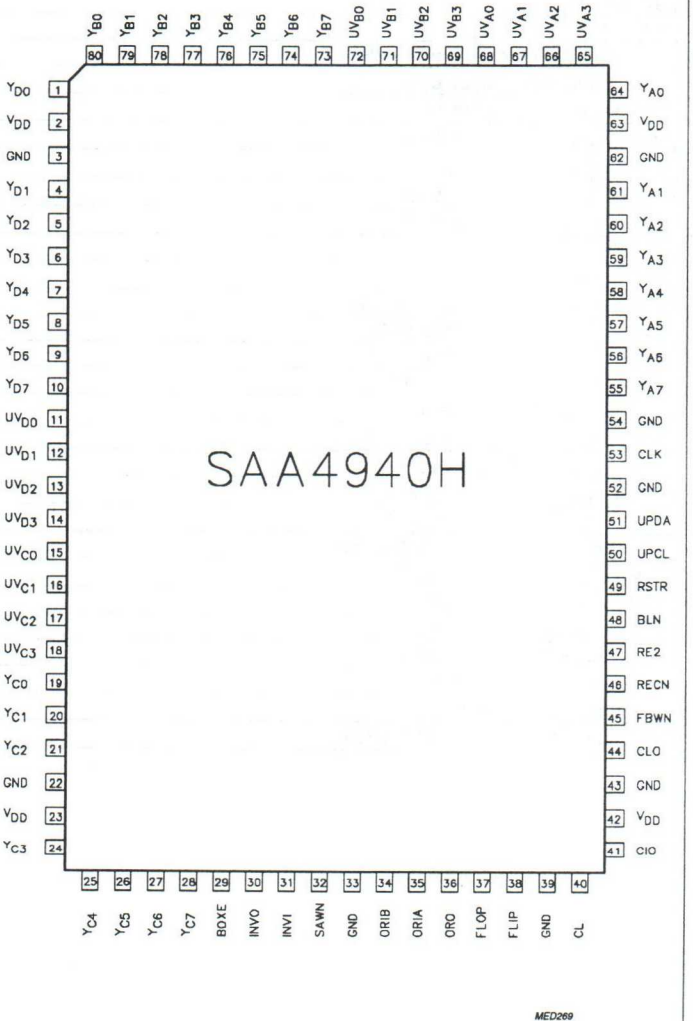


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The main function of the NORIC is shown in Fig.1. The video A and B busses are split into Y data and UV data, which will each have its own processing. Combination of the data from video A and B is carried out by the subtractor/multiplier/adder sections. Video C will therefore be a linear combination of video A and B data, where video D is mainly a copy of video B, but with appropriate processing delay. Grey/colour insert, pixel repetition and sawtooth insert are operated on the video B sources. With K set to 1 both video C and D will be affected by these functions. For noise reduction, K may be fixed for constant noise level reduction or dependent on movement detection for motion adaptive noise reduction.

NOISE REDUCTION

Principle

A recursive algorithm with an external field memory as delay element, is used in accordance with the basic scheme of Fig.3.

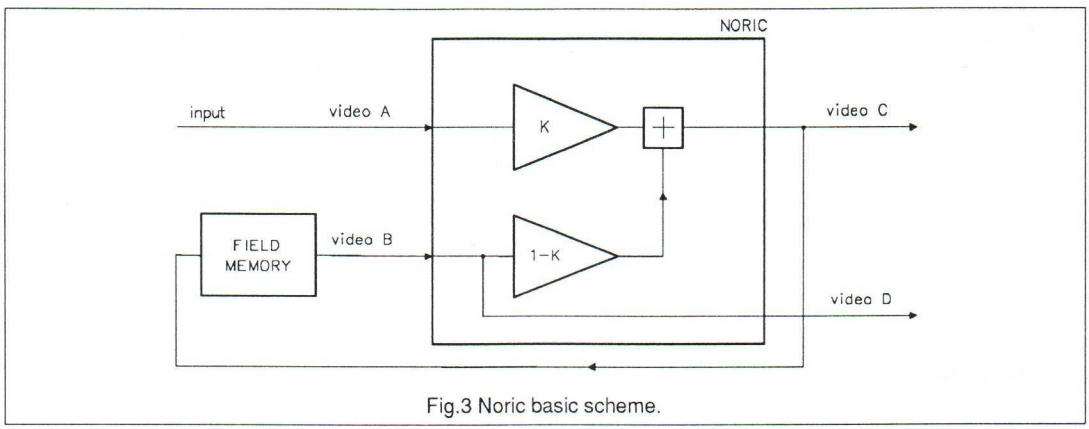


Fig.3 Noric basic scheme.

To save the cost of one of the two multipliers, the basic scheme is converted into the scheme of Fig.4.

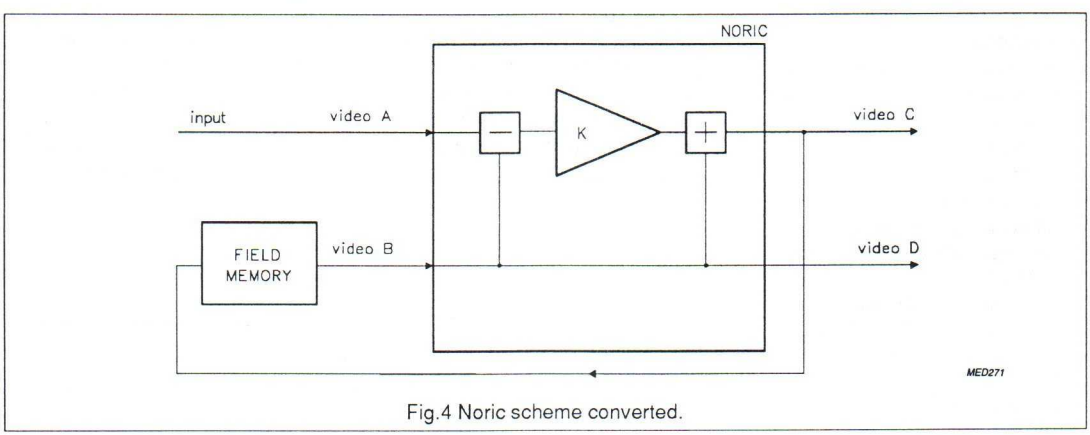


Fig.4 Noric scheme converted.

The transfer function in z-domain of the recursive loop (from video A to video C with incorporated field memory) is:

video C/video A = $K/(1 - (1 - K) \times z^{-1})$

The delay operator z^{-1} is here equivalent to 1 field delay.

The impulse response of video C / video A is an indication for the fading of video C, when e. g. video A has one field white and all others black.

It is seen that the delay of the video C data is low with K is small, so video data from a certain field of video A will remain visible in many fields of video C. This implies a high degree of noise reduction, but it is only appropriate where no movement occurs, otherwise wiping of images is seen. Therefore the factor K should be adapted to the level of movement.

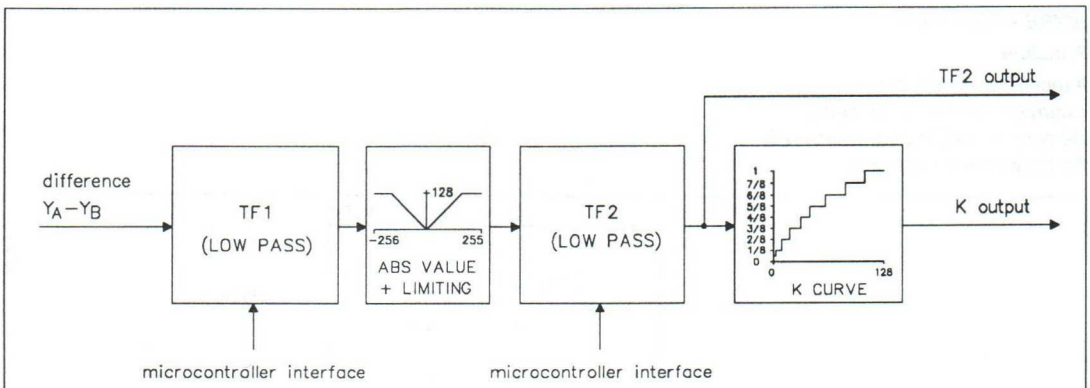


Fig.5 Movement detection.

Implementation

The noise reduction function is based upon the control of the K-factor that interpolates between the direct input video A and the field delayed (already noise reduced) input video B.

The setting of the K-factor is dependent on the operating mode:

a) K is a constant, which can be set to 0, 1/32, 1/16, 1/8, 2/8, 3/8, 4/8, 5/8, 6/8, 7/8 and 8/8.

b) K is dependent on (an eventually filtered version of) the absolute difference in luminance between the output of the field memory and the input.
This dependency is staircase-like, of which the start of each step can be programmed.
An example is shown in Fig.6, where the edges of the steps are programmed as:

K_step0 = 3	(step from K = 1/16 to K = 1/8; 3 x weight of 1)
K_step1 = 7	(step from K = 1/8 to K = 2/8; 7 x weight of 1)
K_step2 = 16	(step from K = 2/8 to K = 3/8; 8 x weight of 2)
K_step3 = 28	(step from K = 3/8 to K = 4/8; 14 x weight of 2)
K_step4 = 44	(step from K = 4/8 to K = 5/8; 11 x weight of 4)
K_step5 = 64	(step from K = 5/8 to K = 6/8; 16 x weight of 4)
K_step6 = 88	(step from K = 6/8 to K = 7/8; 11 x weight of 8)
K_step7 = 120	(step from K = 7/8 to K = 8/8; 15 x weight of 8)

c) K can be switched from fixed (situation a) to adaptive (situation b) inside or outside a rectangular box. This enables the possibility for a split screen of the noise reduction function.

d) K is 0 during 'recirculate', which may be inside or outside a rectangular box. This enables selective updating of the field memory contents, to be used e. g. for multi-PIP.

In the adaptive mode, the circuit of Fig.5 is used for the determination of the K value for each pixel in the video. The (horizontal) low pass filters are useful to discriminate better between noise and movement. Also curves can be implemented that will pass cross-luminance patterns as noise, which will then get reduced. In chapter 'NORIC control' the various transfer functions of TF1 and TF2 are listed.

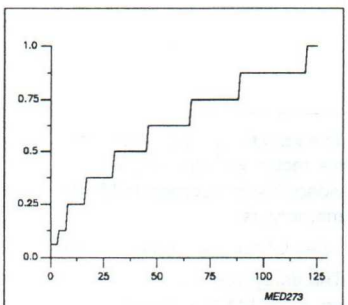


Fig.6 K curve example.

Cross colour and cross luminance reduction

As a side effect of the noise reduction algorithm, disturbances of cross colour and cross luminance will also be reduced.

Cross colour is reduced because the movement detection (that operates on luminance only) will not detect any movement in the cross colour pattern and therefore averages the colour contents over many fields of video. As the colour vector in the cross colour patterns is in various phases (0, 90, 180 and 270 degrees) in successive fields, the average of many fields of video will have significantly less of the cross colour pattern.

Cross luminance is reduced if the cross luminance pattern is not detected as movement by the movement detection algorithm. This can be implemented by using a (horizontal) filter characteristic that has a zero in the frequency area of the luminance pattern. As the cross luminance pattern is in various phases (0, 90, 180 and 270 degrees) in successive fields, the average of many fields of video will have significantly less of the cross pattern.

Colour and pixel repetition generation for side panels, box or border

A constant colour value can be generated and led to the outputs video C and video D. The colour value is set by the microprocessor, by coding the luminance value in 8 bits and the U and V values in their most significant 4 bits each. The least significant U and V bits remain 0. The number of colours to be generated is therefore 64 k.

Side panels are generated where the memory outputs are inactive (RE LOW). The side panels can use the colour generation as described above or maintain the last active video data from the memory on each video line (pixel repetition).

A rectangular box can be generated, in which colour, pixel repetition or a recirculate function can be performed. This rectangular box is defined by the coordinates of the left-upper edge (hor_start_box, vert_start_box) and the right_lower edge (hor_stop_box, vert_stop_box).

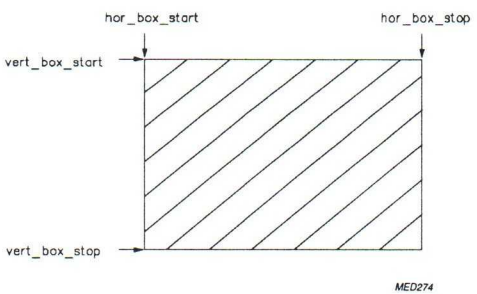


Fig.7 Box dimension and position.

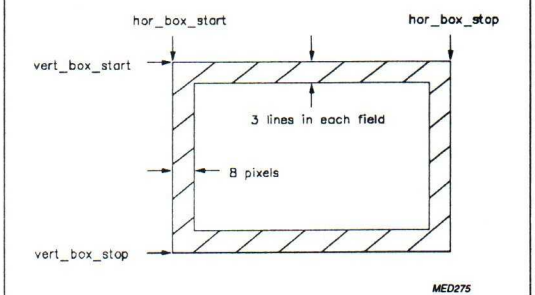


Fig.8 Border dimension and position.

Instead of a rectangular box, a border can be generated, specified in accordance with the parameters in Fig.8. This provision can be used e. g. to generate a border around a 'Picture In Picture' picture.

Cross-fade between two video inputs

If video A and video B are (synchronized) video sources, an interpolation to the video C output is made with a K setting between 0 and 1. Cross fading is therefore a matter of varying K from 0 to 1 or from 1 to 0 by the microprocessor.

Use of NORIC for Multi-PIP

Multi-PIP operation consists of selective updating the memory contents, for the size of a PIP picture. The NORIC can help this process by having recirculated all the memory contents, except a part within a rectangular box.

Implementation of noise reduction split screen

To demonstrate the result of the noise reduction it is easier to show part of the picture with, and the rest of the picture without noise reduction. The rectangular box (not border) can therefore be used to switch between NR on and off. The box may e. g. cover the right half of the picture.

Horizontal sawtooth generation

For easy testing of the board, the luminance part of the video C bus can be applied with a horizontal synchronous sawtooth, that has an increment in every 4 pixels. This mode can be set by either the microprocessor or by applying a LOW level on the SAWN input. This input has an internal pull-up, thus short-circuiting this pin to ground for testing is sufficient, it overrules all other modes in the NORIC.

Solarization

This function reduces the internal signal quantization from 8 to 4 bits. Of the luminance signal Y the lower four bits are constantly kept at 1 which gives a slight positive offset in brightness. The four lower bits of U and V are made equal to the sign-bit which gives a slight decrease in saturation.

Bypass of YUV 4:4:4 data

Although the data from the video A bus undergoes reformatting and formatting operations, normally used to operate on encoded UV data, the NORIC can be controlled to have a transparent throughput from video A to video C and from video B to video D. The data will remain having a delay of 12 clock cycles. All other features in the NORIC are excluded in this mode.

NORIC control

Table 1 Write registers

ADDRESS (HEX)	NAME	BIT
10H	K_step 01	bit 7 to bit 4: K_step 1[3:0]
		bit 3 to bit 0: K_step 0[3:0]
11H	K_step 23	bit 7 to bit 4: K_step 3[3:0]/2
		bit 3 to bit 0: K_step 2[3:0]/2
12H	K_step 45	bit 7 to bit 4: K_step 5[3:0]/4
		bit 3 to bit 0: K_step 4[3:0]/4
13H	K_step 67	bit 7 to bit 4: K_step 7[3:0]/8
		bit 3 to bit 0: K_step 6[3:0]/8
14H	Kfixed	bit 7: ad/fix
		bit 6: up/box
		bit 5 to bit 0: fixed_K[5:0]
15H	Tfilter12	bit 7 to bit 3: Tfilter2_select[5:0]
		bit 2 to bit 0: Tfilter1_select[1:0]
16H	hbox_start	bit 7 to bit 0: hor_box_start[7:0]
17H	hbox_stop	bit 7 to bit 0: hor_box_stop[7:0]
18H	vbox_start_l	bit 7 to bit 0: vert_box_start[7:0] with bit 8 = 0
19H	vbox_start_h	bit 7 to bit 0: vert_box_start[7:0] with bit 8 = 1
1AH	vbox_stop_l	bit 7 to bit 0: vert_box_stop[7:0] with bit 8 = 0
1BH	vbox_stop_h	bit 7 to bit 0: vert_box_stop[7:0] with bit 8 = 1
1CH	display_def	bit 7: dir_le
		bit 6: sola
		bit 5: colour/pixrep
		bit 4 to bit 2: output_mux[2:0]
		bit 1 to bit 0: bln_delay[1:0]
1DH	box_def	bit 7: v_cnt_en
		bit 6: border
		bit 5: inv_box
		bit 4: en_box_ext
		bit 3: en_box_col
		bit 2: en_box_rec
		bit 1: en_box
		bit 0: zero
1EH	Y_value	bit 7 to bit 0: grey_value[7:0]
1FH	UV_value	bit 7 to bit 4: U_value[3:0]/16
		bit 3 to bit 0: V_value[3:0]/16

The function of the bits in the control datawords is explained below:

K_step 0[3:0]	step in adaptive curve from K = 1/16 to K = 1/8; weight of 1
K_step 1[3:0]	step in adaptive curve from K = 1/8 to K = 2/8; weight of 1
K_step 2[3:0]	step in adaptive curve from K = 2/8 to K = 3/8; weight of 2
K_step 3[3:0]	step in adaptive curve from K = 3/8 to K = 4/8; weight of 2
K_step 4[3:0]	step in adaptive curve from K = 4/8 to K = 5/8; weight of 4
K_step 5[3:0]	step in adaptive curve from K = 5/8 to K = 6/8; weight of 4
K_step 6[3:0]	step in adaptive curve from K = 6/8 to K = 7/8; weight of 8
K_step 7[3:0]	step in adaptive curve from K = 7/8 to K = 8/8; weight of 8
ad/fix	adaptive (ad/fix = 1) or fixed (ad/fix = 0) K; note 2
up/box	microprocessor (up/box = 1) or box controlled (up/box = 0) K; note 2
fixed_K[5:0]	determines K value in fixed K mode, see Table 2
Tfilter2_select[5:0]	determines filter 2 characteristic, see Table 5
Tfilter1_select[1:0]	determines filter 1 characteristic, see Table 3
hor_box_start[7:0]	horizontal start position of box with respect to picture
hor_box_stop[7:0]	horizontal stop position of box with respect to picture
vert_box_start[8:0]	vertical start position of box with respect to picture, note 1
vert_box_stop[8:0]	vertical stop position of box with respect to picture, note 1
dir_le	direct control of microprocessor (dir_le = 1) or synchronous with RSTR
sola	solarization on (sola = 1)
colour/pixrep	side panels as colour (colour/pixrep = 1) or pixel repetition
output_mux[2:0]	select throughput of various sources to output, see Table 2
bln_delay[1:0]	determines 1 to 4 clock pulse shift in internal as a function of external BLN
v_cnt_en	vertical counter increments per clock cycle if v_cnt_en = 1
border	border generation (border = 1) instead of box generation
inv_box	inversion of box signal (inv_box = 1)
en_box_ext	enable box signal to external box signal (pin 29, BOXE)
en_box_col	enable box signal to insert colour within box
en_box_rec	enable box signal to recirculate data second memory within box
en_box	overall enable box signal
zero	logical ground level for parts of circuit, should be 0
grey_value[7:0]	luminance level of colour for border/side panels
U_value[3:0]	(B-Y) level of colour for border/side panels; weight of 16; lower bits are forced to logic 0
V_value[3:0]	(R-Y) level of colour for border/side panels; weight of 16; lower bits are forced to logic 0

Notes

1. for vert_box_start and vert_box_stop bit 8 is encoded in the address
2. adaptive/fixed_K selection:

up/box	ad/fix	box *	K
0	0	0	fixed
0	0	1	adaptive
0	1	0	fixed
0	1	1	adaptive
1	0	0	fixed
1	0	1	fixed
1	1	0	adaptive
1	1	1	adaptive

* dynamic box signal, enabled with en_box, maybe inverted with inv_box

Table 2 Output multiplex control

output_mux[2:0]	OUTPUT
000	video
001	Tfilter2
010	K
011	grey
100	video
101	Tfilter2
110	K
111	sawtooth

Table 3 Filter 1 characteristic

Tfilter1_select[1:0]	TF1-TRANSFER(z)
00	1
01	$\frac{1}{2} \times z + 1 + \frac{1}{2} \times z^{-1}$
10	$\frac{1}{2}$
11	$\frac{1}{2} \times z + \frac{1}{2} + \frac{1}{2} \times z^{-1}$

Table 4 Fixed K setting

fixed_K[5:0] HEX	fixed_K[5:0] DEC	K
24	36	0
14	20	1/32
20	32	1/16
21	33	1/8
23	35	2/8
03	03	3/8
0F	15	4/8
09	09	5/8
0B	11	6/8
1A	26	7/8
3A	58	1

Table 5 Filter 2 characteristic

Tfilter2_select[5:0] HEX	DEC	TF2-TRANSFER(z)
00	00	$\frac{1}{2} \times z^2 + \frac{1}{2} \times z + 1 + \frac{1}{2} \times z^{-1} + \frac{1}{2} \times z^{-2}$
01	01	$1 \times z^2 + \frac{1}{2} \times z + 1 + \frac{1}{2} \times z^{-1} + 1 \times z^{-2}$
02	02	$0 \times z^2 + \frac{1}{2} \times z + 1 + \frac{1}{2} \times z^{-1} + 0 \times z^{-2}$
04	04	$\frac{1}{2} \times z^2 + 1 \times z + 1 + 1 \times z^{-1} + \frac{1}{2} \times z^{-2}$
05	05	$1 \times z^2 + 1 \times z + 1 + 1 \times z^{-1} + 1 \times z^{-2}$
06	06	$0 \times z^2 + 1 \times z + 1 + 1 \times z^{-1} + 0 \times z^{-2}$
08	08	$\frac{1}{2} \times z^2 + 0 \times z + 1 + 0 \times z^{-1} + \frac{1}{2} \times z^{-2}$
09	09	$1 \times z^2 + 0 \times z + 1 + 0 \times z^{-1} + 1 \times z^{-2}$
0A	10	$0 \times z^2 + 0 \times z + 1 + 0 \times z^{-1} + 0 \times z^{-2}$
10	16	$\frac{1}{2} \times z^2 + \frac{1}{2} \times z + 2 + \frac{1}{2} \times z^{-1} + \frac{1}{2} \times z^{-2}$
11	17	$1 \times z^2 + \frac{1}{2} \times z + 2 + \frac{1}{2} \times z^{-1} + 1 \times z^{-2}$
12	18	$0 \times z^2 + \frac{1}{2} \times z + 2 + \frac{1}{2} \times z^{-1} + 0 \times z^{-2}$
14	20	$\frac{1}{2} \times z^2 + 1 \times z + 2 + 1 \times z^{-1} + \frac{1}{2} \times z^{-2}$
15	21	$1 \times z^2 + 1 \times z + 2 + 1 \times z^{-1} + 1 \times z^{-2}$
16	22	$0 \times z^2 + 1 \times z + 2 + 1 \times z^{-1} + 0 \times z^{-2}$
18	24	$\frac{1}{2} \times z^2 + 0 \times z + 2 + 0 \times z^{-1} + \frac{1}{2} \times z^{-2}$
19	25	$1 \times z^2 + 0 \times z + 2 + 0 \times z^{-1} + 1 \times z^{-2}$
1A	26	$0 \times z^2 + 0 \times z + 2 + 0 \times z^{-1} + 0 \times z^{-2}$
20	32	$\frac{1}{2} \times z^2 + \frac{1}{2} \times z + 0 + \frac{1}{2} \times z^{-1} + \frac{1}{2} \times z^{-2}$
21	33	$1 \times z^2 + \frac{1}{2} \times z + 0 + \frac{1}{2} \times z^{-1} + 1 \times z^{-2}$
22	34	$0 \times z^2 + \frac{1}{2} \times z + 0 + \frac{1}{2} \times z^{-1} + 0 \times z^{-2}$
24	36	$\frac{1}{2} \times z^2 + 1 \times z + 0 + 1 \times z^{-1} + \frac{1}{2} \times z^{-2}$
25	37	$1 \times z^2 + 1 \times z + 0 + 1 \times z^{-1} + 1 \times z^{-2}$
26	38	$0 \times z^2 + 1 \times z + 0 + 1 \times z^{-1} + 0 \times z^{-2}$
28	40	$\frac{1}{2} \times z^2 + 0 \times z + 0 + 0 \times z^{-1} + \frac{1}{2} \times z^{-2}$
29	41	$1 \times z^2 + 0 \times z + 0 + 0 \times z^{-1} + 1 \times z^{-2}$
2A	42	$0 \times z^2 + 0 \times z + 0 + 0 \times z^{-1} + 0 \times z^{-2}$

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range	−0.5	6.5	V
V_I	input voltage range	−0.5	V_{DD} + 0.5	V
I_O	output current	–	20	mA
T_{amb}	operating ambient temperature range	0	+70	°C
T_{stg}	storage temperature range	−40	+125	°C

CHARACTERISTICS

Recommended operating conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{IH}	HIGH level input voltage	2.2	V_{DD}	V
V_{IL}	LOW level input voltage	0	0.8	V
t_r	input rise time	0	200	ns
t_f	input fall time	0	200	ns

DC Characteristics

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
I_I	input current		–	10^{-5}	10	µA
I_{OL}	LOW level output current;	Lp*	6.0	13.0	–	mA
		Hp*	12.0	26.0	–	mA
I_{OH}	HIGH level output current;	Lp*	−7.0	−7.0	–	mA
		Hp*	−14.0	−14.0	–	mA

Lp* = LOW power output buffer
Hp* = HIGH power output buffer

AC Characteristics (C_L = 15 pF)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
t_r	output rise time	3	–	µs
t_f	output fall time	2	–	µs
I/O capacitance				
C_I	input terminal	10	25	pF
C_O	output terminal	10	25	pF

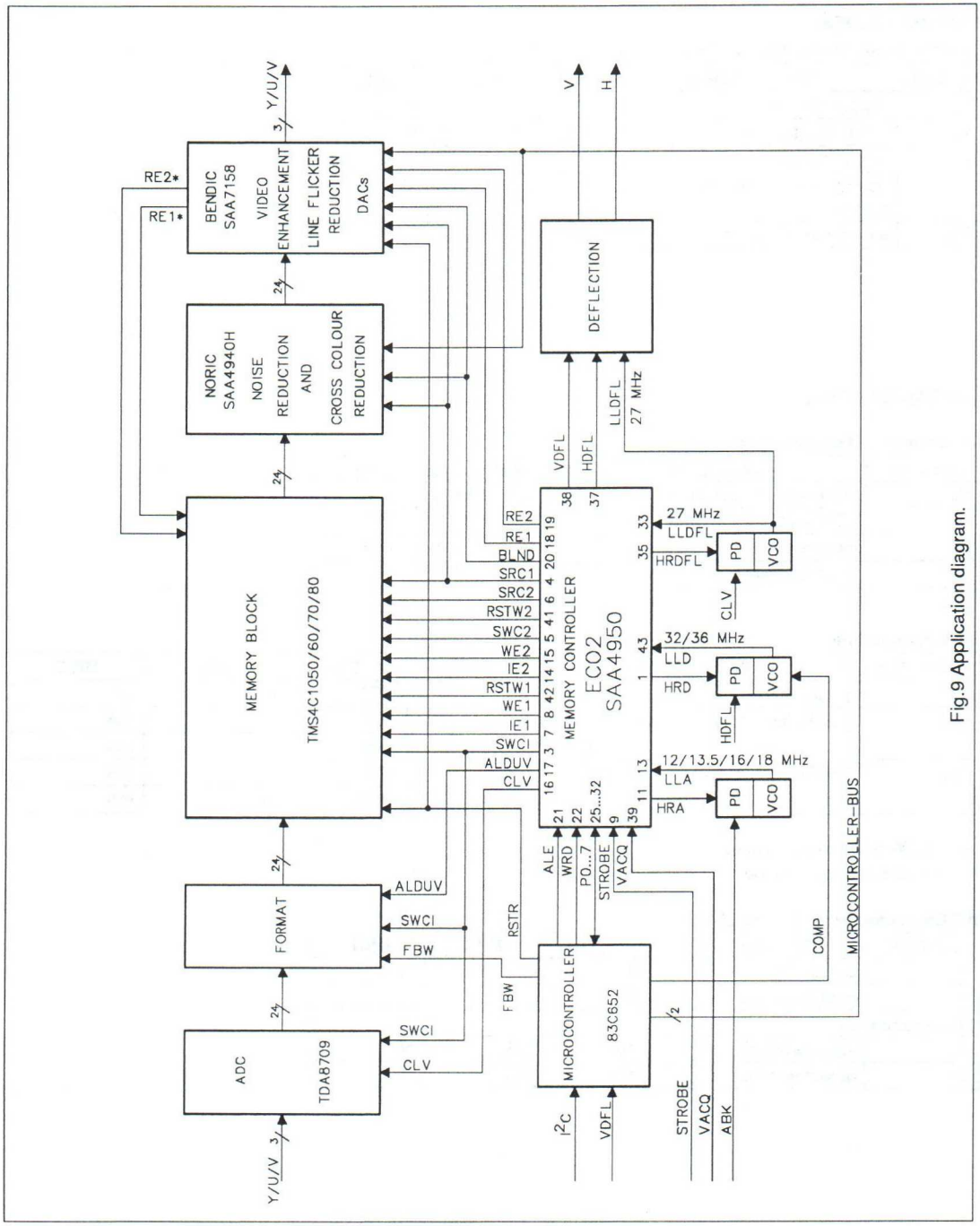


Fig.9 Application diagram.

Monolithic integrated 16:9 compressor SAA4981

FEATURES

- Fixed horizontal compression by a factor of 4/3 for most video standards
- Three fixed screen positions (left, centre and right)
- 5 MHz bandwidth
- Bypass function
- Inputs for luminance and chrominance of side panels
- Standard video inputs and outputs (Y, (B–Y) and (R–Y))
- Horizontal and vertical sync signals are not processed
- Pre filters and post filters on chip.

GENERAL DESCRIPTION

The 16:9 compressor is an IC which compresses the active part of a video line by a factor of 4/3 from e.g. 52 µs to 39 µs. This is necessary to display 4:3 video software on a 16:9 tube in correct proportion. The capacitively coupled video inputs of the IC are: Y, (B–Y) and (R–Y). The synchronisation input of the IC is a line frequent reference signal HREF. The bandwidth of the IC comes up to 5 MHz and the signal delay in the IC is realized with SC-Line Memories (Switched Capacitors Line Memories). The output of the 16:9 compressor also has the format Y, (B–Y) and (R–Y) and provides the following two possibilities:

1. Bypass function (the input signal is not compressed)
2. Compressed video by factor 4/3 with three different fixed screen positions (left, centre and right). The luminance and chrominance of the side panels are determined by the external signals Y_SIDE, BY_SIDE and RY_SIDE.

The horizontal compression is a time discrete and amplitude continuous signal processing. This provides pre and post filters which are realized on chip. The internal clock generation is achieved with a 54 MHz H-PLL which is synchronized to the positive edge of the HREF signal. The function of the IC is controlled by the three control signals CTRL1, CTRL2 and CTRL3.

QUICK REFERENCE DATA

Voltages for video signals are peak-to-peak values for 75% colour bars. All voltages are referenced to $V_{EEA} = V_{EED} = 0$ V.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.75	5	5.5	V
V_{CCD}	digital supply voltage	4.75	5	5.5	V
V_{23-19}	input voltage Y (peak-to-peak value)	–	0.32	0.45	V
V_{22-19}	input voltage (B–Y) (peak-to-peak value)	–	1.33	1.9	V
V_{21-19}	input voltage (R–Y) (peak-to-peak value)	–	1.05	1.5	V
V_{6-19}	HREF top pulse	3.0	–	6.5	V
V_{18-19}	output voltage Y_OUT (peak-to-peak value)	–	0.32	0.5	V
V_{17-19}	output voltage (B–Y)_OUT	–	1.33	2.1	V
V_{16-19}	output voltage (R–Y)_OUT	–	1.05	1.7	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA4981	24	DIL	plastic	SOT101

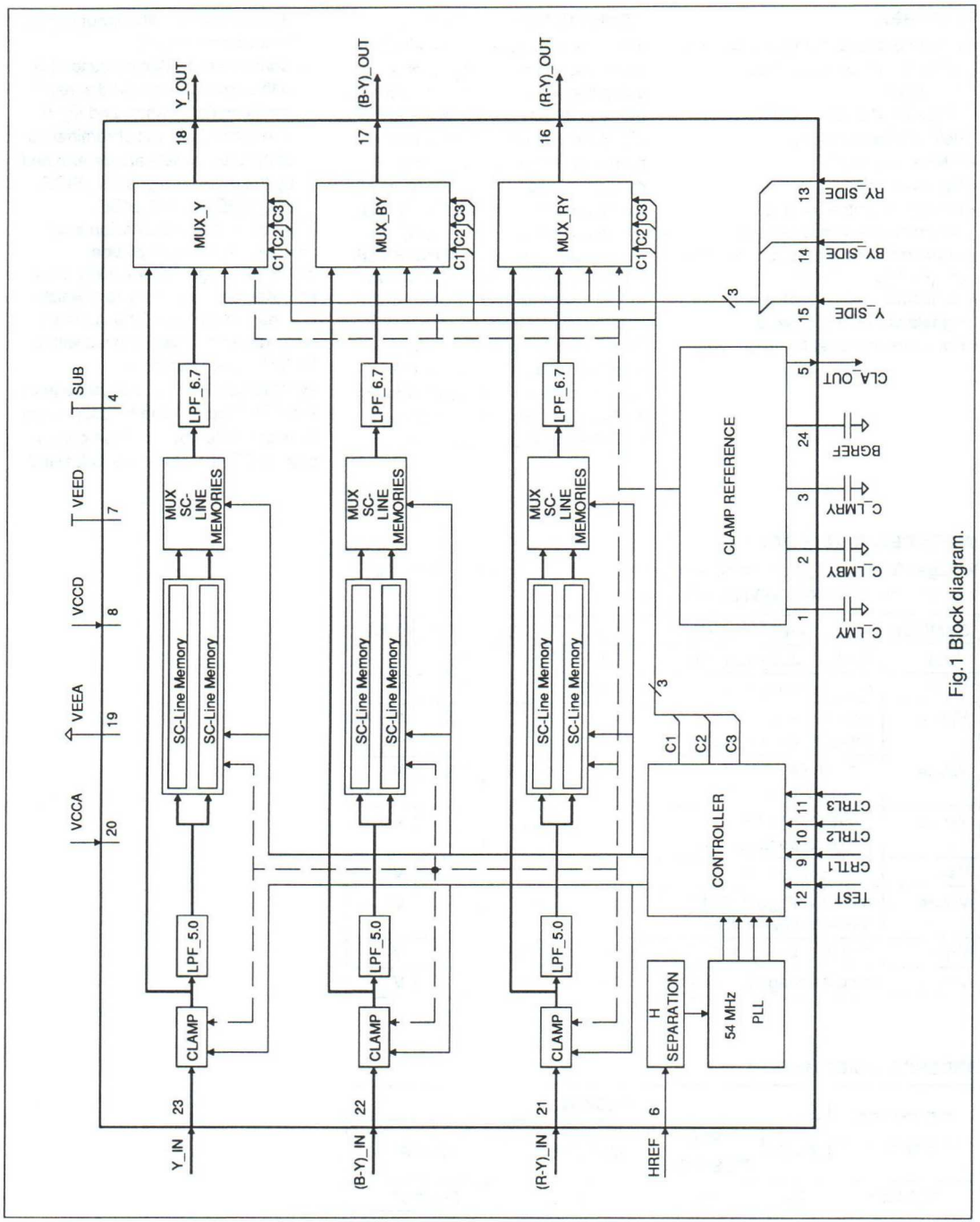


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
C_LMY	1	decoupling capacitor for Y reference voltage
C_LMBY	2	decoupling capacitor for BY reference voltage
C_LMRY	3	decoupling capacitor for RY reference voltage
SUB	4	substrate connection (see application information)
CLA_OUT	5	internal clamping reference voltage output
HREF	6	horizontal reference input
V_{EED}	7	ground for digital section
V_{CCD}	8	positive digital supply voltage
CTRL1	9	control input 1
CTRL2	10	control input 2
CTRL3	11	control input 3
TEST	12	test mode activation
RY_SIDE	13	side panel input for RY
BY_SIDE	14	side panel input for BY
Y_SIDE	15	side panel input for Y
(R–Y)_OUT	16	output signal for (B–Y)
(B–Y)_OUT	17	output signal for (R–Y)
Y_OUT	18	output signal for Y
V_{EEA}	19	ground for analog section
V_{CCA}	20	positive analog supply voltage
(R–Y)_IN	21	input signal for (R–Y)
(B–Y)_IN	22	input signal for (B–Y)
Y_IN	23	input signal for Y
BGREF	24	decoupling capacitor for internal reference voltage

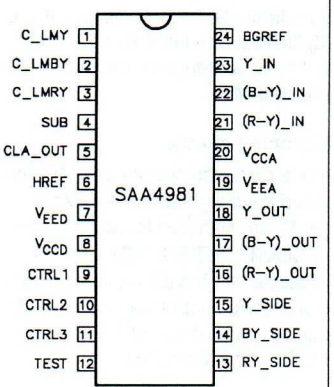


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_x	voltage on any pins (except pin 6 (HREF))	$V_{EEA} - 0.5$ $V_{EED} - 0.5$	$V_{CCA} + 0.5$ $V_{CCD} + 0.5$	V V
V_6	voltage at pin 6 (HREF)	−0.5	+6.5	V
T_{stg}	storage temperature	−25	+150	°C
T_{amb}	operating ambient temperature	−20	+70	°C
P_{tot}	total power dissipation	–	0.5	W
V_{ESD}	electrostatic handling for all pins (note 1) (note 2)	 – –	 ±500 ±4000	 V V

Notes to the Limiting Values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

Quality specification

UZW-B0/FQ-0601
ESD classification A

FUNCTIONAL DESCRIPTION

Applicable video standards

The 16:9 compressor is applicable for the following listed video standards: B, C, D, G, H, I, K, K1, L, M, N. The standards D, I, K, K1, L will show a reduced video bandwidth above 5 MHz.

Clamping circuit

In the clamping circuits CLAMP the video input signals Y, (B–Y) and (R–Y) are clamped to the DC level of CLAMP REFERENCE. This is necessary to have the input signals in the correct input voltage range for the low-pass filters (LPF 5.0) and the SC-Line Memories.

Internal pre filters

Before the signals are sampled to the time discrete and amplitude continuous area a low-pass filtering is necessary to avoid aliasing. Even if the inputs of the IC are already low-pass filtered a filtering is advantageous for EMC (electromagnetic compatibility).
For all three low-pass filters the same transfer function is used because of the same bandwidth for luminance and chrominance signals (up to 5 MHz bandwidth).

SC-Line Memories

Behind the low-pass filters the input signals are fed to the SC-Line Memories. The signals are sampled with a clock frequency of 13.5 MHz. One video line later the signals are read with a clock frequency of 18 MHz in compression mode. The result of the different clock frequencies is a horizontal compression by a factor of 4/3. The clocks and the horizontal starting pulses for the SC-Line Memories come from the controller.
For each signal path two line memories are necessary because e.g. in compression mode in one video line the signals are sampled to the SC-Line Memories with 13.5 MHz and one video line later the signals are read with 18 MHz. In the bypass mode through the SC-Line Memories in one video line the signals are sampled with 13.5 MHz and one video line later the signals are read with 13.5 MHz. The SC-Line Memories are suitable for signals up to 5 MHz bandwidth. With a multiplexer (MUX) behind the SC-Line Memories the sampled video signal is connected to the internal post filters.

Output multiplexer MUX Y, MUX (B–Y) and MUX (R–Y)

The output MUXs are controlled via C1 and C2 by the controller. With the MUXs one of the four input signals of the MUXs is connected to the output of the IC. The MUXs allow fast switching.
The input signals of the MUXs for one component (Y, (B–Y) or (R–Y)) are:

- The ouput signal of the post filter
- The uncompressed signal behind the input clamping
- The clamping reference coming from the block CLAMP REFERENCE
- The signal for the side panel determined by Y_SIDE, BY_SIDE and RY_SIDE

The H-Separation circuit

The 54 MHz H-PLL is locked to the positive edge of the digital HREF signal, which is generated in the H-separation circuit from the input signal HREF. It is also possible to use the positive edge of the burst key of a sandcastle signal.

54 MHz H-PLL

The 13.5 MHz clock frequency for the sampling clock and the 18 MHz clock frequency for the reading clock are generated in the 54 MHz H-PLL. The 13.5 MHz clock and the 18 MHz clock are line locked.

The block CLAMP REFERENCE

In the block CLAMP REFERENCE reference voltages are generated. These DC signals are used in the clamping circuits, as input signals for the output MUXs and as references for the SC-Line Memories.
Four external capacitors at the pins C_LMY, C_LMBY, C_LMRY and BGREF are necessary to smooth the references. A black level reference signal is available at CLA_OUT.

Controller

The controller generates the clocks and the horizontal start signals for the SC-Line Memories and also the control signals for the output MUXs. For three different screen positions (left, centre and right) the timing for the start reading signal and the control signals for the MUXs (C1 and C2) are fixed. For the uncompressed signals a bypass through the SC-Line Memories and a bypass not through the SC-Line Memories are available. When the signals do not pass the line memories, the frequency response is not affected by the si-function. The compression and bypass mode through the line memories are delayed by one line with respect to the bypass mode not through the line memory.
The 16:9 compressor is controlled via the control signals CTRL1, CTRL2 and CTRL3. The test input has to be on low level.

The control signals perform the following functions:

CTRL1	CTRL2	CTRL3	FUNCTION
L	L	L	bypass (through the line memories)
L	H	L	compression, left position
H	L	L	compression, centre position
H	H	L	compression, right position
L	L	H	bypass (not through the line memories)

H = HIGH signal
L = LOW signal

Internal post filters

The output signals of the SC-Line Memories have to be filtered with three low-pass filters (LPF 6.7) to eliminate high frequencies caused by the time discrete signal processing. The cut-off frequency of 6.7 MHz is necessary because as a result of the compression by the factor 3:4 the frequencies are shifted to a higher frequency band with the invers compression factor (e.g. 5 MHz → compression → 6.67 MHz). Due to the common bandwidth requirements for all three outputs of the SC-Line Memories the same transfer function for the filters can be used.
Remark: These filters do not provide an si-correction. This means that an input signal with a frequency of 5 MHz will be damped by 2.1 dB at the output if the signal passes an SC-Line Memory.

Signals for the side panels

The luminance and chrominance of the side panels is determined by the external signals Y_SIDE, BY_SIDE and RY_SIDE. This external generated side panel signal can be referred to the internal black level reference signal via the output CLA_OUT (pin 5).

CHARACTERISTICS

T_{amb} = +25 °C; $V_{CCA} = V_{CCD}$ = 5 V; f_{HREF} = 15.625 kHz; substrate connected to V_{EED}; Y_SIDE, BY_SIDE and RY_SIDE are connected to CLA_OUT; all voltages are referenced to V_{EEA} = 0 V; input signal: EBU colour bar 100/0/75/0 (CCIR recommended 471-1), Y = 0.32 V (p-p), (B–Y) = 1.33 V (p-p), (R–Y) = 1.05 V (p-p); source impedance Z_{is} = 300 Ω; coupling capacitor C_k = 2.2 nF; outputs: loads to ground R_L = 1 MΩ, C_L = 20 pF; measured in Fig.5; test input pin 12 has to be connected to V_{EED}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins 20, 19, 8, 7 and 4) note 1						
V_{CCA}	analog supply voltage		4.75	5	5.5	V
I_{CCA}	analog supply current		35	50	65	mA
V_{CCD}	digital supply voltage		4.75	5	5.5	V
I_{CCD}	digital supply current		1	9	14	mA
Video inputs (pins 23, 22 and 21)						
Y						
V_{23-19}	input voltage (peak-to-peak value)	active video	–	0.32	0.45	V
C_{YI}	input capacitance		–	–	10	pF
I_{Yleak}	input leakage current between clamping		–	–	0.1	µA
R_{Ycla}	input resistance during clamping		–	2	5	kΩ
(B–Y)						
V_{22-19}	input voltage (peak-to-peak value)	active video	–	1.33	1.9	V
C_{UI}	input capacitance		–	–	10	pF
I_{Uleak}	input leakage current between clamping		–	–	0.1	µA
R_{Ucla}	input resistance during clamping		–	2	5	kΩ
(R–Y)						
V_{21-19}	input voltage (peak-to-peak value)	active video	–	1.05	1.5	V
C_{VI}	input capacitance		–	–	10	pF
I_{Vleak}	input leakage current between clamping		–	–	0.1	µA
R_{Vcla}	input resistance during clamping		–	2	5	kΩ
HREF input (pin 6)						
V_{6-19}	voltage of the top pulse		3.0	–	6.5	V
$I_{HREFleak}$	input leakage current		–	–	10	µA
C_{HREF}	input capacitance		–	–	10	pF
V_{slic}	slicing level below top pulse		0.5	0.75	1.0	V
f_{HREF}	input frequency		14.0	15.6	17.2	kHz
t_{HREF}	pulse width		1	–	–	µs
S_{HREF}	steepness	0.5 V under top	400	–	–	mV/ns
Side panel inputs (pins 15, 14 and 13)						
$V_{13,14,15-19}$	input voltage		0.5	–	2.5	V
C_{Sidel}	input capacitance		–	–	10	pF
$I_{Side\ leak}$	input leakage current		–	–	0.1	µA
Control inputs/outputs (pins 9, 10 and 11)						
$V_{9,10,11-7}$	HIGH level input voltage		3.5	–	–	V
	LOW level input voltage		–	–	1.5	V
C_{Ctrll}	input capacitance		–	–	10	pF
$I_{Ctrl\ leak}$	input leakage current		–	–	1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clamping reference output (pin 5)						
V_{5-19}	output voltage		1.3	1.45	1.6	V
R_L	load resistor		10	–	–	kΩ
C_L	load capacitor		–	–	30	pF
External capacitors (pins 1, 2 and 3)						
C_{DL}	value for capacitor		–	100	–	nF
V_{CDL}	output voltage		1.3	1.45	1.6	V
External capacitor (pin 24)						
C_{BGREF}	value for capacitor		–	100	–	nF
V_{BGREF}	output voltage		1.1	1.25	1.4	V
Video output signals (pins 18, 17 and 16)						
Y_OUT						
R_Y	output resistance		–	–	100	Ω
V_{18-19}	output voltage (peak-to-peak value)		–	0.32	0.5	V
S/N	signal-to-noise ratio	0.32 V (p-p) / V_{eff} noise; unweighted; f = 200 kHz to 5 MHz	52	–	–	dB
S/N(FPN)	fixed pattern noise peak-to-peak referenced to 0.32 V (p-p) video	f_{clock} < 5 MHz	42	–	–	dB
α_Y	crosstalk between different inputs	f = 1 MHz	40	–	–	dB
Δt_d	delay between different outputs		–	–	30	ns
t_d	jitter in output signal to input HREF signal		–	–	10	ns
Bypass not through the SC-Line Memories						
G_{Y1}	frequency response	ripple between 0 and 4 MHz	–0.5	–	+0.5	dB
G_{Y2}	frequency response	attenuation at 5 MHz compared to 1 MHz	0	–	–2	dB
Bypass through the SC-Line Memories (note 2)						
G_{Y3}	Y_OUT/Y_IN at input frequency	f = 1 MHz	–1.1	–	+0.9	dB
G_{Y4}		f = 2 MHz	–1.3	–	+0.7	dB
G_{Y5}		f = 3 MHz	–1.7	–	+0.3	dB
G_{Y6}		f = 4 MHz	–2.3	–	–0.3	dB
G_{Y7}		f = 5 MHz	–3.1	–	–1.1	dB
Compressed video (note 2)						
G_{Y8}	Y_OUT/Y_IN at input frequency	f_{in} = 1 MHz; f_{out} = 1.3 MHz	–1	–	+1	dB
G_{Y9}		f_{in} = 2 MHz; f_{out} = 2.7 MHz	–1	–	+1	dB
G_{Y10}		f_{in} = 3 MHz; f_{out} = 4 MHz	–2	–	0	dB
G_{Y11}		f_{in} = 3.75 MHz; f_{out} = 5 MHz	–3	–	–1	dB
G_{Y12}		f_{in} = 4 MHz; f_{out} = 5.3 MHz	–4	–	–1	dB
G_{Y13}		f_{in} = 5 MHz; f_{out} = 6.67 MHz	–6	–	–1	dB
A_{YPre}	pre filter stop-band characteristic, damping factor for input signals	f > 10 MHz	20	–	–	dB
		f > 20 MHz	32	–	–	dB
		f > 100 MHz	42	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
A_{YPost}	post filter stop-band characteristic, damping factor for input signals	f > 14 MHz	20	–	–	dB
		f > 20 MHz	32	–	–	dB
		f > 100 MHz	40	–	–	dB
(B–Y)_OUT						
R_U	output resistance		–	–	100	Ω
V_{17-19}	output voltage (peak-to-peak value)		–	1.33	2.1	V
S/N	signal-to-noise ratio	1.33 V (p-p) / V_{eff} noise; unweighted; f = 200 kHz to 5 MHz	54	–	–	dB
S/N(FPN)	fixed pattern noise peak-to-peak referenced to 1.33 V (p-p) video	f_{clock} < 5 MHz	42	–	–	dB
α_U	crosstalk between different inputs	f = 1 MHz	40	–	–	dB
Δt_d	delay between different outputs		–	–	30	ns
t_d	jitter in output signal to input HREF signal		–	–	10	ns
Bypass not through the SC-Line Memories						
G_{U1}	frequency response	ripple between 0 and 4 MHz	–0.5	–	+0.5	dB
G_{U2}	frequency response	attenuation at 5 MHz compared to 1 MHz	0	–	–2	dB
Bypass through the SC-Line Memories (note 2)						
G_{U3}	(B–Y)_OUT/(B–Y)_IN at input frequency	f = 1 MHz	–1.1	–	+0.9	dB
G_{U4}		f = 2 MHz	–1.3	–	+0.7	dB
G_{U5}		f = 3 MHz	–1.7	–	+0.3	dB
G_{U6}		f = 4 MHz	–2.3	–	–0.3	dB
G_{U7}		f = 5 MHz	–3.1	–	–1.1	dB
Compressed video (note 2)						
G_{U8}	(B–Y)_OUT/(B–Y)_IN at input frequency	f_{in} = 1 MHz; f_{out} = 1.3 MHz	–1	–	+1	dB
G_{U9}		f_{in} = 2 MHz; f_{out} = 2.7 MHz	–1	–	+1	dB
G_{U10}		f_{in} = 3 MHz; f_{out} = 4 MHz	–2	–	0	dB
G_{U11}		f_{in} = 3.75 MHz; f_{out} = 5 MHz	–3	–	–1	dB
G_{U12}		f_{in} = 4 MHz; f_{out} = 5.3 MHz	–4	–	–1	dB
G_{U13}		f_{in} = 5 MHz; f_{out} = 6.67 MHz	–6	–	–1	dB
A_{UPre}	pre filter stop-band characteristic, damping factor for input signals	f > 10 MHz	20	–	–	dB
		f > 20 MHz	32	–	–	dB
		f > 100 MHz	42	–	–	dB
A_{UPost}	post filter stop-band characteristic, damping factor for input signals	f > 14 MHz	20	–	–	dB
		f > 20 MHz	32	–	–	dB
		f > 100 MHz	40	–	–	dB
(R–Y)_OUT						
R_V	output resistance		–	–	100	Ω
V_{16-19}	output voltage (peak-to-peak value)		–	1.05	1.7	V
S/N	signal-to-noise ratio	1.05 V (p-p) / V_{eff} noise; unweighted; f = 200 kHz to 5 MHz	52	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N(FPN)	fixed pattern noise peak-to-peak referenced to 1.05 V (p-p) video	f_{clock} < 5 MHz	40	–	–	dB
α_V	crosstalk between different inputs	f = 1 MHz	40	–	–	dB
Δt_d	delay between different outputs		–	–	30	ns
t_d	jitter in output signal to input HREF signal		–	–	10	ns
Bypass not through the SC-Line Memories						
G_{V1}	frequency response	ripple between 0 and 4 MHz	–0.5	–	+0.5	dB
G_{V2}	frequency response	attenuation at 5 MHz compared to 1 MHz	0	–	–2	dB
Bypass through the SC-Line Memories (note 2)						
G_{V3}	(R–Y)_OUT/(R–Y)_IN at input frequency	f = 1 MHz	–1.1	–	+0.9	dB
G_{V4}		f = 2 MHz	–1.3	–	+0.7	dB
G_{V5}		f = 3 MHz	–1.7	–	+0.3	dB
G_{V6}		f = 4 MHz	–2.3	–	–0.3	dB
G_{V7}		f = 5 MHz	–3.1	–	–1.1	dB
Compressed video (note 2)						
G_{V8}	(R–Y)_OUT/(R–Y)_IN at input frequency	f_{in} = 1 MHz; f_{out} = 1.3 MHz	–1	–	+1	dB
G_{V9}		f_{in} = 2 MHz; f_{out} = 2.7 MHz	–1	–	+1	dB
G_{V10}		f_{in} = 3 MHz; f_{out} = 4 MHz	–2	–	0	dB
G_{V11}		f_{in} = 3.75 MHz; f_{out} = 5 MHz	–3	–	–1	dB
G_{V12}		f_{in} = 4 MHz; f_{out} = 5.3 MHz	–4	–	–1	dB
G_{V13}		f_{in} = 5 MHz; f_{out} = 6.67 MHz	–6	–	–1	dB
A_{VPre}	pre filter stop-band characteristic, damping factor for input signals	f > 10 MHz	20	–	–	dB
		f > 20 MHz	32	–	–	dB
		f > 100 MHz	42	–	–	dB
A_{VPost}	post filter stop-band characteristic, damping factor for input signals	f > 14 MHz	20	–	–	dB
		f > 20 MHz	32	–	–	dB
		f > 100 MHz	40	–	–	dB
Video outputs Y_OUT, (B–Y)_OUT, (R–Y)_OUT						
Ratio of output amplitudes for equal input signals for Y, (B–Y) and (R–Y)						
V_{18-19}/V_{17-19}	Y_OUT/(B–Y)_OUT	V_I = 0.32 V (p-p); signals ≤ 1 MHz	–0.4	–	+0.4	dB
V_{18-19}/V_{16-19}	Y_OUT/(R–Y)_OUT		–0.4	–	+0.4	dB
V_{17-19}/V_{16-19}	(B–Y)_OUT/(R–Y)_OUT	V_I = 1.33 V (p-p)	–0.4	–	+0.4	dB

Notes to the characteristics

1. $\Delta V_1 = |V_{CCA} - V_{CCD}| \leq 300$ mV; $\Delta V_2 = |V_{EED} - V_{EEA}| \leq 300$ mV with V_{EED} = SUB (latch up prevention).
2. This frequency response includes the si-attenuation as a result of the time discrete signal processing. An si-correction is not done.

APPLICATION INFORMATION

See application diagram (Fig.5).

Substrate (pin 4) has to be connected to V_{EED}.

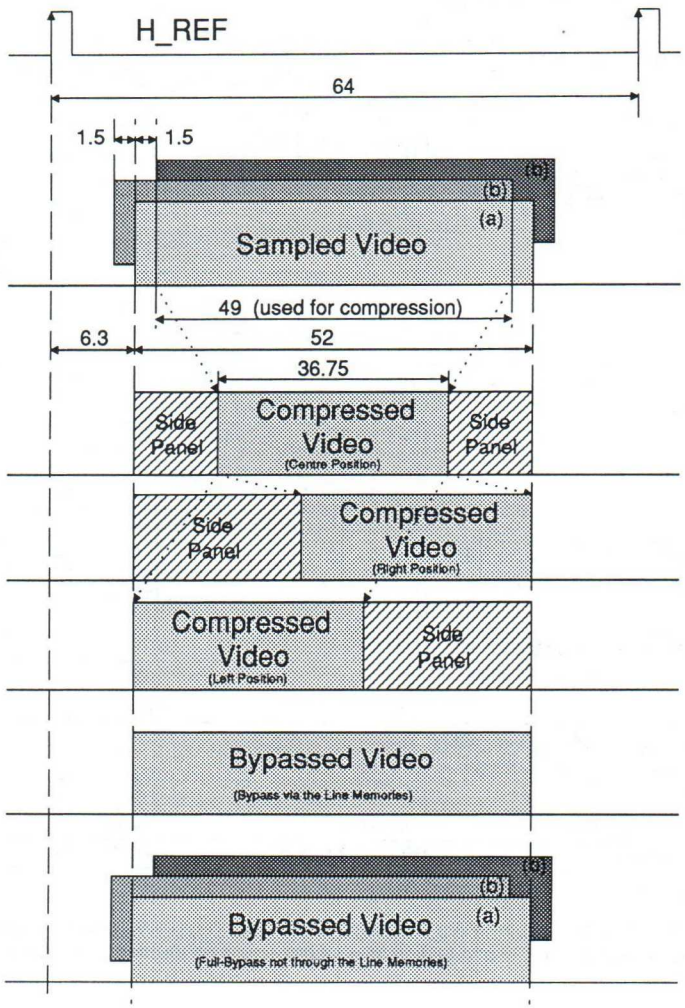
V_{EEA} and V_{EED} / SUB have to be separated as much as possible.

Horizontal timing (see Fig.3)

The horizontal timing refers to the positive edge of the input HREF signal.

The following timing parameters (see Fig.3) are valid for a horizontal frequency of 15.625 kHz.

Input clamping typically starts at t_A = 1.55 µs and ends at t_B = 3.78 µs.



Rem.: (a) Nominal timing for a 52us active video signal to generate a centred compressed video signal
(b) Worst-case picture position for a 52us active video signal to generate no visible blanking between side panels and compressed video
(c) All times in us.

Fig.3 Horizontal timing.

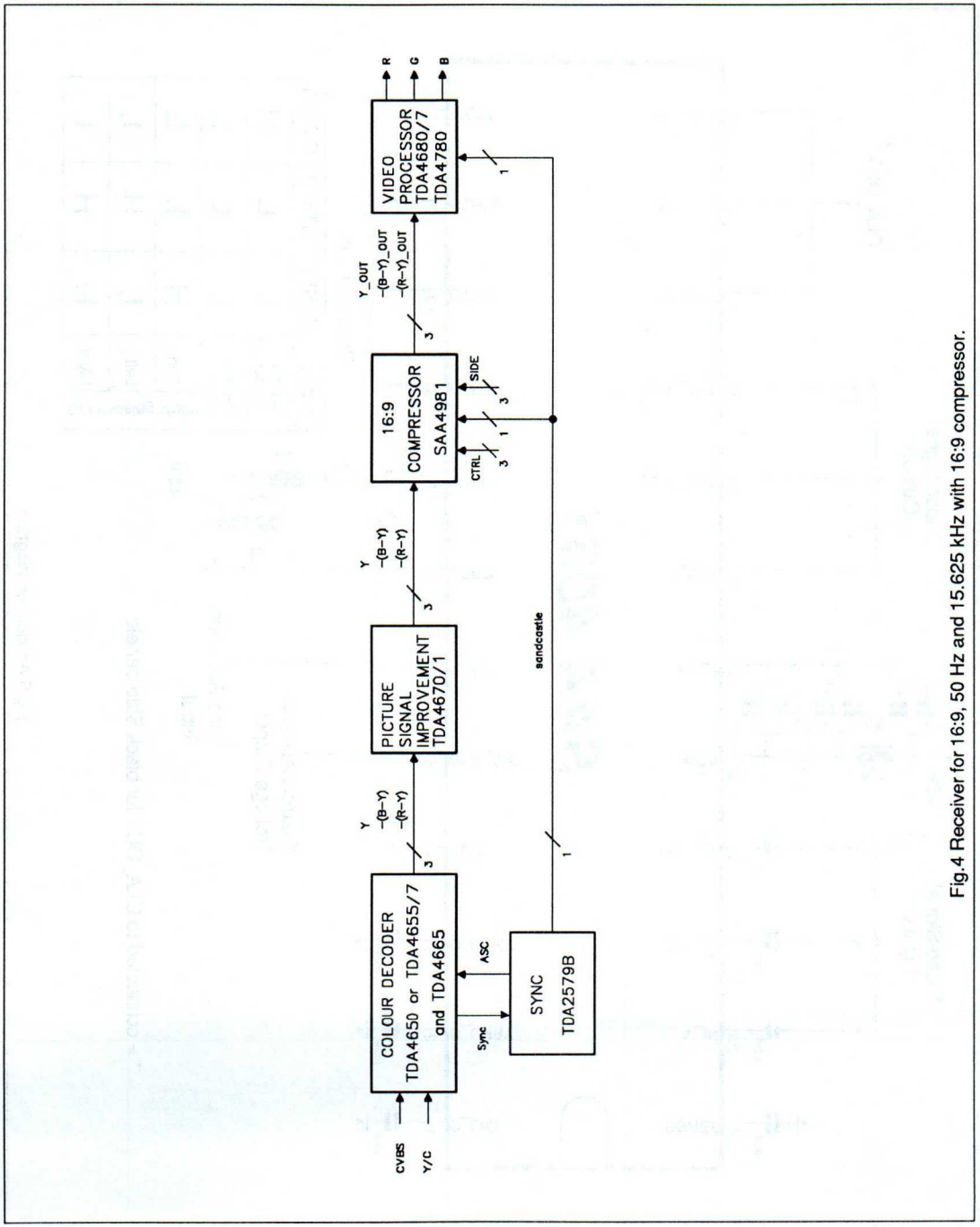
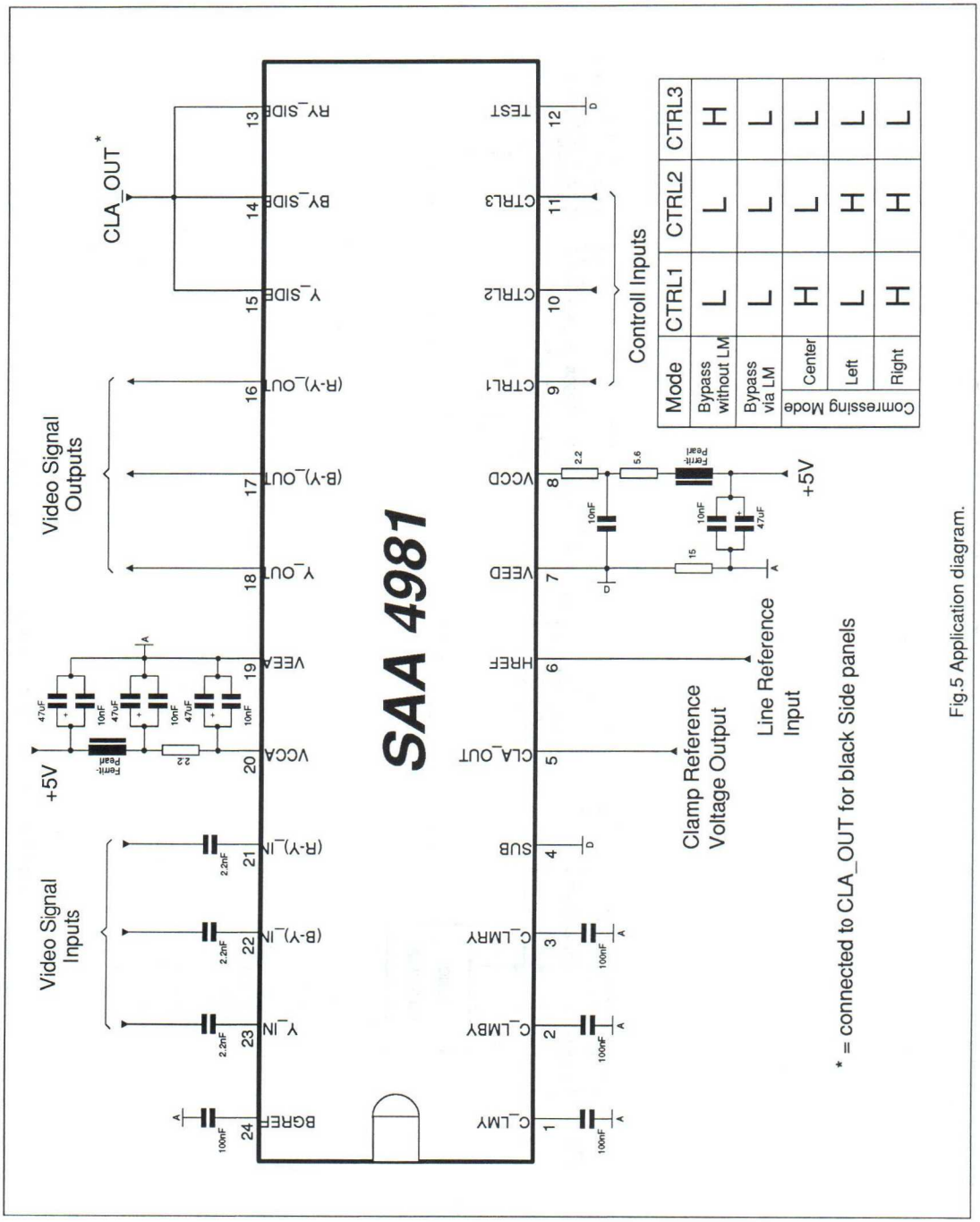


Fig.4 Receiver for 16:9, 50 Hz and 15.625 kHz with 16:9 compressor.



Compressing Mode	Mode	CTRL1	CTRL2	CTRL3
	Bypass without LM	L	L	H
	Bypass via LM	L	L	L
	Center	H	L	L
	Left	L	H	L
	Right	H	H	L

Fig.5 Application diagram.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1991

SAA5191
Teletext video processor

FEATURES

- Adaptive data slicer
- Crystal-controlled data clock regeneration with a bit rate of 6.9375 MHz
- Adaptive sync separator, horizontal phase detector and 13.5 MHz VCO to provide display phase locked loop (PLL)
- TV synchronization at teletext mode

GENERAL DESCRIPTION

The SAA5191 is a bipolar integrated circuit that extracts teletext data from the video signal (CVBS), regenerates the teletext clock (TTC) and synchronizes the text display to the television signals (VCS). This device operates in conjunction with the Digital Video Teletext (back-end) Decoder (DVTB – SAA9042A) or any other compatible device.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 16)	-	12	-	V
I_P	supply current	-	70	-	mA
$V_{i\ CVBS}$	CVBS input signal on pin 27 (peak-to-peak value)				
	at pin 2 LOW	-	1	-	V
	at pin 2 open-circuit	-	2.5	-	V
V_o	output signals TTC and TTD (peak-to-peak value, pins 14, 15)	2.5	3.5	4.5	V
V_{F13}	13.5 MHz clock output signal (peak-to-peak value, pin 17)	1	2	3	V
V_{SYNC}	video sync output signal (peak-to-peak value, pin 1)	-	-	1	V
	SYNC output signal $\overline{TCS}$	200	450	650	mV
VCS	video composite sync level on output pin 25				
	LOW	-	-	0.4	V
	HIGH	2.4	-	5.5	V
T_{amb}	operating ambient temperature	0	-	+70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5191	28	DIL	plastic	SOT117

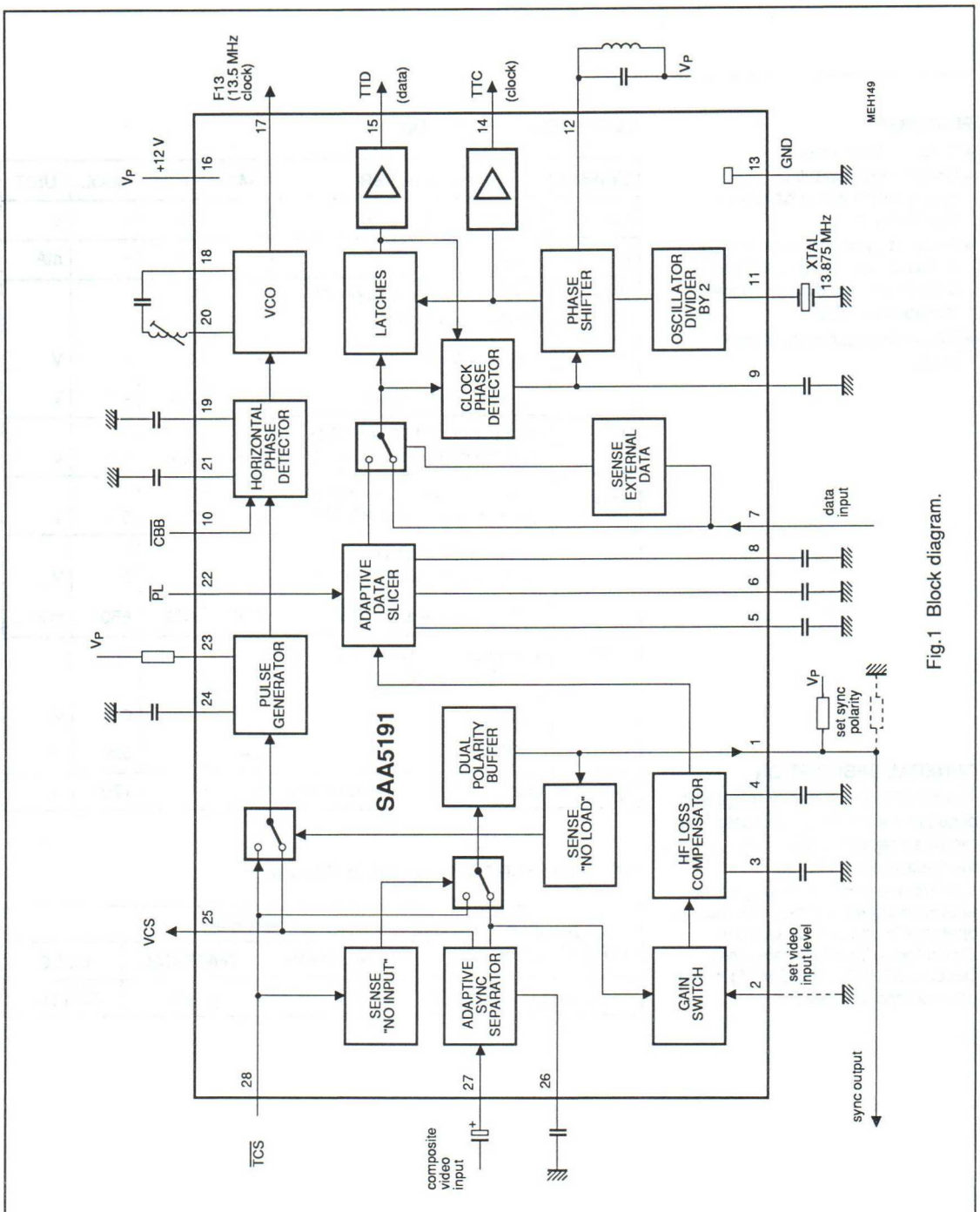


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
STTV	1	sync output signal to TV (positive or negative going)
VILS	2	level select input of video input (LOW equals 1 V)
C_{filt}	3	video filtering capacitor of HF loss compensation
C_{store}	4	HF storage capacitor
C_{ampl}	5	amplitude capacitor
C_{zero}	6	zero level capacitor
EXD	7	external data current input (1)
C_{time}	8	data timing capacitor for the adaptive data slicer
C_{CLK}	9	clock phase detector capacitor
$\overline{CBB}$	10	blanking insertion input
XTAL	11	13.875 MHz crystal (double of data rate)
CLF	12	6.9375 MHz clock frequency filter
GND	13	ground (0 V)
TTC	14	teletext clock output (for computer controlled teletext)
TTD	15	teletext data output (for computer controlled teletext)
V_P	16	+12 V supply voltage
F13	17	13.5 MHz VCO output (for sandcastle generation)
OSCO	18	oscillator output to series LC-circuit or crystal
C_{VCR}	19	short time constant capacitor at video recorder mode (2)
OSCI	20	oscillator input from series LC-circuit or crystal
C_{hor}	21	horizontal phase capacitor / VCR mode
$\overline{PL}$	22	sandcastle input (generated in CCT)
R_T	23	timing resistor for pulse generator
C_T	24	timing capacitor for pulse generator
VCS	25	video composite sync output to CCT
C_{BL}	26	black level capacitor
CVBS	27	composite video input signal from TV
$\overline{TCS}$	28	text-composite/scan-composite sync input ($\overline{TSC}/\overline{SCS}$)

PIN CONFIGURATION

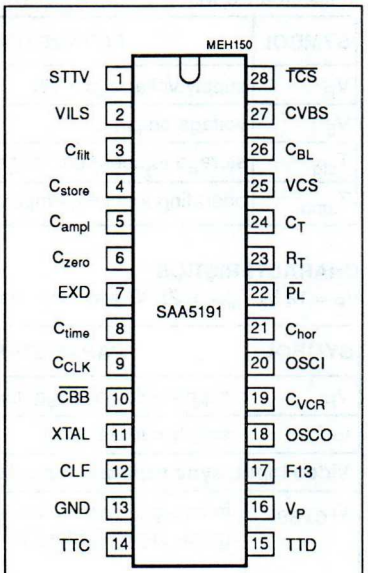


Fig.2 Pin configuration.

Notes to the pinning

(1) Sliced teletext data from external: active HIGH level (current), low impedance input.
(2) While the loop is locking up.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

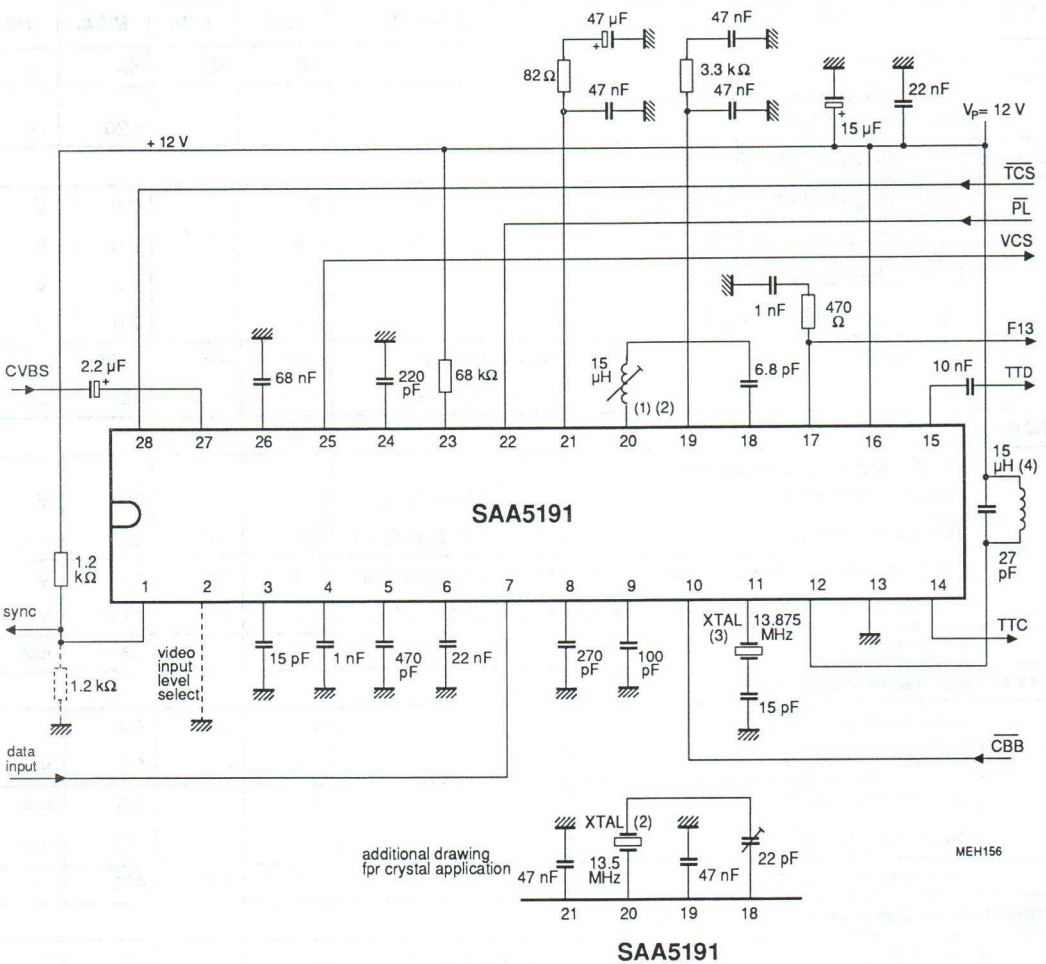
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 16)	0	13.2	V
V_5	voltage on pin 5	0	5.5	V
T_{stg}	storage temperature range	–20	125	°C
T_{amb}	operating ambient temperature range	0	+70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C and measurements taken in Fig.3, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 16)		10.8	12.0	13.2	V
I_P	supply current		50	70	105	mA
Video input, sync separator and data slicer		$Z_S \leq 250\ \Omega$				
$V_{i\ CVBS}$	input signal sync to white (peak-to-peak value, pin 27)	V_2 = LOW	0.7	1	1.4	V
		V_2 = HIGH	1.75	2.5	3.5	V
	sync amplitude (peak-to-peak value)		0.1	-	1	V
	data slicing level	V_2 = LOW	0.3	0.46	0.7	V
		V_2 = HIGH	0.75	1.15	1.75	V
V_2	input voltage LOW (pin 2)		0	-	0.8	V
	input voltage HIGH	open-circuit equals HIGH	2.0	-	5.5	V
I_2	input current LOW		0	-	–150	µA
	input current HIGH	V_2 < 5.5 V	0	-	1	mA
Teletext data output (TTD)						
V_{22}	phase lock pulse (PL) input voltage (peak-to-peak value, pin 22)	phase locked	0	-	3	V
		phase unlocked	3.9	-	5.5	V
$V_{o\ TTD}$	data output signal on pin 15 (peak-to-peak value)		2.5	3.5	4.5	V
V_{15}	DC output voltage	mean level	3	4	5	V
C_L	load capacitance on pin 15		-	-	40	pF
t_r, t_f	rise and fall time		20	30	45	ns
Teletext clock output (TTC)						
$V_{o\ TTC}$	clock output signal on pin 14 (peak-to-peak value)		2.5	3.5	4.5	V
V_{14}	DC output voltage	mean level	3	4	5	V
C_L	load capacitance on pin 14		-	-	40	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r, t_f	rise and fall time		20	30	45	ns
t_d	delay time of falling edge relative to other edges of TTD		-	-	±20	ns
Text/ scan composite sync input ($\overline{TCS}$/$\overline{SCS}$)						
V_{28}	input voltage LOW for $\overline{TCS}$ (pin 28)		0	-	0.8	V
	input voltage HIGH for $\overline{TSC}$		2.0	-	7.0	V
	input voltage LOW for $\overline{SCS}$		0	-	1.5	V
	input voltage HIGH for $\overline{SCS}$		3.5	-	7.0	V
I_{28}	input current	V_{28} = 0 to 7 V	–40	–70	–100	µA
		V_{28} = 10 to V_P	-	-	±5	µA
SYNC output buffer						
V_o	CVBS sync output signal on pin 1 (peak-to-peak value)	$R_{L\,1}$ = 1.2 kΩ to V_P	-	-	1	V
	$\overline{TCS}$ output signal	$R_{L\,1}$ = 1.2 kΩ to GND	200	450	650	mV
V_1	DC output voltage at positive sync signal	$R_{L\,1}$ = 1.2 kΩ to GND	1.0	1.4	2.0	V
	DC output voltage at negative sync signal	$R_{L\,1}$ = 1.2 kΩ to V_P	9.0	10.1	11.0	V
I_1	output current		-	-	±3	mA
Video composite sync output (VCS)						
V_{25}	output voltage LOW (pin 25)		0	-	0.4	V
	output voltage HIGH		2.4	-	5.5	V
I_{25}	output current LOW		0	-	0.5	mA
	output current HIGH		0	-	–1.5	mA
t_d	sync separator delay time		250	350	400	ns
Horizontal phase detector and 13.5 MHz VCO						
V_{10}	input voltage LOW ($\overline{CBB}$), pin 10	blanking inserted	0	-	0.5	V
	blanking insertion HIGH	no blanking	1.0	-	5.5	V
I_{10}	input current		-	-	–5	µA
V_o	13.5 MHz clock output signal (peak-to-peak value, pin 17)		1	2	3	V
V_{17}	DC output voltage	maximum swing	4	-	8.5	V
C_L	load capacitance on pin 17		-	-	40	pF
t_r, t_f	rise and fall time		10	-	30	ns



(1) inductance 15 µH at 1 kHz, C_o = 2.2 pF. Adjust free-running frequency to 13.5 ± 0.1 MHz or apply 13.5 MHz quarz crystal as shown in additional drawing

(2) Crystal: f = 13.5 MHz (e.g. Philips catalogue number 4322 143 04101); adjustment tolerance ±40 • 10^{-6}; load capacitance C_L = 22 pF; resonance resistance R_r = 22 pF; typical motional capacitance C_1 = 23 fF; static parallel capacitance C_o = 5.5 pF; frequency tolerance ±30• 10^{-6} in temperature range T = –20 to +70°. Adjust free-running frequency to 13.5 ± 0.5 MHz.

(3) Crystal: f = 13.875 MHz; adjustment tolerance ±40 • 10^{-6}; load capacitance C_L = 15 pF; typical resonance resistance R_r = 15 Ω (maximum 60 Ω); typical motional capacitance C_1 = 19 fF; static parallel capacitance C_o = 5 pF; frequency tolerance ±30• 10^{-6} in temperature range T = –20 to +70°.

(4) Coil: Fixed inductance 15 µH ±20%, quality factor Q > 20.

Fig.3 Test circuit and application circuit using LC-circuit or a crystal for VCO (clock F13).

TELETEXT VIDEO PROCESSOR

GENERAL DESCRIPTION

The SAA5231 is a bipolar integrated circuit intended as a successor to the SAA5030. It extracts Teletext Data from the video signal, regenerates Teletext Clock and synchronizes the text display to the television syncs. The integrated circuit is intended to work in conjunction with CCT (Computer Controlled Teletext), EUROM or other compatible devices.

Features

- Adaptive data slicer
- Data clock regenerator
- Adaptive sync separator, horizontal phase detector and 6 MHz VCO forming display phase locked loop (PLL)

QUICK REFERENCE DATA

Supply voltage (pin 16)	V_{CC}	typ.	12 V
Supply current (pin 16)	I_{CC}	typ.	70 mA
Video input amplitude (pin 27) (peak-to-peak value)			
pin 2 LOW	$V_{27\text{-}13(p\text{-}p)}$	typ.	1 V
pin 2 HIGH	$V_{27\text{-}13(p\text{-}p)}$	typ.	2,5 V
Storage temperature range	T_{stg}		−20 to + 125 °C
Operating ambient temperature range	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT117).

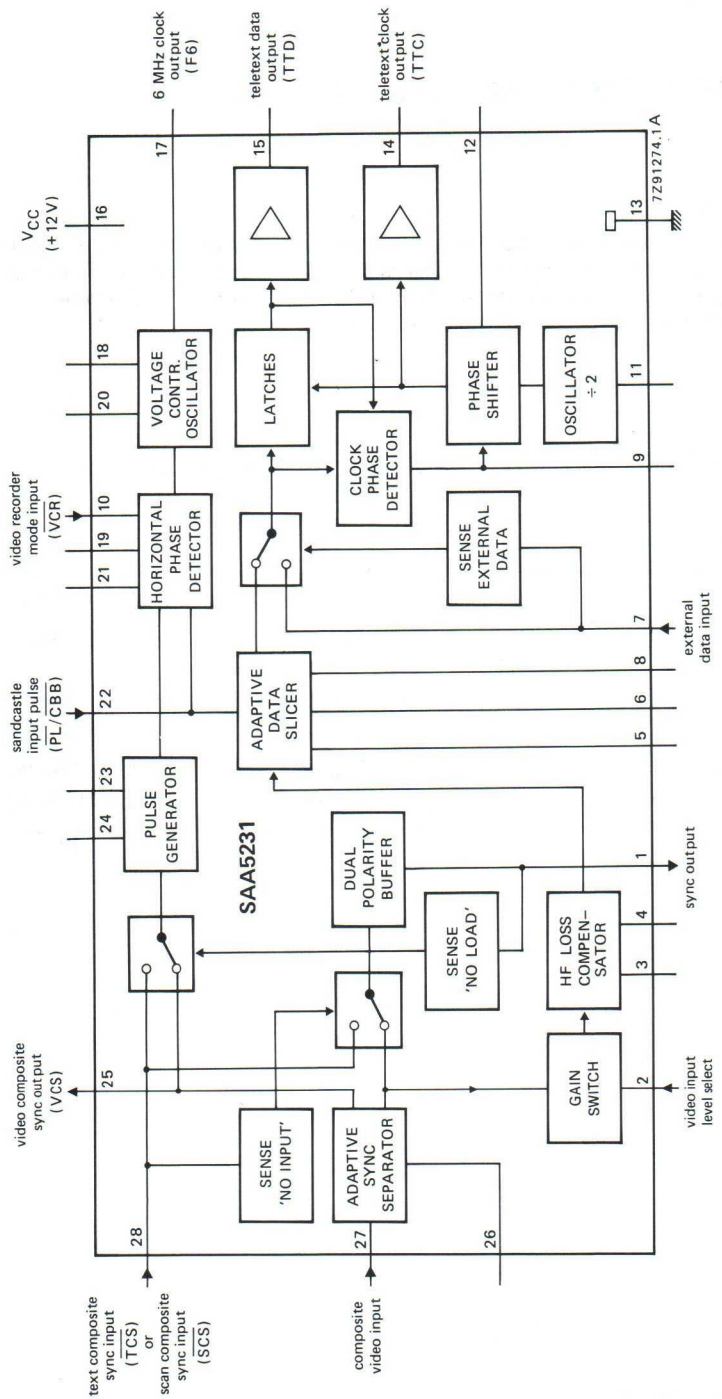


Fig. 1 Block diagram.

PINNING

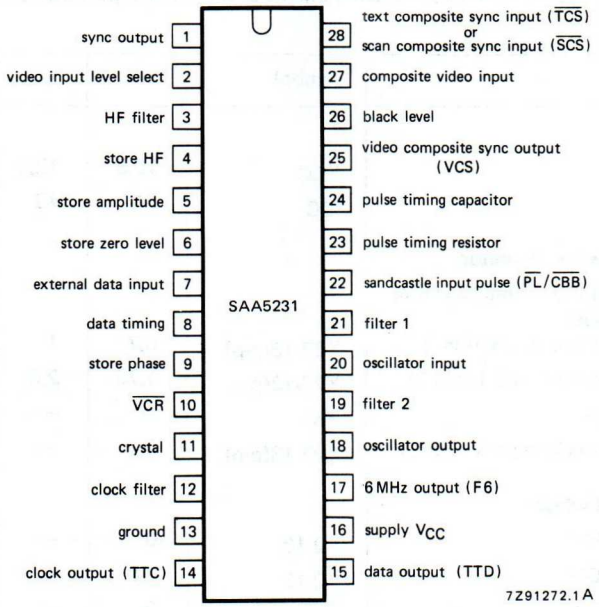


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 16)	V_{CC}	max. 13,2 V
Storage temperature range	T_{stg}	−20 to + 125 °C
Operating ambient temperature	T_{amb}	0 to + 70 °C

CHARACTERISTICS

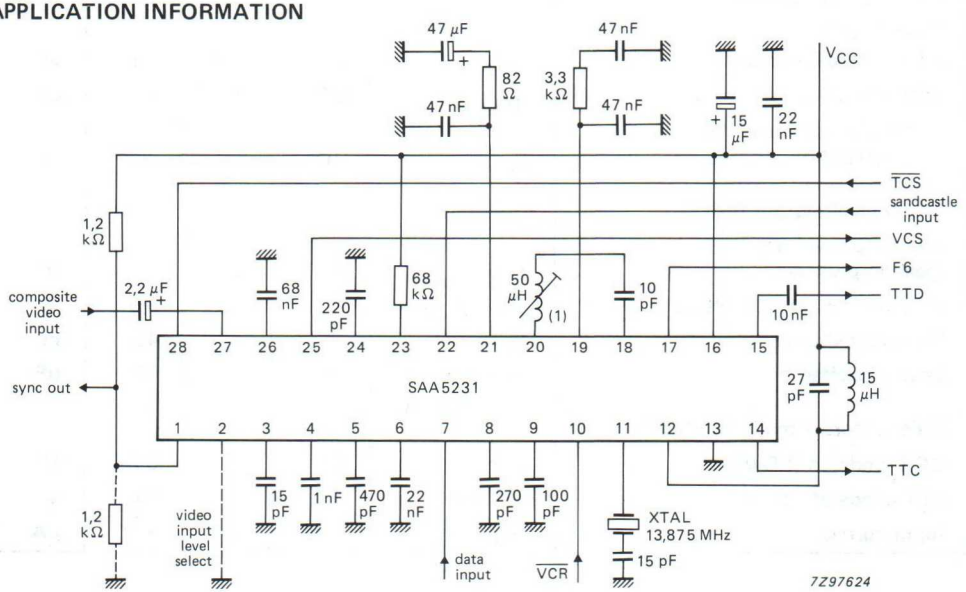
V_{CC} = 12 V; T_{amb} = 25 °C with external components as shown in application circuits unless otherwise stated.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{CC}	10,8	12,0	13,2	V
Supply current	I_{CC}	50	70	105	mA
Video input and sync separator					
Video input amplitude (sync to white) (peak-to-peak value)					
video input select level LOW (pin 2)	$V_{27\text{-}13(p\text{-}p)}$	0,7	1	1,4	V
video input select level HIGH (pin 2)	$V_{27\text{-}13(p\text{-}p)}$	1,75	2,5	3,5	V
Source impedance	$\lvert Z_s \rvert$	–	–	250	Ω
Sync amplitude (peak-to-peak value)	$V_{27\text{-}13(p\text{-}p)}$	0,1	–	1	V
Video input level select					
Input voltage LOW	$V_{2\text{-}13}$	0	–	0,8	V
Input voltage HIGH	$V_{2\text{-}13}$	2,0	–	5,5	V
Input current LOW	I_2	0	–	−150	μA
Input current HIGH	I_2	0	–	1	mA
Text composite sync input ($\overline{TCS}$)					
Input voltage LOW	$V_{28\text{-}13}$	0	–	0,8	V
Input voltage HIGH	$V_{28\text{-}13}$	2,0	–	7,0	V
Scan composite sync input ($\overline{SCS}$)					
Input voltage LOW	$V_{28\text{-}13}$	0	–	1,5	V
Input voltage HIGH	$V_{28\text{-}13}$	3,5	–	7,0	V
Select video sync from pin 1					
Input current (pin 28)					
at V_{28} = 0 to 7 V	I_{28}	−40	−70	−100	μA
at V_{28} = 10 V to V_{CC}	I_{28}	−5	–	+ 5	μA
Video composite sync output (VCS)					
Output voltage LOW	$V_{25\text{-}13}$	0	–	0,4	V
Output voltage HIGH	$V_{25\text{-}13}$	2,4	–	5,5	V
D.C. output current LOW	I_{25}	–	–	0,5	mA
D.C. output current HIGH	I_{25}	–	–	−1,5	mA
Sync separator delay time	t_d	0,25	0,35	0,40	μs

parameter	symbol	min.	typ.	max.	unit
Dual polarity buffer output					
$\overline{TCS}$ amplitude (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	0,20	0,45	0,65	V
Video sync amplitude (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	–	–	1	V
Output current	I_1	–3	–	+ 3	mA
D.C. output voltage					
R_L to ground (0 V)	$V_{1\text{-}13}$	1,0	1,4	2,0	V
R_L to V_{CC} (12 V)	$V_{1\text{-}13}$	9,0	10,1	11,0	V
Sandcastle input pulse ($\overline{PL}/\overline{CBB}$)					
Phase lock pulse (PL)					
PL on (LOW)	$V_{22\text{-}13}$	0	–	3	V
PL off (HIGH)	$V_{22\text{-}13}$	3,9	–	5,5	V
Blanking pulse (CBB)					
CBB on (LOW)	$V_{22\text{-}13}$	0	–	0,5	V
CBB off (HIGH)	$V_{22\text{-}13}$	1,0	–	5,5	V
Input current	I_{22}	–10	–	+ 10	μA
Phase locked loop (PLL)					
Phase detector timing					
Pulse duration using composite video	t_p	2,0	2,4	2,8	μs
using scan composite sync	t_p	3,0	3,5	4,0	μs
time PL must be LOW to make VCO run-free	t_L	100	–	–	μs
6 MHz clock output (F6)					
A.C. output voltage (peak-to-peak value)	$V_{17\text{-}13(p\text{-}p)}$	1	2	3	V
A.C. and d.c. output voltage range	$V_{17\text{-}13(max)}$	4	–	8,5	V
Rise and fall time	$t_r; t_f$	20	–	40	ns
Load capacitance	$C_{17\text{-}13}$	–	–	40	pF
Video recorder mode input ($\overline{VCR}$)					
VCR-mode on (LOW)	$V_{10\text{-}13}$	0	–	0,8	V
VCR-mode off (HIGH)	$V_{10\text{-}13}$	2,0	–	V_{CC}	V
Input current	I_{10}	–10	–	+ 10	μA

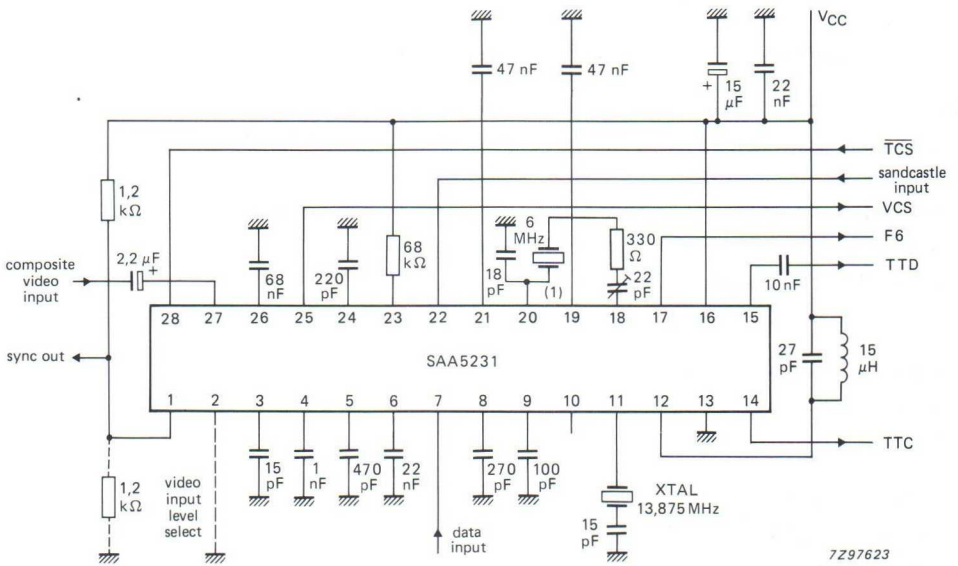
parameter	symbol	min.	typ.	max.	unit
Data slicer					
Data amplitude of video input (pin 27)					
video input level select LOW (pin 2)	V_{27-13}	0,30	0,46	0,70	V
video input level select HIGH (pin 2)	V_{27-13}	0,75	1,15	1,75	V
Teletext clock output					
A.C. output voltage (peak-to-peak value)	$V_{14-13(p-p)}$	2,5	3,5	4,5	V
D.C. output voltage (centre)	V_{14-13}	3,0	4,0	5,0	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	t_r; t_f	20	30	45	ns
Delay of falling edge relative to other edges of TTD	t_d	−20	0	+ 20	ns
Teletext data output					
A.C. output voltage (peak-to-peak value)	$V_{15-13(p-p)}$	2,5	3,5	4,5	V
D.C. output voltage (centre)	V_{15-13}	3,0	4,0	5,0	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	t_r; t_f	20	30	45	ns

APPLICATION INFORMATION



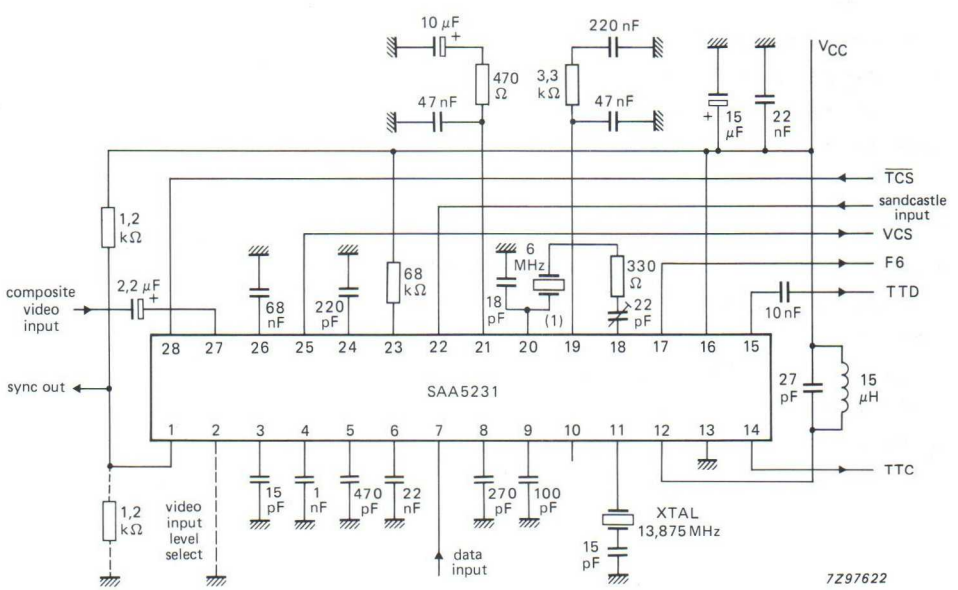
(1) Coil: 50 µH at 1 kHz, C_o = 4 pF. Adjust the free-running frequency to 6000 kHz ± 30 kHz.

Fig. 3a Application circuit using L/C circuit in PLL.



(1) Quartz crystal e.g. catalogue number 4322 143 04101. Adjust the free-running frequency to 6000,2 kHz ± 0,2 kHz.

Fig. 3b Application circuit using quartz crystal in PLL.



(1) Ceramic resonator e.g. Kyocera KBR 6,0 M. Adjust the free-running frequency to 6010 kHz ± 5 kHz.

Fig. 3c Application circuit using ceramic resonator in PLL.

Component specifications

Specifications of some external components in Figs 3a, 3b and 3c.

Quartz crystal 13,875 MHz; Figs 3a, 3b and 3c

Load resonance frequency (f) 13,875 MHz; adjustment tolerance $\pm 40 \cdot 10^{-6}$

Load capacitance (C_L) 20 pF

Temperature range (T) −20 to +70 °C; frequency tolerance maximum $\pm 30 \cdot 10^{-6}$

Resonance resistance (R_r) typical 10 Ω maximum 60 Ω

Motional capacitance (C_1) typical 19 fF

Static parallel capacitance (C_0) typical 5 pF

Fixed inductance Figs 3a, 3b and 3c

Inductance (L) 15 μH ± 20%

Quality factor (Q) minimum 20

Variable inductance Fig. 3a

Inductance (L) 50 μH at 1 kHz

Static parallel capacitance (C_0) typical 4 pF

Quartz crystal Fig. 3b

Preferred type 4322 143 04101

Load resonance frequency (f) 6 MHz; adjustment tolerance $\pm 40 \cdot 10^{-6}$

Load capacitance (C_L) 20 pF

Temperature range (T) −20 to +70 °C; frequency tolerance $\pm 30 \cdot 10^{-6}$

Resonance resistance (R_r) 60 Ω

Motional capacitance (C_1) typical 28 fF

Static parallel capacitance (C_0) typical 7 pF

Ceramic resonator; Fig. 3c

Preferred type KBR 6,0 M, Kyocera

Load resonance frequency (f) 6 MHz; adjustment tolerance ± 0,5%

Load capacitance (C_L) 20 pF

Temperature range (T) −20 to +70 °C; frequency tolerance maximum ± 0,3%

Resonance resistance (R_r) typical 6 Ω

Motional capacitance (C_1) typical 9 pF

Static parallel capacitance (C_0) typical 60 pF

Ageing (10 years) f maximum ± 0,3%

The function is quoted against the corresponding pin number.

1. **Synch output to TV**

   Output with dual polarity buffer, a load resistor to 0 V or + 12 V selects positive-going or negative-going syncs.

2. **Video input level select**

   When this pin is LOW a 1 V video input level is selected. When the pin is not connected it floats HIGH selecting a 2,5 V video input level.

3. **HF filter**

   The video signal for the h.f.-loss compensator is filtered by a 15 pF capacitor connected to this pin.

4. **Store h.f.**

   The h.f. amplitude is stored by a 1 nF capacitor connected to this pin.

5. **Store amplitude**

   The amplitude for the adaptive data slicer is stored by a 470 pF capacitor connected to this pin.

6. **Store zero level**

   The zero level for the adaptive data slicer is stored by a 22 nF capacitor connected to this pin.

7. **External data input**

   Current input for sliced teletext data from external device.
   Active HIGH level (current), low impedance input.

8. **Data timing**

   A 270 pF capacitor is connected to this pin for timing of the adaptive data slicer.

9. **Store phase**

   The output signal from the clock phase detector is stored by a 100 pF capacitor connected to this pin.

10. **Video tape recorder mode ($\overline{\text{VCR}}$)**

    Signal input to command PLL into short time constant mode. Not used in application circuit Fig. 3b or Fig. 3c.

11. **Crystal**

    A 13,875 MHz crystal, 2 x data rate, connected in series with a 15 pF capacitor is applied via this pin to the oscillator and divide-by-two to provide the 6,9375 MHz clock signal.

12. **Clock filter**

    A filter for the 6,9375 MHz clock signal is connected to this pin.

13. **Ground (0 V)**

14. **Teletext clock output (TTC)**

    Clock output for CCT (Computer Controlled Teletext).

APPLICATION INFORMATION (continued)

15. **Teletext data output (TTD)**

    Data output for CCT.

16. **Supply voltage V_{CC} (+ 12 V typ.)**

17. **Clock output (F6)**

    6 MHz clock output for timing and sandcastle generation in CCT.

18. **Oscillator output (6 MHz)**

    A series resonant circuit is connected between this pin and pin 20 to control the nominal frequency of the VCO.

19. **Filter 2**

    A filter with a short time constant is connected to this pin for the horizontal phase detector. It is used in the video recorder mode and while the loop is locking up.

20. **Oscillator input (6 MHz)**

    See pin 18.

21. **Filter 1**

    A filter with a long time constant is connected to this pin for the horizontal phase detector.

22. **Sandcastle input pulse ($\overline{PL}/\overline{CBB}$)**

    This input accepts a sandcastle waveform, which is formed from PL and CBB from the CCT. Signal timing is shown in Fig. 4.

23. **Pulse timing resistor**

    The current for the pulse generator is defined by a 68 kΩ resistor connected to this pin.

24. **Pulse timing capacitor**

    The timing of the pulse generator is determined by a 220 pF capacitor connected to this pin.

25. **Video composite sync output (VCS)**

    This output signal is for CCT.

26. **Black level**

    The black level for the adaptive sync separator is stored by a 68 nF capacitor connected to this pin.

27. **Composite video input (CVS)**

The composite video signal is input via a 2,2 μF clamping capacitor to the adaptive sync separator.

28. **Text composite sync input ($\overline{\text{TCS}}$)/Scan composite sync input ($\overline{\text{SCS}}$)**

$\overline{\text{TCS}}$ is input from CCT or $\overline{\text{SCS}}$ from external sync circuit. $\overline{\text{SCS}}$ is expected when there is no load resistor at pin 1. If pin 28 is not connected the sync output on pin 1 will be the composite video input at pin 27, internally buffered.

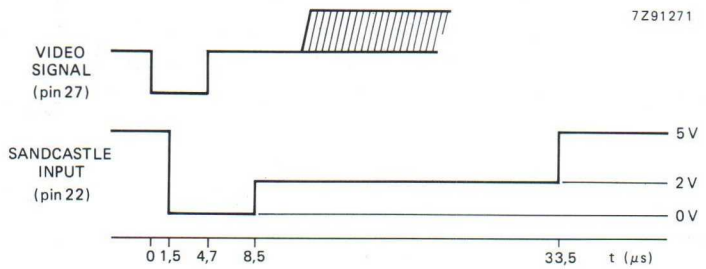


Fig. 4 Sandcastle waveform and timing.

Dual standard VPT decoder and clock calendar

SAA5232

FEATURES

- Digital data slicer
- Separate storage of VPS data (PDC System A) and packet 8/30/2 data (PCD System B) allowing dual standard VPT decoders
- I²C-bus interface with automatic word address increment
- Clock/calendar function with programmable alarm
- Programmable interrupt for data received and alarm
- Low power and low voltage clock/calendar operation
- 256 by 8-bit free static RAM
- SO24L and DIL24 packages

GENERAL DESCRIPTION

Allowing the reception and decoding of both VPS (EBU PDC System A) and packet 8/30/2 (EBU PDC System B) data, the SAA5232 is a dual standard VPS decoder intended for use in manually programmed European video recorders. It incorporates a clock calendar with programmable alarm and permits the reception of real time broadcast switching signals to allow the accurate timing of programme recording.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.5	5	5.5	V
I_{DD}	supply current		–	36	72	mA
V_{DD}bak	supply battery back-up		2	–	–	V
I_{DD}bak	supply current battery back-up	V_{DD}_B = 2 V	–	2	15	µA
V_{syn}	sync amplitude		0.1	0.3	0.6	V
V_{vid}	video amplitude		0.7	1	1.4	V
f_{vpt}	crystal frequency VPT decoder		–	27	–	MHz
f_{clk}	crystal frequency clock calendar		–	32.768	–	kHz

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5232P	24	DIL	plastic	SOT101
SAA5232T	24	mini-pack	plastic	SOT137

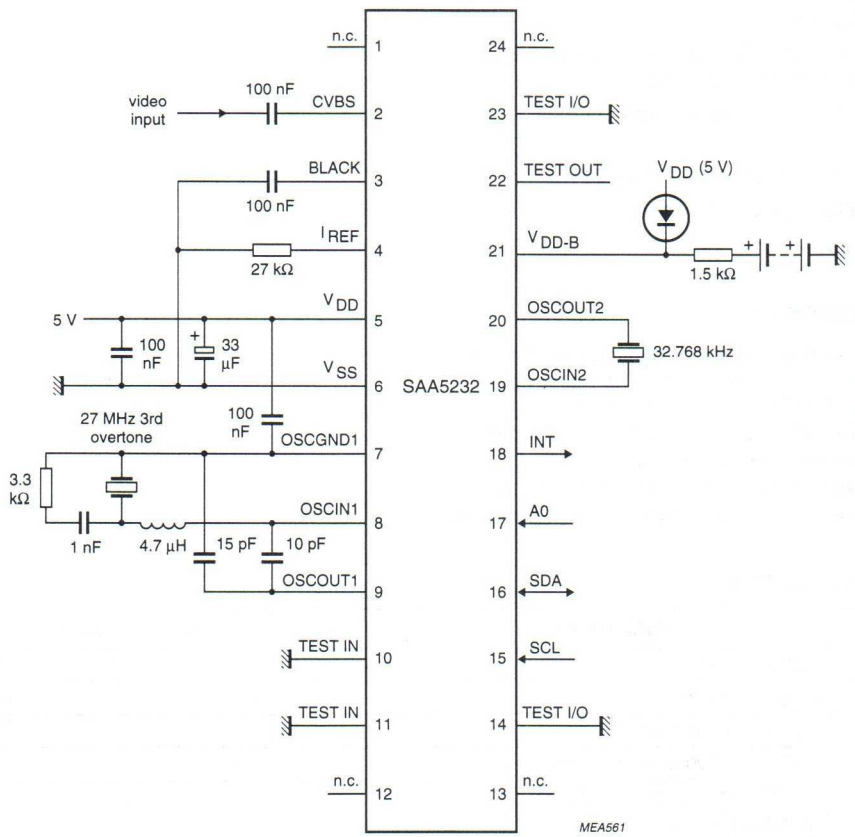


Fig.1 Application diagram.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Dual standard PDC decoder SAA5233

FEATURES

- Digital data slicer
- Acquisition and decoding of VPS data (EBU PDC System A)
- Acquisition and decoding of Teletext packet 8/30/2 data (EBU PDC System B)
- Separate storage of VPS data and packet 8/30/2 allowing dual standard PDC decoders
- I²C-bus interface with automatic word address increment
- Programmable interrupt for data received
- Programmable error level detection
- Single +5 V power supply.

GENERAL DESCRIPTION

The SAA5233 is a dual standard Program Delivery Control (PDC) decoder, allowing the reception and decoding of both VPS data (EBU PDC System A) and Teletext packet 8/30/2 data (EBU PDC System B). It is intended for use in European video recorders which are manually programmed, so that they receive broadcast real time switching signals for accurate timing of program recording.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	30	45	mA
f_{clk}	crystal input frequency	–	27	–	MHz
V_{sync}	CVBS sync voltage amplitude	0.1	0.3	0.6	V
$V_{vid(p-p)}$	CVBS video voltage amplitude (peak-to-peak value)	0.7	1.0	1.4	V
T_{amb}	operating ambient temperature	–20	–	+70	°C
T_{stg}	storage temperature	–55	–	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5233P	16	DIP16	plastic	SOT38-1
SAA5233T	20	SO20L	plastic	SOT163-1

BLOCK DIAGRAM

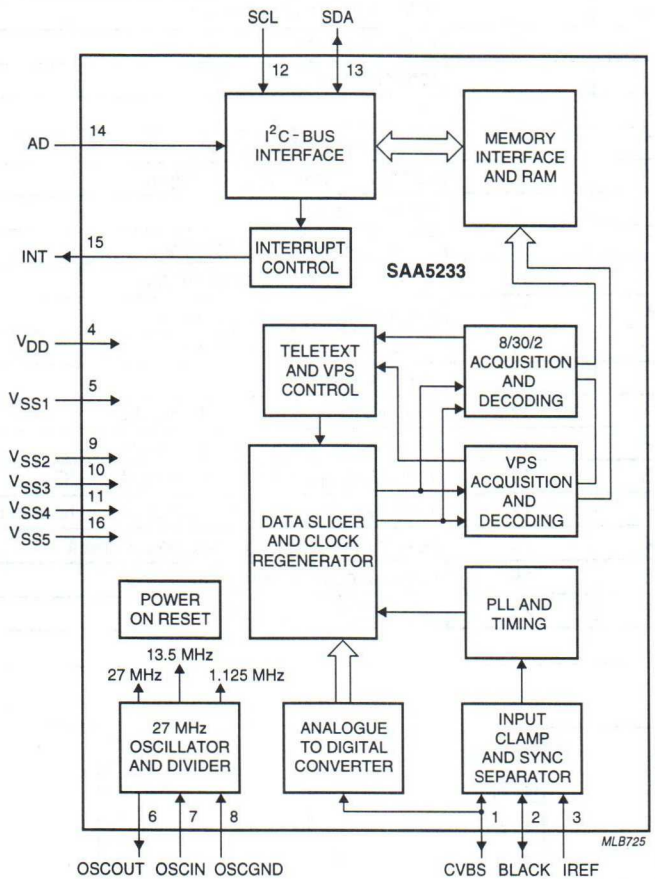


Fig.1 Block diagram; pin numbers for DIP16.

PINNING

SYMBOL	PIN		DESCRIPTION
	DIP16	SO20L	
CVBS	1	1	composite video input
BLACK	2	2	video black level storage pin
n.c.	–	3	not connected
IREF	3	4	reference current input
V_{DD}	4	5	+5 V supply
V_{SS1}	5	6	0 V ground 1 (main ground pin)
OSCOUT	6	7	27 MHz crystal oscillator output
n.c.	–	8	not connected
OSCIN	7	9	27 MHz crystal oscillator input
OSCGND	8	10	27 MHz crystal oscillator ground
V_{SS2}	9	11	0 V ground 2; connect to V_{SS1}
V_{SS3}	10	12	0 V ground 3; connect to V_{SS1}
n.c.	–	13	not connected
V_{SS4}	11	14	connect to V_{SS1} in normal operation
SCL	12	15	serial clock open-drain input for I^2C-bus
SDA	13	16	serial data open-drain input/output for I^2C-bus
i.c.	–	17	internally connected; do not connect in normal operation
AD	14	18	programmable I^2C-bus address bit input
INT	15	19	interrupt open-drain output
V_{SS5}	16	20	connect to V_{SS1} in normal operation

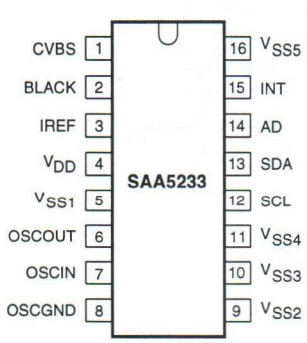


Fig.2 Pin configuration; DIP16.

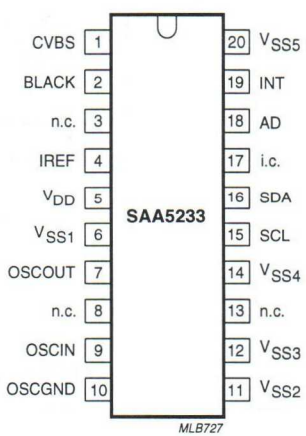


Fig.3 Pin configuration; SO20L.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.3	+6.5	V
V_{Imax}	maximum input voltage (any input)	−0.3	V_{DD} + 0.3	V
V_{Omax}	maximum output voltage (any output)	−0.3	V_{DD} + 0.3	V
I_{IOmax}	maximum DC input or output diode current	–	±20	mA
I_{Omax}	maximum output current (any output)	–	±10	mA
T_{amb}	operating ambient temperature	−20	+70	°C
T_{stg}	storage temperature	−55	+125	°C

QUALITY AND RELIABILITY

This device will meet the requirements of the *"Philips Semiconductors General Quality Specification SNW-FQ-611E"* in accordance with *"Quality Reference Pocketbook (order number 9398 510 34011)"*. The principal requirements are as shown in Tables 1 to 4.

Group A

Table 1 Acceptance tests per lot.

TEST	REQUIREMENTS(1)
Mechanical	cumulative target: <100 ppm
Electrical	cumulative target: <100 ppm

Group B

Table 2 Processability tests (by package family).

TEST	REQUIREMENTS(1)
Solderability	<7% LTPD
Mechanical	<15% LTPD
Solder heat resistance	<15% LTPD

Group C

Table 3 Reliability tests (by process family).

TEST	CONDITIONS	REQUIREMENTS(1)
Operational life	168 hours at T_j = 150 °C	<1500 FPM; equivalent to <100 FITS at T_j = 70 °C
Humidity life	temperature, humidity, bias (1000 hours, 85 °C, 85% RH or equivalent test)	<2000 FPM
Temperature cycling performance	$T_{stg(min)}$ to $T_{stg(max)}$	<2000 FPM

Table 4 Reliability tests (by device type).

TEST	CONDITIONS	REQUIREMENTS(1)
ESD and latch-up	ESD Human body model 2000 V; 100 pF; 1.5 kΩ	<15% LTPD
	ESD Machine model 200 V; 200 pF; 0 Ω	<15% LTPD
	latch-up 100 mA; 1.5 × V_{DD} (absolute maximum)	<15% LTPD

Note to Tables 1 to 4.

1. ppm = fraction of defective devices, in parts per million.
   LTPD = Lot Tolerance Percent Defective.
   FPM = fraction of devices failing at test condition, in Failures Per Million.
   FITS = Failures In Time Standard.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = –20 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DD}	supply current		–	30	45	mA
Inputs						
CVBS						
V_{sync}	sync voltage amplitude		0.1	0.3	0.6	V
$V_{vid(p-p)}$	video voltage amplitude (peak-to-peak value)		0.7	1.0	1.4	V
$V_{dat(text)}$	Teletext data voltage amplitude		0.30	0.46	0.70	V
$V_{dat(vps)}$	VPS data voltage amplitude		0.30	0.50	0.70	V
Z_{source}	source impedance		–	–	250	Ω
Z_I	input impedance		2.5	5.0	–	kΩ
C_I	input capacitance		–	–	10	pF
IREF						
R_{gnd}	resistor to ground		–	27	–	kΩ
V_{IREF}	input reference voltage		–	$0.5V_{DD}$	–	V
AD						
V_{IL}	LOW level input voltage		–0.3	–	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
SCL						
V_{IL}	LOW level input voltage		–0.3	–	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
f_{clk}	clock frequency		0	–	100	kHz
t_r	input rise time	$0.3V_{DD}$ to $0.7V_{DD}$	–	–	1000	ns
t_f	input fall time	$0.7V_{DD}$ to $0.3V_{DD}$	–	–	300	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
INT (OPEN-DRAIN OUTPUT)						
V_{PU}	pull-up voltage at pin		–	–	V_{DD}	
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.4	V
I_{OL}	LOW level output current		–	–	4.0	mA
C_L	load capacitance		–	–	400	pF
t_f	output fall time	C_L = 100 pF; $0.7V_{DD}$ to $0.3V_{DD}$	–	–	100	ns
Inputs/Outputs						
BLACK						
C_{black}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
SDA (OPEN-DRAIN OUTPUT)						
V_{IL}	LOW level input voltage		–0.3	–	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	400	pF
t_r	input rise time	$0.3V_{DD}$ to $0.7V_{DD}$	–	–	1000	ns
t_f	input fall time	$0.7V_{DD}$ to $0.3V_{DD}$	–	–	300	ns
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.4	V
t_f	output fall time	C_L = 400 pF; $0.7V_{DD}$ to $0.3V_{DD}$	–	–	200	ns
CRYSTAL OSCILLATOR (OSCIN; OSCOUT)						
V_{osc}	oscillator voltage amplitude (peak-to-peak value)		–	1.0	–	V
G_v	small signal voltage gain		–	1.0	–	
C_I	input capacitance		–	–	10	pF
C_{fb}	feedback capacitance		–	1	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus timing (see Fig.4)						
f_{clk}	SCL clock frequency		0	–	100	kHz
t_{BUF}	bus free time between a STOP and START		4.7	–	–	µs
$t_{HD;STA}$	repeated START hold time	note 1	4.0	–	–	µs
t_{LOW}	SCL clock LOW time		4.7	–	–	µs
t_{HIGH}	SCL clock HIGH time		4.0	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START		4.7	–	–	µs
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;DAT}$	data set-up time		250	–	–	ns
t_r	SDA, SCL input rise time	$0.3V_{DD}$ to $0.7V_{DD}$	–	–	1 000	ns
t_f	SDA, SCL input fall time	$0.7V_{DD}$ to $0.3V_{DD}$	–	–	300	ns
$t_{SU;STO}$	set-up time for STOP		4.0	–	–	µs

Note

1. After this time the first clock pulse is generated.

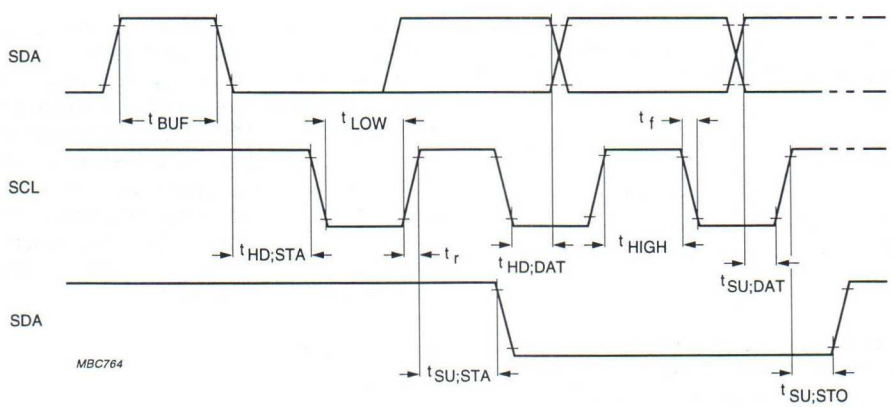


Fig.4 I²C-bus timing diagram.

FUNCTIONAL DESCRIPTION

Control of device

The function of the device is controlled via the I²C-bus. Pin AD provides a choice of two alternative addresses.

The PDC acquisition section requires little software control apart from enabling the interrupts which occur when data is found. Interrupts can be enabled for either Teletext packet 8/30/2 or VPS and both can be enabled to allow for the presence of both standards being transmitted on the same TV channel. The interrupt register is accessed as address 01 WRITE, see Section "Register 01: Interrupt (reset state X00X XXXX)".

When an interrupt is signalled, a bit is set in the status register to indicate its source. Information about the received PDC data is given in the status register D5 and D6. The microcontroller must service the 'data received' interrupts within 40 ms (VPS) or 200 ms (Teletext packet 8/30/2), since new data may be written after this period. The status register is accessed as address 00 READ; see Section "Register 00:Control/Status (reset state XXX0 XX00)". When the status register has been read the data received flags and interrupt signal are reset.

Data of both types is constantly received and stored, but can be selectively acquired by setting bits D1 and D0 of the control register. This allows acquisition of only Teletext packet 8/30/2 on every VBI line or only VPS data on every VBI line. The control register is accessed as address 00 WRITE, see Section "Register 00:Control/Status (reset state XXX0 XX00)".

Storage of PDC data

The PDC data memory is accessed at address 02 (HEX) to 31 (HEX). The exact addresses of Teletext packet 8/30/2 and VPS data is shown in Table 5.

TELETEXT DATA

The Teletext packet 8/30/2 data is stored after hardware Hamming correction. There are 4 data bits stored in the lower nibble of each byte in address 11 (HEX) to 1D (HEX); see Table 13, in the order shown in Table 5. The status message, which is odd parity coded, is stored as a byte which represents a Teletext character in address 1E (HEX) to 31 (HEX); see Table 14.

VPS DATA

The VPS data from Line 16 is stored in register address 02 (HEX) to 0F (HEX) in the order shown in Table 5. VPS data is biphase decoded and stored with 4 data bits stored in the lower nibble of each byte, in the same way as Teletext packet 8/30/2 data; see Tables 11 and 12. In addition to the VCR data, Word 4 (Program Source Identification, ASCII sequential) is stored, which may be useful for future applications.

The stored data is read via the I²C-bus in the normal way. Multiple reception/majority error correction of the data is the responsibility of the control software, the device simply stores the data as transmitted after Hamming or biphase decoding. As both VPS and Teletext packet 8/30/2 signals are stored separately, it is possible to deal with future situations where both EBU PDC System A and EBU PDC System B transmissions may be present on the same TV channel, the defaults and level of service being chosen by the software control.

Error indication

Indication of errors in the received data is given in two ways and is programmable by setting bit D4 in the control register.

The first is a flag to indicate Hamming or biphase errors and is stored with the related data in bit 0 of the upper nibble of the data byte.

The second is no interrupt which is sent to the microcontroller but the data signal quality bit (D7) is set.

The level of interrupt is controlled by the Interrupt Error Level bit which is D4 of the control register. If this bit is not set then an interrupt only occurs if an error free line of either Teletext packet 8/30/2 or VPS data is received and stored in RAM. If this bit is set then an interrupt occurs if the correct framing code and Teletext packet header 8/30/2 is found, or the correct start code for VPS data is found. The data is then stored in the RAM with any errors indicated in the upper nibble. This may be used by more sophisticated software, which could decide the importance of an error in a particular nibble.

I²C-bus interface

FEATURES

- Standard I²C-bus slave transceiver
- Operates from 0 to 100 kHz
- Acknowledge function is performed
- Auto-increment between registers and direct addressing
- Selectable I²C-bus slave address dependent on address pin AD.

Register map

The data received when address locations 00 (HEX) to 31 (HEX) are read or written is shown in Table 5.

Table 5 Register map.

ADDRESS (HEX)	DATA[1]	ADDRESSING
00	control/status	direct
01	interrupt	direct
02	VPS B5	direct/auto-increments to 03
03	VPS B5	direct/auto-increments to 04
04	VPS B11	direct/auto-increments to 05
05	VPS B11	direct/auto-increments to 06
06	VPS B12	direct/auto-increments to 07
07	VPS B12	direct/auto-increments to 08
08	VPS B13	direct/auto-increments to 09
09	VPS B13	direct/auto-increments to 0A
0A	VPS B14	direct/auto-increments to 0B
0B	VPS B14	direct/auto-increments to 0C
0C	VPS B15	direct/auto-increments to 0D
0D	VPS B15	direct/auto-increments to 0E
0E	VPS B4	direct/auto-increments to 0F
0F	VPS B4	stop value
10	–	direct
11	8/30/2 B13	direct/auto-increments to 12
12	8/30/2 B14	direct/auto-increments to 13
13	8/30/2 B15	direct/auto-increments to 14
14	8/30/2 B16	direct/auto-increments to 15
15	8/30/2 B17	direct/auto-increments to 16
16	8/30/2 B18	direct/auto-increments to 17
17	8/30/2 B19	direct/auto-increments to 18
18	8/30/2 B20	direct/auto-increments to 19
19	8/30/2 B21	direct/auto-increments to 1A
1A	8/30/2 B22	direct/auto-increments to 1B
1B	8/30/2 B23	direct/auto-increments to 1C
1C	8/30/2 B24	direct/auto-increments to 1D
1D	8/30/2 B25	direct/auto-increments to 1E
1E	status message	direct/auto-increments to 1F
:	:	direct/auto-increments
31	status message	stop value

Note

1. For the address range 02H to 0FH, even addresses hold the least significant nibble and odd addresses hold the most significant nibble. BXX refers to byte definitions, EBU specification of the domestic video PDC system.

Register 00:Control/Status (reset state XXX0 XX00)

Register 00 is split into two parts. The control part (WRITE only) consisting of bits D4, D1 and D0 and status part (READ only) consisting of bits D7 to D5.

Table 6 Register 00.

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	IEL	–	–	ACQ 8/30/2	ACQ VPS
DSQ	8/30/2 RF	VPS RF	–	–	–	–	–

Table 7 Register 00 bit description.

SYMBOL	BIT	FUNCTION
IEL	D4	Interrupt Error Level. When logic 0, signal only completely valid data lines from Teletext packet 8/30/2 received and VPS received flags. When logic 1, signal valid framing code and Teletext packet header 8/30/2 received or valid start codeword for VPS received.
ACQ 8/30/2 ACQ VPS	D1 D0	Acquire 8/30/2. Acquire VPS. Allows selective decoding of either Teletext packet 8/30/2 data or VPS data. If both are set to the same value the system automatically selects the format being transmitted (see Table 8).
DSQ	D7	Data Signal Quality. When logic 1, good Teletext or VPS data signal is being received. When logic 0, no Teletext or VPS data signal is being received.
8/30/2 RF	D6	8/30/2 Received Flag. When logic 1, and IEL (D4) = logic 0 an error-free Teletext packet 8/30/2 has been received, Hamming decoded and stored in the RAM. When logic 1, and IEL(D4) = logic 1 a Teletext packet with a valid framing code and 8/30/2 header has been received, Hamming decoded and stored in RAM. When logic 0 no Teletext packet 8/30/2 data received.
VPS RF	D5	VPS Received Flag. When logic 1, and IEL(D4) = logic 0, an error-free VPS data line has been received, biphase decoded and stored in the RAM. When logic 1, and IEL(D4) = logic 1 a VPS data line with valid start code has been received, biphase decoded and stored in RAM. When logic 0 no VPS data received.

Table 8 Selection of Teletext packet 8/30/2 data or VPS data.

ACQ 8/30/2	ACQ VPS	FUNCTION
0	0	use automatic selection algorithm for line 16
0	1	acquire only VPS data on every VBI line
1	0	acquire only 8/30/2 data on every line 16
1	1	use automatic selection algorithm for line 16

Register 01: Interrupt (reset state X00X XXXX)

Register R01 is WRITE only.

Table 9 Register 01.

D7	D6	D5	D4	D3	D2	D1	D0
–	8/30/2 IE	VPS IE	–	–	–	–	–

Table 10 Register 01 bit description.

SYMBOL	BIT	FUNCTION
8/30/2 IE	D6	8/30/2 Interrupt Enable. This allows the reception of Teletext packet 8/30/2 data to be signalled on the INT pin. When logic 0 reception of Teletext packet 8/30/2 data is not signalled on INT pin. When logic 1 reception of Teletext packet 8/30/2 data is signalled on INT pin.
VPS IE	D5	VPS Interrupt Enable. This allows the reception of VPS data to be signalled on the INT pin. When logic 0 reception of VPS data is not signalled on INT pin. When logic 1 reception of VPS data is signalled on INT pin.

Register 02 to 0F (HEX): VPS data bytes

A single VPS data bytes is stored as two memory bytes, the least significant nibble of both memory bytes is the data making up the single VPS data byte. The most significant nibble of each memory byte is used to indicate a biphase error in the least significant nibble. This is indicated by the least significant bit being set, the top three bits are not used and are fixed to logic 0 (see Table 11).

Table 11 VPS data bytes.

ADDRESS (HEX)	REGISTER	DATA
02	VPS B5 least significant nibble	0000 1100[1]
03	VPS B5 most significant nibble	0000 0101[1]

Note

1. Equivalent to VPS B5 0101 1100 (MSB to LSB).

Table 12 Register 02.

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	BIPHASE ERROR BIT	DATA BIT 3	DATA BIT 2	DATA BIT 1	DATA BIT 0

Register 11 to 1D (HEX): Teletext packet 8/30/2 data bytes

Data is stored as single bytes. The four least significant bits represent the data. The fifth bit if set indicates a Hamming error in the stored data. The top three bits of the byte are not used and are fixed to logic 0.

Table 13 Register 11.

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	HAMMING ERROR BIT	DATA BIT 3	DATA BIT 2	DATA BIT 1	DATA BIT 0

Register 1E to 31D (HEX): Status display message

Data is stored as bytes which represent a Teletext character. The data is odd parity checked, if a parity error occurs this causes the byte not to be written to the RAM. The MSB is not used and is fixed to logic 0.

Table 14 Register 11.

D7	D6	D5	D4	D3	D2	D1	D0
–	DATA BIT 6	DATA BIT 5	DATA BIT 4	DATA BIT 3	DATA BIT 2	DATA BIT 1	DATA BIT 0

I²C-bus slave address

The slave address for the device can take one of two values dependent on the state of the input pin AD.

Table 15 Device address.

AD	SLAVE ADDRESS
0	0010 001X(1)
1	0010 000X(1)

Note

1. Where X is the R/$\overline{W}$ bit.

I²C-bus increment

The I²C-bus will also increment between registers as listed in Table 16

Table 16 Increment between registers.

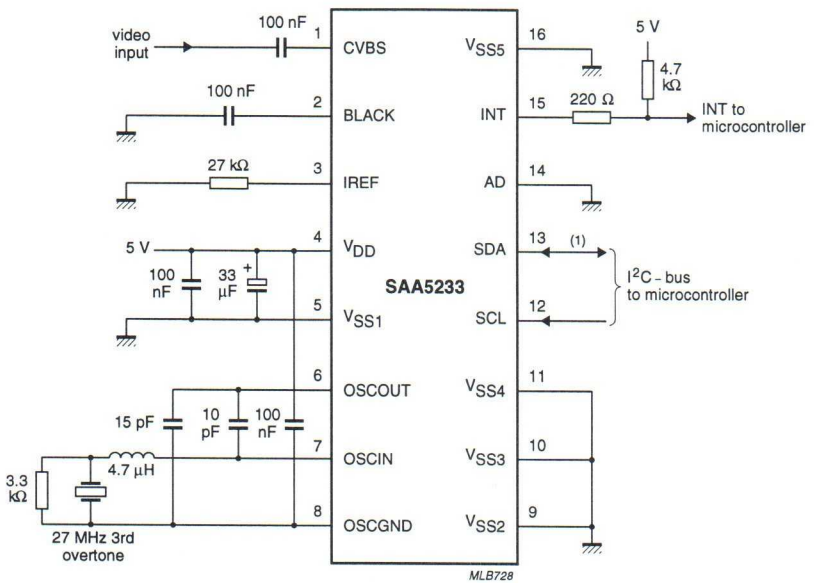
ADDRESS	CONTENTS
02 to 0F (HEX)	VPS data bytes
11 to 31 (HEX)	Teletext packet 8/30/2 data bytes and Status display message

Addressing any register in either of these ranges will initialize an increment until the final stop value provided each byte is acknowledged by the receiver.

Initialization during power-up

The device has an internal power-on reset unit which is used to reset the I²C-bus interface to be a slave transceiver. It also initializes the device to receive only completely valid Teletext packet 8/30/2 and VPS data. The interrupt signals for both Teletext packet 8/30/2 and VPS are disabled.

APPLICATION INFORMATION



(1) I²C-bus address 0010 001R/$\overline{W}$.

Fig.5 Application diagram; DIL16.

Table 17 Crystal characteristics.

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)				
C1	series capacitance	1.7	–	pF
C0	parallel capacitance	5.2	–	pF
C_L	load capacitance	20	–	pF
R_r	resonance resistance	–	50	Ω
R1	series resistance	20	–	Ω
X_a	ageing	–	$\pm 5 \times 10^{-6}$	$year^{-1}$
X_j	adjustment tolerance	–	$\pm 25 \times 10^{-6}$	
X_d	drift	–	$\pm 25 \times 10^{-6}$	

ENHANCED COMPUTER CONTROLLED TELETEXT CIRCUITS
(ECCT)

GENERAL DESCRIPTION

The SAA5243 series are MOS N-channel integrated circuits which perform all the digital logic functions of a 625-line World System Teletext decoder. The SAA5243 series operate in conjunction with the teletext video processor SAA5231, standard static RAMs and are controlled via the 2-wire I²C-bus. The devices can be used to provide videotex display conforming to a serial character attribute protocol.

Features

- Microcomputer controlled for flexibility
- High quality flicker-free display using a 12 x 10 character matrix
- Field flyback (lines 2 to 22), or full channel (all lines) data acquisition
- Up to four simultaneous page requests enabling acquisition during one magazine cycle
- Direct interface up to 8 K bytes static RAM
- Automatic language section of up to seven different languages
- 25th display row for software generated status messages
- Cursor control for videotex/telesoftware
- 7-bits parity or 8-bit data acquisition
- Extension packet reception option
- Standard I²C-bus slave transceiver (slave address 0010001)
- Single 5 volt power supply
- Mask programmable character sets
- Slave sync mode operation
- $\overline{\text{Odd}}$/even field output for de-interlaced displays

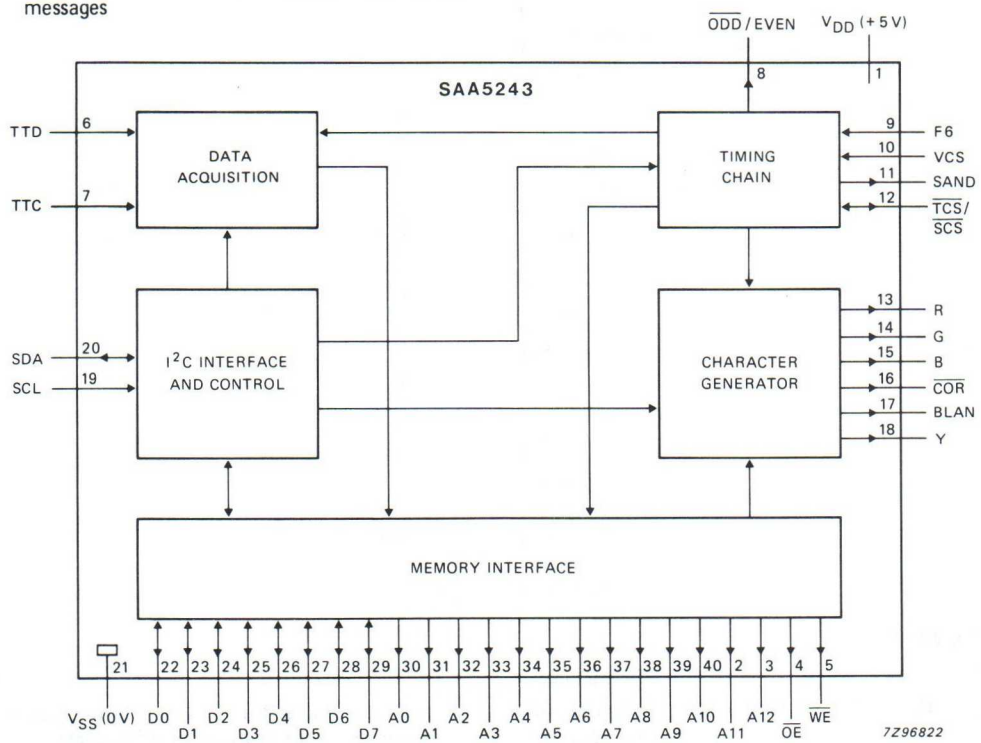


Fig.1 Block diagram.

PACKAGE OUTLINE 40-lead DIL; plastic (SOT129).

ORDERING INFORMATION

type number	version
SAA5243P/E/M2	West European languages
SAA5243P/H	East European languages
SAA5243P/K	Arabic and English languages
SAA5243P/L	Arabic and Hebrew languages
SAA5243P/T	West European and Turkish languages

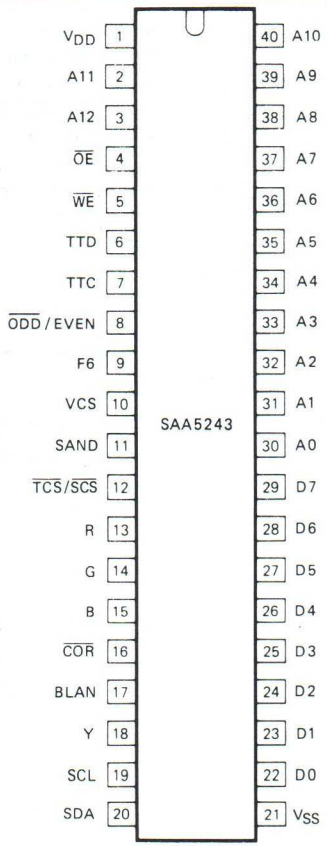


Fig.2 Pinning diagram.

PINNING

1	V_{DD}	**Power supply**: + 5 V power supply pin.
2, 3, 40	A11, A12, A10	**Chapter Address**: three outputs that select which 1 K byte chapter of external RAM is being accessed for any read or write cycle.
4	$\overline{OE}$	**Output Enable**: active low output signal used to control the reading of the external RAM. It occurs continuously at a 1 MHz rate.

5	$\overline{WE}$	**Write Enable**: active low output signal used to control the writing of data to the external RAM. It occurs for a valid write cycle only and is interleaved with the read cycles.
6	TTD	**Teletext Data**: input from the SAA5231 Video Input Processor (VIP2). It is clamped to V_{SS} for 4 to 8 μs of each television line to maintain the correct DC level following the external AC coupling.
7	TTC	**Teletext Clock**: 6.9375 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
8	$\overline{ODD}$/EVEN	**$\overline{Odd}$/Even**: for interlaced mode, the output changes once per field at 2 μs before the end of line 311 (624). The output is high for even fields and low for odd fields.
9	F6	**Character display clock**: 6 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
10	VCS	**Video Composite Sync**: input from the SAA5231 derived from the incoming video signal. Sync pulses are active high.
11	SAND	**Sandcastle**: 3-level sandcastle output to the SAA5231 containing the phase locking and colour burst blanking information.
12	$\overline{TCS}/\overline{SCS}$	**Text Composite Sync/Scan Composite Sync**: as an output an active low composite sync waveform (TCS) with interlaced or non-interlaced format (see Fig.6) which is fed to the SAA5231 to drive the display timebases. Alternatively this pin can act as an input for an active low composite sync waveform (SCS) to 'slave' the display timing circuits.
13, 14, 15	R, G, B	**Red, Green, Blue**: these 3 open drain outputs are the character video signals to the television display circuits. They are active high and contain character and background information.
16	$\overline{COR}$	**Contrast Reduction**: open drain, active low output which allows selective contrast reduction of the television picture to enhance a mixed mode display.
17	BLAN	**Blanking**: open drain, active high output which controls the blanking of the television picture for a normal text display and for a mixed display.
18	Y	**Character foreground**: open drain, active high video output signal containing all the foreground information displayed on the television screen (e.g. for driving a display printer).
19	SCL	**Serial Clock**: input signal which is the I^2C-bus clock from the microcontroller.
20	SDA	**Serial Data**: is the I^2C-bus data line. It is an input/output function with an open drain output.
21	V_{SS}	**Ground**: 0 volts.
22-29	DO-D7	**8 RAM data lines**: 3-state input/output pins which carry the data bytes to and from the external RAM.
30-39	A0-A9	**RAM address**: 10 output signals that determine which byte location within a 1 K byte chapter of external RAM is accessed for any read or write cycle.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range	pin 1	V_{DD}	−0.3	7.5	V
Input voltage range					
VCS, SDA, SCL, D0-D7		V_I	−0.3	7.5	V
TTC, TTD, F6, $\overline{TCS}/\overline{SCS}$		V_I	−0.3	10.0	V
Output voltage range					
SAND, A0-A12, $\overline{OE}$, $\overline{WE}$, D0-D7, SDA, $\overline{ODD}$/EVEN, R, G, B, BLAN, $\overline{COR}$, Y		V_O	−0.3	7.5	V
$\overline{TCS}/\overline{SCS}$		V_O	−0.3	10.0	V
Storage temperature range		T_{stg}	−20	+125	°C
Operating ambient temperature range		T_{amb}	−20	+70	°C

CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 1)	V_{DD}	4.5	5.0	5.5	V
Supply current (pin 1)	I_{DD}	–	160	270	mA
INPUTS (note 1)					
TTD (note 2)					
External coupling capacitor	C_{ext}	–	–	50	nF
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2.0	–	7.0	V
Input data rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input data set-up time (note 4)	t_{DS}	40	–	–	ns
Input data hold time (note 4)	t_{DH}	40	–	–	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
TTC; F6 (note 5)					
DC input voltage range	V_I	−0.3	–	+ 10.0	V
AC input voltage (peak-to-peak value) F6	$V_{I(p-p)}$	1.0	–	7.0	V
AC input voltage (peak-to-peak value) TTC	$V_{I(p-p)}$	1.5	–	7.0	V
Input peaks relative to 50% duty cycle	$\pm V_P$	0.2	–	3.5	V
TTC clock frequency	f_{TTC}	–	6.9375	–	MHz
F6 clock frequency	f_{F6}	–	6.0	–	MHz
Clock rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
VCS					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SCL					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
SCL clock frequency	f_{SCL}	0	–	100	kHz
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
INPUT/OUTPUTS (note 6)					
$\overline{TCS}$ (output)/$\overline{SCS}$ (input)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.5	–	10.0	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 0 to 10 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH					
at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
at I_{OH} = 0.1 mA	V_{OH}	2.4	–	6.0	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SDA (note 7)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V with output off	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	0	–	0.5	V
Output fall time between 3.0 V and 1.0 V levels	t_f	–	–	200	ns
Load capacitance	C_L	–	–	400	pF

parameter	symbol	min.	typ.	max.	unit
INPUT/OUTPUTS (continued)					
D0-D7 (note 8)					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input leakage current at V_I = 0 V to 5.5 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
OUTPUTS (note 6)					
A0-A12; $\overline{OE}$; $\overline{WE}$ (note 8)					
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
$\overline{ODD}$/EVEN					
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SAND (note 9)					
Output voltage LOW at I_{OL} = 0.2 mA	V_{OL}	0	–	0.25	V
Output voltage INTERMEDIATE at I_{OL} = ± 10 μA	V_{OI}	1.1	–	3.1	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SAND (continued)					
Output voltage HIGH at I_{OH} = 0 to −10 μA	V_{OH}	4.0	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0.4 V and 0.9 V levels	t_{r1}	–	–	400	ns
Output rise time V_{OI} to V_{OH} between 3.3 V and 3.8 V levels	t_{r2}	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 3.8 V and 0.4 V levels	t_f	–	–	50	ns
Load capacitance	C_L	–	–	30	pF
R; G; B; $\overline{\text{COR}}$; BLAN; Y (note 10)					
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	0	–	0.4	V
Output voltage LOW at I_{OL} = 5 mA	V_{OL}	0	–	1.0	V
Pull-up voltage as seen at pin	V_{PU}	–	–	6.0	V
Output fall time with a load resistor of 1.2 kΩ to 6 V and measured between 5.5 V and 1.5 V	t_f	–	–	20	ns
Skew delay between outputs with a load resistor of 1.2 kΩ to 6 V and measured on the falling edges at 3.5 V	t_{SK}	–	–	20	ns
Load capacitance	C_L	–	–	25	pF
Output leakage current at V_{PU} = 0 to 6 V with output off	I_{LO}	–	–	10	μA
TIMING					
I²C-bus (note 11)					
Clock low period	t_{LOW}	4	–	–	μs
Clock high period	t_{HIGH}	4	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	170	–	–	ns
Stop set-up time from clock high	$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop	t_{BUF}	4	–	–	μs
Start hold time	$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock low-to-high transition	$t_{SU;STA}$	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
TIMING (continued)					
Memory interface (note 12)					
Cycle time	t_{CY}	–	500	–	ns
Address change to $\overline{OE}$ LOW	t_{OE}	60	–	–	ns
Address active time	t_{ADDR}	450	500	–	ns
$\overline{OE}$ pulse duration	t_{OEW}	320	–	–	ns
Access time from $\overline{OE}$ to data valid	t_{ACC}	–	–	200	ns
Data hold time from $\overline{OE}$ HIGH or address change	t_{DH}	0	–	–	ns
Address change to $\overline{WE}$ LOW	t_{WE}	40	–	–	ns
$\overline{WE}$ pulse duration	t_{WEW}	200	–	–	ns
Data set-up time to $\overline{WE}$ HIGH	t_{DS}	100	–	–	ns
Data hold time from $\overline{WE}$ HIGH	t_{DHWE}	20	–	–	ns
Write recovery time	t_{WR}	25	–	–	ns

Notes to the characteristics

1. All inputs are protected against static charge under normal handling.
2. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor (see Fig.3).
3. Rise and fall times between 10% and 90% levels.
4. Teletext input data set-up and hold times are with respect to a 50% duty cycle level of the rising edge of the teletext clock input (TTC). Data stable 1 $\geqslant$ 2.0 V; data stable 0 $\leqslant$ 0.8 V (see Fig.4).
5. The TTC and F6 inputs have internal clamping diodes and are AC coupled (see Fig.3).
6. All outputs and input/outputs are protected against static charge under normal handling and connection to V_{DD} and V_{SS}.
7. For details of I^2C-bus timing see Fig.8.
8. For details of RAM timing see Fig.9.
9. For details of synchronization timing see Fig.5.
10. For details of display output timing see Fig.7.
11. The I^2C-bus timings are referred to V_{IH} = 3 V and V_{IL} = 1.5 V. For waveforms see Fig.8.
12. The memory interface timings are referred to V_{IL} = 1.5 V. For waveforms see Fig.9.

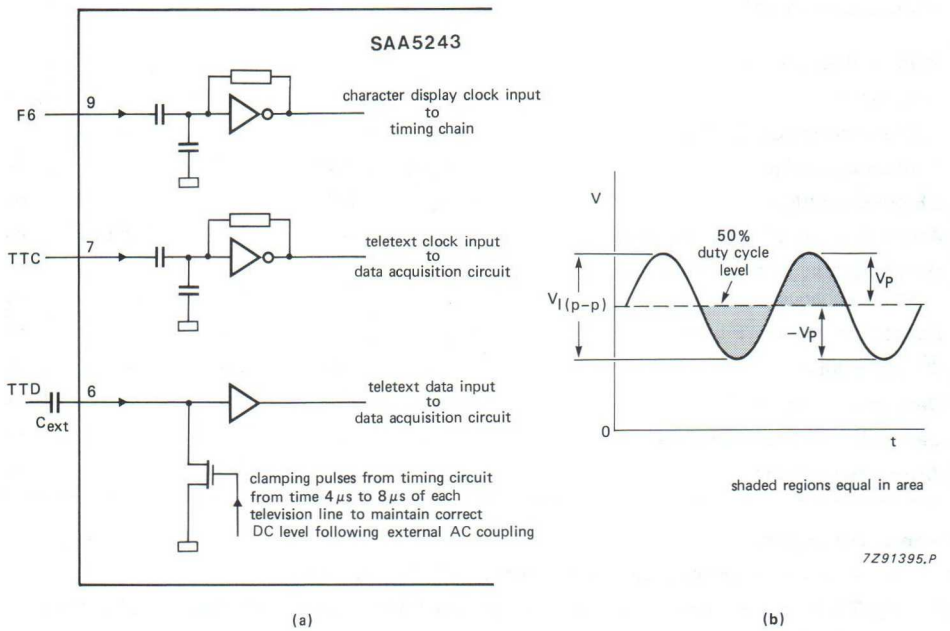
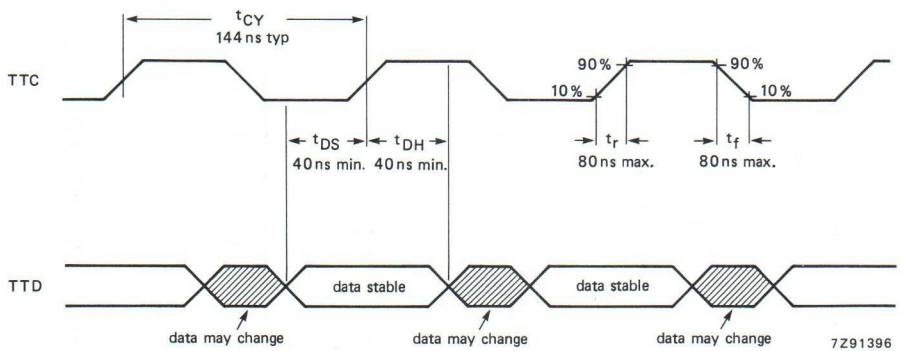


Fig.3 (a) F6, TTC and TTD input circuitry (b) input waveform parameters.



Data stable: 1 is $\geqslant$ 2.0 V; 0 is $\leqslant$ 0.8 V.

Fig.4 Teletext data input timing.

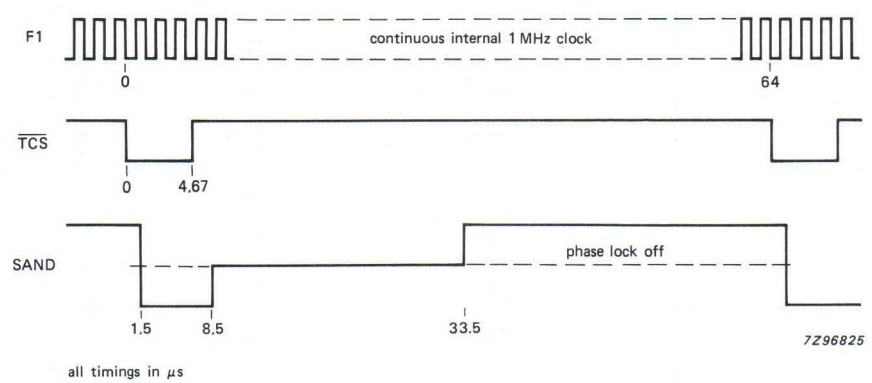
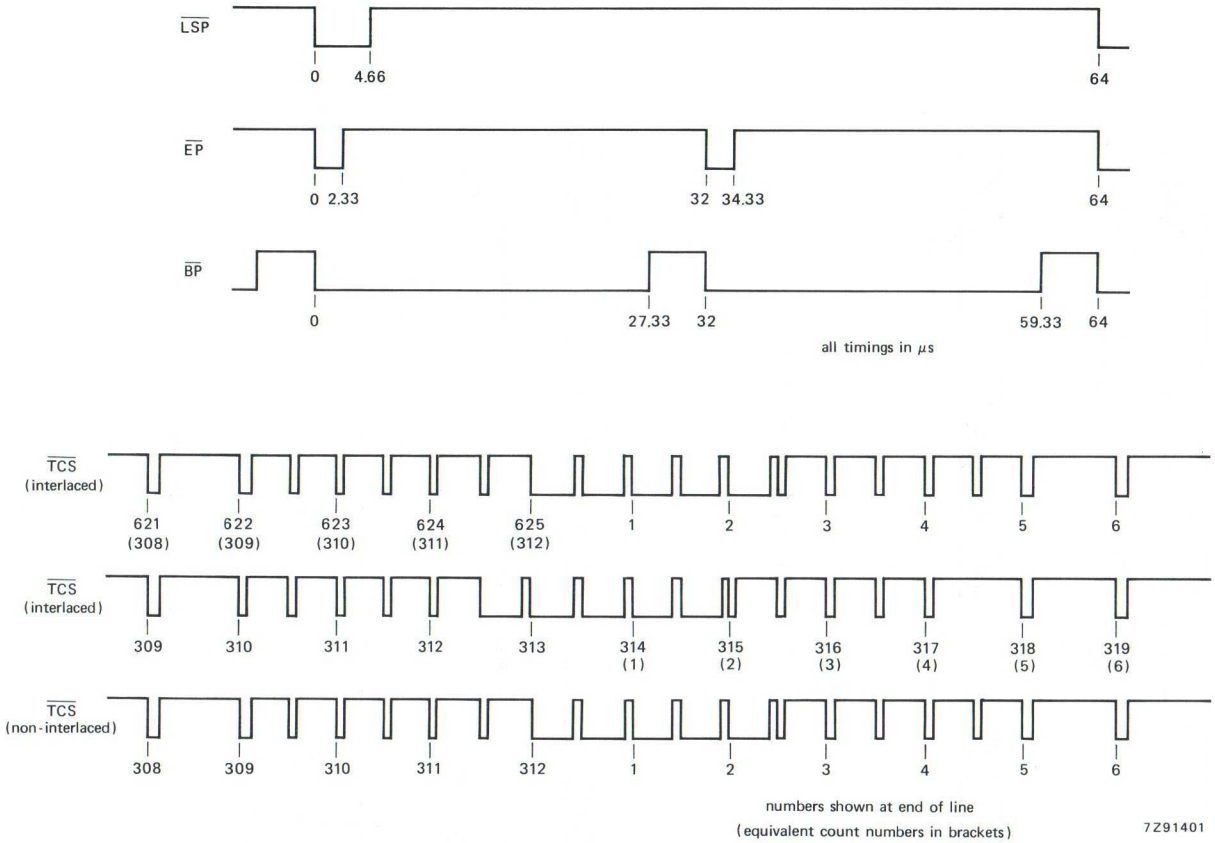


Fig.5 Synchronization timing.



Line sync pulses ($\overline{LSP}$), equalizing pulses ($\overline{EP}$) and broad pulses ($\overline{BP}$) are combined to provide the text composite sync waveform ($\overline{TCS}$) as shown. All timings measured from falling edge of $\overline{LSP}$ with a tolerance of ± 100 ns.

Fig.6 Composite sync waveforms.

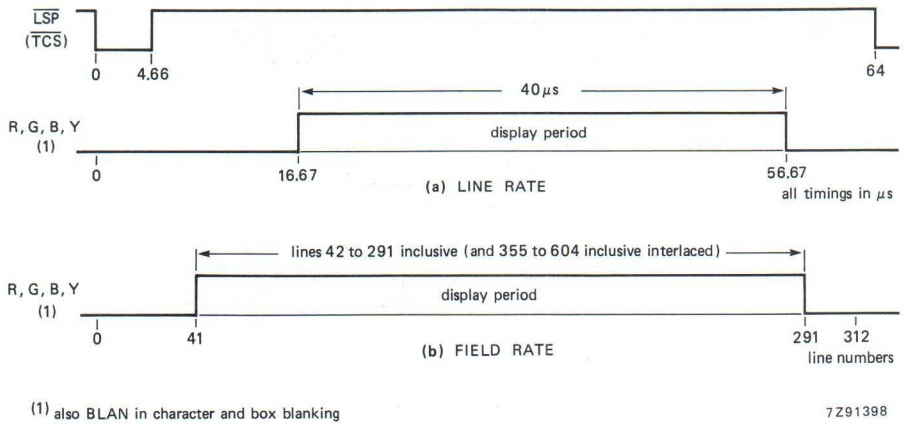


Fig.7 Display output timing (a) line rate (b) field rate.

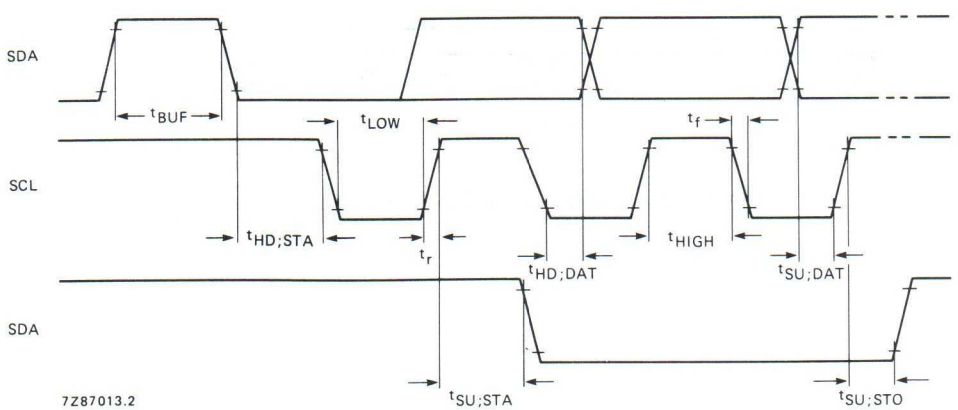


Fig.8 I^2C-bus timing.

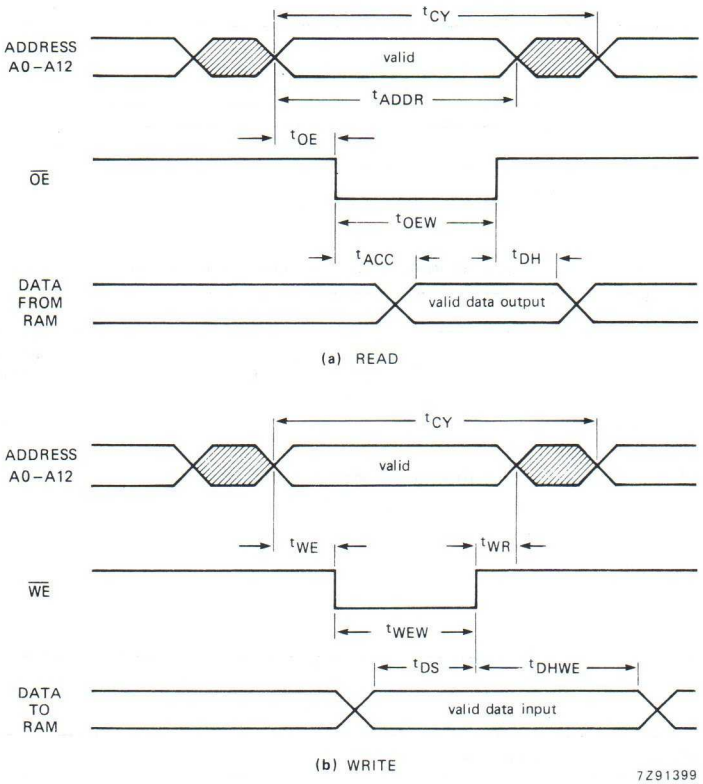
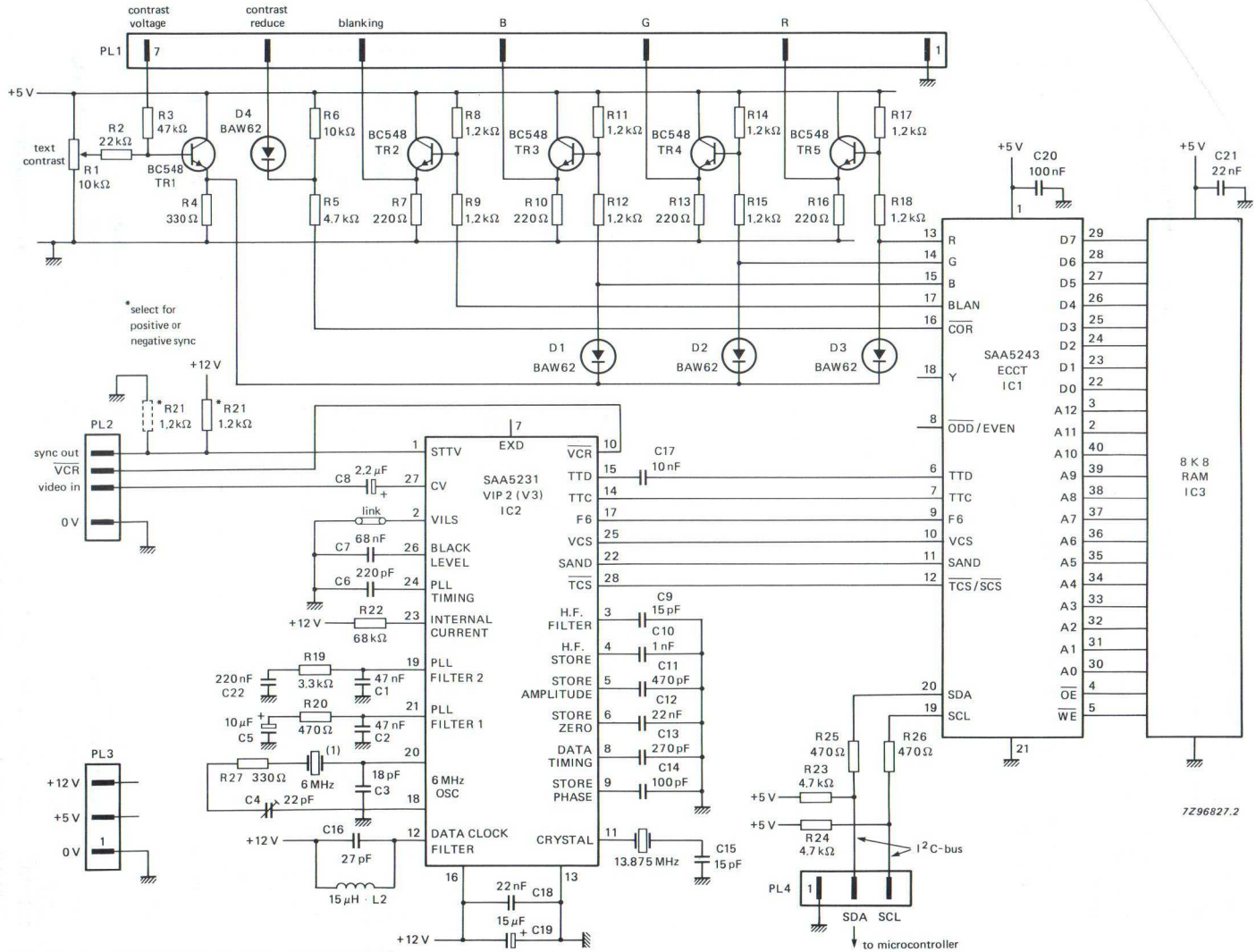


Fig.9 Memory interface timing (a) read (b) write.

APPLICATION INFORMATION



(1) Ceramic resonator e.g. Kyocera KBR 6.0 M.

Fig. 10 ECCT based multi[illegible]ge decoder circuit diagram.

APPLICATION INFORMATION (continued)

ECCT page memory organization

The organization of a page memory is shown in Fig.11. The ECCT provides an additional row compared with first generation decoders bringing the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page as broadcast and row 24 is the extra row available for user-generated status messages.

A MORE DETAILED DESCRIPTION OF ECCT OPERATION AND APPLICATION IS AVAILABLE ON REQUEST.

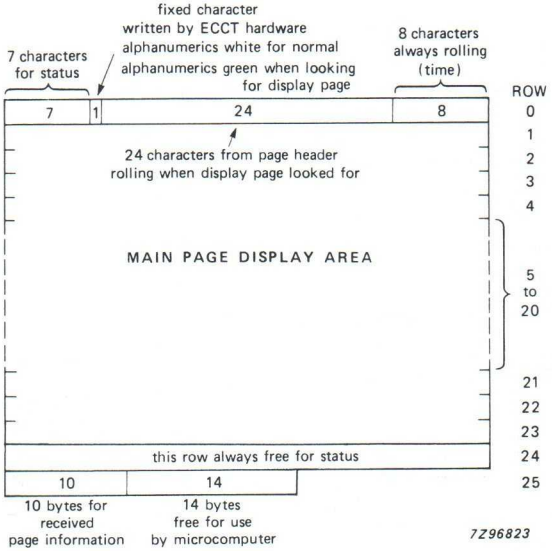


Fig.11 Page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

MAG	magazine	page number	MU	minutes units	page sub-code
PU	page units		MT	minutes tens	
PT	page tens		HU	hours units	
PBLF	page being looked for		HT	hours tens	
$\overline{\text{FOUND}}$	LOW for page has been found		C4-C14	transmitted control bits	
HAM.ER	Hamming error in corresponding byte				

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by ECCT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page. Seven digits are used to identify a page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

Register maps

ECCT mode registers R1 to R11 are shown in Table 2. R1 to R10 are WRITE only; R11 is READ/WRITE.
Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 ECCT register map

D7	D6	D5	D4	D3	D2	D1	D0		
TA	$\overline{7+P}$/ 8 BIT	ACQ. $\overline{ON}$/OFF	EXTENSION PACKET ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0	R1	Mode
—	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request address
—	—	—	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
—	—	—	—	—	A2	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash/subtitle)
STATUS ROW $\overline{BTM}$/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
—	—	—	—	CLEAR MEM.	A2	A1	A0	R8	Active chapter
—	—	—	R4	R3	R2	R1	R0	R9	Active row
—	—	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11	Active data

— bit does not exist

Notes to Table 2

The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^2C transmission byte. TA and TB must be logic 0 for normal operation.
All bits in registers R1 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to logic 1.
All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is enabled but all pages are on hold.

APPLICATION INFORMATION (continued)

Table 2 (continued)

Where:

R1 Mode

T0, T1	interlace/non-interlace 312/313 line control
TCS ON	text composite sync or direct sync select
$\overline{\text{DEW}}$/FULL FIELD	field-flyback or full channel mode
$\overline{7+P}$/8 BIT	7 bits with parity checking or 8-bit mode
TA, TB	test bits; 0 for normal operation
R2 Page request address	
START COLUMN	start column for page request data
ACQ CCT	selects one of four acquisition circuits
BANK SELECT	selects bank of four pages being addressed for acquisition
R3 Page request data	see Table 3
R4 Display chapter	determines which of the 8 pages is displayed
R5, R6 Display control	for normal and newsflash/subtitle
PON	picture on
TEXT	text on
COR	contrast reduction on
BKGND	background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 Display mode

BOX ON 0 (1-23, 24)	boxing function allowed on row 0 (row 1-23, 24)
STATUS ROW $\overline{\text{BTM}}$/TOP	row 25 displayed above or below the main text
R8 to R11	active chapter, row, column and data information written to or read from page memory via the I^2C-bus.

Table 3 Register map for page requests (R3)

Start Column	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

Abbreviations are as for Table 1 except for DO CARE bits.
When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
There are four groups of data shown in Table 3, one for each acquisition circuit (four simultaneous page requests).
Columns auto-increment on successive I^2C transmission bytes.

APPLICATION INFORMATION (continued)

CHARACTER SETS

Several versions of the ECCT are available, offering a variety of character sets. The full character sets are shown in Tables 4a to 4d.

The world system teletext specification allows the selection of national character sets via the page header transmission bits, C12 to C14. These bits are automatically decoded by the ECCT, the resulting character sets are shown in Tables 6a to 6d. For certain languages, control software processing of the extension packet data may be required for optimum useage of the range of available characters. See Fig. 12 for alphanumeric and graphic options.

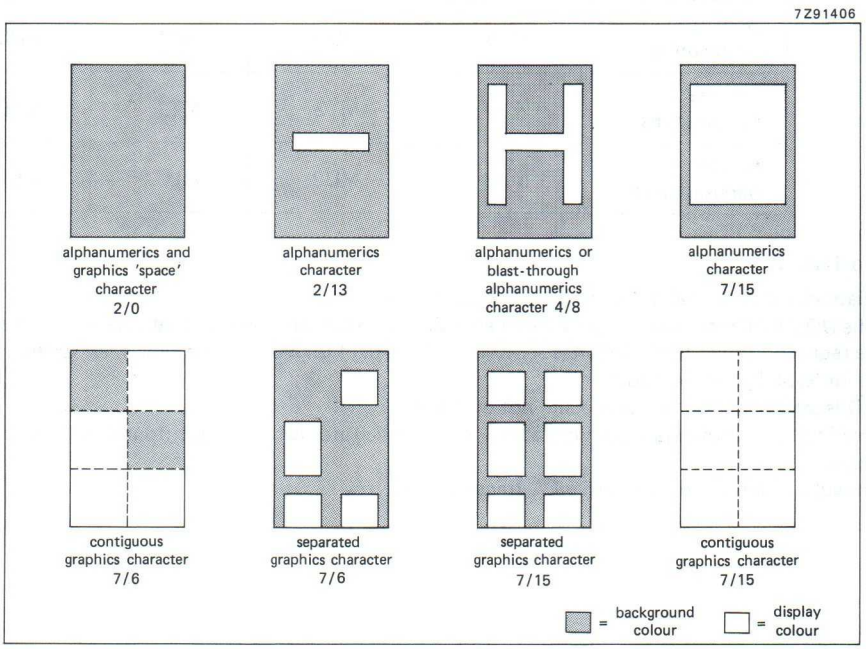


Fig.12 Alphanumeric and graphic options.

Table 4a Character data input decoding, West European languages (SAA5243P/E/M2)

BITS b_4 b_3 b_2 b_1 ↓	row \ column →	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
	b_8 →	0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
	b_7 →	0	0	0	0	0	0	1	1	1		1		0	0	0	0	1	1
	b_6 →	0	0	1	1	1	1	0	0	0		1		0	0	0	1	0	1
	b_5 →	0	1	0	1	1	1	0	1	0		1		0	1	0	1	1	1
0 0 0 0	0	alpha - numerics black	graphics black																
0 0 0 1	1	alpha - numerics red	graphics red																
0 0 1 0	2	alpha - numerics green	graphics green																
0 0 1 1	3	alpha - numerics yellow	graphics yellow																
0 1 0 0	4	alpha - numerics blue	graphics blue																
0 1 0 1	5	alpha - numerics magenta	graphics magenta																
0 1 1 0	6	alpha - numerics cyan	graphics cyan																
0 1 1 1	7	alpha - numerics white **	graphics white																
1 0 0 0	8	flash	conceal display																
1 0 0 1	9	steady **	contiguous graphics **																
1 0 1 0	10	end box **	separated graphics																
1 0 1 1	11	start box	ESC *																
1 1 0 0	12	normal height **	black back - ground **																
1 1 0 1	13	double height	new back - ground																
1 1 1 0	14	SO *	hold graphics																
1 1 1 1	15	SI *	release graphics **																

MBA429

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

APPLICATION INFORMATION (continued)

Table 4b Character data input decoding, East European languages (SAA5243P/H)

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7	0	0	0	0	0	1	1	1	1		1		1	1	1	1	1	1
b_6	0	0	1	1	1	0	0	1	1		1		1	1	1	1	1	1
b_5	0	1	0	0	1	0	1	0	1		0		0	0	0	1	1	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha–numerics black	graphics black			0		P	p				§	É	č	ą	Č	ű
0 0 0 1	1	alpha–numerics red	graphics red	!		1		A	Q	a		q		°	é	é	ę	č	ď
0 0 1 0	2	alpha–numerics green	graphics green	"		2		B	R	b		r		ä	ä	á	ż	ć	Ď
0 0 1 1	3	alpha–numerics yellow	graphics yellow	#		3		C	S	c		s		Ő	Ű	Ę	Ą	Ź	Ť
0 1 0 0	4	alpha–numerics blue	graphics blue	¤		4		D	T	d		t		$	¤	ů	ń	½	Ľ
0 1 0 1	5	alpha–numerics magenta	graphics magenta	%		5		E	U	e		u		⟨	⟩	Á	Ô	ô	Í
0 1 1 0	6	alpha–numerics cyan	graphics cyan	&		6		F	V	f		v		Đ	đ	Ě	Ó	ő	Ľ
0 1 1 1	7	alpha–** numerics white	graphics white	'		7		G	W	g		w		?	↓	ť	Ů	Ú	Ň
1 0 0 0	8	flash	conceal display	(		8		H	X	h		x		ö	ö	ě	ś	ž	ň
1 0 0 1	9	** steady	** contiguous graphics	)		9		I	Y	i		y		ü	å	ú	ı	đ	Ň
1 0 1 0	10	** end box	separated graphics	*		:		J	Z	j		z		ß	ü	š	ź	š	ŕ
1 0 1 1	11	start box	* ESC	+		;		K	Ä	k		ä		Ä	Ä	ť	ž	Ć	Ŕ
1 1 0 0	12	** normal height	black ** back–ground	,		<		L	Ş	l		ş		Ö	Ö	ž	Ś	Ž	Ř
1 1 0 1	13	double height	new back–ground	−		=		M	Ă	m		ă		Ü	Ă	ý	Ł	Đ	Ŧ
1 1 1 0	14	* SO	hold graphics	.		>		N	Ţ	n		ţ		^	Ü	í	ć	Š	Ý
1 1 1 1	15	* SI	** release graphics	/		?		O	_	o				_		ř	ó	ë	Ë

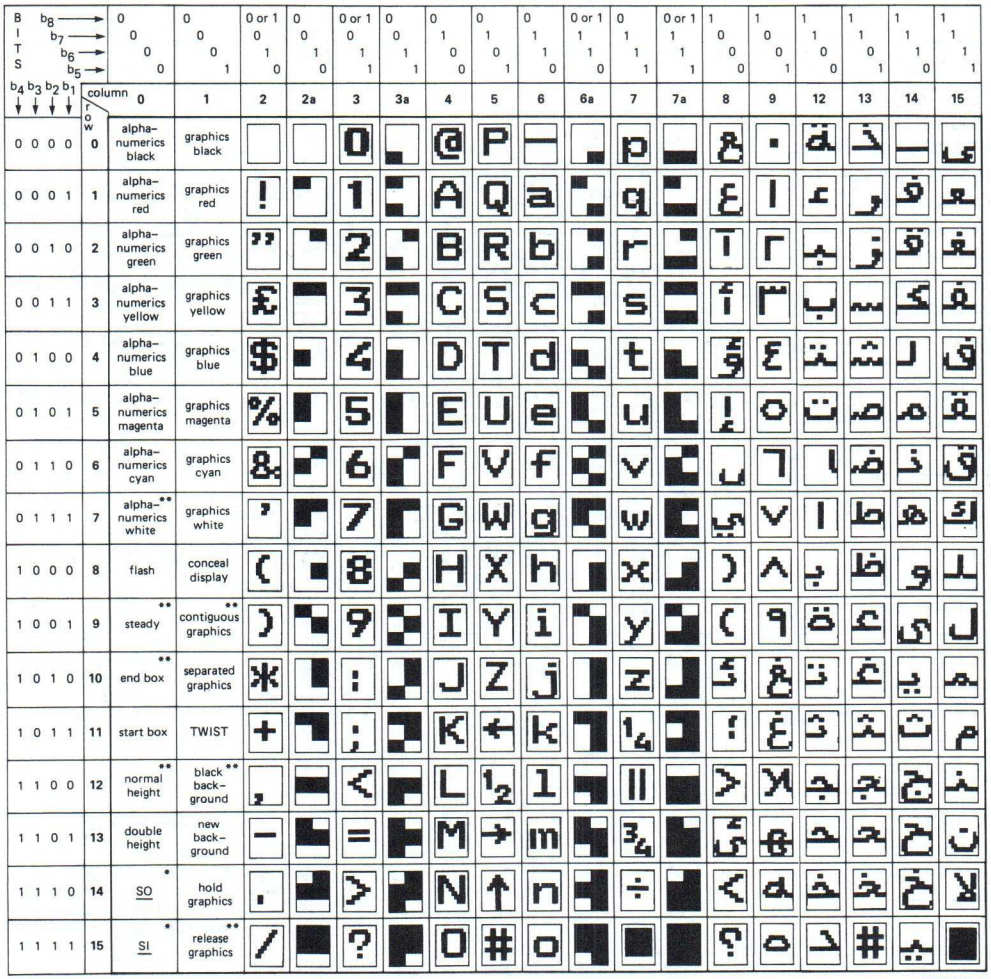
7Z22497.5

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 4c Character data input decoding, Arabic and English languages (SAA5243P/K)

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0	0 or 1	0	0 or 1	1	1	1	1	1	1
b_7	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	1	1
b_6	0	0	1	1	1	0	0	1	1	0	0	1	0	0	1	1	0	1
b_5	0	1	0	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓ row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha–numerics black	graphics black															
0 0 0 1	1	alpha–numerics red	graphics red															
0 0 1 0	2	alpha–numerics green	graphics green															
0 0 1 1	3	alpha–numerics yellow	graphics yellow															
0 1 0 0	4	alpha–numerics blue	graphics blue															
0 1 0 1	5	alpha–numerics magenta	graphics magenta															
0 1 1 0	6	alpha–numerics cyan	graphics cyan															
0 1 1 1	7	alpha–numerics white **	graphics white															
1 0 0 0	8	flash	conceal display															
1 0 0 1	9	steady **	contiguous graphics **															
1 0 1 0	10	end box **	separated graphics															
1 0 1 1	11	start box	TWIST															
1 1 0 0	12	normal height **	black ** background															
1 1 0 1	13	double height	new background															
1 1 1 0	14	SO *	hold graphics															
1 1 1 1	15	SI *	release graphics **															



7Z22660.4

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

APPLICATION INFORMATION (continued)

Table 4d Character data input decoding, Arabic and Hebrew languages (SAA5243P/L)

B I T S b_4 b_3 b_2 b_1 ↓	row	b_8	b_7	b_6	b_5	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	0	0	0	0	alpha-numerics black	graphics black			0		@	P	N		]			•			—	
0 0 0 1	1	0	0	0	1	alpha-numerics red	graphics red	!		1		A	Q										
0 0 1 0	2	0	0	1	0	alpha-numerics green	graphics green	"		2		B	R										
0 0 1 1	3	0	0	1	1	alpha-numerics yellow	graphics yellow	£		3		C	S										
0 1 0 0	4	0	1	0	0	alpha-numerics blue	graphics blue	$		4		D	T										
0 1 0 1	5	0	1	0	1	alpha-numerics magenta	graphics magenta	%		5		E	U										
0 1 1 0	6	0	1	1	0	alpha-numerics cyan	graphics cyan	&		6		F	V										
0 1 1 1	7	0	1	1	1	alpha-numerics white**	graphics white	'		7		G	W										
1 0 0 0	8	1	0	0	0	flash	conceal display	(		8		H	X										
1 0 0 1	9	1	0	0	1	steady**	contiguous graphics**	)		9		I	Y										
1 0 1 0	10	1	0	1	0	end box**	separated graphics	*		:		J	Z										
1 0 1 1	11	1	0	1	1	start box	TWIST	+		;		K	←										
1 1 0 0	12	1	1	0	0	normal height**	black background**	,		<		L	½										
1 1 0 1	13	1	1	0	1	double height	new background	−		=		M	→										
1 1 1 0	14	1	1	1	0	SO*	hold graphics	.		>		N	↑			÷							
1 1 1 1	15	1	1	1	1	SI*	release graphics**	/		?		O	#										

7Z22679.4

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 4e Character data input decoding, West European and Turkish languages (SAA5243P/T)

BITS b_8				0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7				0	0	0	0	0	1	1	1	1		1		1	1	1	1	1	1
b_6				0	0	1	1	1	0	0	1	1		1		0	0	0	0	1	1
b_5				0	1	0	1	1	0	1	0	1		0		0	1	0	1	0	1
b_4	b_3	b_2	b_1	row / column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0	0	0	0	0	alpha - numerics black	graphics black			0		§	P	°		p		@	I	é	à	i	Á
0	0	0	1	1	alpha - numerics red	graphics red	!		1		A	Q	a		q		—	ı	ù	è	¿	À
0	0	1	0	2	alpha - numerics green	graphics green	"		2		B	R	b		r		¼	ş	à	â	ü	È
0	0	1	1	3	alpha - numerics yellow	graphics yellow	#		3		C	S	c		s		£	Ł	£	é	ç	ł
0	1	0	0	4	alpha - numerics blue	graphics blue	$		4		D	T	d		t		$	ğ	$	ï	$	Ï
0	1	0	1	5	alpha - numerics magenta	graphics magenta	%		5		E	U	e		u		←	↓	ä	Ä	¤	Ó
0	1	1	0	6	alpha - numerics cyan	graphics cyan	&		6		F	V	f		v		→	↑	ö	Ö	¤	Ò
0	1	1	1	7	alpha - numerics white **	graphics white	'		7		G	W	g		w		?	?	·	Ç	Ñ	Ú
1	0	0	0	8	flash	conceal display	(		8		H	X	h		x		‖	ö	ò	ô	ñ	æ
1	0	0	1	9	steady **	contiguous graphics **	)		9		I	Y	i		y		¾	ç	è	û	è	Æ
1	0	1	0	10	end box **	separated graphics	*		:		J	Z	j		z		÷	ü	ì	ç	à	ð
1	0	1	1	11	start box	ESC *	+		;		K	Ä	k		ä		←	ş	°	ë	á	Đ
1	1	0	0	12	normal height **	black back - ground **	,		<		L	Ö	l		ö		½	Ö	ç	ê	é	ø
1	1	0	1	13	double height	new back - ground	-		=		M	Ü	m		ü		→	Ç	→	ù	í	Ô
1	1	1	0	14	SO *	hold graphics	.		>		N	^	n		ß		↑	Ü	↑	î	ó	Ã
1	1	1	1	15	SI *	release graphics **	/		?		O	_	o		■		#	Ğ	#	#	ú	ł

MBA428

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

APPLICATION INFORMATION (continued)

Table 4f Character data input decoding, Baltic and Cyrillic Russian (SAA5243P/R)

BITS b_8				0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7				0	0	0	0	0	1	1	1	1		1		0	0	1	1	1	1
b_6				0	0	1	1	1	1	0	0	1		1		0	0	0	0	1	1
b_5				0	1	0	1	1	1	0	1	0		1		0	1	0	1	0	1
b_4	b_3	b_2	b_1	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0	0	0	0	0	alpha - numerics black	graphics black															
0	0	0	1	1	alpha - numerics red	graphics red															
0	0	1	0	2	alpha - numerics green	graphics green															
0	0	1	1	3	alpha - numerics yellow	graphics yellow															
0	1	0	0	4	alpha - numerics blue	graphics blue															
0	1	0	1	5	alpha - numerics magenta	graphics magenta															
0	1	1	0	6	alpha - numerics cyan	graphics cyan															
0	1	1	1	7	alpha - numerics white **	graphics white															
1	0	0	0	8	flash	conceal display															
1	0	0	1	9	steady **	contiguous graphics **															
1	0	1	0	10	end box **	separated graphics															
1	0	1	1	11	start box	ESC *															
1	1	0	0	12	normal height **	black back - ground **															
1	1	0	1	13	double height	new back - ground															
1	1	1	0	14	SO *	hold graphics															
1	1	1	1	15	SI *	release graphics **															

MBA648

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

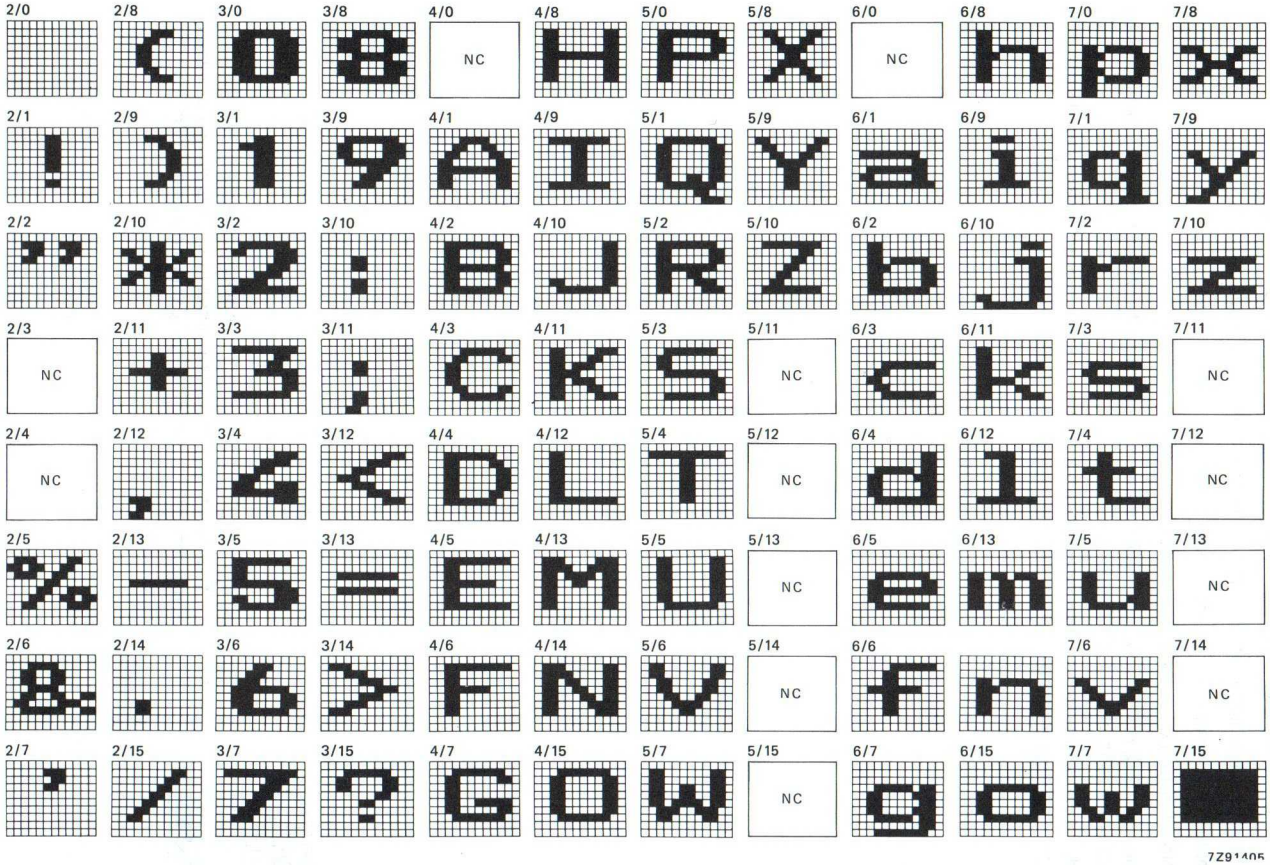
Notes to Table 4

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Codes may be referred to by column and row. For example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows: □
5. National option characters are shown in Table 6.
6. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters (for /E and /H character tables only) to combine with character 8/5.
7. With bit 8 = 0 national option character will be decoded according to the setting of control bits C12 to C14 (see Table 6).



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Table 5 SAA5243 basic character matrix



Where: NC national option character position.

APPLICATION INFORMATION (continued)

Table 6a SAA5243P/E/M2 national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

7Z22659.2

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 5.

Table 6b SAA5243P/H national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
POLISH	0	0	0	#	ń	ą	Ż	Ś	Ł	ć	ó	ę	ż	ś	ł	ź
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
SERBO-CROAT	1	0	1	#	½	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECHOSLOVAK	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN	1	1	1	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

7Z22658.1

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to German. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 5.

APPLICATION INFORMATION (continued)

Table 6c SAA5243P/K national option character set



LANGUAGE	ENGLISH	ARABIC
PHCB (1) (C12, C13, C14)	0 0 0	1 1 1

7Z22790

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English.

Table 6d SAA5243P/L national option character set



(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English.

APPLICATION INFORMATION (continued)

Table 6e SAA5243P/T national option character set

LANGUAGE	PHCB [1]			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
TURKISH	1	1	0	Ţ	ğ	İ	Ş	Ö	Ç	Ü	Ğ	ı	ş	ö	ç	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MBA430

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 5.

Table 6f SAA5243R/L national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)													
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ESTONIAN	0	1	0	#	Õ	Š	Ä	Ö	Ž	Ü	õ	š	ä	ö	ž	ü
LETTISH / LITHUANIAN	0	1	1	#	$	Š	ė	ę	Ž	Č	ū	š	ą	ų	ž	į
RUSSIAN	1	0	0		0	Ю	П	ю	п							
				!	1	А	Я	а	я							
				"	2	Б	Р	б	р							
				#	3	Ц	С	ц	с							
				$	4	Д	Т	д	т							
				%	5	Е	У	е	у							
				ы	6	Ф	Ж	ф	ж							
				'	7	Г	В	г	в							
				(	8	Х	Ь	х	ь							
				)	9	И	Ъ	и	ъ							
				ж	:	Й	З	й	з							
				+	;	К	Ш	к	ш							
				,	<	Л	Э	л	э							
				−	=	М	Щ	м	щ							
				.	>	Н	Ч	н	ч							
				/	?	О	Ы	о	■							

MBA647

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English.

Integrated VIP and teletext decoder (IVT1.1)

SAA5244A

FEATURES

- Complete teletext decoder including page memory in a single 40-pin DIL package
- Single +5 V power supply
- Digital data slicer and display clock phase-locked loop reduces peripheral components to a minimum
- Both video and scan related synchronization modes are supported
- On board single page memory including extension packets for FASTEXT
- Single page acquisition system
- RGB interface to standard colour decoder ICs, push-pull output drive
- Data capture performance similar to SAA5231 (VIP2)
- Simple software control via I²C-bus
- Option for five national languages
- 32 supplementary characters for on-screen displays
- Optional storage of packet 24 in the display memory
- Page links in packets 27 and 8/30 are Hamming decoded
- Separate text and video signal quality detectors, 625/525 video status and language version all readable via I²C-bus
- Automatic ODD/$\overline{\text{EVEN}}$ output control with manual override
- Control of display PLL free-run and rolling header via I²C-bus
- VCS to SCS mode for stable 525 line status display

DESCRIPTION

The Integrated VIP and Teletext (IVT1.1) is a teletext decoder (contained within a single-chip package) for decoding 625-line based World System Teletext transmissions. The teletext decoder hardware is based on a reduced function version of the device SAA5246 (IVT1.0).

The Video Input Processor (VIP) section of the device uses mixed analog and digital designs for the data slicer and the display clock phase-locked loop functions. As a result the number of external components is greatly reduced and no critical or adjustable components are required. A single page static RAM is incorporated in the device thereby giving a genuine single-chip teletext decoder device.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5244AP	40	DIL	plastic	SOT129
SAA5244AP	42	SDIL	plastic	SOT270
SAA5244AGP	44	QFP	plastic	SOT205A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5	5.5	V
I_{DD}	supply current	–	74	148	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature range	–20	–	70	°C

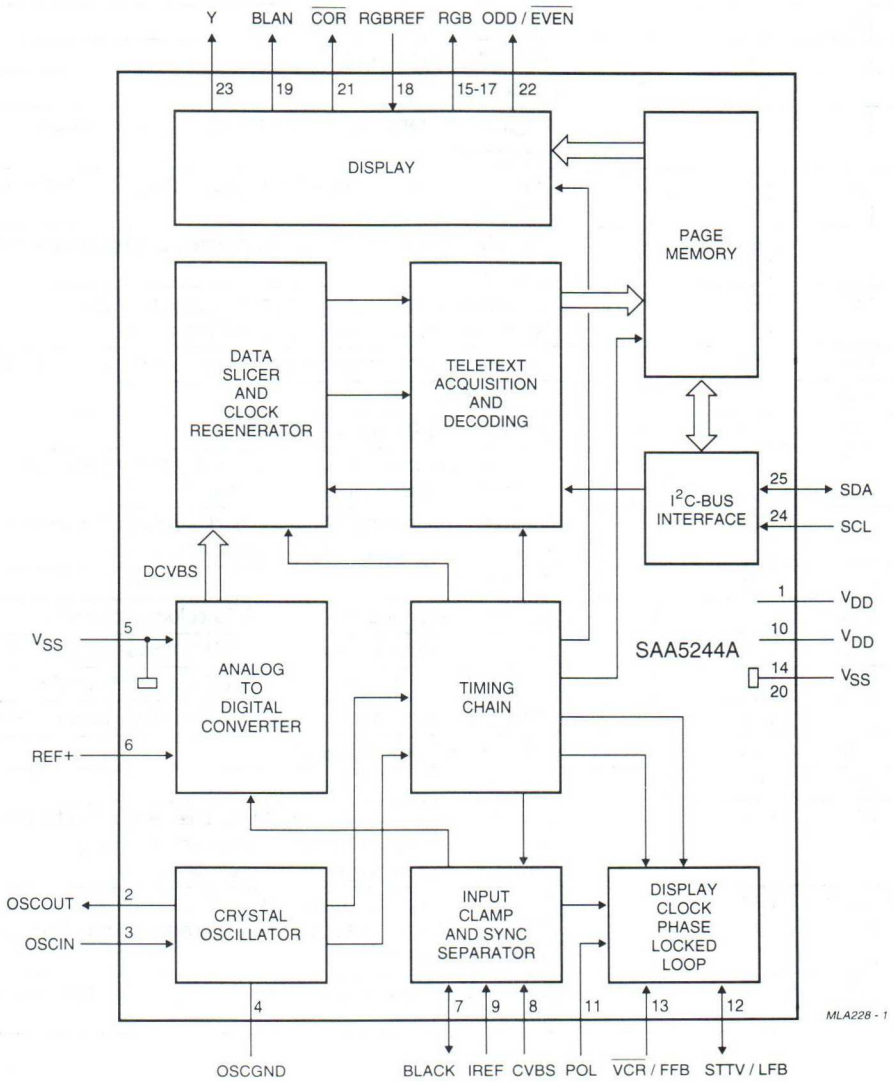


Fig.1 Block diagram for SOT129 (DIL40) package.

PINNING

SYMBOL	SOT129	SOT270	SOT205A	DESCRIPTION
V_{DD}	1	1	18	+5 V supply
OSCOUT	2	2	19	27 MHz crystal oscillator output
OSCIN	3	3	20	27 MHz crystal oscillator input
OSCGND	4	4	21	0 V crystal oscillator ground
V_{SS}	5	5	22	0 V ground
REF–	–	6	–	negative reference voltage for the ADC. The pin should be connected to 0 V
REF+	6	7	23	positive reference voltage for the ADC. The pin should be connected to +5 V
BLACK	7	8	24	video black level storage pin, connected to ground via a 100 nF capacitor
CVBS	8	9	25	composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor
IREF	9	10	26	reference current input pin, connected to ground via a 27 kΩ resistor
V_{DD}	10	11	27	+5 V supply
POL	11	12	28	STTV/LFB/FFB polarity selection pin
STTV/LFB	12	13	29	sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode)
$\overline{VCR}$/FFB	13	14	32	PLL time constant switch/field flyback input pin. Function controlled by an internal register bit (scan sync mode)
V_{SS}	14	15	33	0 V ground
R	15	16	34	dot rate character output of the RED colour information
G	16	17	35	dot rate character output of the GREEN colour information
B	17	18	36	dot rate character output of the BLUE colour information
RGBREF	18	19	37	input DC voltage to define the output high level on the RGB pins
BLAN	19	20	38	dot rate fast blanking output
V_{SS}	20	21	39	0 V ground
$\overline{COR}$	21	22	40	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages; open drain output
ODD/$\overline{EVEN}$	22	23	41	25 Hz output synchronized with the CVBS input's field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents
Y	23	24	42	dot rate character output of teletext foreground colour information; open drain output

SYMBOL	SOT129	SOT270	SOT205A	DESCRIPTION
SCL	24	25	43	serial clock input for the I²C-bus. It can still be driven during power-down of the device
SDA	25	26	44	serial data port for the I²C-bus; open drain output. It can still be driven during power-down of the device
n.c.	–	27, 31, 32	4 to 7 30, 31	not connected
i.c.	26 to 40	28 to 30 33 to 42	1 to 3 8 to 17	internally connected. Must be left open-circuit in application

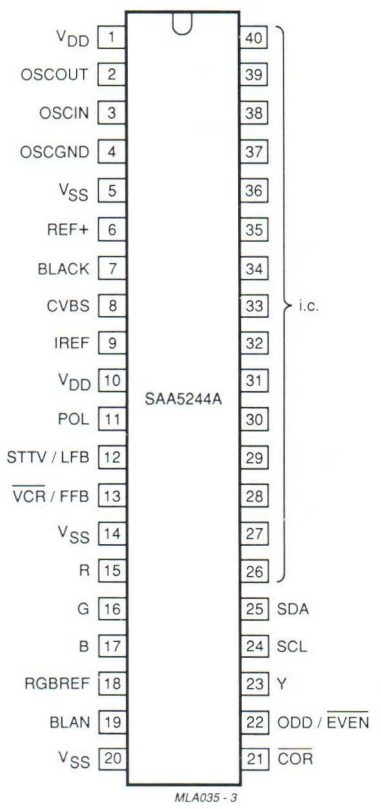


Fig.2 Pin configuration; SOT129 (DIL40).

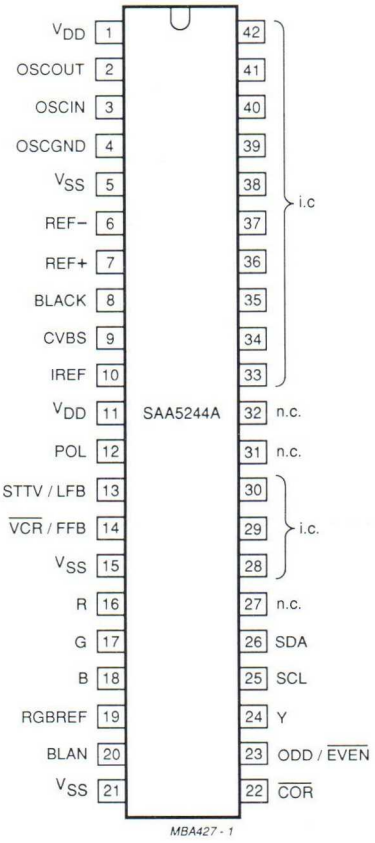


Fig.3 Pin configuration; SOT270 (SDIL42).

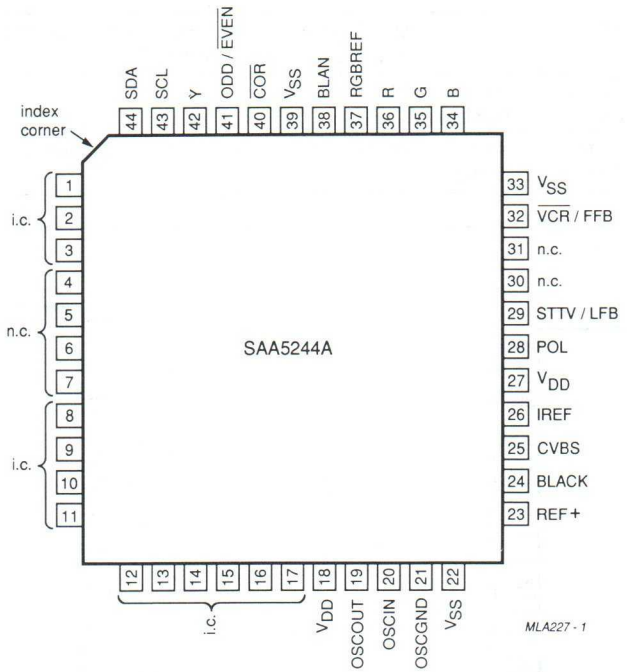


Fig.4 Pin configuration; SOT205A (QFPL44).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	−0.3	6.5	V
V_I	input voltage (any input)	−0.3	V_{DD}+0.5	V
V_O	output voltage (any output)	−0.3	V_{DD}+0.5	V
I_O	output current (each output)	−	±10	mA
I_{IOK}	DC input or output diode current	−	±20	mA
T_{amb}	operating ambient temperature range	−20	70	°C
T_{stg}	storage temperature range	−55	125	°C
V_{stat}	electrostatic handling human body model (note 1)	−2000	2000	V

Note

1. The human body model ESD simulation is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor; this produces a single discharge transient. Reference Philips Semiconductors test method UZW-B0/FQ-A302 (compatible with MIL-STD method 3015.7).

Failure Rate

The failure rate at T_{amb} = 55 °C will be a maximum of 1000 FITS (1 FIT = 1 x 10^{-9} failures per hour).

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −20 to +70 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range (V_{DD}-V_{SS})		4.5	5	5.5	V
I_{DD}	total supply current		–	74	148	mA
Inputs						
CVBS						
V_{syn}	sync amplitude		0.1	0.3	0.6	V
t_{syn}	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		−150	0	150	ns
t_{syd}	change in sync delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{vid(p-p)}$	video input amplitude (peak-to-peak)		0.7	1	1.4	V
	display PLL catching range		±7	–	–	%
Z_{src}	source impedance		–	–	250	Ω
C_I	input capacitance		–	–	10	pF
IREF						
R_g	resistor to ground		–	27	–	kΩ
POL						
V_{IL}	input voltage LOW		−0.3	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	μA
C_I	input capacitance		–	–	10	pF
LFB						
V_{IL}	input voltage LOW		−0.3	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	μA
I_I	input current	note 1	−1	–	1	mA
t_{LFB}	delay between LFB front edge and input video line sync		–	250	–	ns
$\overline{VCR}$/FFB						
V_{IL}	input voltage LOW		−0.3	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	μA
I_I	input current	note 1	−1	–	1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
RGBREF (NOTE 2)						
V_I	input voltage		−0.3	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
I_{DC}	DC current		–	–	10	mA
SCL						
V_{IL}	input voltage LOW		−0.3	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
f_{SCL}	clock frequency		0	–	100	kHz
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
C_I	input capacitance		–	–	10	pF
Inputs/outputs						
CRYSTAL OSCILLATOR (OSCIN; OSCOUT)						
f_{XTAL}	crystal frequency		–	27	–	MHz
G_v	small signal voltage gain		3.5	–	–	–
G_m	mutual conductance	f = 100 kHz	1.5	–	–	mA/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	–	5	pF
BLACK						
C_{blk}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
SDA						
V_{IL}	input voltage LOW		−0.3	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
V_{OL}	output voltage LOW	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	3 to 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
STTV						
G_{stt}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{tcs}	TCS amplitude		0.2	0.3	0.45	V
V_{DCs}	DC shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive current		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
R, G AND B						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	output voltage HIGH	I_{OH} = –1.6 mA; RGBREF ≤ V_{DD}–2 V	RGBREF –0.25 V	RGBREF	RGBREF +0.25 V	V
$\|Z_o\|$	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
I_{DC}	DC current		–	–	–3.3	mA
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
BLAN						
V_{OL}	output voltage LOW	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = –0.2 mA; V_{DD} = 4.5 V	1.1	–	–	V
V_{OH}	output voltage HIGH	I_{OH} = 0 mA; V_{DD} = 5.5 V	–	–	2.8	V
V_{OH}	allowed voltage at pin	with external pull-up	–	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
ODD/$\overline{\text{EVEN}}$						
V_{OL}	output voltage LOW	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = –1.6 mA	V_{DD}–0.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
$\overline{COR}$ AND Y (OPEN DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V
V_{OL}	output voltage LOW	I_{OL} = 5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} −0.5 and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_I = 0 to V_{DD}	−10	–	10	μA
T_{SK}	skew delay between display outputs R, G, B, $\overline{COR}$, Y and BLAN		–	–	20	ns
Timing						
I²C-BUS						
t_{LOW}	clock LOW period		4	–	–	μs
t_{HIGH}	clock HIGH period		4	–	–	μs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	μs
t_{BUF}	START set-up time following a STOP		4	–	–	μs
$t_{HD;STA}$	START hold time		4	–	–	μs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	μs

Notes to the characteristics

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ± 1 mA.
2. RGBREF is the positive supply for the RGB output pins and it must be able to source the I_{OH} current from the R, G and B pins. The leakage specification on RGBREF only applies when there is no current load on the RGB pins.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

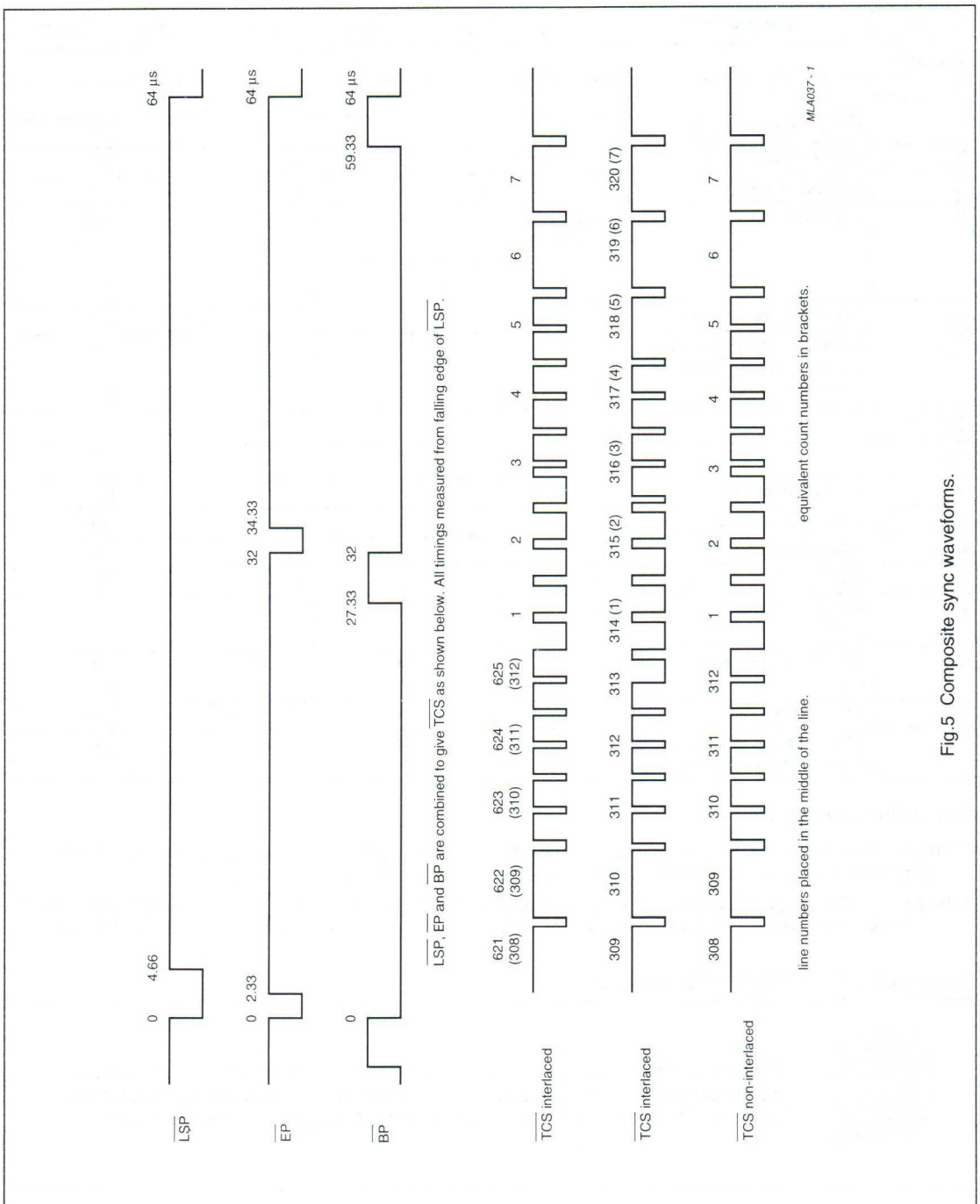


Fig.5 Composite sync waveforms.

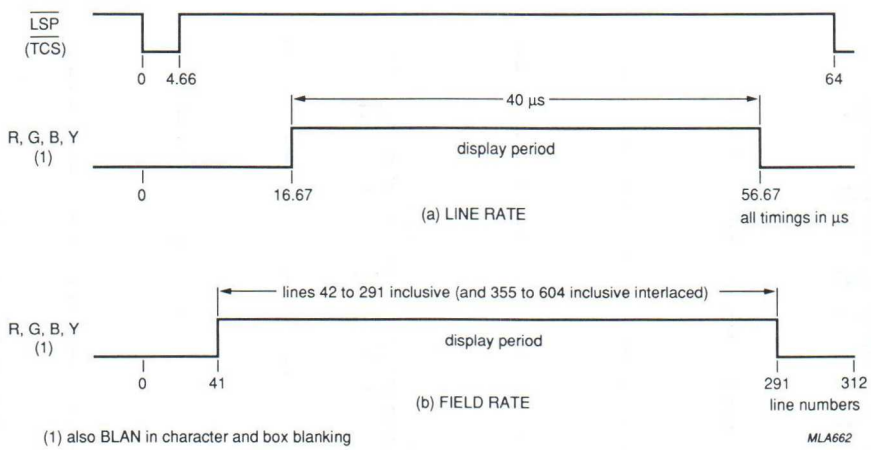


Fig.6 Display output timing (a) line rate (b) field rate.

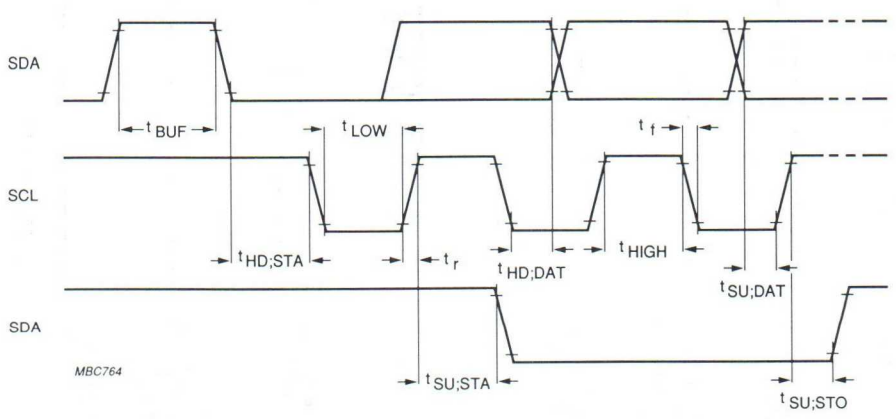


Fig.7 I²C-bus timing.

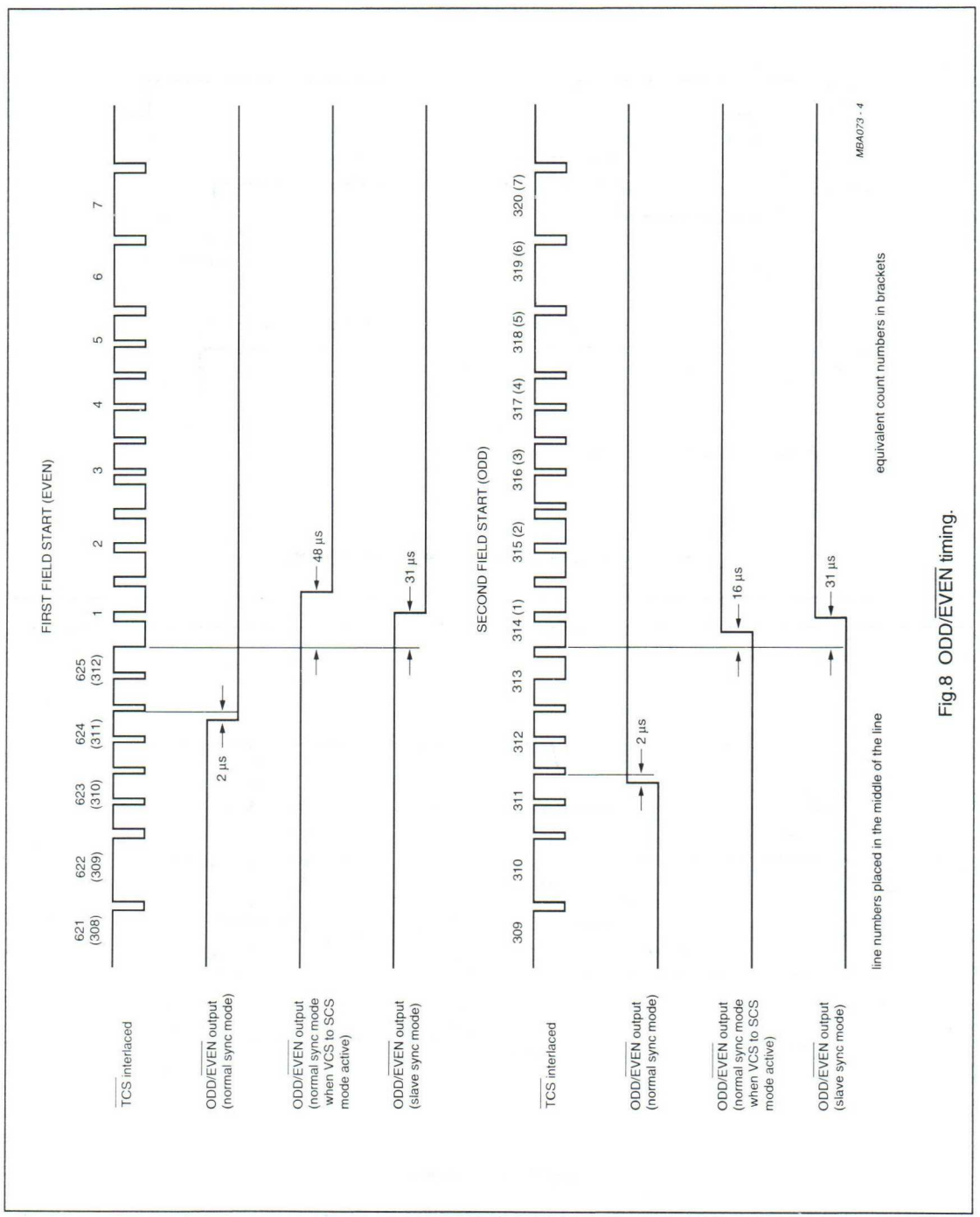
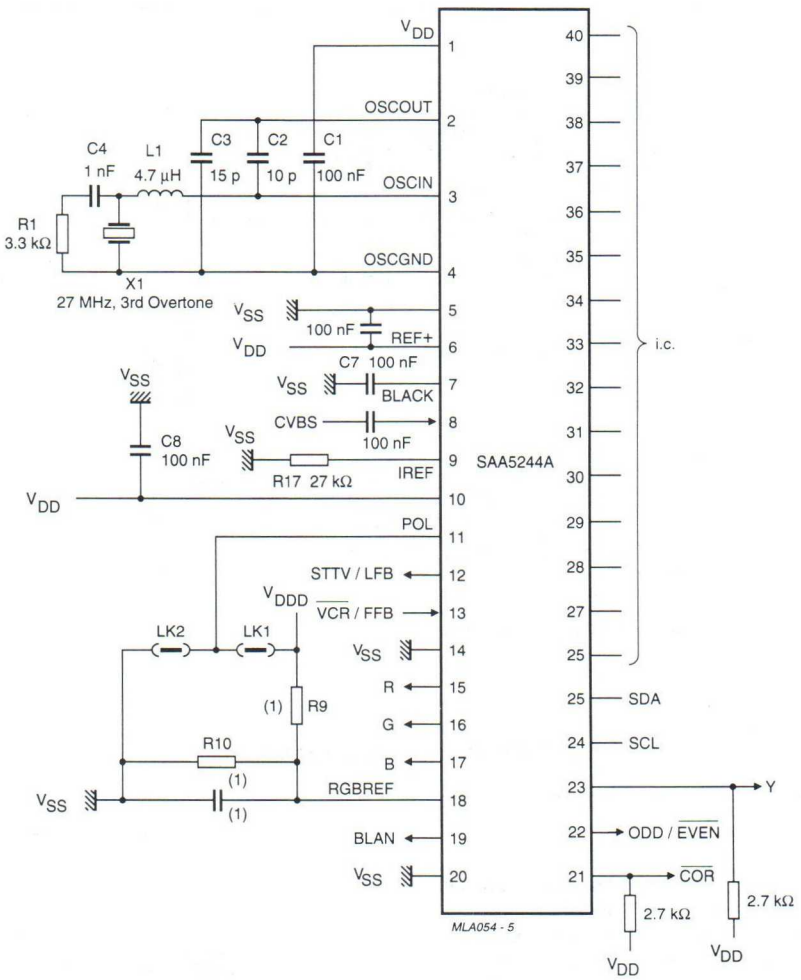


Fig.8 ODD/$\overline{\text{EVEN}}$ timing.

APPLICATION INFORMATION



(1) Value dependent on application.

Fig.9 Application diagram.

SAA5244A page memory organization

The organization of the page memory is shown in Fig.10. The device provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; row 24 is available for software generated status messages and FLOF/FASTEXT prompt information.

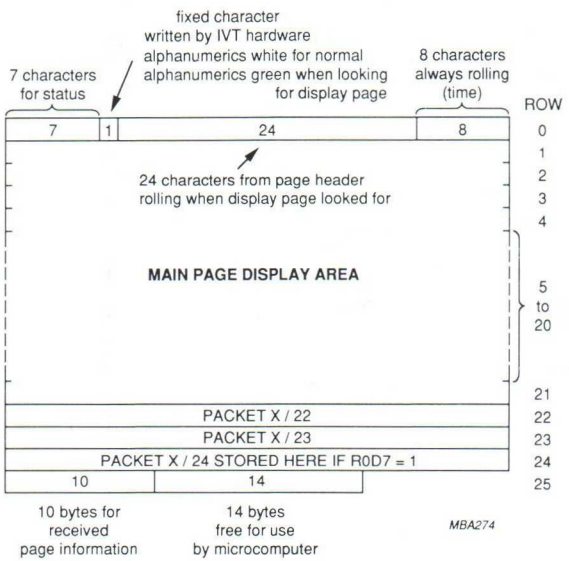


Fig.10 Basic page memory organization.

Row 0:

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by SAA5244A to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25:

The first 10 bytes of row 25 contain control data relating to the received page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

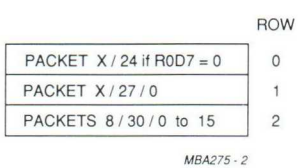


Fig.11 Organization of the extension memory.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

Page number

MAG magazine
PU page units
PT page tens

PBLF page being looked for
$\overline{\text{FOUND}}$ LOW for page has been found
HAM.ER Hamming error in corresponding byte

Page sub-code

MU minutes units
MT minutes tens
HU hours units
HT hours tens

C4-C14 transmitted control bits.

Register maps

SAA5244A mode registers R0 to R11 are shown in Table 2. R0 to R10 are WRITE only; R11 is READ/WRITE. Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 Register map

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Adv. control	0	X24 POS	FREE RUN PLL	AUTO ODD/$\overline{\text{EVEN}}$	DISABLE HDR ROLL	–	DISABLE ODD/$\overline{\text{EVEN}}$	–	$\overline{\text{R11}}$/R11B SELECT
Mode	1	VCS TO SCS	–	ACQ $\overline{\text{ON}}$/OFF	–	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0
Page request address	2	–	–	–	–	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
		–	–	–	–	–	–	–	–
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS TOP	CURSOR ON	REVEAL ON	BOTTOM HALF	DOUBLE HEIGHT	BOX 24	BOX 1-23	BOX 0
		–	–	–	–	–	–	–	–
Cursor row	9	SUPPL. BLAST	CLEAR MEM.	A0	R4	R3	R2	R1	R0
Cursor column	10	SUPPL. ROW 24	SUPPL. ROW 0	C5	C4	C3	C2	C1	C0
Cursor data	11	–	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{\text{625}}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TEXT SIGNAL QUALITY	VCS SIGNAL QUALITY

Notes to Table 2

1. – indicates these bits are inactive and must be written to logic 0 for future compatibility.
2. All bits in registers R0 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R1, R5 and R6 which are set to logic 1.
3. All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha' white (00000111) as the acquisition circuit is enabled but the page is on hold.
4. TB must be set to logic 0 for normal operation.
5. The I²C slave address is 0010001

Register description

R0 ADVANCED CONTROL - auto increments to Register 1

$\overline{R11}$/R11B SELECT	Selects reading of R11 or R11B
DISABLE ODD/$\overline{EVEN}$	Forces ODD/$\overline{EVEN}$ output LOW when logic 1
DISABLE HDR ROLL	Disables green rolling header and time
AUTO ODD/$\overline{EVEN}$	When set forces ODD/$\overline{EVEN}$ low if any TV picture displayed, if DISABLE ODD/$\overline{EVEN}$ = 0
FREE RUN PLL	Will force the PLL to free run in all conditions
X24 POS	Automatic display of FASTEXT prompt row when logic 1

R1 MODE - auto increments to Register 2

T0, T1	Interlace/non-interlace 312/313 line control (see Table 4)
TCS ON	Text composite sync or direct sync select
$\overline{DEW}$/FULL FIELD	Field-flyback or full channel mode
ACQ $\overline{ON}$/OFF	Aquisition circuits turned off when logic 1
VCS TO SCS	When logic 1 enables display of messages with 60 Hz input signal

R2 PAGE REQUEST ADDRESS - auto increments to Register 3

COL SC0 - SC2	Point to start column for page request data (see Table 3)
TB	Must be logic 0 for normal operation

R3 PAGE REQUEST DATA - does not auto increment (see Table 3)

R5 NORMAL DISPLAY CONTROL - auto increments to Register 6

R6 NEWSFLASH/SUBTITLE DISPLAY CONTROL - auto increments to Register 7

PON	Picture on
TEXT	Text on
COR	Contrast reduction on
BKGND	Background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 DISPLAY MODE - does not auto increment

BOX ON 0	Boxing function allowed on Row 0
BOX ON 1-23	Boxing function allowed on Row 1-23
BOX ON 24	Boxing function allowed on Row 24
DOUBLE HEIGHT	To display double height text
BOTTOM HALF	To select bottom half of page when DOUBLE HEIGHT = 1
REVEAL ON	To reveal concealed text
CURSOR ON	To display cursor
STATUS TOP	Row 25 displayed above or below the main text

R9 CURSOR ROW - auto increments to Register 10

R0 to R4	Active row for data written to or read from memory via the I²C-bus
A0	Selects display memory page (when = 0) or extension packet memory (when = 1)
CLEAR MEM.	When set to 1, clears the display memory. This bit is automatically reset
SUPPL. BLAST	When set to 1, column 4b and 5b (of Table 6) are mapped into 4 and 5 respectively, replacing blast-through alphanumerics in graphics mode

R10 CURSOR COLUMN - auto increments to Register 11 or 11B

C0 to C5	Active column for data written to or read from memory via the I²C-bus
SUPPL. ROW 0	When set to 1, column 4b and 5b (of Table 6) are mapped into columns 6 and 7 respectively, just for row 0 columns 0 to 7
SUPPL. ROW 24	When set to 1, column 4b and 5b (of Table 6) are mapped into columns 6 and 7 respectively just for row 24

R11 CURSOR DATA - does not auto increment

D0 to D6	Data read from/written to memory via I²C, at location pointed to by R9 and R10. This location automatically increments each time R11 is accessed

R11B DEVICE STATUS - does not auto increment

VCS SIGNAL QUALITY	Indicates that the video signal quality is good and PLL is phase locked to input video when = 1
TEXT SIGNAL QUALITY	If a good teletext signal is being received when = 1
ROM VER R0 to R4	Indicated language/ROM variant. For Western European = 01000
$\overline{625}$/525 SYNC	If the input video is a 525 line signal when = 1

Table 3 Register map for page requests (R3)

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

1. Abbreviations are as for Table 1 except for DO CARE bits.
2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
3. If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
4. Columns auto-increment on successive I²C-bus transmission bytes.

Table 4 Interlace/non-interlace 312/313 line control (T0 and T1)

T1	T0	RESULT
0	0	interlaced 312.5/312.5 lines
0	1	non-interlaced 312/313 lines (note 1)
1	0	non-interlaced 312/312 lines (note 1)
1	1	scan-locked

Note to Table 4

1 Reverts to interlaced mode if a newsflash or subtitle is being displayed.

Table 5 Crystal characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)					
C1	series capacitance	–	1.7	–	pF
C0	parallel capacitance	–	5.2	–	pF
C_L	load capacitance	–	20	–	pF
Rr	resonant resistance	–	–	50	Ω
R1	series resistance	–	20	–	Ω
Xa	ageing	–	–	±5	10^{-6}/yr
Xj	adjustment tolerance	–	–	±25	10^{-6}
Xd	drift	–	–	±25	10^{-6}

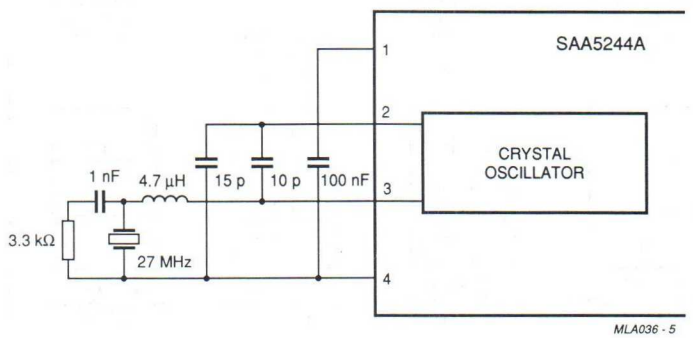


Fig.12 Crystal oscillator application diagram.

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional 2-pin design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone, as shown in Fig.12. The crystal characteristics are given in Table 5.

Character sets

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character sets differ only in 13 national option characters as indicated in Table 8 with reference to their table position in the basic character matrix illustrated in Table 7. The SAA5244A automatically decodes transmission bits C12 to C14. Table 6 illustrates the character matrixs.

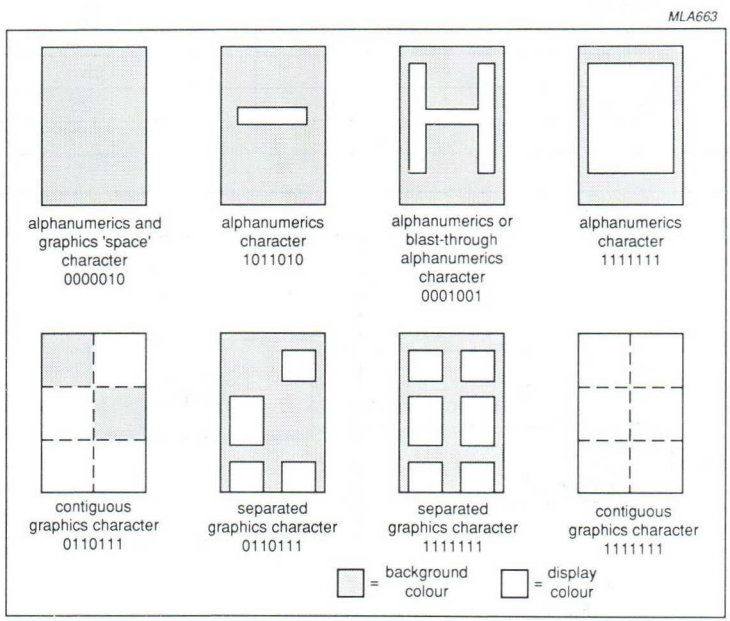
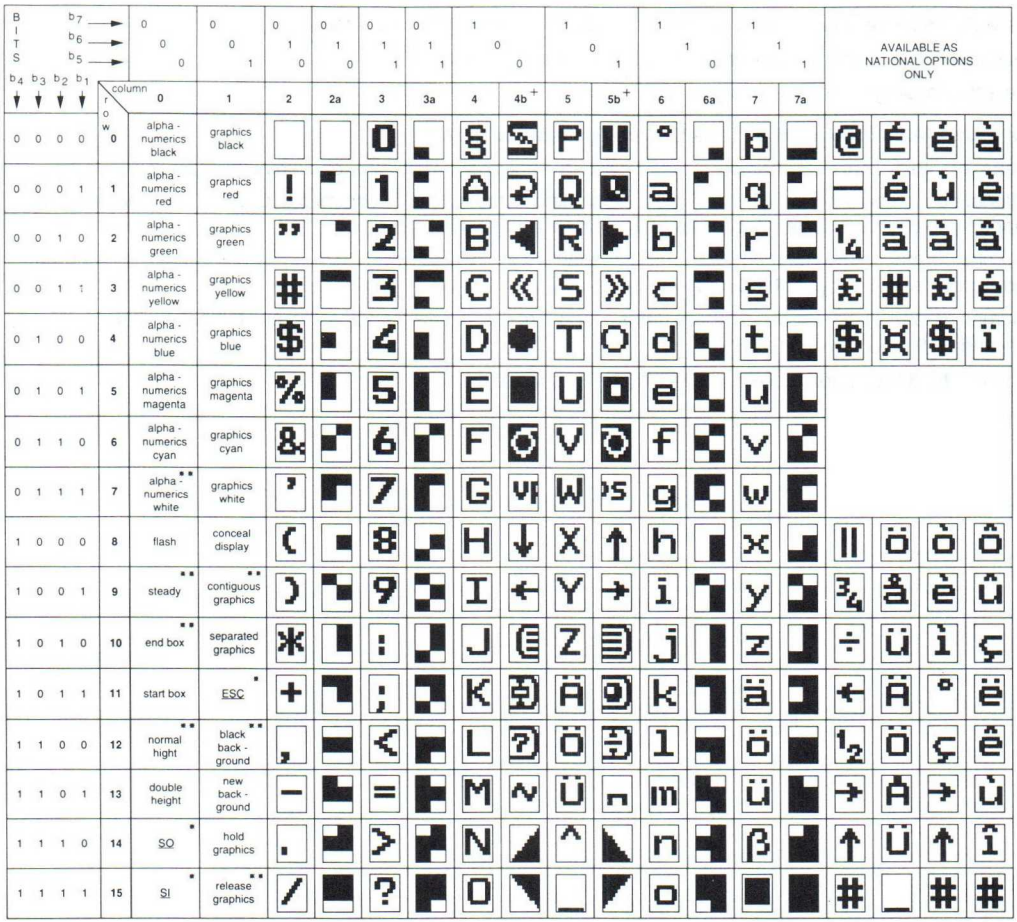


Fig.13 Character format.

Table 6 SAA5244P/A character data input decoding



For character version number (01000) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

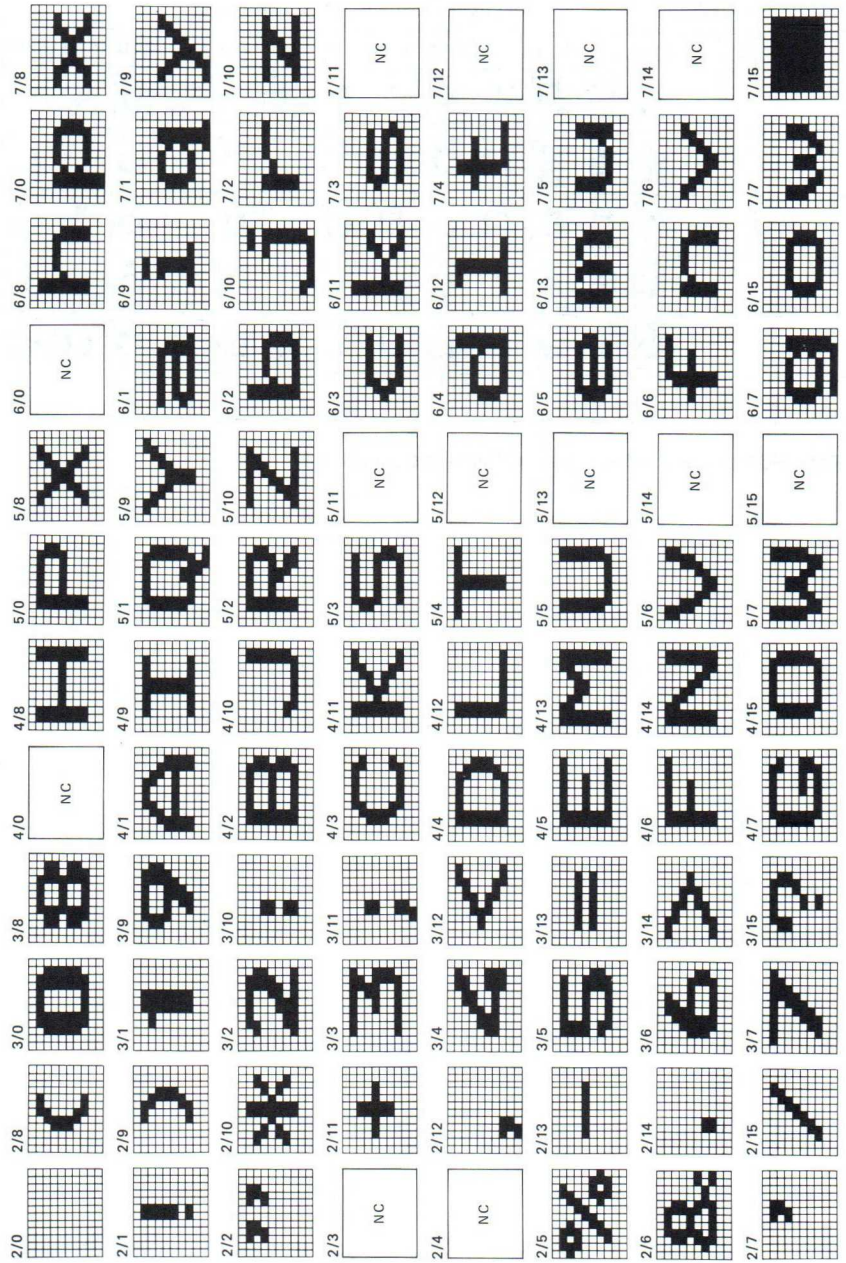
** These control characters are presumed before each row begins.

\+ Columns 4b and 5b can only be accessed when supplementary character bits are set (see Registers 9 and 10).

Notes to Table 6

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Characters may be referred to by column and row, For example 2/5 refers to %.
3. Black represents displayed colour. White represents backgound.
4. Character rectangle shown as follows: 
5. The SAA5244A national option characters are illustrated in Table 8.
6. Characters 4b/11, 4b/12, 5b/10, 5b/11 and 5b/12 are special characters for combining with character 4b/10.
7. National option characters will be developed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Table 8.
8. Columns 4b and 5b are mapped into 4 and 5 respectively (replacing blast-through alphanumerics in the graphics mode) when enabled by R9 bit D7 set to 1.
9. Columns 4b and 5b are mapped into columns 6 and 7 respectively when enabled by R10 bit D6 (row 0 columns 0 to 7) and R10 bit D7 (row 24) set to 1.
10. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.

Table 7 SAA5244A Basic character matrix



Where: NC = national option character position.

Table 8 SAA5244A national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç

MLA664

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

ENHANCED COMPUTER CONTROLLED TELETEXT CIRCUIT

(USECCT)

GENERAL DESCRIPTION

The SAA5245 is a MOS N-channel integrated circuit which performs all the digital logic functions of a 525-line World System Teletext decoder. It operates in conjunction with the teletext video processor SAA5231, standard static RAMs and is controlled via the 2-wire I²C-bus The device can be used to provide videotex display conforming to a serial character attribute protocol.

Features

- Microcomputer controlled for flexibility
- High quality flicker-free display using a 12 x 8 character matrix
- Field flyback (lines 5 to 19), or full channel (all lines) data acquisition
- Up to four simultaneous page requests enabling acquisition during one magazine cycle
- Direct interface up to 8 K bytes static RAM
- Automatic language selection of up to seven different languages
- 25th display row for software generated status messages
- Automatic processing of gearing function
- Cursor control for videotex/telesoftware
- 7-bits parity or 8-bit data acquisition
- Extension packet reception option
- Standard I²C-bus slave transceiver (slave address 0010001)
- Single 5 volt power supply
- Mask programmable character sets
- Slave sync mode operation
- Odd/even field output for de-interlaced displays

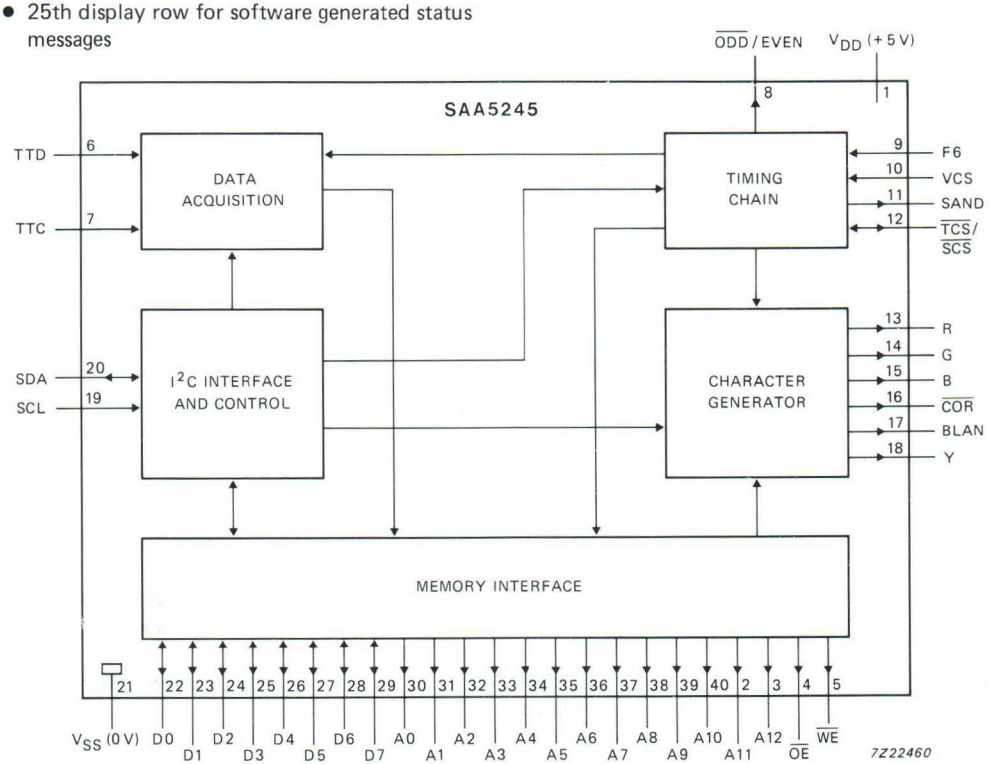


Fig. 1 Block diagram.

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).

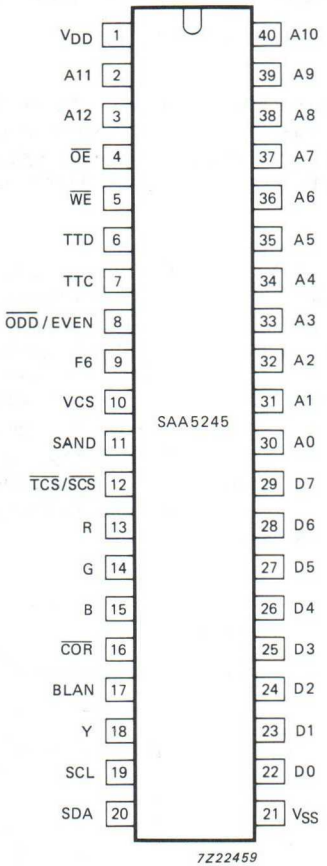


Fig. 2 Pinning diagram.

PINNING

1	V_{DD}	**Power supply**: + 5 V power supply pin.
2, 3, 40	A11, A12, A10	**Chapter Address**: three outputs that select which 1 K byte chapter of external RAM is being accessed for any read or write cycle.
4	$\overline{OE}$	**Output Enable**: active low output signal used to control the reading of the external RAM. It occurs continuously at a 1 MHz rate.
5	$\overline{WE}$	**Write Enable**: active low output signal used to control the writing of data to the external RAM. It occurs for a valid write cycle only and is interleaved with the read cycles.
6	TTD	**Teletext Data**: input from the SAA5231 Video Input Processor (VIP2). It is clamped to V_{SS} for 4 to 8 μs of each television line to maintain the correct DC level following the external AC coupling.

7	TTC	**Teletext Clock**: 5.727 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
8	$\overline{\text{ODD}}$/EVEN	**$\overline{\text{Odd}}$/Even:** for interlaced mode, the output changes once per field at 2 μs before the end of line 1 (263). The output is high for even fields and low for odd fields.
9	F6	**Character display clock**: 6.042 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
10	VCS	**Video Composite Sync**: input from the SAA5231 derived from the incoming video signal. Sync pulses are active high.
11	SAND	**Sandcastle**: 3-level sandcastle output to the SAA5231 containing the phase locking and colour burst blanking information.
12	$\overline{\text{TCS}}$/$\overline{\text{SCS}}$	**Text Composite Sync/Scan Composite Sync**: as an output an active low composite sync waveform (TCS) with interlaced or non-interlaced format (see Fig. 6) which is fed to the SAA5231 to drive the display timebases. Alternatively this pin can act as an input for an active low composite sync waveform (SCS) to 'slave' the display timing circuits.
13, 14, 15	R, G, B	**Red, Green, Blue:** these 3 open drain outputs are the character video signals to the television display circuits. They are active high and contain character and background information.
16	$\overline{\text{COR}}$	**Contrast Reduction**: open drain, active low output which allows selective contrast reduction of the television picture to enhance a mixed mode display.
17	BLAN	**Blanking**: open drain, active high output which controls the blanking of the television picture for a normal text display and for a mixed display.
18	Y	**Character foreground**: open drain, active high video output signal containing all the foreground information displayed on the television screen (e.g. for driving a display printer).
19	SCL	**Serial Clock**: input signal which is the I^2C-bus clock from the microcontroller.
20	SDA	**Serial Data**: is the I^2C-bus data line. It is an input/output function with an open drain output.
21	V_{SS}	**Ground**: 0 volts.
22-29	DO-D7	**8 RAM data lines**: 3-state input/output pins which carry the data bytes to and from the external RAM.
30-39	A0-A9	**RAM address**: 10 output signals that determine which byte location within a 1 K byte chapter of external RAM is accessed for any read or write cycle.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 1)	V_{DD}	−0.3	+ 7.5	V
Input voltage range				
VCS, SDA, SCL, D0 - D7	V_I	−0.3	+ 7.5	V
TTC, TTD, F6, $\overline{TCS}/\overline{SCS}$	V_I	−0.3	+ 10.0	V
Output voltage range				
SAND, A0 - A12, $\overline{OE}$, $\overline{WE}$, D0 - D7, SDA, $\overline{ODD}$/EVEN R, G, B, BLAN, $\overline{COR}$, Y	V_O	−0.3	+ 7.5	V
$\overline{TCS}/\overline{SCS}$	V_O	−0.3	+ 10.0	V
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−20	+ 70	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 1)	V_{DD}	4.5	5.0	5.5	V
Supply current (pin 1)	I_{DD}	–	160	270	mA
INPUTS (note 1)					
TTD (note 2)					
External coupling capacitor	C_{ext}	–	–	50	nF
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2.0	–	7.0	V
Input data rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input data set-up time (note 4)	t_{DS}	40	–	–	ns
Input data hold time (note 4)	t_{DH}	40	–	–	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
TTC; F6 (note 5)					
DC input voltage range	V_I	−0.3	–	+ 10.0	V
AC input voltage (peak-to-peak value) F6	$V_{I(p-p)}$	1.0	–	7.0	V
AC input voltage (peak-to-peak value) TTC	$V_{I(p-p)}$	1.5	–	7.0	V
Input peaks relative to 50% duty cycle	± V_P	0.2	–	3.5	V
TTC clock frequency	f_{TTC}	–	5.727	–	MHz
F6 clock frequency	f_{F6}	–	6.042	–	MHz
Clock rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
VCS					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SCL					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
SCL clock frequency	f_{SCL}	0	–	100	kHz
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
INPUT/OUTPUTS (note 6)					
$\overline{TCS}$ (output)/$\overline{SCS}$ (input)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.5	–	10.0	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 0 to 10 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
at I_{OH} = 0.1 mA	V_{OH}	2.4	–	6.0	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SDA (note 7)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V with output off	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	0	–	0.5	V
Output fall time between 3.0 V and 1.0 V levels	t_f	–	–	200	ns
Load capacitance	C_L	–	–	400	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
INPUT/OUTPUTS (continued)					
D0-D7 (note 8)					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input leakage current at V_I = 0 V to 5.5 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
OUTPUTS (note 6)					
A0-A12; $\overline{OE}$; $\overline{WE}$ (note 8)					
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
$\overline{ODD}$/EVEN					
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SAND (note 9)					
Output voltage LOW at I_{OL} = 0.2 mA	V_{OL}	0	–	0.25	V
Output voltage INTERMEDIATE at I_{OL} = ± 10 μA	V_{OI}	1.1	–	3.1	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SAND (continued)					
Output voltage HIGH at I_{OH} = 0 to −10 μA	V_{OH}	4.0	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0.4 V and 0.9 V levels	t_{r1}	–	–	400	ns
Output rise time V_{OI} to V_{OH} between 3.3 V and 3.8 V levels	t_{r2}	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 3.8 V and 0.4 V levels	t_f	–	–	50	ns
Load capacitance	C_L	–	–	30	pF
R; G; B; $\overline{\text{COR}}$; BLAN; Y (note 10)					
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	0	–	0.4	V
Output voltage LOW at I_{OL} = 5 mA	V_{OL}	0	–	1.0	V
Pull-up voltage as seen at pin	V_{PU}	–	–	6.0	V
Output fall time with a load resistor of 1.2 kΩ to 6 V and measured between 5.5 V and 1.5 V	t_f	–	–	20	ns
Skew delay between outputs with a load resistor of 1.2 kΩ to 6 V and measured on the falling edges at 3.5 V	t_{SK}	–	–	20	ns
Load capacitance	C_L	–	–	25	pF
Output leakage current at V_{PU} = 0 to 6 V with output off	I_{LO}	–	–	10	μA
TIMING					
I²C-bus (note 11)					
Clock low period	t_{LOW}	4	–	–	μs
Clock high period	t_{HIGH}	4	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	170	–	–	ns
Stop set-up time from clock high	$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop	t_{BUF}	4	–	–	μs
Start hold time	$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock low-to-high transition	$t_{SU;STA}$	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
TIMING (continued)					
Memory interface (note 12)					
Cycle time	t_{CY}	–	495	–	ns
Address change to $\overline{OE}$ LOW	t_{OE}	60	–	–	ns
Address active time	t_{ADDR}	450	495	–	ns
$\overline{OE}$ pulse duration	t_{OEW}	320	–	–	ns
Access time from $\overline{OE}$ to data valid	t_{ACC}	–	–	200	ns
Data hold time from $\overline{OE}$ HIGH or address change	t_{DH}	0	–	–	ns
Address change to $\overline{WE}$ LOW	t_{WE}	40	–	–	ns
$\overline{WE}$ pulse duration	t_{WEW}	200	–	–	ns
Data set-up time to $\overline{WE}$ HIGH	t_{DS}	100	–	–	ns
Data hold time from $\overline{WE}$ HIGH	t_{DHWE}	20	–	–	ns
Write recovery time	t_{WR}	25	–	–	ns
QUALITY (note 13)					
Failure rate					
Failure rate at T_{amb} = 55 °C (1×10^{-6} failures per hour)		–	–	1000	FITS

DEVELOPMENT DATA

Notes to the characteristics

1. All inputs are protected against static charge under normal handling.
2. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor (see Fig. 3).
3. Rise and fall times between 10% and 90% levels.
4. Teletext input data set-up and hold times are with respect to a 50% duty cycle level of the rising edge of the teletext clock input (TTC). Data stable $1 \geqslant 2.0$ V; data stable $0 \leqslant 0.8$ V (see Fig. 4).
5. The TTC and F6 inputs have internal clamping diodes and are AC coupled (see Fig. 3).
6. All outputs and input/outputs are protected against static charge under normal handling and connection to V_{DD} and V_{SS}.
7. For details of I^2C-bus timing see Fig. 8.
8. For details of RAM timing see Fig. 9.
9. For details of synchronization timing see Fig. 5.
10. For details of display output timing see Fig. 7.
11. The I^2C-bus timings are referred to V_{IH} = 3 V and V_{IL} = 1.5 V. For waveforms see Fig. 8.
12. The memory interface timings are referred to V_{IL} = 1.5 V. For waveforms see Fig. 9.
13. This device shall meet the requirements of the Elcoma General Quality and Specification for ICs: URV - 4 - 2 - 59/601 (LSI).

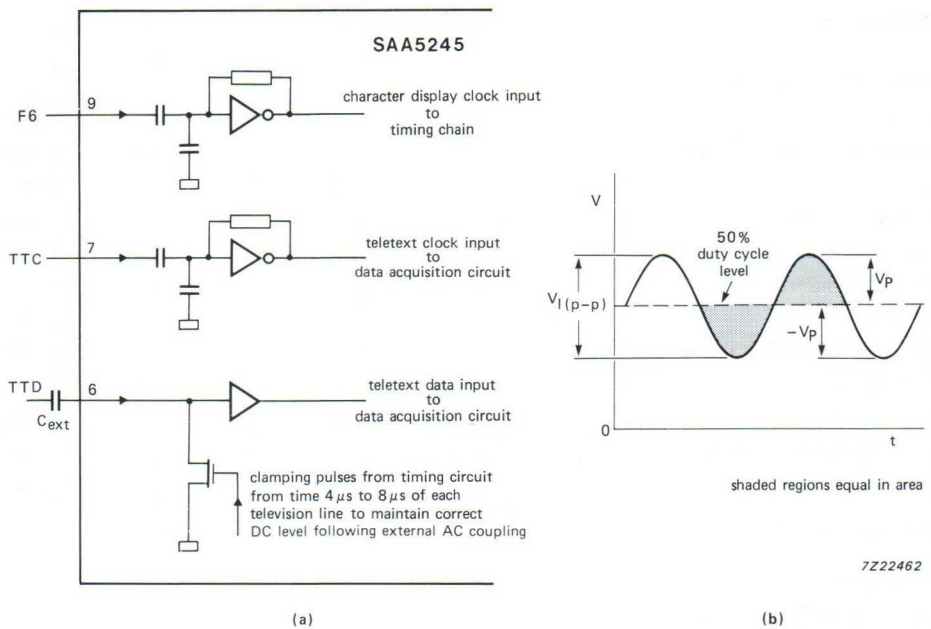
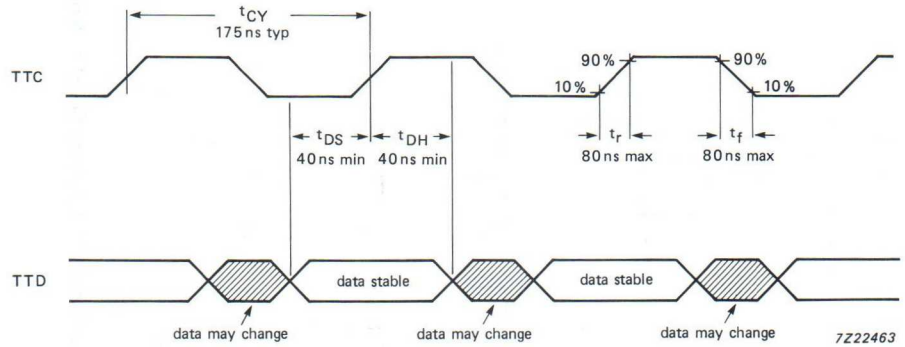


Fig. 3 (a) F6, TTC and TTD input circuitry (b) input waveform parameters.



Data stable: 1 is $\geqslant$ 2.0 V; 0 is $\leqslant$ 0.8 V.

Fig. 4 Teletext data input timing.

DEVELOPMENT DATA

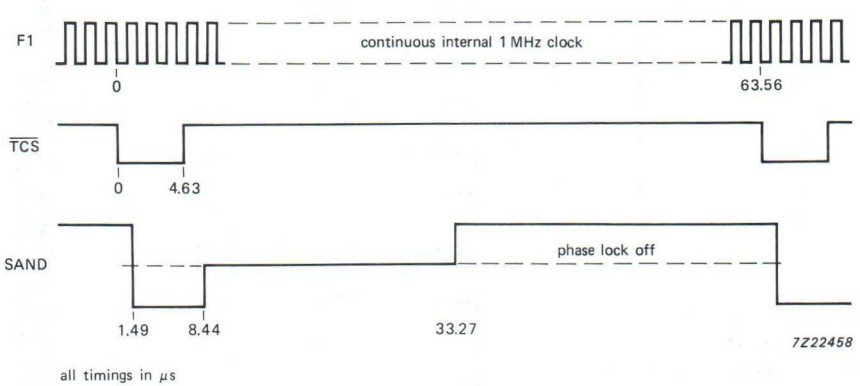
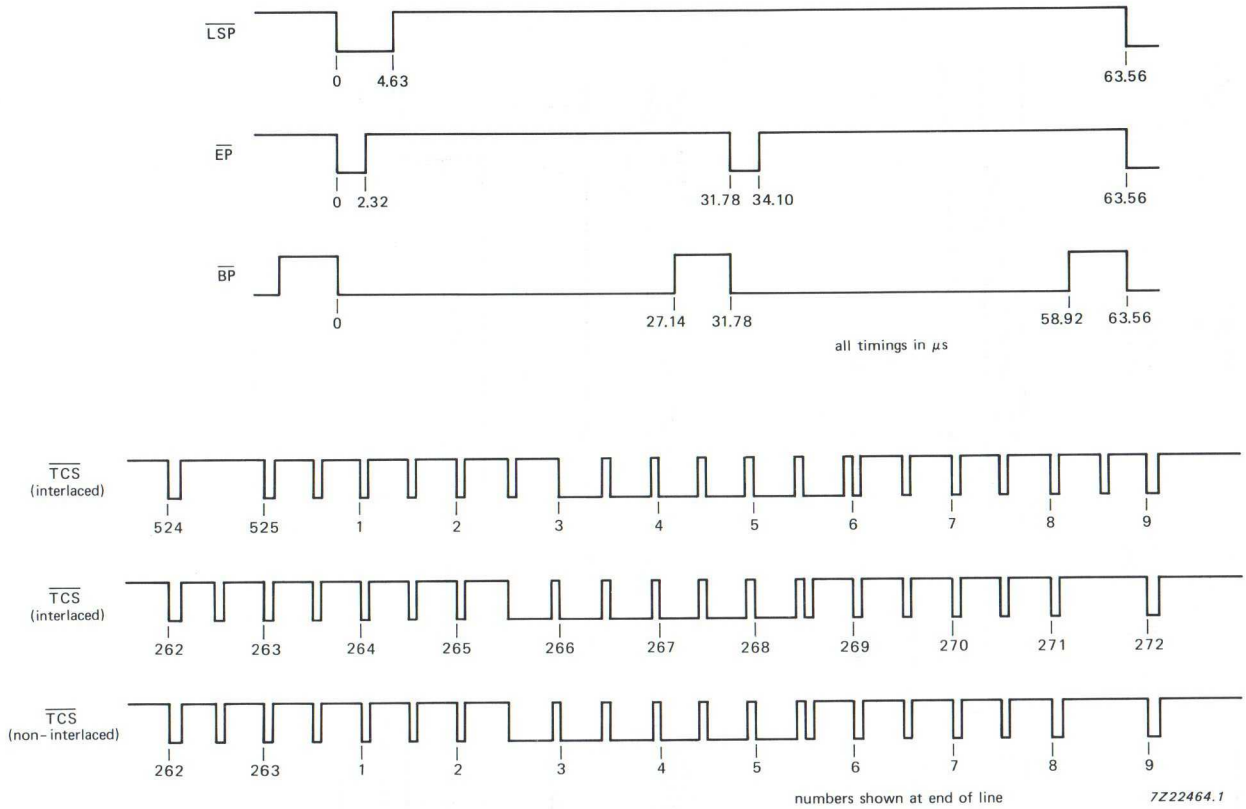


Fig. 5 Synchronization timing.



Line sync pulses ($\overline{LSP}$), equalizing pulses ($\overline{EP}$) and broad pulses ($\overline{BP}$) are combined to provide the text composite sync waveform ($\overline{TCS}$) as shown. All timings measured from falling edge of $\overline{LSP}$ with a tolerance of ± 100 ns.

Fig. 6 Composite sync waveforms (525-line version).

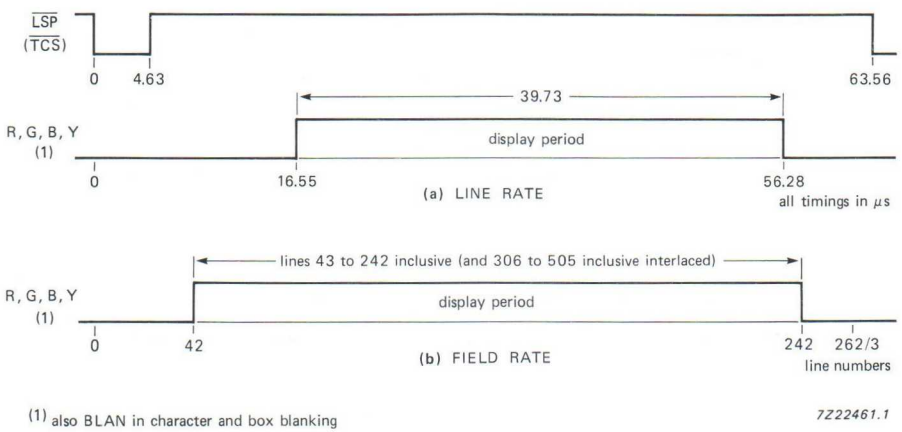


Fig. 7 Display output timing (a) line rate (b) field rate.

DEVELOPMENT DATA

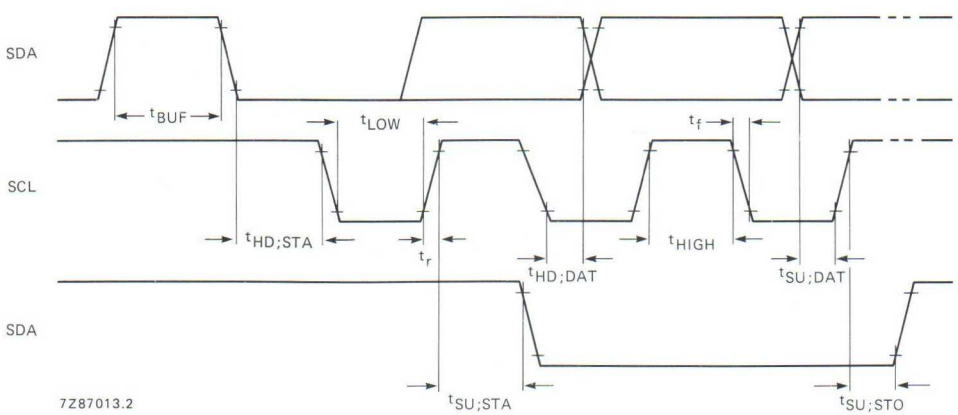


Fig. 8 I²C-bus timing.

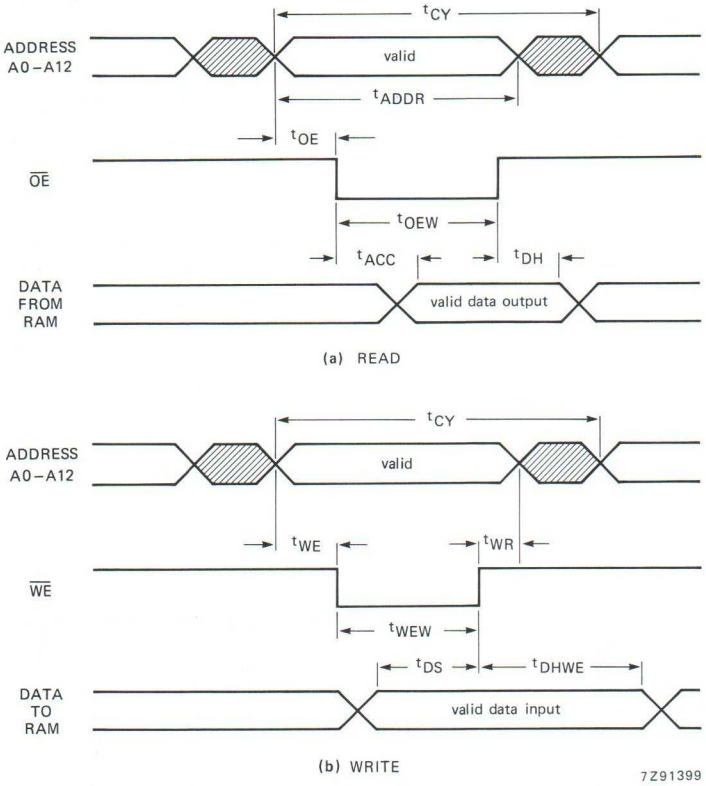


Fig. 9 Memory interface timing (a) read (b) write.

DEVELOPMENT DATA

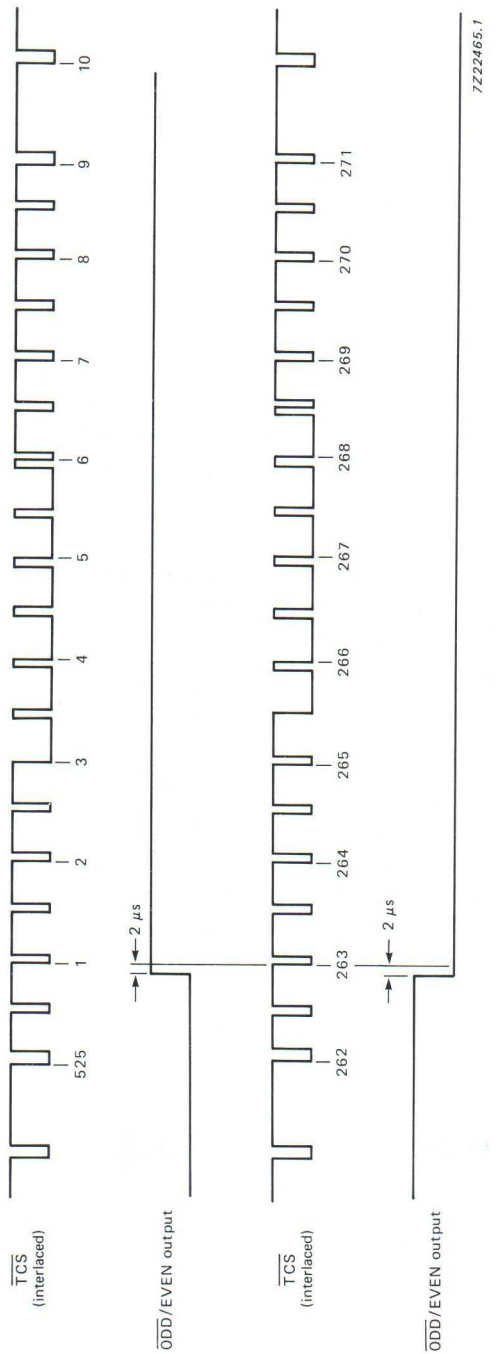


Fig. 10 $\overline{\text{ODD}}$/EVEN timing diagram.

APPLICATION INFORMATION

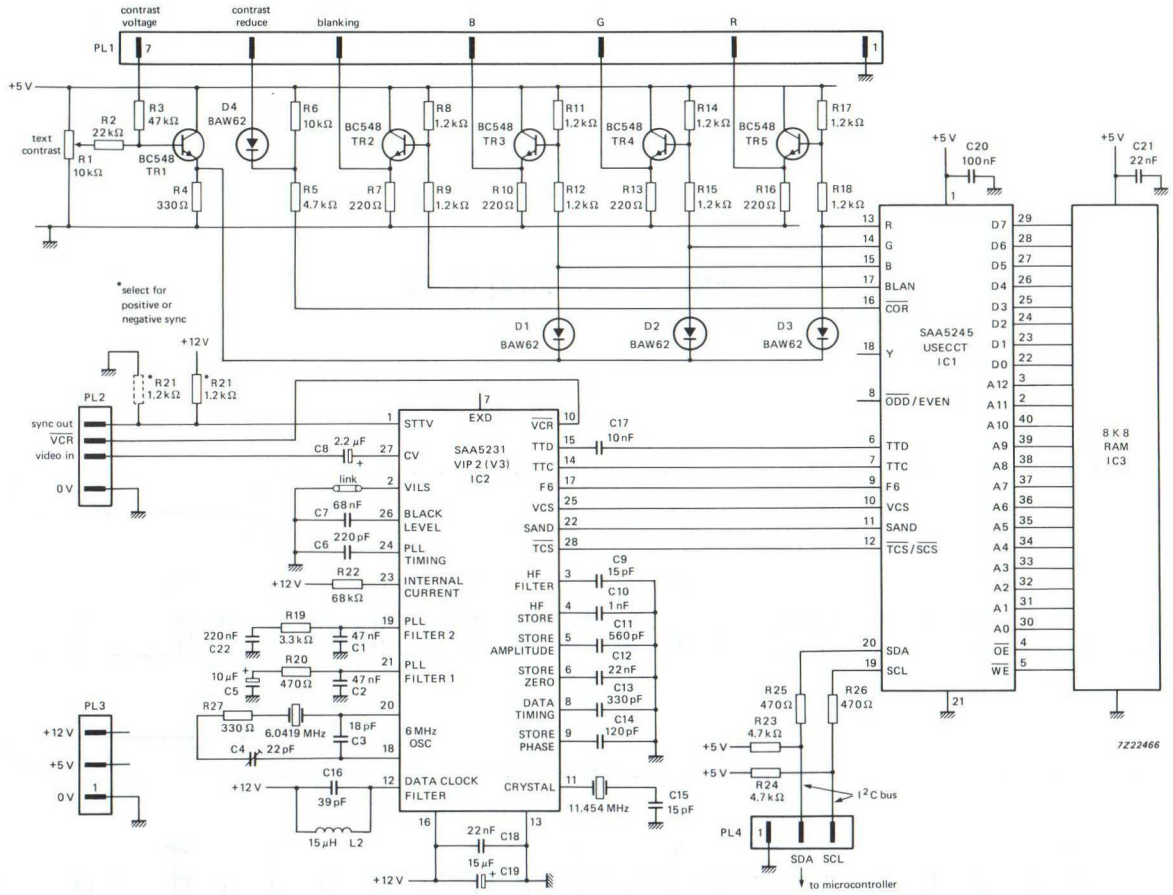


Fig. 11 USECCT based multi-page decoder circuit diagram.

DEVELOPMENT DATA

USECCT page memory organization

The organization of a page memory is shown in Fig. 12. The USECCT provides an additional row compared with first generation decoders bringing the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page as broadcast and row 24 is the extra row available for user-generated status messages.

A MORE DETAILED DESCRIPTION OF USECCT OPERATION AND APPLICATION IS AVAILABLE ON REQUEST.

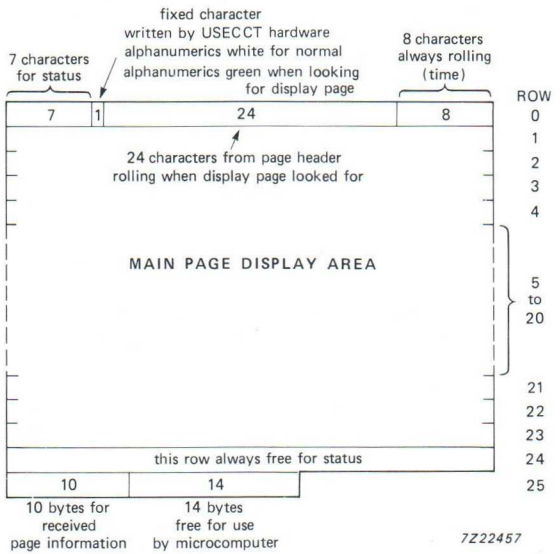


Fig. 12 Page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	0	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

MAG	magazine	page number	MU	minutes units	page sub-code
PU	page units		MT	minutes tens	
PT	page tens		HU	hours units	
$\overline{\text{PBLF}}$	page being looked for		HT	hours tens	
$\overline{\text{FOUND}}$	LOW for page has been found		C4-C14	transmitted control bits	
HAM.ER	Hamming error in corresponding byte				

APPLICATION INFORMATION (continued)

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by USECCT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page. Seven digits are used to identify a page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

Register maps

USECCT mode registers R1 to R11 are shown in Table 2. R1 to R10 are WRITE only; R11 is READ/WRITE.
Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 USECCT register map

		D7	D6	D5	D4	D3	D2	D1	D0
Operating mode	R1	TA	$\overline{7+P}$/ 8 BIT	ACQ. $\overline{ON}$/OFF	EXTENSION PACKET ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0
Page request address	R2	–	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	R3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
Display chapter	R4	–	–	–	–	–	A2	A1	A0
Display control (normal)	R5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash/subtitle)	R6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	R7	STATUS ROW $\overline{BTM}$/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
Active chapter	R8	–	–	–	–	CLEAR MEM.	A2	A1	A0
Active row	R9	–	–	–	R4	R3	R2	R1	R0
Active column	R10	–	–	C5	C4	C3	C2	C1	C0
Active data	R11	D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)

–bit does not exist

Notes to Table 2

The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^2C transmission byte. TA and TB must be logic 0 for normal operation.
All bits in registers R1 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to logic 1.
All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is enabled but all pages are on hold.

Where:

R1 Mode

T0, T1	interlace/non-interlace 262/263 line control
TCS ON	text composite sync or direct sync select
$\overline{\text{DEW}}$/FULL FIELD	field-flyback or full channel mode
$\overline{7+P}$/8 BIT	7 bits with parity checking or 8-bit mode
TA, TB	test bits; 0 for normal operation

R2 Page request address

START COLUMN	start column for page request data
ACQ CCT	selects one of four acquisition circuits
BANK SELECT	selects bank of four pages being addressed for acquisition

R3 Page request data — see Table 3

R4 Display chapter — determines which of the 8 pages is displayed

R5, R6 Display control — for normal and newsflash/subtitle

PON	picture on
TEXT	text on
COR	contrast reduction on
BKGND	background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 Display mode

BOX ON 0 (1-23, 24)	boxing function allowed on row 0 (row 1-23, 24)
STATUS ROW $\overline{\text{BTM}}$/TOP	row 25 displayed above or below the main text

R8 to R11 — active chapter, row, column and data information written to or read from page memory via the I^2C-bus

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

Table 3 Register map for page requests (R3)

Start Column	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	X	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

Abbreviations are as for Table 1 except for D0 CARE bits.
When the D0 CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the D0 CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
There are four groups of data shown in Table 3, one for each acquisition circuit (four simultaneous page requests).
Columns auto-increment on successive I^2C transmission bytes.



Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

CHARACTER SETS

The US teletext specification allows the selection of national character sets via the page header transmission bits, C12 to C14 as shown in Table 4.
USECCT automatically decodes transmission bits C12 to C14. Other combinations of C12 to C14 are defaulted to English in SAA5245P/A. With 8-bit decoding the character matrices are shown in Table 5.

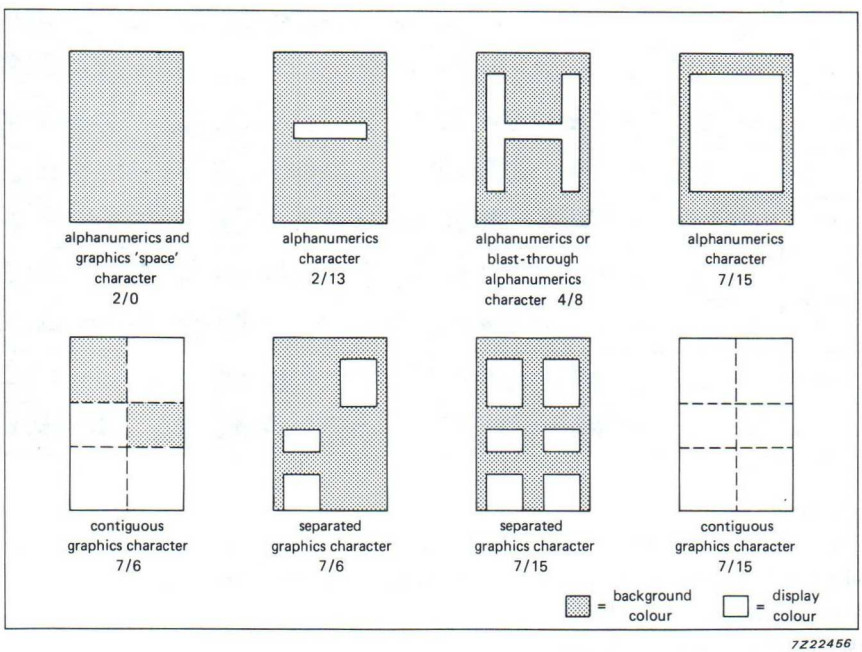
Table 4 Selection of national character sets (SAA5245P/A)

PHCB	ENGLISH	GERMAN	SWEDISH	ITALIAN	FRENCH	SPANISH
C12	0	0	0	0	1	1
C13	0	0	1	1	0	0
C14	0	1	0	1	0	1

Where:

PHCB page header control bits.

DEVELOPMENT DATA



Character bytes are listed as transmitted from b_1 to b_7.

Fig. 13 Character format.

APPLICATION INFORMATION (continued)

Table 5 Character data input decoding (SAA5245A).

BITS b_8	0	0	0 or 1		0 or 1		0	0	0		0		1	1	1	1	1	1
b_7	0	0	0		0		1	1	1		1		0	0	1	1	1	1
b_6	0	0	1		1		0	0	1		1		0	0	0	1	1	1
b_5	0	1	0		1		0	1	0		1		0	1	0	1	0	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓ row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha–numerics black	graphics black															
0 0 0 1	1	alpha–numerics red	graphics red															
0 0 1 0	2	alpha–numerics green	graphics green															
0 0 1 1	3	alpha–numerics yellow	graphics yellow															
0 1 0 0	4	alpha–numerics blue	graphics blue															
0 1 0 1	5	alpha–numerics magenta	graphics magenta															
0 1 1 0	6	alpha–numerics cyan	graphics cyan															
0 1 1 1	7	alpha–numerics white **	graphics white															
1 0 0 0	8	flash	conceal display															
1 0 0 1	9	steady **	contiguous graphics **															
1 0 1 0	10	end box **	separated graphics															
1 0 1 1	11	start box	ESC *															
1 1 0 0	12	normal height **	black background **															
1 1 0 1	13	double height	new background															
1 1 1 0	14	SO *	hold graphics															
1 1 1 1	15	SI *	release graphics **															

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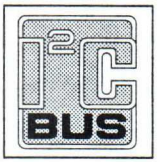
Notes to Table 5

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Codes may be referred to by column and row. For example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows: □
5. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters to combine with character 8/5.
6. With bit 8 = 0 national option characters will be decoded according to the setting of control bits C12 to C14 (see Table 4).

* These control characters are reserved for compatibility with other data codes.
** These control characters are presumed before each row begins.

Integrated VIP and Teletext (IVT1.0)

SAA5246A



FEATURES

- Complete Teletext decoder in a 48-pin DIL, 52-pin shrink DIL, or 64-pin QFP, integrated circuit
- Single +5 V power supply
- Both video and scan related synchronization modes are supported
- RGB interface to standard colour decoder ICs, push-pull output drive
- Digital data slicer and display clock phase-locked loop reduce peripheral components to a minimum
- Data capture performance similar to SAA5231 (VIP2)
- Option for up to seven national languages
- Optional storage of packet 24 in the display memory
- Separate text and video signal quality detectors, 625/525 video status and language version all readable via I²C-bus
- Automatic $\overline{\text{ODD}}$/EVEN output control with override
- Control of display PLL free-run and rolling header via I²C-bus
- VCS to SCS mode for stable 525 line status display.

DESCRIPTION

The SAA5246A is a single-chip teletext decoder IC for decoding 625 line base World System Teletext transmissions. The teletext decoder hardware is based on the Enhanced Computer Controlled ECCT device (SAA5243) with some additional features.
The Video Input Processor section of the device uses mixed analog and digital designs in the data slicer and clock phase-locked-loop functions. As a result the number of external components are greatly reduced and no critical or adjustable components are required.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	64	128	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1.0	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5246AP	48	DIL	plastic	SOT240A
SAA5246AZP	52	shrink DIL	plastic	SOT247
SAA5246AGP	64	QFP	plastic	SOT208A

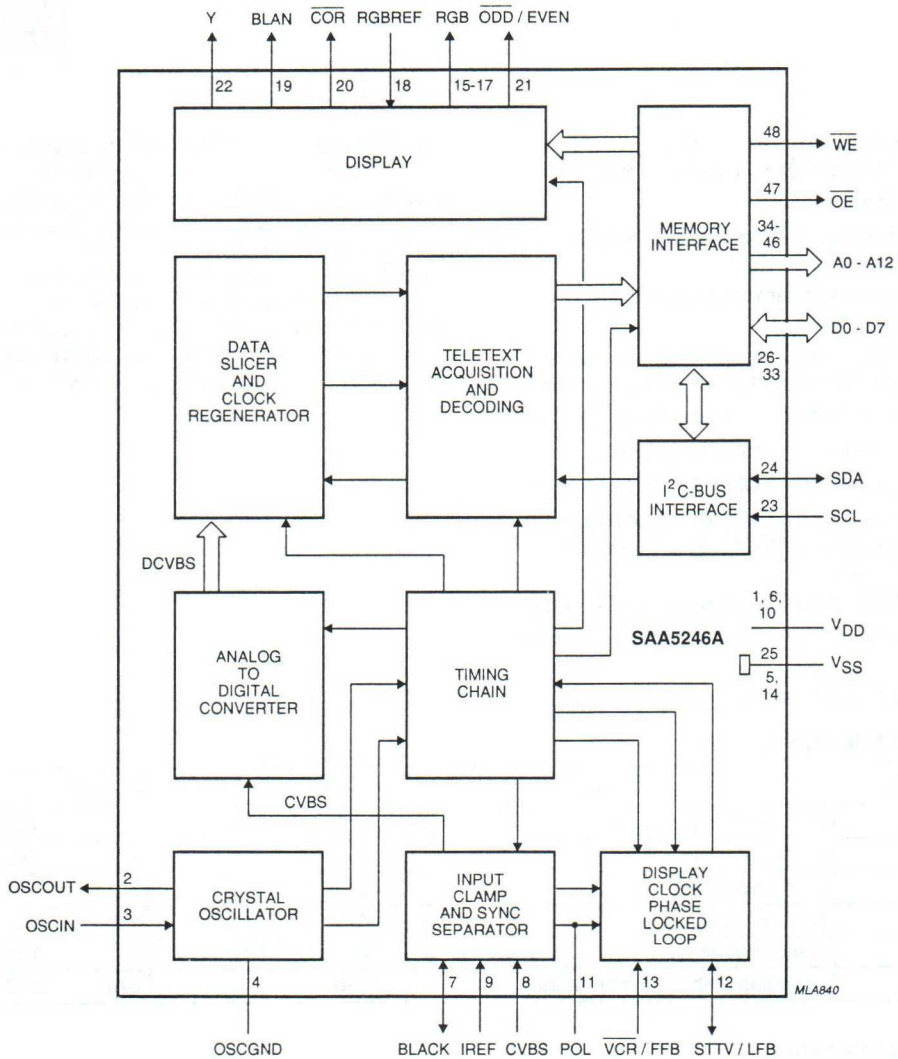


Fig.1 Block diagram for SOT240 (DIL48) package.

PINNING

SYMBOL	PIN			DESCRIPTION
	SOT240	SOT247	SOT208	
OSCOUT	2	1	27	27 MHz crystal oscillator output
OSCIN	3	2	28	27 MHz crystal oscillator input
OSCGND	4	3	29	0 V crystal oscillator ground
V_{SS}	5, 14, 25	4, 5, 15, 26	26, 30, 31, 43, 58	0 V ground
BLACK	7	8	35	video black level storage pin, connected to ground via a 100 nF capacitor
CVBS	8	9	36	composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor
IREF	9	10	37	reference current input pin, connected to ground via a 27 kΩ resistor
V_{DD}	1, 6, 10	6, 11, 52	25, 32, 38	+5 V positive supply
POL	11	12	39	STTV/LFB/FFB polarity selection pin
STTV/LFB	12	13	40	sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode)
$\overline{VCR}$/FFB	13	14	42	PLL time constant switch/field input pin. Function controlled by an internal register bit (scan sync mode)
R	15	16	44	dot rate character output of the RED colour information
G	16	17	45	dot rate character output of the GREEN colour information
B	17	18	47	dot rate character output of the BLUE colour information
RGBREF	18	19	48	input DC voltage to define the output high level on the RGB pins
BLAN	19	20	52	dot rate fast blanking output
$\overline{COR}$	20	21	53	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open-drain output
$\overline{ODD}$/EVEN	21	22	54	a 25 Hz output synchronized to the input CVBS field sync pulses to make a non-interlaced display by adjustment of the vertical deflection currents.
Y	22	23	55	dot rate character output of teletext foreground colour information. Open-drain output
SCL	23	24	56	serial clock input for I²C-bus. It can still be driven HIGH during power-down of the device
SDA	24	25	57	serial data port for the I²C-bus. Open drain output. It can still be driven HIGH during power-down of the device
D0-D5	26-31	27-32	60-64, 3	data ports for the page SRAM
n.c.	–	7, 33, 34	1, 2, 10, 11, 15, 18, 33, 34, 41, 46, 49 - 51, 59	not connected

SYMBOL	PIN			DESCRIPTION
	SOT240	SOT247	SOT208	
D6-D7	32, 33	35, 36	4, 5	data ports for the page SRAM
A0-A12	34-46	37-49	6-9, 12-14, 16, 17, 19-22	address output for the page SRAM
$\overline{OE}$	47	50	23	output enable for the page SRAM
$\overline{WE}$	48	51	24	write enable for the page SRAM

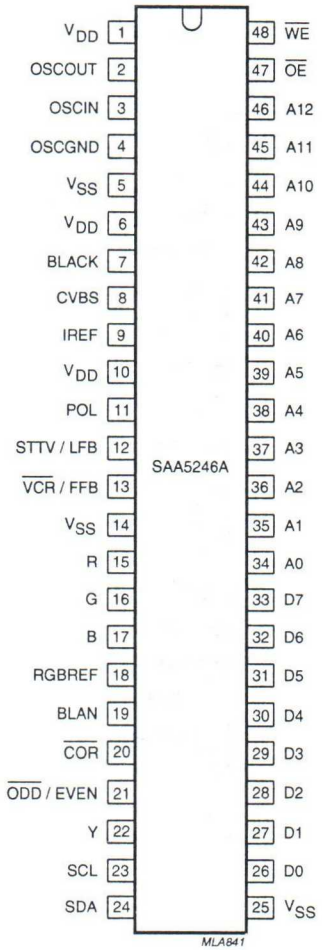


Fig.2 Pin configuration; SOT240 (DIL48).

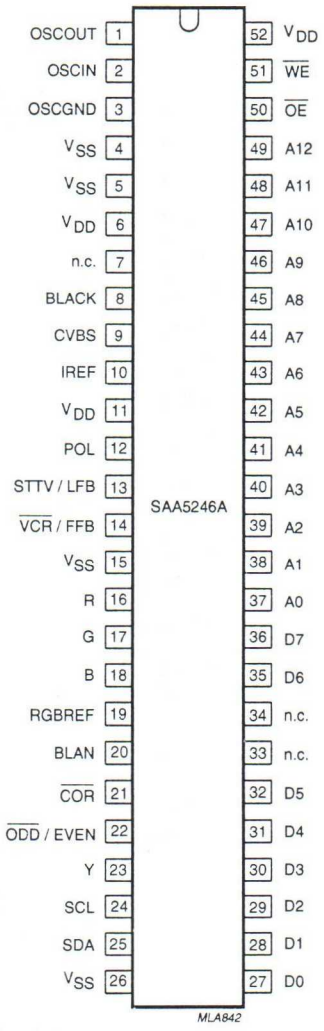


Fig.3 Pin configuration; SOT247 (SDIL52).

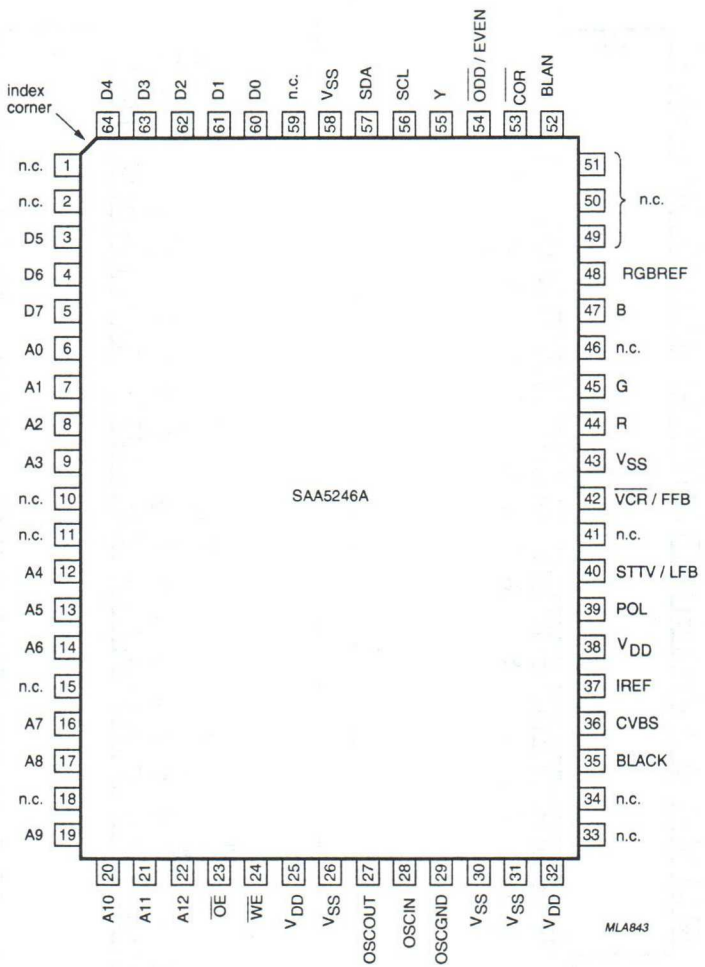


Fig.4 Pin configuration; SOT208 (QFP64).

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	−0.3	6.5	V
V_I	input voltage (any input)	−0.3	V_{DD} +0.5	V
V_O	output voltage (any output)	−0.3	V_{DD} +0.5	V
I_O	output current (each output)	–	±10	mA
I_{IOK}	DC input or output diode current	–	±20	mA
T_{amb}	operating ambient temperature	−20	+70	°C
T_{stg}	storage temperature	−55	+125	°C
V_{stat}	electrostatic handling (see note 1)	−2000	+2000	V

Note to the Limiting values

1. Electrostatic handling is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a 15 ns rise time.

Failure Rate

The failure rate at T_{amb} = 55 °C will be a maximum of 1000 FITS (1 FIT = 1 x 10^{-9} failures per hour).

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −20 to +70 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage range		4.5	5.0	5.5	V
I_{DD}	total supply current		–	64	128	mA
Inputs						
CVBS						
V_{syn}	sync amplitude		0.1	0.3	0.6	V
t_{syn}	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		−150	0	+150	ns
t_{syd}	change in sync delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{vid(p-p)}$	video input amplitude (peak-to-peak)		0.7	1.0	1.4	V
	display PLL catching range		±7	–	–	%
Z_{src}	source impedance		–	–	250	Ω
C_I	input capacitance		–	–	10	pF
IREF						
R_g	resistor to ground		–	27	–	kΩ
POL						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
LFB						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_I	input current	note 1	−1	–	+1	mA
t_{LFB}	delay between LFB front edge and input video line sync		–	250	–	ns
$\overline{VCR}$/FFB						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_I	input current	note 1	−1	–	+1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGBREF						
V_{IL}	LOW level input voltage		−0.3	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_{DC}	DC current		–	–	10	mA
SCL						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
f_{SCL}	clock frequency		0	–	100	kHz
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
C_I	input capacitance		–	–	10	pF
Inputs/outputs						
CRYSTAL OSCILLATOR (OSCIN; OSCOUT)						
f_{XTAL}	crystal frequency		–	27	–	MHz
V_{OSC}	oscillation amplitude (peak-to-peak value)		–	1.5	–	V
G_v	small signal voltage gain		–	1	–	V/V
G_m	mutual conductance		5	–	–	mA/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	1	–	pF
BLACK						
C_{blk}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
SDA						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	3 V to 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF

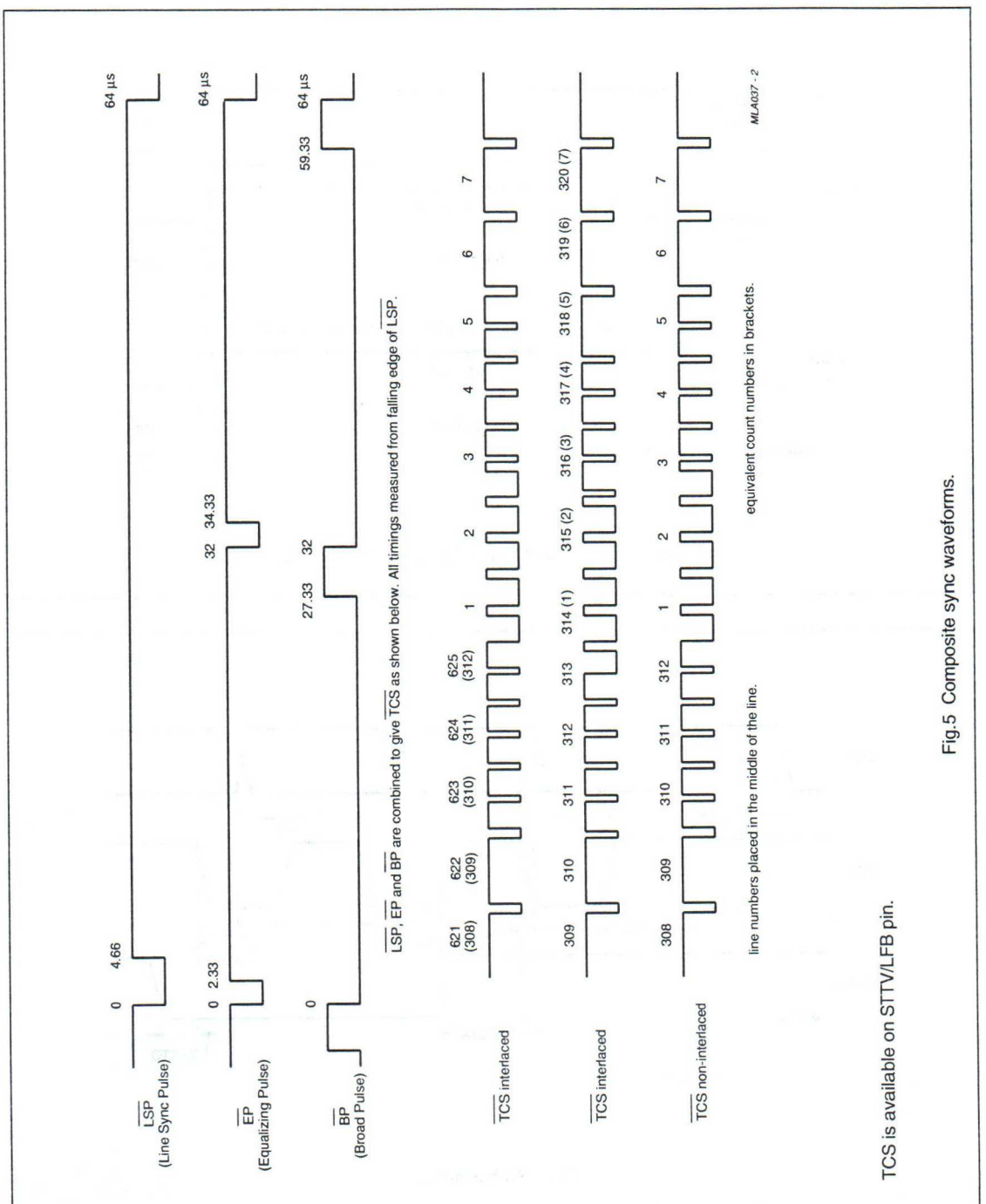
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
D0 TO D7						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current		−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
t_r	output rise time	0.6 V to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	50	ns
C_L	load capacitance		–	–	120	pF
Outputs						
STTV						
G_{stt}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{tcs}	TCS amplitude		0.2	0.3	0.45	V
V_{DCs}	DC shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive current		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
A0 TO A12 ADDRESS OUTPUT TO MEMORY						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 V to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	50	ns
$\overline{OE}$, $\overline{WE}$						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 V to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R, G AND B						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = −1.6 mA; RGBREF ≤ V_{DD}−2 V; note 2	RGBREF −0.25 V	RGBREF	RGBREF +0.25 V	V
I_{DC}	DC current		–	–	−3.3	mA
$\|Z_o\|$	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
BLAN						
V_{OL}	LOW level output voltage	I_{OL} = 0.2 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA; V_{DD} = 4.5 V; note 2	1.1	–	–	V
V_{OH}	HIGH level output voltage	I_{OH} = 0 mA; V_{DD} = 5.5 V; note 2	–	–	2.8	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
$\overline{ODD}$/EVEN						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −1.6 mA	V_{DD}−0.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
$\overline{COR}$ AND Y (OPEN DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V
V_{OL}	LOW level output voltage	I_{OL} = +2 mA	0	–	0.4	V
V_{OL}	LOW level output voltage	I_{OL} = +5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} −0.5 and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
T_{SK}	skew delay between display outputs R, G, B, $\overline{COR}$, Y and BLAN		–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
MEMORY INTERFACE						
t_{CY}	cycle time		–	500	–	ns
t_{OE}	address change to $\overline{OE}$ LOW		55	–	–	ns
t_{ADDR}	address active time		450	500	–	ns
t_{rOEW}	$\overline{OE}$ pulse width read		295	–	–	ns
t_{wOEW}	$\overline{OE}$ pulse width write		100	–	–	ns
t_{ACC}	access time from address data valid		–	–	150	ns
t_{DH}	data hold time from $\overline{OE}$ HIGH or address change		0	–	150	ns
t_{WEW}	$\overline{WE}$ pulse width		100	–	–	ns
t_{DS}	data set-up time to $\overline{WE}$ HIGH		60	–	–	ns
t_{DHWE}	data hold time from $\overline{WE}$ HIGH		20	–	–	ns
t_{WR}	write recovery time		20	–	–	ns
t_{DE}	data enable from $\overline{WE}$ LOW		60	–	–	ns
I^2C-BUS						
t_{LOW}	clock LOW period		4	–	–	µs
t_{HIGH}	clock HIGH period		4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;STA}$	START hold time		4	–	–	µs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	µs

Notes to the characteristics

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ± 1 mA.
2. Can be pulled higher by external pull-up resistor, (maximum leakage current ≈ 200 µA).



TCS is available on STTV/LFB pin.

Fig.5 Composite sync waveforms.

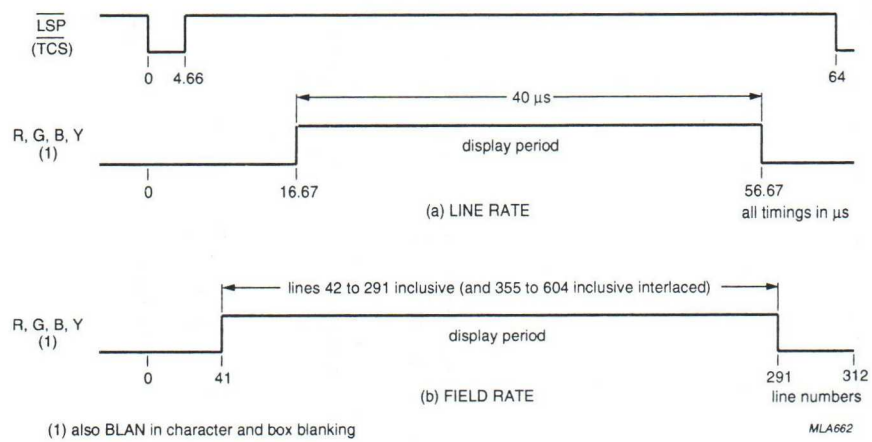


Fig.6 Display output timing (a) line rate (b) field rate.

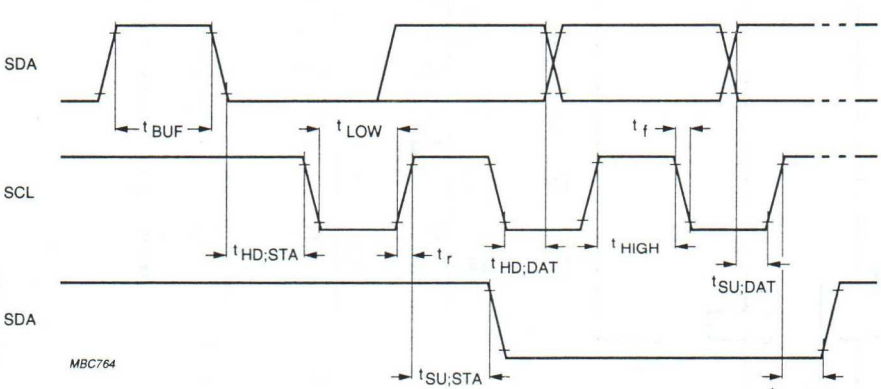
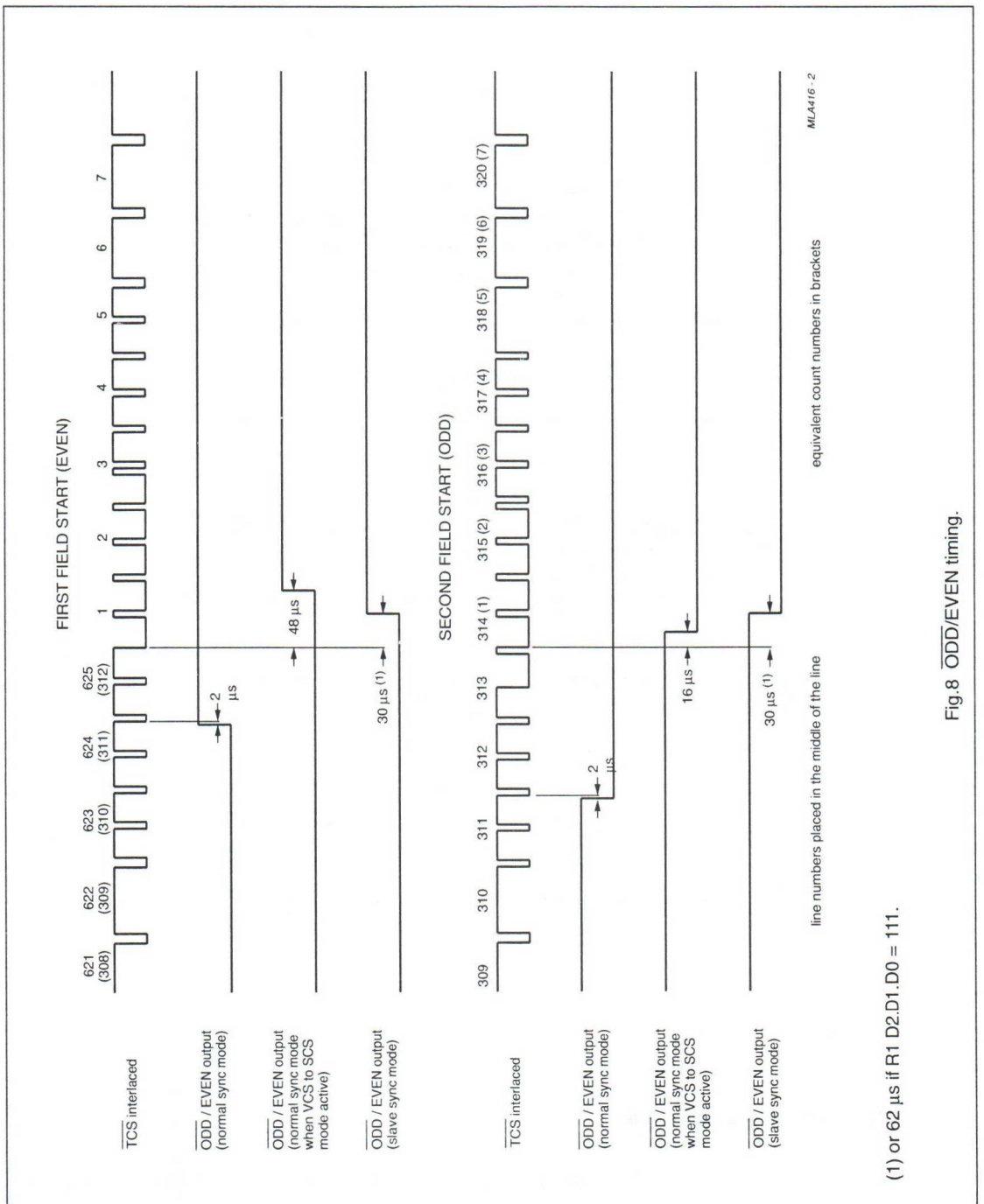
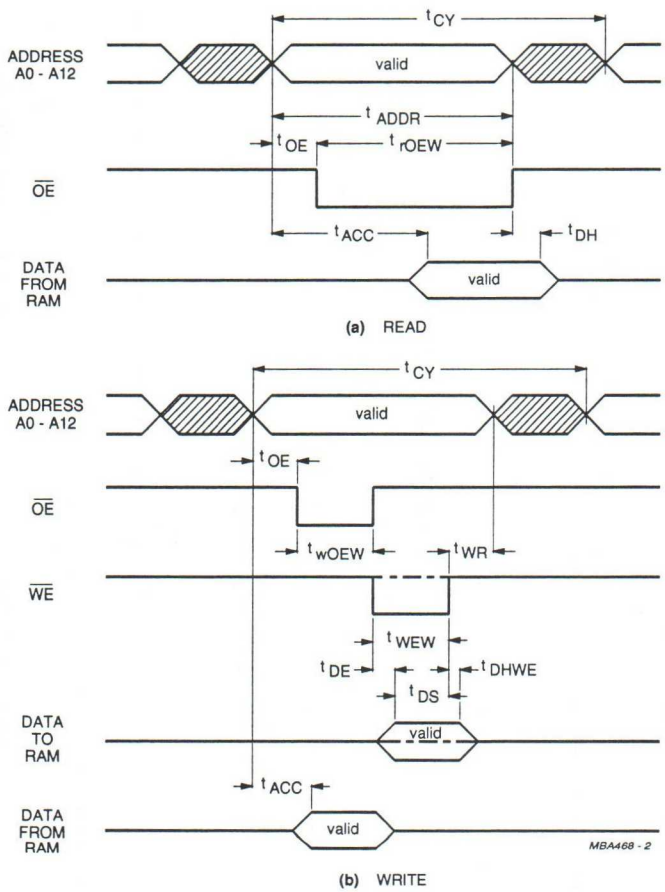


Fig.7 I²C-bus timing.



(1) or 62 µs if R1 D2.D1.D0 = 111.

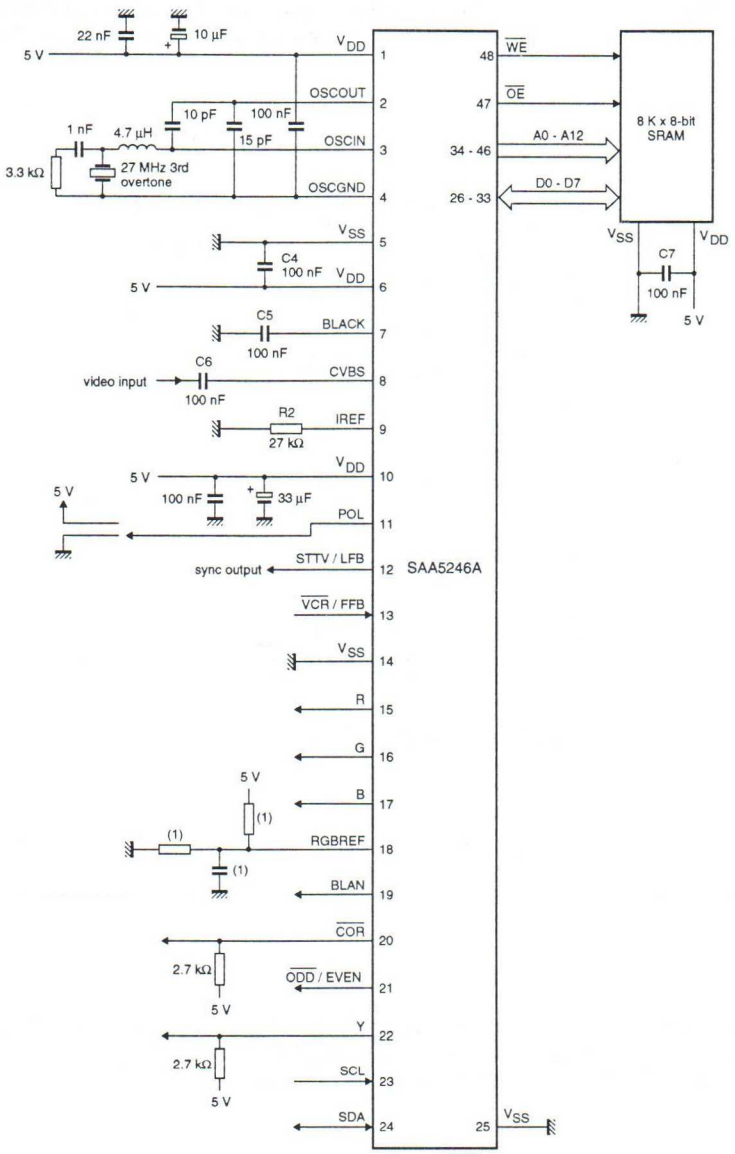
Fig.8 ODD/EVEN timing.



_ _ _ _ Level during flicker stopped cycle.

Fig.9 Memory interface timing (a) read (b) write.

APPLICATION INFORMATION



(1) Value dependent on application

Fig.10 Application diagram (SOT240).

SAA5246A page memory organization

The organization of the page memory is illustrated by Fig.11. The SAA5246A provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; row 24 is the extra row available for software generated status messages and FLOF/FASTEXT prompt information.

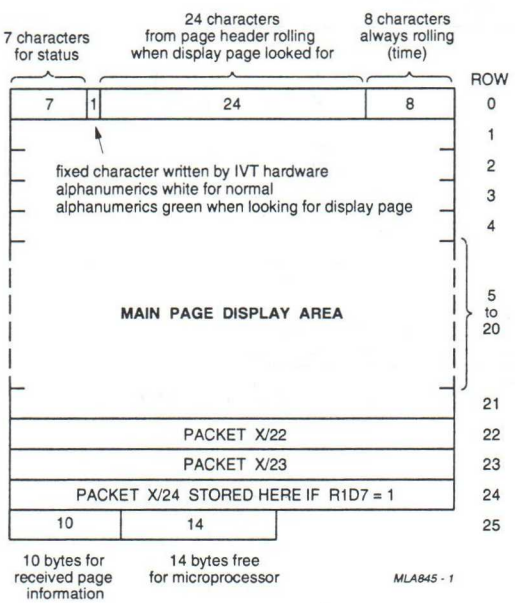


Fig.11 Basic page memory organization.

Note to Fig.11

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by SAA5246A to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of Row 25 contain control data relating to the received page as shown in Table 1. The remaining 14 bytes are free for use by the microprocessor.

Table 1 Row 25 received control data format.

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

Page number

MAG magazine

PU page units

PT page tens

PBLF page being looked for

$\overline{\text{FOUND}}$ LOW for page has been found

HAM.ER Hamming error in corresponding byte

Page sub-code

MU minutes units

MT minutes tens

HU hours units

HT hours tens

C4-C14 transmitted control bits.

When in extension packet enabled mode the rows of information are organized as illustrated by Fig.12.

Row 23 of the extension page, as shown in Fig.12, contains packet 8/30. Packet 8/30 is mapped into the SAA5246A memory as follows:

8/30/0 and 8/30/1 to Chapter 4 Row 23
8/30/2 and 8/30/3 to Chapter 5 Row 23
8/30/4 to 8/30/15 to Chapter 6 Row 23

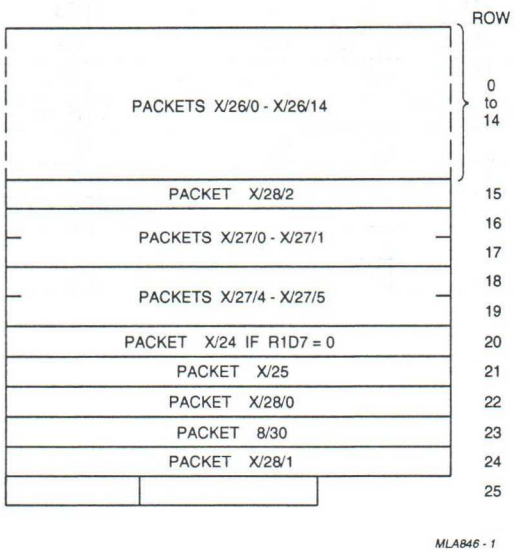


Fig.12 Organization of the extension memory.

Register maps

SAA5246A mode registers R0 to R11 are shown in Table 2. R0 to R10 are WRITE only; R11 is READ/WRITE; R11B is READ only. Register map (R3), for page requests, is shown in detail in Table 4.

Table 2 Register map.

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Adv. control	0	X24 POS	FREE RUN PLL	AUTO $\overline{\text{ODD}}$/EVEN	DISABLE HDR ROLL	–	DISABLE $\overline{\text{ODD}}$/EVEN	VCR MODE	$\overline{\text{R11}}$/R11B SELECT
Mode	1	VCS TO SCS	$\overline{7+P}$/ 8-BIT	ACQ $\overline{\text{ON}}$/OFF	EXT. PACKET ENABLE	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON FFB MODE	T1	T0
Page request address	2	HAM. CHECK	BANK SELECT A2	ACQ CIRCUIT A1	ACQ CIRCUIT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
Display chapter	4	–	–	–	–	–	A2	A1	A0
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS TOP	CURSOR ON	REVEAL ON	BOTTOM HALF	DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
Active chapter	8	–	–	–	–	CLEAR MEM.	A2	A1	A0
Cursor row	9	–	–	–	R4	R3	R2	R1	R0
Cursor column	10	–	–	C5	C4	C3	C2	C1	C0
Cursor data	11	D7	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{625}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	DATA QUALITY	VCS SIGNAL QUALITY

Where:

'–' Indicates a bit which does not exist and must be written to logic 0 for future compatibility.

Notes to Table 2

1. All bits in registers R0 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R1, R5 and R6 which are set to logic 1.
2. All memory is cleared to 'space' (00100000) on power-up, except Row 0 Column 7 Chapter 0, which is 'alpha' white (00000111) as the acquisition circuit is enabled but the page is on hold.
3. TB must be set to logic 0 for normal operation.
4. The I^2C-bus slave address is 0010001.

Register description

R0 ADVANCED CONTROL - auto increments to Register 1

R11/R11B SELECT	Selects reading of R11 or R11B
VCR MODE	Selects short time constant of PLL when logic 1
DISABLE $\overline{\text{ODD}}$/EVEN	Forces $\overline{\text{ODD}}$/EVEN output LOW when logic 1
DISABLE HDR ROLL	Disables green rolling header and time
AUTO $\overline{\text{ODD}}$/EVEN	When set forces $\overline{\text{ODD}}$/EVEN low if any TV picture displayed, if DISABLE $\overline{\text{ODD}}$/EVEN = 0
FREE RUN PLL	Will force the PLL to free run in all conditions
X24 POS	Automatic display of FASTEXT prompt row when logic 1

R1 MODE - auto increments to Register 2

T0, T1	Interlace/non-interlace 312/313 line control (see Table 4)
TCS ON FFB MODE	Text composite sync or direct sync select (see Table 4 for FFB mode selection)
$\overline{\text{DEW}}$/FULL FIELD	Field-flyback or full channel mode
EXT. PACKET ENABLE	Allocates 2K bytes memory per chapter
ACQ $\overline{\text{ON}}$/OFF	Aquisition circuits turned off when logic 1
$\overline{7+\text{P}}$/8-BIT	7 bits with parity checking or 8-bit mode
VCS TO SCS	When logic 1 enables display of messages with 60 Hz input signal

R2 PAGE REQUEST ADDRESS - auto increments to Register 3

HAM. CHECK	When logic 1 enables Hamming 8/4 checking of extension packet 27/0, 27/1 and 8/30/x
COL SC0 - SC2	Point to start column for page request data (see Table 3)
TB	Must be logic 0 for normal operation
ACQ CIRCUIT	Selects one of four acquisition circuits
BANK SELECT	Selects which bank of four chapters is being accessed, when EXT. PACKET ENABLE = 0

R3 PAGE REQUEST DATA - does not auto increment (see Table 3)

R4 DISPLAY CHAPTER - auto increments to Register 5

determines which of the 8 pages is displayed

R5 NORMAL DISPLAY CONTROL - auto increments to Register 6

PON	Picture on
TEXT	Text on
COR	Contrast reduction on
BKGND	Background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R6 NEWSFLASH DISPLAY - auto increments to Register 7

PON	Picture on
TEXT	Text on
COR	Contrast reduction on
BKGND	Background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 DISPLAY MODE - does not auto increment

BOX ON 0	Boxing function allowed on Row 0
BOX ON 1-23	Boxing function allowed on Row 1-23
BOX ON 24	Boxing function allowed on Row 24
DOUBLE HEIGHT	To display double height text
BOTTOM HALF	To select bottom half of page when DOUBLE HEIGHT = 1
REVEAL ON	To reveal concealed text
CURSOR ON	To display cursor
STATUS TOP	Row 25 displayed above or below the main text

R8 ACTIVE CHAPTER - auto increments to Register 9

A0 to A2	Active chapter
CLEAR MEMORY	When set to 1, clears the display memory. This bit is automatically reset

R9 CURSOR ROW - auto increments to Register 10

R0 to R4	Active row for data written to or read from memory via the I²C-bus

R10 CURSOR COLUMN - auto increments to Register 11 or 11B

C0 to C5	Active column for data written to or read from memory via the I²C-bus

R11 CURSOR DATA - does not auto increment

D0 to D7	Data read from/written to memory via I²C, at location pointed to by R8, R9 and R10. This location automatically increments each time R11 is accessed

R11B DEVICE STATUS - does not auto increment

VCS SIGNAL QUALITY	Indicates that the video signal quality is good and PLL is phase locked to input video when = 1
DATA QUALITY	If good Teletext data is detected then = 1
ROM VER R0 to R4	Indicated language/ROM variant. See Table 6
$\overline{625}$/525 SYNC	If the input video is a 525 line signal when = 1

Table 3 Register map for page requests (R3).

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

1. Abbreviations are as for Table 1 except for DO CARE bits.
2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
3. If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
4. Columns auto-increment on successive I²C-bus transmission bytes.
5. 'X' = Don't care.

Table 4 Interlace/non-interlace 312/313 line control and ODD/EVEN field detection option.

TCS ON FFB MODE	T1	T0	RESULT
x	0	0	interlaced 312.5/312.5 lines
x	0	1	non-interlaced 312/313 lines (note 1)
x	1	0	non-interlaced 312/312 lines (note 1)
0	1	1	SCS (scan composite sync) mode: FFB leading edge in first broad pulse of field M7 version onwards
1	1	1	SCS (scan composite sync) mode: FFB leading edge in second broad pulse of field M7 version onwards

Notes to Table 4

1 Reverts to interlaced mode if a newsflash or subtitle is being displayed.

2. 'x' = Don't care.

CLOCK SYSTEMS

Crystal oscillator

The oscillator is a low amplitude, low distortion design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone as illustrated in Fig.13.

Table 5 Crystal characteristics.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)					
C1	series capacitance	–	1.7	–	pF
C0	parallel capacitance	–	5.2	–	pF
C_L	load capacitance	–	20	–	pF
Rr	resonant resistance	–	–	50	Ω
R1	series resistance	–	20	–	Ω
Xa	ageing	–	–	±5	10^{-6}/yr
Xj	adjustment tolerance	–	–	±25	10^{-6}
Xd	drift	–	–	±25	10^{-6}

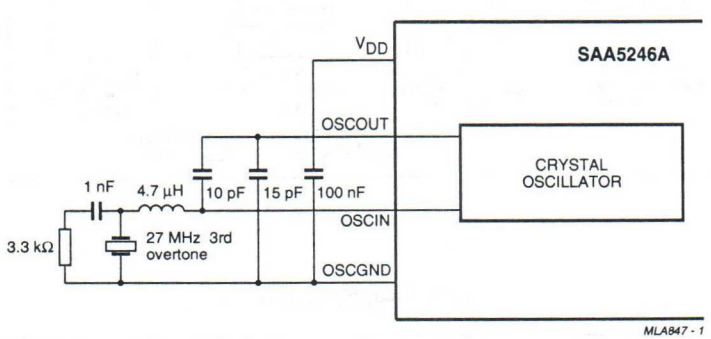


Fig.13 Crystal oscillator application diagram.

Character sets

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character sets differ only in 13 national option characters as indicated in Table 8 with reference to their table position in the basic character matrix illustrated in Table 7. The SAA5246A automatically decodes transmission bits C12 to C14. Table 6 illustrates the character matrixs.

Character bytes are listed as transmitted from b1 to b7.

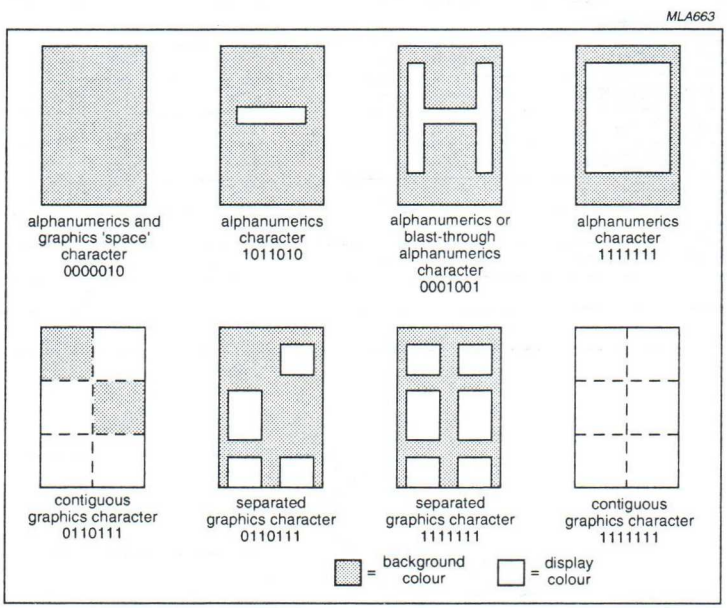
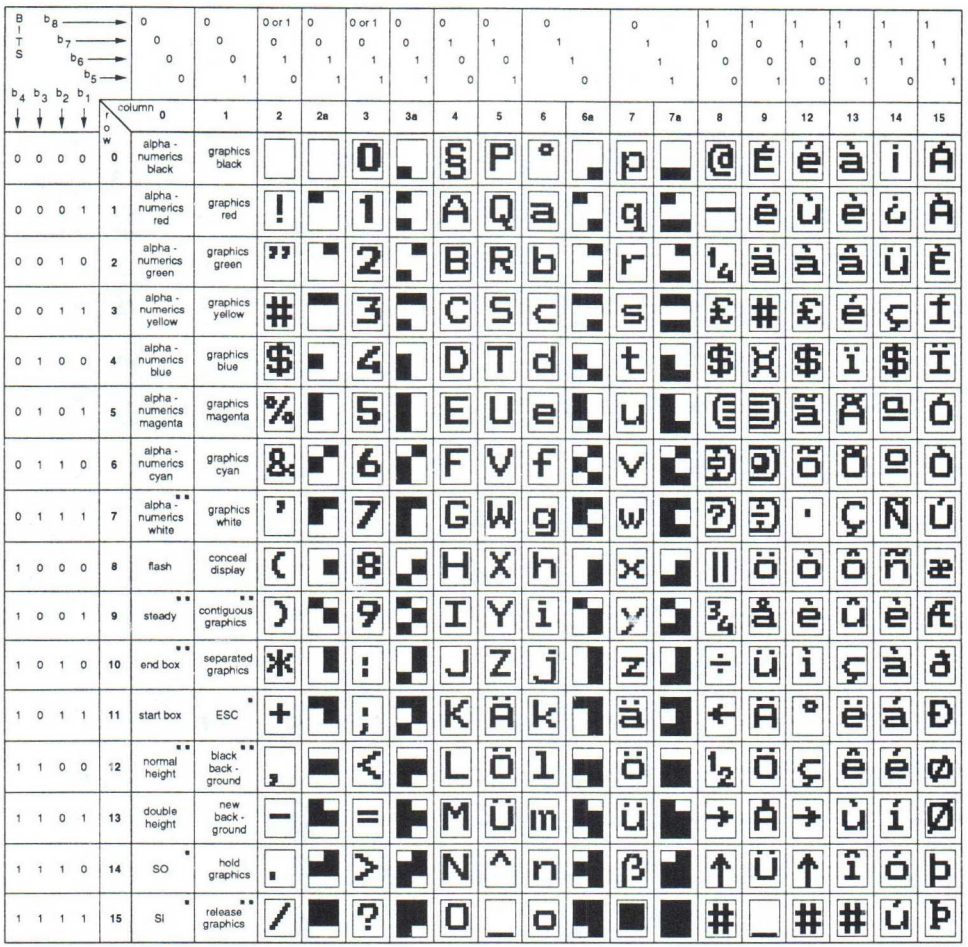


Fig.14 Character format.

Table 6a SAA5246AP/E character data input decoding, West European languages.

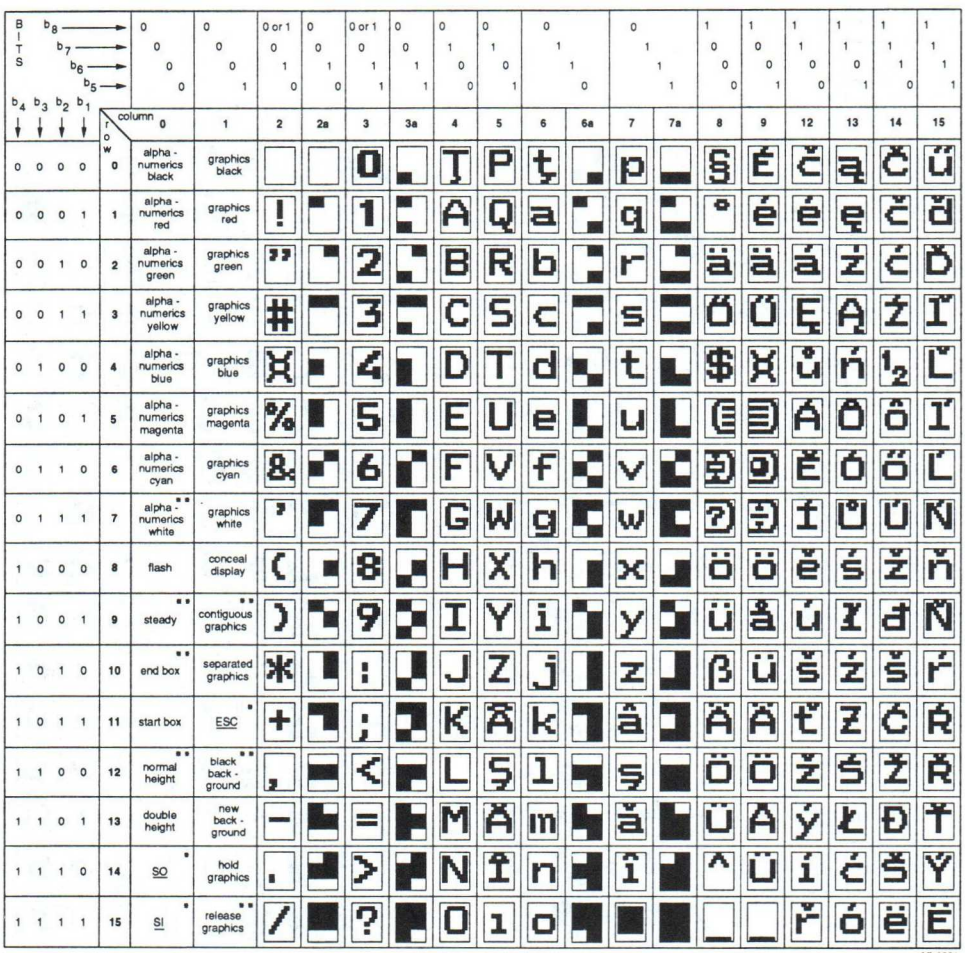


For character version number (00000) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 6b SAA5246AP/H character data input decoding, East European languages.



For character version number (00001) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 6c SAA5246AP/T character data input decoding, West European and Turkish languages.

BITS b_4 b_3 b_2 b_1	row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha - numerics black	graphics black			0		§	P	°		p		@	İ	é	à	i	Á
0 0 0 1	1	alpha - numerics red	graphics red	!		1		A	Q	a		q		—	ı	ù	è	¿	À
0 0 1 0	2	alpha - numerics green	graphics green	"		2		B	R	b		r		¼	ş	à	â	ü	È
0 0 1 1	3	alpha - numerics yellow	graphics yellow	#		3		C	S	c		s		£	Ł	£	é	ç	Ł
0 1 0 0	4	alpha - numerics blue	graphics blue	$		4		D	T	d		t		$	ğ	$	ï	$	Ï
0 1 0 1	5	alpha - numerics magenta	graphics magenta	%		5		E	U	e		u		⟨	⟩	ã	Ã	ª	ó
0 1 1 0	6	alpha - numerics cyan	graphics cyan	&		6		F	V	f		v		⟩	⟩	õ	Õ	º	Ò
0 1 1 1	7	alpha - numerics white **	graphics white	'		7		G	W	g		w		?	÷	·	Ç	Ñ	Ú
1 0 0 0	8	flash	conceal display	(		8		H	X	h		x		‖	ö	ò	ô	ñ	Ł
1 0 0 1	9	steady **	contiguous graphics **	)		9		I	Y	i		y		¾	ç	è	û	è	Ù
1 0 1 0	10	end box **	separated graphics	*		:		J	Z	j		z		÷	ü	ì	ç	à	↓
1 0 1 1	11	start box	ESC *	+		;		K	Ä	k		ä		←	Ş	°	ë	á	É
1 1 0 0	12	normal height **	black back - ground **	,		<		L	Ö	l		ö		½	Ö	ç	ê	é	ä
1 1 0 1	13	double height	new back - ground	−		=		M	Ü	m		ü		→	Ç	→	ù	í	Ô
1 1 1 0	14	SO *	hold graphics	.		>		N	^	n		ß		↑	Ü	↑	î	ó	Ã
1 1 1 1	15	SI *	release graphics **	/		?		O	_	o				#	Ğ	#	#	ú	Ł

MBA431

For character version number (00010) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 6d SAA5246AP/J character data input decoding, Jugoslav languages

B I T S b_4 b_3 b_2 b_1	row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
b_8		0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7		0	0	0	0	0	0	1	1	1		1		0	0	1	1	1	1
b_6		0	0	1	1	1	1	0	0	1		1		0	0	0	0	1	1
b_5		0	1	0	1	1	1	0	1	0		1		0	1	0	1	0	1
0 0 0 0	0	alpha - numerics black	graphics black																
0 0 0 1	1	alpha - numerics red	graphics red																
0 0 1 0	2	alpha - numerics green	graphics green																
0 0 1 1	3	alpha - numerics yellow	graphics yellow																
0 1 0 0	4	alpha - numerics blue	graphics blue																
0 1 0 1	5	alpha - numerics magenta	graphics magenta																
0 1 1 0	6	alpha - numerics cyan	graphics cyan																
0 1 1 1	7	alpha - numerics white **	graphics white																
1 0 0 0	8	flash	conceal display																
1 0 0 1	9	steady **	contiguous graphics **																
1 0 1 0	10	end box **	separated graphics																
1 0 1 1	11	start box	ESC *																
1 1 0 0	12	normal height **	black back - ground **																
1 1 0 1	13	double height	new back - ground																
1 1 1 0	14	SO *	hold graphics																
1 1 1 1	15	SI *	release graphics **																

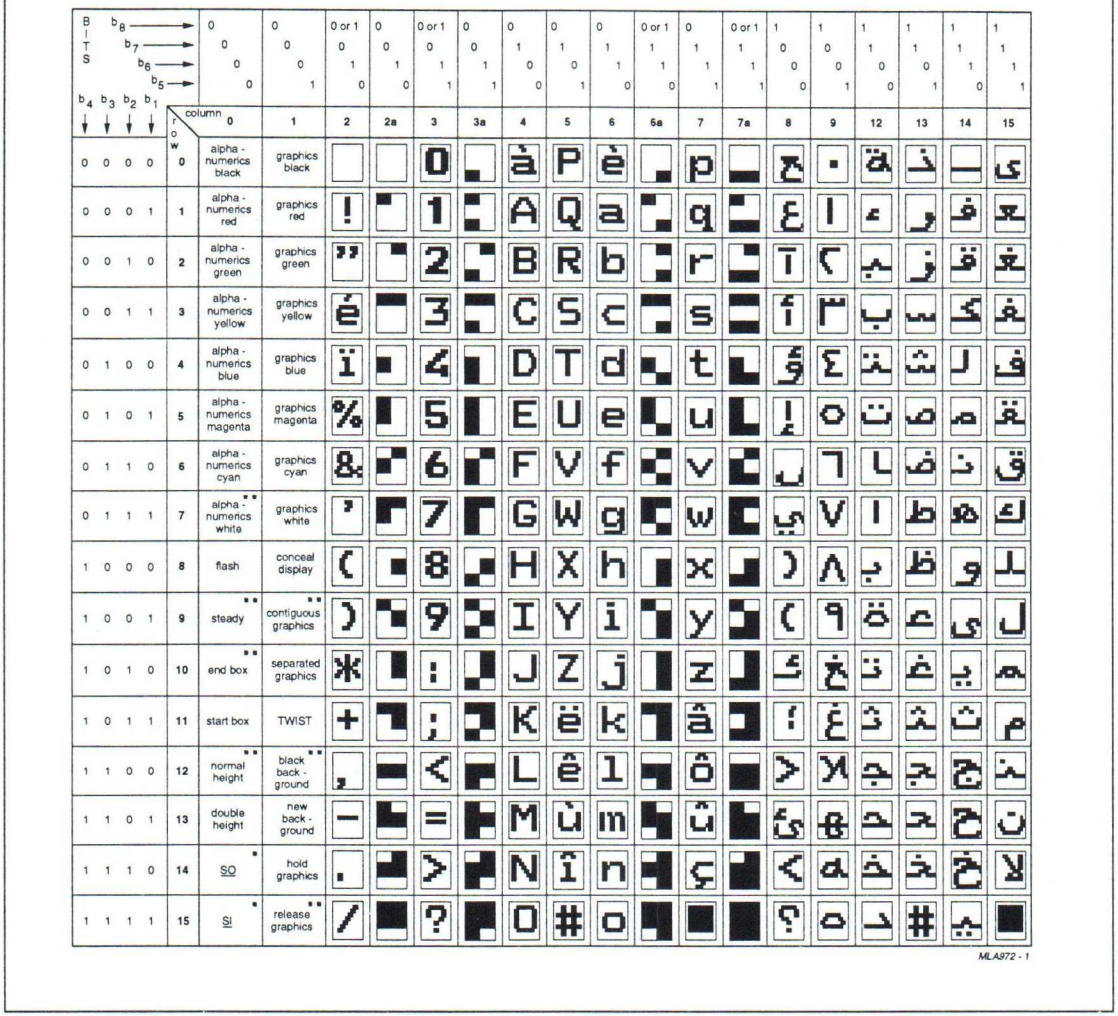
MLA962

For character version number (00011) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 6e SAA5246AP/K character data input decoding, French and Arabic languages.



For character version number (00100) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 6f SAA5246AP/L character data input decoding, Arabic and Hebrew languages.

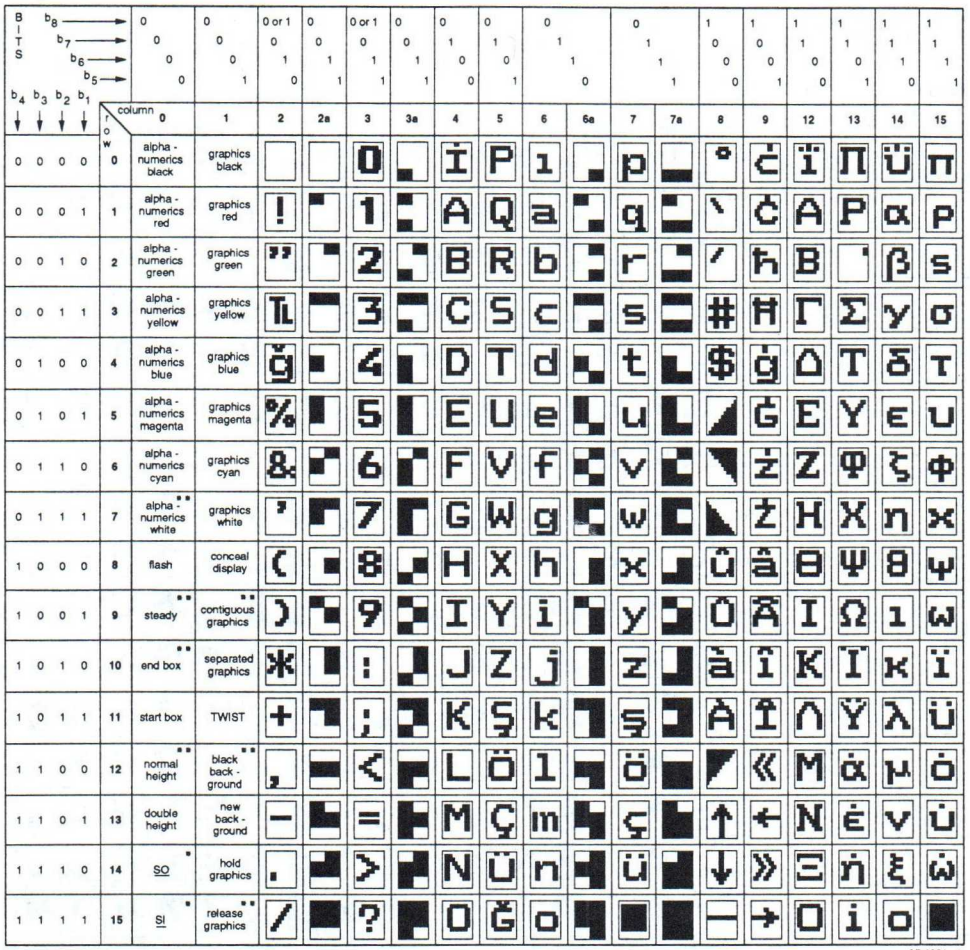


For character version number (00100) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 6h SAA5246AP/I character data input decoding, Greek and Turkish languages.

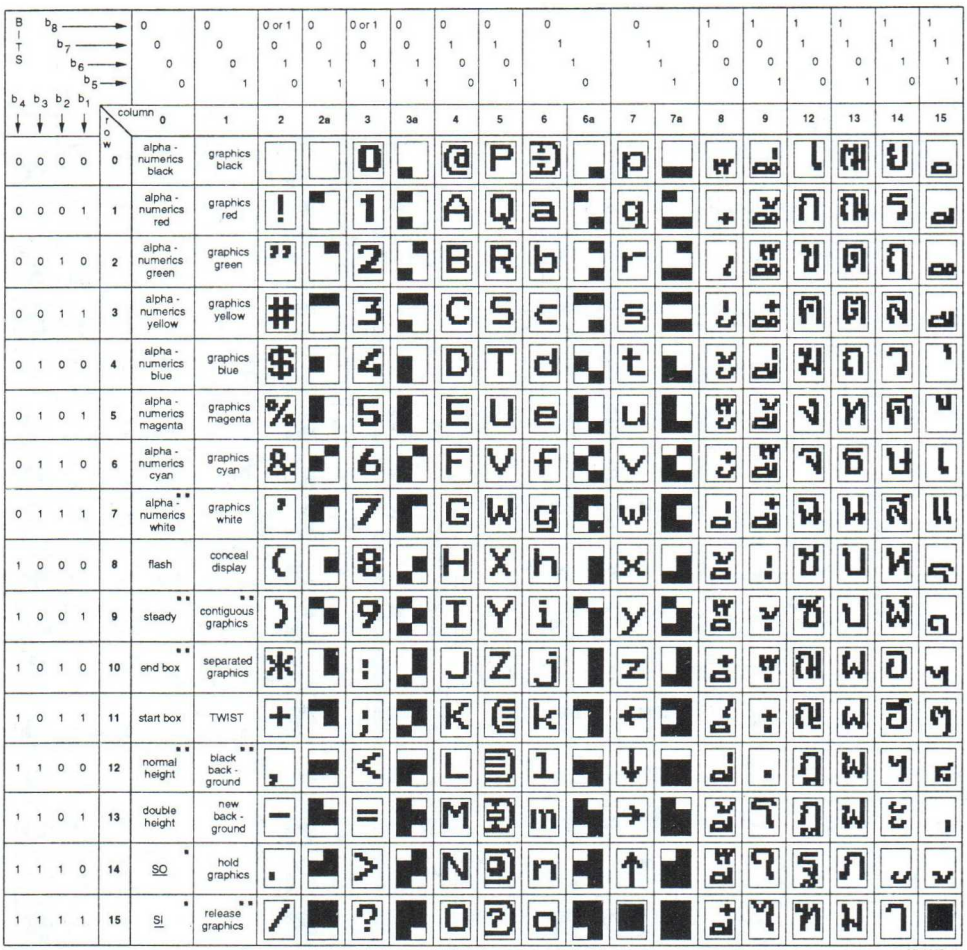


For character version number (00110) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 6i SAA5246AP/S character data input decoding, English and Thai languages.



For character version number (00111) see Register 11B.

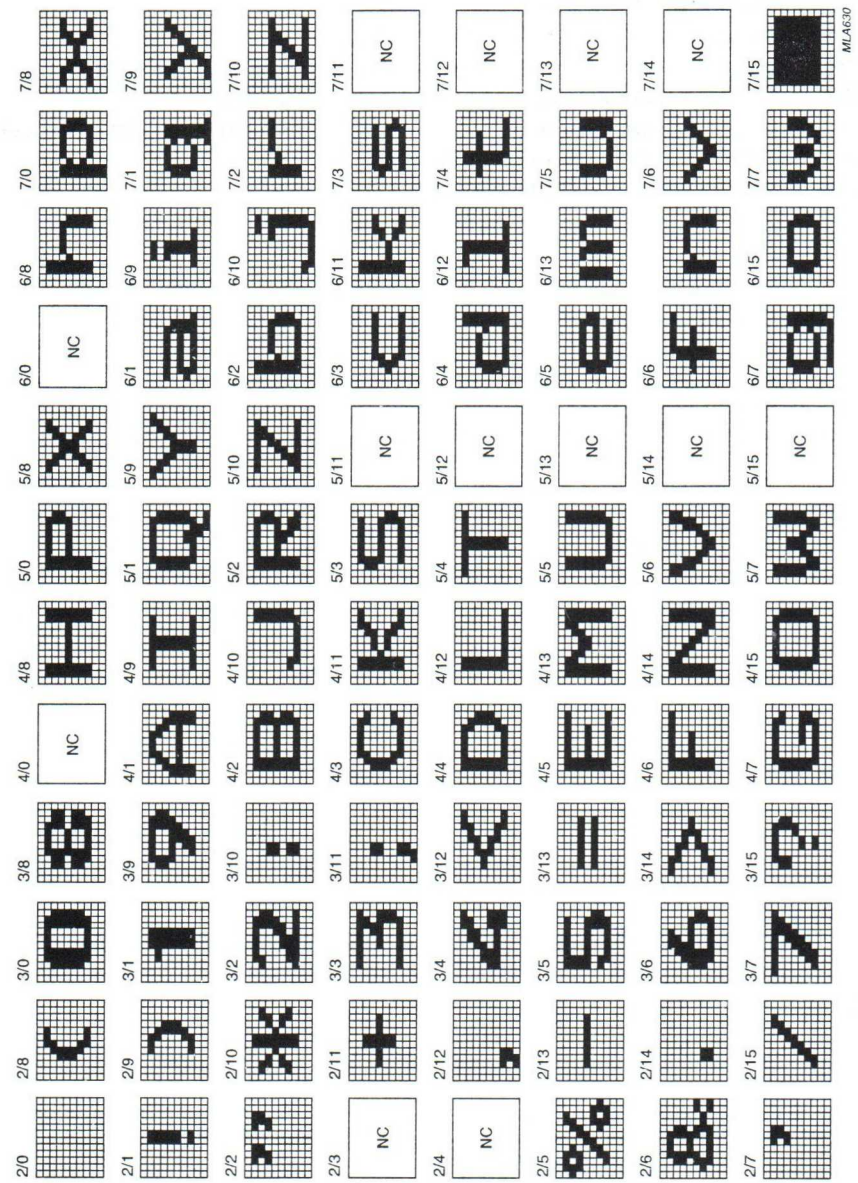
* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Notes to Table 6

1. Control characters shown in Columns 0 and 1 are normally displayed as spaces.
2. Characters may be referred to by column and row, For example 2/5 refers to %.
3. Black represents displayed colour. White represents backgound.
4. The SAA5246A national option characters are illustrated in Table 8.
5. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters for combining with character 8/5 (E, H and T codes only. Characters 5/12, 5/13, 5/14 and 5/15 are combined with 5/11 (S code only).
6. National option characters will be displayed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Table 8.
7. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.

Table 7 SAA5246A basic character matrix.



Where: NC = national option character position.

Table 8a SAA5246AP/E national option character set.

LANGUAGE	PHCB [1]			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MEA559

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

Table 8b SAA5246AP/H national option character set.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
POLISH	0	0	0	#	ń	ą	Ź	Ś	Ł	ć	ó	ę	ż	ś	ł	ź
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
SERBO-CROAT	1	0	1	#	½	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CAECHOSLOVAK	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN	1	1	1	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

MLA966

(1) PHCB are the Page Header Control Bits. Other combinations default to German. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 7.

Table 8c SAA5246AP/T national option character set.

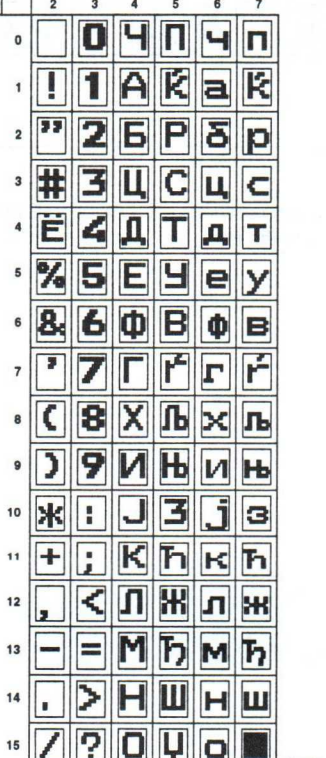
LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)													
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
TURKISH	1	1	0	Ţ	ğ	İ	Ş	Ö	Ç	Ü	Ğ	ı	ş	ö	ç	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MBA430

(1) PHCB are the Page Header Control Bits. Other combinations default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 7.

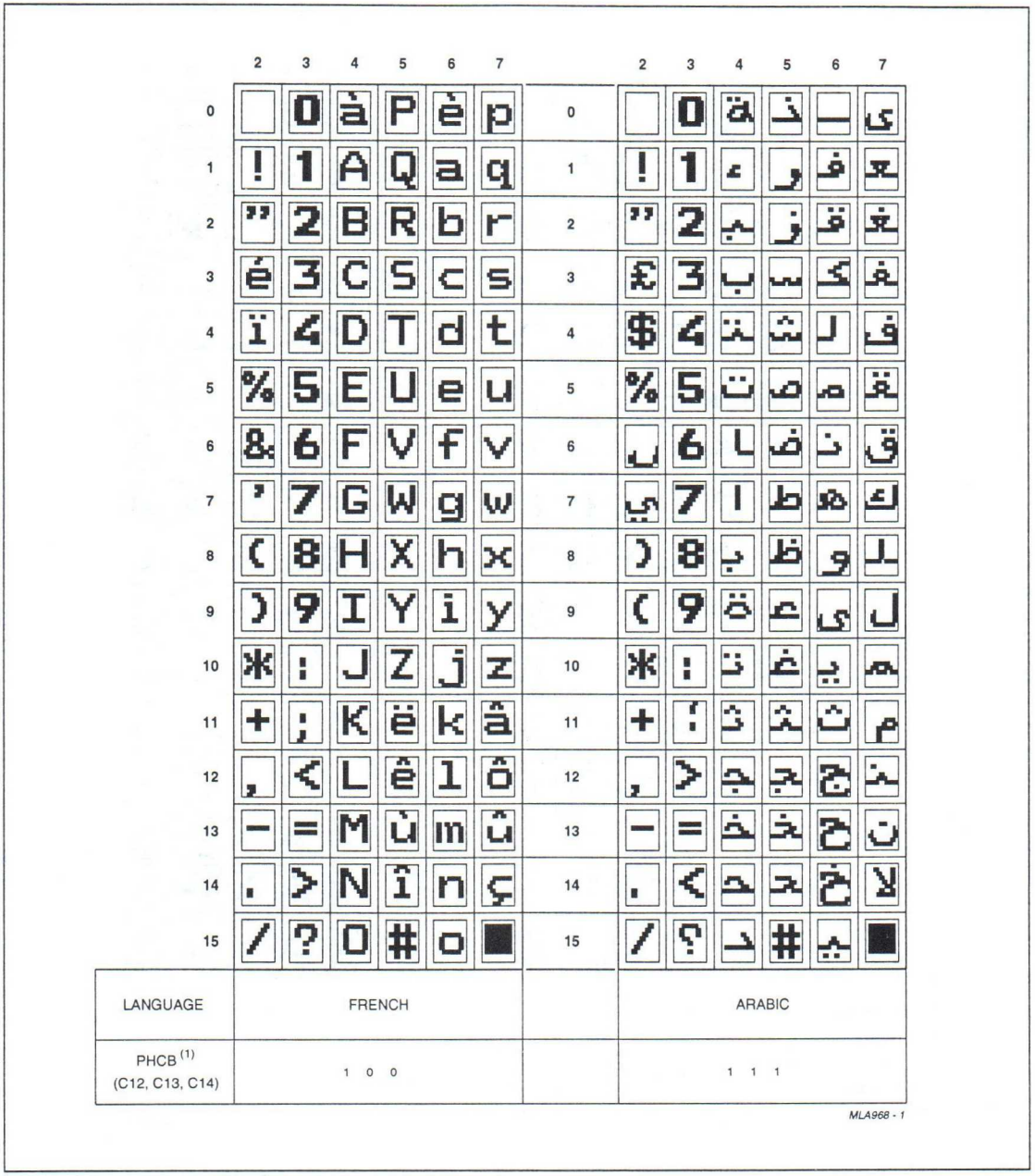
Table 8d SAA5246AP/J national option character set.

LANGUAGE	PHCB[1]			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
SERBO-CROAT LATIN	0	1	0	#	Ë	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
SERBO-CROAT LATIN	0	1	1	#	Ë	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
HUNGARIAN SWEDISH	0	1	1	#	$	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
SERBO-CROAT LATIN	0	1	1	#	Ë	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
SERBO-CROAT	0	1	1	#	Ë	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
(RUMANIAN)	0	1	1	#	$	Ţ	Ă	Ş	Â	Î	ı	ţ	â	ş	ă	î
RUMANIAN	0	1	1	#	$	Ţ	Ă	Ş	Â	Î	ı	ţ	â	ş	ă	î
SERBO-CROATIC CYRILLIC	1	0	0													



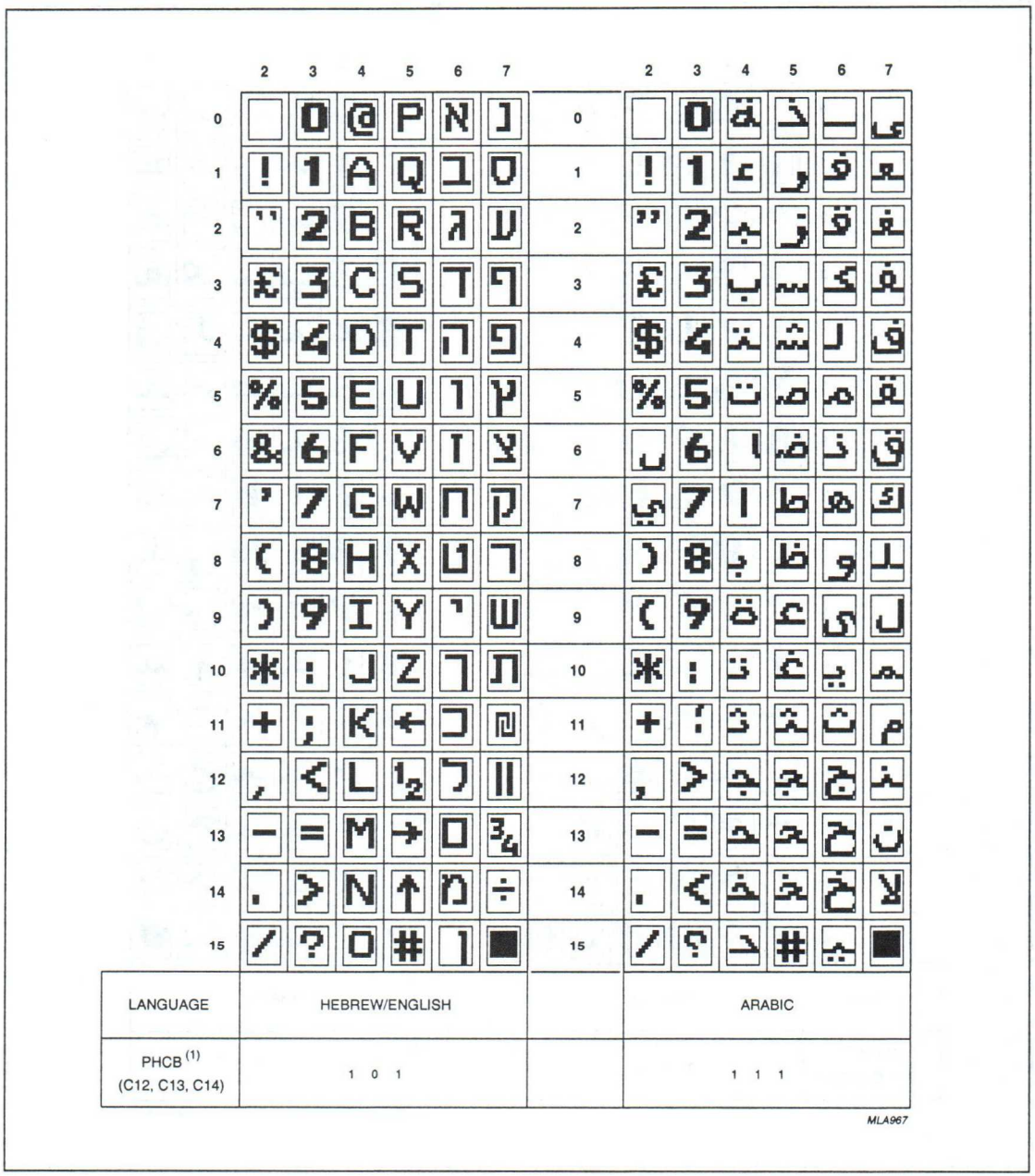
(1) PHCB are the Page Header Control Bits. Other combinations default to Serbo-Croat Latin.

Table 8e SAA5246AP/K national option character set.



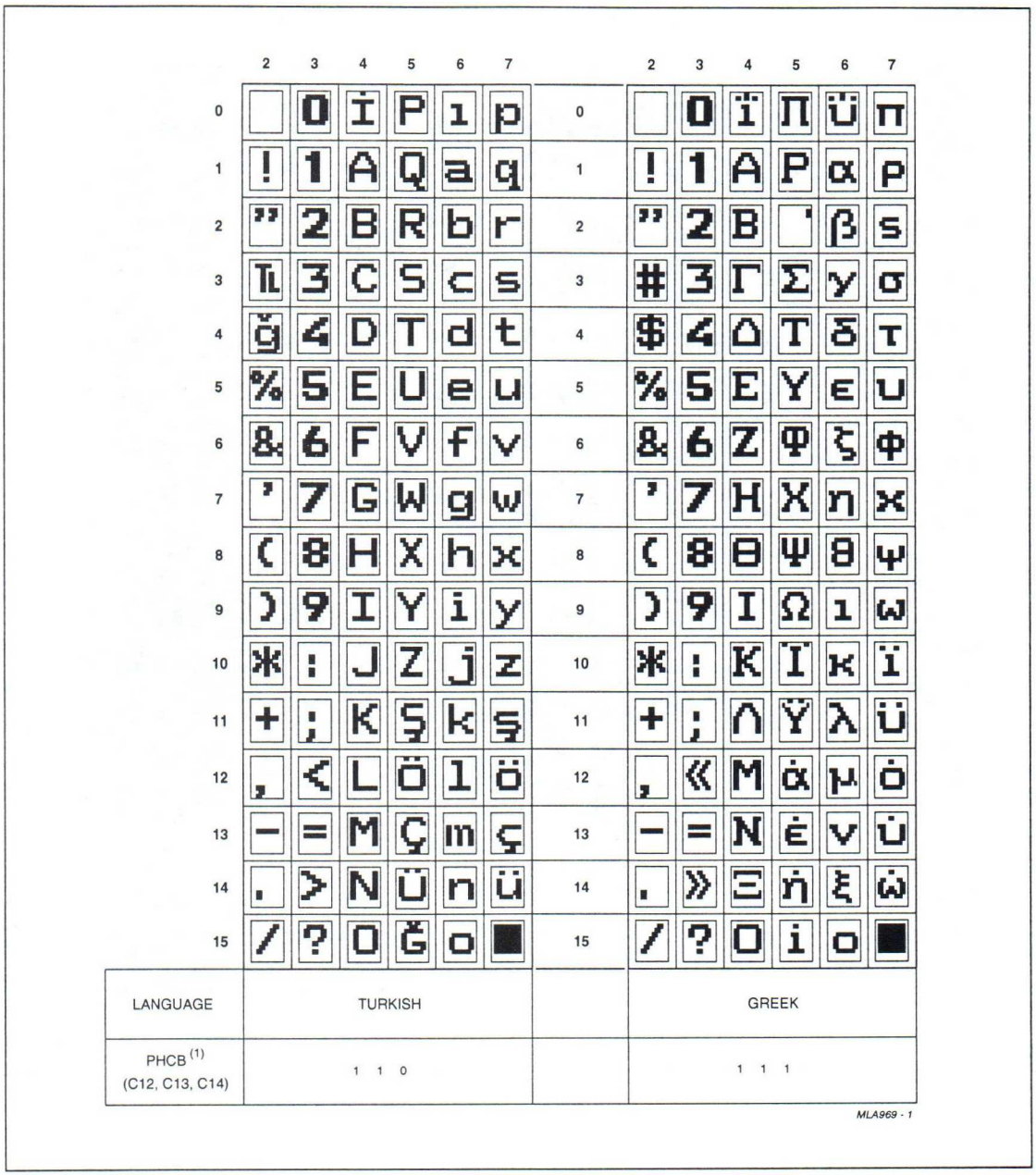
(1) PHCB are the Page Header Control Bits. Other combinations default to French.

Table 8f SAA5246AP/L national option character set.



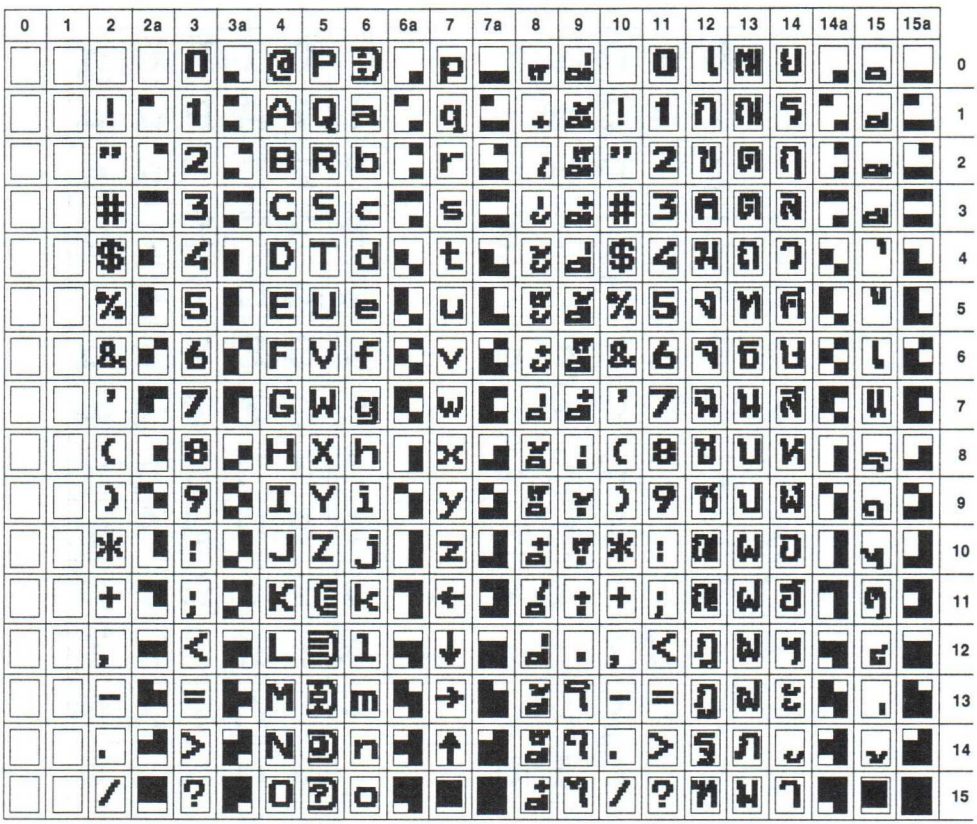
(1) PHCB are the Page Header Control Bits. Other combinations default to Hebrew English.

Table 8h SAA5246AP/I national option character set.



(1) PHCB are the Page Header Control Bits. Other combinations default to Turkish.

Table 8i SAA5246AP/S national option character set (part A).



English (0 0 0) TWIST not invoked	PHCB (1) (C_{12}, C_{13}, C_{14})
OR	
Thai (0 1 0) and TWIST invoked	PHCB (1) (C_{12}, C_{13}, C_{14})

MLA971a

Table 8i SAA5246AP/S national option character set (part B).



(1) PHCB are the Page Header Control Bits. Other combinations default to English.

Integrated VIP and Teletext with Background Memory Controller (IVT1.1BMC)

SAA5247

FEATURES

- Complete background memory controller enabling storage of up to 512 teletext pages in external RAM
- Interfaces to either one 256 K x 4 DRAM, two 256 K x 4 DRAMs or 1 M x 4 DRAM, pin programmable
- Fast background memory scan. Maximum access time to any one of 512 pages = 0.2 s
- Single +5 V power supply
- Digital data slicer and display clock phase-locked loop reduce peripheral components to a minimum
- Both video and scan related synchronization modes are supported
- On board single page memory including extension packets for FASTEXT
- Single page acquisition system
- RGB interface to standard colour decoder ICs, push-pull output drive
- Data capture performance similar to SAA5231 (VIP2)
- Simple software control via I²C-bus and software compatible with SAA5244 (IVT1.1)
- Options for five national languages
- 32 supplementary characters for on-screen displays
- Optional storage of packet 24 in the display memory
- Page links in packets 27 and 8/30 are Hamming decoded
- Separate text and video signal quality detectors, 625/525 video status and language version all readable via I²C-bus
- Automatic ODD/$\overline{\text{EVEN}}$ output control with manual override
- Control of display PLL free-run and rolling header via I²C-bus
- VCS to SCS mode for stable 525 line status display

DESCRIPTION

The Integrated VIP and Teletext (IVT1.1BMC) is a teletext decoder (contained within a single chip package) for decoding 625-line based World System Teletext transmissions, with in-built background memory controller for direct storage of all incoming teletext transmissions. The BMC can store up to 512 teletext pages in external DRAMs; this is rapidly scanned on each page request, thereby giving near instant page access. The teletext decoder is based on the IVT1.1 device (SAA5244) and is designed to be software compatible. The pins are arranged so that one PCB can take either an IVT1.1 or IVT1.1BMC. The Video Input Processor (VIP) section of the device uses mixed analog and digital designs for the data slicer and the display clock phase-locked loop functions. As a result the number of external components is greatly reduced and no critical or adjustable components are required. A single page static RAM is incorporated in the device thereby giving a genuine single-chip teletext decoder device.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5247P/B	48	DIL	plastic	SOT240
SAA5247GP/B	64	QFP	plastic	SOT208

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	90	180	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1.0	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature range	–20	–	+70	°C

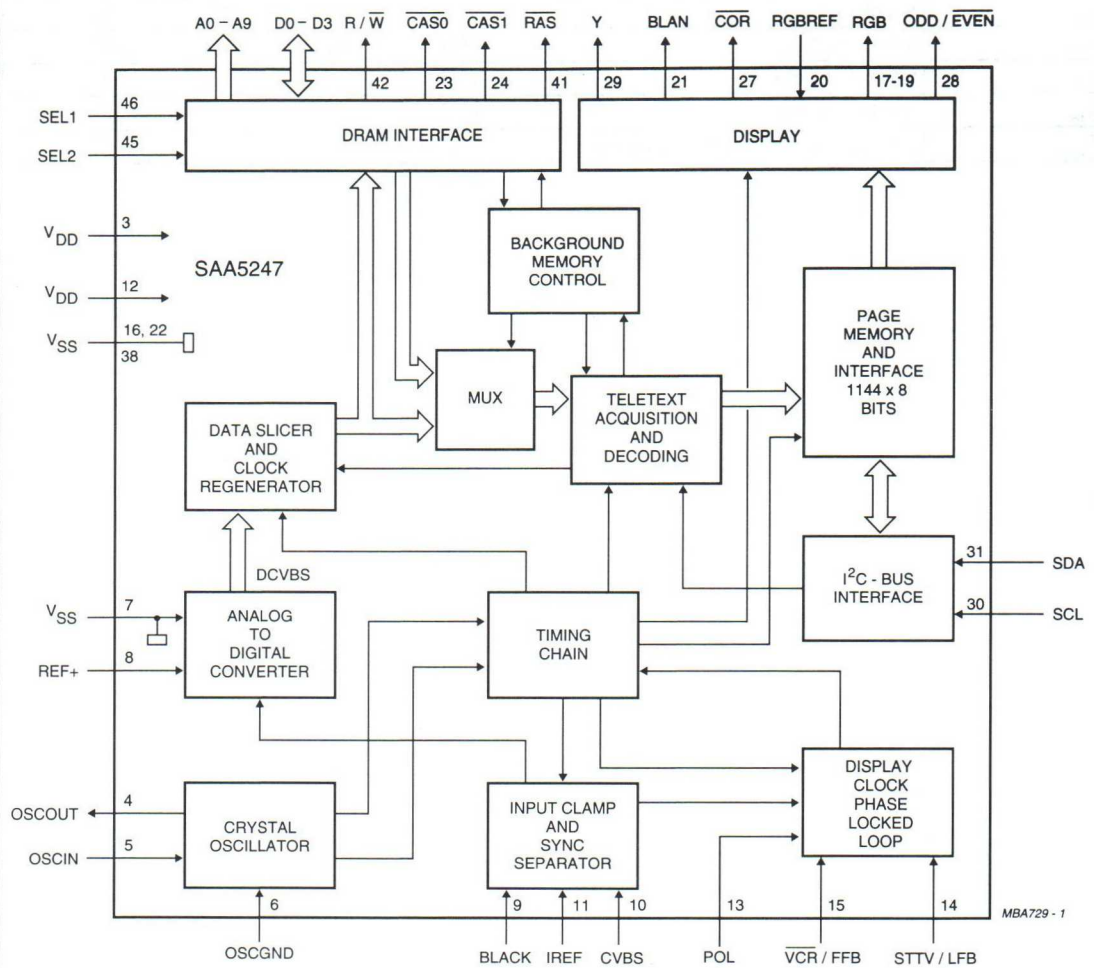


Fig.1 Block diagram for SOT240 (DIL48) package.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT240	SOT208	
n.c.	1	1	not connected
n.c.	2	2	not connected
V_{DD}	3	25	+5 V supply
OSCOUT	4	27	27 MHz crystal oscillator output
OSCIN	5	28	27 MHz crystal oscillator input
OSCGND	6	29	0 V crystal oscillator ground
V_{SS}	7	12	0 V ground
REF+	8	32	positive reference voltage. The pin should be connected to +5 V supply
BLACK	9	35	video black level storage pin, connected to ground via a 100 nF capacitor
CVBS	10	36	composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor
IREF	11	37	reference current input pin, connected to ground via a 27 kΩ resistor
V_{DD}	12	38	+5 V supply
POL	13	39	STTV/LFB/FFB polarity selection pin
STTV/LFB	14	40	sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode)
$\overline{VCR}$/FFB	15	42	PLL time constant switch/field input pin. Function controlled by an internal register bit (scan sync mode)
V_{SS}	16	30	0 V ground
REF–	–	31	negative reference voltage; this pin should be connected to REF+ via a 100 nF capacitor
R	17	49	dot rate character output of the RED colour information
G	18	50	dot rate character output of the GREEN colour information
B	19	51	dot rate character output of the BLUE colour information
RGBREF	20	52	input DC voltage to define the output high level on the RGB pins
BLAN	21	53	dot rate fast blanking output
V_{SS}	22	54, 55	0 V ground
$\overline{CAS0}$	23	56	column address select to external DRAM for BMC function
$\overline{CAS1}$	24	57	column address select to external DRAM for BMC function for second DRAM where two 256 k x 4 devices are used
A4	25	58	address output to external DRAM for BMC function
A3	26	59	address output to external DRAM for BMC function
$\overline{COR}$	27	60	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open drain output
ODD/$\overline{EVEN}$	28	61	25 Hz output synchronized with the CVBS input's field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents
Y	29	62	dot rate character output of teletext foreground colour information. Open drain output

SYMBOL	PIN		DESCRIPTION
	SOT240	SOT208	
SCL	30	63	serial clock input for I²C-bus. It can still be driven HIGH during power-down of the device
SDA	31	64	serial data port for the I²C-bus. Open drain output. It can still be driven HIGH during power-down of the device
A5	32	4	address output to external DRAM for BMC function
A2	33	5	address output to external DRAM for BMC function
A6	34	6	address output to external DRAM for BMC function
A1	35	8	address output to external DRAM for BMC function
A7	36	9	address output to external DRAM for BMC function
A0	37	11	address output to external DRAM for BMC function
V_{SS}	38	43	0 V ground
A8	39	13	address output to external DRAM for BMC function
A9	40	14	address output to external DRAM for BMC function
$\overline{RAS}$	41	15	row address select to external DRAM
R/$\overline{W}$	42	18	read/$\overline{write}$ for external DRAM
D2	43	19	data input/output for external DRAM
D0	44	20	data input/output for external DRAM
SEL2	45	21	RAM select input to choose external DRAM size
SEL1	46	22	RAM select input to choose external DRAM size
D3	47	23	data input/output for external DRAM
D1	48	24	data input/output for external DRAM

The remaining pins for SOT208 are not connected.

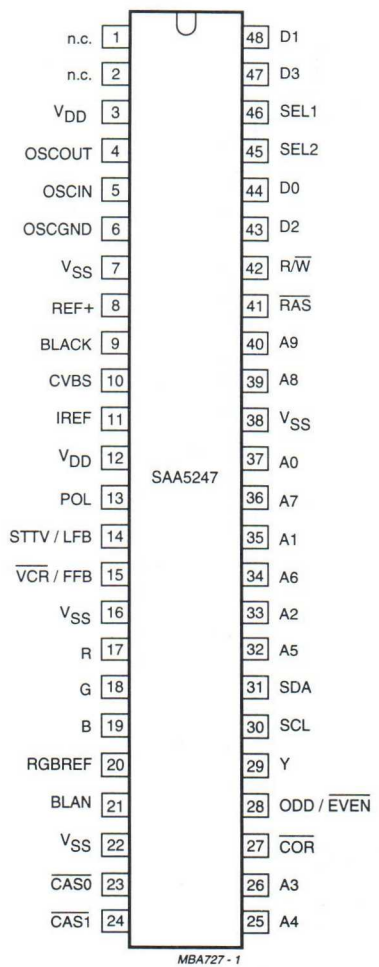


Fig.2 Pin configuration; SOT240 (DIL48).

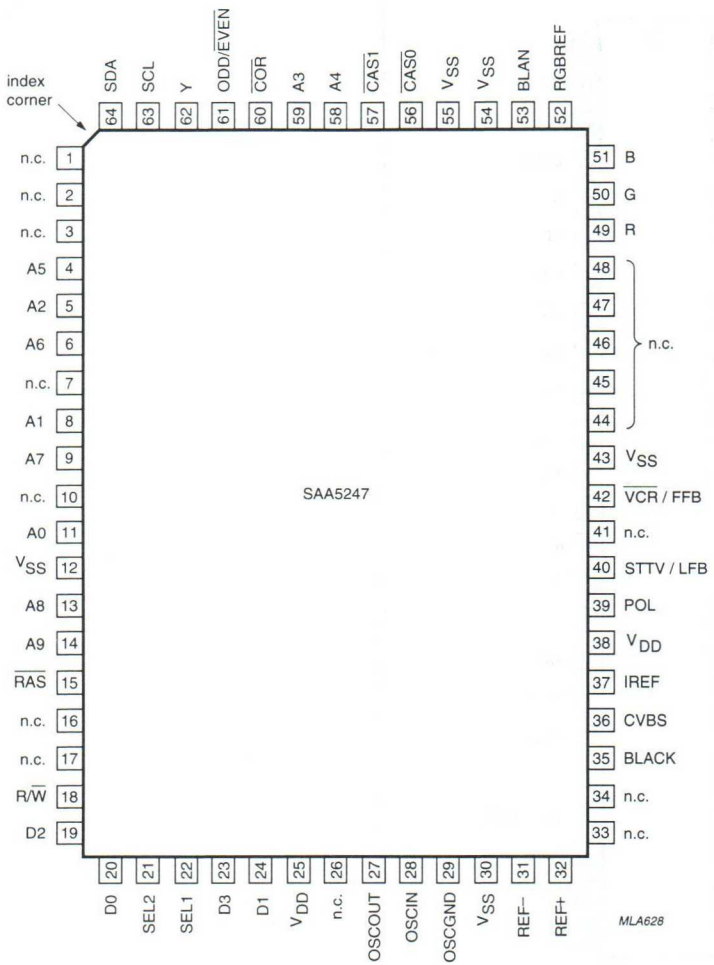


Fig.3 Pin configuration; SOT208 (QFP64).

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	−0.3	+6.5	V
V_I	input voltage (any input)	−0.3	V_{DD}+0.5	V
V_O	output voltage (any output)	−0.3	V_{DD}+0.5	V
V_{Sdiff}	difference between V_{SS} and OSCGND	−0.25	+0.25	V
V_{Ddiff}	difference between V_{DD} and REF+	−0.25	+0.25	V
I_O	output current (each output)	–	±10	mA
I_{IOK}	DC input or output diode current	–	±20	mA
T_{amb}	operating ambient temperature range	−20	+70	°C
T_{stg}	storage temperature range	−55	+125	°C
V_{stat}	electrostatic handling (see note)	−2000	+2000	V

Note

Electrostatic handling is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a 15 ns rise time.

Failure Rate

The failure rate at T_{amb} = 55 °C will be a maximum of 1000 FITS (1 FIT = 1 x 10^{-9} failures per hour).

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = –20 to +70 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage range		4.5	5	5.5	V
I_{DD}	total supply current		–	90	125	mA
Inputs						
CVBS						
V_{syn}	sync amplitude		0.1	0.3	0.6	V
t_{syn}	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		–150	0	150	ns
t_{syd}	change in sync delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{vid(p-p)}$	video input amplitude (peak-to-peak)		0.7	1.0	1.4	V
	display PLL catching range		±7	–	–	%
Z_{src}	source impedance		–	–	250	Ω
C_I	input capacitance		–	–	10	pF
IREF						
R_g	resistor to ground		–	27	–	kΩ
POL						
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
LFB						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
I_I	input current	note 1	–1	–	+1	mA
t_{LFB}	delay between LFB front edge and input video line sync		–	250	–	ns
$\overline{VCR}$/FFB						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
I_I	input current	note 1	–1	–	+1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
RGBREF (NOTE 2)						
V_{IL}	LOW level input voltage		−0.3	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
I_{DC}	DC current		–	–	10	mA
SEL1 AND SEL2						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
SCL						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
f_{SCL}	clock frequency		0	–	100	kHz
t_r	input rise time	10% to 90%	–	–	2	μs
t_f	input fall time	90% to 10%	–	–	2	μs
C_I	input capacitance		–	–	10	pF
Inputs/outputs						
CRYSTAL OSCILLATOR (OSCIN; OSCOUT)						
f_{XTAL}	crystal frequency		–	27	–	MHz
G_v	small signal voltage gain		3.5	–	–	–
G_m	mutual conductance	f = 100 kHz	1.5	–	–	mA/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	–	5	pF
BLACK						
C_{blk}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
SDA						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	10% to 90%	–	–	2	μs
t_f	input fall time	90% to 10%	–	–	2	μs
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	3 V to 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs/outputs						
D0 TO D3						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current		−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
t_r	output rise time	0.6 V to 2.2 V	–	–	20	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	20	ns
C_L	load capacitance		–	–	50	pF
Outputs						
STTV						
G_{stt}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{tcs}	TCS amplitude		0.2	0.3	0.45	V
V_{DCs}	DC shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive current		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
A0 TO A9 ADDRESS OUTPUT TO MEMORY						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.6 V to 2.2 V	–	–	20	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	20	ns
R/$\overline{W}$, $\overline{CAS0}$ AND $\overline{CAS1}$						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.6 V to 2.2 V	–	–	20	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
R, G AND B						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = –1.6 mA; RGBREF ≤ V_{DD}–2 V	RGBREF –0.25 V	RGBREF	RGBREF +0.25 V	V
$\|Z_o\|$	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
I_{DC}	DC current		–	–	–3.3	mA
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
BLAN						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA; V_{DD} = 4.5 V	1.1	–	–	V
V_{OH}	HIGH level output voltage	I_{OH} = 0 mA; V_{DD} = 5.5 V	–	–	2.8	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
ODD/$\overline{\text{EVEN}}$						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
$\overline{\text{COR}}$ AND Y (OPEN DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V
V_{OL}	output voltage LOW	I_{OL} = 5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} –0.5 and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
T_{SK}	skew delay between display outputs R, G, B, $\overline{\text{COR}}$, Y and BLAN		–	–	20	ns

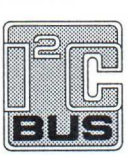
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
DRAM INTERFACE						
t_{RC}	read or write cycle time		344	380	415	ns
t_{RP}	$\overline{RAS}$ precharge time		125	140	155	ns
t_{RAS}	$\overline{RAS}$ pulse width		194	210	230	ns
t_{CAS}	$\overline{CAS}$ pulse width		113	133	153	ns
t_{ASR}	row address set-up time		30	60	80	ns
t_{RAH}	row address hold time		50	60	92	ns
t_{ASC}	column address set-up time		50	60	75	ns
t_{CAH}	column address hold time		50	60	70	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time		130	148	160	ns
t_{RAD}	$\overline{RAS}$ to column address delay time		60	74	105	ns
t_{RSH}	$\overline{RAS}$ hold time		15	60	70	ns
t_{CSH}	$\overline{CAS}$ hold time		260	286	300	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time		60	70	80	ns
t_{DZC}	$\overline{CAS}$ set-up time from data input		200	225	280	ns
t_T	rise and fall times		10	15	20	ns
t_{WCS}	write set-up time		193	212	235	ns
t_{WCH}	write command hold time		116	137	150	ns
t_{DS}	data input set-up time		193	212	235	ns
t_{DH}	data input hold time		42	62	80	ns
t_{RAC}	access time from $\overline{RAS}$		165	183	220	ns
t_{CAC}	access time from $\overline{CAS}$		0	35	40	ns
t_{AA}	access time from address		95	108	120	ns
t_{RCS}	read command set-up time		193	212	235	ns
t_{RCH}	read command hold time to $\overline{CAS}$		0	10	20	ns
t_{RRH}	read command hold time to $\overline{RAS}$		55	65	100	ns
t_{RAL}	column address to $\overline{RAS}$ lead time		90	133	150	ns
t_{OFF1}	output buffer turn-off time		20	30	40	ns
t_{CDD}	$\overline{CAS}$ to data input delay time		25	35	45	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-BUS						
t_{LOW}	clock LOW period		4	–	–	µs
t_{HIGH}	clock HIGH period		4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;STA}$	START hold time		4	–	–	µs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	µs

Notes to the characteristics

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ± 1 mA.
2. RGBREF is the positive supply for the RGB output pins and it must be able to source the I_{OH} current from the R, G and B pins. The leakage specification on RGBREF only applies when there is no current load on the RGB pins.

PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

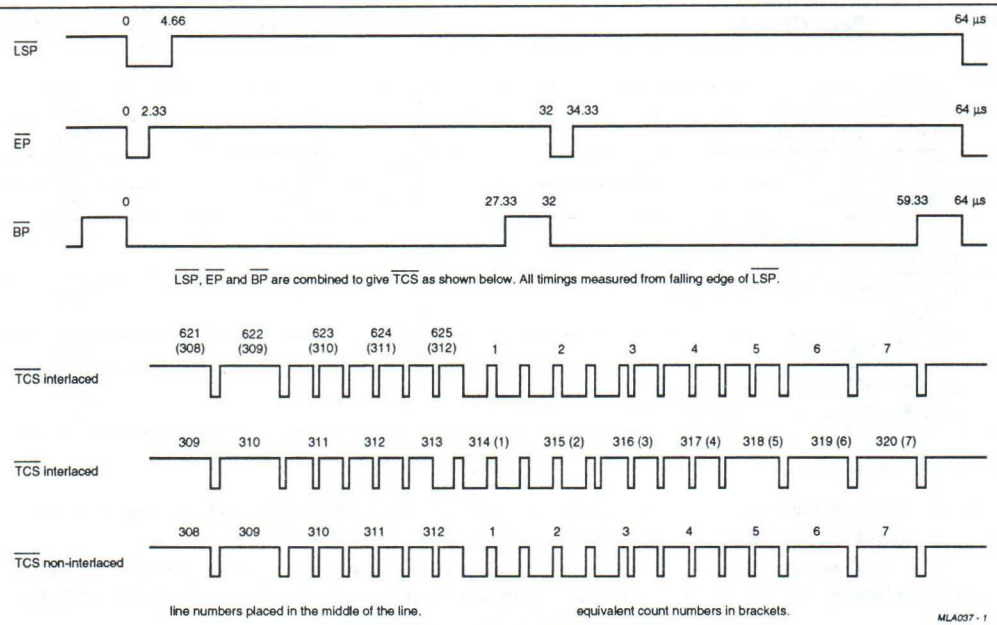


Fig.4 Composite sync waveforms.

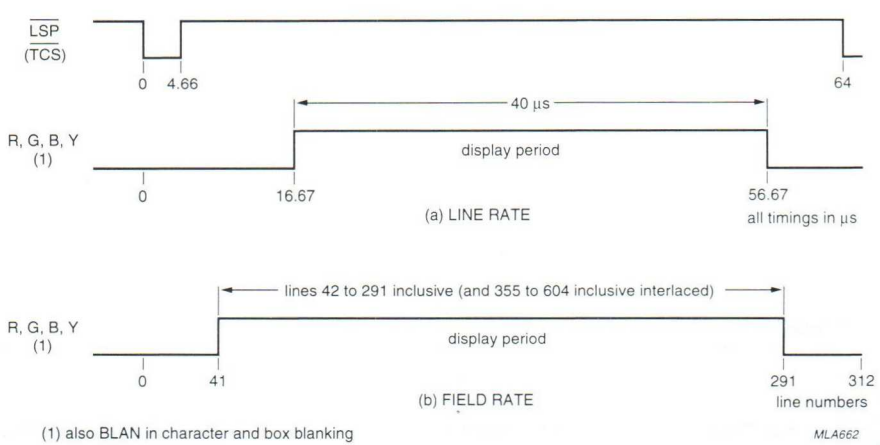


Fig.5 Display output timing (a) line rate (b) field rate.

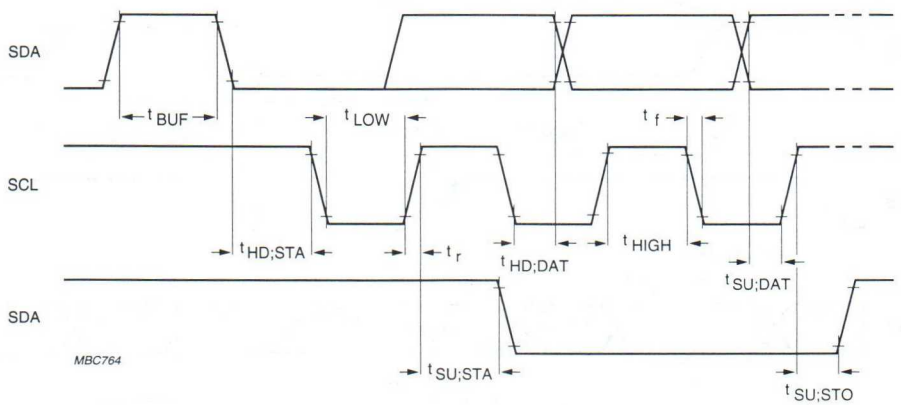


Fig.6 I²C-bus timing.

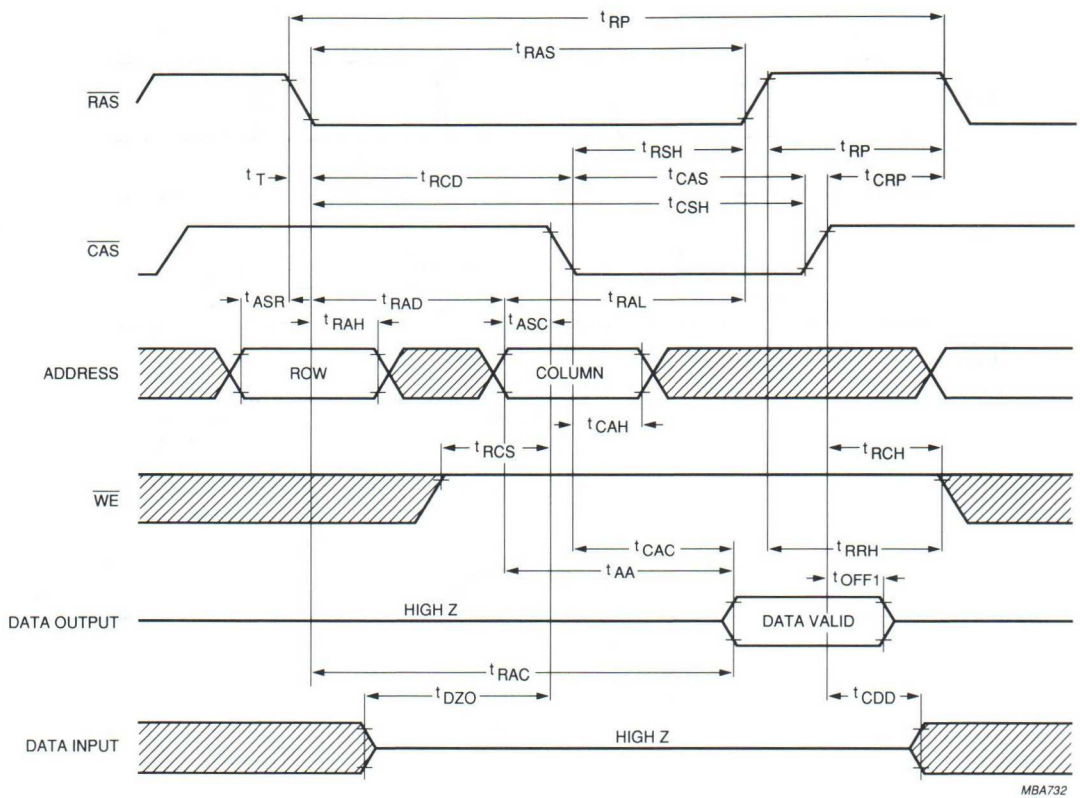


Fig.7 DRAM interface timing; read cycle.

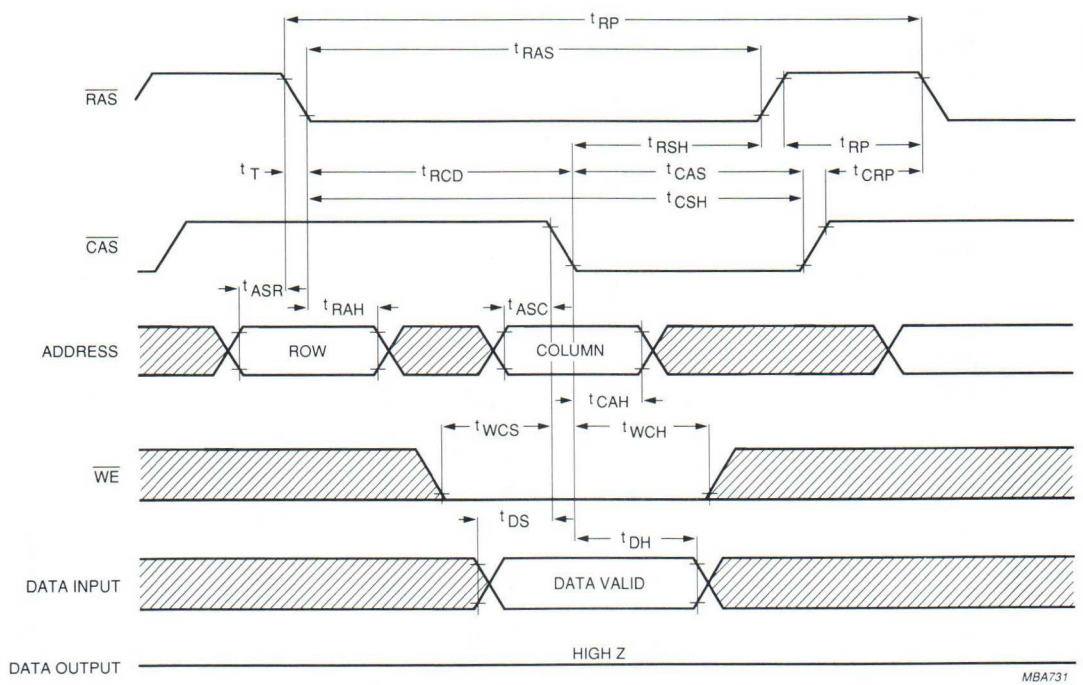


Fig.8 DRAM interface timing; write cycle.

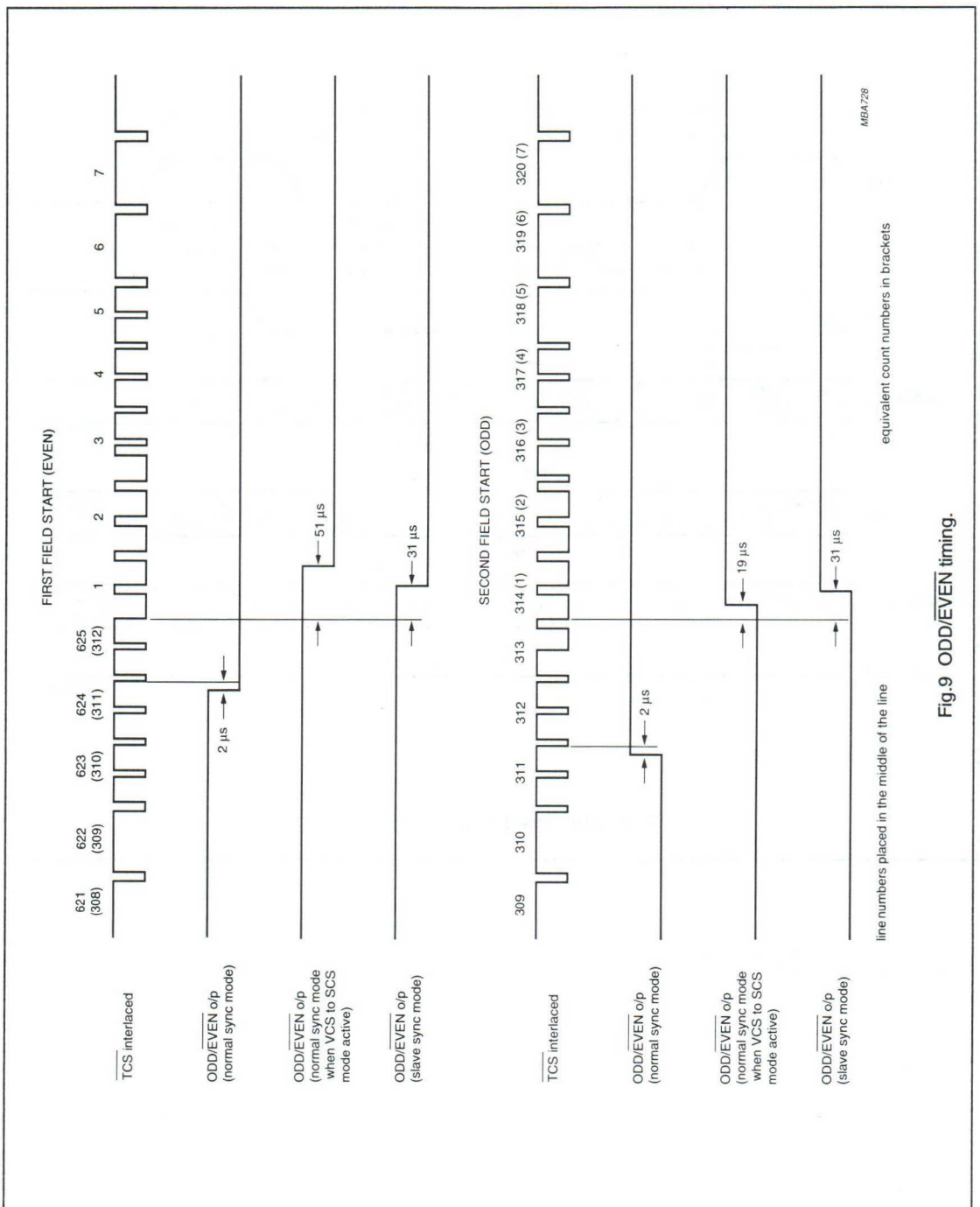


Fig.9 ODD/$\overline{\text{EVEN}}$ timing.

APPLICATION INFORMATION

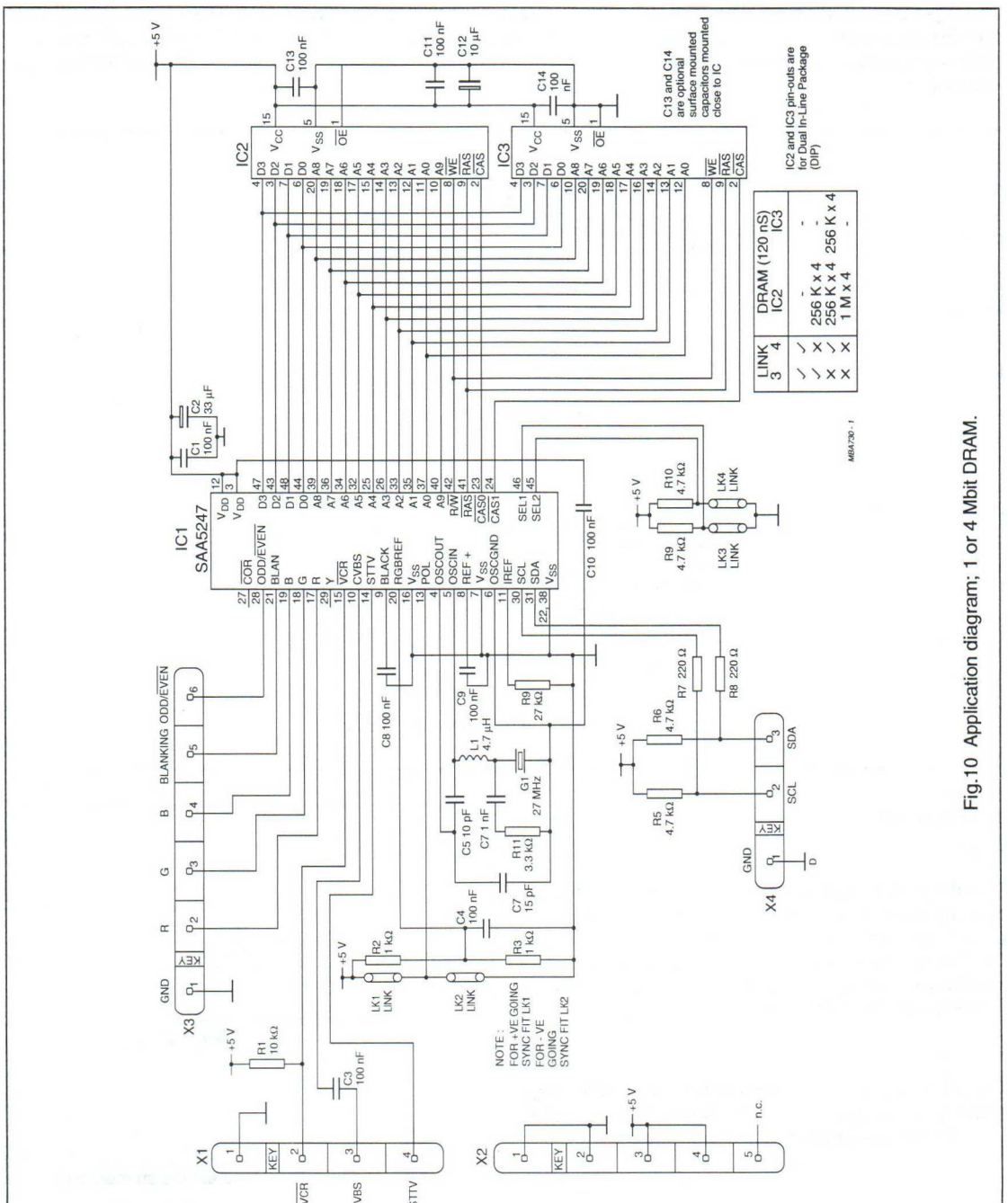


Fig.10 Application diagram; 1 or 4 Mbit DRAM.

IVT1.1BMC page memory organization

The organization of the page memory is illustrated by Fig.11. The IVT1.IBMC provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; Row 24 is the extra row available for software generated status messages and FLOF/FASTEXT prompt information.

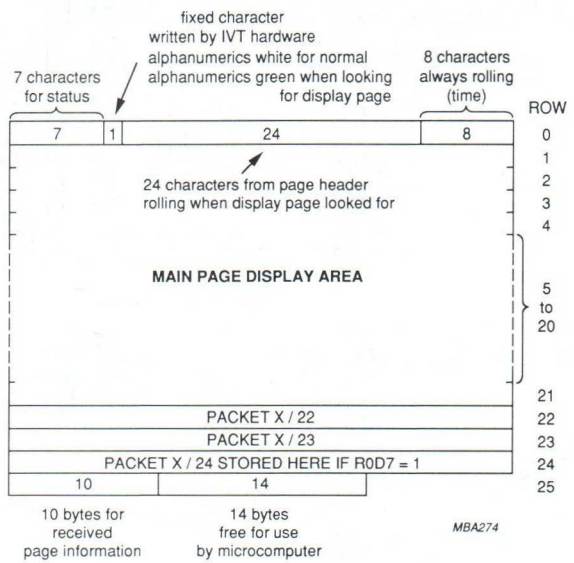


Fig.11 Basic page memory organization.

Note to Fig.11

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by IVT1.1BMC to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of Row 25 contain control data relating to the received page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

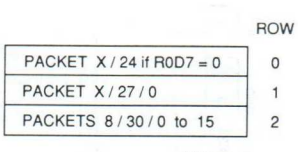


Fig.12 Organization of the extension memory.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

Page number

MAG magazine
PU page units
PT page tens

PBLF page being looked for
$\overline{\text{FOUND}}$ LOW for page has been found
HAM.ER Hamming error in corresponding byte

Page sub-code

MU minutes units
MT minutes tens
HU hours units
HT hours tens

C4-C14 transmitted control bits.

Register maps

IVT1.1BMC mode registers R0 to R11 are shown in Table 2. R0 to R10 are WRITE only; R11 is READ/WRITE. Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 Register map

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Adv. control	0	X24 POS	FREE RUN PLL	AUTO ODD/$\overline{\text{EVEN}}$	DISABLE HDR ROLL	DISPLAY STATUS ROW ONLY	DISABLE ODD/$\overline{\text{EVEN}}$	–	$\overline{\text{R11}}$/R11B SELECT
Mode	1	VCS TO SCS	$\overline{7+P}$/ 8-BIT	ACQ $\overline{\text{ON}}$/OFF	–	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0
Page request address	2	–	–	–	–	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	3	–	–	CLEAR B.M.	PRD4	PRD3	PRD2	PRD1	PRD0
		–	–	–	–	–	–	–	–
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS $\overline{\text{BTM}}$ TOP	CURSOR ON	$\overline{\text{CONCEAL}}$ REVEAL ON	$\overline{\text{TOP}}$/BTM HALF	$\overline{\text{SINGLE}}$ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
		–	–	–	–	–	–	–	–
Cursor row	9	SUPPL. BLAST	CLEAR MEM.	A0	R4	R3	R2	R1	R0
Cursor column	10	SUPPL. ROW 24	SUPPL. ROW 0	C5	C4	C3	C2	C1	C0
Cursor data	11	D7	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{\text{625}}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TEXT SIGNAL QUALITY	VCS SIGNAL QUALITY

Notes to Table 2

1. – indicates these bits are inactive and must be written to logic 0 for future compatibility.
2. All bits in registers R0 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of Registers R1, R5 and R6 which are set to logic 1.
3. All memory is cleared to 'space' (00100000) on power-up, except Row 0 Column 7 Chapter 0, which is 'alpha' white (00000111) as the acquisition circuit is enabled but the page is on hold.
4. TB must be set to logic 0 for normal operation.
5. The I^2C slave address is 0010001

Register description

R0 ADVANCED CONTROL - auto increments to Register 1

$\overline{\text{R11}}$/R11B SELECT	Selects reading of R11 or R11B
DISABLE ODD/$\overline{\text{EVEN}}$	Forces ODD/$\overline{\text{EVEN}}$ output LOW when logic 1
DISPLAY STATUS ROW	When SET = 1 and R1D6 = 1 open (8-bit mode) then all the text display is blanked out apart from the status row, this allows the page memory to be used for non-textural data, such as in the German top system.
DISABLE HDR ROLL	Disables green rolling header and time
AUTO ODD/$\overline{\text{EVEN}}$	When set forces ODD/$\overline{\text{EVEN}}$ low if any TV picture displayed, if DISABLE ODD/$\overline{\text{EVEN}}$ = 0
FREE RUN PLL	Will force the PLL to free run in all conditions
X24 POS	Automatic display of FASTEXT prompt row when logic 1

R1 MODE - auto increments to Register 2

T0, T1	Interlace/non-interlace 312/313 line control (see Table 4)
TCS ON	Text composite sync or direct sync select
$\overline{\text{DEW}}$/FULL FIELD	Field-flyback or full channel mode
ACQ $\overline{\text{ON}}$/OFF	Aquisition circuits turned off when logic 1
$\overline{7 + \text{P}}$/8-BIT	7 bits with parity checking or 8-bit mode.
VCS TO SCS	When logic 1 enables display of messages with 60 Hz input signal

R2 PAGE REQUEST ADDRESS - auto increments to Register 3

COL SC0 - SC2	Point to start column for page request data (see Table 3)
TB	Must be logic 0 for normal operation

R3 PAGE REQUEST DATA - does not auto increment (see Table 3)

CLEAR B.M.	When set to logic 1. Useful when transmission increase channel changes.

R5 NORMAL DISPLAY CONTROL - auto increments to Register 6

R6 NEWSFLASH/SUBTITLE DISPLAY CONTROL - auto increments to Register 7

PON	Picture on
TEXT	Text on
COR	Contrast reduction on
BKGND	Background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 DISPLAY MODE - does not auto increment

BOX ON 0	Boxing function allowed on Row 0
BOX ON 1-23	Boxing function allowed on Row 1-23
BOX ON 24	Boxing function allowed on Row 24
DOUBLE HEIGHT	To display double height text
BOTTOM HALF	To select bottom half of page when DOUBLE HEIGHT = 1
REVEAL ON	To reveal concealed text
CURSOR ON	To display cursor
STATUS TOP	Row 25 displayed above or below the main text

R9 CURSOR ROW - auto increments to Register 10

R0 to R4	Active row for data written to or read from memory via the I²C-bus
A0	Selects display memory page (when = 0) or extension packet memory (when = 1)
CLEAR MEM.	When set to 1, clears the display memory. This bit is automatically reset
SUPPL. BLAST	When set to 1, Column S4 and S5 (of Table 5) are mapped into 4 and 5 respectively, replacing blast-through alphanumerics in graphics mode

R10 CURSOR COLUMN - auto increments to Register 11 or 11B

C0 to C5	Active column for data written to or read from memory via the I²C-bus
SUPPL. ROW 0	When set to 1, Column S4 and S5 (of Table 5) are mapped into Columns 6 and 7 respectively, just for Row 0 Columns 0 to 7
SUPPL. ROW 24	When set to 1, Column S4 and S5 (of Table 5) are mapped into Columns 6 and 7 respectively just for Row 24

R11 CURSOR DATA - does not auto increment

D0 to D6	Data read from/written to memory via I²C, at location pointed to by R9 and R10. This location automatically increments each time R11 is accessed

R11B DEVICE STATUS - does not auto increment

VCS SIGNAL QUALITY	Indicates that the video signal quality is good and PLL is phase locked to input video when = 1
TEXT SIGNAL QUALITY	If a good teletext signal is being received when = 1
ROM VER R0 to R4	Indicated language/ROM variant. For Western European = 01001
$\overline{625}$/525 SYNC	If the input video is a 525 line signal when = 1

Table 3 Register map for page requests (R3)

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

1. Abbreviations are as for Table 1 except for DO CARE bits.
2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
3. If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
4. Columns auto-increment on successive I²C-bus transmission bytes.

Table 4 Interlace/non-interlace 312/313 line control (T0 and T1)

T1	T0	RESULT
0	0	interlaced 312.5/312.5 lines
0	1	non-interlaced 312/313 lines (note 1)
1	0	non-interlaced 312/312 lines (note 1)
1	1	SCS mode (scan composite sync)

Note to Table 4

1 Reverts to interlaced mode if a newsflash or subtitle is being displayed.

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional 2-pin design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone as illustrated in Fig.13.

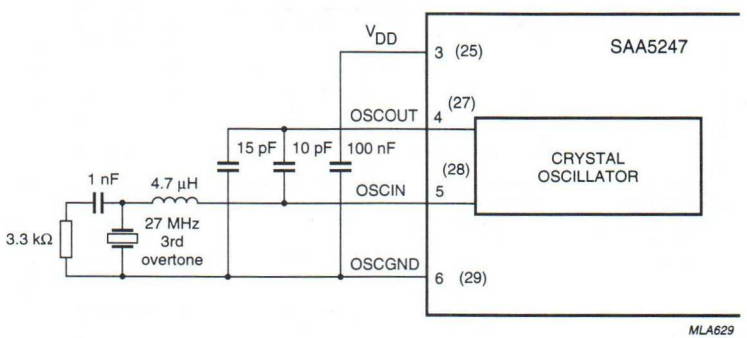


Fig.13 Crystal oscillator application diagram for SOT240; pins in parenthesis are for SOT208.

Table 5 Crystal characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)					
C1	series capacitance	–	1.7	–	pF
C0	parallel capacitance	–	5.2	–	pF
C_L	load capacitance	–	20	–	pF
Rr	resonant resistance	–	–	50	Ω
R1	series resistance	–	20	–	Ω
Xa	ageing	–	–	±5	10^{-6}/yr
Xj	adjustment tolerance	–	–	±25	10^{-6}
Xd	drift	–	–	±25	10^{-6}

Character sets

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character sets differ only in 13 national option characters as indicated in Table 7 with reference to their table position in the basic character matrix illustrated in Table 6. The IVT1.1BMC automatically decodes transmission bits C12 to C14. Table 5 illustrates the character matrixs.

Character bytes are listed as transmitted from b1 to b7.

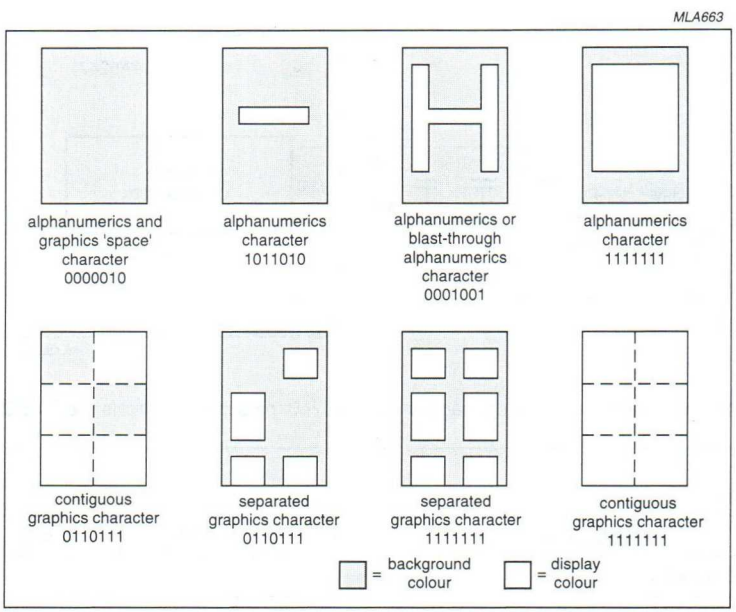
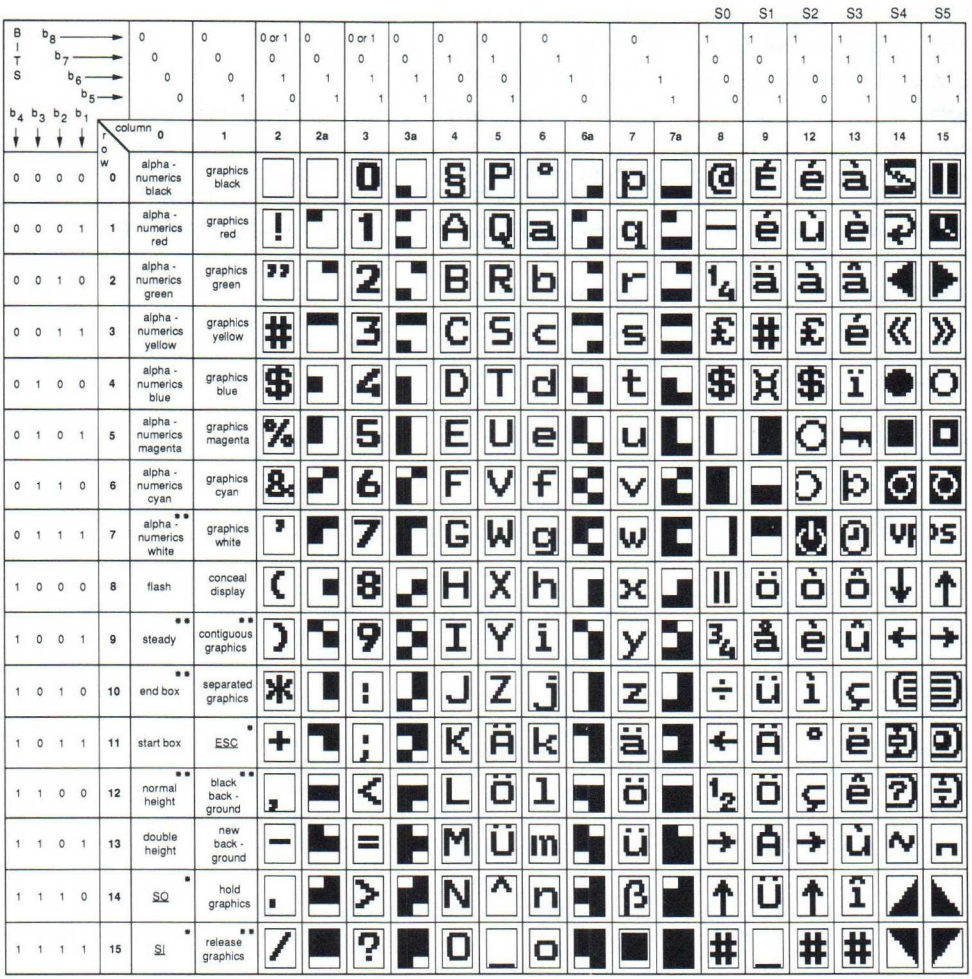


Fig.14 Character format.

Table 5 SAA5247P/B character data input decoding



For character version number (01001) see Register 11B.

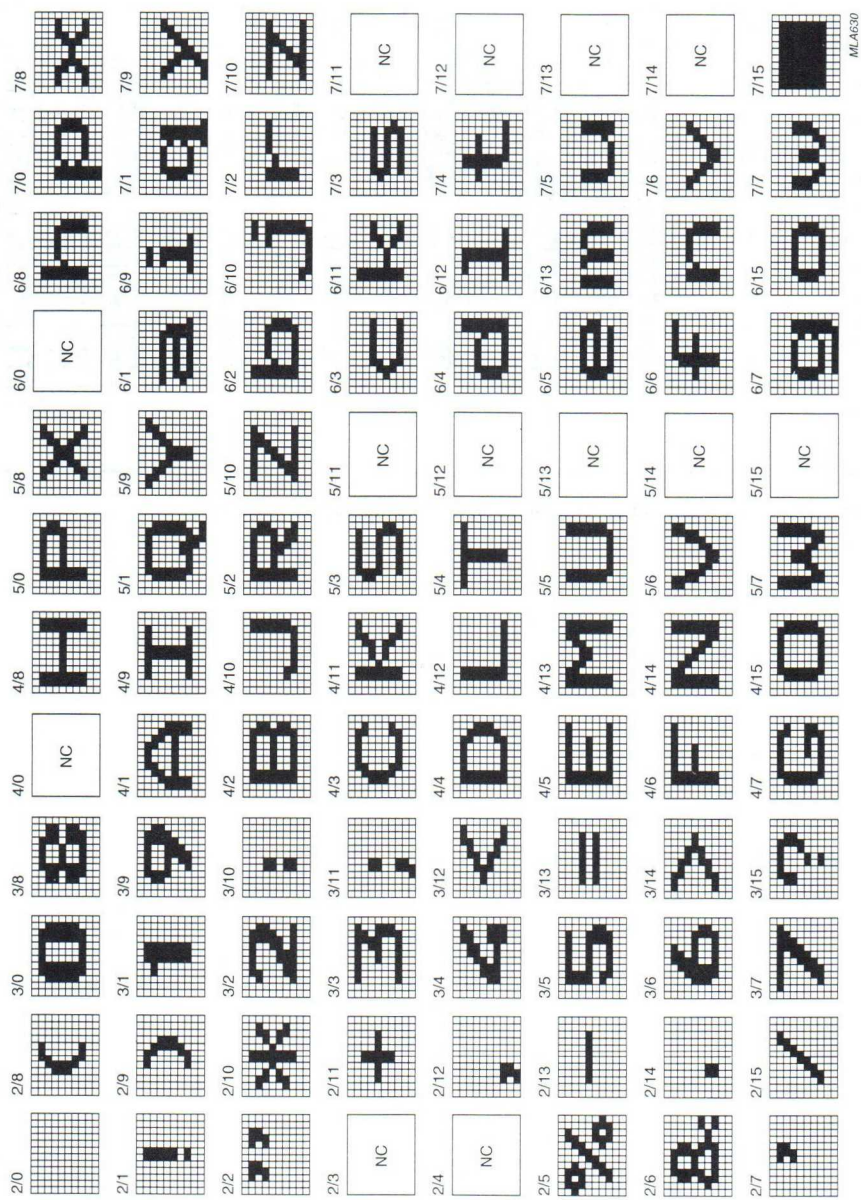
* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Notes to Table 5

1. Control characters shown in Columns 0 and 1 are normally displayed as spaces.
2. Characters may be referred to by column and row, For example 2/5 refers to %.
3. Black represents displayed colour. White represents backgound.
4. Character rectangle shown as follows: 
5. The SAA5247 national option characters are illustrated in Table 7.
6. Characters S4/11, S4/12, S5/10, S5/11 and S5/12 are special characters for combining with character S4/10.
7. National option characters will be developed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Table 7. Therefore columns S0, S1, S2 and S3 are mapped into the basic code table as national options for English, Swedish, Italian and French respectively.
8. Columns S4 and S5 are mapped into Columns 6 and 7 respectively when enabled by R10 bit D6 (Row 0 Columns 0 to 7) and R10 bit D7 (row 24) set to 1.
9. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.
8. Columns S4 and S5 replace columns 4 and 5 respectively when enabled by R9 bit D7 set to 1.
9. Columns S4 and S5 are directly accessible with column address 1110 and 1111 respectively.

Table 6 SAA5247 basic character matrix



Where: NC = national option character position.

Table 7 SAA5247 national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç

MLA664

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

Single-chip Teletext and VPS decoder (IVT1.0VPS)

SAA5248

FEATURES

- Complete Teletext and VPS decoder in a 52-pin shrink DIL, or 64-pin QFP, integrated circuit
- Separate storage of VPS data (PDC System A) and packet 8/30/2 data (PDC System B) allowing dual standard VPT decoders
- Data valid output available to indicate reception of error-free VPS or packet 8/30/2 data.
- Packet 8/30/2 stored separately from other packets 8/30
- Software compatible with SAA5246 (apart from new VPS features).
- Hardware compatible with the SAA5246 teletext decoder.
- Single +5 V power supply
- Both video and scan related synchronization modes are supported
- RGB interface to standard colour decoder ICs, push-pull output drive
- Digital data slicer and display clock phase-locked loop reduce peripheral components to a minimum
- Data capture performance similar to SAA5231 (VIP2)
- Option for up to seven national languages
- Optional storage of packet 24 in the display memory
- Separate text and video signal quality detectors, 625/525 video status and language version all readable via I²C-bus
- Automatic $\overline{\text{ODD}}$/EVEN output control with override
- Control of display PLL free-run and rolling header via I²C-bus
- VCS to SCS mode for stable 525 line status display

DESCRIPTION

The SAA5248 is a single-chip teletext decoder IC for decoding 625 line base World System Teletext transmissions. The device is based on IVT1.0 (SAA5246) with the addition of reception facilities for the 2.5 MHz biphase VPS signal. It is intended for use in video recorders, in particular to implement the VPT facility (VCR Programming via Teletext). With suitable software, both VPT standards (EBU PDC System A and System B) can be accommodated to allow operation from any European VPT transmission.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5248ZP/E	52	SDIL	plastic	SOT247
SAA5248GP/E	64	QFP	plastic	SOT208

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	65	130	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1.0	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature range	–20	–	+70	°C

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT 247	SOT208	
OSCOUT	1	27	27 MHz crystal oscillator output
OSCIN	2	28	27 MHz crystal oscillator input
OSCGND	3	29	0 V crystal oscillator ground
V_{SS}	4, 5, 15, 26	26, 30, 31, 43, 58	0 V ground
n.c.	7	-	not connected
BLACK	8	35	video black level storage pin, connected to ground via a 100 nF capacitor
CVBS	9	36	composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor
IREF	10	37	reference current input pin, connected to ground via a 27 kΩ resistor
V_{DD}	6, 11, 52	25, 32, 38	+5 V positive supply
POL	12	39	STTV/LFB/FFB polarity selection pin
STTV/LFB	13	40	sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode)
$\overline{VCR}$/FFB	14	42	PLL time constant switch/field input pin. Function controlled by an internal register bit (scan sync mode)
R	16	44	dot rate character output of the RED colour information
G	17	45	dot rate character output of the GREEN colour information
B	18	47	dot rate character output of the BLUE colour information
RGBREF	19	48	input DC voltage to define the output high level on the RGB pins
BLAN	20	52	dot rate fast blanking output
$\overline{COR}$	21	53	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open-drain output
$\overline{ODD}$/EVEN or $\overline{DV}$	22	54	In $\overline{ODD}$/EVEN mode a 25 MHz output synchronized to the input CVBS field sync pulses to make a non-interlaced display by adjustment of the vertical deflection currents. In $\overline{DV}$ mode a VPT data valid signal used to indicate reception of error-free VPS or 8/30/ format 2 data
Y	23	55	dot rate character output of teletext foreground colour information. Open-drain output
SCL	24	56	serial clock input for I²C-bus. It can still be driven HIGH during power-down of the device
SDA	25	57	serial data port for the I²C-bus. Open drain output. It can still be driven HIGH during power-down of the device

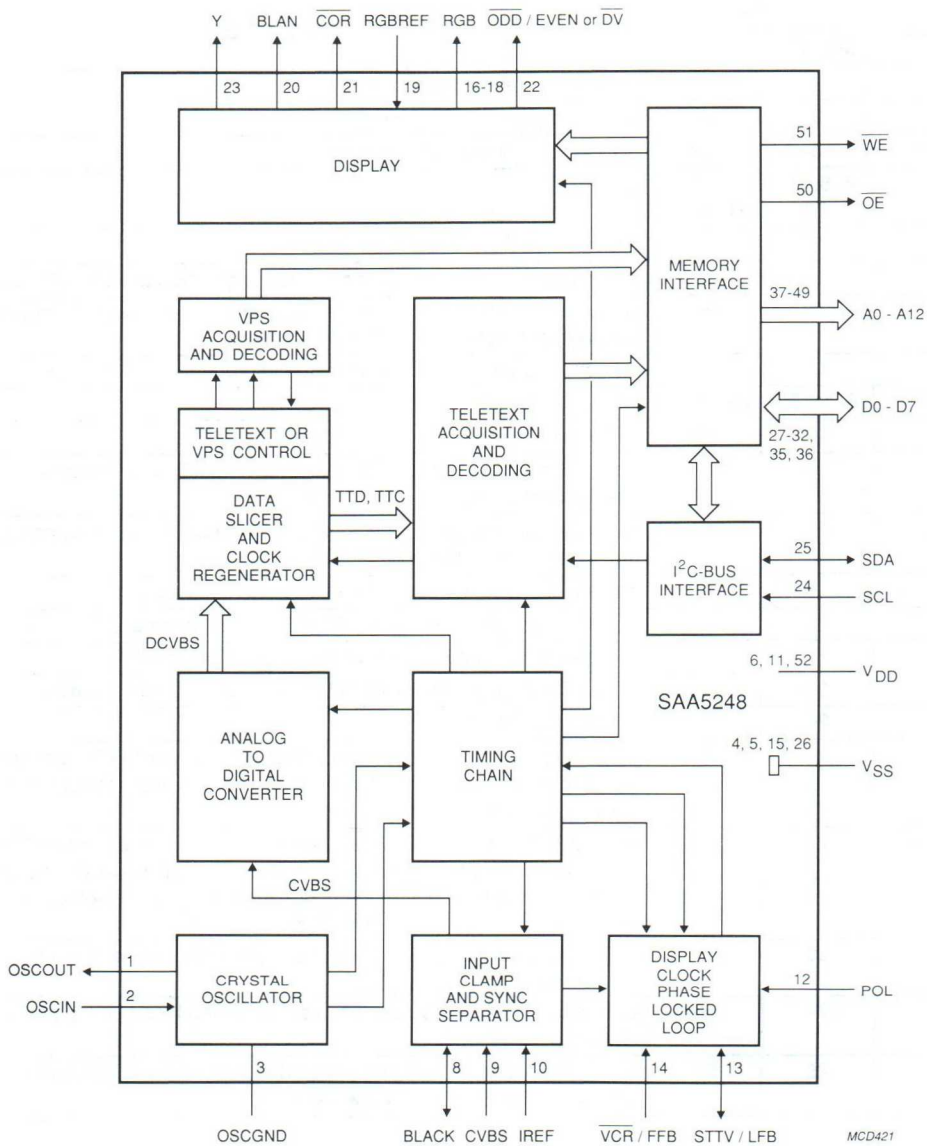


Fig.1 Block diagram for SOT247 (SDIL52) package.

SYMBOL	PIN		DESCRIPTION
	SOT 247	SOT208	
D0-D5	27-32	60 - 64, 3	data ports for the page RAM
n.c.	33, 34	1, 2, 10, 11, 15, 18, 33, 34, 41, 46, 49 - 51, 59	not connected
D6-D7	35, 36	4, 5	data ports for the page RAM
A0-A12	37-49	6-9, 12-14, 16, 17, 19-22	address output for the page SRAM
$\overline{OE}$	50	23	output enable for the page SRAM
$\overline{WE}$	51	24	write enable for the page SRAM

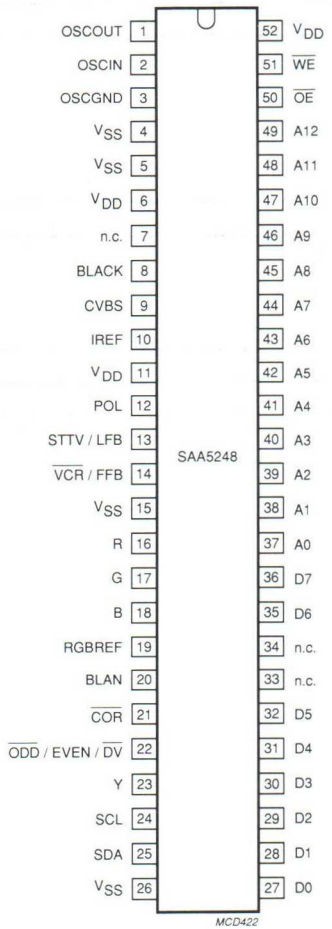


Fig.2 Pin configuration; SOT247 (SDIL52).

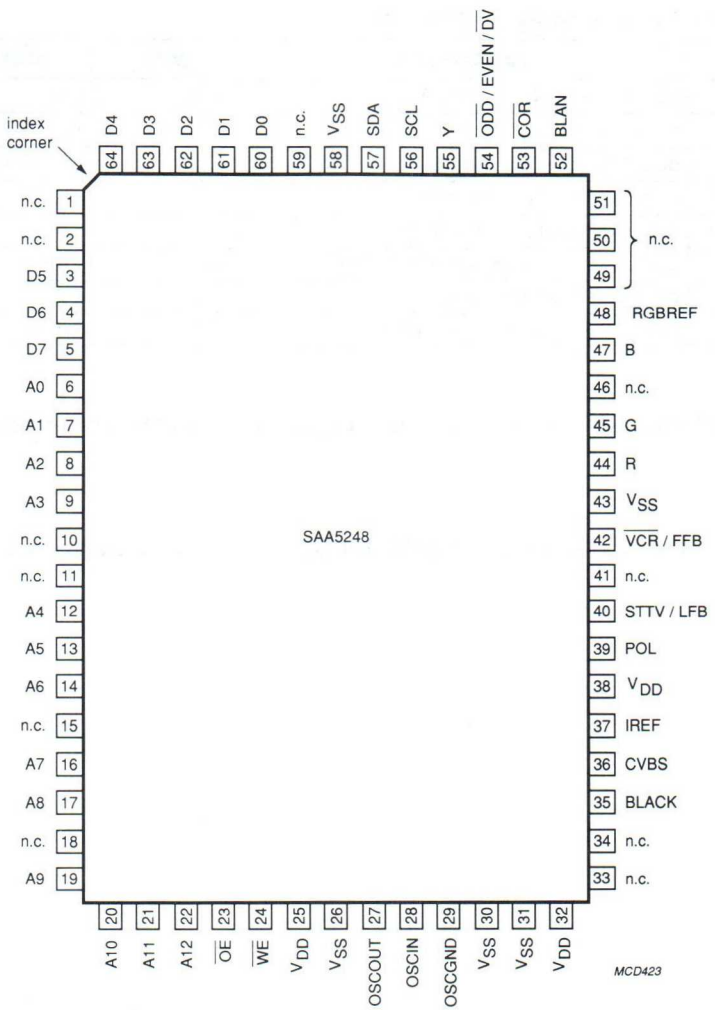


Fig.3 Pin configuration; SOT248 (QFP64).

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	−0.3	6.5	V
V_I	input voltage (any input)	−0.3	V_{DD} +0.5	V
V_O	output voltage (any output)	−0.3	V_{DD} +0.5	V
I_O	output current (each output)	−	±10	mA
I_{IOK}	DC input or output diode current	−	±20	mA
T_{amb}	operating ambient temperature range	−20	+70	°C
T_{stg}	storage temperature range	−55	+125	°C
V_{stat}	electrostatic handling (see note)	−2000	+2000	V

Note

Electrostatic handling is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a 15 ns rise time.

Failure Rate

The failure rate at T_{amb} = 55 °C will be a maximum of 1000 FITS (1 FIT = 1 x 10^{-9} failures per hour).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
RGBREF						
V_{IL}	LOW level input voltage		−0.3	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_{DC}	DC current		–	–	10	mA
SCL						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
f_{SCL}	clock frequency		0	–	100	kHz
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
C_I	input capacitance		–	–	10	pF
Inputs/outputs						
CRYSTAL OSCILLATOR (OSCIN; OSCOUT)						
f_{XTAL}	crystal frequency		–	27	–	MHz
V_{OSC}	oscillation amplitude (peak-to-peak value)		–	1.5	–	V
G_v	small signal voltage gain		–	1	–	V/V
G_m	mutual conductance		5	–	–	mA/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	1	–	pF
BLACK						
C_{blk}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
SDA						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	3 V to 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = –20 to +70 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage range		4.5	5.0	5.5	V
I_{DD}	total supply current		–	65	130	mA
Inputs						
CVBS						
V_{syn}	sync amplitude		0.1	0.3	0.6	V
t_{syn}	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		–150	0	+150	ns
t_{syd}	change in sync delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{vid(p-p)}$	video input amplitude (peak-to-peak)		0.7	1.0	1.4	V
	display PLL catching range		±7	–	–	%
Z_{src}	source impedance		–	–	250	Ω
C_I	input capacitance		–	–	10	pF
IREF						
R_g	resistor to ground		–	27	–	kΩ
POL						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
LFB						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
I_I	input current	note 1	–1	–	+1	mA
t_{LFB}	delay between LFB front edge and input video line sync		–	250	–	ns
$\overline{VCR}$/FFB						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
I_I	input current	note 1	–1	–	+1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs/outputs						
D0 TO D7						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current		−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
t_r	output rise time	0.6 V to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	50	ns
C_L	load capacitance		–	–	120	pF
Outputs						
STTV						
G_{stt}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{tcs}	TCS amplitude		0.2	0.3	0.45	V
V_{DCs}	DC shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive current		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
A0 TO A12 ADDRESS OUTPUT TO MEMORY						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 V to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	50	ns
$\overline{OE}$, $\overline{WE}$						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 V to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
R, G AND B						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = −1.6 mA; RGBREF ≤ V_{DD}−2 V	RGBREF −0.25 V	RGBREF	RGBREF +0.25 V	V
I_{DC}	DC current		–	–	−3.3	mA
$\|Z_o\|$	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
BLAN						
V_{OL}	LOW level output voltage	I_{OL} = 0.2 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA; V_{DD} = 4.5 V	1.1	–	–	V
V_{OH}	HIGH level output voltage	I_{OH} = 0 mA; V_{DD} = 5.5 V	–	–	2.8	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
$\overline{ODD}$/EVEN OR $\overline{DV}$						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −1.6 mA	V_{DD}−0.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
$\overline{COR}$ AND Y (OPEN DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V
V_{OL}	LOW level output voltage	I_{OL} = +2 mA	0	–	0.4	V
V_{OL}	LOW level output voltage	I_{OL} = +5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} −0.5 and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
T_{SK}	skew delay between display outputs R, G, B, $\overline{COR}$, Y and BLAN		–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
MEMORY INTERFACE						
t_{CY}	cycle time		–	500	–	ns
t_{OE}	address change to $\overline{OE}$ LOW		55	–	–	ns
t_{ADDR}	address active time		450	500	–	ns
t_{rOEW}	$\overline{OE}$ pulse width read		295	–	–	ns
t_{wOEW}	$\overline{OE}$ pulse width write		100	–	–	ns
t_{ACC}	access time from address data valid		–	–	150	ns
t_{DH}	data hold time from $\overline{OE}$ HIGH or address change		0	–	150	ns
t_{WEW}	$\overline{WE}$ pulse width		100	–	–	ns
t_{DS}	data set-up time to $\overline{WE}$ HIGH		60	–	–	ns
t_{DHWE}	data hold time from $\overline{WE}$ HIGH		20	–	–	ns
t_{WR}	write recovery time		20	–	–	ns
t_{DE}	data enable from $\overline{WE}$ LOW		60	–	–	ns
I^2C-BUS						
t_{LOW}	clock LOW period		4	–	–	µs
t_{HIGH}	clock HIGH period		4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;STA}$	START hold time		4	–	–	µs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	µs

Notes to the characteristics

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ± 1 mA.
2. Can be pulled higher by external pull-up resistor, (maximum leakage current ≈200 µA).

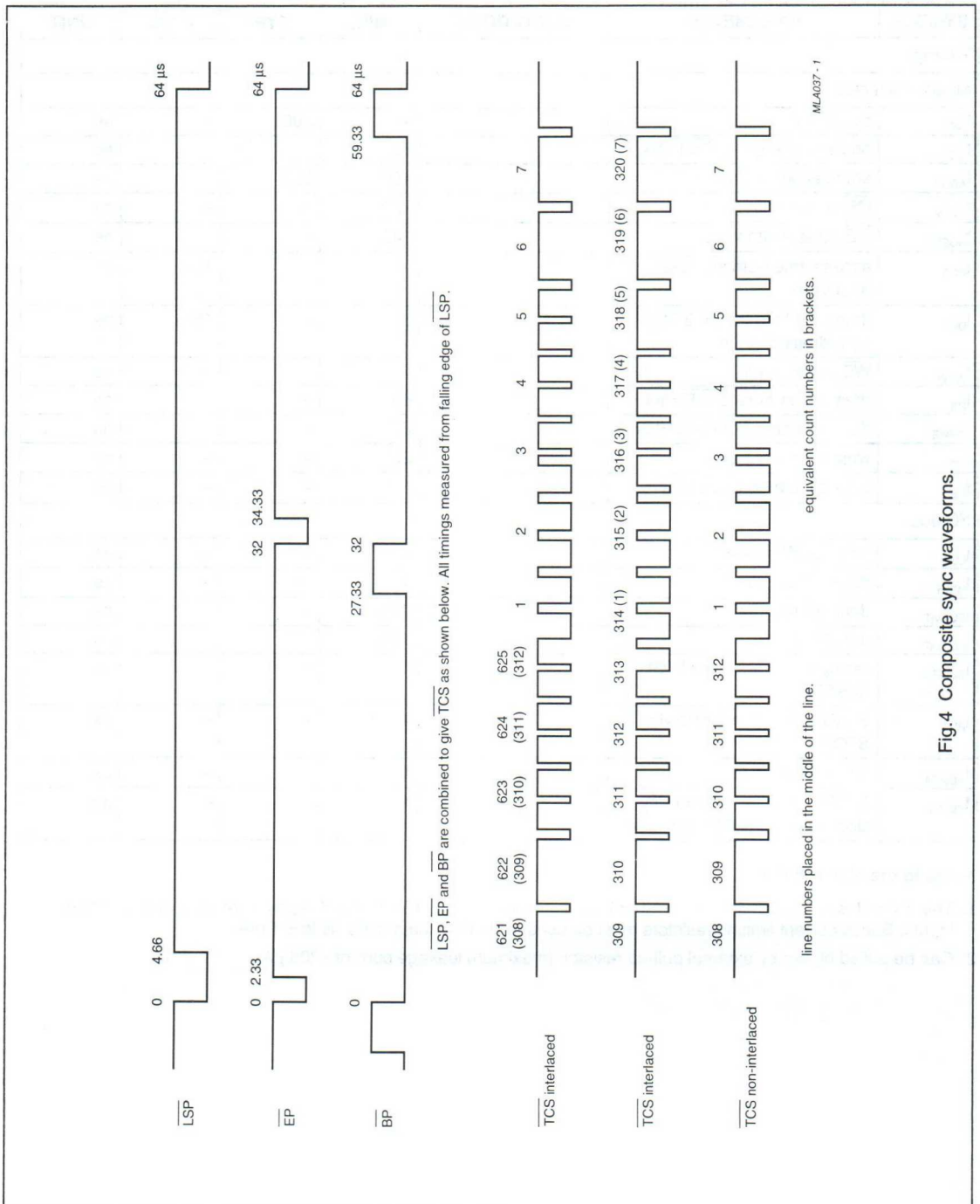


Fig.4 Composite sync waveforms.

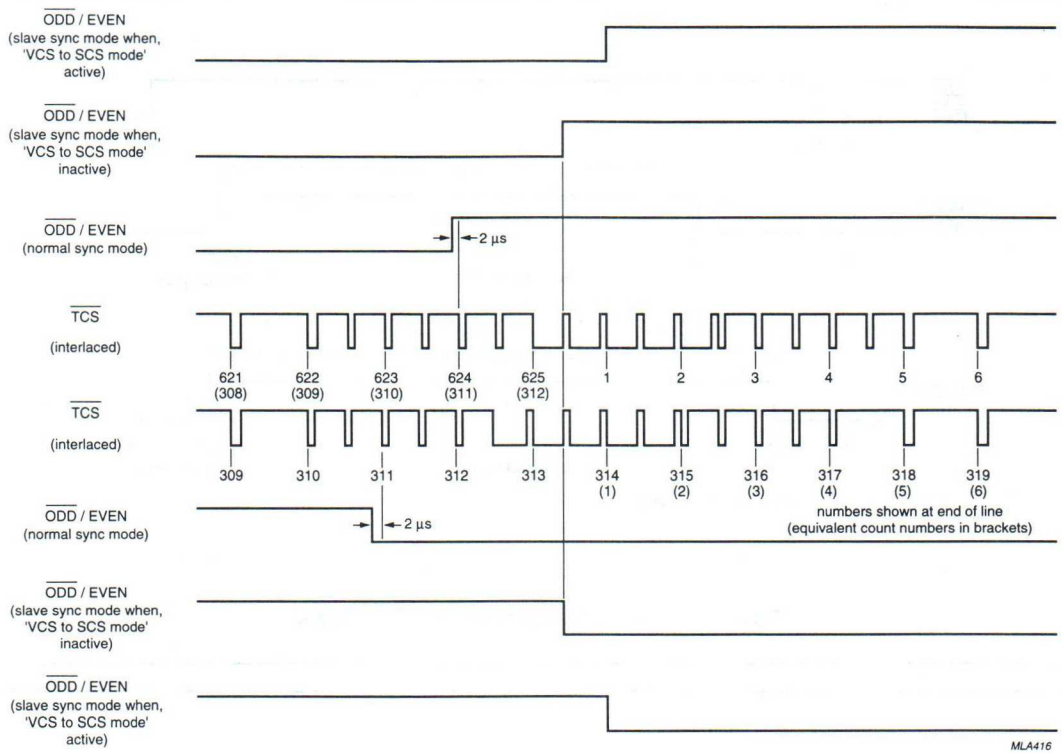


Fig.7 $\overline{\text{ODD}}$/EVEN timing.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

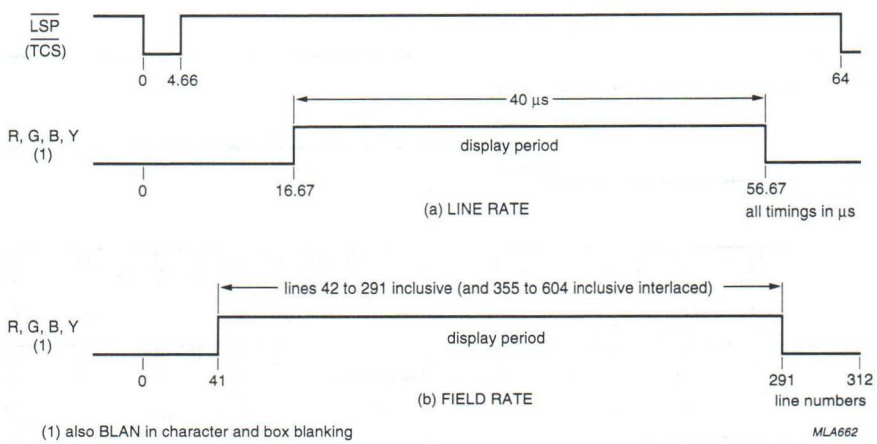


Fig.5 Display output timing (a) line rate (b) field rate.

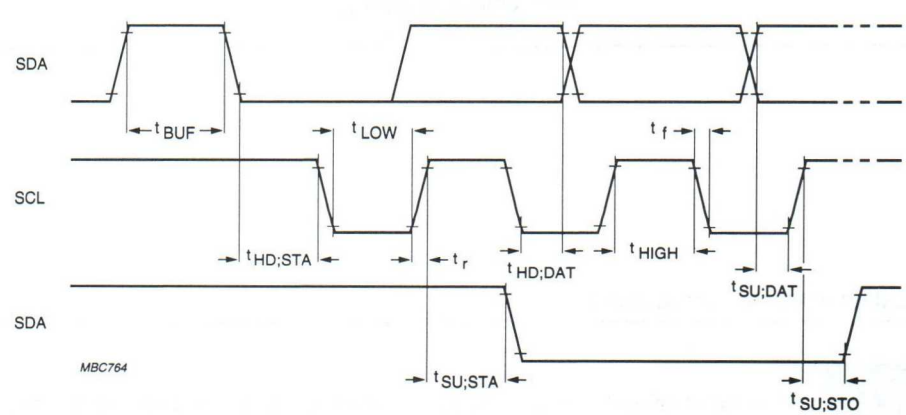
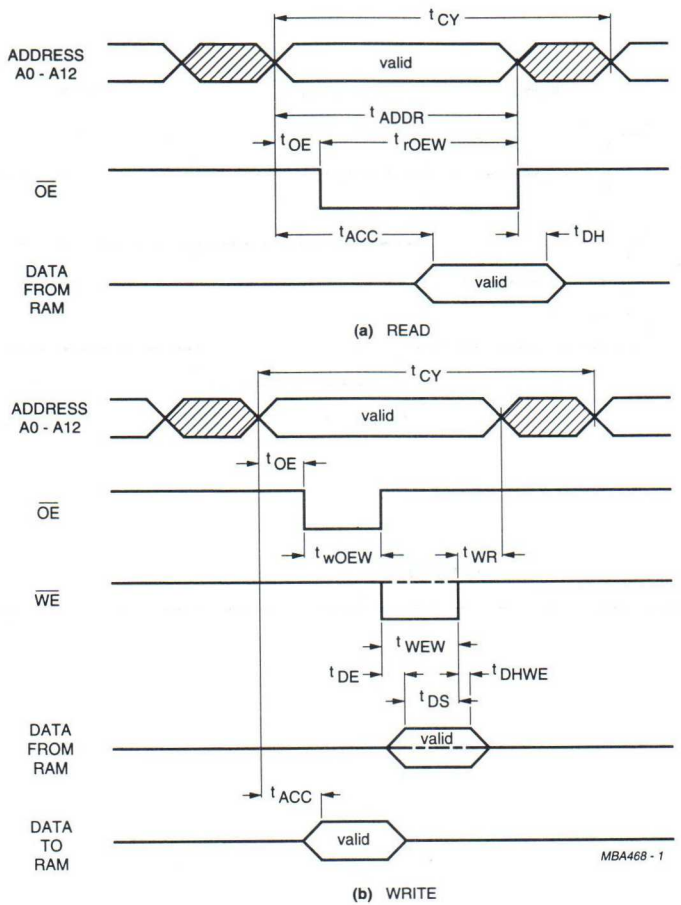


Fig.6 I²C-bus timing.



_.-._.-._ Level during flicker stopped cycle.

Fig.9 Memory interface timing (a) read (b) write.

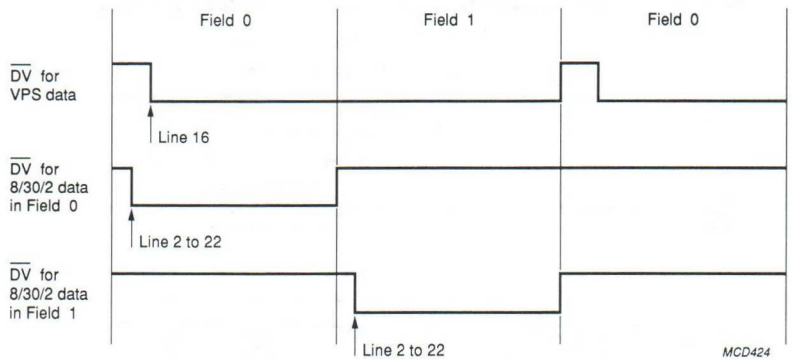
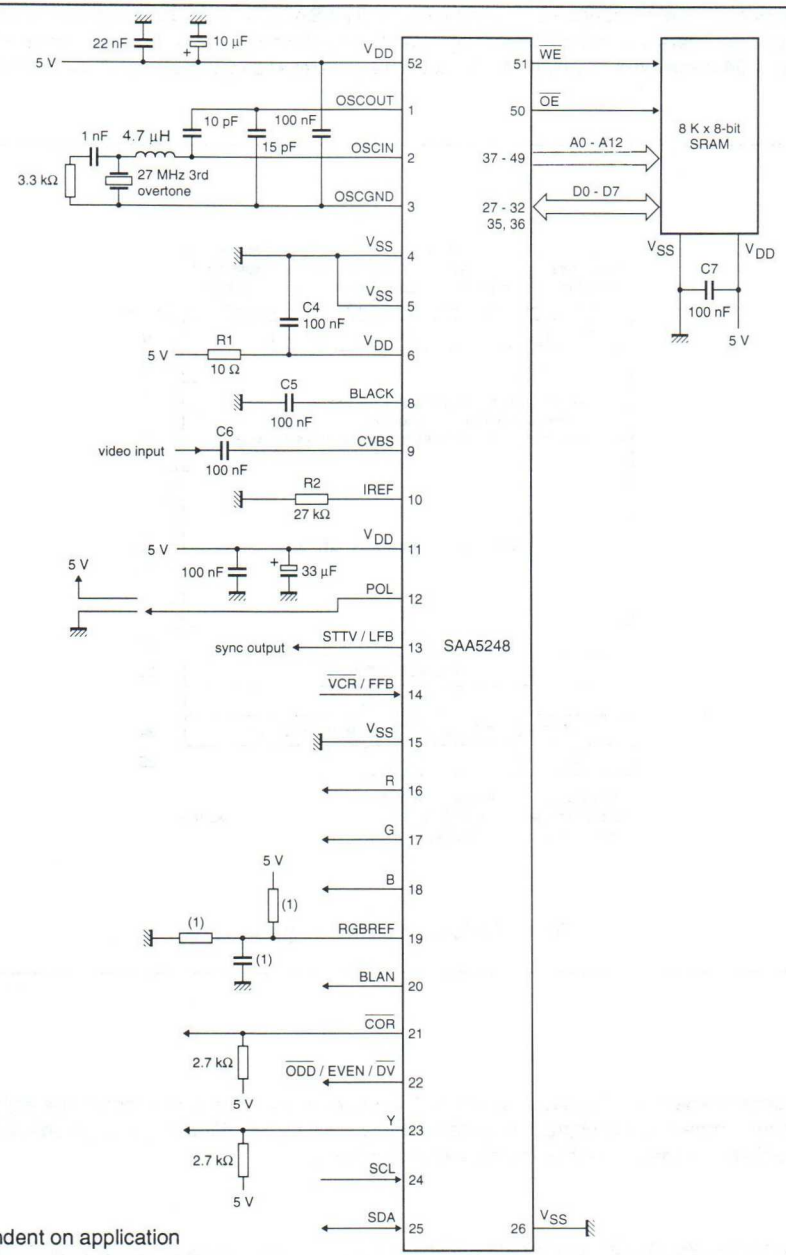


Fig.8 Data Valid timing ($\overline{DV}$).

APPLICATION INFORMATION



(1) Value dependent on application

Fig.10 Application diagram.

SAA5248 page memory organization

The organization of the page memory is illustrated by Fig.11. The SAA5248 provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; Rrow 24 is the extra row available for software generated status messages and FLOF/FASTEXT prompt information.

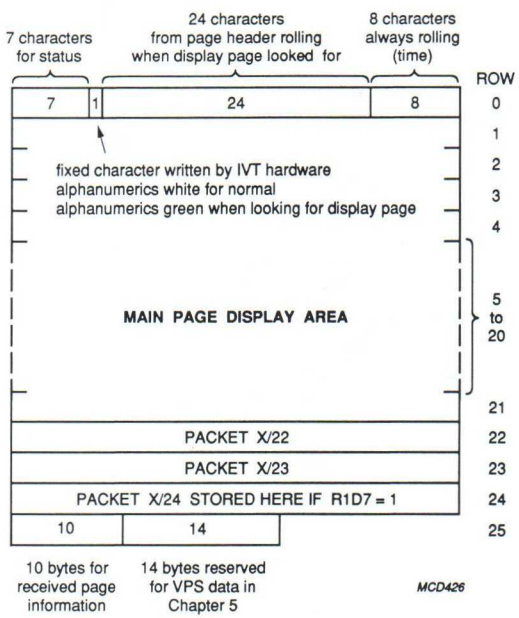


Fig.11 Basic page memory organization.

Note to Fig.11

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by SAA5248 to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of Row 25 contain control data relating to the received page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer, except in Chapter 5 (see Fig.13 where they are reserved for VPS data.

VPT data memory organization

To simplify the software for dual-standard VPT decoders, the VPS data from line 16 is stored in Row 25 of Chapter 5 of the page memory, and is aligned to match the packet 8/30 format 2 data as far as possible.

Column	0	1	2	3	4	5	6	7	8	9	10	11
8/30/2 data Row 23 Chapter 5	D	INITIAL PAGE						b13	b14	b15	b16	b17
VPS data Row 25 Chapter 5	RECEIVED PAGE INFORMATION										B.11	

Column	12	13	14	15	16	17	18	19	20	21	22	23
8/30/2 data Row 23 Chapter 5	b18	b19	b20	b21	b22	b23	b24	b25	STATUS DISPLAY			
VPS data Row 25 Chapter 5	B.12		B.13		B.14		B.15		B.4		B.5	

Column	24 – 39
8/30/2 data Row 23 Chapter 5	STATUS DISPLAY CONTINUED

MCD428 - 1

Fig.13 Memory organization details.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

Page number

MAG magazine

PU page units

PT page tens

PBLF page being looked for

$\overline{\text{FOUND}}$ LOW for page has been found

HAM.ER Hamming error in corresponding byte

When in extension packet enabled mode the rows of information are organized as illustrated by Fig.12.

Row 23 of the extension page, as shown in Fig.12, contains packet 8/30. Packet 8/30 is mapped into the SAA5248 memory as follows:

8/30/0 and 8/30/1 to Chapter 4 Row 23
8/30/2 and 8/30/3 to Chapter 5 Row 23
8/30/4 to 8/30/15 to Chapter 6 Row 23

Page sub-code

MU minutes units

MT minutes tens

HU hours units

HT hours tens

C4-C14 transmitted control bits.

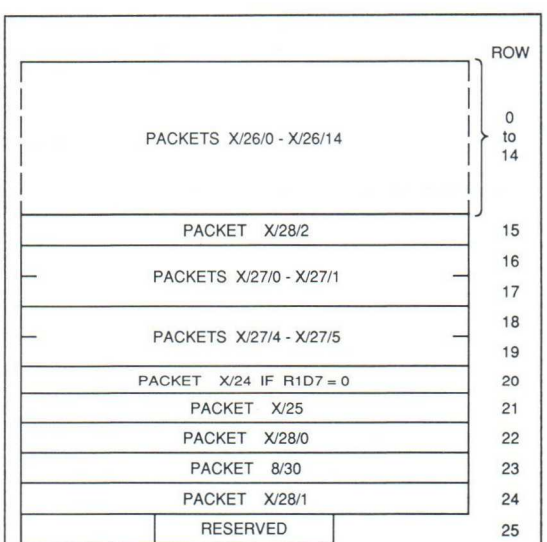


Fig.12 Organization of the extension memory.

Notes to Table 2

1. All bits in registers R0 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R1, R5 and R6 which are set to logic 1.
2. All memory is cleared to 'space' (00100000) on power-up, except Row 0 Column 7 Chapter 0, which is 'alpha' white (00000111) as the acquisition circuit is enabled but the page is on hold.
3. TB must be set to logic 0 for normal operation.
4. The I²C-bus slave address is 0010001

Register maps

SAA5248 mode registers R0 to R11 are shown in Table 2. R0 to R10 are WRITE only; R11 is READ/WRITE. Register map (R3), for page requests, is shown in detail in Table 4.

Table 2 Register map

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Adv. control	0	X24 POS	FREE RUN PLL	AUTO $\overline{\text{ODD}}$/ EVEN*	DISABLE HDR ROLL	–	DISABLE $\overline{\text{ODD}}$/ EVEN*	VCR MODE	$\overline{\text{R11}}$/R11B SELECT
Mode	1	VCS TO SCS	$\overline{7+P}$/ 8-BIT	ACQ $\overline{\text{ON}}$/OFF	EXT. PACKET ENABLE	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0
Page request address	2	HAM. CHECK 27, 28, 8/30	BANK SELECT A2	ACQ CIRCUIT A1	ACQ CIRCUIT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
Display chapter	4	–	–	–	–	–	A2	A1	A0
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS TOP	CURSOR ON	REVEAL ON	BOTTOM HALF	DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
Active chapter	8	–	–	–	VPS ENABLE	CLEAR MEM.	A2	A1	A0
Cursor row	9	–	–	–	R4	R3	R2	R1	R0
Cursor column	10	–	–	C5	C4	C3	C2	C1	C0
Cursor data	11	D7	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{625}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	DATA QUALITY	VCS SIGNAL QUALITY

Where:

* Also used to enable Data Valid ($\overline{\text{DV}}$) output on $\overline{\text{ODD}}$/EVEN pin.

'–' Indicates a bit which does not exist and must be written to logic 0 for future compatibility.

Register description

R0 ADVANCED CONTROL - auto increments to Register 1

$\overline{R11}$/R11B SELECT	Selects reading of R11 or R11B
VCR MODE	Selects short time constant of PLL when logic 1
DISABLE $\overline{ODD}$/EVEN	Forces $\overline{ODD}$/EVEN output LOW when logic 1 (see Table 3)
DISABLE HDR ROLL	Disables green rolling header and time
AUTO $\overline{ODD}$/EVEN	When set forces $\overline{ODD}$/EVEN low if any TV picture displayed, if DISABLE $\overline{ODD}$/EVEN = 0 (see Table 3)
FREE RUN PLL	Will force the PLL to free run in all conditions
X24 POS	Automatic display of FASTEXT prompt row when logic 1

R1 MODE - auto increments to Register 2

T0, T1	Interlace/non-interlace 312/313 line control (see Table 5)
TCS ON	Text composite sync or direct sync select
$\overline{DEW}$/FULL FIELD	Field-flyback or full channel mode
EXT. PACKET ENABLE	Allocates 2.8 k memory per chapter
ACQ $\overline{ON}$/OFF	Aquisition circuits turned off when logic 1
$\overline{7 + P}$/8-BIT	7 bits with parity checking or 8-bit mode
VCS TO SCS	When logic 1 enables display of messages with 60 Hz input signal

R2 PAGE REQUEST ADDRESS - auto increments to Register 3

HAM. CHECK 27 28 8/30	When logic 1 enables hamming checking of extension packet 27, 28, 8/30
COL SC0 - SC2	Point to start column for page request data (see Table 4)
TB	Must be logic 0 for normal operation
ACQ CIRCUIT	Selects one of four acquisition circuits
BANK SELECT	Selects which bank of four pages is being accessed

R3 PAGE REQUEST DATA - does not auto increment (see Table 4)

R4 DISPLAY CHAPTER - auto increments to Register 5

determines which of the 8 pages is displayed

R5 NORMAL DISPLAY CONTROL - auto increments to Register 6

PON	Picture on
TEXT	Text on
COR	Contrast reduction on
BKGND	Background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R6 NEWSFLASH DISPLAY - auto increments to Register 7

PON	Picture on
TEXT	Text on
COR	Contrast reduction on
BKGND	Background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 DISPLAY MODE - does not auto increment

BOX ON 0	Boxing function allowed on Row 0
BOX ON 1-23	Boxing function allowed on Row 1-23
BOX ON 24	Boxing function allowed on Row 24
DOUBLE HEIGHT	To display double height text
BOTTOM HALF	To select bottom half of page when DOUBLE HEIGHT = 1
REVEAL ON	To reveal concealed text
CURSOR ON	To display cursor
STATUS TOP	Row 25 displayed above or below the main text

R8 ACTIVE CHAPTER - auto increments to Register 9

A0 to A2	Active chapter
CLEAR MEMORY	When set to 1, clears the display memory. This bit is automatically reset
VPS ENABLE	Set to 1 to enable VPS decoding

R9 CURSOR ROW - auto increments to Register 10

R0 to R4	Active row for data written to or read from memory via the I²C-bus

R10 CURSOR COLUMN - auto increments to Register 11 or 11B

C0 to C5	Active column for data written to or read from memory via the I²C-bus

R11 CURSOR DATA - does not auto increment

D0 to D7	Data read from/written to memory via I²C, at location pointed to by R8, R9 and R10. This location automatically increments each time R11 is accessed

R11B DEVICE STATUS - does not auto increment

VCS SIGNAL QUALITY	Indicates that the video signal quality is good and PLL is phase locked to input video when = 1
DATA QUALITY	If good data (either Teletext or VPS) is detected then = 1
ROM VER R0 to R4	Indicated language/ROM variant. See Table 7
$\overline{625}$/525 SYNC	If the input video is a 525 line signal when = 1

Table 5 Interlace/non-interlace 312/313 line control (T0 and T1)

T1	T0	RESULT
0	0	interlaced 312.5/312.5 lines
0	1	non-interlaced 312/313 lines (note 1)
1	0	non-interlaced 312/312 lines (note 1)
1	1	SCS mode (scan composite sync)

Note to Table 5

1 Reverts to interlaced mode if a newsflash or subtitle is being displayed.

Table 3 $\overline{ODD}$/EVEN/$\overline{DV}$ truth table

AUTO $\overline{ODD}$/EVEN	DISABLE $\overline{ODD}$/EVEN	$\overline{ODD}$/EVEN OUTPUT
0	0	$\overline{ODD}$/EVEN output continuously
0	1	$\overline{ODD}$/EVEN statically low
1	0	$\overline{ODD}$/EVEN active only when no TV picture displayed
1	1	Data Valid ($\overline{DV}$) output

Table 4 Register map for page requests (R3)

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{HOLD}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 4

1. Abbreviations are as for Table 1 except for DO CARE bits.
2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
3. If $\overline{HOLD}$ is set LOW, the page is held and not updated.
4. Columns auto-increment on successive I²C-bus transmission bytes.
5. 'X' = Don't care.

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional 2-pin design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone as illustrated in Fig.14.

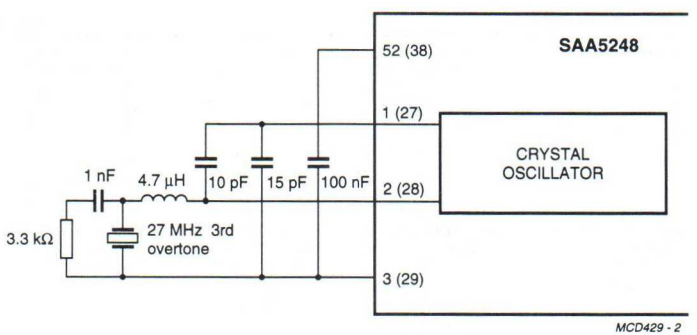


Fig.14 Crystal oscillator application diagram for SOT247; pins in parenthesis are for SOT208.

Table 6 Crystal characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)					
C1	series capacitance	–	1.7	–	pF
C0	parallel capacitance	–	5.2	–	pF
C_L	load capacitance	–	20	–	pF
Rr	resonant resistance	–	–	50	Ω
R1	series resistance	–	20	–	Ω
Xa	ageing	–	–	±5	10^{-6}/yr
Xj	adjustment tolerance	–	–	±25	10^{-6}
Xd	drift	–	–	±25	10^{-6}

Character sets

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character sets differ only in 13 national option characters as indicated in Table 9 with reference to their table position in the basic character matrix illustrated in Table 8. The SAA5248 automatically decodes transmission bits C12 to C14. Table 7 illustrates the character matrixs.

Character bytes are listed as transmitted from b1 to b7.

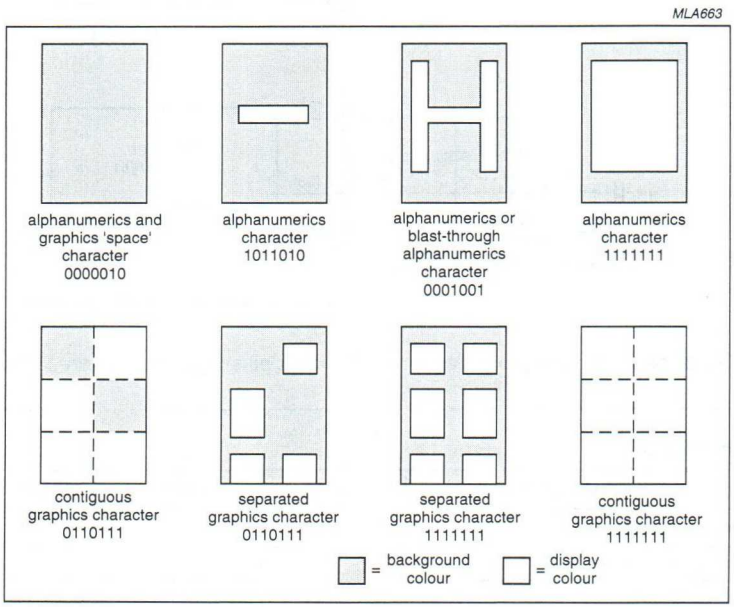


Fig.15 Character format.

Table 7 SAA5248P/E character data input decoding

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7	0	0	0	0	0	0	1	1	1		1		0	0	0	0	1	1
b_6	0	0	1	1	1	1	0	0	1		1		0	0	0	1	0	1
b_5	0	1	0	1	0	1	0	1	0		1		0	1	0	1	0	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0 alpha - numerics black	graphics black			0		§	P	°		p		@	É	é	à	i	Á
0 0 0 1	1 alpha - numerics red	graphics red	!		1		A	Q	a		q		—	é	ù	è	¿	À
0 0 1 0	2 alpha - numerics green	graphics green	"		2		B	R	b		r		¼	ä	à	â	ü	È
0 0 1 1	3 alpha - numerics yellow	graphics yellow	#		3		C	S	c		s		£	#	£	é	ç	Í
0 1 0 0	4 alpha - numerics blue	graphics blue	$		4		D	T	d		t		$	¤	$	ï	$	Ï
0 1 0 1	5 alpha - numerics magenta	graphics magenta	%		5		E	U	e		u		←	↑	ã	Ã	ø	Ó
0 1 1 0	6 alpha - numerics cyan	graphics cyan	&		6		F	V	f		v		→	↓	õ	Õ	Ø	Ò
0 1 1 1	7 alpha - numerics white **	graphics white	'		7		G	W	g		w		?	→	·	Ç	Ñ	Ú
1 0 0 0	8 flash	conceal display	(		8		H	X	h		x		‖	ö	ò	ô	ñ	æ
1 0 0 1	9 steady **	contiguous graphics **	)		9		I	Y	i		y		¾	å	è	û	è	Æ
1 0 1 0	10 end box **	separated graphics	*		:		J	Z	j		z		÷	ü	ì	ç	à	ð
1 0 1 1	11 start box	ESC *	+		;		K	Ä	k		ä		←	Ä	°	ë	á	Ð
1 1 0 0	12 normal height **	black back - ground **	,		<		L	Ö	l		ö		½	Ö	ç	ê	é	ø
1 1 0 1	13 double height	new back - ground	−		=		M	Ü	m		ü		→	Á	→	ù	í	Ø
1 1 1 0	14 SO *	hold graphics	.		>		N	^	n		ß		↑	Ü	↑	î	ó	þ
1 1 1 1	15 SI *	release graphics **	/		?		O	_	o		■		#	_	#	#	ú	Þ

MBA429

For character version number (00000) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Notes to Table 7

1. Control characters shown in Columns 0 and 1 are normally displayed as spaces.
2. Characters may be referred to by column and row, For example 2/5 refers to %.
3. Black represents displayed colour. White represents backgound.
4. Character rectangle shown as follows: 
5. The SAA5248 national option characters are illustrated in Table 9.
6. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters for combining with character 8/5.
7. National option characters will be developed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Table 9.
8. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.

Table 8 SAA5248 basic character matrix



Where: NC = national option character position.

Table 9 SAA5248 national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)													
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MEA559

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

Integrated VIP and Teletext with Background Memory Controller (IVT1.1BMCX)

SAA5249

FEATURES

- Complete teletext decoder featuring a background memory controller in a single 48-pin DIL package. Capable of storing of up to 512 teletext pages in an external DRAM, giving instant access to the teletext data.
- Automatic processing of extension packet 26 for widest possible language decoding. All our standard language options can be available, and the language option is readable via I²C-bus.
- 100% hardware compatible with the SAA5247 - plug-in replacement and with the possibility of extra market in those countries with packet 26 transmissions. Still pin-aligned to SAA5254 and SAA5244A.
- 100% software compatible with the SAA5247, and SAA5244A, except if the special OSD symbols were used. Also 100% software compatible to SAA5254. In all events there is a change to the ROM ID number.
- The device is pin-aligned with the other members of the new Philips teletext decoder family, i.e. SAA5281 and the SAA5254, making one hardware solution for the whole range.
- Low software overhead for the microprocessor.
- RGB interface to standard colour decoder ICs, push-pull output drive.

DESCRIPTION

The Integrated VIP and Teletext (IVT1.1BMCX) is a teletext decoder (contained within a single chip package) for decoding 625-line based World System Teletext transmissions. With its built-in background memory controller the device can store incoming teletext packets in the external 1M4 DRAM. With this large packet store which can be rapidly scanned, we can achieve near instantaneous access to all the pages transmitted by the broadcaster.

This version of the decoder also contains some extra hardware to process extension packet 26 automatically, extending the markets to which the TV chassis can be shipped and offering many more language options for the set maker.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	90	120	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1.0	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5249P/E	48	DIL	plastic	SOT240A
SAA5249GP/E	64	QFP (note 1)	plastic	SOT319

Note to the quick reference data

1. When using IR reflow soldering it is recommended that the Dry Packing instructions in the *Quality Reference Pocketbook (order number 9398 510 34011)* are followed.

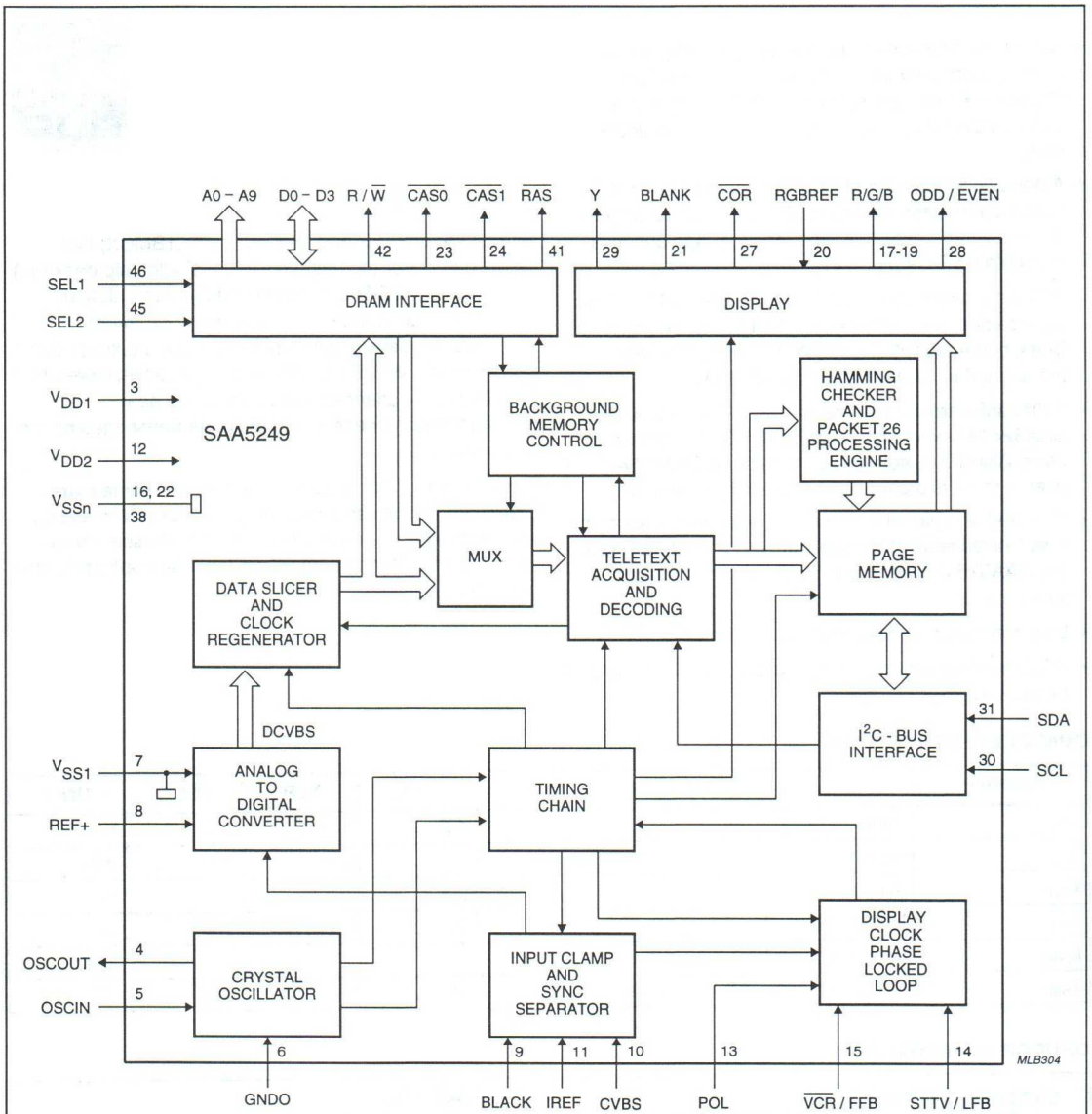


Fig.1 Block diagram for SOT240A (DIL48) package.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT240A	SOT319[1]	
n.c.	1	1	Not connected.
n.c.	2	2	Not connected.
V_{DD1}	3	25	+5 V supply.
OSCOUT	4	27	27 MHz crystal oscillator output.
OSCIN	5	28	27 MHz crystal oscillator input.
GNDO	6	29	0 V crystal oscillator ground.
V_{SS1}	7	12	0 V ground.
REF+	8	32	Positive reference voltage. This pin should be connected to ground via a 100 nF capacitor.
BLACK	9	35	Video black level storage pin. This pin should be connected to ground via a 100 nF capacitor.
CVBS	10	36	Composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor.
IREF	11	37	Reference current input pin, connected to ground via a 27 kΩ resistor.
V_{DD2}	12	38	+5 V supply.
POL	13	39	STTV/LFB/FFB polarity selection pin.
STTV/LFB	14	40	Sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode).
$\overline{VCR}$/FFB	15	42	PLL time constant switch/field input pin. Function controlled by an internal register bit (scan sync mode).
V_{SS2}	16	30	0 V ground.
REF–	–	31	Negative reference voltage. This pin should be connected to REF+ via a 100 nF capacitor.
R	17	49	Dot rate character output of the RED colour information.
G	18	50	Dot rate character output of the GREEN colour information.
B	19	51	Dot rate character output of the BLUE colour information.
RGBREF	20	52	Input DC voltage to define the output high level on the RGB pins.
BLANK	21	53	Dot rate fast blanking output.
V_{SS3}	22	54, 55	0 V ground; internally connected for SOT319.
$\overline{CAS0}$	23	56	Column address select to external DRAM for BMCX function.
$\overline{CAS1}$	24	57	Column address select to external DRAM for BMCX function for second DRAM where two 256 k x 4 devices are used.
A4	25	58	Address output to external DRAM for BMCX function.
A3	26	59	Address output to external DRAM for BMCX function.
$\overline{COR}$	27	60	Programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open drain output.
ODD/$\overline{EVEN}$	28	61	25 Hz output synchronized with the CVBS input field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents.

SYMBOL	PIN		DESCRIPTION
	SOT240A	SOT319[1]	
Y	29	62	Dot rate character output of teletext foreground colour information. Open drain output.
SCL	30	63	Serial clock input for I²C-bus. It can still be driven HIGH during power-down of the device.
SDA	31	64	Serial data port for the I²C-bus. Open drain output. It can still be driven HIGH during power-down of the device.
A5	32	4	Address output to external DRAM for BMCX function.
A2	33	5	Address output to external DRAM for BMCX function.
A6	34	6	Address output to external DRAM for BMCX function.
A1	35	8	Address output to external DRAM for BMCX function.
A7	36	9	Address output to external DRAM for BMCX function.
A0	37	11	Address output to external DRAM for BMCX function.
V_{SS4}	38	43	0 V ground.
A8	39	13	Address output to external DRAM for BMCX function.
A9	40	14	Address output to external DRAM for BMCX function.
$\overline{RAS}$	41	15	Row address select to external DRAM.
R/$\overline{W}$	42	18	Read/$\overline{write}$ for external DRAM.
D2	43	19	Data input/output for external DRAM.
D0	44	20	Data input/output for external DRAM.
SEL2	45	21	RAM select input to choose external DRAM size.
SEL1	46	22	RAM select input to choose external DRAM size.
D3	47	23	Data input/output for external DRAM.
D1	48	24	Data input/output for external DRAM.

Note to the pinning

1. The remaining pins for SOT319 are not connected.

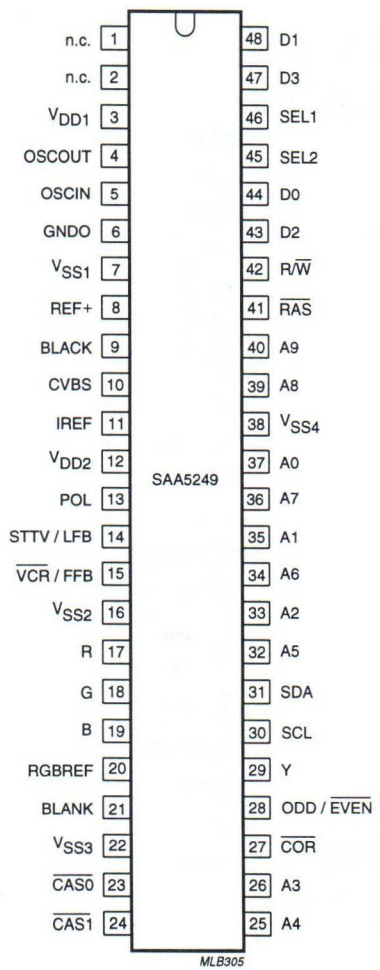


Fig.2 Pin configuration; SOT240A (DIL48).

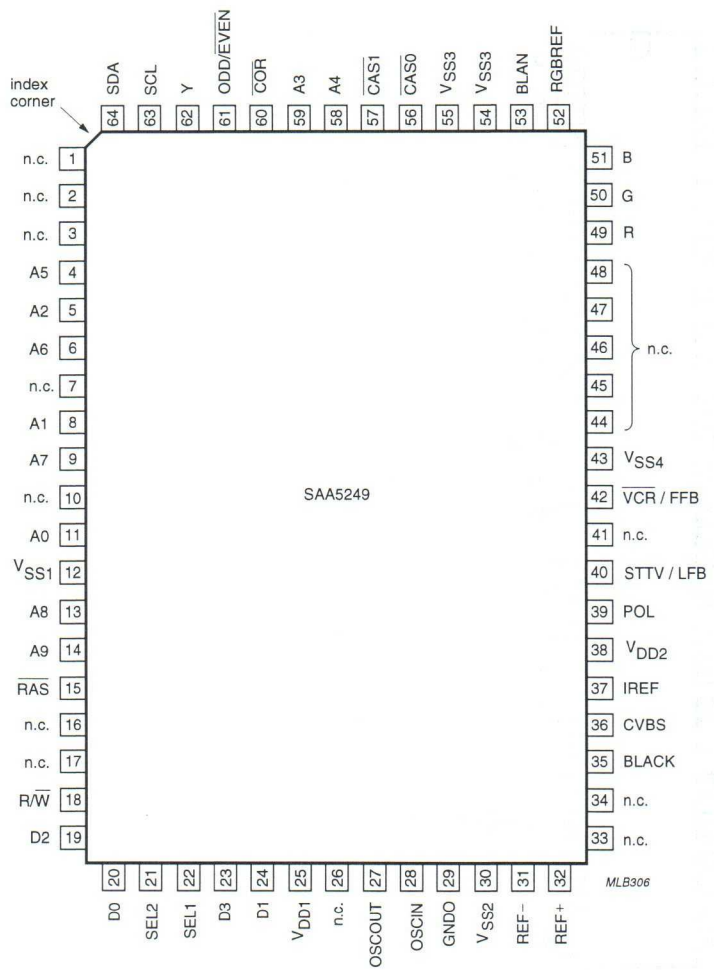


Fig.3 Pin configuration; SOT319 (QFP64).

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	−0.3	+6.5	V
V_I	input voltage (any input)	−0.3	V_{DD}+0.5	V
V_O	output voltage (any output)	−0.3	V_{DD}+0.5	V
I_O	output current (each output)	−	±10	mA
I_{IOK}	DC input or output diode current	−	±20	mA
T_{amb}	operating ambient temperature	−20	+70	°C

QUALITY AND RELIABILITY

This device will meet Philips Semiconductors General Quality Specification for Business group *Consumer Integrated Circuits SNW-FQ-611-Part E*. The principal requirements are shown in Tables 1 to 4.

Group A

Table 1 Acceptance tests per lot.

TEST	CONDITIONS	REQUIREMENTS(1)
Mechanical		cumulative target: < 100 ppm
Electrical		cumulative target: < 100 ppm

Group B

Table 2 Processability tests (by package family).

TEST	CONDITIONS	REQUIREMENTS(1)
Solderability		< 7% LTPD
Mechanical		< 15% LTPD
Solder heat resistance		< 15% LTPD

Group C

Table 3 Reliability tests (by process family).

TEST	CONDITIONS	REQUIREMENTS(1)
Operational life	168 hours at T_j = 150 °C	< 1500 FPM; equivalent to < 100 FITS at T_j = 70 °C
Humidity life	temperature, humidity, bias (1000 hours, 85 °C, 85% RH or equivalent test)	< 2000 FPM
Temperature cycling performance	$T_{stg(min)}$ to $T_{stg(max)}$	< 2000 FPM

Table 4 Reliability tests (by device type).

TEST	CONDITIONS	REQUIREMENTS(1)
ESD and latch-up	ESD Human body model 2000 V, 100 pF, 1.5 kΩ	< 15% LTPD
	ESD Machine model 200 V, 100 pF, 1.5 kΩ	< 15% LTPD
	latch-up 100 mA, 1.5 × V_{DD} (absolute maximum)	< 15% LTPD

Notes to Tables 1 to 4.

1. ppm = fraction of defective devices, in parts per million.
   LTPD = Lot Tolerance Percent Defective.
   FPM = fraction of devices failing at test condition, in Failures Per Million.
   FITS = Failures In Time Standard.

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −20 to +70 °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DDtot}	total supply current		–	90	120	mA
Inputs						
CVBS						
V_{sync}	sync amplitude		0.1	0.3	0.6	V
$t_{d(sync)}$	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		−150	0	+150	ns
$\Delta t_{d(sync)}$	change in sync delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{vid(p-p)}$	video input amplitude (peak-to-peak value)		0.7	1.0	1.4	V
	display PLL catching range		±7	–	–	%
Z_{source}	source impedance		–	–	250	Ω
C_I	input capacitance		–	–	10	pF
IREF						
R_{gnd}	resistor to ground		–	27	–	kΩ
POL						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
LFB						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
I_I	input current	note1	−1	–	+1	mA
$t_{d(LFB)}$	delay between LFB front edge and input video line sync		–	250	–	ns
$\overline{VCR}$/FFB						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
I_I	input current	note1	−1	–	+1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGBREF (NOTE 2)						
V_{IL}	LOW level input voltage		−0.3	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
I_{DC}	DC current		–	–	10	mA
SEL1 AND SEL2						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
SCL						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
f_{SCL}	clock frequency		0	–	100	kHz
t_r	input rise time	10% to 90%	–	–	2	μs
t_f	input fall time	90% to 10%	–	–	2	μs
C_I	input capacitance		–	–	10	pF
Inputs/outputs						
CRYSTAL OSCILLATOR (OSCIN; OSCOUT)						
f_{XTAL}	crystal frequency		–	27	–	MHz
G_v	small signal voltage gain		3.5	–	–	
G_m	mutual conductance	f = 100 kHz	1.5	–	–	mA/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	–	5	pF
BLACK						
C_{blk}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
SDA						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	10% to 90%	–	–	2	μs
t_f	input fall time	90% to 10%	–	–	2	μs
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	3 V to 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
D0 TO D3						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current		−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
t_r	output rise time	0.6 V to 2.2 V	–	–	20	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	20	ns
C_L	load capacitance		–	–	50	pF
Outputs						
STTV						
G_{stt}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{tcs}	TCS amplitude		0.2	0.3	0.45	V
V_{DCs}	DC shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive current		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
A0 TO A9 ADDRESS OUTPUT TO MEMORYA0 TO A9						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.6 V to 2.2 V	–	–	20	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	20	ns
R/$\overline{W}$, $\overline{CAS0}$ AND $\overline{CAS1}$						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.6 V to 2.2 V	–	–	20	ns
t_f	output fall time	2.2 V to 0.6 V	–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R, G AND B						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = –1.6 mA; RGBREF ≤ V_{DD}–2 V	RGBREF – 0.25	RGBREF	RGBREF + 0.25	V
$\|Z_o\|$	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
I_{DC}	DC current		–	–	–3.3	mA
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
BLANK						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA; V_{DD} = 4.5 V	1.1	–	–	V
V_{OH}	HIGH level output voltage	I_{OH} = 0 mA; V_{DD} = 5.5 V	–	–	2.8	V
V_{OH}	allowed voltage at pin	with external pull-up	–	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
ODD/$\overline{\text{EVEN}}$						
V_{OL}	LOW level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
$\overline{\text{COR}}$ AND Y (OPEN DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V
V_{OL}	output voltage LOW	I_{OL} = 5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} – 0.5 V and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
t_{skew}	skew delay between display outputs R, G, B, $\overline{\text{COR}}$, Y and BLANK		–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
DRAM INTERFACE						
t_{RC}	read or write cycle time		344	380	415	ns
t_{RP}	$\overline{RAS}$ precharge time		125	140	155	ns
t_{RAS}	$\overline{RAS}$ pulse width		194	210	230	ns
t_{CAS}	$\overline{CAS}$ pulse width		113	133	153	ns
t_{ASR}	row address set-up time		30	60	80	ns
t_{RAH}	row address hold time		50	60	92	ns
t_{ASC}	column address set-up time		50	60	75	ns
t_{CAH}	column address hold time		50	60	70	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time		130	148	160	ns
t_{RAD}	$\overline{RAS}$ to column address delay time		60	74	105	ns
t_{RSH}	$\overline{RAS}$ hold time		15	60	70	ns
t_{CSH}	$\overline{CAS}$ hold time		260	286	300	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time		60	70	80	ns
t_{DZO}	$\overline{CAS}$ set-up time from data input		200	225	280	ns
t_r, t_f	rise and fall times		10	15	20	ns
t_{WCS}	write set-up time		193	212	235	ns
t_{WCH}	write command hold time		116	137	150	ns
t_{DS}	data input set-up time		193	212	235	ns
t_{DH}	data input hold time		42	62	80	ns
t_{RAC}	access time from $\overline{RAS}$		165	183	220	ns
t_{CAC}	access time from $\overline{CAS}$		0	35	40	ns
t_{AA}	access time from address		95	108	120	ns
t_{RCS}	read command set-up time		193	212	235	ns
t_{RCH}	read command hold time to $\overline{CAS}$		0	10	20	ns
t_{RRH}	read command hold time to $\overline{RAS}$		55	65	100	ns
t_{RAL}	column address to $\overline{RAS}$ lead time		90	133	150	ns
t_{OFF1}	output buffer turn-off time		20	30	40	ns
t_{CDD}	$\overline{CAS}$ to data input delay time		25	35	45	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I^2C-BUS						
t_{LOW}	clock LOW period		4	–	–	µs
t_{HIGH}	clock HIGH period		4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;STA}$	START hold time		4	–	–	µs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	µs

Notes to the characteristics

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ±1 mA.
2. RGBREF is the positive supply pin for the RGB output pins and it must be able to source the I_{OH} current from the R, G and B pins. The leakage specification on RGBREF only applies when there is no current load on the RGB pins.

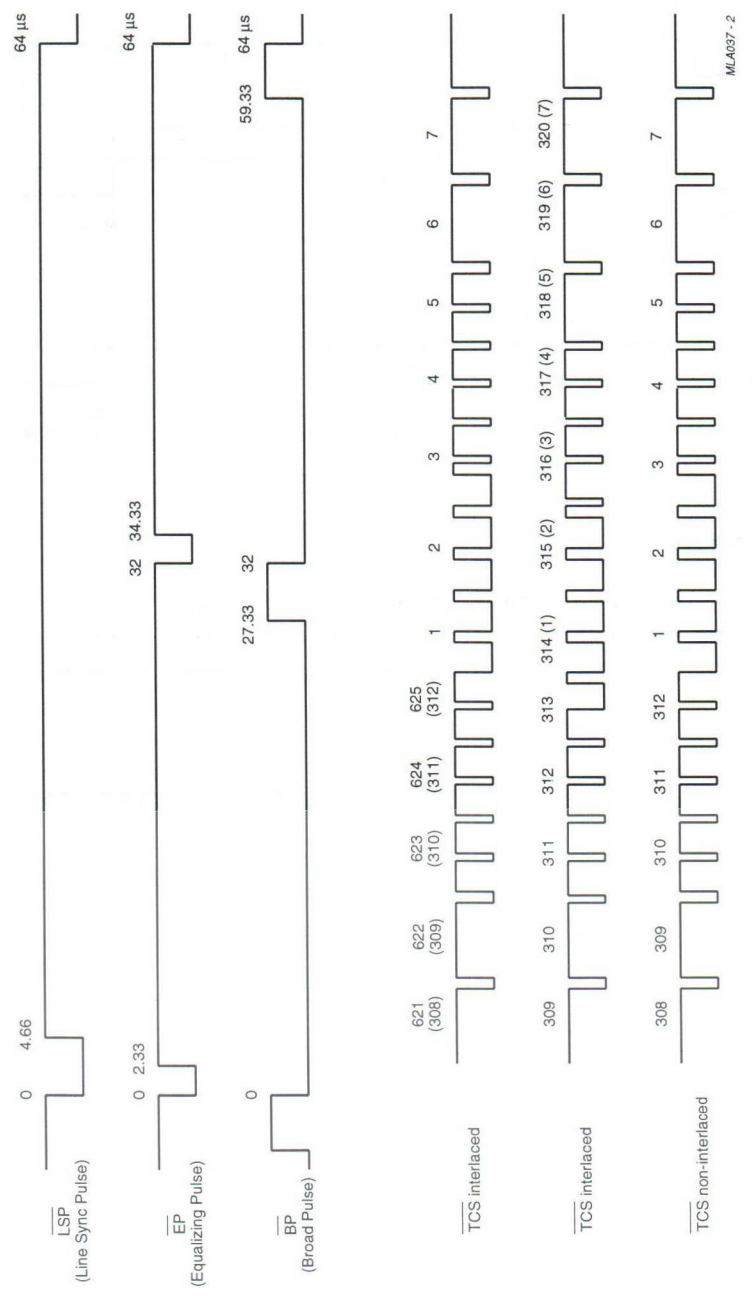
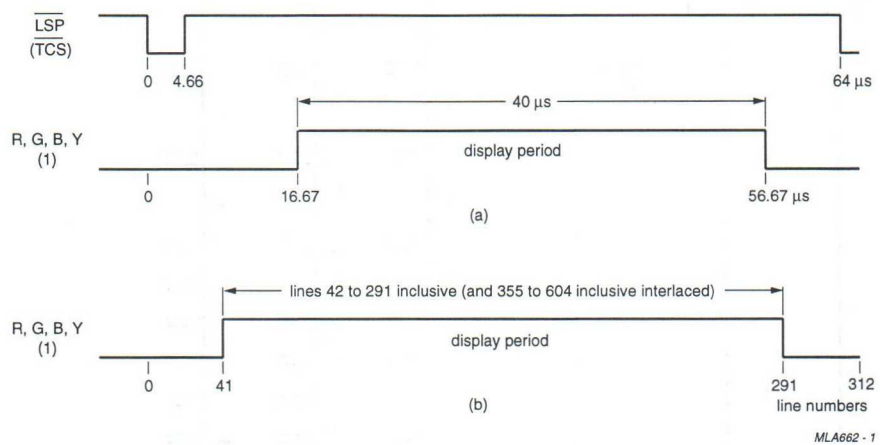


Fig.4 Composite sync waveforms.



(1) Also BLANK in character and box blanking.

Fig.5 Display output timing (a) line rate (b) field rate.

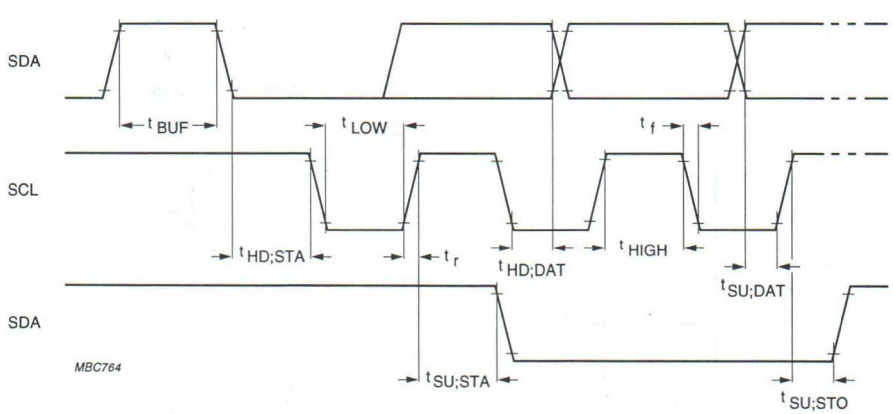


Fig.6 I²C-bus timing.

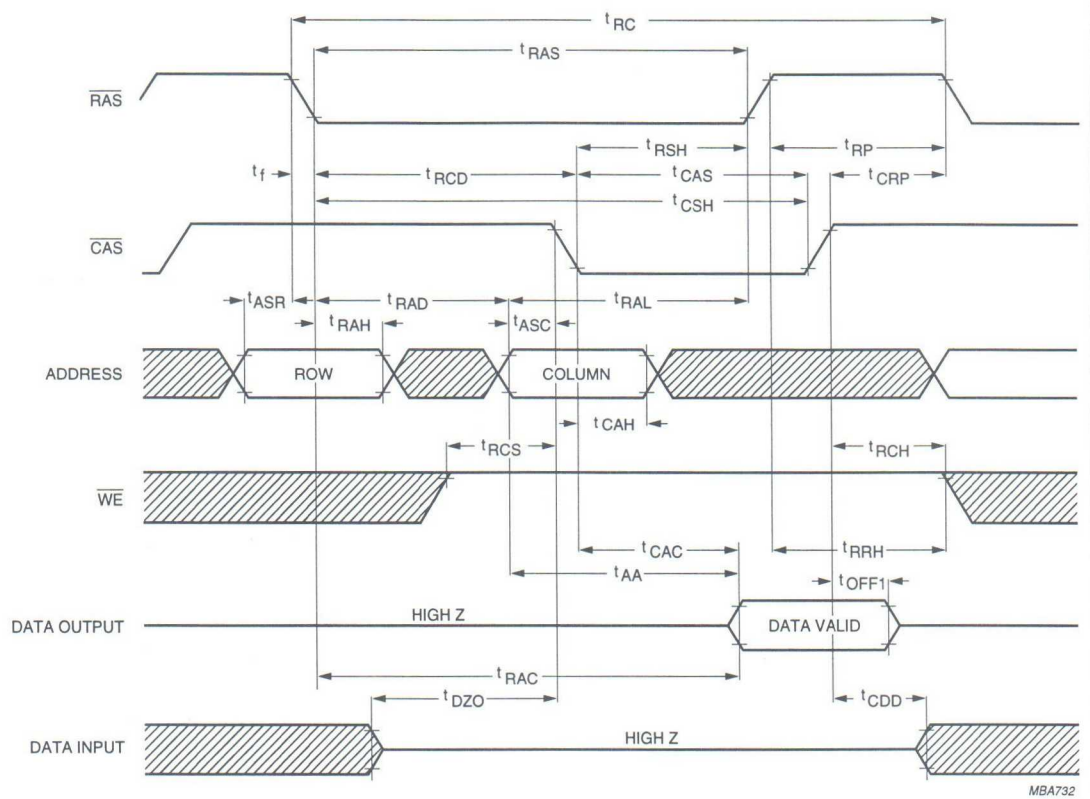


Fig.7 DRAM interface timing; read cycle.

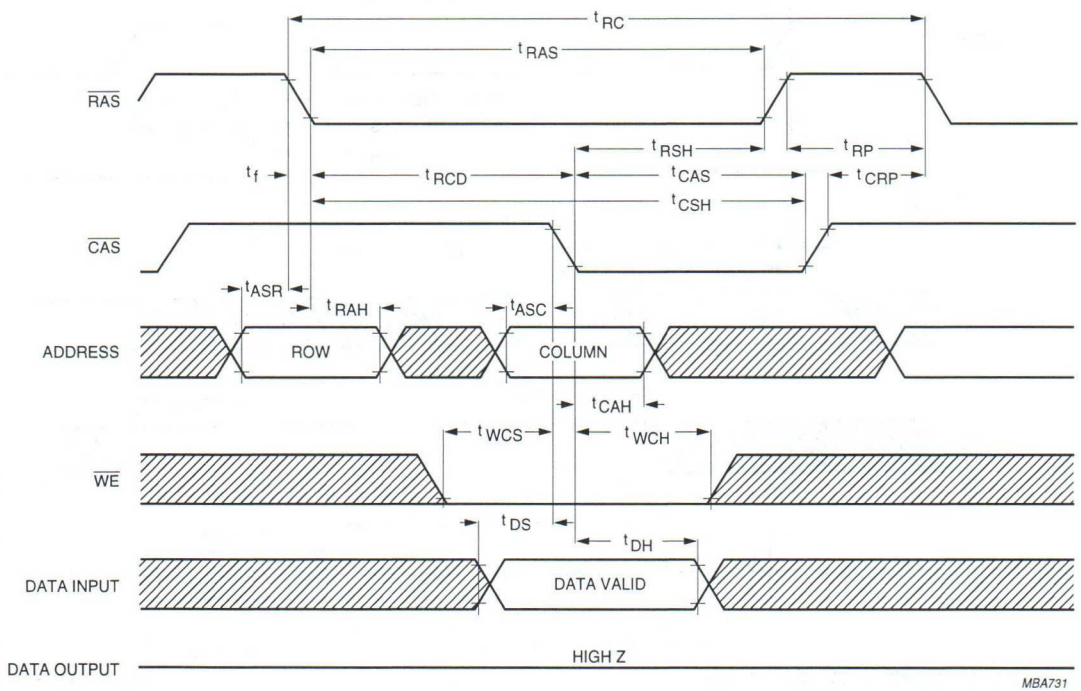


Fig.8 DRAM interface timing; write cycle.

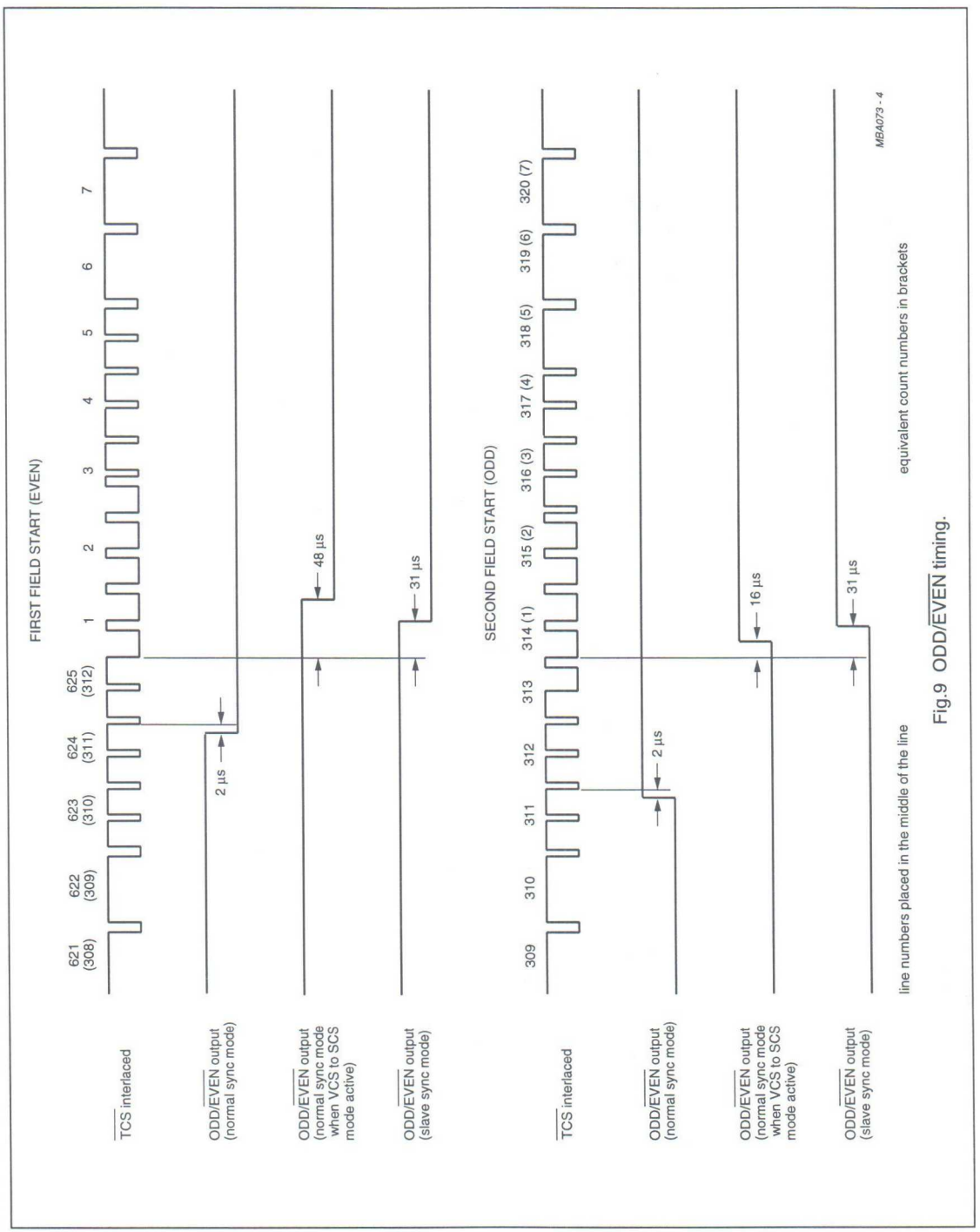


Fig.9 ODD/$\overline{\text{EVEN}}$ timing.

APPLICATION INFORMATION

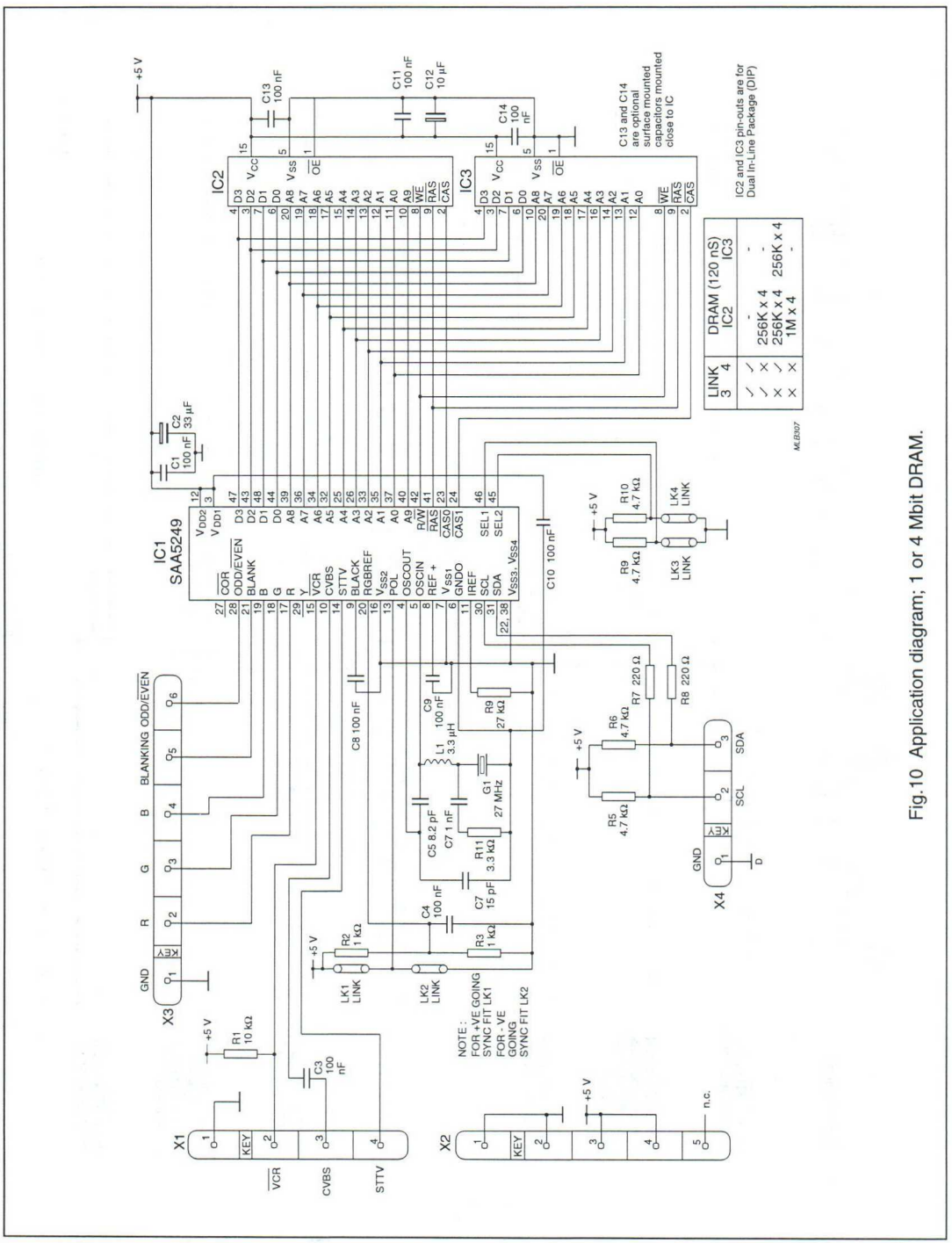


Fig.10 Application diagram; 1 or 4 Mbit DRAM.

IVT1.1BMCX page memory organization

The organization of the page memory is illustrated by Fig.11. The IVT1.1BMCX provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; Row 24 is the extra row available for software generated status messages and FLOF/FASTEXT prompt information.

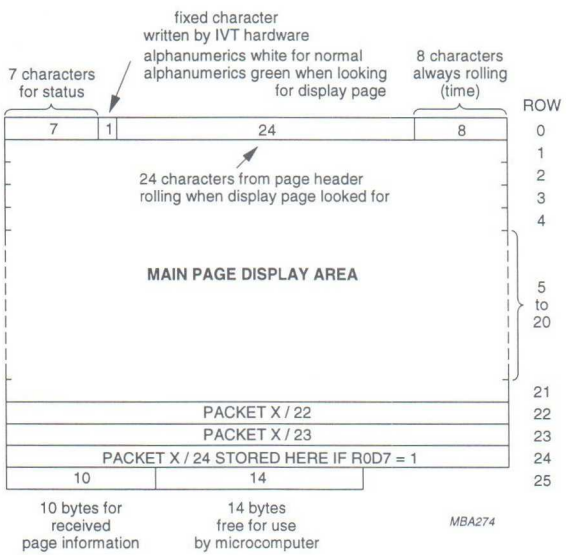


Fig.11 Basic page memory organization.

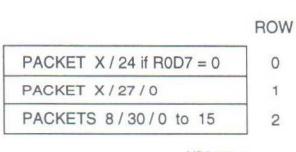


Fig.12 Organization of the extension memory.

REMARK TO FIG.11

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by IVT1.1BMCX to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of Row 25 contain control data relating to the received page as shown in Table 5. The remaining 14 bytes are free for use by the microcomputer.

Table 5 Row 25 received control data format.

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Table 6 Page number and sub-code for Table 5.

Page number	
MAG	magazine
PU	page units
PT	page tens
PBLF	page being looked for
$\overline{\text{FOUND}}$	LOW for page has been found
HAM.ER	Hamming error in corresponding byte
Page sub-code	
MU	minutes units
MT	minutes tens
HU	hours units
HT	hours tens
C4-C14	transmitted control bits

Register maps

IVT1.1BMCX mode registers R0 to R11 are shown in Table 7. R0 to R10 are WRITE only; R11 is READ/WRITE. Register map (R3), for page requests, is shown in detail in Table 9.

Table 7 Register map (notes 1 to 5).

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Adv. control	0	X24 POS	FREE RUN PLL	AUTO $\overline{\text{ODD/EVEN}}$	DISABLE HDR ROLL	DISPLAY SRATUS ROW ONLY	DISABLE $\overline{\text{ODD/EVEN}}$	–	$\overline{\text{R11}}$/R11B SELECT
Mode	1	VCS TO SCS	$\overline{7+P}$/ 8-BIT	ACQ $\overline{\text{ON}}$/OFF	DISABLE PKT 26	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0
Page request address	2	–	–	–	–	TB	START COLUM N SC2	START COLUMN SC1	START COLUMN SC0
Page request data	3	–	–	CLEAR B.M.	PRD4	PRD3	PRD2	PRD1	PRD0
		–	–	–	–	–	–	–	–
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS $\overline{\text{BTM}}$ TOP	CURSOR ON	$\overline{\text{CONCEAL}}$ REVEAL ON	$\overline{\text{TOP}}$/BTM HALF	$\overline{\text{SINGLE}}$ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
		–	–	–	–	–	–	–	–
Cursor row	9	–	CLEAR MEM.	A0	R4	R3	R2	R1	R0
Cursor column	10	–	–	C5	C4	C3	C2	C1	C0
Cursor data	11	D7	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{\text{625}}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TEXT SIGNAL QUALITY	VCS SIGNAL QUALITY

Notes to Table 7

1. The dash (–) indicates these bits are inactive and must be written to logic 0 for future compatibility.
2. All bits in registers R0 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of Registers R1, R5 and R6 which are set to logic 1.
3. All memory is cleared to space (00100000) on power-up, except Row 0 Column 7 Chapter 0, which is alpha white (00000111) as the acquisition circuit is enabled but the page is on hold.
4. TB must be set to logic 0 for normal operation.
5. The I^2C slave address is 0010001.

Table 8 Register description.

R0 ADVANCED CONTROL - auto increments to Register 1	
$\overline{R11}$/R11B SELECT	Selects reading of R11 or R11B.
DISABLE ODD/$\overline{EVEN}$	Forces ODD/$\overline{EVEN}$ output LOW when logic 1.
DISPLAY STATUS ROW	When SET = 1 and R1D6 = 1 open (8-bit mode) then all the text display is blanked out apart from the status row, this allows the page memory to be used for non-textural data, such as in the German TOP system.
DISABLE HDR ROLL	Disables green rolling header and time.
AUTO ODD/$\overline{EVEN}$	When set forces ODD/$\overline{EVEN}$ LOW if any TV picture displayed, if DISABLE ODD/$\overline{EVEN}$ = 0.
FREE RUN PLL	Will force the PLL to free run in all conditions.
X24 POS	Automatic display of FASTEXT prompt row when logic 1.
R1 MODE - auto increments to Register 2	
T0, T1	Interlace/non-interlace 312/313 line control (see Table 10).
TCS ON	Text composite sync or direct sync select (see Table 10 for FFB mode selection).
$\overline{DEW}$/FULL FIELD	Field-flyback or full-channel mode.
DISABLE PKT 26	Disable automatic processing of packet 26.
ACQ $\overline{ON}$/OFF	Acquisition circuits turned off when logic 1.
$\overline{7 + P}$/8-BIT	7 bits with parity checking or 8-bit mode.
VCS TO SCS	When logic 1 enables display of messages with 60 Hz input signal.
R2 PAGE REQUEST ADDRESS - auto increments to Register 3	
COL SCO - SC2	Point to start column for page request data (see Table 9).
TB	Must be logic 0 for normal operation.
R3 PAGE REQUEST DATA - does not auto increment (see Table 9)	
CLEAR B.M.	When set to logic 1. Useful when transmission channel changes.
R5 NORMAL DISPLAY CONTROL - auto increments to Register 6	
R6 NEWSFLASH/SUBTITLE DISPLAY CONTROL - auto increments to Register 7; note 1	
PON	Picture on.
TEXT	Text on.
COR	Contrast reduction on.
BKGND	Background colour on.

R7 DISPLAY MODE - does not auto increment	
BOX ON 0	Boxing function allowed on Row 0.
BOX ON 1-23	Boxing function allowed on Rows1 to 23.
BOX ON 24	Boxing function allowed on Row 24.
DOUBLE HEIGHT	To display double height text.
BOTTOM HALF	To select bottom half of page when DOUBLE HEIGHT = 1.
REVEAL ON	To reveal concealed text.
CURSOR ON	To display cursor.
STATUS TOP	Row 25 displayed above or below the main text.
R9 CURSOR ROW - auto increments to Register 10	
R0 to R4	Active row for data written to or read from memory via the I^2C-bus.
A0	Selects display memory page (when = 0) or extension packet memory (when = 1).
CLEAR MEM.	When set to 1, clears the display memory. This bit is automatically reset.
R10 CURSOR COLUMN - auto increments to Register 11 or 11B	
C0 to C5	Active column for data written to or read from memory via the I^2C-bus.
R11 CURSOR DATA - does not auto increment	
D0 to D7	Data read from/written to memory via I^2C-bus, at location pointed to by R9 and R10. This location automatically increments each time R11 is accessed.
R11B DEVICE STATUS - does not auto increment	
VCS SIGNAL QUALITY	Indicates that the video signal quality is good and PLL is phase locked to input video when = 1.
TEXT SIGNAL QUALITY	If a good teletext signal is being received when logic 1.
ROM VER R0 to R4	Indicated language/ROM variant. For Western European = 11000.
$\overline{625}$/525 SYNC	If the input video is a 525 line signal when logic 1.

Note to Table 8

1. These functions have IN and OUT referring to inside and outside the boxing function respectively.

Table 9 Register map for page requests (R3); notes 1 to 5.

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	DO CARE Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	DO CARE Page tens	PT3	PT2	PT1	PT0
2	DO CARE Page units	PU3	PU2	PU1	PU0
3	DO CARE Hours tens	X	X	HT1	HT0
4	DO CARE Hours units	HU3	HU2	HU1	HU0
5	DO CARE Minutes tens	X	MT2	MT1	MT0
6	DO CARE Minutes units	MU3	MU2	MU1	MU0

Notes to Table 9

1. Abbreviations are as for Table 5 except for DO CARE bits.
2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, normal or timed page selection.
3. If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
4. Columns auto-increment on successive I^2C-bus transmission bytes.
5. X = Don't care.

Table 10 Interlace/non-interlace 312/313 line control and ODD/EVEN field detection option; notes 1 and 2.

TCS ON FFB MODE	T1	T0	RESULT
X	0	0	interlaced 312.5/312.5 lines
X	0	1	non-interlaced 312/313 lines (note 1)
X	1	0	non-interlaced 312/313 lines (note 1)
0	1	1	SCS (scan composite sync) mode: FFB leading edge in first broad pulse of field
1	1	1	SCS (scan composite sync) mode: FFB leading edge in second broad pulse of field

Notes to Table 10

1. Reverts to interlaced mode if a newsflash or subtitle is being displayed.
2. X = Don't care.

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional 2-pin design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone as illustrated in Fig.13.

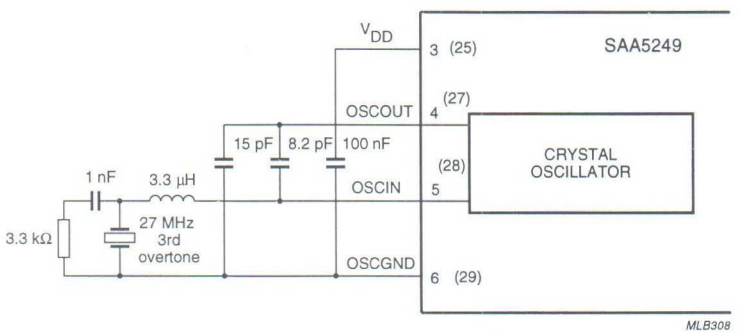


Fig.13 Crystal oscillator application diagram for SOT240A; pins in parenthesis are for SOT319.

Table 11 Crystal characteristics (see Fig.13).

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)					
C1	series capacitance	–	1.7	–	pF
C0	parallel capacitance	–	5.2	–	pF
C_L	load capacitance	–	20	–	pF
R_r	resonance resistance	–	–	50	Ω
R1	series resistance	–	20	–	Ω
X_a	ageing	–	–	±5	10^{-6}/year
X_j	adjustment tolerance	–	–	±25	10^{-6}
X_d	drift	–	–	±25	10^{-6}

CHARACTER SETS

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character sets differ only in 13 national option characters as indicated in the Tables 16, 17 and 18 with reference to their table position in the basic character matrix illustrated in Table 15. The IVT1.1BMCX automatically decodes transmission bits C12 to C14. Tables 12, 13 and 14 illustrate the character matrixes.

Character bytes are listed as transmitted from b1 to b7.

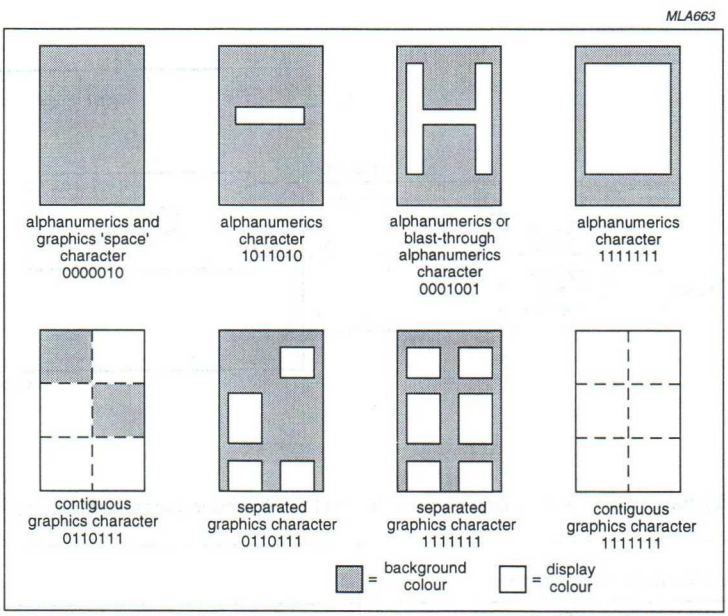


Fig.14 Character format.

Table 12 SAA5249P/E character data input decoding, West European languages; notes 1 to 9.
For character version number (11000) see Register 11B.

BITS b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0	0	0	0	0	0	0	0	0	alpha - numerics black	graphics black			0		§	P	°		p		@	É	é	à	i	Á
0	0	0	1	0	0	0	1	1	alpha - numerics red	graphics red	!		1		A	Q	a		q		—	é	ù	è	¿	À
0	0	1	0	0	0	1	0	2	alpha - numerics green	graphics green	"		2		B	R	b		r		¼	ä	à	ä	ü	È
0	0	1	1	0	0	1	1	3	alpha - numerics yellow	graphics yellow	#		3		C	S	c		s		£	#	£	é	ç	Í
0	1	0	0	0	1	0	0	4	alpha - numerics blue	graphics blue	$		4		D	T	d		t		$	¤	$	ï	$	Ï
0	1	0	1	0	1	0	1	5	alpha - numerics magenta	graphics magenta	%		5		E	U	e		u		←	↑	ã	Ã	ª	Ó
0	1	1	0	0	1	1	0	6	alpha - numerics cyan	graphics cyan	&		6		F	V	f		v		→	↓	õ	Õ	º	Ò
0	1	1	1	0	1	1	1	7	alpha - numerics white (2)	graphics white	'		7		G	W	g		w		↑	→	·	Ç	Ñ	Ú
1	0	0	0	1	0	0	0	8	flash	conceal display	(		8		H	X	h		x		↓	ö	ò	ô	ñ	æ
1	0	0	1	1	0	0	1	9	steady (2)	contiguous graphics (2)	)		9		I	Y	i		y		¾	å	è	û	è	Æ
1	0	1	0	1	0	1	0	10	end box (2)	separated graphics	*		:		J	Z	j		z		÷	ü	ì	ç	à	ð
1	0	1	1	1	0	1	1	11	start box	ESC (1)	+		;		K	Ä	k		ä		←	Ä	°	ë	á	Ð
1	1	0	0	1	1	0	0	12	normal height (2)	black back - ground (2)	,		<		L	Ö	l		ö		½	Ö	ç	ê	é	ø
1	1	0	1	1	1	0	1	13	double height	new back - ground	−		=		M	Ü	m		ü		→	Á	→	ù	í	Ø
1	1	1	0	1	1	1	0	14	SO (1)	hold graphics	.		>		N	^	n		ß		↑	Ü	↑	î	ó	þ
1	1	1	1	1	1	1	1	15	SI (1)	release graphics (2)	/		?		O	_	o		■		#	_	#	#	ú	Þ

MBA429

Table 13 SAA5249P/H character data input decoding, West European languages; notes 1 to 9.
For character version number (11001) see Register 11B.

BITS b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
									0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
									0	0	0	0	0	0	1	1	1		1		0	0	1	1	1	1
									0	0	1	1	1	1	0	0	0		1		0	0	0	0	1	1
									0	0	1	1	1	1	0	1	1		1		0	0	0	1	0	1
									0	1	0	1	0	1	1	0	0		1		0	1	1	0	0	1
									0	1	1	1	1	1	1	0	1		1		0	1	1	0	1	0
									0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0	0	0	0	0	0	0	0	0	alpha - numerics black	graphics black																
0	0	0	0	0	0	0	1	1	alpha - numerics red	graphics red																
0	0	0	0	0	0	1	0	2	alpha - numerics green	graphics green																
0	0	0	0	0	0	1	1	3	alpha - numerics yellow	graphics yellow																
0	0	0	0	0	1	0	0	4	alpha - numerics blue	graphics blue																
0	0	0	0	0	1	0	1	5	alpha - numerics magenta	graphics magenta																
0	0	0	0	0	1	1	0	6	alpha - numerics cyan	graphics cyan																
0	0	0	0	0	1	1	1	7	alpha - numerics white (2)	graphics white																
0	0	0	0	1	0	0	0	8	flash	conceal display																
0	0	0	0	1	0	0	1	9	steady (2)	contiguous graphics (2)																
0	0	0	0	1	0	1	0	10	end box (2)	separated graphics																
0	0	0	0	1	0	1	1	11	start box	ESC (1)																
0	0	0	0	1	1	0	0	12	normal height (2)	black back - ground (2)																
0	0	0	0	1	1	0	1	13	double height	new back - ground																
0	0	0	0	1	1	1	0	14	SO (1)	hold graphics																
0	0	0	0	1	1	1	1	15	SI (1)	release graphics (2)																

MLA961

Table 14 SAA5249P/T character data input decoding, West European and Turkish languages; notes 1 to 9.
For character version number (11010) see Register 11B.

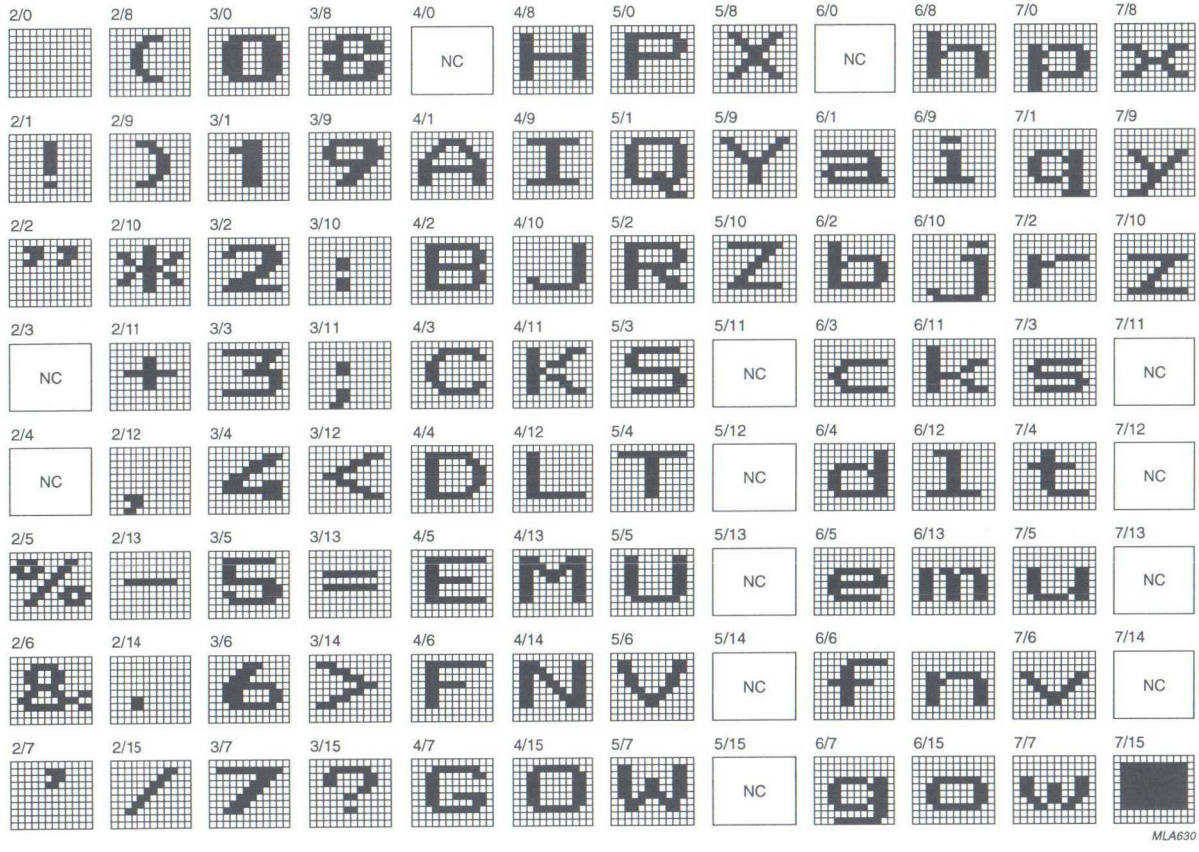
BITS b_4 b_3 b_2 b_1	row	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
b_8		0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7		0	0	0	0	0	0	1	1	1		1		0	0	1	1	1	1
b_6		0	0	1	1	1	1	0	0	1		1		0	0	0	0	1	1
b_5		0	1	0	1	1	1	0	1	0		1		0	1	0	1	0	1
0 0 0 0	0	alpha - numerics black	graphics black																
0 0 0 1	1	alpha - numerics red	graphics red																
0 0 1 0	2	alpha - numerics green	graphics green																
0 0 1 1	3	alpha - numerics yellow	graphics yellow																
0 1 0 0	4	alpha - numerics blue	graphics blue																
0 1 0 1	5	alpha - numerics magenta	graphics magenta																
0 1 1 0	6	alpha - numerics cyan	graphics cyan																
0 1 1 1	7	alpha - numerics white [2]	graphics white																
1 0 0 0	8	flash	conceal display																
1 0 0 1	9	steady [2]	contiguous graphics [2]																
1 0 1 0	10	end box [2]	separated graphics																
1 0 1 1	11	start box	ESC [1]																
1 1 0 0	12	normal height [2]	black back - ground [2]																
1 1 0 1	13	double height	new back - ground																
1 1 1 0	14	SO [1]	hold graphics																
1 1 1 1	15	SI [1]	release graphics [2]																

MBA431

Notes to Tables 12, 13 and 14

1. These control characters are reserved for compatibility with other data codes.
2. These control characters are presumed before each row begins.
3. Control characters shown in Columns 0 and 1 are normally displayed as spaces.
4. Characters may be referred to by column and row (for example 2/5 refers to %).
5. Black represents displayed colour. White represents background.
6. The SAA5249 national option characters are illustrated in Tables 16, 17 and 18.
7. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters for combining with character 8/5 (E, H and T codes only. Characters 5/12, 5/13, 5/14 and 5/15 are combined with 5/11 (S code only).
8. National option characters will be displayed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Tables 16, 17 and 18.
9. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.

Table 15 SAA5249 basic character matrix; note 1.



Note to Table 15

1. Where: NC = national option character position.

Table 16 SAA5249P/E national option character set.

LANGUAGE	PHCB [1]			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

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Note to Table 16

1. PHCB are the Page Header Control Bits. Other combinations default to English.

Table 17 SAA5249P/H national option character set.

LANGUAGE	PHCB [1]			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
POLISH	0	0	0	#	ń	ą	Ź	Ś	Ł	ć	ó	ę	ż	ś	ł	ź
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
SERBO-CROAT	1	0	1	#	½	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECHOSLOVAKIA	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN	1	1	1	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

MLA966

Note to Table 17

1. PHCB are the Page Header Control Bits. Other combinations default to German. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 15.

Table 18 SAA5249P/T national option character set.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
TURKISH	1	1	0	Ţ	ğ	İ	Ş	Ö	Ç	Ü	Ğ	ı	ş	ö	ç	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MBA430

Note to Table 18

1. PHCB are the Page Header Control Bits. Other combinations default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 15.

INTERFACE FOR DATA ACQUISITION AND CONTROL (for multi-standard teletext systems)

GENERAL DESCRIPTION

The SAA5250 is a CMOS Interface for Data Acquisition and Control (CIDAC) designed for use in conjunction with the Video Input Processor (SAA5230) in a multi-standard teletext decoder. The device retrieves data from a user selected channel (channel demultiplexer), as well as providing control signals and consecutive addressing space necessary to drive a 2 K bytes buffer memory.

The system operates in accordance with the following transmission standards:

- French Didon Antiope specification D2 A4-2 (DIDON)
- North American Broadcast Teletext specification (NABTS)
- U.K. teletext (CEEFAX)

Features

- 7,5 MHz maximum conversion rate
- Three prefixes; DIDON, NABTS and U.K. teletext (CEEFAX)
- Mode without prefix
- Internal calculation of the validation (VAL) and colour burst blanking (CBB) signals, if programmed
- Programmable framing code and channel numbers
- Error parity calculation or not (odd parity)
- Hamming processing of the prefix byte
- Full channel or VBI reception
- Slow/fast mode (detection of page flags or not)
- Maximum/default format up to 63 bytes
- Addressing space of 2 K bytes of the static memory
- Multiplexed address/data information is compatible with Motorola or Intel microcontrollers
- CIDAC is 'MOTEL' compatible

PACKAGE OUTLINES

SAA5250P: 40-lead DIL; plastic (SOT129).
SAA5250T: 40-lead mini-pack; plastic (VSO40; SOT158).

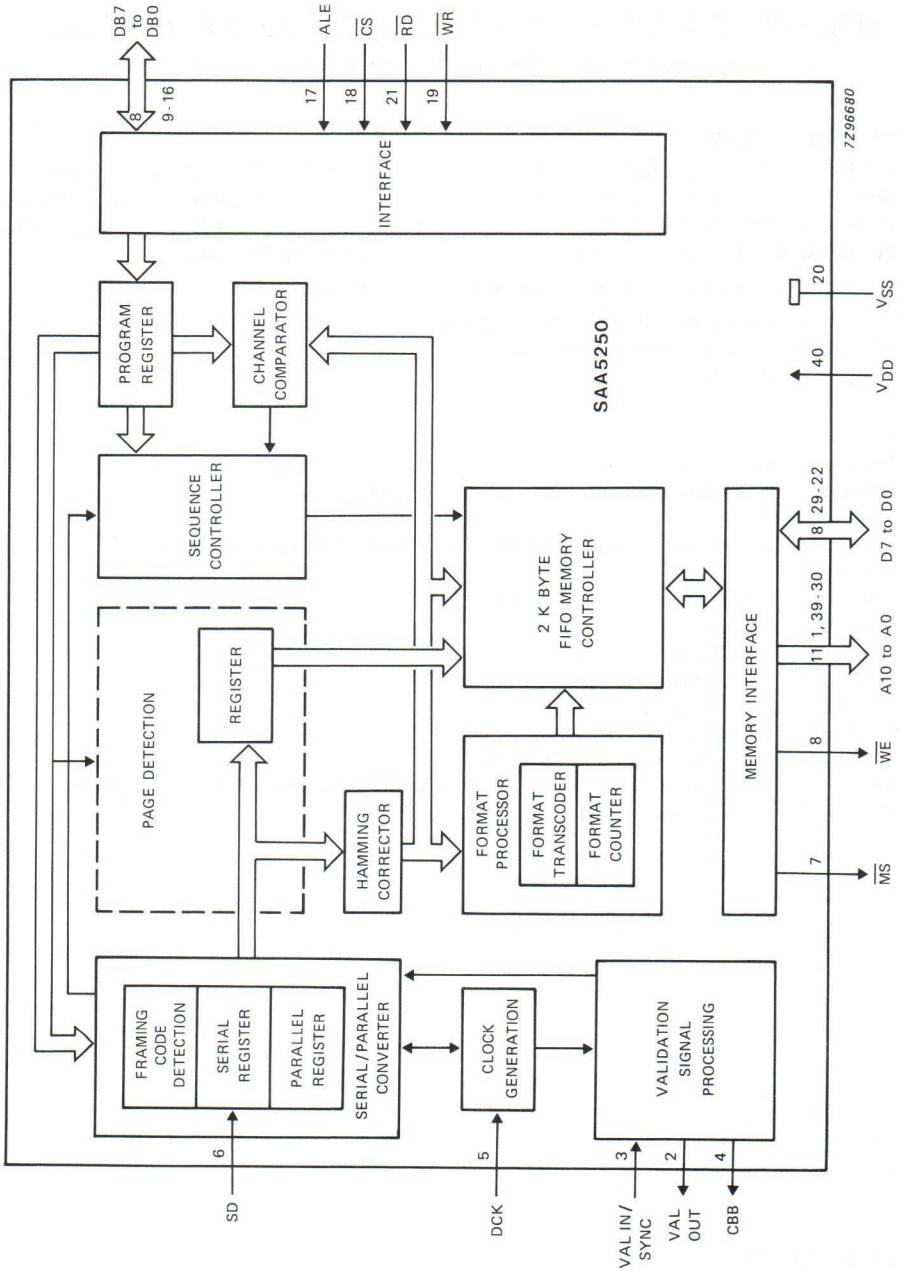


Fig. 1 Block diagram.

DEVELOPMENT DATA

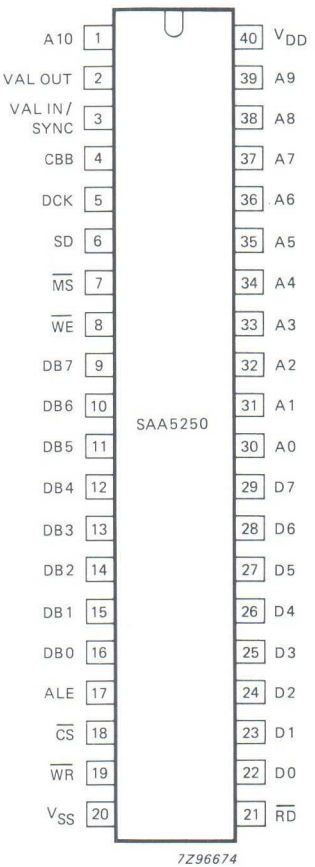


Fig. 2 Pinning diagram.

PINNING FUNCTION

mnemonic	pin no.	function
A10 and A0 to A9	1 and 30 to 39	Memory address outputs used by CIDAC to address a 2 K byte buffer memory
VAL OUT	2	Validation output signal used to control the location of the window for the framing code
VAL IN/SYNC	3	Validation input signal (line signal) used to give or calculate a window for the framing code detection
CBB	4	Colour burst blanking output signal used by the SAA5230 as a data slicer reset pulse
DCK	5	Data clock input, in synchronization with the serial data signal
SD	6	Serial data input, arriving from the demodulator
$\overline{MS}$	7	Chip enable output signal for buffer memory selection
$\overline{WE}$	8	Write command output for the buffer memory
DB7 to DB0	9 to 16	8-bit three state input/output data/address bus used to transfer commands, data and status between the CIDAC registers and the CPU
ALE	17	Demultiplexing input signal for the CPU data bus
$\overline{CE}$	18	Chip enable input for the SAA5250
$\overline{WR}$	19	Write command input (when LOW)
V_{SS}	20	ground
$\overline{RD}$	21	Read command input (when LOW)
D0 to D7	22 to 29	8-bit three state input/output data bus used to transfer data between CIDAC and the buffer memory
V_{DD}	40	+5 V power supply

FUNCTIONAL DESCRIPTION

Microcontroller interface

The microcontroller interface communicates with the CPU via the handshake signals DB7 – DB0, ALE, CS, $\overline{RD}$, $\overline{WR}$. The microcontroller interface produces control commands as well as programming the registers to write their contents or read incoming status/data information from the buffer memory. The details of the codes used to address the registers are given in Table 2.

The CIDAC is 'MOTEL' compatible (MOTEL compatible means it is compatible with standard **Mo**torola or In**tel** microcontrollers). It automatically recognizes the microcontroller type (such as the 6801 or 8501) by using the ALE signal to latch the state of the $\overline{RD}$ input. No external logic is required.

Table 1 Recognition signals

CIDAC	8049/8051 timing 1	6801/6805 timing 2
ALE $\overline{RD}$ $\overline{WR}$	ALE $\overline{RD}$ $\overline{WR}$	AS DS, E, $\Phi 2$ R/$\overline{W}$

Table 2 CIDAC register addressing

codes						
R	W	CS	DB2	DB1	DB0	function
1	0	0	0	0	0	write register R0
1	0	0	0	0	1	write register R1
1	0	0	0	1	0	write register R2
1	0	0	0	1	1	write register R3
1	0	0	1	0	0	write register R4
1	0	0	1	0	1	write register R5
1	0	0	1	1	0	write command register R6 (initialization command)
1	0	0	1	1	1	write register R7
0	1	0	0	0	0	read status
0	1	0	0	0	1	read data register
0	1	0	0	1	0	test (not used)
0	1	0	0	1	1	test (not used)

DEVELOPMENT DATA

Register organization

R0 register

Table 3 R0 Register contents

R04 slow/fast mode	R03 parity	R02 to R00 used prefixes
0 = slow mode 1 = fast mode	0 = no parity control 1 = odd parity	000 = DIDON long 001 = DIDON medium 010 = DIDON short 011 = not used 100 = U.K. teletext 101 = NABTS 110, 111 = without prefix

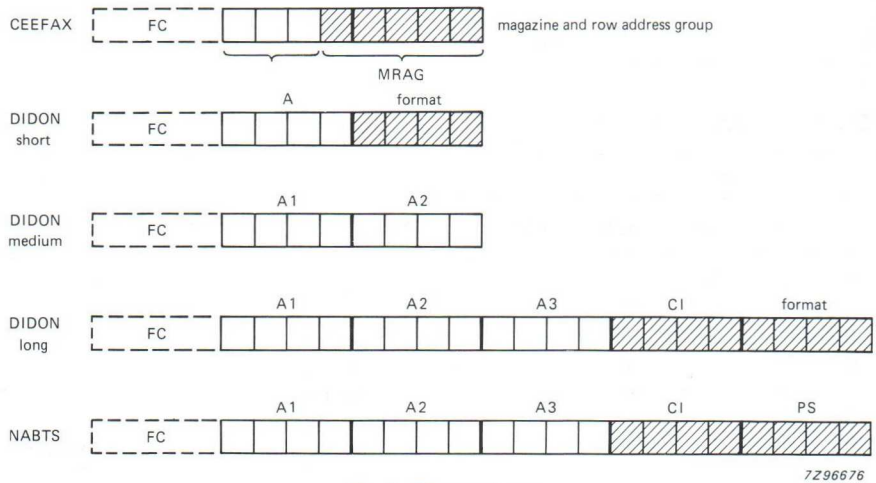


Fig. 3 Five prefixes.

All of the bytes (see Fig. 3) are Hamming protected. The hatched bytes are always stored in the memory in order to be processed by the CPU (see section 'Prefix processing'). In the mode without prefix all of the bytes which follow the framing code are stored in the memory until the end of the data packet, the format is then determined by the contents of the R3 register.

If R03 = 0; no parity control is carried out and the 8-bits of the incoming data bytes are stored in the fifo memory.

If R03 = 1; the 8th bit of the bytes following the prefix (data bytes) represents the result of the odd parity control.

If R04 = 0; the device operates in the slow mode. The CIDAC retrieves data from the user selected magazine (see section 'R1 and R2') and without searching for a start to a page stores the data into the FIFO memory.

If R04 = 1; the device operates in the fast mode. Prior to writing into the FIFO memory, the CIDAC searches for a start to a page which is variable due to the different prefixes:

- DIDON (long, medium and short): using the redundant bytes, SOH RS, X RS and SOH X (where X is a bit affected by a parity error)
- NABTS, the least significant bit of the PS byte is set to 1
- U.K. teletext, ROW = 0

R1 register

Table 4 R1 Register contents

R17 VAL IN/SYNC	R16 to R14 format table	R13 to R10 channel numbers (first digit)
1 = VAL 0 = SYNC	000 = list 1 001 = list 2 010 = list 3 011 = list 4 1XX = maximum/default value used (R3)	first digit hexadecimal value

Note

X = don't care

If VAL IN/SYNC = 1; the line signal immediately produces a validation signal for the framing code detection.

If VAL OUT = 0; the line signal is used as a starting signal for an internally processed validation signal (see Fig. 15). The framing code window width is fixed at 13 clock periods and the delay is determined by the contents of the R5 register (R56 to R50).

At any moment the user is able to ensure that the framing code window is correctly located. This is accomplished by the VAL OUT pin reflecting the internal validation signal. A CBB signal with programmable width (see section 'R7 register') can also be generated, this is used as a data slicer reset pulse by the SAA5230. The line signal is used as the starting point of the internal CBB signal width fixed by the contents of the R7 register.

If R16 = 0; then bits R15 and R14 provide the format table number using DIDON long and short prefixes (see Table 6).

If R16 = 1; then the format is determined by the contents of the R3 register.

The bits R13 to R10 represent the first channel number to be checked in the prefix. In U.K. teletext mode only 3 bits are required, so R13 = X.

Table 5 Format table

format byte B8, B6, B4 and B2	list 1	list 2	list 3	list 4
0000	0	0	0	0
0001	1	1	1	1
0010	2	2	2	2
0011	3	3	3	3
0100	4	5	6	7
0101	8	9	10	11
0110	12	13	14	15
0111	16	17	18	19
1000	20	21	22	23
1001	24	25	26	27
1010	28	29	30	31
1011	32	33	34	35
1100	36	37	38	39
1101	40	41	42	43
1110	44	45	46	47
1111	48	49	50	51

Note

B8 = MSB and B2 = LSB.

R2 register

Table 6 R2 Register contents

R27 to R24	R23 to R20
channel number, third digit	channel number, second digit
(hexadecimal value, third digit)	(hexadecimal value, second digit)

Note

R27 and R23 = MSB and R24 and R20 = LSB

The R2 register provides the other two parts of the channel number (depending on the prefix) that require checking.

R3 register

Table 7 R3 register contents

R35 to R30 6-bit format maximum/default value
000000 = 0 000001 = 1 – – – 111111 = 63

This 6-bit byte gives:

- In the DIDON long and short mode, a maximum format in case of corrupted transmission (multiple errors on the Hamming corrector)
- A possible 63-bit format for all types of prefix

R4 register

Table 8 R4 register contents

R47 to R40
8-bit register used for storing the framing code value which will be compared with the third byte of each data line

R5 register

Table 9 R5 register contents

R57 negative/positive	R56 to R50 synchronization delay
0 = negative edge for sync signal 1 = positive edge for sync signal	7-bit sync delay, giving a maximum delay of $(2^7 - 1) \times 10^6$ μs/F (Hz)

Note

F = data clock acquisition frequency (DCK).

Using R57 it is possible to start the internal synchronization delay (t_{DVAL}) on the positive or negative edge.

R6 write command register

This is a fictitious register. Only the address code (see Table 2) is required to reset the CIDAC. See Table 11 for the status of the FIFO memory on receipt of this command.

R7 register

Table 10 R7 register contents

R75 to R70
6-bit register used to give a maximum colour burst blanking signal of: $(2^6 - 1) \times 10^6$ µs/F (Hz)

Note

F = data clock acquisition frequency.

Fifo status register (read R0 register)

Table 11 Fifo register contents

DB2 to DB0		
DB2 = 1 memory empty	DB1 = 1, data not present in the read data register	DB0 = 0 memory not full

Once the relevant prefix and the right working modes have been given by the corresponding registers, a write command to the R6 register enables the CIDAC to accept and process serial data.

Channel comparator

This is a four bit comparator which compares the three user hexadecimal defined values in R1 and R2 to the corresponding bytes of the prefix coming from the Hamming corrector. If the three bytes match, the internal process of the prefix continues. If they do not match the CIDAC returns to a wait state until the next broadcast data package is received.

FIFO memory controller

The FIFO memory contains all the necessary functions required for the control of the 11-bit address memory (2 K byte). The functions contained in the FIFO memory are as follows:

- write address register (11-bits)
- read address register (11-bits)
- memory pointer (11-bits)
- address multiplexer (11-bits)
- write data register (8-bits)
- read data register (8-bits)
- data multiplexer
- control logic

The FIFO memory provides the memory interface with the following:

- 11-bit address bus (A10 to A0)
- 8-bit data bus (D7 to D0)
- two control signals, memory select ($\overline{MS}$) and write enable ($\overline{WE}$)

Operation

The CIDAC uses the same clock signal for data acquisition and internal processing, this allows the CIDAC to have a write and a read cycle during each character period (see Fig. 13). The first half of the character period is a write cycle and the second half is a read cycle. Consequently, for an 8 MHz bit rate the maximum memory cycle time is 500 ns.

When the first data byte is written into the FIFO memory, thus transferred into the read register, the FIFO memory enters the status shown in Table 12.

Table 12 FIFO status

DB2 to DB0		
DB2 = 1 memory empty	DB1 = 0 data available	DB0 = 0 memory not full

When the FIFO memory is full two events occur:

- the write address register points to the next address after the last written address
- when new data is to be written, the memory select signal output ceases

Memory interface

The memory interface contains all the buffers for the memory signals mentioned in the section 'FIFO memory controller'.

Page detection

This part of the CIDAC contains a parallel register with logic which detects (only in fast mode) a start of a page or data group (see section 'R0 register').

Hamming correction (see Tables 13 and 14)

The Hamming correction provides (see section 'Prefix processing'):

- hexadecimal value of the Hamming code
- accept/reject code signal
- parity information

Table 13 Hamming correction (coding)

Hexadecimal notation	B8	B7	B6	B5	B4	B3	B2	B1
0	0	0	0	1	0	1	0	1
1	0	0	0	0	0	0	1	0
2	0	1	0	0	1	0	0	1
3	0	1	0	1	1	1	1	0
4	0	1	1	0	0	1	0	0
5	0	1	1	1	0	0	1	1
6	0	0	1	1	1	0	0	0
7	0	0	1	0	1	1	1	1
8	1	1	0	1	0	0	0	0
9	1	1	0	0	0	1	1	1
A	1	0	0	0	1	1	0	0
B	1	0	0	1	1	0	1	1
C	1	0	1	0	0	0	0	1
D	1	0	1	1	0	1	1	0
E	1	1	1	1	1	1	0	1
F	1	1	1	0	1	0	1	0

Note

$B7 = B8 \oplus B6 \oplus B4$
$B5 = B6 \oplus B4 \oplus \overline{B2}$
$B3 = B4 \oplus \overline{B2} \oplus B8$
$B1 = \overline{B2} \oplus B8 \oplus B6$

$\oplus$ = exclusive OR gate function
B8, B6, B4 and B2 = data bits
B7, B5, B3 and B1 = redundancy bits

Table 14 Hamming correction (decoding)

A	B	C	D	interpretation	information
1	1	1	1	no error	accepted
0	0	1	0	error on B8	corrected
1	1	1	0	error on B7	accepted
0	1	0	0	error on B6	corrected
1	1	0	0	error on B5	accepted
1	0	0	0	error on B4	corrected
1	0	1	0	error on B3	accepted
0	0	0	0	error on B2	corrected
0	1	1	0	error on B1	accepted
A.B.C = 0			1	multiple errors	rejected

Note

$A = B8 \oplus B6 \oplus B2 \oplus B1$
$B = B8 \oplus B4 \oplus B3 \oplus B2$
$C = B6 \oplus B5 \oplus B4 \oplus B2$
$D = B8 \oplus B7 \oplus B6 \oplus B5 \oplus B4 \oplus B3 \oplus B2 \oplus B1$

$\oplus$ = exclusive OR gate function

Format processing

The format processing consists of two parts:

part 1

A format transcoder produces a 6-bit code (up to 63) and uses the following as inputs:

- DIDON long and short prefixes;
  hamming corrected code (4-bits)
  accept/reject code condition
  table number (see section 'R1 register', bits R15 and R14)
- Other prefixes (R16 = 1)
- 6-bit maximum/default format (see section 'R3 register')

part 2

A format counter operating at the character clock frequency which receives the 6-bit code from the format transcoder and is used to check the data packet length following the prefix.

Serial/parallel converter

The serial/parallel converter consists of three parts:

- An 8-bit shift register which receives the SD input and operates at the bit frequency (DCK).
- An 8-bit parallel register used for storage.
- A framing code detection circuit. This logic circuit compares the 8-bits of the R4 register with that of the serial register. If seven bits out of eight match (in coincidence with a validation window), it produces a start signal for a new teletext data line to the sequence controller.

Clock generation

The clock generator does the following:

- acts as a buffer for the DCK clock
- generates the character clock

As soon as a framing code has been detected, a divide by 8 counter is initialized and the character clock is started. The clock drives the following:

- sequence controller
- parallel registers
- format counter

Processing of VAL and CBB signals

The circuit has one input (VAL IN/SYNC) and two outputs (VAL OUT and CBB). The circuit consists of:

- 7-bit counter operating at DCK frequency which produces the framing code validation pulse delay
- 7-bit comparator which compares the contents of the R5 register (bits R56 to R50) to the bit counter
- a 6-bit counter operating at DCK frequency which produces the CBB pulse width
- 6-bit comparator which compares the contents of the R7 register (bits R75 to R70) to the bit counter
- control logic required to provide the start condition for the VAL signal and the CBB pulse width (on the negative or positive edge of the sync signal)

The CBB signal usefulness occurs when the associated video processor:

- has no sandcastle pulse to send back to the demodulator
- carries out the synchronization of the time base clock. In this event the CBB acts as a data slicer reset pulse

The VAL OUT is a control signal which reflects the internal framing code window.

Prefix processing (see Table 21)

Figs 4 to 9 show the acquisition flow charts for each prefix type coded in the R0 register (bits R02 to R00).

As soon as an initialization command is received by the CIDAC, a write command to the R6 register (only the address is significant), is ready to receive data from a dedicated channel number and store the data in the FIFO memory (explained in the following paragraphs, each paragraph being dedicated to an individual type of prefix).

DIDON long (see Fig. 4)

In this mode, the continuity index, format and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

Table 15 Continuity index processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	X	CI3	CI2	CI1	CI0

Table 16 Format processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	F5	F4	F3	F2	F1	F0

Note

A/R = 0, if rejected
A/R = 1, if accepted
X = don't care

DIDON mediun (see Fig. 5)

Only data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

DIDON short (see Fig. 6)

In this mode, format and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

Table 17 Format processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	F5	F4	F3	F2	F1	F0

NABTS (see Fig. 7)

In this mode, the continuity index, packet structure and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

Table 18 Continuity index processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	X	CI3	CI2	CI1	CI0

Table 19 Packet structure processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	X	PS3	PS2	PS1	PS0

U.K. teletext (see Fig. 8)

In this mode, the magazine and row address group (two bytes) and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a flag detection.)

Table 20 Magazine and row address group processing results

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	RW4	RW3	RW2	RW1	RW0

Without prefix

All the data following the framing code are stored in the FIFO memory.

Table 21 Prefix processing

prefixes	construction of prefixes	bytes stored in FIFO memory during slow mode	bytes stored in FIFO memory during fast mode
DIDON long	A1, A2, A3, CI, F and D	CI, F and D	CI*, F* and D*
DIDON medium	A1, A2 and D	D	D*
DIDON short	A1, F and D	F and D	F* and D*
NABTS	A1, A2, A3 CI, PS and D	CI, PS and D	CI*, PS* and D*
U.K. teletext	MRAG and D	MRAG and D	MRAG* and D*
without prefix		all bytes of the data packet following the framing code are written into the FIFO memory	

Note

* = after page/flag detection
A1, A2, A3 are channel numbers
CI = continuity index
F = format
PS = packet structure
D = data
MRAG = magazine and row address group

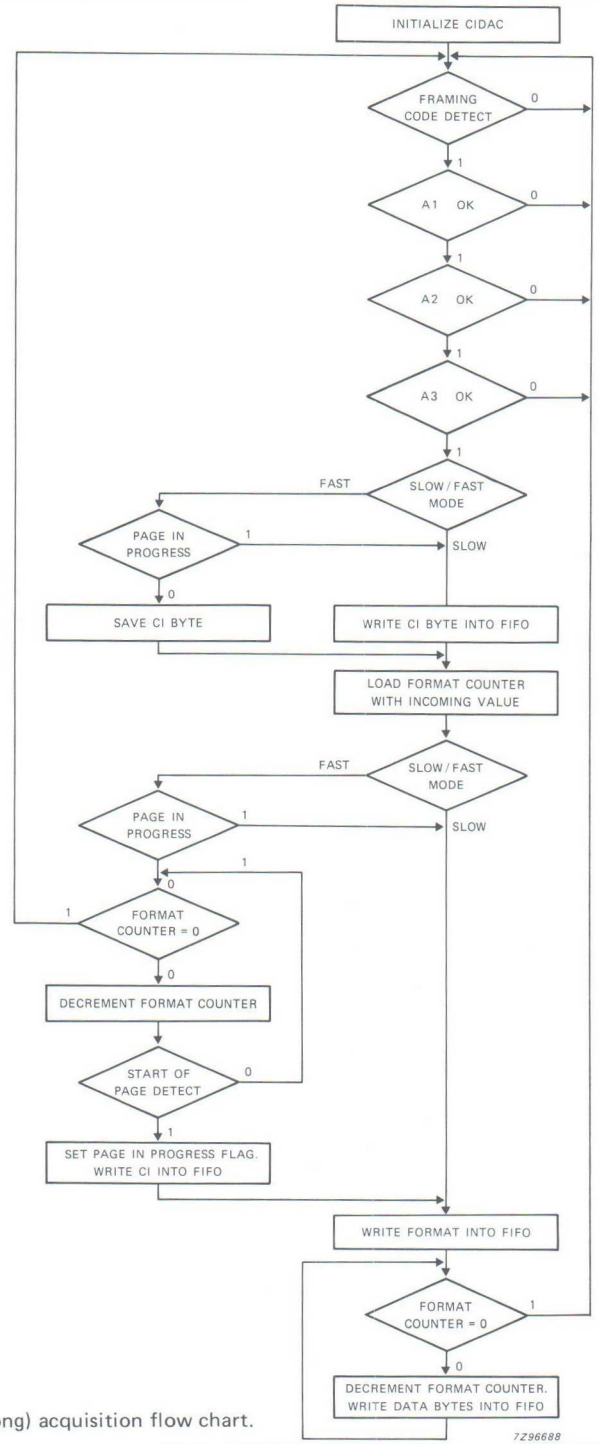


Fig. 4 DIDON (long) acquisition flow chart.

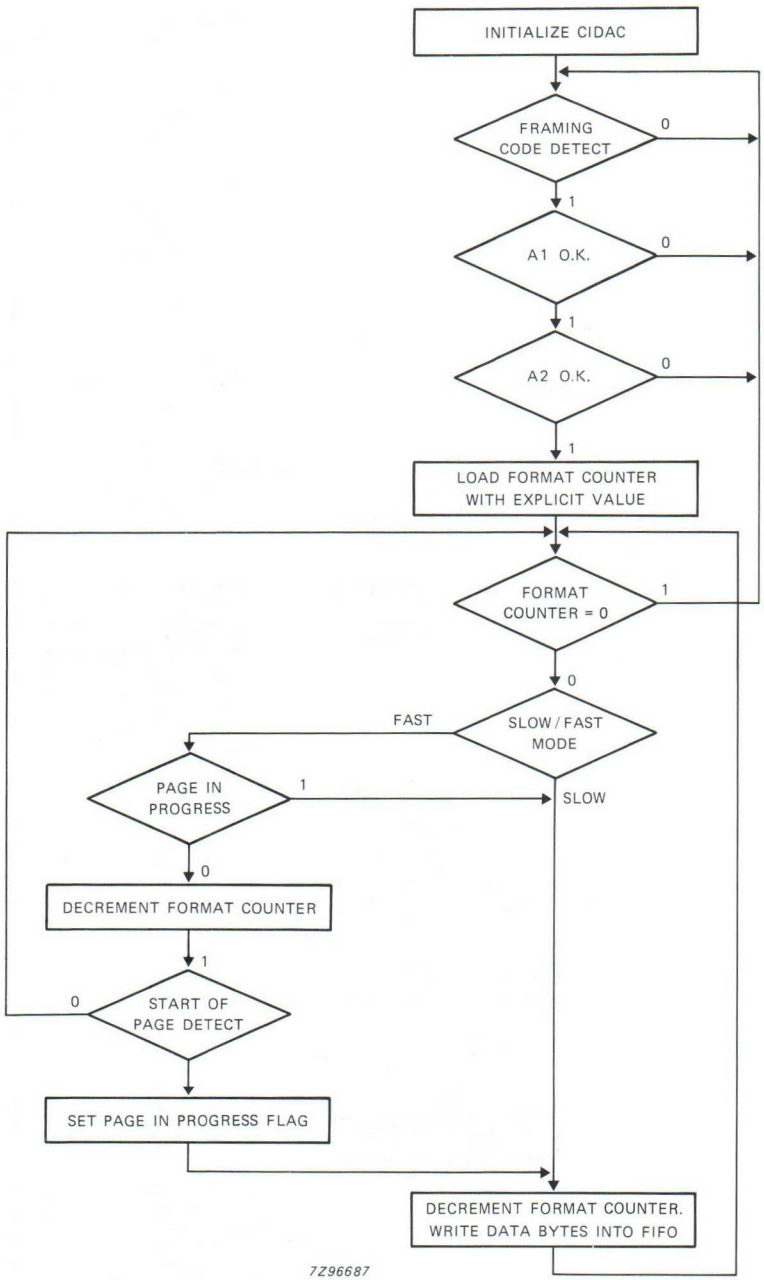


Fig. 5 DIDON (medium) acquisition flow chart.

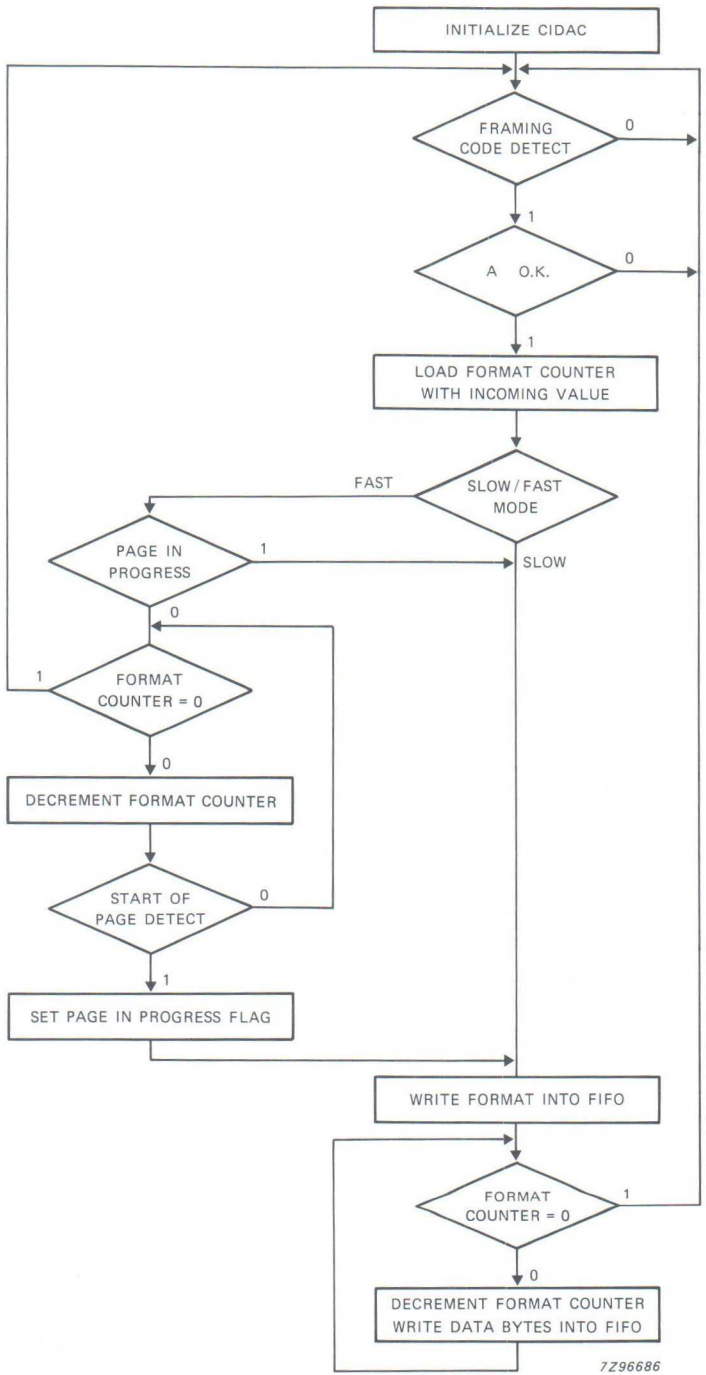


Fig. 6 DIDON (short) acquisition flow chart.

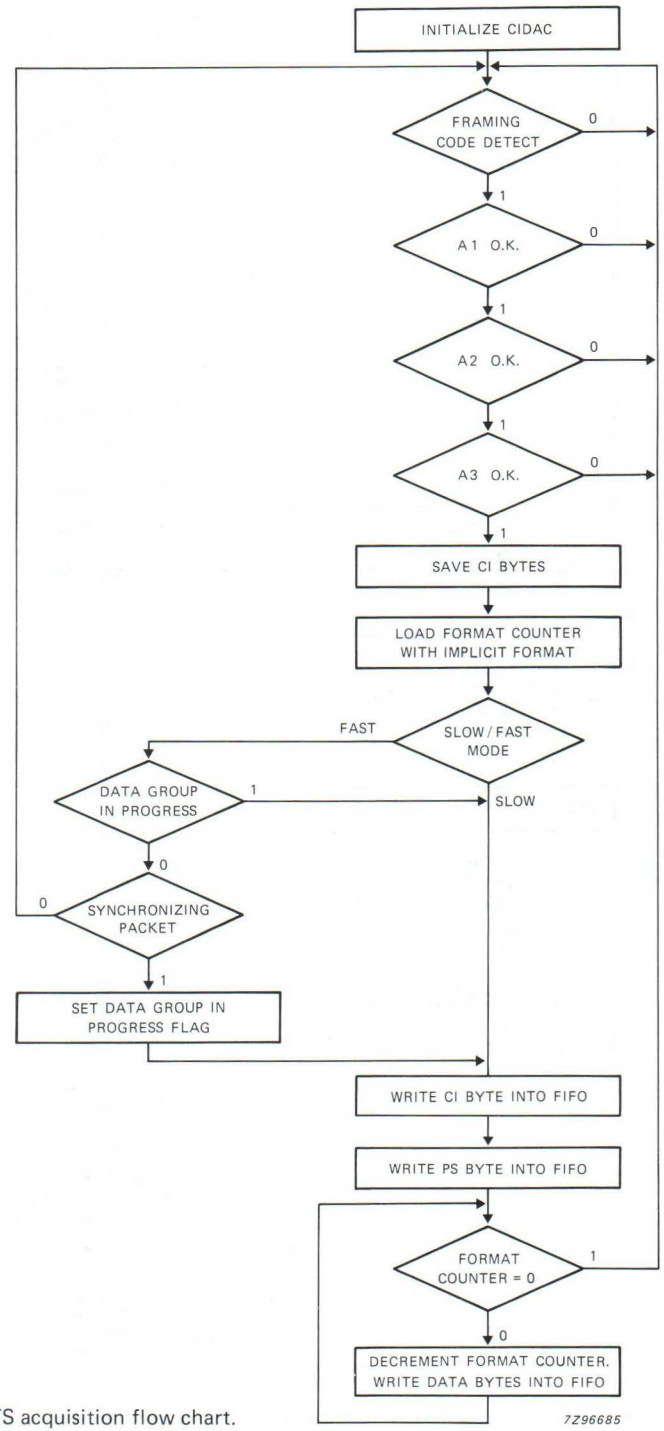


Fig. 7 NABTS acquisition flow chart.

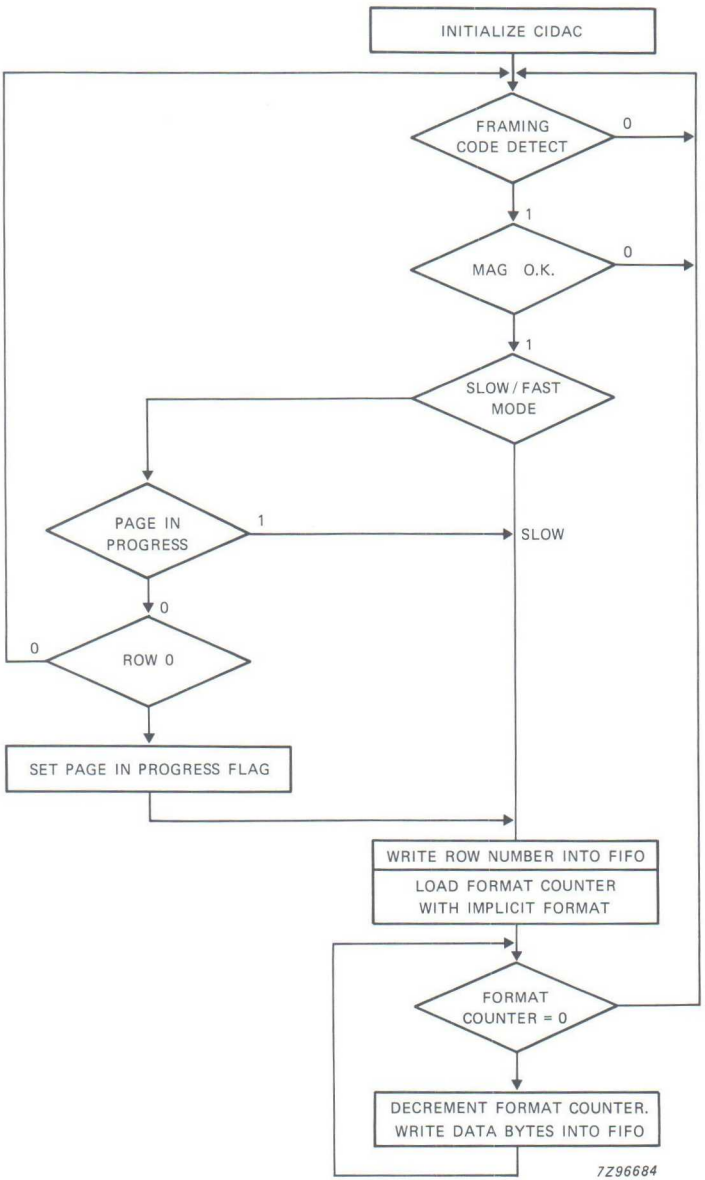


Fig. 8 U.K. teletext acquisition flow chart.

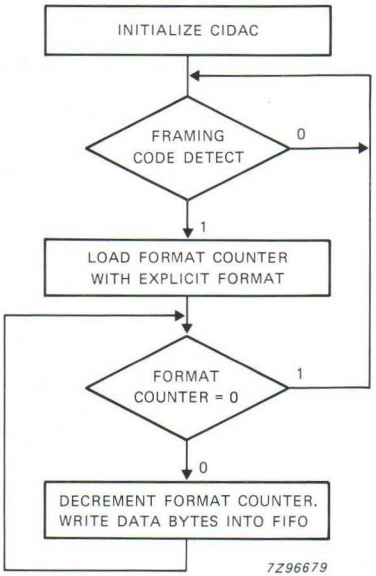


Fig. 9 Without prefix acquisition chart.

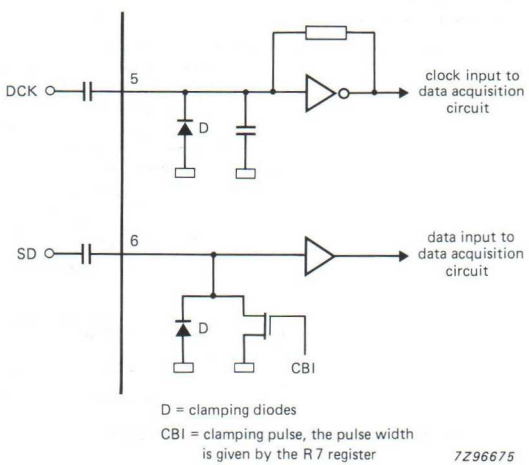


Fig. 10 SD and DCK input circuitry.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0,3	6,5	V
Input voltage range		V_I	−0,3	V_{DD}+0,3	V
Total power dissipation		P_{tot}	−	400	mW
Operating ambient temperature range		T_{amb}	0	70	°C
Storage temperature range		T_{stg}	−20	+125	°C

D.C. CHARACTERISTICS (except SD and DCK)

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = 0 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{DD}	4,5	5,0	5,5	V
Input voltage HIGH		V_{IH}	2	−	V_{DD}	V
Input voltage LOW		V_{IL}	−	−	0,8	V
Input leakage current		I_I	−	−	1,0	μA
Output voltage HIGH	I_{load} = 1 mA	V_{OH}	V_{DD}−0,4	−	−	V
Output voltage LOW	I_{load} = 4 mA, at pins 9 to 16 and 22 to 29	V_{OL}	−	−	0,4	V
	I_{load} = 1 mA all other outputs	V_{OL}	−	−	0,4	V
Power dissipation		P	−	5	−	mW
Input capacitance		C_I	−	−	7,5	pF

DEVELOPMENT DATA

SD and DCK D.C. CHARACTERISTICS (see Fig. 10)

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 0 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
DCK						
Input voltage range (peak-to-peak value)		$V_{I(p-p)}$	2,0	–	–	V
Input current	V_I = 0 to V_{DD}	I_I	5	–	200	μA
Input capacitance		C_I	–	–	30	pF
External coupling capacitor		C_{ext}	10	–	–	nF
SD						
D.C. input voltage range HIGH	note 1	V_{IH}	2,0	–	–	V
D.C. input voltage range LOW	note 2	V_{IL}	–	–	0,8	V
A.C. input voltage (peak-to-peak value)		$V_{I(p-p)}$	2,0	–	–	V
Input leakage current	V_I = 0 to V_{DD}	I_I	–	–	10	μA
Input capacitance		C_I	–	–	30	pF
External coupling capacitor		C_{ext}	10	–	–	nF

A.C. CHARACTERISTICS

V_{DD} = 5 V ±10%; Reference levels for all inputs and outputs, V_{IH} = 2 V; V_{IL} = 0,8 V; V_{OH} = 2,4 V; V_{OL} = 0,4 V; C_L = 50 pF on DB7 to DB0; T_{amb} = 0 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Microcontroller interface	Figs 11 and 12					
Cycle time		t_{CY}	400	–	–	ns
Address pulse width		t_{LHLL}	50	–	–	ns
$\overline{RD}$ HIGH or $\overline{WR}$ to ALE HIGH	Fig. 11	t_{AHRD}	0	–	–	ns
DS LOW to AS HIGH	Fig. 12	t_{AHRD}	0	–	–	ns
ALE LOW to $\overline{RD}$ LOW or $\overline{WR}$ LOW	Fig. 11	t_{ALRD}	30	–	–	ns
AS LOW to DS HIGH	Fig. 12	t_{ALRD}	30	–	–	ns
Write pulse width		t_{WL}	120	–	–	ns
Address and chip select set-up time		t_{ASL}	10	–	–	ns
Address and chip select hold time		t_{AHL}	20	–	–	ns
Read to data out period		t_{RD}	–	–	130	ns
Data hold after $\overline{RD}$		t_{DR}	10	–	100	ns
R/$\overline{W}$ to DS set-up time	Fig. 12	t_{RWS}	40	–	–	ns
R/$\overline{W}$ to DS hold time	Fig. 12	t_{RWH}	10	–	–	ns
Data set-up time	write cycle	t_{DW}	50	–	–	ns
Data hold time	write cycle	t_{WD}	10	–	–	ns
Read pulse width	note 3	t_{RL}	150 or DCK + 50	–	–	ns

DEVELOPMENT DATA

A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Memory interface	Fig. 13					
$\overline{WE}$ LOW to DCK falling edge		t_{WEL}	10	–	80	ns
$\overline{WE}$ HIGH to DCK falling edge		t_{WEH}	10	–	80	ns
$\overline{MS}$ LOW to DCK rising edge		t_{MSL}	10	–	80	ns
$\overline{MS}$ HIGH to DCK rising edge		t_{MSH}	10	–	85	ns
Address output from DCK rising edge		t_{AV}	10	–	120	ns
Data output from $\overline{WE}$ falling edge		t_{DWL}	0	–	10	ns
Data hold from $\overline{WE}$ rising edge		t_{DWH}	0	–	–	ns
Address set-up time to data	note 4	t_{AD}	–	–	3 x DCK – 110	ns
$\overline{WE}$ pulse width	note 5	t_{WEW}	3 x DCK	–	–	ns
$\overline{MS}$ pulse width	note 6	t_{MSW}	2 x DCK	–	–	ns
Demodulator interface (see SD and DCK D.C. CHARACTERISTICS)	Fig. 14					
DCK LOW	conversion rate $<$ 7,5 MHz	t_{DCKL}	55	–	–	ns
DCK HIGH	conversion rate $<$ 7,5 MHz	t_{DCKH}	55	–	–	ns
Serial data set-up time		t_{SSD}	0	–	–	ns
Serial data hold time		t_{HSD}	30	–	–	ns
Validation signal set-up time		t_{SVALI}	50	–	–	ns
Validation signal hold time		t_{HVALI}	50	–	–	ns
Other I/O signals	Fig. 15					
User definable width as a multiple of DCK period		t_{WCBB}	0	–	63	DCK
Validation signal width	note 7	t_{WVAL}	X	12	X	DCK
User definable delay as a multiple of DCK period		t_{DVAL}	0	–	127	DCK

Notes to the characteristics

1. Unless R7 = 00 the value given is unacceptable.
2. When CBI signal is maintained at 0 V (R7 = 00) and if SD input signal is correctly referenced to ground, no coupling capacitor is required.
3. DCK + 50 is the DCK period plus 50 ns.
4. 3 x DCK − 110 is 3 x DCK period − 110 ns.
5. 3 x DCK is 3 x DCK period.
6. 2 x DCK is 2 x DCK period.
7. X = irrelevant.

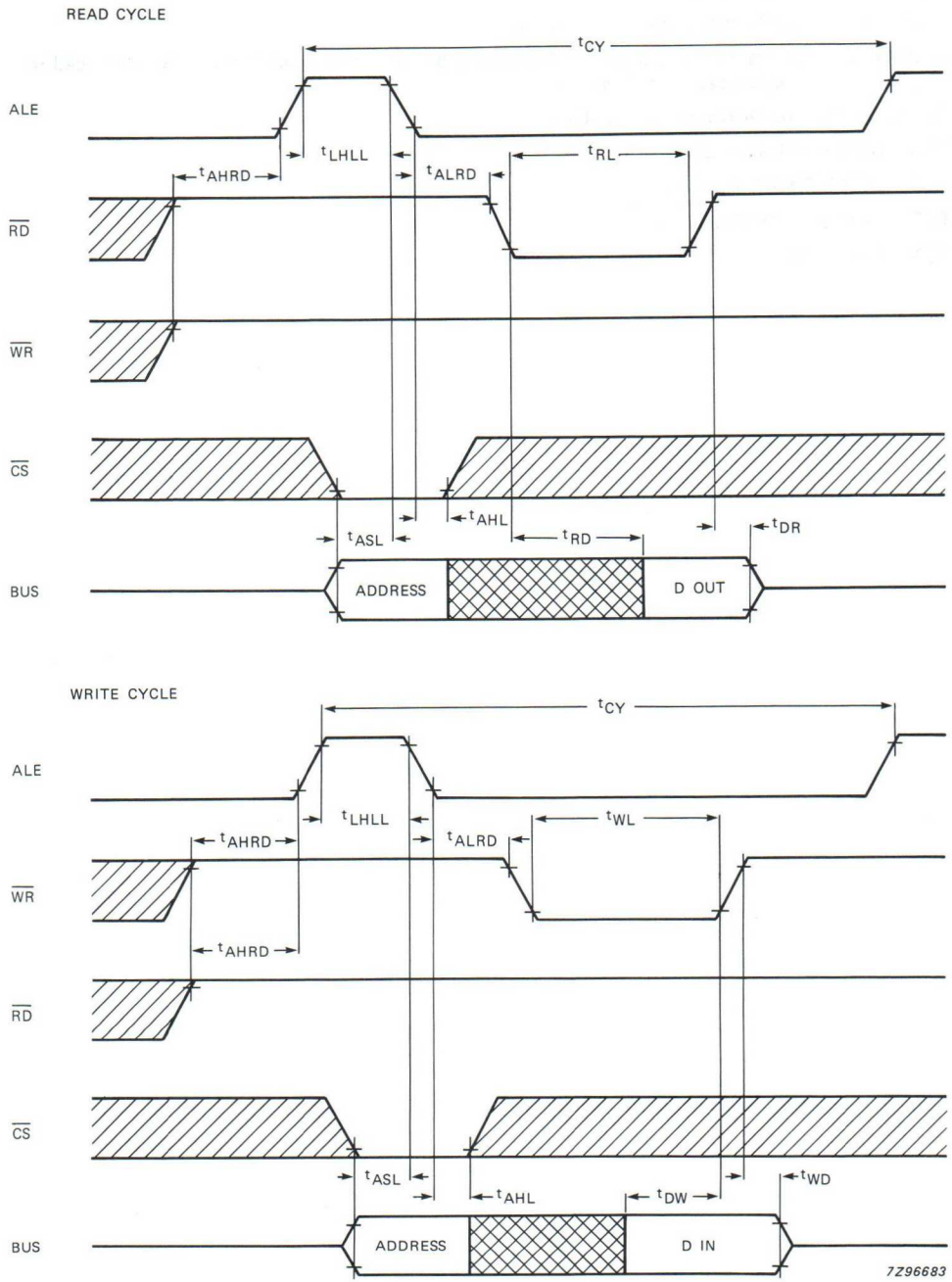


Fig. 11 Timing diagram for microcontroller interface (Intel).

DEVELOPMENT DATA

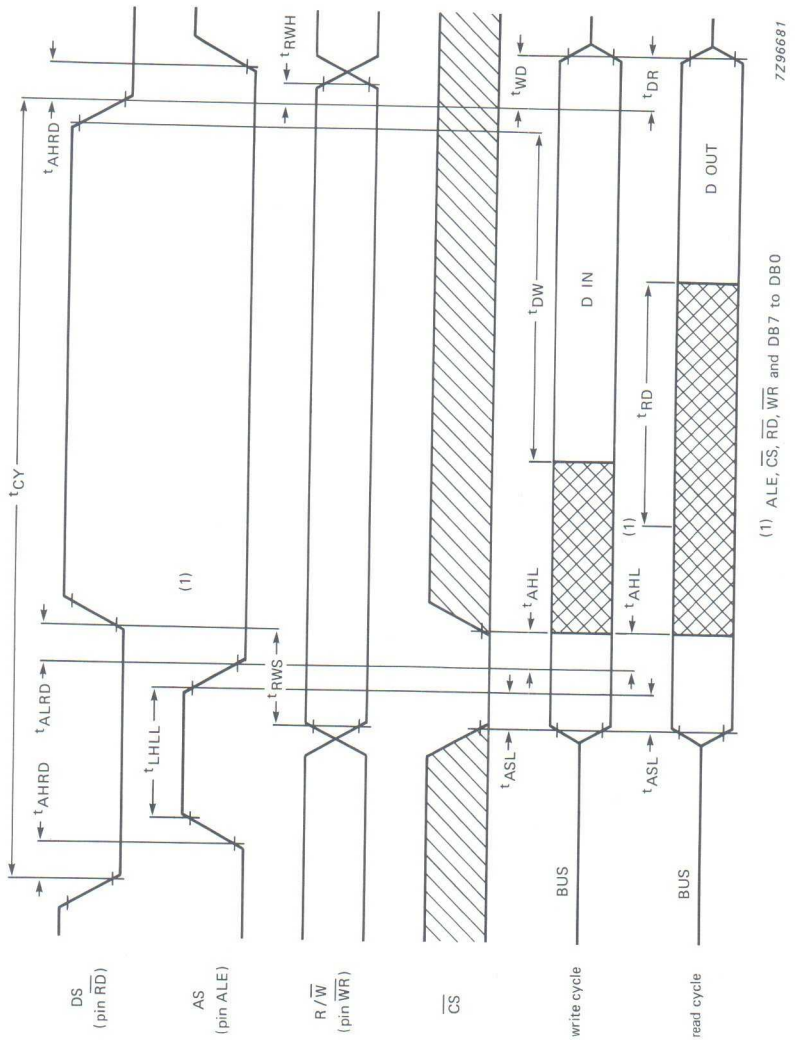


Fig. 12 Timing diagram for microcontroller interface (Motorola).

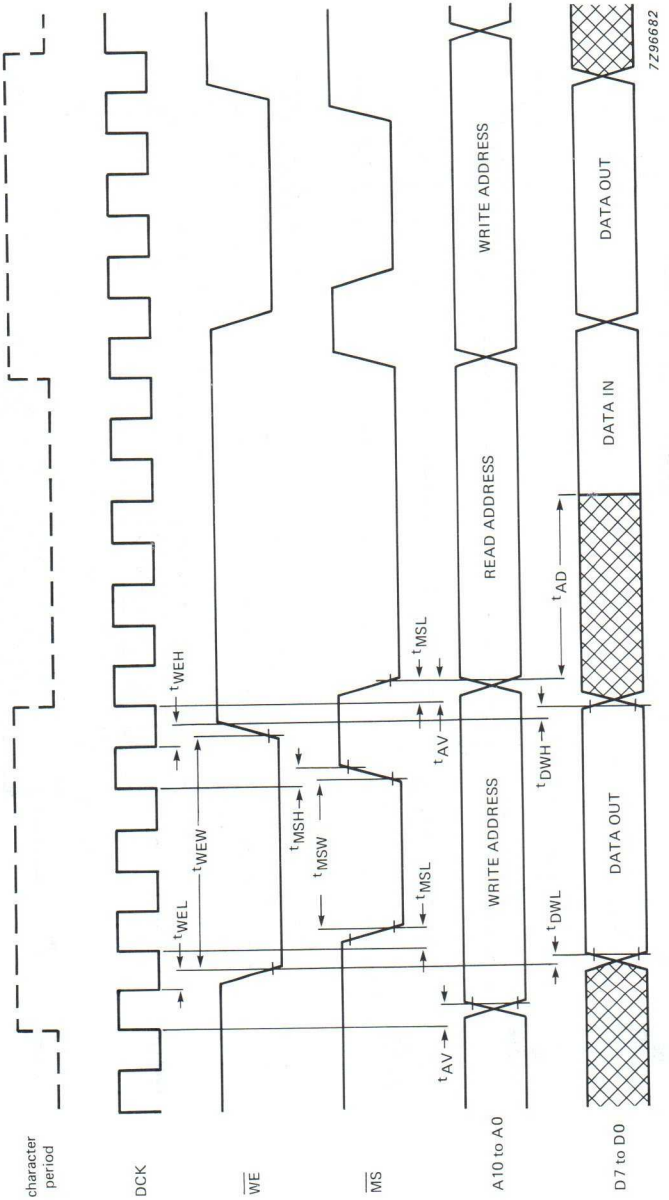


Fig. 13 Timing diagram for memory interface.

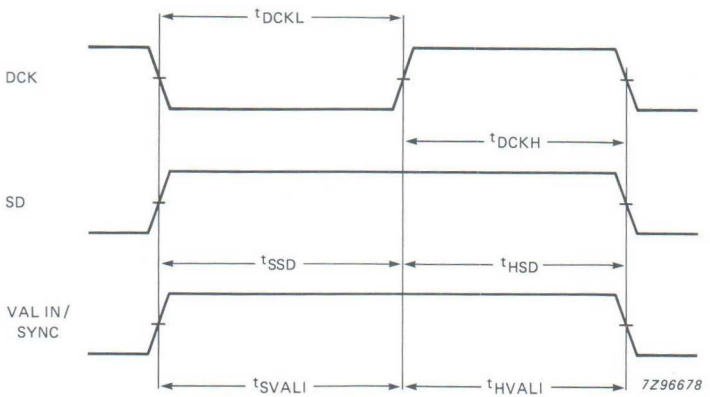


Fig. 14 Timing diagram for demodulator interface.

DEVELOPMENT DATA

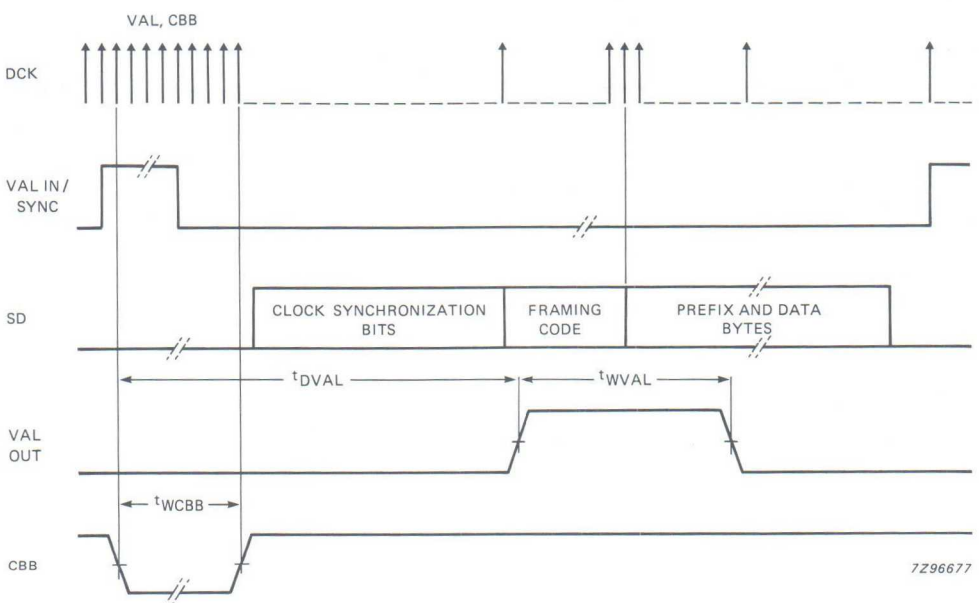


Fig. 15 Timing diagram for all other I/O signals.

Line twenty-one acquisition and display (LITOD)

SAA5252

FEATURES

- Complete 'stand-alone' Line 21 decoder in one package
- On-chip display RAM allowing full page Text mode
- Enhanced character display modes
- Full colour captions
- RGB interface for standard colour decoder ICs
- Automatic handling of Field 2 data
- Automatic selection of (1H, 1V), (2H, 1V) or (2H, 2V) scan modes
- Onboard OSD facility using Character generator
- RGB inputs to support existing OSD ICs
- I²C-bus or 'stand-alone' pin control
- Automatic data-ready signal generation on data acquisition
- Can decode signals recorded on standard VHS and S-VHS tape.

GENERAL DESCRIPTION

The SAA5252 (LITOD) is a single-chip CMOS device, which will acquire, decode and display Line 21 Closed Captioning data from a 525-line composite video signal. Operation as an On-Screen Display (OSD) device is also possible. Normal and line progressive scan modes are supported.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	30	–	mA
V_{syn}	CVBS sync amplitude	0.1	0.3	0.6	V
V_{vid}	CVBS video amplitude	0.7	1.0	1.4	V
T_{amb}	operating ambient temperature	–20	–	+70	°C
T_{stg}	storage temperature	–55	–	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5252P	24	DIL	plastic	SOT101
SAA5252T	24	SO24L	plastic	SOT137-1

BLOCK DIAGRAM

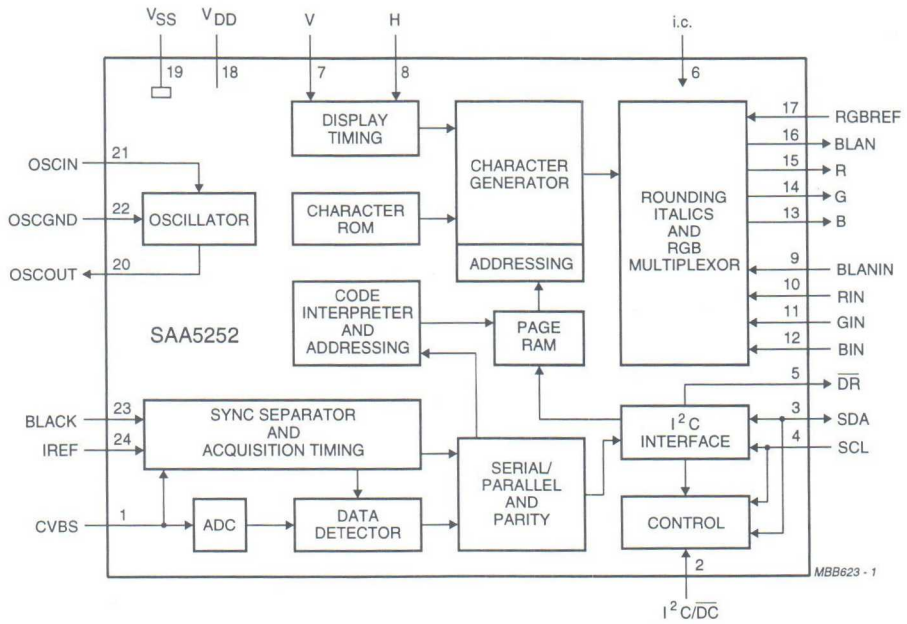


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CVBS	1	composite video input; signal should be connected via a 100 nF capacitor
$I^2C/\overline{DC}$	2	input selects I^2C or Direct Control
SDA	3	serial data port for I^2C-bus or mode select input for direct control
SCL	4	serial clock input for I^2C-bus or mode select input for direct control
$\overline{DR}$	5	data-ready signal to microcontroller (active-LOW) or mode select input for direct control
i.c.	6	internally connected; connect to V_{SS} for normal operation
V	7	vertical reference input for display timing
H	8	horizontal reference input for display timing
BLANIN	9	video blanking input from external OSD device
RIN	10	RED video input from external OSD device
GIN	11	GREEN video input from external OSD device
BIN	12	BLUE video input from external OSD device
B	13	BLUE video output
G	14	GREEN video output
R	15	RED video output
BLAN	16	video blanking output
RGBREF	17	input voltage defining output HIGH level for RGB pins for closed captioning output
V_{DD}	18	+5 V supply
V_{SS}	19	0 V ground
OSCOUT	20	oscillator output
OSCIN	21	oscillator input
OSCGND	22	oscillator ground
BLACK	23	video black level storage input; connected to V_{SS} via 100 nF capacitor
IREF	24	reference current input; connected to V_{SS} via 27 kΩ resistor

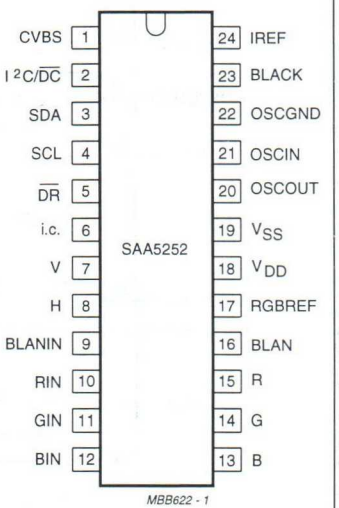


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)		−0.3	+6.5	V
V_{Imax}	maximum input voltage (any input)	note 1	−0.3	V_{DD} + 0.5	V
V_{Omax}	maximum output voltage (any output)	note 1	−	V_{DD} + 0.5	V
V_{dif}	difference between V_{SS} and OSCGND		−	±0.25	V
I_{IOK}	DC input or output diode current		−	±20	mA
I_{Omax}	maximum output current (each output)		−	±10	mA
T_{amb}	operating ambient temperature		−20	+70	°C
T_{stg}	storage temperature		−55	+125	°C
V_{es}	electrostatic handling				
	human body model	note 2	−2000	+2000	V
	machine model	note 3	−200	+200	V

Notes

1. This maximum value has an absolute maximum of 6.5 V independent of V_{DD}.
2. The human body model ESD simulation is equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor, which produces a single discharge transient. Reference *"Philips Semiconductors Test Method UZW-BO/FQ-A302 (similar to MIL-STD 883C method 3015.7)"*.
3. The machine model ESD simulation is equivalent to discharging a 200 pF capacitor via a resistor and series inductor with effective dynamic values of 25 Ω and 2.5 μH, which produces a damped oscillating discharge. Reference *"Philips Semiconductors Test Method UZW-BO/FQ-B302 (similar to EIAJ IC-121 Test Method 20 condition C)"*.

Quality

This device will meet the requirements of the *"Philips Semiconductors General Quality Specification UZW-BO/FQ-0601"* in accordance with *"Quality Reference Pocketbook (order number 9398 510 34011)"*. This details the acceptance criteria for all Q & R tests applied to the product.

CHARACTERISTICS

V_{DD} = 5 to 5.5 V; V_{SS} = 0 V; T_{amb} = –20 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DDtot}	total supply current		–	30	–	mA
Inputs						
CVBS (PIN 1)						
V_{syn}	sync voltage amplitude		0.1	0.3	0.6	V
$V_{vid(p-p)}$	video voltage amplitude (peak-to-peak value)		0.7	1.0	1.4	V
V_{dat}	caption data voltage amplitude		0.25	0.35	0.49	V
Z_{source}	source impedance		–	–	250	Ω
V_I	input switching voltage level of sync separator		1.7	2.0	2.3	V
Z_I	input impedance		2.5	5	–	kΩ
C_I	input capacitance		–	–	10	pF
IREF (PIN 24)						
R_{24}	resistor to ground		–	27	–	kΩ
V_{24}	voltage on pin 24		–	$\frac{1}{2}V_{DD}$	–	V
H (PIN 8)						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
I_{Imax}	maximum input current		–1	–	+1	mA
C_I	input capacitance		–	–	10	pF
t_r	pulse rise time		–	–	5	µs
t_f	pulse fall time		–	–	5	µs
t_W	pulse width					
	scan mode 1H		1	12	63	µs
	scan mode 2H		1	6	31	µs
V (PIN 7)						
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
I_{Imax}	maximum input current		–1	–	+1	mA
C_I	input capacitance		–	–	10	pF
t_r	pulse rise time		–	–	5	ns
t_f	pulse fall time		–	–	5	ns
t_W	pulse width		1	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGBREF (PIN, 17)						
V_I	input voltage		−0.3	–	V_{DD}	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
R, G AND B (PINS 15, 14 AND 13; NOTE 1)						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
Z_I	input impedance		2.5	5.0	–	kΩ
BLANIN (PIN 9)						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
t_r	input rise time	between 10% and 90%	–	–	80	ns
t_f	input fall time	between 90% and 10%	–	–	80	ns
$I^2C/\overline{DC}$ (PIN 2)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
SCL (PIN 4)						
V_{IL}	LOW level input voltage		−0.3	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD} + 0.5	V
f_{clk}	clock frequency		0	–	100	kHz
t_r	input rise time	between 10% and 90%	–	–	2	µs
t_f	input fall time	between 90% and 10%	–	–	2	µs
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
Inputs/outputs						
CERAMIC RESONATOR (PINS 20, 21 AND 22; SEE FIG.5)						
f_{osc}	oscillator frequency		11.82	12	12.18	MHz
C0	parallel capacitance		–	5.35	–	pF
C1	series capacitance		–	37.4	–	pF
L1	series inductance		–	35.5	–	µH
R1	series resistance		–	6	25	Ω
BLACK (PIN 23)						
C_{black}	storage capacitor to ground		–	100	–	nF
V_{black}	black level voltage for nominal sync amplitude		1.8	2.15	2.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SDA (PIN 3; OPEN DRAIN)						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	between 10% and 90%	–	–	2	µs
t_f	input fall time	between 90% and 10%	–	–	2	µs
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	between 3 V and 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF
$\overline{DR}$ (PIN 5; OPEN DRAIN)						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
t_f	output fall time	between 4 V and 1 V with 3.3 kΩ to 5 V	–	–	50	ns
C_L	load capacitance		–	–	100	pF
Outputs						
R, G AND B (PINS 15, 14 AND 13; CAPTION MODE)						
V_{OL}	LOW level output voltage	I_{OL} = +2 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = −2 mA	V_{17} − 0.3	V_{17}	V_{17} + 0.4	V
Z_O	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
t_r	output rise time	between 10% and 90%	–	–	10	ns
t_f	output fall time	between 90% and 10%	–	–	10	ns
BLAN (PIN 16)						
V_{OL}	LOW level output voltage	I_{OL} = +2 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −2 mA	1.1	–	2.8	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	between 10% and 90%	–	–	10	ns
t_f	output fall time	between 90% and 10%	–	–	10	ns
t_{skew}	skew delay time between display and R, G, B, BLAN		–	–	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C timing (see Fig.3)						
t_{LOW}	clock LOW time		4	–	–	µs
t_{HIGH}	clock HIGH time		4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH-to-STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;STA}$	START hold time		4	–	–	µs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	µs
t_r	output rise time	between 10% and 90%	–	–	10	ns
t_f	output fall time	between 90% and 10%	–	–	10	ns

Note

1. These inputs are analog, V_{IL} and V_{IH} values are quoted as a guide for digital RGB users.

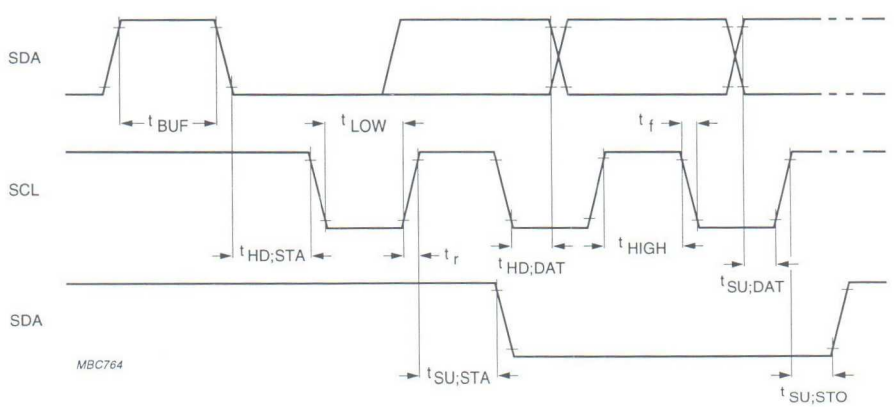
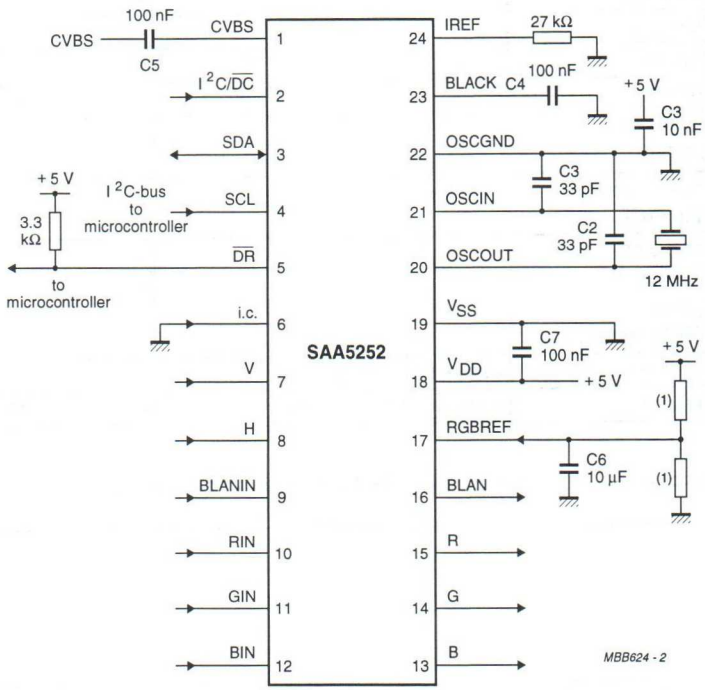


Fig.3 I²C-bus timing diagram.

APPLICATION INFORMATION



(1) Value dependent on application.

Fig.4 Application diagram.

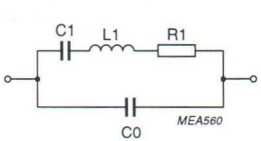


Fig.5 Ceramic resonator equivalent circuit.

DISPLAY GENERATOR

General Description

The displayed characters are defined on a 5-by-12 matrix within a 7-by-13 window, allowing one blank pixel either side of the character and a blank pixel row above. There are a number of display options available controlled by Register 1, or external pins in 'stand-alone' mode.

The three display modes are video, text and caption, the device is powered up in the video mode.

The display generator reads the Pre-amble Address Code (PAC) then the data associated with that row. Each character is then rounded after which it can be italicized and/or underlined, depending on the PAC or mid-row codes, before being passed on to the output circuitry. Figure 6 shows the character set.

Display of external On-Screen Display (OSD) facilities

The R, G, B and BLAN outputs of the display have the capability to be put in a 3-state mode allowing other OSD devices to take control of the television R, G, B and BLAN signals.

When the BLANIN is held HIGH then the R, G, B and BLAN outputs from display are disabled and the R, G, B and BLAN signals come directly from the RGBIN and BLANIN inputs. This will allow On-Screen Display to be placed on top of the captioning without any corruption, leaving the captions intact when the On-Screen Display is switched off (BLANIN goes LOW). In this form of operation the RGBIN and RGBOUT pins can be considered transparent; BLANIN goes through the normal output buffer to BLAN.

Table 1 Register map (WRITE).

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
00	DF$\overline{1}$/2	RGB, BLAN +$\overline{ve}$/–ve	H +ve/–$\overline{ve}$	V +ve/–$\overline{ve}$	H3	H2	H1	H0
01	CLEAR	CH 2/$\overline{1}$	$\overline{\text{NARROW}}$ /WIDE	ACQ OFF	EN1	EN0	M1	M0
02	–	–	–	–	ROW3	ROW2	ROW1	ROW0
03	–	–	–	COL4	COL3	COL2	COL1	COL0
04	–	OSD6	OSD5	OSD4	OSD3	OSD2	OSD1	OSD0

Table 2 Register map (READ).

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
00	POR	0	0	0	$\overline{F1}$/F2	EDS	PARITY SHUTDOWN	DATA READY
01	PARITY ERROR	DATA BIT 7	DATA BIT 6	DATA BIT 5	DATA BIT 4	DATA BIT 3	DATA BIT 2	DATA BIT 1
02	PARITY ERROR	DATA BIT 7	DATA BIT 6	DATA BIT 5	DATA BIT 4	DATA BIT 3	DATA BIT 2	DATA BIT 1



The '0' and 'zero' use the same character, 4Fh.

Fig.6 Character set.

I²C INTERFACE

Description of WRITE registers

The write subaddresses auto increment from 0 through to 4 at which point they stay until a new write subaddress is sent. Registers are set to all logic 0 at power-up.

Table 3 Register 0 WRITE (Control Byte 1).

BIT	DESCRIPTION
D0 to D3	H0 to H3 set the offset position from the start of the horizontal sync pulse, set to a nominal value on reset.
D4	Vertical sync pulse expected to be negative going logic 0 or positive-going logic 1.
D5	Horizontal sync pulse expected to be negative going logic 0 or positive-going logic 1.
D6	Video outputs will be positive going logic 0 or negative-going logic 1.
D7	Data field select. When set to logic 0 Field 1 is decoded, when set to logic 1 Field 2 is decoded.

Table 4 Register 1 WRITE (Control Byte 2).

BIT	DESCRIPTION
D0, D1	Display mode selection bits. Table 8 shows the possible display modes.
D2, D3	Enhanced caption mode selection bits. Table 9 shows the possible enhanced caption modes.
D4	When set to logic 1 acquisition of caption data is inhibited to allow the display to be used for On-Screen Display purposes.
D5	Acquisition window selection. When set to logic 0 only Line 21 is checked for caption data. When set to logic 1, lines 19 to 23 of both fields are checked, allowing encrypted video signals to be handled.
D6	User channel selection.
D7	Clears the page memory when set HIGH. The page memory will be within two fields (30 ms).

Table 5 Register 2 WRITE (On-Screen Display data row address).

BIT	DESCRIPTION
D0 to D3	Row 0 to 3 sets the row address for On-Screen Display. This stored value will be incremented by overflow increments of Register 3.

Table 6 Register 3 WRITE (On-Screen Display data column address).

BIT	DESCRIPTION
D0 to D4	Columns 0 to 4 sets the column address for On-Screen Display. This stored value will be incremented by writes to Register 4.

Table 7 Register 4 WRITE (On-Screen Display data).

BIT	DESCRIPTION
D0 to D6	OSD0 to OSD6, On-Screen Display data bits writing to this register causes Register 3 to increment its stored value.

Table 8 Display modes.

DISPLAY MODE OPTIONS	M1	M0
Video only	0	0
Text mode	0	1
Normal caption mode	1	0
Enhanced caption mode	1	1

Table 9 Enhanced caption modes.

ENHANCED CAPTION MODES	EN1	EN0
Enhanced caption modes	EN1	EN0
Shadowed character/Video background	0	0
Shadowed character/Mesh background	0	1
Normal character/Video background	1	0
Normal character/Mesh background	1	1

Description of READ registers

The read subaddresses auto increment from 0 through to 2 at which point they stay until a new read subaddress is sent.

All the bits in Table 10 are reset to logic 0 after the register is read.

Table 10 Register 0 READ (status).

BIT	DESCRIPTION
D0	Data ready (new data has been acquired).
D1	Parity error shut-down, goes HIGH when SAA5252 has a parity shut-down condition.
D2	Indicates the following bytes are extended data service bytes.
D3	Indicates Field 1 or Field 2 data bytes.
D7	Indicates Power-On Reset (POR) has occurred, all I^2C-bus write registers have been reset to logic 0.

Table 11 Register 1 READ (first data byte).

BIT	DESCRIPTION
D0 to D6	Data Bit 1 to Data Bit 7 (see note 1).
D7	Parity error flag bit. Bit goes HIGH when a parity error has occurred.

Note

1. In the Line 21, specification data bits are numbered D1 to D8.

Table 12 Register 2 READ (second data byte).

BIT	DESCRIPTION
D0 to D6	Data Bit 1 to Data Bit 7 (see note 1).
D7	Parity error flag bit. Bit goes HIGH when a parity error has occurred.

Note

1. In the Line 21, specification data bits are numbered D1 to D8.

Interface to microcontroller using I²C-bus

The interface to the microcontroller is via the two-wire serial I²C-bus, and optionally by a Data-Ready signal ($\overline{DR}$). On power up the microcontroller initializes the device by an I²C-bus WRITE to Registers 0 (Control Byte 1). The I²C-bus subaddress is then auto incremented to point to Register 1 (Control Byte 2). These two registers configure the device to the users requirements.

If the device is to be used for data acquisition only, then there are three methods by which the microcontroller can be informed of the arrival of valid Line 21 data:

- It can poll the $\overline{DR}$ pin, if the function has been enabled, and wait for it to go LOW.
- It can use the negative edge of the $\overline{DR}$ signal to cause an interrupt.
- It can poll the Data Ready bit (bit D0 of the status byte, I²C-bus READ Register 0).

When valid data is detected, the microcontroller must initiate an I²C-bus READ of Registers 0, 1 and 2. The first and second data bytes from the most recently received Line 21 are in Register 1 and Register 2 respectively.

The $\overline{DR}$ pin, and the Data Ready bit (Status bit D0) will be cleared after any register has been read. POR is reset after Register 0 has been read.

'STAND-ALONE' (NON I²C-BUS) OPERATION

To set the SAA5252 for 'stand-alone' operation pin 2 (I²C/$\overline{DC}$) is tied LOW. This will change the operation of the SCL, SDA and $\overline{DR}$ pins to mode select inputs which will select as shown in Table 13.

In the caption mode the SAA5252 operates in the basic Normal character/Black background mode. This complies with the FCC ruling. In the Enhanced caption mode the set-up will be Shadowed character/Video background. SDA and SCL in the 'stand-alone' operation act as bits M0 and M1 in Table 8.

Table 13 Stand-alone modes.

$\overline{DR}$	SCL	SDA	MODE OF OPERATION	CHANNEL RECEPTION
0	0	0	Video mode	Channel 1
0	0	1	Text mode	Channel 1
0	1	0	Normal captions	Channel 1
0	1	1	Enhanced captions	Channel 1
1	0	0	Video mode	Channel 2
1	0	1	Text mode	Channel 2
1	1	0	Normal captions	Channel 2
1	1	1	Enhanced captions	Channel 2

Integrated VIP and teletext decoder (IVT1.1X)

SAA5254

FEATURES

- Complete teletext decoder including page memory and FASTEXT links in a single 40-pin DIL package
- Automatic processing of extension packet 26 for widest possible language decoding. All our standard language options can be available, and language option is readable via I²C-bus
- 100% hardware compatible with the SAA5244A; plug-in replacement and extra market
- 100% hardware compatible with the SAA5244A, except if the special OSD symbols were used with the SAA5244A, except ROM identification number
- The device is pin-aligned with the other members of the new Philips teletext decoder family, i.e. SAA5280 and the SAA5249, making one hardware solution for the full range
- Low software overhead for the control microprocessor
- Single page acquisition system
- RGB interface to standard colour decoder ICs, push-pull output drive
- Separate text and video signal quality detectors.

DESCRIPTION

The Integrated VIP and Teletext decoder (IVT1.1X) is designed to decode 625-line based World System Teletext transmissions. This single-chip teletext decoder hardware is based on the SAA5244A with which it is completely compatible.

Like the SAA5244A the device contains all the hardware necessary to decode the teletext, but the SAA5254 also contains extra hardware to process the extension packet 26 characters automatically, extending the markets to which the TV chasis can be shipped and opening the possibility of many more language options.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5254P	40	DIL	plastic	SOT129
SAA5254GP	44	QFP	plastic	SOT205A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	90	120	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1.0	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature	−20	–	+70	°C

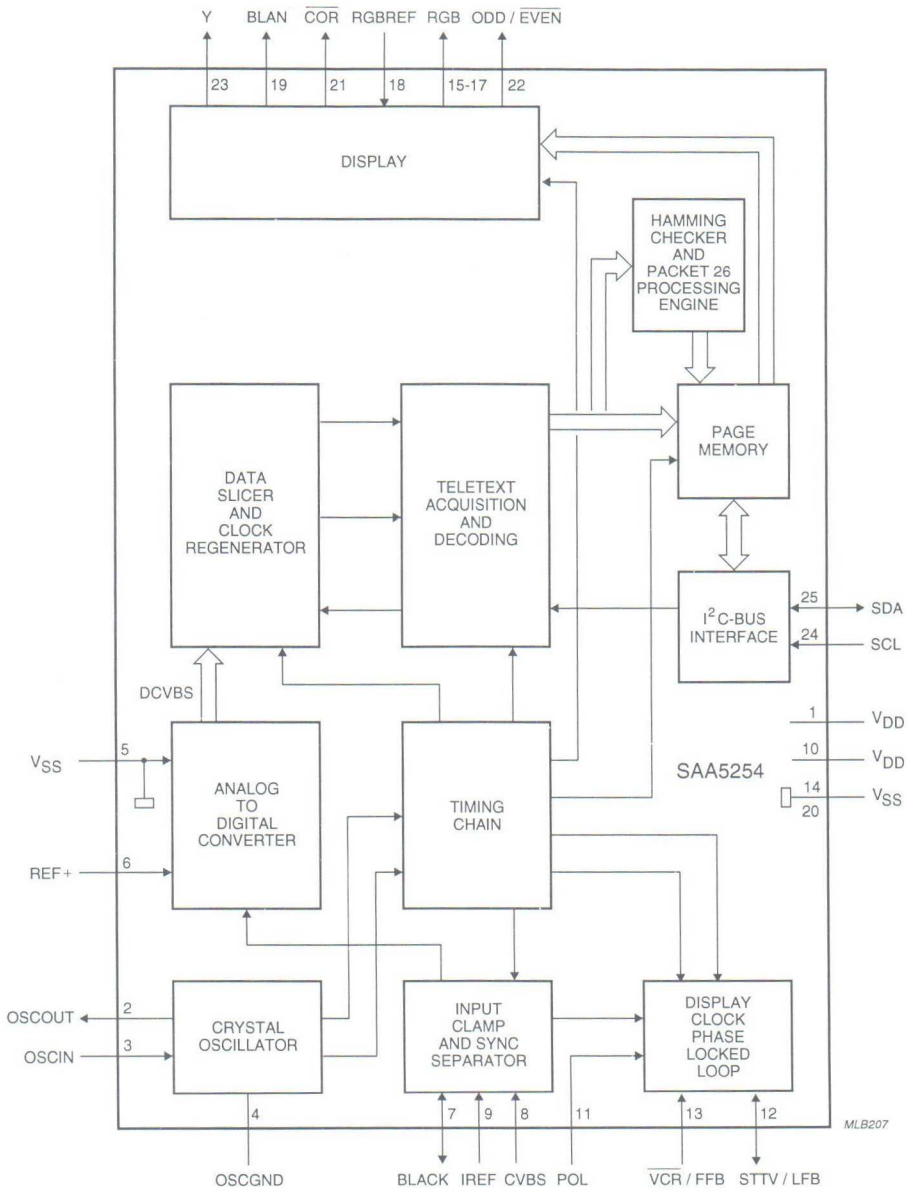


Fig.1 Block diagram for SOT129 (DIL40) package.

PINNING

SYMBOL	SOT129	SOT205A	DESCRIPTION
V_{DD}	1	18	+5 V supply.
OSCOUT	2	19	27 MHz crystal oscillator output.
OSCIN	3	20	27 MHz crystal oscillator input.
OSCGND	4	21	0 V crystal oscillator ground.
V_{SS}	5	22	0 V ground.
REF+	6	23	Positive reference voltage for the ADC. This pin should be connected to +5 V.
BLACK	7	24	Video black level storage pin, connected to ground via a 100 nF capacitor.
CVBS	8	25	Composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor.
IREF	9	26	Reference current input pin, connected to ground via a 27 kΩ resistor.
V_{DD}	10	27	+5 V supply.
POL	11	28	STTV/LFB/FFB polarity selection pin.
STTV/LFB	12	29	Sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode).
$\overline{VCR}$/FFB	13	32	PLL time constant switch/field flyback input pin. Function controlled by an internal register bit (scan sync mode).
V_{SS}	14	33	0 V ground.
R	15	34	Dot rate character output of the RED colour information.
G	16	35	Dot rate character output of the GREEN colour information.
B	17	36	Dot rate character output of the BLUE colour information.
RGBREF	18	37	DC input voltage to define the output high level on the RGB pins.
BLAN	19	38	Dot rate fast blanking output.
V_{SS}	20	39	0 V ground.
$\overline{COR}$	21	40	Programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages; open drain output.
ODD/$\overline{EVEN}$	22	41	25 Hz output synchronized with the CVBS input's field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents.
Y	23	42	Dot rate character output of teletext foreground colour information; open drain output.
SCL	24	43	Serial clock input for the I²C-bus. It can still be driven during power-down of the device.
SDA	25	44	Serial data port for the I²C-bus; open drain output. It can still be driven during power-down of the device.
n.c.	–	4 to 7 30, 31	Not connected.
i.c.	26 to 40	1 to 3 8 to 17	Internally connected. Must be left open-circuit in application .

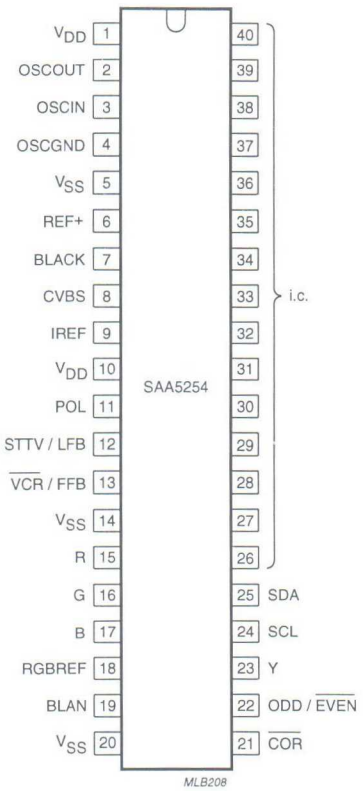


Fig.2 Pin configuration; SOT129 (DIL40).

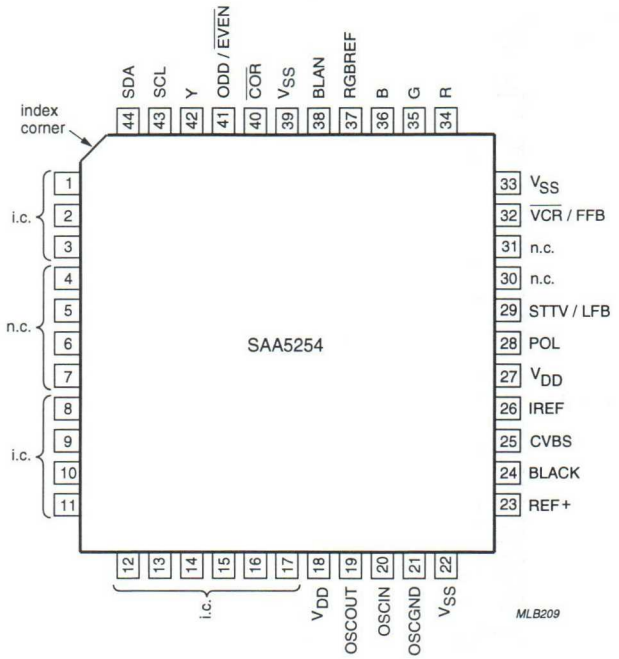


Fig.3 Pin configuration; SOT205A (QFPL44).

QUALITY AND RELIABILITY

This device will meet Philips Semiconductors (Business Group ICs) general quality Specification for Integrated Circuits SNW-FQ-611-Part E. The principal requirements are shown in Tables 1 to 4.

Group A

Table 1 Acceptance tests per lot.

TEST	CONDITIONS	REQUIREMENTS
Mechanical		cumulative target: < 100 PPM
Electrical		cumulative target: < 100 PPM

Group B

Table 2 Processability tests (by package family).

TEST	CONDITIONS	REQUIREMENTS
Solderability		< 7% LTPD
Mechanical		< 15% LTPD
Solder heat resistance		< 15% LTPD

Group C

Table 3 Reliability tests (by process family).

TEST	CONDITIONS	REQUIREMENTS
Operational life	168 hours at T_j = 150 °C	< 1500 FPM; equivalent to < 100 FITS at T_j = 70 °C
Humidity life	temperature, humidity, bias (1000 hours, 85 °C, 85% RH or equivalent test)	< 2000 FPM
Temperature cycling performance	$T_{stg(min)}$ to $T_{stg(max)}$	< 2000 FPM

Table 4 Reliability tests (by device type).

TEST	CONDITIONS	REQUIREMENTS
ESD and latch-up	ESD Human body model 2000 V, 100 pF, 1.5 kΩ	< 15% LTPD
	ESD Machine model 200 V, 200 pF, 0 Ω	< 15% LTPD
	latch-up 100 mA, 1.5 x V_{DD} (absolute maximum)	< 15% LTPD

Notes to Tables 1 to 4.

PPM = fraction of defective devices, in Parts Per Million.
LTPD = Lot Tolerance Percent Defective.
FPM = fraction of devices failing at test condition, in Failures Per Million.
FITS = Failures In Time Standardized.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	−0.3	6.5	V
V_I	input voltage (any input)	−0.3	V_{DD}+0.5	V
V_O	output voltage (any output)	−0.3	V_{DD}+0.5	V
I_O	output current (each output)	−	±10	mA
I_{IOK}	DC input or output diode current	−	±20	mA
T_{amb}	operating ambient temperature	−20	+70	°C

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −20 to +70 °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range (V_{DD}-V_{SS})		4.5	5.0	5.5	V
I_{DD}	total supply current		−	90	120	mA
Inputs						
CVBS						
V_{syn}	sync amplitude		0.1	0.3	0.6	V
t_{syn}	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		−150	0	+150	ns
t_{syd}	change in sync delay between all black and all white video input at nominal levels		0	−	25	ns
$V_{vid(p-p)}$	video input amplitude (peak-to-peak value)		0.7	1.0	1.4	V
	display PLL catching range		±7	−	−	%
Z_{src}	source impedance		−	−	250	Ω
C_I	input capacitance		−	−	10	pF
IREF						
R_g	resistor to ground		−	27	−	kΩ
POL						
V_{IL}	LOW level input voltage		−0.3	−	+0.8	V
V_{IH}	HIGH level input voltage		2.0	−	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	−	+10	µA
C_I	input capacitance		−	−	10	pF

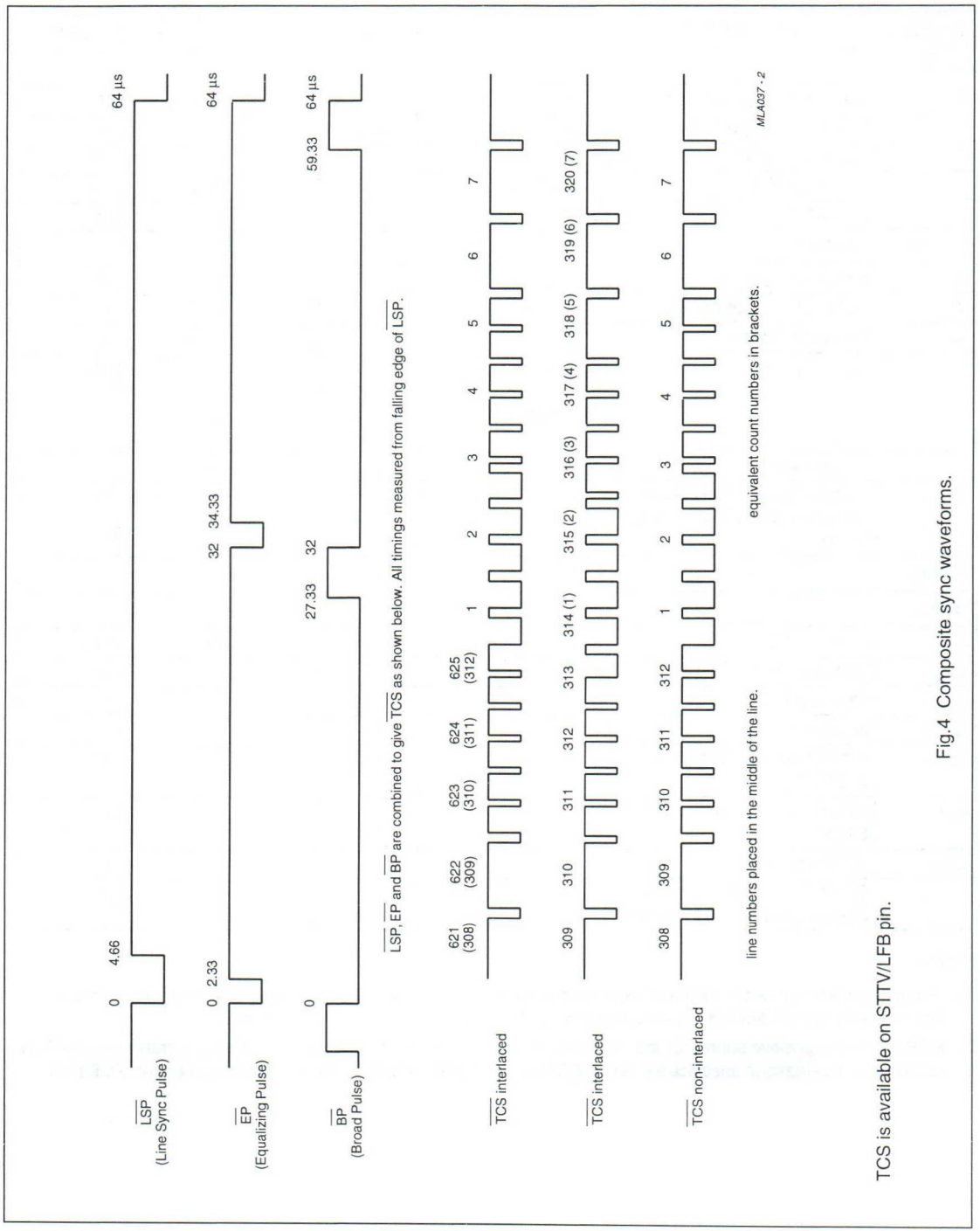
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LFB						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_I	input current	note 1	−1	–	+1	mA
t_{LFB}	delay between LFB front edge and input video line sync		–	250	–	ns
$\overline{VCR}$/FFB						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_I	input current	note 1	−1	–	+1	mA
RGBREF (NOTE 2)						
V_I	input voltage		−0.3	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_{DC}	DC current		–	–	10	mA
SCL						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
f_{SCL}	clock frequency		0	–	100	kHz
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
C_I	input capacitance		–	–	10	pF
Inputs/outputs						
CRYSTAL OSCILLATOR (OSCIN; OSCOUT)						
f_{XTAL}	crystal frequency		–	27	–	MHz
G_v	small signal voltage gain		3.5	–	–	–
G_m	mutual conductance	f = 100 kHz	1.5	–	–	mA/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	–	5	pF
BLACK						
C_{blk}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
SDA						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SDA						
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	3 to 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF
Outputs						
STTV						
G_{stt}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{tcs}	TCS amplitude		0.2	0.3	0.45	V
V_{DCs}	DC shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive current		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
R, G AND B						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = –1.6 mA; RGBREF ≤ V_{DD}–2 V	RGBREF –0.25 V	RGBREF	RGBREF +0.25 V	V
$\|Z_o\|$	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
I_{DC}	DC current		–	–	–3.3	mA
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
BLAN						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA; V_{DD} = 4.5 V	1.1	–	–	V
		I_{OH} = 0 mA; V_{DD} = 5.5 V	–	–	2.8	V
V_{OH}	allowed voltage at pin	with external pull-up	–	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ODD/$\overline{\text{EVEN}}$						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −1.6 mA	V_{DD}−0.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
$\overline{\text{COR}}$ AND Y (OPEN DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V
V_{OL}	LOW level output voltage	I_{OL} = 5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} −0.5 and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
T_{SK}	skew delay between display outputs R, G, B, $\overline{\text{COR}}$, Y and BLAN		–	–	20	ns
Timing						
I^2C-BUS						
t_{LOW}	clock LOW period		4	–	–	µs
t_{HIGH}	clock HIGH period		4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;STA}$	START hold time		4	–	–	µs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	µs

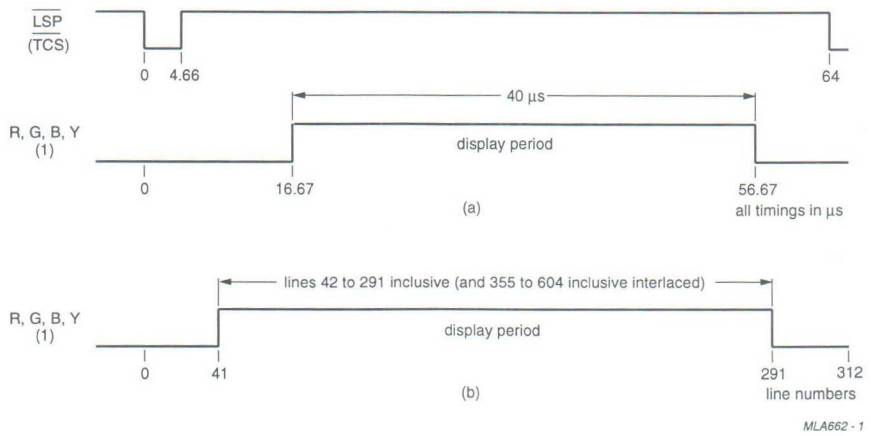
Notes

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ± 1 mA.
2. RGBREF is the positive supply for the RGB output pins and it must be able to source the I_{OH} current from the R, G and B pins. The leakage specification on RGBREF only applies when there is no current load on the RGB pins.



TCS is available on STTV/LFB pin.

Fig.4 Composite sync waveforms.



(1) Also BLAN in character and box blanking.

Fig.5 Display output timing (a) line rate (b) field rate.

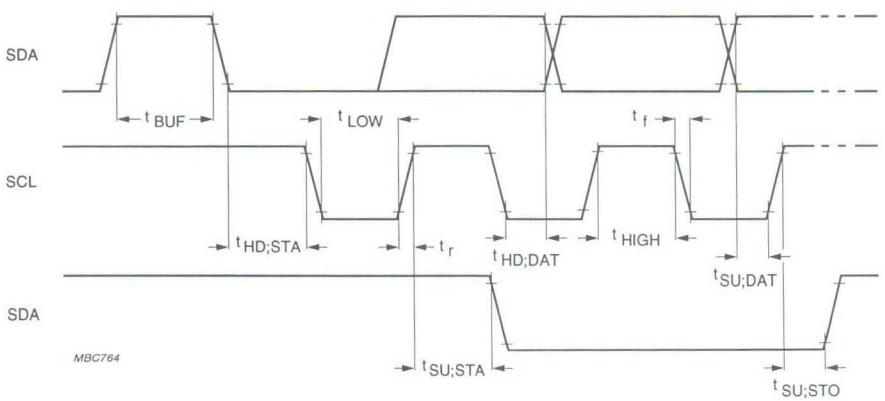


Fig.6 I²C-bus timing.

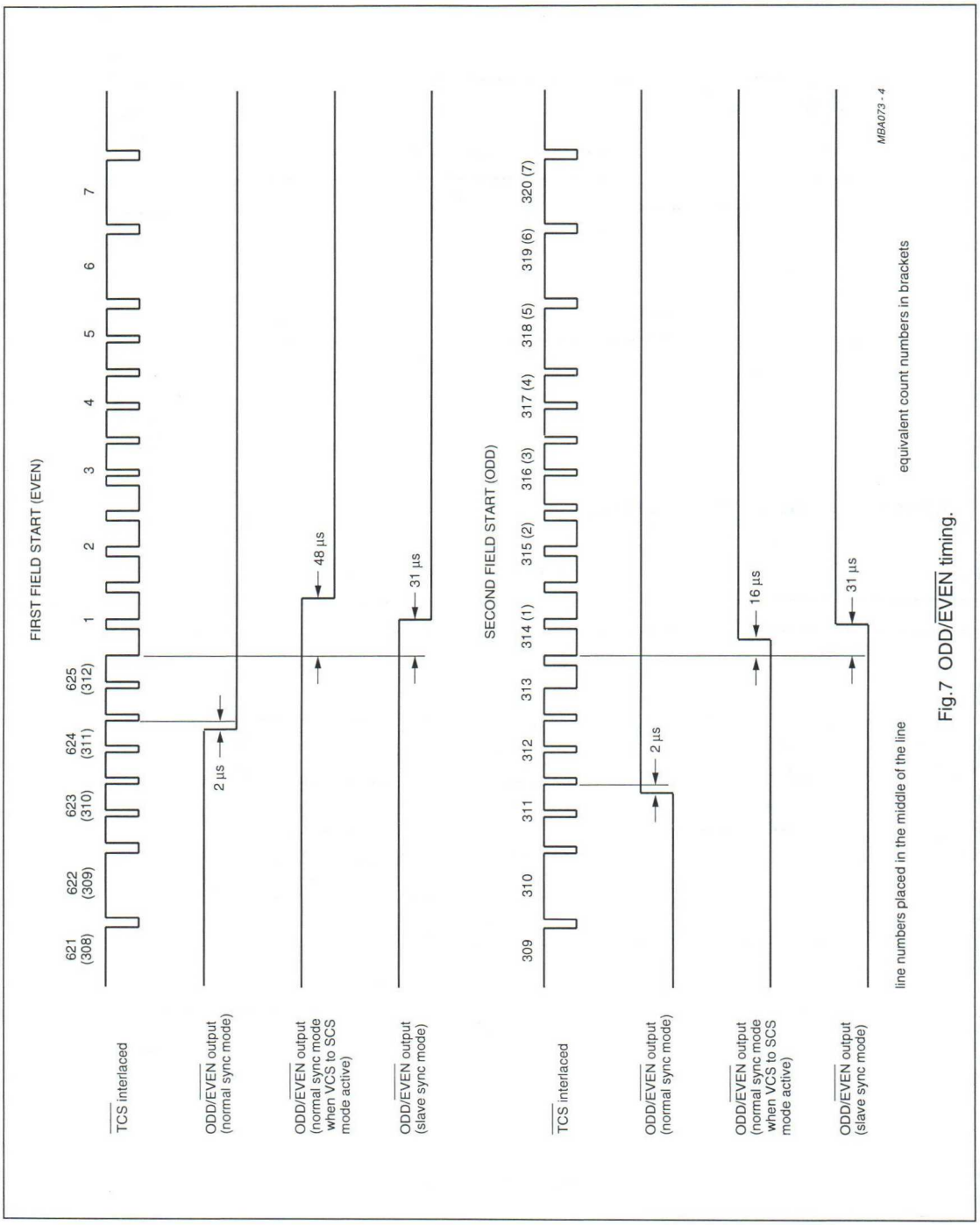
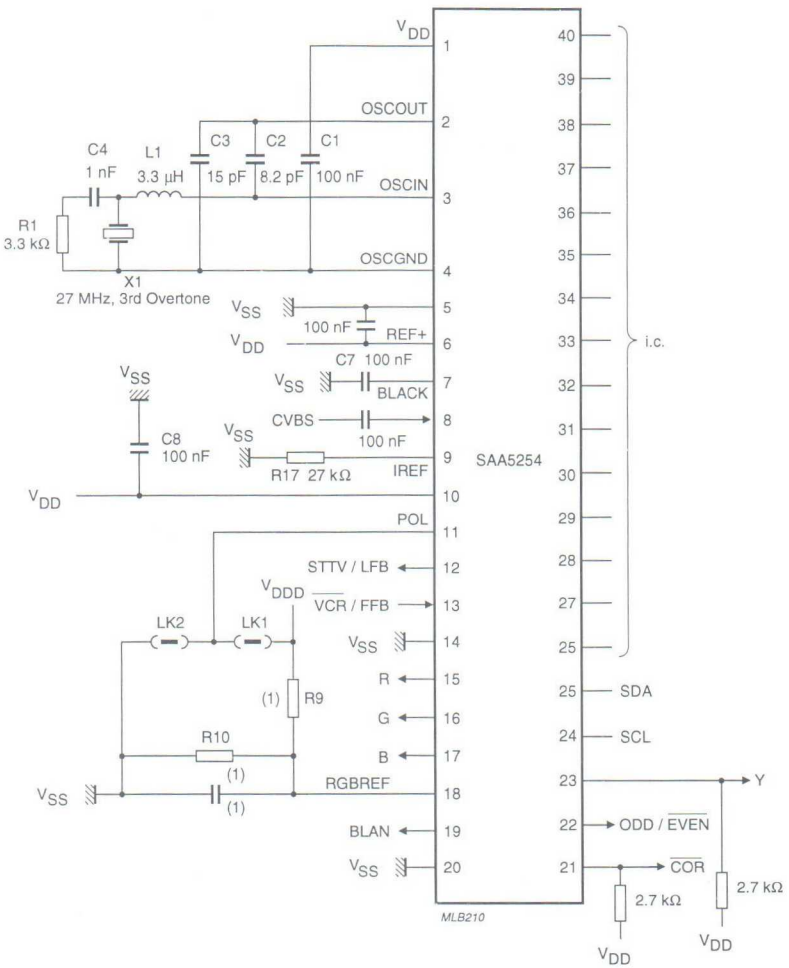


Fig.7 ODD/$\overline{\text{EVEN}}$ timing.

APPLICATION INFORMATION



(1) Value dependent on application.

Fig.8 Application diagram.

SAA5254 page memory organization

The organization of the page memory is shown in Fig.9. The device provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; row 24 is available for software generated status messages and FLOF/FASTEXT prompt information.

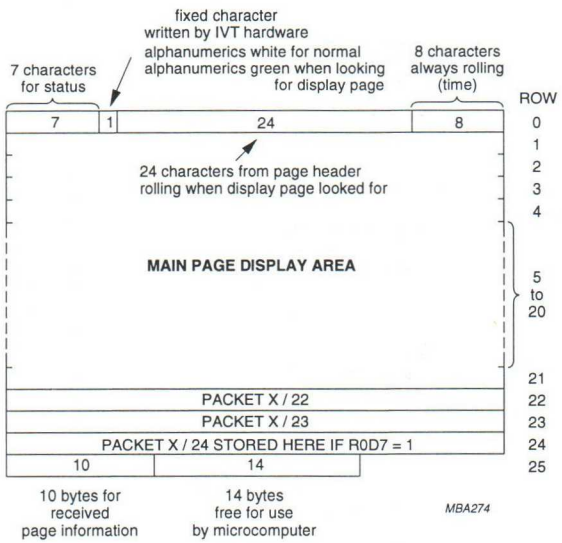


Fig.9 Basic page memory organization.

Row 0:

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by SAA5254 to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25:

The first 10 bytes of row 25 contain control data relating to the received page as shown in Table 5. The remaining 14 bytes are free for use by the microcomputer.



Fig.10 Organization of the extension memory.

Table 5 Row 25 received control data format.

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

Page number

MAG magazine
PU page units
PT page tens

PBLF page being looked for
$\overline{\text{FOUND}}$ LOW for page has been found
HAM.ER Hamming error in corresponding byte

Page sub-code

MU minutes units
MT minutes tens
HU hours units
HT hours tens

C4-C14 transmitted control bits.

Register maps

SAA5254 mode registers R0 to R11 are shown in Table 6. R0 to R10 are WRITE only; R11 is READ/WRITE. Register map (R3), for page requests, is shown in detail in Table 7.

Table 6 Register map.

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Adv. control	0	X24 POS	FREE RUN PLL	AUTO ODD/$\overline{\text{EVEN}}$	DISABLE HDR ROLL	DISPLAY STATUS ROW ONLY	DISABLE ODD/$\overline{\text{EVEN}}$	–	$\overline{\text{R11}}$/R11B SELECT
Mode	1	VCS TO SCS	$\overline{7+P}$/ 8-BIT	ACQ $\overline{\text{ON}}$/OFF	DISABLE PKT 26	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0
Page request address	2	–	–	–	–	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
		–	–	–	–	–	–	–	–
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS TOP	CURSOR ON	REVEAL ON	BOTTOM HALF	DOUBLE HEIGHT	BOX 24	BOX 1-23	BOX 0
		–	–	–	–	–	–	–	–
Cursor row	9	–	CLEAR MEM.	A0	R4	R3	R2	R1	R0
Cursor column	10	–	–	C5	C4	C3	C2	C1	C0
Cursor data	11	D7	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{\text{625}}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TEXT SIGNAL QUALITY	VCS SIGNAL QUALITY

Notes to Table 6

1. – indicates these bits are inactive and must be written to logic 0 for future compatibility.
2. All bits in registers R0 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R1, R5 and R6 which are set to logic 1.
3. All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha' white (00000111) as the acquisition circuit is enabled but the page is on hold.
4. TB must be set to logic 0 for normal operation.
5. The I^2C slave address is 0010001

Register description

R0 ADVANCED CONTROL - auto increments to Register 1

$\overline{R11}$/R11B SELECT	Selects reading of R11 or R11B
DISABLE ODD/$\overline{EVEN}$	Forces ODD/$\overline{EVEN}$ output LOW when logic 1
DISPLAY STATUS ROW	When SET = 1 and R1D6 = 1 open (8-bit mode) then all the text display is blanked out apart from the status row, this allows the page memory to be used for non-textural data, such as in the German TOP system
DISABLE HDR ROLL	Disables green rolling header and time
AUTO ODD/$\overline{EVEN}$	When set forces ODD/$\overline{EVEN}$ low if any TV picture displayed, if DISABLE ODD/$\overline{EVEN}$ = 0
FREE RUN PLL	Will force the PLL to free run in all conditions
X24 POS	Automatic display of FASTEXT prompt row when logic 1

R1 MODE - auto increments to Register 2

T0, T1	Interlace/non-interlace 312/313 line control (see Table 8)
TCS ON	Text composite sync or direct sync select (see Table 8 for FFB mode selection)
$\overline{DEW}$/FULL FIELD	Field-flyback or full channel mode
$\overline{7+P}$/8-BIT	7 bits with parity checking or 8-bit mode
ACQ $\overline{ON}$/OFF	Aquisition circuits turned off when logic 1
DISABLE PKT 26	Disable automatic processing of packet 26
VCS TO SCS	When logic 1 enables display of messages with 60 Hz input signal

R2 PAGE REQUEST ADDRESS - auto increments to Register 3

COL SC0 - SC2	Point to start column for page request data (see Table 7)
TB	Must be logic 0 for normal operation

R3 PAGE REQUEST DATA - does not auto increment (see Table 7)

R5 NORMAL DISPLAY CONTROL - auto increments to Register 6

R6 NEWSFLASH/SUBTITLE DISPLAY CONTROL - auto increments to Register 7

PON	Picture on
TEXT	Text on
COR	Contrast reduction on
BKGND	Background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 DISPLAY MODE - does not auto increment

BOX ON 0	Boxing function allowed on Row 0
BOX ON 1-23	Boxing function allowed on Row 1-23
BOX ON 24	Boxing function allowed on Row 24
DOUBLE HEIGHT	To display double height text
BOTTOM HALF	To select bottom half of page when DOUBLE HEIGHT = 1
REVEAL ON	To reveal concealed text
CURSOR ON	To display cursor
STATUS TOP	Row 25 displayed above or below the main text

R9 CURSOR ROW - auto increments to Register 10

R0 to R4	Active row for data written to or read from memory via the I²C-bus
A0	Selects display memory page (when = 0) or extension packet memory (when = 1)
CLEAR MEM.	When set to 1, clears the display memory. This bit is automatically reset

R10 CURSOR COLUMN - auto increments to Register 11 or 11B

C0 to C5	Active column for data written to or read from memory via the I²C-bus

R11 CURSOR DATA - does not auto increment

D0 to D7	Data read from/written to memory via I²C, at location pointed to by R9 and R10. This location automatically increments each time R11 is accessed

R11B DEVICE STATUS - does not auto increment

VCS SIGNAL QUALITY	Indicates that the video signal quality is good and PLL is phase locked to input video when = 1
TEXT SIGNAL QUALITY	If a good teletext signal is being received when = 1
ROM VER R0 to R4	Indicated language/ROM variant. For Western European = 11000
$\overline{625}$/525 SYNC	If the input video is a 525 line signal when = 1

Table 7 Register map for page requests (R3).

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 7

1. Abbreviations are as for Table 5 except for DO CARE bits.
2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
3. If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
4. Columns auto-increment on successive I²C-bus transmission bytes.
5. X = Don't care.

Table 8 Interlace/non-interlace 312/313 line control and ODD/EVEN field detection option.

TCS ON FFB MODE	T1	T0	RESULT
x	0	0	interlaced 312.5/312.5 lines
x	0	1	non-interlaced 312/313 lines (note 1)
x	1	0	non-interlaced 312/312 lines (note 1)
0	1	1	SCS (scan composite sync) mode: FFB leading edge in first broad pulse of field
1	1	1	SCS (scan composite sync) mode: FFB leading edge in second broad pulse of field

Notes to Table 8

1. Reverts to interlaced mode if a newsflash or subtitle is being displayed.
2. x = Don't care.

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional 2-pin design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone, as shown in Fig.11. The crystal characteristics are given in Table 9.

Table 9 Crystal characteristics.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)					
C1	series capacitance	–	1.7	–	pF
C0	parallel capacitance	–	5.2	–	pF
C_L	load capacitance	–	20	–	pF
Rr	resonant resistance	–	–	50	Ω
R1	series resistance	–	20	–	Ω
Xa	ageing	–	–	±5	10^{-6}/yr
Xj	adjustment tolerance	–	–	±25	10^{-6}
Xd	drift	–	–	±25	10^{-6}

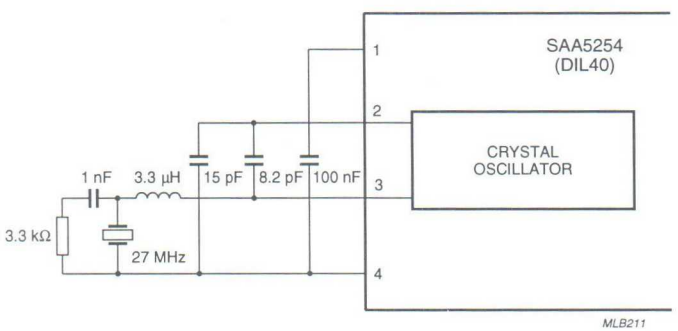


Fig.11 Crystal oscillator application diagram.

Character sets

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character sets differ only in 13 national option characters as indicated in Table 12 with reference to their table position in the basic character matrix illustrated in Table 11. The SAA5254 automatically decodes transmission bits C12 to C14. Table 10 illustrates the character matrixs.

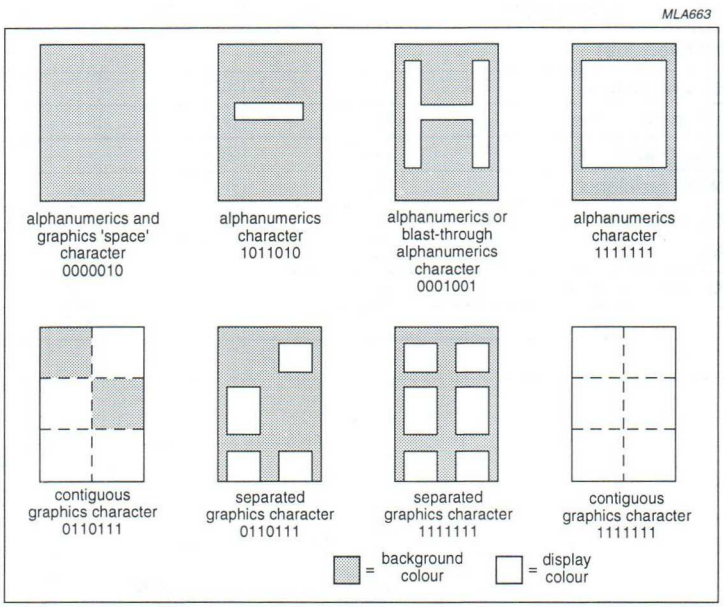


Fig.12 Character format.

Table 10a SAA5254P/E character data input decoding, West European languages.

BITS b_8				0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7				0	0	0	0	0	0	1	1	1		1		1	1	1	1	1	1
b_6				0	0	1	1	1	1	0	0	1		1		1	1	1	1	1	1
b_5				0	1	0	1	1	1	0	1	0		1		0	0	0	1	1	1
b_4	b_3	b_2	b_1	column / row	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0	0	0	0	0	alpha - numerics black	graphics black																
0	0	0	1	1	alpha - numerics red	graphics red																
0	0	1	0	2	alpha - numerics green	graphics green																
0	0	1	1	3	alpha - numerics yellow	graphics yellow																
0	1	0	0	4	alpha - numerics blue	graphics blue																
0	1	0	1	5	alpha - numerics magenta	graphics magenta																
0	1	1	0	6	alpha - numerics cyan	graphics cyan																
0	1	1	1	7	alpha - numerics white **	graphics white																
1	0	0	0	8	flash	conceal display																
1	0	0	1	9	steady **	contiguous graphics **																
1	0	1	0	10	end box **	separated graphics																
1	0	1	1	11	start box	ESC *																
1	1	0	0	12	normal height	black back - ground **																
1	1	0	1	13	double height	new back - ground																
1	1	1	0	14	SO *	hold graphics																
1	1	1	1	15	SI *	release graphics **																

MBA429

For character version number (11000) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 10b SAA5254P/H character data input decoding, East European languages.

BITS b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓	row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
		b_8 0 b_7 0 b_6 0 b_5 0	0 0 0 1	0 or 1 0 1 0	0 0 1 0	0 or 1 0 1 1	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1		
0 0 0 0	0	alpha - numerics black	graphics black																
0 0 0 1	1	alpha - numerics red	graphics red																
0 0 1 0	2	alpha - numerics green	graphics green																
0 0 1 1	3	alpha - numerics yellow	graphics yellow																
0 1 0 0	4	alpha - numerics blue	graphics blue																
0 1 0 1	5	alpha - numerics magenta	graphics magenta																
0 1 1 0	6	alpha - numerics cyan	graphics cyan																
0 1 1 1	7	alpha - numerics white **	graphics white																
1 0 0 0	8	flash	conceal display																
1 0 0 1	9	steady **	contiguous graphics **																
1 0 1 0	10	end box **	separated graphics																
1 0 1 1	11	start box	ESC *																
1 1 0 0	12	normal height **	black back - ground **																
1 1 0 1	13	double height	new back - ground																
1 1 1 0	14	SO *	hold graphics																
1 1 1 1	15	SI *	release graphics **																

MLA961

For character version number (11001) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 10c SAA5254P/T character data input decoding, West European and Turkish languages.

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0	0	1	1	1	1	1	1
b_7	0	0	0	0	0	0	1	1	1	1	0	0	1	1	1	1
b_6	0	0	1	1	1	1	0	0	1	1	0	0	1	1	1	1
b_5	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0 alpha - numerics black	graphics black			0		§	P	°		p		@	İ	é	à	i	Á
0 0 0 1	1 alpha - numerics red	graphics red	!		1		A	Q	a		q		—	ı	ù	è	¿	À
0 0 1 0	2 alpha - numerics green	graphics green	"		2		B	R	b		r		¼	ş	à	â	ü	È
0 0 1 1	3 alpha - numerics yellow	graphics yellow	#		3		C	S	c		s		£	Ł	£	é	ç	Í
0 1 0 0	4 alpha - numerics blue	graphics blue	$		4		D	T	d		t		$	ğ	$	ï	$	Ï
0 1 0 1	5 alpha - numerics magenta	graphics magenta	%		5		E	U	e		u				ã	Ã	ª	ó
0 1 1 0	6 alpha - numerics cyan	graphics cyan	&		6		F	V	f		v				õ	Õ	º	Ò
0 1 1 1	7 alpha - numerics white **	graphics white	'		7		G	W	g		w		?		·	Ç	Ñ	Ú
1 0 0 0	8 flash	conceal display	(		8		H	X	h		x		‖	ö	ò	ô	ñ	Ì
1 0 0 1	9 ** steady	** contiguous graphics	)		9		I	Y	i		y		¾	ç	è	û	è	Ù
1 0 1 0	10 ** end box	separated graphics	*		:		J	Z	j		z		÷	ü	ì	ç	à	↓
1 0 1 1	11 start box	* ESC	+		;		K	Ä	k		ä		←	Ş	°	ë	á	É
1 1 0 0	12 ** normal height	** black back - ground	,		<		L	Ö	l		ö		½	Ö	ç	ê	é	ä
1 1 0 1	13 double height	new back - ground	−		=		M	Ü	m		ü		→	Ç	→	ù	í	Ó
1 1 1 0	14 * SO	hold graphics	.		>		N	^	n		ß		↑	Ü	↑	î	ó	Ã
1 1 1 1	15 * SI	** release graphics	/		?		O	_	o				#	Ğ	#	#	ú	Î

MBA431

For character version number (11010) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Notes to Table 10

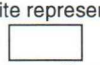
1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Characters may be referred to by column and row, For example 2/5 refers to %.
3. Black represents displayed colour. White represents backgound.
4. Character rectangle shown as follows: 
5. The SAA5254 national option characters are illustrated in Table 12.
6. Characters 4b/11, 4b/12, 5b/10, 5b/11 and 5b/12 are special characters for combining with character 4b/10.
7. National option characters will be developed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Table 12.
8. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.

Table 11 SAA5254 Basic character matrix.



Where: NC = national option character position.

Table 12a SAA5254P/E national option character set.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MEA559

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

Table 12b SAA5254P/H national option character set.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
POLISH	0	0	0	#	ń	ą	Ż	Ś	Ł	ć	ó	ę	ż	ś	ł	ź
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
SERBO-CROAT	1	0	1	#	½	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECHOSLOVAKIA	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN	1	1	1	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

MLA966

(1) PHCB are the Page Header Control Bits. Other combinations default to German. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 11.

Table 12c SAA5254P/T national option character set.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
TURKISH	1	1	0	Ţ	ğ	İ	Ş	Ö	Ç	Ü	Ğ	ı	ş	ö	ç	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MBA430

(1) PHCB are the Page Header Control Bits. Other combinations default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 11.

Integrated VIP and teletext decoder (IVT2.0)

SAA5260

FEATURES

- Complete teletext decoder in a single 48-pin DIL package
- Single +5 V power supply
- Digital data slicer and display clock phase-locked loop reduce peripheral components to a minimum
- Both video and scan related synchronization modes are supported
- 4096 colour palette, with 16 different foreground plus 16 different background colours
- Full row and border background colours covering the whole screen area
- Background colour control characters for highlighting text areas
- 224 characters in ROM (12 x 10 matrix), giving wide language coverage and additional graphics symbols for on-screen displays
- Double width and double size decoding as well as double height
- Foreground character processing for language extension possible without display flicker
- Analog RGB outputs with simple interface to colour decoder ICs
- Data capture performance similar to SAA5231 (VIP2)
- 5 channel acquisition system for fast page capture
- Pointer system to connect any acquisition channel to any page memory
- Interfaces to 32 K x 8-bit static RAM (8 K x 8 also possible)
- Extension packet option including full error correction in hardware (8/4 and 24/18 Hamming)
- 7-bit + parity, 8-bit, full page Hamming and mixed Hamming/7-bit + parity acquisition options, selected per channel to allow e.g. optimum TOP decoding
- End of page detectors with interrupt generation for fast data processing
- Separate text and video signal quality detectors, 625/525 video status and language version all readable via I²C-bus
- Automatic ODD/$\overline{\text{EVEN}}$ output control with manual override
- Control of display PLL free-run and rolling header via I²C-bus
- VCS to SCS mode for stable 525 line status display
- Option for battery back-up of page memory.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5	5.5	V
I_{DD}	supply current	–	75	150	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature range	–20	–	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5260P/E	48	DIL	plastic	SOT240

DESCRIPTION

The SAA5260 is a single-chip teletext decoder IC for decoding 625-line based World System Teletext transmissions. The device is based on the IVT1.0 (SAA5246) with additional features to provide a higher performance decoder. A larger memory (32 K x 8) can be connected for faster access to pages and better display facilities are provided, including more symbols and colours.

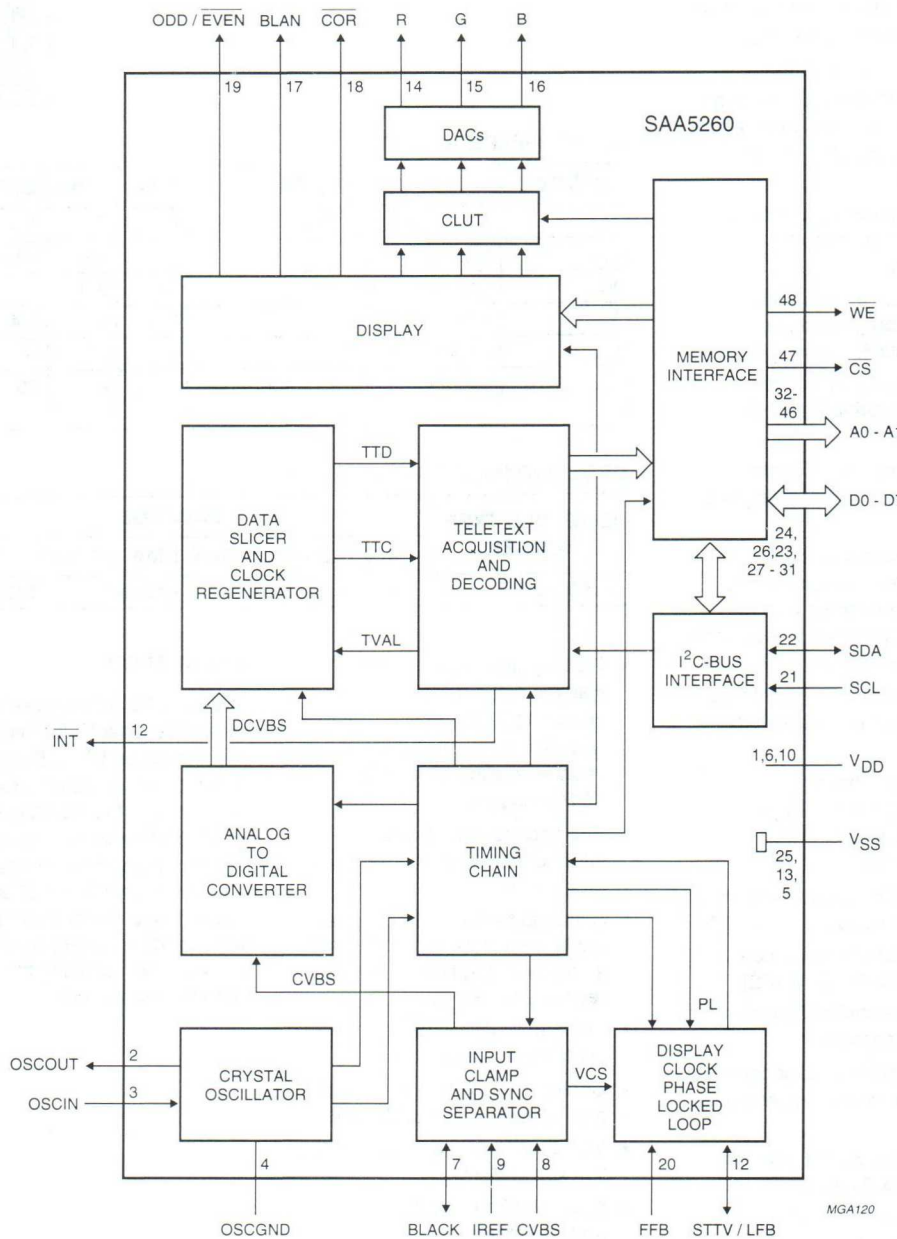


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD}	1, 6, 10	+5 V supply
OSCOUT	2	27 MHz crystal oscillator output
OSCIN	3	27 MHz crystal oscillator input
OSCGND	4	0 V crystal oscillator ground
V_{SS}	5, 13, 25	0 V ground
BLACK	7	video black level storage pin, connected to ground via a 100 nF capacitor
CVBS	8	composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor
IREF	9	reference current input pin, connected to ground via a 27 kΩ resistor
STTV/LFB	11	sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode)
$\overline{INT}$	12	interrupt output from end of page detector, X/27, X/29 and 8/30 flags
R	14	dot rate character output of the RED colour information
G	15	dot rate character output of the GREEN colour information
B	16	dot rate character output of the BLUE colour information
BLAN	17	dot rate fast blanking output
$\overline{COR}$	18	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open drain output
ODD/$\overline{EVEN}$	19	25 Hz output synchronized with the CVBS input's field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents
FFB	20	field flyback input
SCL	21	serial clock input for I²C-bus. It can still be driven HIGH during power-down of the device
SDA	22	serial data port for the I²C-bus. Open drain output. It can still be driven HIGH during power-down of the device
D2	23	data input/output for external RAM
D0	24	data input/output for external RAM
D1	26	data input/output for external RAM
D3 to D7	27 to 31	data inputs/outputs for external RAM
A0 to A14	32 to 46	address outputs for external RAM
$\overline{CS}$	47	output to RAM if memory not to be cleared on power-up
$\overline{WE}$	48	write enable to external RAM

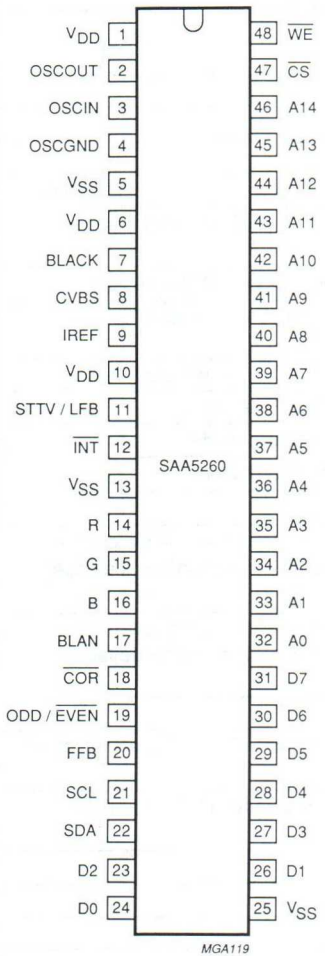


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	−0.3	6.5	V
V_I	input voltage (any input)	−0.3	V_{DD}+0.5	V
V_O	output voltage (any output)	−0.3	V_{DD}+0.5	V
I_O	output current (each output)	−	±10	mA
I_{IOK}	DC input or output diode current	−	±20	mA
T_{amb}	operating ambient temperature range	−20	70	°C
T_{stg}	storage temperature range	−55	125	°C
V_{stat}	electrostatic handling human body model (note 1)	−2000	2000	V

Note

1. The human body model ESD simulation is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor; this produces a single discharge transient. Reference Philips Semiconductors test method UZW-B0/FQ-A302 (compatible with MIL-STD method 3015.7).

Failure Rate

The failure rate at T_{amb} = 55 °C will be a maximum of 1000 FITS (1 FIT = 1 x 10^{-9} failures per hour).

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −20 to +70 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		4.5	5	5.5	V
I_{DD}	total supply current		–	75	150	mA
Inputs						
CVBS						
V_{syn}	sync amplitude		0.1	0.3	0.6	V
t_{syn}	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		−150	0	150	ns
t_{syd}	change in CVBS to TCS delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{vid(p-p)}$	video input amplitude (peak-to-peak)		0.7	1	1.4	V
	display PLL catching range		±7	–	–	%
Z_{src}	source impedance		–	–	250	Ω
C_I	input capacitance		–	–	10	pF
IREF						
R_g	resistor to ground		–	27	–	kΩ
V_g	voltage on pin 9		–	$V_{DD}/2$	–	V
LFB						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
I_I	input current	note 1	−1	–	1	mA
t_{LFB}	delay between LFB front edge and input video line sync		–	250	–	ns
FFB						
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
I_I	input current	note 1	−1	–	1	mA
SCL						
V_{IL}	LOW level input voltage		−0.3	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
f_{SCL}	clock frequency		0	–	150	kHz
t_r	input rise time	10% to 90%	–	–	2	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_f	input fall time	90% to 10%	–	–	2	µs
C_I	input capacitance		–	–	10	pF
Inputs/outputs						
BLACK						
C_{blk}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	10	µA
D0 TO D7						
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	10	µA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
C_L	load capacitance		–	–	120	pF
SDA						
V_{IL}	LOW level input voltage		–0.3	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	10	µA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	3 to 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF
Outputs						
STTV						
G_{stt}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{tcs}	TCS amplitude		0.2	0.3	0.45	V
V_{DCs}	DC shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
A0 TO A14 ADDRESS OUTPUT TO MEMORY						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
C_I	input capacitance		–	–	120	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
$\overline{WE}$						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
CS						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
C_L	load capacitance		–	–	120	pF
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
R, G AND B						
R_L	load resistance to V_{SS}		–	150	–	Ω
I_{OL}	output current (black level)		–10	0	10	μA
I_{OL}	output current (full amplitude)	at nominal V_{DD}	–6.0	–6.67	–7.3	mA
C_L	load capacitance		–	–	20	pF
t_r	output rise time	10% to 90%; R_L = 150 Ω; C_L = 20 pF	–	–	20	ns
t_f	output fall time	90% to 10%; R_L = 150 Ω; C_L = 20 pF	–	–	20	ns
BLAN						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.2 mA	1.1	–	–	V
V_{OH}	HIGH level output voltage	I_{OH} = 0 mA	–	–	2.8	V
V_{OH}	allowed voltage at pin	with extenal pull-up	–	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
ODD/$\overline{EVEN}$						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –1.6 mA	V_{DD}–0.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns
$\overline{COR}$ (OPEN DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.4	V
V_{OL}	LOW level output voltage	I_{OL} = 5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} −0.5 and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
TSK	skew delay between display outputs R, G, B, $\overline{COR}$, and BLAN		–	–	20	ns
$\overline{INT}$ (OPEN DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
I_{LO}	output leakage current		−10	–	10	µA
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 3.3 kΩ to V_{DD} measured between 4 V and 1 V	–	–	50	ns
Timing						
I²C-BUS						
f_{DAT}	I²C data rate for:					
	all registers		–	–	150	kHz
	all registers except display RAM write/reads		–	–	350	kHz
	other devices on bus (IVT will not lock up)		–	–	400	kHz
t_{LOW}	clock LOW period		1.4	–	–	µs
t_{HIGH}	clock HIGH period		1.4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;STA}$	START hold time		1.4	–	–	µs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		1.4	–	–	µs
RAM INTERFACE						
t_{CY}	cycle time		–	500	–	ns
t_{ADDR}	address active time		450	500	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{ACC}	access time from address		–	–	150	ns
t_{DH}	data hold time from address		0	–	–	ns
t_{WE}	$\overline{WE}$ LOW from address change		40	–	–	ns
t_{WEW}	$\overline{WE}$ pulse width		100	–	–	ns
t_{DS}	data set-up time to $\overline{WE}$ HIGH		60	–	–	ns
t_{DHWE}	data hold time from $\overline{WE}$ HIGH		0	–	20	ns
t_{WR}	write recovery time		20	–	–	ns
t_{DE}	data enable from $\overline{WE}$ LOW		10	–	–	ns

Note to the characteristics

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ± 1 mA.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

Fig.3 Composite sync waveforms.

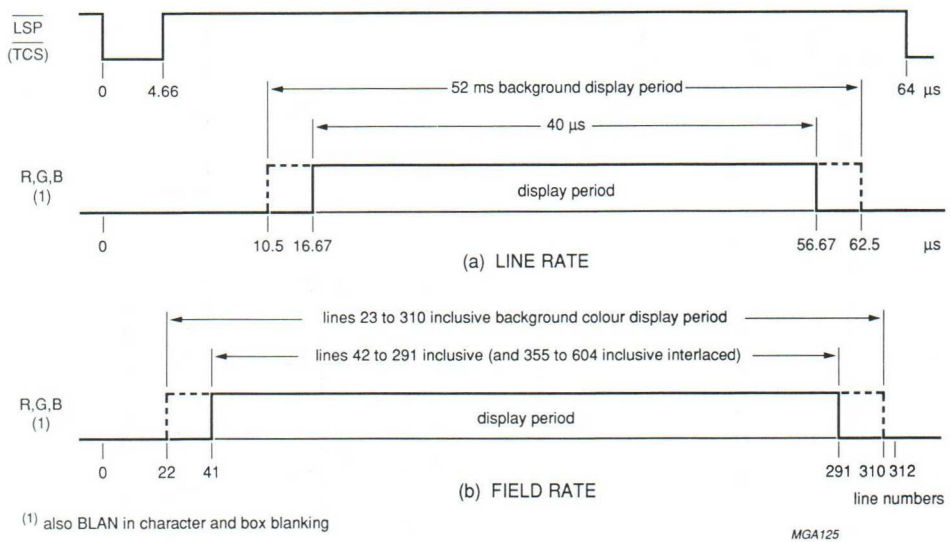


Fig.4 Display output timing (a) line rate (b) field rate.

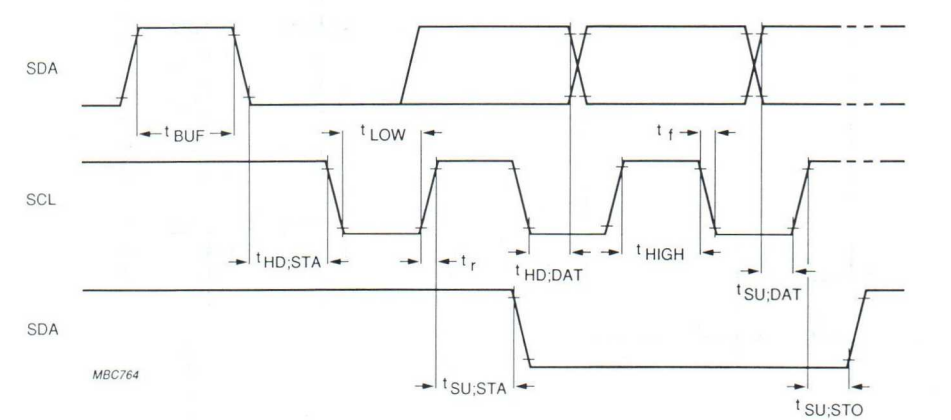


Fig.5 I²C-bus timing.

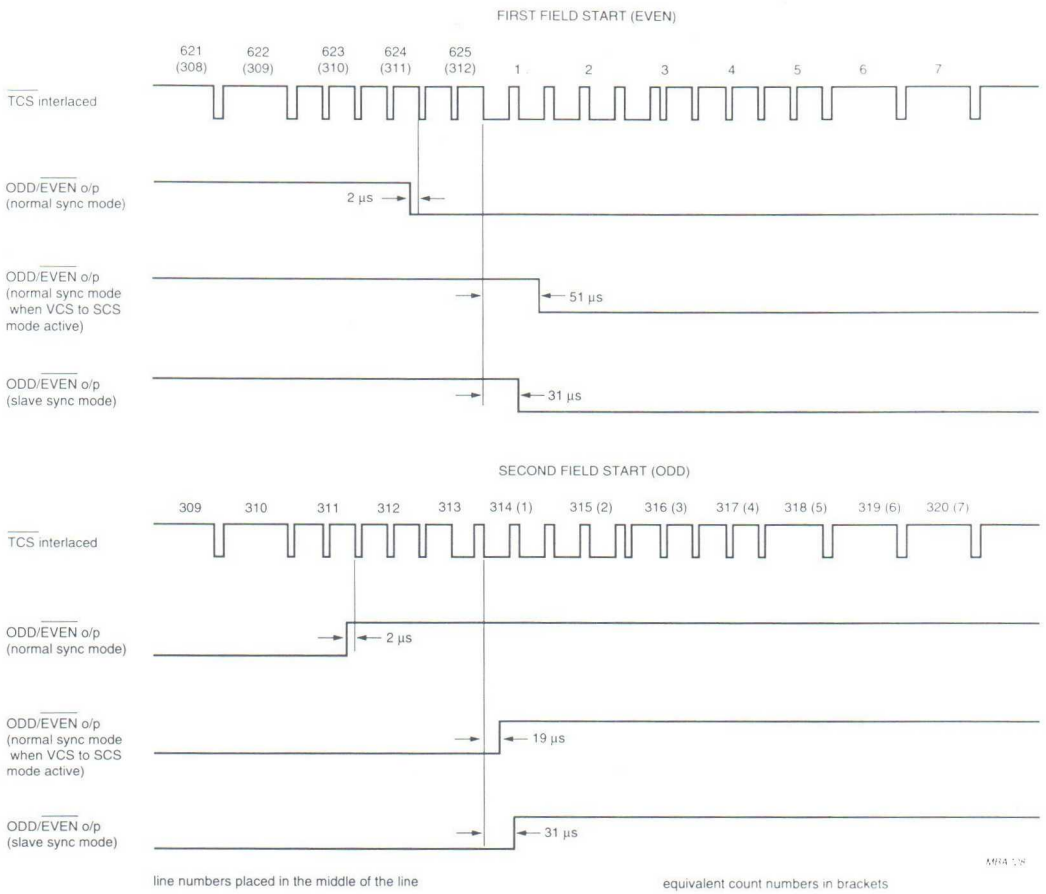


Fig.6 ODD/EVEN timing.

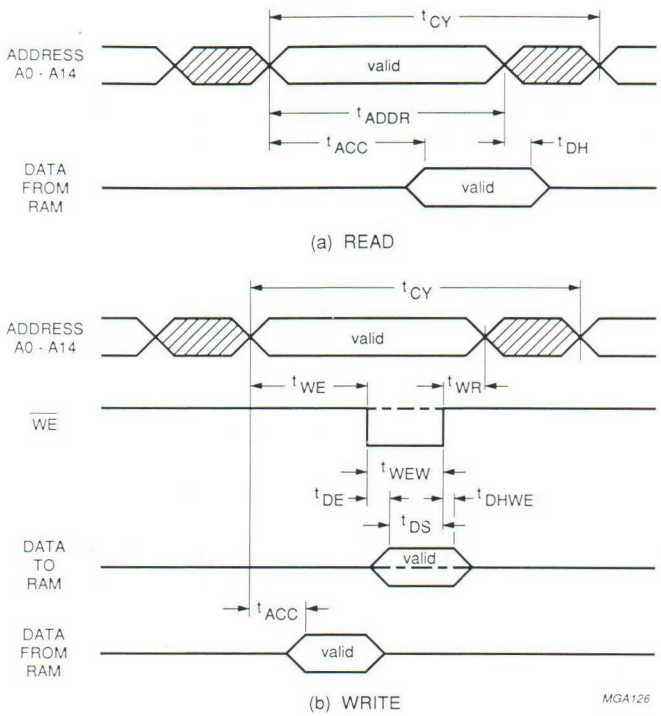


Fig.7 Memory interface timing (a) read (b) write.

APPLICATION INFORMATION

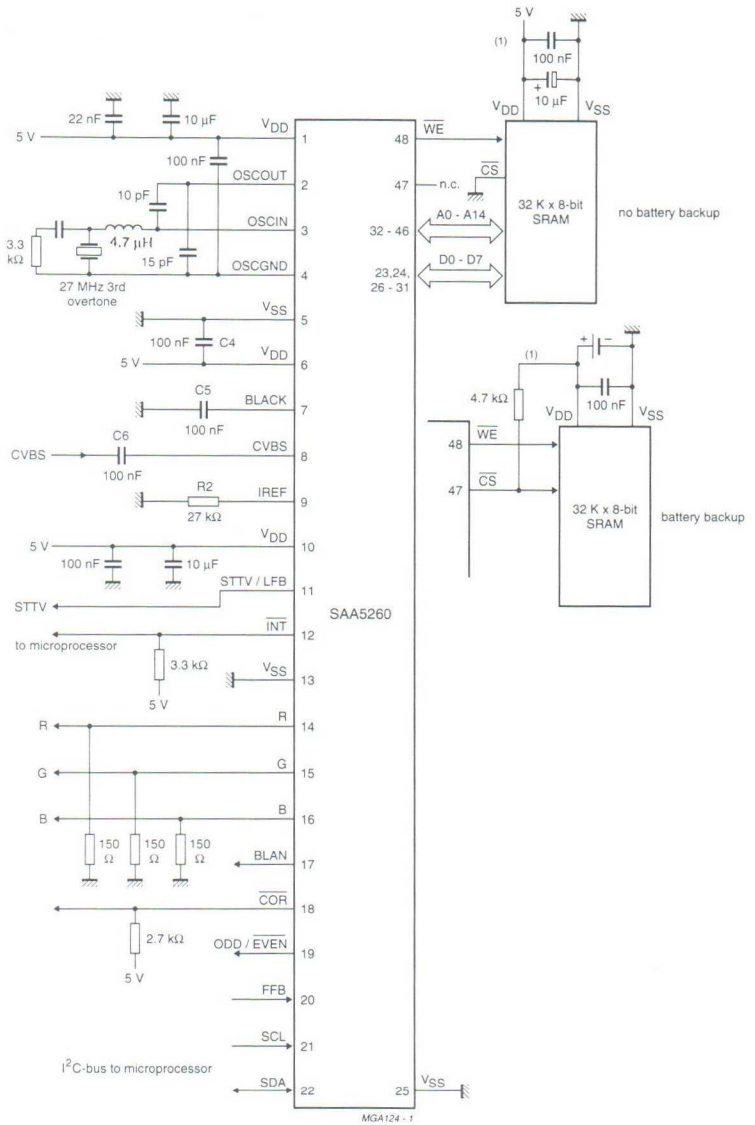
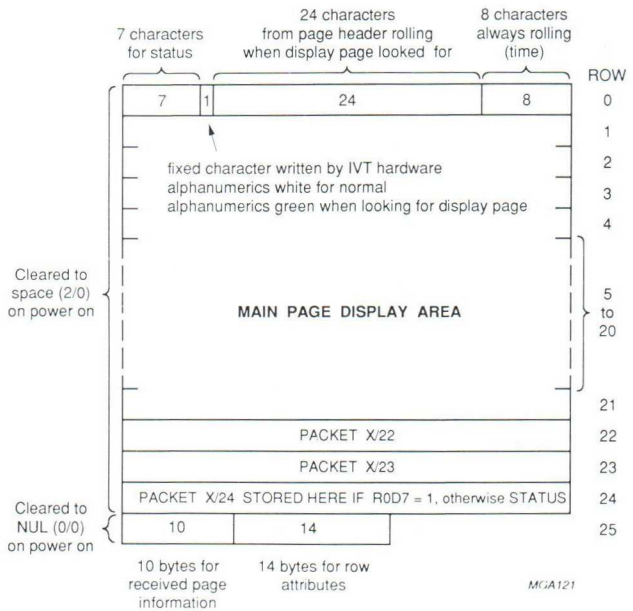


Fig.8 Application diagram.

(1) Optional connections if battery backed up memory required. The 5 V supply shown comes from battery. If battery back-up is not used, then $\overline{CS}$ of RAM is connected to ground and the $\overline{CS}$ output from the device is not used.

SAA5260 page memory organization

The organization of the page memory is shown in Fig.9. The display format is 40 characters by 25 rows. Rows 0 to 23 form the teletext page; row 24 is available for software generated status messages and FLOF/FASTEXT prompt information.



Row 0:
Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by SAA5260 to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25:
The first 10 bytes of row 25 contain control data relating to the received page as shown in Table 1.

Fig.9 Basic page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

Page number

MAG magazine

PU page units

PT page tens

PBLF page being looked for

$\overline{\text{FOUND}}$ LOW for page has been found

HAM.ER Hamming error in corresponding byte

Page sub-code

MU minutes units

MT minutes tens

HU hours units

HT hours tens

C4-C14 transmitted control bits.

The remaining 14 bytes of row 25 contain the row attributes for defining the default background colour of each row and the chapter from which it is to be displayed, as shown in Table 2.

Table 2 Row 25 row attributes

D0	TR	R0R	R2R	R4R	R6R	R8R	R10R	R12R	R14R	R16R	R18R	R20R	R22R	R24R
D1	TG	R0G	R2G	R4G	R6G	R8G	R10G	R12G	R14G	R16G	R18G	R20G	R22G	R24G
D2	TB	R0B	R2B	R4B	R6B	R8B	R10B	R12B	R14B	R16B	R18B	R20B	R22B	R24B
D3	-	DR0	DR2	DR4	DR6	DR8	DR10	DR12	DR14	DR16	DR18	DR20	DR22	DR24
D4	BR	R1R	R3R	R5R	R7R	R9R	R11R	R13R	R15R	R17R	R19R	R21R	R23R	-
D5	BG	R1G	R3G	R5G	R7G	R9G	R11G	R13G	R15G	R17G	R19G	R21G	R23G	-
D6	BB	R1B	R3B	R5B	R7B	R9B	R11B	R13B	R15B	R17B	R19B	R21B	R23B	-
D7	-	DR1	DR3	DR5	DR7	DR9	DR11	DR13	DR15	DR17	DR19	DR21	DR23	-
COLUMN	10	11	12	13	14	15	16	17	18	19	20	21	22	23

R, G and B are the settings of the default background colour attribute. They only correspond to RED, GREEN and BLUE colour outputs when the colour look-up table is in the default condition; at other times, they are simply entries in the colour look-up table.

T — Top border of screen, above row 0 (or above status row if R1D7 = 1)

B — Bottom border of screen, below the status row (or below row 23 if R10D7 = 1)

R1 etc. — Row 1 display

DR2 etc. — Display row 2 etc. defines whether the text for this display row comes from the normal display chapter register (0) or supplementary display chapter register (1)

These letters are combined as appropriate, e.g. R8R = red default background for row 8, BG = green default background for bottom screen border.

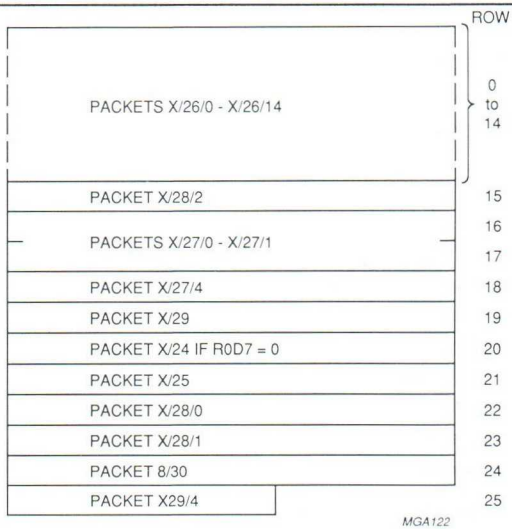


Fig.10 Organization of the extension memory.

Extension packet memory organization

When in extension packet enable mode, the rows of information are organized as shown in Fig.10.

The page-related extension packets are stored in the next higher memory chapter relative to the corresponding basic page data, e.g. basic page chapter 6, extension packets chapter 7.

Some extension packets are not page related; these are stored in the chapters as shown in Tables 3 and 4.

Packet 8/30: Stored in a chapter according to the designation code. Pairs of designation codes are stored in the same chapter, owing to the use of the LSB as a flag indicating VBI or full channel.

Table 3 Packet 8/30 storage

PACKET	CHAPTER
8/30/0, 8/30/1	1
8/30/2, 8/30/3	3
8/30/4, 8/30/5	5
8/30/6, 8/30/7	7
8/30/8, 8/30/9	9
8/30/10, 8/30/11	11
8/30/12, 8/30/13	13
8/30/14, 8/30/15	15

Packet 29: Two versions are stored in row 19, X/29/0 (for colour definition) and X/29/1 (for character set definition) and one in row 25, X/29/4.

Table 4 Packet 29 storage

PACKET	CHAPTER
8/30/0 and 4	1
1/29/0 and 4	3
2/29/0 and 4	5
3/29/0 and 4	7
4/29/0 and 4	9
5/29/0 and 4	11
6/29/0 and 4	13
7/29/0 and 4	15
8/29/1	17
1/29/1	19
2/29/1	21
3/29/1	23
4/29/1	25
5/29/1	27
6/29/1	29
7/29/1	31

Register maps

SAA5260 mode registers are shown in Table 5. R0 to R15 are WRITE only; R16A is READ/WRITE; R16B and R16C are READ only.

Table 5 Register map

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Mode	0	X24 POS	EXTN. PACKET ENABLE	$\overline{\text{DEW}}$/ FULL FIELD	DISABLE HDR ROLL	B.T. NUMBER ENABLE	POL	BOX TIME	BOX HEADER
Sync	1	VCS TO SCS	FREE RUN PLL	AUTO ODD/ $\overline{\text{EVEN}}$	DISABLE ODD/ $\overline{\text{EVEN}}$	VCR	TCS ON	T1	T0
Acq. control	2	ACQ. $\overline{\text{ON}}$/OFF	ACQ. CCT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
Acq. Mode A	4	–	–	–	H4	H3	H2	H1	H0
Acq. Mode B	5	–	–	–	S4	S3	S2	S1	S0
Display chapter (normal)	6	–	–	–	A4	A3	A2	A1	A0
Display chapter (supplm.)	7	–	–	CLUT SELECT	A4	A3	A2	A1	A0
Display (normal)	8	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display (news flash)	9	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control	10	STATUS $\overline{\text{BTM}}$/TOP	CURSOR ON	$\overline{\text{CONCEAL}}$ REVEAL	$\overline{\text{TOP}}$/ BOTTOM	$\overline{\text{SINGLE}}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
CLUT data 1	11	G3	G2	G1	G0	R3	R2	R1	R0
CLUT data 2	12	A3	A2	A1	A0	B3	B2	B1	B0
Active chapter	13	–	–	CLEAR MEM.	A4	A3	A2	A1	A0
Active row	14	–	CURSOR MOVE	INC BY ROW	R4	R3	R2	R1	R0
Active column	15	$\overline{\text{R16C}}$/ R16C	$\overline{\text{R16A}}$/ R16B	C5	C4	C3	C2	C1	C0

Table 5 Register map *(continued)*

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Active data	16A	D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)
Device status	16B	$\overline{625}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TEXT SIGNAL QUALITY	VCS SIGNAL QUALITY
End of page flags	16C	8/30 ARRIVED	X/29 ARRIVED	X/27 ARRIVED	AC4	AC3	AC2	AC1	AC0

Notes to Table 5

1. – indicates these bits are inactive and must be written to logic 0 for future compatibility.
2. All bits in registers R0 to R15 are cleared to logic 0 on power-up, except bits D0 and D1 of registers R1, R8 and R9 which are set to logic 1. The CLUT data (accessed from R11 and R12) is cleared to normal "level 1" colours.

Register description

R0 MODE - auto increments to Register 1

BOX HEADER	Selects automatic boxing of first 7 characters on display Row 0
BOX TIME	Selects automatic boxing of last 8 characters on display Row 0
POL	Selects polarity of STTV output or LFB and FFB input signals. (When POL = 1, then TCS will be positive-going syncs and LFB/FFB will be negative; when POL = 0, TCS will be negative-going syncs and LFB/FFB positive)
B.T.NUMBERS ENABLE	Selects blast-through numbers instead of supplementary background colour attributes
DISABLE HDR ROLL	Stops the display update of rolling time and green rolling header during page request when = 1. Time updates on page reception only
$\overline{\text{DEW}}$/FULL FIELD	Field-flyback or full channel mode
EXTN. PACKET ENABLE	Enables reception and storage of extension packets in 2 K x 8-bits per page when = 1
X24 POS	Automatic display of FASTEXT prompt row when = 1

R1 SYNC - auto increments to Register 2

T0, T1	Interlace/non-interlace 312/313 line or scan sync control
TCS ON	Text composite sync or direct sync select
VCR	Selects VCR mode for display PLL
DISABLE ODD/$\overline{\text{EVEN}}$	ODD/$\overline{\text{EVEN}}$ unconditionally forced low if = 1
AUTO ODD/$\overline{\text{EVEN}}$	If = 1 then ODD/$\overline{\text{EVEN}}$ output only active when no picture is present
FREE RUN PLL	Forces display PLL to free run at 6 MHz when = 1
VCS TO SCS	Connects VCS from video sync separator to display field sync detector to enable stable display status messages with 60 Hz rasters

R2 ACQ. CONTROL - auto increments to Register 3

START COLUMN	Start column for page request data
TB	Must be logic 0 for normal operation
ACQ. CCT	Selects one of five acquisition circuits
ACQ. $\overline{\text{ON}}$/OFF	Entire acquisition function turned off when = 1

R3 PAGE REQUEST DATA - does not auto increment

Table 6 shows the full register map for page requests. The mapping of Register 3 is dependent on the start column indicated in Register 2.

Table 6 Register map for page requests (R3)

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	$\overline{\text{CLEAR}}$ $\overline{\text{RX}}$	$\overline{\text{ROLL}}$	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0
7	CH4	CH3	CH2	CH1	CH0

Notes to Table 6

1. When the DO CARE bit is set to logic 1, this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0, the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
2. There are five versions of Table 6, one for each acquisition channel. This allows five simultaneous page requests.
3. $\overline{\text{ROLL}}$ set low to give rolling headers on page search.
4. $\overline{\text{CLEAR}}$ $\overline{\text{RX}}$ set low to clear old page on first reception.
5. Columns auto-increment on successive I²C-bus transmission bytes. Column 7 auto increments back to Column 0.
6. CH0 to CH4 are pointer bits (LSB to MSB) giving the current chapter address for that acquisition channel.

Where:

Page number

MAG	magazine
PU	page units
PT	page tens
$\overline{\text{HOLD}}$	set LOW to hold and not update page
CH	chapter address bit

Page sub-code

MU	minutes units
MT	minutes tens
HU	hours units
HT	hours tens.

R4 ACQ. MODE A - auto increments to Register 5

R5 ACQ. MODE B - auto increments to Register 6

These bits determine the type of acquisition to be performed by each of the five acquisition channels. H is Hamming and S is select. The four combinations are shown in Table 7.

Table 7 Truth table for acquisition Modes A and B

H	S	FUNCTION
0	0	7-bit plus parity
0	1	8-bit (no error checking)
1	0	8/4 Hamming checking over the full page
1	1	mixed 8/4 Hamming (Columns 0 to 7, 20 to 27) and 7-bit plus parity (Columns 8 to 9, 28 to 39)

R6 NORMAL DISPLAY CHAPTER - auto increments to Register 7

A0 to A4 Selects one of 32 chapters for display. This register is used for full pages of display, when the current display row bit is set to 0

R7 SUPPLEMENTARY DISPLAY CHAPTER - auto increments to Register 8

A0 to A4 Selects one of 32 chapters for display This register is used when the current display row bit is set to 1, for e.g. status messages on a text page

CLUT SELECT Determines which CLUT will be written to by Registers 11 and 12. If set to 1, access is to the supplementary display chapter colour entries

R8 NORMAL DISPLAY CONTROL - auto increments to Register 9

R9 NEWSFLASH/SUBTITLE DISPLAY CONTROL - auto increments to Register 10

PON Picture on

TEXT Text on

COR Contrast reduction on

BKGND Background colour on.

These functions have IN and OUT bits referring to inside and outside the boxing function respectively.

R10 DISPLAY CONTROL - does not auto increment

BOX ON 0	Boxing function allowed on Row 0
BOX ON 1-23	Boxing function allowed on Row 1-23
BOX ON 24	Boxing function allowed on Row 24
STATUS ROW $\overline{\text{BTM}}$/TOP	Row 24 displayed above or below the main text

R11 CLUT DATA 1 - auto increments to Register 12

R0 to R3	Red colour value
G0 to G3	Green colour value

R12 CLUT DATA 2 - auto increments to Register 11

B0 to B3	Blue colour value
A0 to A3	Address of colour entry

R13 ACTIVE CHAPTER - auto increments to Register 14

A0 to A4	Active chapter address for I²C-bus

CLEAR MEM.Clears the external memory to power-on state

R14 ACTIVE ROW - auto increments to Register 15

R0 to R4	Active row address for I²C-bus
INC BY ROW	When set the active address increments by row on R16A accesses instead of by column
CURSOR MOVE	When set the active I2C Row and columns are read and used to update the cursor position on the display

R15 ACTIVE COLUMN - auto increments to Register 16A/16B/16C depending on bits D6/7 of Register 15

C0 to C5	Active column address for I²C-bus
$\overline{\text{R16A}}$/R16B	Selects either Register 16A (read/write) or 16B (read only)
$\overline{\text{R16C}}$/R16C	Selects Register 16C (read only) or allows selection of Registers 16A or 16B

R16A ACTIVE DATA

D0 to D7 (R/W)	Data bits (read/write)

R16B DEVICE STATUS - does not auto increment

VCS SIGNAL QUALITY	Indicates that video signal quality is good and PLL is phase-locked to input video signal when = 1
TEXT SIGNAL QUALITY	If a good teletext signal is being received, then = 1
ROM VER R4-0	Indicates language/ROM variant. For Western European = 10000
$\overline{\text{625}}$/525 SYNC	If the input video is a 525 line signal then = 1

R16C END OF PAGE AND PACKET FLAGS - does not auto increment

AC0 to AC4	Set to 1 if an end of page has been detected in the corresponding acquisition channel
X/27 ARRIVED	Set to 1 if packet X27/0-1 and 4 arrives
X/29 ARRIVED	Set to 1 if packet X29/0-1 arrives
8/30 ARRIVED	Set to 1 if packet 8/30/0-3 arrives

Table 8 Crystal characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)					
C1	series capacitance	-	1.7	-	pF
C0	parallel capacitance	-	5.2	-	pF
CL	load capacitance	-	20	-	pF
Rr	resonant resistance	-	-	50	Ω
R1	series resistance	-	20	-	Ω
Xa	ageing	-	-	±5	10^{-6}/yr
Xj	adjustment tolerance	-	-	±25	10^{-6}
Xd	drift	-	-	±25	10^{-6}

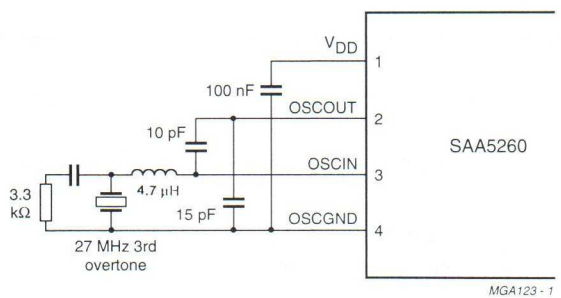


Fig.11 Crystal oscillator application diagram.

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional 2-pin design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone, as shown in Fig.11. The crystal characteristics are given in Table 8.

Character sets

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. For languages based on the Roman alphabet, the basic 96 character sets differ only in 13 national option characters. For the Western European version of SAA5260, these national option characters are shown in Table 9, with reference to their position in the basic character matrix illustrated in Table 10.

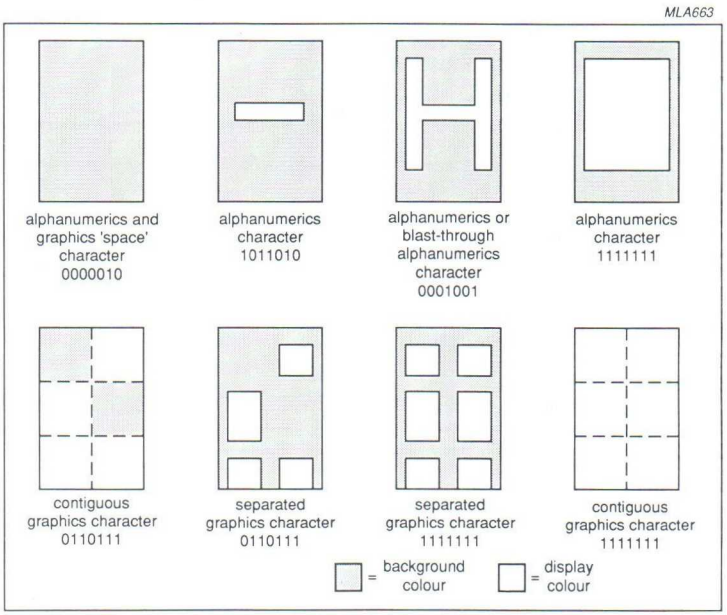


Fig.12 Character format.

Table 9 SAA5260P/E Western European national option character set

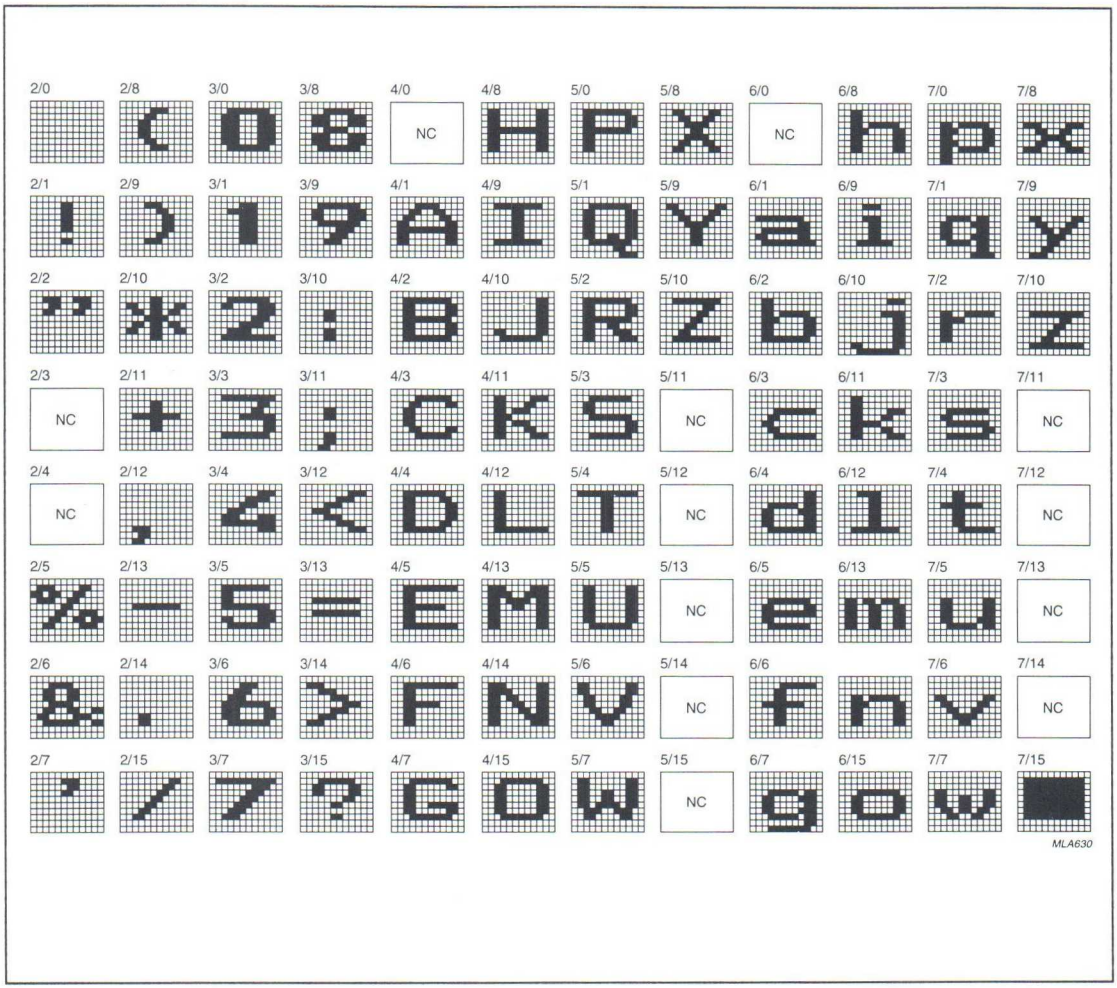
The SAA5260 automatically decodes transmission bits C12 to C14. Table 11 illustrates the 8-bit decoding of the character matrices.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MEA559

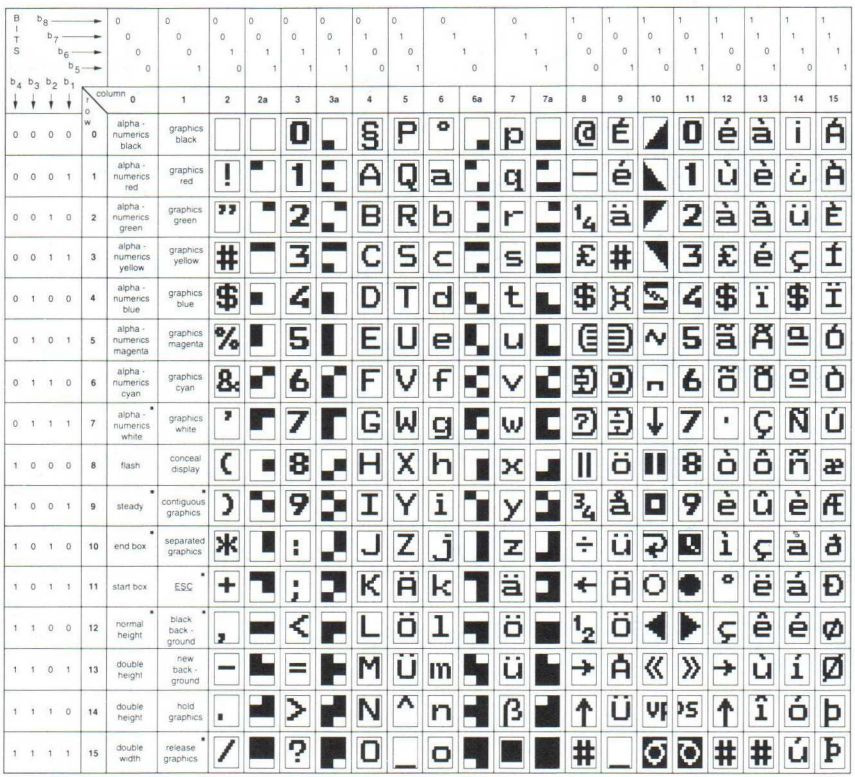
(1) PHCB are the Page Header Control Bits. Other combinations default to English.

Table 10 SAA5260 Western European basic character matrix



Where: NC = national option character position.

Table 11 SAA5260P/E character data input decoding (Western European Version)



For character version number (10000), see Register 16B.

* These control characters are presumed before each row begins.

Notes to Table 11

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Columns may be referred to by columns and row, for example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. The SAA5260 national option characters are illustrated in Table 9.
5. Character 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters for combining with character 8/5.
6. With bit 8 = 0, national characters will be decoded according to the setting of control bits C12 to C14 (see Table 9).
7. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.
8. Column 11 rows 0 to 7 are normally special attributes for setting the background colour. The numerals 0 to 7 are obtained instead when R0D3 is set to 1, to allow blast-through alphanumeric numbers in graphics mode.

Colour Facilities

Table 12 shows the format for both supplementary and normal page colour look-up tables (CLUTs). 12 bits are used for each colour entry. This allows the display colours to be chosen from a palette of 4096 different shades (16 levels possible on each of the R, G, B output pins from the internal DAC).

There are a total of 16 addresses in each CLUT, allowing each of the 8 foreground colour and 8 background colour values defined by the control characters to be assigned a particular shade, and separate colours to be assigned for normal and supplementary display pages.

On power-on, both CLUTs are cleared to full amplitude values corresponding to the R, G and B address inputs to give the normal 'level 1' display colours as shown in Table . They can then be re-defined by the microcomputer via the I²C-bus if required; registers R11 and R12 defining CLUT data and address, and R7D5 defining the CLUT to be used. R7D5 = 0 selects the CLUT for the normal page, while R7D5 = 1 selects the CLUT for the supplementary display page.

CLUT addressing and defaults

ADDRESS		MEANING	DEFAULT VALUE		
binary	decimal		R	G	B
0 0 0 0	0	BLACK background	0000	0000	0000
0 0 0 1	1	RED background	1111	0000	0000
0 0 1 0	2	GREEN background	0000	1111	0000
0 0 1 1	3	YELLOW background	1111	1111	0000
0 1 0 0	4	BLUE background	0000	0000	1111
0 1 0 1	5	MAGENTA background	1111	0000	1111
0 1 1 0	6	CYAN background	0000	1111	1111
0 1 1 1	7	WHITE background	1111	1111	1111
1 0 0 0	8	BLACK foreground	0000	0000	0000
1 0 0 1	9	RED foreground	1111	0000	0000
1 0 1 0	10	GREEN foreground	0000	1111	0000
1 0 1 1	11	YELLOW foreground	1111	1111	0000
1 1 0 0	12	BLUE foreground	0000	0000	1111
1 1 0 1	13	MAGENTA foreground	1111	0000	1111
1 1 1 0	14	CYAN foreground	0000	1111	1111
1 1 1 1	15	WHITE foreground	1111	1111	1111

Single chip teletext/VPS and line 23 decoder including 4/8 page memory

SAA5280

FEATURES

- Hardware compatible with SAA5246 and SAA5248
- Software compatible with SAA5248 and most applications of SAA5246
- Built-in 8 K memory for 4/8 page storage
- Meshing display within boxes
- Cursor decoupling from I²C-bus
- Automatic display of Packet X/24 from extension memory
- Separate data checking algorithms and points for each acquisition channel
- 24 : 18 Hamming checking
- Automatic Packet X/26 extension character processing
- VPS and Line 23 decoding and storage

GENERAL DESCRIPTION

The SAA5280 is hardware compatible with the SAA5246 and SAA5248 devices and may be used with existing boards and software. It contains 8K8 of on-chip memory allowing the device to be used as a single-chip teletext receiver. It also contains additional features (see features).

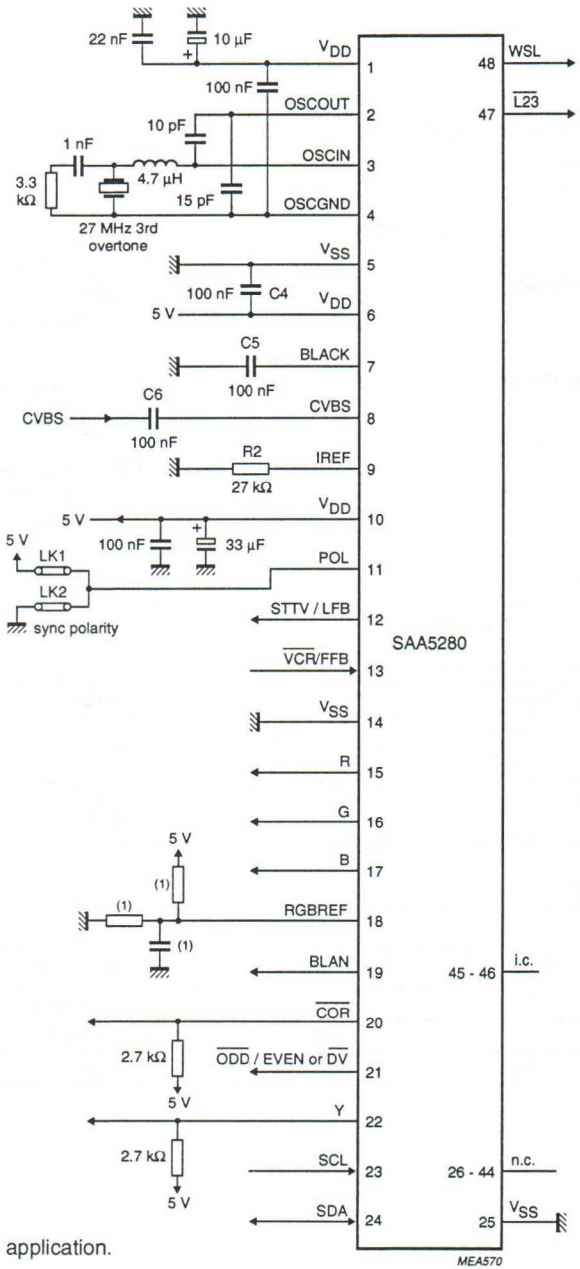
On power-up all new features remain transparent and no functional difference will be observed. To maintain software compatibility, the existing register map has been modified to include the extra device functions. These new features are controlled from two new registers, R12 and R12B.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5	5.5	V
I_{DD}	supply current	–	75	150	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1	1.4	V
f_{xtal}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature	–20	–	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5280P/E	48	DIL	plastic	SOT240
SAA5280ZP/E	52	SDIL	plastic	SOT247
SAA5280GP/E	64	QFP	plastic	SOT208



(1) Value dependent upon application.

Fig.1 Application diagram.

PINNING

SYMBOL	PIN			DESCRIPTION
	SOT240	SOT247	SOT208	
OSCOUT	2	1	27	27 MHz crystal oscillator output
OSCIN	3	2	28	27 MHz crystal oscillator input
OSCGND	4	3	29	0 V crystal oscillator ground
V_{SS}	5, 14, 25	4, 5, 15, 26	30, 31, 43, 58, 26	0 V ground
n.c.	–	7	–	not connected
BLACK	7	8	35	video black level storage pin, connected to analog ground via a 27 kΩ resistor
CVBS	8	9	36	composite video input pin. A positive-going 1 V (peak-to-peak) input is required; connected via 100 nF capacitor
IREF	9	10	37	reference current input pin; connected to analog ground via a 27 kΩ resistor
V_{DD}	1, 10, 6	6, 11, 52	32, 38, 25	+5 V supply
POL	11	12	39	STTV/LFB/FFB polarity selection pin
STTV/LFB	12	13	40	sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode)
$\overline{VCR}$/FFB	13	14	42	PLL time constant switch/field input pin. Function controlled by an internal register bit (scan sync mode)
R	15	16	44	dot rate character output of the RED colour information
G	16	17	45	dot rate character output of the GREEN colour information
B	17	18	47	dot rate character output of the BLUE colour information
RGBREF	18	19	48	input DC voltage to define the output high level on the RGB pins
BLAN	19	20	52	dot rate fast blanking output
$\overline{COR}$	20	21	53	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open drain output
$\overline{ODD}$/EVEN or $\overline{DV}$	21	22	54	in $\overline{ODD}$/EVEN mode a 25 Hz output synchronized to the input CVBS field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents. In $\overline{DV}$ mode a VPT data valid signal used to indicate reception of error-free VPS or 8/30/format 2 data
Y	22	23	55	dot rate character output of teletext foreground colour information. Open drain output
SCL	23	24	56	serial clock input for I²C-bus. It can still be driven HIGH during device power-down
SDA	24	25	57	serial data port for the I²C-bus. Open drain output. It can still be driven HIGH during device power-down

SYMBOL	PIN			DESCRIPTION
	SOT240	SOT247	SOT208	
SDA	24	25	57	serial data port for the I²C-bus. Open drain output. It can still be driven HIGH during device power-down
n.c.	26-44	27-47	1-20, 34, 41, 46, 49-51	not connected
i.c.	45, 46	48, 49	21, 22	internally connected; normally connected to ground
WSL	48	51	24	Line 23 decoder output "wide screen letterbox"
$\overline{L23}$	47	50	23	interrupt on detection of Line 23 signalling bits "wide screen"

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

REGISTER MAP

SAA5280 mode registers R0 to R12B are shown below. R0 to R10 and R12 are WRITE only; R11 is READ/WRITE.

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Adv. control	0	X24 POS	FREE RUN PLL	AUTO $\overline{\text{ODD}}$/ EVEN	DISABLE HDR ROLL	$\overline{\text{R12}}$/R12B	DISABLE $\overline{\text{ODD}}$/ EVEN	VCR MODE	$\overline{\text{R11}}$/R11B
Mode	1	VCS TO SCS	$\overline{7+P}$/ 8-BIT	ACQ $\overline{\text{ON}}$/OFF	EXT. PACKET ENABLE	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0
Page request address	2	HAM. CHECK 27, 28, 8/30	BANK SELECT A2	ACQ CIRCUIT A1	ACQ CIRCUIT A0	MESH $\overline{\text{OFF}}$/ON	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
Display chapter	4	–	–	–	–	–	A2	A1	A0
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS TOP	CURSOR ON	REVEAL ON	BOTTOM HALF	DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
Active chapter	8	–	–	–	VPS ENABLE	CLEAR MEM.	A2	A1	A0
Cursor row	9	–	–	–	R4	R3	R2	R1	R0
Cursor column	10	–	–	C5	C4	C3	C2	C1	C0
Cursor data	11	D7	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{\text{625}}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	DATA QUALITY	VCS SIGNAL QUALITY
Advanced Control 2A	12	H3	H2	H1	H0	S3	S2	S1	S0
Advanced Control 2B	12B	–	WSL LEVEL	WSL OVERRIDE	L23 ENABLE	VPS ENABLE	HAM CHECK X/26	PROCESS PK X/26	DISPLAY PK X26

Integrated Video input processor and Teletext decoder (IVT1.8*)

SAA5281

FEATURES

- Complete Teletext and VPS decoding in a single package
- Built-in 8K × 8 memory for up to 8 page storage
- Enhanced mode allows 7 Fastext pages and 8 pages of TOP to be captured
- Ability to request only subtitle pages
- Acquisition and decoding of VPS data
- Data valid output available to indicate reception of error-free VPS or packet 8/30/2 data
- Software and hardware compatible with SAA5246 and SAA5248
- Meshing display within boxes
- Separate data checking algorithms and pointers for each acquisition channel
- 24 : 18 Hamming checker
- Automatic packet 26 extension character processing
- Indication of Line 23 for external use
- 13.5 MHz clock output to drive external microcontroller
- Detection of Spanish transmissions to disable flicker-stopper
- Compatible with Philips' one-chip TV IC (TDA836X) for scan-locking applications.

DESCRIPTION

The IVT1.8* is a single-chip Teletext decoder IC for decoding 625-line based World System Teletext transmissions. The device is based on IVT1.0VPS and has reception facilities for the 5 MHz biphase VPS signal. It is intended for use in video recorders, in particular to implement the VPT facility (VCR programming via Teletext). With suitable software both VPT standards (EBU PDC System A and System B) can be accommodated to allow operation from any European VPT transmission. Automatic processing of packet 26 transmissions is also possible. No external memory is required as an 8K × 8 DRAM is included on-chip for up to 8 page storage. An enhanced mode allows 7 Fastext pages to be stored, with one chapter used to store extension packets.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	75	150	mA
V_{sync}	sync voltage amplitude	0.1	0.3	0.6	V
$V_{vid(p-p)}$	video input voltage amplitude (peak-to-peak value)	0.7	1.0	1.4	V
f_{xtal}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5281P	48	DIP48	plastic	SOT240-1
SAA5281ZP	52	SDIP52	plastic	SOT247-1

BLOCK DIAGRAM

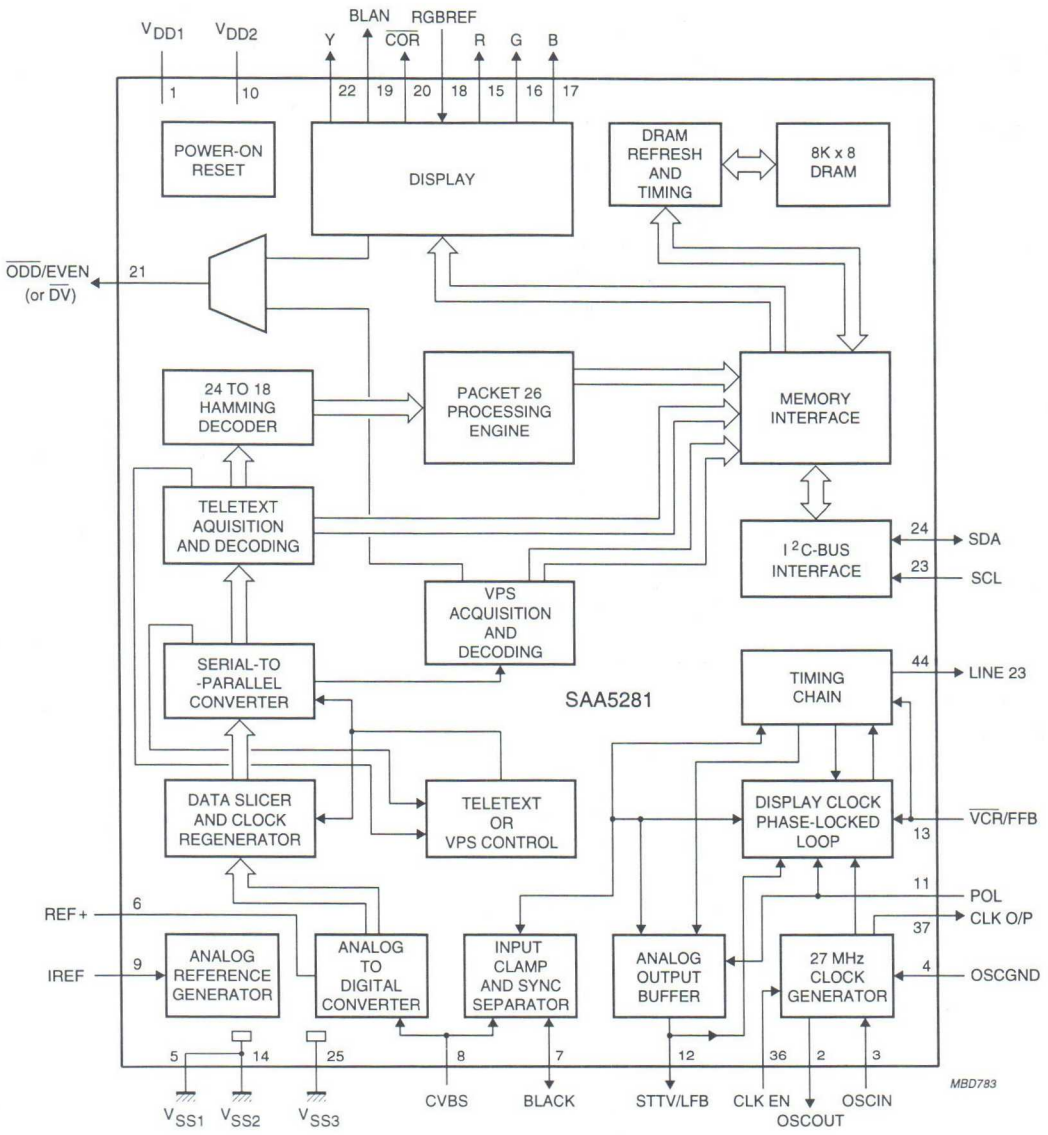


Fig.1 Block diagram; pin numbers for DIP48 (SOT240-1).

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT240-1	SOT247-1	
V_{DD1}	1	52	+5 V supply 1.
OSCOUT	2	1	27 MHz crystal oscillator output.
OSCIN	3	2	27 MHz crystal oscillator input.
OSCGND	4	3	0 V crystal oscillator ground.
V_{SS1}	5	4, 5	0 V ground.
REF+	6	6	Positive reference voltage for ADC. This pin should be connected to ground via a 100 nF capacitor.
BLACK	7	8	Video black level storage input/output. This pin should be connected to ground via a 100 nF capacitor.
CVBS	8	9	Composite video input. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor.
IREF	9	10	Reference current input, connected to ground via a 27 kΩ resistor.
V_{DD2}	10	11	+5 V supply 2.
POL	11	12	STTV/LFB/FFB polarity selection input.
STTV/LFB	12	13	Sync to TV output line flyback input. Function controlled by an internal register bit (scan sync mode).
$\overline{VCR}$/FFB	13	14	PLL time constant switch/field input. Function controlled by an internal register bit (scan sync mode).
V_{SS2}	14	15	0 V ground; connected to V_{SS1} for normal operation.
R	15	16	Dot rate character output of the RED colour information.
G	16	17	Dot rate character output of the GREEN colour information.
B	17	18	Dot rate character output of the BLUE colour information.
RGBREF	18	19	Input DC voltage to define the output high level on the RGB pins.
BLAN	19	20	Dot rate fast blanking output.
$\overline{COR}$	20	21	Programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open-drain output.
$\overline{ODD}$/EVEN (or $\overline{DV}$)	21	22	In $\overline{ODD}$/EVEN mode a 25 Hz output synchronized with the CVBS input field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents. In $\overline{DV}$ mode a VPT data valid signal is used to indicate reception of error-free VPS or 8/30 format 2 data.
Y	22	23	Dot rate character output of teletext foreground colour information. Open-drain output.
SCL	23	24	Serial clock input for I²C-bus. It can still be driven HIGH during power-down of the device.
SDA	24	25	Serial data port for the I²C-bus. Open-drain output. It can still be driven HIGH during power-down of the device.
V_{SS3}	25	26	0 V ground.
i.c.	26 to 35, 38 to 43, 45 to 48	27 to 32, 35 to 38, 41 to 46, 48 to 51	Internally connected. Normally open-circuit.

SYMBOL	PIN		DESCRIPTION
	SOT240-1	SOT247-1	
CLK EN	36	39	Clock enable input to enable the clock output (CLP O/P; pin 37). Internal pull-down normally disables clock.
CLK O/P	37	40	13.5 MHz clock output to drive an external microcontroller.
LINE 23	44	47	Output for indication of Line 23 for use with external circuitry.
n.c.	–	7, 33, 34	Not connected. Normally open-circuit.

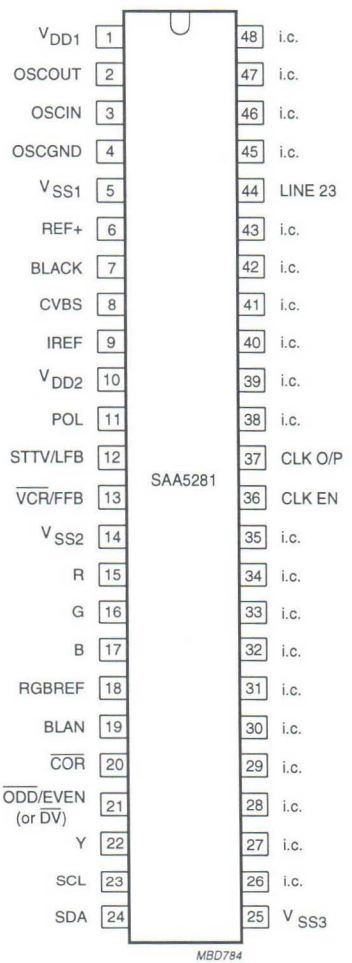


Fig.2 Pin configuration; SOT240-1 (DIP48).

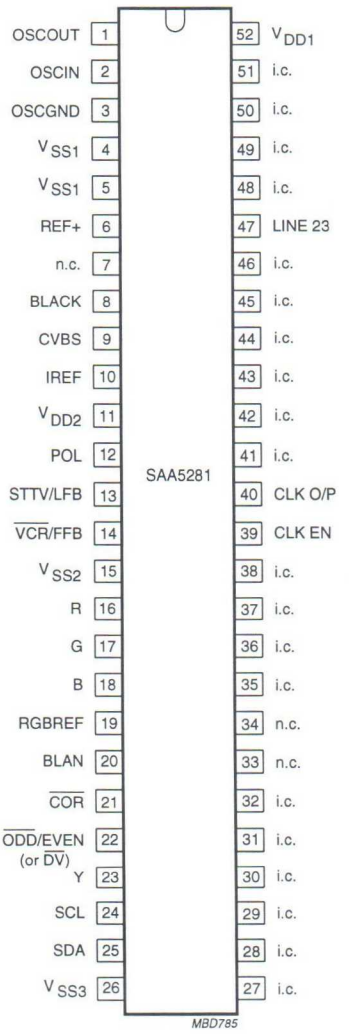


Fig.3 Pin configuration; SOT247-1 (SDIP52).

QUALITY AND RELIABILITY

This device will meet Philips Semiconductors General Quality Specification for Business group *"Consumer Integrated Circuits SNW-FQ-611-Part E"*. The principal requirements are shown in Tables 1 to 4.

Group A

Table 1 Acceptance tests per lot.

TEST	REQUIREMENTS(1)
Mechanical	cumulative target: <100 ppm
Electrical	cumulative target: <100 ppm

Group B

Table 2 Processability tests (by package family).

TEST	REQUIREMENTS(1)
Solderability	<7% LTPD
Mechanical	<15% LTPD
Solder heat resistance	<15% LTPD

Group C

Table 3 Reliability tests (by process family).

TEST	CONDITIONS	REQUIREMENTS(1)
Operational life	168 hours at T_j = 150 °C	<1500 FPM; equivalent to <100 FITS at T_j = 70 °C
Humidity life	temperature, humidity, bias 1000 hours, 85 °C, 85% RH (or equivalent test)	<2000 FPM
Temperature cycling performance	$T_{stg(min)}$ to $T_{stg(max)}$	<2000 FPM

Table 4 Reliability tests (by device type).

TEST	CONDITIONS	REQUIREMENTS(1)
ESD and latch-up	ESD Human body model 2000 V, 100 pF, 1.5 kΩ	<15% LTPD
	ESD Machine model 200 V, 200 pF, 0 Ω	<15% LTPD
	latch-up 100 mA, 1.5 × V_{DD} (absolute maximum)	<15% LTPD

Notes to Tables 1 to 4

1. ppm = fraction of defective devices, in parts per million.
   LTPD = Lot Tolerance Percent Defective.
   FPM = fraction of devices failing at test condition, in Failures Per Million.
   FITS = Failures In Time Standard.

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	−0.3	+6.5	V
V_I	input voltage (any input)	−0.3	V_{DD} + 0.5	V
V_O	output voltage (any output)	−0.3	V_{DD} + 0.5	V
I_O	output current (each output)	–	±10	mA
I_{IOK}	DC input or output diode current	–	±20	mA
T_{amb}	operating ambient temperature	−20	+70	°C

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −20 to +70 °C; pin numbers refer DIP48 package; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DDtot}	total supply current		–	75	150	mA
Inputs						
CVBS						
V_{sync}	sync voltage amplitude		0.1	0.3	0.6	V
$V_{burst(p-p)}$	colour burst amplitude (peak-to-peak value)		0.0	0.3	4.0	V
$t_{d(sync)}$	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		−150	0	+150	ns
$\Delta t_{d(sync)}$	change in sync delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{vid(p-p)}$	video input voltage amplitude (peak-to-peak value)		0.7	1.0	1.4	V
$V_{dat(text)}$	teletext data voltage amplitude		0.29	0.46	0.71	V
$\Delta f/f$	display PLL capture range		±7	–	–	%
Z_{source}	source impedance		–	–	250	Ω
V_I	input switching voltage level of sync separator		1.7	2.0	2.3	V
Z_I	input impedance		2.5	5.0	–	kΩ
C_I	input capacitance		–	–	10	pF
IREF						
R_{gnd}	resistor to ground		–	27	–	kΩ
V_i	input voltage		–	$0.5V_{DD}$	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
POL						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
LFB						
V_{IL}	LOW level input voltage		−0.3	–	tbf	V
V_{IH}	HIGH level input voltage		tbf	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_{Imax}	maximum input current	note 1	−1	–	+1	mA
t_{dLFB}	delay between LFB front edge and input video line sync		–	250	–	ns
$\overline{VCR}$/FFB						
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
I_{Imax}	maximum input current	note 1	−1	–	+1	mA
RGBREF						
V_{IL}	LOW level input voltage		−0.3	–	V_{DD}	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
SCL						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
f_{clk}	clock frequency		0	–	100	kHz
t_r	input rise time	between 10% and 90%	–	–	2	µs
t_f	input fall time	between 90% and 10%	–	–	2	µs
Inputs/outputs						
CRYSTAL OSCILLATOR (OSCIN; OSCOUT)						
$V_{osc(p-p)}$	oscillator voltage amplitude (peak-to-peak value)		–	1.0	–	V
G_v	small signal voltage gain		–	1.0	–	
G_m	mutual conductance		5.0	–	–	mS
C_I	input capacitance		–	–	10	pF
C_{fb}	feedback capacitance		–	1	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BLACK						
C_{black}	storage capacitor to ground		–	100	–	nF
V_{black}	black level voltage for nominal sync amplitude		1.8	2.15	2.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
SDA (OPEN-DRAIN INPUT/OUTPUT)						
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD} + 0.5	V
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	400	pF
t_r	input rise time	between 10% and 90%	–	–	2	µs
t_f	input fall time	between 90% and 10%	–	–	2	µs
t_f	output fall time	between 3 V and 1 V	–	–	200	ns
Outputs						
STTV						
G_{sttv}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{tcs}	TCS voltage amplitude		0.2	0.3	0.45	V
ΔV_{tcs}	DC shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive current		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
R, G AND B						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = –1.6 mA; $V_{RGBREF} < V_{DD} - 2$ V; note 2	V_{RGBREF} – 0.25	V_{RGBREF}	V_{RGBREF} + 0.5	V
$\|Z_o\|$	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
t_r	output rise time	between 10% and 90%	–	–	20	ns
t_f	output fall time	between 90% and 10%	–	–	20	ns
BLAN						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = – 0.2 mA	1.1	–	–	V
		I_{OH} = 0 mA	–	–	2.8	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	between 10% and 90%	–	–	20	ns
t_f	output fall time	between 90% and 10%	–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\overline{ODD}/EVEN$ OR $\overline{DV}$						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −1.6 mA	V_{DD} − 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	between 0.6 V and 2.2 V	–	–	50	ns
t_f	output fall time	between 0.6 V and 2.2 V	–	–	50	ns
$\overline{COR}$ AND Y (OPEN-DRAIN OUTPUTS)						
V_{OH}	HIGH level pull-up output voltage		–	–	V_{DD}	V
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.4	V
		I_{OL} = 5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} − 0.5 V and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
t_{skew}	skew delay between display outputs R, G, B, $\overline{COR}$, Y and BLAN		–	–	20	ns
I²C-bus timing (see Fig.4)						
t_{LOW}	SCL clock LOW time		4.0	–	–	µs
t_{HIGH}	SCL clock HIGH time		4.0	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4.0	–	–	µs
t_{BUF}	START set-up time following a STOP		4.0	–	–	µs
$t_{HD;STA}$	START hold time		4.0	–	–	µs
$t_{SU;STA}$	START set-up time following a clock LOW-to-HIGH transition		4.0	–	–	µs

Notes

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ±1 mA.
2. Voltage level V_{OH} for R, G and B outputs is taken to be the mean value during the output HIGH time. If higher R, G and B voltage V_{OH} levels are required RGBREF voltage level may be raised and a pull-up resistor used at each of these pins provided current specification (I_{OL}) is not exceeded.

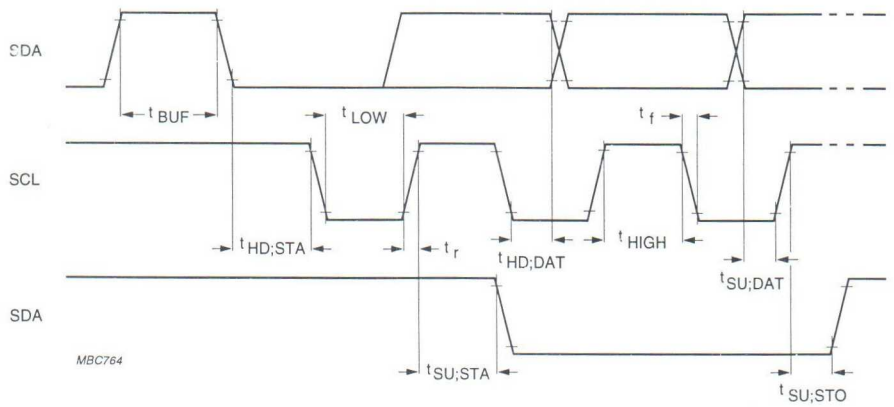
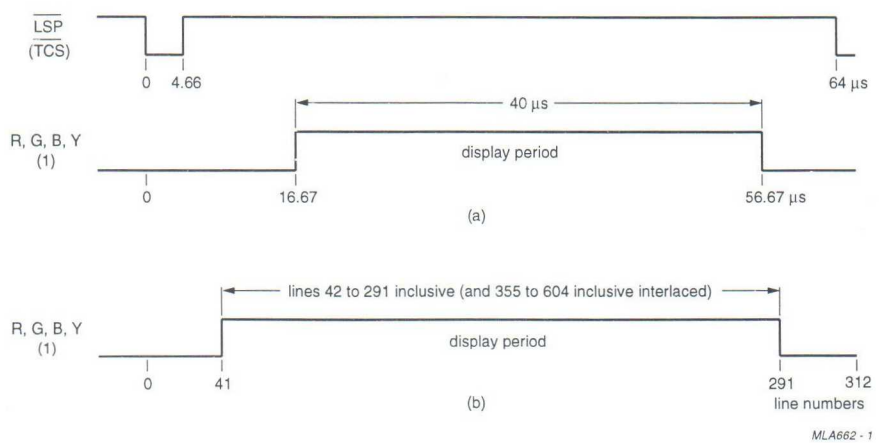


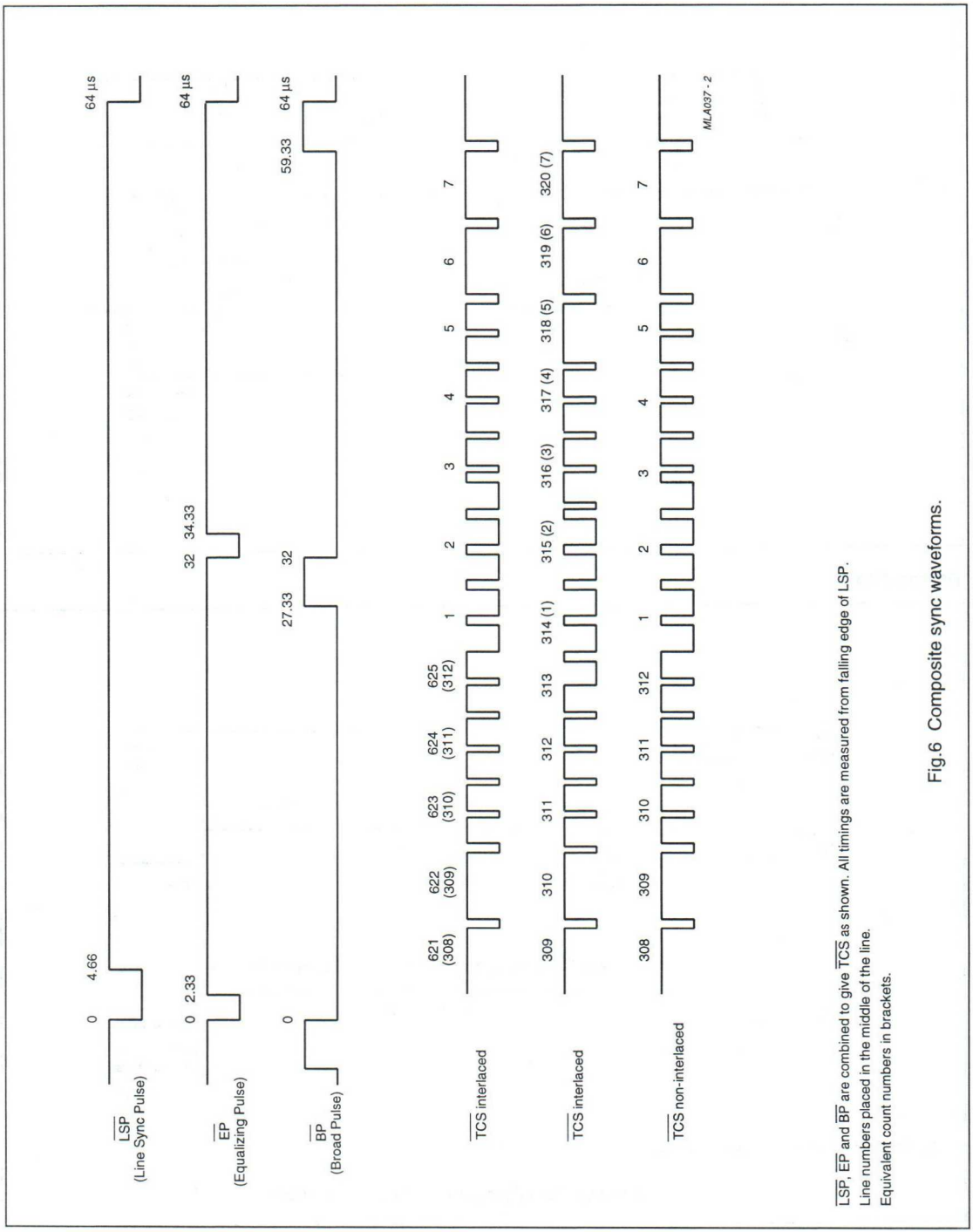
Fig.4 I²C-bus timing.

TIMING CHAIN



(1) Also BLAN in character and box blanking.

Fig.5 Display output timing (a) line rate (b) field rate.



LSP, EP and BP are combined to give TCS as shown. All timings are measured from falling edge of LSP.
Line numbers placed in the middle of the line.
Equivalent count numbers in brackets.

Fig.6 Composite sync waveforms.

Line numbers placed in the middle of the line.
Equivalent count numbers in brackets.
(1) Or 62 µs if Register 1 D2.D1.D0 equals 1 1 1.

Fig.7 $\overline{\text{ODD}}$/EVEN timing.

ON-CHIP MEMORY

Page memory organization

The organization of the page memory is illustrated by Fig.8. The IVT1.8* provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; row 24 is the extra row available for software generated status messages and FLOF/FASTEXT prompt information.

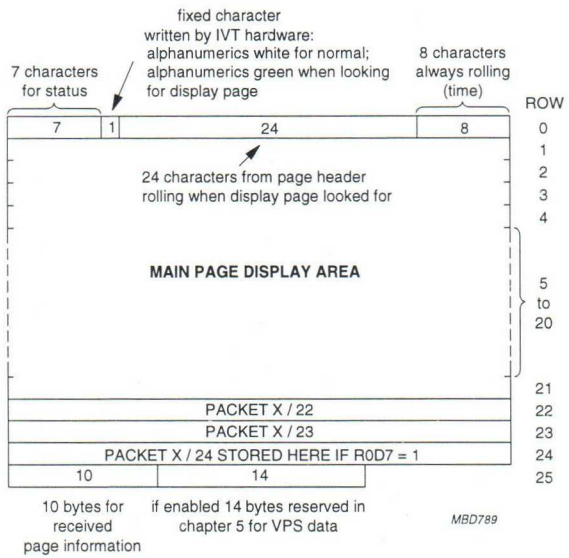


Fig.8 Basic page memory organization.

REMARK TO FIG.8

Row 0

Row 0 is for the page header. The first seven characters (0 to 6) are free for status messages. Character 8 is an alphanumeric white or green control character, written automatically by IVT1.8* to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page as shown in Table 5. The remaining 14 bytes are free for use by the microcomputer.

Table 5 Row 25 received control data format.

ROW 25										
D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Table 6 Page number and sub-code for Table 5.

BIT NAME	DESCRIPTION
Page number	
MAG	magazine
PU	page units
PT	page tens
PBLF	page being looked for
$\overline{\text{FOUND}}$	LOW for page has been found
HAM.ER	Hamming error in corresponding byte
Page sub-code	
MU	minutes units
MT	minutes tens
HU	hours units
HT	hours tens
C4 to C14	transmitted control bits

Extension packet memory organization

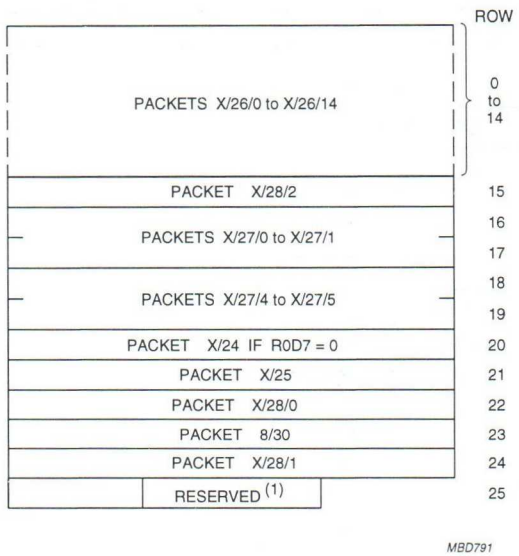
When in normal extension packet enabled mode the rows of information are organized as illustrated in Fig.9.

Row 23 of the extension page, as shown in Fig.9, contains packet 8/30. Packet 8/30 is mapped into the IVT1.8* memory as follows:

8/30/0 and 8/30/1 to Chapter 4 Row 23

8/30/2 and 8/30/3 to Chapter 5 Row 23

8/30/4 to 8/30/15 to Chapter 6 Row 23.



(1) Row 25 reserved for VPS data in Chapter 5.

Fig.9 Organization of the extension memory.

ENHANCED MODE

In enhanced mode, the number of extension packets captured is reduced to the minimum required for FASTEXT operation. The first seven chapters can then be used for storage, using the system of pointers. The arrangement of extension packets is shown in Fig.10.

When in enhanced mode and extension packets are disabled, normal 8-page mode is in operation, but the X/26 engine is enabled (unlike normal 8-page mode).

	ROW
CHAPTER 0 PACKET 24	0
CHAPTER 0 PACKETS 27 / 0	1
CHAPTER 1 PACKET 24	2
CHAPTER 1 PACKETS 27 / 0	3
CHAPTER 2 PACKET 24	4
CHAPTER 2 PACKETS 27 / 0	5
CHAPTER 3 PACKET 24	6
CHAPTER 3 PACKETS 27 / 0	7
CHAPTER 4 PACKET 24	8
CHAPTER 4 PACKETS 27 / 0	9
CHAPTER 5 PACKET 24	10
CHAPTER 5 PACKETS 27 / 0	11
CHAPTER 6 PACKET 24	12
CHAPTER 6 PACKETS 27 / 0	13
not used	14
not used	15
PACKETS 8 / 30 / 0,1	16
PACKETS 8 / 30 / 2,3	17
PACKETS 8 / 30 / 4 to 15	18
not used	19 to 24

MBD788

Fig.10 Organization of the extension memory in enhanced mode.

VPT data memory organization

To simplify the software for dual-standard VPT decoders, the VPS data from line 16 is stored in row 25 of Chapter 5 of the page memory, and is aligned to match the packet 8/30 format 2 data as far as possible. The 8/30 format 2 packet is Hamming coded and by setting the appropriate register control bit the data is stored after hardware Hamming correction. There are 4 data bits stored in each column address of memory with an additional Hamming error bit. The data equivalent to the VPS signal is found in columns 12 to 19.

Although the VPS data is not Hamming protected, it is stored with 4 data bits per column address in the same way with an additional biphase error bit. The extra space in Row 25 is allocated to two more Line 16 words. They are Word 15 (reserved) and Word 4 (Program Source Identification, ASCII sequential) which may be useful for future applications. Details of the memory organization are shown in Fig.11.

The stored data can be read from memory via the I²C-bus in the normal way. Multiple reception/majority error correction of the VPS data is the responsibility of the control software, the device simply stores the data as transmitted after biphase decoding.

As both VPS and 8/30/2 signals are stored in separate memory locations, it is possible to deal with future situations where both System A and System B transmissions may be present on the same TV channel, the defaults and level of service chosen by the control software.

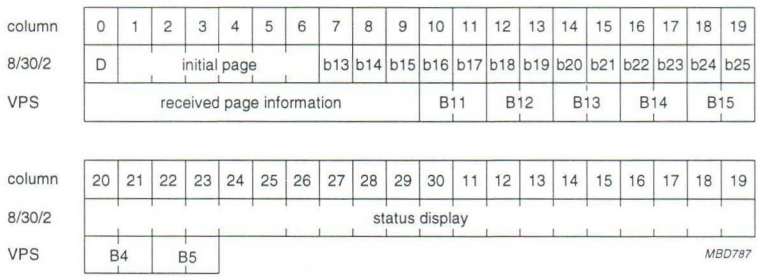


Fig.11 Detailed memory organization.

Register maps

IVT1.8* mode registers R0 to R13 are shown in Table 7. R0 to R10, R12 and R13 are WRITE only; R11 is READ/WRITE, R11B is read only. Register map (R3), for page requests, is shown in detail in Table 11.

Table 7 Register map (notes 1 to 4).

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
NAME	No.								
Advanced control	0	X/24 POS	FREE RUN PLL	AUTO $\overline{\text{ODD}}$/EVEN	DISABLE HDR ROLL	CBB SLAVE SYNC	DISABLE $\overline{\text{ODD}}$/EVEN	VCR MODE	$\overline{\text{R11}}$/R11B SELECT
Mode	1	VCS TO SCS	$\overline{7+P}$/ 8-BIT	ACQ $\overline{\text{ON}}$/OFF	EXT PKT ENABLE	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0
Page request address	2	HAM CHECK 27, 8/30	BANK SELECT A2	ACQ CCT A1	ACQ CCT A0	0	SC2	SC1	SC0
Page request data	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
Display chapter	4	–	–	–	–	FREEZE HEADER ONLY	A2	A1	A0
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS $\overline{\text{BTM}}$/TOP	CURSOR ON	$\overline{\text{CONCEAL}}$/ REVEAL ON	$\overline{\text{TOP}}$/BTM HALF	$\overline{\text{SINGLE}}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1 to 23	BOX ON 0
Active chapter	8	–	–	–	VPS ENABLE	CLEAR MEM	A2	A1	A0
Cursor row	9	–	–	–	R4	R3	R2	R1	R0
Cursor column	10	–	–	C5	C4	C3	C2	C1	C0
Cursor data	11	D7	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{\text{625}}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TEXT SIGNAL QUALITY	VCS SIGNAL QUALITY
Advanced control 2A	12	H3	H2	H1	H0	S3	S2	S1	S0
Advanced control 2B	13	ENHANC MODE	CURSOR FREEZE/ DEVICE IDENT	MESHING ENABLE	VPS ENABLE	POINTS ENABLE	HAM CHECK 24 : 18	DISABLE PKT X/26	AUTO DISPLAY PKT X/24

Notes to Table 7

1. The dash (–) indicates these bits are inactive and must be written to logic 0 for future compatibility.
2. Certain registers are auto-incremented following an I²C-bus transmission byte. These are Register R0 to R3, R4 to R7 and R8 to R12 or R13.
3. All bits in Registers R0 to R13 are cleared to logic 0 on power-up except bits D0 and D1 of Registers R1, R5 and R6 which are set to logic 1.
4. All memory is cleared to space (00100000) on power-up, except Row 0 Column 7 Chapter 0, which is alpha white (00000111) as the acquisition circuit is enabled but all pages are on hold.

Table 8 Register description.

REGISTER BIT D0 TO D7	FUNCTION
R0 AVANCED CONTROL - auto-increments to Register 1	
$\overline{\text{R11}}$/R11B SELECT	Selects reading of R11 if LOW or R11B if HIGH.
VCR MODE	If logic 1 selects short time constant mode of PLL.
DISABLE $\overline{\text{ODD}}$/EVEN	Forces $\overline{\text{ODD}}$/EVEN output LOW when logic 1 (see Table 9).
CBB SLAVE SYNC	When set will modify internal slave sync timing to allow connection to sandcastle of Philips one-chip TV IC (TDA8362).
DISABLE HDR ROLL	Stops the display update of rolling time and green rolling header during page requests when logic 1. Time updates on page reception only.
AUTO $\overline{\text{ODD}}$/EVEN	If logic 1 then $\overline{\text{ODD}}$/EVEN output only active when no TV picture displayed (see Table 9).
FREE RUN PLL	Will force the display PLL to free run at 6 MHz when logic 1.
X/24 POS	Automatic display of FASTEXT prompt row when logic 1. Will also cause Row 24 data transmitted by packet 26 to be written to display, rather than extension memory.
R1 MODE - auto-increments to Register 2	
T0, T1	Interlace/non-interlace 312/313 line control (see Table 10).
TCS ON	Text composite sync or direct sync select (see Table 10 for FFB mode selection).
$\overline{\text{DEW}}$/FULL FIELD	Field-flyback or full-channel mode.
EXT PKT ENABLE	Enables reception and storage of extension packets when logic 1.
ACQ $\overline{\text{ON}}$/OFF	Acquisition circuits turned off when logic 1.
$\overline{\text{7 + P}}$/8-BIT	7 bits with parity checking or 8-bit mode.
VCS TO SCS	Connects VCS from video sync separater to display field sync detector to enable stable display of 60 Hz status messages when logic 1.
R2 PAGE REQUEST ADDRESS - auto-increments to Register 3	
SC0 to SC2	Start column for page request data (see Table 11).
0	Must be logic 0 for normal operation.
ACQ CCT A0, A1	Selects one of four acquisition circuits.
BANK SELECT A2	Selects bank of four pages being addressed for acquisition.
HAM CHECK 27, 8/30	8/4 Hamming check packet 27 and 8/30 data.
R3 PAGE REQUEST DATA - does not auto-increment	
PRD0 to PRD4	See Table 11.

REGISTER BIT D0 TO D7	FUNCTION
R4 DISPLAY CHAPTER - auto-increments to Register 5	
A0 to A2	Selects one of 8 display chapters.
FREEZE HEADER ONLY	Freezes the rolling header, but (unlike R0D4) allows the time to roll.
R5 NORMAL DISPLAY CONTROL - auto-increments to Register 6	
R6 NEWSFLASH/SUBTITLE DISPLAY CONTROL - auto-increments to Register 7; note 1	
PON	Picture on.
TEXT	Text on.
COR	Contrast reduction on.
BKGND	Background colour on.
R7 DISPLAY MODE - does not auto-increment	
BOX ON 0	Boxing function allowed on Row 0.
BOX ON 1 to 23	Boxing function allowed on Rows1 to 23.
BOX ON 24	Boxing function allowed on Row 24.
$\overline{\text{SINGLE}}$/DOUBLE HEIGHT	To display double height text.
$\overline{\text{TOP}}$/BTM HALF	To select bottom half of page when DOUBLE HEIGHT is logic 1.
$\overline{\text{CONCEAL}}$/REVEAL ON	To reveal concealed text.
CURSOR ON	To display cursor.
STATUS $\overline{\text{BTM}}$/TOP	Row 25 displayed above or below the main text.
R8 ACTIVE CHAPTER - auto-increments to Register 9	
A0 to A2	Active chapter for data written to or read from memory via the I^2C-bus.
CLEAR MEM	When set to logic 1, clears the display memory. This bit is automatically reset.
VPS ENABLE	VPS acquisition enabled when logic 1.
R9 CURSOR ROW - auto-increments to Register 10	
R0 to R4	Active row for data written to or read from memory via the I^2C-bus.
R10 CURSOR COLUMN - auto-increments to Register 11 or 11B	
C0 to C5	Active column for data written to or read from memory via the I^2C-bus.
R11 CURSOR DATA - does not auto-increment	
D0 to D7	Data read from/written to memory via I^2C-bus, at location pointed to by R9 and R10. This location automatically increments each time R11 is accessed.
R11B DEVICE STATUS - does not auto-increment	
VCS SIGNAL QUALITY	Indicates that the video signal quality is good and PLL is phase-locked to input video when logic 1.
TEXT SIGNAL QUALITY	If a good teletext signal is being received then logic 1.
ROM VER R0 to R4	Indicated language/ROM variant. For Western European is logic 0. R3 and R4 are set HIGH if R13 D6 is logic 1.
$\overline{\text{625}}$/525 SYNC	If the input video is a 525 line signal then logic 1.
R12 ADVANCED CONTROL 2A - does not auto-increment	
S0 to S3, H0 to H3	Each acquisition channel can be programmed to process its page in one of four ways as shown in Table 12.

REGISTER BIT D0 TO D7	FUNCTION
R13 ADVANCED CONTROL 2B - does not auto-increment	
AUTO DISPLAY PKT X/24	Status row will show the contents of the row of the extension memory (packet 24) when logic 1.
DISABLE PKT X/26	Output taken from processing engine written to the display memory when logic 0. Operates independent of the acquisition.
HAM CHECK 24 : 18	When logic 1 all packet 26 data is stored in extension memory unchecked.
POINTS ENABLE	Enable for acquisition pointers when logic 1.
VPS ENABLE	VPS acquisition enabled when logic 1.
MESHING ENABLE	Enables meshing display function in box mode.
CURSOR FREEZE/ DEVICE IDENT	When logic 1, cursor position not updated even if active row and column change. This bit will also cause R3 and R4 of the ROM code in Register R11B to be set HIGH. This allows software to identify the device as an IVT1.8*. An internal '1.8 mode' flag is also set, which enables the operation of R0D4, R4D4 and the subtitle bit in R3.
ENHANC MODE	When logic 1, extension packet data is mapped into the last chapter. Only packet 24, 27/0 and 8/30 are stored. Chapters 0 to 6 can then be used for page storage. If extension packets are not enabled, 8 pages are stored as normal, but X/26 engine is enabled.

Note

1. These functions have IN and OUT referring to inside and outside the boxing function respectively.

Table 9 $\overline{\text{ODD}}$/EVEN selection.

AUTO $\overline{\text{ODD}}$/EVEN	DISABLE $\overline{\text{ODD}}$/EVEN	RESULT
0	0	$\overline{\text{ODD}}$/EVEN output continuous
0	1	$\overline{\text{ODD}}$/EVEN statically LOW
1	1	$\overline{\text{ODD}}$/EVEN active only when no TV picture displayed
1	1	$\overline{\text{DV}}$ output to indicate reception of error-free 8/30/format 2 packet or VPS line

Table 10 Interlace/non-interlace 312/313 line control and $\overline{\text{ODD}}$/EVEN field detection option.

TCS ON FFB MODE[2]	T1	T0	RESULT
X	0	0	interlaced 312.5/312.5 lines
X	0	1	non-interlaced 312/313 lines (note 1)
X	1	0	non-interlaced 312/313 lines (note 1)
0	1	1	SCS (scan composite sync) mode: FFB leading edge in first broad pulse of field
1	1	1	SCS (scan composite sync) mode: FFB leading edge in second broad pulse of field

Notes

1. Reverts to interlaced mode if a newsflash or subtitle is being displayed.
2. X = don't care.

Table 11 Register map for page requests (R3); notes 1 to 6.

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	DO CARE Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	DO CARE Page tens	PT3	PT2	PT1	PT0
2	DO CARE Page units	PU3	PU2	PU1	PU0
3	DO CARE Hours tens	SUBTITLE	X	HT1	HT0
4	DO CARE Hours units	HU3	HU2	HU1	HU0
5	DO CARE Minutes tens	X	MT2	MT1	MT0
6	DO CARE Minutes units	MU3	MU2	MU1	MU0
7	X	X	CH2	CH1	CH0

Notes

1. Abbreviations are as given in Table 6 except for DO CARE bits and CH = chapter address for acquisition chapter.
2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, normal or timed page selection.
3. If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
4. Columns auto-increment on successive I^2C-bus transmission bytes.
5. The SUBTITLE bit is only present when the device is in "1.8 mode" (i.e. R13D6 has been set HIGH).
6. X = don't care.

Table 12 Acquisition channel programming.

H0 to H3[1]	S0 to S3[1]	CHECKING ALGORITHM FOR ACQUISITION CHANNEL X
0	0	7-bit + parity for whole page
0	1	8-bit for whole page
1	0	8/4 Hamming check for whole page
1	1	mixed 8/4 Hamming (columns 0 to 7, 20 to 27) and 7-bit + parity (columns 8 to 19, 28 to 39)

Note

1. These register bits operate in conjunction with $\overline{7+P}$/ 8-BIT (Register 1, Bit D6) which will over-ride the choice of data checker if set, setting all channels to 8-bit only. If this bit is not set H0 to H3 and S0 to S3 will determine the data checking (default to 7-bit + parity).

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional Colpitts 3-pin design operating at 27 MHz. The oscillator is sinusoidal and linear, with a controlled output amplitude. This reduces the radiated and conducted level of the 27 MHz fundamental frequency, and reduces the power dissipation in the quartz crystal. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone as illustrated in Fig.12. The crystal characteristics are given in Table 13.

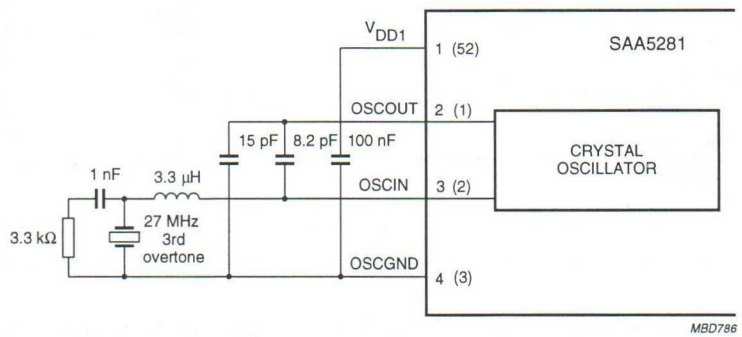


Fig.12 Crystal oscillator application diagram for SOT240-1; pins in parenthesis are for SOT247-1.

Table 13 Crystal characteristics (see Fig.12).

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)				
C1	series capacitance	1.7	–	pF
C0	parallel capacitance	5.2	–	pF
C_L	load capacitance	20	–	pF
R_r	resonance resistance	–	50	Ω
R1	series resistance	20	–	Ω
X_a	ageing	–	$\pm 5 \times 10^{-6}$	$year^{-1}$
X_j	adjustment tolerance	–	$\pm 25 \times 10^{-6}$	
X_d	drift	–	$\pm 25 \times 10^{-6}$	

CHARACTER SETS

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character sets differ only in 13 national option characters as indicated in the Tables 18, 19 and 20 with reference to their table position in the basic character matrix illustrated in Table 17. The IVT1.8* automatically decodes transmission bits C12 to C14. Tables 14, 15 and 16 illustrate the character matrixes.

Character bytes are listed as transmitted from b1 to b7.

Meshing

This is an alternative method of displaying teletext subtitles, or similar boxed text superimposed on the TV picture and operates by showing reduced contrast TV pictures in place of the (black) background within the boxed area. The Meshing effect is produced by toggling the BLAN signal from IVT at pixel rate. By starting at the same point each field, and toggling the start position each line, a chequered pattern will result. This allows movement to be seen behind the text information. The MESH $\overline{\text{OFF}}$/ON bit in Register 13 D5 controls this function. Normally at zero, compatibility with IVT1.0 is maintained.

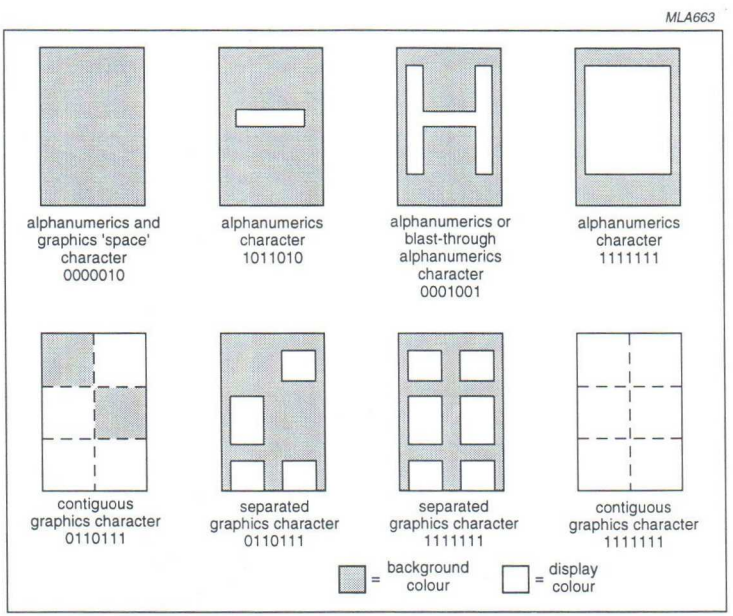


Fig.13 Character format.

Table 14 SAA5281P/E character data input decoding, West European languages; notes 1 to 9.
For character version number (11000) see Register 11B.

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0	0	0	1	1	1	1	1	1
b_7	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	1	1
b_6	0	0	1	1	1	1	0	0	1	1	1	0	0	1	1	0	0
b_5	0	1	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1

b_4 b_3 b_2 b_1	row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha - numerics black	graphics black			0		§	P	°		p		@	É	é	à	¡	Á
0 0 0 1	1	alpha - numerics red	graphics red	!		1		A	Q	a		q		—	é	ù	è	¿	À
0 0 1 0	2	alpha - numerics green	graphics green	"		2		B	R	b		r		¼	ä	à	â	ü	È
0 0 1 1	3	alpha - numerics yellow	graphics yellow	#		3		C	S	c		s		£	#	£	é	ç	Í
0 1 0 0	4	alpha - numerics blue	graphics blue	$		4		D	T	d		t		$	¤	$	ï	$	Ï
0 1 0 1	5	alpha - numerics magenta	graphics magenta	%		5		E	U	e		u		←	↔	ã	Ã	¤	Ó
0 1 1 0	6	alpha - numerics cyan	graphics cyan	&		6		F	V	f		v		→	↕	õ	Õ	º	Ô
0 1 1 1	7	alpha - numerics white [2]	graphics white	'		7		G	W	g		w		?	↑	·	Ç	Ñ	Ú
1 0 0 0	8	flash	conceal display	(		8		H	X	h		x		‖	ö	ò	ô	ñ	æ
1 0 0 1	9	steady [2]	contiguous graphics [2]	)		9		I	Y	i		y		¾	å	è	û	è	Æ
1 0 1 0	10	end box [2]	separated graphics	*		:		J	Z	j		z		÷	ü	ì	ç	à	ð
1 0 1 1	11	start box	ESC [1]	+		;		K	Ä	k		ä		←	Ä	°	ë	á	Ð
1 1 0 0	12	normal height [2]	black background [2]	,		<		L	Ö	l		ö		½	Ö	ç	ê	é	ø
1 1 0 1	13	double height	new background	-		=		M	Ü	m		ü		→	Å	→	ù	í	Ø
1 1 1 0	14	SO [1]	hold graphics	.		>		N	^	n		ß		↑	Ü	↑	î	ó	þ
1 1 1 1	15	SI [1]	release graphics [2]	/		?		O	_	o		■		#	_	#	#	ú	Þ

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Table 15 SAA5281P/H character data input decoding, East European languages; notes 1 to 9.
For character version number (11001) see Register 11B.

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7	0	0	0	0	0	0	1	1	1		1		0	0	1	1	1	1
b_6	0	0	1	1	1	1	0	0	1		1		0	0	1	1	1	1
b_5	0	1	0	0	1	1	0	1	0		1		0	1	0	1	0	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0 alpha - numerics black	graphics black																
0 0 0 1	1 alpha - numerics red	graphics red																
0 0 1 0	2 alpha - numerics green	graphics green																
0 0 1 1	3 alpha - numerics yellow	graphics yellow																
0 1 0 0	4 alpha - numerics blue	graphics blue																
0 1 0 1	5 alpha - numerics magenta	graphics magenta																
0 1 1 0	6 alpha - numerics cyan	graphics cyan																
0 1 1 1	7 alpha - numerics white (2)	graphics white																
1 0 0 0	8 flash	conceal display																
1 0 0 1	9 steady (2)	contiguous graphics (2)																
1 0 1 0	10 end box (2)	separated graphics																
1 0 1 1	11 start box	ESC (1)																
1 1 0 0	12 normal height (2)	black back - ground (2)																
1 1 0 1	13 double height	new back - ground																
1 1 1 0	14 SO (1)	hold graphics																
1 1 1 1	15 SI (1)	release graphics (2)																

MLA961

Table 16 SAA5281P/T character data input decoding, West European and Turkish languages; notes 1 to 9.
For character version number (11010) see Register 11B.

BITS b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	row \ column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
	0	0	0					0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
	0	0	1					0	0	0	0	0	0	1	1	1		1		0	0	0	0	1	1
	0	1	0					0	0	1	1	1	1	0	0	1		1		0	0	0	1	0	1
	0	1	1					0	1	0	1	1	1	0	1	0		1		0	1	0	0	0	1
0	0	0	0					0	alpha - numerics black	graphics black															
0	0	0	1					1	alpha - numerics red	graphics red															
0	0	1	0					2	alpha - numerics green	graphics green															
0	0	1	1					3	alpha - numerics yellow	graphics yellow															
0	1	0	0					4	alpha - numerics blue	graphics blue															
0	1	0	1					5	alpha - numerics magenta	graphics magenta															
0	1	1	0					6	alpha - numerics cyan	graphics cyan															
0	1	1	1					7	alpha - numerics white [2]	graphics white															
1	0	0	0					8	flash	conceal display															
1	0	0	1					9	steady [2]	contiguous graphics [2]															
1	0	1	0					10	end box [2]	separated graphics															
1	0	1	1					11	start box	ESC [1]															
1	1	0	0					12	normal height [2]	black back - ground [2]															
1	1	0	1					13	double height	new back - ground															
1	1	1	0					14	SO [1]	hold graphics															
1	1	1	1					15	SI [1]	release graphics [2]															

MBA431

Notes to Tables 14, 15 and 16

1. These control characters are reserved for compatibility with other data codes.
2. These control characters are presumed before each row begins.
3. Control characters shown in Columns 0 and 1 are normally displayed as spaces.
4. Characters may be referred to by column and row (for example 2/5 refers to %).
5. Black represents displayed colour. White represents background.
6. The SAA5281 national option characters are illustrated in Tables 18, 19 and 20.
7. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters for combining with character 8/5 (E, H and T codes only). Characters 5/12, 5/13, 5/14 and 5/15 are combined with 5/11 (S code only).
8. National option characters will be displayed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Tables 18, 19 and 20.
9. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.

Table 17 SAA5281 basic character matrix; note 1.

Note

1. Where NC = national option character position.

Table 18 SAA5281P/E national option character set.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MLB458

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

Table 19 SAA5281P/H national option character set.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
POLISH	0	0	0	#	ń	ą	Ż	Ś	Ł	ć	ó	ę	ż	ś	ł	ź
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
SERBO-CROAT	1	0	1	#	½	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECHOSLOVAKIA	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN	1	1	1	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

MLA966

(1) PHCB are the Page Header Control Bits. Other combinations default to German. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 17.

Table 20 SAA5281P/T national option character set.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
TURKISH	1	1	0	Ţ	ğ	İ	Ş	Ö	Ç	Ü	Ğ	ı	ş	ö	ç	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MBA430

(1) PHCB are the Page Header Control Bits. Other combinations default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 17.

APPLICATION INFORMATION

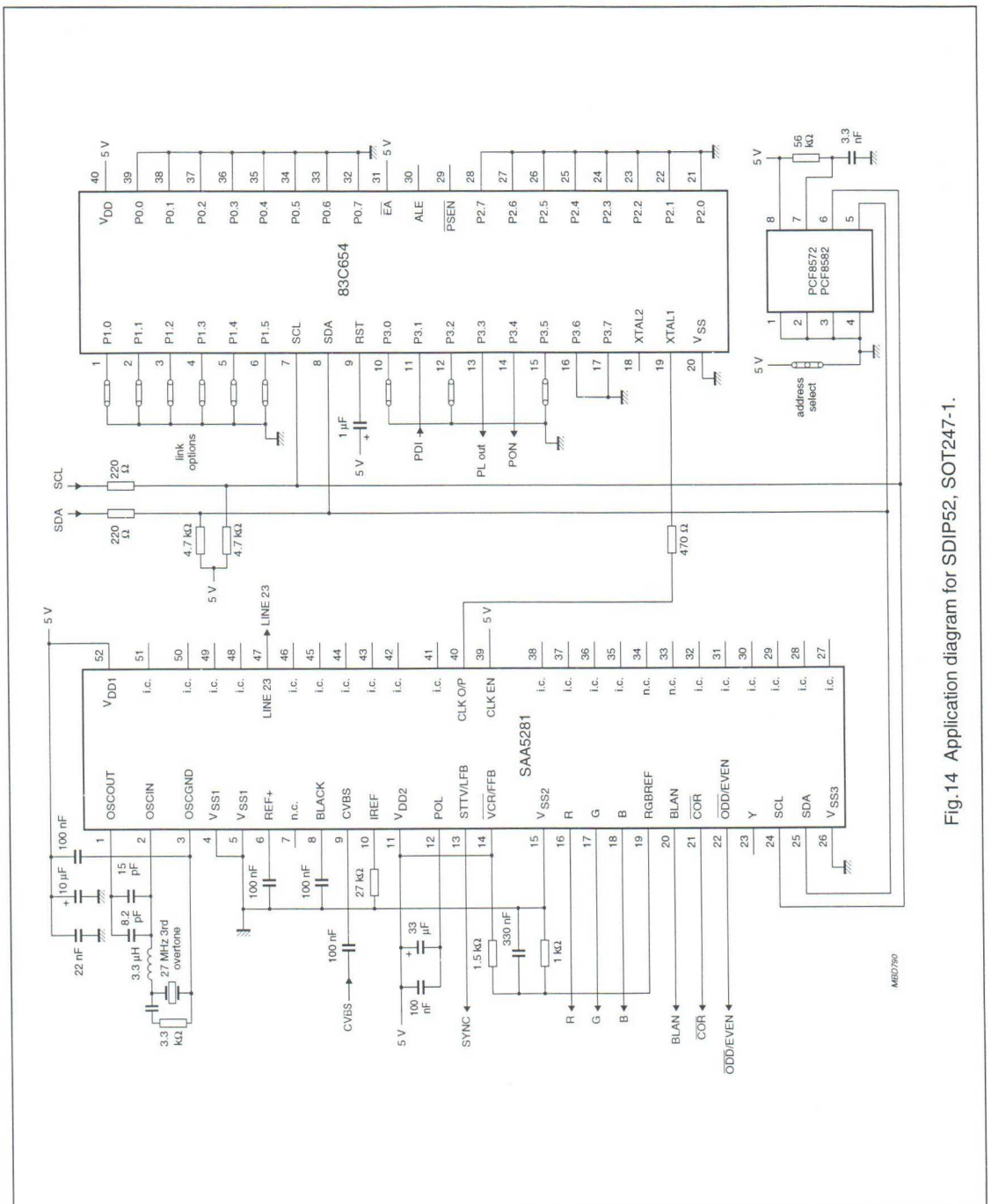


Fig.14 Application diagram for SDIP52, SOT247-1.

One page Economy Teletext/TV microcontroller

SAA5290

FEATURES

General

- Complete one page teletext decoder and TV microcontroller in a single 52-pin package
- Eastern European, Western European and Turkish language variants covered in one device
- Double size, double width and double height character capability for On-Screen Display (OSD)
- Enhanced display features including meshing and shadowing
- Separate display and acquisition timing for increased flexibility
- Minimum peripheral component count
- 525 line and 625 line display synchronization
- Standby mode through power-down of teletext and analog hardware.

Microcontroller

- 16 kbytes masked ROM (16 kbytes EEPROM variant for product development)
- 256 bytes of on-chip RAM
- Six 6-bit Pulse Width Modulators (PWM) and one 14-bit precision PWM
- 4-bit Digital-to-Analog Converter (DAC) and comparator with a 3-input multiplexer allowing implementation of 3 Analog-to-Digital Converters (ADC) in software
- 2 high current (10 mA) open-drain outputs
- Interrupt logic 0 triggered on rising and falling edges, providing pulse-width measurement for remote control decoding
- Master and slave bit-level I²C-bus hardware.

DESCRIPTION

The SAA5290 is a single-chip one page teletext decoder and television control microcontroller. The device will decode 625-line based World System Teletext transmissions and provides television control functions and On-Screen Display (OSD) functions.

The teletext decoder hardware is a derivative of the SAA5254 (IVT1.1X), and the TV control functionality provided by an on-chip industrial standard 80C51 microcontroller. A single-page static RAM is included on-board providing a complete one page teletext decoder and OSD memory.

The SAA5290 is available as a mask-programmed ROM version. An EEPROM version is also available for product development. Both versions are available in an SDIP52 package.

ORDERING INFORMATION

TYPE NUMBER	MEMORY	PACKAGE		
		NAME	DESCRIPTION	VERSION
SAA5290ZP/nnn(1)	ROM	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1
SAA5290ZP/NVI(2)	EEPROM	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1

Notes

1. nnn is a three-digit number referencing the microcontroller program ROM mask.
2. I is a digit number referring to the language variant of the SAA5290ZP/NV.

One page Economy Teletext/TV microcontroller

SAA5290

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DDM}	microcontroller supply current	–	25	40	mA
I_{DDA}	analog supply current	–	35	50	mA
I_{DDT}	teletext supply current	–	20	30	mA
f_{xtal}	crystal frequency	–	12	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C

BLOCK DIAGRAM

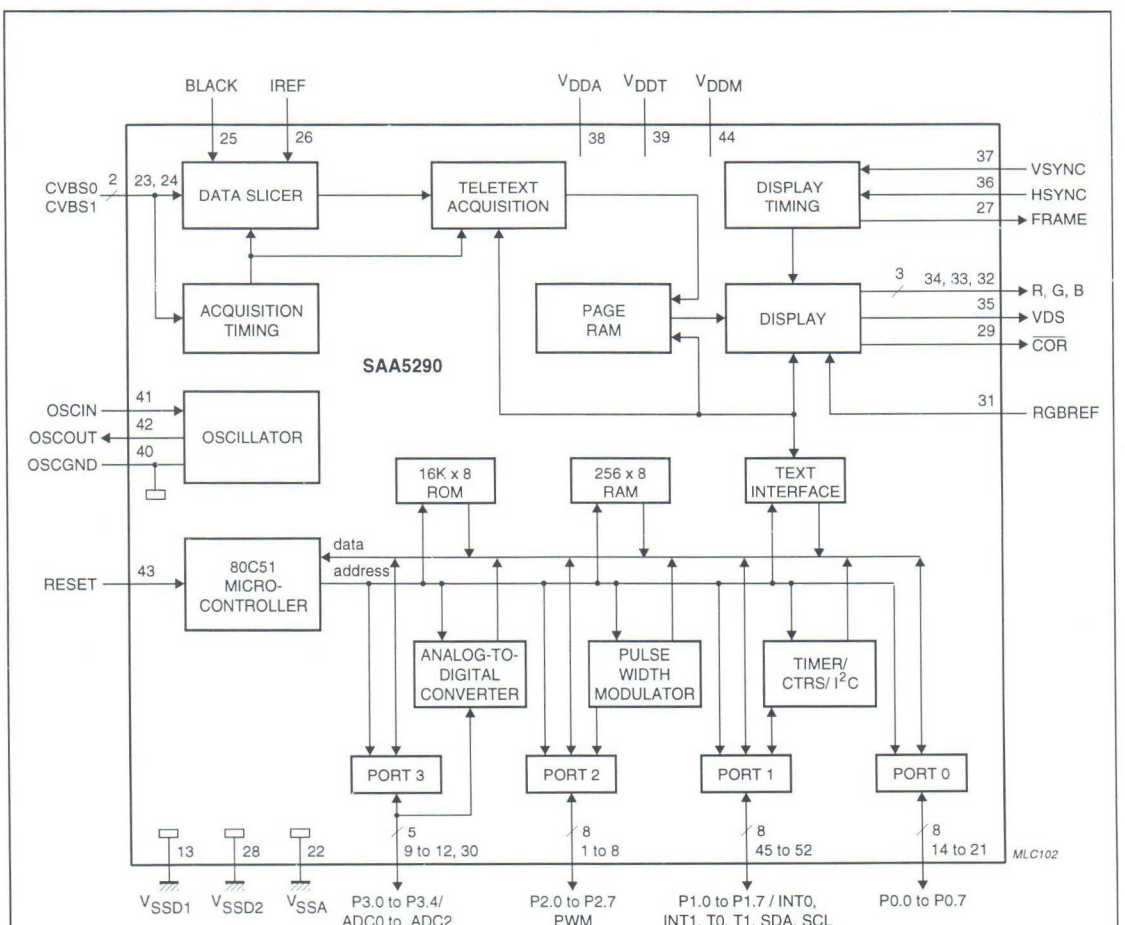


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
P2.0/TPWM	1	**PORT 2**: 8-bit open-drain bidirectional port with alternative functions. P2.0/TPWM is the output for the 14-bit high precision PWM. P2.1/PWM0 to P2.6/PWM5 are the outputs for the 6-bit PWMs 0 to 5.
P2.1/PWM0	2	
P2.2/PWM1	3	
P2.3/PWM2	4	
P2.4/PWM3	5	
P2.5/PWM4	6	
P2.6/PWM5	7	
P2.7	8	
P3.0/ADC0	9	**PORT 3**: 5-bit open-drain bidirectional port with alternative functions. P3.0/ADC0 to P3.2/ADC2 are the inputs for the software ADC facility.
P3.1/ADC1	10	
P3.2/ADC2	11	
P3.3	12	
P3.4	30	
V_{SSD1}	13	digital ground 1 for teletext and microcontroller circuits.
P0.0	14	**PORT 0**: 8-bit open-drain bidirectional port. P0.5 and P0.6 have 10 mA current sinking capability at 0.5 V for direct drive of LEDs.
P0.1	15	
P0.2	16	
P0.3	17	
P0.4	18	
P0.5	19	
P0.6	20	
P0.7	21	
V_{SSA}	22	analog ground.
CVBS0	23	Composite video input. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor.
CVBS1	24	
BLACK	25	Video black level storage input. This pin should be connected to V_{SSA} via a 100 nF capacitor.
IREF	26	Reference current input for analog circuits, connected to V_{SSA} via a 27 kΩ resistor.
FRAME	27	De-interlace output synchronized with the VSYNC pulse to produce a non-interlaced display by adjustment of the vertical deflection currents.
V_{SSD2}	28	Digital ground 2.
$\overline{COR}$	29	Open-drain, active LOW output which allows selective contrast reduction of the TV picture to enhance a mixed mode display.
RGBREF	31	DC input voltage to define the output HIGH level on the RGB pins.
B	32	Dot rate character output of the BLUE colour information.
G	33	Dot rate character output of the GREEN colour information.
R	34	Dot rate character output of the RED colour information.
VDS	35	Video/data switch push-pull output for dot rate fast blanking.
HSYNC	36	Horizontal sync dedicated input for a TTL-level version of the horizontal sync pulse. The polarity of this pulse is programmable by register bit TXT1.H POLARITY.

SYMBOL	PIN	DESCRIPTION
VSYNC	37	Vertical sync dedicated input for a TTL-level version of the vertical sync pulse. The polarity of this pulse is programmable by register bit TXT1.V POLARITY.
V_{DDA}	38	+5 V analog power supply.
V_{DDT}	39	+5 V teletext power supply.
OSCGND	40	Crystal oscillator ground.
OSCIN	41	12 MHz crystal oscillator input.
OSCOUT	42	12 MHz crystal oscillator output.
RESET	43	If the reset input is HIGH for 2 machine cycles (24 oscillator periods) while the oscillator is running, the SAA5290 is reset. This pin should be connected to V_{DDM} via a 2.2 µF capacitor.
V_{DDM}	44	+5 V microcontroller power supply.
P1.0/INT1	45	**PORT 1**: 8-bit open-drain bidirectional port with alternative functions. P1.0/INT1 is external interrupt 1 which can be triggered on the rising and falling edge of the pulse. P1.1/T0 is the counter/timer 0. P1.2/INT0 is external interrupt 0. P1.3/T1 is the counter/timer 1. P1.6/SCL is the serial clock input for I^2C-bus. P1.7/SDA is the serial data port for the I^2C-bus.
P1.1/T0	46	
P1.2/INT0	47	
P1.3/T1	48	
P1.6/SCL	49	
P1.7/SDA	50	
P1.4	51	
P1.5	52	

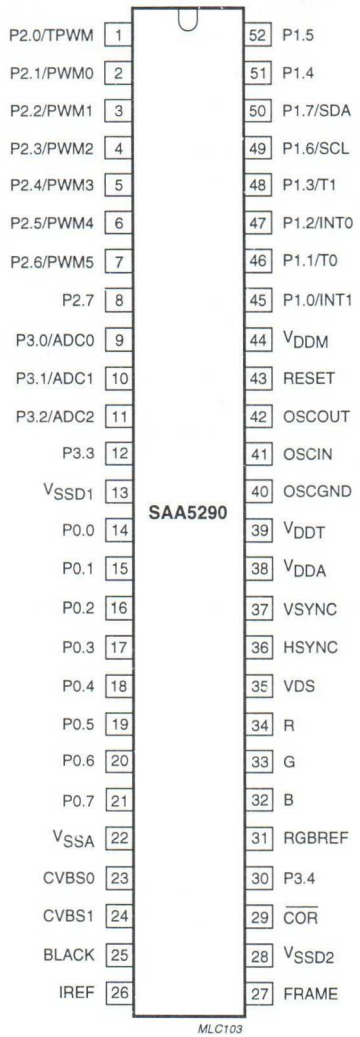


Fig.2 Pin configuration.

QUALITY AND RELIABILITY

This device will meet Philips Semiconductors General Quality Specification for Business group *"Consumer Integrated Circuits SNW-FQ-611-Part E"* (see *"Quality Reference Handbook"*, order number 9398 510 63011). The principal requirements are shown in Tables 1 to 4.

Group A

Table 1 Acceptance tests per lot

TEST	REQUIREMENTS(1)
Mechanical	cumulative target: <80 ppm
Electrical	cumulative target: <80 ppm

Group B

Table 2 Processability tests (by package family)

TEST	REQUIREMENTS(1)
Solderability	<7% LTPD
Mechanical	<15% LTPD
Solder heat resistance	<15% LTPD

Group C

Table 3 Reliability tests (by process family)

TEST	CONDITIONS	REQUIREMENTS(1)
Operational life	168 hours at T_j = 150 °C	<1500 FPM; equivalent to <100 FITS at T_j = 70 °C
Humidity life	temperature, humidity, bias 1000 hours, 85 °C, 85% RH (or equivalent test)	<2000 FPM
Temperature cycling performance	$T_{stg(min)}$ to $T_{stg(max)}$	<2000 FPM

Table 4 Reliability tests (by device type)

TEST	CONDITIONS	REQUIREMENTS(1)
ESD and latch-up	ESD Human body model 2000 V, 100 pF, 1.5 kΩ	<15% LTPD
	ESD Machine model 200 V, 200 pF, 0 Ω	<15% LTPD
	latch-up 100 mA, 1.5 × V_{DD} (absolute maximum)	<15% LTPD

Notes to Tables 1 to 4

1. ppm = fraction of defective devices, in parts per million.
   LTPD = Lot Tolerance Percent Defective.
   FPM = fraction of devices failing at test condition, in Failures Per Million.
   FITS = Failures In Time Standard.

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)		−0.3	+6.5	V
V_I	input voltage (any input)	note 1	−0.3	V_{DD} + 0.5	V
V_O	output voltage (any output)	note 1	−0.3	V_{DD} + 0.5	V
I_O	output current (each output)		–	±10	mA
I_{IOK}	DC input or output diode current		–	±20	mA
ΔV_{SS}	difference between V_{SSD}, V_{SSA} and OSCGND		–	±0.1	V
ΔV_{DD}	difference between V_{DDM}, V_{DDT} and V_{DDA}	note 2	–	±0.1	V
T_{amb}	operating ambient temperature		−20	+70	°C
T_{stg}	storage temperature		−55	+125	°C

Notes

1. This maximum value has an absolute maximum of 6.5 V independent of V_{DD}.
2. Except in standby mode.

CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage (V_{DD} to V_{SS})		4.5	5.0	5.5	V
I_{DDM}	microcontroller supply current		–	25	40	mA
I_{DDA}	analog supply current		–	35	50	mA
I_{DDT}	teletext supply current		–	20	30	mA
Digital inputs						
RESET						
V_{IL}	LOW level input voltage		−0.3	–	$0.2V_{DD}$ − 0.1	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	4	pF
HSYNC AND VSYNC						
V_{thf}	switching threshold falling		$0.2V_{DD}$	–	–	V
V_{thr}	switching threshold rising		–	–	$0.8V_{DD}$	V
V_{HYS}	hysteresis voltage		–	$0.33V_{DD}$	–	V
C_I	input capacitance		–	–	4	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital outputs						
R, G AND B (note 1)						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = –2 mA	V_{RGBREF} – 0.3	V_{RGBREF}	V_{RGBREF} + 0.4	V
$\|Z_O\|$	output impedance		–	–	150	Ω
C_L	load capacitance		–	–	50	pF
I_O	DC output current		–	–	–4	mA
t_r	output rise time	between 10% and 90%; C_L = 50 pF	–	–	20	ns
t_f	output fall time	between 90% and 10%; C_L = 50 pF	–	–	20	ns
$\overline{COR}$ (OPEN-DRAIN OUTPUT)						
V_{OH}	HIGH level pull-up output voltage		–	–	V_{DD}	V
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.5	V
I_{OL}	LOW level output current		–	–	2	mA
C_L	load capacitance		–	–	25	pF
VDS						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = –1.6 mA	V_{DD} – 0.3	–	V_{DD} + 0.4	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	between 10% and 90%; C_L = 50 pF	–	–	20	ns
t_f	output fall time	between 90% and 10%; C_L = 50 pF	–	–	20	ns
R, G, B AND VDS						
t_{skew}	skew delay between any two pins		–	–	20	ns
FRAME						
V_{OH}	HIGH level output voltage	I_{OL} = 8 mA	0	–	0.5	V
V_{OL}	LOW level output voltage	I_{OL} = –8 mA	V_{DD} – 0.5	–	V_{DD}	V
I_{OL}	LOW level output current		–8	–	+8	mA
C_L	load capacitance		–	–	100	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital input/outputs						
P0.0 TO P0.4, P0.7, P1.0 TO P1.5, P2.0 TO P2.7 AND P3.0 TO P3.5						
V_{IL}	LOW level input voltage		−0.3	–	$0.2V_{DD} - 0.1$	V
V_{IH}	HIGH level input voltage		$0.2V_{DD} + 0.9$	–	$V_{DD} + 0.3$	V
C_I	input capacitance		–	–	4	pF
V_{OL}	LOW level output voltage	I_{OL} = 3.2 mA	0	–	0.45	V
C_L	load capacitance		–	–	50	pF
P0.5 AND P0.6						
V_{IL}	LOW level input voltage		−0.3	–	$0.2V_{DD} - 0.1$	V
V_{IH}	HIGH level input voltage		$0.2V_{DD} + 0.9$	–	$V_{DD} + 0.3$	V
C_I	input capacitance		–	–	4	pF
V_{OL}	LOW level output voltage	I_{OL} = 10 mA	0	–	0.45	V
C_L	load capacitance		–	–	50	pF
P1.6 AND P1.7						
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	$V_{DD} + 0.3$	V
C_I	input capacitance		–	–	5	pF
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.5	V
C_L	load capacitance		–	–	400	pF
t_f	output fall time	between 3 and 1 V	–	–	200	ns
Analog inputs						
CVBS0 AND CVBS1						
V_{sync}	sync voltage amplitude		0.1	0.3	0.6	V
$V_{vid(p-p)}$	video input voltage amplitude (peak-to-peak value)		0.7	1.0	1.4	V
Z_{source}	source impedance		–	–	250	Ω
V_{IH}	HIGH level input voltage		3.0	–	$V_{DD} + 0.3$	V
$\|Z_I\|$	input impedance		2.5	5.0	–	kΩ
C_I	input capacitance		–	–	10	pF
IREF						
R_{gnd}	resistor to ground		–	27	–	kΩ
RGBREF (note 1)						
V_I	input voltage		−0.3	–	V_{DD}	V
I_I	DC input current		–	–	12	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADC0, ADC1 AND ADC2						
V_{IL}	LOW level input voltage		−0.3	–	V_{DD}	V
Analog input/output						
BLACK						
C_{black}	storage capacitor to ground		–	100	–	nF
V_{black}	black level voltage for nominal sync amplitude		1.8	2.15	2.5	V
I_{LI}	input leakage current		−10	–	+10	μA
Crystal oscillator						
OSCIN						
V_{IL}	LOW level input voltage		−0.3	–	$0.2V_{DD} - 0.1$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.3$	V
C_I	input capacitance		–	–	10	pF
OSCOUT						
f_{osc}	crystal oscillator frequency		–	12	–	MHz
C_O	output capacitance		–	–	10	pF
CRYSTAL SPECIFICATION (note 2)						
f_{xtal}	nominal frequency		–	12	–	MHz
C_L	load capacitance		–	32	–	pF
C1	series capacitance	$T_{amb} = 25$ °C	–	18.5	–	fF
C0	parallel capacitance	$T_{amb} = 25$ °C	–	4.9	–	pF
R_r	resonance resistance	$T_{amb} = 25$ °C	–	35	–	Ω
T_{xtal}	temperature range		−20	+25	+70	°C
X_j	adjustment tolerance	$T_{amb} = 25$ °C	–	–	$\pm 50 \times 10^{-6}$	
X_d	drift		–	–	$\pm 30 \times 10^{-6}$	

Notes

1. All RGB current is sourced from the RGBREF pin. The maximum effective series resistance between RGBREF and the R, G and B pins is 150 Ω.
2. Crystal order number 4322 143 05561.

Table 5 Characteristics for the I²C-bus interface

SYMBOL	PARAMETER	INPUT	OUTPUT	I²C-BUS SPECIFICATION
SCL timing				
$t_{HD;STA}$	START condition hold time	≥4.0 µs	note 1	≥4.0 µs
t_{LOW}	SCL LOW time	≥4.7 µs	note 1	≥4.7 µs
t_{HIGH}	SCL HIGH time	≥4.0 µs	≥4.0 µs; note 2	≥4.0 µs
t_{rC}	SCL rise time	≤1.0 µs	note 3	≤1.0 µs
t_{fC}	SCL fall time	≤0.3 µs	≤0.3 µs; note 4	≤0.3 µs
SDA timing				
$t_{SU;DAT1}$	data set-up time	≥250 ns	note 1	≥250 ns
$t_{HD;DAT}$	data hold time	≥0 ns	note 1	≥0 ns
$t_{SU;STA}$	repeated START set-up time	≥4.7 µs	note 1	≥4.7 µs
$t_{SU;STO}$	STOP condition set-up time	≥4.0 µs	note 1	≥4.0 µs
t_{BUF}	bus free time	≥4.7 µs	note 1	≥4.7 µs
t_{rD}	SDA rise time	≤1.0 µs	note 3	≤1.0 µs
t_{fD}	SDA fall time	≤0.3 µs	≤0.3 µs; note 4	≤0.3 µs

Notes

1. This parameter is determined by the user software. It must comply with the I²C-bus specification.
2. This value gives the auto-clock pulse length which meets the I²C-bus specification for the special crystal frequency. Alternatively, the SCL pulse must be timed by software.
3. The rise time is determined by the external bus line capacitance and pull-up resistor. It must be less than 1 µs.
4. The maximum capacitance on bus lines SDA and SCL is 400 pF.

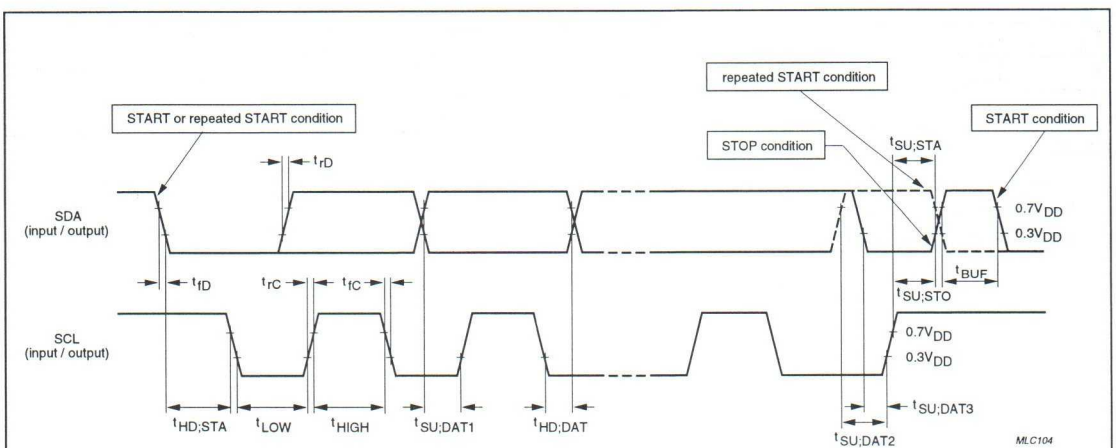


Fig.3 I²C-bus interface timing.

FUNCTIONAL DESCRIPTION

Introduction

The SAA5290 is an integrated teletext decoder and microcontroller. The teletext decoder is derived from the SAA5254 single page teletext decoder IC, with a number of enhancements to increase its suitability for on-screen display applications. The microcontroller is a derivative of the industry standard 80C51 microcontroller. A block diagram of the SAA5290 is given in Fig.1.

Microcontroller

The functionality of the microcontroller used on the SAA5290 is described here with reference to the industry standard 80C51 microcontroller. A full description of its functionality can be found in the handbook *80C51-based 8-bit microcontrollers IC20*. Using the 80C51 as a reference, the changes made for the SAA5290 fall into two categories, features not supported by the SAA5290 and features found on the SAA5290 but not supported by the 80C51.

80C51 features not supported by the SAA5290

Interrupt priority

The IP SFR is not implemented and all interrupts are treated with the same priority level. The SAA5290 retains the normal prioritization of interrupts within a level.

Table 6 Interrupts and their vector addresses

EVENT	PROGRAM MEMORY ADDRESS
Reset	000H
External INT0	003H
Timer 0	00BH
External INT1	013H
Timer 1	01BH
I^2C-bus	053H

Off-chip memory

The SAA5290 does not support the use of off-chip program memory or off-chip data memory. This means that the SAA5290 does not have any of $\overline{EA}$, $\overline{RD}$, $\overline{WR}$, ALE or $\overline{PSEN}$ pins. The 4 MOVX instructions which move data to and from external RAM should not be used.

Idle and power-down modes

Idle and power-down modes are not supported by the SAA5290. As a consequence, the respective bits in PCON are not available.

UART function

The 80C51 UART is not available in the SAA5290. As a consequence the SCON and SBUF SFRs are removed and the ES bit in the IE SFR is unavailable.

Additional features for the SAA5290

The following features are provided by the SAA5290 in addition to the standard 80C51 features.

Interrupts

The external INT1 interrupt is modified to generate an interrupt on both the rising and falling edges of the INT1 pin, when EX1 bit is set. This facility allows for software pulse width measurement for handling of a remote control.

Bit level I^2C-bus interface

The bit-level serial I/O supports the I^2C-bus. P1.6/SCL and P1.7/SDA are the serial I/O pins. These two pins meet the I^2C-bus specification concerning the input levels and output drive capability. Consequently, these pins have an open-drain output configuration. All the four following modes of the I^2C-bus are supported.

- Master transmitter
- Master receiver
- Slave transmitter

- Slave receiver.

The advantages of the bit-level I²C-bus hardware, compared with a full software I²C-bus implementation are:

- The hardware can generate the SCL pulse
- Testing a single bit (RBF or WBF respectively) is sufficient as a check for error-free transmission.

The bit-level I²C-bus hardware operates on serial bit level and performs the following functions:

- Filtering the incoming serial data and clock signals
- Recognizing the START condition
- Generating a serial interrupt request SI after reception of a START condition and the first falling edge of the serial clock
- Recognizing the STOP condition
- Recognizing a serial clock pulse on the SCL line
- Latching a serial bit on the SDA line (SDI)
- Stretching the SCL LOW period of the serial clock to suspend the transfer of the next serial data bit
- Setting Read Bit Finished (RBF) when the SCL clock pulse has finished and Write Bit Finished (WBF) if there is no arbitration loss detected (i.e. SDA = logic 0 while SDO = logic 1)
- Setting a serial clock LOW-to-HIGH detected (CLH) flag
- Setting a Bus Busy (BB) flag on a START condition and clearing this flag on a STOP condition
- Releasing the SCL line and clearing the CLH, RBF and WBF flags to resume transfer to the next serial data bit
- Generating an automatic clock if the single bit data register S1BIT is used in master mode.

The following functions must be done in software:

- Handling the I²C-bus START interrupts
- Converting serial data to parallel data when receiving
- Converting parallel data to serial data when transmitting
- Comparing the received slave address with its own address
- Interpreting the acknowledge information
- Guarding the I²C-bus status if RBF or WBF = logic 0.

Additionally, if acting as master:

- Generating START and STOP conditions
- Handling bus arbitration
- Generating serial clock pulses if S1BIT is not used.

Three SFRs support the function of the bit-level I²C-bus hardware, they are S1INT, S1BIT and S1SCS.

LED SUPPORT

Port pins P0.5 and P0.6 have a 10 mA current sinking capability to enable LEDs to be driven directly.

PWM DACs

The SAA5290 has six 6-bit PWM DACs and one14-bit PWM DAC. These allow direct control of other parts of the television.

The low resolution 6 bit DACs are controlled by their corresponding SFR (PWM0 to PWM5) and are connected as alternative outputs of Port P2. The port bit corresponding to the PWM should be set to logic 1 for correct operation of the PWM.

Table 7 Special Function Registers PWM0 to PWM5

D7	D6	D5	D4	D3	D2	D1	D0
PWE	–	PV5	PV4	PV3	PV2	PV1	PV0

If the PWE bit for a particular port is set to logic 1, the PWM is active and controls its assigned port pin. If the PWE bit is set to logic 0 the corresponding port pin is controlled by the bit in the corresponding port register for that port.

The output of the PWM is a pulse of period 21.33 µs with a duty cycle determined by the binary value, PV5 to PV0, multiplied by 0.33 µs. The 14 bit PWM is controlled with SFR registers TDACL and TDACH.

Table 8 Special Function Register TDACL

D7	D6	D5	D4	D3	D2	D1	D0
TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0

Table 9 Special Function Register TDACH

D7	D6	D5	D4	D3	D2	D1	D0
PWE	–	TD13	TD12	TD11	TD10	TD9	TD8

If the PWE bit is set to logic 1, the TPWM is active and controls Port P2.0. If the PWE bit is set to logic 0 the port pin is controlled by the bit in the corresponding port register for P2.0.

The output of the TPWM is a pulse of period 42.66 µs with a duty cycle determined by the binary value, TD13 to TD7, multiplied by 0.33 µs.

The 7 least significant bits, TD6 to TD0, extend the HIGH time of a proportion of the pulses by 0.33 μs. If the LSB is set then 1 in 128 cycles is extended, if bit 1 is set then 1 in 64 cycles is extended, and so on.

SOFTWARE ADC

Up to 3 successive approximation ADCs can be implemented in software by making use of the on-board 4-bit DAC and multiplexed voltage comparator. The software ADC uses 3 analog inputs which are multiplexed with P3.0 to P3.2.

The control of the ADC is achieved using the SAD SFR. SAD.5 and SAD.6 select one of the three inputs to pass to the comparator. The other input comes from the DAC whose input is set by SAD bits 0 to 3. The output of the comparator is SAD bit 7 and is valid by the next instruction after starting the comparison by setting SAD.ST to logic 1.

Microcontroller interfacing

The 80C51 CPU communicates with the peripheral functions using Special Function Registers (SFRs) which are addressed as RAM locations. The registers in the teletext decoder appear as normal SFRs in the microcontroller memory map, but are written to using a serial bus. This bus is controlled by dedicated hardware which uses a simple handshake system for software synchronization. The SFR memory map is given in Table 10.

Table 10 SAA5290 Special Function Register map (note 1)

SYMBOL	DESCR.	DIRECT ADDR. (HEX)	BIT ADDRESS, SYMBOL OR ALTERNATIVE PORT FUNCTION								RESET VALUE (HEX)
			MSB							LSB	
ACC[2]	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
B[2]	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR:	Data Pointer (2 bytes):										
DPH	High byte	83H	–	–	–	–	–	–	–	–	00H
DPL	Low byte	82H	–	–	–	–	–	–	–	–	00H
IE[2][3]	Interrupt Enable	A8H	AF	AE	AD	AC	AB	AA	A9	A8	X0H
			EA	ES1	*	*	ET1	EX1	ET0	EX0	
P0[2]	Port 0	80H	87	86	85	84	83	82	81	80	FFH
P1[2]	Port 1	90H	97	96	95	94	93	92	91	90	FFH
P2[2]	Port 2	A0H	A7	A6	A5	A4	A3	A2	A1	A0	FFH
P3[2][3]	Port 3	B0H	–	–	–	B4	B3	B2	B1	B0	XXX11111B
PCON[3]	Power Control	87H	*	*	*	*	GF1	GF0	*	*	XXXX00XXB
PSW[2]	Program Status Word	D0H	D7	D6	D5	D4	D3	D2	D1	D0	000000X0B
			CY	AC	F0	RS1	RS0	0V	*	P	
PWM0[3]	Pulse Width Modulator 0	D5H	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	–
PWM1[3]	Pulse Width Modulator 1	D6H	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	–
PWM2[3]	Pulse Width Modulator 2	D7H	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	–
PWM3[3]	Pulse Width Modulator 3	DCH	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	–
PWM4[3]	Pulse Width Modulator 4	DDH	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	–
PWM5[3]	Pulse Width Modulator 5	DEH	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	–
S1BIT[3]	Serial I^2C data	D9H	SDI/ SDO	*	*	*	*	*	*	*	00H

SYMBOL	DESCR.	DIRECT ADDR. (HEX)	BIT ADDRESS, SYMBOL OR ALTERNATIVE PORT FUNCTION								RESET VALUE (HEX)
			MSB							LSB	
S1INT[3]	Serial I²C interrupt	DAH	SI	*	*	*	*	*	*	*	–
S1SCS[2][3]	Serial I²C control	D8H	DF	DE	DD	DC	DB	DA	D9	D8	–
			SDI/ SDO	SCI/ SDO	CLH	BB	RBF	WBF	STR	ENS	
SAD[2] [3]	Software A to D	E8H	EF	EE	ED	EC	EB	EA	E9	E8	00H
			VHI	CH1	CH0	ST	SAD3	SAD2	SAD1	SAD0	
SP	Stack Pointer	81H	8F	8E	8D	8C	8B	8A	89	88	07H
TCON[2]	Timer/counter control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
TDACH	TPWM High byte	D3H	PWE	*	TD13	TD12	TD11	TD10	TD9	TD8	00H
TDACL	TPWM Low byte	D2H	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0	00H
TH0	Timer 0 High byte	8CH	–	–	–	–	–	–	–	–	00H
TH1	Timer 1 High byte	8DH	–	–	–	–	–	–	–	–	00H
TL0	Timer 0 Low byte	8AH	–	–	–	–	–	–	–	–	00H
TL1	Timer 1 Low byte	8BH	–	–	–	–	–	–	–	–	00H
TMOD	Timer/counter mode	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	00H
TXT0[3]	Teletext register 0	C0H	X24 POS	*	AUTO FRAME	DISABLE HDR ROLL	DISPLAY STATUS ROW ONLY	DISABLE FRAME	*	*	00H
TXT1[3]	Teletext register 1	C1H	*	8-BIT	ACQ OFF	X26	FULL FIELD	FIELD POLARITY	H POLARITY	V POLARITY	00H
TXT2[3]	Teletext register 2	C2H	*	*	*	*	*	SC2	SC1	SC0	00H
TXT3[3]	Teletext register 3	C3H	*	*	*	PRD4	PRD3	PRD2	PRD1	PRD0	00H

SYMBOL	DESCR.	DIRECT ADDR. (HEX)	BIT ADDRESS, SYMBOL OR ALTERNATIVE PORT FUNCTION								RESET VALUE (HEX)
			MSB							LSB	
TXT4[3]	Teletext register 4	C4H	*	*	EAST/ $\overline{\text{WEST}}$	*	B MESH ENABLE	C MESH ENABLE	TRANS ENABLE	SHADOW ENABLE	00H
TXT5[3]	Teletext register 5	C5H	BKGND OUT	BKGND IN	$\overline{\text{COR}}$ OUT	$\overline{\text{COR}}$ IN	TEXT OUT	TEXT IN	PICTURE ON OUT	PICTURE ON IN	00000011B
TXT6[3]	Teletext register 6	C6H	BKGND OUT	BKGND IN	$\overline{\text{COR}}$ OUT	$\overline{\text{COR}}$ IN	TEXT OUT	TEXT IN	PICTURE ON OUT	PICTURE ON IN	00000011B
TXT7[3]	Teletext register 7	C7H	STATUS ROW TOP	CURSOR ON	$\overline{\text{CONCEAL}}$ /REVEAL	$\overline{\text{TOP}}$/ BTM	$\overline{\text{SNG}}$/DBL HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	00H
TXT8[3]	Teletext register 8	C8H	*	*	*	*	*	*	*	$\overline{\text{CVBS0}}$/ CVBS1	00H
TXT9[3]	Teletext register 9	C9H	*	CLEAR MEM.	A0	R4	R3	R2	R1	R0	00H
TXT10[3]	Teletext register 10	CAH	*	*	C5	C4	C3	C2	C1	C0	00H
TXT11[3]	Teletext register 11	CBH	D7	D6	D5	D4	D3	D2	D1	D0	00H
TXT12[3]	Teletext register 12	CCH	$\overline{\text{625}}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TXT ON	VIDEO QUALITY	
TXT13[2][3]	Teletext register 13	B8H	BF	BE	BD	BC	BB	BA	B9	B8	00H
			*	*	*	*	*	*	*	TXT I/FACE BUSY	

Notes

1. The star (*) indicates these bits are inactive and must be written to logic 0 for future compatibility.
2. SFRs are bit addressable.
3. SFRs are modified or added to the 80C51 SFRs.

Table 11 SFR description

REGISTER	FUNCTION
IE - Interrupt Enable	
EA	Disable all interrupts (logic 0) or use individual enable bits (logic 1).
ES1	I^2C-bus interrupt enable (logic 1).
ET1	Enable Timer 1 overflow interrupt (logic 1).
EX1	Enable external interrupt 1 (logic 1).
ET0	Enable Timer 0 overflow interrupt (logic 1).
EX0	Enable external interrupt 0 (logic 1).
PCON - Power Control	
GF0	General purpose flag bit 0.
GF1	General purpose flag bit 1.
PWM0 to PWM5 - 6-bit Pulse Width Modulator control registers	
PWE	Activate this 6-bit PWM and take over port pin (logic 1).
PV0 to PV5	Value to output by this 6-bit PWM.
SAD - Software ADC control	
VHI	Analog input voltage greater than DAC output voltage (logic 1).
CH0 and CH1	See Table 12.
ST	Initiate voltage comparison (logic 1). This is automatically reset.
SAD0 to SAD3	4-bit DAC input value. The DAC output of this value is compared with analog input voltage.
S1BIT - Serial I^2C-bus data (READ)	
SDI	I^2C-bus data bit latched-in from SDA on the last rising edge of SCL.
S1BIT - Serial I^2C-bus data (WRITE)	
SDO	I^2C-bus data bit output.
S1INT - Serial I^2C-bus interrupt	
SI	I^2C-bus interrupt flag.
S1SCS - Serial I^2C-bus control (READ)	
SDI	Serial data input at SDA.
SCI	Serial clock input at SCL.
CLH	Clock LOW-to-HIGH transition flag.
BB	Bus busy flag.
RBF	Read bit finished flag.
WBF	Write bit finished flag.
STR	Clock stretching enable (logic 1).
ENS	Enable serial I/O (logic 1).

REGISTER	FUNCTION
S1SCS - Serial I²C-bus control (WRITE)	
SDO	Serial data output at SDA.
SCO	Serial clock output at SCL.
CLH	Clock LOW-to-HIGH transition.
STR	Clock stretching enable (logic 1).
ENS	Enable serial I/O (logic 1).
TDACH - 14-bit PWM MSB register	
PWE	Activate this 14-bit PWM and take over port pin (logic 1).
TD8 to TD13	6 LSBs of this value to be output by the 14-bit PWM.
TDACL - 14-bit PWM LSB register	
TD0 to TD7	8 LSBs of this value to be output by the 14-bit PWM.
TXT0 - Teletext register 0 (WRITE only)	
X24 POSITION	Store packet 24 in extension packet memory (logic 0) or page memory (logic 1).
AUTO FRAME	Frame output switched off automatically if any video displayed (logic 1).
DISABLE HDR ROLL	Do not write rolling headers and time into memory (logic 1).
STATUS ROW ONLY	Display only memory row (logic 1).
DISABLE FRAME	Frame output always LOW (logic 1).
TXT1 - Teletext register 1 (WRITE only)	
8-BIT	Data in packets 0 to 24 written into memory without error checking (logic 1).
ACQ OFF	Prevent teletext acquisition section writing to memory (logic 1).
X26	Disable automatic processing of packet 26 data (logic 1).
FULL FIELD	Accept teletext on TV lines 2 to 22 only (logic 0) or on any line (logic 1).
FIELD POLARITY	VSYNC in first half of the line (logic 0) or second half of the line (logic 1) at start of even field.
H POLARITY	HSYNC input positive-going (logic 0) or negative-going (logic 1).
V POLARITY	VSYNC input positive-going (logic 0) or negative-going (logic 1).
TXT2 - Teletext register 2 (WRITE only)	
SC0 to SC2	Start column at which page request data written into TXT3 SFR is placed.
TXT3 - Teletext register 3 (WRITE only)	
PRD0 to PRD4	Page request data.
TXT4 - Teletext register 4 (WRITE only)	
B MESH ENABLE	Enable meshing of area with black background (logic 1).
C MESH ENABLE	Enable meshing of area with other background colours (logic 1).
TRANS ENABLE	Black background colour is transparent i.e. video is displayed (logic 1).
SHADOW ENABLE	Enable south-east shadowing (logic 1).
EAST/$\overline{\text{WEST}}$	Western European languages displayed (logic 0) or Eastern European languages displayed (logic 1).

REGISTER	FUNCTION
TXT5 - Teletext register 5 (WRITE only)	
BKGND OUT	Background colour displayed outside teletext boxes (logic 1).
BKGND IN	Background colour displayed inside teletext boxes (logic 1).
$\overline{\text{COR}}$ OUT	$\overline{\text{COR}}$ output active outside teletext boxes (logic 1).
$\overline{\text{COR}}$ IN	$\overline{\text{COR}}$ output active inside teletext boxes (logic 1).
TEXT OUT	Text displayed outside teletext boxes (logic 1).
TEXT IN	Text displayed inside teletext boxes (logic 1).
PICTURE ON OUT	Video picture displayed outside teletext boxes (logic 1).
PICTURE ON IN	Video picture displayed inside teletext boxes (logic 1).
TXT6 - Teletext register 6 (WRITE only)	
–	This register has the same meaning as TXT5 but is only invoked if either newsflash (C5) or the subtitle (C6) bit in Row 25 of the basic page memory is set.
TXT7 - Teletext register 7 (WRITE only)	
STATUS ROW TOP	Display Row 24 below (logic 0) or above (logic 1) teletext page.
CURSOR ON	Display cursor at location pointed to by TXT9 and TXT10 (logic 1).
$\overline{\text{CONCEAL}}$/REVEAL	Display characters in areas with the conceal attribute set (logic 1).
$\overline{\text{TOP}}$/BOTTOM	Display Rows 0 to 11 (logic 0) or 12 to 23 (logic 1) when the double height bit is set.
$\overline{\text{SNG}}$/DBL HEIGHT	Display each character at twice normal height (logic 1).
BOX ON 24	Enable teletext boxes in memory Row 24 (logic 1).
BOX ON 1-23	Enable teletext boxes in memory Rows 1 to 23 (logic 1).
BOX ON 0	Enable teletext boxes in memory Row 0 (logic 1).
TXT8 - Teletext register 8 (WRITE only)	
$\overline{\text{CVBS0}}$/CVBS1	CVBS0 input (logic 0) or CVBS1 (logic 1) inputs used for teletext.
TXT9 - Teletext register 9 (WRITE only)	
CLEAR MEMORY	Write 20H into every location in teletext memory (logic 1).
A0	Access basic page memory (logic 0) or extension packet memory (logic 1) with TXT11 SFR.
R0 to R4	Memory row to be accessed with TXT11 SFR.
TXT10 - Teletext register 10 (WRITE only)	
C0 to C5	Memory column to be accessed with TXT11 SFR.
TXT11 - Teletext register 11	
D0 to D7	data byte written to, or read from, teletext memory.

REGISTER	FUNCTION
TXT12 - Teletext register 12 (READ only)	
$\overline{625}$/525 SYNC	A 625 line CVBS signal (logic 0), or a 525 line CVBS signal (logic 1) is being input.
ROM VER R0 to R4	Mask programmable to identify character set version.
TXT ON	Teletext power has been applied to the device (logic 1).
VIDEO QUALITY	CVBS input can be locked on by the teletext decoder (logic 1).
TXT13 - Teletext register 13 (READ only)	
TXT I/FACE BUSY	Text interface busy and no access for either READ or WRITE is allowed to SFRs TXT0 to TXT11 (logic 1). This register bit performs the software handshake to the teletext control registers.

Table 12 CH1 and CH0 selection

CH1	CH0	INPUT PIN
0	0	none
0	1	ADC0
1	0	ADC1
1	1	ADC2

TELETEXT DECODER FUNCTIONAL DESCRIPTION

Data slicer

The data slicer extracts the digital teletext data from the incoming analog waveform. This is performed by sampling the CVBS waveform and processing the samples to extract the teletext data and clock.

Acquisition timing

The acquisition timing is generated from a logic level positive-going composite sync signal 'VCS'. This signal is generated by the sync separator circuit which adaptively slices the sync pulses at 50% of their height. It is able to do this over a wide range of sync amplitudes by using the same basic principle used on VIP1 (SAA5230) and VIP2 (SAA5231).

Figure 4 is a block diagram showing the principles of operation. It relies upon the fact that the ratio of the sync width to the line time is approximately 13 : 1. In order to slice the sync pulse at the correct 50% level two currents are generated.

One is constant and is proportional to the difference between the black level of the video and the slicing level. The other is produced only when the video is below the slicing level, and is also proportional to the difference between the slicing level and the input, but has a magnitude13 times greater.

The black level is determined by a sync-gated peak detector. The video is negatively peak detected into an external capacitor (BLACK, pin 25), but not during the sync pulse VCS. The two currents are integrated on the CVBS input coupling capacitor and the net effect is to alter the mean input voltage until the (fixed) slicing level is correct.

The acquisition clocking and timing are locked to the VCS signal using a digital phased-locked-loop. The phase error in the acquisition phase-locked-loop is detected by a signal quality circuit which disables acquisition if poor signal quality is detected.

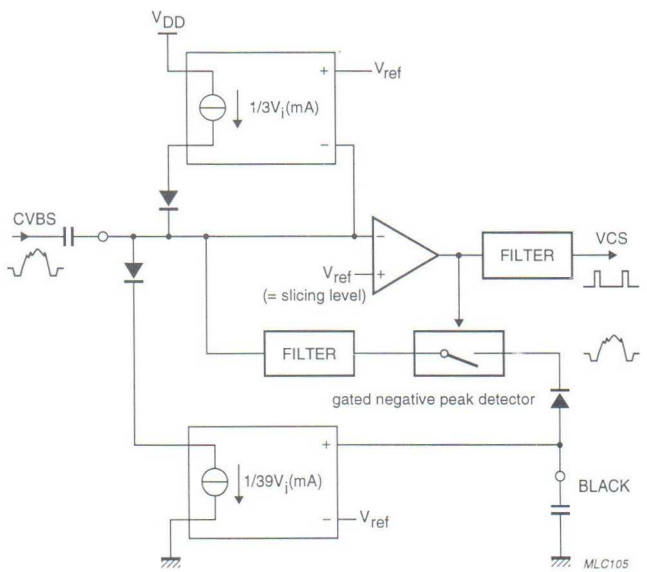


Fig.4 Sync separator block diagram.

Teletext acquisition

The SAA5290 is able to acquire 625-line World System Teletext. Teletext is acquired under control of the on-board 80C51 microcontroller. Pages are requested by writing a series of bytes into the TXT3 SFR which corresponds to the number of the page required. The bytes written into TXT3 are put into a small RAM with an auto-incrementing address. The start address for the RAM is set using the SFR TXT2 register. Table 13 shows the contents of the page request RAM.

If the 'DO CARE' bit for part of the page number is set to logic 0 then that part of the page number is ignored when the acquisition section is deciding whether a page being received off air should be stored or not. For example if the 'DO CARE' bits for the 4 subcode digits are all set to logic 0 then every subcode version of the page will be captured.

When the '$\overline{\text{HOLD}}$' bit is set to logic 0 the acquisition section will not recognize any page as having the correct page number and no pages will be captured.

Table 13 Register map for page requests (TXT3); note 1

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	DO CARE Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	DO CARE Page tens	PT3	PT2	PT1	PT0
2	DO CARE Page units	PU3	PU2	PU1	PU0
3	DO CARE Hours tens	X	X	HT1	HT0
4	DO CARE Hours units	HU3	HU2	HU1	HU0
5	DO CARE Minutes tens	X	MT2	MT1	MT0
6	DO CARE Minutes units	MU3	MU2	MU1	MU0

Note

1. X = don't care.

Page memory organization

The acquired teletext packets each contain 40 bytes of data and one packet is stored in each row of the text memory. The page memory organization is given in Fig.5. Rows 0 to 23 form the teletext page; Row 24 is available for status messages and FLOF/FASTEXT prompt information.

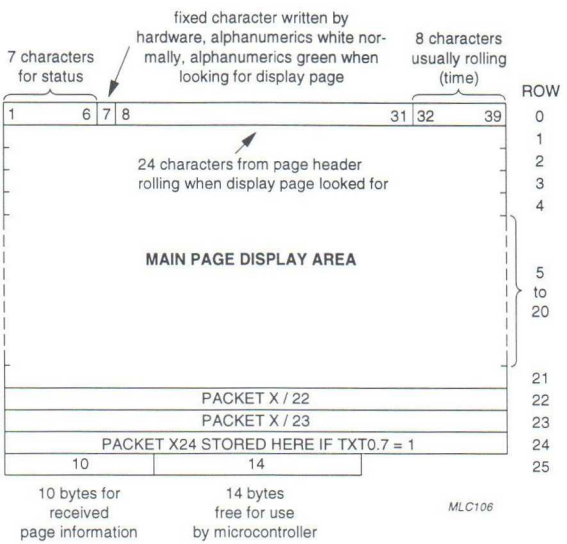


Fig.5 Basic page memory organization.

Row 0 (see Fig.5)

Row 0 is for the page header. The first seven characters (0 to 6) are free for status messages. Character 8 is an alphanumeric white or green control character, written automatically by SAA5290 to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25 (see Fig.5)

The first 10 bytes of row 25 contain control data relating to the received page as shown in Table 14. The remaining 14 bytes are free for use by the microcontroller.

Extension packet memory organization

If TXT0.X24 POS bit is set to logic 0, then Packet 24 is written into Row 0 of the extension memory.

Packet X27/0 is written to Row 1 of the extension memory, with bytes 0 to 37 being Hamming checked automatically.

Packet 8/30 is written to Row 2 of the extension memory, with bytes 0 to 6 being 8/4 Hamming checked, bytes 7 to 19 unchecked and bytes 20 to 39 odd parity checked.

Packet 26 processing

The SAA5290 contains on-board hardware processing of Packet 26 data. If a character corresponding to that being transmitted is available in the character set then the correct character code is written into the display memory.

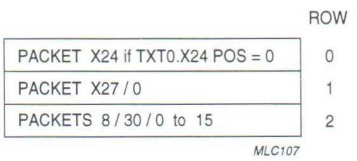


Fig.6 Organization of the extension memory.

Table 14 Row 25 received control data format

ROW 25										
D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Table 15 Page number and sub-code for Table 14

BIT NAME	DESCRIPTION
Page number	
MAG	magazine
PU	page units
PT	page tens
PBLF	page being looked for
HAM.ER	Hamming error in corresponding byte
Page sub-code	
MU	minutes units
MT	minutes tens
HU	hours units
HT	hours tens
C4 to C14	transmitted control bits

Display

The capabilities of the display are based on the requirements of level 1 teletext, with some enhancements for use with locally generated On-Screen Displays (OSD).

The display consists of 25 rows each of 40 characters, with the characters displayed being those from Rows 0 to 24 of the basic page memory. The page memory stores 8-bit character codes which correspond to 260 displayable characters and 44 control codes, normally displayed as spaces. Each character is defined by a matrix 12 pixels high and 10 pixels deep. When displayed each pixel is 0.5 µs wide and 1 TV line, in each field, high.

The SAA5290 signals the TV display circuits to display the RGB outputs of the SAA5290 rather than video picture by setting VDS HIGH. The way in which this signal is switched is controlled by the TXT5 and TXT6 SFRs. There are three control functions: background on, text on and picture on. There are separate bits for each function for inside and outside teletext boxes and if the newsflash or subtitle bits are set. This allows the software to configure the type of display required. The effect of the combination of these bits is given in Table 16. The $\overline{\text{COR}}$ bits in Register 5 and Register 6 control when the output is pulled LOW. This output is intended to act on the TV display circuits to reduce the contrast of the video display.

The display character set is given in Fig.9. The character set provided contains all the characters required to display Eastern and Western European languages. Register bit TXT4.EAST/$\overline{\text{WEST}}$ sets whether Eastern or Western languages are set with the C12 to C14 bits. In order to make on-screen displays easy to use, the SAA5290 contains additional display attributes in Column 11.

Control codes are categorized as 'set at' or 'set after'. 'Set at' means the code has effect at the current character position and 'set after' means they have effect from the following character. Codes 11/0 to 11/7 are always 'set at'. Codes 11/11 to 11/15 are 'set after' when defining the start of an OSD box and 'set at' when ending an OSD box. Codes 11/12 to 11/15 force a box condition allowing on-screen display messages to be displayed without having to erase the whole contents of the teletext page.

On-screen displays are only available in TV mode and not in text mode. In mixed text and TV mode the displayed screen is not defined if an OSD box is encountered in the page memory.

Table 16 Display mode

PICTURE ON	TEXT ON	BACKGROUND ON	RESULT
0	0	X	text mode, black screen
0	1	0	text mode, background always black
0	1	1	text mode
1	0	X	TV mode
1	1	0	mixed mode and TV mode
1	1	1	text mode, TV picture outside text area

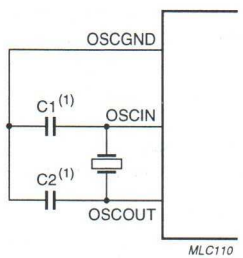
Display timing

The display circuitry is driven from the H/VSYNC inputs, and is independent of the input video signal. Consequently HSYNC and VSYNC are always required to slave synchronize the display.

The FRAME output of the SAA5290 is provided to facilitate de-interlacing the teletext display. The behaviour of FRAME is controlled via the register bits TXT0.DISABLE FRAME, TXT0.AUTO FRAME and TXT1.FIELD POLARITY. If the active edge of VSYNC occurs in the first half of a TV line then the field is even, and if the active edge of VSYNC is in the second half of a line then the field is odd. The active edge is controlled with TXT1.V POLARITY. With TXT0.AUTO FRAME LOW FRAME is HIGH for an odd field and LOW for an even field. With TXT0.AUTO FRAME HIGH FRAME is only active when text is being displayed, when video is displayed it is forced LOW. When TXT0.DISABLE FRAME is HIGH FRAME is always LOW. If TXT1.FIELD POLARITY is logic 1 then VSYNC is delayed by 32 µs before being applied to the display timing circuits.

Clock generator

The oscillator circuit of the SAA5290 is a single-stage inverting amplifier in a Pierce oscillator configuration. The circuitry between OSCIN and OSCOUT is basically an inverter biased to the transfer point. A crystal must be used as the feedback element to complete the oscillator circuitry. It is operated in parallel resonance. OSCIN is the high gain amplifier input and OSCOUT is the output. To drive the SAA5290 externally OSCIN is driven from an external source and OSCOUT is left open-circuit.



(1) The values of C1 and C2 depend on the crystal specification: $C1 = C2 = 2C_L$.

Fig.7 Oscillator circuit.

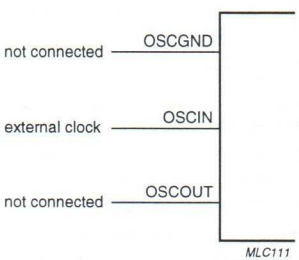


Fig.8 Oscillator circuit driven from external source.

CHARACTER SETS

Fig.9 SAA5290 European character set.

LANGUAGE	PHCB				CHARACTER POSITION (COLUMN / ROW)												
	E/W	C12	C13	C14	2/3	2/4	4/0	5/B	5/C	5/D	5/E	5/F	6/0	7/B	7/C	7/D	7/E
ENGLISH	0	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	0	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	0	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à
TURKISH	0	1	1	0	Ţ	ğ	İ	Ş	Ö	Ç	Ü	Ğ	ı	ş	ö	ç	ü
ENGLISH	0	1	1	1	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
POLISH	1	0	0	0	#	ń	ą	Ż	Ś	Ł	ć	ó	ę	ż	ś	ł	ź
GERMAN	1	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
ESTONIAN	1	0	1	0	#	õ	Š	Ä	Ö	Ž	Ü	Õ	š	ä	ö	ž	ü
GERMAN	1	0	1	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
GERMAN	1	1	0	0	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SERBO-CROAT	1	1	0	1	#	Ë	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECHOSLOVAKIA	1	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN	1	1	1	1	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

MLC109

Fig.10 SAA5290 European national option characters.

APPLICATION INFORMATION

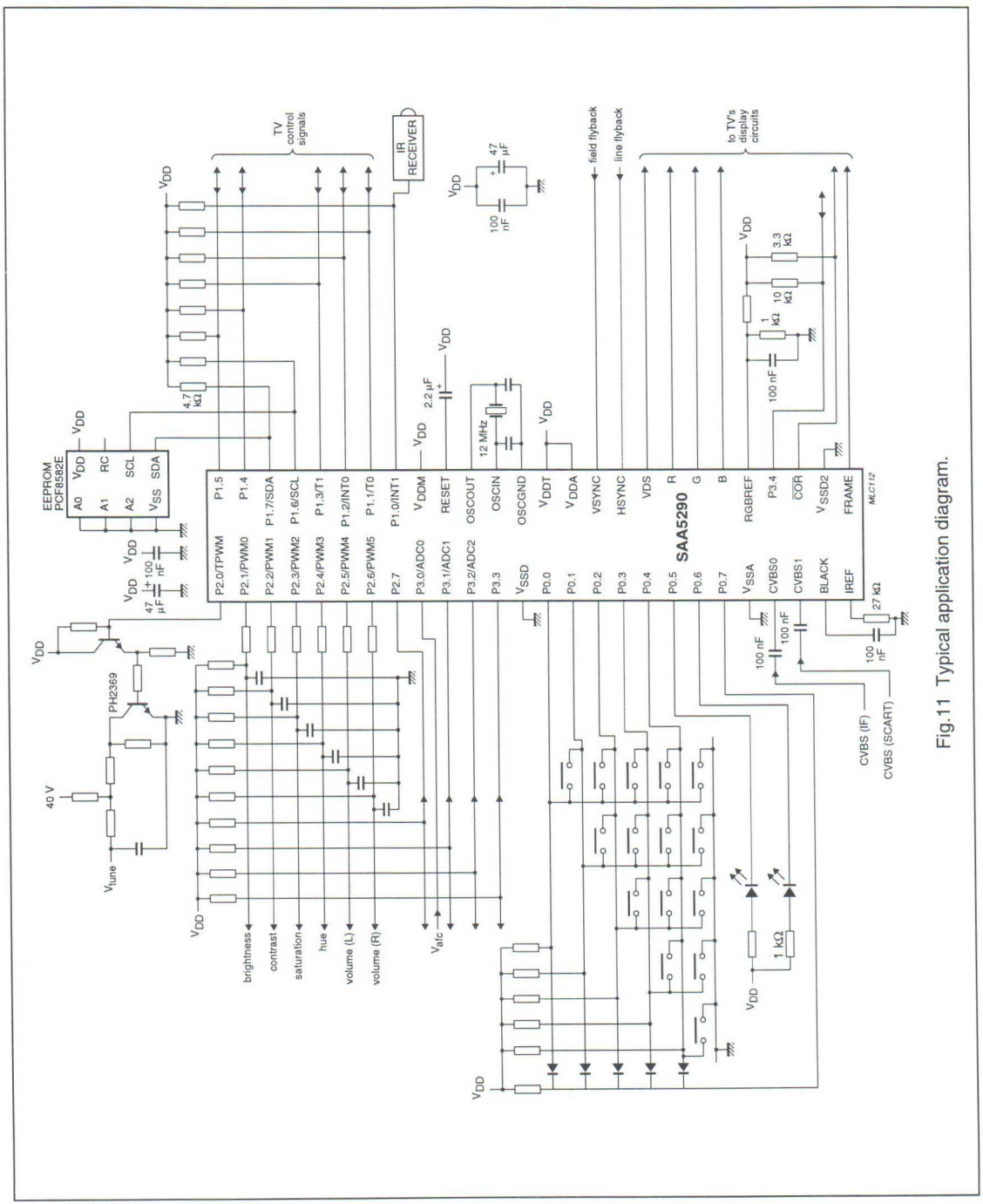


Fig.11 Typical application diagram.

SINGLE-CHIP COLOUR CRT CONTROLLER (FTFROM)

GENERAL DESCRIPTION

The SAA5355 FTFROM (Five-Two-Five-ROM) is a single-chip VLSI NMOS crt controller capable of handling the display functions required for a 525-line, level-3 videotex decoder. Only minimal hardware is required to produce a videotex terminal using FTFROM — the simplest configuration needs just a microcontroller and 4 Kbytes of display memory.

Features

- Minimal additional hardware required
- Screen formats of 40/80 character by 1-to-25 row display
- 512 alphanumeric or graphical characters on-chip or extendable off-chip
- Serial attribute storage (STACK) and parallel attribute storage
- Dynamically redefinable character (DRCS) capability over full field
- Interfaces with 8/16-bit microprocessors with optional direct memory access
- On-chip scroll map minimizes data to be transferred when scrolling
- 32 on-screen colours redefinable from a palette of 4096
- Three on-chip digital-to-analogue converters which compensate for crt non-linearity
- Memory interface capable of supporting multi-page terminals. FTFROM can access up to 128 Kbytes of display memory
- Programmable cursor
- Programmable local status row
- Three synchronization modes:

stand-alone	built-in oscillator operating with an external 6,041957 MHz crystal
simple slave	directly synchronized from the source of text composite sync
phase-locked slave	indirect synchronization allows picture-in-text displays (e.g. VCR/VLP video with text overlay)

- On-chip timing with composite sync output
- Zoom feature which allows the height of any group of rows to be increased to enhance legibility

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).

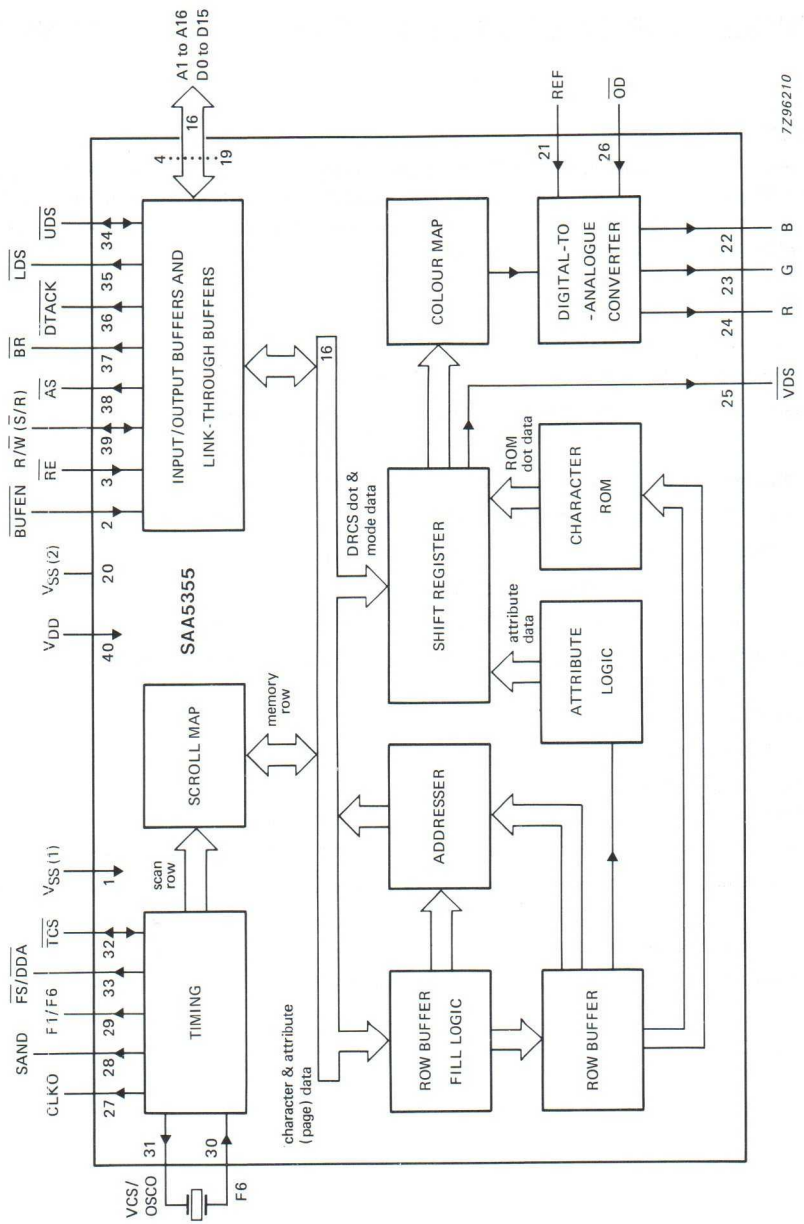


Fig. 1 Block diagram.

PINNING

1	$V_{SS(1)}$	Ground (0 V).
2	$\overline{BUFEN}$	Buffer enable input to the 8-bit link-through buffer.
3	$\overline{RE}$	Register enable input. This enables A1 to A6 and $\overline{UDS}$ as inputs, and D8 to D15 as input/outputs.
4 to 19	A16 to A1/ D15 to D0	Multiplexed address and data bus input/outputs. These pins also function as the 8-bit link-through buffer.
20	$V_{SS(2)}$	Ground (0 V).
21	REF	Analogue reference input.
22	B	Analogue outputs (signals are gamma-corrected).
23	G	
24	R	
25	$\overline{VDS}$	Switching output for dot, screen (row), box and window video data; for use when video signal is present (e.g. from tv, VLP, alpha + photographic layer). This output is LOW for tv display and HIGH for text and will interface directly with a number of colour decoder ICs (e.g. TDA3563, TDA3562A).
26	$\overline{OD}$	Output disable causing R, G, B and $\overline{VDS}$ outputs to go to high-impedance state. Can be used at dot-rate.
27	CLKO	12 MHz clock output for hard-copy dot synchronization (referenced to output dots).
28	SAND	Sandcastle feedback output for SAA5230 teletext video processor or other circuit. Used when the display must be locked to the video source (e.g. VLP). The phase-lock part of the sandcastle waveform can be disabled to allow free-running of the SAA5230 phase-locked loop.
29	F1/F6	1,00699 MHz or 6,041957 MHz output.
30	F6	6,041957 MHz clock input (e.g. from SAA5230). Internal a.c. coupling is provided.
31	VCS/OSCO	Video composite sync input (e.g. from SAA5230) for phase reference of vertical display timing when locking to a video source (e.g. VLP) or, in stand-alone sync mode, output from internal oscillator circuit (fixed frequency).
32	$\overline{TCS}$	Text composite sync input/output depending on master/slave status.
33	$\overline{FS}/\overline{DDA}$	Field sync pulse output or defined-display-area flag output (both referenced to output dots).
34	$\overline{UDS}$	Upper data strobe input/output.
35	$\overline{LDS}$	Lower data strobe output.
36	$\overline{DTACK}$	Data transfer acknowledge (open drain output).
37	$\overline{BR}$	Bus request to microprocessor (open drain output).
38	$\overline{AS}$	Address strobe output to external address latches.
39	$R/\overline{W}$ ($\overline{S}/R$)	Read/write input/output. Also serves as send/receive for the link-through buffer.
40	V_{DD}	Positive supply voltage (+ 5 V).

PINNING (continued)

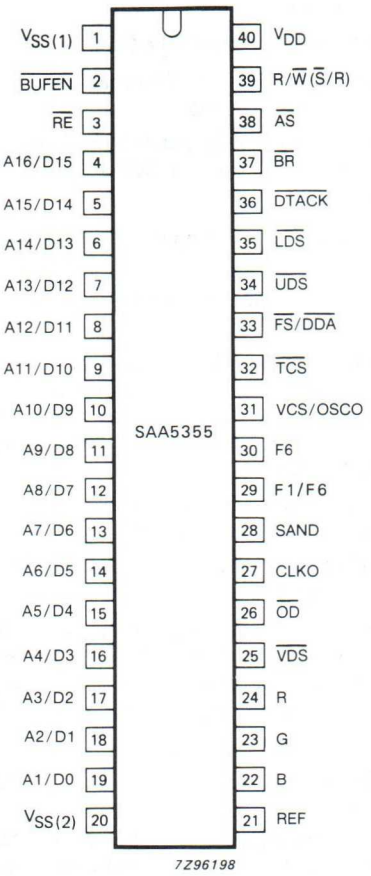


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 40)	V_{DD}	−0,3 to + 7,5 V
Maximum input voltage (except F6, $\overline{TCS}$, REF)	V_{Imax}	−0,3 to + 7,5 V
Maximum input voltage (F6, $\overline{TCS}$)	V_{Imax}	−0,3 to + 10,0 V
Maximum input voltage (REF)	V_{REF}	−0,3 to + 3,0 V
Maximum output voltage	V_{Omax}	−0,3 to + 7,5 V
Maximum output current	I_{Omax}	10 mA
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

Outputs other than CLKO, OSCO, R, G, B, and $\overline{VDS}$ are short-circuit protected.

CHARACTERISTICS

V_{DD} = 5 V ± 5%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 40)	V_{DD}	4,75	5,0	5,25	V
Supply current (pin 40)	I_{DD}	–	–	350	mA
INPUTS					
F6 (note 1)					
Slave modes (Fig. 3)					
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	–	7,0	V
Input peaks relative to 50% duty factor	$\pm V_P$	0,2	–	3,5	V
Input leakage current at V_I = 0 to 10 V; T_{amb} = 25 °C	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	12	pF
Stand-alone mode (Fig. 4)					
Series capacitance of crystal	C_1	–	28	–	fF
Parallel capacitance of crystal	C_0	–	7,1	–	pF
Resonance resistance of crystal	R_r	–	–	60	Ω
Gain of circuit	G	–	–	*	V/V
$\overline{\text{BUFEN}}$, $\overline{\text{RE}}$, $\overline{\text{OD}}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,5	V
Input current at V_I = 0 to V_{DD}+ 0,3 V; T_{amb} = 25 °C	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	7	pF
REF (Fig. 5)					
Input voltage	V_{REF}	0	1 to 2	2,7	V
Resistance (pin 21 to pin 20) with REF supply and R, G, B outputs OFF	R_{REF}	–	125	–	Ω

* Value under investigation.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS					
SAND					
Output voltage high level at I_O = 0 to −10 μA	V_{OH}	4,2	–	V_{DD}	V
Output voltage intermediate level at I_O = −10 to + 10 μA	V_{OI}	1,3	2,0	2,7	V
Output voltage low level at I_O = 0,2 mA	V_{OL}	0	–	0,2	V
Load capacitance	C_L	–	–	130	pF
F1/F6, CLKO, $\overline{DDA}$/$\overline{FS}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
$\overline{LDS}$, $\overline{AS}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF
$\overline{DTACK}$, $\overline{BR}$ (open drain outputs)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	150	pF
Capacitance (OFF state)	C_{OFF}	–	–	7	pF
R, G, B (note 2)					
Output voltage HIGH (note 3) at I_{OH} = −100 μA; V_{REF} = 2,7 V	V_{OH}	2,4	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Output resistance during line blanking	R_{OBL}	–	–	150	Ω
Output capacitance (OFF state)	C_{OFF}	–	–	12	pF
Output leakage current (OFF state) at V_I = 0 to V_{DD}+ 0,3 V; T_{amb} = 25 °C	I_{OFF}	−10	–	+ 10	μA

parameter	symbol	min.	typ.	max.	unit
$\overline{VDS}$					
Output voltage HIGH at $I_{OH} = -250\ \mu A$	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 2$ mA	V_{OL}	0	–	0,4	V
Output voltage LOW at $I_{OL} = 1$ mA	V_{OL}	0	–	0,2	V
Output leakage current (OFF state) at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_{OFF}	−10	–	+ 10	μA
INPUT/OUTPUTS					
VCS/OSCO					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input current (output OFF) at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Load capacitance	C_L	–	–	50	pF
$\overline{TCS}$					
Input voltage HIGH	V_{IH}	3,5	–	10,0	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200$ to $100\ \mu A$	V_{OH}	2,4	–	6,0	V
Output voltage LOW at $V_{OL} = 3,2$ mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
A1/D0 to A16/D15, $\overline{UDS}$, R/$\overline{W}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input current at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200\ \mu A$	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 3,2$ mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TIMING (note 4)					
F6 (Fig. 3)					
Rise and fall times	t_r, t_f	10	–	80	ns
Frequency	f_{F6}	5,9	–	6,1	MHz
CLKO, F1/F6, R, G, B, $\overline{VDS}$ $\overline{FS}$/$\overline{DDA}$, $\overline{OD}$ (notes 5, 6 and Fig. 6)					
CLKO HIGH time	t_{CLKH}	25	–	–	ns
CLKO LOW time	t_{CLKL}	15	–	–	ns
CLKO rise and fall times	t_{CLKr} t_{CLKf}	–	–	10	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ change	t_{VCH}	10	–	–	ns
R, G, B, $\overline{VDS}$ valid to CLKO rise	t_{VOC}	10	–	–	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ valid	t_{COV}	–	–	60	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ floating after $\overline{OD}$ fall	t_{FOD}	0	–	30	ns
Skew between outputs R, G, B, $\overline{VDS}$	t_{VS}	–	–	20	ns
R, G, B, $\overline{VDS}$ rise and fall times	t_{Vr}, t_{Vf}	–	–	30	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ active after $\overline{OD}$ rise	t_{UOD}	0	–	60	ns
CLKO HIGH to $\overline{FS}$/$\overline{DDA}$ change	t_{DCH}	10	–	60	ns
$\overline{FS}$/$\overline{DDA}$ valid to CLKO rise	t_{DOC}	5	–	–	ns
F1 HIGH time (note 7)	t_{F1H}	–	500	–	ns
F1 LOW time (note 7)	t_{F1L}	–	500	–	ns
F6 HIGH time	t_{F6H}	–	83	–	ns
F6 LOW time	t_{F6L}	–	83	–	ns
$\overline{OD}$ to CLKO rise set-up	t_{ODS}	–	–	45	ns
$\overline{OD}$ to CLKO HIGH hold	t_{ODH}	–	–	0	ns
MEMORY ACCESS TIMING (notes 8, 9 and Fig. 7)					
$\overline{UDS}$, $\overline{LDS}$, $\overline{AS}$					
Cycle time	t_{cyc}	–	500	–	ns
$\overline{UDS}$ HIGH to bus-active for address output	t_{SAA}	75	–	–	ns
Address valid set-up to $\overline{AS}$ fall	t_{ASU}	20	–	–	ns
Address valid hold from $\overline{AS}$ LOW	t_{ASH}	20	–	–	ns
Address float to $\overline{UDS}$ fall	t_{AFS}	0	–	–	ns

parameter	symbol	min.	typ.	max.	unit
$\overline{AS}$ LOW to $\overline{UDS}$ fall delay	t_{ATD}	50	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ HIGH time	t_{HDS}	220	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ LOW time	t_{LDS}	200	–	–	ns
$\overline{AS}$ HIGH time	t_{HAS}	125	–	–	ns
$\overline{AS}$ LOW time	t_{LAS}	320	–	–	ns
$\overline{AS}$ LOW to $\overline{UDS}$ HIGH	t_{AUH}	305	–	–	ns
Data valid set-up to $\overline{UDS}$ rise	t_{DSU}	30	–	–	ns
Data valid hold from $\overline{UDS}$ HIGH	t_{DSH}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{AS}$ rise delay	t_{UAS}	0	–	15	ns
$\overline{AS}$ LOW to data valid	t_{AFA}	–	–	275	ns
Link-through buffers					
(notes 8, 9 and Fig. 8)					
$\overline{BUFEN}$ LOW to output valid	t_{BEA}	–	–	100	ns
Link-through delay time	t_{LTD}	–	–	85	ns
Input data float prior to direction change	t_{IFR}	0	–	–	ns
Output float after direction change	t_{OFR}	–	–	60	ns
Output float after $\overline{BUFEN}$ HIGH	t_{BED}	–	–	60	ns
Microprocessor READ from FTFROM					
(Fig. 9)					
R/$\overline{W}$ HIGH set-up to $\overline{UDS}$ fall	t_{RUD}	0	–	–	ns
$\overline{UDS}$ LOW to returned-data access time	t_{UDA}	–	–	210	ns
$\overline{RE}$ LOW to returned data access time	t_{REA}	–	–	210	ns
Data valid to $\overline{DTACK}$ LOW delay	t_{DTL}	40	–	–	ns
$\overline{DTACK}$ LOW to $\overline{UDS}$ rise	t_{DLU}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ fall	t_{UDR}	0	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DSD}	250	–	350	ns
Address valid to $\overline{UDS}$ fall	t_{AUL}	0	–	–	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
MEMORY ACCESS TIMING (continued)					
Microprocessor WRITE to FTFROM (Fig. 10)					
Write cycle time (note 10)	t_{WCY}	500	–	–	ns
R/$\overline{W}$ LOW set-up to $\overline{UDS}$ fall	t_{WUD}	0	–	–	ns
$\overline{RE}$ LOW to $\overline{UDS}$ fall	t_{RES}	30	–	–	ns
Address valid to $\overline{UDS}$ fall	t_{ASS}	30	–	–	ns
$\overline{UDS}$ LOW time	t_{LUS}	100	–	–	ns
Data valid to $\overline{UDS}$ rise	t_{DSS}	80	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DTA}	0	–	60	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ rise	t_{UDW}	0	–	–	ns
F1/F6 to memory access cycle (Fig. 11)					
$\overline{UDS}$ HIGH to F6 (component of F1/F6) rise	t_{UF6}	20	–	–	ns
F6 (component of F1/F6) HIGH to $\overline{UDS}$ rise	t_{F6U}	40	–	–	ns
SYNCHRONIZATION and BLANKING					
$\overline{TCS}$, SAND, $\overline{FS}$/$\overline{DDA}$					
See Fig. 12 for timing relationships and Fig. 13 for vertical sync and blanking waveforms.					

Notes to the characteristics

1. Pin 30 must be biased externally.
2. 16-level analogue voltage outputs.
3. Output voltage guaranteed when programmed for top level.
4. All timings are related to a 6,00 MHz clock.
5. CLKO, R, G, B, F1/F6, $\overline{VDS}$: C_L = 25 pF.
   $\overline{FS}$/$\overline{DDA}$: C_L = 50 pF
6. CLKO, F1/F6, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$: reference levels = 0,8 to 2,0 V
   R, G, B: reference levels = 0,8 to 2,0 V with V_{REF} = 2,7 V
7. These times may momentarily be reduced to a nominal 83 ns in slave-sync mode at the moment of re-synchronization.
8. C_L = 150 pF.
9. Reference levels = 0,8 to 2,0 V.
10. Microprocessor write cycle times of less than 500 ns are permitted but often result in Wait States being generated, the precise timing of $\overline{DTACK}$ will than depend on the internal synchronization time.

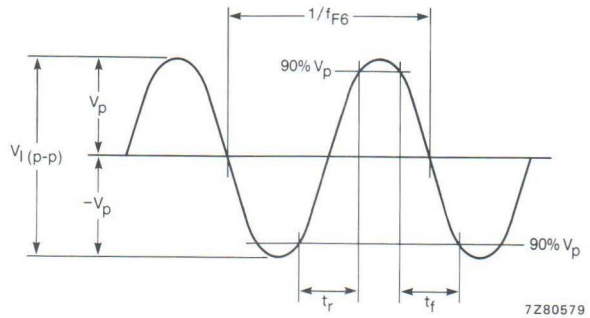
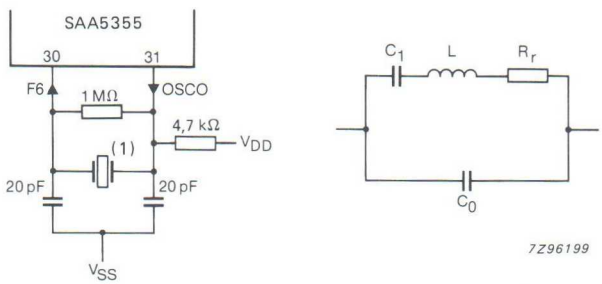


Fig. 3 F6 input waveform.



(1) for 525-line operation, frequency = 6,041957 MHz.

Fig. 4(a) Oscillator circuit for SAA5355 stand-alone sync mode and (b) equivalent circuit of crystal at resonance (see **characteristics** for values).

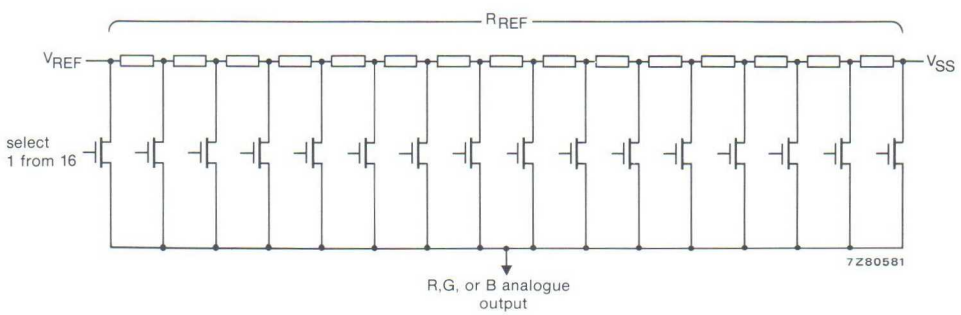


Fig. 5 Circuit arrangement giving one-of-sixteen reference voltage levels for the R, G or B analogue outputs.

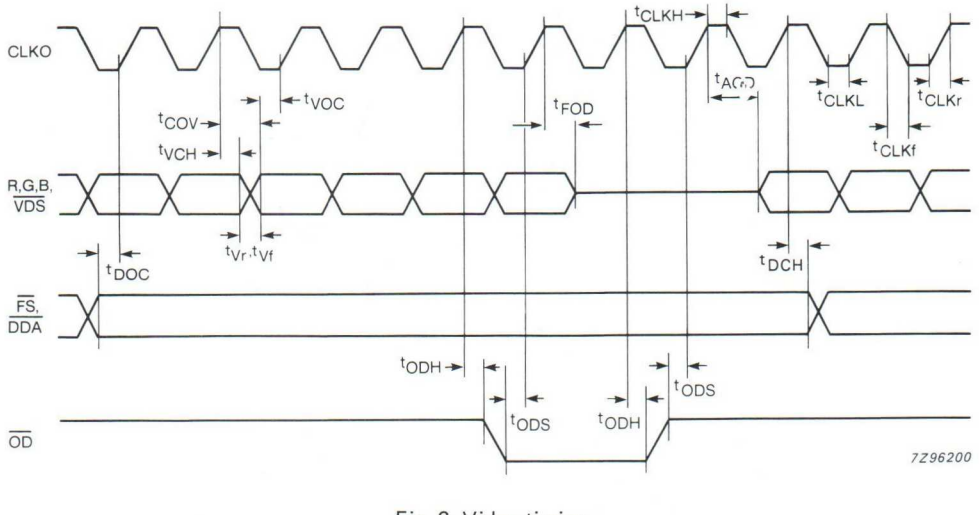


Fig. 6 Video timing.

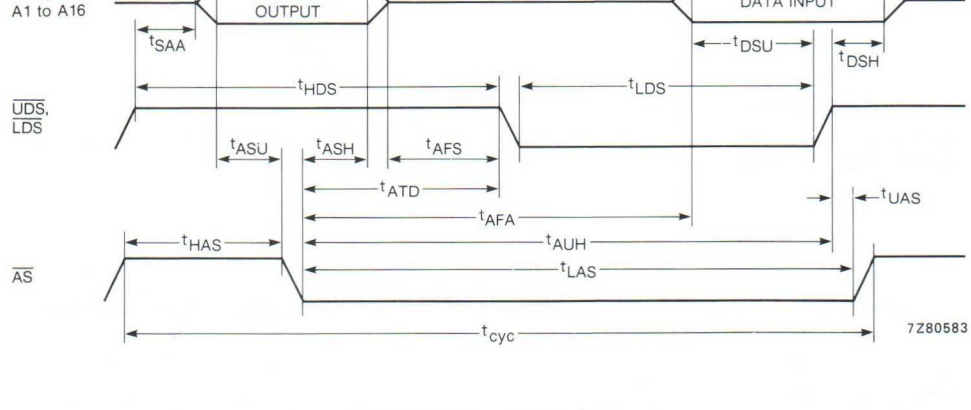


Fig. 7 Memory access timing.

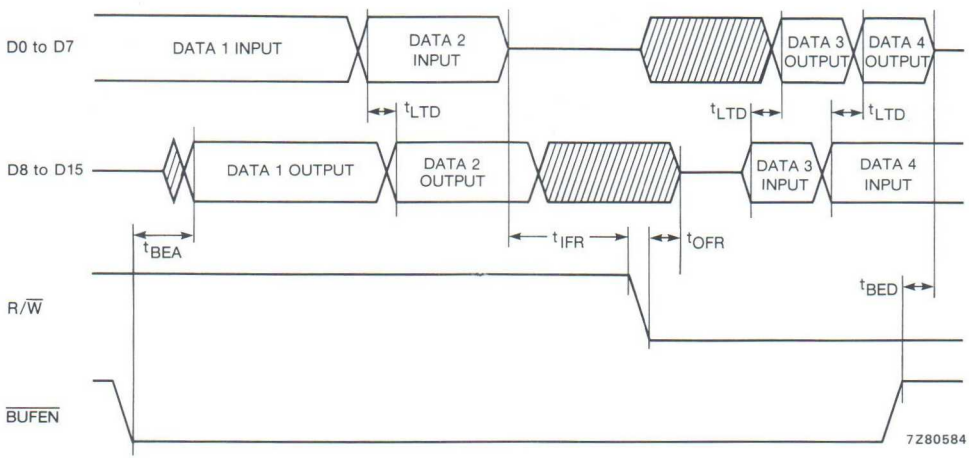


Fig. 8 Timing of link-through buffers.

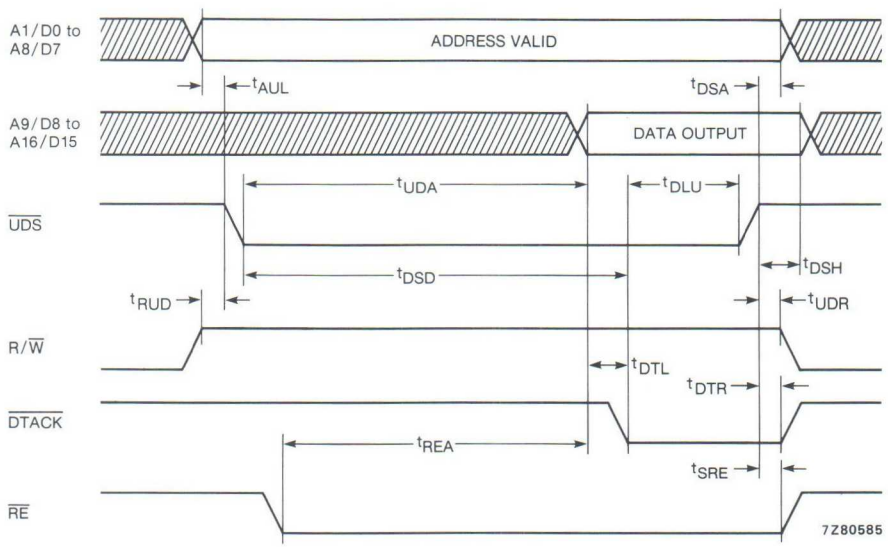


Fig. 9 Timing of microprocessor read from FTFROM.

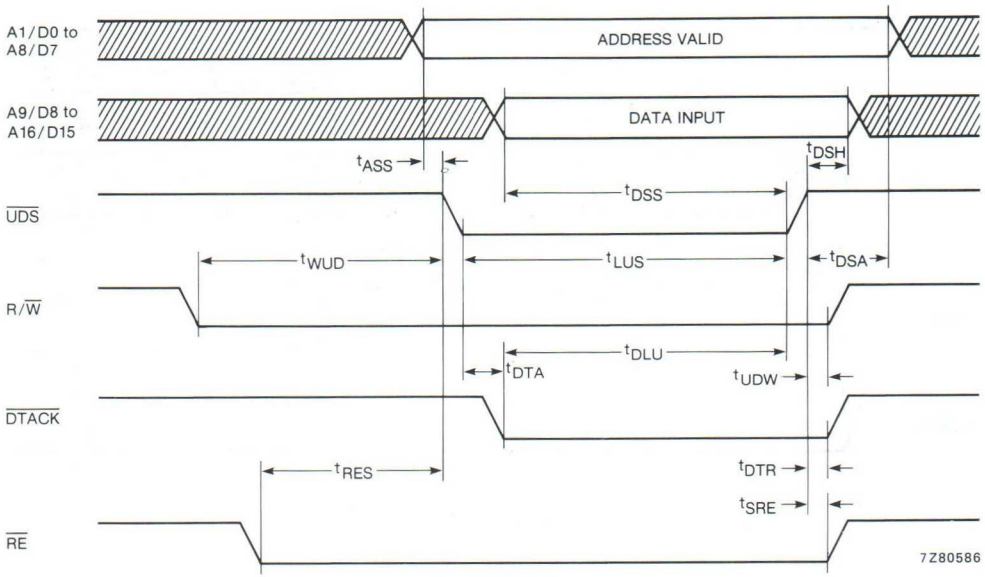


Fig. 10 Timing of microprocessor write to FTFROM.

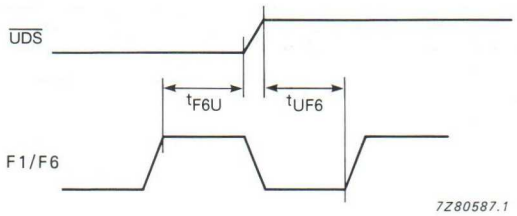


Fig. 11 Timing of F1/F6 to memory access cycle.

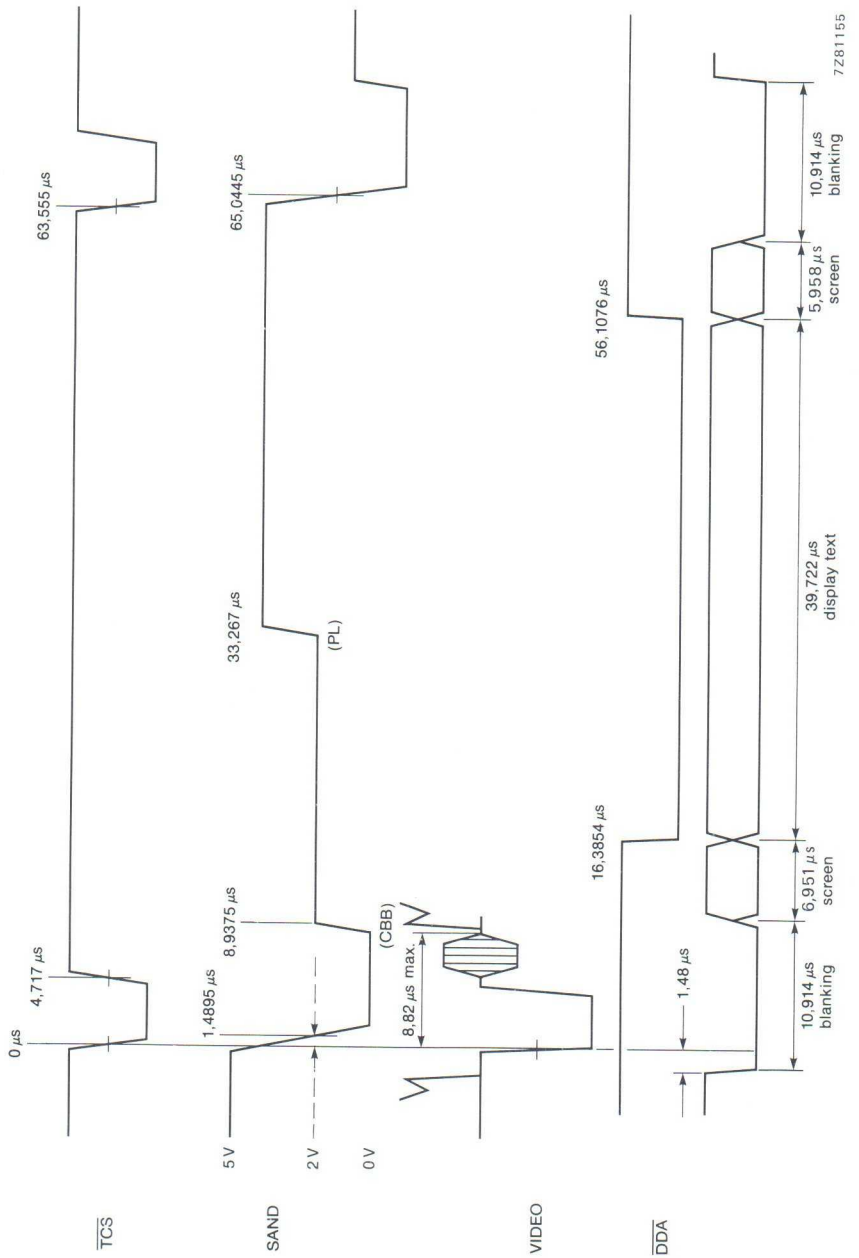


Fig. 12 Timing of synchronization and blanking outputs; all timings are nominal and assume $f_{F6} = 6{,}041957$ MHz.

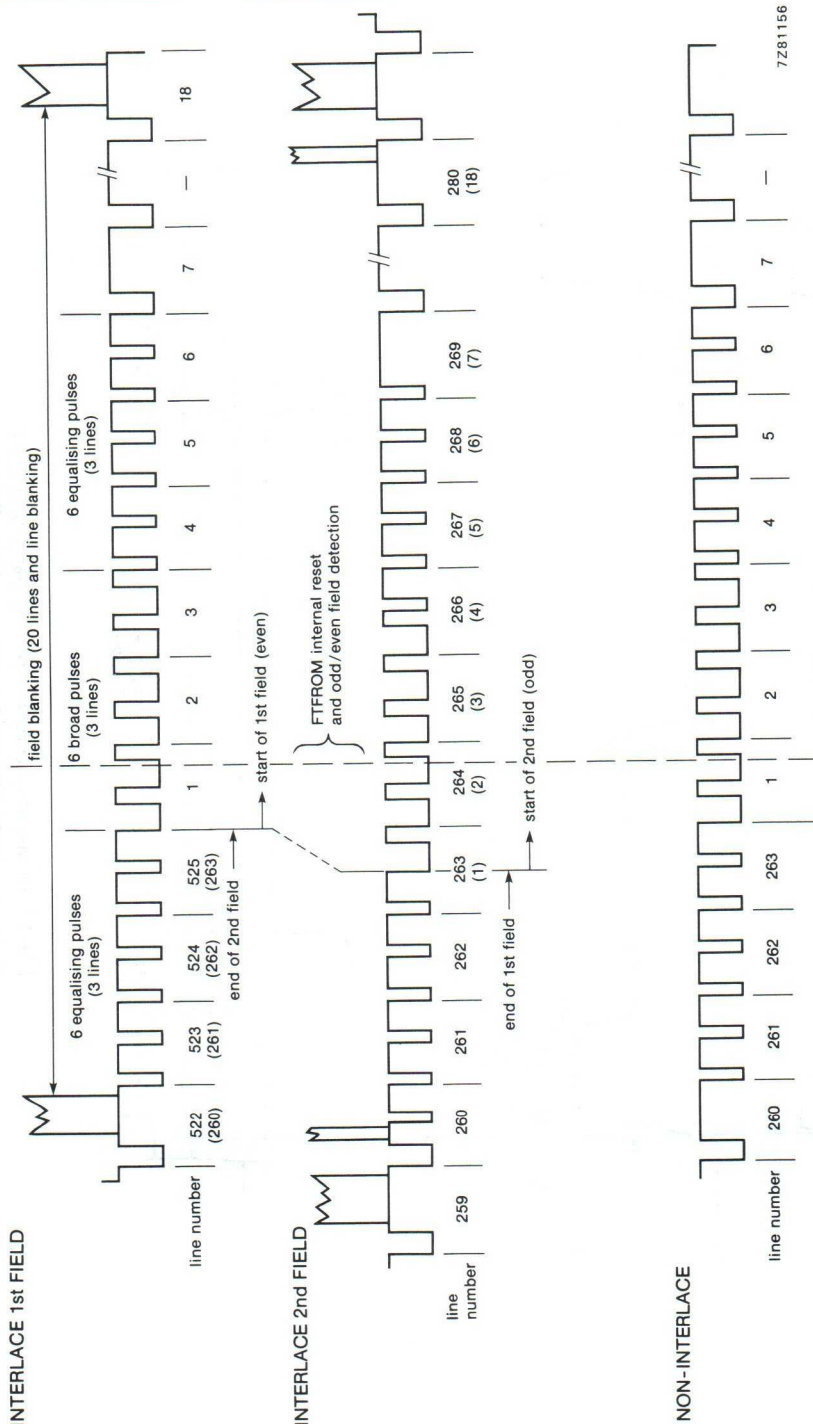


Fig. 13 Vertical synchronization and blanking waveforms; separation of broad pulses = 4,717 μs; equalizing pulse widths = 2,23 μs.

APPLICATION INFORMATION

More detailed application information is available on request

BASIC VIDEOTEX DECODER CONFIGURATION

A basic, practical decoder configuration is shown in Fig. 14, reference should also be made to the block diagram Fig. 1.

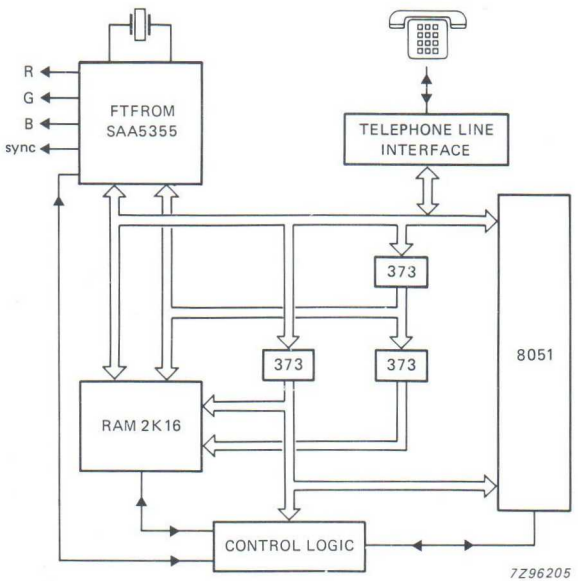


Fig. 14 Basic videotex decoder configuration.

Character and attribute data is fetched from the external memory, processed by the row buffer fill logic according to the stack coding scheme (in stack mode) and then fed into one half of the dual display row buffer. The data fetch process takes place during one line-flyback period (per row) and, since time is required to complete the fill, the other half of the dual row buffer is used for display. The row buffers exchange functions on alternate rows – each holds the 40 columns of 32 bits required to define explicitly every character in a row.

The addresser is used for row buffer filling and for fetching screen colours, and during the display time it is also used for addressing DRCS characters.

Timing

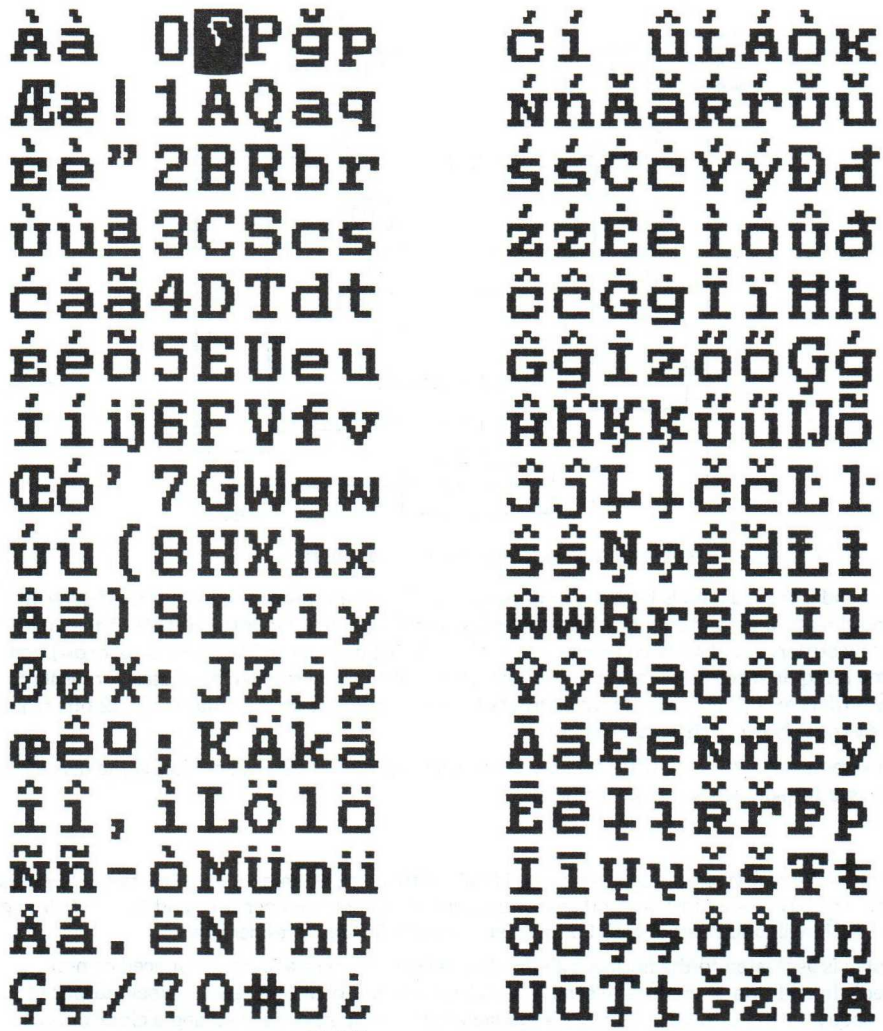
The timing chain operates from an external 6,041957 MHz clock or an on-chip fixed-frequency crystal oscillator. The basic video format is 40 characters per row, 20/21 rows per page and 10 video lines per row. FTFROM will also operate with 25 rows per page and 9 video lines per row.

The display is generated to the normal 525-line/59,94 Hz scanning standard (interlaced or non-interlaced). In addition to composite sync (pin 32) for conventional timebases, a clock output at approximately 1 MHz or 6 MHz (pin 29) is available for driving other devices, and a clock output (pin 27) is available for hard-copy dot synchronization. A defined-display-area timing signal (pin 33) simplifies the application of external peripherals such as a light pen; this signal is nominally coincident with the character dot information.

APPLICATION INFORMATION (continued)

Character generation

FTFROM supports eight character tables, each of (nominally) 128 characters. Four tables are in on-chip ROM and contain fixed characters and four are stored in an external RAM. The fixed character tables (Tables 0 to 3), shown in Figs 15 and 16, are applicable to 10-lines-per-row applications. For 9 lines per row applications, the characters will be as shown but with the last line removed from alpha characters and line 5 (labelling 0 to 9) removed from mosaic and line drawing characters.



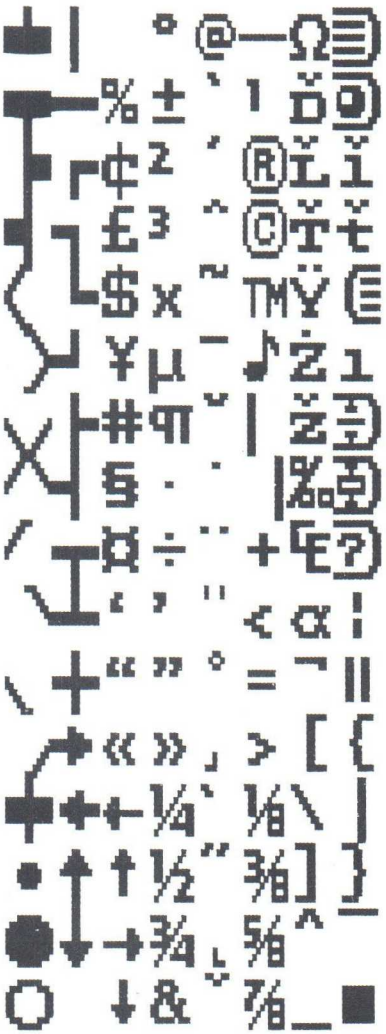
7Z96211

(a)

7Z96212

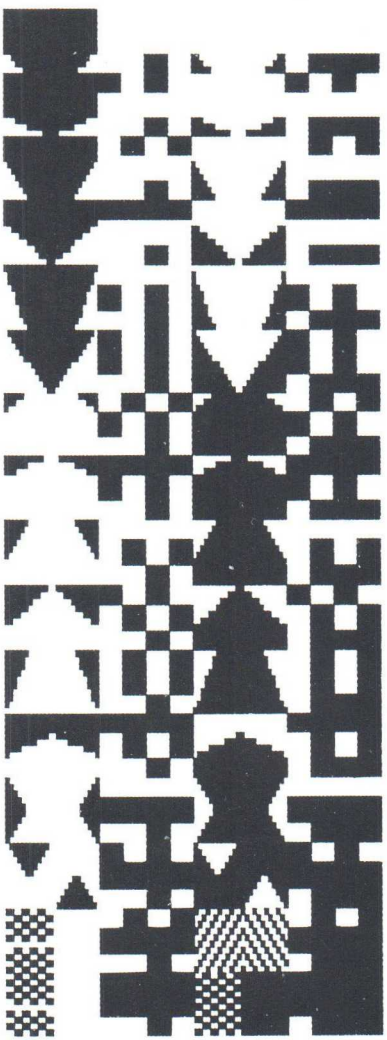
(b)

Fig. 15 On-chip characters: (a) Table 0; (b) Table 1.



7Z96213

(a)



7Z96214

(b)

Fig. 16 On-chip characters: (a) Table 2; (b) Table 3.

APPLICATION INFORMATION (continued)

Character generation (continued)

The 128 most commonly used characters are contained in Table 0, these are the standard upper and lower-case letters of the Roman alphabet, numerals, punctuation and the more common accented characters. In normal text transmission, Table 0 is used most of the time. Table 1 contains other accented characters. Miscellaneous characters, mathematical symbols, the line drawing character set and accents without associated symbols are contained in Table 2. Table 3 contains the block mosaics for the basic alpha-mosaic service and also the new smooth mosaics.

The four tables stored in the external RAM (Tables 4 to 7) are used for DRCS.

Scroll map

The scroll map uses a 26-byte area of on-chip RAM and functions in association with the timing chain. It maps the scan row on to the fetched memory row so allowing the stored page to be displayed in any row order. For each row, a 1-byte pointer to the display memory row is stored in the scroll map. This allows scrolling without the need for data transfer to, or from, side storage.
Additional control bits are stored, allowing 1 to 25 rows to be displayed at any location on the screen.

Colour map and digital-to-analogue converters

The colour map RAM contains thirty-two 12-bit words that are loaded by the microprocessor and read out in three 4-bit groups at pixel rate. Each group is fed to a non-linear (gamma-corrected) D-A converter. The resulting R, G and B outputs are low-impedance with peak-to-peak amplitudes controlled by the reference voltage applied at pin 21.

Cursor

The cursor is available in the stack mode. Its position, character code, character table, foreground colour, background colour, lining and flash attributes are all software programmable via internal register bits.

NON-VIDEOTEX APPLICATIONS

For non-Videotex applications, the device will also support the following operating modes:

Explicit fill mode. An alternative 40 character/rows mode which does not use the memory compression technique of stack coding. More display memory is required but there are no limitations on the number of display attribute changes per row.

80 characters/rows mode. When operating with 80 characters per row, the available display attributes are eight foreground colours, eight (potentially different) background colours (including transparent) as well as underline and blink.

Full field DRCS mode. This mode is not mutually exclusive to the explicit fill and 80 characters/rows modes but rather the available DRCS memory is expanded so that the whole screen can be covered, thus enabling a 'bit map'. All ROM-based characters and all display attributes remain available.

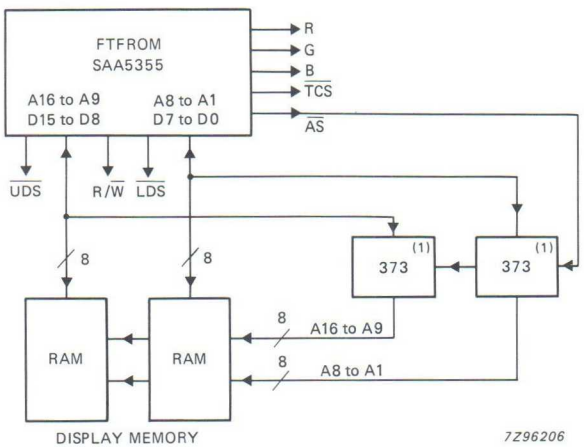
MICROPROCESSOR and RAM BUS INTERFACE

Three types of data transfer take place at the bus interface:

- FTFROM fetches data from the display memory
- The microprocessor reads from, or writes to, FTFROM's internal register map
- The microprocessor accesses the display memory

FTFROM access to display memory (Figs 17 and 18)

FTFROM accesses the external display memory via a 16-bit multiplexed address and data bus with a cycle time of 496,5 ns (F6 = 6,041957 MHz). The address strobe ($\overline{AS}$) signal from FTFROM flags the bus cycle and writes the address into octal latches (74LS373). The display data is stored in bytes of upper (most-significant) and lower (least-significant) display information and is always fetched in pairs of bytes (upper + lower = 16 bits). The upper and lower display RAM sections are enabled simultaneously by the upper and lower data strobes (respectively $\overline{UDS}$ and $\overline{LDS}$) which are always asserted together to fetch a 16-bit word. The read/write control R/$\overline{W}$ is included although FTFROM only reads from the display memory.



(1) 74LS373 octal transparent latch (3-state)

Fig. 17 Simple RAM interface circuit for display memory access.

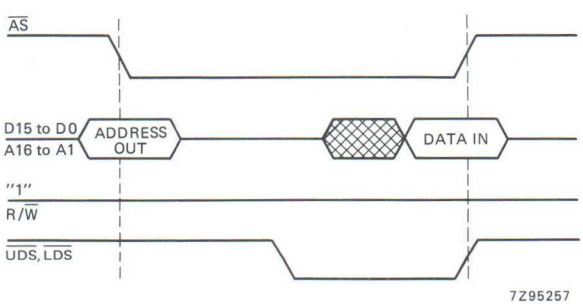


Fig. 18 Bus timing for display memory access.

APPLICATION INFORMATION (continued)

FTFROM access to display memory (continued)

The display memory organization uses the word/byte addressing convention adopted for the SCN68000 microprocessor series. Data fetched on the 16-bit bus is considered in terms of bytes where the even numbered bytes use the upper (most-significant) part of the bus as shown in Fig. 19. The word addresses are numerically the same as the upper byte that they contain – there are no odd-numbered word addresses.

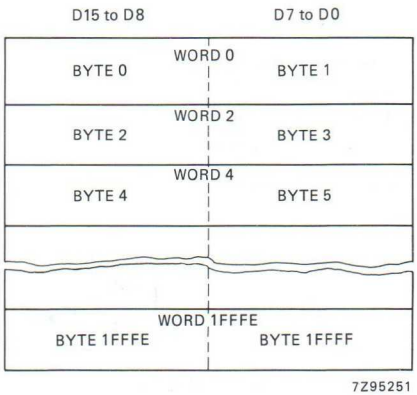


Fig. 19 Display memory word/byte organization.

Warning time

As FTFROM is a real-time display device, it must have direct access to the display memory with priority over the microprocessor and other peripheral devices. This is achieved by FTFROM issuing a bus request ($\overline{BR}$) signal for the duration of the memory access plus a programmable advance warning time which allows the microprocessor to complete its current bus cycle.

In systems where the buses of the microprocessor and FTFROM are intimately connected (connected systems), $\overline{BR}$ may be used to suspend all microprocessor activity so that FTFROM can act as a dedicated DMA controller. In systems where the two buses are separated by buffers (disconnected systems), $\overline{BR}$ may be used either to generate an interrupt or as a direct signal. To these ends, the warning time between the assertion of $\overline{BR}$ and the beginning of FTFROM's bus activity is programmable to be between 0 and 22,84 μs.

Microprocessor access to register map

FTFROM has a set of internal registers which, when memory-mapped, behave as an 8-bit wide RAM connected to the upper part of the data bus (Fig. 20). The control signals $\overline{UDS}$ and R/$\overline{W}$ are reversed to become inputs and the register map is enabled by the signal $\overline{RE}$. Addresses are input via the lower part of the bus. A data transfer acknowledge signal ($\overline{DTACK}$) indicates to the microprocessor that the data transfer is complete.

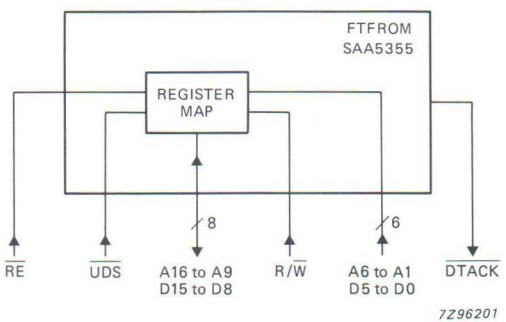


Fig. 20 Microprocessor access to register map.

The main data and address paths used in a connected 68000 interface are shown in Fig. 21. The outputs from the octal latches (74LS373) are enabled only when the 68000 has made the bus available in response to a bus request ($\overline{BR}$). When the register map is accessed data is transferred via the upper part of the bus and the microprocessor's low-order address is passed to FTFROM via the octal buffers (74LS244). At the same time the bidirectional buffers (74LS245) disable the signals from the low order data bus of the 68000.

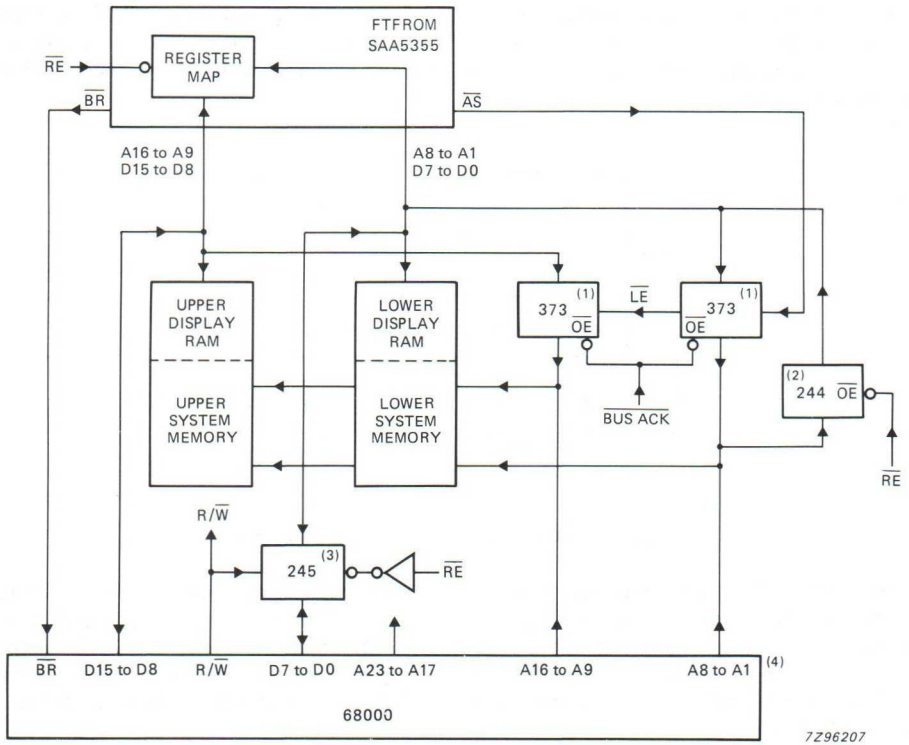
The buffers '244 and '245 may be omitted in a 16-bit write-only configuration where the least-significant data byte is interpreted by FTFROM as an address. Here it will generally be necessary for the microprocessor to hold a (readable) 'master copy' of FTFROM's scroll map contents at a location in its main memory.

8-bit microprocessors

Although the control bus is optimised for the SCN68000 16-bit microprocessor unit, FTFROM will operate with a number of widely differing industry-standard 8, 16 or more-bit microprocessors or microcontrollers (e.g. SCN68008, MAB8051). The interfacing of 8-bit microprocessors to the 16-bit wide display memory is made simple by FTFROM's on-chip link-through buffer which provides the microprocessor with bidirectional access to the lower (odd) half of the memory. The link-through buffer is enabled by the buffer-enable signal $\overline{BUFEN}$, and the send/receive direction is controlled by the signal $\overline{S}$/R.

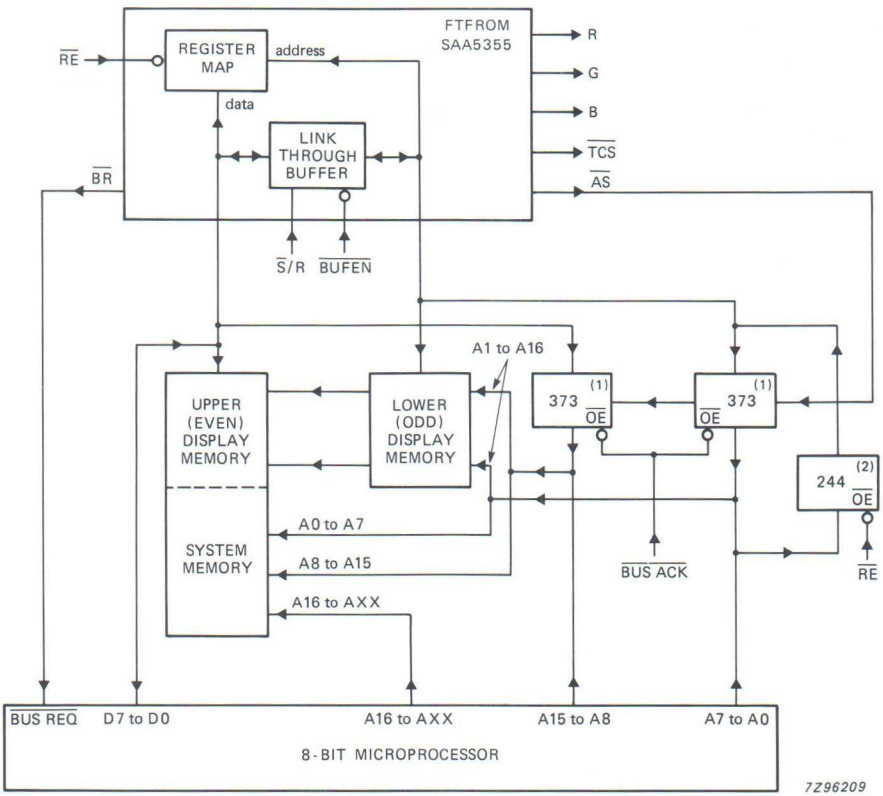
The main data and address paths used in a connected 8-bit microprocessor system are shown in Fig. 22. The interface is similar to that of the 16-bit system but here the display memory does not receive A0 as an address, rather A0 is used as the major enabling signal for $\overline{BUFEN}$ (enables when HIGH).

APPLICATION INFORMATION (continued)



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal transceiver (3-state)
(4) SCN68000 microprocessor unit

Fig. 21 Connected 16-bit microprocessor system.



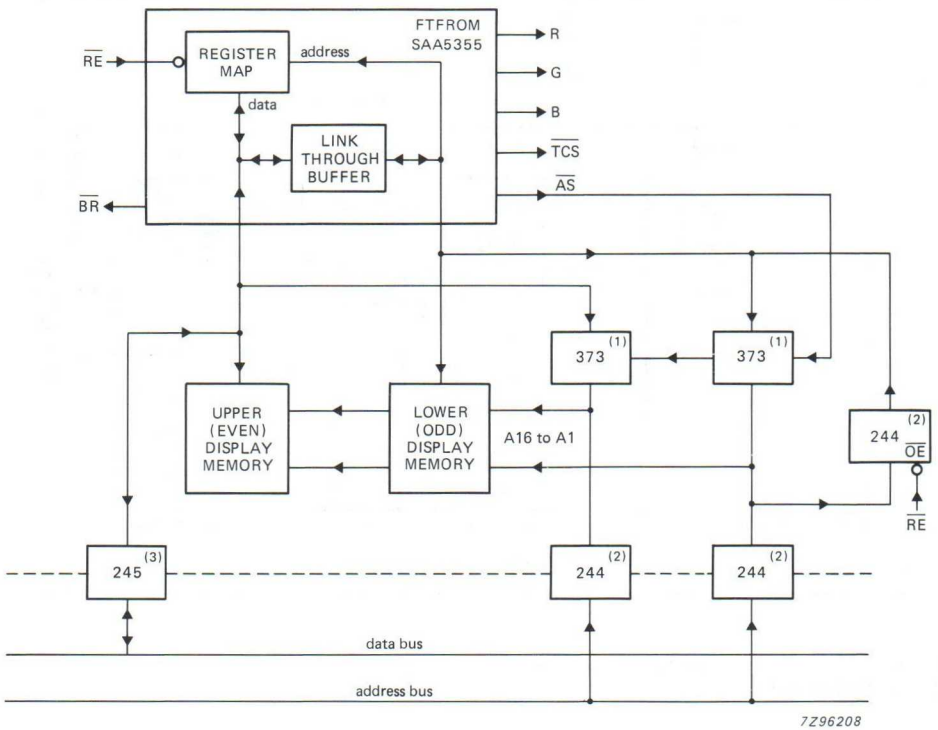
(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)

Fig. 22 Connected 8-bit microprocessor system.

APPLICATION INFORMATION (continued)

Disconnected systems

For many applications it may be desirable to disconnect FTFROM and the display memory from the microprocessor and its ROM, RAM and other peripherals by using isolating buffers as shown in Fig. 23. The two parts of the system then operate independently and communicate only when the microprocessor accesses FTFROM's register map or the display memory.



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal bus transceiver (3-state)

Fig. 23 Disconnected 8-bit system.

Synchronization

Stand-alone mode

As a stand-alone device (e.g. in terminal applications) FTFROM can output a composite sync signal ($\overline{TCS}$) to the display timebase IC or to a monitor. Timing is obtained from a 6,041957 MHz on-chip oscillator using an external crystal as shown in Fig. 24.

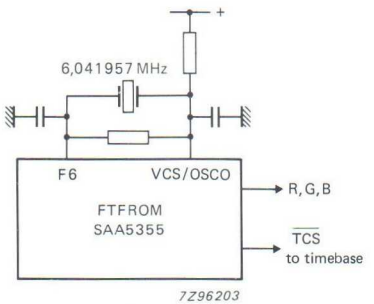


Fig. 24 Stand-alone synchronization mode.

Simple-slave

In the simple-slave mode FTFROM synchronizes directly to another device as shown in Fig. 25. FTFROM's horizontal counter is reset by the falling edge of $\overline{TCS}$. A dead time of 250 ns is built in to avoid resetting the counter at every tv line and so prevents screen jitter.
Field synchronization is made using FTFROM's internal field sync separator.

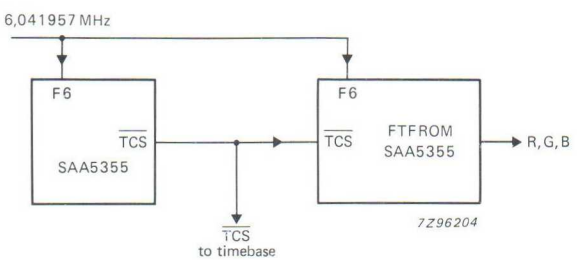


Fig. 25 Simple-slave (direct sync) mode.

APPLICATION INFORMATION (continued)

Synchronization (continued)

Phase-locked slave

The phase-locked slave (indirect sync) mode is shown in Fig. 26. A phase-locked VCO in the SAA5230 teletext video processor provides sync to the timebases. When FTFROM is active, its horizontal counter forms part of the phase control loop – a horizontal reference is fed back to the SAA5230 from the SAND output and a vertical reference is generated by feeding separated composite sync to FTFROM's field sync separator via the VCS input. In the phase-locked slave mode, the display derived from FTFROM can sync with that from a tv source or a local VLP player, thus giving picture-in-text display possibilities.

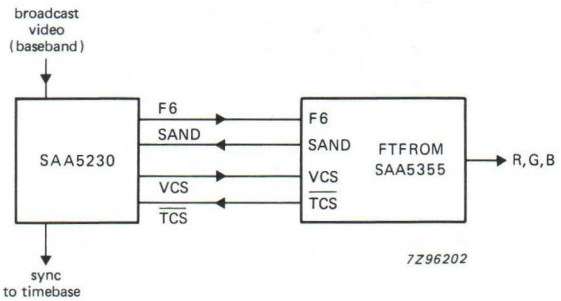


Fig. 26 Phase-locked slave (indirect sync) mode.

Digital multistandard colour decoder with SCART interface (DMSD2-SCART)

SAA7151B

1. FEATURES

- 8-bit performance on chip for luminance and chrominance signal processing for PAL, NTSC and SECAM standards
- Separate 8-bit luminance and 8-bit chrominance input signals from Y/C, CVBS, S-Video (S-VHS or Hi8) sources
- SCART signal insertion by means of RGB/YUV convertion; fast switch handling
- Horizontal and vertical sync detection for all standards
- Real time control output RTCO
- Fast sync recovery of vertical blanking for VCR signals (bottom flutter compensation)
- Controls via the I^2C-bus
- User programmable aperture correction (horizontal peaking)
- Cross-colour reduction by chrominance comb-filtering (NTSC) or by special cross-colour cancellation (SECAM)
- 8-bit quantization of output signals in 4:1:1 or 4:2:2 formats
- 720 active samples per line
- The YUV bus supports a data rate of 13.5 MHz (CCIR 601).
  - ($864 \times f_H$) for 50 Hz
  - ($858 \times f_H$) for 60 Hz
- Compatible with memory-based features (line-locked clock)
- One 24.576 MHz crystal oscillator for all standards

2. GENERAL DESCRIPTION

The SAA7151B is a digital multistandard colour-decoder having two 8-bit input channels, one for CVBS or Y, the other for chrominance or time-multiplexed colour-difference signals.

3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 18, 28, 37 and 52)	4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37 and 52)	-	100	250	mA
V_I	input levels	TTL-compatible			
V_O	output levels	TTL-compatible			
T_{amb}	operating ambient temperature	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7151B	68	mini-pack PLCC	plastic	SOT188

5. BLOCK DIAGRAM

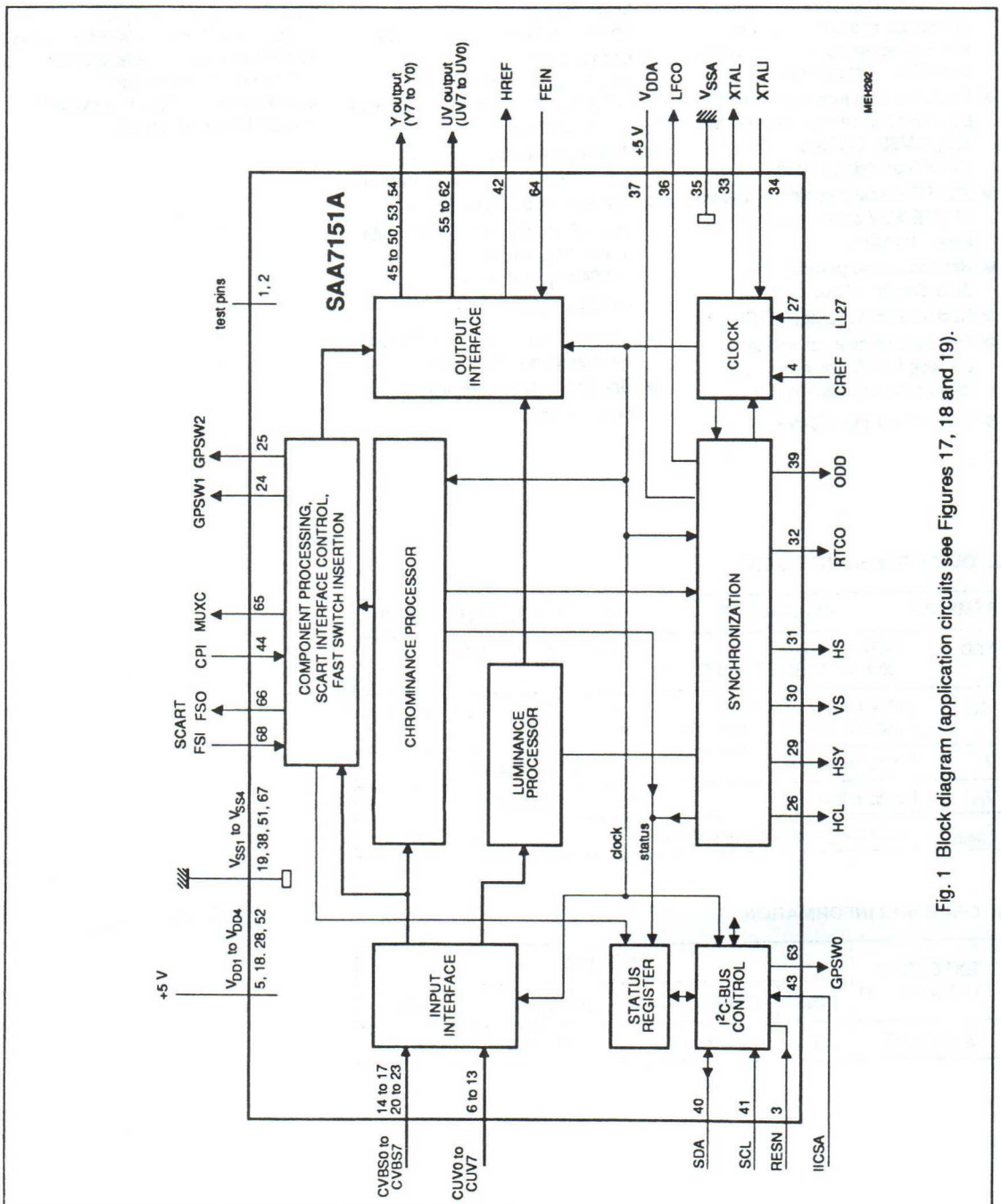


Fig. 1 Block diagram (application circuits see Figures 17, 18 and 19).

6. PINNING

SYMBOL	PIN	DESCRIPTION
SP	1	connected to ground (shift pin for testing)
AP	2	connected to ground (action pin for testing)
RESN	3	reset, active-LOW
CREF	4	clock reference, sync from external to ensure in-phase signals on the Y-, CUV- and YUV-bus
V_{DD1}	5	+5 V supply input 1
CUV0	6	chrominance input data bits CUV7 to CUV0 (digitized chrominance signals in two's complement format from a S-Video source (S-VHS, Hi8) or time-multiplexed colour-difference signals from a YUV(RGB) source or both in combination)
CUV1	7	
CUV2	8	
CUV3	9	
CUV4	10	
CUV5	11	
CUV6	12	
CUV7	13	
CVBS0	14	CVBS lower input data bits CVBS3 to CVBS0 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS1	15	
CVBS2	16	
CVBS3	17	
V_{DD2}	18	+5 V supply input 2
V_{SS1}	19	ground 1 (0 V)
CVBS4	20	CVBS upper input data bits CVBS7 to CVBS4 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS5	21	
CVBS6	22	
CVBS7	23	
GPSW1	24	status bit output FSST0 or port 1 output for general purpose (programmable by subaddress 0C)
GPSW2	25	status bit output FSST1 or port 2 output for general purpose (programmable by subaddress 0C)
HCL	26	black level clamp pulse output (begin and stop programmable), e.g. for TDA8708A (ADC)
LL27	27	line-locked system clock input signal (27 MHz)
V_{DD3}	28	+5 V supply input 3
HSY	29	hor. sync pulse reference output (begin and stop programmable), e.g. for gain adj.TDA8708A (ADC)
VS	30	vertical sync output signal (Fig.10)
HS	31	horizontal sync output signal (Fig.14; start point programmable)
RTCO	32	real time control output; serial increments of HPLL and FSCPLL and status PAL or SECAM sequence (Fig.9)
XTAL	33	24.576 MHz clock output (open-circuit for use with external oscillator)
XTALI	34	24.576 MHz connection for crystal or external oscillator (TTL compatible squarewave)

SYMBOL	PIN	DESCRIPTION
V_{SSA}	35	analog ground
LFCO	36	line frequency control output signal, multiple of horizontal frequency (nominal 6.75 MHz)
V_{DDA}	37	+5 V supply input for analog part
V_{SS2}	38	ground 2 (0 V)
ODD	39	odd/even field identification output (odd = HIGH)
SDA	40	I^2C-bus data line
SCL	41	I^2C-bus clock line
HREF	42	horizontal reference for YUV data outputs (for active line 720Y samples long)
IICSA	43	set module address input of I^2C-bus (LOW = 1000 101X; HIGH = 1000 111X)
CPI	44	clamping pulse input (digital clamping of external UV signals)
Y7	45	Y signal output bits Y7 to Y2 (luminance), part of the digital YUV-bus
Y6	46	
Y5	47	
Y4	48	
Y3	49	
Y2	50	
V_{SS3}	51	ground 3 (0 V)
V_{DD4}	52	+5 V supply input 4
Y1	53	Y signal output bits Y1 to Y0 (luminance), part of the digital YUV-bus
Y0	54	
UV7	55	UV signal output bits UV7 to UV0, part of the digital YUV-bus
UV6	56	
UV5	57	
UV4	58	
UV3	59	
UV2	60	
UV1	61	
UV0	62	
GPSW0	63	port output for general purpose (programmable by subaddress 0D)
FEIN	64	fast enable input (active-LOW to control fast switching due to YUV data; HIGH = YUV high-Z
MUXC	65	multiplexer control output; source select signal for external ADC (UV signal multiplexing)
FSO	66	fast switch and sync insertion output; gated FS signal from FSI or sync insertion pulse in full screen RGB mode
V_{SS4}	67	ground 4 (0 V)
FSI	68	fast switch input signal fed from SCART/peri-TV connector (indicates fast insertion of RGB signals)

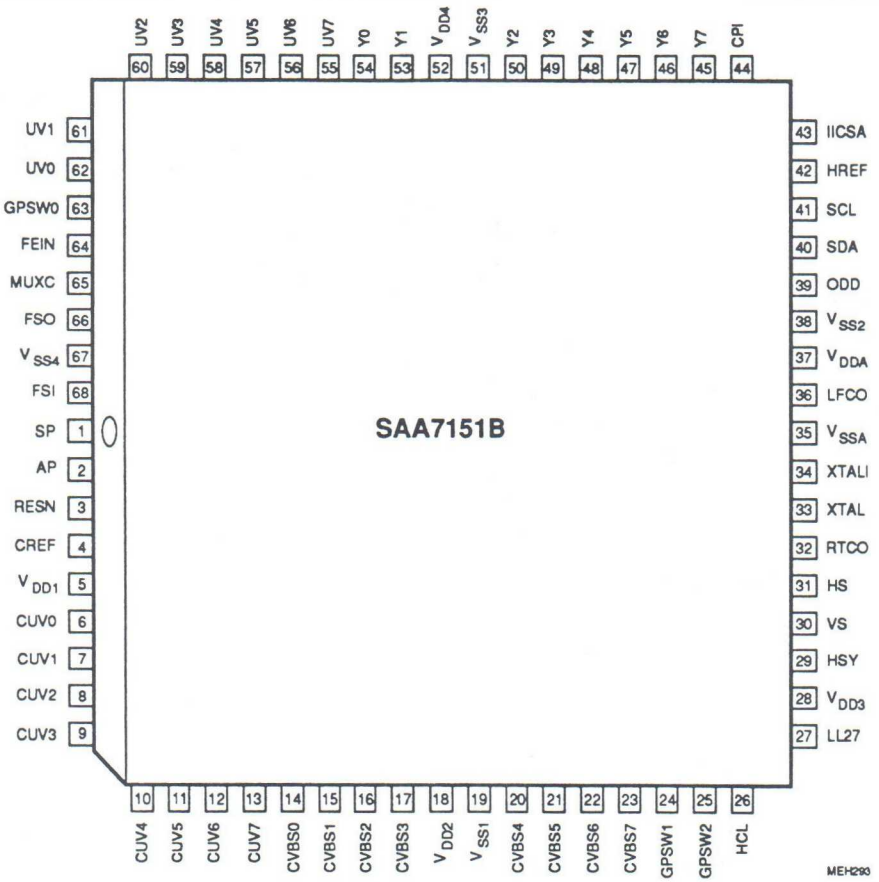


Fig.2 Pin configuration.

7. FUNCTIONAL DESCRIPTION

System configuration

The SAA7151B system processes digital TV signals with line-locked clock in PAL, SECAM and NTSC standards (CVBS or S-Video) as well as RGB signals coming from a SCART/peri-TV connector. The different source signals are switched, if necessary matrixed and converted (Fig.3 and Table 1).
8-bit CVBS data (digitized composite video) and 8-bit UV data (digitized chrominance and/or time-multiplexed colour-difference signals) are fed to the SAA7151B. The data rate is 27 MHz.

Chrominance processing

The 8-bit chrominance input signal (signal "C" out of CVBS or Y/C in Fig.4a) is fed via the input interface to a bandpass filter for eliminating the DC component, then to the quadrature demodulator. Subcarrier signals from the local oscillator (DTO1) with 90 degree phase shift are applied to its multiplier inputs. The frequency depends on set TV standard.

The multipliers operate as a quadrature demodulator for all PAL and NTSC signals; it operates as a frequency down-mixer for SECAM signals.
The two multiplier output signals are converted to a serial UV data stream and applied to two low-pass filter stages, then to a gain controlled amplifier. A final multiplexed low-pass filter achieves, together with the preceding stages, the required bandwidth performance.
The from PAL and NTSC originated signals are applied to a comb-filter. The signals, originated from SECAM, are fed through a cloche filter (0 Hz centre frequency), a phase demodulator and a differentiator to obtain frequency-demodulated colour-difference signals.

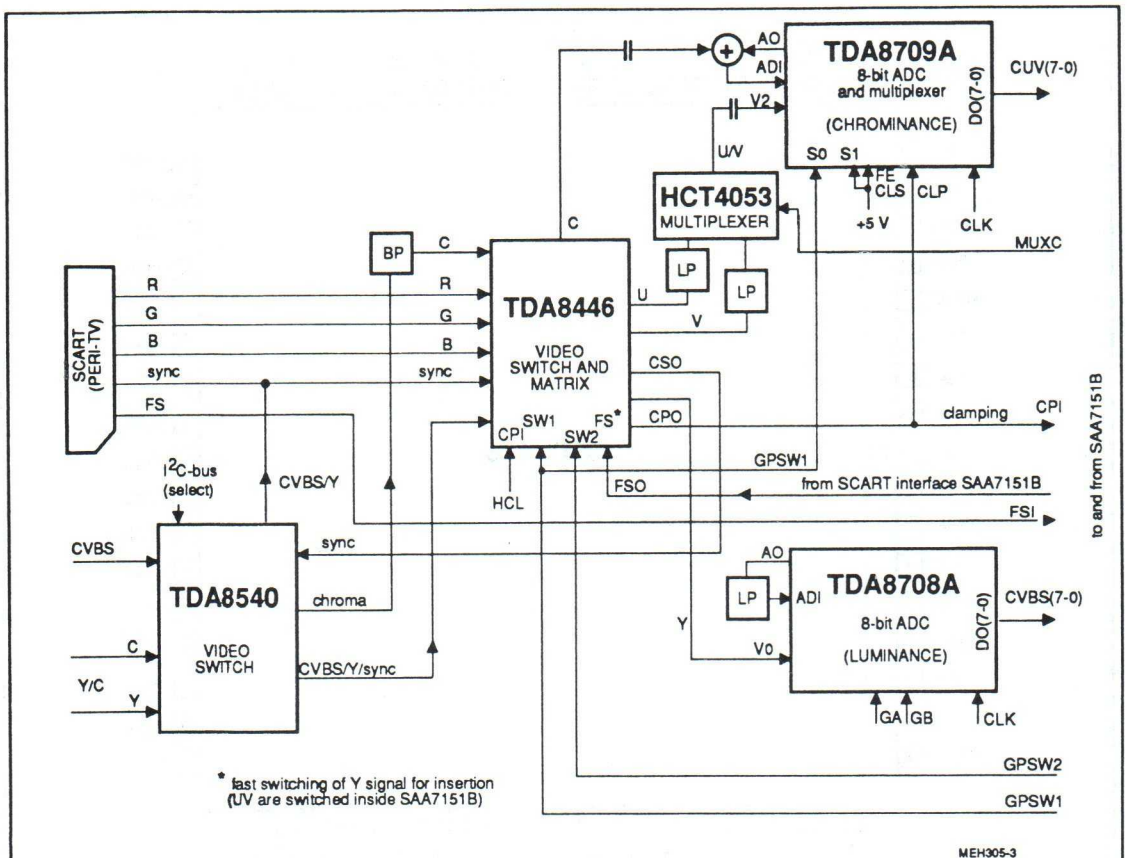


Fig.3 System configuration, RGB fast switch interface included (SCART).

The SECAM signals are fed after de-emphasis to a cross-over switch, to provide the both serial-transmitted colour-difference signals. These signals are finally fed via the fast switch to the output formatter stages and to the output interface. Chrominance signals are output in parallel (4:2:2) on the YUV-bus. The data rate of Y signal (pixel rate) is 13.5 MHz. UV signals have a data rate of 13.5 MHz/2 for the 4:2.2 format (Table 2) respectively 13.5 MHz/4 for the 4:1.1 format (Table 3)

Component processing and SCART interface control

The 8-bit multiplexed colour-difference input signal (signal CUV, Fig.1, out of matrixed RGB in Fig.3) is fed via the input interface to a chrominance stop filter (UV signal only can pass through; Figures 20 to 22). Here it is clamped and fed to the offset compensation which can be enabled or disabled via the I²C-bus.

For matrixed RGB signals – the full screen SCART mode and the fast insertion mode (blanking/switching) are selectable. The chrominance stop filter is automatically bypassed in full screen SCART mode.

Full screen RGB mode (SCART):

The CUV digital input signal (7-0) consists of time-multiplexed samples for U and V. An offset correction for both signals is applied to correct external clamping errors. An internal timing correction compensates for slight differences in timing during sampling. The U and V signals are delay-compensated and fed to the output formatter. The format 4:2:2 or 4:1:1 is generated by a switchable filter.

The control signals for the front end (Figures 3 and 18) MUXC, status bits FSST1, FSST0 (outputs GPSW2, GPSW1) and FSO are generated by the SAA7151B.

Table 1 SCART interface control (Fig.3)

MODE	CONNECTION FSO	GPSW 2	GPSW 1	MUXC	chroma output of TDA8446 to TDA8709A	TDA8709A selected input	CUV (7-0)	luminance fast switch TDA8446	input selector (via I²C-bus) TDA8540
RGB only	0	0	0	0	high-Z	VIN2	U/V	sync (RGB)	sync (RGB)
	0	0	0	1					
Y/C or CVBS only	0	0	1	0	C	VIN1	C	Y (Y/C) or CVBS	Y (Y/C) or CVBS
	0	0	1	1					
Fast switch	0	1	0	0	C	VIN2	0.5(C+U)/ 0.5(C+V)	Y (Y/C) or CVBS	Y (Y/C) or CVBS
	0	1	0	1					
	0	1	1	0	not used				
	0	1	1	1					
RGB only	1	0	0	0	high-Z	VIN2	U/V	Y (RGB)	sync (RGB)
	1	0	0	1					
	1	0	1	0	not used				
	1	0	1	1					
Fast switch	1	1	0	0	C	VIN2	0.5(C+U)/ 0.5(C+V)	Y (RGB)	Y (Y/C) or CVBS
	1	1	0	1					
	1	1	1	0	not used				
	1	1	1	1					

Fast insertion mode:

Fast insertion is applied by FSI pulse to ensure correct timing. The RGB source signal is matrixed into UV and inserted into the CVBS or Y/C source signal after two field periods if FSI pulses are received. The output FSO is set to HIGH during a determined insertion window (screen plain minus 6 % of horizontal and vertical deflection). Switch over depends on the phase of FSI in relation to the valid pixel sequence depending on the phase-different weighting factors. They are applied to the original and the inserted UV data (Figures 5 and 6)
The control signals for the front end (Table 1) MUXC, FSO, status bits FSST1 and FSST0 (outputs GPSW2 and GPSW1) are generated by the SAA7151B .

The amplitude of chrominance and colour-difference signals are scaled down by factor 2 to avoid overloading of the chrominance analog-to-digital converter. The amplitudes are reduced in the TDA8446 by signals on lines GPSW2 and GPSW1.

Luminance processing

The luminance input signal, a digital CVBS format or an 8-bit luminance format (S-Video), is fed through a sample rate converter to reduce the data rate to 13.5 MHz (Fig.4b).

Sample rate is converted by means of a switchable pre-filter. High frequency components are emphasized to compensate for loss in the following chrominance trap filter. This chrominance trap filter (f_o = 4.43 MHz or f_o = 3.58 MHz centre frequency selectable) eliminates the most of the colour carrier signal, therefore, it must be bypassed for S-Video signals.

The high frequency components of the luminance signal can be "peaked" in two bandpass filters with selectable transfer characteristic. A coring circuit (±1 LSB) can improve the signal , this signal is then added to the original signal. A switchable amplifier achieves a common DC amplification, because the DC gains are different in both chrominance trap modes. Additionally, a cut-off sync pulse is generated for the original signal in both modes.

Synchronization

The luminance output signal is fed to the synchronization stage. Its bandwidth is reduced to 1 MHz in a low-pass filter (sync pre-filter). The sync pulses are sliced and fed to the phase detectors to be compared with the sub-divided clock frequency. The resulting output signal is applied to the loop filter to

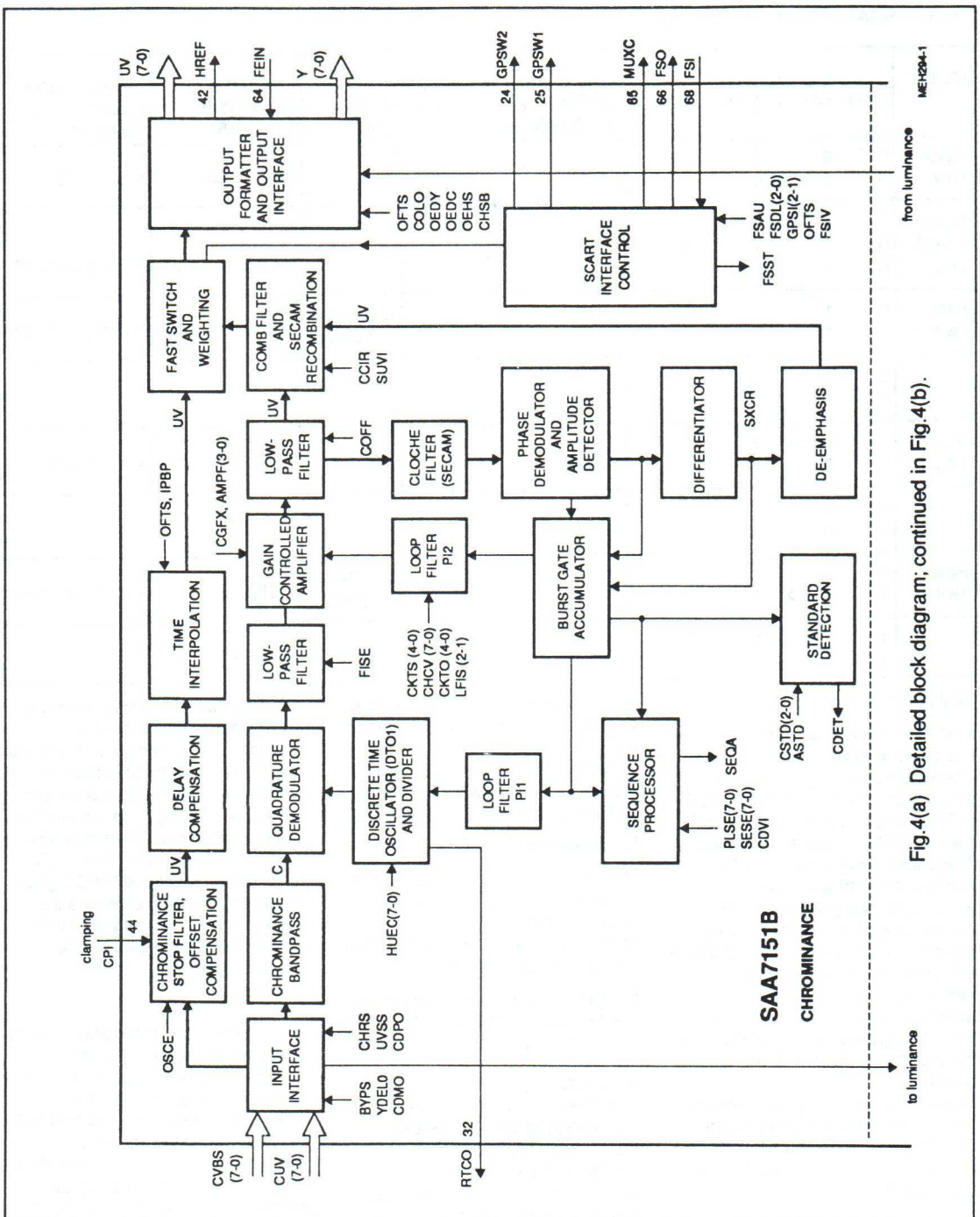


Fig.4(a) Detailed block diagram; continued in Fig.4(b).

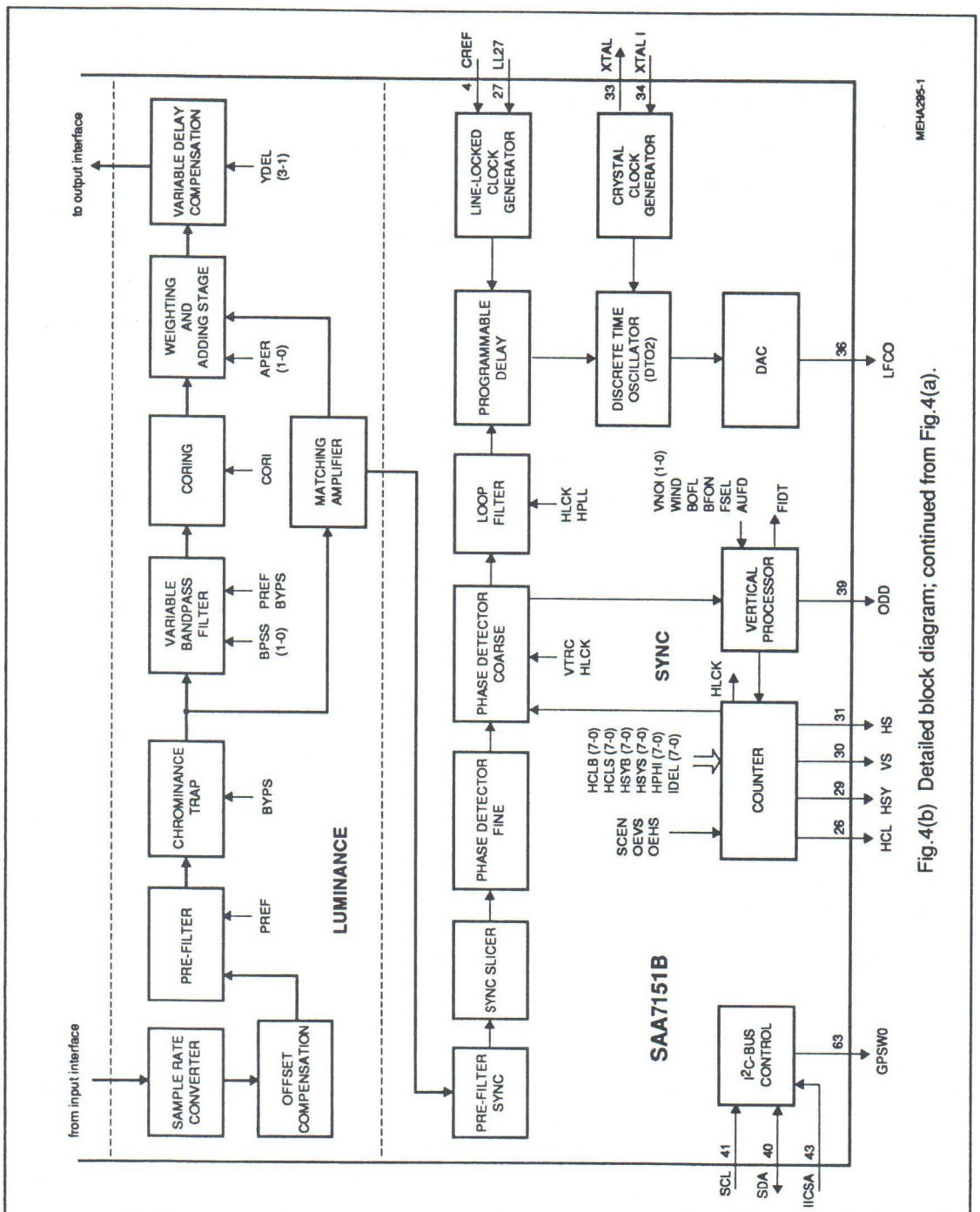


Fig.4(b) Detailed block diagram; continued from Fig.4(a).

accumulate all phase deviations. There are three groups of output timing signals:

a. signals related to data output signals (HREF)
b. signals related to the input signals (HSY, and HCL)
c. signals related to the internal sync phase

All horizontal timings are derived from the main counter, which represents the internal sync phase. The HREF signal only with its critical timing is phase-compensated in relationship to the data output signal. Future circuit improvements could slightly influence the processing delays of some internal stages to achieve a changed timing due to the timing groups b and c.
The HREF signal only controls the data multiplexer phase and the data output signals.

All timings of the following diagrams are measured with nominal input signals, for example coming from a pattern generator. Processing delay times are taken between input and data output, respectively between internal sync reference (main counter = 0) and the rising edge of HREF.

Line locked clock frequency

LFCO is required in an external PLL (SAA7157) to generate the line-locked clock frequency LL27 and CREF.

YUV-bus, digital outputs

The 16-bit YUV-bus transfers digital data from the output interfaces to a feature box, or to the digital-to-analog converter (DAC). Outputs are controlled via the I²C-bus in normal selections, or they are controlled by output enable chain (FEIN, pin 64). The YUV-bus data rate 13.5 MHz. Timing is achieved by marking each second positive rising edge of the clock LL27 synchronized by CREF.

YUV-bus formats
4 : 2 : 2 and 4 : 1 : 1

The output signals Y7 to Y0 are the bits of the digital luminance signal. The output signals UV7 to UV0 are the bits of the digital colour-difference signal. The frames in the Tables 2 and 3 are the time to transfer a full set of samples. In case of 4 : 2 : 2 format two luminance samples are transmitted in comparision to one U and one V sample within one frame. The time frames are controlled by the HREF signal, which determines the correct UV data phase. The YUV data outputs can be enabled or set to 3-state position by means of the FEIN signal. FEIN = LOW enables the output; HIGH on this pin forces the Y and U/V outputs to a high-impedance state (Fig,5).

Table 2 for the 4 : 2 : 2 format (720 pixels per line). The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

OUTPUT	PIXEL BYTE SEQUENCE					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7(MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Table 3 for the 4 : 1 : 1 format (720 pixels per line). The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

OUTPUT	PIXEL BYTE SEQUENCE							
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7 (MSB)	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			

Signal levels (Figures 11 and 12)

The nominal input and output signal levels are defined by a colour bar signal with 75 % colour, 100 % saturation and 100 % luminance amplitude (EBU colour bar).

CUV-bus input format

The CUV-bus transfers the digital chrominance/colour-difference signals from the ADC to the SAA7151B (Fig.5; Table 1):

- normal mode for digital chrominance transmission.
- UV colour-difference mode for colour-difference signals UV (out of matrixed RGB signals)
- FS mode (fast switch mode; UV inserted into chrominance signal C with addition of the two signal spectra).

RTCO output

The RTCO output signal (Fig.9) contains serialized information about actual clock frequency, subcarrier frequency and PAL/SECAM sequence. This signal may preferably be used with the frequency-locked digital video encoder SAA7199B.

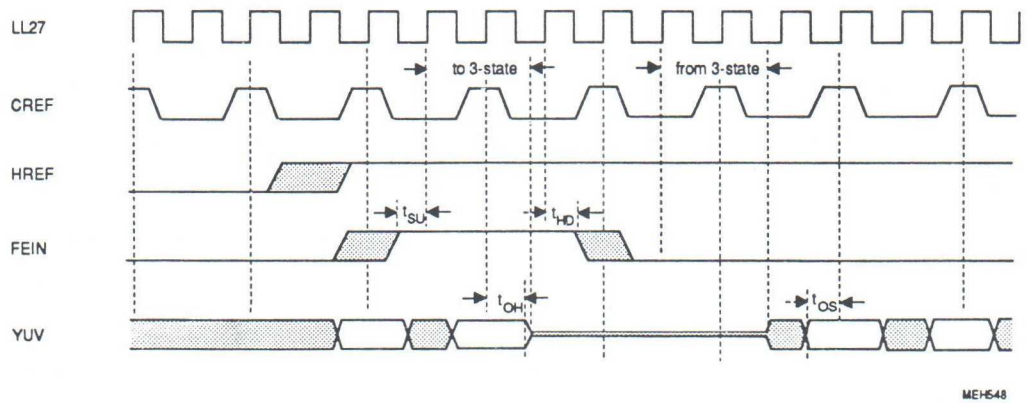


Fig.5 Timing example of fast enable input (FEIN).

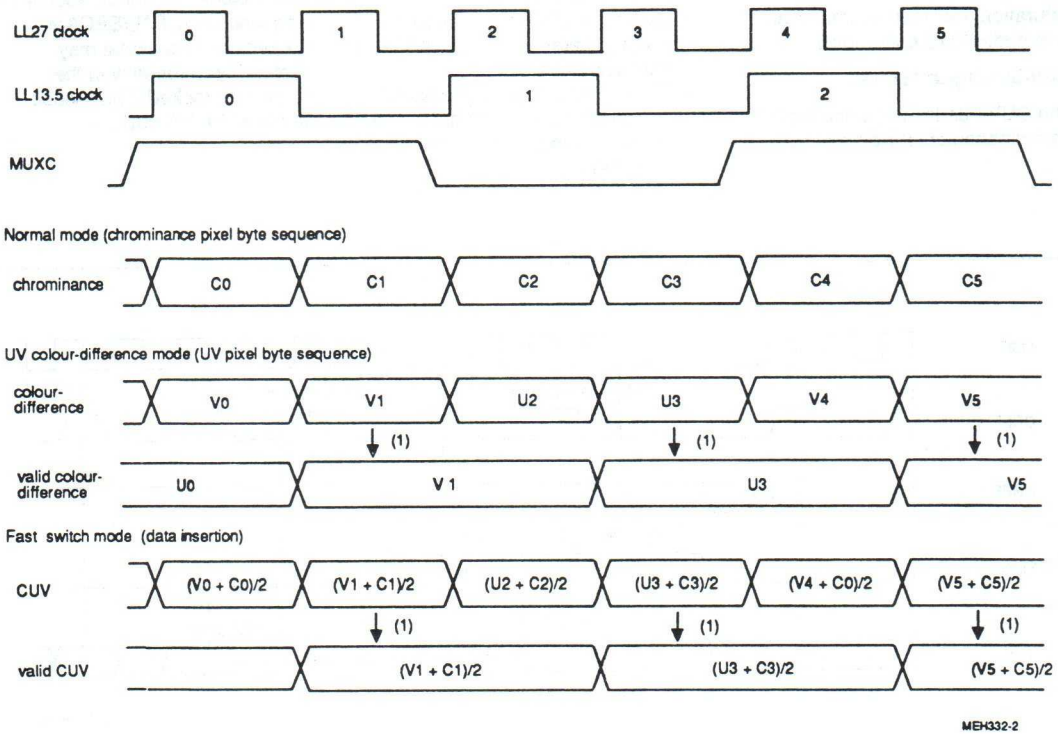


Fig.6 CUV input formats.
(1) each second sample only after a MUXC change is taken for down-sampling to 13.5 MHz to reduce cross-talk components between U and V signals.

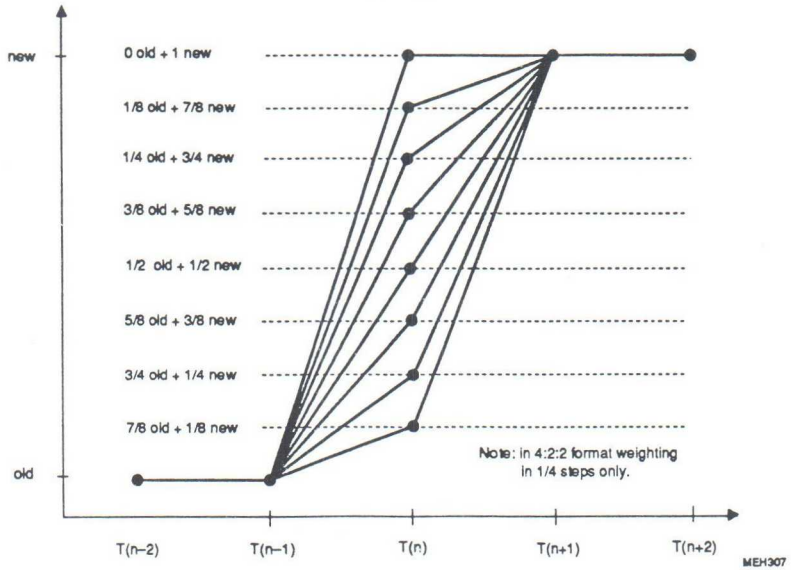


Fig.7 Addition of weighted components.

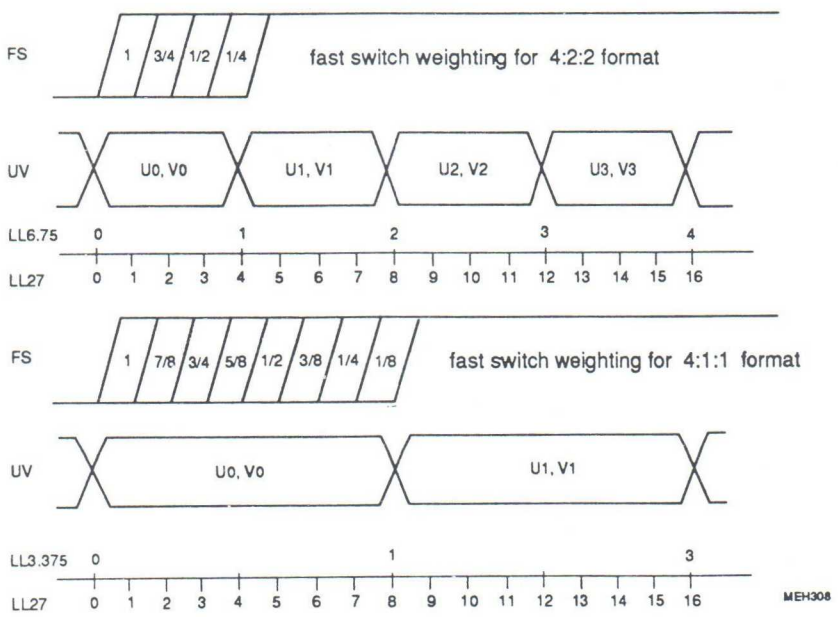


Fig.8 Weighting factors of fast switching for 4:2:2 and 4:1:1 formats.

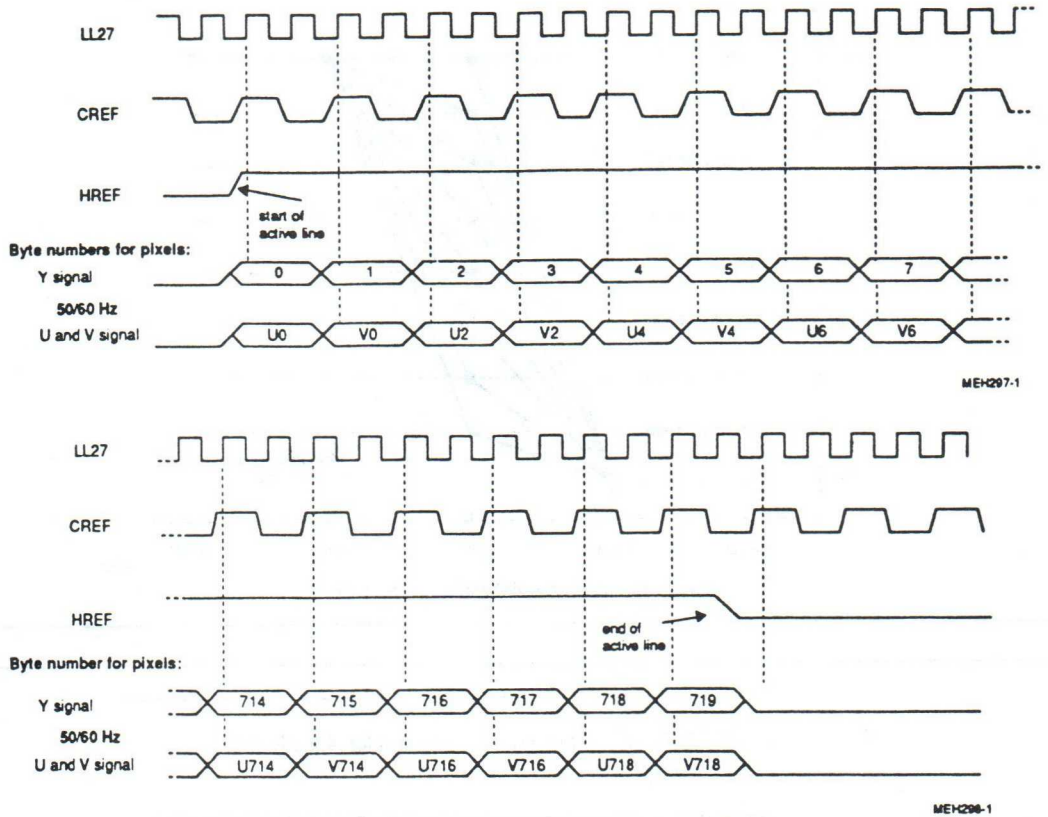


Fig.9 Line control by HREF in 4:2:2 format for 50 Hz and 60 Hz systems.

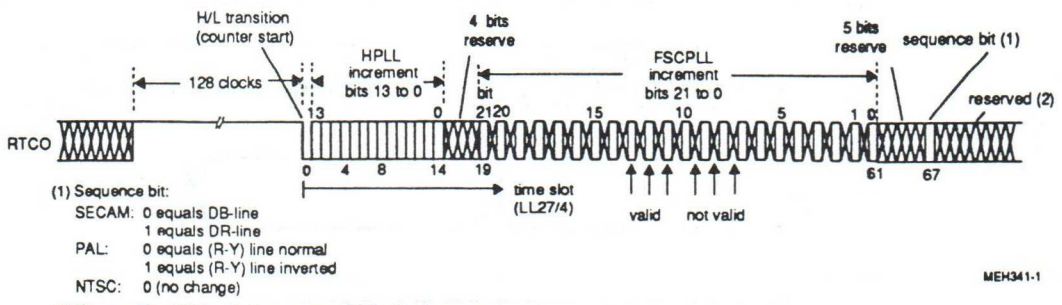


Fig.10 RTCO timing.

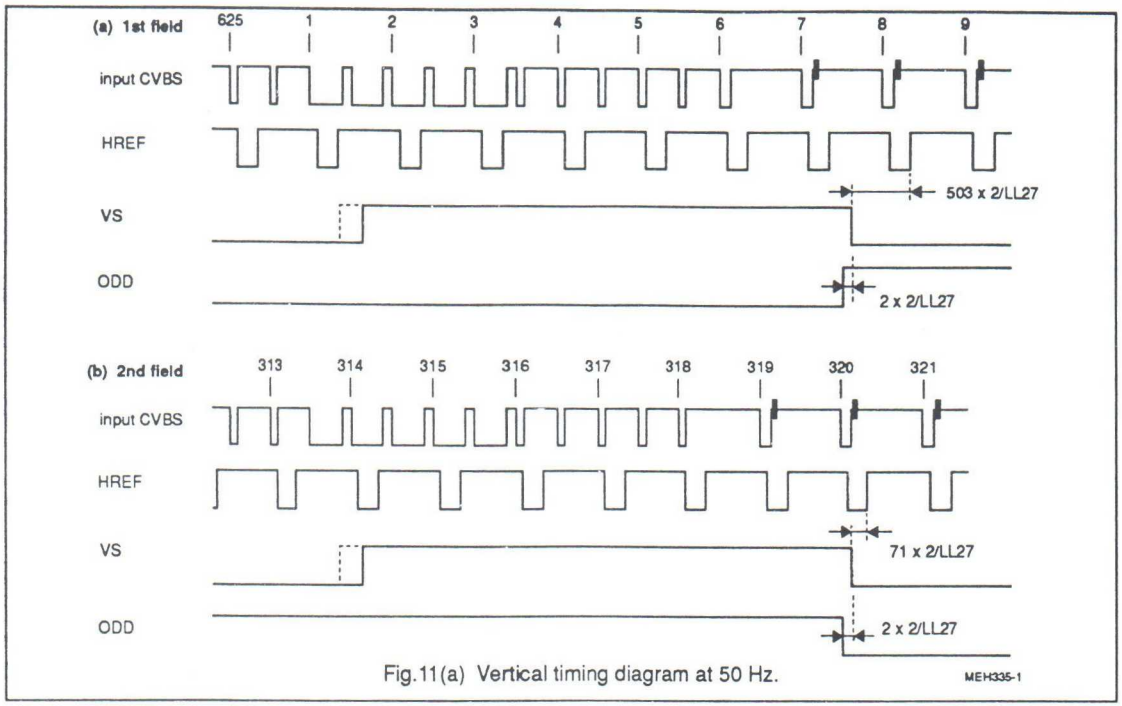


Fig.11(a) Vertical timing diagram at 50 Hz.

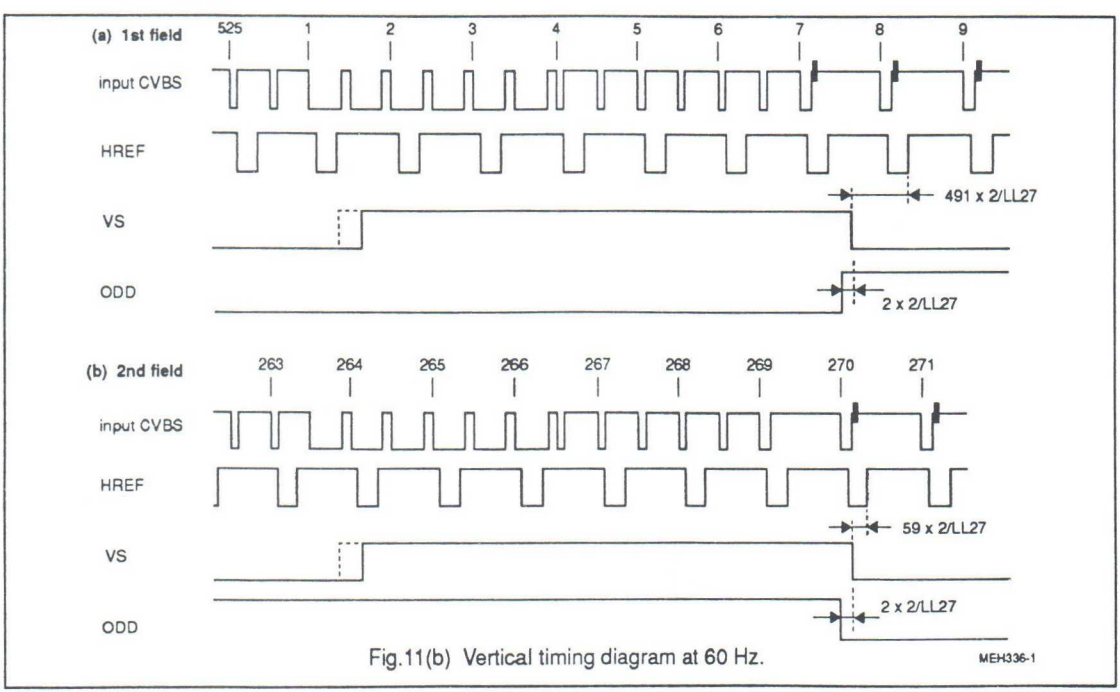
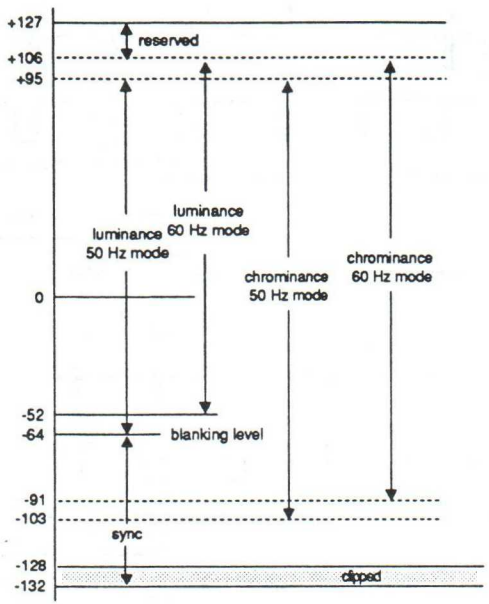
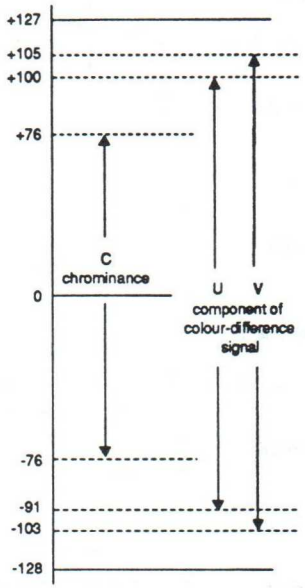


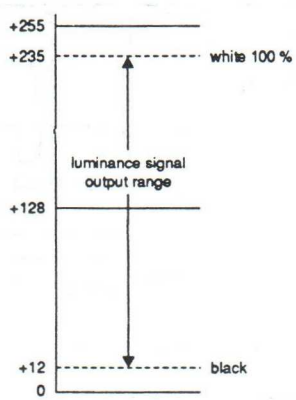
Fig.11(b) Vertical timing diagram at 60 Hz.



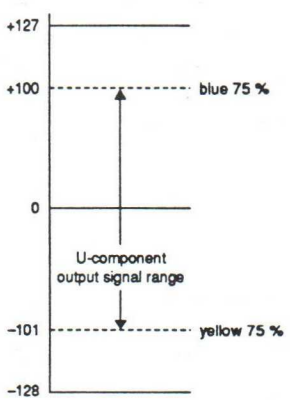
(a) CVBS input signal range.



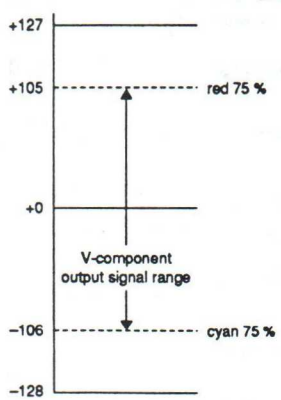
(b) CUV input signal range (U and V out of RGB; in FS mode ranges x 0.5).



(c) Y output signal range.



(d) U output signal range (B-Y).

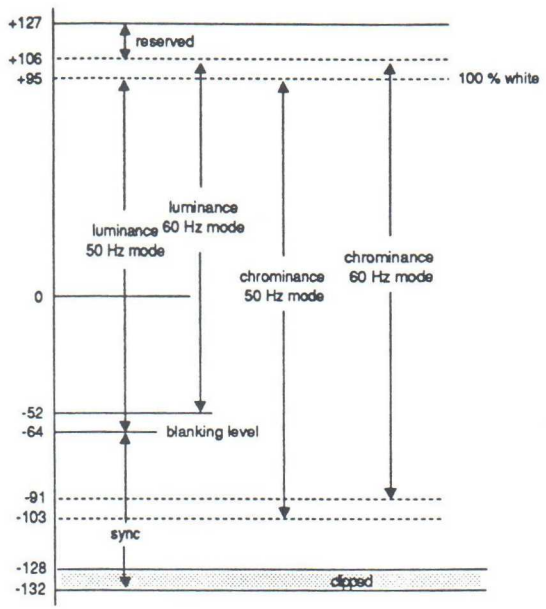


(e) V output signal range (R-Y).

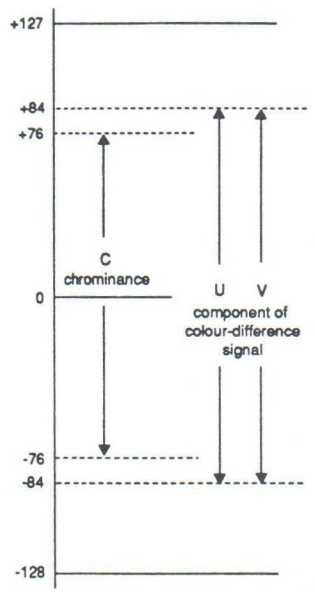
MEH299-3

Notes: 1. All levels are related to EBU colour bar.
2. Values in decimal at 100 % luminance and 75 % chrominance amplitude.

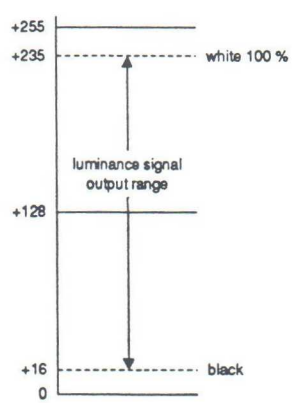
Fig.12 Input and output signal ranges in DTV mode (digital TV).



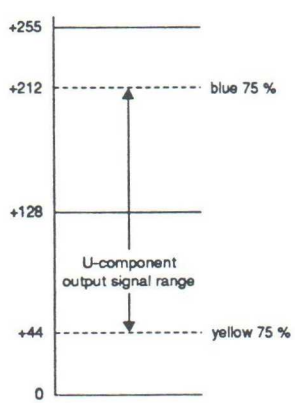
(a) CVBS input signal range.



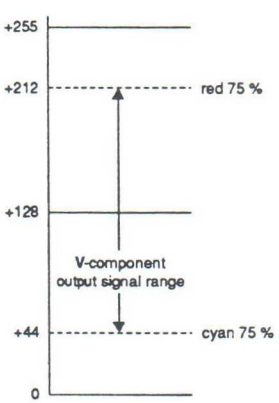
(b) CUV input signal range (U and V out of RGB; in FS mode ranges x 0.5).



(c) Y output signal range.



(d) U output signal range (B-Y).



(e) V output signal range (R-Y).

MEH300 -3

Notes: 1. All levels are related to EBU colour bar.
2. Values in decimal at 100 % luminance and 75 % chrominance amplitude.
3. For SECAM input signals the CCIR levels will be exceeded.

Fig.13 Input and output signal ranges in CCIR mode.

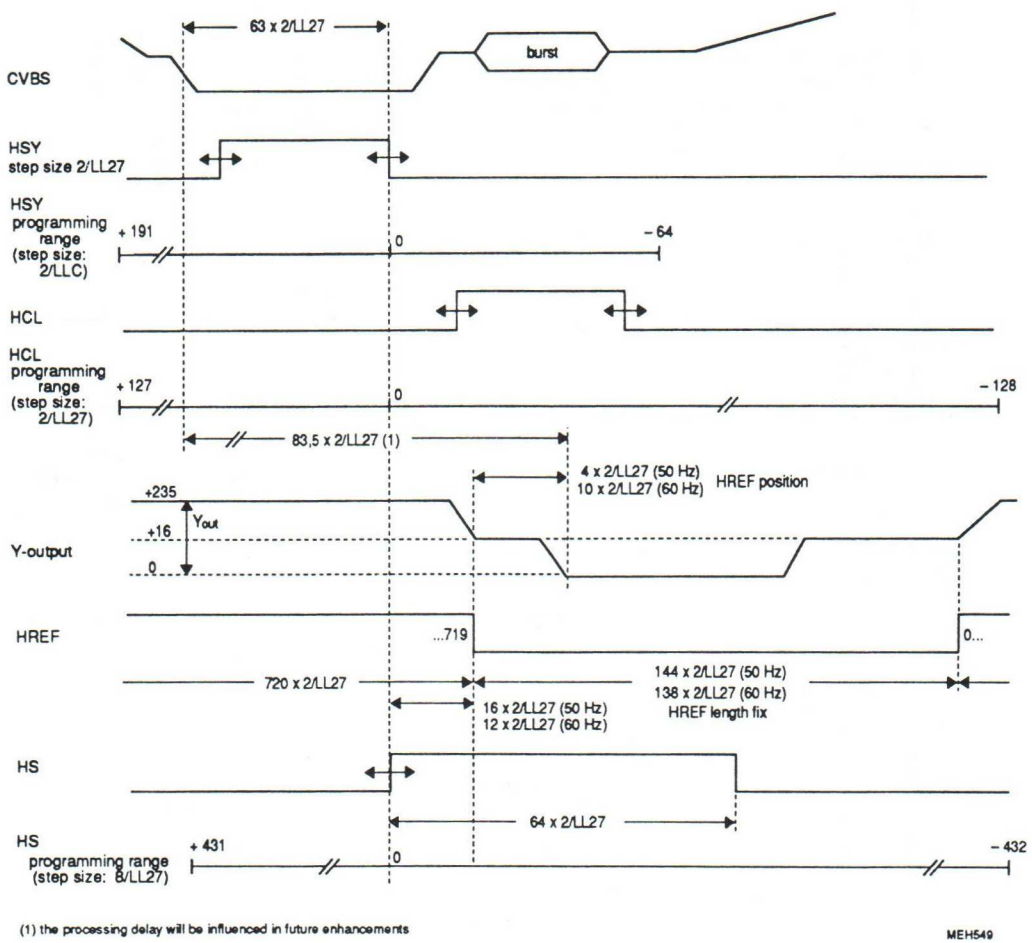


Fig.14 Horizontal sync and clamping timing for 50/60 Hz (signals HSY, HCL, HREF and HS).

8. LIMITING VALUES

In accordance with the Absolute Maximum Rating ystem (IEC 134); ground pins 19, 35, 38, 51 and 67 as well as supply pins 5, 18, 28, 37 and 52 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 18, 28, 37, 52)	–0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{SS\ A} - V_{SS(1\ to\ 4)}$	-	±100	mV
V_I	voltage on all inputs	–0.5	V_{DD}+0.5	V
V_O	voltage on all outputs ($I_{O\ max}$ = 20 mA)	–0.5	V_{DD}+0.5	V
P_{tot}	total power dissipation	-	2.5	W
T_{stg}	storage temperature range	–65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±2000	V

9. CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 5, 18, 28, 37, 52)		4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37, 52)	V_{DD} = 5 V; inputs LOW; outputs not connected	-	100	250	mA
I²C-bus, SDA and SCL (pins 40 and 41)						
V_{IL}	input voltage LOW		–0.5	-	1.5	V
V_{IH}	input voltage HIGH		3	-	V_{DD}+0.5	V
$I_{40,41}$	input current		-	-	±10	µA
I_{ACK}	output current on pin 40	acknowledge	3	-	-	mA
V_{OL}	output voltage at acknowledge	I_{40} = 3 mA	-	-	0.4	V
Data, clock and control inputs (pins 3, 4, 6 to 17, 20 to 23, 27, 34, 64 and 68); Figures 12 and 13						
V_{IL}	LL27 input voltage (pin 27)	LOW	–0.5	-	0.6	V
V_{IH}		HIGH	2.4	-	V_{DD}+0.5	V
V_{IL}	other input voltages	LOW	–0.5	-	0.8	V
V_{IH}		HIGH	2.0	-	V_{DD}+0.5	V
I_{leak}	input leakage current		-	-	10	µA
C_I	input capacitance	data inputs; note 1	-	-	8	pF
		I/O high-impedance	-	-	8	pF
		clock inputs	-	-	10	pF
$t_{SU.DAT}$	input data set-up time	Fig.15	11	-	-	ns
$t_{HD.DAT}$	input data hold time		3	-	-	ns

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.; inputs and outputs are protected against electrostatic discharge in normal handling. Normal precautions appropriate to handle MOS devices is recommended ("Handling MOS Devices").

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
YUV-bus, HREF and VS outputs (pins 30, 42, 45 to 50 and pins 53 to 62), Figures 9 and 12 to 13						
V_{OL}	output voltage LOW	notes 1 and 2	0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitor		15	-	50	pF
LFCO output (pin 36)						
V_o	output signal (peak-to-peak value)	note 2	1.4	-	2.6	V
V_{36}	output voltage range		1	-	V_{DD}	V
Control outputs (pins 24 to 26, 29, 31, 32, 33, 39, 63, 65 and 66); Fig.11, 14 and 15						
V_{OL}	output voltage LOW	notes 1 and 2	0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitor		7.5	-	25	pF
Timing of YUV-bus and control outputs		Figures 9 and 11				
t_{OH}	output signal hold time	YUV, HREF, VS at C_L = 15 pF;	13	-	-	ns
		controls at C_L = 7.5 pF	13	-	-	ns
t_{OS}	output set-up time	YUV, HREF, VS at C_L = 50 pF;	20	-	-	ns
		controls at C_L = 25 pF	20	-	-	ns
t_{SZ}	data output disable transition time	to 3-state condition	22	-	-	ns
t_{ZS}	data output enable transition time	from 3-state condition	20	-	-	ns
Chrominance PLL						
f_C	catching range		±400	-	-	Hz
Crystal oscillator		Figures 17 and 18; note 3				
f_n	nominal frequency	3rd harmonic	-	24.576	-	MHz
$\Delta f / f_n$	permissible deviation f_n		-	-	±50	10^{-6}
	temperature deviation from f_n		-	-	±20	10^{-6}
X1	crystal specification:					
	temperature range T_{amb}		0	-	70	°C
	load capacitance C_L		8	-	-	pF
	series resonance resistance R_S		-	40	80	Ω
	motional capacitance C_1		-	1.5±20%	-	fF
	parallel capacitance C_0		-	3.5±20%	-	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Line locked clock input LL27 (pin 27)		Fig.8 and 15				
t_{LL27}	cycle time	note 4	35	-	39	ns
t_p	duty factor	t_{LL27H} / t_{LL27}	40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns

Notes to the characteristics

1. Data output signals are Y7 to Y0 and UV7 to UV0. All other are control output signals.
2. Levels are measured with load circuit. YUV-bus, HREF and VS outputs with 1.2 kΩ in parallel to 50 pF at 3 V (TTL load); LFCO output with 10 kΩ in parallel to 15 pF and other outputs with 1.2 kΩ in parallel to 25 pF at 3 V (TTL load).
3. Recommended crystal: Philips 4322 143 05291.
4. t_{SU}, t_{HD}, t_{OH} and t_{OD} include t_r and t_f.

Table 4 High-impedance control for YUV-bus (Fig.15)

OEDY	OEDC	FEIN	Y(7:0)	UV(7:0)
0	0	0	Z	Z
0	1	0	Z	active
1	0	0	active	Z
1	1	0	Z	Z
X	X	1	Z	Z

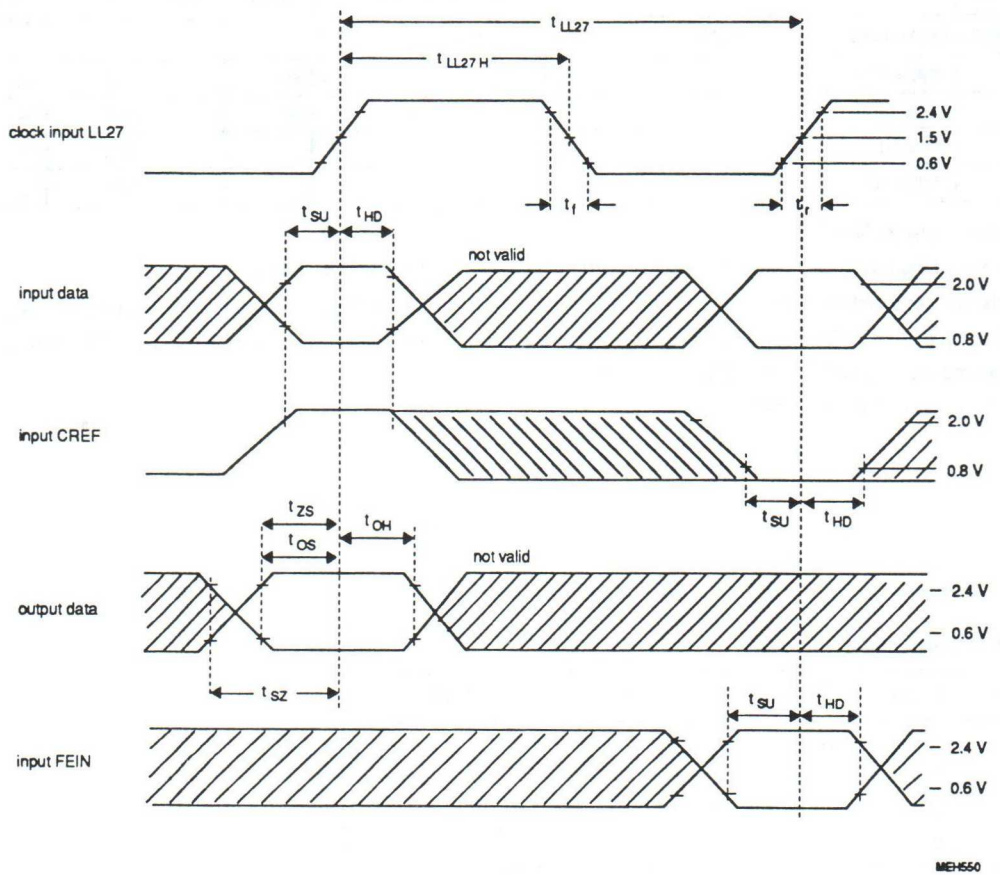


Fig.15 Data input and output timing diagram.

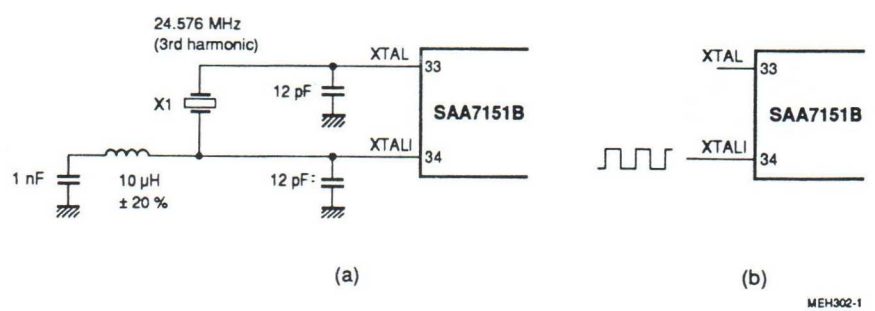


Fig.16 Oscillator application (a) and optional clock from external (b).

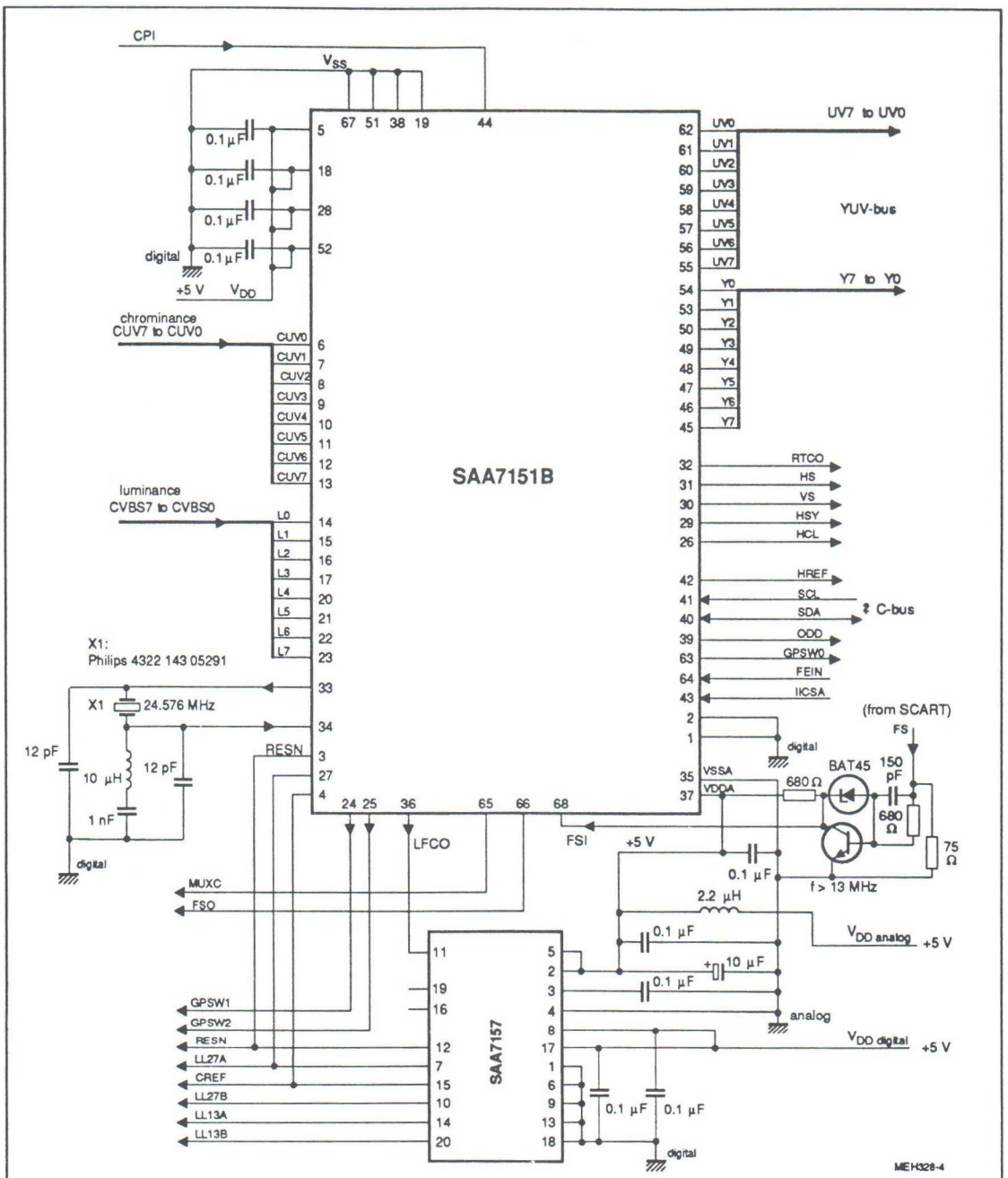


Fig.17 Application of SAA7151B.

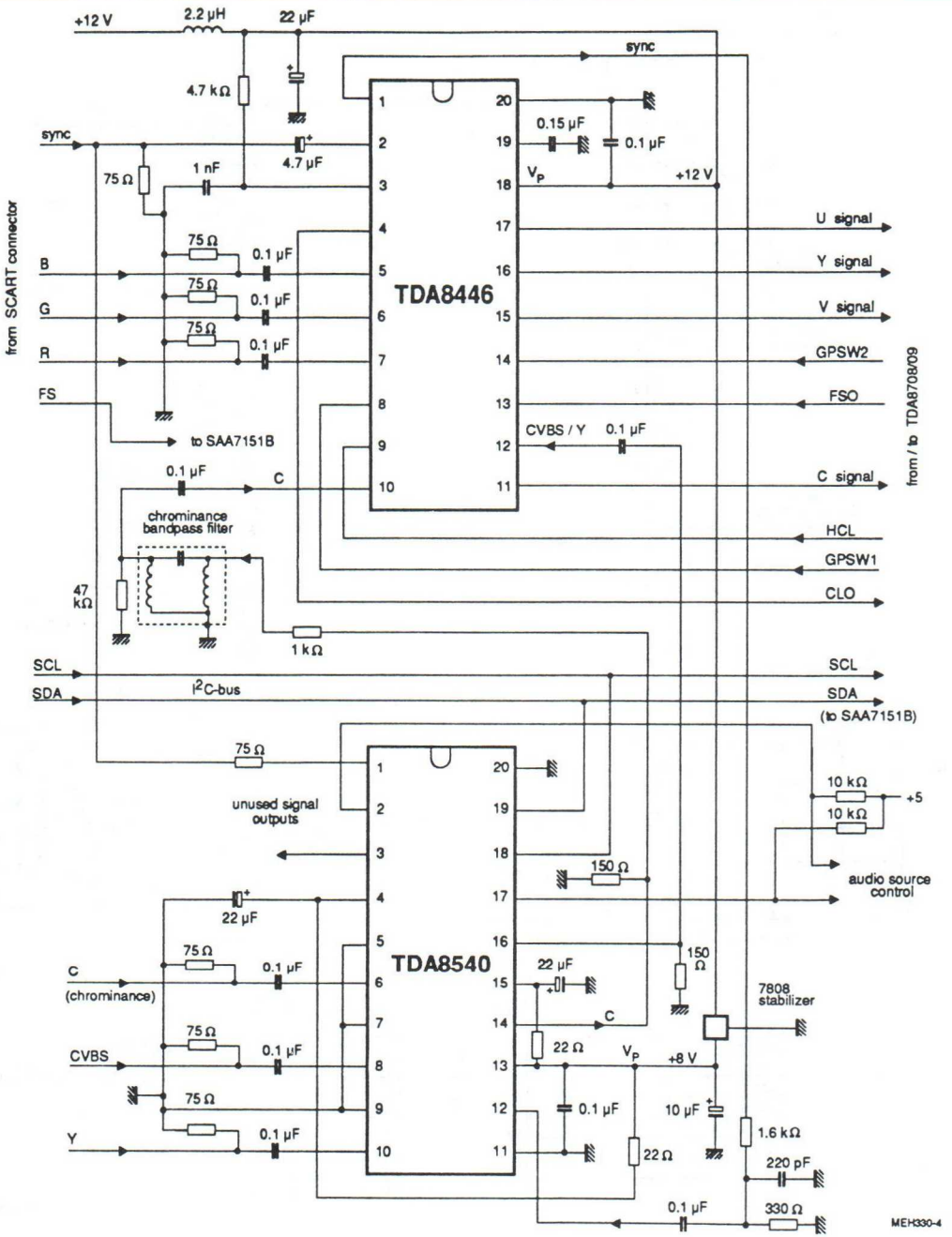


Fig.18 Application of input signal selecting (SCART interface).

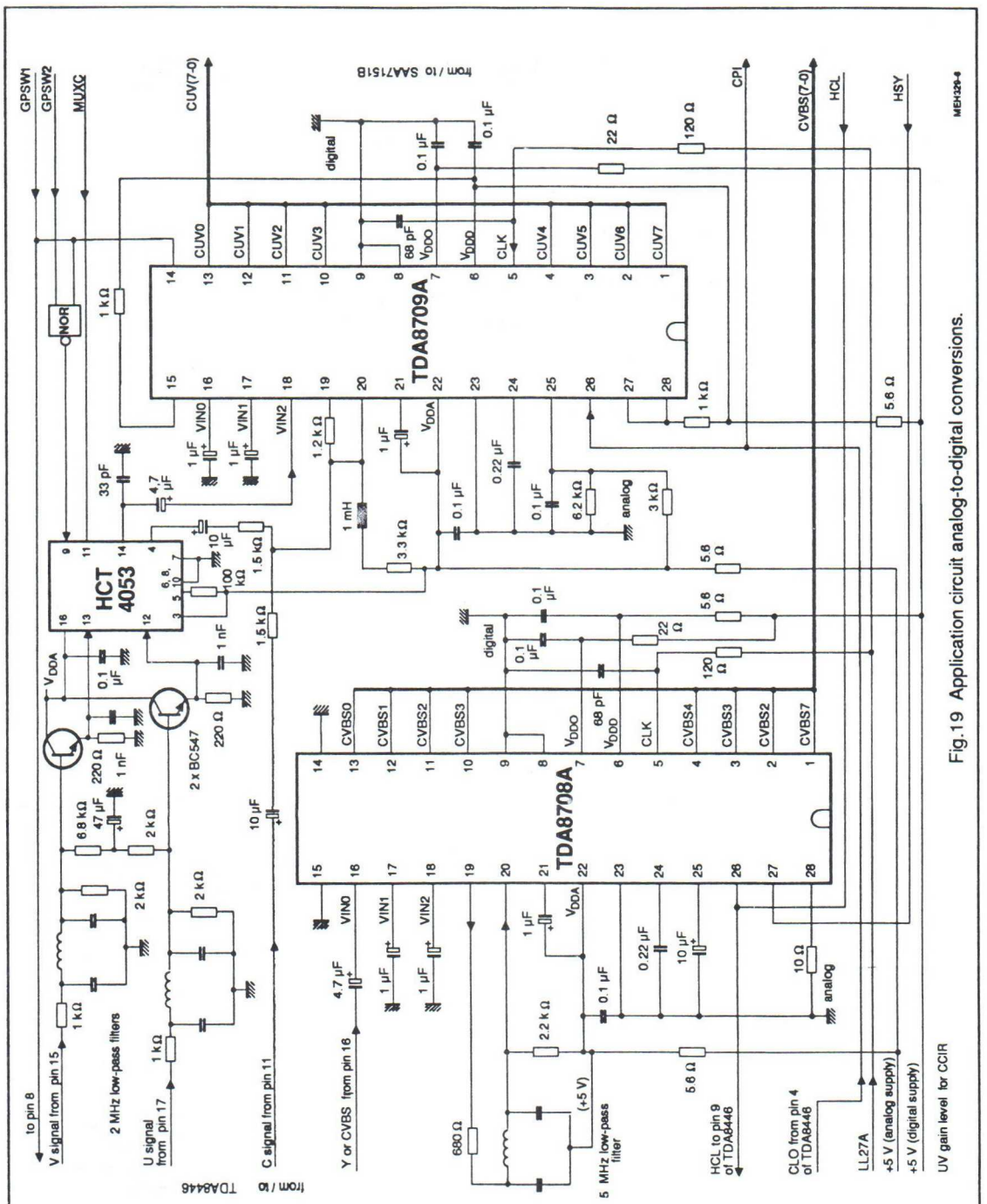


Fig.19 Application circuit analog-to-digital conversions.

10. I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = **1000 101X** (IICSA = LOW) **or 1000 111X** (IICSA = HIGH)
A = acknowledge, generated by the slave
SUBADDRESS* = subaddress byte (Table 5)
DATA = data byte (Table 5)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Remarks: - Prior to reset of the IC all outputs are undefined.
- After power-on reset, the control register 12 (hex) is set to 00 (hex).

Table 5 I²C-bus; DATA for status byte (X in address byte = 1; slave address 8B (hex) at IICSA = LOW or 8F (hex) at IICSA = HIGH)

FUNCTION		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
status byte		STTC	HLCK	FIDT	FSST1	FSST0	CDET2	CDET1	CDET0

Function of the bits:

STTC — Status time constant (to be used for gogical combfilter SAA7152) 0 = TV mode; 1 = VCR mode

HLCK — Horizontal PLL information: 0 = HPLL locked; 1 = HPLL unlocked

FIDT — Field information: 0 = 50 Hz system detected; 1 = 60 Hz system detected

FSST1 to FSST0 — Fast swiching output mode:

FSST1	FSST0	mode
0	0	RGB; FSI = HIGH (pin 68)
0	1	Y/C; FSI = LOW (pin 68)
1	0	fast switching (toggle)
1	1	not used

CDET2 to CDET0 — Identified colour standard

CDET2	CDET2	CDET2	standard
0	0	0	PAL-B/G, -H, -I; 50 Hz
0	0	1	PAL-N; 50 Hz
0	1	0	SECAM; 50 Hz
0	1	1	PAL-M; 60 Hz
1	0	0	PAL 4.43; 60 Hz
1	0	1	NTSC-M; 60 Hz
1	1	0	NTSC 4.43; 60 Hz
1	1	1	black/white

Table 6 I²C-bus; subaddress and data bytes for writing (X in address byte = 0; slave address 8A (hex) at IICSA = LOW or 8E at IICSA = HIGH)

function	subaddress byte	data byte D7	D6	D5	D4	D3	D2	D1	D0
increment delay	00	IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0
H-sync HSY begin	01	HSYB7	HSYB6	HSYB5	HSYB4	HSYB3	HSYB2	HSYB1	HSYB0
H-sync HSY stop	02	HSYS7	HSYS6	HSYS5	HSYS4	HSYS3	HSYS2	HSYS1	HSYS0
H-clamp HCL begin	03	HCLB7	HCLB6	HCLB5	HCLB4	HCLB3	HCLB2	HCLB1	HCLB0
H-clamp HCL stop	04	HCLS7	HCLS6	HCLS5	HCLS4	HCLS3	HCLS2	HCLS1	HCLS0
H-sync after PHI1	05	HPHI7	HPHI6	HPHI5	HPHI4	HPHI3	HPHI2	HPHI1	HPHI0
luminance control	06	BYPS	PREF	BPSS1	BPSS0	BFBY	CORI	APER1	APER0
hue control	07	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
miscellaneous controls #1	08	CSTD2	CSTD1	CSTD0	CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0
miscellaneous controls #2	09	OSCE	LFIS1	LFIS0	CKTS4	CKTS3	CKTS2	CKTS1	CKTS0
PAL switch sensitivity	0A	PLSE7	PLSE6	PLSE5	PLSE4	PLSE3	PLSE2	PLSE1	PLSE0
SECAM switch sensitivity	0B	SESE7	SESE6	SESE5	SESE4	SESE3	SESE2	SESE1	SESE0
miscellaneous controls #3	0C	FSAU	GPSI2	GPSI1	CGFX	AMPF3	AMPF2	AMPF1	AMPF0
miscellaneous controls #4	0D	COLO	CHSB	GPSW0	SUVI	SXCR	FSDL2	FSDL1	FSDL0
miscellaneous controls #5	0E	CCIR	COFF	OEHS	OEVS	UVSS	CHRS	CDMO	CDPO
miscellaneous controls #6	0F	AUFD	FSEL	HPLL	SCEN	VTRC	MUIV	FSIV	WIND
miscellaneous controls #7	10	ASTD	OFTS	IPBP	CDVI	YDEL3	YDEL2	YDEL1	YDEL0
chroma gain reference	11	CHCV7	CHCV6	CHCV5	CHCV4	CHCV3	CHCV2	CHCV1	CHCV0
miscellaneous controls #8	12	OEDY	OEDC	VNOI1	VNOI0	BFON	BOFL2	BOFL1	BOFL0

Function of the bits of Table 6

IDEL7 to IDEL0

"00"

Increment delay time , step size = 4/LL27 = 148 ns*

D7	D6	D5	D4	D3	D2	D1	D0	decimal multiplier	note
1	1	1	1	1	1	1	1	–1 to –110	minimum –148 ns
1	0	0	1	0	0	1	0		–16.3 µs (outside available range)
1	0	0	1	0	0	0	1	–111 to –214	–16.44 µs
0	0	1	0	1	0	1	0		–31.7 µs (maximum value at FSEL = 1)
0	0	1	0	1	0	0	1	–215	–31.85 µs (outside central counter range at FSEL = 1 **)
0	0	1	0	1	0	0	0	–216	–32.0 µs (maximum value at FSEL = 0 **)
0	0	1	0	0	1	1	1	–217 to –256	–32.148 µs (outside central counter range at FSEL = 0 **)
0	0	0	0	0	0	0	0		–37.9 µs (outside central counter **)

* an internal sign-bit D8 set to HIGH indicates that all values are always negative

** H-PLL does not operate in this condition; the system clock frequency is set to a value fixed by the last update and is within ±7.1 % of the nominal frequency.

HSYB7 to HSYB0
HSYS7 to HSYS0
"01" and "02"

Horizontal sync begin, step size = 2/LL27 = 74 ns
Horizontal sync stop, step size = 2/LL27 = 74 ns

D7	D6	D5	D4	D3	D2	D1	D0	decimal multiplier	note
1	0	1	1	1	1	1	1	191 to 1	−14.2 µs (maximum negative value)
0	0	0	0	0	0	0	1		−74 ns
0	0	0	0	0	0	0	0	0	0 equals reference value
1	1	1	1	1	1	1	1	−1 to −64	+74 ns
1	1	0	0	0	0	0	0		+4.7 µs

HCLB7 to HCLB0
HCLS7 to HCLS0
"03" and "04"

Horizontal clamp begin, step size = 2/LL27 = 74 ns
Horizontal clamp stop, step size = 2/LL27 = 74 ns

D7	D6	D5	D4	D3	D2	D1	D0	decimal multiplier	note
0	1	1	1	1	1	1	1	127 to 1	−9.4 µs (maximum negative value)
0	0	0	0	0	0	0	1		−74 ns
0	0	0	0	0	0	0	0	0	0 equals reference value
1	1	1	1	1	1	1	1	−1 to −128	+74 ns
1	0	0	0	0	0	0	0		+9.5 µs (maximum positive value)

HPHI7 to HPHI0
"05"

Horizontal sync start, step size = 8/LL27 = 296 ns

D7	D6	D5	D4	D3	D2	D1	D0	decimal multiplier	note
0	1	1	1	1	1	1	1	+127 to +109	) forbidden (outside available central
0	1	1	0	1	1	0	1		) counter range)
0	1	1	0	1	1	0	0	+108 to +1	−32 µs (maximum negative value)
0	0	0	0	0	0	0	1		−0.296 ns
0	0	0	0	0	0	0	0	0	0 equals reference value
1	1	1	1	1	1	1	1	−1 to −107	+0.296 µs
1	0	0	1	0	1	0	1		+31.7 µs (maximum positive value)
1	0	0	1	0	1	0	0	−108 to −128	) forbidden (outside available central
1	0	0	0	0	0	0	0		) counter range)

BYPS
"06"

Input mode select bit: 0 = CVBS mode (chroma trap active)
1 = S-Video mode (chroma trap by-passed)

PREF

Use of pre-emphasis (to be used if chrominance trap is active):
0 = pre-filter bypassed; 1 = pre-filter on

BPSS1 to BPSS0

Aperture bandpass to select different centre frequencies (Figures 23 to 38):

BPSS1	BPSS0	centre frequency
0	0	4.1 MHz
0	1	3.8 MHz
1	0	2.6 MHz
1	1	2.9 MHz

"06" continued

BFBY: Bandfilter bypass switching: 0 = bandfilter active; 1 = bandfilter bypassed

CORI: Coring function: 0 = coring off; 1 = ±1 LSB coring

APER1 to APER0: Aperture factor (Figures 23 to 38):

APER1	APER0	factor
0	0	0
0	1	0.25
1	0	0.5
1	1	1

HUE7 to HUE0 "07": Hue control from +178.6° to −180.0°, equals data bytes 7F to 80 (hex); 0° equals 00.

CSTD2 to CSTD0 "08": Forced colour standard of input signal;

CSTD2	CSTD1	CSTD0	standard
0	0	0	PAL-B/G, -H, -I; 50 Hz
0	0	1	PAL-N; 50 Hz
0	1	0	SECAM; 50 Hz
0	1	1	PAL-M; 60 Hz
1	0	0	PAL 4.43; 60 Hz
1	0	1	NTSC-M; 60 Hz
1	1	0	NTSC 4.43; 60 Hz
1	1	1	black/white

CKTQ4 to CKTQ0: Colour killer threshold QAM (PAL/NTSC):

CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0	
1	1	1	1	1	approximately −30 to −24 dB
1	0	0	0	0	−24 dB to −18 dB
0	0	0	0	0	

OSCE "09": External UV offset compensation: 0 = disabled; 1 = enabled

LFIS1 to LFIS0: Chrominance gain control (AGC filter):

LFIS1	LFIS0	control of loop filter time constant
0	0	slow
0	1	medium
1	0	fast
1	1	actual gain, stored (for test purposes only)

CKTS4 to CKTS0: Colour killer threshold SECAM as previously described under CKTQ subaddress"08"

PLSE7 to PLSE0 "0A"

PAL switch sensitivity from LOW to HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.

SESE7 to SESE0 "0B"

SECAM switch sensitivity from LOW to HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.

FSAU; GPSI2, and GPSI1 "0C"

Set port outputs (general purpose switching, internal)

FSAU	GPSI2	GPSI1	output GPSW2 (pin 25)	output GPSW1 (pin 24)
0	0	0	LOW	LOW
0	0	1	LOW	HIGH
0	1	0	HIGH	LOW
0	1	1	HIGH	HIGH
1	X	X	status bit FSST1 set	status bit FSST0 set

CGFX

Chrominance gain pre-determination: 0 = gain controlled via loop; 1 = gain set by AMPF-bits

AMPF3 to AMPF0

Chrominance amplification factor

AMPF3	AMPF2	AMPF1	AMPF0	gain
0	0	0	0	–6 dB
0	1	0	0	0 dB
0	1	0	1	+1.5 dB
.	.	.	.	+3 to +16.5 dB (approximately 1.5 dB steps)
1	1	1	1	+17 dB

COLO "0D"

Colour-on bit: 0 = colour-killer automatically enabled ; 1 = forced colour-on.

CHSB

Chrominance (UV) output code: 0 = two's complement; 1 = straightly binary

GPSW0

General purpose port output (pin 63): 0 = LOW; 1 = HIGH

SUVI

SECAM UV output signal polarity: 0 = U and V positive; 1 = U and V negative

SXCR

SECAM cross-colour reduction: 0 = off; 1 = on

FDSL2 to FDSL0

Fast switching delay adjustment in 37 ns steps:

FDSL2	FDSL1	FDSL0	delay
0	0	0	0
0	0	1	37 ns
0	1	0	74 ns
0	1	1	111 ns
1	0	0	–148 ns (negative delay)
1	0	1	–111 ns
1	1	0	–74 ns
1	1	1	–37 ns

CCIR "0E"	Set CCIR mode: 0 = digital TV mode (DTV); 1 = CCIR mode
COFF	Set colour off: 0 = colour on; 1 = colour off
OEHS	Enable horizontal sync outputs HS and HREF: 0 = output high-impedance; 1 = HS and HREF enabled
OEVS	Enable vertical sync output VS: 0 = output high-impedance; 1 = VS enabled
UVSS	Select UV pixel sample: 1 = first pixel after U/V signal has changed; 0 = second pixel (free of crosstalk signals)
CHRS	S-Video input mode: 0 = chrominance signal from CVBS or CUV input and controlled by BYPS (subaddress 06); 1 = S-Video mode; chrominance signal from CUV input
CDMO, CDPO	Chrominance delay: CDMO 0 → CDPO 0 → no delay CDMO 1 → CDPO X → –37 ns (negative delay) CDMO 0 → CDPO 1 → +37 ns
AUFD "0F"	Automatical field detection: 0 = field selection by FSEL-bit; 1 = automatical field detection
FSEL	Field select (AUFD-bit = 0): 0 = 50 Hz (625 lines); 1 = 60 Hz (525 lines)
HPLL	Horizontal PLL: 0 = PLL closed; 1 = PLL open, horizontal frequency fixed
SCEN	Sync and clamping pulse enable: 0 = HCL and HSY outputs HIGH (pins 26 and 29); 1 = HCL and HSY outputs active.
VTRC	VTR/TV mode select: 0 = TV mode (slow time constant); 1 = VTR mode (fast time constant).
MUIV	MUXC signal invertion: 0 = inverted; 1 = not inverted
FSIV	Fast switch input signal inversion: 0 = not inverted; 1 = inverted
WIND	Narrow fast switch window : 0 = off; 1 = on
ASTD "10"	Automatic standard switching: 0 = off; 1 = on
OFTS	Select output format: 0 = 4 : 1 : 1 format; 1 = 4 : 2 : 2 format.
IPBP	External UV signal interpolation filter: 0 = active; 1 = bypassed
CDVI	Chrominance PLL filter selection for: 0 = VTR or TV source; 1 = fast time constant for FSC-PLL (only for special applications)
YDEL3 to YDEL0	Luminance delay compensation in 37 ns steps: YDEL3 YDEL2 YDEL1 YDEL0 → delay 0 0 0 0 / 0 1 1 1 → 0 to 259 ns (step 0 to 7) 1 0 0 0 / 1 1 1 1 → –296 to –37 ns (negative delay; step –8 to –1)

CHCV7 to CHCV0 "11" — Chroma gain reference value

D7	D6	D5	D4	D3	D2	D1	D0	gain	
1	1	1	1	1	1	1	1	maximum gain	
	:				:			to	)
1	0	1	1	0	0	1	1	DTV level	) default programmed values
	:				:			to	) dependend on application
0	0	1	1	1	1	0	1	CCIR level	)
	:				:			to	)
0	0	0	0	0	0	0	0	minimum gain	

OEDY "12" — Enable Y signals on YUV-bus: 0 = output high-impedance; 1 = output active (dependent on FEIN)

OEDC — Enable UV signals on YUV-bus: 0 = output high-impedance; 1 = output active (dependent on FEIN)

VNOI1, VNOI0 — Vertical noise reduction mode:

VNOI1	VNOI0	mode
0	0	normal
0	1	searching
1	0	free-running
1	1	bypassed

BFON — Bottom flutter compensation switching: 0 = off; 1 = on (controlled by BOFL-bit)

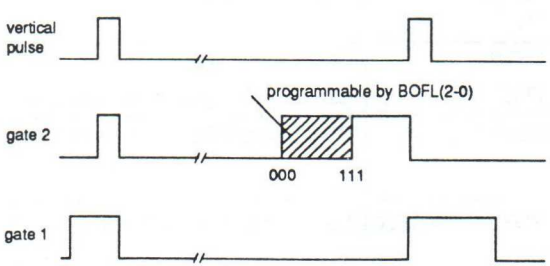
BOFL2 to BOFL0 — Bottom flutter compensation

BOFL2	BOFL1	BOFL0	start at line number
0	0	0	297 for PAL (247 for NTSC; active to end of field)
0	0	1	298 for PAL (248 for NTSC; active to end of field)
.	.	.	. .
1	1	0	303 for PAL (253 for NTSC; active to end of field)
1	1	1	304 for PAL (254 for NTSC; active to end of field)

The bottom flutter circuit is able to compensate for horizontal phase jump of up to ±16 µs.

Note: The bottom flutter gate is active at
- HPLL is locked
- HPLL in VTR mode
- the vertical noise limiter (VNL) is in the VTR mode
- gating is switched by BFON-bit = 1 (subaddress 12)

Gate 2	Gate 1	HPLL function
0	0	normal
1	0	disabled
0	1	double speed
1	1	unused



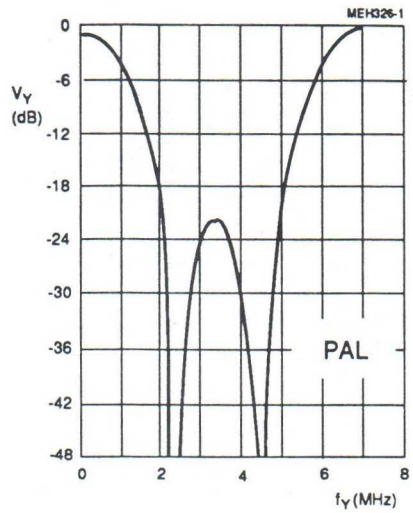


Fig.20 Frequency response of chroma stop filter in colour-difference mode for 50 Hz PAL. Filter is only active in fast switching mode, but bypassed in RGB mode. The selected filter is dependent on actual detected colour standard.

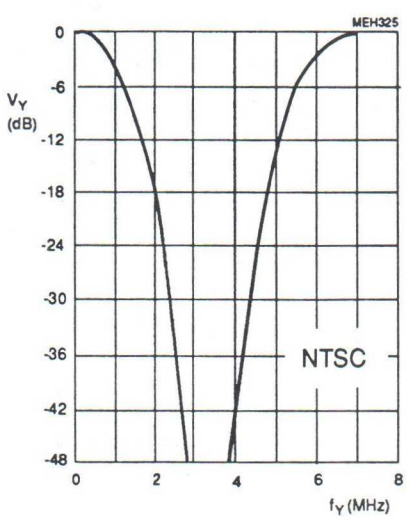


Fig.21 Frequency response of chroma stop filter in colour-difference mode for 60 Hz NTSC. Filter is only active in fast switching mode, but bypassed in RGB mode. The selected filter is dependent on actual detected colour standard.

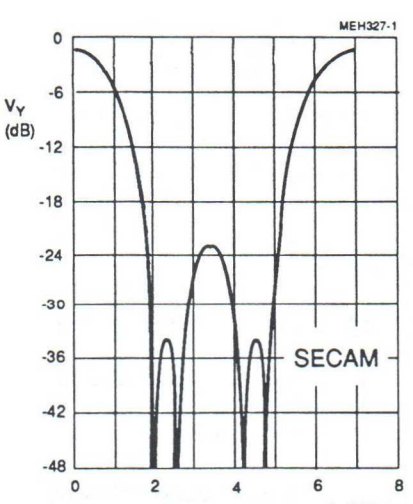


Fig.22 Frequency response of chroma stop filter in colour-difference mode for 50 Hz SECAM. Filter is only active in fast switching mode, but bypassed in RGB mode. The selected filter is dependent on actual detected colour standard.

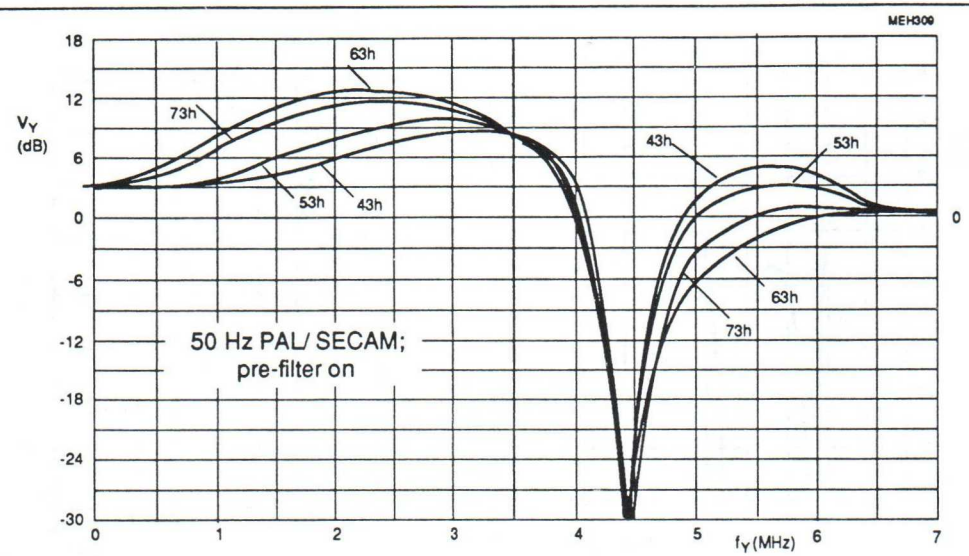


Fig.23 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter on ; and bandfilter on.

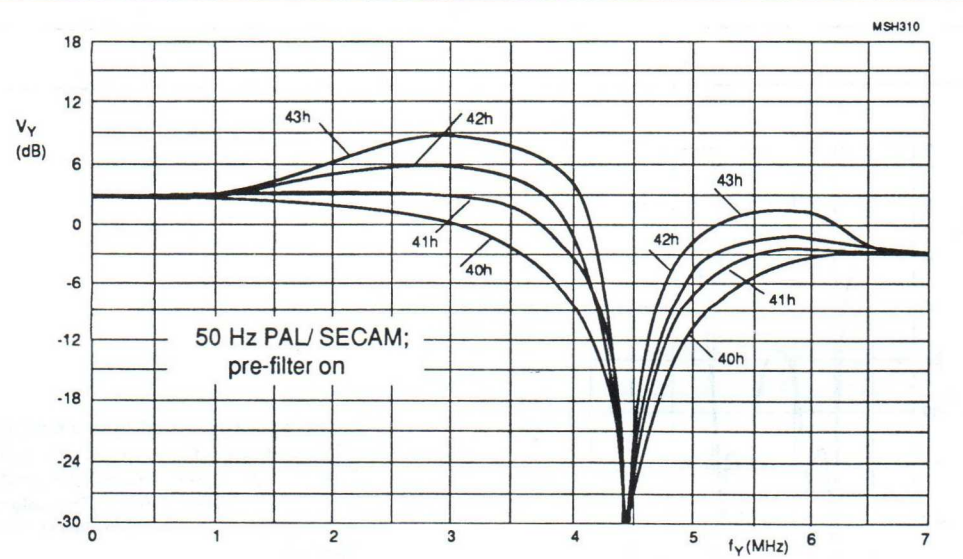


Fig.24 3.8 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter on and bandfilter on.

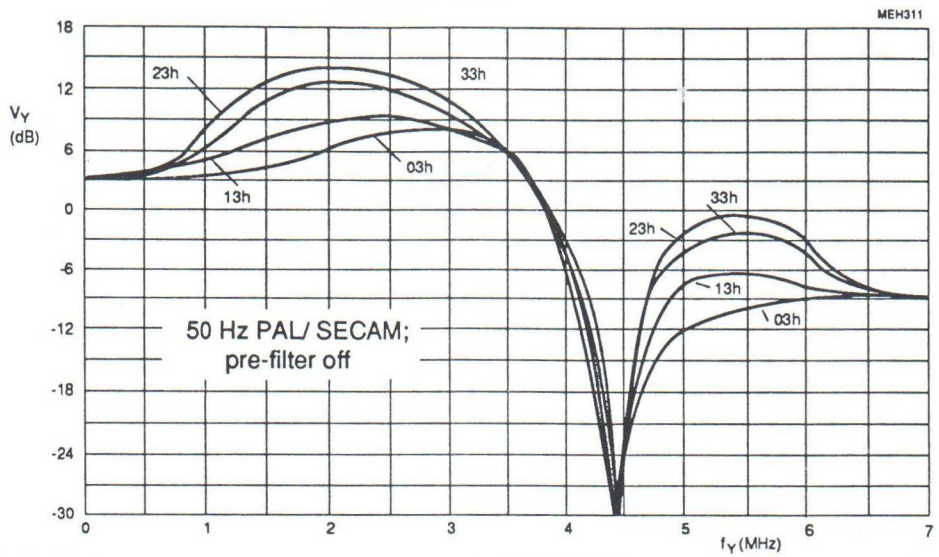


Fig.25 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter off ; and bandfilter on.

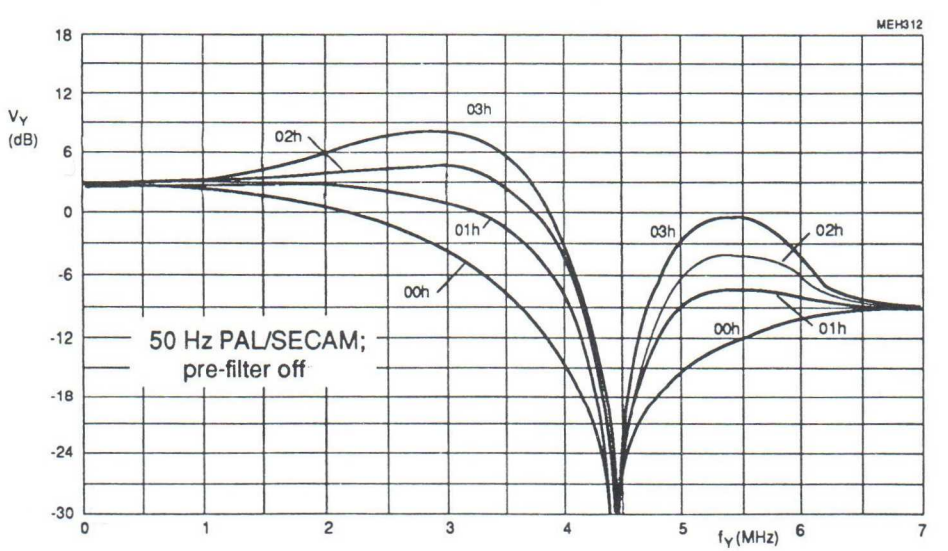


Fig.26 4.1 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter off and bandfilter on.

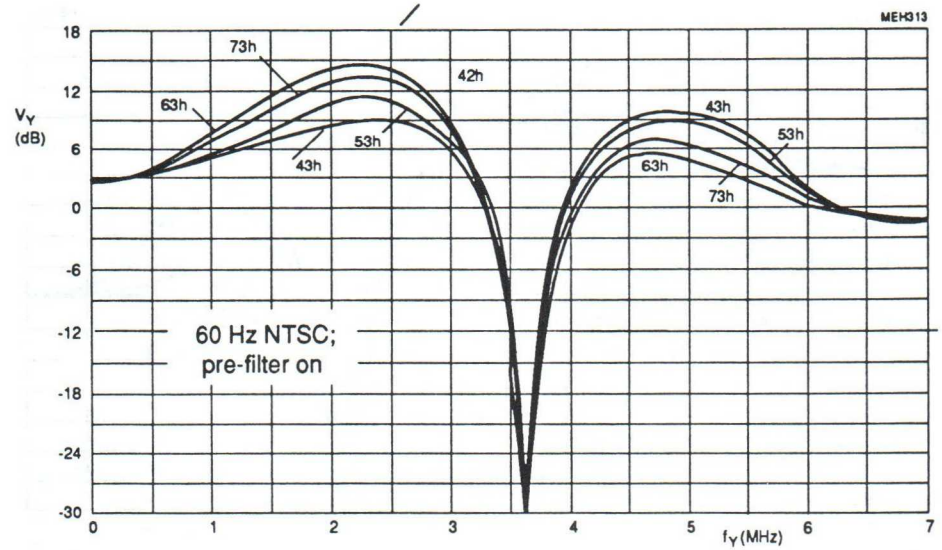


Fig.27 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter on ; and bandfilter on.

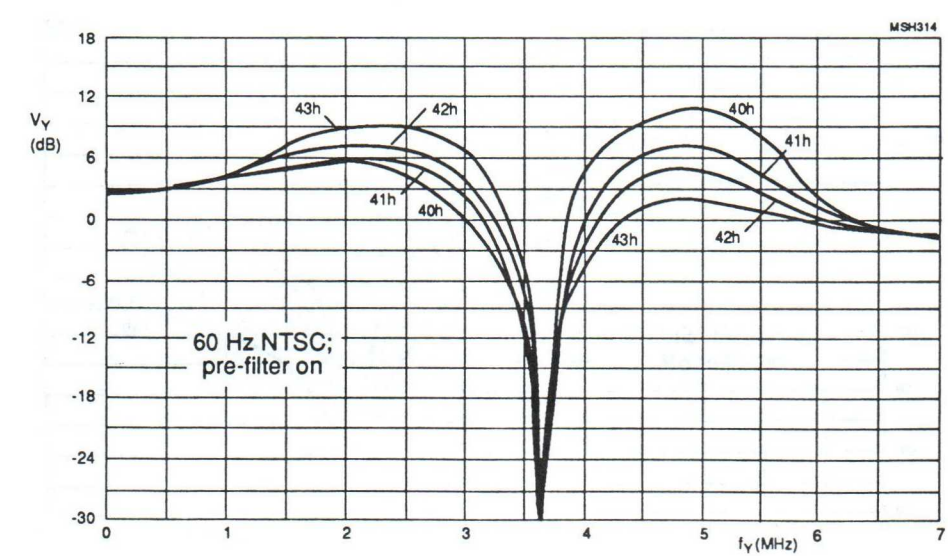


Fig.28 3.8 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter on and bandfilter on.

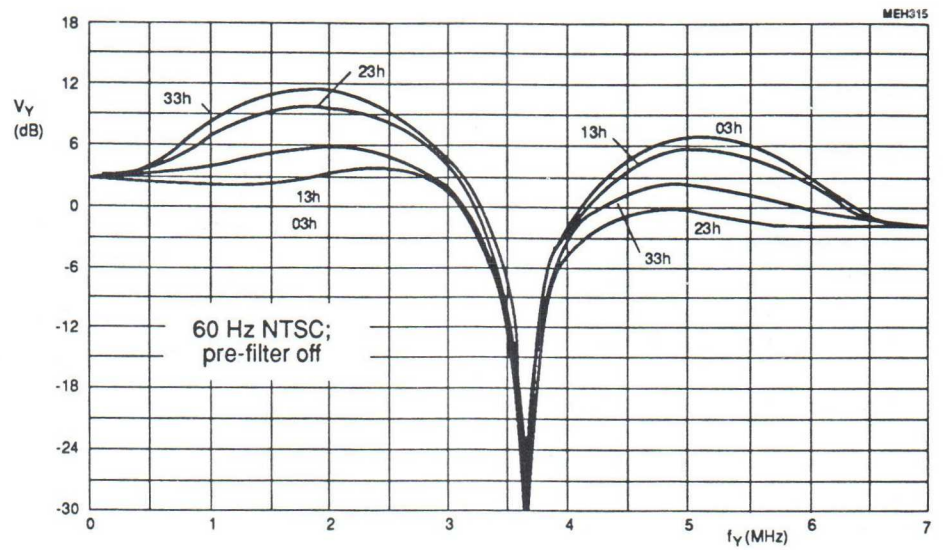


Fig.29 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter off ; and bandfilter on.

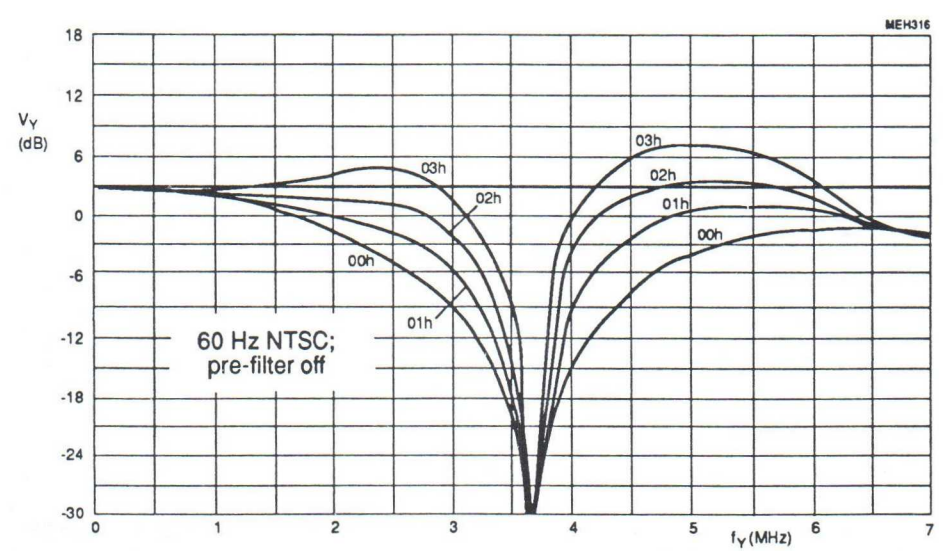


Fig.30 4.1 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter off and bandfilter on.

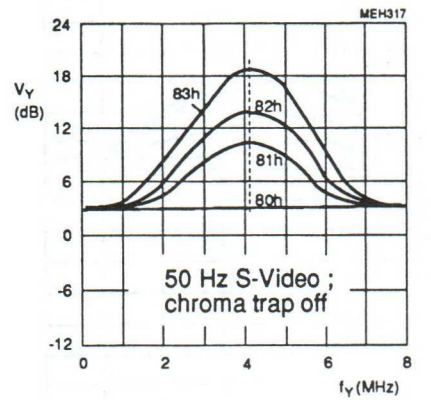


Fig.31 4.1 MHz luminance peaking control control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

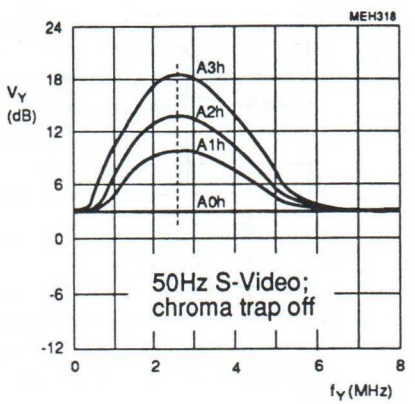


Fig.32 2.6 MHz luminance peaking control control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

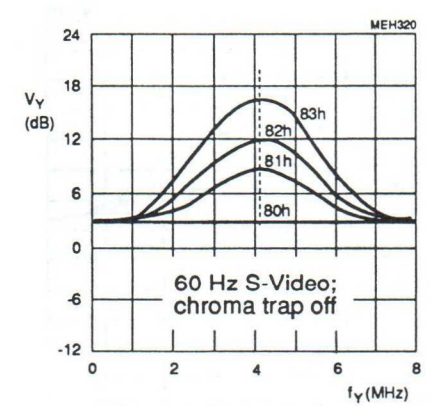


Fig.33 4.1 MHz luminance peaking control control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

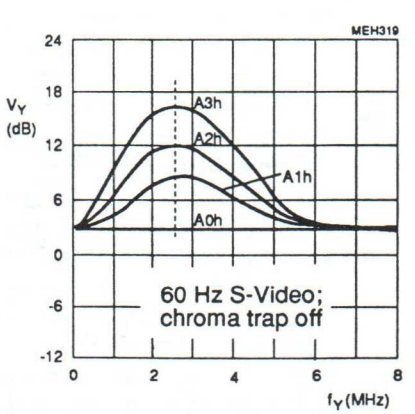


Fig.34 2.6 MHz luminance peaking control control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

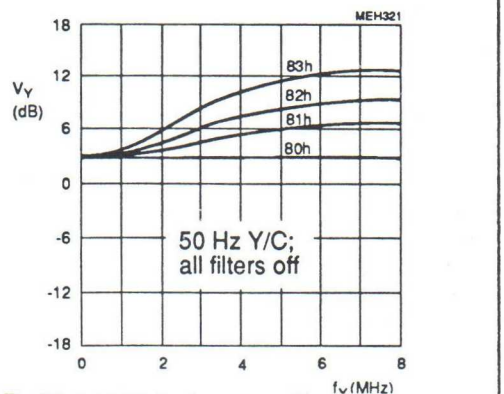


Fig.35 4.1 MHz luminance peaking control in 50 Hz / S-VHS mode as a function of four different aperture factors controllable by subaddress byte 06.

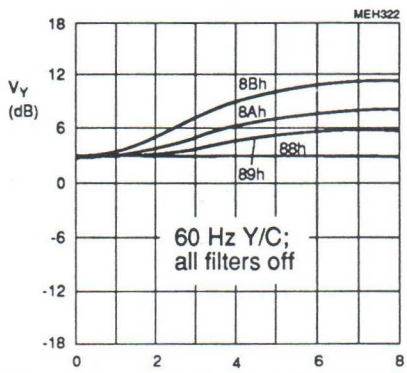


Fig.36 4.1 MHz luminance peaking control in 60 Hz / S-VHS mode as a function of four different aperture factors controllable by subaddress byte 06.

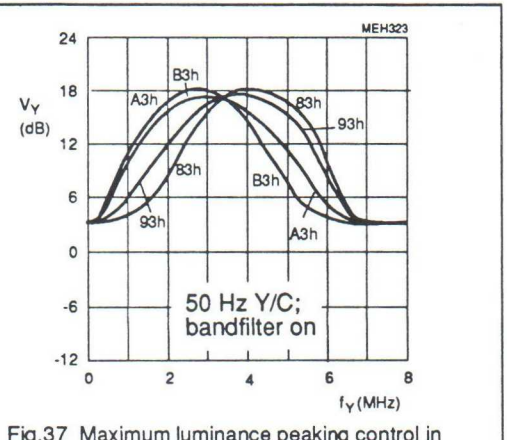


Fig.37 Maximum luminance peaking control in 50 Hz / S-VHS mode as a function of four aperture centre frequencies controllable by subaddress byte 06.

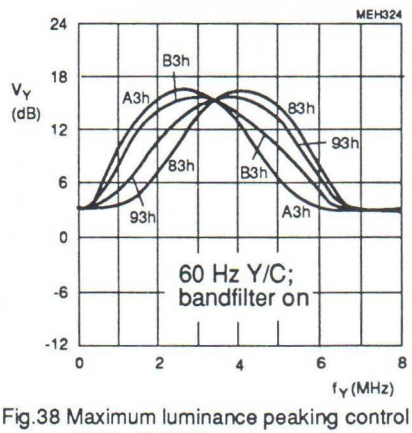


Fig.38 Maximum luminance peaking control in 60 Hz / S-VHS mode as a function of four aperture centre frequencies controllable by subaddress byte 06.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

11. PROGRAMMING EXAMPLE

Coefficients to set operation for application circuits Figures 17, 18 and 19. Values recommended for PAL CVBS input signal and 4:2:2 CCIR output signal (all numbers of the Table 6 are hex values).

Table 7 Recommended default values (note 1)

SUBADDRESS	BIT NAME	FUNCTION	VALUE (HEX)
00	IDEL(7-0)	increment delay	4D
01	HSYB(7-0)	horizontal sync HSY begin	3D
02	HSYS(7-0)	horizontal sync HSY stop	0D
03	HCLB(7-0)	horizontal clamping HCL begin	F3
04	HCLS(7-0)	horizontal clamping HCL stop	C6
05	HPHI(7-0)	horizontal sync after PHI1	FB
06	BYPS, PREF, BPSS(1-0) BFBY, CORI, APER(1-0)	luminance bandwidth control:	02 (note 2)
07	HUEC(7-0)	hue control (0 degree)	00
08	CSTD(2-0), CKTQ(4-0)	miscellanous controls #1	09
09	OSCE, LFIS(1-0),CKTS(4-0)	miscellanous controls #2	C0
0A	PLSE(7-0)	PAL switch sensitivity	4D
0B	SESE(7-0)	SECAM switch sensitivity	40
0C	FSAU, GPSI(2-1), CGFX, AMPF(3-0)	miscellanous controls #3	80
0D	COLO, CHSB, GPSW0, SUVI, SXCR, FSDL(2-0)	miscellanous controls #4	60
0E	CCIR, COEF, OEHS, OEVS UVSS, CHRS, CDMO, CDPO	miscellanous controls #5	B4
0F	AUFD, FSEL, HPLL, SCEN, VTRC, MUIV, FSIV, WIND	miscellanous controls #6	9F
10	ASTD, OFTS, IPBP, CDVI, YDEL(3-0)	miscellanous controls #7	C0
11	CHCV(7-0)	nominal chrominance gain	4F
12	OEDY, OEDC, VNOI(1-0), BFON, BOFL(2-0)	miscellanous controls #8	C2

Notes to Table 7

1 Slave address is 8A (hex) at IICSA = LOW or 8E (hex) at IICSA = HIGH.

2 Dependent on applications (Figures 23 to 38)

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	May 1992

SAA7157

Clock signal generator circuit for digital TV systems (SCGC)

FEATURES

- Clock generation suitable for digital TV systems (line-locked)
- PLL frequency multiplier to generate 4 times of input frequency
- Dividers to generate clocks LL1.5A, LL1.5B, LL3A and LL3B (4th and 2nd multiples of input frequency)
- PLL mode or VCO mode selectable
- Reset control and power fail detection
- Suitable for applications with feature box and picture memory

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8, 17)	4.5	5.0	5.5	V
I_{DDA}	analog supply current	3	-	9	mA
I_{DDD}	digital supply current	10	-	60	mA
V_{LFCO}	LFCO input voltage (peak-to-peak value)	1	-	V_{DDA}	V
f_i	input frequency range	6.0	-	7.25	MHz
V_I	input voltage LOW input voltage HIGH	0 2.0	- -	0.8 V_{DDD}	V V
V_O	output voltage LOW output voltage HIGH	0 2.6	- -	0.6 V_{DDD}	V V
T_{amb}	operating ambient temperature range	0	-	70	°C

GENERAL DESCRIPTION

The SAA7157 generates all clock signals required for a digital TV system suitable for the SAA715x family and the SAA7199B (DENC). The circuit operates in either the phase-locked loop mode (PLL) or voltage controlled oscillator mode (VCO).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7157	20	DIL	plastic	SOT146
SAA7157T	20	mini-pack (SO20)	plastic	SOT163A

Clock signal generator circuit for digital TV systems (SCGC)

SAA7157

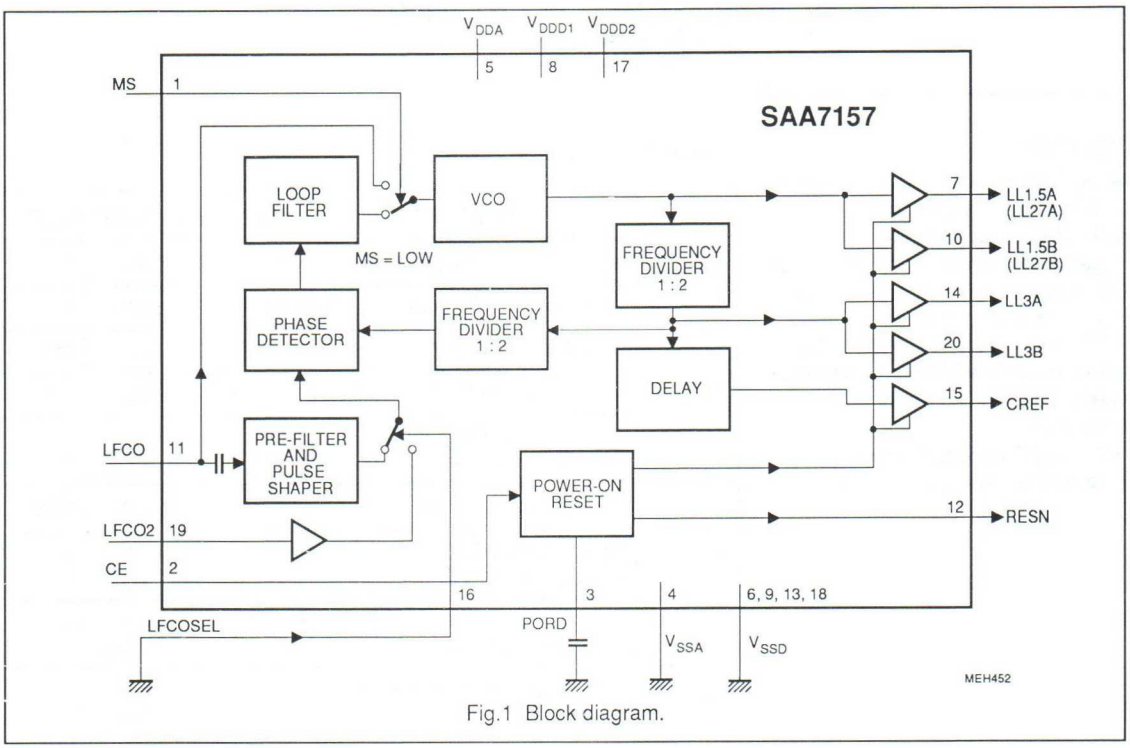


Fig.1 Block diagram.

FUNCTION DESCRIPTION

The SAA7157 generates all clock signals required for a digital TV system suitable for the SAA715x family consisting of an 8-bit analog-to-digital converter (ADC8), digital video multistandard decoder (DMSD2) and video enhancement and D/A processor circuit (VEDA). Optional extras (feature box, video memory etc.) can be driven via external buffers, advantageous for a digital TV system based on display standard conversion concepts.
The 6.75 MHz input signal LFCO (triangular waveform) coming from the DMSD or LFCO2 is multiplied to 27 MHz by the PLL (including phase detector, loop filter, VCO and frequency divider) and output on LL1.5A (pin7) and LL1.5B (pin 10). The 13.5 MHz frequencies are generated by dividers using ratio of 1:2 and are output on LL3A (pin 14) and LL3B (pin 20).

The rectangular output signals have 50 % duty factor. Outputs with equal frequency may be connected together externally. The clock outputs go HIGH during power-on reset (and chip enable) to ensure that no output clock signals are available before the PLL has locked-on.

Mode select MS

The LFCO input signal is directly connected to the VCO at MS = HIGH. The circuit operates as an oscillator and frequency divider. This function is not tested.

Source select LFCOSEL

Line frequency control signal (LFCO) is selected by LFCOSEL input.
LFCOSEL = LOW:
signal from LFCO (pin 11) is selected.
LFCOSEL = HIGH:
signal from LFCO2 (pin 19) is selected.
This function is not tested.

Chip enable CE

The buffer outputs are enabled and RESN is set to HIGH by CE = HIGH (Fig.4).
CE = LOW sets the clock outputs HIGH and RESN output LOW.

CREF output

TV2 digital clock reference output signal. Clock qualifier signal to TV system with 2 times of LFCO or LFCO2 frequency.

Power-on reset

Power-on reset is activated at power-on, when the supply voltage decreases below 3.5 V (Fig.4) or when chip enable is done. The indicator output RESN is LOW for a time determined by capacitor on pin 3. The RESN signal can be applied to reset other circuits of this digital TV system.
The LFCO or LFCO2 input signals have to be applied before RESN becomes HIGH.

Clock signal generator circuit for digital TV systems (SCGC)

SAA7157

PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	mode select input (LOW = PLL mode)
CE	2	chip enable /reset (HIGH = outputs enabled)
PORD	3	power-on reset delay, dependent on external capacitor
V_{SSA}	4	analog ground (0 V)
V_{DDA}	5	analog supply voltage (+5 V)
V_{SSD1}	6	digital ground 1 (0 V)
LL1.5A	7	line-locked clock output signal 1.5A (4 times f_{LFCO})
V_{DDD1}	8	digital supply voltage 1 (+5 V)
V_{SSD2}	9	digital ground 2 (0 V)
LL1.5B	10	line-locked clock output signal 1.5B (4 times f_{LFCO})
LFCO	11	line-locked frequency control input signal 1
RESN	12	reset output (active-LOW, Fig.4)
V_{SSD3}	13	digital ground 3 (0 V)
LL3A	14	line-locked clock output signal 3A (2 times f_{LFCO})
CREF	15	clock reference output, qualifier signal (2 times f_{LFCO})
LFCOSEL	16	LFCO source select (LOW = LFCO selected)*
V_{DDD2}	17	digital supply voltage 2 (+5 V)
V_{SSD4}	18	digital ground 4 (0 V)
LFCO2	19	line-locked frequency control input signal 2*
LL3B	20	line-locked clock output signal 3B (2 times f_{LFCO})

PIN CONFIGURATION

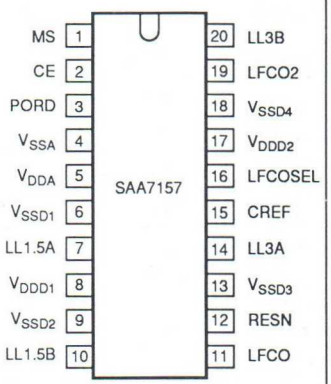


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); ground pins as well as supply pins together connected.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	−0.5	7.0	V
V_{DDD}	digital supply voltage (pins 8 and 17)	−0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{DDA} - V_{DDD}$	-	±100	mV
V_O	output voltage (I_{OM} = 20 mA)	−0.5	V_{DDD}	V
P_{tot}	total power dissipation (DIL20)	0	1.1	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling** for all pins	-	tbf	V

* MS and LFCO2 functions are not tested. LFCO2 is a multiple of horizontal frequency.

** Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal handling precautions appropriate to "Handling MOS devices ".

CHARACTERISTICS

V_{DDA} = 4.5 to 5.5 V; V_{DDD} = 4.5 to 5.5 V; f_{LFCO} = 6.0 to 7.25 MHz and T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8 and 17)		4.5	5.0	5.5	V
I_{DDA}	analog supply current (pin 5)		3	-	9	mA
I_{DDD}	digital supply current ($I_8 + I_{17}$)	note 1	10	-	60	mA
V_{reset}	power-on reset threshold voltage	Fig.4	-	3.5	-	V
Input LFCO (pin 11)						
V_{11}	DC input voltage		0	-	V_{DDA}	V
V_i	input signal (peak-to-peak value)		1	-	V_{DDA}	V
f_{LFCO}	input frequency range		6.0	-	7.25	MHz
C_{11}	input capacitance		-	-	10	pF
Inputs MS, CE, LFCOSEL and LFCO2 (pins 1, 2, 16 and 19); note 3						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}	V
f_{LFCO2}	input frequency range for LFCO2		6.0	-	7.25	MHz
I_{LI}	input leakage current	LFCOSEL	50	-	150	µA
		others	-	-	10	µA
C_I	input capacitance		-	-	5	pF
Output RESN (pin 12)						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.4	-	V_{DDD}	V
t_d	RESN delay time	C_3 = 0.1µF; Fig.4	20	-	200	ms
Output CREF (pin 15)						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.6	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.4	-	V_{DDD}	V
f_{CREF}	output frequency CREF	Fig.3	-	2 $f_{LFCO(2)}$		MHz
C_L	output load capacitance		15	-	40	pF
t_{SU}	set-up time	Fig.3; note 1	12	-	-	ns
t_{HD}	hold time	Fig.3; note 1	4	-	-	ns
Output signals LL1.5A, LL1.5B, LL3A and LL3B (pins 7, 10, 14, and 20); note 3						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.6	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.6	-	V_{DDD}	V
t_{comp}	composite rise time	Fig.3; notes 1 and 2	-	-	8	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{LL}	output frequency LL1.5A	Fig.3	-	4 $f_{LFCO(2)}$		MHz
	output frequency LL1.5B		-	4 $f_{LFCO(2)}$		MHz
	output frequency LL3A		-	2 $f_{LFCO(2)}$		MHz
	output frequency LL3B		-	2 $f_{LFCO(2)}$		MHz
t_r, t_f	rise and fall times	note 1; Fig.3	-	-	5	ns
t_{LL}	duty factor LL1.5A, LL1.5B, LL3A and LL3B (mean values)	note 1; Fig.3; at 1.5 V level	43	50	57	%

Notes to the characteristics

1. f_{LFCO} = 7.0 MHz and output load 40 pF (Fig.3). V_{SSA} and V_{SSD} short connected together.
2. t_{comp} is the rise time from LOW of all clocks to HIGH of all clocks (Fig.3) including rise time, skew and jitter components. Measurements taken between 0.6 V and 2.6 V. Skew between two LLx clocks will not deviate more than ±2 ns if output loads are matched within 20 %.
3. MS and LFCO2 functions not tested.

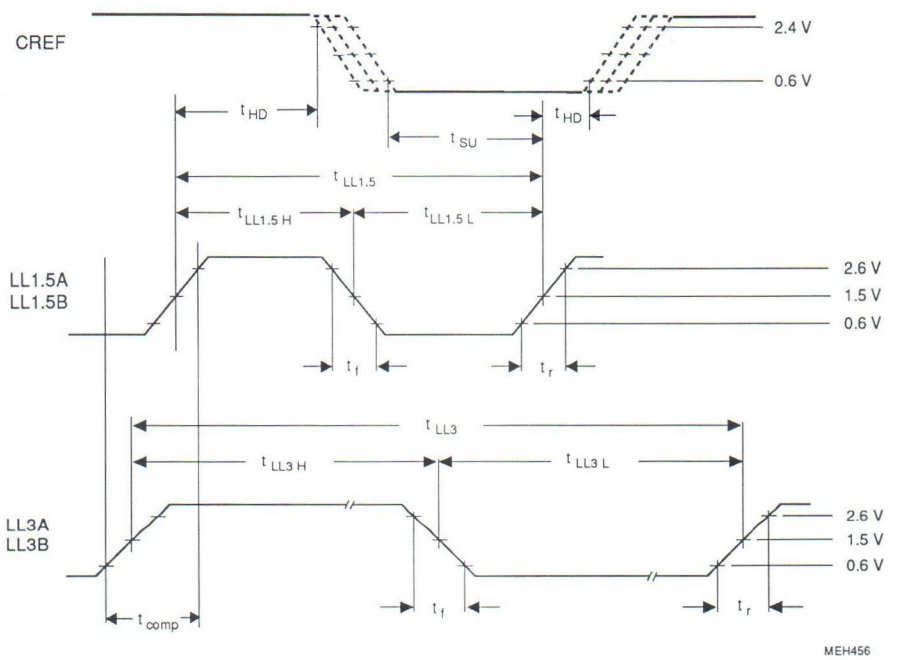


Fig.3 Output timing.

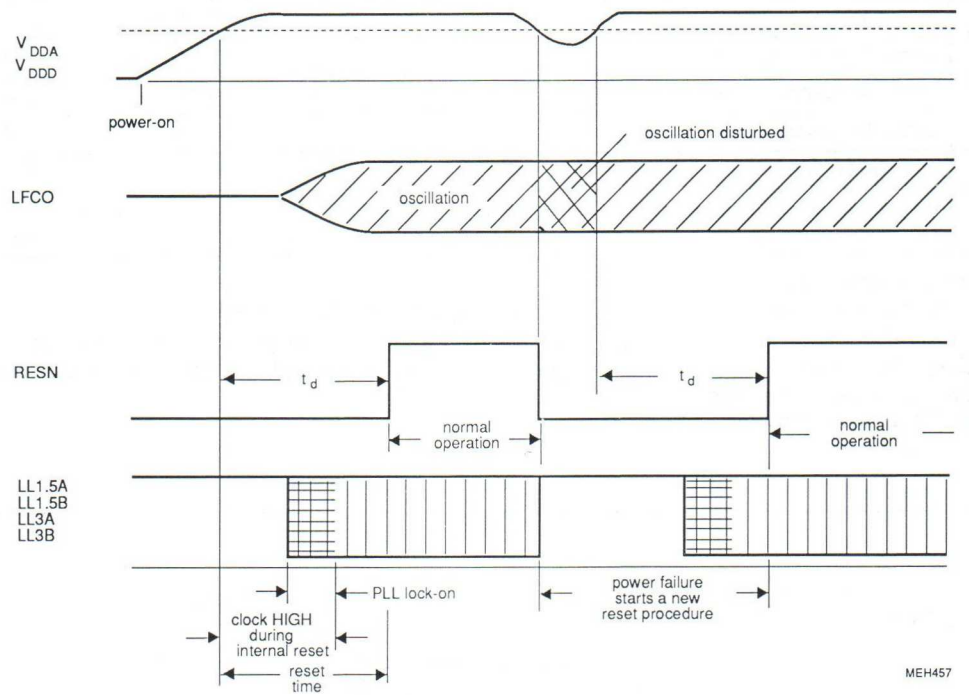


Fig.4 Reset procedure.

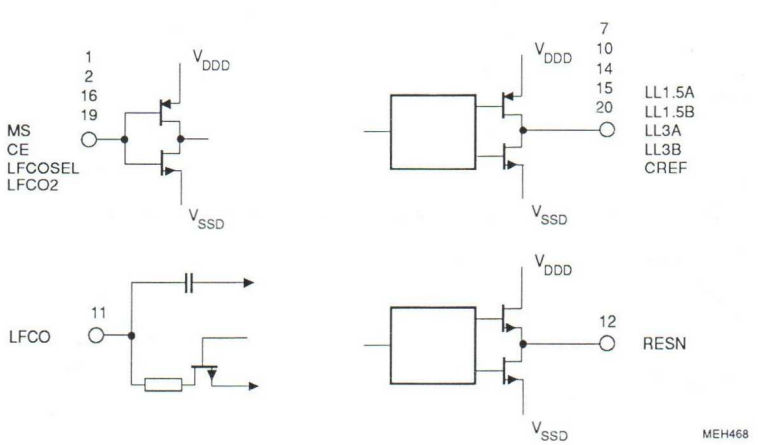


Fig.5 Internal circuit.

Back END IC SAA7158

FEATURES

- Line Flicker Reduction (LFR) by means of MEDIAN filtering
- Vertical zoom
- Digital colour transient improvement
- Digital luminance peaking
- Movie phase detection
- 4:4:4 YUV data throughput selectable, standard is 4:1:1 Y/U/V
- D/A conversion
- UART interface.

GENERAL DESCRIPTION

Application Environment

The Back END IC (abbreviated as BENDIC) is designed to cooperate with an 8051 type of microprocessor, the ECO3 (SAA4951) memory controller and Texas Instruments TMS4C2970 memories, but other configurations may be applicable. Fig.1 shows the block diagram of the feature box. The nominal clock frequency of the IC is 27 MHz or 32 MHz, with a maximum of 36 MHz.

The system supports the digital Y/U/V bus for selection of different video signal sources. The Y/U/V bus and the BENDIC data input are fully synchronous with respect to the clock signal. A line reference signal BLN for timing control purposes has to be provided by external elements which always controls the system timing, independent of active signal sources or desired functions.

Analog Characteristics

The BENDIC contains 3 independent, high speed digital to analog converters for luminance and colour difference signal processing and conversion. The resolution of the two DA converters for the colour difference signals is 8 bit. The luminance peaking up to 6 dB at high frequencies widens the resolution of the luminance channel. To avoid aliasing effects due to time discrete amplitude limiting the resolution of 9-bit is offered for the luminance conversion. All output stages provide high performance output stages for driving lines with low impedance line termination.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	4.5	5.5	V
	analcg supply voltage	4.75	5.25	V
T_{amb}	operating ambient temperature	0	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7158WP	68	PLCC	plastic	SOT188

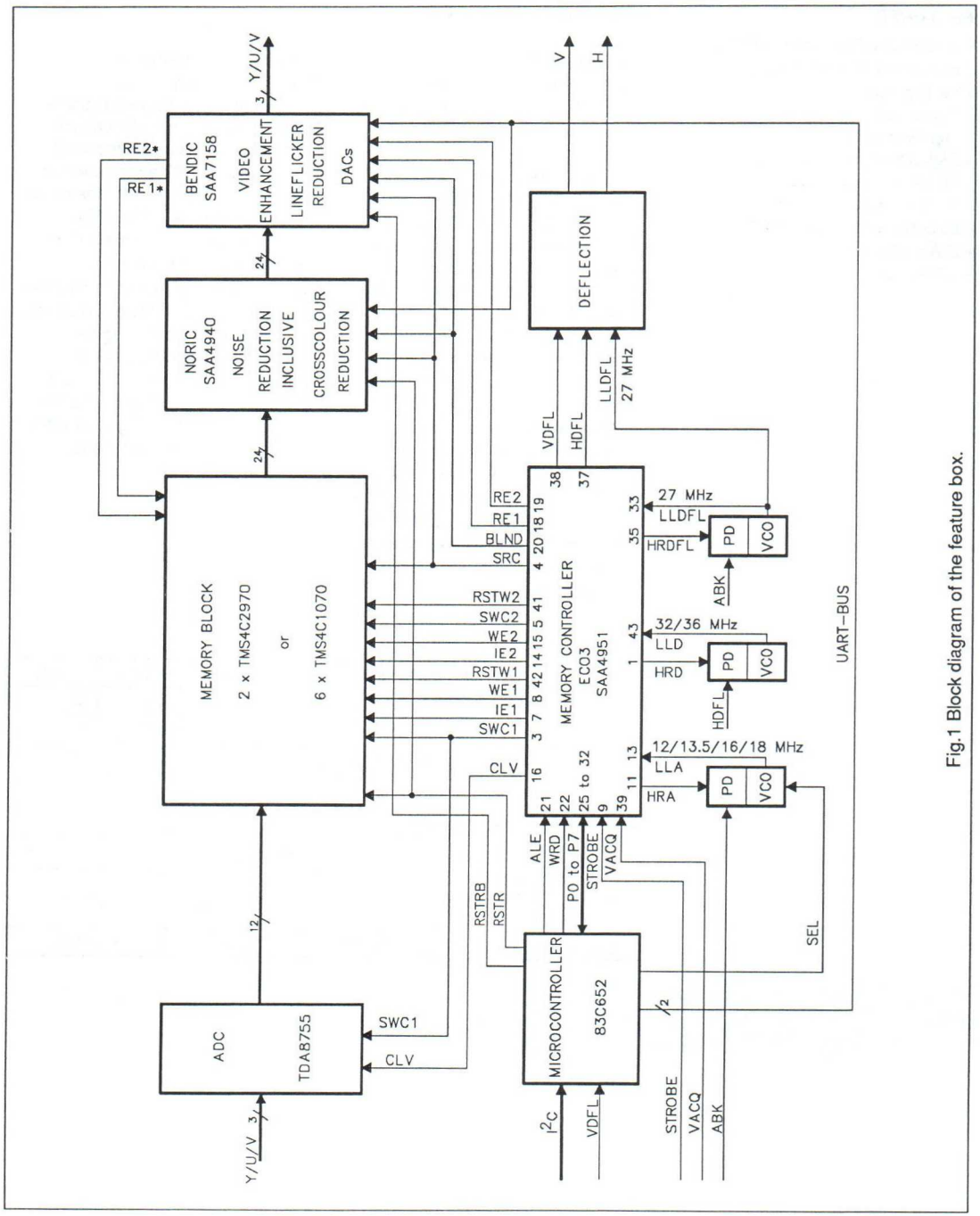


Fig.1 Block diagram of the feature box.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
TEST1/AP	1	input	action pin for testing; to be connected to V_{SS}
Y0-0	2	3-state output	feedback_data to second memory, Y bit 0
Y0-1	3	3-state output	feedback_data to second memory, Y bit 1
Y0-2	4	3-state output	feedback_data to second memory, Y bit 2
Y0-3	5	3-state output	feedback_data to second memory, Y bit 3
Y0-4	6	3-state output	feedback_data to second memory, Y bit 4
Y0-5	7	3-state output	feedback_data to second memory, Y bit 5
V_{DD1}	8	supply	positive digital supply voltage (+5 V)
V_{SS1}	9	ground	digital ground
Y0-6	10	3-state output	feedback_data to second memory, Y bit 6
Y0-7	11	3-state output	feedback_data to second memory, Y bit 7
UV0-0	12	3-state output	feedback_data to second memory, UV bit 0
UV0-1	13	3-state output	feedback_data to second memory, UV bit 1
UV0-2	14	3-state output	feedback_data to second memory, UV bit 2
UV0-3	15	3-state output	feedback_data to second memory, UV bit 3
TEST2/SP	16	input	shift pin for testing; to be connected to V_{SS}
RE2_OUT	17	output	redirected read enable to memory 2
RE1_OUT	18	output	redirected read enable to memory 1
RSTR	19	input	memory read, µP interface and movie detection reset
RE2_IN	20	input	input for read enable to memory 2
RE1_IN	21	input	input for read enable to memory 1
BLN	22	input	blanking signal
µPCL	23	input	clock for interface with 8051 UART, mode 0
µPDA	24	in/output	data for interface with 8051 UART, mode 0
V_{SS2}	25	ground	digital ground
CLK	26	input	master clock, nominal 27 (32) MHz
V_{DD2}	27	supply	positive digital supply voltage (+5 V)
V1-0/Y2-0	28	input	V data, bit 0 in 4:4:4; Y data second memory, bit 0
V1-1/Y2-1	29	input	V data, bit 1 in 4:4:4; Y data second memory, bit 1
V1-2/Y2-2	30	input	V data, bit 2 in 4:4:4; Y data second memory, bit 2
V1-3/Y2-3	31	input	V data, bit 3 in 4:4:4; Y data second memory, bit 3
V1-4/Y2-4	32	input	V data, bit 4 in 4:4:4; Y data second memory, bit 4
V1-5/Y2-5	33	input	V data, bit 5 in 4:4:4; Y data second memory, bit 5
V1-6/Y2-6	34	input	V data, bit 6 in 4:4:4; Y data second memory, bit 6
V1-7/Y2-7	35	input	V data, bit 7 in 4:4:4; Y data second memory, bit 7
U1-0/UV2-0	36	input	U data, bit 0 in 4:4:4; UV data second memory, bit 0
U1-1/UV2-1	37	input	U data, bit 1 in 4:4:4; UV data second memory, bit 1
U1-2/UV2-2	38	input	U data, bit 2 in 4:4:4; UV data second memory, bit 2
U1-3/UV2-3	39	input	U data, bit 3 in 4:4:4; UV data second memory, bit 3
V_{SS3}	40	ground	digital ground
U1-4/UV1-0	41	input	U data, bit 4 in 4:4:4; UV data first memory, bit 0
U1-5/UV1-1	42	input	U data, bit 5 in 4:4:4; UV data first memory, bit 1
U1-6/UV1-2	43	input	U data, bit 6 in 4:4:4; UV data first memory, bit 2
U1-7/UV1-3	44	input	U data, bit 7 in 4:4:4; UV data first memory, bit 3
Y1-0	45	input	Y data first memory, bit 0
Y1-1	46	input	Y data first memory, bit 1
Y1-2	47	input	Y data first memory, bit 2

SYMBOL	PIN	TYPE	DESCRIPTION
Y1-3	48	input	Y data first memory, bit 3
Y1-4	49	input	Y data first memory, bit 4
Y1-5	50	input	Y data first memory, bit 5
Y1-6	51	input	Y data first memory, bit 6
Y1-7	52	input	Y data first memory, bit 7
V_{SUB}	53	analog ground	substrate pin; connect to analog ground (V_{SSA})
RFHY	54	analog input	connect C = 100 nF to analog ground (V_{SSA})
RFLY	55	analog input	connect to analog ground (V_{SSA})
RFLC	56	analog input	connect to analog ground (V_{SSA})
RFHC	57	analog input	connect C = 100 nF to analog ground (V_{SSA})
V_{DDA4}	58	analog supply	analog supply voltage for reference ladders of the three DA converters and for current sources of the output buffers
CUR	59	analog input	current input for analog output buffers (0.4 mA from V_{DDA4} = 5 V); connect with R = 15 kΩ
V_{DDA3}	60	analog supply	analog supply voltage for output buffer AY
AY	61	analog output	analog luminance Y output
V_{SSA3}	62	analog ground	analog ground for output buffer AY
V_{DDA2}	63	analog supply	analog supply voltage for output buffer AU
AU	64	analog output	analog (B–Y) or –(B–Y) output
V_{SSA2}	65	analog ground	analog ground for output buffer AU
V_{SSA1}	66	analog ground	analog ground for output buffer AV
AV	67	analog output	analog (R–Y) or –(R–Y) output
V_{DDA1}	68	supply	analog supply voltage for output buffer AV

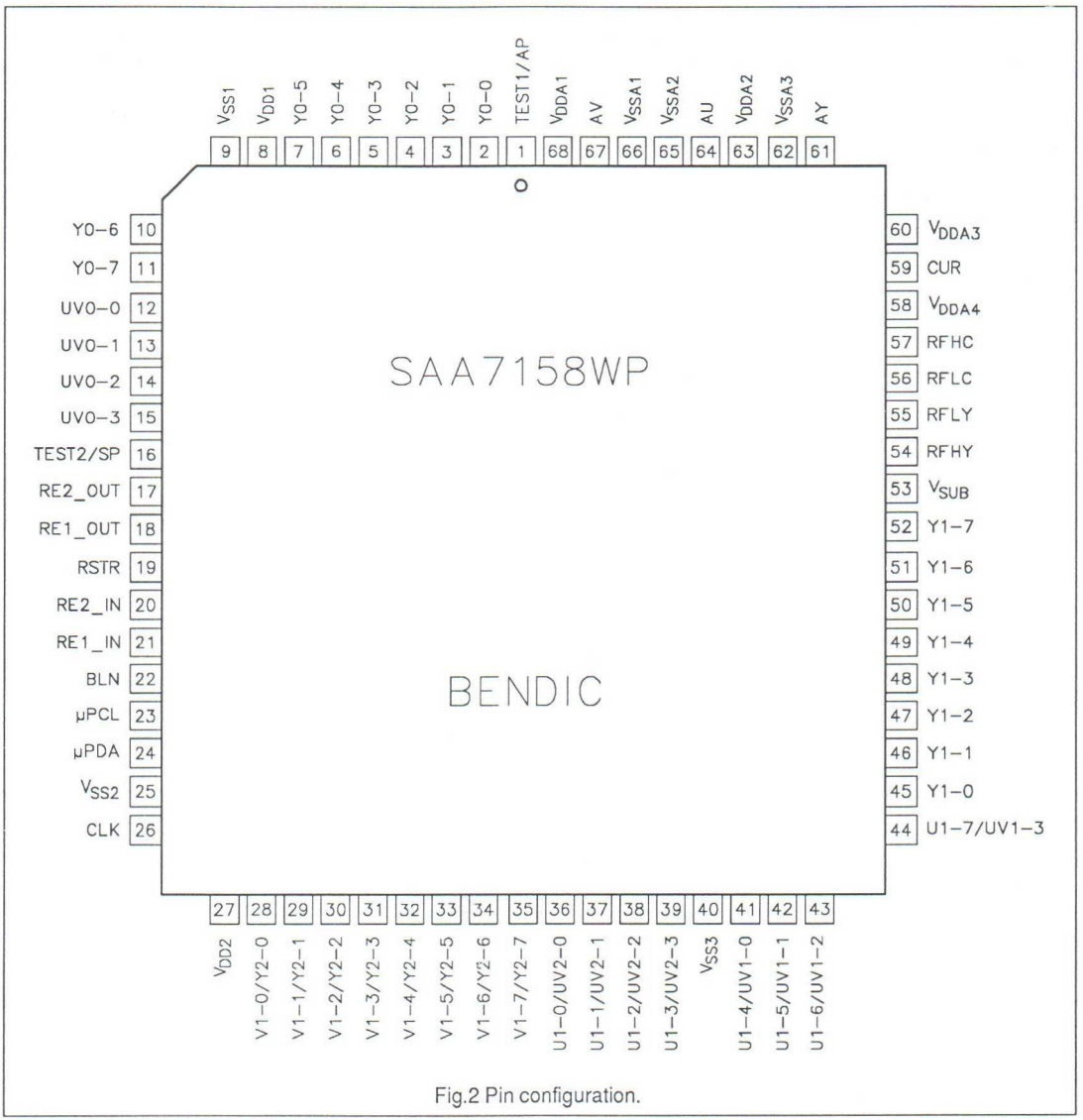


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Block Diagram

The BENDIC will be produced in a CMOS double metal process. It is possible to feed the BENDIC with 8-bit wide luminance and chrominance signals Y/U/V in 4:1:1 mode from the digital Y/U/V bus and to run it in a bypass mode with Y/U/V in 4:4:4 mode without any bandwidth reduction.

The BENDIC contains the processing functions as depicted in Fig.3.

Following functions are available:

Datapath:

- 1H - 4:1:1 line memory, 852 words by 8-bits luminance + 4-bits multiplexed chrominance
- REFORMATTER to get 8-bit wide UV from the Y/U/V bus format
- MIX UV and MIX Y to interpolate between actual and 1H-delayed input signals, programmable for realization of vertical zoom
- MEDIAN filter in luminance processing path for line flicker reduction
- MOVIE PHASE DETECT for supporting line flicker reduction control
- PEAKING for luminance channel
- UPSAMPLING and DCTI for chrominance transient improvement
- HOLD/GREY/BLANK blocks for blanking and grey level insertion
- RE PROCESSING controls read enable for first and second memory, outputs are programmable for different applications
- Data switches for field select, mix/median select, 4:1:1/4:4:4 select
- DAC blocks for digital to analog conversion of Y, U, V video signals
- REGISTER with 3-state control for direct output of Y/U/V 1 input to memories.

Control:

- µP INTERFACE for the control of BENDIC functions, including zoom control
- TIMING CONTROL and TEST as support blocks.

All video data signal processing inside the BENDIC is phaselinear and nonrecursive (except line delay in recirculation mode).

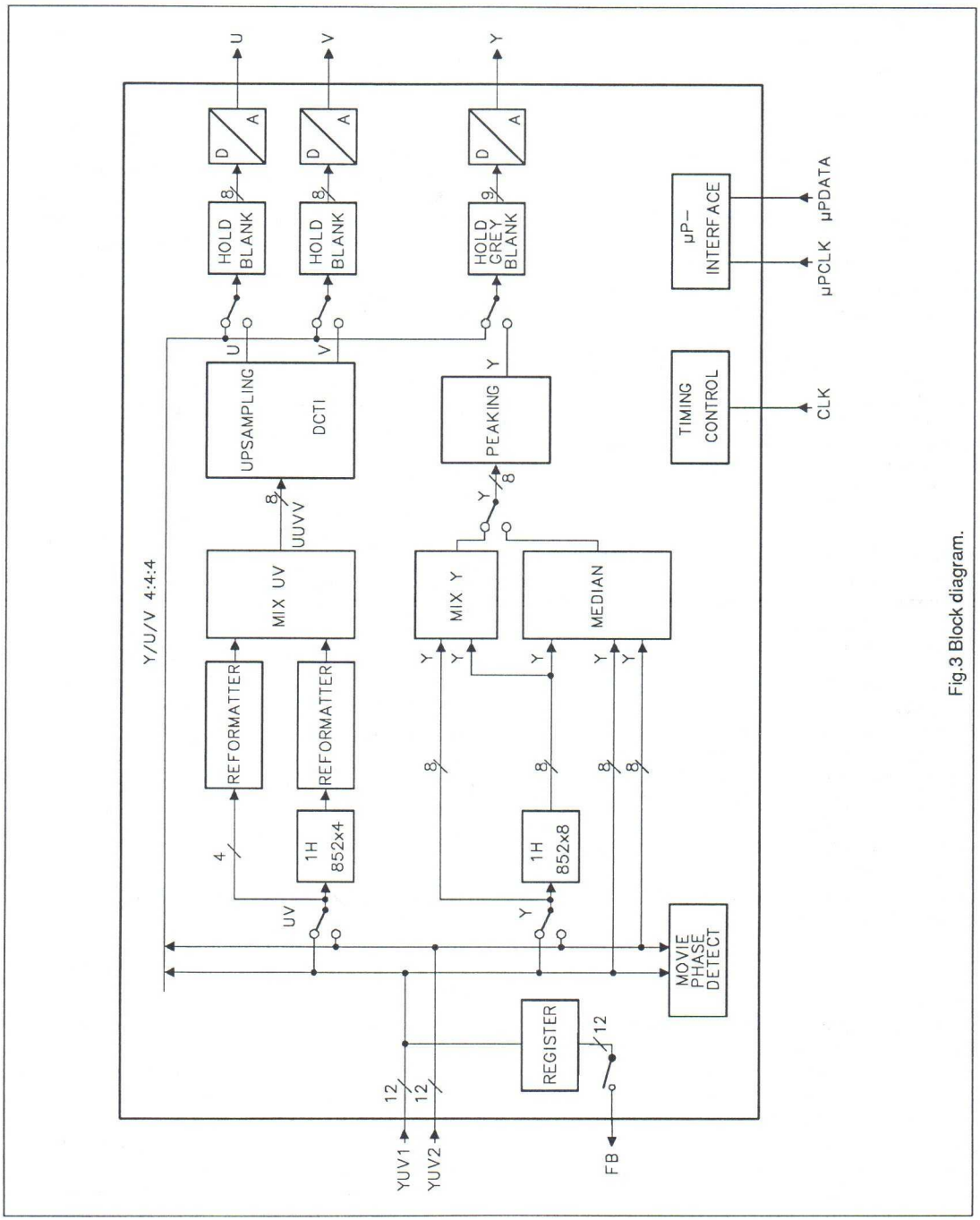


Fig.3 Block diagram.

Data Path Signal processing

- 1H - 4:1:1 line memory, 852 words by 8-bits luminance + 4-bits multiplexed chrominance

The Y/U/V line memory is organized as 852 x 12 bits. It works as a shift register with recirculation mode if desired. The line start is synchronized to RE, and if there are more than 852 words to be stored it will stop and hold.

- REFORMATTER to get 8-bit wide UV from the Y/U/V bus format

The reformatter changes the 4:1:1 format of UV signals into a sequential 8-bit U and V data stream with a sampling rate of half the master clock.

- MIX UV and MIX Y to interpolate between actual and 1H-delayed input signals, programmable for realization of vertical zoom

The function of the MIX-blocks is to interpolate between two input sources A and B (original signal and 1H-delayed signal). Possible interpolation coefficients are $\{1 \text{ or } \frac{3}{4} \text{ or } \frac{1}{2} \text{ or } \frac{1}{4} \text{ or } 0\} \times (A - B) + B$.

- MEDIAN filter in luminance processing path for line flicker reduction

The median filter consists of two different median filters working in parallel with full clock rate. Filters for up and downsampling are implemented with an 8-bit output.

- MOVIE PHASE DETECT for supporting line flicker reduction control

A pixel by pixel luminance level comparison is made on the active video of two consecutive fields from the memory. The absolute difference of the 4 most significant bits of each pixel from the two fields is added to the accumulated value of the current field in a register. The highest significant two bytes thereof are transferred during field blanking period with rising edge of RSTR signal into a register that can be read via the µP interface. After reading the register will be cleared.

- PEAKING for luminance channel

The H-peaking of the luminance channel compensates the bandwidth reduction caused by various components of the TV signal processing chain. Because of the possibility to convert over and undershoots it is even possible to precompensate the si-amplitude attenuation of the D/A converter by 6 dB. The absolutely phaselinear filters can be programmed: frequency response, amplitude of the high frequency signals and degree of coring is controlled via the µP interface. Frequency responses c. f. separate application sheet.

- UPSAMPLING and DCTI for chrominance transient improvement

After upsampling of U and V, in the DCTI block the U and V signals are processed with a look-backwards/look-forwards device. The chrominance signal values are stored in a 26 tap pixel delay line. Controlled by a multiplexer select signal K the values are read from the pixel delay line into the output registers of DCTI. The calculation of the K signal is done within this block. To determine the number of steps to look back and forwards the following relation is used:

$$\frac{d}{dt}\left\{\left|\frac{dU}{dt}\right| + \left|\frac{dV}{dt}\right|\right\}.$$

U and V are processed serially with the same circuitry. The final upsampling towards the master clock for D/A conversion is part of the algorithm and done by linear interpolation between two adjacent taps of choice. It is controlled by the K signal too.

- HOLD/GREY/BLANK blocks for blanking and grey level insertion

The function of these blocks is to insert desired levels for Y, U and V, where no active video is present. BLANKing is performed during line and field blanking period indicated by BLN. GREY is performed where RE indicates that the memory is not read out, and pixel repetition is switched off by the µP interface; the grey value comes via the µP interface. HOLD is performed if pixel repetition is selected by the µP interface; the last value of Y, U and V is kept until RE is active again.

- RE PROCESSING controls read enable for first and second memory

Here the output signals RE1 and RE2 are shifted by adding a programmable delay of 5, 6, 7 or 8 clock pulses with respect to the input signals. In addition RE1 will be influenced in case of zoom.

- data switches for field select, mix/median select, 4:1:1/4:4:4 select

The switches shown in the block diagram Fig.3 are controlled via the µP interface and allow control of the data streams inside the BENDIC.

- DAC blocks for digital to analog conversion of Y, U, V video signals

The D/A conversion is performed in the DAC blocks. The converters consist of the resistor strings to be connected externally and three buffers with a 25 Ω serial resistor at the output built in. To get 75 Ω impedance externally three 50 Ω resistors have to be used near the pins. The capacitive load at the outputs should not exceed 30 pF.

• REGISTER with 3-state control for direct output of Y/U/V 1 input to memories

The 3-state switch with internal register is supplied for the feedback data to the second memory. The feedback bus is a copy of the field1 bus, but with 4 clockpulses delay. 3-state control is done via μP interface.

The control signals

CLK
Line locked clock of maximal 36 MHz.
This is the system clock. Within the BENDIC the CLK signal is distributed to the different blocks.

BLN
Blanking NOT signal.
This signal marks the horizontal and vertical blanking and defines with its rising edge the start phase of the UV 4:1:1 format. A programmable delay of 0, 1, 2 or 3 clock pulses shifts the internal pulse with respect to the input.

RE1_in
Read enable memory 1 signal.
This signal is generated by the memory controller and its HIGH state determines the read enable on the first memory bank, after it is processed by BENDIC for the ZOOM mode and fine shift of the edges.

RE2_in
Read enable memory 2 signal.
This signal is generated by the memory controller and its HIGH state determines the read enable on the second memory bank, including a fine shift of the edges.
note:
RE1_in and RE2_in are processed in the BENDIC to:
– external signals: RE1_out and RE2_out
– RE with correct internal delay to match datapath delays, is used to define the edges between video and side panels (grey insertion or pixel repetition).

RSTR
Reset signal
This signal is transferred (asynchronous with CLK) by e. g. a microprocessor to reset the communication between the microprocessor and the BENDIC. CLK has to be present in this case. In a typical application, RSTR is an active HIGH pulse, issued only in the vertical blanking period. During RSTR HIGH-state, the 'feedback_data' lines are switched to 3-state, temporarily overruling the mode that has been set by the microprocessor. By this provision, RSTR can be used to prevent data collision on the 3-state databus, e. g. during a power on sequence. Also, this signal is used to transfer the 'movie phase detect' data to a register that can be read by the microprocessor.

μPCL
Microprocessor interface clock signal
This signal is transferred (asynchronous with CLK) by a microprocessor (8051, UART mode 0) as communication clock signal at 1 MHz.

μPDA
Microprocessor interface data signal
This signal is transferred or received (asynchronous with CLK) by a microprocessor (8051, UART mode 0) as communication data signal at 1 MBaud, related to μPCL. Data is valid at the rising edge of μPCL.

The external control

The μP interface has the following functions:
– Receive settings from the μP
– Transmit movie phase detect data to the μP
The interface is based on a two wire interface, one for clock, the other for bidirectional data form. It is compatible with the 8051 family UART mode 0 interface. The μP is the master of the communication, it generates the clock (nominal 12 MHz/12 = 1 MHz), only active when transfer is done.
The protocol for the communication is:
8 addressbits are sent by the μP (LSB first), if the address is a write address then 8 databits (LSB first) are sent by the μP, else (if the address is a read address) 8 databits are sent by BENDIC.
RSTR is used to reset the phase of the address/data transfer. The negative going edge of RSTR clears the address register. After reset the first transmitted bit is to be taken as the first (LSB) bit of an address.
For field1/field2 selection and for mix/median selection, 4 addresses are used to select each of the four combinations. A databyte is not obligatory after each of these four addresses, but a dummy databyte is needed if the transmission is to be followed by a further one.

Table 1 Write address table.

ADDRESS (HEX)	FUNCTION	BIT
1	dataformat setting	bit2: invUV
		bit3: UV8bit
		bit4: UVbin
		bit5: Yclip
		bit6: 4:4:4
		bit7: feedback
2	grey value setting	bit4: grey(0)
		bit5: grey(1)
		bit6: grey(2)
		bit7: grey(3)
3	read enable setting	bit0: re1_d(0)
		bit1: re1_d(1)
		bit2: inv_re1
		bit3: re2_d(0)
		bit4: re2_d(1)
		bit5: inv_re2
		bit6: bln_d(0)
		bit 7: bln_d(1)
4	zoom setting	bit0: lps
		bit1: pixrep
		bit2: black16
		bit3: zoom(0)
		bit4: zoom(1)
		bit5: zoom(2)
		bit6: zoom(3)
		bit7: zoom(4)
5	CTI setting	bit4: range(0)
		bit5: range(1)
		bit6: gain(0)
		bit7: gain(1)
6	peaking setting, average UV select	bit0: av_w_med
		bit1: WG(0)
		bit2: WG(1)
		bit3: BFB
		bit4: BP(0)
		bit5: BP(1)
		bit6: coring(0)
		bit7: coring(1)
7C	multiplexer setting	SET select field1 OFF; select median OFF (all databits are dummy)
7D	multiplexer setting	SET select field1 ON; select median OFF (all databits are dummy)
7E	multiplexer setting	SET select field1 OFF; select median ON (all databits are dummy)
7F	multiplexer setting	SET select field1 ON; select median ON (all databits are dummy)

The function of the bits in the control datawords are explained below:

feedback	HI: feedback output is 3-state enabled = outputs active
4:4:4	HI: YUV-4:4:4 mode selected instead of 4:1:1 mode
Yclip	HI: Y signal after peaking is clipped and converted to 9-bit range
UVbin	HI: UV signals are taken from input as binary signals instead 2's complement
UV8bit	HI: UV signals are taken from input as 8-bit values instead of 7-bit
invUV	HI: UV signals are inverted before the DACs (outputs = –U and –V)
grey(3:0)	determines highest 4 bits in shade of grey in side panels
bln_d(1:0)	shifts the internal BLN signal from 0 to 3 clock pulses with respect to input
re2_d(1:0)	shifts 5 to 8 clock pulses the RE2 output signal versus input
re1_d(1:0)	shifts 5 to 8 clock pulses the RE1 output signal versus input, additionally influenced by zoom
inv_re2	HI: RE2 output is polarity reversed in relation to RE2 input
inv_re1	HI: RE1 output is polarity reversed in relation to RE1 input
zoom(4:0)	determines vertical zoom factor, which is (32/zoom(4:0)); zoom(4:0) = 0 is equivalent to no zoom
black16	HI: the Y signal value during the blanking period is 16 instead of 0
pixrep	HI: side panels have the same Y, U and V as on the edge of the last video information
lps	HI: functional test mode for line on line median on/off
range(1:0)	determines maximum in CTI range of looking back/looking forward
gain(1:0)	determines gain of CTI function
coring(1:0)	determines coring level in Y peaking
av_w_med	enable average UV while median in Y (UV := 1/2 x direct + 1/2 x delayed)
BP(1:0)	determines frequency response in Y peaking
WG(1:0)	determines weighted addition in Y peaking with 1 or 1/2 or 1/4 or 0
BFB	HI: determines bypass for BF1 in Y peaking

The BENDIC provides the correlation of two subsequent fields with its 'Movie phase detector' via the μP interface. The MSB or LSB values of this correlation factor is read from the BENDIC by sending an addressbyte and subsequently receiving a databyte from it, according to Table 2.

Table 2 Read address table.

ADDRESS (HEX)	BIT
80	bit0: corr(0)
	bit1: corr(1)
	bit2: corr(2)
	bit3: corr(3)
	bit4: corr(4)
	bit5: corr(5)
	bit6: corr(6)
	bit7: corr(7)

ADDRESS (HEX)	BIT
81	bit0: corr(8)
	bit1: corr(9)
	bit2: corr(10)
	bit3: corr(11)
	bit4: corr(12)
	bit5: corr(13)
	bit6: corr(14)
	bit7: corr(15)

corr(15:0) is the measured Y correlation factor between two successive fields.

CHARACTERISTICS

Specification of input/output and clock levels and timing

The following table shows the specifications of input/output/clock levels and timing for T_{amb} = 0 to +70 °C; V_{DD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD1-2}	digital supply voltages		4.5	–	5.5	V
V_{DDA1-4}	analog supply voltages		4.75	–	5.25	V
I_{DD1-2}	supply current digital		–	–	250	mA
I_{DDA1-4}	supply current analog	note 1	–	–	18	mA
Digital inputs						
V_{IL}	LOW level input voltage		–0.5	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current		–	–	10	µA
C_{IC}	input capacitance (clocks)		–	–	10	pF
C_{ID}	input capacitance (data)		–	–	10	pF
C_{IZ}	input capacitance (I/O in high Z)		–	–	10	pF
Reference and current inputs						
I_{CUR}	input current		–	–	0.4	mA
Digital outputs						
V_{OH}	HIGH level output voltage	note 2	2.4	–	V_{DD1-2}	V
V_{OL}	LOW level output voltage	note 2	0	–	0.6	V
Timing						
t_{CLK}	CLK cycle time		27	–	41	ns
k_{CLK}	CLK duty cycle $t_{CLK-HIGH}/t_{CLK}$		40	–	60	%
t_r	CLK rise time		–	–	5	ns
t_f	CLK fall time		–	–	6	ns
t_{SU}	input data setup time		–	–	5	ns
t_{HD}	input data hold time		–	–	6	ns
t_{OH}	output data hold time	note 2	6	–	–	ns
t_{OD}	output data delay time	note 2	–	–	25	ns
Data output loads (3-state outputs)						
C_{ld}	output load capacitance		10	–	35	pF
Characteristics of the DA converters						
RSL_Y	resolution of the Y DAC		–	9	–	bit
RSL_C	resolution of the U and V DAC		–	8	–	bit
B	analog signal bandwidth (–3 dB)		20	–	–	MHz
CT	crosstalk between channels		–	–	–42	dB
DNL	differential nonlinearity	referred to 8 MSB's	–	–	±0.5	LSB
INL	integral nonlinearity	referred to 8 MSB's	–	–	±1	LSB
V_{out}	output voltage (without load)		–	2 V_{p-p}	–	V

Notes to the characteristics

1. f_{CLK} = 36 MHz, f_{data} = 18 MHz (rectangular full scale); without output load.
2. Timings and levels have to be measured with load circuits 1.2 kΩ connected to 3.0 V (TTL load), and C_L = 25 pF.

APPLICATION NOTE FOR THE ANALOG PART OF BENDIC

The digital to analog conversion is done in parallel for the three channels. The DA converters (8-bit for U and V; 9-bit for Y) are based on resistor strings with low impedance output buffers. They are designed for 2 V_{p-p} unloaded output swing. To avoid integral nonlinearity errors, the minimum output voltage is 200 mV; so the DC range for unloaded output is between 0.2 and 2.2 V.

A serial resistor of 25 Ω is integrated at the outputs of the buffers. With 50 Ω in series - close to the ouput pins - the nominal output voltage for 75 Ω line termination is 1 V_{p-p} with a DC range of 0.1 to 1.1 V. Amplitude matching to external requirements has to be done with external dividers. Capacitance load should not exceed 30 pF.

The DAC's require three separate analog supply voltages V_{DDA1-3} and analog ground lines V_{SSA1-3} for the output buffers.

The accuracy of an external voltage reference input V_{DDA4} directly influences the output amplitude of the video signals.

The current input CUR supplies the output buffers with a current of about 0.3 mA at V_{DDA} = 5 V, if a resistor of 15 kΩ is connected to this pin.

A larger current improves the output bandwidth but makes the integral nonlinearity worse.

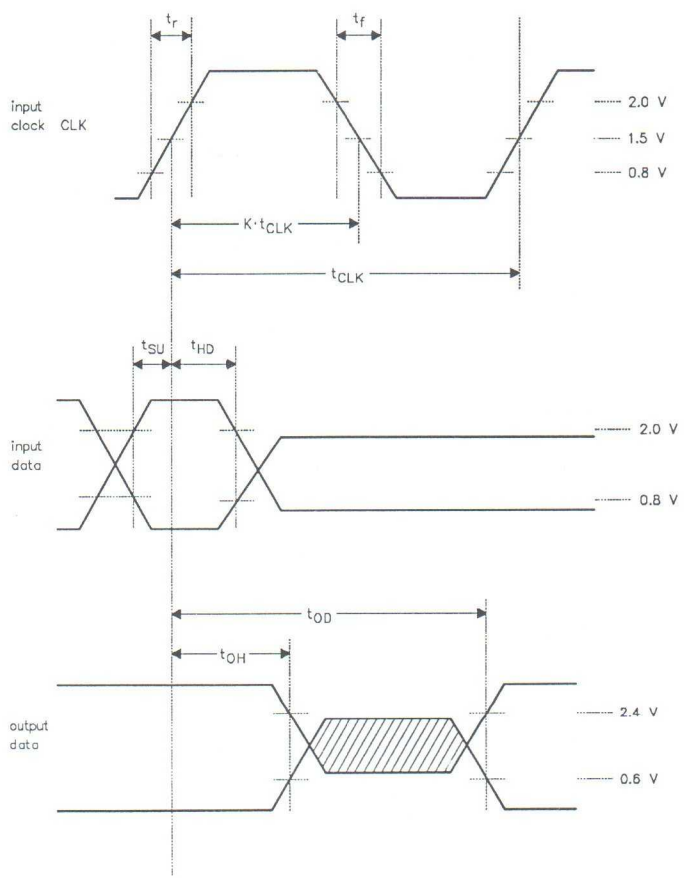


Fig.4 Timing diagram.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	April 1993

SAA7165

Video enhancement and D/A processor (VEDA2)

FEATURES

- CMOS circuit to enhance video data and to convert luminance and colour-difference signals from digital-to-analog
- Digital colour transient improvement block DCTI to increase the sharpness of colour transitions. The improved pin-compatible SAA7165 can supercede the SAA9065.
- 16-bit parallel input for 4:1:1 and 4:2:2 YUV data
- Data clock input LLC (line-locked clock) for a data rate up to 32 MHz
- 8-bit luminance and 8-bit multiplexed colour-difference formats (optional 7-bit formats)
- MC input to support various clock and pixel rates
- Formatter for YUV input data; 4:2:2 format, 4:1:1 format and filter characteristics selectable
- HREF input to determine the active line (number of pixels)
- Controllable peaking of luminance signal
- Coring stage with controllable threshold to eliminate noise in luminance signal
- Interpolation filter suitable for both formats to increase the data rate in chrominance path
- Polarity of colour-difference signals selectable
- All functions controlled via I²C-bus

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage digital part	4.5	5	5.5	V
V_{DDA}	supply voltage analog part	4.75	5	5.25	V
I_{DD}	total supply current	-	tbf	-	mA
V_{IL}	input voltage LOW on YUV-bus	−0.5	-	0.8	V
V_{IH}	input voltage HIGH on YUV-bus	2	-	V_{DDD}+0.5	V
f_{LLC}	input data rate	-	-	32	MHz
$V_{o\ Y,CD}$	output signal Y, ±(R–Y) and ±(B–Y) (peak-to-peak value)	-	2	-	V
$R_{L\ Y,CD}$	output load resistance	125	-	-	Ω
ILE	DC integral linearity error in output signal (8-bit data)	-	-	1	LSB
DLE	DC differential error in output signal (8-bit data)	-	-	0.5	LSB
T_{amb}	operating ambient temperature range	0	-	70	°C

- Separate digital-to-analog converters (9-bit resolution for Y; 8-bit for colour-difference signals)
- 1 V (p-p)/ 75 Ω outputs realized by two resistors
- No external adjustments

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7165	44	PLCC	plastic	SOT187

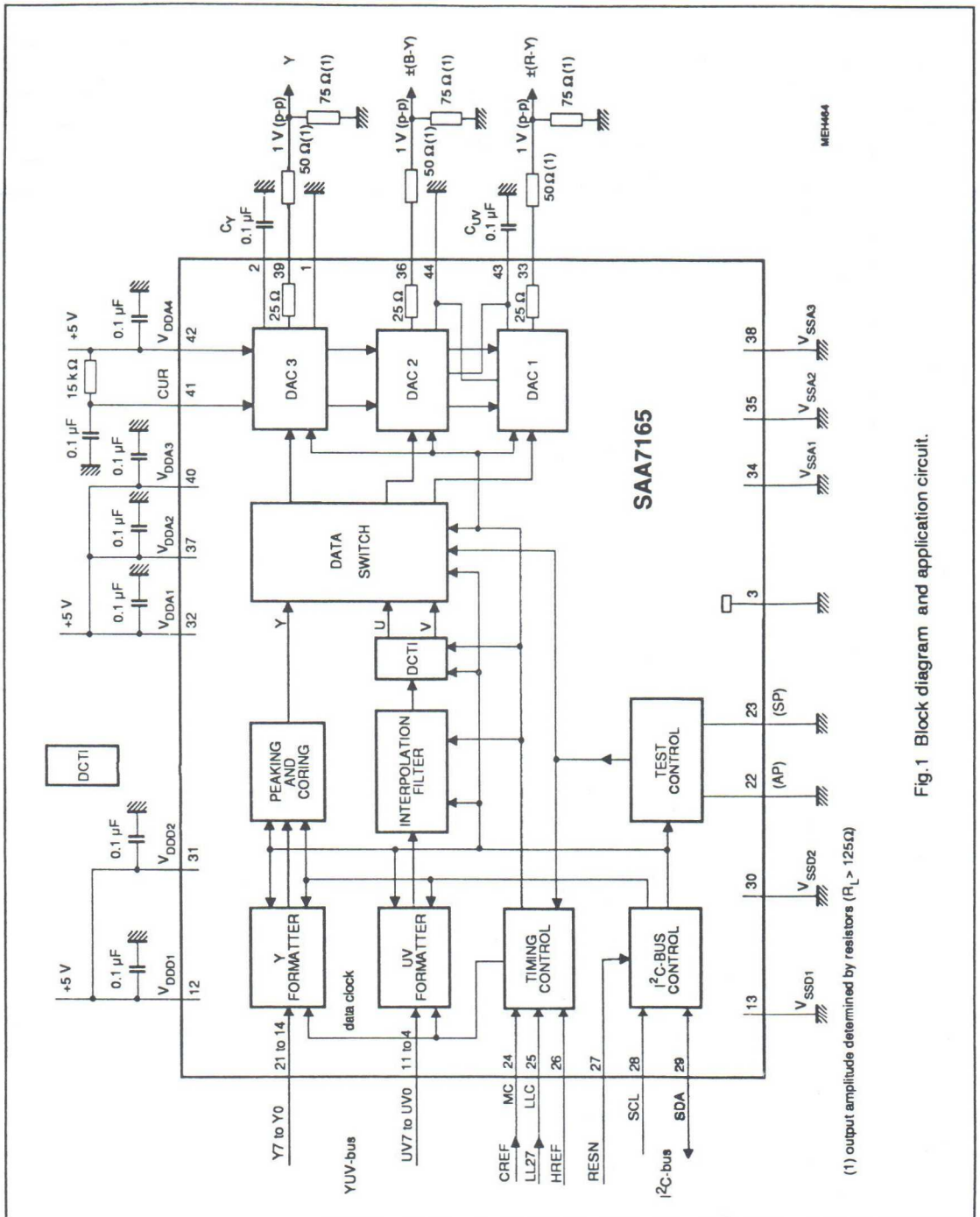


Fig.1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
$REFL_Y$	1	low reference of luminance DAC (connected to V_{SSA1})
C_Y	2	capacitor for luminance DAC (high reference)
SUB	3	substrate (connected to V_{SSA1})
UV0	4	UV signal input bits UV7 to UV0 (digital colour-difference signal)
UV1	5	
UV2	6	
UV3	7	
UV4	8	
UV5	9	
UV6	10	
UV7	11	
V_{DDD1}	12	+5 V digital supply voltage 1
V_{SSD1}	13	digital ground 1 (0 V)
Y0	14	Y signal input bits Y7 to Y0 (digital luminance signal)
Y1	15	
Y2	16	
Y3	17	
Y4	18	
Y5	19	
Y6	20	
Y7	21	
AP	22	connected to ground (action pin for testing)
SP	23	connected to ground (shift pin for testing)
MC	24	data clock CREF (13.5 MHz e. g.); at MC = HIGH the LLC divider-by-two is inactive
LLC	25	line-locked clock signal (LL27 = 27 MHz)
HREF	26	data clock for YUV data inputs (for active line 768Y or 640Y long)
RESN	27	reset input (active LOW)
SCL	28	I^2C-bus clock line
SDA	29	I^2C-bus data line
V_{SSD2}	30	digital ground 2 (0 V)
V_{DDD2}	31	+5 V digital supply voltage 2
V_{DDA1}	32	+5 V analog supply voltage for buffer of DAC 1
(R–Y)	33	±(R–Y) output signal (analog signal)
V_{SSA1}	34	analog ground 1 (0 V)

SYMBOL	PIN	DESCRIPTION
V_{SSA2}	35	analog ground 2 (0 V)
(B–Y)	36	±(B–Y) output signal (analog colour-difference signal)
V_{DDA2}	37	+5 V analog supply voltage for buffer of DAC 2
V_{SSA3}	38	analog ground 3 (0 V)
Y	39	Y output signal (analog luminance signal)
V_{DDA3}	40	+5 V analog supply voltage for buffer of DAC 3
CUR	41	current input for analog output buffers
V_{DDA4}	42	supply and reference voltage for the three DACs
C_{UV}	43	capacitor for chrominance DACs (high reference)
$REFL_{UV}$	44	low reference of chrominance DACs (connected to V_{SSA1})

PIN CONFIGURATION

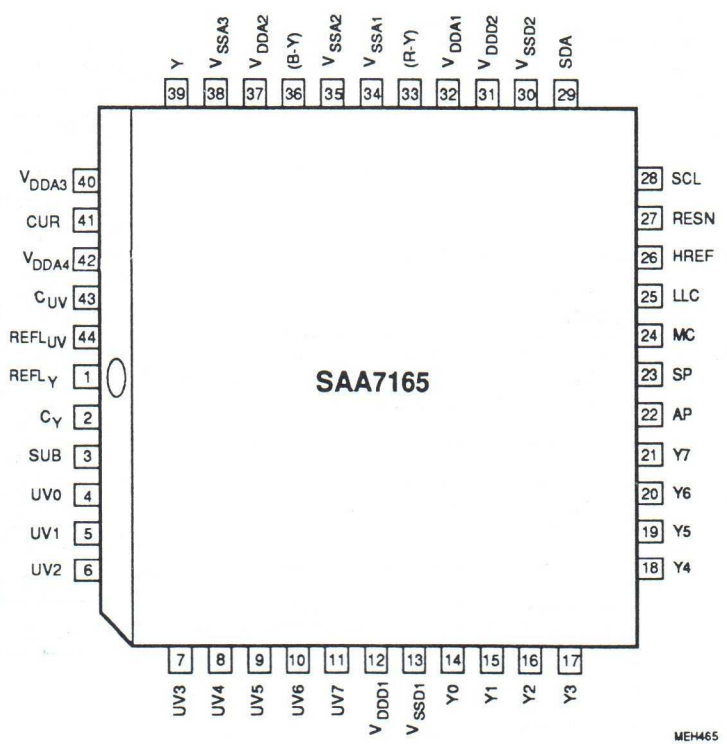


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The CMOS circuit SAA7165 processes digital YUV-bus data up to a data rate of 30 MHz. The data inputs Y7 to Y0 and UV7 to UV0 (Fig.1) are provided with 8-bit data. The data of digital colour-difference signals U and V are in a multiplexed state (serial in 4:2:2 or 4:1:1 format; Tables 2 and 3).

Data is read with the rising edge of LLC (line-locked clock) to achieve a data rate of LLC at MC = HIGH only. If MC is supplied with the frequency CREF (LLC/2 for example), data is read only at every second rising edge (Fig.3). The 7-bit YUV input data are also supported by means of the R78-bit (R78 = 0). Additionally, the luminance data format is converted for internal use into a two's complement format by inverting MSB. The Y input byte (bits Y7 to Y0) represent luminance information; the UV input byte (bits UV7 to UV0) one of the two digital colour-difference signals in 4:2:2 format (Table 2).

The HREF input signal (HREF = HIGH) determines the start and the end of an active line (Fig.3) the number of pixels respectively . The analog output Y is blanked at HREF = LOW, the ±(B–Y) and ±(R–Y) outputs are in a colourless state. The blanking level can be set by the BLV-bit. The SAA7165 is controllable via the I^2C-bus

Y and UV formatters

The input data formats are formatted into the internally used processing formats (separate for 4:2:2 and 4:1:1 formats). The IFF, IFC and IFL bits control the input data format and determine the right interpolation filter (Figures 10 to 13).

Peaking and coring

Peaking is applied to the Y signal to compensate several bandwidth reductions of the external pre-processing. Y signals can be improved to obtain a better sharpness.

There are the two switchable bandpass filters BF1 and BF 2 controlled via the I^2C-bus by the bits BP1, BP0 and BFB. Thus, a frequency response is achieved in combination with the peaking factor K (Figures 5 to 9; K is determined by the bits BFB, WG1 and WG0).

The coring stage with controllable threshold (4 states controlled by CO1 and CO0 bits) reduces noise disturbances (generated by the bandpass gain) by suppressing the amplitude of small high-frequent signal components. The remaining high-frequent peaking component is available for a weighted addition after coring.

Table 1 LLC and MC configuration modes in DMSD applications

PIN	INPUT SIGNAL	COMMENT
LLC MC	LLC (LL27) CREF	The data rate on YUV-bus is half the clock rate on pin LLC, e. g. in SAA7151B, SAA7191 and SAA7191B single scan operation.
LLC MC	LLC (LL27) MC = HIGH	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e. g. in double scan applications.
LLC MC	LLC2/LL3 MC = HIGH	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e. g. SAA9051 single scan operation.
Note: YUV data are only latched with the rising edge of LLC at MC = HIGH.		

INPUT	PIXEL BYTE SEQUENCE					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7(MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Interpolation

The chrominance interpolation filter consists of various filter stages, multiplexers and de-multiplexers to increase the data rate of the colour-difference signals by a factor of 2 or 4. The switching of the filters by the bits IFF, IFC and IFL is described previously. Additional signal samples with significant amplitudes between two consecutive signal samples of the low data rate are generated. The time-multiplexed U and V samples are stored in parallel for converting.

Data switch

The digital signals are adapted to the conversation range. U and V data have 8-bit formats again; Y can have 9 bits dependent on peaking. Blanking and switching to colourless level is applied here. Bits can be inverted by INV-bit to change the polarity of colour-difference output signals.

Digital colour transient improvement (DCTI)

The DCTI circuit improves the transition behaviour of the UV colour-difference signals. As the CVBS signal allows for a 4 : 1 : 1 bandwidth representation only, the DCTI improves the transients to the same performance as signals coming from a 4 : 2 : 2 source – or even more.
In order to obtain the point of inflection, the second derivative of the signal is calculated. The improved transition is centered with respect to the point of inflection of the original signal. Thus, there is no horizontal shift of the resulting signal.

The transition area length to be improved is controlled via I^2C-bus by the bits LI1 and LI0 (Table 4); the sensitivity of the DCTI block is controlled by the bits GA1 and GA0. The CMO bit controls the colour detail sensitivity. It should be set to 1 (ON) if the video signal contains fine colour details (recommended operation mode).

Digital-to-analog converters

Conversion is separate for Y, U and V. The converters use resistor chains with low-impedance output buffers. The minimum output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V floating. An application for 1 V/ 75 Ω on outputs is shown in Fig.1.

Each digital-to-analog converter has its own supply and ground pins suitable for decoupling. The reference voltage, supplying the resistor chain of all three DACs, is the supply voltage V_{DDA4}. The current into pin 41 is 0.3 mA ; a larger current improves the bandwidth but increases the integral non-linearity.

Table 3 Data format 4 : 1 : 1

INPUT	PIXEL BYTE SEQUENCE							
Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			

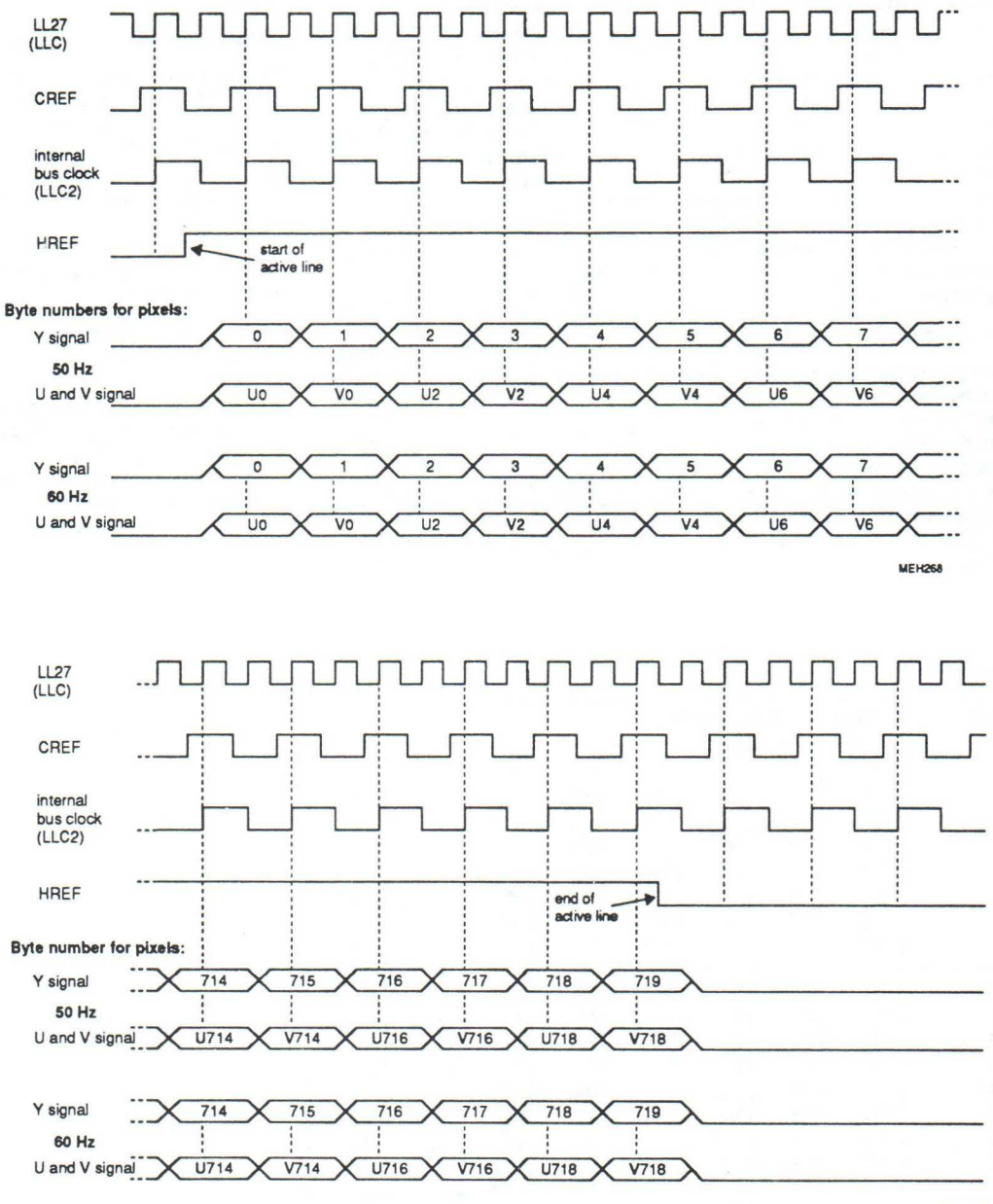


Fig.3 Line control by HREF for 4 : 2 : 2 format, CREF = 13.5 MHz; HREF = 720 pixel; 50 Hz and 60 Hz field.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD1}	supply voltage range (pin 12)	−0.3	7	V
V_{DDD2}	supply voltage range (pin 31)	−0.3	7	V
V_{DDA1}	supply voltage range (pin 32)	−0.3	7	V
V_{DDA2}	supply voltage range (pin 37)	−0.3	7	V
V_{DDA3}	supply voltage range (pin 40)	−0.3	7	V
V_{DDA4}	supply voltage range (pin 42)	−0.3	7	V
$V_{diff\ GND}$	difference voltage $V_{SSD} - V_{SSA}$	-	±100	mV
V_n	voltage on all input pins 4 to 11, 14 to 27 and 41	−0.3	V_{DDD}	V
V_n	voltage on analog output pins 33, 36 and 39	−0.3	V_{DDD}	V
P_{tot}	total power dissipation	0	tbf	mW
T_{stg}	storage temperature range	−55	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	±2000	-	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction-to-ambient in free air	46 K/W

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; LLC = LL27; MC = CREF = 13.5 MHz; T_{amb} = 0 to 70 °C; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD1}	supply voltage range (pin 12)	for digital part	4.5	5	5.5	V
V_{DDD2}	supply voltage range (pin 31)	for digital part	4.5	5	5.5	V
V_{DDA1}	supply voltage range (pin 32)	for buffer of DAC 1	4.75	5	5.25	V
V_{DDA2}	supply voltage range (pin 37)	for buffer of DAC 2	4.75	5	5.25	V
V_{DDA3}	supply voltage range (pin 40)	for buffer of DAC 3	4.75	5	5.25	V
V_{DDA4}	supply voltage range (pin 42)	DAC reference voltage	4.75	5	5.25	V
I_{DDD}	supply current (I_{DDD1} + I_{DDD2})	for digital part	-	tbf	tbf	mA
I_{DDA}	supply current (I_{DDA1} to I_{DDA4})	for DACs and buffers	-	tbf	tbf	mA
YUV-bus inputs (pins 4 to 11 and 14 to 21)		Figures 3 and 4				
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance	V_I = HIGH	-	-	10	pF
I_{LI}	input leakage current		-	-	4.5	µA
Inputs MS1, MS2, MC, LLC, HREF and RESN (pins 22 to 27)						
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance	V_I = HIGH	-	-	10	pF
I_{LI}	input leakage current		-	-	4.5	µA
V_{24}	MC input voltage for LL27	27 MHz data rate	2.0	-	V_{DDD}+0.5	V
	CREF signal on MC input	CREF data rate; note 1	-	-	-	V
I²C-bus SCL and SDA (pins 28 and 29)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3.0	-	V_{DDD}+0.5	V
I_I	input current	V_I = LOW or HIGH	-	-	±10	µA
V_{ACK}	output voltage at acknowledge (pin 29)	I_{29} = 3 mA	-	-	0.4	V
I_{29}	output current	during acknowledge	3	-	-	mA
Digital-to-analog converters (pins 1, 2, 41, 42, 43 and 44)						
V_{DAC}	input reference voltage for internal resistor chains (pin 42)		4.75	5	5.25	V
I_{CUR}	input current (pin 41)	R_{41-42} = 15 kΩ	-	300	-	µA
$V_{1,44}$	reference voltage LOW	pin connected to V_{SSA1}	-	0	-	V
C_L	external blocking capacitor to V_{SSA1} for reference voltage HIGH (pins 2 and 43)		-	0.1	-	µF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{LLC}	data conversation rate (clock)	Fig.3	-	-	32	MHz
Res	resolution	luminance DAC	-	9	-	bit
		chrominance DACs	-	8	-	bit
ILE	DC integral linearity error	8-bit data	-	-	1.0	LSB
DLE	DC differential error	8-bit data	-	-	0.5	LSB
Y, ±(R–Y) and ±(B–Y) analog outputs (pins 39, 33 and 36)						
V_o	output signal voltage (peak-to-peak value)	without load	-	2	-	V
$V_{33,36,39}$	output voltage range	without load; note 2	0.2	-	2.2	V
V_{39}	output blanking level	Y output; note 3	-	16	-	LSB
$V_{33,36}$	output no-colour level	±(R–Y), ±(B–Y); note 4	-	128	-	LSB
$R_{33,36,39}$	internal serial output resistance		-	25	-	Ω
$R_{L\ 33,36,39}$	output load resistance	external load	125	-	-	Ω
B	output signal bandwidth	-3 dB	20	-	-	MHz
t_d	signal delay from input to Y output		-	tbf	-	ns
LLC timing (pins 25)		LLC; Fig.3				
t_{LLC}	cycle time		33	37	41	ns
$t_{p\,H}$	pulse width		40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
YUV-bus timing (pins 4 to 11 and 14 to 21)		Fig.5				
t_{SU}	input data set-up time		11	-	-	ns
t_{HD}	input data hold time		3	-	-	ns
MC timing (pin24)		Fig.5				
t_{SU}	input data set-up time		11	-	-	ns
t_{HD}	input data hold time		3	-	-	ns
RESN timing (pin 27)						
t_{SU}	set-up time after power-on or failure	active LOW; note 5	4 x t_{LLC}	-	-	ns

Notes to the characteristics

1. YUV-bus data is read at MC = HIGH (pin 24) clocked with LLC (Fig.5) . Data is read only with every second rising edge of LLC when CREF = LLC/2 on MC-pin 24.
2. 0.2 to 2.2 V ouput voltage range at 8-bit DAC input data. The data word can increase to 9-bit dependent on peaking factor.
3. The luminance signal is set to the digital black level: 16 LSB for BLV-bit = 0; 0 LSB for BLV-bit = 1.
4. The chrominance amplitudes are set to the digital colourless level of 128 LSB.
5. The circuit is prepared for a new data initialization.

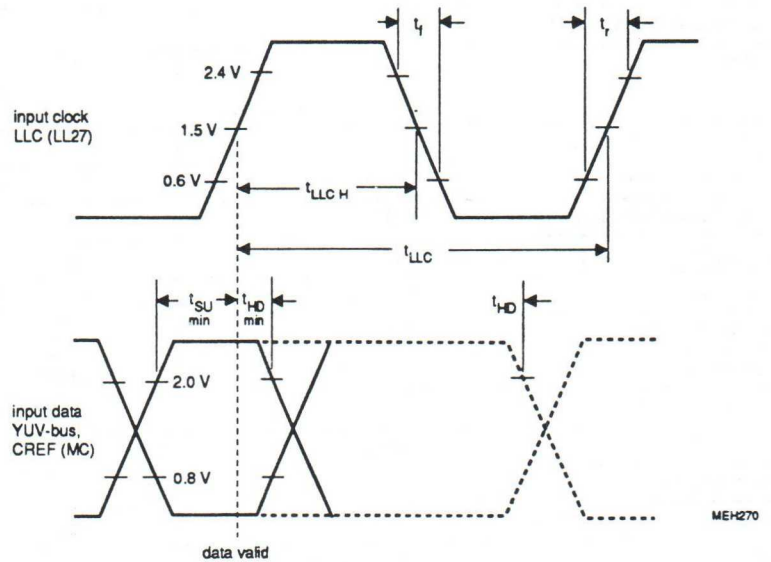


Fig.4 YUV-bus data and CREF timing.

PROCESSING DELAY	LLC CYCLES	REMARKS
YUV digital input to YUV analog output	66 132	at MC = "1" at MC = LLC/2

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = **1011 111X**
A = acknowledge, generated by the slave
SUBADDRESS* = subadress byte (Table 4)
DATA = data byte (Table 4)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 4 I²C-bus transmission

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Peaking and coring	01	AFB	CO1	CO0	BP1	BP0	BFB	WG1	WG0
Input formats; interpolation	02	IFF	IFC	IFL	CMO	LI1	LI0	GA1	GA0
Input/output setting	03	0	0	DC1	DC0	DRP	BLV	R78	INV

Bit functions in data bytes:

"01"
CO1 and CO0 — Control of coring threshold:

CO1	CO0	
0	0	coring off
0	1	small noise reduction
1	0	medium noise reduction
1	1	high noise reduction

AFB, BP1, BP0, BFB — Bandpass filter selection:

AFB	BP1	BP0	BFB	
X	0	0	0	characteristic Fig.5
X	0	1	0	characteristic Fig.6
X	1	0	0	characteristic Fig.7
X	1	1	0	characteristic Fig.8
0	X	X	1	BF1 filter bypassed Fig.9(a)
1	X	X	1	BF1 filter bypassed Fig.9(b)

BFB, WG1 and WG0 — Peaking factor K:

BFB	WG1	WG0	
0	0	0	K = 1/8; minimum peaking
0	0	1	K = 1/4
0	1	0	K = 1/2
0	1	1	K = 1; maximum peaking
1	0	0	K = 0; peaking off
1	0	1	K = 1/4; minimum peaking
1	1	0	K = 1/2
1	1	1	K = 1; maximum peaking

"02" IFF, IFC, IFL — Input format and filter control at 13.5 MHz data rate:

IFF	IFC	IFL	
0	0	0	4 : 1 : 1 format; –3 dB attenuation at 1.6 MHz video frequency; Fig.10
0	0	1	4 : 1 : 1 format; –3 dB attenuation at 600 kHz video frequency; Fig.11
0	1	X	4 : 1 : 1 format; –3 dB attenuation at 1.2 MHz video frequency; Fig.12
1	0	0	4 : 2 : 2 format; –3 dB attenuation at 1.6 MHz video frequency; Fig.10
1	0	1	4 : 2 : 2 format; –3 dB attenuation at 600 kHz video frequency; Fig.11
1	1	X	4 : 2 : 2 format; –3 dB attenuation at 2.5 MHz video frequency; Fig.13

CMO — Choice modulation: 0 = modulation off; 1 = modulation on

LI1 and LI0 — DCTI timing range:

LI1	LI0	range
0	0	+4 / –4
0	1	+6 / –6
1	0	+8 / –8
1	1	+12 / –12

GA1 and GA0 — DCTI gain factor:

GA1	GA0	factor
0	0	off
0	1	1/4
1	0	1/2
1	1	1

"03" DC1 and DC0 — Delay compensation of luminance signal:

DC1	DC0	delayed clock cycles
0	0	0
0	1	+1
1	0	–2
1	1	–1

DRP	UV input data code:	0 = two's complement; 1 = offset binary
BLV	Blanking level on Y output:	0 = 16 LSB; 1 = 0 LSB
R78	YUV input data solution:	0 = 7-bit data; 1 = 8-bit data
INV	Polarity of colour-difference output signals:	0 = normal polarity equal to input signal 1 = inverted polarity



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

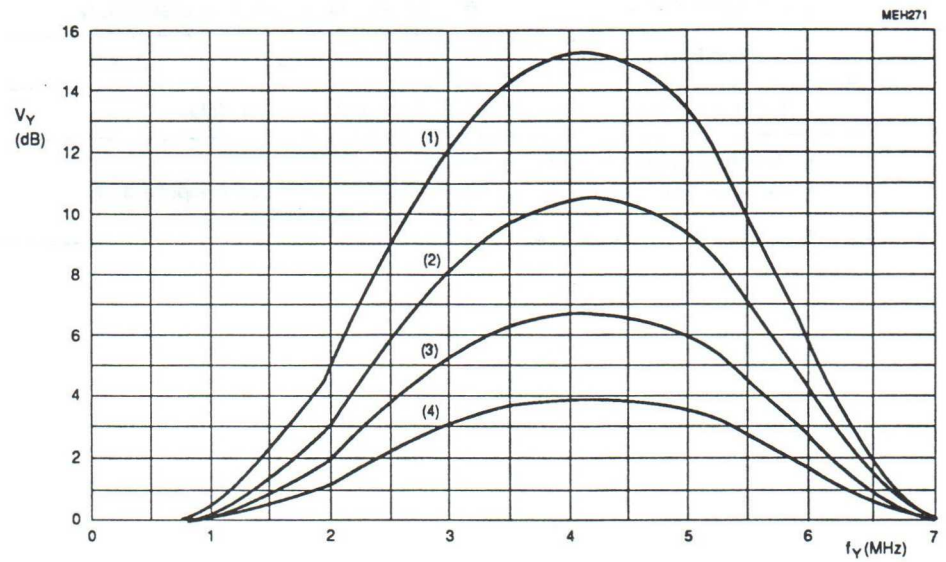


Fig.5 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 0 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

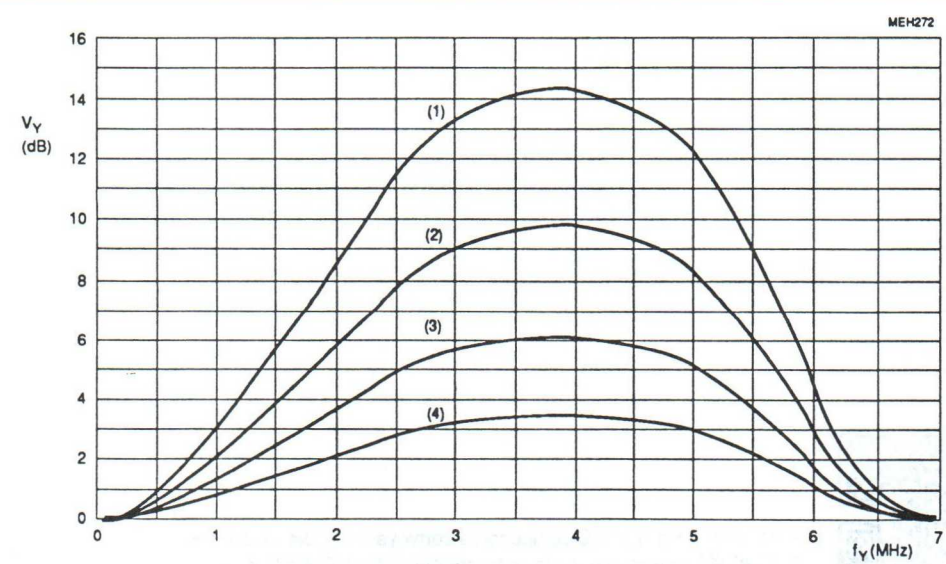


Fig.6 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 1 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

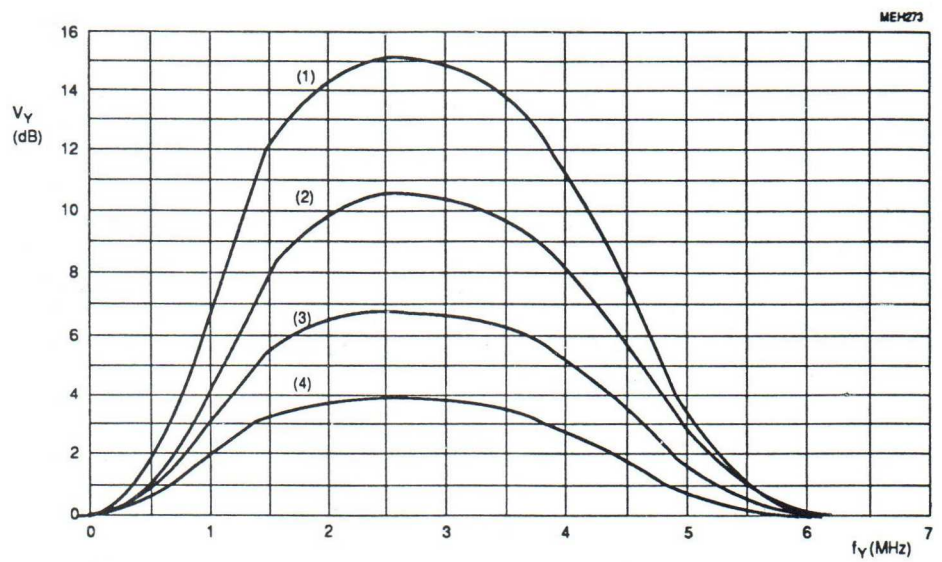


Fig.7 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 0 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

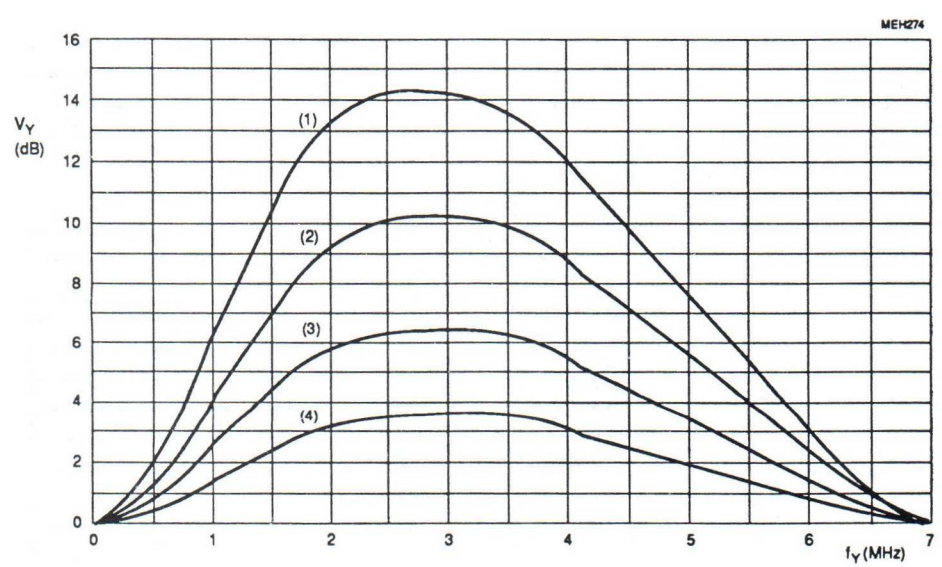


Fig.8 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 1 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

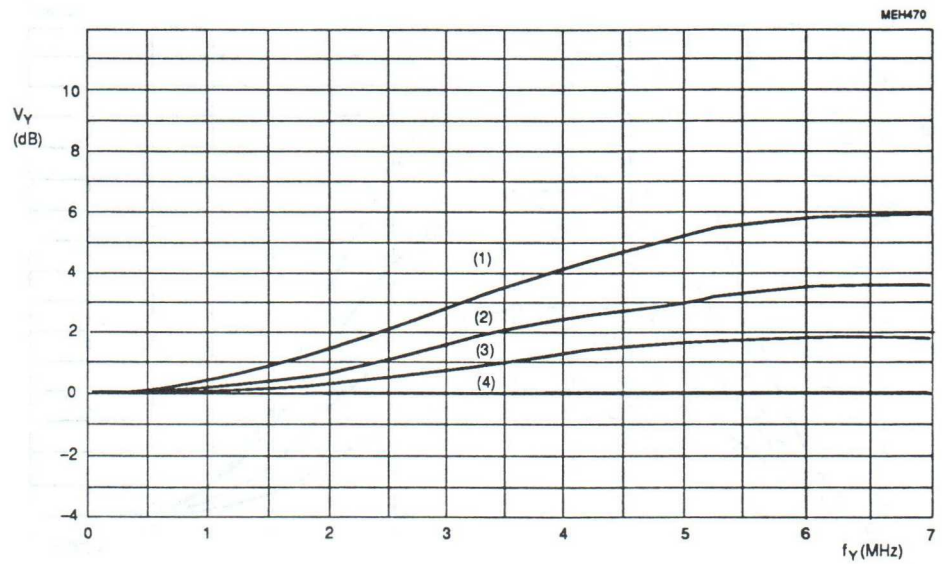


Fig.9(a) Peaking frequency response with I²C-bus control bits AFB = 0, BP1 = 0, BP0 = 0 and BFB = 1; bandpass filter BF1 bypassed and peaking off; (1) K = 1, (2) K = 1/2, (3) K = 1/4 and (4) K = 0

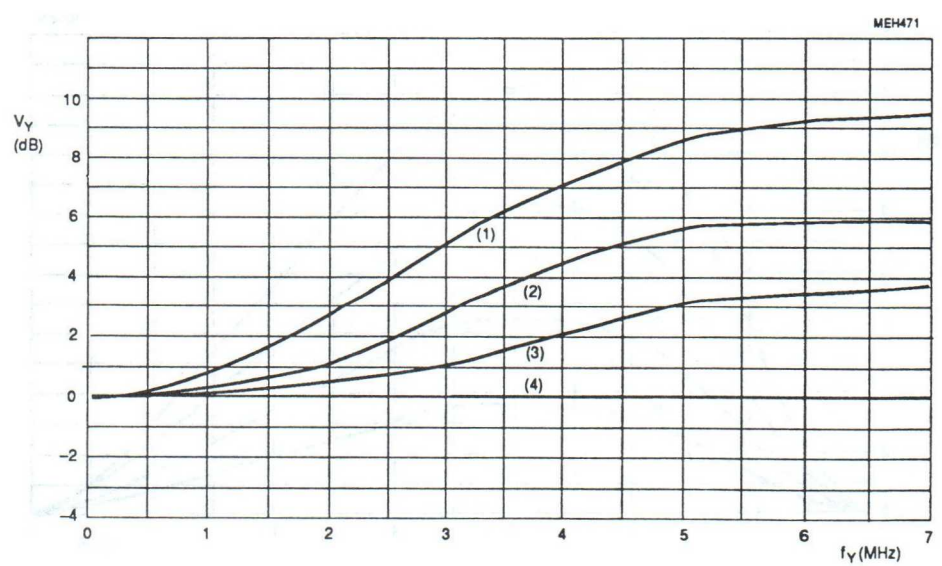


Fig.9(b) Peaking frequency response with I²C-bus control bits AFB = 1, BP1 = 0, BP0 = 0 and BFB = 1; bandpass filter BF1 bypassed and peaking off; (1) K = 1, (2) K = 1/2, (3) K = 1/4 and (4) K = 0.

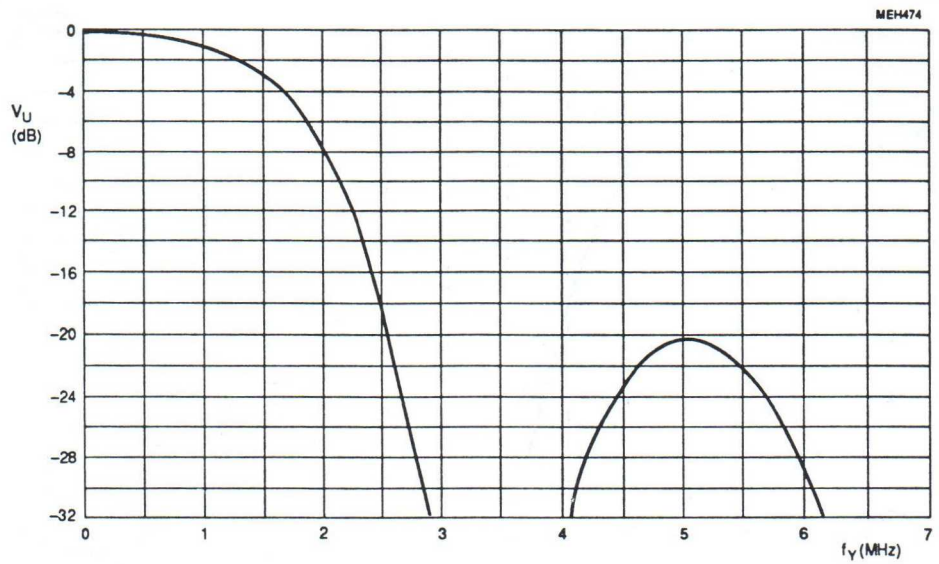


Fig.10 Interpolation filter at DCTI off with I²C-bus control bits IFF = 0; IFC = 0 and IFL = 0 in 4:1:1 format and control bits IFF = 1; IFC = 0 and IFL = 0 in 4:2:2 format; 13.5 MHz data rate.

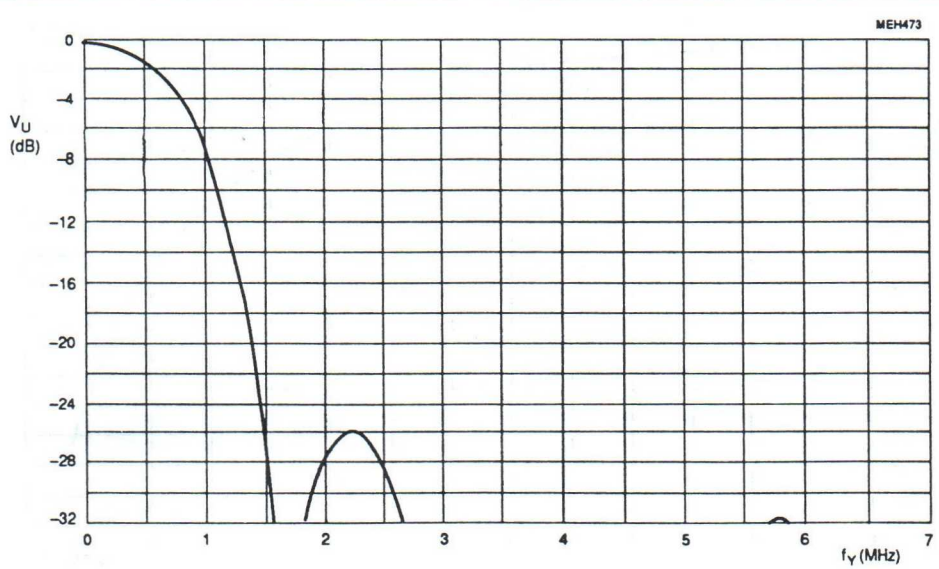


Fig.11 Interpolation filter at DCTI off with I²C-bus control bits IFF = 0; IFC = 0 and IFL = 1 in 4:1:1 format and control bits IFF = 1; IFC = 0 and IFL = 1 in 4:2:2 format; 13.5 MHz data rate.

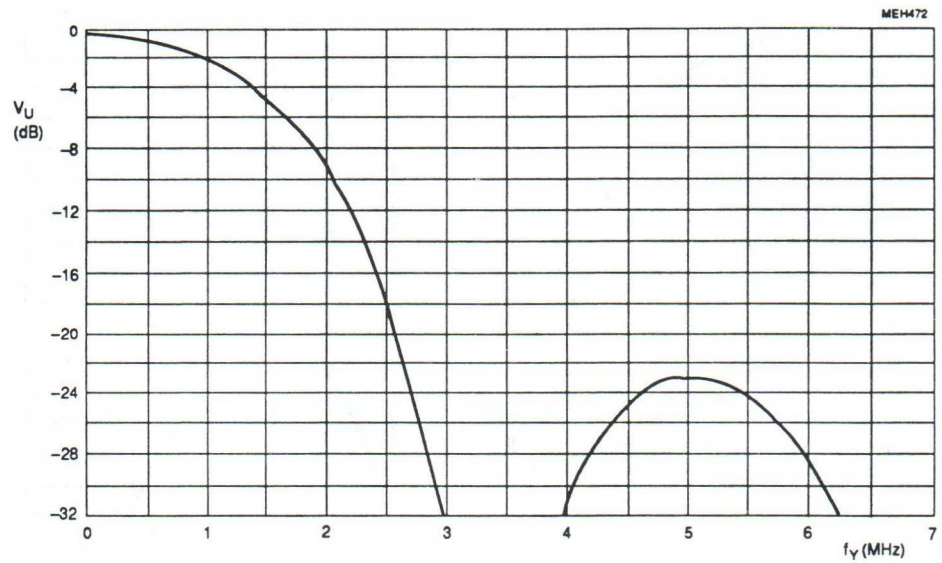


Fig.12 Interpolation filter at DCTI off with I²C-bus control bits IFF = 0; IFC = 1 and IFL = 0 in 4:1:1 format; 13.5 MHz data rate.

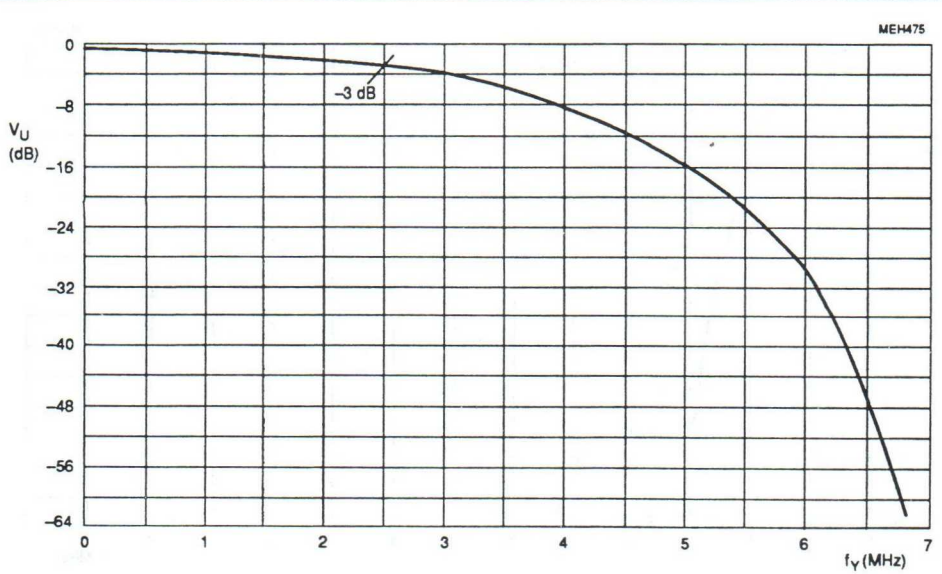


Fig.13 Interpolation filter with I²C-bus control bits IFF = 1; IFC = 1 and IFL = X in 4:2:2 format; 13.5 MHz data rate.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	April 1992

SAA7169

35 MHz triple 9-bit D/A converter for high-speed video

FEATURES

- CMOS circuit to convert high-speed video data from digital to analog
- Three equal 9-bit digital-to-analog converters
- Input signals TTL-compatible
- Input registers for positive edge-triggered data signals
- Clock frequency for a conversion rate up to 35 MHz
- 20 MHz analog bandwidth
- 2 V (p-p) analog output voltage range without load on output (0.2 to 2.2 V DC)
- 1 V / 75 Ω outputs (0.1 to 1.1 V DC); Fig.1
- No de-glitching circuit required
- Typical 225 mW power dissipation

GENERAL DESCRIPTION

The triple high-speed D/A converter can be used in applications for

- desktop video processing
- digital television
- graphic displays
- television decoders
- general high frequency conversion

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage digital part	4.5	5	5.5	V
V_{DDA}	supply voltage analog part	4.75	5	5.25	V
$I_{DD\ tot}$	total supply current	-	-	38	mA
V_I	data input levels	TTL-compatible			
f_{CLK}	conversion frequency	1	-	35	MHz
V_o	nominal output amplitude on pins 1, 3, 43 (peak-to-peak value)	-	2	-	V
B	bandwidth (–3 dB)	20	-	-	MHz
DNL	differential non-linearity	-	-	±0.5	LSB
INL	integral non-linearity	-	-	±0.2	%
α_{CR}	crosstalk attenuation	48	-	-	dB
R_o	internal serial output resistance	-	25	-	Ω
R_L	output load resistance	125	-	-	Ω
T_{amb}	operating ambient temperature range	0	-	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7169	44	PLCC	plastic	SOT187

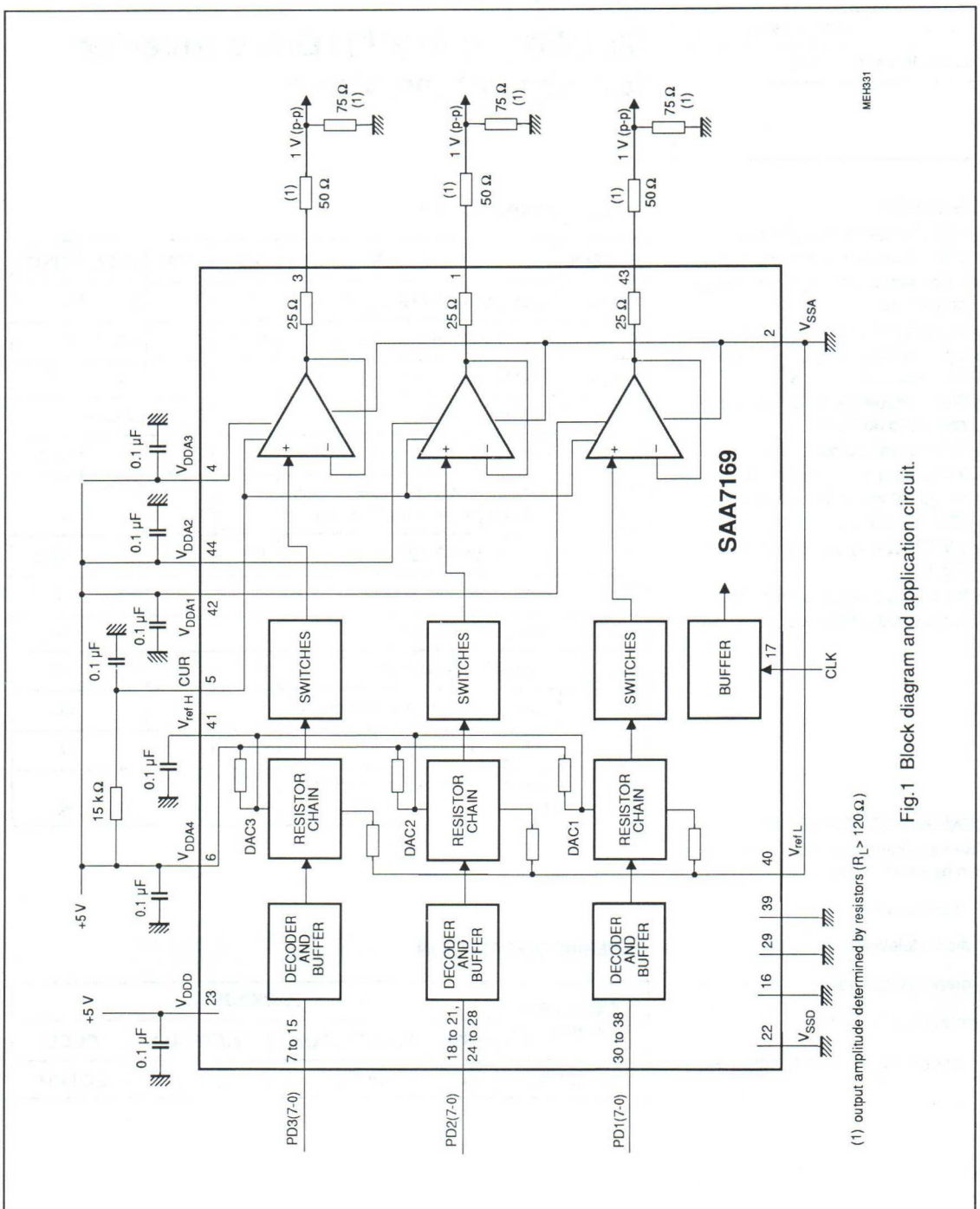


Fig.1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{o\,2}$	1	analog output voltage of channel 2
V_{SSA}	2	analog ground (0 V)
$V_{o\,3}$	3	analog output voltage of channel 3
V_{DDA3}	4	+5 V supply voltage for buffer amplifier of channel 3
CUR	5	current input for analog output buffers, decoupled to V_{SSA}
V_{DDA4}	6	+5 V supply voltage for analog reference part
PD3(8)	7	9-bit data input of channel 3
PD3(7)	8	
PD3(6)	9	
PD3(5)	10	
PD3(4)	11	
PD3(3)	12	
PD3(2)	13	
PD3(1)	14	
PD3(0)	15	
i.c.	16	connect to digital ground (input not used)
CLK	17	clock frequency input
PD2(8)	18	9-bit data input of channel 2 (bits PD2(8-5))
PD2(7)	19	
PD2(6)	20	
PD2(5)	21	
V_{SSD}	22	digital ground (0 V)
V_{DDD}	23	+5 V supply voltage for digital part
PD2(4)	24	9-bit data input of channel 2 (bits PD2(4-0))
PD2(3)	25	
PD2(2)	26	
PD2(1)	27	
PD2(0)	28	
i.c.	29	connect to digital ground (input not used)
PD1(8)	30	9-bit data input of channel 1 (bits PD1(8-4))
PD1(7)	31	
PD1(6)	32	
PD1(5)	33	
PD1(4)	34	

SYMBOL	PIN	DESCRIPTION
PD1(3)	35	9-bit data input of channel 1 (bits PD1(3-0))
PD1(2)	36	
PD1(1)	37	
PD1(0)	38	
i.c.	39	connect to digital ground (input not used)
$V_{ref\ L}$	40	reference voltage LOW; analog ground (V_{SSA})
$V_{ref\ H}$	41	internal generated reference voltage HIGH, decoupled to V_{SSA}
V_{DDA1}	42	+5 V supply voltage for buffer amplifier of channel 1
$V_{o\ 1}$	43	analog output voltage of channel 1
V_{DDA2}	44	+5 V supply voltage for buffer amplifier of channel 2

PIN CONFIGURATION

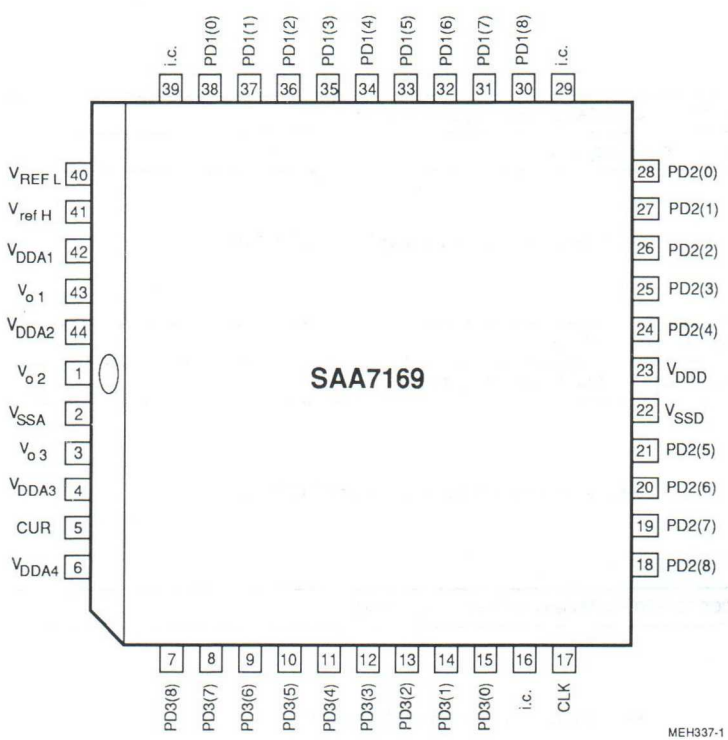


Fig.2 Pin configuration.

35 MHz triple 9-bit D/A converter for high-speed video

SAA7169

FUNCTIONAL DESCRIPTION

The integrated monolithic CMOS circuit SAA7169 is a triple 9-bit digital-to-analog converter for high-speed video applications. Its three channels are equal. The maximum conversion rate is 35 MHz.

The converters use a combination of resistor chains with low-impedance output buffers. The bottom output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V. Fig.1 shows the application for 1 V/ 75 Ω outputs, using the serial 25 Ω + 50 Ω resistors.

Each digital-to-analog converter has its own supply pin for purpose of decoupling. V_{DDA4} is the supply voltage for the resistor chains of the three DACs. The accuracy of this supply voltage influences directly the output amplitudes.
The current CUR into pin 5 is 0.3 mA (V_{DDA4} = 5 V, R_{5-6} = 15 kΩ); a larger current improves the bandwidth but increases the integral non-linearity.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage range (pin 23)	−0.3	7	V
V_{DDA1}	analog supply voltage range (pin 42)	−0.3	7	V
V_{DDA2}	analog supply voltage range (pin 44)	−0.3	7	V
V_{DDA3}	analog supply voltage range (pin 4)	−0.3	7	V
V_{DDA4}	analog supply voltage range (pin 6)	−0.3	7	V
$V_{diff\ GND}$	difference voltage $V_{SSD} - V_{SSA(1\ to\ 4)}$	-	±100	mV
V_n	voltage on all input pins 7 to 15, 18 to 21 and 24 to 40	−0.3	V_{DDD}	V
P_{tot}	total power dissipation	0	tbf	mW
T_{amb}	operating ambient temperature range	0	70	°C
T_{stg}	storage temperature range	−65	150	°C
V_{ESD}	electrostatic handling* for all pins	±2000	-	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; CLK = 35 MHz; f_{DATA} = 17.5 MHz (squarewave, full scale); T_{amb} = 0 to 70 °C; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage range (pin 23)	for digital part	4.5	5	5.5	V
V_{DDA1}	supply voltage range (pin 42)	for buffer of DAC 1	4.75	5	5.25	V
V_{DDA2}	supply voltage range (pin 44)	for buffer of DAC 2	4.75	5	5.25	V
V_{DDA3}	supply voltage range (pin 4)	for buffer of DAC 3	4.75	5	5.25	V
V_{DDA4}	supply voltage range (pin 6)	DAC reference voltage	4.75	5	5.25	V
I_{DDD}	supply current	for digital part; note 1	-	-	20	mA
I_{DDA}	supply current (I_{DDA1} to I_{DDA4})	without load on outputs	-	-	18	mA
9-bit data inputs (pins 7 to 15; 18 to 21, 24 to 28 and 30 to 38)						
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance		-	-	10	pF
I_{leak}	input leakage current		-	-	10	µA
t_{SU}	data set-up time	Fig.3	11	-	-	ns
t_{HD}	data hold time		3	-	-	ns
CLK input (pin 17)		Fig.3				
f_{CLK}	frequency range		1	-	35	MHz
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance		-	-	10	pF
I_{leak}	input leakage current		-	-	10	µA
t_{CLK}	cycle time		28.5	-	-	ns
t_{pH}	duty factor	t_{CLKH} / t_{CLK}	40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
Digital-to-analog converters (pins 5, 6 and 40)						
V_{DDA4}	reference input voltage for internal resistor chains (pin 6)		4.75	5	5.25	V
I_{CUR}	input current (pin 5)	R_{6-5} = 15 kΩ	-	-	400	µA
Analog outputs V_{o1}; V_{o2} and V_{o3} (pins 43, 1 and 3)						
V_o	nominal output signal (peak-to-peak value)	without load	-	2	-	V
$V_{43, 1, 3}$	minimum output voltage	without load; V_{DDA4} = 5 V	0.16	-	0.24	V
	maximum output voltage	without load; V_{DDA4} = 5 V	2.1	-	2.3	V
DTDM	DAC to DAC matching	between all channels	-	-	|30|	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
B	output signal bandwidth	-3 dB	20	-	-	MHz
α_{CR}	crosstalk attenuation	note 2	48	-	-	dB
DNL	differential non-linearity	9-bit data; R_L = 125 Ω	-	-	±0.5	LSB
INL	integral non-linearity	9-bit data; R_L = 125 Ω	-	-	±0.2	%
$R_{43, 1, 3}$	internal serial output resistor		-	25	-	Ω
$R_{L\ 43, 1, 3}$	load resistance on output		125	-	-	Ω

Notes to the characteristics

1. With f_{CLK} = 35 MHz; f_{DATA} = 17.5 MHz (squarewave, full scale)
2. Crosstalk from channel to channel. One DAC with digital 5 MHz (sinusoidal, full scale) input signal, the other input data LOW. Measurements taken on outputs with 5.46 MHz filters (–3 dB at 5.87 MHz and –45 dB at 7.24 MHz).

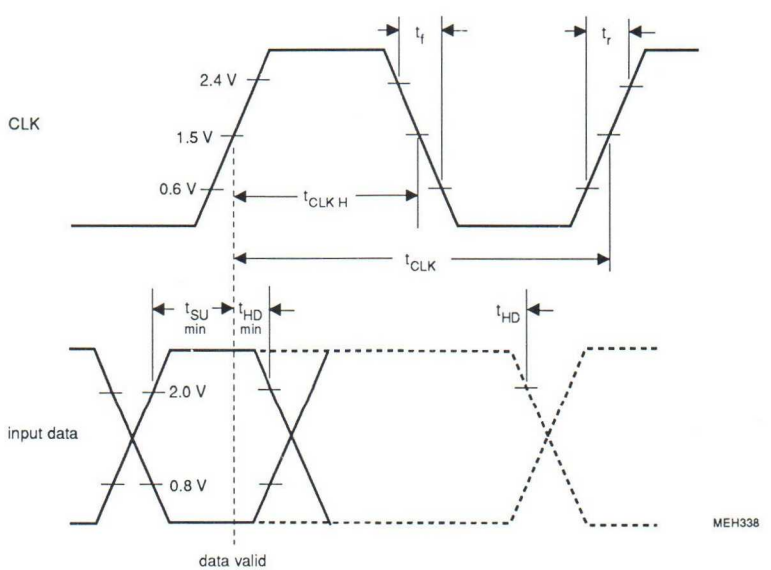


Fig.3 Input data timing.

Digital video scaler

SAA7186



CONTENTS

1. FEATURES
2. GENERAL DESCRIPTION
3. QUICK REFERENCE DATA
4. ORDERING INFORMATION
5. BLOCK DIAGRAM
6. PINNING
7. FUNCTIONAL DESCRIPTION
8. OPERATION CYCLE
9. I²C-BUS FORMAT
10. LIMITING VALUES
11. DC CHARACTERISTICS
12. AC CHARACTERISTICS
13. PROCESSING DELAYS
14. PROGRAMMING EXAMPLE
15. PACKAGE OUTLINE
16. UPDATE HISTORY
17. SOLDERING
18. DEFINITIONS

Digital video scaler SAA7186

1. FEATURES

- Scaling of video picture windows down to randomly sized windows
- Processes maximum 1023 pixels per line and 1023 lines per field
- Two-dimensional data processing for improved signal quality of scaled video data and for compression of video data
- 16-bit YUV input data buffer
- Interlace/non-interlace video data processing and field control
- Line memories in Y path and UV path to store two lines, each with 2 x 768 x 8 bit capacity
- Vertical sync processing by scale control
- Non-scaled mode to get full picture or to gate videotext lines
- UV input and output data binary/two's complement
- Switchable RGB matrix and anti-gamma ROMs
- 16-word FIFO register for 32-bit output data
- Output formats: 5-bit and 8-bit RGB, 8-bit YUV or 8-bit monochrome

2. GENERAL DESCRIPTION

The CMOS circuit SAA7186 scales and filters digital video data to randomly sized picture windows. YUV input data in 4:2:2 format are required (SAA7191B source).

3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5	5.5	V
$I_{DD\ tot}$	total supply current (inputs LOW, without output load)	-	-	180	mA
V_I	data input level	TTL-compatible			
V_O	data output level	TTL-compatible			
LLC	input clock frequency	-	-	32	MHz
T_{amb}	operating ambient temperature range	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7186	100	QFP	plastic	SOT317

5. BLOCK DIAGRAM

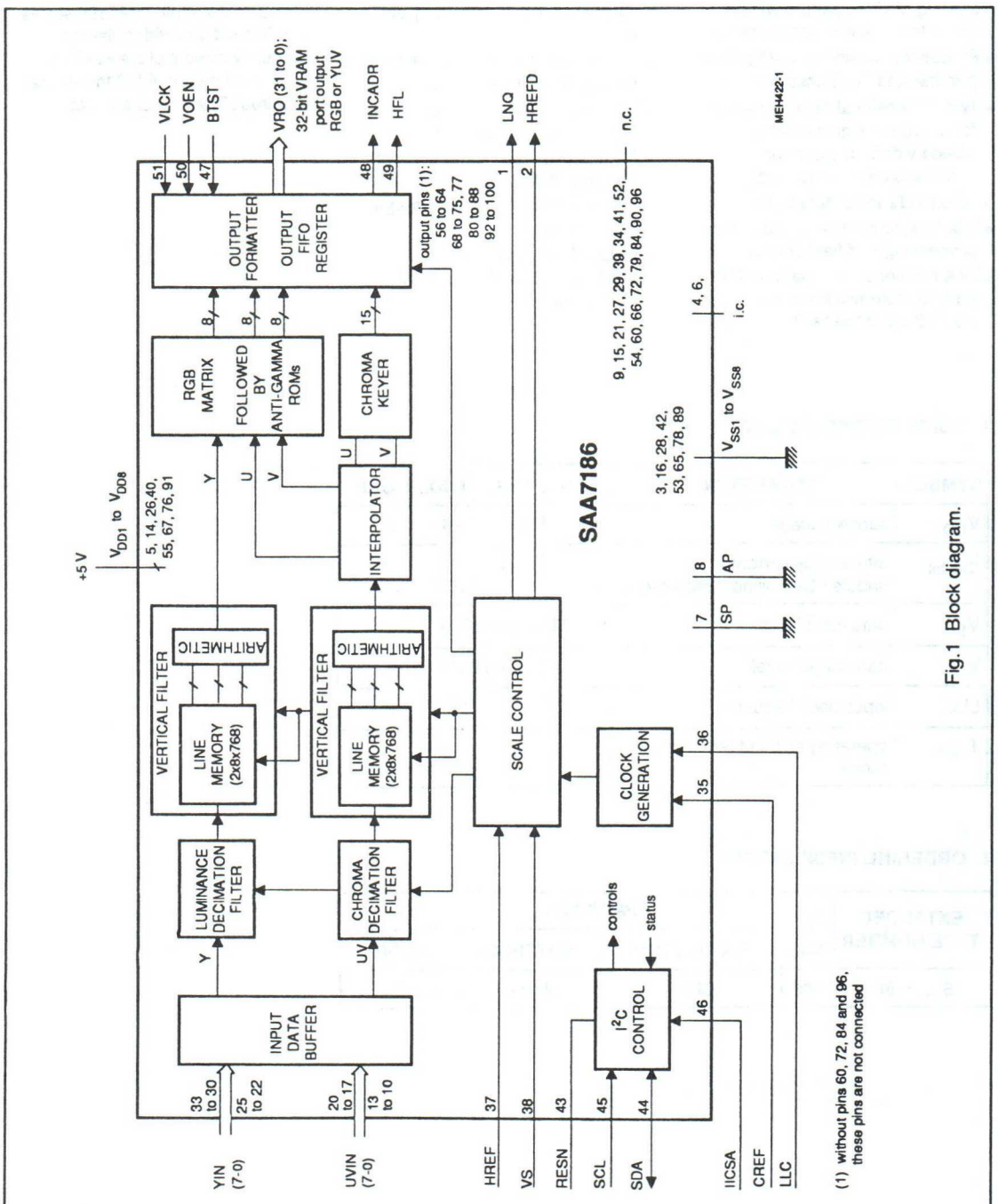


Fig.1 Block diagram.

6. PINNING

SYMBOL	PIN	STATUS	DESCRIPTION
LNQ	1	O	line qualifier signal; active polarity defined by QPL-bit in "10" (VCLK strobed)
HREFD	2	O	delay-compensated HREF output signal (VCLK strobed)
V_{SS1}	3	-	GND1 (0 V)
i.c.	4	-	internally connected
V_{DD1}	5	-	+5 V supply voltage 1
i.c.	6	-	internally connected
SP	7	I	connected to ground (shift pin for testing)
AP	8	I	connected to ground (action pin for testing)
n.c.	9	-	not connected
UVIN0	10	I	time-multiplexed colour-difference input data (bits 0 to 3)
UVIN1	11	I	
UVIN2	12	I	
UVIN3	13	I	
V_{DD2}	14	-	+5 V supply voltage 2
n.c.	15	-	not connected
V_{SS2}	16	-	GND2 (0 V)
UVIN4	17	I	time- multiplexed colour-difference input data (bits 4 to 7)
UVIN5	18	I	
UVIN6	19	I	
UVIN7	20	I	
n.c.	21	-	not connected
YIN0	22	I	luminance input data (bits 0 to 3)
YIN1	23	I	
YIN2	24	I	
YIN3	25	I	
V_{DD3}	26	-	+5 V supply voltage 3
n.c.	27	-	not connected
V_{SS3}	28	-	GND3 (0 V)
n.c.	29	-	not connected
YIN4	30	I	luminance input data (bits 4 to 7)
YIN5	31	I	
YIN6	32	I	
YIN7	33	I	
n.c.	34	-	not connected

SYMBOL	PIN	STATUS	DESCRIPTION
CREF	35	I	clock reference, external sync signal
LLC	36	I	line-locked system clock input signal (twice of pixel rate)
HREF	37	I	horizontal reference, pixel data clock signal (also present during vertical blanking)
VS	38	I	vertical sync input signal (approximately 6 lines long)
n.c.	39	-	not connected
V_{DD4}	40	-	+5 V supply voltage 4
n.c.	41	-	not connected
V_{SS4}	42	-	GND4 (0 V)
RESN	43	I	reset input (active-LOW for at least 30LLC periods)
SDA	44	I/O	IIC-bus data line
SCL	45	I	IIC-bus clock line
IICSA	46	I	set module address input of IIC-bus (LOW = B8, HIGH = BC)
BTST	47	I	output disable input; HIGH sets all data outputs to high-impedance state
INCADR	48	O	line increment / vertical reset control output line
HFL	49	O	FIFO register half-full flag output
VOEN	50	I	VRAM port output enable input (active-LOW)
VCLK	51	I	FIFO register clock input signal
n.c.	52	-	not connected
V_{SS5}	53	-	GND5 (0 V)
n.c.	54	-	not connected
V_{DD5}	55	-	+5 V supply voltage 5
VRO31	56	O	video output; 32-bit VRAM output port (bits 31 to 28)
VRO30	57	O	
VRO29	58	O	
VRO28	59	O	
n.c.	60	-	not connected
VRO27	61	O	video output; 32-bit VRAM output port (bits 27 to 24)
VRO26	62	O	
VRO25	63	O	
VRO24	64	O	
V_{SS6}	65	-	GND6 (0 V)
n.c.	66	-	not connected
V_{DD6}	67	-	+5 V supply voltage 6
VRO23	68	O	video output; 32-bit VRAM output port (bits 23 to 22)
VRO22	69	O	

SYMBOL	PIN	STATUS	DESCRIPTION
VRO21	70	O	video output; 32-bit VRAM output port (bits 21 to 20)
VRO20	71	O	
n.c.	72	-	not connected
VRO19	73	O	video output; 32-bit VRAM output port (bits 19 to 17)
VRO18	74	O	
VRO17	75	O	
V_{DD7}	76	-	+5 V supply voltage 7
VRO16	77	O	video output; 32-bit VRAM output port (bit16)
V_{SS7}	78	-	GND7 (0 V)
n.c.	79	-	not connected
VRO15	80	O	video output; 32-bit VRAM output port (bits 15 to 12)
VRO14	81	O	
VRO13	82	O	
VRO12	83	O	
n.c.	84	-	not connected
VRO11	85	O	video output; 32-bit VRAM output port (bits 11 to 8)
VRO10	86	O	
VRO9	87	O	
VRO8	88	O	
V_{SS8}	89	O	GND8 (0 V)
n.c.	90	-	not connected
V_{DD8}	91	-	+5 V supply voltage 8
VRO7	92	O	video output; 32-bit VRAM output port (bits 7 to 4)
VRO6	93	O	
VRO5	94	O	
VRO4	95	O	
n.c.	96	-	not connected
VRO3	97	O	video output; 32-bit VRAM output port (bits 3 to 0)
VRO2	98	O	
VRO1	99	O	
VRO0	100	O	

PIN CONFIGURATION

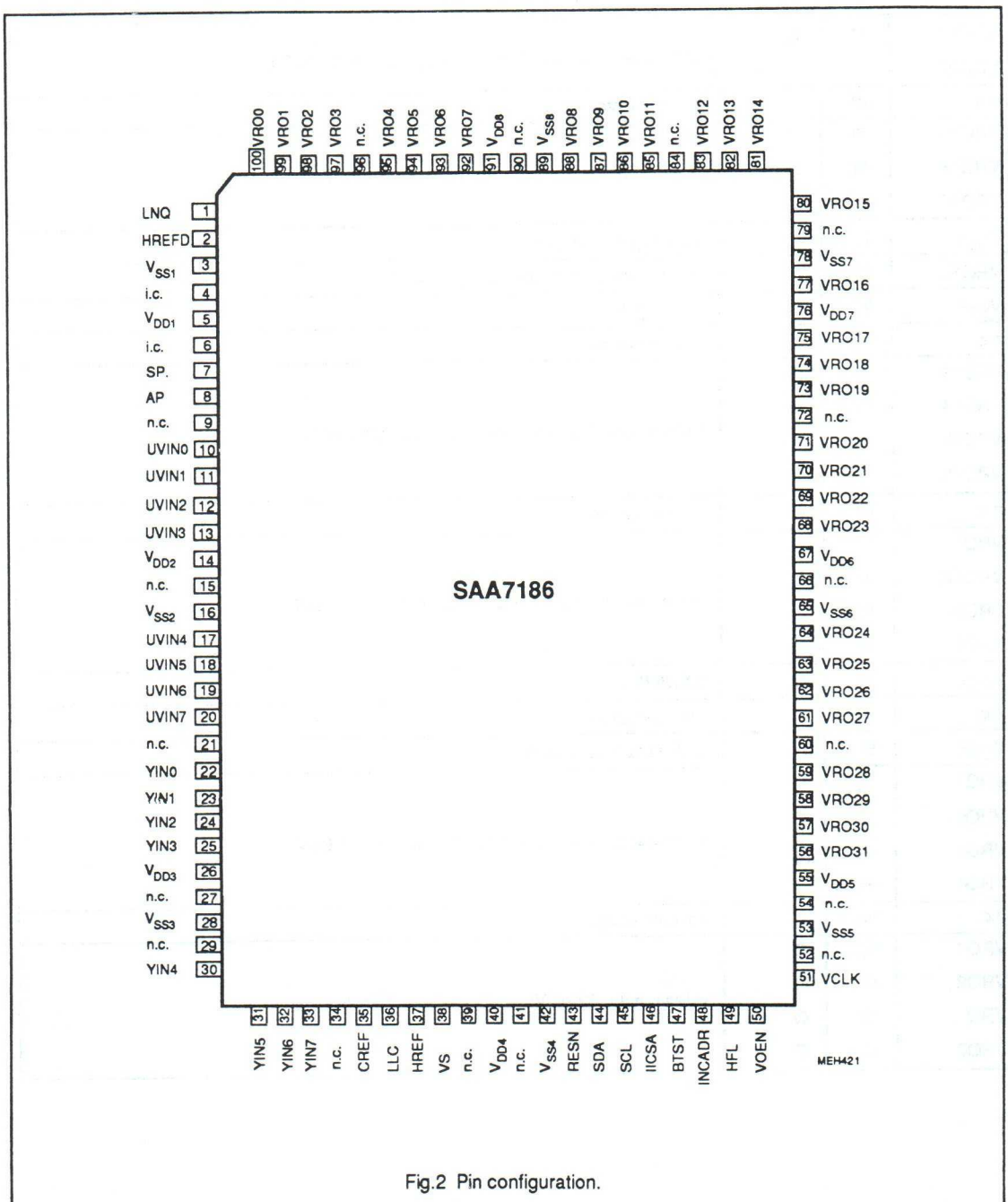


Fig.2 Pin configuration.

7. FUNCTIONAL DESCRIPTION

The input port is output of Philips digital video multistandard decoders (SAA7151B, SAA7191B) or other similar sources.
The SAA7186 input supports the 16-bit YUV 4:2:2 format.
The video data from the input port are converted into a unique internal two's complement data stream and are processed in horizontal direction in two separate decimation filters. Then they are processed in vertical direction by the vertical processing unit (VPU).
Chrominance data are interpolated to a 4:4:4 format; a chroma keying bit is generated.
The 4:4:4 YUV data are then converted from the YUV to the RGB domain in a digital matrix. ROM tables in the RGB data path can be used for anti-gamma correction of gamma-corrected input signals. Uncorrected RGB and YUV signals can be bypassed.
A scale control unit generates reference and gate signals for scaling of the processed video data. After data formatting to the various VRAM port formats, the scaled video data are buffered in the 16 word x 32-bit output FIFO register. The FIFO output is directly connected to the VRAM output bus VRO(31-0). Specific reference signals support an easy memory interfacing.
All functions of the SAA7186 are controlled via I²C-bus using 17 subaddresses. The external microcontroller can get information by reading the status register.

Video input port

The 16-bit YUV input data in 4:2:2 format (Table 1) consist of 8-bit luminance data Y (pins YIN(7-0)) and 8-bit time-multiplexed colour-difference data UV (pins UVIN(7-0)).
The input data are clocked in by the signals LLC and CREF (Fig.3). HREF and VS inputs define the video scan pattern (window).

Sequential input data

- are limited to maximum 768 active pixels per line if the vertical filter is active
- UV can be processed in straight binary and two's complement representation (controlled by TCC)

Decimation filters

The decimation filters perform accurate horizontal filtering of the input data stream.
Signal characteristics are matched in front of the pixel decimation stage, thus disturbing artifacts, caused by the pixel dropping, are reduced.
The signal bandwidth can be reduced in steps of:
2-tap filter = –6 dB at 0.325 pixel rate
3-tap filter = –6 dB at 0.25 pixel rate
4-tap filter = –6 dB at 0.21 pixel rate
5-tap filter = –6 dB at 0.125 pixel rate
9-tap filter = –6 dB at 0.075 pixel rate

The different characteristics are choosen dependent on the defined scaling parameters in an adaptive filter mode (AFS-bit = 1).
The filter characteristics can also be selected independently by control bits HF2 to HF0 at AFS-bit = 0.

Vertical filters

Y and UV data are handled in separate filters (Fig.1). Each of the two line memories has a capacity of 2 x 768 x 8-bit. Thus two complete video lines of 4:2:2 YUV data can be stored. The VPU is split into two memory banks and one arithmetic unit. The available processing modes, respectively transfer functions, are selectable by the bits VP1 and VP0 if AFS = 0.
An adaptive mode is selected by AFS = 1. Disturbing artifacts, generated by line dropping, are reduced.

Adaptive filter selection (AFS = 1):

scaling ratio	filter function (refer to I²C section)
XD/XS	horizontal
≤1	bypassed
≤14/15	filter 1
≤11/15	filter 6
≤7/15	filter 3
≤3/15	filter 4
YD/YS	vertical
≤1	bypassed
≤13/15	filter 1
≤4/15	filter 2

RGB matrix

Y data and UV data are converted after interpolation into RGB data according to CCIR601 recommendation. Data are bypassed in YUV or monochrome modes.

Table 1 4 : 2 : 2 format (pixels per line). The time frames are controlled by the HREF signal.

INPUT	PIXEL BYTE SEQUENCE				
YIN7	Ye7	Yo7	Ye7	Yo7	Ye7
YIN6	Ye6	Yo6	Ye6	Yo6	Ye6
YIN5	Ye5	Yo5	Ye5	Yo5	Ye5
YIN4	Ye4	Yo4	Ye4	Yo4	Ye4
YIN3	Ye3	Yo3	Ye3	Yo3	Ye3
YIN2	Ye2	Yo2	Ye2	Yo2	Ye2
YIN1	Ye1	Yo1	Ye1	Yo1	Ye1
YIN0	Ye0	Yo0	Ye0	Yo0	Ye0
UVIN7	Ue7	Ve7	Ue7	Ve7	Ue7
UVIN6	Ue6	Ve6	Ue6	Ve6	Ue6
UVIN5	Ue5	Ve5	Ue5	Ve5	Ue5
UVIN4	Ue4	Ve4	Ue4	Ve4	Ue4
UVIN3	Ue3	Ve3	Ue3	Ve3	Ue3
UVIN2	Ue2	Ve2	Ue2	Ve2	Ue2
UVIN1	Ue1	Ve1	Ue1	Ve1	Ue1
UVIN0	Ue0	Ve0	Ue0	Ve0	Ue0
Y frame	0	1	2	3	4
UV frame	0		2		4

e = even pixel; o = odd pixel

The matrix equations are these considering the digital quantization:

R = Y + 1.375 V
G = Y − 0.703125 V − 0.34375 U
B = Y + 1.734375 U.

Anti-gamma ROM tables:
ROM tables are implemented at the matrix output to provide anti-gamma correction of the RGB data. A curve for a gamma of 1.4 is implemented

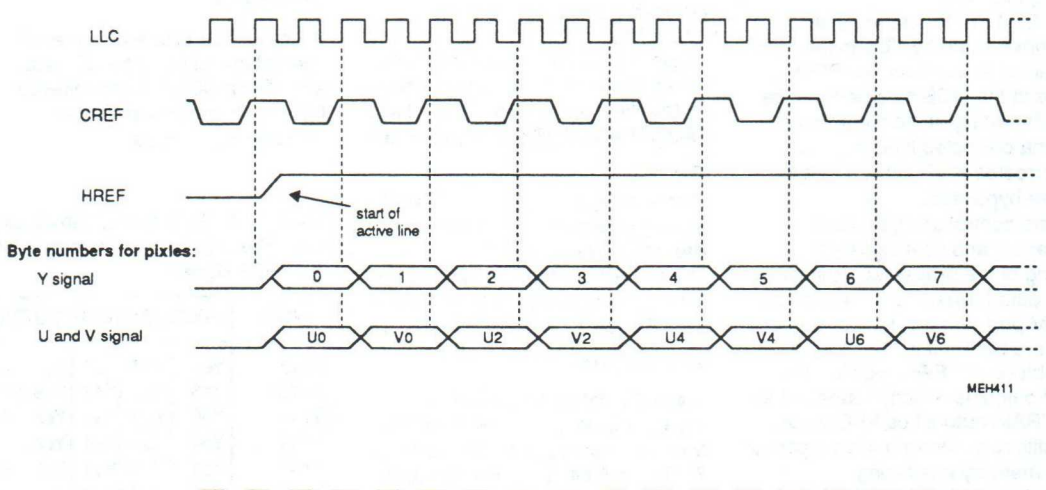
The tables can be used (RTB-bit = 0) to compensate gamma correction for linear data representation of RGB output data.

Chrominance signal keyer

The keyer generates an alpha signal to achieve a 5-5-5 +α RGB alpha output signal. Therefore, the processed UV data amplitudes are compared with thresholds set via I²C-bus (subaddresses "0C to 0F"). A logical "1" signal is generated if the amplitude is inside the specified amplitude range, otherwise a logical "0" is generated.
Keying can be switched off by setting the lower limit higher than the upper limit ("0C or 0E" and "0D or 0F").

Scale control and vertical regions

The scale control block SC includes vertical address/sequence counters to define the current position in the input field and to address the internal VPU memories.
To perform scaling, XD of XS pixel selection in horizontal direction and YD of YS line selection in vertical direction are applied. The pixel and line dropping are controlled at the input of the FIFO register.
To control the decimation filter function and the vertical data processing in the adaptive mode



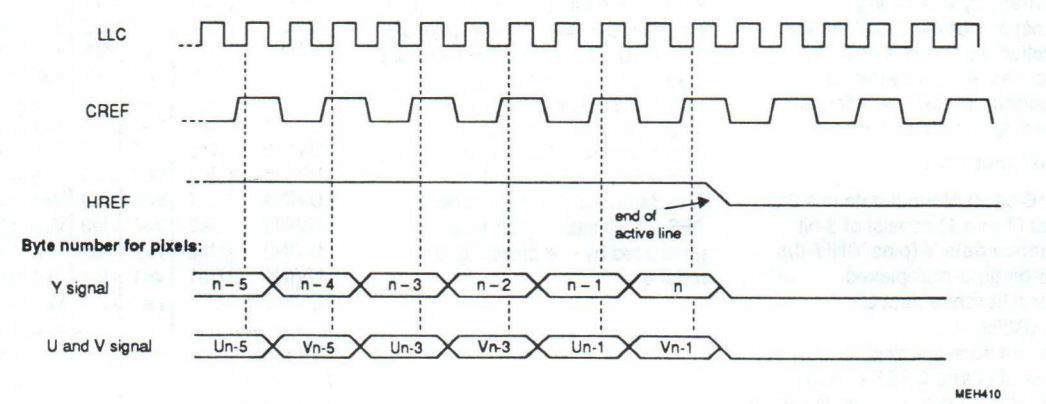


Fig.3 Horizontal and data multiplex timing.

(AFS = 1), the scaling ratio in horizontal and vertical direction is estimated in the SC block.

The input field can be divided into two vertical regions – the bypass region and the scaling region, which are defined via I²C-bus by the parameters VS, VC, YO and YS.

Vertical bypass region:

Data are not scaled and independent of I²C-bits FS1, FS0 the output format is always 8-bit grayscale (monochrome). The SAA7186 outputs all active pixels of a line, defined by the HREF input signal if the vertical bypass region is active. This can be used, for example, to store videotext information in the field memory.

The start line of the bypass region is defined by VS; the number of lines to be bypassed is defined by VC.

Vertical scaling region:

Data is scaled with start at line YO and the output format is selected when FS1, FS0 are valid.
This is the "normal operation" area.

The input/output screen dimensions in horizontal and vertical direction are defined by the parameters

XO, XS and XD for horizontal

YO, YS and YD for vertical.

The circuit processes XS samples of a line. Remaining pixels are ignored if a line is longer than XS. If a line is shorter than XS, processing is aborted when the falling edge of HREF is detected.

Vertical regions in Fig.4:

- the two regions can be programmed via I²C-bus, whereby regions should not overlap (active region overrides the bypass region).
- the start of a normal active picture depends on video standard and has to be programmed to the correct value.
- the offsets XO and YO have to be set according to the internal processing delays to ensure the complete number of destination pixels and lines (Table 6).
- the scaling parameters can be used to perform a panning function over the video frame/field.

Output data representation and levels

Output data representation of the YUV data can be modified by bit MCT (subaddress 10).
The DC gain is 1 for YUV input data. The corresponding RGB levels are defined by the matrix equations. The luminance levels are limited according to CCIR 601

16 (239) = black
235 (20) = white
(..) = grayscale luminance levels

if the YUV or monochrome luminance output formats are selected.

The signal levels of the RGB formats are limited in 8-bit to "0" or "255". For the 5-bit RGB formats a truncation from 8-bit to 5-bit is implemented.

Fill values are inserted dependent on longword position and destination size:

- "0" in RGB formats and for Y two'2 complement U, V
- "128" for U, V (straight binary)
- "255" in 8-bit grayscale format

The unused output values of the YUV and grayscale formats can be used for other purposes.

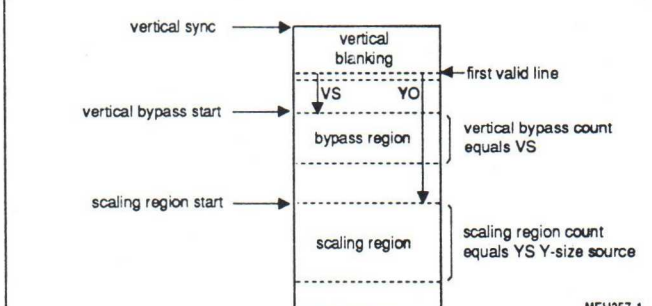


Fig.4 Vertical regions.

Table 2 VRAM port output data formats at EFE-bit = 0 dependend on FS1 and FS0 bits (set via I²C-bus)

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB 5-5-5 + 1 32-BIT WORDS			FS1 = 0; FS0 = 1 YUV 4:2:2 32-BIT WORDS			FS1 = 1; FS0 = 0 YUV 4:2:2 TEST 16-BIT WORDS			FS1 = 1; FS0 = 1 8-bit monochrome 32-BIT WORDS		
PIXEL ORDER	n	n+2	n+4	n	n+2	n+4	n	n+1	n+2	n n+1	n+4 n+5	n+8 n+9
VRO31	α	α	α	Ye7	Ye7	Ye7	Ye7	Yo7	Ye7	Ya7	Ya7	Ya7
VRO30	R4	R4	R4	Ye6	Ye6	Ye6	Ye6	Yo6	Ye6	Ya6	Ya6	Ya6
VRO29	R3	R3	R3	Ye5	Ye5	Ye5	Ye5	Yo5	Ye5	Ya5	Ya5	Ya5
VRO28	R2	R2	R2	Ye4	Ye4	Ye4	Ye4	Yo4	Ye4	Ya4	Ya4	Ya4
VRO27	R1	R1	R1	Ye3	Ye3	Ye3	Ye3	Yo3	Ye3	Ya3	Ya3	Ya3
VRO26	R0	R0	R0	Ye2	Ye2	Ye2	Ye2	Yo2	Ye2	Ya2	Ya2	Ya2
VRO25	G4	G4	G4	Ye1	Ye1	Ye1	Ye1	Yo1	Ye1	Ya1	Ya1	Ya1
VRO24	G3	G3	G3	Ye0	Ye0	Ye0	Ye0	Yo0	Ye0	Ya0	Ya0	Ya0
VRO23	G2	G2	G2	Ue7	Ue7	Ue7	Ue7	Ve7	Ue7	Yb7	Yb7	Yb7
VRO22	G1	G1	G1	Ue6	Ue6	Ue6	Ue6	Ve6	Ue6	Yb6	Yb6	Yb6
VRO21	G0	G0	G0	Ue5	Ue5	Ue5	Ue5	Ve5	Ue5	Yb5	Yb5	Yb5
VRO20	B4	B4	B4	Ue4	Ue4	Ue4	Ue4	Ve4	Ue4	Yb4	Yb4	Yb4
VRO19	B3	B3	B3	Ue3	Ue3	Ue3	Ue3	Ve3	Ue3	Yb3	Yb3	Yb3
VRO18	B2	B2	B2	Ue2	Ue2	Ue2	Ue2	Ve2	Ue2	Yb2	Yb2	Yb2
VRO17	B1	B1	B1	Ue1	Ue1	Ue1	Ue1	Ve1	Ue1	Yb1	Yb1	Yb1
VRO16	B0	B0	B0	Ue0	Ue0	Ue0	Ue0	Ve0	Ue0	Yb0	Yb0	Yb0
PIXEL ORDER	n+1	n+3	n+5	n+1	n+3	n+5	OUTPUTS NOT USED			n+2 n+3	n+6 n+7	n+10 n+11
VRO15	α	α	α	Yo7	Yo7	Yo7	X	X	X	Yc7	Yc7	Yc7
VRO14	R4	R4	R4	Yo6	Yo6	Yo6	X	X	X	Yc6	Yc6	Yc6
VRO13	R3	R3	R3	Yo5	Yo5	Yo5	X	X	X	Yc5	Yc5	Yc5
VRO12	R2	R2	R2	Yo4	Yo4	Yo4	X	X	X	Yc4	Yc4	Yc4
VRO11	R1	R1	R1	Yo3	Yo3	Yo3	X	X	X	Yc3	Yc3	Yc3
VRO10	R0	R0	R0	Yo2	Yo2	Yo2	X	X	X	Yc2	Yc2	Yc2
VRO9	G4	G4	G4	Yo1	Yo1	Yo1	X	X	X	Yc1	Yc1	Yc1
VRO8	G3	G3	G3	Yo0	Yo0	Yo0	X	X	X	Yc0	Yc0	Yc0
VRO7	G2	G2	G2	Ve7	Ve7	Ve7	X	X	X	Yd7	Yd7	Yd7
VRO6	G1	G1	G1	Ve6	Ve6	Ve6	X	X	X	Yd6	Yd6	Yd6
VRO5	G0	G0	G0	Ve5	Ve5	Ve5	X	X	X	Yd5	Yd5	Yd5
VRO4	B4	B4	B4	Ve4	Ve4	Ve4	X	X	X	Yd4	Yd4	Yd4
VRO3	B3	B3	B3	Ve3	Ve3	Ve3	X	X	X	Yd3	Yd3	Yd3
VRO2	B2	B2	B2	Ve2	Ve2	Ve2	X	X	X	Yd2	Yd2	Yd2
VRO1	B1	B1	B1	Ve1	Ve1	Ve1	X	X	X	Yd1	Yd1	Yd1
VRO0	B0	B0	B0	Ve0	Ve0	Ve0	X	X	X	Yd0	Yd0	Yd0

α = keying bit; R, G, B, Y. U and V = digital signals; e = even pixel number; o = odd pixel number; a b c d = consecutive pixels

Table 3 VRAM port output data formats at EFE-bit = 1 dependend on FS1 and FS0 bits (set via I²C-bus)

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB 5-5-5 + 1 16-BIT WORDS			FS1 = 0; FS0 = 1 YUV 4:2:2 16-BIT WORDS			FS1 = 1; FS0 = 0 RGB 8-8-8 24-BIT WORDS			FS1 = 1; FS0 = 1 8-bit monochrome 16-BIT WORDS		
PIXEL ORDER	n	n+1	n+2	n	n+1	n+2	n	n+1	n+2	n n+1	n+2 n+3	n+4 n+5
VRO31	α	α	α	Ye7	Yo7	Ye7	R7	R7	R7	Ya7	Ya7	Ya7
VRO30	R4	R4	R4	Ye6	Yo6	Ye6	R6	R6	R6	Ya6	Ya6	Ya6
VRO29	R3	R3	R3	Ye5	Yo5	Ye5	R5	R5	R5	Ya5	Ya5	Ya5
VRO28	R2	R2	R2	Ye4	Yo4	Ye4	R4	R4	R4	Ya4	Ya4	Ya4
VRO27	R1	R1	R1	Ye3	Yo3	Ye3	R3	R3	R3	Ya3	Ya3	Ya3
VRO26	R0	R0	R0	Ye2	Yo2	Ye2	R2	R2	R2	Ya2	Ya2	Ya2
VRO25	G4	G4	G4	Ye1	Yo1	Ye1	R1	R1	R1	Ya1	Ya1	Ya1
VRO24	G3	G3	G3	Ye0	Yo0	Ye0	R0	R0	R0	Ya0	Ya0	Ya0
VRO23	G2	G2	G2	Ue7	Ve7	Ue7	G7	G7	G7	Yb7	Yb7	Yb7
VRO22	G1	G1	G1	Ue6	Ve6	Ue6	G6	G6	G6	Yb6	Yb6	Yb6
VRO21	G0	G0	G0	Ue5	Ve5	Ue5	G5	G5	G5	Yb5	Yb5	Yb5
VRO20	B4	B4	B4	Ue4	Ve4	Ue4	G4	G4	G4	Yb4	Yb4	Yb4
VRO19	B3	B3	B3	Ue3	Ve3	Ue3	G3	G3	G3	Yb3	Yb3	Yb3
VRO18	B2	B2	B2	Ue2	Ve2	Ue2	G2	G2	G2	Yb2	Yb2	Yb2
VRO17	B1	B1	B1	Ue1	Ve1	Ue1	G1	G1	G1	Yb1	Yb1	Yb1
VRO16	B0	B0	B0	Ue0	Ve0	Ue0	G0	G0	G0	Yb0	Yb0	Yb0
PIXEL ORDER	n	n+1	n+2	n	n+1	n+2	n	n+1	n+2	n n+1	n+2 n+3	n+4 n+5
VRO15	X	X	X	X	X	X	B7	B7	B7	X	X	X
VRO14	X	X	X	X	X	X	B6	B6	B6	X	X	X
VRO13	X	X	X	X	X	X	B5	B5	B5	X	X	X
VRO12	X	X	X	X	X	X	B4	B4	B4	X	X	X
VRO11	X	X	X	X	X	X	B3	B3	B3	X	X	X
VRO10	X	X	X	X	X	X	B2	B2	B2	X	X	X
VRO9	X	X	X	X	X	X	B1	B1	B1	X	X	X
VRO8	X	X	X	X	X	X	B0	B0	B0	X	X	X
VRO7(1)(2)	α	α	α	α	X	α	α	α	α	α	α	α
VRO6 (2)	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E
VRO5 (2)	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT
VRO4 (2)	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT
VRO3	X	X	X	X	X	X	X	X	X	X	X	X
VRO2 (2)	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF
VRO1 (2)	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ
VRO0 (2)	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ

α = keying bit; R, G, B, Y. U and V = digital signals; e = even pixel number; o = odd pixel number; a b c d = consecutive pixels; O/E = odd/even flag

(1) YUV 16-bit format: the keying signal α is defined only for YU time steps. The corresponding YV sample has also to be keyed. The α signal in monochrome mode can be used only in the transparent mode (TTR = 1), in this case Ya = Yb.

(2) Data valid only when transparent mode active (TTR-bit = 1) and VCLK pin connected to LLC/2 clock rate.

Output FIFO register and VRAM output port

The output FIFO register is the buffer between the video data stream and the VRAM data input port. Resized video data are buffered and formatted. 32-, 24- and 16-bit video data modes are supported. The various formats are selected by the bits EFE, FS1 and FS0. VRAM port formats are shown in Tables 2 and 3. The FIFO register capacity is 16 word x 32 bit (for 32-, 24-, or 16-bit video data). The bits LW1 and LW0 can be used to define the position of the first pixel each line in the 32-bit longword formats or to shift the UV sequence to VU in the 16-bit YUV formats (LW1 = 1).

VRAM port inputs are:
VCLK to clock the FIFO register output data and VOEN to enable output data.

VRAM port outputs are:
the HFL flag (half-full flag), the signal INCADR (refer to section "data burst transfer") and the reference signals for pixel and line selection on outputs VRO(7-0) (only for 24- and 16-bit video data formats refer to "transparent data transfer").

VRAM port transfer procedures

Data transfer on the VRAM port can be done asynchroneously controlled by outputs HFL, INCADR and input VCLK (data burst transfer with bit TTR = 0).

Data transfer on the VRAM port can be done synchroneously controlled by output reference signals on outputs VRO(7-0) and a clock rate of LLC/2 on input VCLK (transparent data transfer with bit TTR = 1 and EFE = 1).
The scaling capability of the SAA7186 can be used in various applications.

Data burst transfer mode

Data transfer on the VRAM port is asynchroneously (TTR = 0). This mode can be used for all output formats. Four signals for communication with the external memory are provided.

- HFL flag, the half-full flag of the FIFO output register is raised when the FIFO contains at least 8 data words (HFL = HIGH).
  By setting HFL = 1, the SAA7186 requests a data burst transfer by the external memory controller, that has to start a transfer cycle within the next 32 LLC cycles for 32-bit longword modes (16 LLC cycles for 16- and 24-bit modes). If there are pixels in the FIFO at the end of a line, which are not transferred, the circuit fills up the FIFO register with "fill pixels" until it is half-full and sets the HFL flag to request a data burst transfer. After transfer is done, HFL is used in combination with INCADR to indicate the line increments (Figures 6 and 7).
- INCADR output signal is used in combination with HFL to control horizontal and vertical address generation for a memory controller. The pulse sequence depends on field formats (interlace/ non-interlace or odd/even fields, Figures 6 and 7) and control bits OF (subaddress 00).

  HFL = 1 at the rising edge of INCADR:
  the end of line is reached, request for line address increment
  HFL = 0 at the rising edge of INCADR:
  the end of field/frame is reached, request for line and pixel addresses reset
  (The distance from the last half-full request HFL to the INCADR pulse may be longer than 64 x LLC. The HFL state is defined for minimum 4 x LLC in front of the rising edge of INCADR and minimum 2 x LLC afterwards.)
- VCLK input signal to clock the FIFO register output data VRO(n). New data are placed on the VRO(n) port with the rising edge of VCLK (Fig.5).
- VOEN input enables output data VRO(n).The outputs are in 3-state mode at VOEN = HIGH.
  VOEN changes only when VCLK is LOW. If VCLK pulses are applied during VOEN = HIGH, the outputs remain inactive, but the FIFO register accepts the pulses.

Transparent data transfer mode

Data transfer on the VRAM port can be achieved synchroneously (TTR =1). With a contineous clock rate of LLC/2 on input VCLK, the SAA7186 delivers a contineously processed data stream. Therefore, the extended formats of the VRAM output port have to be selected (bit EFE = 1; Table 3). The reference and gate signals on outputs VRO(6-1) and the LNQ signal are delivered in each field (means scaled and ignored fields). The PXO signal (also VRO0) is only delivered in active fields.
The output signals VRO(7-0) can be used to buffer qualified pre-processed RGB or YUV video data (notice: the YUV data are only valid in qualified time slots). Control output signals in Table 3 are:

α	keying signal of the chroma keyer
O/E	odd/even field bit according to the internal field processing
VGT	vertical gate signal, "1" marks the scaling window in vertical direction from YO to (YO + YS) lines, cut by VS.
HGT	horizontal gate signal, "1" marks horizontal direction from XO to (XO + XS) lines, cut by HREF.
HRF	delay compensated horizontal reference signal.
LNQ	line qualifier signal, active polarity is defined by QPL bit.
PXQ	pixel qualifier signal, active polarity is defined by QPP bit.

Power-on reset

- the FIFO register contents are undefined
- outputs VRO are set to high-impedance state
- output INCADR = HIGH
- output HFL = LOW until the VPE bit is set to "1"
- subaddress "10" is set to 00h and VPE-bit in subaddress "00" is set to zero (Table 4).

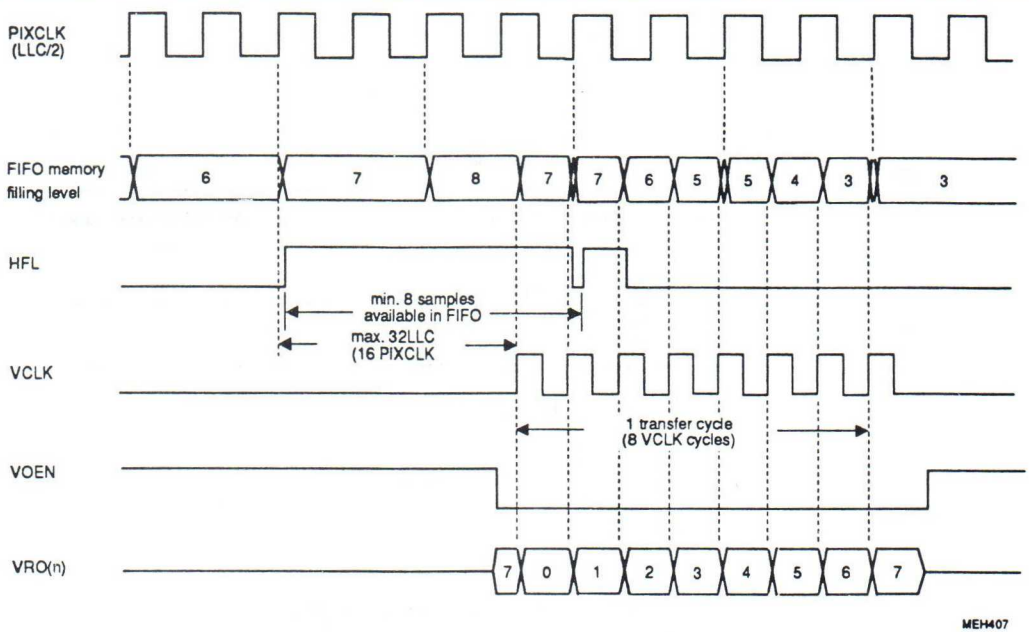


Fig.5 Output port transfer to VRAM at 32-bit data format without scaling. If VCLK cycles occur at VOEN = HIGH, the FIFO register is unchanged, but the outputs VRO(31-0) remain in 3-state position.

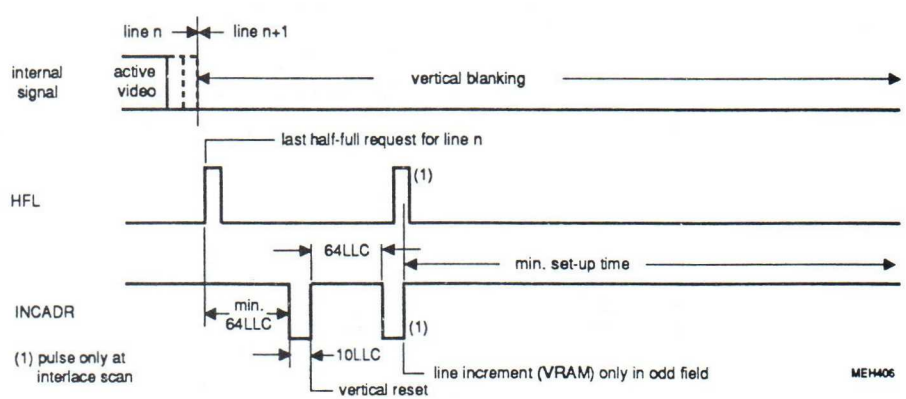


Fig.6 Vertical reset timing to the VRAM.

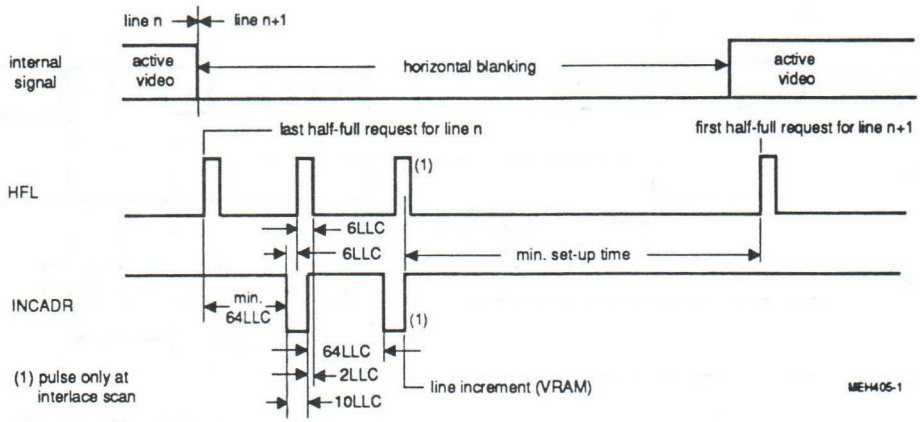


Fig.7 Horizontal increment timing to the VRAM.

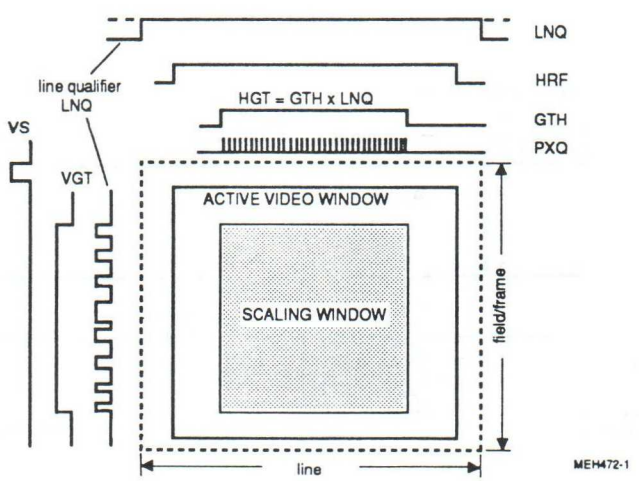


Fig.8 Reference signals for scaling window.

Field processing

The phase of the field sequence (odd/even dependent on inputs HREF and VS) is detected by means of the falling edge of VS. The current field phase is reported in the status byte by the OEF bit (Table 5). OEF bit can be stable 0 or 1 for non-interlaced input frames or non standard input signals VS and/or HREF (nominal condition for VS and HREF – SAA7191 B with active vertical noise limiter). A free-running odd/even flag is generated for internal field processing if the detection reports a stable OEF bit.

The POE bit (subaddress 0B) can be used to change the polarity of the internal flag (in case of non-standard VS and HREF signals) to control the phase of the free-running flag, and to compensate mis-detections. Thus, the SAA7186 can be used under various VS/HREF timing conditions.

The SAA7186 operates on fields. To support progressive displays and to avoid movement blurring and artifacts, the circuit can process both or single fields of interlaced or non-interlaced input data. Therefore the OF bits can be used. The bits OF1 and OF0 (Table 6) determine the INCADR/HFL generation in "data burst transfer mode". One of the fields (odd or even) is ignored when OF1 = 1; then no line increment sequence (INCADR/HFL) is generated, the vertical reset pulse is only generated.

With OF1 = OF0 = 0 the circuit supports correct interlaced data storage. Two INCADR/HFL sequences are generated in each qualified line; additionally an INCADR/HFL sequence after the vertical reset sequence of an odd field is generated. Thereby, the scaled lines are automatically stored in the right sequence.

8. OPERATION CYCLE

The operation is synchronized by the input field. The cycle is specified in the flow chart (Fig.9).
The circuit is inactive after power-on reset, VPO is 0 and the FIFO control is set "empty". The internal control registers are updated with the falling edge of VS signal. The circuit is switched active and waits for a transmission of VS and a vertical reset sequence to the memory controller. Afterwards, the circuit waits for the beginning of a scaling or bypass region. The processing of a current line is finished when a vertical sync pulse appears. The circuit performs a coefficient update and generates a new vertical reset (if it is still active).

Line processing starts when a line is decided to be active, the circuit starts to scale it. Active pixels are loaded into the FIFO register. An HFL flag is generated to initialize a data transfer when eight words are completed. The line end is reached when the programmed pixel number is processed or when a horizontal sync pulse occurs. If there are pixels in the FIFO register, it is filled up until it is half-full to cause a data transfer. Horizontal increment pulses are transmitted after this data transfer.

Remarks:
The SAA7186 will always wait for the HREF/VS pulse before the line increment/vertical reset sequence is performed.
After each line/field, the FIFO control is set to empty when INCADR/HFL sequence is transmitted.
No additional actions are necessary if the memory controller has ignored the HFL signal. There is no need to handle overflow/underflow of the FIFO register.

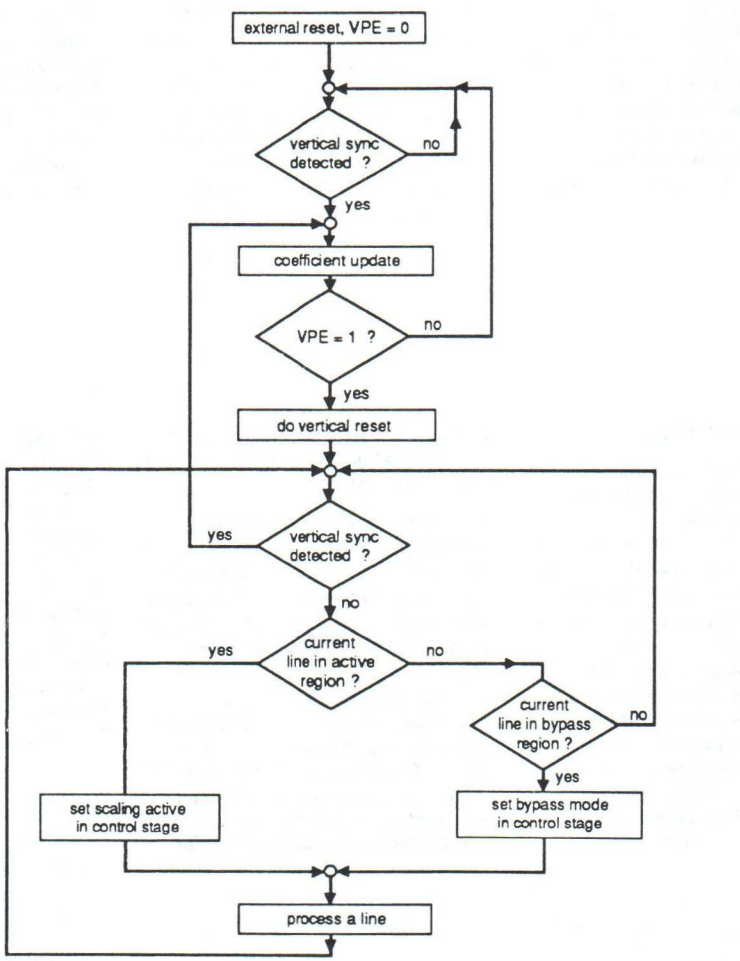


Fig.9 Operation cycle

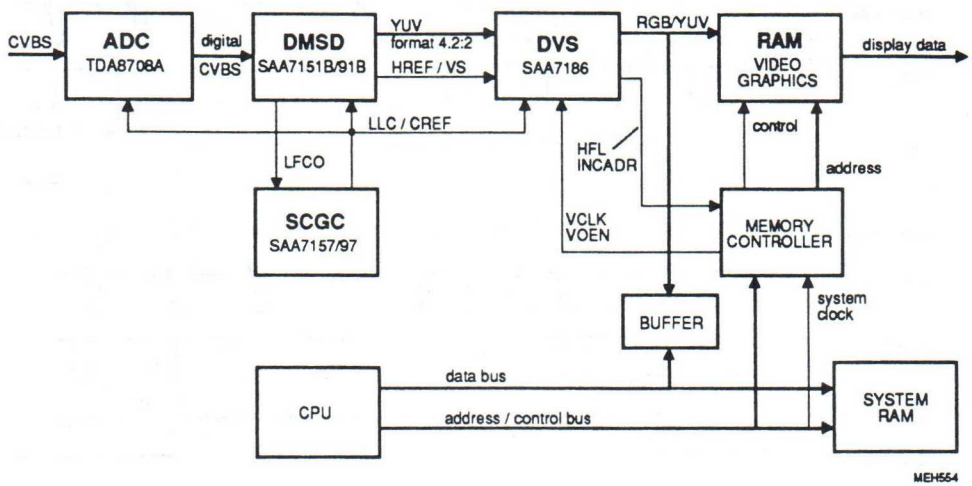


Fig.10 SAA7186 system configuration in Data Burst Transfer Mode (TTR = , VCLK = continuous).

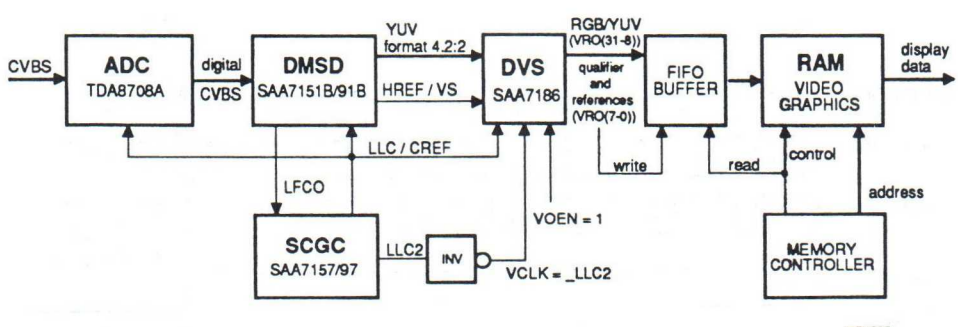


Fig.11 SAA7186 system configuration in Transparent Data Transfer Mode (TTR = 1, EFE = 1, VCLK = continuous (_LLC2)).

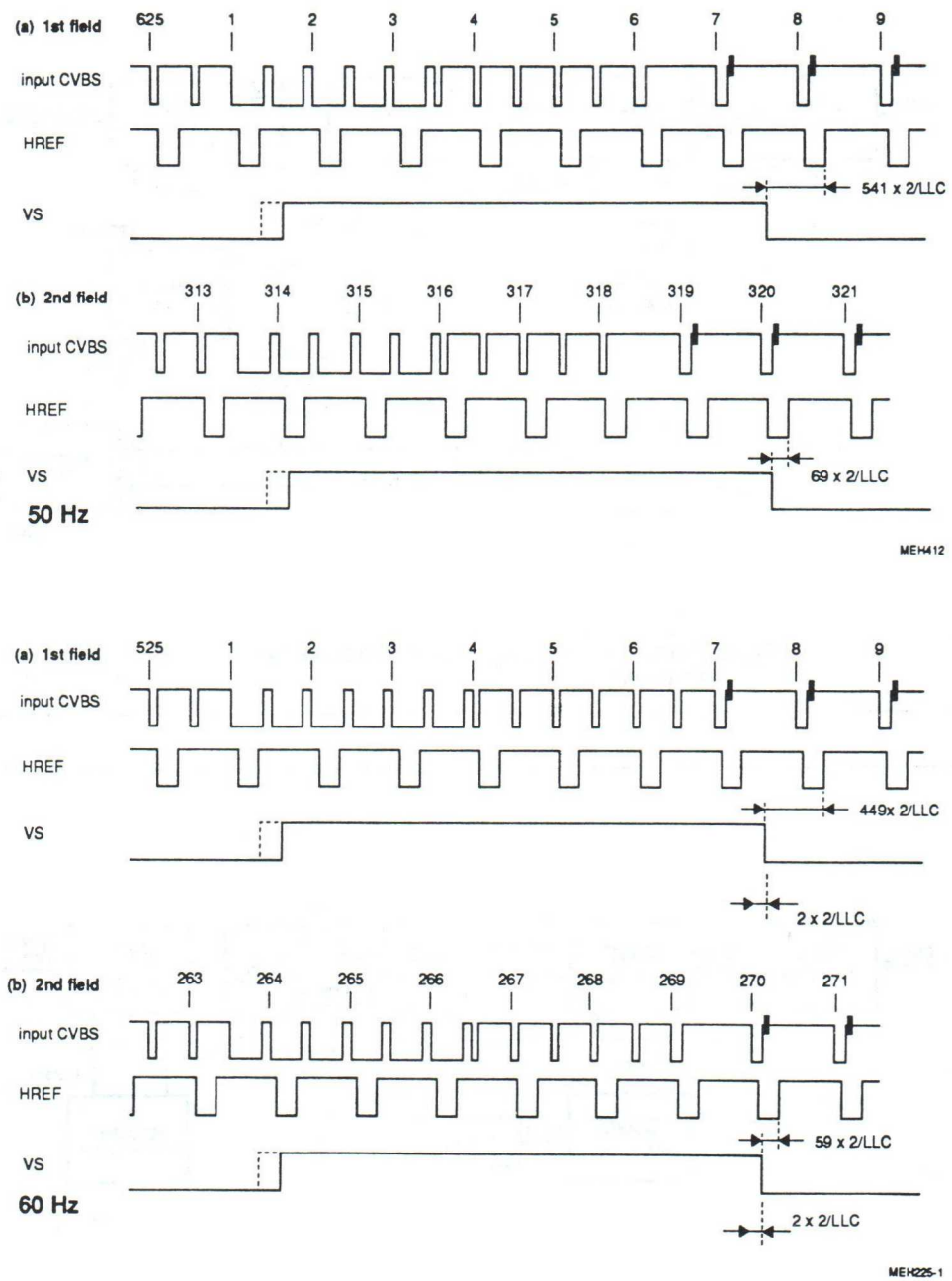


Fig.12 VS timing for video input source SAA7191B.

9. I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = **1011 100X** (IICSA = LOW) **or 1011 110X** (IICSA = HIGH)
A = acknowledge, generated by the slave
SUBADDRESS* = subaddress byte (Table 4)
DATA = data byte (Table 4)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 4 I²C-bus; subaddress and data bytes for writing (X in address byte = 0).

FUNCTION	SUBADDRESS	DATA D7	D6	D5	D4	D3	D2	D1	D0	DF*
Formats and sequence	00	RTB	OF1	OF0	VPE	LW1	LW0	FS1	FS0	tbf
Output data pixel/line	01	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0	
continued in	04							XD9	XD8	
Input data pixel/line	02	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
continued in	04					XS9	XS8			
Horizontal window start	03	XO7	XO6	XO5	XO4	XO3	XO2	XO1	XO0	
Pixel decimation filter	04	HF2	HF1	HF0	XO8	XS9	XS8	XD9	XD8	
Output data lines/field	05	YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0	
continued in	09							YD9	YD8	
Input data lines/field	06	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
continued in	09					YS9	YS8			
Vertical window start	07	YO7	YO6	YO5	YO4	YO3	YO2	YO1	YO0	
AFS/vertical processing	08	AFS	VP1	VP0	YO8	YS9	YS8	YD9	YD8	
Vertical bypass start	09	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0	
continued in	0B				VS8					
Vertical bypass count	0A	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	
continued in	0B	TCC	0	0	VS8	0	VC8	0	POE	
Chroma keying										
lower limit for V	0C	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	
upper limit for V	0D	VU7	VU6	VU5	VU4	VU3	VU2	VU1	VU0	
lower limit for U	0E	UL7	UL6	UL5	UL4	UL3	UL2	UL1	UL0	
upper limit for U	0F	UU7	UU6	UU5	UU4	UU3	UU2	UU1	UU0	
Byte 10**	10	0	0	0	MCT	QPL	QPP	TTR	EFE	
Unused	11 to 1F									

*) Default register contents fill in by hand
**) Byte 10 is set to 00h after power-on reset.

Table 5 I²C-bus status byte (X in address byte = 1)

FUNCTION		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
status byte		ID3	ID2	ID1	ID0	0	0	OEF	SVP

Function of status bits:

ID3 to ID0 — Software version of SAA7186 compatible with

ID3	ID2	ID1	ID0	version
0	0	0	1	1

OEF — Identification of field sequence dependent on inputs HREF and VS:
0 = even field detected; 1 = odd field detected

SVP — State of VRAM port:
0 = inputs HFL and INCADR inactive;
1 = inputs HFL and INCADR active.

Table 6 Function of the register bits of Table 4

"00" RTB — ROM table bypass switch:
0 = anti-gamma ROM active
1 = table is bypassed

OF1 to OF0 — Set output field mode:

OF1	OF0	field mode DVS process
0	0	both fields for interlaced storage
0	1	both fields for non-interlaced storage
1	0	odd fields only (even fields ignored) for non-interlaced storage
1	1	even fields only(odd fields ignored) for non-interlaced storage

VPE — VRAM port outputs enable:
0 = HFL and INCADR inactive; VRO outputs in 3-state position (HFL = LOW, INCADR = HIGH)
1 = HFL and INCADR enabled; VRO outputs dependent on VOEN

LW1 to LW0 — First pixel position in VRO data for FS1 = 0; FS0 = 0 (RGB) and FS1 = 0; FS0 = 1(YUV):

LW1	LW0	31 to 24	23 to 16	15 to 8	7 to 0	
0	0	pixel 0	pixel 0	pixel 1	pixel 1	EFE = 0, TRR = 0
0	1	pixel 0	pixel 0	pixel 1	pixel 1	
1	0	black	black	pixel 0	pixel 0	
1	1	black	black	pixel 0	pixel 0	

First pixel position in VRO data for FS1 = 1; FS0 = 1 (monochrome):

LW1	LW0	31 to 24	23 to 16	15 to 8	7 to 0	
0	0	pixel 0	pixel 1	pixel 2	pixel 3	EFE = 0, TRR = 0
0	1	black	pixel 0	pixel 1	pixel 2	
1	0	black	black	pixel 0	pixel 1	
1	1	black	black	black	pixel 0	
0	0	pixel 0	pixel 1	X	X	EFE = 1, TRR = 0; LW only effects the greyscale formar
0	1	black	pixel 0	X	X	
1	0	pixel 0	pixel 1	X	X	
1	1	black	pixel 0	X	X	

FS1 to FS0

FIFO output register format select (EFE- bit see "10"):

EFE	FS1	FS0	output format (Tables 2 and 3)
0	0	0	RGB 5-5-5 + alpa; 2x16-bit/pixel; 32-bit word length; RGB matrix on, VRAM output format
0	0	1	YUV 4:2:2; 2x16-bit/pixel; 32-bit word length; RGB matrix off, VRAM output format
0	1	0	YUV 4:2:2; video test mode; 1x16-bit/pixel;16-bit word length; RGB matrix off, optional output format
0	1	1	monochrome mode; 4x8-bit/pixel; 32-bit word length; RGB matrix off, VRAM output format
1	0	0	RGB 5-5-5 + alpa; 1x16-bit/pixel; 16-bit word length; RGB matrix on, VRAM output + transparent format
1	0	1	YUV 4:2:2 + alpa; 1x16-bit/pixel; 16-bit word length; RGB matrix off, VRAM output + transparent format
1	1	0	RGB 8-8-8 + alpa; 1x24-bit/pixel; 24-bit word length; RGB matrix on, VRAM output + transparent format
1	1	1	monochrome mode; 2x8-bit/pixel; 16-bit word length; RGB matrix off, VRAM output + transparent format

"01 and 04"
XD9 to XD0

Pixel number per line (straight binary) on output (VRO):
00 0000 0000 to 11 1111 1111 (number of XS pixels as a maximum)

"02 and 04"
XS9 to XS0

Pixel number per line (straight binary) on inputs (YIN and UVIN):
00 0000 0000 to 11 1111 1111 (number of input pixels per line as maximum)

"03 and 04"
XO8 to XO0

Horizontal start position (straight binary) of scaling window (take care of active pixel number per line).

start with 1st pixel after HREF rise = 0 0001 0000 to 1 1111 1111 (010 to 1FF)

window start and window end may be cut by internal delay compensated HREF = 0 phase. XO has to be matched to the internal processing delay to get full scaling range

"04"
HF2 to HF0

Horizontal decimation filter (Figures 13 and 14):

HF2	HF1	HF0	taps	filter
0	0	0	2	filter 1 $(1/2\ (1 + z^{-1}))$
0	0	1	3	filter 2 $(1/4\ (1 + 2z^{-1} + z^{-2}))$
0	1	0	5	filter 3 $(1/8\ (1 + 2z^{-1} + 2z^{-2} + 2z^{-3} + z^{-4}))$
0	1	1	9	filter 4 $(1/16\ (1 + 2z^{-1} + 2z^{-2} + 2z^{-3} + 2z^{-4} + 2z^{-5} + 2z^{-6} + 2z^{-7} + z^{-8}))$
1	0	0	1	filter bypassed
1	0	1	1	filter bypassed + delay in Y channel of 1T
1	1	0	8	filter 5 $(1/16\ (1 + 3z^{-1} + 3z^{-2} + z^{-3} + z^{-4} + 3z^{-5} + 3z^{-6} + z^{-7}))$
1	1	1	4	$(1/8\ (1 + 3z^{-1} + 3z^{-2} + z^{-3}))$

"05 and 08"
YD9 to YD0

Line number per output field (straight binary):
00 0000 0000 to 11 1111 1111 (number of YS lines as a maximum)

"06 and 08" YS9 to YS0	Line number per input field (straight binary): 00 0000 0000 0 line 11 1111 1111 1023 lines (maximum = number of lines/field – 3)
"07 and 08" YO8 to YO0	Vertical start of scaling window. "0" equals 3rd line after rising slope of VS input signal. Take care of active line number per field (straight binary). 0 0000 0000 start with 3rd line after the rising slope of VS 0 0000 0011 start with 1st line after the falling slope of nominal VS (SAA7151B/91B) 1 1111 1111 511 + 3 lines after the rising slope of VS (maximum value)
"08" AFS	Adaptive filter switch: 0 = off; use VP1, VP0 and HF2 to HF0 bits 1 = on; filter characteristics are selected by the scaler
VP1 to VP0	Vertical data processing VP1 VP0 | processing 0 0 | bypassed 0 1 | delay of one line $H(z) = z^{-H}$ 1 0 | vertical filter 1: $(H(z) = 1/2 (1 + z^{-H}))$ 1 1 | vertical filter 2: $(H(z) = 1/4 (1 + 2z^{-H} + z^{-2H}))$
"09 and 0B" VS8 to VS0	Vertical bypass start, sets begin of the bypass region (straight binary). Scaling region overrides bypass region (YO bits): 0 0000 0000 start with 3rd line after the rising slope of VS 0 0000 0011 start with 1st line after the falling slope of nominal VS (SAA7151B/91B) 1 1111 1111 511 + 3 lines after the rising slope of VS (maximum value)
"0A and 0B" VC8 to VC0	Vertical bypass count, sets length of bypass region (straight binary): 0 0000 0000 0 line length 1 1111 1111 511 lines length (maximum = number of lines/field – 3)
TCC	Two's complement input data select (U, V): 0 = binary input data 1 = two's complement input data
POE	Polarity, internally detected odd/even flag O/E: 0 = flag unchanged; 1 = flag inverted
"0C" VL7 to VL0	Set lower limit for V colour-difference signal (8 bit; two's complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
"0D" VU7 to VU0	Set upper limit for V colour-difference signal (8 bit; two's complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level

"0E" UL7 to UL0	Set lower limit for U colour-difference signal (8 bit; two´s complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
"0F" UU7 to UU0	Set upper limit for U colour-difference signal (8 bit; two´s complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
"10" MCT	Monochrome and two´s complement output data select: 0 = inverse grayscale luminance (if grayscale is selected by FS bits) or straight binary U, V data output 1 = non-inverse monochrome luminance (if grayscale is selected by FS bits) or two`complement U, V data output
QPL	Line qualifier polarity flag : 0 = LNQ is active-LOW (pin 1 and on VRO1, pin 99); 1 = LNQ is active-HIGH
QPP	Pixel qualifier polarity flag : 0 = PXQ is active-LOW (VRO0, pin 100); 1 = PXQ is active-HIGH
TTR	Transparent data transfer: 0 = normal operation (VRAM protocol valid,) 1 = FIFO register transparent (output FIFO in shift register mode)
EFE	Extended formats enable, FS-bits in subaddress "00"

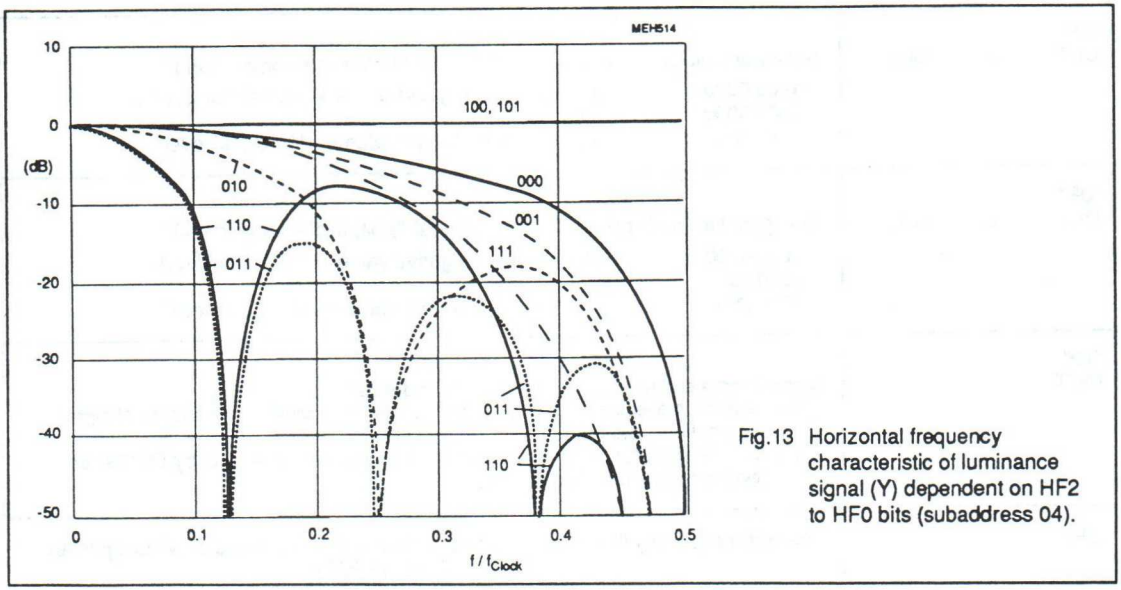


Fig.13 Horizontal frequency characteristic of luminance signal (Y) dependent on HF2 to HF0 bits (subaddress 04).

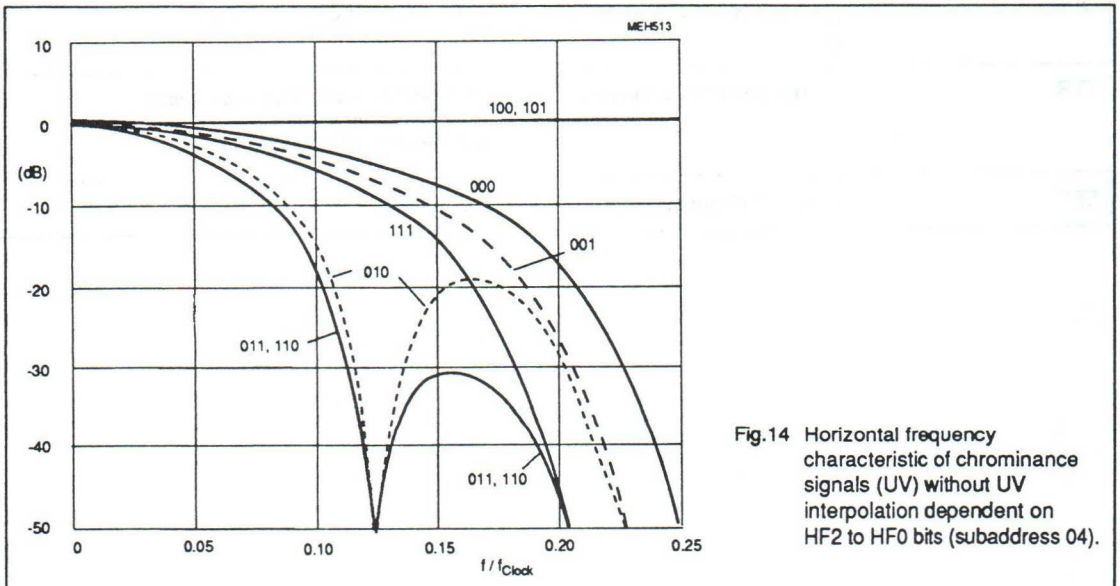


Fig.14 Horizontal frequency characteristic of chrominance signals (UV) without UV interpolation dependent on HF2 to HF0 bits (subaddress 04).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

10. LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 14, 26, 40, 55, 67, 76 and 91)	−0.5	6.5	V
V_I	DC input voltage on all pins	−0.5	V_{DD}	V
I_{DD}	supply current (pins 5, 14, 26, 40, 55, 67, 76 and 91)	-	70	mA
P_{tot}	total power dissipation	0	1	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±2000	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

11. DC CHARACTERISTICS

V_{DD1} to V_{DD8} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 5, 14, 26, 40, 55, 67, 76 and 91)		4.5	5	5.5	V
I_P	total supply current ($I_{DD1} + I_{DD2} + I_{DD3} I_{DD4} + I_{DD5} + I_{DD6} + I_{DD7} + I_{DD8}$)	inputs LOW and outputs without load	-	80	-	mA
Data and control inputs						
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DD}+0.5	V
I_{LI}	input leakage current	V_{IL} = 0	-	-	10	µA
C_I	input capacitance	data	-	-	8	pF
		clocks	-	-	10	pF
Data and control outputs						
V_{OL}	output voltage LOW	note 1	-	-	0.6	V
V_{OH}	outputt voltage HIGH	note 1	2.4	-	-	V
3-state outputs						
$I_{O\,off}$	high-impedance output current		-	-	±5	µA
C_O	high-impedance output capacitance		-	-	8	pF
I²C-bus, SDA and SCL (pins 44 and 45)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3	-	V_{DD}+0.5	V
$I_{44, 45}$	input current		-	-	±10	µA
I_{ACK}	output current on pin 44	acknowledge	3	-	-	mA
V_{OL}	output voltage at acknowledge	I_{44} = 3 mA	-	-	0.4	V

12. AC CHARACTERISTICS

V_{DD1} to V_{DD8} = 4.5 to 5.5 V; T_{amb} = 0 to 60 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LLC timing (pin 36)		Fig.11				
t_{LLC}	cycle time		31	-	45	ns
t_p	pulse width (duty factor)	$t_{LLC\,H} / t_{LLC}$	40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
Input data and CREF timing		Fig.15				
t_{SU}	setup time		11	-	-	ns
t_{HD}	hold time		3	-	-	ns
VCLK timing (pin 51)		Fig.16				
t_{VCLK}	VRAM port clock cycle time	note 2	50	-	200	ns
$t_{p\,L}$, $t_{p\,H}$	LOW and HIGH times	note 3	17	-	-	ns
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
Output data and reference signal timing		Figures 15 and 16				
C_L	load capacitance	VRO outputs	15	-	40	pF
		other outputs	7.5	-	25	pF
t_{OH}	VRO data hold time	C_L = 10 pF; note 4	0	-	-	ns
t_{OHL}	related to LLC (INCADR, HFL)	C_L = 10 pF; note 5	0		-	ns
t_{OHV}	related to VCLK (HFL)	C_L = 10 pF; note 5	0		-	ns
t_{OD}	VRO data delay time	C_L = 40 pF; note 4	-	-	25	ns
t_{ODL}	related to LLC (INCADR, HFL)	C_L = 25 pF; note 5	-	-	60	ns
t_{ODV}	related to VCLK (HFL)	C_L = 25 pF; note 5	-	-	60	ns
t_D	output disable time to 3-state	C_L = 40 pF; note 6	-	-	40	ns
t_E	output enable time from 3-state	C_L = 40 pF; note 6	-	-	40	ns
$t_{HFL\,VOE}$	HFL maximum response time	VRAM port enabled	-	-	810	ns
$t_{HFL\,VCLK}$	HFL maximum response time	HFL set at beginning of VCLK burst	-	-	840	ns

Notes to the caracteristics

1. Levels are measured with load circuit. VRO outputs with 1.2 kΩ in parallel to 25 pF at 3 V (TTL load).
2. Maximum t_{VCLK} = 200 ns for test mode only. The applicable maximum cycle time depends on data format, horizontal scaling and input data rate.
3. Measured at 1,5 V level; $t_{p\,L}$ may be unlimited.
4. Timings of VRO refer to the rising edge of VLCK.
5. The timing of INCADR refers to LLC; the rising edge of HFL always refers to LLC. During a VRAM transfer is the falling edge of HFL generated by VCLK. Both edges of HFL refer to LLC during horizontal increment and vertical reset cycles.
6. Asynchronous signals with timing refering to the 1.5 V switching point of VOEN input signal (pin 50).

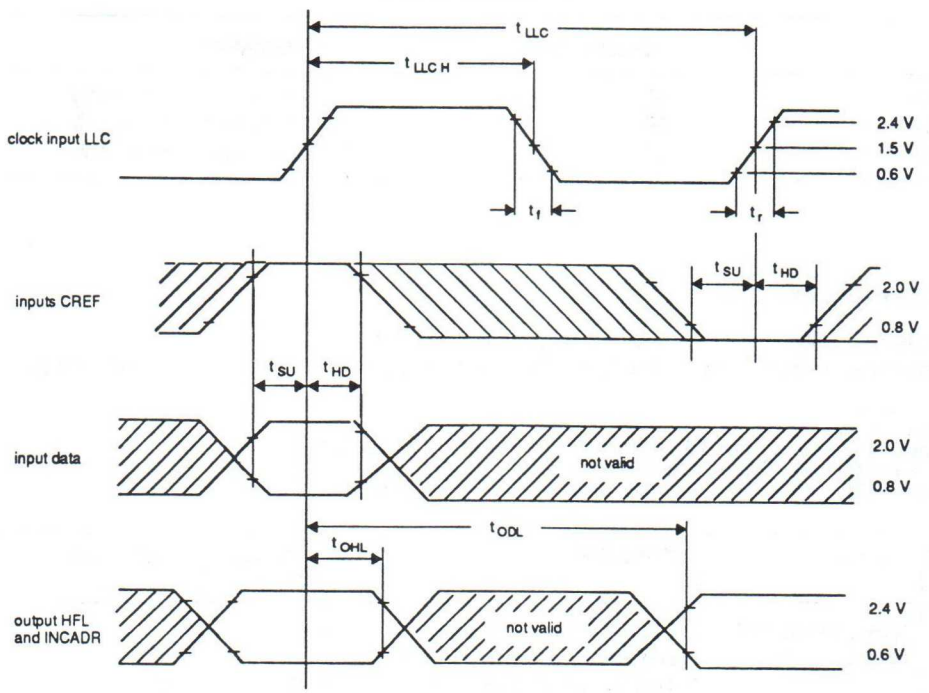


Fig.15 Data input timing (LLC).

MEH408-1

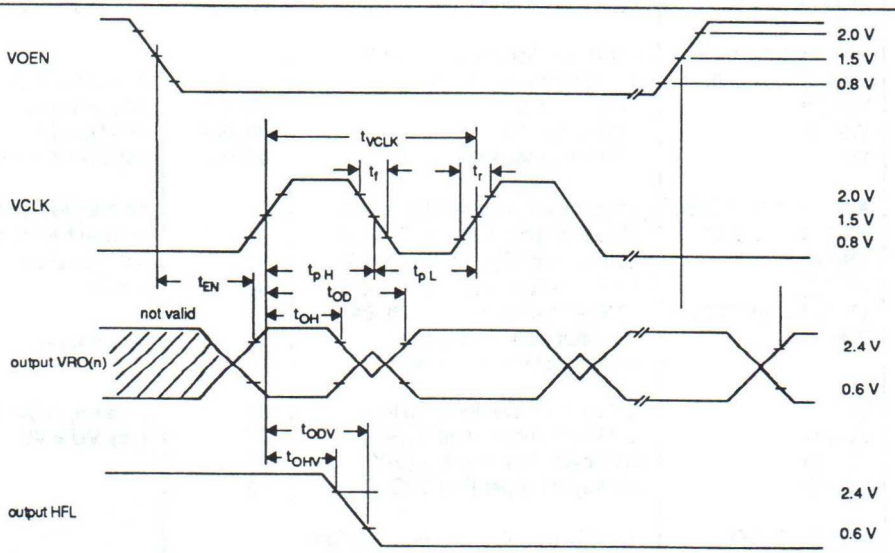


Fig.16 Data output timing (VCLK).

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13. PROCESSING DELAYS

PORTS	DELAY IN LLC	REMARKS`
YIN to VRO	58	in transparent mode only
UVIN to VRO	58	in transparent mode only
HREF to VRO	58	in transparent mode only

14. PROGRAMMING EXAMPLE

Slave address byte is B8h at pin IICSA = 0 (or BCh at pin IICSA = +5 V).
This example shows the setting via I²C-bus for the processing of a picture segment at 1:1 horizontal and vertical scale.

Values in brackets [..]:
If no scaling or panning is wanted,
the parameters XD, XS, YD and YS should be set to the maximum value 3FFh.
the parameters XO and YO should be set to the minimum value 000h.
(in this case, HREF and VS from external define the SAA7186 processing window).

SUBADDR. (hex)	BITS	FUNCTION	VALUE (hex)	COMMENT
00	RTB, OF(1:0), VPE, LW(1:0), FS(1:0),	ROM table control and field sequence processing; VRAM port enable; output format select	11	(1)
01	XD(7:0)	LSB´s output pixel/line	80 [FF]	384 pixels out
02	XS(7:0)	LSB´s input pixel/line	80 [FF]	384 pixels in
03	XO(7:0)	LSB´s for horizontal window start	10 [00]	1st pixel after HREF = 1
04	HF(2:0), XO(8), XS(9, 8), XD(9, 8)	horizontal filter select and MSB´s of subaddresses 01, 02, 03	85 [8F]	horizontal filter bypassed
05	YD(7:0)	LSB´s output lines/field	90 [FF]	144 lines out
06	YS(7:0)	LSB´s input lines/field	90 [FF]	144 lines in
07	YO(7:0)	LSB´s vertical window start	03 [00]	1st line after VS = 0; (2)
08	AFS, VP(1:0), YO(8), YS(9, 8), YD(9, 8)	adaptive and vertical filter select; MSB´s of subaddresses 05, 06, 07	00 [FF]	no adaptive select vertical filter bypassed
09	VS(7:0)	LSB´s vertical bypass start position	00	not bypassed
0A	VC(7:0)	LSB´s vertical bypass lines/field	00	region
0B	VS(8), VC(8), TCC, POE	MSB´s of subaddresses 09, 0A; UV input data representation and odd/even polarity switch	00	defined; (3) (4)
0C	VL(7:0)	UV keyer: lower limit V (R-Y)	00	) keying is switched off
0D	VU(7:0)	UV keyer: upper limit V (R-Y)	FF	) by VU < VL
0E	UL(7:0)	UV keyer: lower limit U (B-Y)	00	-
0F	UU(7:0)	UV keyer: upper limit U (B-Y)	00	-
10	MCT, QPP, QPL, TTR, EFE	Y or UV output data representation, output data transfer mode, pixel/ line qualifier polarity.	00	(5)

Notes to the programming examples

(1) RTB = 0 ROM table is active (only for RGB formats)
OF = 00 SAA7186 processes the both fields for interlaced display
VPE = 1 VRAM port is enabled

LW = 00 longword position of first pixel in each output line = 0
FS = 01 16-bit 4:2:2 YUV output format is selected

(2) for nominal VS length of 6 x H-period (input SAA7191B respectively SAA7151B with active VNL)

(3) TTC = 0 straight binary UV input data expected

(4) odd/even polarity unchanged - can be used to change the field sequence if phase relations between HREF and VS are not according to SAA7191B respectively SAA7151B specification

(5) MCT = 0 when EFE, FS = 001h: UV output data are straight binary
QPP = 0 the pixel qualifier PXQ is "0"-active (if TTR, EFE = 1)

QPL = 0 line qualifier LNQ is "0"-active (if TTR, EFE = 1)
TTR = 0 VRAM port is set to data burst transfer
EFE = 0 32-bit longword formats selected.

Digital multistandard colour decoder, square pixel (DMSD-SQP)

SAA7191B



CONTENTS

1. FEATURES
2. GENERAL DESCRIPTION
3. QUICK REFERENCE DATA
4. ORDERING INFORMATION
5. BLOCK DIAGRAM
6. PINNING
7. FUNCTIONAL DESCRIPTION
8. LIMITING VALUES
9. CHARACTERISTICS
10. I²C-BUS FORMAT
11. PACKAGE OUTLINE
12. UPDATE HISTORY
13. SOLDERING
14. DEFINITIONS

Digital multistandard colour decoder, square pixel (DMSD-SQP)

SAA7191B

1. FEATURES

- Separate 8-bit luminance (Y or CVBS) and 8-bit chrominance inputs (CVBS or C) from CVBS, Y/C, S-Video (S-VHS or Hi8) sources
- Luminance and chrominance signal processing for standards PAL-B/G, NTSC-M, SECAM
- Horizontal and vertical sync detection for all standards
- Real-time control output RTCO to be used for frequency-locked digital video encoder (SAA7199B). RTCO contains serialized information about actual clock frequency, subcarrier frequency and PAL/SECAM sequence.
- Controls via the I^2C-bus
- User programmable aperture correction (horizontal peaking)
- Compatible with memory-based features (line-locked clock)
- Cross-colour reduction by chrominance comb-filtering (NTSC) or by special cross colour cancellation (SECAM)
- 8-bit quantization of input signals
- 768/640 active samples per line equals 50/60 Hz (SQP)
- The YUV bus supports data rates of 780 x f_H equal to 12.2727 MHz for 60 Hz (NTSC-M) and 944 x f_H equal to 14.75 MHz for 50 Hz (PAL–B/G, SECAM) in 4 : 1 : 1 or 4 : 2 : 2 formats (via the I^2C-bus)
- One crystal oscillator of 26.8 MHz

2. GENERAL DESCRIPTION

The SAA7191B is a digital multistandard colour decoder suitable for 8-bit CVBS input signals or for 8-bit luminance and 8-bit chrominance input signals (Y/C).

The SAA7191B is down-compatible with SAA7191. The SAA7191B has additional outputs RTCO, GPSW0 and ODD. These new outputs are in high-impedance state when NFEN-bit = 0.

3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage (pins 5, 18, 28, 37 and 52)	4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37 and 52)	-	100	250	mA
V_{IL}	input levels	TTL-compatible			
V_{OL}	output levels	TTL-compatible			
T_{amb}	operating ambient temperature	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7191B	68	PLCC	plastic	SOT188

5. BLOCK DIAGRAM

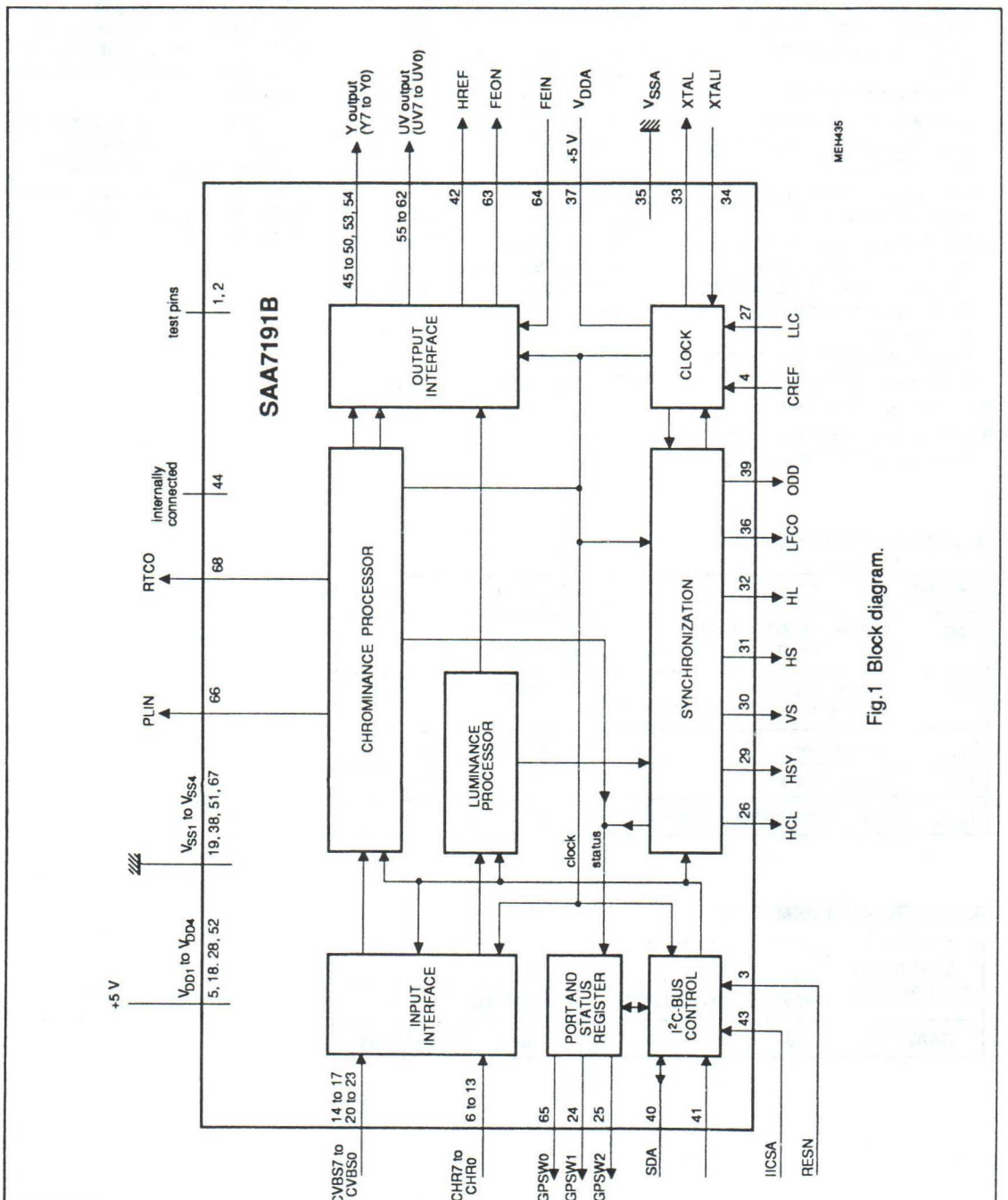


Fig.1 Block diagram.

6. PINNING

SYMBOL	PIN	DESCRIPTION
SP	1	connected to ground (shift pin for testing)
AP	2	connected to ground (action pin for testing)
RESN	3	reset, active LOW
CREF	4	clock reference, sync from external to ensure in-phase signals on the YUV-bus
V_{DD1}	5	+5 V supply input 1
CHR0	6	chrominance input data bits CHR7 to CHR0 from a Y/C (VHS, Hi8) source in two's complement format
CHR1	7	
CHR2	8	
CHR3	9	
CHR4	10	
CHR5	11	
CHR6	12	
CHR7	13	
CVBS0	14	luminance respectively CVBS lower input data bits CVBS3 to CVBS0 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS1	15	
CVBS2	16	
CVBS3	17	
V_{DD2}	18	+5 V supply input 2
V_{SS1}	19	ground 1 (0 V)
CVBS4	20	luminance respectively CVBS upper input data bits CVBS7 to CVBS4 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS5	21	
CVBS6	22	
CVBS7	23	
GPSW1	24	Port 1 output for general purpose (programmable)
GPSW2	25	Port 2 output for general purpose (programmable)
HCL	26	black level clamp pulse (programmable), e.g. for TDA8708 (ADC)
LLC	27	line-locked clock input signal (29.5 MHz for 50 Hz system; 24.5454 MHz for 60 Hz system)
V_{DD3}	28	+5 V supply input 3
HSY	29	horizontal sync indicator output signal (programmable), e.g. for TDA8708 (ADC)
VS	30	vertical sync output signal
HS	31	horizontal sync output signal (programmable)
HL	32	horizontal lock flag, HIGH = PLL locked
XTAL	33	26.8 MHz clock output
XTALI	34	26.8 MHz connection for crystal or external oscillator (TTL compatible squarewave)

SYMBOL	PIN	DESCRIPTION
V_{SSA}	35	analog ground
LFCO	36	line frequency control output signal, multiple of horizontal frequency (7.375 MHz/6.136363 MHz)
V_{DDA}	37	+5 V supply input for analog part
V_{SS2}	38	ground 2 (0 V)
ODD	39	odd/even field identification output (odd = HIGH); active only at NFEN-bit = 1
SDA	40	I^2C-bus data line
SCL	41	I^2C-bus clock line
HREF	42	horizontal reference output for valid YUV data (for active line 768Y or 640Y samples long)
IICSA	43	set module address input (LOW = 1000 101X; HIGH = 1000 111X)
i.c.	44	internally connected
Y7	45	Y signal output bits Y7 to Y2 (luminance), part of the digital YUV-bus
Y6	46	
Y5	47	
Y4	48	
Y3	49	
Y2	50	
V_{SS3}	51	ground 3 (0 V)
V_{DD4}	52	+5 V supply input 4
Y1	53	Y signal output bits Y1 to Y0 (luminance), part of the digital YUV-bus
Y0	54	
UV7	55	UV signal output bits UV7 to UV0 (colour-difference), part of the digital YUV-bus
UV6	56	
UV5	57	
UV4	58	
UV3	59	
UV2	60	
UV1	61	
UV0	62	
FEON	63	output active flag (active LOW when Y and UV data in high-impedance state)
FEIN	64	fast enable input (active LOW to control fast switching due to YUV data)
GPSW0	65	Port 0 output for general purpose (programmable); active only at NFEN-bit = 1
PLIN	66	PAL flag (active LOW at inverted line); SECAM flag (LOW equals DR, HIGH equals DB line)
V_{SS4}	67	ground 4 (0 V)
RTCO	68	real-time control output active at NFEN-bit = 1; Fig.7

Digital multistandard colour decoder, square pixel (DMSD-SQP)

SAA7191B

PIN CONFIGURATION

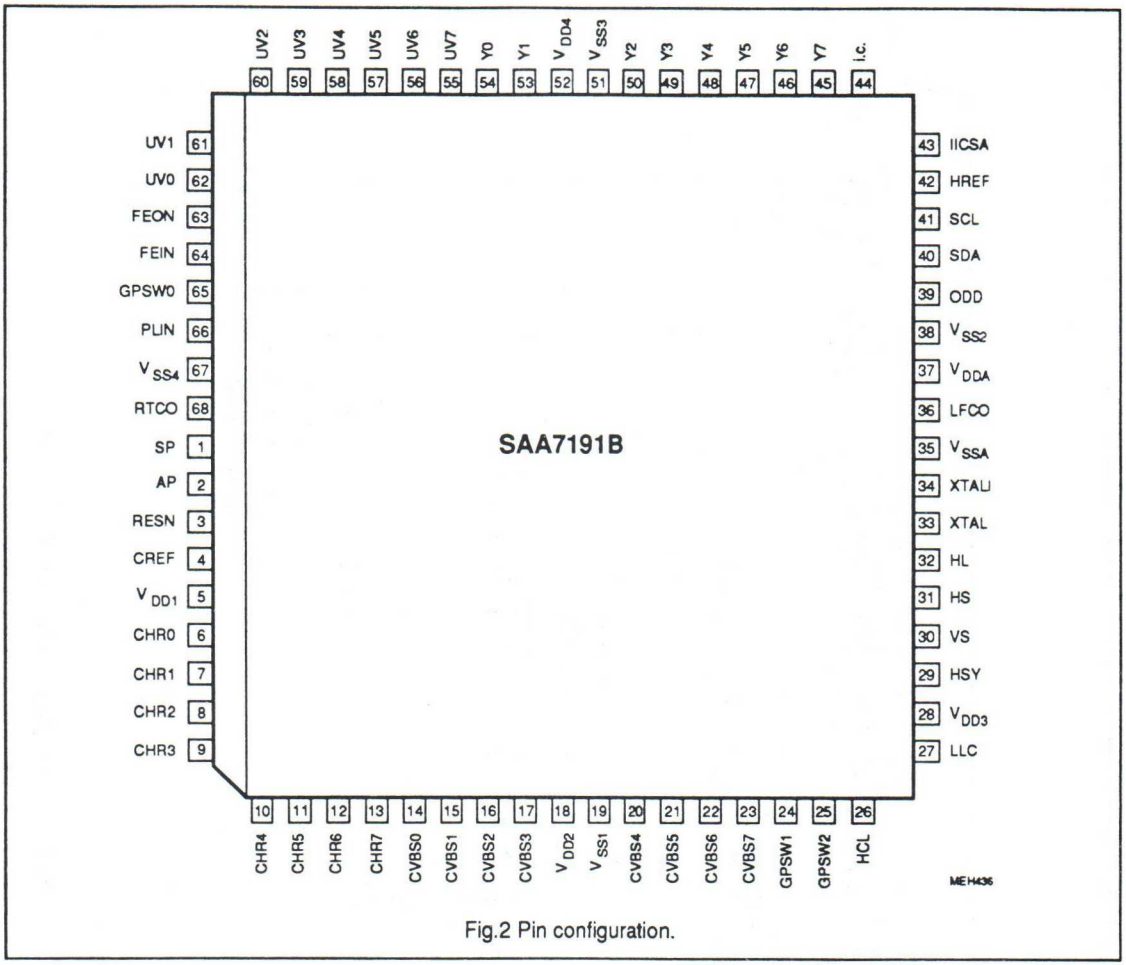


Fig.2 Pin configuration.

7. FUNCTIONAL DESCRIPTION

Chrominance processor

The 8-bit chrominance input signal (CVBS or chrominance format). passes a bandpass filter to eliminate DC components and to decimate the sample rate before it is fed to the two multipliers (quadrature demodulator), Fig.3(a).
Two subcarrier signals from a local oscillator (0 and 90 degree) are fed to the multiplicator inputs of the multipliers. The multipliers operate as a quadrature demodulator for all PAL and NTSC signals; it operates as a frequency down-mixer for SECAM signals.
The two multiplier output signals are converted to a serial data stream and applied to three low-pass filter stages, then to a gain controlled amplifier. A final multiplexed low-pass filter achieves, together with the preceding stages, the required bandwidth performance.
The signals, originated from PAL and NTSC, are applied to a comb-filter.
The signals, originated from SECAM, are fed through a Cloche filter (0 Hz centre frequency), a phase demodulator and a differentiator to obtain frequency-demodulated colour-difference signals.
The SECAM signals are fed after de-emphasis to a cross-over switch, to provide the both serial-transmitted colour-difference signals. These signals are fed finally to the output formatter stages and to the output interface.

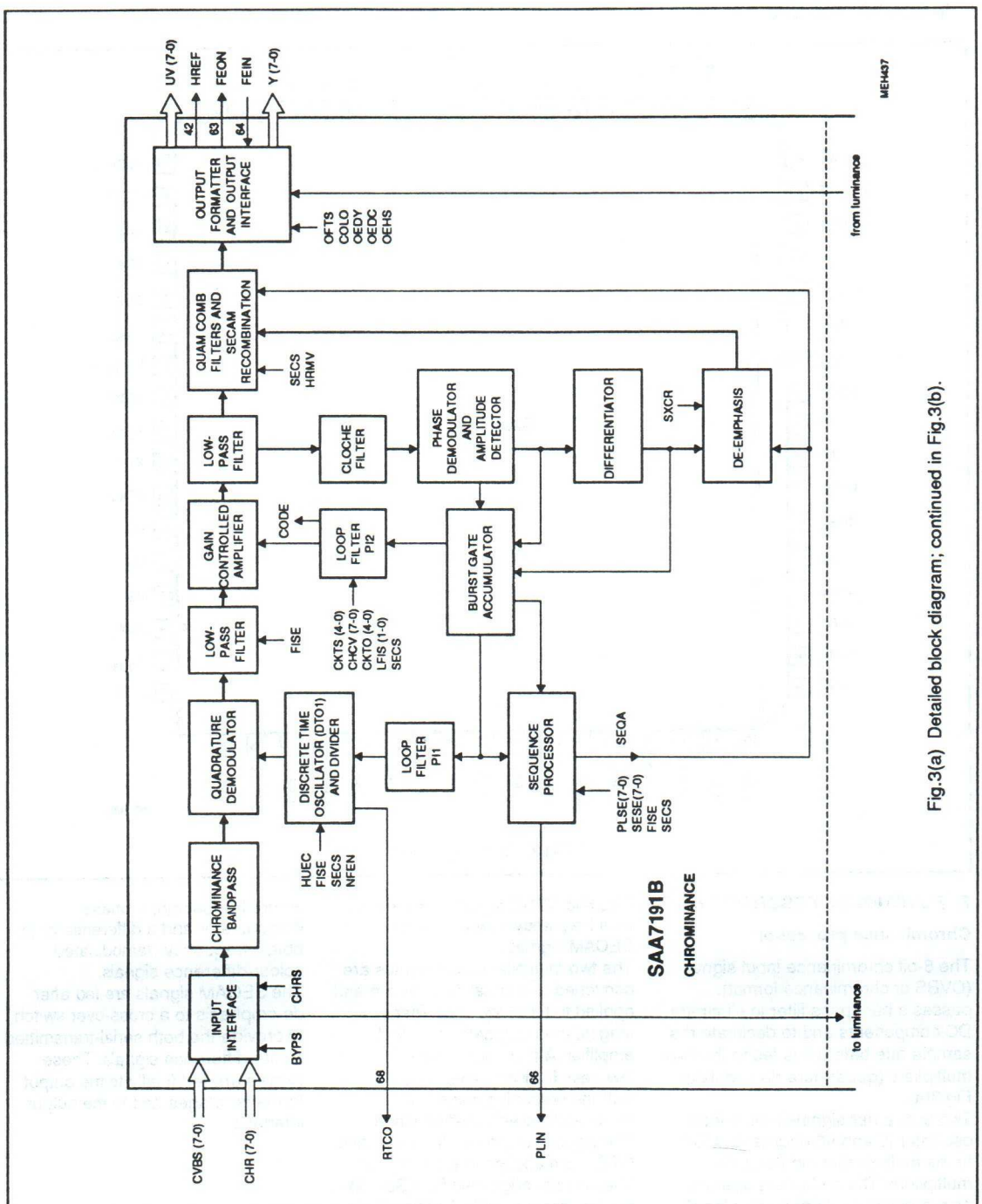


Fig.3(a) Detailed block diagram; continued in Fig.3(b).

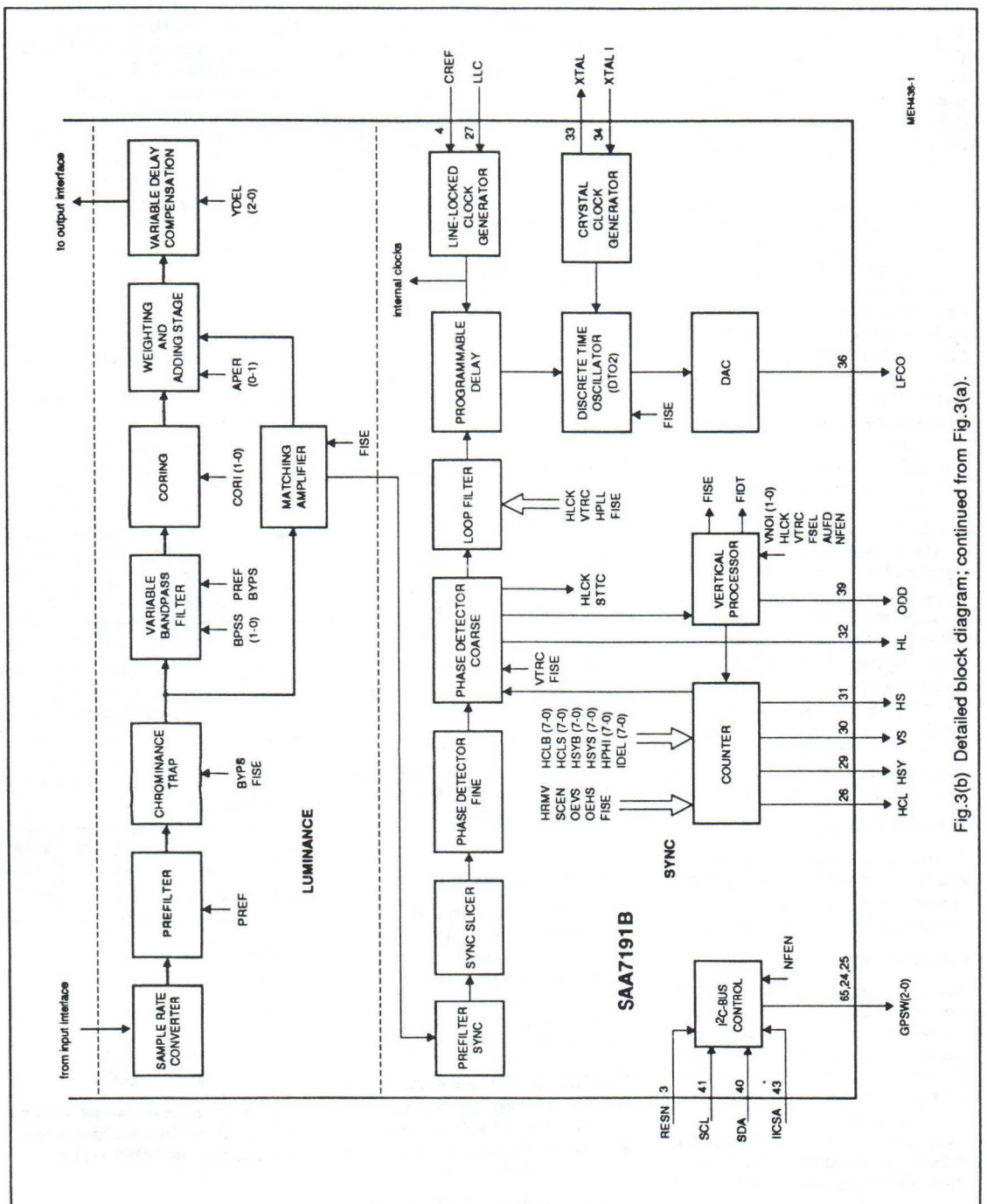


Fig.3(b) Detailed block diagram; continued from Fig.3(a).

Luminance processor

The luminance input signal, a digital CVBS format or an 8-bit luminance format (S-VHS, Hi8), is fed through a sample rate converter to reduce the data rate to 14.75 MHz for PAL and SECAM (12.2727 MHz for NTSC), Fig.3(b).

Sample rate is converted by means of a switchable pre-filter. High frequency components are emphasized to compensate for loss in the following chrominance trap filter. This chrominance trap filter (f_o = 4.43 MHz or f_o = 3.58 MHz centre frequency selectable) eliminates most of the colour carrier signal, therefore, it must be by-passed for S-Video (S-VHS and Hi8) signals.
The high frequency components of the luminance signal can be "peaked" (control for sharpness improvement via the I²C-bus) in two bandpass filters with selectable transfer characteristic.
A coring circuit with selectable characteristic improves the signal once more, this signal is then added to the original ("unpeaked") signal. A switchable amplifier achieves a common DC amplification, because the DC gains are different in both chrominance trap modes.
The improved luminance signal is fed to the variable delay compensation.

Processing delay

The delay from input to output is 220 LLC cycles if YDEL is set to 0. The processing delay will be influenced in future enhancements.

Synchronization

The luminance output signal is fed to the synchronization stage. Its bandwidth is reduced to 1 MHz in a low-pass filter. The sync pulses are sliced and fed to the phase detectors to be compared with the sub-divided clock frequency.
The resulting output signal is applied to the loop filter to accumulate all phase deviations. Adjustable output signals (e. g. HCL and HSY) are generated according to peripheral requirements (TDA8708A, TDA8709A). The output signals HS, VS and PLIN are locked to the timing reference signal HREF (Figures 6 and 7).
There is no absolute timing reference guaranteed between the input signal and the HREF signal as further improvements to the circuit may change the total processing delay. It is therefore not recommended to use them for applications, which ask for absolute timing accuracy to the input signals.
The loop filter signal drives an oscillator to generate the line frequency control output signal LFCO.

Table 1 Clock frequencies in MHz for 50/60 Hz systems

CLOCK	50 Hz	60 Hz
LLC	29.5	24.545454
LLC2	14.75	12.272727
LLC4	7.375	6.136136
LLC8	3.6875	3.068181

Line locked clock frequency

LFCO is required in an external PLL (SAA7197) to generate the line locked clock frequency.

YUV-bus, digital outputs

The 16-bit YUV-bus transfers digital data from the output interfaces to a feature box, or to the digital-to-analog converter (DAC). Outputs are controlled via the I²C-bus in normal selections, or they are controlled by output enable chain (FEIN on pin 64, Fig.4).
The YUV-bus data rate equals LLC2 in Table 1. Timing is achieved by marking each second positive rising edge of the clock LLC in conjunction with CREF (clock reference).

YUV-bus formats 4:2:2 and 4:1:1

The output signals Y7 to Y0 are the bits of the digital luminance signal. The output signals UV7 to UV0 are the bits of the multiplexed colour-difference signals (B–Y) and (R–Y). The frame in the following tables is the time, required to transfer a full set of samples. In case of 4 : 2 : 2 format two luminance samples are transmitted in comparision to one U and one V sample within one frame.

Table 2 4 : 2 : 2 format (768 pixels per line for 50 Hz system; 640 pixels per line for 60 Hz system)

OUTPUT	PIXEL BYTE SEQUENCE					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7(MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Notes to Table 2

1. Data rate: LLC2
2. Sample frequency:
   Y LLC2
   U LLC4
   V LLC4

The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

Table 3 4 : 1 : 1 format (768 pixels per line for 50 Hz system and 640 pixels per line for 60 Hz system)

OUTPUT	PIXEL BYTE SEQUENCE							
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7 (MSB)	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			

Fast enable is achieved by setting input FEIN to LOW. This signal is used to control fast switching on the digital YUV-bus. HIGH on this pin forces the Y and U/V outputs to a high-impedance state. The signal FEON is LOW when the Y and U/V outputs are in this high-impedance state (Fig.4).
The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

Notes to Table 3

Data rate:		LLC2
sample frequency:	Y	LLC2
	U	LLC8
	V	LLC8

Table 4 Digital output control

OEDY	OEDC	FEIN	Y(7:0)	UV(7:0)	FEON
X	X	0	active	active	1
0	0	1	Z	Z	0
0	1	1	Z	active	1
1	0	1	active	Z	1
1	1	X	active	active	1

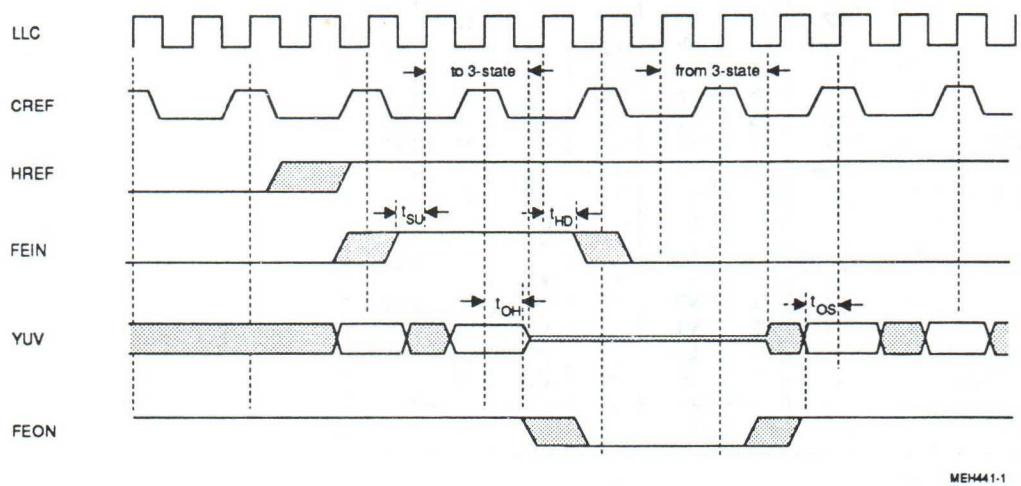
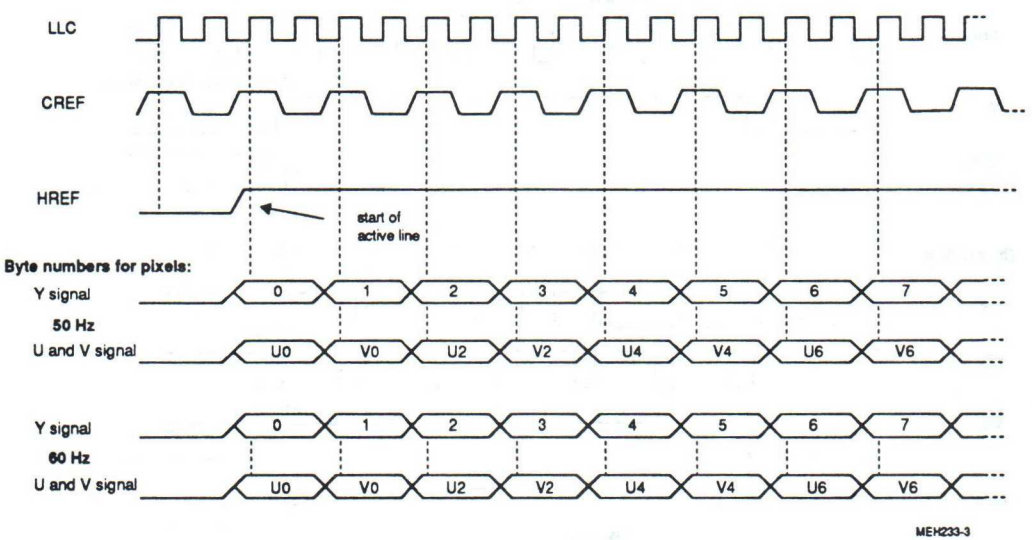


Fig.4 Timing example of fast enable input FEIN.



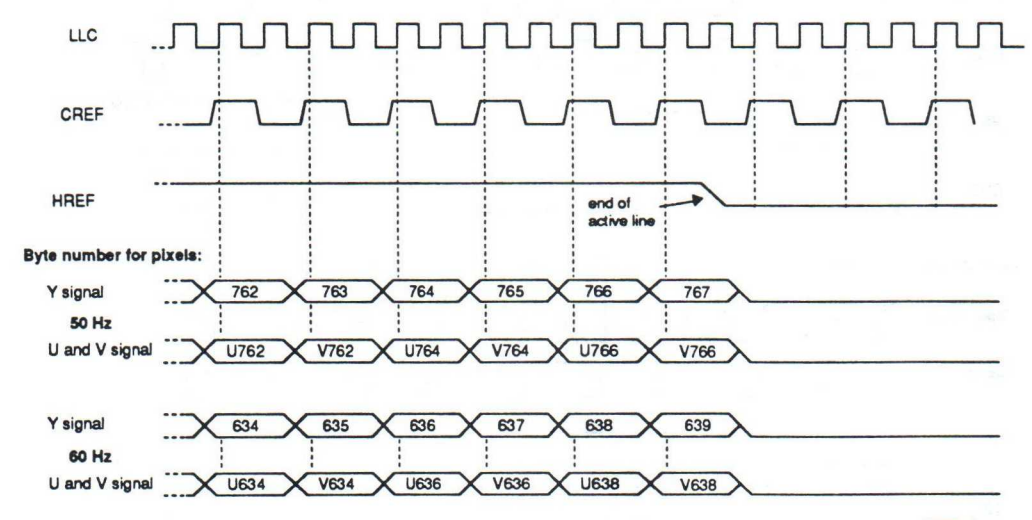


Fig.5 Line control by HREF in 4:2:2 format for 50 Hz and 60 Hz systems.

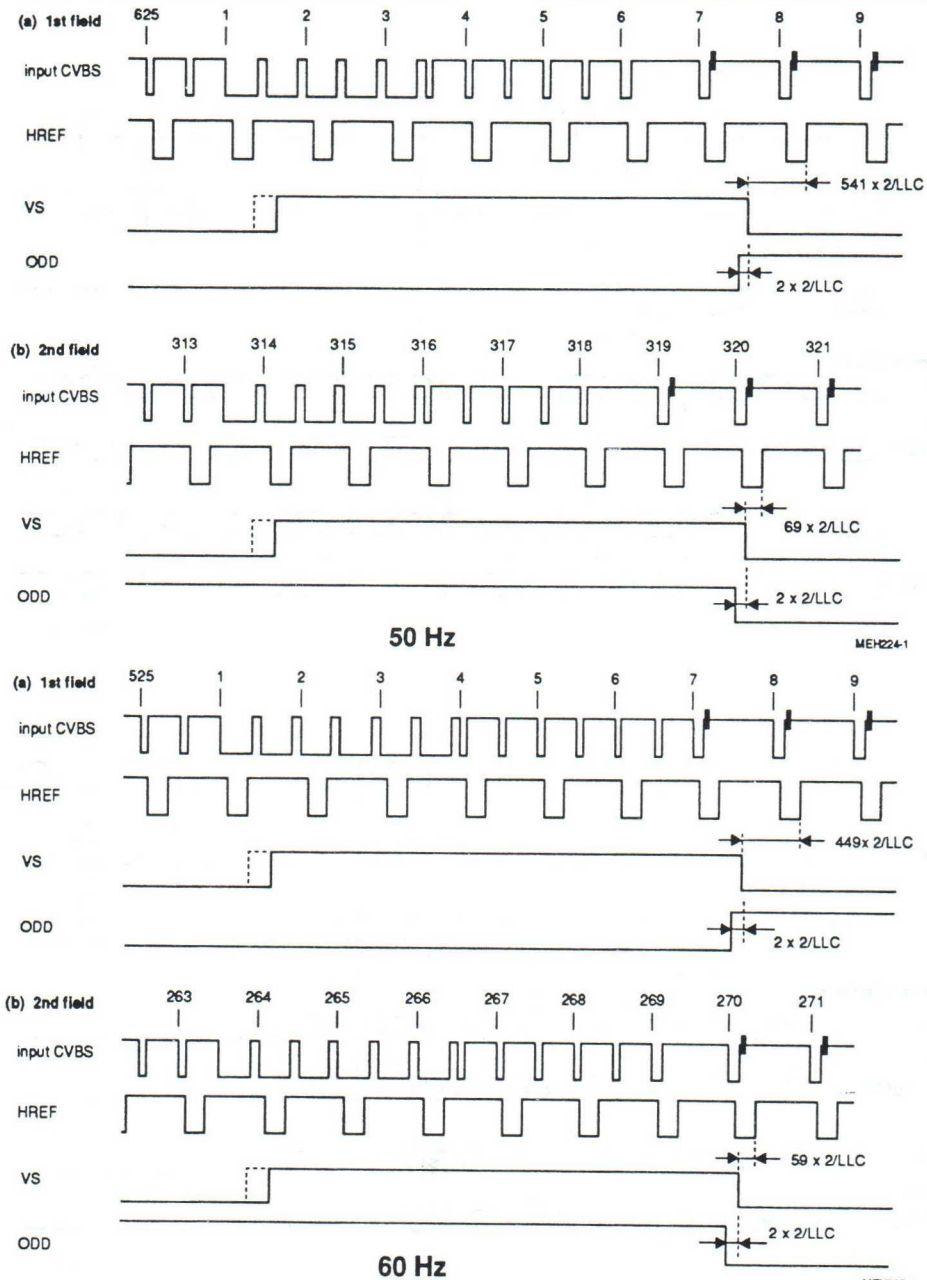


Fig.6 Vertical timing diagram for 50 / 60 Hz.

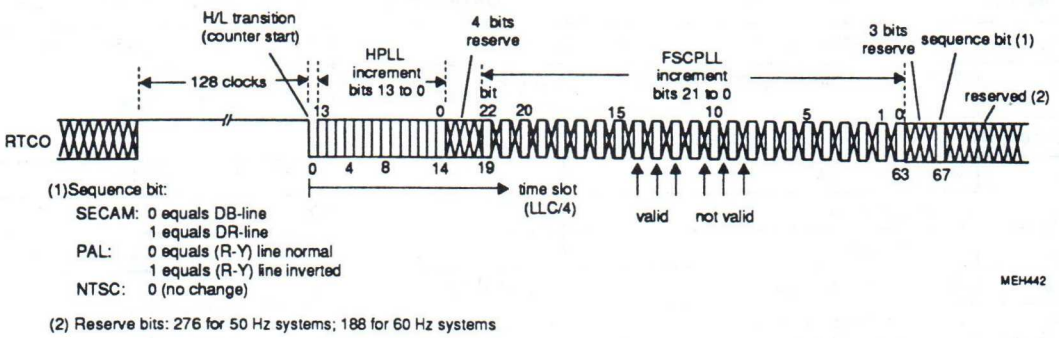


Fig.7 RTCO timing.

8. LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); ground pins 19, 35, 38, 51 and 67 as well as supply pins 5, 18, 28, 37 and 52 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 18, 28, 37, 52)	−0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{SS\ A} - V_{SS\ (1\ to\ 4)}$	-	±100	mV
V_I	voltage on all inputs	−0.5	V_{DD}+0.5	V
V_O	voltage on all outputs ($I_{O\ max}$ = 20 mA)	−0.5	V_{DD}+0.5	V
P_{tot}	total power dissipation	-	2.5	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±2000	V

* Equivalent to discharging a 100 pF capacitor through an 1.5 kΩ series resistor.

9. CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 5, 18, 28, 37, 52)		4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37, 52)	V_{DD} = 5 V; inputs LOW; outputs not connected	-	100	250	mA
I²C-bus, SDA and SCL (pins 40 and 41)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3	-	V_{DD}+0.5	V
$I_{40,41}$	input current		-	-	±10	μA
I_{ACK}	output current on pin 40	acknowledge	3	-	-	mA
V_{OL}	output voltage at acknowledge	I_{40} = 3 mA	-	-	0.4	V
Data clock and control inputs (pins 3, 4, 6 to 17, 20 to 23, 27, 34, 43 and 64), Fig.10						
V_{IL}	LLC input voltage LOW (pin 27)		−0.5	-	0.6	V
V_{IH}	LLC input voltage HIGH		2.4	-	V_{DD}+0.5	V
V_{IL}	other input voltage LOW		−0.5	-	0.8	V
V_{IH}	other input voltage HIGH		2.0	-	V_{DD}+0.5	V
I_{LI}	input leakage current		-	-	10	μA
C_I	input capacitance	data inputs; note 1	-	-	8	pF
		I/O high-ohmic	-	-	8	pF
		clock inputs	-	-	10	pF
$t_{SU.DAT}$	input data set-up time	Fig.8	11	-	-	ns
$t_{HD.DAT}$	input data hold time		3	-	-	ns
LFCO output (pin 36)						
V_o	output signal (peak-to-peak value)	note 2	1.4	-	2.6	V
V_{36}	output voltage range		1	-	V_{DD}	V
YUV-bus, HREF and VS outputs (pins 30, 42, 45 to 50 and pins 53 to 62)			Figures 11 and 15 to 25			
V_{OL}	output voltage LOW	notes 1 and 2	0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitance		15	-	50	pF
Control outputs (pins 24 to 26, 29, 31, 32, 39, 63, 65,66 and 68); Fig.12						
V_{OL}	output voltage LOW	notes 1 and 2	0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitance		7.5	-	25	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing of YUV-bus and control outputs		Fig.7				
t_{OH}	output signal hold time	YUV, HREF, VS at C_L = 15 pF	13	-	-	ns
		controls at C_L = 7.5 pF	13	-	-	ns
t_{OS}	output set-up time	YUV, HREF, VS at C_L = 50 pF;	14	-	-	ns
		controls at C_L = 25 pF	14	-	-	ns
t_{SZ}	data output disable transition time	to 3-state condition	16	-	-	ns
t_{ZS}	data output enable transition time	from 3-state condition	14	-	-	ns
t_{RTCO}	RTCO timing			Fig.7		
Chrominance PLL						
f_C	catching range		±400	-	-	Hz
Crystal oscillator		Fig.9				
f_n	nominal frequency	3rd harmonic	-	26.8	-	MHz
$\Delta f / f_n$	permissible deviation f_n		-	-	±50	10^{-6}
	temperature deviation from f_n		-	-	±20	10^{-6}
X1	crystal specification:					
	temperature range T_{amb}		0	-	70	°C
	load capacitance C_L		8	-	-	pF
	series resonance resistance R_S		-	50	80	Ω
	motional capacitance C_1		-	1.1±20%	-	fF
	parallel capacitance C_0		-	3.5±20%	-	pF
	Philips catalogue number		9922 520 30004			
Line locked clock input LLC (pin 27)		Fig.8				
t_{LLC}	cycle time	note 3	31	-	45	ns
t_p	duty factor	t_{LLCH} / t_{LLC}	40	-	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns

Notes to the characteristics

1. Data output signals are Y7 to Y0 and UV7 to UV0. All others are control output signals.
2. Levels are measured with load circuit. YUV-bus, HREF and VS outputs with 1.2 kΩ in parallel to 50 pF at 3 V (TTL load); LFCO output with 10 kΩ in parallel to 15 pF and other outputs with 1.2 kΩ in parallel to 25 pF at 3 V (TTL load).
3. t_{SU}, t_{HD}, t_{OH} and t_{OD} include t_r and t_f.

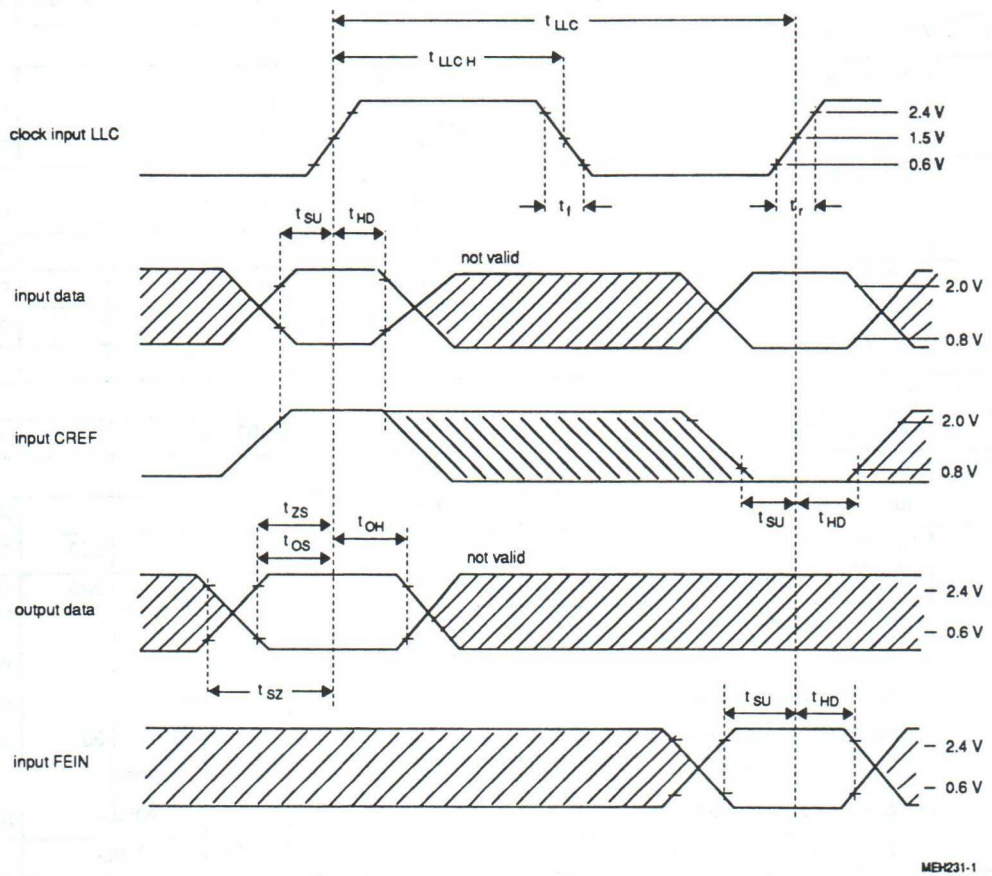


Fig.8 Data input and output timing diagram.

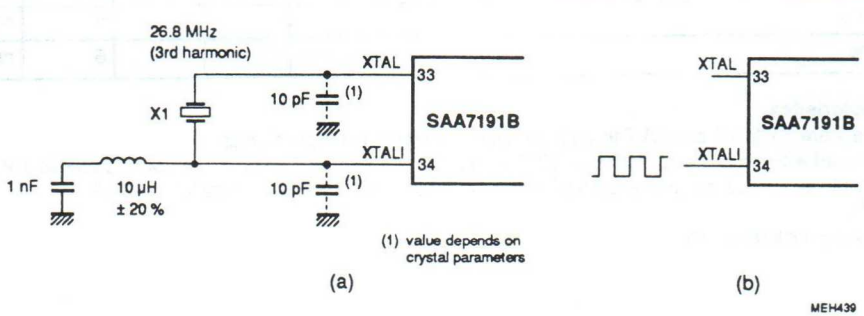
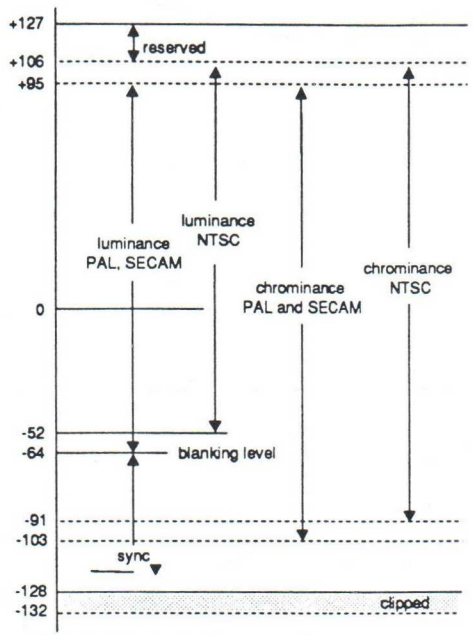
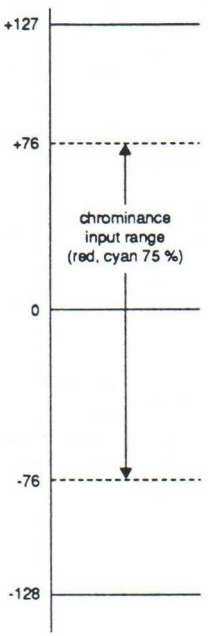


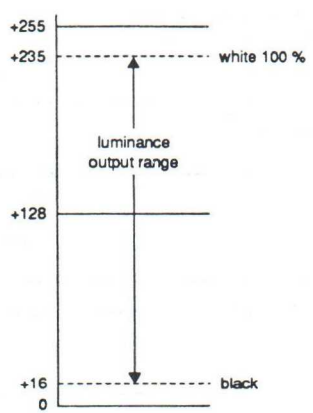
Fig.9 Oscillator application (a) and optional clock from external source (b).



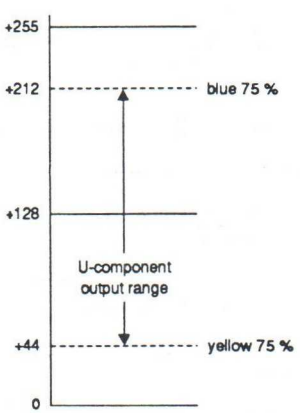
(a) CVBS7 to CVBS0 input signal range.



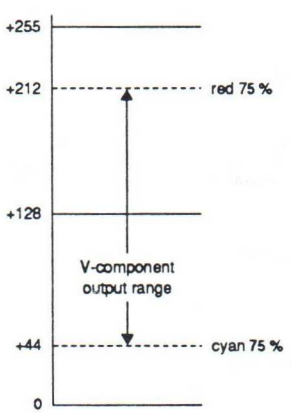
(b) CHR7 to CHR0 input signal range.



(c) Y output signal range.



(d) U output signal range (B-Y).



(e) V output signal range (R-Y).

MEH254-2

Notes: 1. All levels are related to EBU colour bar.
2. Values in decimal at 100 % luminance and 75 % chrominance amplitude.

Fig.10 Input and output signal ranges.

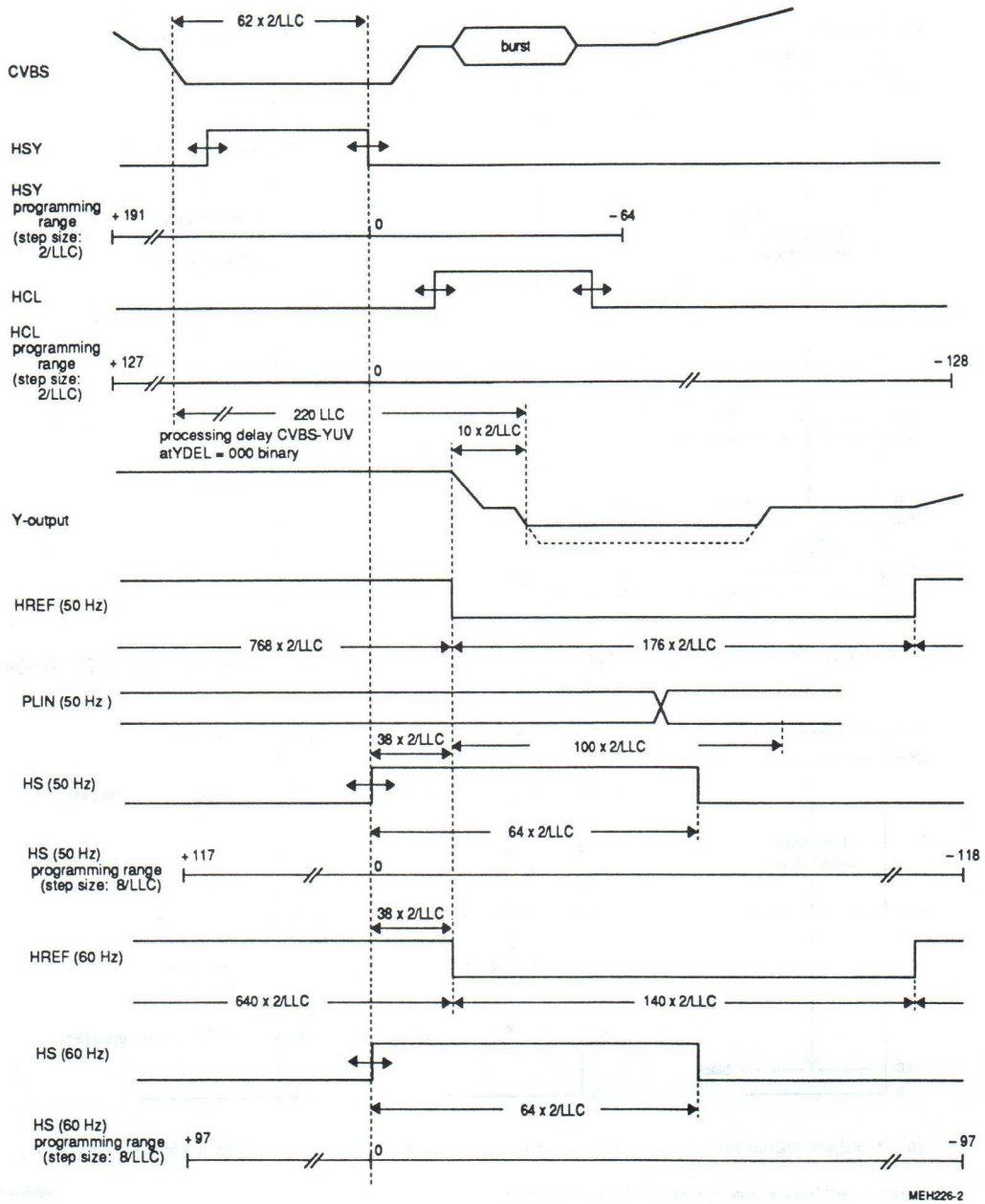


Fig.12 Horizontal sync at HRMV = 0 and HRFS = 0 for 50/60 Hz (signals HSY, HCL, HREF and PLIN).

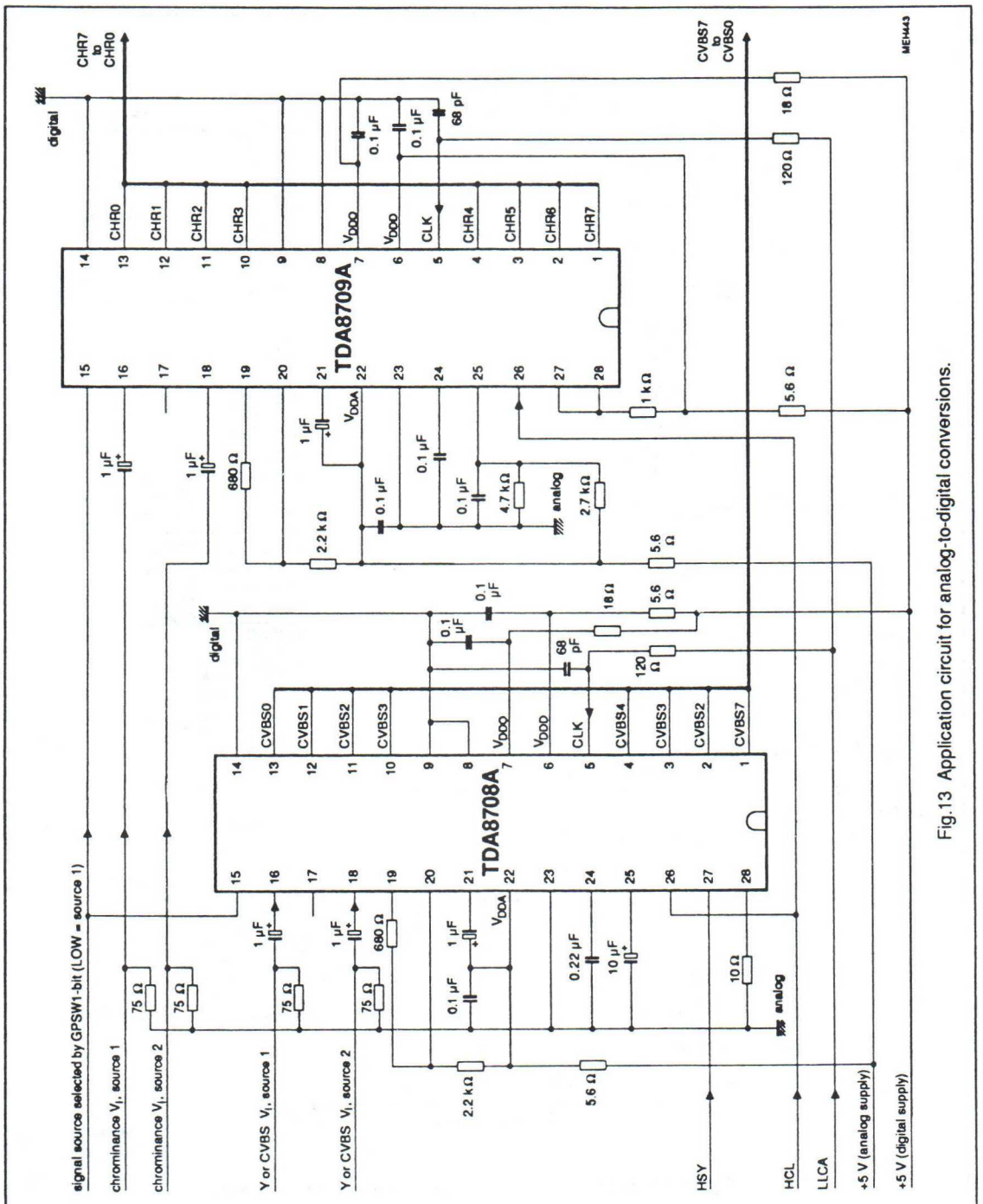


Fig.13 Application circuit for analog-to-digital conversions.

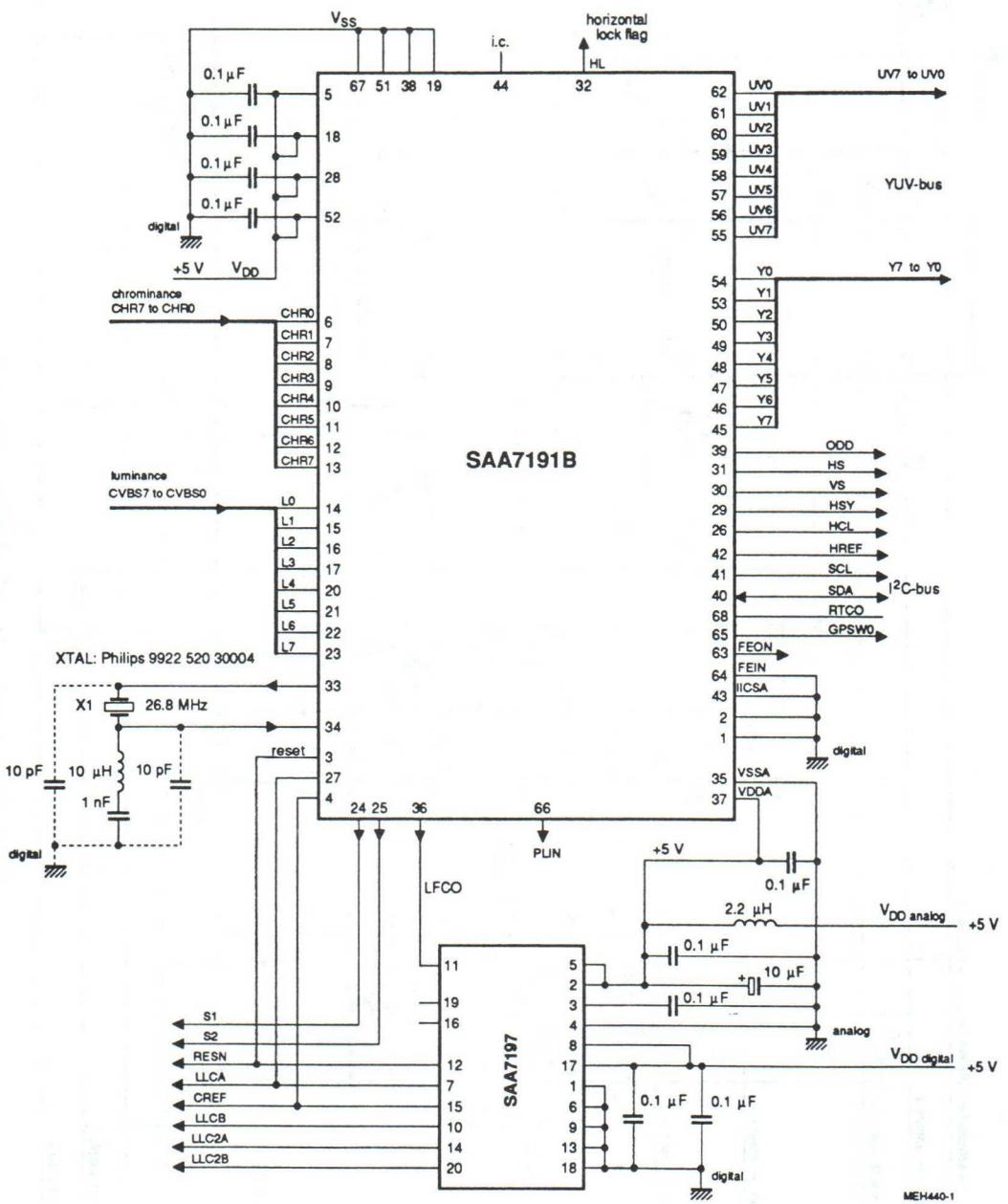


Fig.14 Application circuit for digital multistandard colour decoder.

10. I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = **1000 101X** (IICSA = LOW) **or 1000 111X** (IICSA = HIGH)
A = acknowledge, generated by the slave
SUBADDRESS* = subaddress byte (Table 5)
DATA = data byte (Table 5)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 5 I²C-bus; DATA for status byte (X = 1 in address byte; 8Bh at IICSA = LOW or 8Fh at IICSA = HIGH).

FUNCTION		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
status byte		STTC	HLCK	FIDT	X	X	X	X	CODE

Function of the bits:

STTC — Horizontal time constant information for future application with logical combfilter only:
0 = TV time constant (slow);
1 = VCR time constant (fast)

HLCK — Horizontal PLL information: 0 = HPLL locked; 1 = HPLL unlocked

FIDT — Field information: 0 = 50 Hz system detected; 1 = 60 Hz system detected

CODE — Colour information: 0 = no colour detected; 1 = colour detected

Table 6 I²C-bus; subaddress and data bytes for writing (X = 0 in address byte; 8Ah at IICSA = LOW or 8Eh at IICSA = HIGH).

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Increment delay	00	IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0
H sync begin, 50 Hz	01	HSYB7	HSYB6	HSYB5	HSYB4	HSYB3	HSYB2	HSYB1	HSYB0
H sync stop, 50 Hz	02	HSYS7	HSYS6	HSYS5	HSYS4	HSYS3	HSYS2	HSYS1	HSYS0
H clamp begin, 50 Hz	03	HCLB7	HCLB6	HCLB5	HCLB4	HCLB3	HCLB2	HCLB1	HCLB0
H clamp stop, 50 Hz	04	HCLS7	HCLS6	HCLS5	HCLS4	HCLS3	HCLS2	HCLS1	HCLS0
H sync after PHI1, 50 Hz	05	HPHI7	HPHI6	HPHI5	HPHI4	HPHI3	HPHI2	HPHI1	HPHI0
Luminance control	06	BYPS	PREF	BPSS1	BPSS0	CORI1	CORI0	APER1	APER0
Hue control	07	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
Colour killer threshold QAM	08	CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0	0	0	0
Colour-killer threshold SECAM	09	CKTS4	CKTS3	CKTS2	CKTS1	CKTS0	0	0	0
PAL switch sensitivity	0A	PLSE7	PLSE6	PLSE5	PLSE4	PLSE3	PLSE2	PLSE1	PLSE0
SECAM switch sensitivity	0B	SESE7	SESE6	SESE5	SESE4	SESE3	SESE2	SESE1	SESE0
Chroma gain control settings	0C	COLO	LFIS1	LFIS0	0	0	0	0	0
Standard/mode control	0D	VTRC	0	0	0	NFEN	HRMV	GPSW0	SECS
I/O and clock control	0E	HPLL	OEDC	OEHS	OEVS	OEDY	CHRS	GPSW2	GPSW1
Control #1	0F	AUFD	FSEL	SXCR	SCEN	OFTS	YDEL2	YDEL1	YDEL0
Control #2	10	0	0	0	0	0	HRFS	VNOI1	VNOI0
Chroma gain reference	11	CHCV7	CHCV6	CHCV5	CHCV4	CHCV3	CHCV2	CHCV1	CHCV0
Not used, is acknowledged	12	0	0	0	0	0	0	0	0
Not used, is acknowledged	13	0	0	0	0	0	0	0	0
H sync begin, 60 Hz	14	HS6B7	HS6B6	HS6B5	HS6B4	HS6B3	HS6B2	HS6B1	HS6B0
H sync stop, 60 Hz	15	HS6S7	HS6S6	HS6S5	HS6S4	HS6S3	HS6S2	HS6S1	HS6S0
H clamp begin, 60 Hz	16	HC6B7	HC6B6	HC6B5	HC6B4	HC6B3	HC6B2	HC6B1	HC6B0
H clamp stop, 60 Hz	17	HC6S7	HC6S6	HC6S5	HC6S4	HC6S3	HC6S2	HC6S1	HC6S0
H sync after PHI1, 60 Hz	18	HP6I7	HP6I6	HP6I5	HP6I4	HP6I3	HP6I2	HP6I1	HP6I0

Note to Table 6

- Default values of register contents to obtain a picture see Table 6.
- All unused control bits must be programmed with "0" (zero) as indicated in Table 5.

Function of the bits of Table 5

IDEL7 to IDEL0 "00"	Increment delay time (dependent on application), step size = 4 / LLC. The delay time is selectable from –4 / LLC (–1 decimal multiplier) to –1024 / LLC (–256 decimal multiplier) equals data FF to 00 (hex). Different processing times in the chrominance channel and the clock generation could result in phase errors in the chrominance processing by transients in clock frequency. An adjustable delay (IDEL) is necessary if the processing time in the clock generation is unknown.
HSYB7 to HSYB0 "01"	Horizontal sync begin for 50 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two's complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.
HSYS7 to HSYS0 "02"	Horizontal sync stop for 50 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two's complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.
HCLB7 to HCLB0 "03"	Horizontal clamp start for 50 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).
HCLS7 to HCLS0 "04"	Horizontal clamp stop for 50 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).
HPHI7 to HPHI0 "05"	Horizontal sync after PHI1 for 50 Hz, step size = 8 / LLC. The delay time is selectable from –936 /LLC (+117 decimal multiplier) to +944 /LLC (–118 decimal multiplier) equals data 75 to 8A (hex).
BYPS "06"	input mode select bit: 0 = CVBS mode (chrominance trap active) 1 = S-Video mode (chrominance trap bypassed)
PREF	use of pre-filter: 0 = pre-filter off; 1 = pre-filter on; PREF may be used if chrominance trap is active.
BPSS1 to BPSS0	Aperture bandpass to select different characteristics with maximums (0.2 to 0.3 x LLC / 2): BPSS1 BPSS0 | characteristics 0 0 |) 0 1 |) Figures 16 to 25 1 0 |) 1 1 |)
CORI1 to CORI0 "06"	Coring range for high frequency components according to 8-bit luminance, Fig.15. CORI1 CORI0 | coring 0 0 | coring off 0 1 | ±1 LSB 1 0 | ±2 LSB 1 1 | ±3 LSB

<table>
<tr><td>APER1 to APER0
"06"</td><td>Aperture bandpass filter weights high frequency components of luminance signal:
<table>
<tr><th>APER1</th><th>APER0</th><th>factor</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0.25</td></tr>
<tr><td>1</td><td>0</td><td>0.5</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table>
Figures 16 to 25</td></tr>
<tr><td>HUE7 to HUE0
"07"</td><td>Hue control from +178.6° to −180.0°, equals data bytes 7F to 80 (hex); 0° equals 00.</td></tr>
<tr><td>CKTQ4 to CKTQ0
"08"</td><td>Colour-killer threshold QAM from approximately −30 dB to −18 dB, equals data bytes F8 to 07 (hex)</td></tr>
<tr><td>CKTS4 to CKTS0
"09"</td><td>Colour-killer threshold SECAM from approximately −30 dB to −18 dB, equals data bytes. F8 to 07 (hex)</td></tr>
<tr><td>PLSE7 to PLSE0
"0A"</td><td>PAL switch sensitivity from LOW-to-HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.</td></tr>
<tr><td>SESE7 to SESE0
"0B"</td><td>SECAM switch sensitivity from LOW-to-HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.</td></tr>
<tr><td>COLO
"0C"</td><td>Colour on bit: 0 = automatic colour-killer enabled; 1 = forced colour on.</td></tr>
<tr><td>LFIS1 to LFIS0
"0C"</td><td>Chrominance gain control (AGC filter):
<table>
<tr><th>LFIS1</th><th>LFIS0</th><th></th><th>loop filter time constant</th></tr>
<tr><td>0</td><td>0</td><td>=</td><td>slow</td></tr>
<tr><td>0</td><td>1</td><td>=</td><td>medium</td></tr>
<tr><td>1</td><td>0</td><td>=</td><td>fast</td></tr>
<tr><td>1</td><td>1</td><td>=</td><td>actual gain, stored for test purposes only</td></tr>
</table></td></tr>
<tr><td>VTRC
"0D"</td><td>VTR/TV mode bit : 0 = TV mode (slow time constant); 1 = VTR mode (fast time constant)</td></tr>
<tr><td>NFEN</td><td>SAA7191B-specified functions enable (RTCO, ODD and GPSW0 outputs)
0 = outputs set to high-impedance (circuit equals SAA7191); 1 = outputs active</td></tr>
<tr><td>HRMV</td><td>HREF generation: 0 = like SAA7191; 1 = HREF is 8 x LLC2 clocks earlier</td></tr>
<tr><td>GPSWO</td><td>General purpose switch 0: 0 = output pin 65 LOW; 1 = output pin 65 HIGH</td></tr>
<tr><td>SECS</td><td>SECAM mode bit : 0 = other standards; 1 = SECAM</td></tr>
<tr><td>HPLL
"0E"</td><td>Horizontal clock PLL: 0 = PLL closed;
1 = PLL circuit open and horizontal frequency fixed.</td></tr>
<tr><td>OEDC</td><td>Colour-difference output enable: 0 = data outputs UV7 to UV0 can be set to high-impedance via FEIN
1 = data outputs UV7 to UV0 active.</td></tr>
<tr><td>OEHS</td><td>H-sync output enable (pins 31 and 42): 0 = HS and HREF outputs high-impedance
1 = HS and HREF outputs active.</td></tr>
<tr><td>OEVS</td><td>V-sync output enable (pin 30): 0 = VS output high-impedance
1 = VS output active.</td></tr>
</table>

OEDY	Luminance output enable: 0 = data outputs Y7 to Y0 can be set to high-impedance via FEIN 1 = data outputs Y7 to Y0 active.
CHRS	S-VHS bit (chrominance from CVBS or from chrominance input): 0 = controlled by BYPS-bit (subaddress 06) 1 = chrominance from chrominance input (CHR7 to CHR0)
GPSW2 to GPSW1 to "0E"	General purpose switches : GPSW2 GPSW1 | set port output pins 24 (GPSW2) and 25 (GPSW1) 0 0 0 1 1 0 1 1 | use is dependent on application
AUFD "0F"	Automatic field detection: 0 = field selection by FSEL-bit; 1 = automatic field detection.
FSEL	Field select (AUFD-bit = 0): 0 = 50 Hz (625 lines); 1 = 60 Hz (525 lines)
SXCR	SECAM cross-colour reduction: 0 = reduction off; 1 = reduction on.
SCEN	Sync and clamping pulse enable: 0 = HCL and HSY outputs HIGH (pins 26 and 29); 1 = HCL and HSY outputs active
OFTS	Select output format: 0 = 4 : 1 : 1 format; 1 = 4 : 2 : 2 format.
YDEL2 to YDEL0	Luminance delay compensation: YDEL2 YDEL1 YDEL0 | figure 0 0 0 | 0 x 2 / LLC 0 0 1 | +1 x 2 / LLC 0 1 0 | +2 x 2 / LLC 0 1 1 | +3 x 2 / LLC 1 0 0 | –4 x 2 / LLC 1 0 1 | –3 x 2 / LLC 1 1 0 | –2 x 2 / LLC 1 1 1 | –1 x 2 / LLC step size = 2 / LLC = 67.8 ns for 50 Hz 81.5 ns for 60 Hz
HRFS "10"	Select HREF position: 0 = normal, HREF is matched to YUV output port; 1 = HREF is matched to CVBS intput port.
VNOI1 to VNOI0	Vertical noise reduction VNOI1 VNOI0 | mode 0 0 | normal 0 1 | searching window 1 0 | auto-deflection 1 1 | vertical noise reduction bypassed

<table>
<tr><td>CHCV7 to CHCV0
UV "11"</td><td>Chrominance gain control (nominal values) for QAM-modulated input signals, effects output amplitude (SECAM with fixed gain):
<table><tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>gain</th></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>maximum gain</td></tr><tr><td></td><td>:</td><td></td><td></td><td></td><td>:</td><td></td><td></td><td>to)</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>CCIR level for PAL)) default programmed</td></tr><tr><td></td><td>:</td><td></td><td></td><td></td><td>:</td><td></td><td></td><td>to) values dependend</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>CCIR level for NTSC)) on application</td></tr><tr><td></td><td>:</td><td></td><td></td><td></td><td>:</td><td></td><td></td><td>to)</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>minimum gain</td></tr></table></td></tr>
<tr><td>HS6B7 to HS6B0
"14"</td><td>Horizontal sync begin for 60 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two´s complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.</td></tr>
<tr><td>HS6S7 to HS6S0
"15"</td><td>Horizontal sync stop for 60 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two´s complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.</td></tr>
<tr><td>HC6B7 to HC6B0
"16"</td><td>Horizontal clamp begin for 60 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).</td></tr>
<tr><td>HC6S7 to HC6S0
"17"</td><td>Horizontal clamp stop for 60 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).</td></tr>
<tr><td>HP6I7 to HP6I0
"18"</td><td>Horizontal sync after PHI1 for 60 Hz, step size = 8 / LLC. The delay time is selectable from –776 /LLC (+97 decimal multiplier) to +776 /LLC (–97 decimal multiplier) equals data 61 to 9F (hex).</td></tr>
</table>

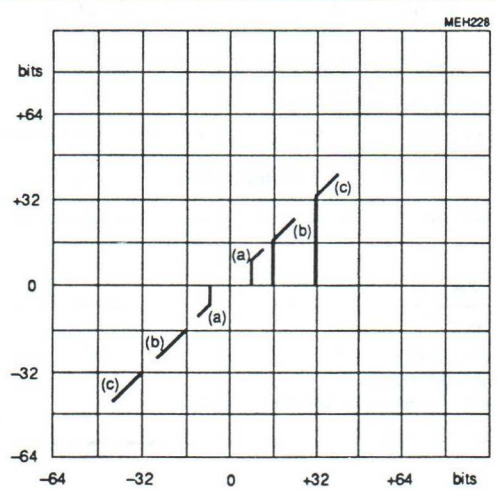


Fig.15 Coring function adjustment by subaddress 06 to affect the bandfilter output signal. The thresholds are related to the 13-bit word width in the luminance processing part and influence the 1LSB to 3LSB (Y0 to Y2) with respect to the 8-bit luminance output

(a) CORI1 = 0; CORI0 = 1

(b) CORI1 = 1; CORI0 = 0

(a) CORI1 = 1; CORI0 = 1

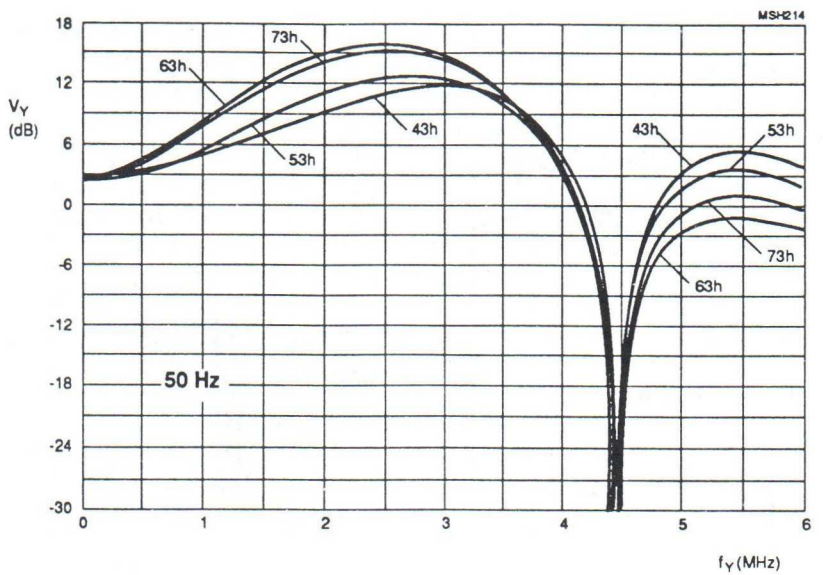


Fig.16 Luminance control in 50 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; maximum aperture bandpass filter characteristic.

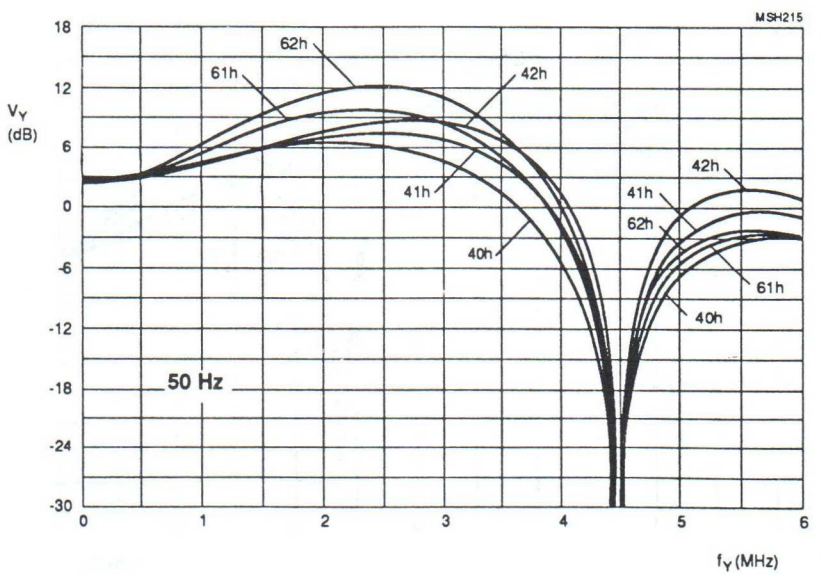


Fig.17 Luminance control in 50 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; other aperture bandpass filter characteristics.

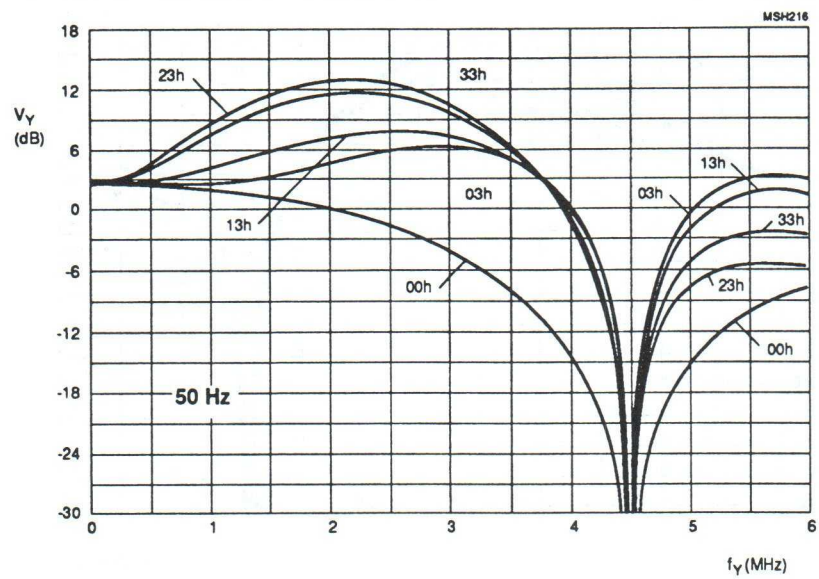


Fig.18 Luminance control in 50 Hz / CVBS mode controllable by subaddress byte 06; pre-filter off and coring off; maximum aperture bandpass filter characteristic.

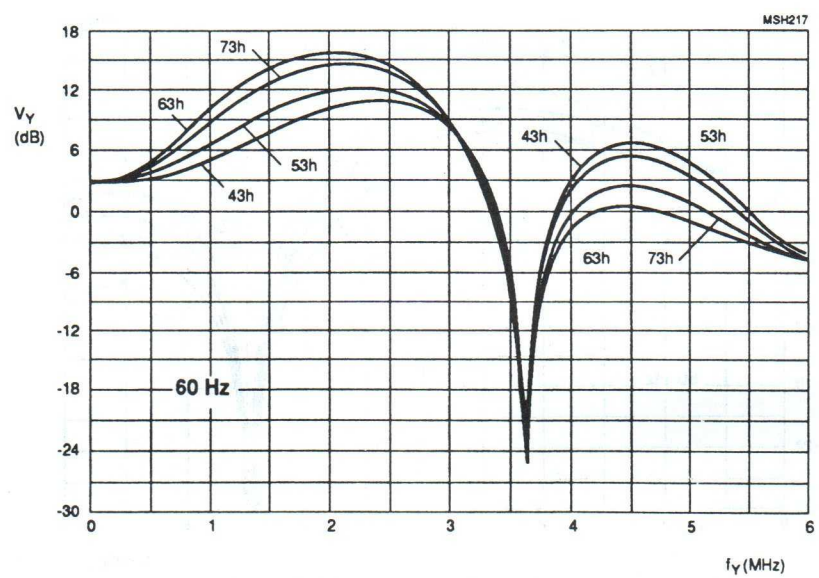


Fig.19 Luminance control in 60 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; maximum aperture bandpass filter characteristic.

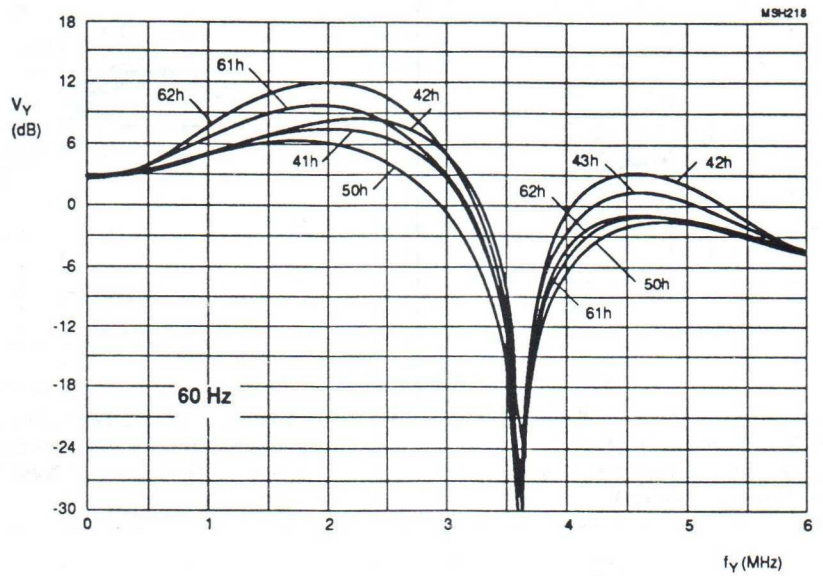


Fig.20 Luminance control in 60 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; other aperture bandpass filter characteristics.

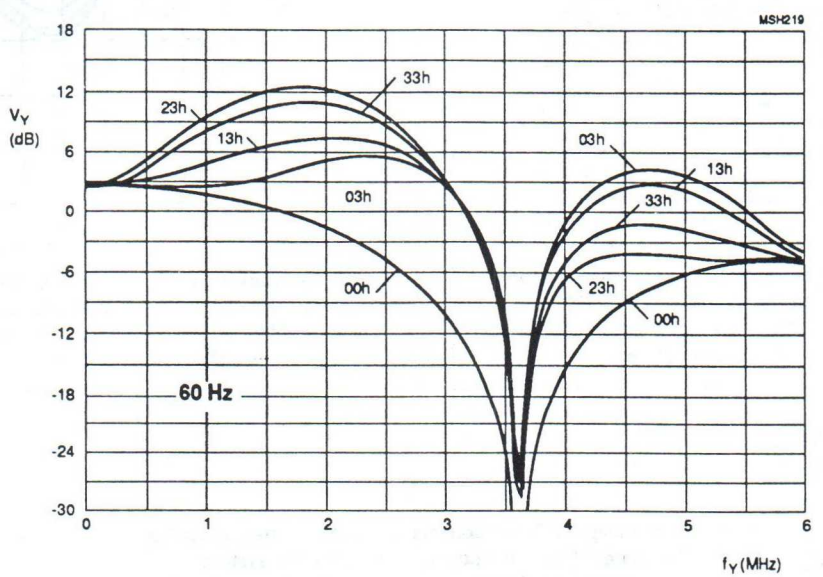


Fig.21 Luminance control in 60 Hz / CVBS mode controllable by subaddress byte 06; pre-filter off and coring off; maximum and minimum aperture bandpass filter characteristics.

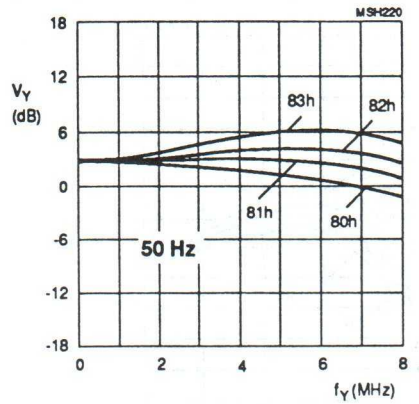


Fig.22 Luminance control in 50 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter off and coring off; different aperture bandpass filter characteristics.

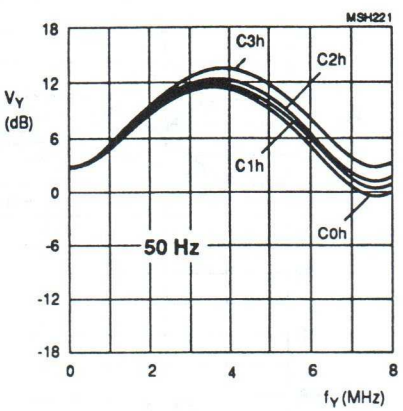


Fig.23 Luminance control in 50 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter on and coring off; different aperture bandpass filter characteristics.

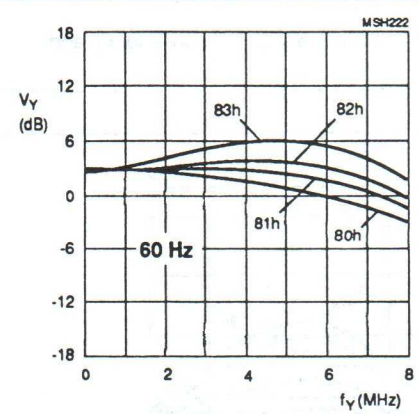


Fig.24 Luminance control in 60 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter off and coring off; different aperture bandpass ffilter characteristics.

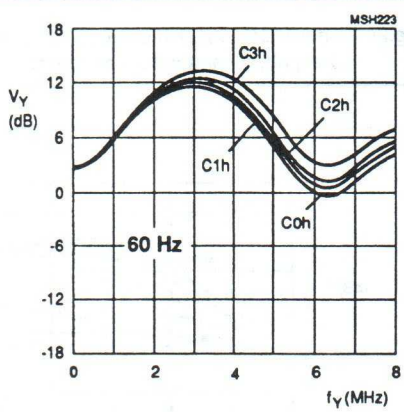
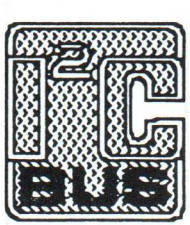


Fig.25 Luminance control in 60 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter on and coring off; different aperture bandpass filter characteristics.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

PROGRAMMING EXAMPLE

Coefficients to set operation for application circuits Figures 13 and 14. (All numbers of the Table 6 are hex values). Slave address byte is 8A at pin 43 = 0 V (or 8E at pin 43 = +5 V).

Table 7 Recommended default values

SUBADDRESS	BIT NAME	FUNCTION	VALUE (HEX)
00	IDEL(7-0)	increment delay	50
01	HSYB(7-0)	H sync beginning for 50 Hz	30
02	HSYS(7-0)	H sync stop for 50 Hz	00
03	HCLB(7-0)	H clamping beginning for 50 Hz	E8
04	HCLS(7-0)	H clamping stop for 50 Hz	B6
05	HPHI(7-0)	H sync position for 50 Hz	F4
06	BYPS, PREF, BPSS(1-0) CORI(1-0), APER(1-0)	luminance bandwidth control:	01(1)
07	HUEC(7-0)	hue control (0 degree)	00
08	CKTQ(4-0)	colour-killer threshold QUAM	F8
09	CKTS(4-0)	colour-killer threshold SECAM	F8
0A	PLSE(7-0)	PAL switch sensitivity	90
0B	SESE(7-0)	SECAM switch sensitivity	90
0C	COLO, LFIS(1-0)	chroma gain control settings	00
0D	VTRC, NFEN,HRMV, GPSW0 and SECS	standard/mode control	00(2)(4), 01(3)(4)
0E	HPLL, OEDC, OEHS, OEVS OEDY, CHRS, GPSW(2-1)	I/O and clock control	79, 7E(5)
0F	AUFD, FSEL, SXCR, SCEN, OFTS, YDEL(2-0)	miscellaneous control #1	91(6), 99(7)
10	HRFS, VNOI(1-0)	miscellaneous control #2	00
11	CHCV(7-0)	chrominance gain nominal value	2C(8), 59(9)
12	-	set to zero	00
13	-	set to zero	00
14	HS6B(7-0)	H sync beginning for 60 Hz	34
15	HS6S(7-0)	H sync stop for 60 Hz	0A
16	HC6B(7-0)	H clamping beginning for 60 Hz	F4
17	HC6S(7-0)	H clamping stop for 60 Hz	CE
18	HP6I(7-0)	H sync position for 60 Hz	F4

Notes to Table 7

(1) dependent on application (Figures 16 to 25)
(2) for QUAM standards
(3) for SECAM
(4) HPLL is in TV mode; value for VCR mode is 80 (81 for SECAM VCR mode)
(5) for Y/C mode
(6) 4:1:1 format
(7) 4:2:2 format
(8) nominal value for UV CCIR level with NTSC source
(9) nominal value for UV CCIR level with PAL source

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	August 1990

SAA7192
Digital colour space converter

INTRODUCTION

The Digital Color Space Converter (DCSC) is a matrix which is used to transform 8-bit digital input signals, i.e. Y (luminance), Cr (colour, R-Y) and Cb (colour, B-Y), into an RGB 8-bit format in accordance with the CCIR-601 recommendations.
The system accepts the formats of the DMSD2 family of decoders at the input. The maximum data rate is 16 MHz. The propagation delay of the device is constant. A matched pipeline delay line is available to enable the HREF signal to be synchronized with the video data at the output.

SYSTEM FUNCTIONS

The DCSC consists of the following functional blocks, as illustrated in Fig.1:

- Input Formatter with;
  multiplexer
  Y-delay line
  Cr and Cb Interpolating filters
- Conversion matrix
- Video look up tables
- Pipeline delay line
- I²C-bus interface

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7192	68	PLCC	plastic	SOT188AA,AGA

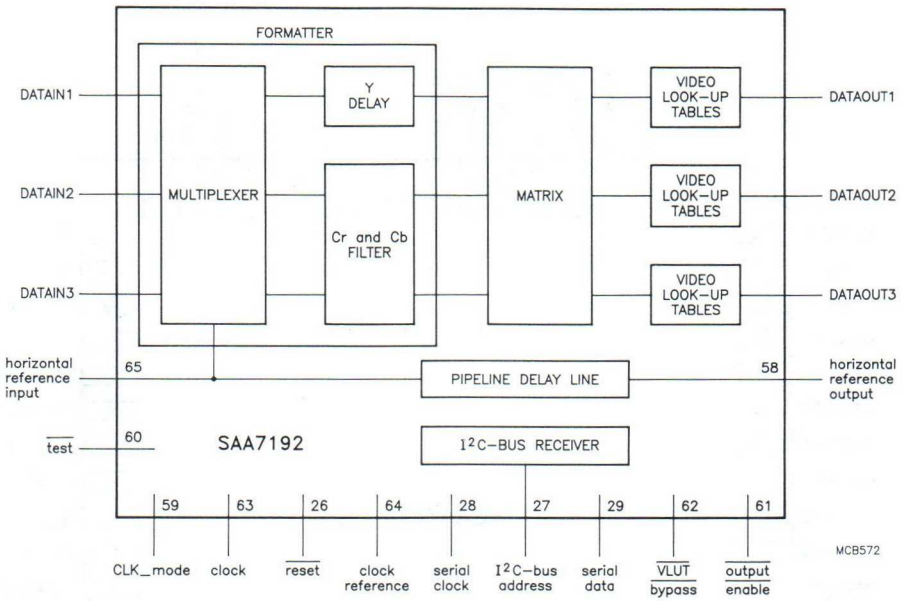


Fig.1 Block diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

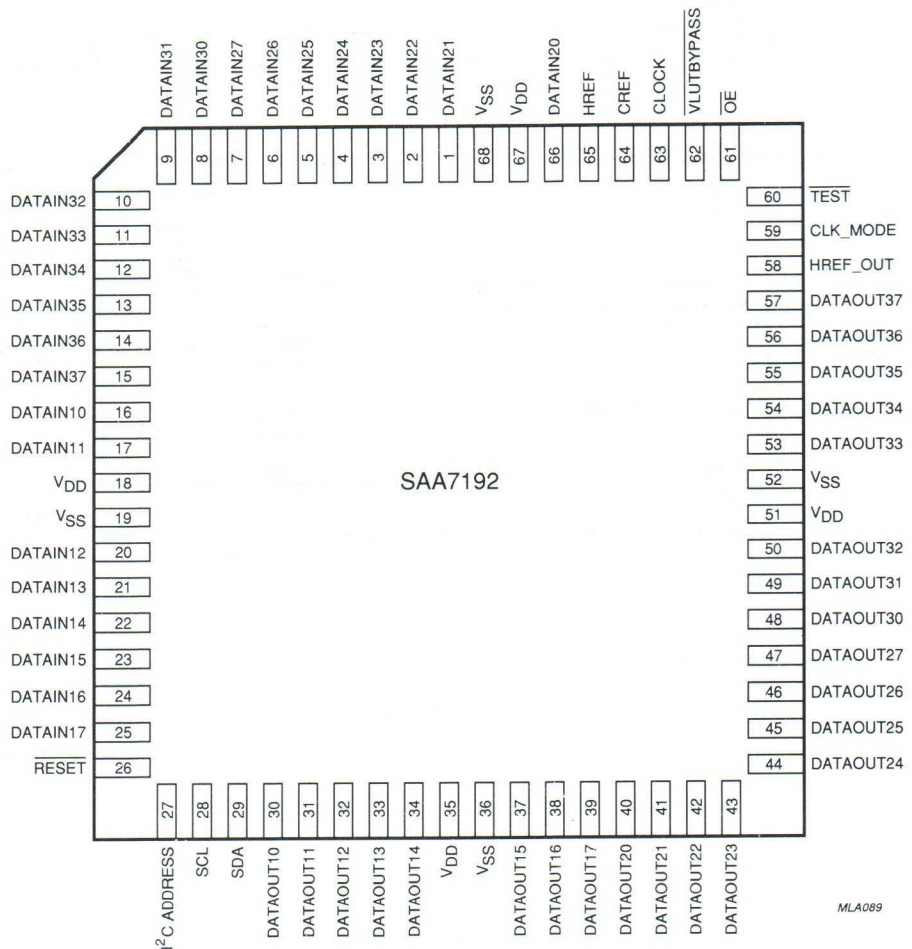


Fig.2 Pinning diagram.

Functional modes

Table 1 Functional Modes.

MODE	FUNCTION
1	4:1:1 filter, no matrix, no VLUT; DATAOUT = upsampled DATAIN
2	4:1:1 filter, matrix, no VLUT; DATAOUT = RGB
3	4:1:1 filter, no matrix, VLUT; DATAOUT = upsampled DATAIN multiplied by the factor loaded into the VLUT
4	4:1:1 filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT
5	4:2:2 filter, no matrix, no VLUT; DATAOUT = upsampled DATAIN
6	4:2:2 filter, matrix, no VLUT; DATAOUT = RGB
7	4:2:2 filter, no matrix, VLUT; DATAOUT = upsampled DATAIN multiplied by the factor loaded into the VLUT
8	4:2:2 filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT
9	no filter, no matrix, no VLUT; DATAOUT = DATAIN "Process Bypass"
10	no filter, matrix, no VLUT; DATAOUT = RGB
11	no filter, no matrix, VLUT; DATAOUT = DATAIN multiplied by the factor loaded into the VLUT.
12	no filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT

Figures 3 to 9b illustrate the various functional modes.

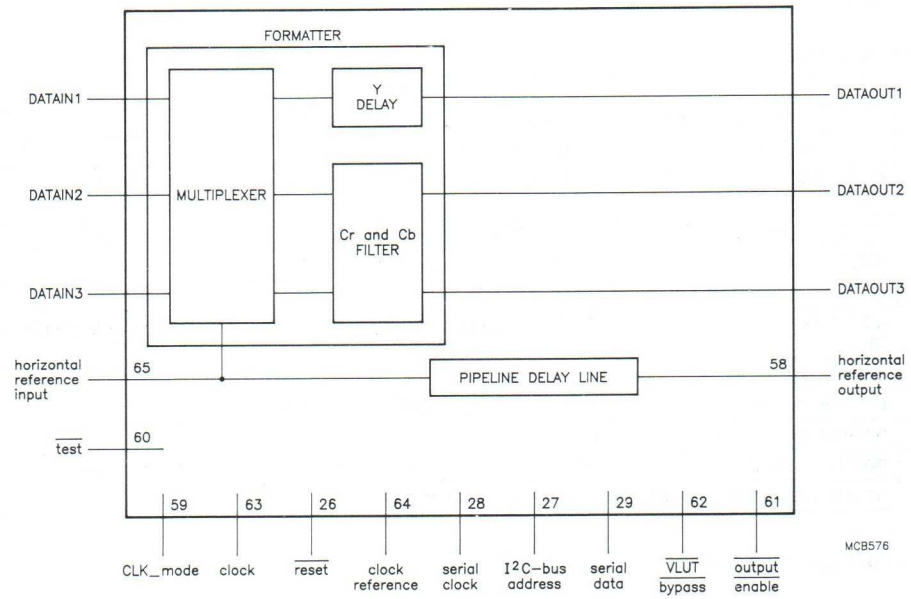


Fig.3 Functional mode 1 and 5.

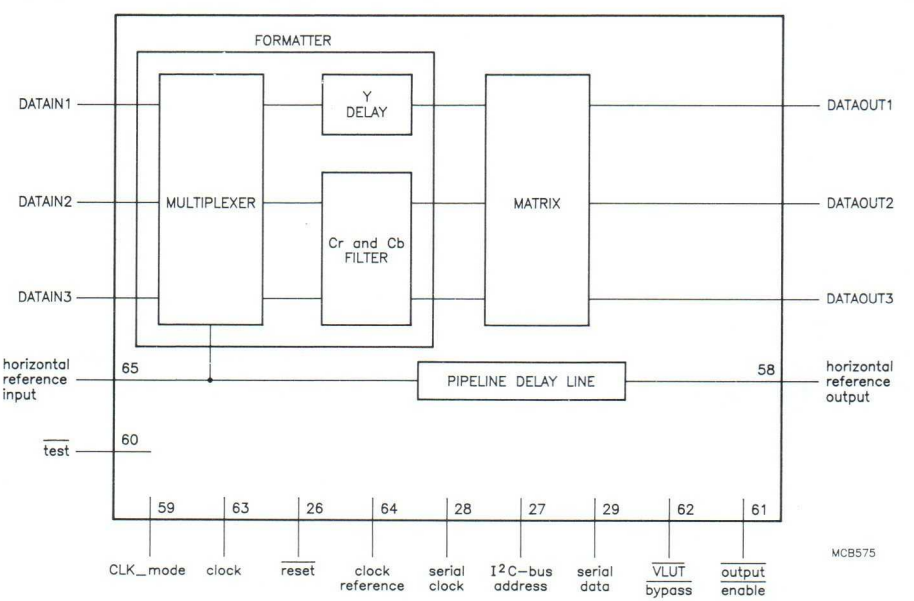


Fig.4 Functional mode 2 and 6.

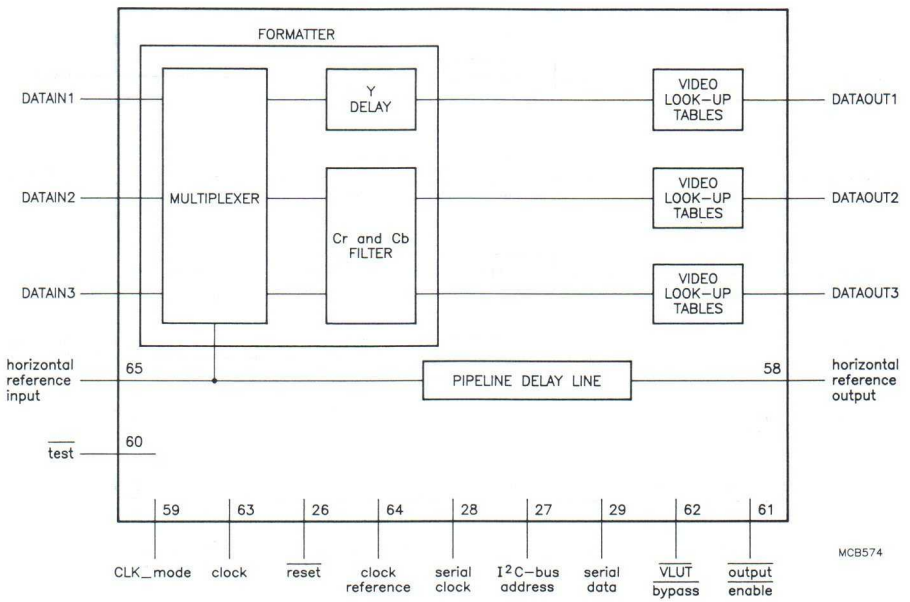


Fig.5 Functional mode 3 and 7.

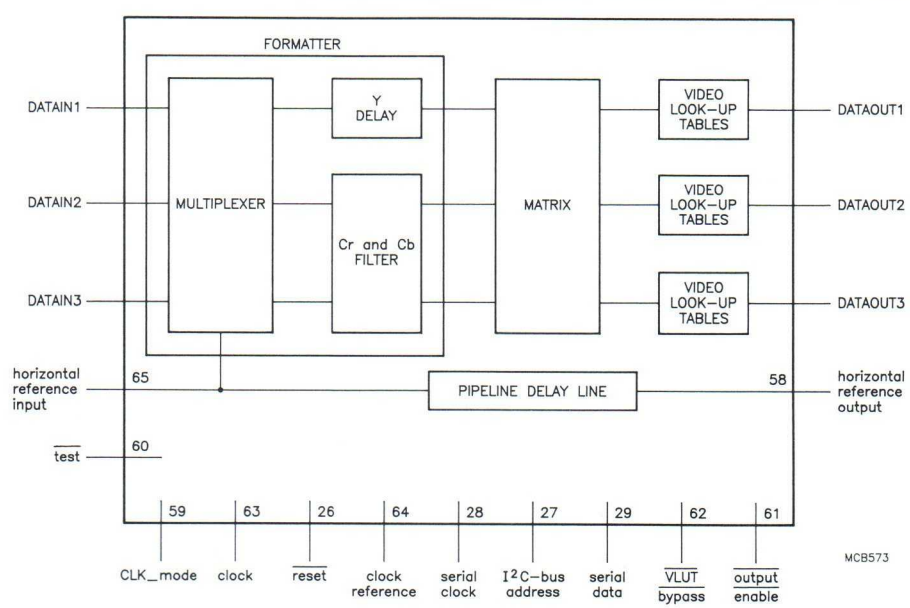


Fig.6 Functional mode 4 and 8.

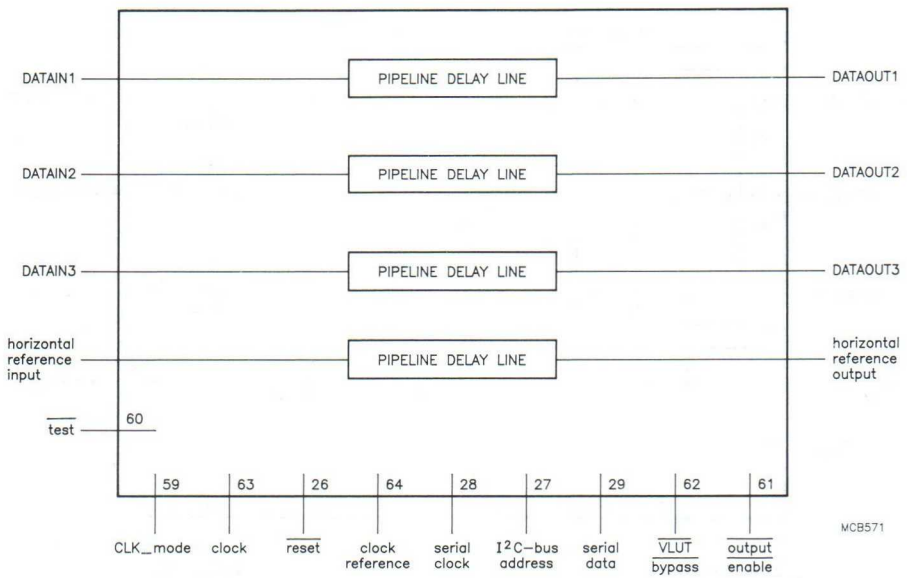


Fig.7 Functional mode 9.

Fig.8 Functional mode 10.

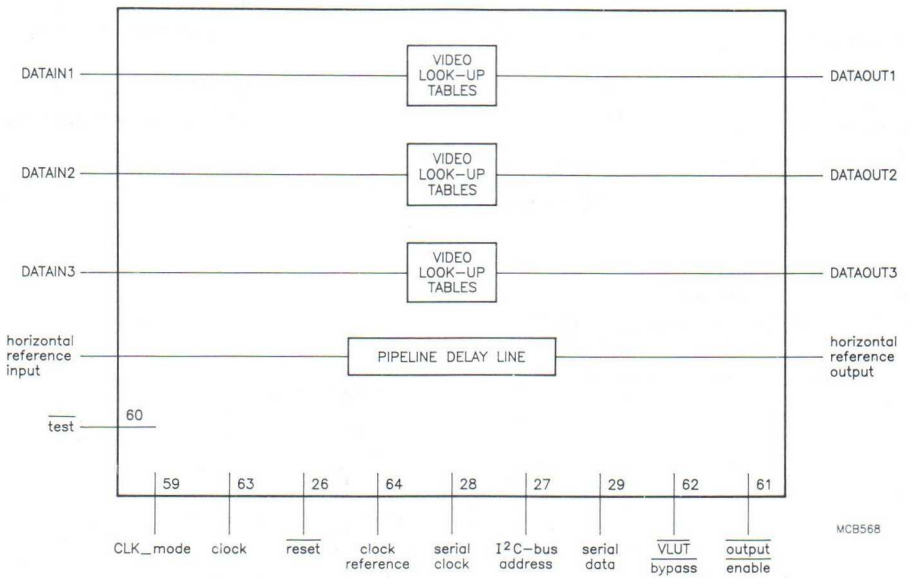


Fig.9a Functional mode 11.

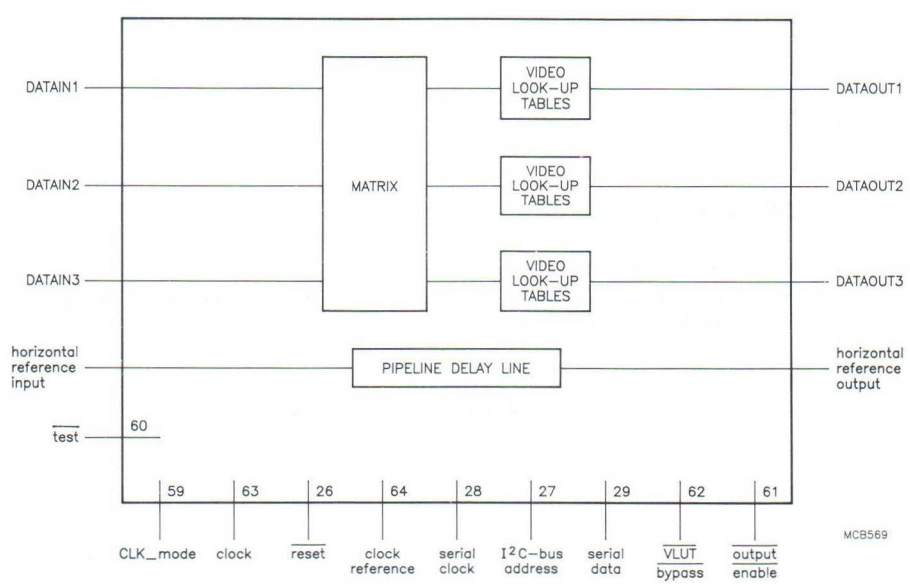


Fig.9b Functional mode 12.

Control facilities

After power-up all internal control signals of the device are at undefined values. The I²C-bus receiver must, therefore, be reset by using the external RESET signal. The control signals are then set to:

IICOE = 1
output in 3-state

FMTCNTRL = 4
format 4:4:4

$\overline{\text{MATBYPASS}}$ = 0
matrix bypassed

$\overline{\text{VLUTLOAD}}$ = 1
VLUT at READ operation

$\overline{\text{INRESET}}$ = 0
input data set to fixed values

Table 2 Input formats and functional modes

FMTCNTRL	$\overline{\text{MATBYPASS}}$	$\overline{\text{VLUTBYPASS}}$	FUNCTIONS
0	0	0	mode 1, input format 1 (DMSD2 format)
0	1	0	mode 2, input format 1 (DMSD2 format)
1	0	0	mode 1, input format 2
1	1	0	mode 2, input format 2
2	0	0	mode 5, input format 3 (DMSD2 format)
2	1	0	mode 6, input format 3 (DMSD2 format)
3	0	0	mode 5, input format 4 (parallel IN)
3	1	0	mode 6, input format 4 (parallel IN)
4	0	0	mode 9, input format 5 (parallel IN)
4	1	0	mode 10, input format 5 (parallel IN)
x	x	1	each of the above described modes will be multiplied by the factor loaded into the VLUT.

Note

The modes are given in Table 1.

The other control signals are:

$\overline{\text{VLUTLOAD}}$ = logic 1: VLOAD inactive
= logic 0: VLOAD datalines active to load VLUT

$\overline{\text{INRESET}}$ = logic 1: input latches at the formatter are always transparent
= logic 0: at the end of each active video line the input latches have to be set to fixed values (Y to 16; Cr and Cb to 128; if HREF = 0)

CLK_MODE = logic 1: DMSD mode (LL27 clock of DMSD feeds the DCSC)
= logic 0: DCSC is fed by a maximum 16 MHz clock without CREF signal.

Table 3 Output enable control

IICOE	$\overline{OE}$	CONTROL LINE TO DRIVER STAGES
0	X	1 = DATAOUT in high impedance mode
1	1	1 = DATAOUT in high impedance mode
1	0	0 = DATAOUT working

Note

IICOE: output enable control of I^2C-bus (enables $\overline{OE}$)
$\overline{OE}$: output enable (fast switch)

SYSTEM I/O INTERFACES

Input signals

VIDEO DATA (DATAIN)

Table 4 Format 1 (4:1:1, semi-parallel, DMSD2 format)

DATAIN1 - Y	luminance signal, 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black, quantization level 16 100 IRE; white, quantization level 235
DATAIN3 - U, V	multiplexed colour difference signals 4-bit; corresponds to UV7 to UV4 of DMSD2
Sampling frequency	1/4 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN2	not used

Table 5 Timing of Format 1; pin (DATAIN) and bit (U,V) numbers are indicated except clock

Y; 7 to 0	Y	Y	Y	Y	Y	Y	Y
DATAIN2, 7	U7	U5	U3	U1	U7	U5	U3
DATAIN2, 6	U6	U4	U2	U0	U6	U4	U2
DATAIN2, 5	V7	V5	V3	V1	V7	V5	V3
DATAIN2, 4	V6	V4	V2	V0	V6	V4	V2
Clock A	1	2	3	4	5	6	7

Table 6 Format 2 (4:1:1, semi-parallel, customized format)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cr, Cb	multiplexed colour difference signals,8-bit
Sampling frequency	1/4 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN2	not used

Table 7 Timing of Format 2; the indexes show the clock (sample) number

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cr, Cb	Cb0		Cr0		Cb4		Cr4
Clock A	0	1	2	3	4	5	6

Table 8 Format 3 (4:2:2, semi-parallel, DMSD2 format)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cr, Cb	multiplexed colour difference signals corresponds to UV7 to UV0 of DMSD2
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN2	not used

Table 9 Timing of Format 3

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cr, Cb	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4	Cb6
Clock A	0	1	2	3	4	5	6

Table 10 Format 4 (4:2:2, Y-Cr-Cb, parallel)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cb	colour difference signal B-Y, 8-bit
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128b
DATAIN2 - Cr	colour difference signal R-Y, 8-bit
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128

Table 11 Timing of Format 4

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cb	Cb0		Cb2		Cb4		Cb6
Cr	Cr0		Cr2		Cr4		Cr6
Clock A	0	1	2	3	4	5	6

Table 12 Format 5 (4:4:4, Y-Cr-Cb, parallel)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	maximum 16.0 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN2 - Cr	colour difference signal R-Y, 8-bit
Sampling frequency	maximum 16.0 MHz
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless, binary 128
DATAIN3 - Cb	colour difference signal B-Y, 8-bit
Sampling frequency	maximum 16.0 MHz
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128

Table 13 Timing of Format 5

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cb	Cb0	Cb1	Cb2	Cb3	Cb4	Cb5	Cb6
Cr	Cr0	Cr1	Cr2	Cr3	Cr4	Cr5	Cr6
Clock A	0	1	2	3	4	5	6

CONTROL DATA

Clock

The line locked clock LL27 (denoted as CLOCK at the DCSC input) is twice the data rate of that specified for the DMSD2 family of decoders. The data rate is denoted as CLOCK_A in Tables 5, 7, 9, 11 and 13.

The data rate on the input (DATAIN) is as follows;

12.2727 MHz; 60 Hz signals (from SAA7191)
13.5 MHz; CCIR signals (from SAA7151)
14.75 MHz; 50 Hz signals (from SAA7191)
16.0 MHz; maximum frequency

Timing reference (Fig.10)

The timing reference signal from the SAA7151/7191 is used to synchronize the multiplexer and refers to the LL27 clock. Each alternative positive slope, marked by a CREF signal, is used to obtain data. The horizontal reference signal, HREF, indicates the active part of a line and also synchronizes the multiplexer.

CREF The clock reference signal is a clock qualifier signal distributed by the clock generator of the DMSD system. The frequency is identical to the sample rates denoted in the input and the output formats (see Video data and Operating conditions).

HREF Horizontal reference signal is the line reference signal of the YUV-bus. A positive slope marks the beginning of the active part of a line. The length of the active part corresponds to the number of samples (see Operating conditions).

Table 14 Real-time control signals

$\overline{OE}$	= 1 : = 0 :	switches the output to high-z mode output enable, output stage in use
$\overline{VLUTBYPASS}$	= 1 : = 0 :	VLUT's in use VLUT's bypassed
$\overline{RESET}$	= 1 : = 0 :	device in use general reset
CLK_MODE	= 1 : = 0 :	DMSD mode (LL27 clock of DMSD feeds the DCSC) DCSC is feed by a clock signal with a maximum data rate of 16 MHz (without CREF signal).

Table 15 I²C-bus controls

FMTCNTRL	= 0 : = 1 : = 2 : = 3 : = 4 : = 5 : = 6 : = 7 :	4:1:1 format, DMSD2 format 4:1:1 format, customized format 4:2:2 format, from DMSD2 4:2:2 format, parallel 4:4:4 format, parallel not used not used not used
$\overline{MATBYPASS}$	= 1 : = 0 :	matrix in use matrix bypassed
$\overline{VLUTLOAD}$	= 1 : = 0 :	VLOAD inactive VLOAD data lines active to load VLUT
VLUTDATA	:	load VLUT's via I²C-bus (256 x 8-bit)
$\overline{INRESET}$	= 1 : = 0 :	input latches at the formatter are always transparent at the end of each active video line the input latches have to be set to fixed values (Y to 16; Cr, Cb to 128; if HREF = 0)
IICOE	= 1 : = 0 :	$\overline{OE}$ enabled switches the output to high impedance mode

Output signals

VIDEO DATA

$\overline{OE}$ (output enable, fast switch, active LOW) and IICOE (I^2C output enable, active HIGH) switchs the DATAOUT lines when in the high-impedance mode (see Control facilities).

Table 16 Format of DATAOUT (RGB if matrix in use)

DATAOUT1 (0 to 7)	Red
DATAOUT2 (0 to 7)	Green
DATAOUT3 (0 to 7)	Blue
To all three DATAOUT lines:	
Sampling frequency	12 to 16 MHz
Level	0 IRE; quantization level 16 100 IRE; quantization level 235

AUXILIARY DATA

Pipelined external reference signal HREF_OUT (delayed HREF).

The delay line (wordlength 1-bit) has the same duration as the signal processing of the video data lines.

OPERATING CONDITIONS

Electrical Conditions

Start-up condition

No particular function except the external power-on-reset e.g. for I^2C-bus interface (RESET) is intended.

Operating time

As this device will be used in computers, it has been designed to operate continuously.

Temperature range

Refer to the characteristics.

Backup

No backup capability (standby) is provided internally.

Power down mode

No power-down capability is provided internally.

CHARACTERISTICS

SYMBOL	PARAMETERS	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DD}	supply voltage range		4.5	5.5	V
Inputs					
V_{IL}	input voltage LOW (SDA, SCL)		−0.5	1.5	V
V_{IH}	input voltage HIGH (SDA, SCL)		3.0	V_{DD} +0.5	V
V_{IL}	input voltage LOW (any other)		−0.5	0.8	V
V_{IH}	input voltage HIGH (any other)		2.0	V_{DD} +0.5	V
I_{LI}	input leakage current		-	10	μA
C_I	input capacitance (clocks)		-	10	pF
C_I	input capacitance (data)		-	8	pF
Outputs					
V_{OH}	output voltage HIGH	note 1	2.4	V_{DD}	V
V_{OL}	output voltage LOW	note 1	0	0.6	V
C_L	output load capacitance (data and HREF)		15	40	pF
Timing					
t_{LL27}	cycle time	note 2	31	45	ns
k_{LL27}	duty factor		40	60	%
t_r	rise time		-	5	ns
t_f	fall time		-	6	ns
t_{CDL}	duty time LOW	note 3	26	-	ns
t_{CDH}	duty time HIGH		18	-	ns
t_{CS}	CREF set-up time		*	11	ns
t_{CH}	CREF hold time		*	3	ns
t_{HS}	HREF set-up time		*	11	ns
t_{HH}	HREF hold time		*	3	ns
$t_{SU;DAT}$	input data set-up time		11	-	ns
$t_{HD;DAT}$	input data hold time		3	-	ns
t_{OH}	ouput hold time		13	-	ns
$t_{OS;DAT}$	output data set-up time		14	-	ns
t_{SZ}	output disable time to 3-state		*	-	ns
t_{ZS}	output enable time from 3-state		*	-	ns

Note to the characteristics

1. The levels must be measured with the following load circuits; 0.6 kΩ to 3.0 V (2 TTL load); C_L = 40 pF.

2. DMSD-mode means that the DCSC will work in a DMSD environment. The CLOCK and the clock reference signal CREF is fed by the SCGC (SAA7157).

3. 16 MHz-mode means that the DCSC will work in any other environment. The CREF signal will be set to HIGH, the CLOCK signal can be any clock up to 16 MHZ.

* Value to be fixed

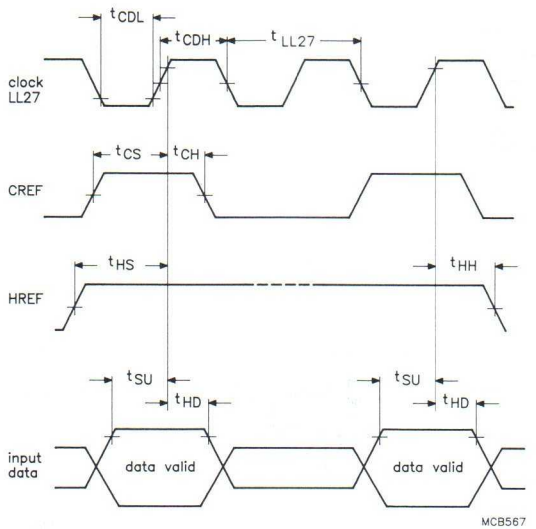


Fig.10 Input timing diagram.

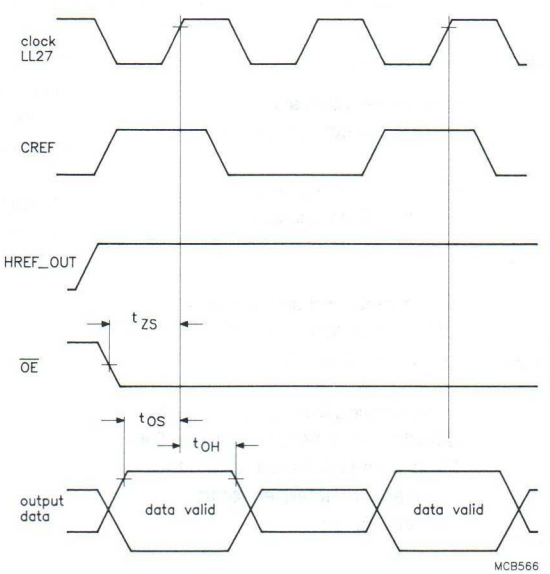


Fig.11 Output timing diagram.

Error condition

So as to inhibit unwanted operations, no information signal is available to the peripheral circuits. In the advent of an error the system has to be started again by applying the $\overline{\text{RESET}}$ signal.

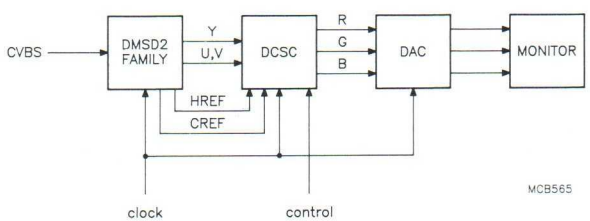


Fig.12 Application example.

SYSTEM BLOCK DESCRIPTION

INPUT FORMATTER

The formatter consist of five functional blocks;

- the multiplexer, which decodes the luminance and chrominance input signals
- the filter, which interpolates the samples of the incoming signal to get an upsampled data rate as at DATAIN1
- the luminance delay line;
- the timing control which creates the internal reference signals from the various inputs
- the bypass output multiplexer

Multiplexer

The data applied at DATAIN1 to DATAIN3 is converted as follows;

FIL1 : Y Luminance
FIL2 : Cb colour-difference signal B-Y
FIL3 : Cr colour-difference signal R-Y

The formats and data rates of DATAIN are described in 'Video data' (see tables 4 to 13).

The sampling frequency of the FIL data lines is 16 MHz maximum. The levels of the FIL data lines are the same as characterized for the DATAIN signals.

The timing reference signals CLOCK, HREF and CREF, for distinguishing the incoming data signals, are described in 'Control data'.

The signal FMTCNTRL is used to control the multiplexer and the filter.

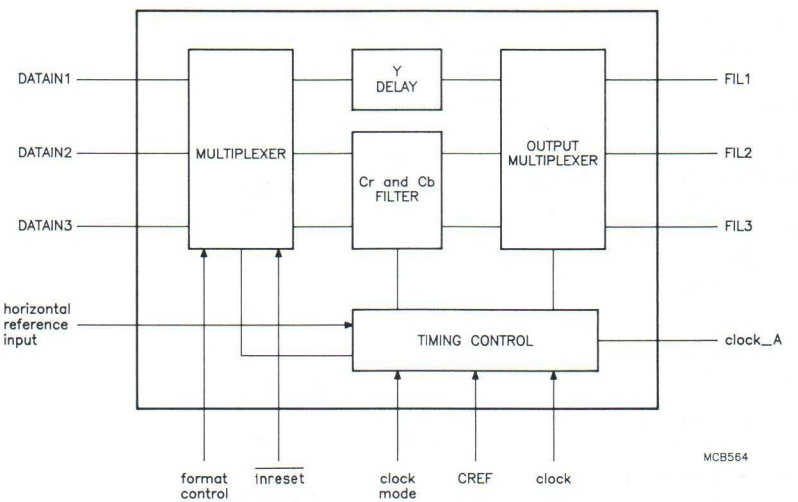


Fig.13 Input formatter.

FMTCNTRL = 0 : 4:1:1 format; DMSD2 format
= 1 : 4:1:1 format; customized format
= 2 : 4:2:2 format; from DMSD2
= 3 : 4:2:2 format; parallel
= 4 : 4:4:4 format; parallel
= 5 : not used
= 6 : not used
= 7 : not used

$\overline{\text{INRESET}}$ = 1 : input latches transparent
= 0 : input latches has to be set to fixed values (Y to 16, Cr, Cb to 128) if HREF = 0

CLK_MODE = 1 : DMSD mode (LL27 clock of DMSD feeds the DCSC)
= 0 : DCSC is feed by a clock of maximum 16 MHz without CREF signal.

Timing control

The timing control unit generates the required control signals from the incoming reference signals and the internally used CLOCK_A.

Filter and delay line

In the various functional modes the signal FMTCNTRL switches in the required filters (FMTCNTRL is described in 'Control data'). In all modes the same propagation delay will be realized, (the reference is Cb0).

DELAY LINE (LUMINANCE-DELAY)

At all frequencies and in all formats, there is a delay line to compensate for the delay of the signal processing time needed in the chrominance section.

CHROMINANCE FILTER

The filter for the Cr and Cb signal is realized in one filter design.

Format 1, 2 4:1:1

An interpolating filter is inserted to convert the original sampling frequency to the sampling frequency of the luminance signal i.e. four times the colour signal. Figure 14 illustrates the frequency response of the chrominance section.

Format 3, 4 4:2:2

An interpolating filter is inserted to convert the original sampling frequency to the sampling frequency of the luminance signal i.e. twice the colour signal. Figure 15 illustrates the frequency response of the chrominance section.

Format 5 4:4:4

A bypass with a specified delay is inserted.

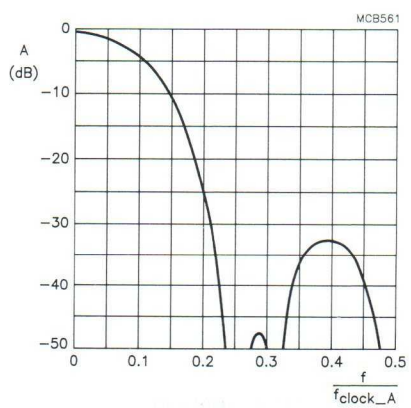


Fig.14 Frequency response of 4:1:1 filter.

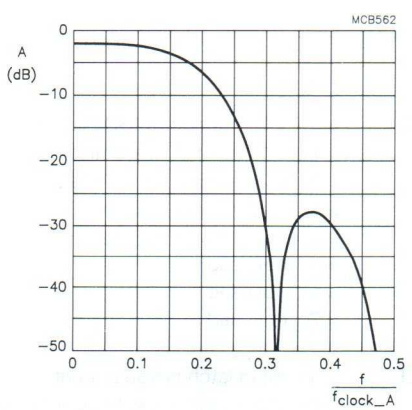


Fig.15 Frequency response of 4:2:2 filter

CONVERSIONAL MATRIX

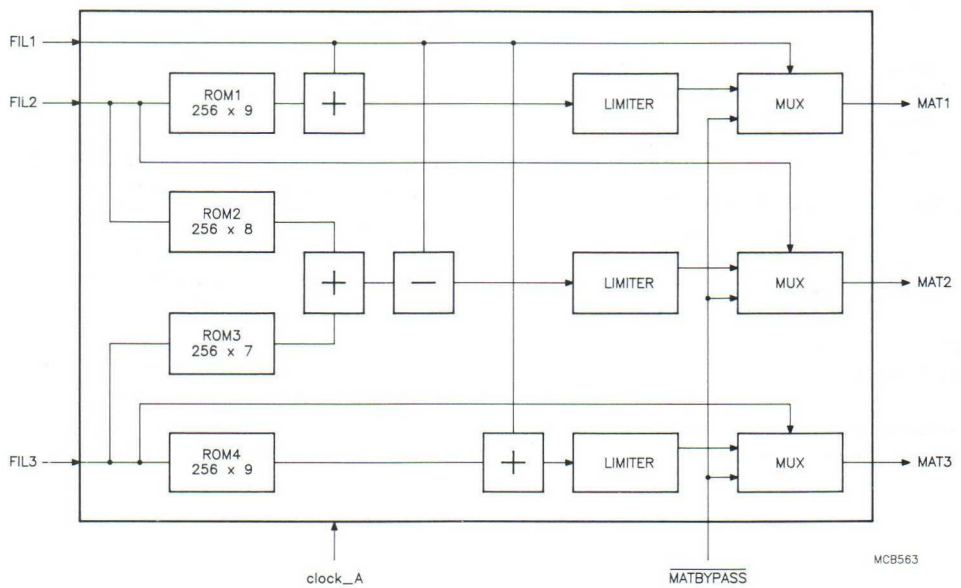


Fig.16 Block diagram MATRIX.

The properties of the conversion matrix are as follows:

- the conversion equations are (according to CCIR 601, with respect to the different quantisation on Y, Cb and Cr);

  Red = Y + 1.371 (Cr - 0.5)
  Green = Y - 0.698 (Cr - 0.5) - 0.336 (Cb - 0.5)
  Blue = Y + 1.732 (Cb - 0.5)

- the accuracy of the signal processing is within ± 0.5% of the accuracy of a theoretical conversion.

- the input and output data lines are 8-bit.

- $\overline{\text{MATBYPASS}}$ switches the matrix in bypass. The bypass has the same propagation delay as the matrix itself.

Input/Output Data

The levels are as follows:

FIL1 : luminance signal Y
: 0 IRE; black, quantization level 16
100 IRE; white, quantization level 235

FIL2 : multiplexed colour difference signals Cr
: bottom peak; quantization level 16
: top peak; quantization level 240
: colourless; quantization level 128

FIL3 : multiplexed colour difference signals Cb
: bottom peak; quantization level 16
: top peak; quantization level 240
: colourless; quantization level 128

The data rate on the input is maximum 16 MHz

The levels at the input and output, for some specific colour patterns, are given in Table 17.

CONTROL SIGNALS

$\overline{\text{MATBYPASS}}$ = 1 : matrix in use
= 0 : matrix bypassed

Functional description

Four ROMs are used to obtain the coefficients with the required accuracy.

In the advent of non-standard input levels the limiter reduces the possible data values at the output (red, green, blue channel) to values between 0 and 255. Consequently, all negative values are set to 0 and all values higher than 255 are set to 255.

Table 17 Levels at the functional blocks

test number	Y FIL1	CR FIL2	CB FIL3	MAT1 R	MAT2 G	MAT3 B
1 (white)	235	128	128	235	235	235
2 (black)	16	128	128	16	16	16
3 (red)	82	240	90	235	16	16
4 (green)	145	34	54	16	236	16
5 (blue)	41	110	240	16	16	235

VIDEO LOOK-UP TABLE AND OUTPUT STAGE

Functional description

The $\overline{\text{VLUTLOAD}}$ signal enables the memories to obtain data from the VLUTDATA signal via the I²C-bus (auto-increment mode). The three RAMs will also obtain the same data.

$\overline{\text{VLUTBYPASS}}$ will bypass the VLUT's in clock period time (real time switch).

In computer applications the VLUT is also known as Colour Look-Up Table (CLUT).

In the DCSC this table might be used to invert the Gamma-correction of a camera. This correction is applied to compensate for the non-linear relationship between the video voltage applied to the cathode and the light output of the phosphor of a CRT.
The Gamma-correction function (also known as Gradation) is given as;

$Y = X^{\gamma}$

The VLUT's are realized by 256 x 8-bit RAMs.

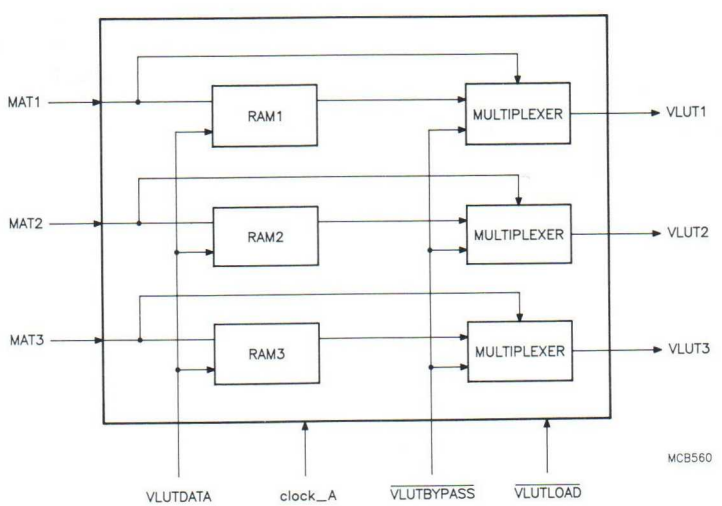


Fig.17 Block diagram video look up table.

I²C-bus receiver

Functional description

At switch-on all internal control signals are at undefined values and the I²C-bus receiver must, therefore, be reset by the external $\overline{\text{RESET}}$ signal. After reset the control signals will be set as follows:

IICOE	= logic 1	$\overline{\text{OE}}$ enabled
FMTCNTRL	= 4	format 4:4:4
$\overline{\text{MATBYPASS}}$	= logic 0	matrix bypassed
$\overline{\text{VLUTLOAD}}$	= logic 1	VLUT at read operation
$\overline{\text{INRESET}}$	= logic 0	input data set to fixed values

Receiver organisation

The address for the DCSC is as follows:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	1	0	0	0	X	0

write only

hardware programmable address bit

S	DCSC ADDRESS	A	SUB-ADDRESS	A	DATA BYTE	A	P

where S = start
A = acknowledge
P = stop

Table 18 Sub-address and data byte formats

HEX SUBADD	BINARY - DATA								FUNCTION
	D7	D6	D5	D4	D3	D2	D1	D0	
00	X	X	X	X	X	0	0	0	input formatter to Format 1
00	X	X	X	X	X	0	0	1	input formatter to Format 2
00	X	X	X	X	X	0	1	0	input formatter to Format 3
00	X	X	X	X	X	0	1	1	input formatter to Format 4
00	X	X	X	X	X	1	0	0	input formatter to Format 5
00	X	X	X	X	0	X	X	X	matrix bypassed
00	X	X	X	X	1	X	X	X	matrix in use
00	X	X	X	0	X	X	X	X	input data at fixed values
00	X	X	X	1	X	X	X	X	input data to formatter
00	X	X	1	X	X	X	X	X	$\overline{OE}$ enabled
00	X	X	0	X	X	X	X	X	output stages 3-state
00	X	0	X	X	X	X	X	X	VLUT write enabled
00	X	1	X	X	X	X	X	X	VLUT read enabled
01	X	X	X	X	X	X	X	X	VLUTDATA

where;

D0 to D2 = FMTCONTROL
D3 = $\overline{MATBYPASS}$
D4 = $\overline{INRESET}$
D5 = IICOE
D6 = $\overline{VLUTLOAD}$
D7 = not used

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	May 1992

SAA7197

Clock signal generator circuit for Desktop Video systems (SCGC)

FEATURES

- Suitable for Desktop Video systems
- Two different sync sources selectable
- PLL frequency multiplier to generate 4 times of input frequency
- Dividers to generate clocks LLCA, LLCB, LLC2A and LLC2B (2nd and 4th multiples of input frequency)
- PLL mode or VCO mode selectable
- Reset control and power fail detection

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8, 17)	4.5	5.0	5.5	V
I_{DDA}	analog supply current	3	-	9	mA
I_{DDD}	digital supply current	10	-	60	mA
V_{LFCO}	LFCO input voltage (peak-to-peak value)	1	-	V_{DDA}	V
f_i	input frequency range	5.5	-	8.0	MHz
V_I	input voltage LOW input voltage HIGH	0 2.0	- -	0.8 V_{DDD}	V V
V_O	output voltage LOW output voltage HIGH	0 2.6	- -	0.6 V_{DDD}	V V
T_{amb}	operating ambient temperature range	0	-	70	°C

GENERAL DESCRIPTION

The SAA7197 generates all clock signals required for a digital TV system suitable for the SAA719x family. The circuit operates in either the phase-locked loop mode (PLL) or voltage controlled oscillator mode (VCO).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7197	20	DIL	plastic	SOT146
SAA7197T	20	mini-pack (SO20)	plastic	SOT163A

Clock signal generator circuit for Desktop Video systems (SCGC)

SAA7197

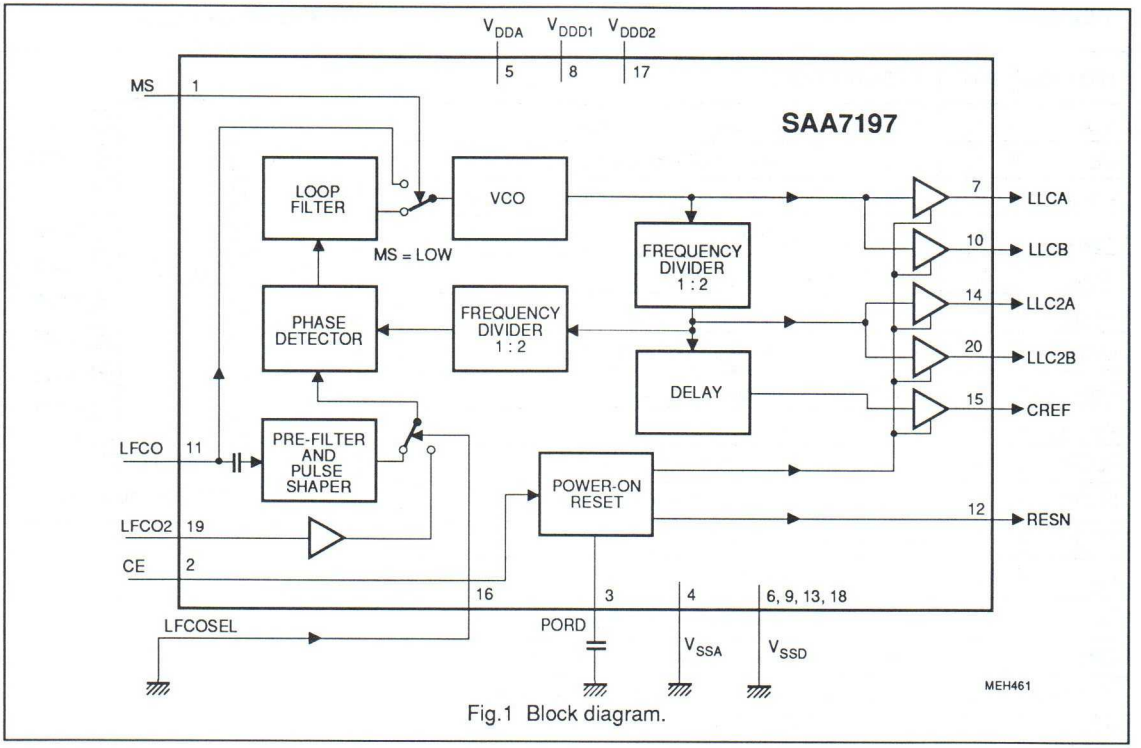


Fig.1 Block diagram.

FUNCTION DESCRIPTION

The SAA7197 generates all clock signals required for a digital TV system suitable for the SAA719x family consisting of an 8-bit analog-to-digital converter (ADC8), digital video multistandard decoder, square pixel (DMSD-SQP), digital video colour space converter (DCSC) and optional extentions. The SAA7197 completes a system for Desktop Video applications in conjunction with memory controllers.

The input signal LFCO is a digital-to-analog converted signal provided by the DMDS-SQPs horizontal PLL. It is the multiple of the line frequency:

7.38 MHz = 472 x f_H in 50 Hz systems
6.14 MHz = 360 x f_H in 60 Hz systems

LFCO2 (TTL-compatible signal from an external reference source) can be applied to pin 19 (LFCOSEL = HIGH).

The input signal LFCO or LFCO2 is multiplied by factors 2 or 4 in the PLL (including phase detector, loop filter, VCO and frequency divider) and output on LLCA (pin7), LLCB (pin 10), LLC2A (pin 14) and LLC2B (pin 20). The rectangular output signals have 50 % duty factor. Outputs with equal frequency may be connected together externally. The clock outputs go HIGH during power-on reset (and chip enable) to ensure that no output clock signals are available the PLL has locked-on.

Mode select MS

The LFCO input signal is directly connected to the VCO at MS = HIGH. The circuit operates as an oscillator and frequency divider. This function is not tested.

Source select LFCOSEL

Line frequency control signal LFCO (pin 11) is selected by LFCOSEL = LOW. LFCOSEL = HIGH selects LFCO2 input signal (pin 19). This function is not tested.

Chip enable CE

The buffer outputs are enabled and RESN set HIGH by CE = HIGH (Fig.4). CE = LOW sets the clock outputs HIGH and RESN output LOW.

CREF output

2 f_{LFCO} output to control the clock dividers of the DMSD-SQP chip family.

Power-on reset

Power-on reset is activated at power-on, when the supply voltage decreases below 3.5 V (Fig.4) or when chip enable is done. The indicator output RESN is LOW for a time determined by capacitor on pin 3. The RESN signal can be applied to reset other circuits of this digital TV system.
The LFCO or LFCO2 input signals have to be applied before RESN becomes HIGH.

Clock signal generator circuit for Desktop Video systems (SCGC)

SAA7197

PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	mode select input (LOW = PLL mode)*
CE	2	chip enable /reset (HIGH = outputs enabled)
PORD	3	power-on reset delay, dependent on external capacitor
V_{SSA}	4	analog ground (0 V)
V_{DDA}	5	analog supply voltage (+5 V)
V_{SSD1}	6	digital ground 1 (0 V)
LLCA	7	line-locked clock output signal (4 times f_{LFCO})
V_{DDD1}	8	digital supply voltage 1 (+5 V)
V_{SSD2}	9	digital ground 2 (0 V)
LLCB	10	line-locked clock output signal (4 times f_{LFCO})
LFCO	11	line-locked frequency control input signal 1
RESN	12	reset output (active-LOW, Fig.4)
V_{SSD3}	13	digital ground 3 (0 V)
LLC2A	14	line-locked clock output signal 2A (2 times f_{LFCO})
CREF	15	clock reference output, qualifier signal (2 times f_{LFCO})
LFCOSEL	16	LFCO source select (LOW = LFCO selected)*
V_{DDD2}	17	digital supply voltage 2 (+5 V)
V_{SSD4}	18	digital ground 4 (0 V)
LFCO2	19	line-locked frequency control input signal 2*
LLC2B	20	line-locked clock output signal 2B (2 times f_{LFCO})

PIN CONFIGURATION

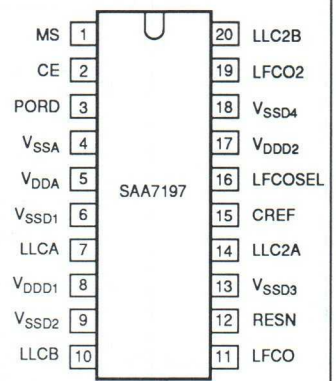


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); ground pins as well as supply pins together connected.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	–0.5	7.0	V
V_{DDD}	digital supply voltage (pins 8 and 17)	–0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{DDA} - V_{DDD}$	-	±100	mV
V_O	output voltage (I_{OM} = 20 mA)	–0.5	V_{DDD}	V
P_{tot}	total power dissipation (DIL20)	0	1.1	W
T_{stg}	storage temperature range	–65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling** for all pins	-	tbf	V

* MS and LFCO2 functions are not tested. LFCO2 is a multiple of horizontal frequency.

** Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal handling precautions appropriate to "Handling MOS devices ".

CHARACTERISTICS

$V_{DDA} = V_{DDD} = 4.5$ to 5.5 V; $f_{LFCO} = 5.5$ to 8.0 MHz and $T_{amb} = 0$ to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8 and 17)		4.5	5.0	5.5	V
I_{DDA}	analog supply current (pin 5)		3	-	9	mA
I_{DDD}	digital supply current ($I_8 + I_{17}$)	note 1	10	-	60	mA
V_{reset}	power-on reset threshold voltage	Fig.4	-	3.5	-	V
Input LFCO (pin 11)						
V_{11}	DC input voltage		0	-	V_{DDA}	V
V_i	input signal (peak-to-peak value)		1	-	V_{DDA}	V
f_{LFCO}	input frequency range		5.5	-	8.0	MHz
C_{11}	input capacitance		-	-	10	pF
Inputs MS, CE, LFCOSEL and LFCO2 (pins 1, 2, 16 and 19); note 3						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}	V
f_{LFCO2}	input frequency range for LFCO2		5.5	-	8.0	MHz
I_{LI}	input leakage current	LFCOSEL	50	-	150	µA
		others	-	-	10	µA
C_I	input capacitance		-	-	5	pF
Output RESN (pin 12)						
V_{OL}	output voltage LOW	$I_{OL} = 2$ mA	0	-	0.4	V
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.4	-	V_{DDD}	V
t_d	RESN delay time	$C_3 = 0.1$µF; Fig.4	20	-	200	ms
Output CREF (pin 15)						
V_{OL}	output voltage LOW	$I_{OL} = 2$ mA	0	-	0.6	V
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.4	-	V_{DDD}	V
f_{CREF}	output frequency CREF	Fig.3	-	$2 f_{LFCO(2)}$		MHz
C_L	output load capacitance		15	-	40	pF
t_{SU}	set-up time	Fig.3; note 1	12	-	-	ns
t_{HD}	hold time	Fig.3; note 1	4	-	-	ns
Output signals LLCA, LLCB, LLC2A and LLC2B (pins 7, 10, 14, and 20); note 3						
V_{OL}	output voltage LOW	$I_{OL} = 2$ mA	0	-	0.6	V
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.6	-	V_{DDD}	V
t_{comp}	composite rise time	Fig.3; notes 1 and 2	-	-	8	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{LL}	output frequency LLCA	Fig.3	-	4 $f_{LFCO(2)}$		MHz
	output frequency LLCB		-	4 $f_{LFCO(2)}$		MHz
	output frequency LLC2A		-	2 $f_{LFCO(2)}$		MHz
	output frequency LLC2B		-	2 $f_{LFCO(2)}$		MHz
t_r, t_f	rise and fall times	Fig.3	-	-	5	ns
t_{LL}	duty factor LLCA, LLCB, LLC2A and LLC2B (mean values)	note 1; Fig.3; at 1.5 V level	40	50	60	%

Notes to the characteristics

1. f_{LFCO} = 7.0 MHz and output load 40 pF (Fig.3). V_{SSA} and V_{SSD} connected together.
2. t_{comp} is the rise time from LOW of all clocks to HIGH of all clocks (Fig.3) including rise time, skew and jitter components. Measurements taken between 0.6 V and 2.6 V. Skew between two LLx clocks will not deviate more than ±2 ns if output loads are matched within 20 %.
3. MS and LFCO2 functions not tested.

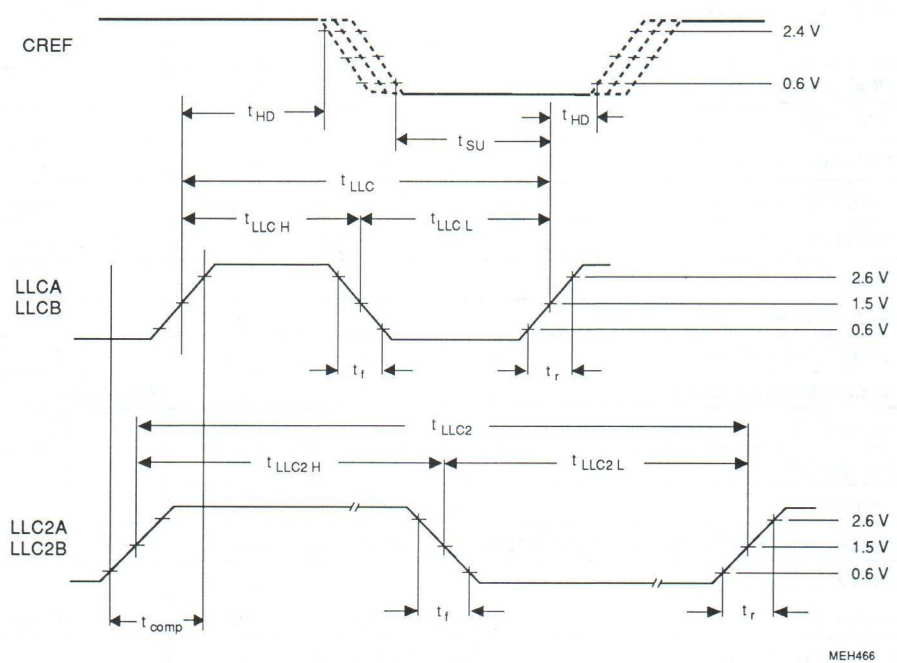


Fig.3 Output timing.

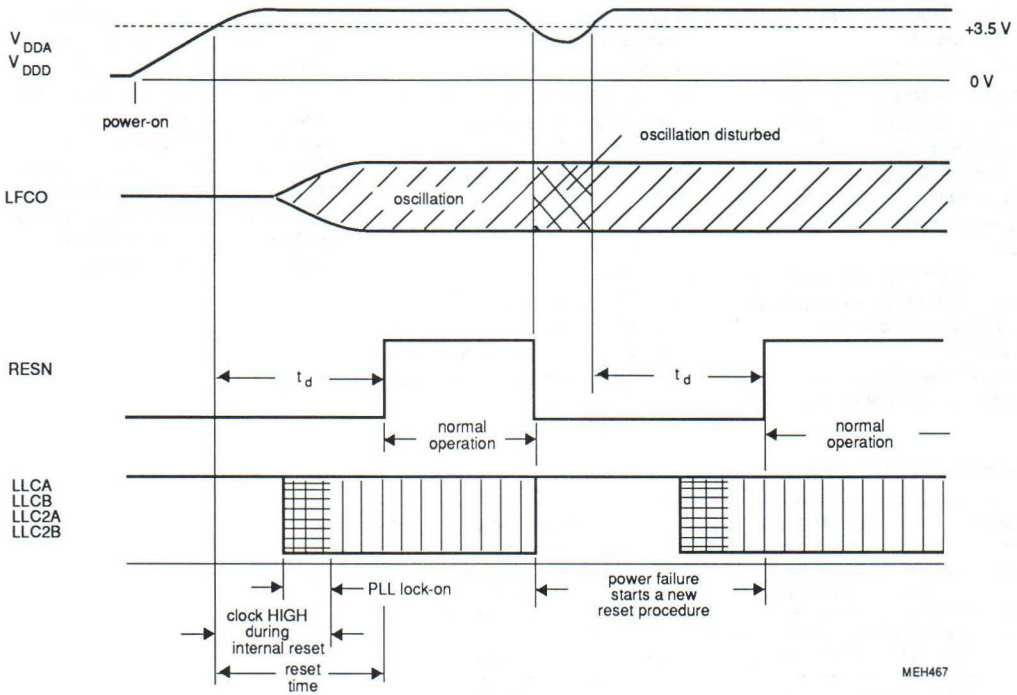


Fig.4 Reset procedure.

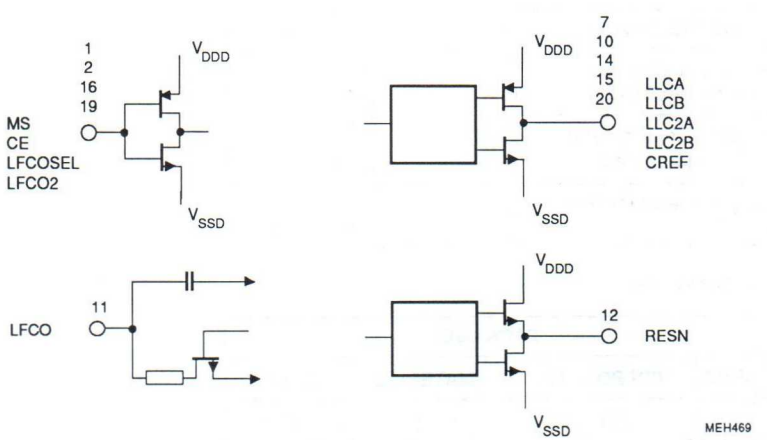


Fig.5 Internal circuit.

Digital video encoder, GENLOCK-capable — SAA7199B

1. FEATURES

- Monolithic integrated CMOS video encoder circuit
- Standard MPU (12 lines) and I²C-bus interfaces for controls
- Three 8-bit signal inputs PD(7-0) for RGB respectively YUV or indexed colour signals (Tables 10 to 17)
- Square pixel and CCIR input data rates
- Band-limited composite sync pulses
- Three 256X8 colour look-up tables (CLUTs) e. g. for gamma-correction
- External subcarrier from a digital decoder (SAA7151B or SAA7191B)
- Multi-purpose key for real-time format switching
- Autonomous internal blanking
- Optional GENLOCK operation with adjustable horizontal sync timing and adjustable subcarrier phase
- Stable GENLOCK operation in VCR standard playback mode
- Optional still video capture extension
- Three suitable video 9-bit digital-to-analog converters
- Composite analog output signals CVBS, Y and C for PAL/NTSC
- "Line 21" data insertion possible

2. GENERAL DESCRIPTION

The SAA7199B encodes digital base-band colour/video data into analog Y, C and CVBS signals (S-Video included). Pixel clock and data are line-locked to the horizontal scanning frequency of the video signal. The circuit can be used in a square pixel or in a consumer TV application. Flexibility is provided by programming facilities via MPU-bus (parallel) or I²C-bus (serial).

3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage range (pins 2, 21 and 41)	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage range (pins 64, 66, 70 and 72)	4.75	5.0	5.25	V
I_P	total supply current	-	-	200	mA
V_I	input signal levels	TTL-compatible			
V_o	analog output signals Y, C and CVBS without load (peak-to-peak value)	-	2	-	V
R_L	output load resistance	90	-	-	Ω
ILE	LF integral linearity error in output signal (9-bit DAC)	-	-	±1	LSB
DLE	LF differential linearity error in output signal (9-bit DAC)	-	-	±0.5	LSB
T_{amb}	operating ambient temperature range	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7199B	84	PLCC	plastic	SOT189CG

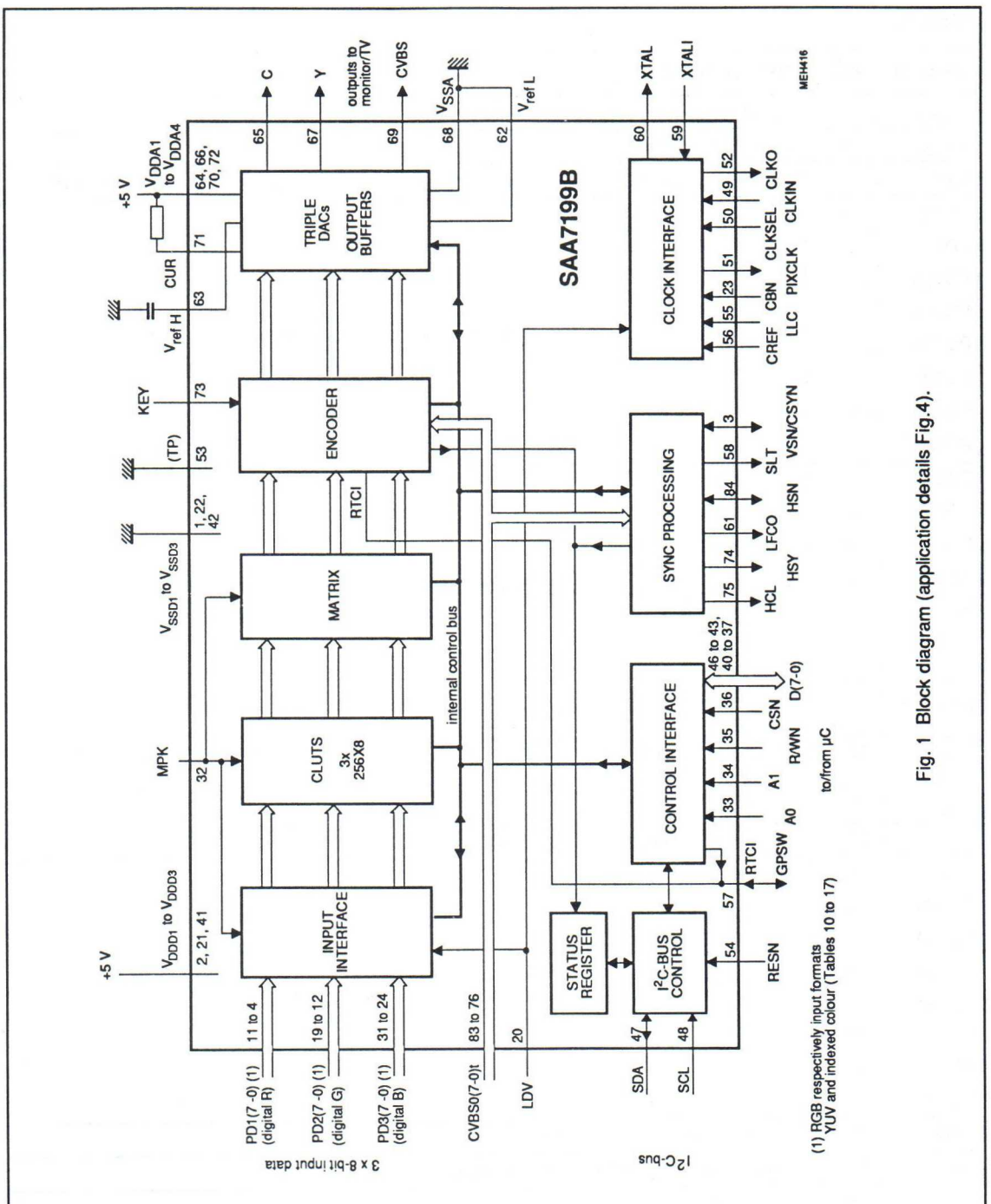


Fig. 1 Block diagram (application details Fig.4).

(1) RGB respectively input formats YUV and indexed colour (Tables 10 to 17)

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSD1}	1	digital ground 1 (0 V)
V_{DDD1}	2	+5 V digital supply 1
VSN	3	vertical sync output (3-state), conditionally composite sync output; active LOW or active HIGH
PD1(0)	4	data 1 input: digital signal R (red) respectively V signal (formats in Table 6)
PD1(1)	5	
PD1(2)	6	
PD1(3)	7	
PD1(4)	8	
PD1(5)	9	
PD1(6)	10	
PD1(7)	11	
PD2(0)	12	data 2 input: digital signal G (green) respectively Y signal or indexed colour data (formats in Table 6)
PD2(1)	13	
PD2(2)	14	
PD2(3)	15	
PD2(4)	16	
PD2(5)	17	
PD2(6)	18	
PD2(7)	19	
LDV	20	load data clock input signal to input interface (samples PDn(7-0), CBN, MPK, KEY and RTCI)
V_{DDD2}	21	+5 digital supply 2
V_{SSD2}	22	digital ground 2 (0 V)
CBN	23	composite blanking input; active LOW
PD3(0)	24	data 3 input: digital signal B (blue) respectively U signal (formats in Table 6)
PD3(1)	25	
PD3(2)	26	
PD3(3)	27	
PD3(4)	28	
PD3(5)	29	
PD3(6)	30	
PD3(7)	31	
MPK	32	multi-purpose key; active HIGH
A0	33	subaddress bit A0 for microcomputer access (Table 3)
A1	34	subaddress bit A1 for microcomputer access (Table 3)

SYMBOL	PIN	DESCRIPTION
R/WN	35	read/ write not input signal from microcontroller
CSN	36	chip select input for parallel interface; active LOW
D0	37	bidirectional port from/to microcontroller (bits D3 to D0)
D1	38	
D2	39	
D3	40	
V_{DDD3}	41	+5 V digital supply 3
V_{SSD3}	42	digital ground 3
D4	43	bidirectional port from/to microcontroller (bits D7 to D4)
D5	44	
D6	45	
D7	46	
SDA	47	I^2C-bus data line
SCL	48	I^2C-bus clock line
CLKIN	49	external clock signal input (maximum 60 MHz)
CLKSEL	50	clock source select input
PIXCLK	51	CLKO/2 or conditionally CLKO output signal
CLKO	52	selected clock output signal (LLC or CLKIN)
TP	53	connect to ground (test pin)
RESN	54	reset input; active LOW
LLC	55	line-locked clock input signal from external CGC
CREF	56	clock qualifier of external CGC
GPSW / RTCI	57	general purpose switch output (set via I^2C-bus or MPU-bus); real-time control input, defined by I^2C or MPU programming
SLT	58	GENLOCK flag (3-state): HIGH = sync lost in GENLOCK mode; LOW = otherwise
XTALI	59	crystal oscillator input (26.8 or 24.576 MHz)
XTAL	60	crystal oscillator output
LFCO	61	line frequency control output signal for external CGC
$V_{ref\,L}$	62	reference LOW voltage of DACs (resistor chains)
$V_{ref\,H}$	63	reference HIGH voltage of DACs (resistor chains)
V_{DDA4}	64	+5 V analog supply 4 for resistor chains of the DACs
C	65	chrominance analog output signal C
V_{DDA1}	66	+5 V analog supply 1 for output buffer amplifier of DAC1
Y	67	luminance analog output signal Y
V_{SSA}	68	analog ground (0 V)

SYMBOL	PIN	DESCRIPTION
CVBS	69	CVBS analog output signal
V_{DDA2}	70	+5 V analog supply 2 for output buffer amplifier of DAC2
CUR	71	current input for analog output buffers
V_{DDA3}	72	+5 V analog supply 3 for output buffer amplifier of DAC3
KEY	73	key signal to insert CVBS input signal into encoded CVBS output signal; active HIGH
HSY	74	horizontal sync indicator output signal; active HIGH (3-state output to ADC)
HCL	75	horizontal clamping output; active HIGH (3-state output)
CVBS0	76	digital CVBS input signal
CVBS1	77	
CVBS2	78	
CVBS3	79	
CVBS4	80	
CVBS5	81	
CVBS6	82	
CVBS7	83	
HSN	84	horizontal sync output; active LOW or active HIGH for 60/66/72 x PIXCLK at 12.27/13.5/14.75 MHz (3-state output)

FUNCTIONAL DESCRIPTION

The SAA7199B is a digital video encoder that translates digital RGB, YUV or 8-bit indexed colour signals into the analog PAL/NTSC output signals Y (luminance), C (4.43/3.58 MHz chrominance) and CVBS (composite signal including sync).

Four different modes are selectable (Table 9):

- stand-alone mode (horizontal and vertical timings are generated)
- slaver mode (stand-alone unit that accepts external horizontal and vertical timing), and optional real-time information for subcarrier/clock from a digital colour decoder
- GENLOCK mode (GENLOCK capabilities are achieved in conjunction with determined ICs).
- test mode (only clock signal is required)

The input data rate (pixel sequence) has an integer relationship to the number of horizontal clock cycles (Table 1). A sufficient stable external clock signal ensures correct encoding. The generated clock frequency in the GENLOCK mode may deviate by ±7 % depending on the reference signal which is corresponding to its input sync signal. The clock will be nominal in the GENLOCK mode when the reference signal is absent (nominal with crystal oscillator accuracy for TV time constants, and nominal ±1.4 % for VCR time constants).

The on-chip colour conversion matrix provides CCIR 601 code-compatible transcoding of RGB to YUV data.

RGB data out of bounds, with respect to CCIR 601 specification, can be clipped to prevent over-loading of the colour modulator. RGB data input can be either in linear colour space or in gamma-corrected colour space. YUV data must be gamma-corrected according to CCIR 601. This circuit operates primarily in a 24-bit colour space (3 x 8-bit) but can also accomodate different data formats (4:1:1, 4:2:2 and 4:4:4) as well as 8-bit indexed pseudo-colour space operations (FMT-bits in Table 6).

RGB CLUTs on chip provide gamma-correction and/or other CLUT functions. They consist of programmable tables to be loaded

Table 1 Pixel relationships

ACTIVE PIXELS PER LINE	FIELD RATE	MULTIPLES OF LINE FREQUENCY	PIXCLK OUTPUT SIGNAL (MHz)	XTAL (MHz)
640 (square)	60 Hz	780	12.272727	26.8
720	60 Hz	858	13.5	24.576
768 (square)	50 Hz	944	14.75	26.8
720	50 Hz	864	13.5	24.576

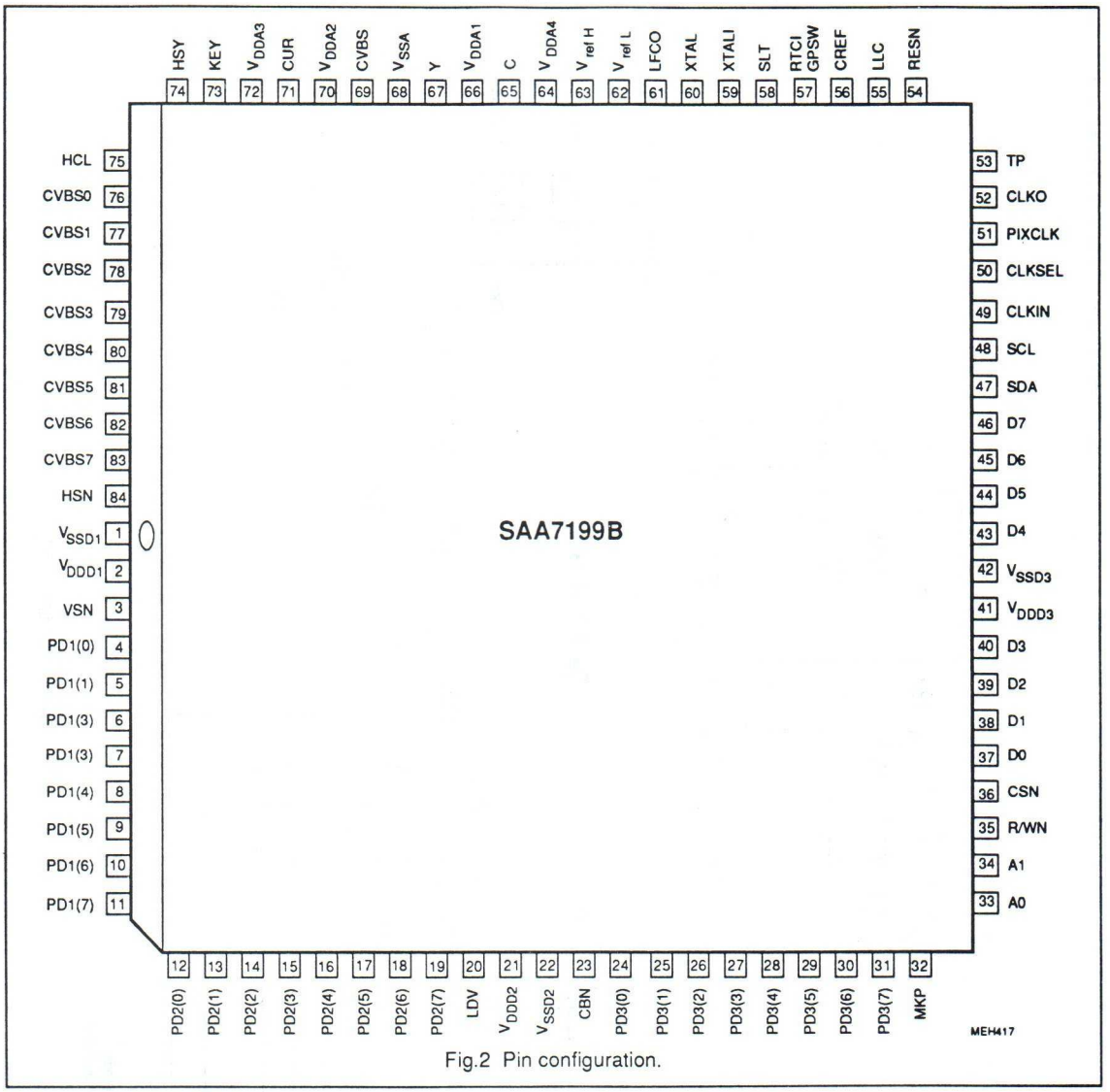


Fig.2 Pin configuration.

independently, and they generate 24-bit gamma-corrected output signals from 24-bit data of one of the input formats or from 8-bit indexed pseudo-colour data.

Required modulation is performed. The digital YUV data is encoded according to standards RS-170A (composite NTSC) and CCIR 624-4 (composite PAL-B/G). S-Video output signal is available (Y/C) as well as some sub-standard output signals (STD-bits in Table 6). A 7.5 IRE set-up level is automatically selected in the 60 Hz mode – there is none in 50 Hz mode.

The analog signal outputs can drive directly into terminated 75 Ω coaxial lines, a passive external filter is recommended (Figures 3 and 13). Analog post-filtering is required (LP in Fig.3).

GENLOCK to an external reference signal is achieved by addition of a video ADC and a clock generator combination. Thus, the system is enabled to lock on a stable video source or to a stable VCR source (normal playback). The SAA7199B, the ADC and the clock generator

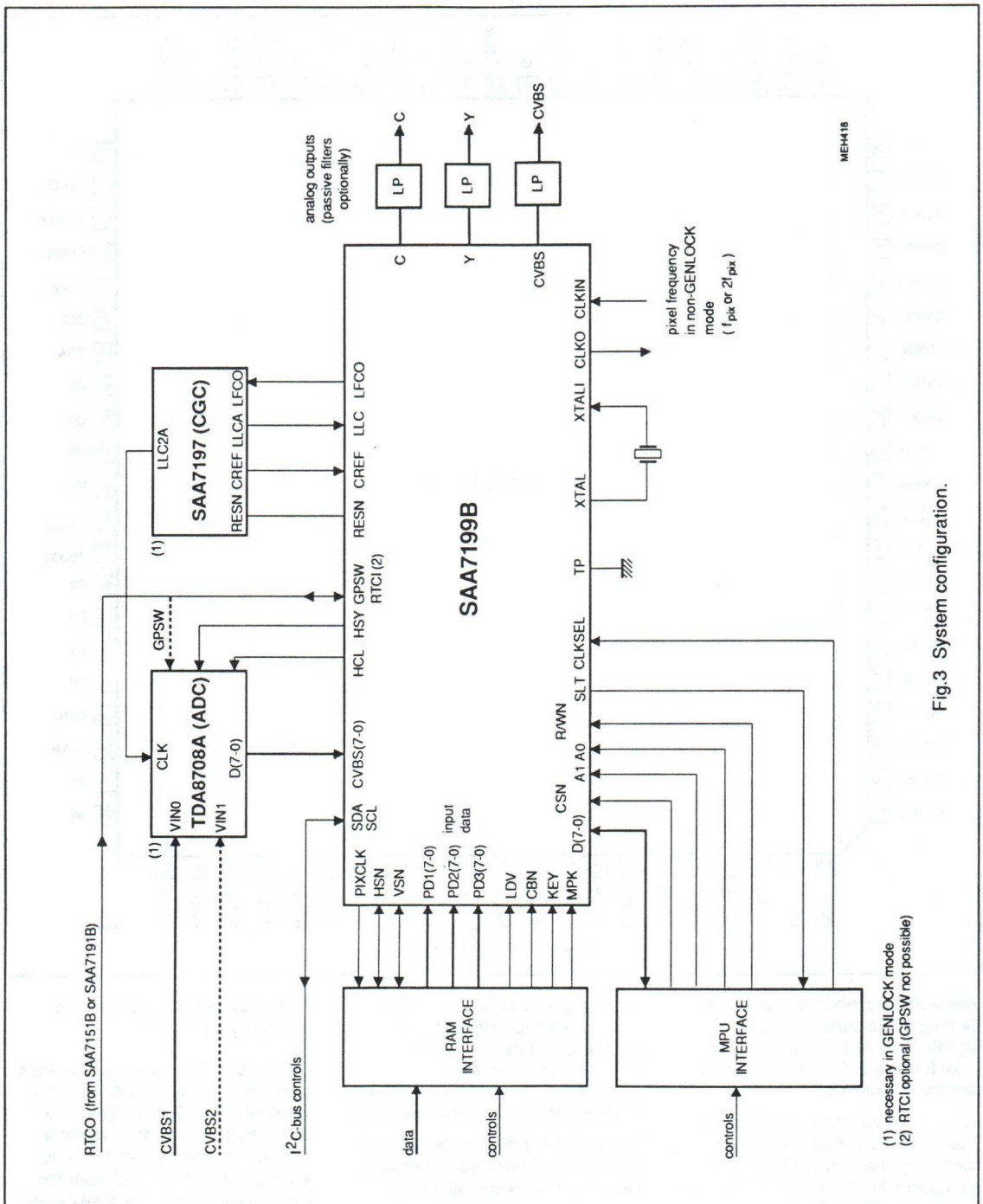


Fig.3 System configuration.

combination (Fig.3) form a control loop achieving a highly stable line-locked clock. The clock has to be generated by a crystal oscillator without this possibility.
The GENLOCK mode is not available in a single device set-up.

Control Interface

The SAA7199B supports a standard parallel MPU interface as well as the serial I²C-bus interface. The MPU has a direct access to internal control registers and colour tables. Update is possible at any time, excluding coincident internal reading and external writing of the same cell (the current pixel value could be destroyed).
The two interfaces of Table 2 are selected automatically. However, the I²C control is inactive when the MPU interface is selected by CSN = LOW. No simultaneous access must occur. I²C-bus and MPU control complement each other and have access to common registers controlled via a common internal bus. The programmer can use virtually identical programs.
The internal memory space is devided into the look-up table and the control table, each with its own 8-bit address register is used as a pointer for specific location. This address register is provided with auto-incrementation and can be written by only one addressing.

The look-up table contains three banks of 256 bytes. Therefore, each read or write cycle must access to all three banks in a determined order. The support logic is part of the control interface.

Timing (Fig.3).

The reference to generate internal clocks from LLC in GENLOCK operation with SAA7197 is CREF (CREF = LLC/2). In this case input CLKSEL is HIGH and the SRC-bit is 1.

In non-GENLOCK operation the signal from CLKIN is used and LDV is clock reference (input CLKSEL = 0; SCR-bit = CPR-bit = 0).

Table 2 Access to the contol interface

SYMBOL	DESCRIPTION
SDA (I²C-bus) SCL	serial data line (bi-directional) clock line
A1, A0 (MPU-bus) R/WN CSN GPSW RESN	address inputs read/write control chip select; I²C-bus disabled (at LOW) general purpose switch output (bit of control register) reset signal (active-LOW)

Table 3 Address assignment

ADDRESS INPUTS A1	A0	I²C-BUS SUBADDRESS	SELECTION
0	0	00	ADR-CLUT (address register of look-up tables)
0	1	01	DATA-CLUT
1	0	02	ADR-CTRL (index register of control table)
1	1	03	DATA-CTRL

Pins LLC and CLKIN are tied together when no switching between LLC and CLKIN is applied. In Fig.3 it is assumed that LLC and CLKIN are double the pixel clock frequency of CREF respectively LDV.
CREF must be at the same frequency (or constant HIGH or LOW) when LLC is at pixel clock frequency.
CPR-bit = 1 if CLKIN is at pixel clock frequency.
Buffered CLKO signal is always delayed. LLC or CLKIN signals are according to CLKSEL

Mapping

Mapping of external control signals onto internal bus. The method is simple. The MPU- bus contains the signals of Table 4 (names in chip-internal nomenclature).

Bit allocation

The Bit Allocation Map (BAM) shows the individual control signals, used to control the different operational modes of the circuit. The I²C-bus is normally used for control. The SAA7199B additionally has a MPU-bus interface for direct microprocessor connection. The following BAM resembles the I²C-bus type but can be also used for the parallel bus. The control registers of Table 5 are indexed from 00 to 0F (hex). Auto-incrementation is applied.

Digital-to-analog converters

The converters use a combination of resistor chains with low-impedance output buffers. The bottom output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V. Fig.15 shows the application for 1.23 V/ 75 Ω outputs, using the serial 25 Ω + 22 Ω resistors.

Each digital-to-analog converter has its own supply pin for purpose of decoupling. V_{DDA4} is the supply voltage for the resistor chains of the three DACs. The accuracy of this supply voltage influences directly the output amplitudes.
The current CUR into pin 71 is 0.3 mA (V_{DDA4} = 5 V, $R_{64\text{-}71}$ = 20 kΩ); a larger current improves the bandwidth but increases the integral non-linearity.

Table 4 Signals on the internal bus

SYMBOL	DESCRIPTION	
R-WN	Select read/write (read = 1; write = 0)	
C-TN	Control table/look-up table (control table = 1; look-up table = 0)	
D-AN	Select data/address (data = 1; address = 0)	
DI/DO(0-7)	Data bus on port inputs/outputs D7 to D0	
EN	Enable from control interface to synchronize data transfer	
INTERNAL PARALLEL BUS	**PARALLEL INTERFACE**	**I²C-BUS INTERFACE**
R-WN	R/WN (pin 35)	LSB of slave address byte (read = HIGH; write = LOW)
C-TN	A1 (pin 34)	X) 4 subaddresses after decoding
A-TN	A0 (pin 33)	X)
DI/DO(0-7)	D7 to D0	Data bits D7 to D0 for each subaddress
EN	CSN and R/WN	Enable by every 9th clock of sample of SCL (control of serial-to-parallel conversion)

Table 5 Bit allocation map (I²C-bus access in Table 8)

INDEX BINARY	INDEX HEX	DATA BYTE D7	D6	D5	D4	D3	D2	D1	D0	DF**
Input processing										
0000 0000	00	VTBY	FMT2	FMT1	FMT0	SCBW	CCIR	MOD1	MOD0	5C
0000 0001	01	TRER7	TRER6	TRER5	TRER4	TRER3	TRER2	TRER1	TRER0	XX
0000 0010	02	TREG7	TREG6	TREG5	TREG4	TREG3	TREG2	TREG1	TREG0	XX
0000 0011	03	TREB7	TREB6	TREB5	TREB4	TREB3	TREB2	TREB1	TREB0	XX
Sync processing										
0000 0100	04	SYSEL1	SYSEL0	SCEN	VTRC	NINT	HPLL	HLCK*	OEF*	10
0000 0101	05	0	0	GDC5	GDC4	GDC3	GDC2	GDC1	GDC0	21
0000 0110	06	IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0	52
0000 0111	07	0	0	PSO5	PSO4	PSO3	PSO2	PSO1	PSO0	32
Control, clock and output formatter										
0000 1000	08	DD	KEYE	SRC	CPR	COKI	IM	GPSW	SRSN	64
0000 1001	09	0	BAME	MPKC1	MPKC0	IEPI	RTSC	RTIN	RTCE	02
0000 1010+	0A+	0	0	0	0	0	0	0	0	00
0000 1011+	0B+	0	0	0	0	0	0	0	0	00
Encoder control										
0000 1100	0C	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0	XX++
0000 1101	0D	FSCO7	FSCO6	FSCO5	FSCO4	FSCO3	FSCO2	FSCO1	FSCO0	00
0000 1110	0E	0	0	0	CLCK*	STD3	STD2	STD1	STD0	0C
0000 1111+	0F+	0	0	0	0	0	0	0	0	

*) read only bits +) reserved ++) adjust as required.

**) DF is the default value for a typical programming example: GENLOCK mode for a VCR; non-gamma-corrected RGB data (realtime keying is possible). SLT will be set if there is no horizontal lock. NTSC-M standard with normal colour bandwidth and 12.2727 MHz pixel rate. CSYN signal will be provided, coming 8 pixel clocks earlier, to compensate pipeline delay in the previous RAM interface. The encoded CVBS is 12 clocks earlier than the CVBS reference on the input of the previous ADC. The CLUTs are bypassed at MPK = HIGH in real-time.

Table 6 Function of register bits of Table 5

Index "00" VTBY	Video look-up table by-pass: 0 = not bypassed; 1 = bypassed (OR connectable with MPK)			
FMT2 to FMT0	Input formats:			
	FMT2	FMT1	FMT0	format
	0	0	0	YUV 4:1:1 format; DMSD2 compatible
	0	0	1	YUV 4:1:1 format; customized
	0	1	0	YUV 4:2:2 format; DMSD2 compatible
	0	1	1	YUV 4:2:2 format; customized
	1	0	0	YUV 4:4:4 format
	1	0	1	RGB 4:4:4 format
	1	1	0	reserved
	1	1	1	8-bit indexed colour
SCBW	Chrominance bandwidth: 0 = enhanced; 1 = standard			
CCIR	Select level: 0 = DMSD2 levels; 1 = CCIR levels			
MOD1 to MOD0	Select mode:			
	MOD1	MOD0	mode	
	0	0	GENLOCK mode	
	0	1	stand-alone mode	
	1	0	slave mode	
	1	1	test mode	
Index "01" TRER7 to TRER0	Test register Red (read/write via MPU-bus; write only via I²C-bus)			
Index "02" TREG7 to TREG0	Test register Green (read/write via MPU-bus; write only via I²C-bus)			
Index "03" TREB7 to TREB0	Test register Blue (read/write via MPU-bus; write only via I²C-bus)			
Index "04" SYSEL1 to SYSEL0	Sync select:			
	SYSEL1	SYSEL0	synchronized from	
	0	0	CSYN (active LOW; pin 3)	
	0	1	HSN and VSN (active LOW; pins 84 and 3)	
	1	0	CSYN (active HIGH; pin 3)	
	1	1	HSN and VSN (active HIGH; pins 84 and 3)	
SCEN	Sync/clamping (HSY/HCL) enable: 0 = disabled (set to HIGH); 1 = enabled			
VTRC	Select TV/VTR mode: 0 = 0 TV mode (slow); 1 = VTR mode (fast)			
NINT	Select interlace of encoded signal: 0 = interlaced (262.5/262.5 or 312.5/312.5) 1 = non-interlaced (262/262 or 312/312 in modes 1 and 3 only)			

HPLL	Select horizontal lock: 0 = lock enabled; 1 = lock disabled (crystal reference)
OEF	Status bit field organization (to be read): 0 = even field; 1 = odd field
HLCK	Status bit sync indication (to be read): 0 = locked to external sync 1 = external sync lost
Index "05" GDC5 to GDC0	GENLOCK delay compensation, note 1: data 00 to 3F equals timing of CVBS output signal is (46 – GDC) pixel clocks = t_{ofs} earlier with respect to reference point t_{REF1}. (t_{REF1} corresponds to the falling edge of the horizontal sync pulse of CVBS input signal; t_{ofs} is designated for propagation delay of extern GENLOCK source, Fig.10).
Index "06" IDEL7 to IDEL0	Increment delay: update of line-locked clock frequency (Table 5, data "43" hex recommended)
Index "07" PSO7 to PSO0	Phase sync in output signal, note 1: data 00 to 3F equals to active slope of HSN, VSN/CSYN is (58 – PSO) pixel clocks = t_{Rint} earlier with respect to reference point t_{REF2}. (t_{REF2} corresponds to PSO = 58; t_{Rint} is designated for pipeline delay of the feeding RAM interface, Fig.10).
Index "08" DD	Digital video encoder disable: 0 = enabled; 1 = disabled
KEYE	Keying enable: 0 = disabled; 1 = enabled (logically AND-connected with KEY)
SRC	Clock source: 0 = external system clock; 1 = DTV2 system clock
CPR	Clock phase reference: 0 = LDV is (pin 20); 1 = LDV is not
COKI	Colour-killer: 0 = colour on; 1 = colour off (subcarrier is switched off)
IM	Interrupt mask: 1 = interrupt not masked at sync lost (pin 58) 0 = interrupt masked.at sync lost (pin 58)
GPSW	General purpose switch at bit RTIN = 1: 0 = pin 57 LOW; 1 = pin 57 HIGH
SRSN	Software reset: 0 = no reset; 1 = reset (see reset procedure)
Index "09" BAME	Burst amplitude indication: 0..= burst amplitude measurement is overridden; colour lock always assumed 1 = burst amplitude is used to control the CLCK status bit, recommended for reference signal without subcarrier burst (pure black and white) in order to avoid PLL hunting.

<table>
<tr><td>MPKC1 to MPKC0</td><td>Multi-purpose key control: At MKP = LOW (pin 32) are all functions as given by software programming;
MKP = HIGH sets in real-time with respect to PDn(7-0).
<table>
<tr><th colspan="2">Set by bits</th><th colspan="4">in function blocks</th></tr>
<tr><th>MPKC1</th><th>MPKC0</th><th>input formatter</th><th>CLUTs</th><th>matrix</th><th>level matching</th></tr>
<tr><td>0</td><td>0</td><td>control via CCIR bit and FMT bits</td><td>bypass</td><td>control via FMT bits</td><td>control via CCIR bit</td></tr>
<tr><td>0</td><td>1</td><td>Format 5 (RGB) CCIR level</td><td>active, no indexed colour</td><td>active</td><td>CCIR level</td></tr>
<tr><td>1</td><td>X</td><td>Format 7 (indexed colour) CCIR level</td><td>active, indexed colour</td><td>active</td><td>CCIR level</td></tr>
</table></td></tr>
<tr><td>IEPI</td><td>Polarity of external PAL-ID signal (H/2 signal) from RTCI input (pin 57):
0 = not inverted; 1 = inverted</td></tr>
<tr><td>RTSC</td><td>Real-time select control:
0 = Real-time control HPLL increment is selected, that means, information about actual clock frequency from the digital colour decoder is received (SAA7151B or SAA7191B); the corresponding subcarrier frequency is calculated.
1 = Real-time control FSC increment with PAL-ID is selected, that means, information about actual subcarrier frequency and PAL-ID from the digital colour decoder is received (SAA7151B or SAA7191B).</td></tr>
<tr><td>RTIN</td><td>Select real-time control input:
0 = pin 57 is input for RTCI signal
1 = pin 57 is port output GPSW.</td></tr>
<tr><td>RTCE</td><td>Real-time control enabled: 0 = disabled; 1 = enabled (RTIN = 0)</td></tr>
<tr><td>Index "0C"
CHPS7 to CHPS0</td><td>Phase adjustment between chrominance output signal and reference:
00 to FF equals 0° to 358.59375° in steps of 1.40625°.</td></tr>
<tr><td>Index "0D"
FSC7 to FSC0</td><td>Fine adjustment of subcarrier frequency in non-GENLOCK modes:
00 to 7F increasing and FF to 80 decreasing equal approximately $\pm 450 \times 10^{-6}$ of the subcarrier frequency in 256 steps.</td></tr>
<tr><td>Index "0E"
CLCK</td><td>Lock to external chrominance (to be read): 0 = possible; 1 = not possible.</td></tr>
</table>

STD3 to STD0	Colour encoding standards:

STD3	STD2	STD1	STD0	standard
0	0	0	0	NTSC 4.43; 60 Hz; SQP (12.27 MHz)
0	0	0	1	NTSC 4.43; 50 Hz; SQP (14.75 MHz)
0	0	1	0	PAL-B/G 4.43; 50 Hz; SQP (14.75 MHz)
0	0	1	1	NTSC 4.43; 60 Hz; CCIR (13.5 MHz)
0	1	0	0	NTSC 4.43; 50 Hz; CCIR (13.5 MHz)
0	1	0	1	PAL-B/G 4.43; 50 Hz; CCIR (13.5 MHz)
0	1	1	0	reserved
0	1	1	1	reserved
1	0	0	0	PAL-M; 60 Hz; SQP (12.27 MHz)
1	0	0	1	PAL-M; 60 Hz; CCIR (13.5 MHz)
1	0	1	0	PAL-N; 50 Hz; CCIR (13.5 MHz)
1	0	1	1	PAL-N; 50 Hz; SQP (14.75 MHz)
1	1	0	0	NTSC-M; 60 Hz; SQP (12.27 MHz)
1	1	0	1	NTSC-M; 60 Hz; CCIR (13.5 MHz)
1	1	1	0	reserved
1	1	1	1	reserved

Status bits to be read via I²C-bus:	Table 7
Status bits to be read by microcontroller :	All registers from 00 up to 0F can be read via MPU-bus. Read-only bits are OEF, HCLK (index "04") and CLCK (index "0E")

Note to Table 6

Field blanking (Figures 11 and 12): normally, video to be encoded should not become active after the active edge of VSN or CSYN before line 22.5 at 50 Hz (line 18 at 60 Hz). Total internal field blanking is 11 lines at 50 Hz (13 lines at 60 Hz).

Colour look-up tables (CLUTs)

The CLUTs consist of RAM tables. The RAM tables can be loaded – with X = 0 to 255 according to equation 1 – for the signals R, G and B . Gamma-correction (pre-distortion) by following equation:

$$Y = \mathrm{NINT}(b + a \times X1^{1/g}); \quad Y(X \leq 16) = 16; \quad Y(X \geq 235) = 235 \quad \text{(equation 1)}$$

with g = 2.2 is

$$a = 219 / (235^{-2.2} - 16^{-2.2})$$

$$b = 16 - a \times 16^{-2.2}$$

The RAM tables are loaded via MPU-bus or via I²C-bus (Table 8).

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = **1011 000X**
A = acknowledge, generated by the slave
SUBADDRESS* = subadress byte (Table 8)
DATA = data byte (Table 5)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 7 I²C-bus status byte (address byte "B1")

FUNCTION		STATUS BYTE D7	D6	D5	D4	D3	D2	D1	D0
Read status		0	0	0	0	FFOS	OEF	CLCK	HLCK

Function of the bits:

FFOS — first field of sequence: 0 = false; 1 = first of 4 fields for NTSC (first of 8 fields for PAL). FFOS is not valid for non-interlaced signals.
OEF — field organization: 0 = even field; 1 = odd field
CLCK — possibility of lock to external chrominance: 0 = possible; 1 = not possible
HLCK — sync indication: 0 = locked to external sync; 1 = external sync lost.

Table 8 I²C-bus write bytes (address byte "B0")

ACCESS TO CONTROL REGISTERS Address byte "B0" — subaddress byte "02" — index byte (00 to 0F, Table 5) — data bytes (auto-increment)
ACCESS TO CLUTS REGISTERS Address byte "B0" — subaddress byte "00" — CLUT address bytes (00 to FF) — 3 data bytes for one RGB sequence (auto-increment)



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Table 9 Four different modes

STAND-ALONE MODE The SAA7199B receives a line-locked clock CLKIN and generates CSYN or HSN/VSN output signals, which trigger the RGB respectively the YUV source signal to provide data and composite blanking CBN.
SLAVE MODE The SAA7199B receives the line-locked clock CLKIN, CSYN or HSN/VSN, CBN and data from an RGB respectively YUV source. The sync inputs are edge-sensitive; the minimum active length is 1 PIXCLK. Optionally, a real-time control signal RTCI is received from a digital colour decoder.
GENLOCK MODE Horizontal and vertical sync as well as colour are locked on a received CVBS reference signal. The CVBS reference signal generates also a line-locked clock by the SAA7197 clock generator. Auxiliary signals HCL and HSY as well as CSYN or HSN/VSN are generated to trigger the RGB respectively the YUV source providing data and composite blanking CBN.
TEST MODE Like stand-alone mode, but data to be encoded are the contents of the test registers TRER, TREGand TREB. VSN/CSYN and HSN outputs are in 3-state condition.

Relationship between horizontal frequency and colour subcarrier frequency in non-GENLOCK mode

a) Internal subcarrier frequency with n = integer:

PAL: $f_{SC} = f_H (n/4 + 1/625)$ respectively $f_H (n/4 + 1/525)$ NTSC: $f_{SC} = f_H (n/2)$

Necessary conditions: Non-GENLOCK mode; RTCE = 0, FSCO = 00h; phase coupling of the two frequencies is given by definite phase reset every 8th fields at PAL (4th fields at NTSC).

FSCO ≠ 00h adjusts the subcarrier frequency, phase reset is disabled and phase between f_{SC} and f_H is not constant.

b) External subcarrier frequency:

f_{SC} is given by RTCI real-time input from a digital colour decoder.

Necessary conditions: Slave mode; RTCE = 1, RTSC = 1. The 8th respectively 4th field reset is enabled at FSCO = 00h (disabled at FSCO ≠ 00h). The subcarrier frequency itself is not influenced by FSCO bits, it is given by real-time increment.

c) External HPLL increment:

f_{SC} is calculated by means of RTCI real-time input signal from a digital colour decoder. The frequency of f_{SC} depends on the absolute crystal frequency value used by the digital colour decoder.

Necessary conditions: Slave mode; RTCE = 1, RTSC = 0. The 8th respectively 4th field reset is enabled at FSCO = 00h (disabled at FSCO ≠ 00). The subcarrier frequency itself is influenced by FSCO bits.

The absolute phase relationship between sync and subcarrier (colour burst out) can be influenced in all three cases by CHPS(7-0) register byte (index "0C").

Data input formats

One clock cycle equals 12.27 MHz, 13.5 MHz or 14.75 MHz (Cb = (B-Y) equals U; Cr = (R-Y) equals V; (n) = number of pixel).

Table 10 Format 0: DMSD2-compatible YUV 4:1:1 format (FMT-bits in index "00"= 000)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7)	Cb7(0)	Cb5(0)	Cb3(0)	Cb1(0)	Cb7(4)	Cb5(4)	Cb3(4)	Cb1(4)
PD3(6)	Cb6(0)	Cb4(0)	Cb2(0)	Cb0(0)	Cb6(4)	Cb4(4)	Cb2(4)	Cb0(4)
PD3(5)	Cr7(0)	Cr5(0)	Cr3(0)	Cr1(0)	Cr7(4)	Cr5(4)	Cr3(4)	Cr1(4)
PD3(4)	Cr6(0)	Cr4(0)	Cr2(0)	Cr0(0)	Cr6(4)	Cr4(4)	Cr2(4)	Cr0(4)
PD3(3-0)	not used							
PD1(7-0)	not used							

Table 11 Format 1: Customized YUV 4:1:1 format (FMT-bits in index "00" = 001)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7)	Cb7(0)	-	Cr7(0)	-	Cb7(4)	-	Cr7(4)	-
PD3(6)	Cb6(0)	-	Cr6(0)	-	Cb6(4)	-	Cr6(4)	-
PD3(5)	Cb5(0)	-	Cr5(0)	-	Cb5(4)	-	Cr5(4)	-
PD3(4)	Cb4(0)	-	Cr4(0)	-	Cb4(4)	-	Cr4(4)	-
PD3(3)	Cb3(0)	-	Cr3(0)	-	Cb3(4)	-	Cr3(4)	-
PD3(2)	Cb2(0)	-	Cr2(0)	-	Cb2(4)	-	Cr2(4)	-
PD3(1)	Cb1(0)	-	Cr1(0)	-	Cb1(4)	-	Cr1(4)	-
PD3(0)	Cb0(0)	-	Cr0(0)	-	Cb0(4)	-	Cr0(4)	-
PD1(7-0)	not used							

Table 12 Format 2: DMSD2-compatible YUV 4:2:2 format (FMT-bits in index "00" = 010)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7)	Cb7(0)	Cr7(0)	Cb7(2)	Cr7(2)	Cb7(4)	Cr7(4)	Cb7(6)	Cr7(6)
PD3(6)	Cb6(0)	Cr6(0)	Cb6(2)	Cr6(2)	Cb6(4)	Cr6(4)	Cb6(6)	Cr6(6)
PD3(5)	Cb5(0)	Cr5(0)	Cb5(2)	Cr5(2)	Cb5(4)	Cr5(4)	Cb5(6)	Cr5(6)
PD3(4)	Cb4(0)	Cr4(0)	Cb4(2)	Cr4(2)	Cb4(4)	Cr4(4)	Cb4(6)	Cr4(6)
PD3(3)	Cb3(0)	Cr3(0)	Cb3(2)	Cr3(2)	Cb3(4)	Cr3(4)	Cb3(6)	Cr3(6)
PD3(2)	Cb2(0)	Cr2(0)	Cb2(2)	Cr2(2)	Cb2(4)	Cr2(4)	Cb2(6)	Cr2(6)
PD3(1)	Cb1(0)	Cr1(0)	Cb1(2)	Cr1(2)	Cb1(4)	Cr1(4)	Cb1(6)	Cr1(6)
PD3(0)	Cb0(0)	Cr0(0)	Cb0(2)	Cr0(2)	Cb0(4)	Cr0(4)	Cb0(6)	Cr0(6)
PD1(7-0)	not used							

Table 13 Format 3: Customized YUV 4:2:2 format (FMT-bits in index "00" = 011)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7-0)	Cb (0)	-	Cb (2)	-	Cb (4)	-	Cb (6)	-
PD1(7-0)	Cr (0)	-	Cr (2)	-	Cr (4)	-	Cr (6)	-

Table 14 Format 4: YUV 4:4:4 format (FMT-bits in index "00" = 100)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7-0)	Cb (0)	Cb (1)	Cb (2)	Cb (3)	Cb (4)	Cb (5)	Cb (6)	Cb (7)
PD1(7-0)	Cr (0)	Cr (1)	Cr (2)	Cr (3)	Cr (4)	Cr (5)	Cr (6)	Cr (7)

Table 15 Format 5: RGB 4:4:4 format (FMT-bits in index "00" = 101)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD1(7-0)	R(0)	R(1)	R(2)	R(3)	R(4)	R(5)	R(6)	R(7)
PD2(7-0)	G(0)	G(1)	G(2)	G(3)	G(4)	G(5)	G(6)	G(7)
PD3(7-0)	B(0)	B(1)	B(2)	B(3)	B(4)	B(5)	B(6)	B(7)

Table 16 Format 7: Indexed colour format (FMT-bits in index "00" = 111). Input codes 0 to 255 are allowed, output code of CLUTs should preferably be the same as given in Format 5

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7-0)	INC(0)	INC(1)	INC(2)	INC(3)	INC(4)	INC(5)	INC(6)	INC(7)

Table 17 Input data levels for formats 0 to 4 and 5; EBU colour bar: 100 % white equals 100 IRE intensity; 75 % colour saturation for formats 1 to 4, 100 % for format 5

INPUT CHANNEL	LEVEL	DIGITAL LEVEL	CODE	CCIR-BIT	FORMAT
Y channel	0 IRE 100 IRE	12 230	offset binary	0	formats 0 to 4
Cb channel	bottom peak colourless top peak	–101 0 100	two's complement	0	formats 0 to 4
Cr channel	bottom peak colourless top peak	–106 0 105	two's complement	0	formats 0 to 4
Y channel	0 IRE 100 IRE	16 235	offset binary	1	formats 0 to 4
Cb channel	bottom peak colourless top peak	44 128 212	offset binary	1	formats 0 to 4
Cr channel	bottom peak colourless top peak	44 128 212	offset binary	1	formats 0 to 4
R, G and B	0 IRE 100 IRE	16 235	offset binary	1	format 5

GENLOCK input data

Table 18 Format 7: CVBS GENLOCK input data format has 8-bit word length. The input data come from an analog-to-digital converter (TDA8708) with gain-controlled and clamped CVBS or VBS signals

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
CVBS7 to CVBS0	CVBS(0)	CVBS(1)	CVBS(2)	CVBS(3)	CVBS(4)	CVBS(5)	CVBS(6)	CVBS(7)

CONDITIONS OF CVBS INPUT SIGNAL	TWO'S COMPLEMENT REPRESENTATION	
sync bottom	coresponding to binary code	–128
0 IRE (black)	coresponding to binary code	–64*
100 IRE (white)	coresponding to binary code	95
top peak of 75 % colour	coresponding to binary code	95
bottom peak of 75 % colour	coresponding to binary code	–100

* If exactly matched levels are wanted in the internal multiplexer, the value 0 IRE should correspond to –68 and 100 IRE to 82.

Encoding data levels

Input data levels are transformed in three stages:

- in the matrix when RGB or indexed colour is applied (formats 5 and 7)
- in the normalizing amplifier depending on 50/60 Hz mode and CCIR-bit (index "00")
- in the modulator

Table 19(a) Y and C output levels in **50 Hz** mode (PAL) for RGB input levels (100/100 colour bar)

SIGNAL	INPUT DATA			MATRIX OUTPUT DATA			NORMALIZER OUTPUT DATA			MODULATOR OUTPUT DATA	
	R	G	B	(R-Y)	Y	(B-Y)	V*	Y	U	Y	C**
white	235	235	235	128	235	128	0	421	0	421	0
yellow	235	235	16	146	210	16	29	387	−132	387	±135
cyan	16	235	235	16	170	166	−184	332	44	332	±189
green	16	235	16	34	145	54	−155	297	−87	297	±178
magenta	235	16	235	221	107	202	152	245	86	245	±175
red	235	16	16	240	82	90	183	211	−45	211	±188
blue	16	16	235	110	41	240	−30	154	131	154	±134
black	16	16	16	128	16	128	0	120	0	120	0
blanking	X	X	X	X	X	X	X	X	X	120	0
burst	X	X	X	X	X	X	45	X	−45	X	±63
top sync	X	X	X	X	X	X	X	X	X	0	X

Table 19(b) Y and C output levels in **60 Hz** mode (NTSC) for RGB input levels (100/100 colour bar)

SIGNAL	INPUT DATA			MATRIX OUTPUT DATA			NORMALIZER OUTPUT DATA			MODULATOR OUTPUT DATA	
	R	G	B	(R-Y)	Y	(B-Y)	V	Y	U	Y	C**
white	235	235	235	128	235	128	0	416	0	416	0
yellow	235	235	16	146	210	16	29	385	−132	385	±135
cyan	16	235	235	16	170	166	−184	335	44	335	±189
green	16	235	16	34	145	54	−155	303	−87	303	±178
magenta	235	16	235	221	107	202	152	256	86	256	±175
red	235	16	16	240	82	90	183	225	−45	225	±188
blue	16	16	235	110	41	240	−30	173	131	173	±134
black	16	16	16	128	16	128	0	142	0	142	0
blanking	X	X	X	X	X	X	X	X	X	120	0
burst	X	X	X	X	X	X	0	X	−64	X	±64
top sync	X	X	X	X	X	X	X	X	X	0	X

X = not defined; * the V component is inverted in the PAL line; ** the ± figures are peak values of the subcarrier signal.

Chrominance filtering in the encoder

1. Decimation for 4:4:4 formats input data (Formats 4, 5 and 7; Fig.4).
2. Interpolation for 4:1:1 input data into 4:2:2 data – also suitable to reduce the bandwidth of 4:2:2 data. This filter is controlled by SCBW-bit (SCWB = 1 means active).
3. Interpolation at 13.5 MHz for 4:2:2 input data into 4:4:4 data before modulating baseband signals onto the colour subcarrier. Figures 5, 6 and 7 show the overall transfer characteristics of chrominance in "standard bandwidth condition" (SCBW = 1). Figures 8 and 9 show the overall transfer characteristics of chrominance in "enhanced bandwidth condition" (SCBW = 0), which is not possible for 4:1:1 input data. The transfer curves are slightly different at 12.27 and 14.75 MHz.

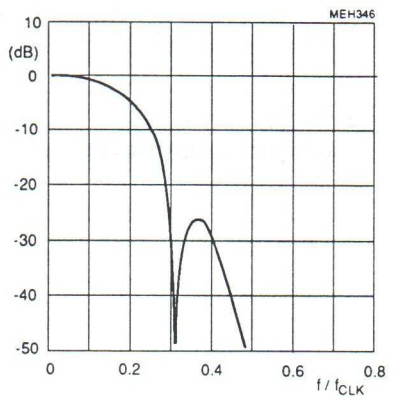


Fig.4 Transfer characteristics of 4:4:4 to 4:2:2 decimator.

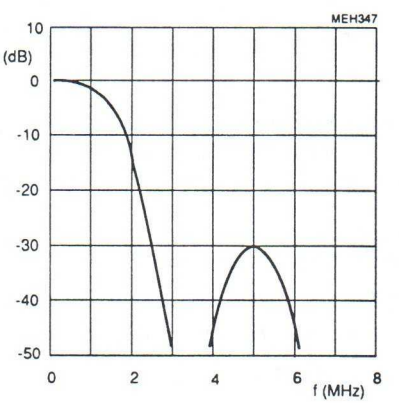


Fig.5 Overall transfer characteristics 4:1:1 input data.

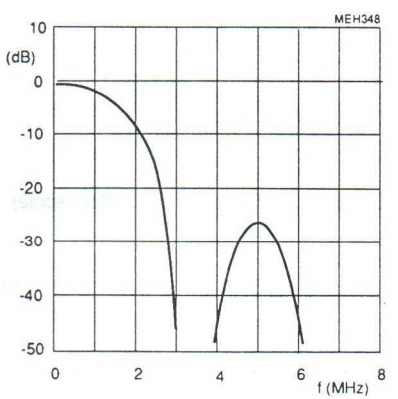


Fig.6 Overall transfer characteristics 4:2:2 input data (SCBW-bit = 1).

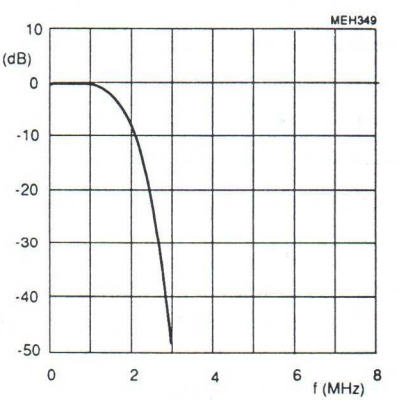


Fig.7 Overall transfer characteristics 4:4:4 input data (SCBW-bit = 1).

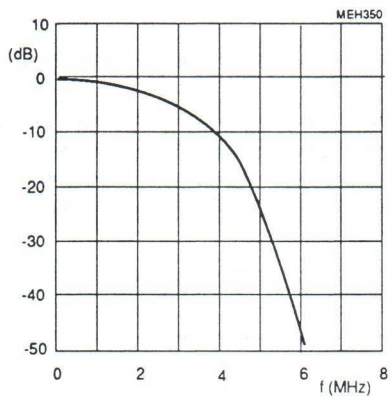


Fig.8 Overall transfer characteristics 4:2:2 input data (SCBW-bit = 0).

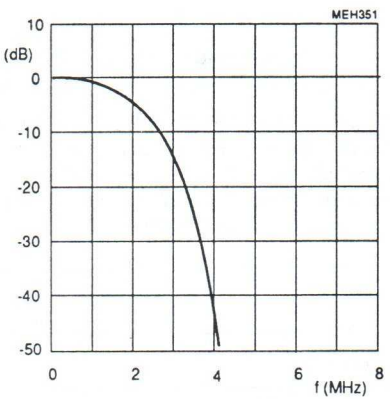


Fig.9 Overall transfer characteristics 4:4:4 input data (SCBW-bit = 0).

Accuracy of matrix

Evaluation of quantization errors.

The RGB to YUV matrix is realized according to the following algorithm:

Y = INT ((NINT(R x 2 x 0.299) + NINT(G x 2 x 0.587) +NINT(B x 2 x 0.114)) / 2)

U = NINT ((B-Y) x 0.57722)

V = NINT ((R-Y) x 0.72955)

Errors can occur in the calculation of Y, which in consequence influence the U and V outputs.
The greatest positive error occurs, if in all of the three for Y calculation used ROMs the values are rounded up to 0.5 LSB, and no truncation error of 0.5 LSB is generated after summation:

(3 x 0,5 LSB) / 2 = +0.75 LSB;
with truncation "error": (3 x 0,5 LSB) / 2 – 0.5 LSB = +0.25 LSB.

The greatest negative error occurs at rounding off in all the three ROMs and by consecutive truncation:

3 x (–0,5 LSB) / 2 – 0.5 LSB = –1.25 LSB.

As a result, the matrix error can be ±1 digit, which corresponds to approximately ±0.5% differential non-linearity.

Estimation of noise by quantization

The sum of all sqared quantization errors is SS normalized to 220^3 input combinations (3-dimensional colour scale).

SS = 0.187545 LSB^2.

Compared with noise energy for ideal quantization, SSI = 1/12 LSB^2 results in a deterioration by the conversion matrix of

D = 10 log (0.187545 x 12) = 3.5 dB (equals 0.5 bit).

If SS is the sum of all sqared quantization errors, normalized to 220 input combinations of a grey-scale (R = G = B), then is

SS = 0.12273 LSB^2.

Compared with noise energy for ideal quantization, SSI = 1/12 LSB^2 results in a deterioration by the conversion matrix of

D = 10 log (0.12273 x 12) = 1.7 dB (equals 0.25 bit).

Normalizing amplifiers in luminance channel

The absolute amplification error for 50 Hz non-set-up signals is 0.375 %; differential non-linearity is –0.333 % (equals –1 LSB).
The absolute amplification error for 60 Hz set-up signals is –1.5 %; differential non-linearity is –0.365 % (equals –1 LSB).

Normalizing amplifiers in chrominance channel

The absolute amplification error is approximately ±0.5 % with a truncation error of –0.5 LSB.

The subcarrier amplitude for standards with luminance set-up is the same as for the standards without luminance set-up.

Modulator

The absolute amplification error is –0.39 %; there is no truncation error.

Functional timing

GENLOCK mode:
The encoded signal can be generated earlier with respect to CVBS(7-0) bits (offset t_{ofs} set by GDC-bits; index "05"). The HSN output signal can be generated early by PSO-bits (index "07") with respect to CBN to compensate for pipelining delay t_{Rint} of the RAM interface (valid also in stand-alone mode).

The horizontal timing is independent of active video at data inputs PDn(7-0). The line blanking period on the outputs is set to approximately 12 µs in 50 Hz standards (11 µs in 60 Hz standards).

Slave mode:
HSN pin is used as an input. The active edge of the input signal is assumed to fit to the incoming CBN signal. Deviations can be compensated in the range of the GCD-bits (index "05").

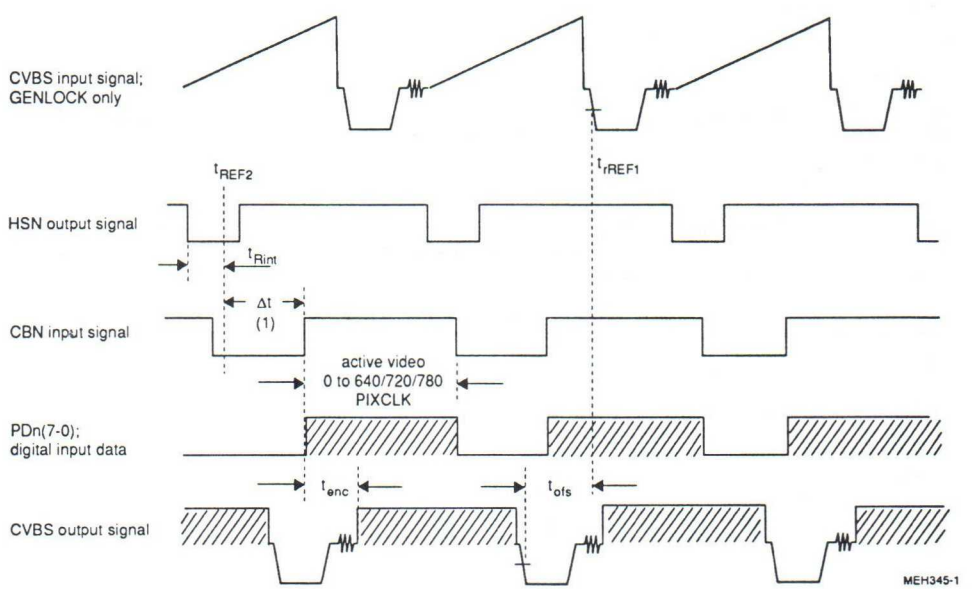


Fig.10 Horizontal timing. t_{Rint} = pipeline delay of RAM interface adjustable from –5 to +58 pixel clocks (PIXCLK); t_{ofs} = propagation delay of external GENLOCK line adjustable from –17 to +46 pixel clocks.

(1) Δt = 125 x PIXCLK at 12.27 MHz
Δt = 163 x PIXCLK at 14.75 MHz
Δt = 134 x PIXCLK at 13.50 MHz / 50 Hz mode
Δt = 122 x PIXCLK at 13.50 MHz / 60 Hz mode

The t_{enc} time is the total delay from data input to analog CVBS output; it is 55 pixel clock periods long (PIXCLK) plus the propagation delay of the LDV input register regardless of mode and colour standard.
The key input signal is delay-compensated with respect to PDn(7-0)data input.
The generated vertical field and burst blanking sequences are shown in Fig.11 (50 Hz PAL) and Fig.12 (60 Hz NTSC).

Reset

Prior to a reset all outputs are undefined. RESN = LOW sets the circuit into the slave mode: MOD1 bit = 1; MOD0-bit = 0. All other control register bits are set to zero. The outputs CSYN/VSN, HSN, SLT, HSY and HCL are automatically set to high-impedance state. The I^2C-bus interface is set to a slave receiver.
The D(7-0) pins of the MPU interface are inputs during RESN = LOW. As the circuit requires an external clock signal on pin CLKIN in slave mode, the clock select signal CLKSEL (pin 50) must be LOW during RESN = LOW (pin 54). The LOW time of RESN is preliminary at least 50 pixel clock periods long.

Disable chip

All analog outputs are set to zero by DD-bit = 1 (index "08"); while the outputs CSYN/VSN, HSN, HCL, HSY and SLT are set to high-impedance state. The internal clock is divided by 4 at DD-bit = 1.
The circuit can be disabled for any reason. It must be disabled when CLKIN exceeds 32 MHz. After setting DD-bit = 1, the CLKIN input signal can be set to a frequency of < 60 MHz (modification of control registers and RAM tables is not ensured).
To enable the circuit again, CLKIN must be set to a frequency < 32 MHz, a reset (hardware) then is required to set DD-bit to zero.

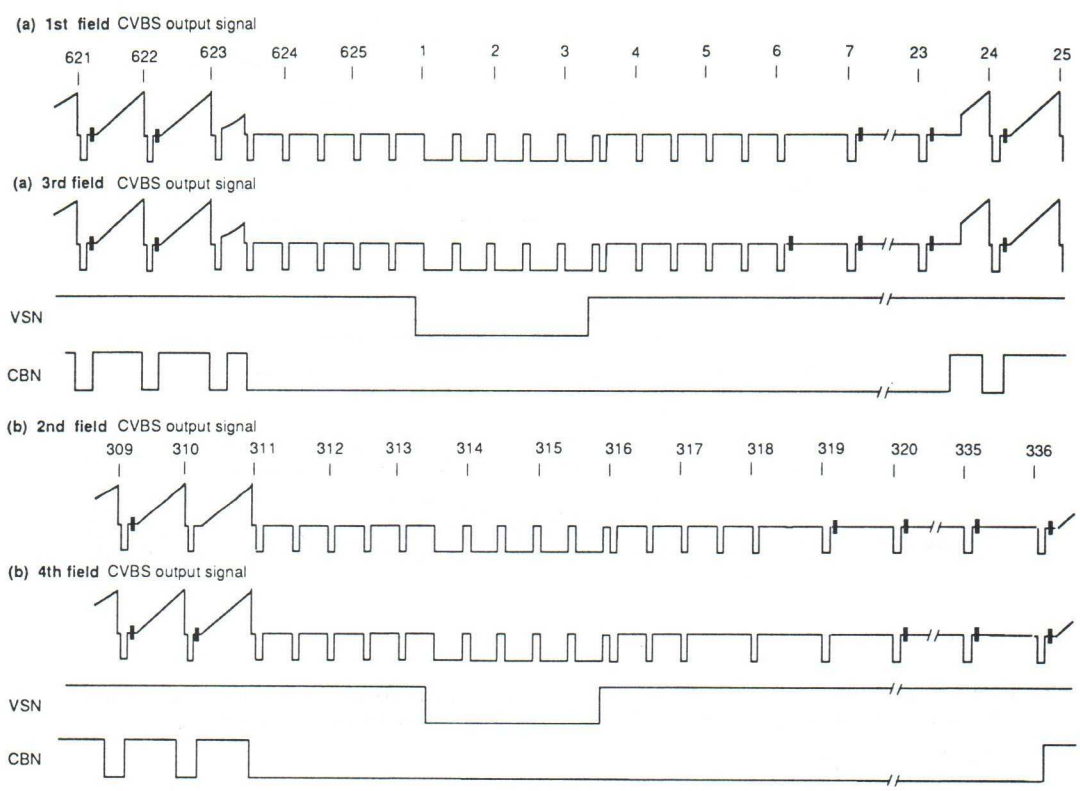


Fig.11 Vertical field and burst blanking sequence for PAL 50 Hz mode.

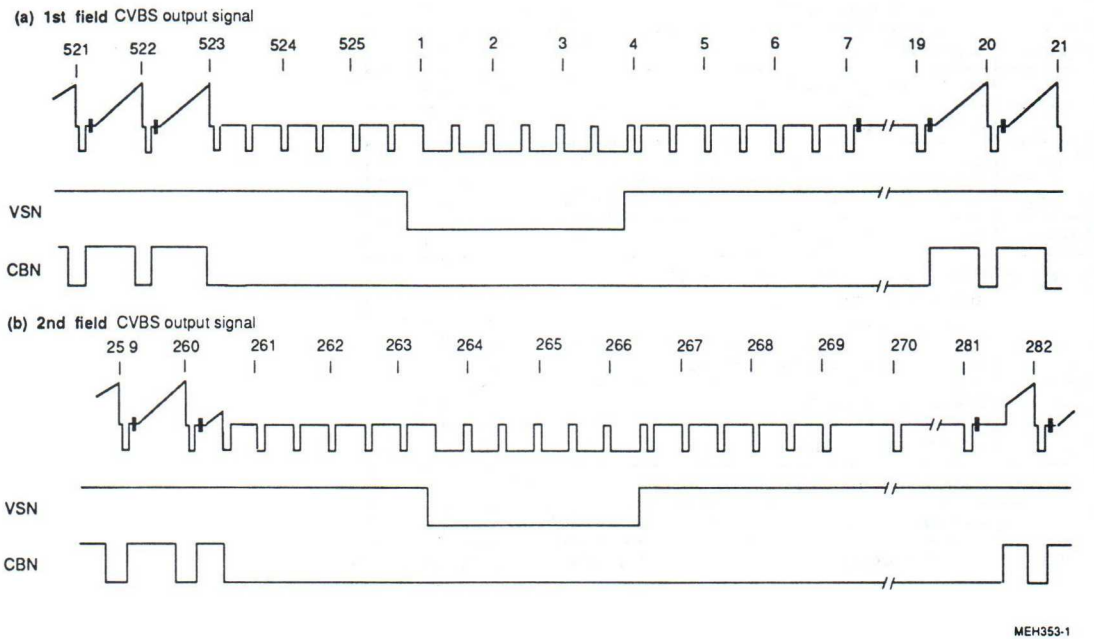


Fig.12 Vertical field and burst blanking sequence for NTSC 60 Hz mode.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD1}	supply voltage (pin 2)	–0.3	7	V
V_{DDD2}	supply voltage (pin 21)	–0.3	7	V
V_{DDD3}	supply voltage (pin 41)	–0.3	7	V
V_{DDA1}	supply voltage (pin 66)	–0.3	7	V
V_{DDA2}	supply voltage (pin 70)	–0.3	7	V
V_{DDA3}	supply voltage (pin 72)	–0.3	7	V
V_{DDA4}	supply voltage (pin 64)	–0.3	7	V
$V_{diff\ GND}$	difference voltage between digital and analog ground pins ($V_{DDDn} - V_{DDAn}$)	-	±100	mV
V_n	voltage on all pins, grounds excluded	0	V_P	V
P_{tot}	total power dissipation	-	1.1	W
T_{stg}	storage temperature range	–65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	±2000	-	V

* Equivalent to discharging a 100 pF capacitor through an 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage range (pins 2, 21 and 42)		4.5	5	5.5	V
V_{DDA}	analog supply voltage range (pins 66, 70 and 72)		4.75	5	5.25	V
I_{DDD}	digital supply current I_{DDD1} to I_{DDD3}	40 pF output load	-	-	140	mA
I_{DDA}	analog supply current I_{DDA1} to I_{DDA3}	40 pF output load	-	-	60	mA
Data and control inputs (pins 3 to 20, 23 to 40, 43 to 46, 49, 50, 54 to 56, 59, 73 and 76 to 84)						
V_{IL}	input voltage LOW	note 1	0	-	0.8	V
V_{IH}	input voltage HIGH	note 1	2.0	-	V_{DDD}+ 0.5	V
I_{LI}	input leakage current		-	-	±1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_I	input capacitance	data inputs	-	-	8	pF
		CLKIN, LLC, LDV	-	-	10	pF
		3-state I/O	-	-	10	pF
LFCO output (pin 61)						
V_o	output signal (peak-to-peak value)		1.4	-	2.6	V
V_{61}	output voltage range		0	-	V_{DDD}	V
Data and other control outputs (pins 3, 51, 52, 57, 58, 60, 74 and 75)						
V_{OL}	output voltage LOW	note 2	0	-	0.6	V
V_{OH}	output voltage HIGH	note 2	2.4	-	V_{DDD}	V
C, Y and CVBS analog outputs (pins 65, 67 and 69)						
V_o	output signal (peak-to-peak value)	without load; V_{DDA} = 5 V	-	2	-	V
$V_{65,67,69}$	minimum output voltage	without load; V_{DDA} = 5 V	-	0.2	-	V
	maximum output voltage	without load; V_{DDA} = 5 V	-	2.2	-	V
$R_{65,67,69}$	internal serial output resistance	not tested	18	25	35	Ω
$R_{L\ 65,67,69}$	output load resistance	recommendation	90	-	-	Ω
B	output signal bandwidth	-3 dB	10	-	-	MHz
ILE	LF integral linearity error	9-bit data	-	-	±1.0	LSB
DLE	LF differential linearity error	9-bit data	-	-	±0.5	LSB
I_{CUR}	input current (pin 71)	Fig.1; $R_{70\text{-}71}$ = 20 kΩ	-	300	-	µA
I²C-bus SDA and SCL (pins 47 and 48)						
V_{IL}	input voltage LOW		–0.5	-	1.5	V
V_{IH}	input voltage HIGH		3.0	-	V_{DDD}+0.5	V
I_I	input current	V_I = LOW or HIGH	-	-	±10	µA
V_{OL}	SDA output voltage (pin 47)	I_{47} = 3 mA	-	-	0.4	V
I_{47}	output current	during acknowledge	3	-	-	mA
Crystal oscillator		Fig.14				
f_n	nominal frequency	3rd harmonic; Table 1	-	24.576	-	MHz
		3rd harmonic; Table 1	-	26.8	-	MHz
$\Delta f / f_n$	permissible deviation f_n		-	50	-	10^{-6}
X1	crystal specification:					
	temperature range T_{amb}		0	-	70	°C
	load capacitance C_L		8	-	-	pF
	series resonance resistance R_S		-	40	80	Ω
	motional capacitance C_1		-	1.5±20%	-	fF
	parallel capacitance C_0		-	3.5±20%	-	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LLC and LDV timing (pins 55 and 20)		Fig.16				
t_{LLC}	cycle time	note 3	31.5	-	44.5	ns
t_{CH}	pulse width		40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
t_{LDV}	cycle time		63	-	89	ns
t_{SUL}	LDV set-up time		4	-	-	ns
t_{HDL}	LDV hold time		10	-	-	ns
PIXCLK and CLKO timing (pins 51 and 52)		Fig.16				
t_{DCK}	PIXCLK and CLKO delay time		-	-	25	ns
PD1(7-0), PD2(7-0), PD3(7-0), CBN, MPK, KEY and RTCI input timing (pins 4 to 19, 23 to 32, 57 and 73)						
t_{SUD}	input data set-up time	Fig.16	4	-	-	ns
t_{HDD}	input data hold time		6	-	-	ns
CVBS (7-0), VSN/CSYN and HSN timing (pins 76 to 83, 3 and 84)						
t_{SU}	input data set-up time	Fig.17	10	-	-	ns
t_{HD}	input data hold time		5	-	-	ns
CREF timing (pin 56)		Fig.17				
t_{SUC}	input set-up time		10	-	-	ns
t_{HDC}	input hold time		2	-	-	ns
MPU timing A1, A0, R/WN, CSN, D(7-0) (pins 33 to 36, 37 to 40 and 43 to 46); Fig.18						
t_{SA}	A1 and A0 address set-up time (pins 33, 34)		4	-	-	ns
t_{HA}	A1 and A0 address hold time		25	-	-	ns
t_{SR}	R/WN set-up time (pin 35)		4	-	-	ns
t_{HR}	R/WN hold time		25	-	-	ns
t_{CL} ,t_{CH}	CSN pulse width LOW and HIGH	note 4	95	-	-	ns
t_{SW}	data set-up time (D7 to D0)	write	80	-	-	ns
t_{HW}	data hold time (D7 to D0)	write	5	-	-	ns
t_{HDR}	data output hold time (D7 to D0)	read	5	-	-	ns
t_{ZR}	delay to driven ports (D7 to D0)	read	5	-	-	ns
t_{DR}	delay to ports valid (D7 to D0)	read; note 5	-	-	275	ns
t_{RZ}	port outputs disable time (D7 to D0)	read	-	-	25	ns
Output timing (pins 3, 74, 75 and 84)		Fig.17				
t_{OD}	output delay time	minimum clock period; note 6	-	20	40	ns

Notes to the characteristics

1. XTAL, XTALI and TP are not characterized with respect to levels; CLKO is characterized up to 32 MHz and PIXCLK up to 16 MHz
2. Levels are measured with load circuit. LFCO output with 10 kΩ in parallel to 15 pF and other outputs with 1.2 kΩ in parallel to 40 pF at 3V (TTL load).
3. t_{LLC} has to be in the range 63 to 89 ns at CREF = HIGH (pin 56); t_{LLC} = 16.5 ns is allowed only if the multiplexer clock is active.
4. $t_{PIXCLK(min)}$ + 5 ns.
5. 3 x ($t_{PIXCLK(min)}$ + 5 ns).
6. 40 ns at low supply voltage (4 V) and high temperature (70 °C).

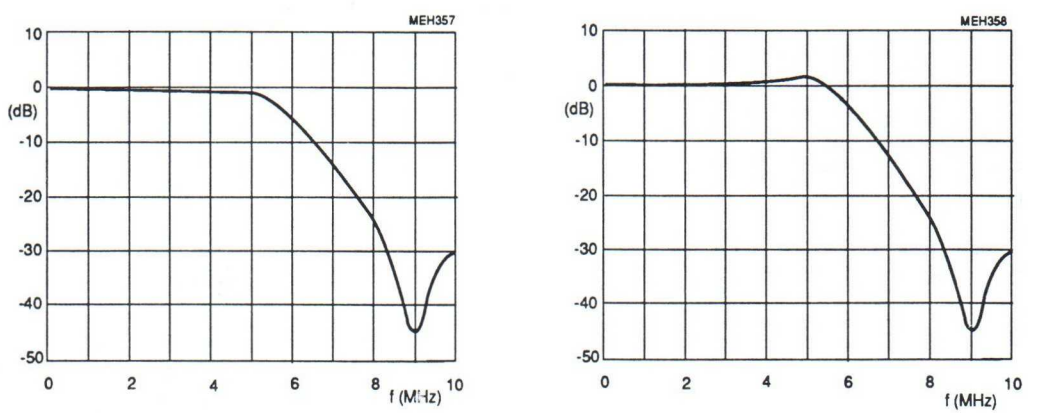


Fig.13 Characteristics of low-pass post-filters. Left: without compensation of DC hold characteristic. Right: with compensation of DC hold characteristic.

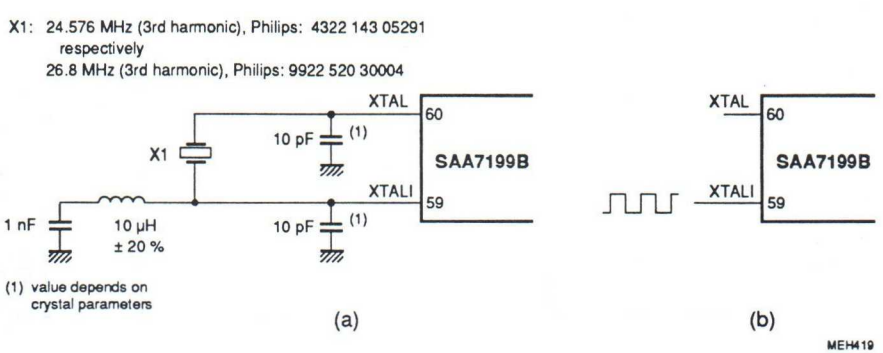
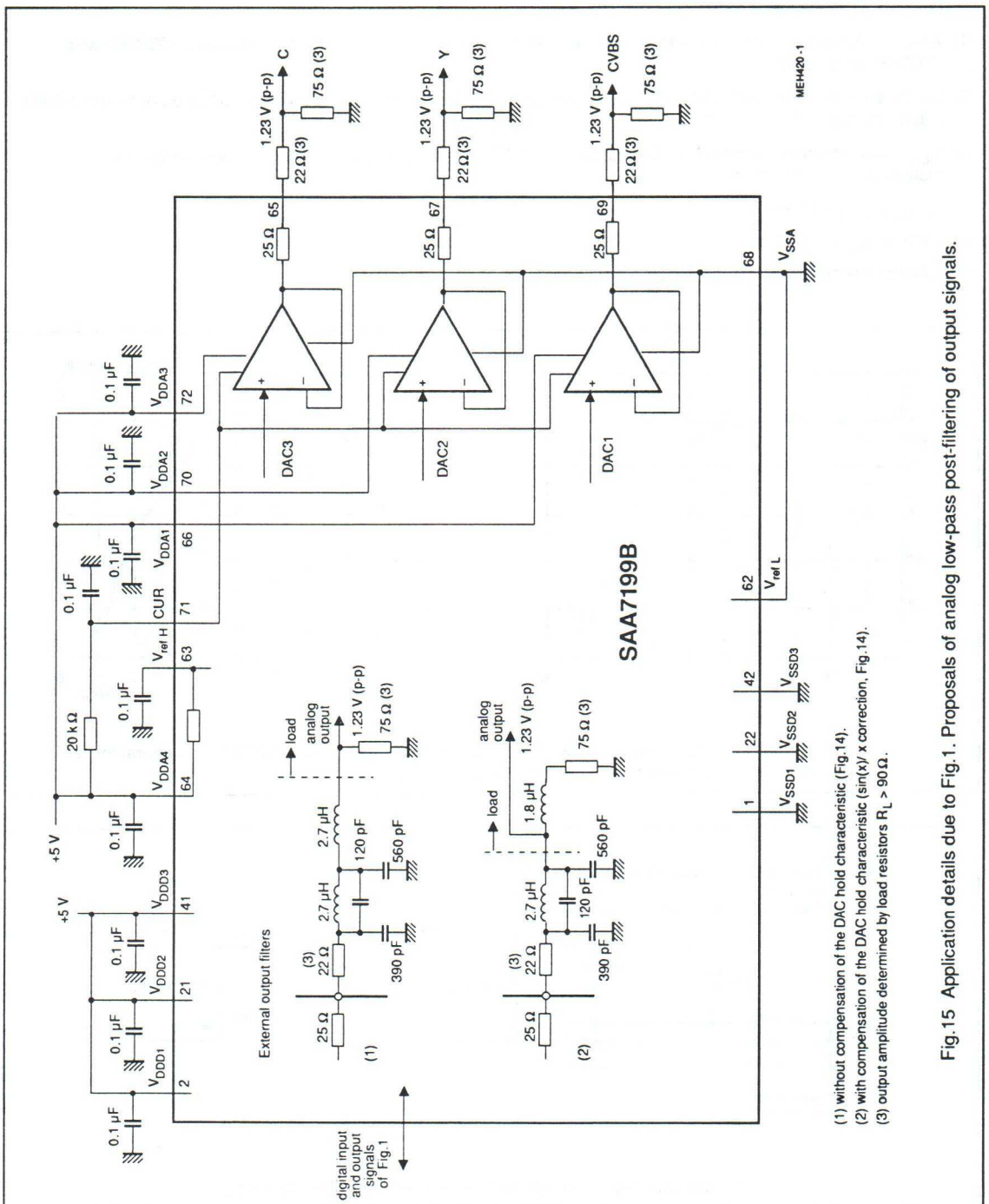


Fig.14 Oscillator application (a) and optional external clock sync (b).



(1) without compensation of the DAC hold characteristic (Fig.14).
(2) with compensation of the DAC hold characteristic ($\sin(x)/x$ correction, Fig.14).
(3) output amplitude determined by load resistors $R_L > 90\ \Omega$.

Fig.15 Application details due to Fig.1. Proposals of analog low-pass post-filtering of output signals.

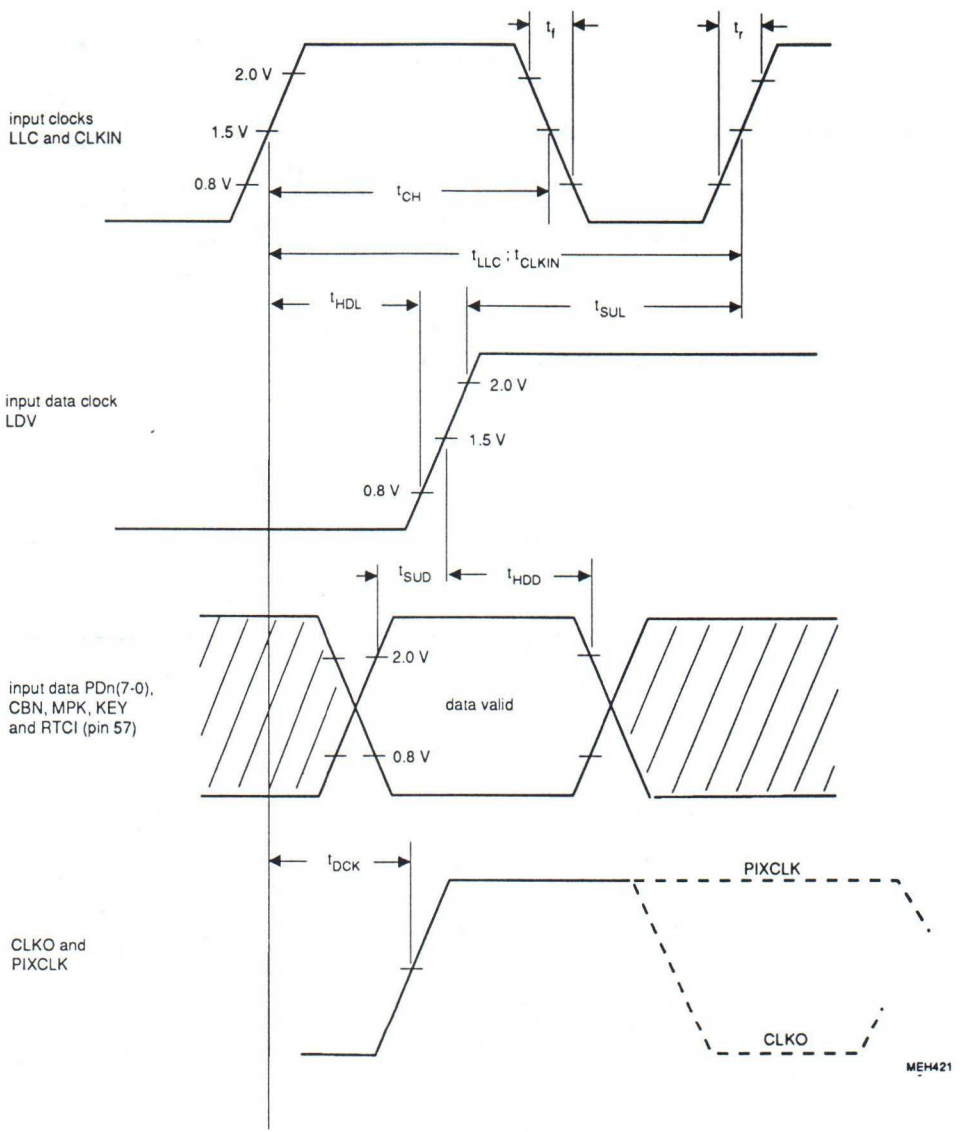


Fig.16 LDV input data timing.

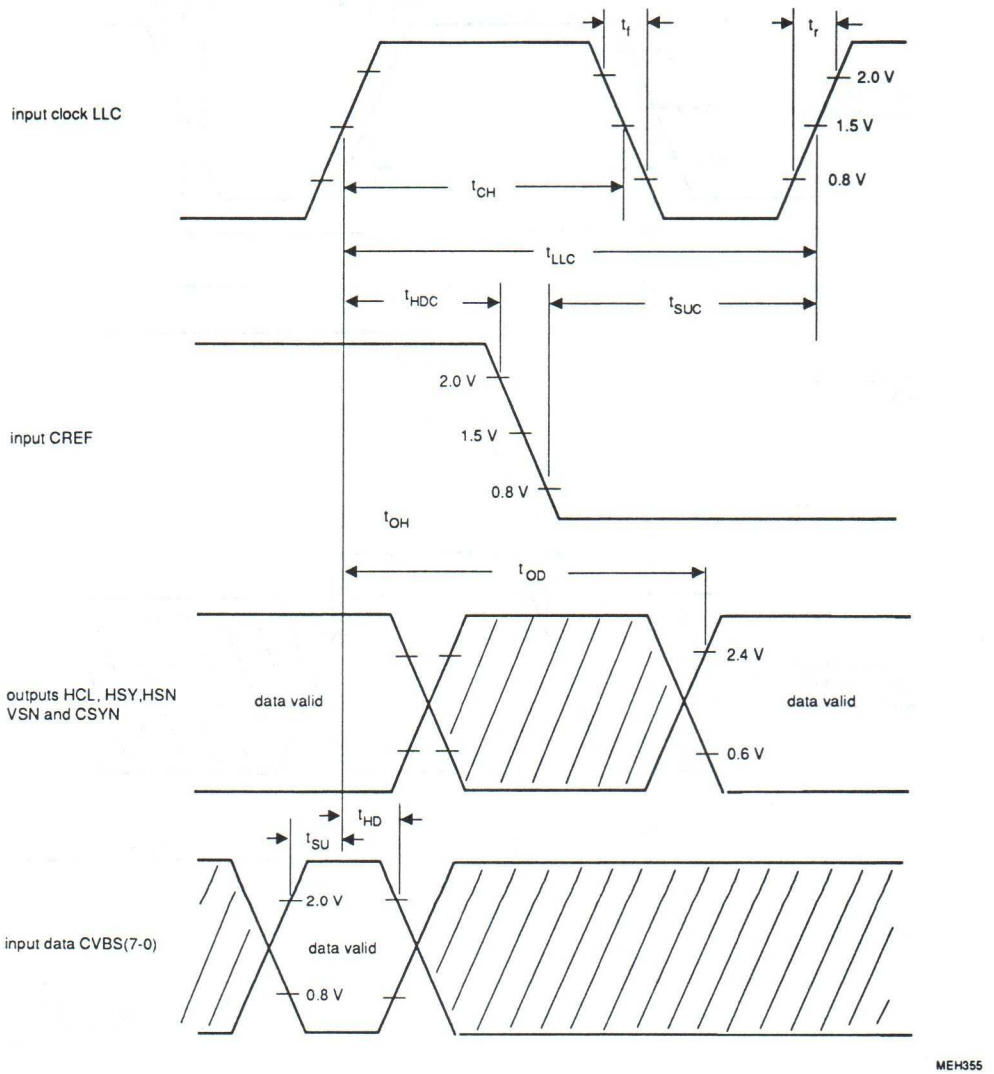


Fig.17 Clock and data timing.

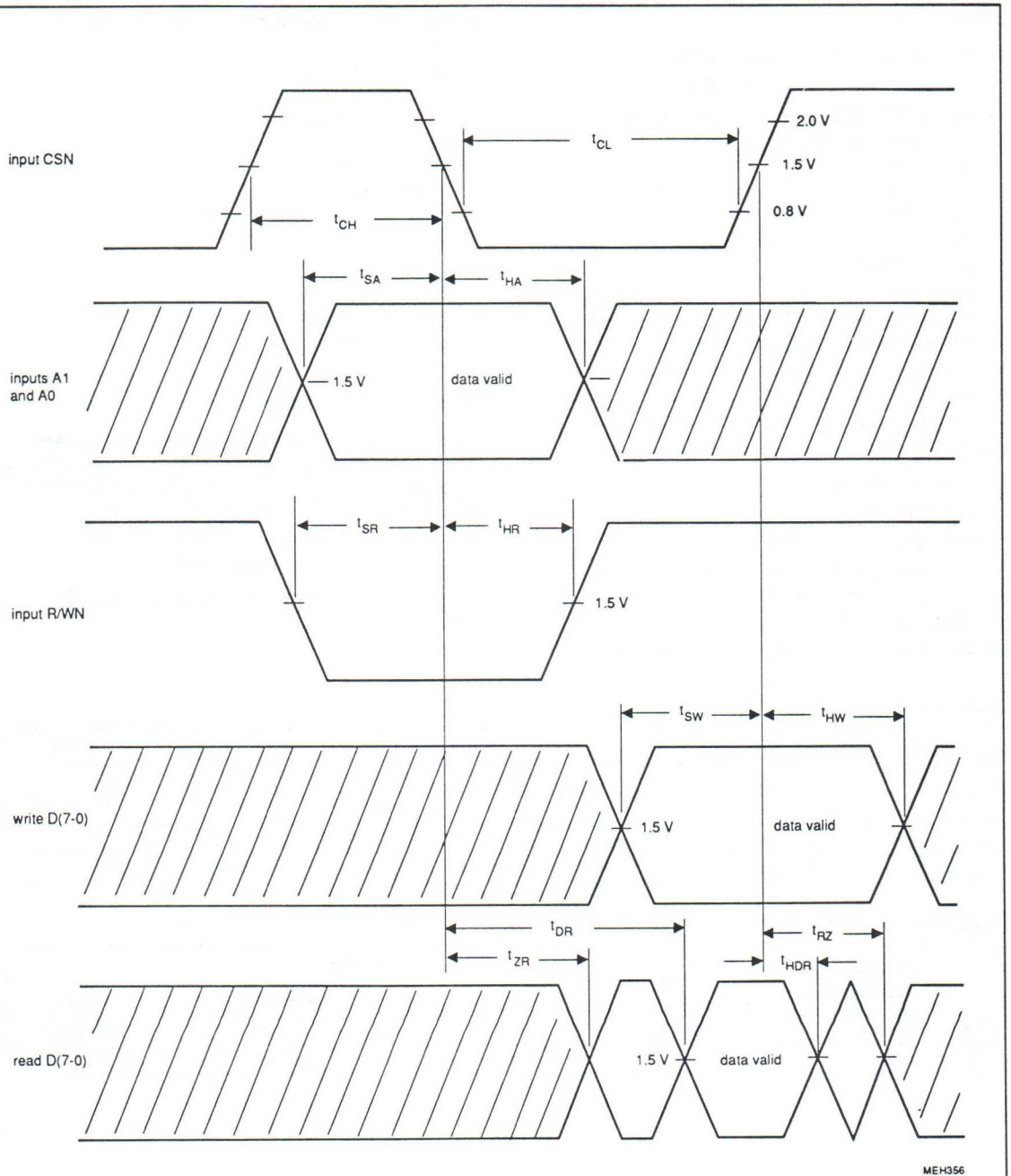


Fig.18 MPU-bus timing.

Terrestrial Digital Sound Decoder (TDSD2)

SAA7282

FEATURES

- Full EBU NICAM 728 specification decoder
- Microcomputer controlled via I²C-bus
- Automatic decoding and output configuration depending upon transmission:
  - digital stereo
  - digital mono and data
  - 2 independent mono signals
- On board RAM for de-interleaving and 10 to 14-bit word expansion
- Automatic mute function which silences the digital data and switches to FM sound (if valid) when error rate exceeds user definable limit
- User mute function ($\overline{\text{MUTE}}$ pin) to enable user to perform muting to their own software algorithm if required, or to simply silence the output
- 4 times over-sampling digital filter
- Selectable digital de-emphasis
- 256 times over-sampling Noise Shapers
- Fully integrated 1-bit DACs
- Integrated switching networks allowing selection between NICAM Sound, FM Sound or external "Daisy-Chain" input
- Digital Audio Interface conforming with EBU/IEC 958
- I²C-bus transceiver enabling a master device to read:
  - status information
  - error count byte
  - additional data bits

  and write:
  - switch control codes
  - decoder control
  - upper and lower error rate limits.

APPLICATIONS

- Television receivers
- Video cassette recorders.

GENERAL DESCRIPTION

Performing all digital decoding functions for a NICAM 728 digital stereo sound system, the SAA7282 is a highly integrated CMOS circuit which only requires a DQPSK (Differential Quadrature Phase Shift Keying) demodulator (TDA8732) and minimum external components to achieve a full NICAM solution.

The device may also be interfaced to other DQPSK demodulators.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	50	100	mA
f_{XTAL}	crystal frequency	–	8.192	–	MHz
T_{amb}	operating ambient temperature	0	–	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7282ZP	32	DIL32SHR	plastic	SOT232A
SAA7282GP	44	QFP	plastic	SOT205AG

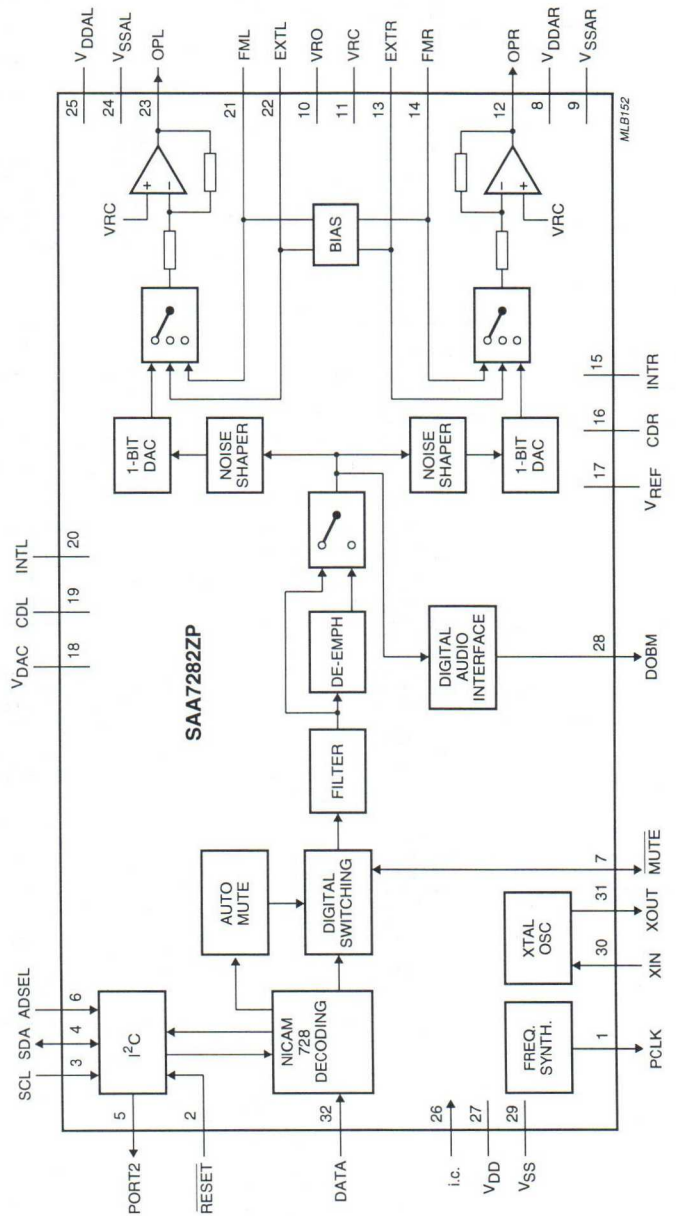


Fig.1 Block diagram; pin numbering for SOT232A.

PINNING

SYMBOL	SOT205AG	SOT232A	DESCRIPTION
DOBM	1	28	digital audio interface output
V_{SS}	2	29	ground connection for the digital section
n.c.	3	–	not connected
XIN	4	30	crystal input at 256fs (8.192 MHz)
XOUT	5	31	crystal output at 256fs (8.192 MHz)
DATA	6	32	serial data input at 728 kbits/s from DQPSK demodulator
PCLK	7	1	output clock at 728 kHz to DQPSK demodulator
$\overline{\text{RESET}}$	8	2	active LOW reset; used to set the device in a valid initial condition
SCL	9	3	clock input for I²C control bus
SDA	10	4	data port for I²C control bus, input/open drain output
PORT2	11	5	output mirroring the I²C control register bit PORT2
n.c.	12	–	not connected
ADSEL	13	6	I²C-bus slave address selection input; allows selection of one of two separate slave addresses, defaults to logic 1
$\overline{\text{MUTE}}$	14	7	active LOW mute input; when set LOW, sets the digital data to zero and either silences the output or switches it to analog FM, depending on the status of MUTEDEF (control bit in the I²C register) and RSSF; overriden by automute (if automute is used, then $\overline{\text{MUTE}}$ is automatically pulled LOW)
n.c.	15 to 17	–	not connected
V_{DDAR}	18	8	analog supply voltage for the right audio channel
V_{SSAR}	19	9	analog ground connection for the right audio channel
VRO	20	10	internal reference voltage buffer output
VRC	21	11	internal reference voltage buffer HIGH impedance node
n.c.	22	–	not connected
OPR	23	12	analog output from the right audio channel
EXTR	24	13	external analog input to the right audio channel
FMR	25	14	FM sound input to the right audio channel
INTR	26	15	integrator output from the right audio channel
CDR	27	16	integrator connection to an external damping capacitor
n.c.	28	–	not connected
V_{REF}	29	17	reference voltage input; 2.5 V (typical)
V_{DAC}	30	18	quiet V_{SS} to DACs
CDL	31	19	integrator connection to an external damping capacitor
INTL	32	20	integrator output from the left audio channel
FML	33	21	FM sound input to the left audio channel
EXTL	34	22	external analog input to the left audio channel
OPL	35	23	analog output from the left audio channel

SYMBOL	SOT205AG	SOT232A	DESCRIPTION
n.c.	36	–	not connected
V_{SSAL}	37	24	analog ground connection for the left audio channel
V_{DDAL}	38	25	analog supply voltage for the left audio channel
n.c.	39 to 41	–	not connected
i.c.	42	26	internally connected; must be left open-circuit in application
n.c.	43	–	not connected
V_{DD}	44	27	digital supply voltage

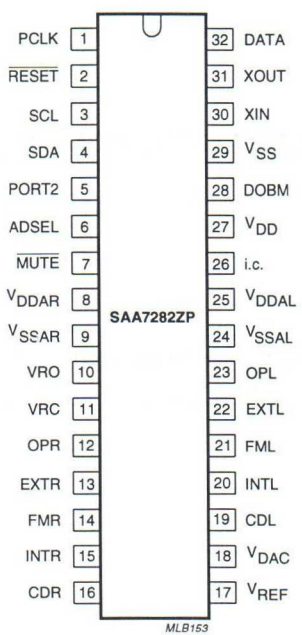


Fig.2 Pin configuration (SOT232A).

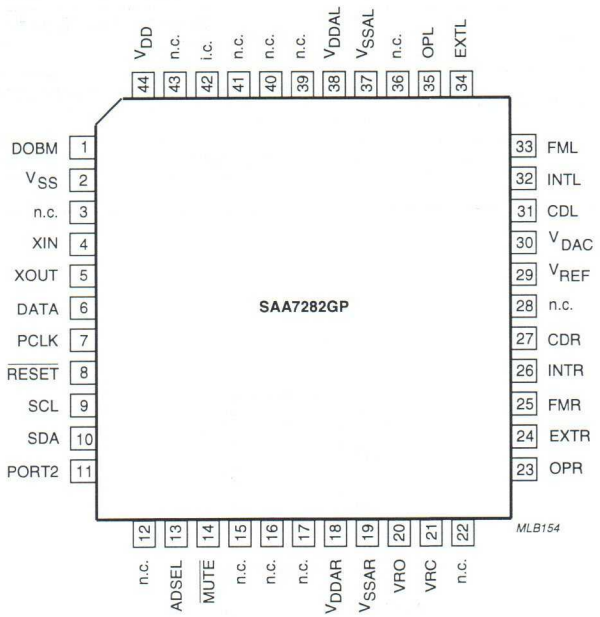


Fig.3 Pin configuration (SOT205AG).

I²C-BUS FORMATS

The SAA7282 contains an I²C-bus slave transceiver permitting a master device to:

- Read decoder status information derived from the transmitted digital audio signal
- Read an error count byte to determine the bit error rate for user mute purposes and to indicate quality of NICAM signal
- Read additional transmitted data bits. Their purpose has yet to be defined but accessibility is provided to allow future services to be implemented in receiver software
- Write control codes to select the available analog switching configurations
- Write upper and lower error count limits for automatic muting function

The device slave address is A(7:1)(R/$\overline{W}$) = 101101X(R/$\overline{W}$). An ADSEL pin is provided to allow selection of one of two different slave addresses via programmable address bit A1. (X = ADSEL logic level).

The SAA7282 does not acknowledge the I²C-bus general call address.

The slave receiver format is:

S SLAVE_ADDR.0 ACK SUB_ADDR ACK DATA BYTE ACK P

<–n bytes–>

Where S = start, ACK = acknowledge, P = stop.

Auto-increment of the sub-address is provided with wrap-around from 02 (HEX) to 00 (HEX).

The slave receiver data byte format, as a function of sub-address, is as shown in Table 1.

Table 1 Slave receiver data byte.

SUB-ADDRESS	RESET VALUE HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	90	M1/$\overline{M2}$	DMSEL	SSWIT3	SSWIT2	SSWIT1	PORT2	MUTEDEF	AMDIS
01	50	EMAX7	EMAX6	EMAX5	EMAX4	EMAX3	EMAX2	EMAX1	EMAX0
10	14	EMIN7	EMIN6	EMIN5	EMIN4	EMIN3	EMIN2	EMIN1	EMIN0

M1/$\overline{M2}$

This bit in conjunction with DMSEL bit, determines the output configuration in dual mono mode (see Table 2). Power-on resets to logic 1.

DMSEL

This bit determines whether one or both of the dual mono signals are output (see Table 2). Power-on resets to logic 0.

PORT2

PORT2 controls a bit out, providing direct access to a dedicated output pin (PORT2) via the I²C-bus. See Table 3. Power-on resets to logic 0.

SSWIT3/2/1

These bits control the analog switching, selecting between the FM, external, and NICAM signals. With the NICAM source the signals select whether the de-emphasis is performed and what gain is applied after the filtering and de-emphasis stage. The signal states and their meaning are listed in Table 4. Power-on resets to 0/1/0.

AMDIS

This bit enables and disables the automute function (which is activated according to the error limit registers). Power-on resets to enabled (i.e. AMDIS = logic 0). AMDIS should be disabled for the user definable mute ($\overline{\text{MUTE}}$) to be used.

MUTEDEF

This defines the operation of the user definable $\overline{\text{MUTE}}$ pin when it is pulled LOW externally. If MUTEDEF is HIGH and RSSF = logic 1, the output of the device is switched to FM input. If MUTEDEF is HIGH and RSSF = logic 0, or if MUTEDEF is LOW, the output is muted. Power on resets to LOW.

ERROR LIMIT REGISTERS

UPPER ERROR LIMIT REGISTER

This defines the number of errors in 128 ms period which will cause automute to switch IN. User definable, but power on resets to 50 Hex.

LOWER ERROR LIMIT REGISTER

This defines the number of errors in 128 ms period which will cause automute to switch OUT. User definable, but power on resets to 14 Hex.

Table 2 Output as a function of M1/$\overline{\text{M2}}$ and DMSEL.

DMSEL	M1/$\overline{\text{M2}}$	FUNCTION
0	0	selects DIGITAL; L = M2, R = M2
0	1	selects DIGITAL; L = M1, R = M1
1	0	selects DIGITAL; L = M2, R = M1
1	1	selects DIGITAL; L = M1, R = M2

Table 3 Port 2 control.

PORT2	PIN OUTPUT STATE
0	LOW
1	HIGH

Table 4 SSWIT signal states and function.

SSWIT3	SSWIT2	SSWIT1	FUNCTION
0	0	0	NICAM source de-emphasis switched out, no gain
0	0	1	NICAM source de-emphasis switched in, no gain
0	1	0	NICAM source de-emphasis switched in, +6 dB gain; power-on reset state
0	1	1	NICAM source de-emphasis switched in, +12 dB gain
1	x	0	external inputs switched in, no change to previous de-emphasis/gain setting
1	x	1	FM inputs switched in, no change to previous de-emphasis/gain setting

Note to Table 4

Where x = don't care.

Slave Transmitter

The slave transmitter formats are illustrated thus:

- S SLAVE_ADDR.1 A STATUS_BYTE NA P

In this format the bus master reads the STATUS_BYTE once.

- S SLAVE_ADDR.1 A STATUS_BYTE A ERROR_BYTE NA P

In this format the bus master reads two bytes of STATUS_BYTE and ERROR_BYTE.

- S SLAVE_ADDR.1 A STATUS_BYTE A ERROR_BYTE A AD_BYTE_0 A AD_BYTE_1 NA P

In this format the bus master reads four bytes of STATUS_BYTE, ERROR BYTE and two additional bytes, AD_BYTE_0 and AD_BYTE_1. The additional data bytes contain the eleven additional data bits AD0 to AD10 together with information regarding their status.

Where NA = no acknowledge.

Table 5 Data byte formats.

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
STATUS_BYTE	PONRES	S/$\overline{M}$	D/$\overline{S}$	VDSP	RSSF	$\overline{OS}$	AM	$\overline{CFC}$
ERROR_BYTE	E7	E6	E5	E4	E3	E2	E1	E0
AD_BYTE_0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
AD_BYTE_1	OVW	SAD	0	CI2	CI1	AD10	AD9	AD8

The bits may be defined as follows:

PONRES

This bit is a power-on reset detection bit. It is set HIGH after a power-on reset or supply reduction and is cleared LOW when the STATUS_BYTE is read.

S/$\overline{M}$ (stereo/mono indication)

S/$\overline{M}$ = logic 1 indicating an incoming stereo transmission.
S/$\overline{M}$ = logic 0 indicating that the incoming transmission is not stereo.

D/$\overline{S}$ (dual/single mono indication)

D/$\overline{S}$ = logic 1 indicating an incoming dual mono transmission.
D/$\overline{S}$ = logic 0 indicating that the incoming transmission is not dual mono.

VDSP

This bit indicates that the decoded signal is valid digital sound. When VDSP = logic 0 the incoming transmission carries either a 704 kbit/s transparent data channel or a currently undefined format and the device automatically switches to FM regardless of RSSF.

RSSF

RSSF is the reserve sound switching flag indication equal to the C4 bit in the NICAM transmission. RSSF = logic 1 when the FM sound signal is carrying the same programme material as the digitally modulated carrier (specifically the M1 signal in the event of a dual mono transmission). RSSF = logic 0 when the FM signal is not reproduced within the digital signal.

$\overline{OS}$

This bit provides an active LOW indication that the decoder is out of sync. If $\overline{OS}$ = logic 1 the decoder is frame synchronized and has obtained C0 (16 frame) sync. If $\overline{OS}$ = logic 0, the decoder is out of sync and the indicator bits are as given in Table 6.

AM

This bit indicates when the automuting function has switched from the NICAM sound to the conventional FM sound. This enables the software controller to display the relevant information to the customer, for example, on screen display. If AM bit = logic 0 no switching has been carried out by the automuting function. If AM bit = logic 1 then the automuting function has switched to the FM inputs.

$\overline{CFC}$

Signals a change of configuration at the 16-frame boundary. It is cleared to logic 1 by the I²C-bus reading the status register.

E7 to E0

This is an error count byte which counts the number of error flags in a 128 ms period. The register is updated every 128 ms.

AD10 to AD0

These are the additional data bits from the transmission and are updated every 1 ms. This provides a data capacity of 11 kbit/s.

SAD

SAD is the 'status additional data' bit. This is set to logic 1 when new bits AD10 to AD0 are latched into the I²C-bus registers. It is automatically reset to logic 0 when AD_BYTE_1 is read by the bus master.

OVW

OVW is the overwrite indicator for the additional data. This bit is set when the transmission overwrites additional data bits which have not been read by the bus master. This bit is automatically reset to logic 0 when AD_BYTE_1 is read by the bus master.

CI1 to CI2

These represent the CI bits which are extracted by a majority logic process from the parity checks of the last ten samples in a frame (samples 55 to 64). CI1 will be conveyed by the parity grouping of samples 55 to 59 and CI2 will be conducted by the parity grouping of samples 60 to 64. Both parity groups will be even for UK transmissions such that CI2 = logic 0 and CI1 = logic 0. The transmissions of countries following the specification issued by the EBU (Document SPB424; Digital sound transmissions in terrestrial television) will allow odd or even parity groups, thus providing an additional 2 kbit/s data capacity.

Table 6 Indicator bits functional truth table.

TRANSMISSION	C1	C2	C3	S/$\overline{M}$	D/$\overline{S}$	VDSP	$\overline{OS}$
Stereo	0	0	0	1	0	1	1
M1 + M2	0	1	0	0	1	1	1
M1 + data	1	0	0	0	0	1	1
Transparent data	1	1	0	0	0	0	1
Any currently undefined combination of C1, C2, C3				0	0	0	1
Decoder unsynchronized ($\overline{OS}$ = logic 0)				note 1	note 1	0	0

Note

1. Holds last value before synchronization loss or stereo (S/$\overline{M}$ = logic 1; D/$\overline{S}$ = logic 0) if synchronization not achieved since power-on reset.

DIGITAL AUDIO INTERFACE IEC/EBU 958

Block structure

The output is grouped into a block of 192 consecutive frames providing, for each channel the 192 channel status data bits. The start of a block is designated by a special sub-frame preamble.

Frame structure

Each frame is uniquely composed of two sub-frames. The rate of transmission of frames corresponds exactly to the source sampling frequency. In the 2-channel operation, samples taken from both channels are transmitted by time multiplexing in consecutive sub-frames. Sub-frames related to Channel 1 (left or 'A' channel in stereophonic operation and primary channel in monophonic operation) normally use preamble M. However the preamble is changed to preamble B once every 192 frames. This defines the block structure used to organize the channel status information. Sub-frames of Channel 2 (right or 'B' channel in stereophonic operation and secondary channel in monophonic operation) always use preamble W.

Sub-frame structure

Each frame is divided into 32 time-slots numbered 0 to 31.

Time-slots 0 to 3 carry one of three permitted preambles. These are used to affect synchronization of sub-frames, frames and blocks.

Time-slots 4 to 27 carry the audio sample word in linear two's complement representation. The most significant bit is carried by time-slot 27.

Time-slot 28 carries the validity flag associated with the audio sample word. This flag is set to logic 0 if the audio sample is reliable. If set to logic 1 then the sample is unreliable.

Time-slot 29 carries one bit of the user data channel. In this application this is not used and so is set to logic 0.

Time-slot 30 carries one bit of the channel status word associated with the audio channel transmitted in the same sub-frame.

Time-slot 31 carries a parity bit such that time-slots 4 to 31 inclusive will carry an even number of ones and an even number of zeros.

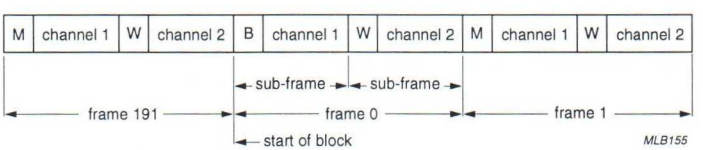


Fig.4 Frame format.

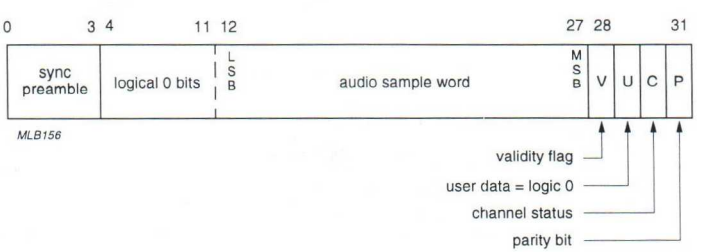


Fig.5 Sub-frame format.

Channel coding

Time-slots are encoded as biphase mark data. Each bit transmitted is represented by a symbol comprising two consecutive binary states. The first state of a symbol is always different from the second state of the previous symbol. The second state of the symbol is identical to the first if the bit being transmitted is logic 0, however it is different if the bit is logic 1 (see Table 7).

Table 7 Channel coding.

Preceding state	0	1
Transmitted bit	Channel coding	
0	11	00
1	10	01

Preambles

Preambles are specific patterns providing synchronization and identification of the sub-frames and blocks.

A set of three preambles is used. These preambles are transmitted in the time allocated to four time-slots and are represented by eight succesive states. The first state of the preamble is always different from the second state of the previous symbol. Depending on this state the preambles are as shown in Table 8.

Table 8 Preambles.

Preceding state	0	1
Preamble	Channel coding	
B	11101000	00010111
M	11100010	00011101
W	11100100	00011011

The preambles preceding each digital audio sample are used to indicate the beginning of a sample as follows:

- **Preamble B** indicates the start of Channel A data and the beginning of a block
- **Preamble M** indicates the start of Channel A data but not the beginning of a block
- **Preamble W** indicates the start of Channel B data.

Channel status

The channel status information is organized in 192-bit words. The first bit of each word is carried in the frame with Preamble B. The 192-bit word is organized into sections as shown in Table 9.

Table 9 Channel status codes.

BIT	CODE	DESCRIPTION
0	0	consumer
1	0	sound data
2	1	digital copy permitted
3, 4	00	indicates digital de-emphasis switched in
	11	indicates digital de-emphasis switched out
5	0	
6, 7	00	
8 to 15	00110001	category code
16 to 19	0000	source code (don't care)
20 to 23	0000	channel number (don't care)
24 to 27	1100	sampling frequency (32 kHz)
28, 29	00	clock accuracy (level II)
30 to 191	all 0s	

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	note 1	−0.5	+6.5	V
$V_{I(max)}$	maximum input voltage (any input)		−0.5	V_{DD}+0.5	V
$V_{O(max)}$	maximum output voltage		−0.3	V_{DD}+0.5	V
I_{IOK}	DC input or output diode current		–	±20	mA
$I_{O(max)}$	output current (each output)		–	±10	mA
T_{amb}	ambient operating temperature		0	+70	°C
T_{stg}	storage temperature		−55	+125	°C
V_{stat}	electrostatic handling	notes 2 and 3	−2000	+2000	V

Notes

1. All V_{DD} and V_{SS} connections must be made externally to the same power supply.
2. Electrostatic handling is equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a 15 ns rise time.
3. 1000 V V_{SSAL} pin.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage	see Fig.9	4.5	5.0	5.5	V
I_{DD}	total supply current		–	50	100	mA
V_{SS}, V_{SSAL}, V_{SSAR}, V_{DAC}	ground supply voltage		0	–	0	V
V_{DDAL}, V_{DDAR}	analog supply voltage	see Fig.9	4.5	5.0	5.5	V
Digital inputs						
DATA						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
I_{LI}	input leakage current		−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
ADSEL (this pin is internally pulled HIGH when not connected)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
Z_I	input impedance		–	50	–	kΩ
C_I	input capacitance		–	–	10	pF
$\overline{\text{RESET}}$ (Schmitt trigger input)						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}	V
V_{hys}	hysteresis		$0.05V_{DD}$	–	–	V
SCL						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}	V
V_{hys}	hysteresis		$0.05V_{DD}$	–	–	V
I_{LI}	input leakage current		−10	–	+10	µA
C_I	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital input/output						
SDA						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}	V
V_{hys}	hysteresis		$0.05V_{DD}$	–	–	V
I_{LI}	input leakage current		–10	–	+10	μA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.4	V
C_L	load capacitance					
	active pull-up		–	–	400	pF
	passive pull-up		–	–	200	pF
MUTE I/O (this pin has an internal pull-up)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 2.8 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage		2.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
Z_I	input impedance		–	50	–	kΩ
Digital outputs						
PORT2, PCLK, DOBM						
V_{OL}	LOW level output voltage	I_{OL} = 2.8 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = 800 μA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
Crystal oscillator						
f_c	crystal frequency		–	8.192	–	MHz
gm	mutual conductance	at 100 kHz	1.5	-	–	mA/V
Av	small signal gain	Av = gm.Ro	3.5	–	-	V/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		-	–	5	pF
C_O	output capacitance		-	–	10	pF
XIN						
V_{IL}	LOW level input voltage		0	–	1	V
V_{IH}	HIGH level input voltage		3.5	–	V_{DD}	V
I_{LI}	input leakage current		–10	–	+10	μA
C_I	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital filter specification						
f_s	output sample frequency		–	128	–	kHz
PR	pass band ripple	at 0 Hz to 15 kHz	–	–	±0.01	dB
SBA	stop band attenuation	at f ≥17 kHz	30	–	–	dB
Digital de-emphasis						
DEV	deviation from ideal		–	–	±0.09	dB
ANALOG SECTION (measured at V_{DD} = 5 V and T_{amb} = 25 °C)						
Reference voltage buffer						
VRC output						
V_{rc}	voltage reference at VRC	see Fig.10	$0.45V_{DDAR}$	$0.5V_{DDAR}$	$0.55V_{DDAR}$	V
DACs						
V_{REF} input						
V_{ref}	reference input voltage		–	$0.5V_{DD}$	–	V
Switching operational amplifiers						
C_L	output load capacitance		–	–	300	pF
R_L	output load resistance		3	–	–	kΩ
Z_O	output impedance		–	150	–	Ω
G	output gain		–0.35	0	+0.35	dB
PSRR	power supply rejection ratio		–	40	–	dB
External inputs selected (FML, FMR, EXTL, EXTR)						
V_{ain}	input voltage level (RMS value)		–	–	1.1	V
S/N	signal-to-noise ratio (relative to 1 V RMS, unity gain)	FM or EXT	90	100	–	dB
THD	total harmonic distortion (unity gain, O/P = 1 V RMS)	FM or EXT	–	–90	–70	dB
CHM	channel matching	FM or EXT, 1 kHz	–	0	0.5	dB
NICAM inputs selected (INTL, INTR)						
V_{ain}	input voltage level (RMS value)	at 0 dB; V_{REF} = 2.5 V	0.9	1.0	1.1	V
THD+N	total harmonic distortion plus noise	NICAM 728; notes 2 and 3	–	–80	–75	dB
CHM	channel matching	0 dB, 1 kHz	–	0	0.5	dB
DIGS	digital silence level	$\overline{\text{MUTE}}$ on	–	–80	–	dB
Timing (all timing values refer to V_{IH} and V_{IL} levels)						
DATA with respect to PCLK (see Fig.7)						
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		250	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SDA with repect to SCL (see Fig.8)						
f_{SCL}	SCL clock frequency		0	–	400	kHz
t_{BUF}	bus free time		1300	–	–	ns
$t_{HD;STA}$	start code hold time		600	–	–	ns
t_{LOW}	SCL clock LOW time		1300	–	–	ns
t_{HIGH}	SCL clock HIGH time		600	–	–	ns
$t_{SU;STA}$	start code set-up time		600	–	–	ns
$t_{HD;DAT}$	data hold time	note 4	0	–	–	ns
$t_{SU;DAT}$	data set-up time	note 5	100	–	–	ns
t_r	SDA and SCL rise time		50	–	300	ns
t_f	SDA and SCL fall time		50	–	300	ns
$t_{SU;STO}$	stop code set-up time		600	–	–	ns
t_{of}	output fall time	note 6	50	–	200	ns

Notes

1. Outputs OPL and OPR are measured with external components as recommended in Fig.11.
2. Total analog performance is limited by dynamic range of the NICAM 728 system. Due to compansion the quantization noise is never lower than approximately –62 dB with respect to the input level.
3. Measured with a –30 dB, 1 kHz NICAM 728 input signal.
4. Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.
5. If a fast I²C-bus device is used in an up to 100 kbit/s I²C-bus system, then the requirement $t_{SU;DAT} \geq 250$ ns is always fulfilled if this device cannot stretch the LOW level of the SCL signal. If a device stretches the LOW level of the SCL signal, then data to SDA must be asserted ($t_{RD(max)} + t_{SU;DAT}$) = 1000 + 250 = 1250 ns before the SCL signal is released to be compatible with the up to 100 kbit/s I²C-bus specification.
6. The output fall time is measured between 3.0 V and 1.5 V for a bus capacitance of 400 pF and an active pull-up.

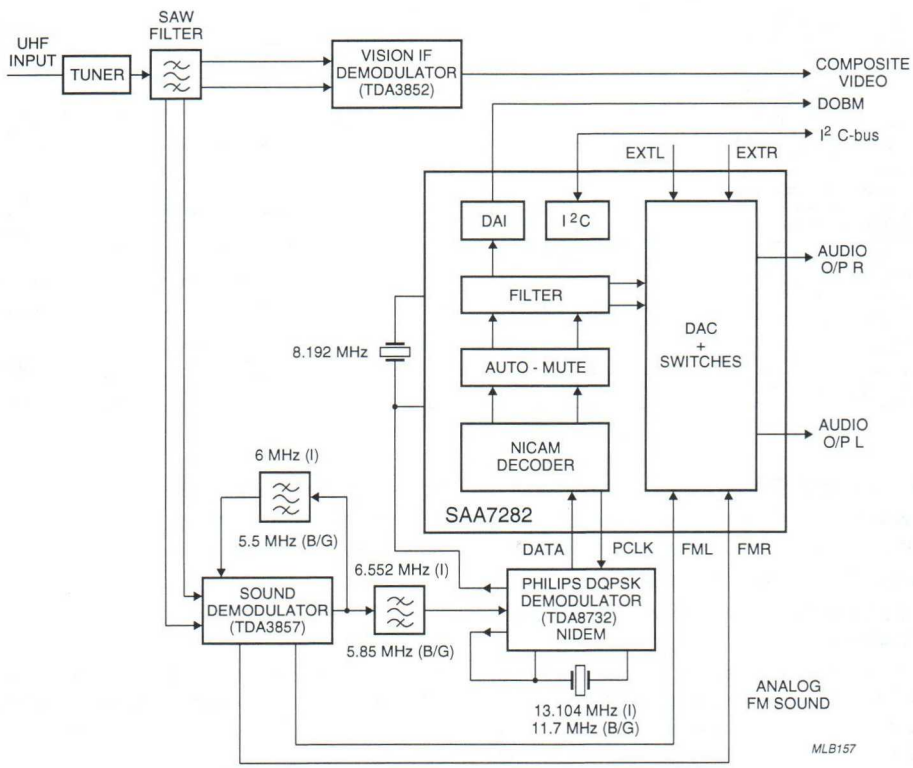


Fig.6 System block diagram showing SAA7282 with TDA8732.

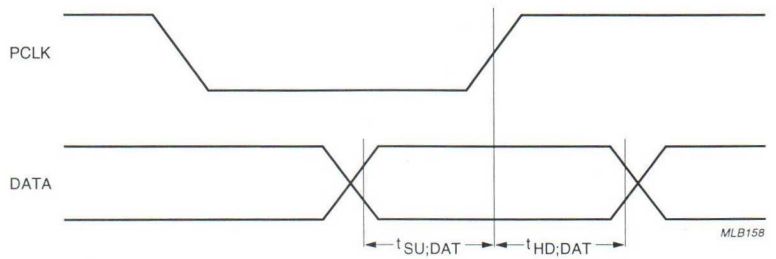


Fig.7 Data output timing.

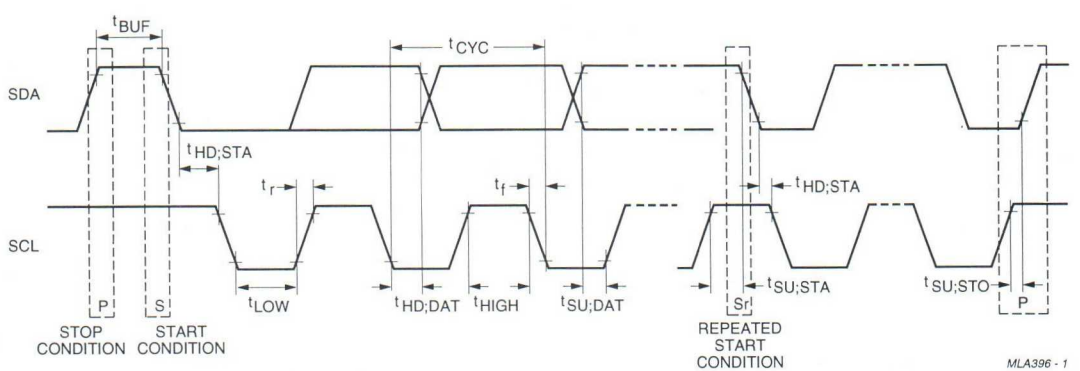


Fig.8 I²C-bus interface timing.

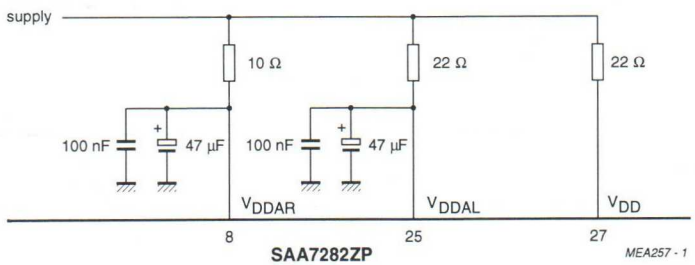


Fig.9 V_{DD} external circuitry.

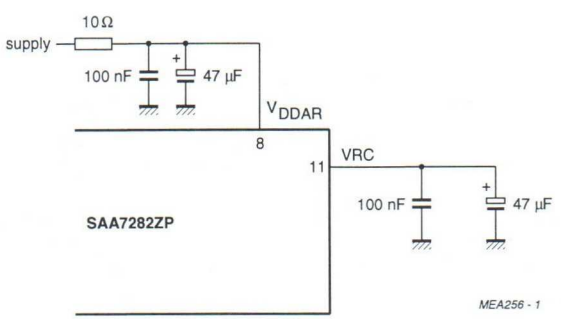


Fig.10 VRC external circuitry (same external circuit values also required for VRO).

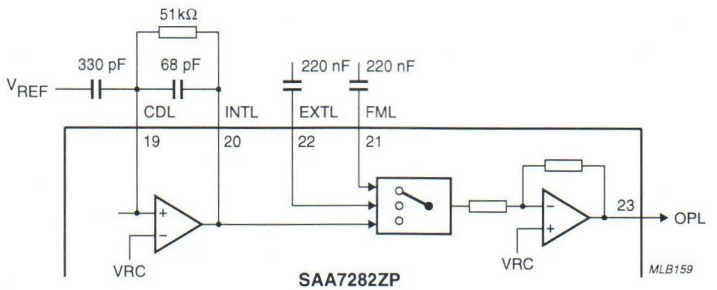


Fig.11 External circuitry for left channel DAC (same external circuit values also required for right channel DAC).

Multi-standard Teletext IC for standard and features TV

SAA9042

FEATURES

General

- Interfaces with analog and digital TV systems
- Multi-media compatible
- Directly interfaces up to 1 Mbit dynamic RAM
- Fully independent acquisition and display timing
- 3 display modes
  - normal (1H/1V)
  - progressive scan (2H/1V)
  - 100 Hz/120 Hz (2H/2V)
- I²C-bus controlled
- Single 5 V power supply.

Acquisition

- Simultaneous update of up to 8 pages
- Up to 100 page background memory capability
- Software selectable 625/525 line operation
- Full Level-One Features (FLOF) operation
- Table Of Pages (TOP) compatible
- VCR Programming via Teletext (VPT) and Program Delivery Control (PDC) compatible
- Vertical Blanking Interval (VBI) and full channel operation
- Extension packets 26/27/28/29 and 30 fully decoded.

Display

- Stable display by slaving from scan-related timing signals
- Automatic selection of six different languages
- Versions for Western and Eastern Europe and Turkey
- Storage of 192 characters (13 × 10 dot matrix)
- Software controlled RGB level removes the need for hardware adjustment
- Up to 27 display rows; 0 to 24 and up to 2 status rows.

GENERAL DESCRIPTION

The SAA9042 is a CMOS integrated circuit designed for reception, decoding and display of 625 and 525 line World System Teletext (WST).

It is used in conjunction with a teletext video processor (SAA5191) for data regeneration, and a single-chip 64K × 4-bit or 256K × 4-bit dynamic RAM page memory.

The SAA9042 acquires teletext packets defined at levels 1, 2 and 3 in the WST specification and produces a level 1 display.

The device is microcontroller controlled via the standard I²C-bus and is compatible with analog, digital and features TV.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DD}	supply current		–	100	–	mA
f_{clk}	clock frequency	625 line	–	6.9375	–	MHz
		525 line	–	5.7272	–	MHz
T_{amb}	operating ambient temperature		−20	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9042	40	DIL	plastic	SOT129

BLOCK DIAGRAM

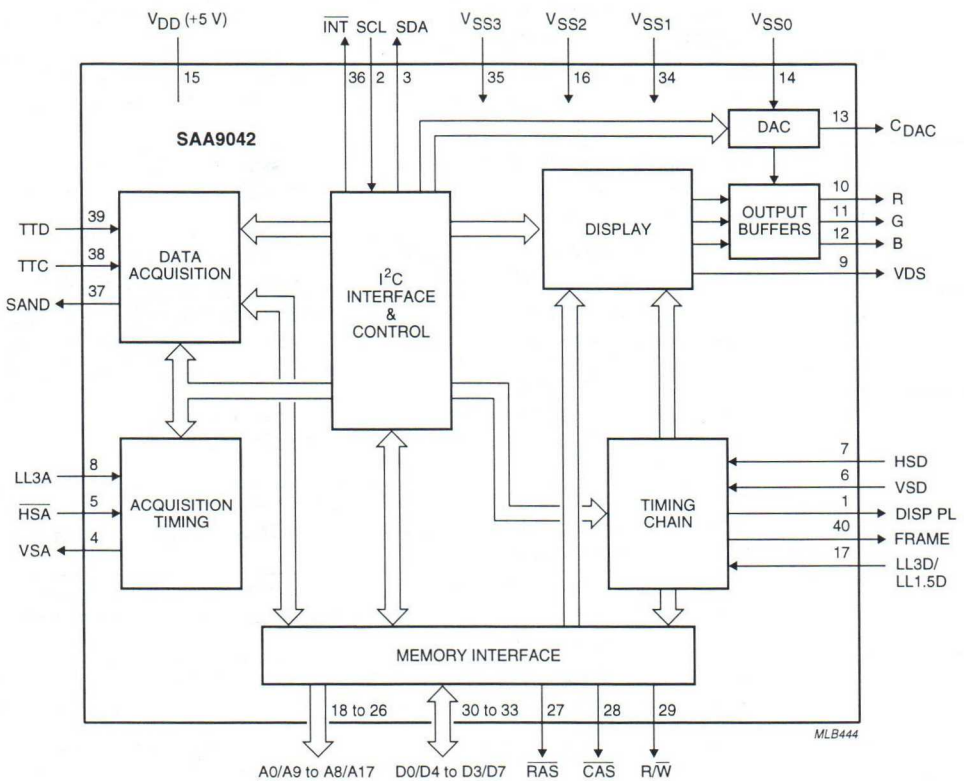


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DISP PL	1	Display PL: a programmable decode from the display-timing chain which can be used as a reference signal in an external PLL in scan-locked applications.
SCL	2	Serial Clock: input signal which is the I^2C-bus clock from the microcontroller.
SDA	3	Serial Data: is the I^2C-bus data line connected to the microcontroller. It is an input/output function with an open-drain output.
VSA	4	Vertical Synchronization Acquisition: synchronization signal from the SAA5191 (VCS), derived from the incoming video. This input enables field timing to be established in the acquisition section.
$\overline{HSA}$	5	Horizontal Synchronization Acquisition: horizontal synchronization signal derived from the incoming video e.g. burst gate pulse. This active LOW input enables line timing to be established in the acquisition section.
VSD	6	Vertical Synchronization Display: synchronization signal indicating the vertical position of the TV picture. This input allows field synchronization of the display section.
HSD	7	Horizontal Synchronization Display: synchronization signal indicating the horizontal position of the TV picture. This input allows line synchronization of the TV picture.
LL3A	8	Line-Locked system clock: 13.5 MHz system clock input for the acquisition section.
VDS	9	Video/Data Switch: push-pull active HIGH 3-state output which controls the switching between text (HIGH) and normal TV (LOW) picture for both normal text and superimposed displays.
R	10	Red: analog 3-state output which contains video character and background information for text display. The output level is adjustable over 16 steps and is controlled by V_{SS0}, V_{DD} and an internal register.
G	11	Green: analog 3-state output which contains video character and background information for text display. The output level is adjustable over 16 steps and is controlled by V_{SS0}, V_{DD} and an internal register.
B	12	Blue: analog 3-state output which contains video character and background information for text display. The output level is adjustable over 16 steps and is controlled by V_{SS0}, V_{DD} and an internal register.
C_{DAC}	13	DAC output: DAC output level, requires an external decoupling capacitor >1 µF.
V_{SS0}	14	Ground: ground connection 0 for video outputs.
V_{DD}	15	Power Supply: +5 V (typ.).
V_{SS2}	16	Ground: ground connection 2.
LL3D/LL1.5D	17	Line-Locked system clock: 13.5 MHz or 27 MHz system clock input for the display, memory interface and control sections.
A0/A9 to A8/A17	18 to 26	Address: multiplexed address outputs for the external nibble-wide dynamic RAM (DRAM). With a 256 kbit (64K × 4) DRAM the address pin A8 is not used.
$\overline{RAS}$	27	Row Address Strobe: active LOW output for the external DRAM.
$\overline{CAS}$	28	Column Address Strobe: active LOW output for the external DRAM.
R/$\overline{W}$	29	Read/Write: active LOW write enable signal for the external DRAM.
D3/D7 to D0/D4	30 to 33	Data: data inputs/outputs from the external nibble-wide DRAM.
V_{SS1}	34	Ground: ground connection 1.
V_{SS3}	35	Ground: ground connection 3.

SYMBOL	PIN	DESCRIPTION
$\overline{INT}$	36	Interrupt: open-drain active LOW output which provides an interrupt signal for a microcontroller indicating the arrival of a page or packet in any one of the acquisition channels, change in newsflash/subtitle status or power-on reset.
SAND	37	Sandcastle: 3-level output for the SAA5191 representing the PL/$\overline{CBB}$ signal, derived from the acquisition timing chain.
TTC	38	Teletext Clock: input from the SAA5191 supplied via an external coupling capacitor.
TTD	39	Teletext Data: input from the SAA5191 supplied via an external coupling capacitor, internally clamped to V_{SS} for 4 to 8 µs of each line to maintain the correct DC level.
FRAME	40	Frame: output for de-interlacing circuits. The signal is LOW for even fields and HIGH for odd fields when text but no picture is displayed. It is forced LOW when a TV picture is present.

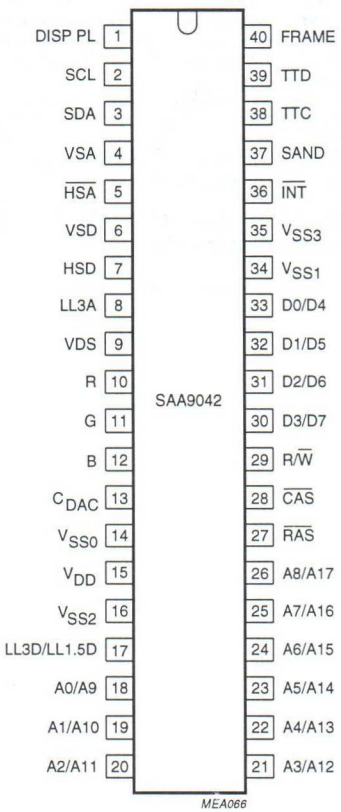


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). All voltages are with respect to VSS1/2/3. VSS0 is considered as an output.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	DC supply voltage		−0.5	+6.5	V
I_{DD}	DC supply current		tbf	tbf	mA
V_I	DC input voltage		−0.5	V_{DD} + 0.5	V
I_I	DC input current		−20	+20	mA
V_O	DC output voltage		−0.5	V_{DD} + 0.5	V
I_O	DC output current		−20	+20	mA
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		−20	+70	°C
V_{es}	electrostatic handling	note 1	−1000	+1000	V

Note

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; $V_{SS1/2/3}$ = 0 V; T_{amb} = −20 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	DC supply voltage	note 1	4.5	5.0	5.5	V
I_{DD}	DC supply current		–	100	–	mA
Inputs; note 2						
TTD; NOTE 3						
$V_{I(p-p)}$	input voltage (peak-to-peak value)		2.0	–	5.0	V
C_{ext}	external coupling capacitor		–	22	50	nF
t_r, t_f	input rise and fall times	notes 4 and 26	10	–	80	ns
$t_{SU;DAT}$	input data set-up time	note 5	40	–	–	ns
$t_{HD;DAT}$	input data hold up time	note 5	40	–	–	ns
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance	note 26	–	7	–	pF
t_{CLon}	clamp start time	note 6	3.5	4.0	4.5	µs
t_{CLoff}	clamp finish time	note 6	7.5	8.0	8.5	µs
I_{CL}	clamp output current	note 7	1.0	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TTC; NOTE 8						
$V_{I(p-p)}$	input voltage (peak-to-peak value)		2.0	–	5.0	V
C_{ext}	external coupling capacitor		–	10	10	nF
I_{IM}	peak input current		−10	–	+10	mA
V_{IM}	input voltage (peak value) relative to 50% duty factor		±0.2	–	±3.5	V
t_r, t_f	input rise and fall times	notes 4 and 26	10	–	80	ns
C_I	input capacitance	note 26	–	7	–	pF
V_{CL}	input clamp voltage		1.2	1.4	1.6	V
f_{clk}	clock frequency	625 line	–	6.9375	–	MHz
		525 line	–	5.7272	–	MHz
$\overline{HSA}$; NOTE 9						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
t_r, t_f	input rise and fall times	notes 4 and 26	–	–	500	ns
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance	note 26	–	–	7	pF
VSA						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage	note 27	2.0	–	V_{DD}	V
t_r, t_f	input rise and fall times	notes 4 and 26	–	–	500	ns
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance	note 26	–	–	7	pF
LL3A; TTL MODE; FIG.4						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
t_{CA}	LL3A cycle time	note 10	69	74	80	ns
t_{CAH}	LL3A HIGH time		28	–	–	ns
t_{CAL}	LL3A LOW time		28	–	–	ns
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−100	–	+100	µA
C_I	input capacitance	note 26	–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LL3A; AC MODE; F = 13.5 MHz; SEE FIG.4						
V_{ACM}	mean voltage level	notes 25 and 26	−12	–	+12	V
$V_{AC(p-p)}$	AC voltage (peak-to-peak value)		1.0	–	3.0	V
V_{ACH}	voltage HIGH w.r.t. mean		0.3	–	2.0	V
V_{ACL}	voltage LOW w.r.t. mean		−2.0	–	−0.3	V
msr	input mark/space ratio w.r.t. mean t_{ACH}/t_{ACL} or t_{ACL}/t_{ACH}	note 28	30 : 70	–	70 : 30	
C_s	series capacitance		47	100	220	pF
Z_i	input impedance	notes 24 and 26	10	–	–	kΩ
SCL; NOTE 31						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}	V
t_r	input rise time	notes 4 and 26	–	–	1	µs
t_f	input fall time	notes 11 and 26	–	–	300	ns
I_{LI}	input leakage current	note 12; V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance	note 26	–	–	7	pF
HSD						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
t_r, t_f	input rise and fall times	notes 4 and 26	–	50	500	ns
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance	note 26	–	–	7	pF
VSD						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
t_r, t_f	input rise and fall times	notes 4 and 26	–	–	500	ns
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance	note 26	–	–	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LL3D/LL1.5D; TTL MODE						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
t_r, t_f	input rise and fall times	notes 4 and 26	–	–	10	ns
t_{CA}	LL3D/LL1.5D cycle time	13.5 MHz	69	74	80	ns
		27.0 MHz	35	37	40	ns
t_{CAH}	LL3D/LL1.5D HIGH time	13.5 MHz	28	–	–	ns
		27.0 MHz	14	–	–	ns
t_{CAL}	LL3D/LL1.5D LOW time	13.5 MHz	28	–	–	ns
		27.0 MHz	14	–	–	ns
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–100	–	+100	µA
C_I	input capacitance	note 26	–	–	10	pF
LL3D/LL1.5D; AC MODE; f = 13.5 MHz OR 27 MHz; SEE FIG.4						
V_{ACM}	mean voltage level	notes 25 and 26	–12	–	+12	V
$V_{AC(p-p)}$	AC voltage		1.0	–	3.0	V
V_{ACH}	voltage HIGH w.r.t. mean		0.3	–	2.0	V
V_{ACL}	voltage LOW w.r.t. mean		–2.0	–	–0.3	V
msr	input mark/space ratio w.r.t. mean t_{ACH}/t_{ACL} or t_{ACL}/t_{ACH}	note 28	30 : 70	–	70 : 30	
C_s	series capacitance		47	100	220	pF
Z_i	input impedance	notes 24 and 26	10	–	–	kΩ
Inputs/outputs; note 13						
SDA; OPEN-DRAIN I/O; NOTE 31						
V_{IL}	LOW level input voltage		0	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DD}	V
t_r	input rise time	notes 4 and 26	–	–	1	µs
t_f	input fall time	notes 11 and 26	–	–	300	ns
I_{LI}	input leakage current	V_I = 0 to V_{DD}; note 12; with output off	–10	–	+10	µA
C_I	input capacitance	note 26	–	–	7	pF
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	0	–	0.4	V
t_f	output fall time	notes 11 and 26	–	–	300	ns
C_L	load capacitance		–	–	400	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
D0/D4 TO D3/D7						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
I_{LI}	input leakage current	note 12; V_I = 0 to V_{DD}; with output off	−10	–	+10	μA
C_I	input capacitance	note 26	–	–	7	pF
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −200 μA	2.4	–	V_{DD}	V
t_r, t_f	output rise and fall times between 0.6 V and 1.8 V	note 26	–	–	10	ns
C_L	load capacitance	note 21	–	–	100	pF
Outputs; note 13						
SAND; NOTE 22						
V_{OL}	LOW level output voltage	I_{OL} = 0.2 mA	0	–	0.3	V
V_{OI}	intermediate level output voltage	I_{OI} = ±30 μA	1.3	–	2.7	V
V_{OH}	HIGH level output voltage	I_{OH} = 0 to −10 μA	4.0	–	V_{DD}	V
t_r	output rise time V_{OL} to V_{OI} between 0.4 V and 1.1 V	note 26	–	–	400	ns
t_r	output rise time V_{OL} to V_{OH} between 2.9 V and 4.0 V	note 26	–	–	200	ns
t_f	output fall time V_{OH} to V_{OL} between 4.0 V and 0.4 V	note 26	–	–	50	ns
C_L	load capacitance		–	–	30	pF
$\overline{\text{INT}}$; OPEN-DRAIN OUTPUT						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
I_{LO}	output leakage current	V_{PU} = 0 V to V_{DD}; with output off	−10	–	+10	μA
t_f	output fall time	notes 15 and 26	–	–	50	ns
C_L	load capacitance		–	–	100	pF
A0/A9 TO A8/A17						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −200 μA	2.4	–	V_{DD}	V
t_r, t_f	output rise and fall times between 0.6 V and 1.8 V	note 26	–	–	10	ns
C_L	load capacitance	note 23	–	–	100	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\overline{RAS}$, $\overline{CAS}$ AND R/$\overline{W}$						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –200 µA	2.4	–	V_{DD}	V
t_r, t_f	output rise and fall times between 0.6 V and 1.8 V	note 26	–	–	10	ns
C_L	load capacitance	note 23	–	–	100	pF
DISP PL AND FRAME						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –200 µA	2.4	–	V_{DD}	V
t_r, t_f	output rise and fall times	notes 16 and 26	–	–	200	ns
C_L	load capacitance		–	–	200	pF
R, G, B; 3-STATE; NOTE 29						
V_{OL}	LOW level output voltage	I_{OL} = 2.0 mA; note 17	V_{SS0}	–	V_{SS0} + 0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = –2 mA; note 18	–	note 30	–	V
t_r, t_f	output rise and fall times between 0.6 V and 1.8 V	notes 4, 17 and 26	–	–	10	ns
C_L	load capacitance		–	–	30	pF
C_{off}	output capacitance	off state; note 26	–	–	10	pF
I_{off}	output leakage current	off state; V_I = 0 to V_{DD}	–10	–	+10	µA
VDS; 3-STATE; NOTE 29						
V_{OL}	LOW level output voltage	I_{OL} = 1.0 mA	0	–	0.2	V
V_{OH}	HIGH level output voltage	I_{OH} = –200 µA	1.1	–	2.8	V
t_r, t_f	output rise and fall times	note 26	–	–	10	ns
C_L	load capacitance		–	–	30	pF
I_{off}	output leakage current	off state; V_I = 0 to V_{DD}	–10	–	+10	µA
t_{skew}	skew delay between R, G, B and VDS outputs	note 19	–	–	10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
I²C-BUS; NOTE 20; FIG.3						
f_{SCL}	SCL clock frequency	note 31	0	–	100	kHz
t_{LOW}	clock LOW period		4	–	–	µs
t_{HIGH}	clock HIGH period		4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;STA}$	START hold time		4	–	–	µs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	µs
MEMORY INTERFACE; NOTE 14; FIGS 5 AND 6						
t_{CY}	cycle time		–	481	–	ns
t_T	transition time		–	–	10	ns
$t_{W;RAS}$	$\overline{RAS}$ pulse width		120	–	–	ns
$t_{PC;RAS}$	$\overline{RAS}$ precharge time		90	–	–	ns
$t_{HD;CAS}$	$\overline{CAS}$ hold time		120	–	–	ns
$t_{CY;PM}$	page mode cycle time		120	–	–	ns
t_d	$\overline{RAS}$ to $\overline{CAS}$ delay time		25	–	–	ns
$t_{W;CAS}$	$\overline{CAS}$ pulse width		60	–	–	ns
$t_{PC;CAS}$	$\overline{CAS}$ precharge time		50	–	–	ns
$t_{SU;ROW}$	row address set-up time		0	–	–	ns
$t_{HD;ROW}$	row address hold time		15	–	–	ns
$t_{SU;COL}$	column address set-up time		0	–	–	ns
$t_{HD;COL}$	column address hold time		20	–	–	ns
$t_{SU;RD}$	read command set-up time		0	–	–	ns
$t_{HD;RDC}$	read command hold time referenced to $\overline{CAS}$		0	–	–	ns
$t_{HD;RDR}$	read command hold time referenced to $\overline{RAS}$		10	–	–	ns
$t_{ACC;CAS}$	access time from $\overline{CAS}$		–	–	60	ns
$t_{W;WR}$	write command pulse width		50	–	–	ns
$t_{HD;WR}$	write command hold time		40	–	–	ns
$t_{SU;DATI}$	data input set-up time		0	–	–	ns
$t_{HD;DATI}$	data input hold time		40	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{ACC;RAS}$	access time from $\overline{RAS}$		–	–	120	ns
$t_{HD;RC}$	$\overline{RAS}$ hold time after $\overline{CAS}$		60	–	–	ns
$t_{PC;CR}$	$\overline{CAS}$ to $\overline{RAS}$ precharge time		20	–	–	ns
$t_{HD;COLR}$	column address hold time referenced to $\overline{RAS}$		80	–	–	ns
$t_{HD;DATIR}$	data input hold time referenced to $\overline{RAS}$		100	–	–	ns

Notes

1. The rise time of V_{DD} from 0 to 4.5 V must be >150 ns to ensure that the internal power-on reset triggers. For this circuit to reset the chip, V_{DD} must be initially <1.0 V or fall to <1.0 V for at least 100 ns. Spikes on V_{DD} are tolerable provided that V_{DD} is not reduced to <2.5 V.
2. All inputs are protected against static charge under normal handling.
3. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor.
4. Rise and fall times are measured between 10% and 90% levels.
5. Teletext input data set-up and hold times are measured with respect to 50% duty factor level of the rising edge of the teletext clock input (TTC). Data stable 1 ≥ 2.0 V, data stable 0 ≤ 0.8 V.
6. Clamp times measured from the line sync reference point, assuming acquisition timing is set correctly.
7. Clamping transistor on, $V_{TTD} - V_{SS1} \leq 0.1$ V.
8. The TTC input has an internal clamping diode.
9. $\overline{HSA}$ is falling edge triggered.
10. Minimum and maximum cycle times are ±7.1% of the typical value.
11. Fall time is measured between 3.0 V and 1.5 V.
12. Applies even when $V_{DD} = 0$ V.
13. All input/outputs and outputs are protected against static charge under normal handling.
14. For details of memory interface timings to and from external DRAM see Figs 5 and 6.
15. Output fall time measured between 4.0 V and 1.0 V levels with a 3.3 kΩ load to 5.0 V.
16. Output rise and fall times measured between 0.8 V and 2.0 V levels.
17. Measured with $I_{OL} = 2.0$ mA, $V_{SS0} = V_{SS1/2/3}$ and output voltage (C_{DAC}) = 1.5 V.
18. Measured with $I_{OH} = -2$ mA, $V_{SS0} = V_{SS1/2/3}$ and output voltage (C_{DAC}) = 0.5 to 1.5 V.
19. Skew delay time measured at 0.7 V levels.
20. For details of I²C-bus timings see Fig.3; timings are referenced to $V_{IH} = 3.0$ V and $V_{IL} = 1.5$ V.
21. Load capacitance measured with two DRAM data inputs; 50 pF maximum.
22. A current of 1 μA flows out of the SAA5191 while its SAND input is in the range of 1 V to 3.5 V.
23. Load capacitance measured with eight DRAM data inputs; 80 pF maximum.
24. Through a 200 pF capacitor with a 13.5 MHz sinewave.
25. To be applied via a series capacitor only.
26. This specification point is included because of its importance to the application environment; it is not however guaranteed.
27. When connected to the SAA5191, it is acceptable for the clock frequency to initially attain ≤15 MHz in order to achieve synchronization.

28. When connected to the SAA5191, it is acceptable for the input voltage to attain V_{DD} + 0.9 V. The input current must be restricted as specified in the limiting values.
29. These outputs can be made 3-state via the I²C-bus.
30. Typical values adjustable over 0.5 to 1.5 V via the I²C-bus.
31. A standard (100 kHz) I²C interface is implemented. Fast mode (400 kHz) is not supported.

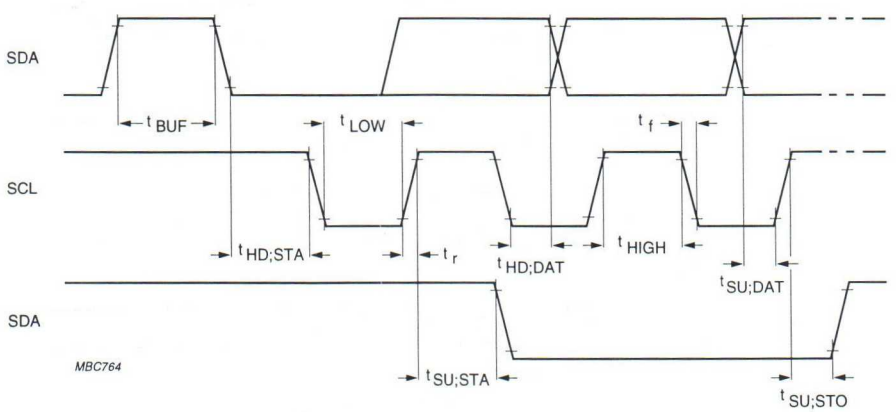


Fig.3 I²C-bus timing.

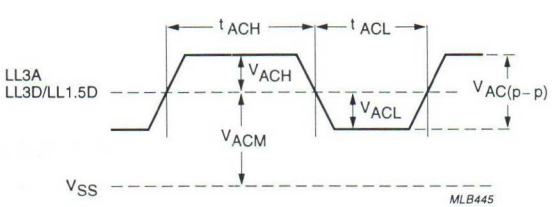


Fig.4 Line-locked system clock LL3A and LL3D/LL1.5D timing diagram.

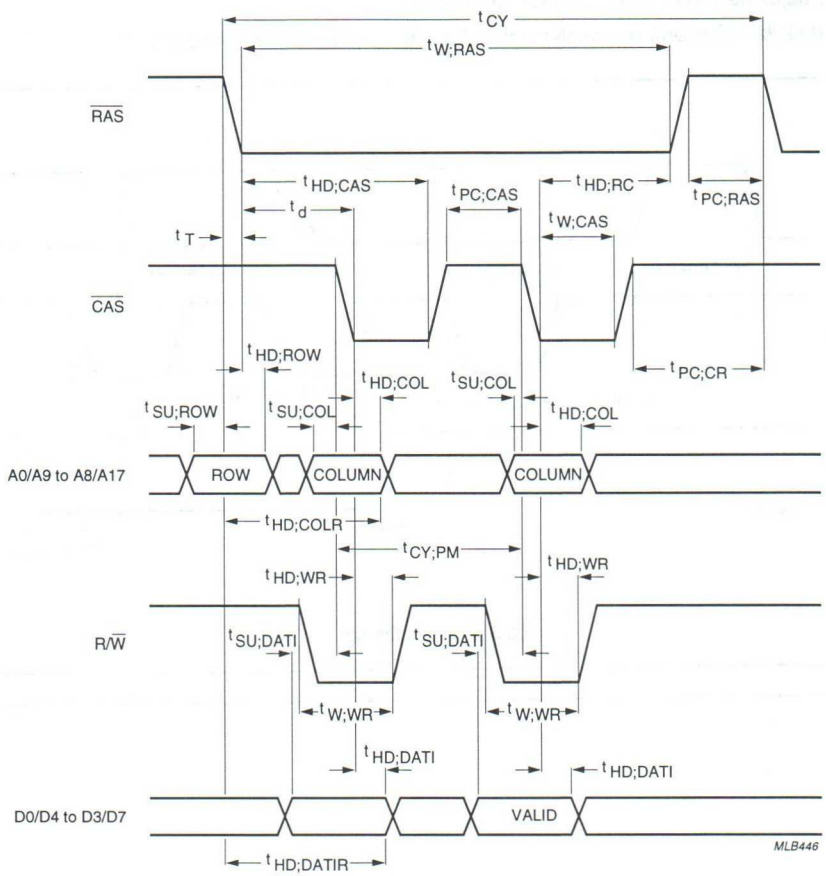


Fig.5 Memory interface timing for write cycle to external DRAM.

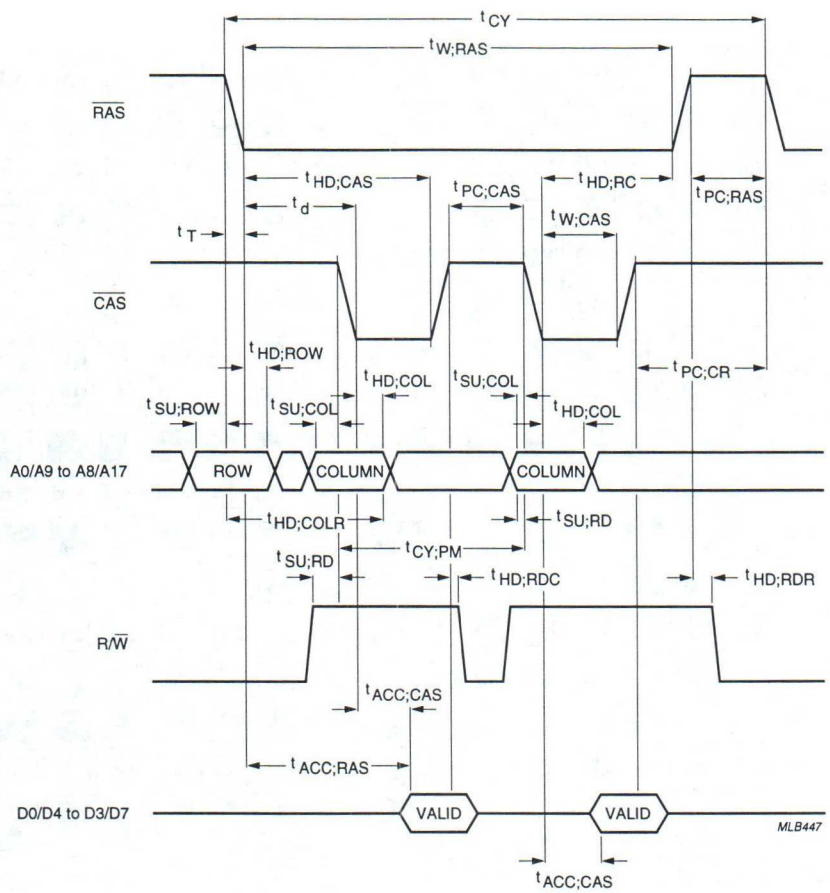


Fig.6 Memory interface timing for read cycle from external DRAM.

CHARACTER SETTINGS

The different character settings are explained in Tables 1 to 6.

Table 1 SAA9042A West European character set; for N.O. (national option character position) see Table 2.

Notes to Table 1

1. These control characters are reserved for compatibility with other data codes.
2. These control characters are presumed before each rows begins.

Table 2 SAA9042A West European national option sets.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN (2)	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MEA559

Notes

1. Where PHCB are the Page Header Control Bits. Other combinations of PHCB default to English.
2. Basic character set is Italian. Selected when the force language bit (D5) in the display set-up register (R12) is set to logic 1.

Table 3 SAA9042B Eastern European character set; for N.O. (national option character position) see Table 4.

Notes to Table 3

1. These control characters are reserved for compatibility with other data codes.
2. These control characters are presumed before each rows begins.

Table 4 SAA9042B Eastern European national option sets.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
POLISH	0	0	0	#	ń	ą	Ż	Ś	Ł	ć	ó	ę	ż	ś	ł	ź
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
SERBO-CROAT	1	0	1	#	½	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECHOSLOVAK	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
ROMANIAN (2)	1	1	1	#	¤	Ţ	Â	Ş	A	Î	ı	ţ	â	ş	ă	î

MLB450

Notes

1. Other combinations of C12, C13 and C14 default to German.
2. Basic character set is Romanian. Selected when the force language bit (D5) in the display set-up register (R12) is set to logic 1.

Table 5 SAA9042C Euro-Turkish character set; for N.O. (national option character position) see Table 6.

Notes to Table 5

1. These control characters are reserved for compatibility with other data codes.
2. These control characters are presumed before each rows begins.

Table 6 SAA9042C Euro-Turkish national option sets.

LANGUAGE	PHCB [1]			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
ITALIAN [2]	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à
TURKISH	1	1	0	Ţ	ğ	İ	Ş	Ö	Ç	Ü	Ğ	ı	ş	ö	ç	ü

MLB452

Notes

1. Other combinations of C12, C13 and C14 default to English.
2. Basic character set is Italian. Selected when the force language bit (D5) in the display set-up register (R12) is set to logic 1.

APPLICATION INFORMATION

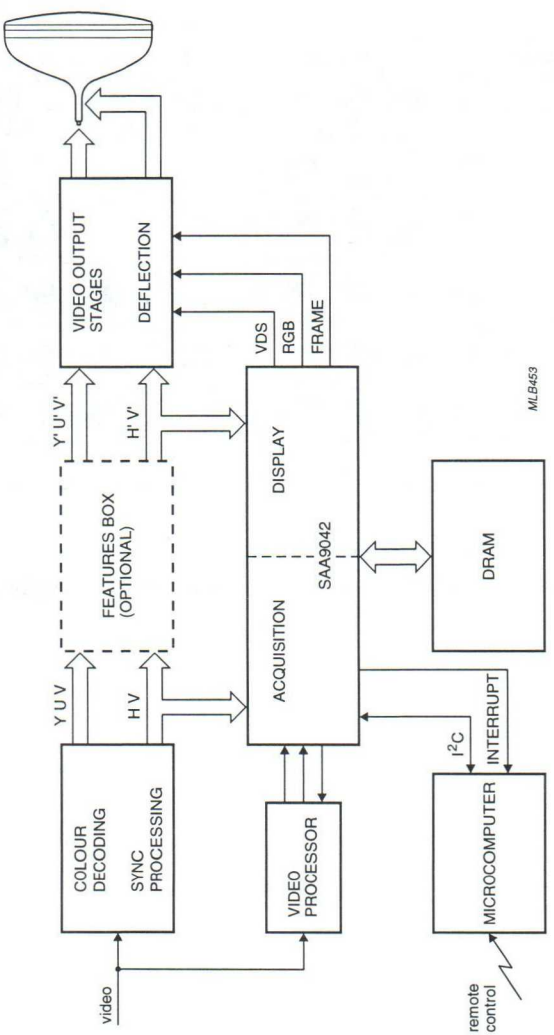
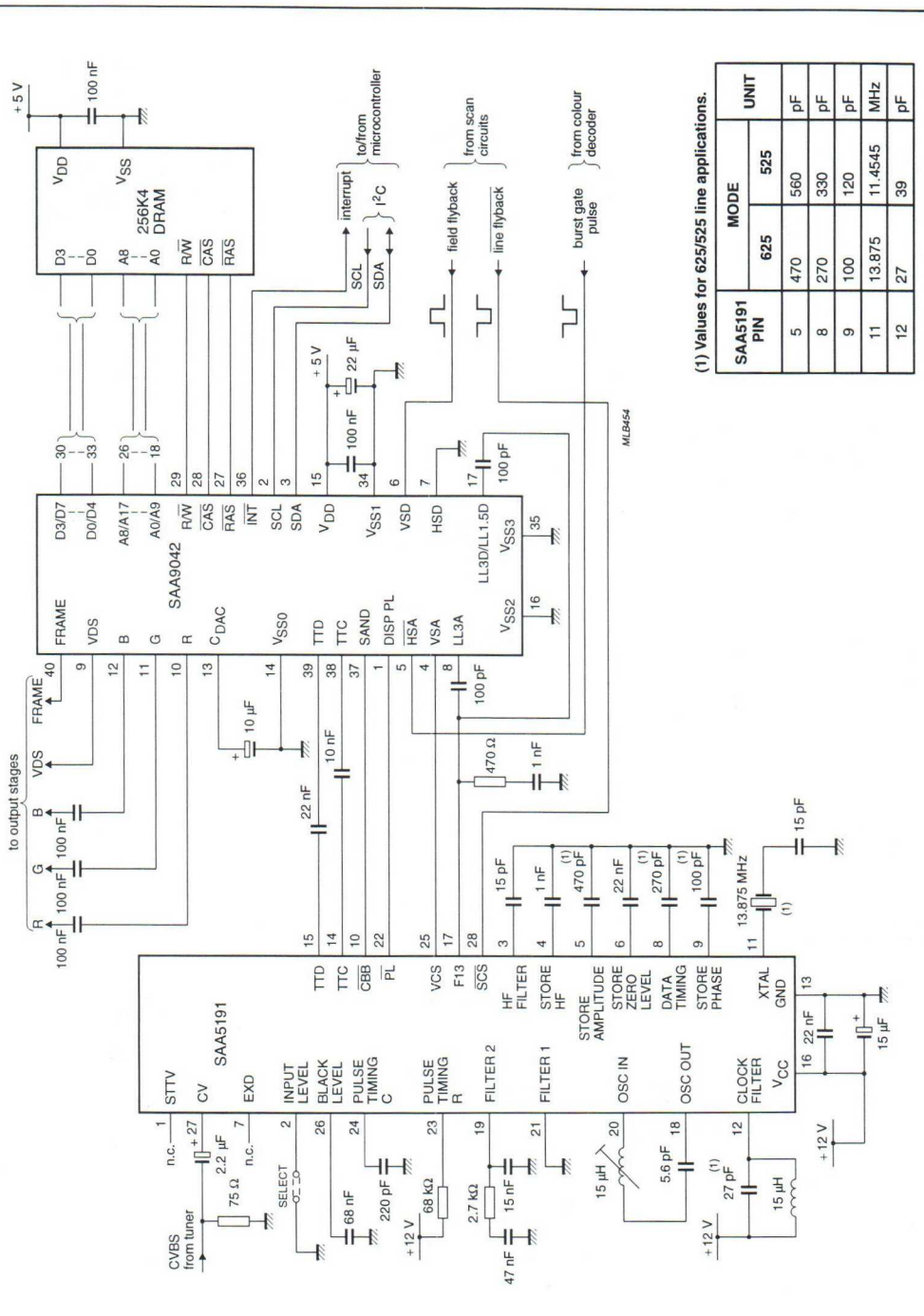


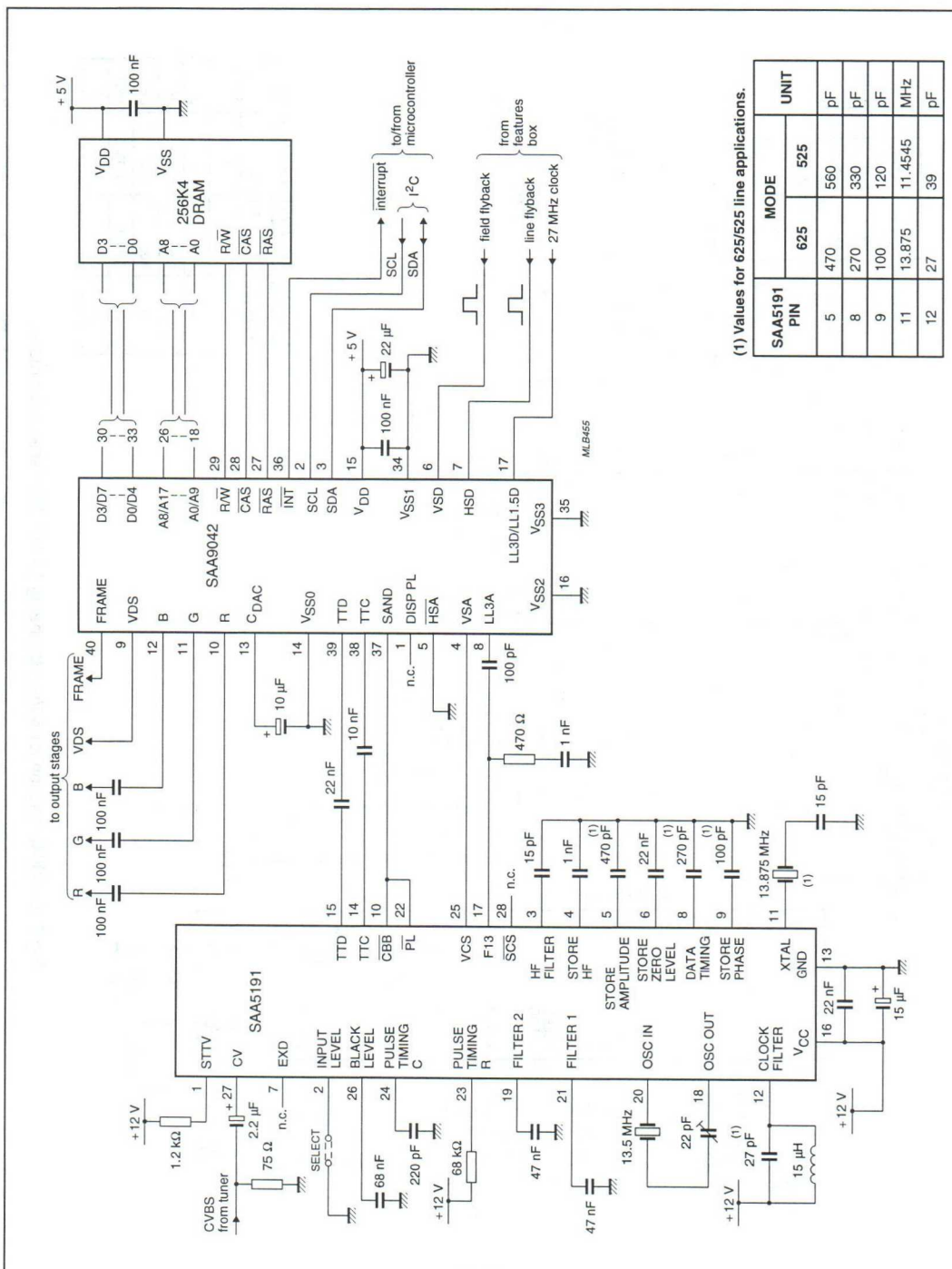
Fig.7 Basic system configuration.



(1) Values for 625/525 line applications.

SAA5191 PIN	MODE		UNIT
	625	525	
5	470	560	pF
8	270	330	pF
9	100	120	pF
11	13.875	11.4545	MHz
12	27	39	pF

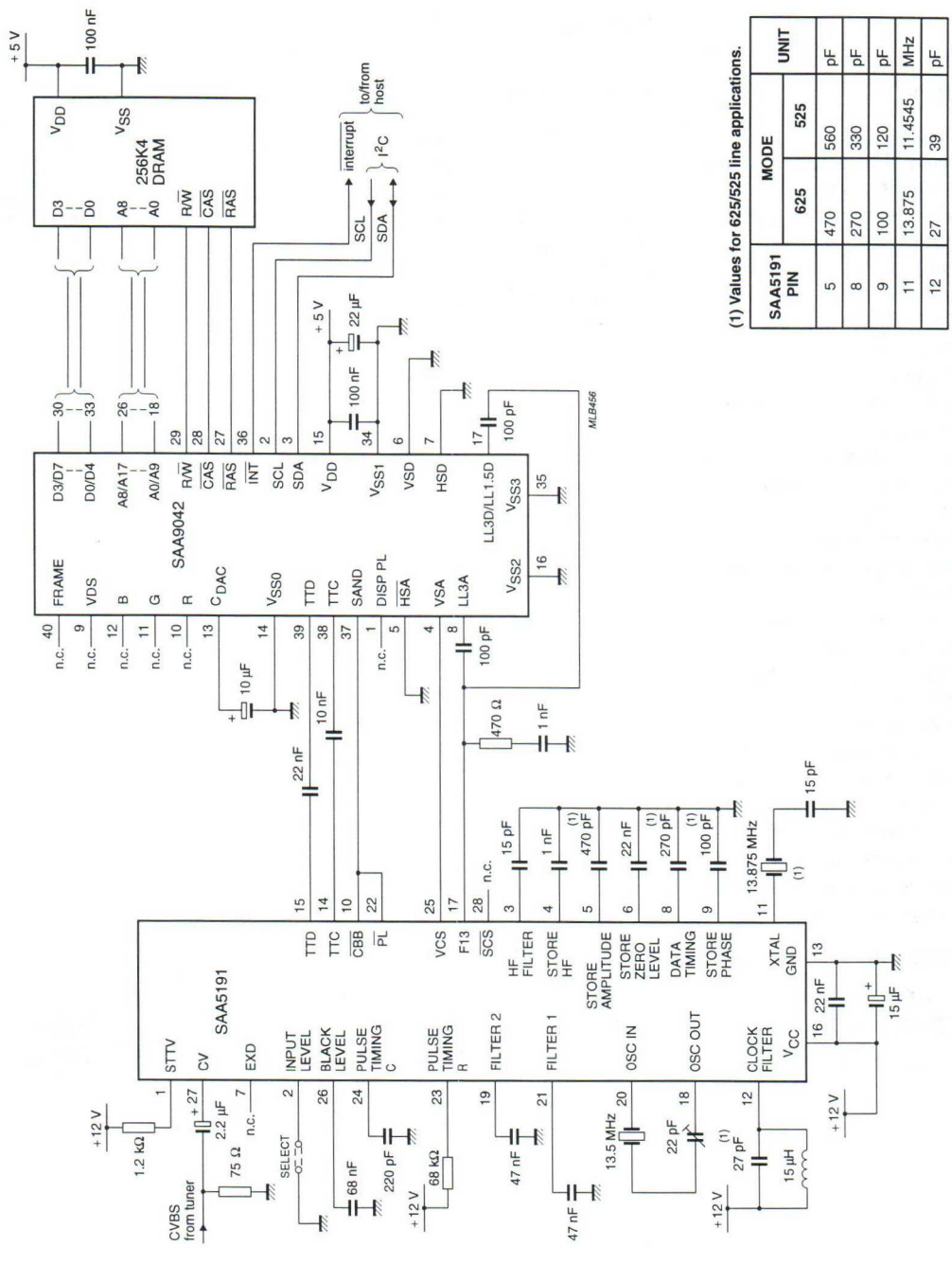
Fig.8 SAA9042 solution for 50/60 Hz analog TV (1H/1V) - scan sync mode.



(1) Values for 625/525 line applications.

SAA5191 PIN	MODE		UNIT
	625	525	
5	470	560	pF
8	270	330	pF
9	100	120	pF
11	13.875	11.4545	MHz
12	27	39	pF

Fig.9 SAA9042 solution for features TV (2H/1V or 2H/2V).



(1) Values for 625/525 line applications.

SAA5191 PIN	MODE		UNIT
	625	525	
5	470	560	pF
8	270	330	pF
9	100	120	pF
11	13.875	11.4545	MHz
12	27	39	pF

Fig.10 SAA9042 solution for multi-media applications.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	July 1990

SAA9051

Digital multistandard TV decoder with separate chrominance and luminance inputs

FEATURES

- All operations based on a sampling frequency of 13.5 MHz, providing:
  - full adaptability to all transmission standards
  - capability for memory-based features
- Separate chrominance and luminance input (Y/C)
- CVBS input for standard applications
- CVBS throughput capability for SECAM application
- Luminance signal processing for all TV standards (PAL, NTSC, SECAM, B/W)
- Horizontal and vertical synchronization detection for all standards
- Chrominance signal processing for all quadrature amplitude modulated colour-carrier signals
- Requires only one crystal
- Controlled via the I²C-bus
- User-programmable aperture correction (horizontal peaking)
- Compatible with memory-based features (line-locked clock)
- Cross-colour reduction by chrominance comb-filter (NTSC)
- Wide range hue control

GENERAL DESCRIPTION

The SAA9051 digital multistandard decoder (S-DMSD) performs demodulation and decoding of all quadrature modulated colour TV standards, as well as performing luminance and processing for all TV standards with CVBS or Y/C input signals.



ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9051	68	PLCC	plastic	SOT188

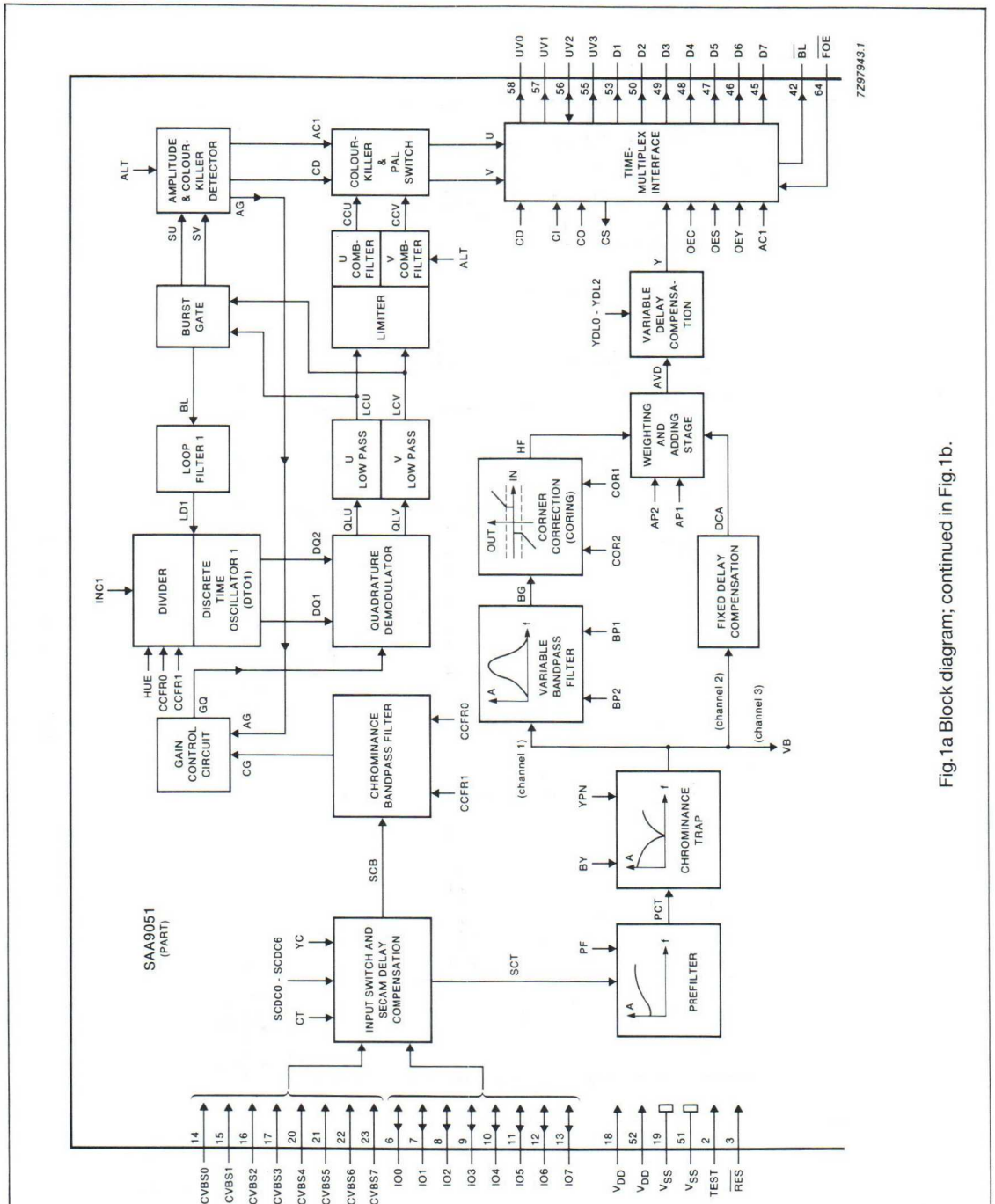


Fig.1a Block diagram; continued in Fig.1b.

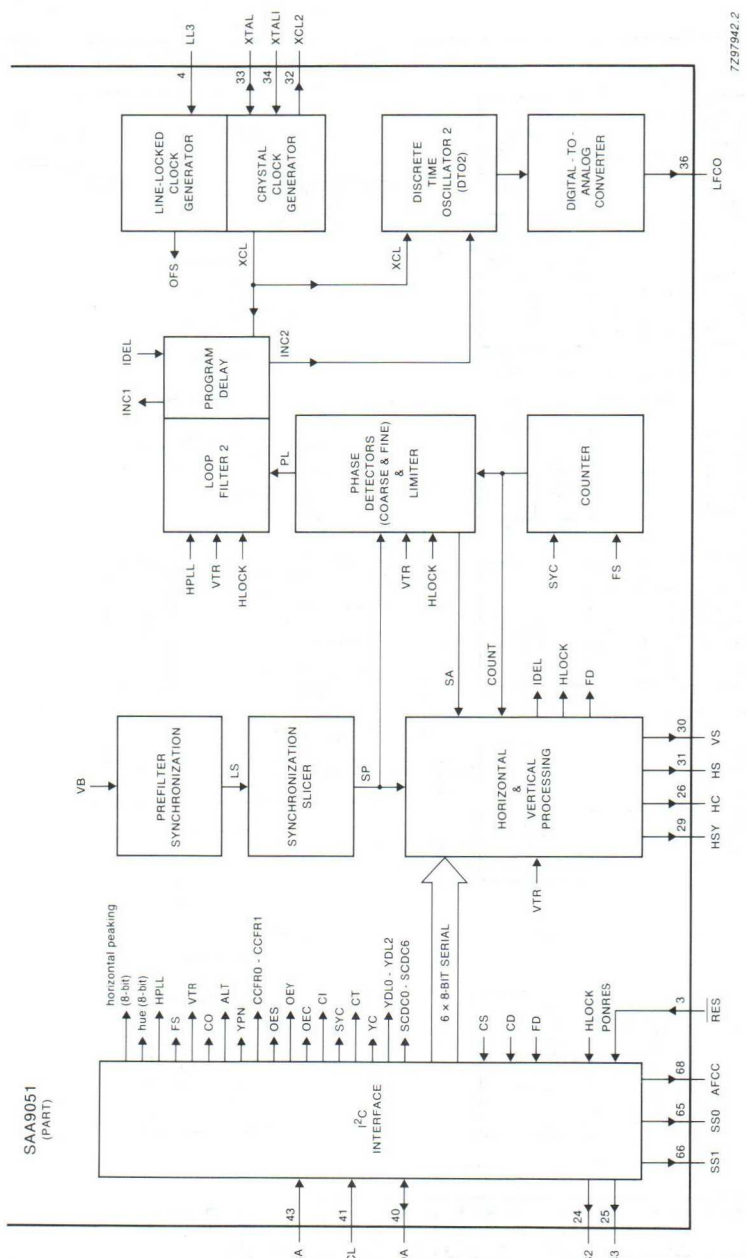


Fig.1b Block diagram; from Fig.1a.

PIN CONFIGURATION

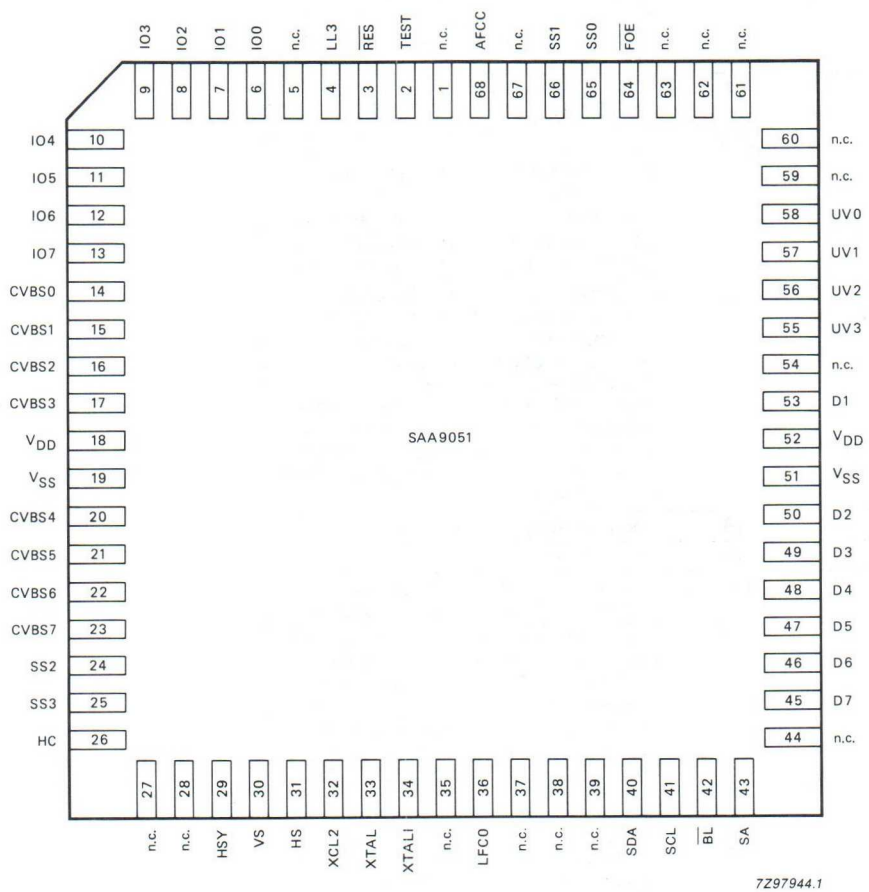


Fig.2 Pinning configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
TEST	2	test input (active HIGH); when HIGH enables scan-test mode
$\overline{RES}$	3	reset input (active LOW); results in the I²C-bus control registers 1 to 3 and internal stages being reset during the reset phase. The minimum LOW period of $\overline{RES}$ is 120 LL3 clock cycles
LL3	4	13.5 MHz line-locked system clock
n.c.	5	not connected
IO0 (LSB) – IO7 (MSB)	6 – 13	bidirectional data path; chrominance input for separate luminance and chrominance input (Y/C) or CVBS output for SECAM decoder SAA9056. Two's complement format (IO0 is only used internally for CVBS throughput)
CVBS0 (LSB) – CVBS7 (MSB)	14 – 17, 20 – 23	digitalized composite video blanking and synchronization signals; containing luminance, chrominance and all synchronization information or luminance, blanking and synchronization signals in the event of separate luminance and chrominance (Y/C) input. Two's complement format (CVBS0 is only used internally for CVBS throughput)
V_{DD}	18	positive supply voltage (+5 V)
V_{SS}	19	ground (0 V)
SS2 – SS3	24 – 25	source select output signals; I²C-bus controlled, TTL compatible switches
HC	26	programmable horizontal output pulse; when used in conjunction with the TDA9045 or TDA8708 it indicates the black-level position before analog-to-digital conversion. The start and stop times are programmable, between – 9.4 µs and +9.5 µs in steps of 74 ns, via the I²C-bus
n.c.	27 – 28	not connected
HSY	29	programmable horizontal output pulse; when used in conjunction with the TDA9045 OR TDA8708 it indicates the synchronization pulse position before analog-to-digital conversion. The start and stop times are programmable, between –14.2 µs and +4.7 µs in steps of 74 ns, via the I²C-bus
VS	30	vertical synchronization output; indicates the vertical position of the picture for 50/60 Hz field frequency

PINNING (continued)

SYMBOL	PIN	DESCRIPTION
HS	31	horizontal synchronization pulse output (duration = 64 LL3 clock cycles). HS is programmable, between −32 µs and +32 µs in steps of 300 ns, via the I²C-bus
XCL2	32	clock output; half of the crystal clock frequency (12.288 MHz). In phase with XTAL (pin 33)
XTAL	33	crystal oscillator input/inverting amplifier output; input to the internal clock generator from an external oscillator or output of the inverting amplifier to an external crystal (24.576 MHz)
XTALI	34	input to the inverting amplifier from an external crystal (24.576 MHz); connect to ground if an external oscillator is used
n.c.	35	not connected
LFCO	36	line frequency control; analog output representing a multiple of the line frequency (6.75 MHz) with 4-bit resolution, the phase of which is compared to the system clock by the CGC (SAA9057)
n.c.	37 – 39	not connected
SDA	40	I²C-bus serial data input/output
SCL	41	I²C-bus serial clock input
$\overline{BL}$	42	blanking signal output (active LOW); indicates the active video and line blanking periods. $\overline{BL}$ also synchronizes the data multiplexers/demultiplexers
SA	43	I²C-bus select address; input for selection of the appropriate I²C-bus slave address
D7 (MSB) – D1 (LSB)	45 – 50, 53	luminance data output
V_{SS}	51	ground (0 V)
V_{DD}	52	positive supply voltage (+5 V)
n.c.	54	not connected
UV3 – UV0	55 – 58	multiplexed PAL or NTSC colour difference signal output or SECAM CS input signal from the SECAM decoder. Output data format is two's complement. The multiplexer is synchronized to the rising-edge of $\overline{BL}$
n.c.	59 – 63	not connected
$\overline{FOE}$	64	fast output enable signal (active LOW); sets D1 – D7 and UV0 – UV3 outputs to the HIGH-impedance Z-state

SYMBOL	PIN	DESCRIPTION
SS0 – SS1	65 – 66	source select output signals, set via the I²C-bus; used to control the input switch (e.g. TDA9045)
n.c.	67	not connected
AFCC	68	additional output for circuit control; activated via the I²C-bus

FUNCTIONAL DESCRIPTION

(see Fig.1)

The S-DMSD performs demodulation and decoding for all quadrature modulated colour TV standards (PAL-B, G, H, I, M, N, NTSC 4.43 MHz, NTSC-M), as well as performing luminance and parts of the synchronization processing for TV standards (PAL, NTSC and SECAM). All of the controllable functions, user as well as factory adjustments, are accessed via I²C-bus. Thereby enhancing the adaptability of the digital TV concept.

Operation is based on a line-locked sampling frequency of 13.5 MHz, making the system fully adaptable to all line frequencies and requiring only one crystal for all TV standards.

The S-DMSD is designed to operate in conjunction with the SAA9057A (CGC). If the CGC is not utilized the designer must ensure:

- a reset pulse is applied to the S-DMSD after a power failure
- that a continuous clock signal (minimum 1 MHz) is connected to the S-DMSD.

Y/C processing

In the Y/C mode, the following occurs:

- The chrominance signal is input at the IO port (IO0 – IO7) and transmitted via the input switch/ SECAM delay compensation circuit (multiplexer) to the chrominance bandpass filter (see section chrominance path)
- The other components, Y signal and synchronization pulse, are input via inputs CVBS0 – CVBS7 and transmitted via the input switch/SECAM delay compensation circuit to the luminance prefilter.

CVBS processing

In the CVBS mode:

- The CVBS signal is separated into its luminance (VBS) and chrominance (CG) parts by the chrominance trap and bandpass circuits. These circuits can be switched by the standard identification signals (CCFR0, CCFR1/YPN) according to the detected colour-carrier frequency, 3.58 MHz or 4.43 MHz.
- On reception of a SECAM signal the signal is transmitted to the SECAM decoder (SAA9056) via the IO port (IO0 – IO7). Bit CT enables the 3-state buffer between both parts.

Luminance path

The luminance path is separated into three channels after the chrominance trap stage (see Fig.1). The following occurs:

CHANNEL 1 SIGNAL

The channel 1 signal is transmitted to the programmable bandpass filter where the high luminance frequencies are removed (centre frequency is programmable via bits BP1 and BP2). The signal BC is transmitted to the coring (corner correction) stage where low amplitude noise is removed (amount of low amplitude noise removal is programmable via bits COR1 and COR2). The signal HF is transmitted to the weighting and adding stage, see section 'Combining channel 1 and channel 2 signals'.

CHANNEL 2 SIGNAL

The channel 2 signal is transmitted to the fixed delay compensation stage where delay compensation and black level adjustment occurs. The signal DCA is transmitted to the weighting and adding stage, see section 'Combining channel 1 and channel 2 signals'.

FUNCTIONAL DESCRIPTION (continued)

Luminance path (continued)

CHANNEL 3 SIGNAL

The channel 3 signal VB is transmitted to the prefilter synchronization stage, see section 'Synchronization path'.

COMBINING CHANNEL 1 AND CHANNEL 2 SIGNALS

The channel 1 signal HF is weighted and added to the Channel 2 signal DCA. The combined signals are matched to the specified amplitude and the word size is reduced to 7 bits. The signal AVD is transmitted to the variable delay compensation stage where compensation for IF group delays occurs, the amount of delay is programmable (from −4 to +3 LL3 clock cycles, see note) via bits YDL0 – YDL2. The signal Y is transmitted to the time multiplexed interface where the signal is output via D1 – D7.

Note

Differences in the delay compensation required for PAL and NTSC are catered for by identification signal YPN which switches the chrominance trap to the appropriate colour-carrier frequency 3.58 MHz or 4.43 MHz.

Chrominance path

In the chrominance path the following occurs (see Fig.1):

The chrominance signal CG is transmitted from the chrominance bandpass stage to the gain control circuit (see note 1). The gain control stage ensures that the chrominance signal has constant burst amplitude. The signal GQ is transmitted to the quadrature demodulator, where demodulation of the quadrature modulated chrominance signal GQ to colour difference signals occurs. The signals QLU and QLV are transmitted to a low-pass filter for filtering. The signals LCU and LCV are transmitted to the limiter and comb-filter stage. The comb-filter stage (see note 2) separates remaining vertically correlated luminance components for NTSC (for PAL, the signals are phase corrected). The signals CCU and CCV are transmitted to the colour-killer and PAL switch stage (see note 3). At this stage signals which do not comply with the selected standard are removed. In PAL mode this stage restores the correct phase of signal V. The signals are then transmitted to the time multiplexed interface and output via UV0 – UV3.

Notes

1. The gain control stage is controlled by signal AG which is derived form the amplitude and colour-killer detector stage (ACKD). A non-standard burst to amplitude ratio results in an automatic colour-leveling stage functioning as an amplitude detector to ensure correct amplitude and avoid overflow/ limiter defects.
2. The comb-filter can be altered from alternate to non-alternate mode by the ALT signal.
3. The colour-killer and PAL switch stage are controlled by the amplitude and colour-killer detection circuit using signals AC1 and CD.

COLOUR-CARRIER FREQUENCY REGENERATION

The regeneration of the colour-carrier frequency is performed by the phase-locked-loop (PLL) which comprises of a quadrature demodulator, low-pass filter, burst gate, loop filter 1 and divider/discrete time oscillator (DTO1). The DTO1 is controlled by the standard identification signals CCFR0 – CCFR1 and the Hue signal which influences the demodulation phase of the chrominance signal.

Synchronization path

In the synchronization circuit, prefilter synchronization is implemented to normalize the synchronization pulse slopes. A synchronization-slicer provides the detected synchronization pulses (SP) to the horizontal and vertical processing and phase detector stages.

HORIZONTAL AND VERTICAL PROCESSING

The horizontal and vertical processing comprises part of a PLL circuit for regeneration of the horizontal synchronization (HS) and an adaptive filter for detection of the vertical synchronization (VS). The horizontal and vertical processing also generates:

- coincidence signal HLOCK which controls the mute function
- standard identification signal FD which identifies nominal 525 or 625 lines per picture.

PHASE DETECTORS

The phase detectors that receive the SP signal, also part of the PLL, control the generation of the line-locked clock (PL). Loop filter 2, which has a variable bandwidth dependent on the time constant signal VTR, generates two increment signals (INC1 and INC2) with different delays. INC2 is programmable via the increment delay signal IDEL. INC1 corrects the regenerated subcarrier frequency at DTO1 and INC2 performs phase incrementing of DTO2. The crystal clock generator provides a stable 24.576 MHz clock input to DTO2 which in turn supplies the 4-bit DAC with a digital control signal of 432 or 429 times the line frequency. The analog output LFCO from the DAC is transmitted to the SAA9057 (CGC).

Output interface

The signals OES, OEY, OEC, CO, CI and CD control the output interface (see Fig.5). All but one of these signals are received via the I²C-bus, the exception being signal CD which is detected in the S-DMSD. A power-ON reset results in these signals being set to zero.

Table 1 OES signal

OES	OUTPUTS	OUTPUT STATUS
0	HS and VS	inactive (HIGH-impedance Z-state)
1	HS and VS	active

Table 2 CO, CI and CD signals

CO	CI	CD	OUTPUTS	OUTPUT STATUS
0	X	X	UV0 – UV3	colour OFF (zero)
1	0	0	UV0 – UV3	colour OFF (controlled by CD)
1	0	1	UV0 – UV3	colour ON (controlled by CD)
1	1	X	UV0 – UV3	colour forced ON

Where:

X = don't care.

$\overline{\text{FOE}}$ signal

In PIPCO (picture-in-picture controller, SAA9068) applications, the PIPCO requires access to the digital YUV-bus on a pixel time-base. This requirement is catered for by PIPCO generated signal $\overline{\text{FOE}}$, which forces all data output of the S-DMSD and DSD (SAA9056) into the HIGH-impedance Z-state. The $\overline{\text{FOE}}$ signal does not affect the synchronization data lines (HS and VS) or the blanking data line ($\overline{\text{BL}}$), see Fig.6.

FUNCTIONAL DISCRIPTION (continued)

Output interface (continued)

Table 3 OEC, OEY, $\overline{FOE}$, $\overline{BL}$, D1 – D7 and UV0 – UV3 signals

OEC	OEY	$\overline{FOE}$	$\overline{BL}$	D1 – D7	UV0 – UV3	REMARKS
0	0	X	HIZS	HIZS	HIZS	status after power-ON reset
1	1	1	active	HIZS	HIZS	
1	1	0	active	active	active	
0	1	1	active	HIZS	HIZS	
0	1	0	active	active	active	

Where:

X = don't care
HIZS = HIGH-impedance Z-state.

Note to Table 3

1. Combinations other than those shown in Table 3 are not allowed.

CS signal

The CS signal is transmitted from the digital SECAM decoder (DSD) during the H-blanking period and is received via the UV2 input (see Fig.5). The CS bit is read by the S-DMSD once per line at LL3 clock cycle number 748, see Fig.7.

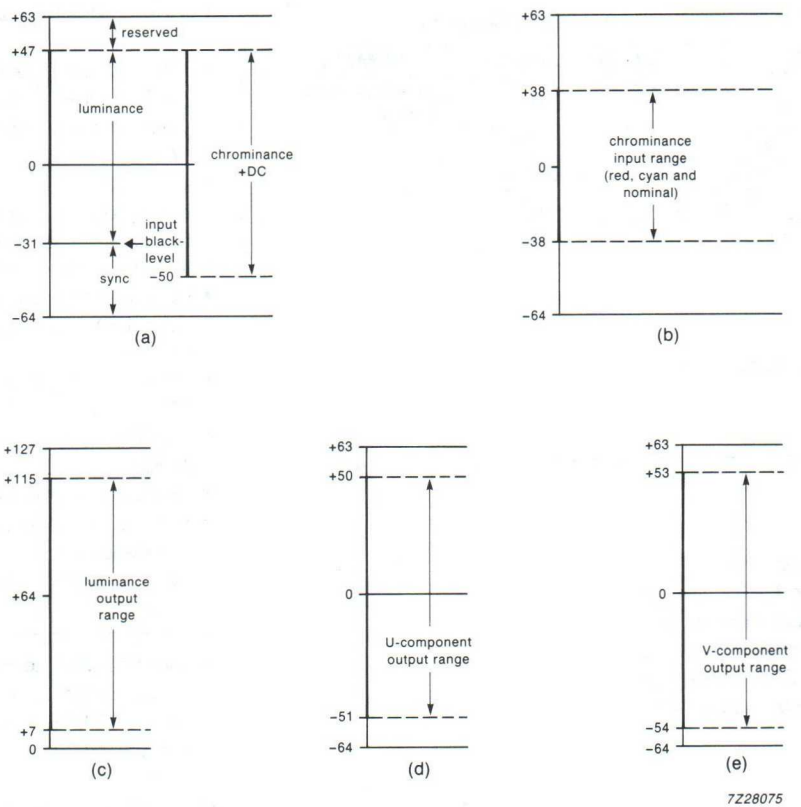
I²C bus interface (see Tables 1 to 3)

The following control signals are received via the I²C bus interface:

- standard identification signals (CCFR0, CCFR1, ALT, FS, YPN)
- video recorder/TV time constant (VTR)
- hue control (HUE)
- delay programming of the horizontal signals (HS, HC, HSY)
- increment-delay (IDEL)
- luminance aperture-correction control (BY, PF, BP2, COR2, COR1, AP2, AP1)
- luminance delay compensation (YDL0, YDL1, YDL2)
- fixed clock generation command (HPLL)
- internal colour ON/OFF (CO)
- internal colour forced ON, test purposes only (CI)
- synchronization output enable (OES)
- luminance output enable (OEY)
- chrominance output enable (OEC)
- switch signals (source select signals SS0, SS1, SS2, SS3)
- additional output for circuit control (AFCC)
- chrominance source select CVBS/ chrominance input/output (CT/ YC).
- SECAM chrominance delay compensation (SCDC0, SCDC21, SCDC2, SCDC3, SCDC4, SCDC5, SCDC6).

Signals transmitted from the S-DMSD via the I²C bus are:

- standard identification signals (FD, CS)
- colour-killer status signal (CD)
- coincidence information (HLOCK)
- power-on-reset of S-DMSD (PONRES).



(a) CVBS1 to CVBS7 input range

(b) IO1 to IO7 input range

(c) Y output range

(d) U output range –(B – Y)

(e) V output range –(R – Y)

Fig.3 Diagram showing input/output range of the S-DMSD; all levels in EBU colour bar, values in binary, 100% luminance and 75% chrominance amplitude.

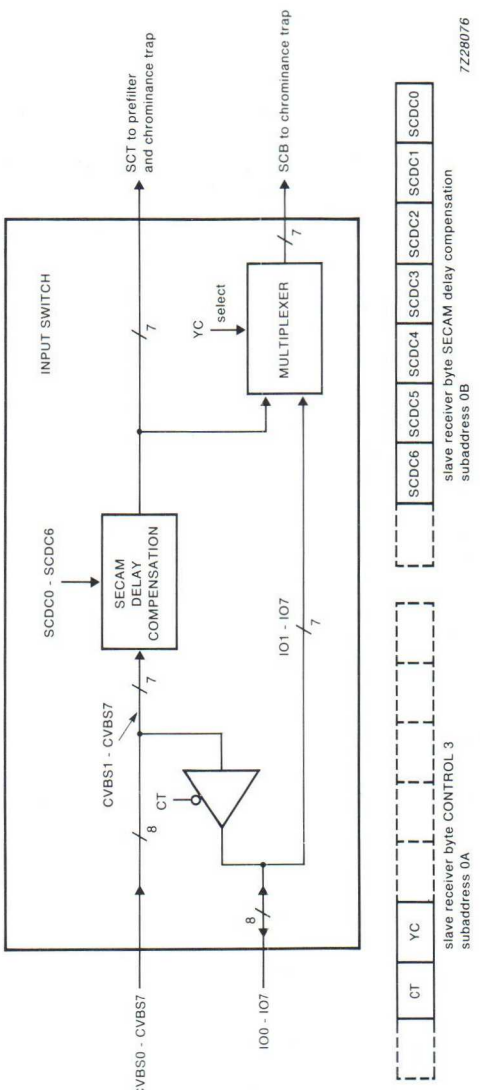


Fig.4 Schematic diagram of the input switch.

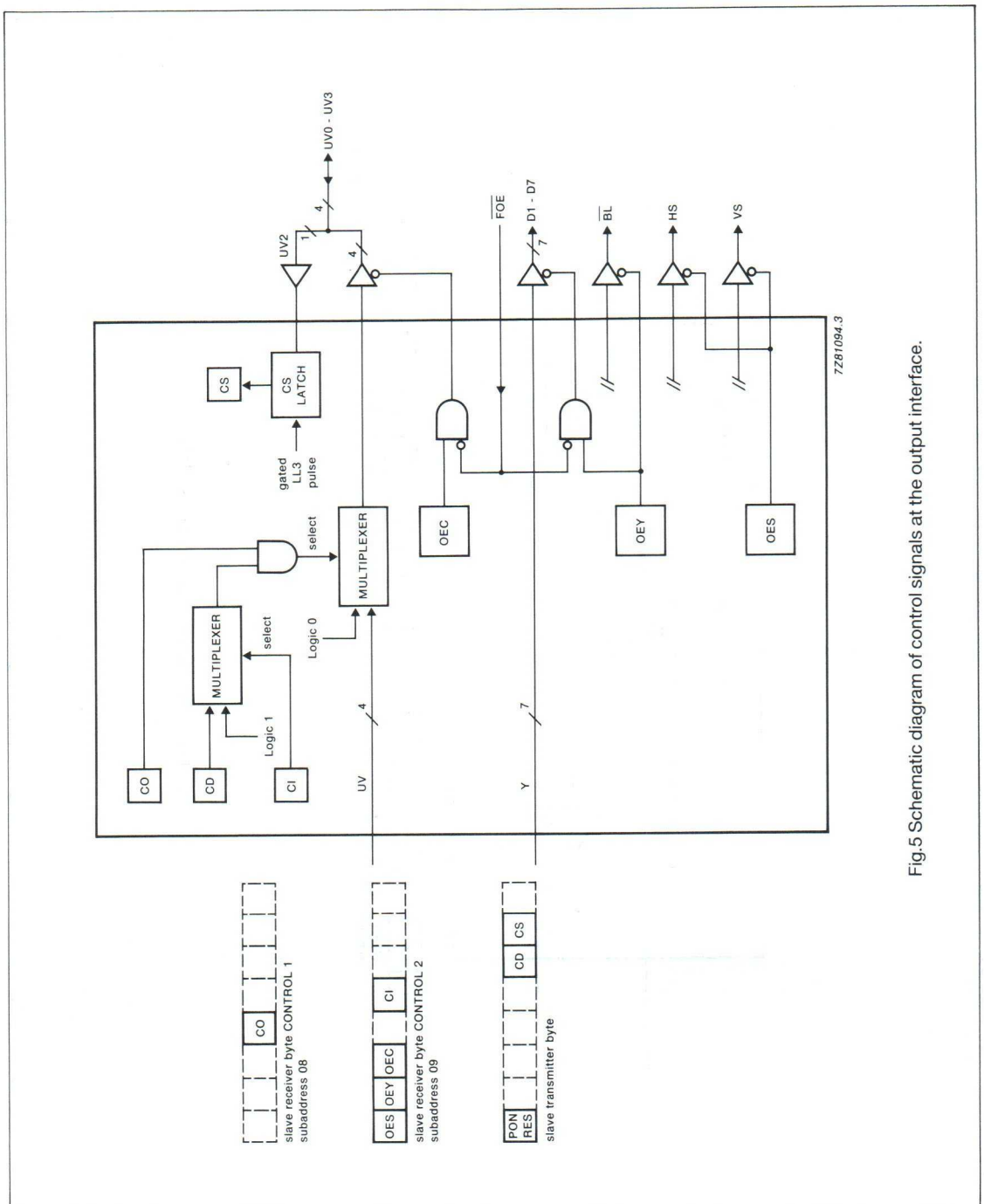


Fig.5 Schematic diagram of control signals at the output interface.

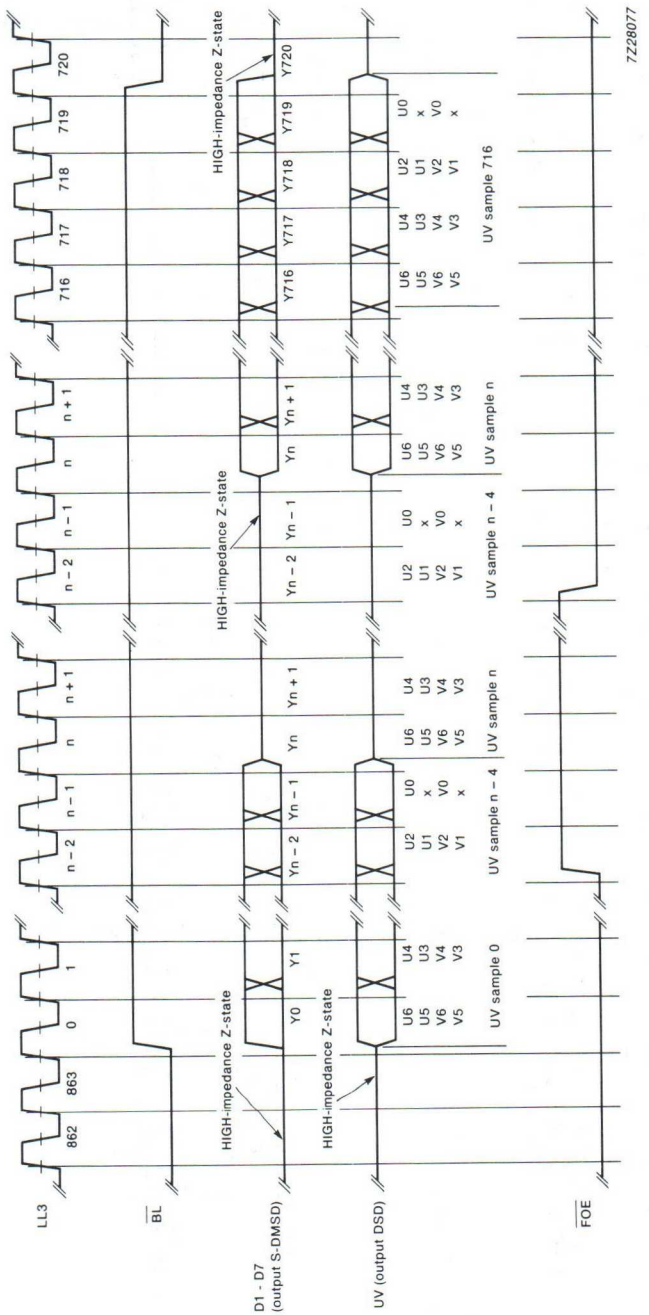
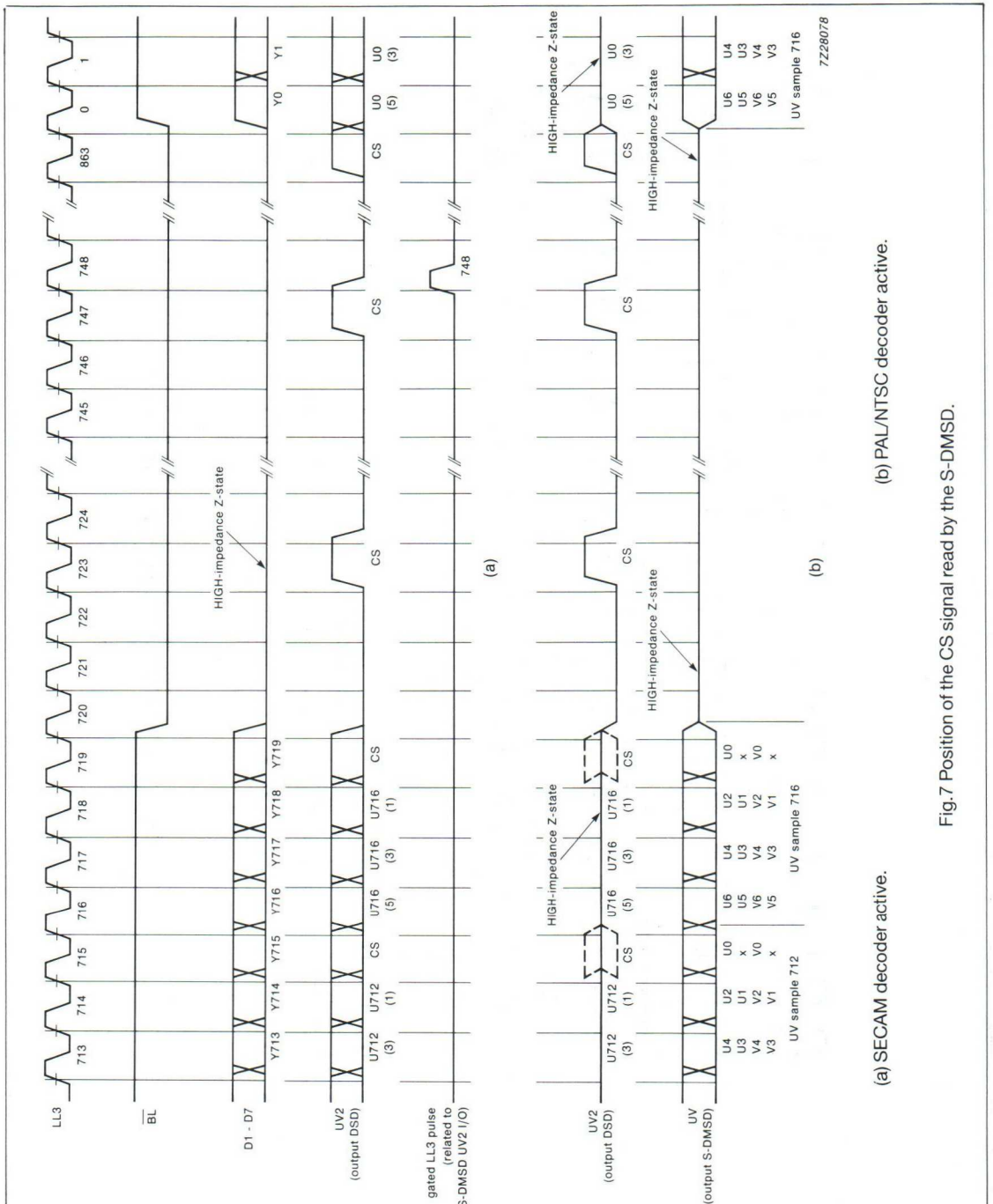


Fig.6 Timing waveform of the output data and $\overline{FOE}$ signals.



(a) SECAM decoder active.

(b) PAL/NTSC decoder active.

Fig.7 Position of the CS signal read by the S-DMSD.

SLAVE RECEIVER ORGANIZATION

Slave address and receiver format

There are two slave addresses, programmable via input SA, which determine the operating mode of the S-DMSD, see Table 4.

Table 4 Slave addresses

SLAVE RECEIVER ADDRESS								REMARKS
SA	A6	A5	A4	A3	A2	A1	A0	*	
0	1	0	0	0	1	0	1	0	binary value (8A hex)
1	1	0	0	0	1	1	1	0	binary value (8E hex)

Where:

* = logic 0, receiver mode
* = logic 1, transmitter mode.

Table 5 Subaddress byte and data byte formats

REGISTER FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Increment delay IDEL	00	A07	A06	A05	A04	A03	A02	A01	A00
HSY start time	01	A17	A16	A15	A14	A13	A12	A11	A10
HSY stop time	02	A27	A26	A25	A24	A23	A22	A21	A20
HC start time	03	A37	A36	A35	A34	A33	A32	A31	A30
HC stop time	04	A47	A46	A45	A44	A43	A42	A41	A40
HS start time (after PHI1)	05	A57	A56	A55	A54	A53	A52	A51	A50
Horizontal peaking	06	BY	PF	BP2	BP1	COR2	COR1	AP2	AP1
Hue control	07	A77	A76	A75	A74	A73	A72	A71	A70
Control 1	08	HPLL	FS	VTR	CO	ALT	YPN	CCFR1	CCFR0
Control 2	09	OES	OEY	OEC	X	CI	AFCC	SS1	SS0
Control 3	0A	SYC	CT	YC	SS3	SS2	YDL2	YDL1	YDL0
SECAM delay compensation	0B	X	SCDC6	SCDC5	SCDC4	SCDC3	SCDC2	SCDC1	SCDC0
Reserved	0C – 0F	X	X	X	X	X	X	X	X

Where:

X = don't care.

Notes to Table 5

The subaddress is automatically incremented. This enables quick initialization, within one transmission, by the I²C-bus controller.

The subaddresses shown are acknowledged by the device. Subaddresses 10 to 1F (reserved for the SECAM decoder SAA9056) are not acknowledged. The subaddress counter wraps-around from 1F to 00. Subaddresses 20 to FF are not allowed.

After power-on-reset the control registers 1 to 3 (subaddresses 08, 09 and 0A) are, with the exception of bits YDL0 – YDL2 of counter 3, set to logic 0. All other registers are undefined.

The least significant bit of an analog control or alignment register is defined as AX0.

SUBADDRESS 00

Table 6 Increment delay control IDEL (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/13.5 MHz = 148 ns)	CONTROL BITS*							
		A07	A06	A05	A04	A03	A02	A01	A00
–1 to –110	–148 ns (min. value)	1	1	1	1	1	1	1	1
–1 to –110	–16.3 µs (outside available range)	1	0	0	1	0	0	1	0
–111 to –214	–16.44 µs	1	0	0	1	0	0	0	1
–111 to –214	–31.7 µs (max. value if FS = logic 1)	0	0	1	0	1	0	1	0
–215	–31.85 µs (outside central counter range if FS = logic 1)**		0		0		1		0
–216	–32 µs (max. value if FS = logic 0)**	0	0	1	0	1	0	0	0
–217 to –256	–32.148 µs (outside central counter if FS = logic 0)**		0		0		1		0
–217 to –256	–37.9 µs (outside central counter)**	0	0	0	0	0	0	0	0

Where:

* A sign bit, designated A08 and internally set to HIGH, indicate values are always negative.

** The horizontal PLL does not operate in this condition. The system clock frequency is set to a value fixed by the last update and is within ±7.1% of the nominal frequency.

SUBADDRESS 01

Table 7 Horizontal synchronization HSY start time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 1/13.5 MHz = 74 ns)	CONTROL BITS							
		A17	A16	A15	A14	A13	A12	A11	A10
+ 191 to + 1	–14.2 µs (max. negative value)	1	0	1	1	1	1	1	1
+ 191 to + 1	–0.074 µs	0	0	0	0	0	0	0	1
0	0 µs reference point	0	0	0	0	0	0	0	0
–1 to –64	+0.074 µs	1	1	1	1	1	1	1	1
–1 to –64	+4.7 µs (max. positive value)	1	1	0	0	0	0	0	0

SUBADDRESS 02

Table 8 Horizontal synchronization HSY stop time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/13.5 MHz = 148 ns)	CONTROL BITS							
		A27	A26	A25	A24	A23	A22	A21	A20
+ 191 to + 1	−14.2 μs (max. negative value)	1	0	1	1	1	1	1	1
+ 191 to + 1	−0.074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1 to −64	+0.074 μs	1	1	1	1	1	1	1	1
−1 to −64	+4.7 μs (max. positive value)	1	1	0	0	0	0	0	0

SUBADDRESS 03

Table 9 Horizontal clamp HC start time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/13.5 MHz = 148 ns)	CONTROL BITS							
		A37	A36	A35	A34	A33	A32	A31	A30
+ 127 to + 1	−9.4 μs (max. negative value)	0	1	1	1	1	1	1	1
+ 127 to + 1	−0.074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1 to −128	+0.074 μs	1	1	1	1	1	1	1	1
−1 to −128	+9.5 μs (max. positive value)	1	0	0	0	0	0	0	0

SUBADDRESS 04

Table 10 Horizontal clamp HC stop time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/13.5 MHz = 148 ns)	CONTROL BITS							
		A47	A46	A45	A44	A43	A42	A41	A40
+ 127 to + 1	−9.4 μs (max. negative value)	0	1	1	1	1	1	1	1
+ 127 to + 1	−0.074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1 to −128	+0.074 μs	1	1	1	1	1	1	1	1
−1 to −128	+9.5 μs (max. positive value)	1	0	0	0	0	0	0	0

SUBADDRESS 05

Table 11 Horizontal synchronization HS start time after PHI1 (application dependent); 50 Hz; 625 lines (FS = 0)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 4/13.5 MHz = 296 ns)	CONTROL BITS							
		A57	A56	A55	A54	A53	A52	A51	A50
+ 127 to + 109	Forbidden; outside available central counter range		0		1		1		1
+ 127 to + 109	Forbidden; outside available central counter range		0		1		1		0
+ 108 to + 1	−32 µs (max. negative value)	0	1	1	0	1	1	0	0
+ 108 to + 1	−0.296 µs	0	0	0	0	0	0	0	1
0	0 µs reference point	0	0	0	0	0	0	0	0
−1 to −107	+0.296 µs	1	1	1	1	1	1	1	1
−1 to −107	+31.7 µs (max. pos. value)	1	0	0	1	0	1	0	1
−108 to −128	Forbidden; outside available central counter range		1		0		0		1
−108 to −128	Forbidden; outside available central counter range		1		0		0		0

Table 12 Horizontal synchronization start time after PHI1 (application dependent); 60 Hz; 525 lines (FS = 1)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 4/13.5 MHz = 296 ns)	CONTROL BITS							
		A57	A56	A55	A54	A53	A52	A51	A50
+ 127 to + 107	Forbidden; outside available central counter range		0		1		1		1
+ 127 to + 107	Forbidden; outside available central counter range		0		1		1		0
+ 106 to + 1	−31.8 µs (max. negative value)	0	1	1	0	1	0	1	0
+ 106 to + 1	−0.294 µs	0	0	0	0	0	0	0	1
0	0 µs reference point	0	0	0	0	0	0	0	0
−1 to −107	+0.294 µs	1	1	1	1	1	1	1	1
−1 to −107	+31.5 µs (max. pos. value)	1	0	0	1	0	1	0	1
−108 to −128	Forbidden; outside available central counter range		1		0		0		1
−108 to −128	Forbidden; outside available central counter range		1		0		0		0

Programming IDEL, HSY, HC and HS

The variables IDEL, HSY, HC and HS are programmed using data words via the I²C-bus. In the following examples a decrease in value corresponds to an increase in time.

IDEL (Fig.8)

The IDEL data word compensates for the time delays in data processing between loop filter 2, quadrature demodulator and internal/external (system) signal paths. The internal delay (t_{REF}) is the period required for INC1 to pass from the loop filter 2, through the divider and through DTO1. This delay corrects the relationship between the subcarrier frequency and the line frequency. The external path is a result of the following time delays (time delay is given in term of LL3 clock cycles):

- t_{IDEL}; programmable delay time
- t_a; processing time of DTO2 and the DAC
- t_b; chrominance bandpass and gain control stage delay times
- t_{CGC}; clock generator circuit delay time
- t_{ADC}; analog-to-digital converter delay time
- t_{INP}; input switch delay time.

As delay t_a and t_b are known constants, t_{IDEL} is programmed, range of −115 to −214/216 LL3 clock cycles, as follows:

- $t_{IDEL} = -115 - 0.5$ (* - $t_{CGC} - t_{ADC} - t_{INP}$).

HSY

Referring to Fig.9 point (1) and periods a and b:

- HSY start time = $t_{(1)}$ − a (LL3 clock cycles)
- HSY stop time = $t_{(1)}$ − b (LL3 clock cycles)

Programming range of HSY start/stop time: +191 to −64 (LL3 clock cycles).

HC

Referring to Fig.9 point (1) and periods c and d:

- HC start time = $t_{(1)}$ − c (LL3 clock cycles)
- HC stop time = $t_{(1)}$ − d (LL3 clock cycles)

Programming range of HSY start/stop time: +127 to −128 (LL3 clock cycles).

HS

The HS reference positions in PAL and NTSC modes are shown in Fig.9 at points (3) and (4) respectively. To move the HS pulse to the centre of blanking pulse BL the following equation is used:

- HS (NTSC);

  position of HS relative to the zero point (LL3 clock cycles)
  4 LL3 clock cycles

- HS (PAL);

  position of HS relative to the zero point (LL3 clock cycles)
  4 LL3 clock cycles

The length of HS is 64 LL3 clock cycles.

* Value to be fixed.

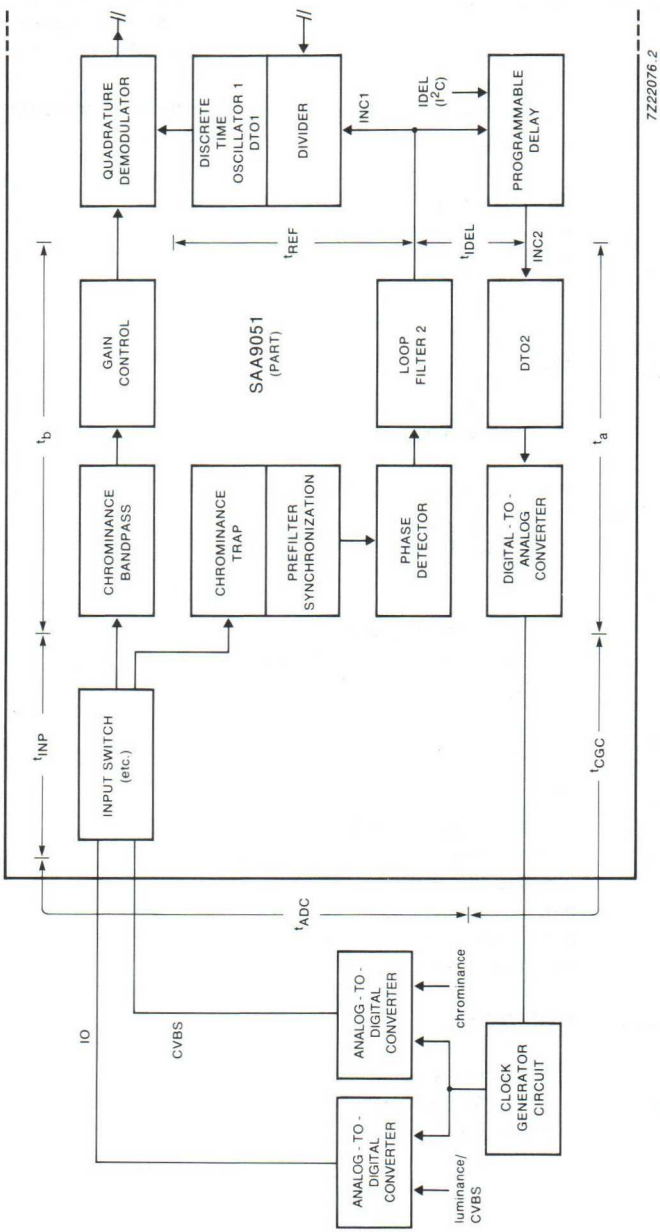
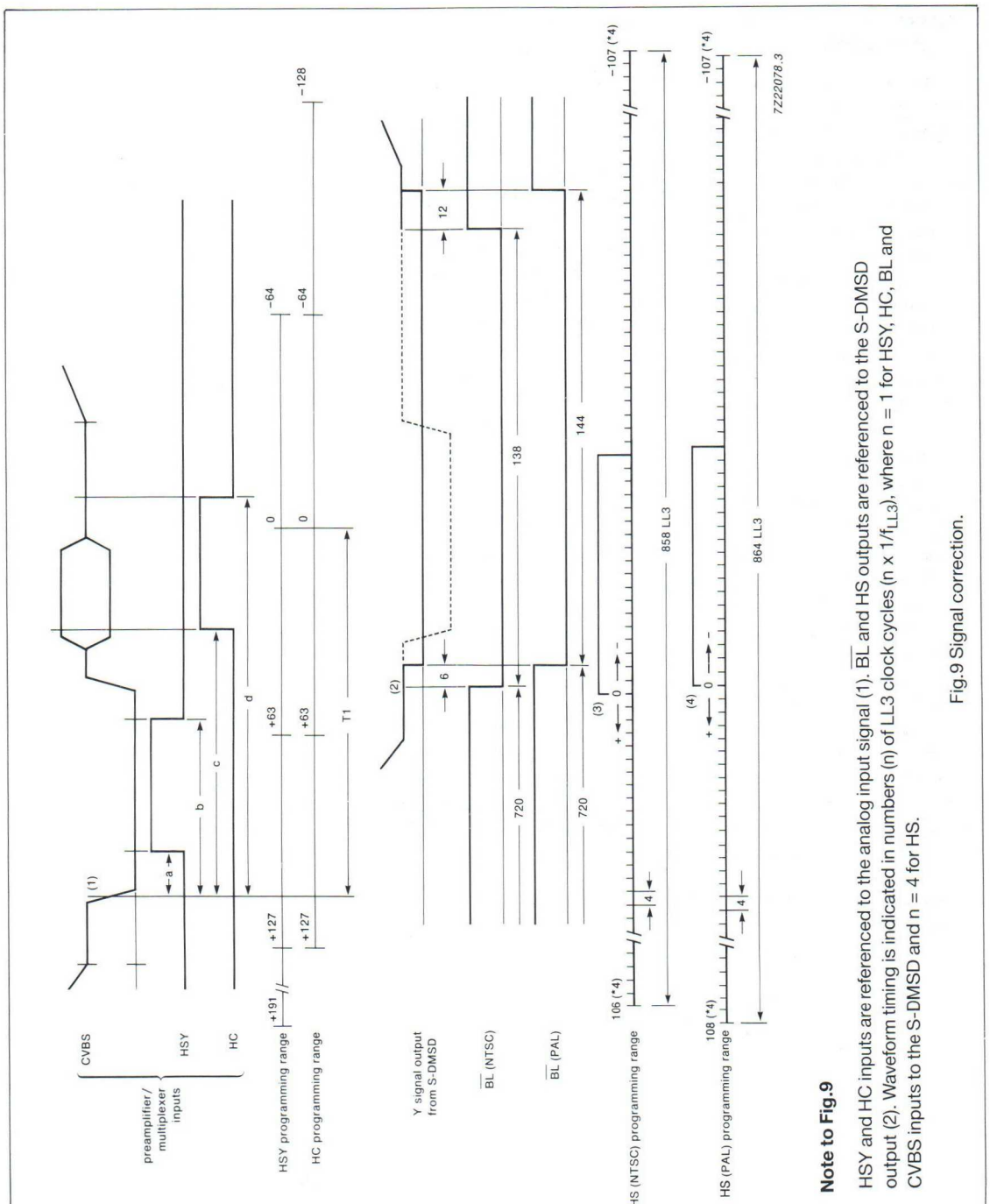


Fig.8 Compensation of delay times by incrementing delay control IDEL.



Note to Fig.9

HSY and HC inputs are referenced to the analog input signal (1). $\overline{BL}$ and HS outputs are referenced to the S-DMSD output (2). Waveform timing is indicated in numbers (n) of LL3 clock cycles ($n \times 1/f_{LL3}$), where n = 1 for HSY, HC, BL and CVBS inputs to the S-DMSD and n = 4 for HS.

Fig.9 Signal correction.

Programming of the luminance path of the S-DMSD

The VBS (without chrominance) or CVBS input signal enters the prefilter (a high-pass transfer function with maximum amplification of 9.5 dB). The control bit PF switches the filter into the bypass mode. The next stage is the chrominance trap which can be programmed (zero point) to 4.43 MHz (PAL) or 3.58 MHz (NTSC) by the control bit YPN. Bit BY activates the bypass function for the YUV mode of the S-DMSD. The chrominance trap output signal is then divided into three channels:

- Channel 1 signal; The channel 1 signal is transmitted to the programmable bandpass filter where the high luminance frequencies are removed, the centre frequency is programmable via bits BP1 and BP2. The signal BC is transmitted to the coring (corner correction) stage where low amplitude noise is removed, the amount of low amplitude noise removal is programmable via bits COR1 and COR2. The signal HF is transmitted to the weighting stage and adding stage, see 'Combining channel 1 and channel 2 signals'.
- Channel 2 signal; The channel 2 signal is transmitted to the fixed delay compensation stage where delay compensation and black level adjustment occurs. The signal DCA is transmitted to the weighting and adding stage, see section 'Combining channel 1 and channel 2 signals'.
- Combining Channel 1 and Channel 2 signals; The channel 1 signal HF is weighted, programmable via bits AP2 and AP1 and added to the Channel 2 signal DCA. The combined signals are matched to the specified amplitude and the word size is reduced to 7-bits. The signal AVD is transmitted to the variable delay compensation stage where compensation for IF group delays occurs, the amount of delay is programmable (from −4 to +3 LL3 clock cycles, see note) via bits YDL0 – YDL2. The signal Y is transmitted to the time multiplexed interface where the signal is output via D1 – D7.

Note

Differences in the delay compensation required for PAL and NTSC are catered for by identification signal YPN which switches the chrominance trap to the appropriate colour-carrier frequency 3.58 MHz or 4.43 MHz.

- Channel 3 signal; The channel 3 signal VB is transmitted to the pre-filter synchronization stage, see section 'Synchronization path'.

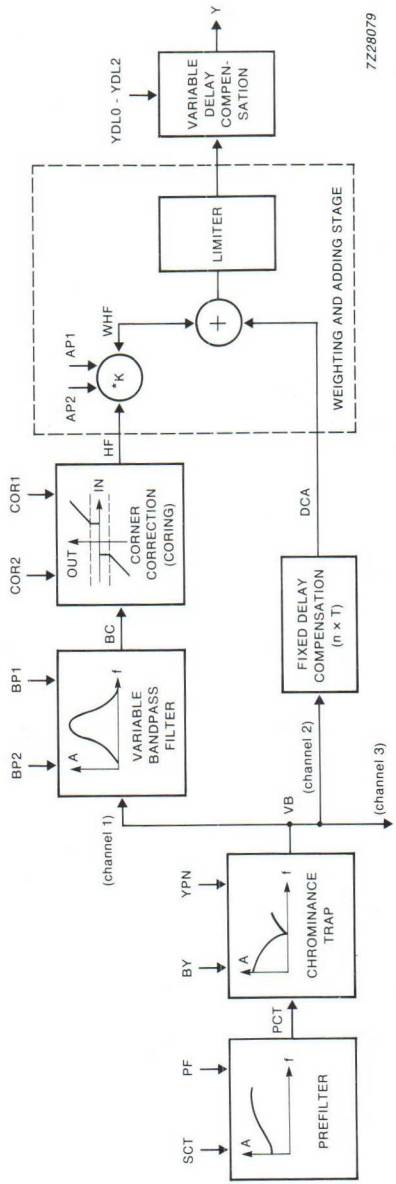


Fig. 10 Luminance path of the S-DMSD.

SUBADDRESS 06

Table 13 Chrominance trap select (BY switches the chrominance trap to the bypass mode; YPN selects the notch-frequency)

PREFILTER	CONTROL BITS	
	BY	YPN
PAL (4.43 MHz)	0	0
NTSC (3.58 MHz)	0	1
bypass	1	X

Table 14 Disconnecting the luminance prefilter (user dependent)

PREFILTER	CONTROL BIT PF
ON	0
OFF	1

Table 15 Bandpass control (BP1 and BP2 control the centre frequency of the bandpass filter, see Figs 12 to 15)

BANDPASS TYPE (CENTRE FREQUENCY)	CONTROL BITS	
	BP2	BP1
type 1 (4.1 MHz)	0	0
type 2 (3.8 MHz)	0	1
type 3 (2.6 MHz)	1	0
type 4 (2.9 MHz)	1	1

Table 16 Coring threshold level (COR1 and COR2 control the suppression of low amplitude and high frequency signal components, see Fig.11)

THRESHOLD	CONTROL BITS	
	COR2	COR1
coring off	0	0
coring on (–8 to 7 LSB)	0	1
coring on (–16 to 15 LSB)	1	0
coring on (–32 to 31 LSB)	1	1

Note to Table 16

The thresholds are related the word width of the bandpass filter (12 bits).

Table 17 Aperture correction factor (AP1 and AP2 select the weighting factor K of the high frequency (HF) luminance components, see Fig.10)

WEIGHTING FACTOR K	CONTROL BITS	
	AP2	AP1
0.	0	0
0.25	0	1
0.5	1	0
1.	1	1

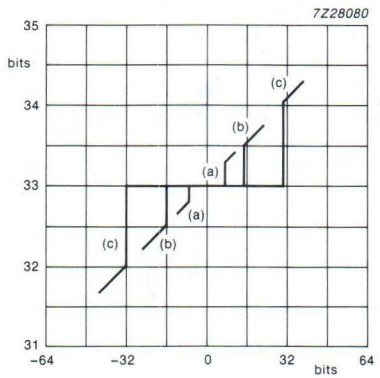


Fig.11 Coring stage response; (a) for COR2 = 0 and COR1 = 1; (b) for COR2 = 1 and COR1 = 0; (c) for COR2 = 1 and COR1 = 1.

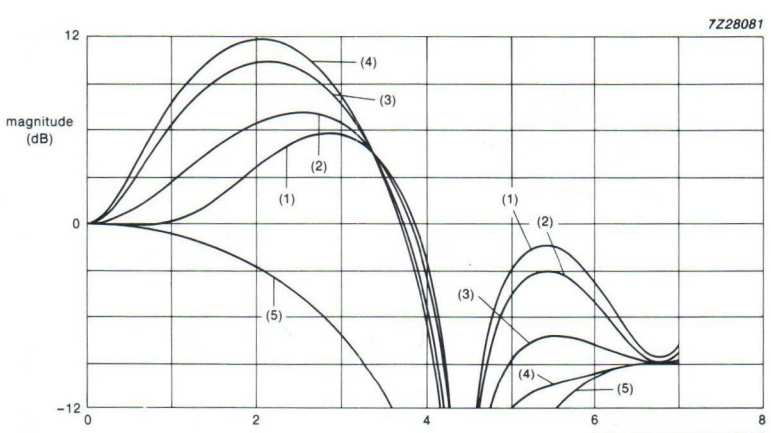


Fig.12 Magnitude of the frequency response of the unlimited summation signal (combining channel 1 and channel 2); PAL mode; prefilter OFF; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

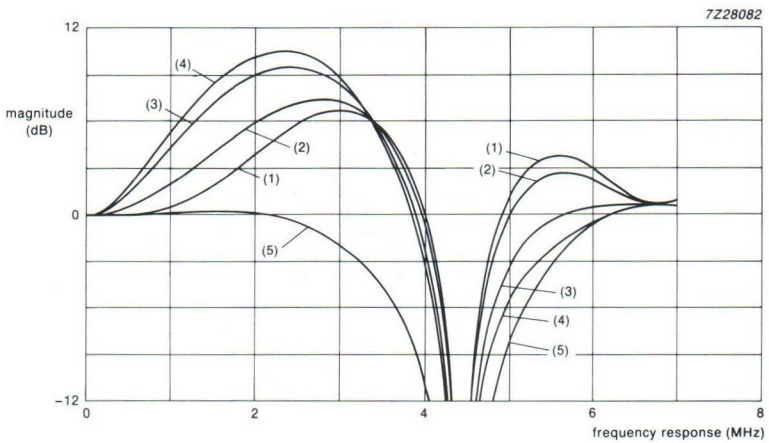


Fig.13 Magnitude of the frequency response of the unlimited summation signal (combining channel 1 and channel 2); PAL mode; prefilter ON; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

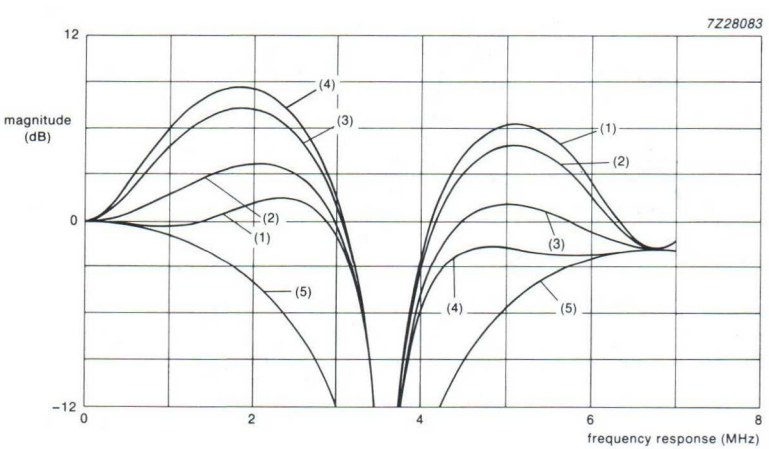


Fig.14 Magnitude of the frequency response of the unlimited summation signal (combining channel 1 and channel 2); NTSC mode; prefilter OFF; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

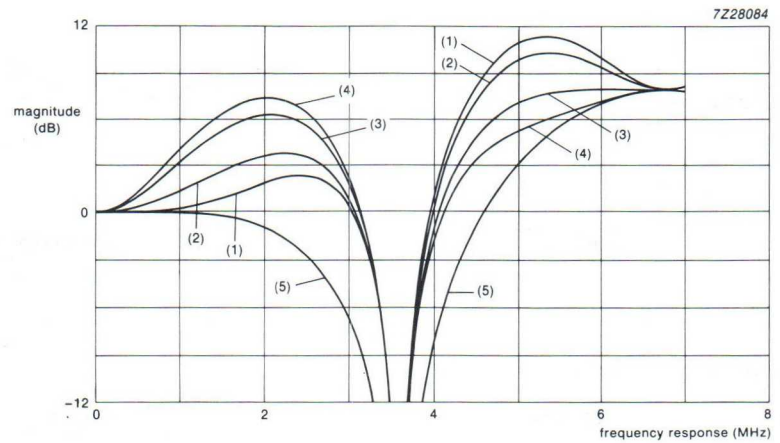


Fig.15 Magnitude of the frequency response of the unlimited summation signal (combining channel 1 and channel 2); NTSC mode; prefilter ON; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

SUBADDRESS 07

Table 18 Hue phase (user dependent, see notes 1 to 3)

HUE PHASE (deg)	CONTROL BITS							
	A77	A76	A75	A74	A73	A72	A71	A70
+ 178.6 to 0	1	1	1	1	1	1	1	1
0.	1	0	0	0	0	0	0	0
0. to −180	0	0	0	0	0	0	0	0

Notes to Table 18

1. Step size per least significant bit (A70) = 1.4 degree.
2. Reference point for positive colour difference signals = 0 degree.
3. The hue phase may be shifted ±180 degrees from the reference point using bit A77, the colour difference signals are then switched from normally positive to negative polarity.

SUBADDRESS 08

Table 19 Horizontal clock PLL (application dependent)

FUNCTION	HPLL CONTROL BIT
horizontal clock PLL open, horizontal frequency fixed	1
horizontal clock PLL closed	0

Table 20 Field frequency select (system mode dependent)

FUNCTION	CONTROL BIT FS
60 Hz; 525-line mode	1
50 Hz; 625-line mode	0

Table 21 VTR/TV mode select (system mode dependent)

FUNCTION	CONTROL BIT VTR
VTR mode	1
TV mode	0

Table 22 Colour on control (system mode dependent)

FUNCTION	CONTROL BIT CO
colour ON	1
colour OFF (all colour output samples zero)	0

Table 23 Alternate/non–alternate mode (system mode dependent)

FUNCTION	CONTROL BIT ALT
alternate mode (PAL)	1
non-alternate mode (NTSC)	0

Table 24 Chrominance trap select and amplitude matching (system mode dependent)

CHROMINANCE TRAP	CONTROL BIT YPN
3.58 MHz	1
4.43 MHz	0

Table 25 Colour carrier frequency control (system mode dependent)

COLOUR CARRIER FREQUENCY	CONTROL BITS	
	CCFR1	CCFR0
4 433 618.75 Hz (PAL-B, G, H, 1; NTSC 4.43)	0	0
3 575 611.49 Hz (PAL-M)	0	1
3 582 056.25 Hz (PAL-N)	1	0
3 579 545 Hz (NTSC-M)	1	1

SUBADDRESS 09

Table 26 Synchronization output enable (system mode dependent)

FUNCTION	CONTROL BIT OES
outputs HS and VS active	1
outputs HS and VS HIGH-impedance Z-state	0

Table 27 Y-output enable (system mode dependent)

FUNCTION	CONTROL BIT OEY
outputs D0 – D6 and $\overline{BL}$ active	1
outputs D0 – D6 and $\overline{BL}$ HIGH-impedance Z-state	0

Table 28 Chrominance output enable (system mode dependent)

FUNCTION	CONTROL BIT OEC
outputs UV0 – UV3 active; if CD = logic 1, chrominance signal output; if CD = logic 1, zero signal	1
outputs UV0 – UV3 HIGH-impedance Z-state	0

Table 29 Internal colour forced ON/OFF (test purposes only)

FUNCTION	CONTROL BIT CI
colour forced ON, if CO = logic 1 (CD = X) or colour OFF, if CO = logic 0 (CD = X)	1
colour OFF, if CO = logic 0 (CD = X) or colour controlled by CD, if CO = logic 1	0

Where:

X = don't care.

Table 30 Additional output for circuit control

FUNCTION	CONTROL BIT AFCC
output AFCC = HIGH	1
output AFCC = LOW	0

Table 31 Source-select (system mode dependent)

FUNCTION	CONTROL BIT SS0 – SS3
output SS0 – SS3 = HIGH	1
output SS0 – SS3 = LOW	0

Note to Table 31

SS2 and SS3 are part of subaddress 0A.

SUBADDRESS 0A

Table 32 Disabling of HSY and HC pulses (system mode dependent)

FUNCTION	CONTROL BIT SYC
HYS and HC output pulses disabled	1
HSY and HC output pulses enabled	0

Table 33 Chrominance input/output 3-state control

FUNCTION	CONTROL BIT CT
CVBS output active	1
output HIGH-impedance Z-state	0

Table 34 Chrominance source select

FUNCTION	CONTROL BIT YC
Y/C separate inputs	1
CVBS input	0

Table 35 Variable delay compensation of the luminance path (YDL0 – YDL2 control the luminance delay in order to compensate different chrominance delays throughout the system)

DELAY (N =)	CONTROL BITS		
	YDL2	YDL1	YDL0
0	0	0	0
+ 1	0	0	1
+ 2	0	1	0
+ 3	0	1	1
− 4	1	0	0
− 3	1	0	1
− 2	1	1	0
− 1	1	1	1

Note to Table 35

The delay is given in terms of clock cycles:

- 13.5 MHz = N x 74 ns.

SUBADDRESS 0B

Table 36 SECAM chrominance delay compensation (system mode dependent)

PROGRAMMABLE DELAY*	CONTROL BITS						
	SCDC6	SCDC5	SCDC4	SCDC3	SCDC2	SCDC1	SCDC0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.
4	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.
8	0	0	0	1	0	0	0
.	.	.	.	.	.	.	.
16	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.
32	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.
63	0	1	1	1	1	1	1
64	1	1	1	0	0	0	0
65	1	1	1	0	0	0	1
.	.	.	.	.	.	.	.
79	1	1	1	1	1	1	1
Maximum delay selected by single control bit							
	16	32	16	8	4	2	1

* Delay in number of LL3 clock cycles.

SLAVE TRANSMITTER ORGANIZATION

Slave transmitter format

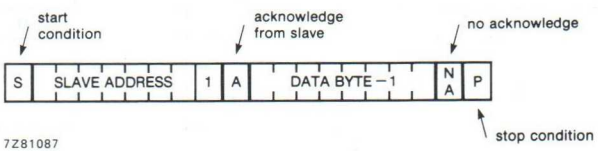


Fig.16 Slave transmitter format (a general call address is not acknowledged).

Note to Fig.16

Data bits D0, D3 and D5 are inverted in slave transmitter byte.

The format of data byte 1 is:

D7	D6	D5	D4	D3	D2	D1	D0
PONRES	HLOCK	1	FD	0	CD	CS	0

Table 37 Description of data byte 1

BIT	DESCRIPTION
PONRES	Status bit for power-on-reset ($\overline{RES}$) and after a power failure. logic 1 after the first power-on-reset and after a power failure. Also set to logic 1 after a severe voltage dip that may have disturbed slave receiver data in the PAL/NTSC decoder (SAA9050). PONRES sets all data bits of control registers 1 and 2 to zero. logic 0 after a successful read of the PAL/NTSC decoder status byte
HLOCK	Status bit for horizontal frequency lock (transmitter identification, stop or mute bit): logic 1 if horizontal frequency is not locked (no transmitter available); logic 0 if horizontal frequency is locked (transmitter received)
FD	Detected field frequency status bit: logic 1 when received signal has 60 Hz synchronization pulses; logic 0 when received signal has 50 Hz synchronization pulses
CD	PAL/NTSC colour-detected status bit: logic 1 when PAL/NTSC colour signal is detected; logic 0 when no PAL/NTSC colour signal is detected
CS	SECAM colour-detected status bit: logic 1 when SECAM colour signal is detected; logic 0 when no SECAM colour signal is detected.

Default coefficients set for the S-DMSD and SAA9056

The default coefficients are set for operation with the TDA8703 or TDA8708, these devices are analog-to-digital converters with built-in sample rate converter. The 3-state outputs of the chrominance ADC are controlled by the SS3 switch in this example (all numbers are hex values).

The slave addresses are as follows:

- S-DMSD; 8A or 8E
- SAA9056; 8A or 8E

Table 38 Slave address (SAA9051 part)

SUBADDRESS	FUNCTION	SHORT DELAY	LONG DELAY
00	inc. delay	5E	7E
01	HSY start	37	73
02	HSY stop	07	43
03	HC start	F6	32
04	HC stop	C7	03
05	HS start	FF	FF
06	H-peaking	02	02
07	HUE control	00	00
08	control 1	38 (77 NTSC)	38 (77 NTSC)
09	control 2	E3	E3 (D3 SECAM)
0A	control 3	58 (28 YUV mode)	58 (28 YUV mode)
0B	SECAM delay	00	3C

Notes to Table 38

1. Subaddress 05; application dependent.
2. Subaddress 08; HPLL is in the VTR mode. Hex value for TV mode is 18 (58 for NTSC).

Table 39 Slave address (SAA9056 part)

SUBADDRESS	FUNCTION	VALUE
10	luminance delay	C0 – FF
11	$\overline{BL}$ delay	00
12	burst gate start	42
13	burst gate stop	56
14	sensitivity	20
15	filter	24
16	control	00 (02 active)

Note to Table 39

Subaddress 16; set to 04 when used in conjunction with SAA9056 and the CS bit is to be transmitted in the horizontal blanking.

Table 40 Operating modes of the S-DMSD

INPUT	CT	YC	SS3	CE	SCDC	IDEL	YPN	BY	FS	ALT	CCFR1	CCFR0	REMARKS
PAL B, G, H, I													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	0	0	0	1	0	0	
YUV	0	1	0	0	A	A	0 (1)	1	0	1	0	0	
PAL M													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	1	0	1	1	0	1	
YUV	0	1	0	0	A	A	1 (0)	1	1	1	0	1	
PAL N													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	0	0	0	1	1	0	
YUV	0	1	0	0	A	A	0 (1)	1	0	1	1	0	
SECAM													
CVBS	1	0 (1)	1	1	B	B	0	0	0	0 (1)	0 (1)	0 (1)	
YUV	0	1 (0)	0	1	B	B	0 (1)	1	0	0 (1)	0 (1)	0 (1)	
NTSC 4.43 MHz													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	0	0	0	0	0	0	use FS = 1 for 60 Hz vertical frequency
YUV	0	1	0	0	A	A	0 (1)	1	1	0	0	0	use FS = 1 for 60 Hz vertical frequency
NTSC M													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	1	0	1	0	1	1	
YUV	0	1	0	0	A	A	1 (0)	1	1	0	1	1	

Where:

A = short time delay.
B = long time delay.

Notes to Table 40

1. SS3 is assumed to control the 3-state output of the chrominance ADC (active LOW).
2. To avoid data collision care must be taken with the programming of CT and SS3 (in this equal they are always equal).

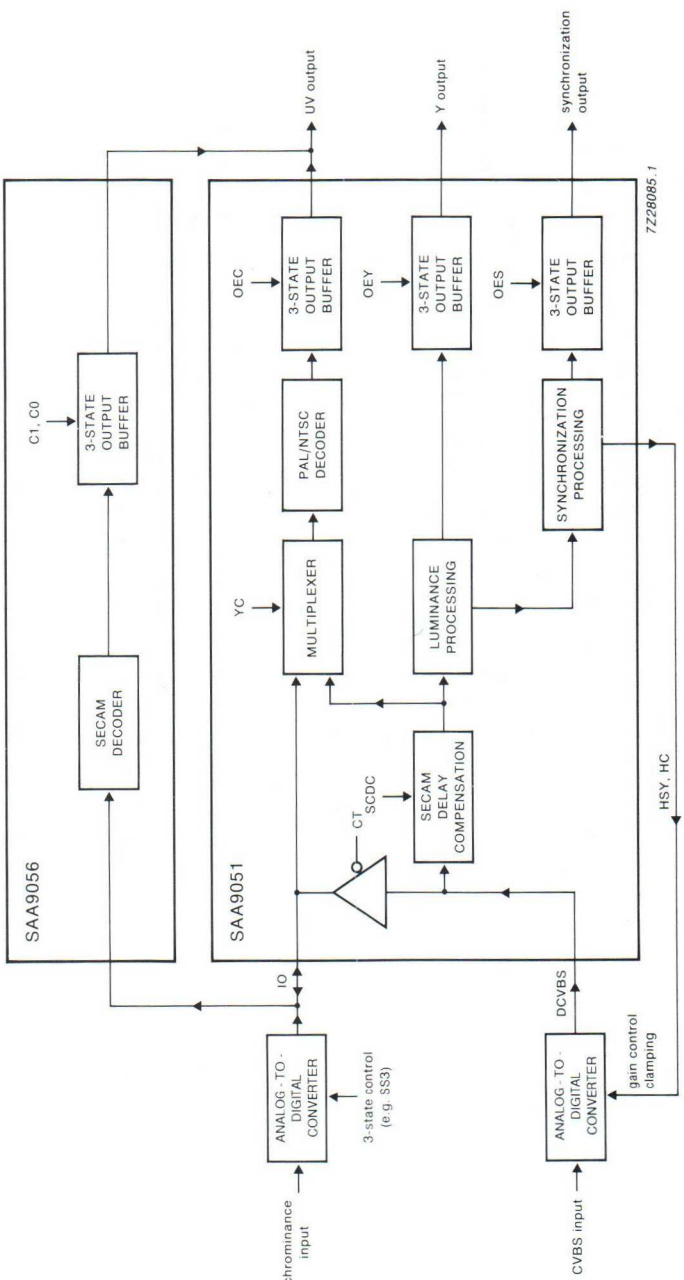
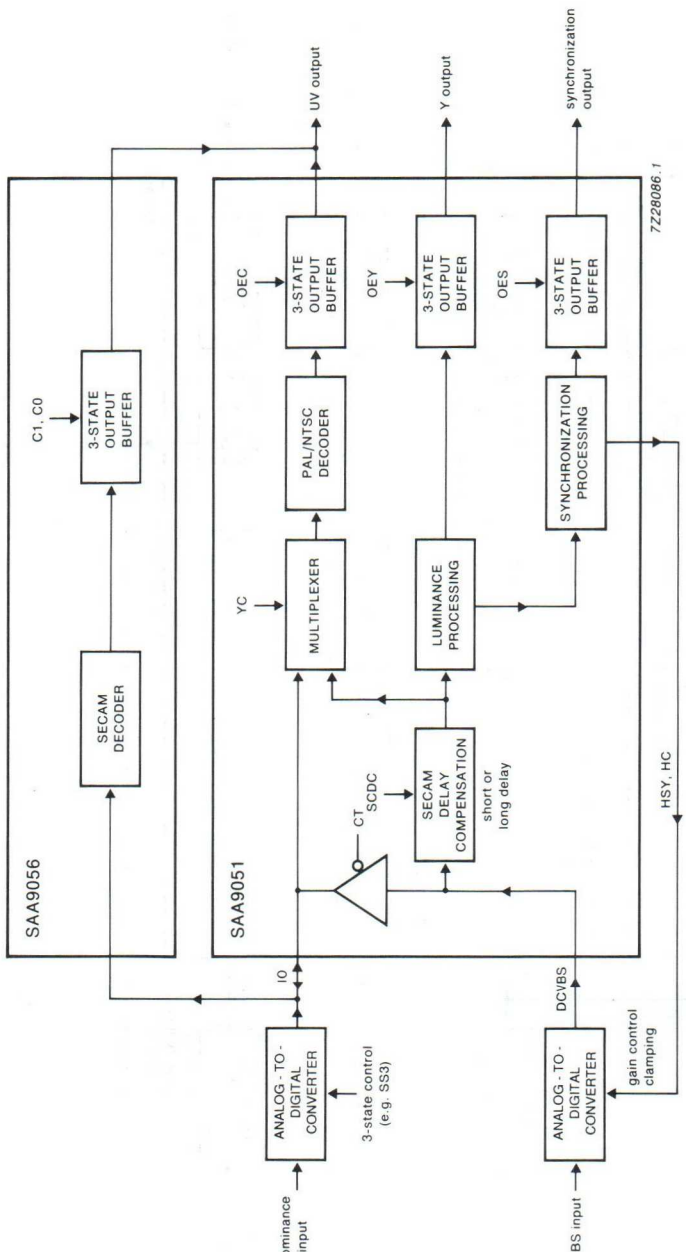
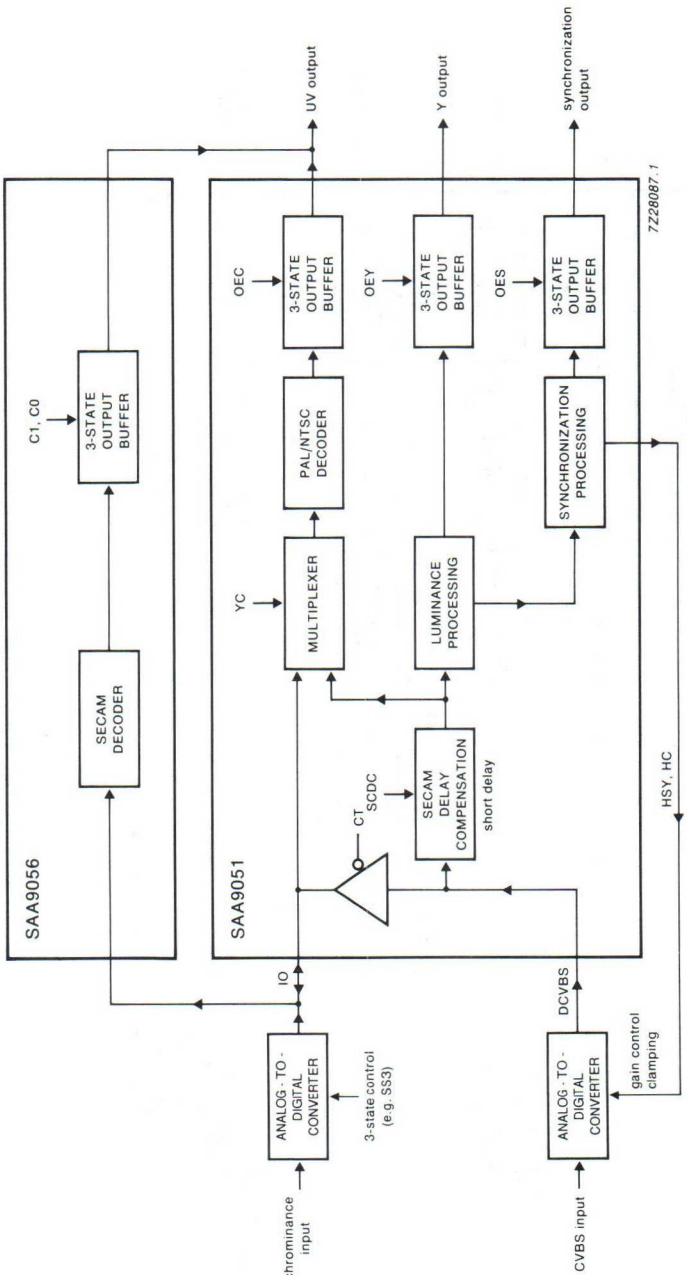


Fig.17 SAA9051 signal flow when used in conjunction with SAA9056.



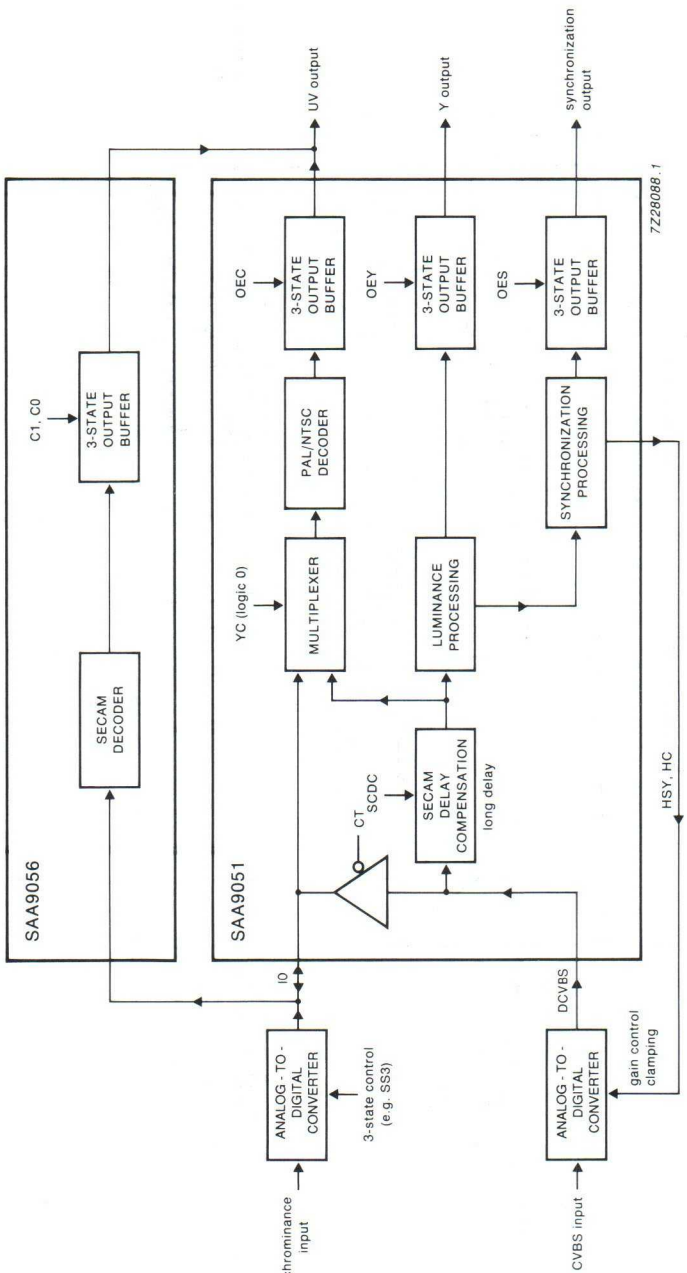
(a) PAL or NTSC with CVBS input signal.

Fig.18 Signal flow in different operating modes.



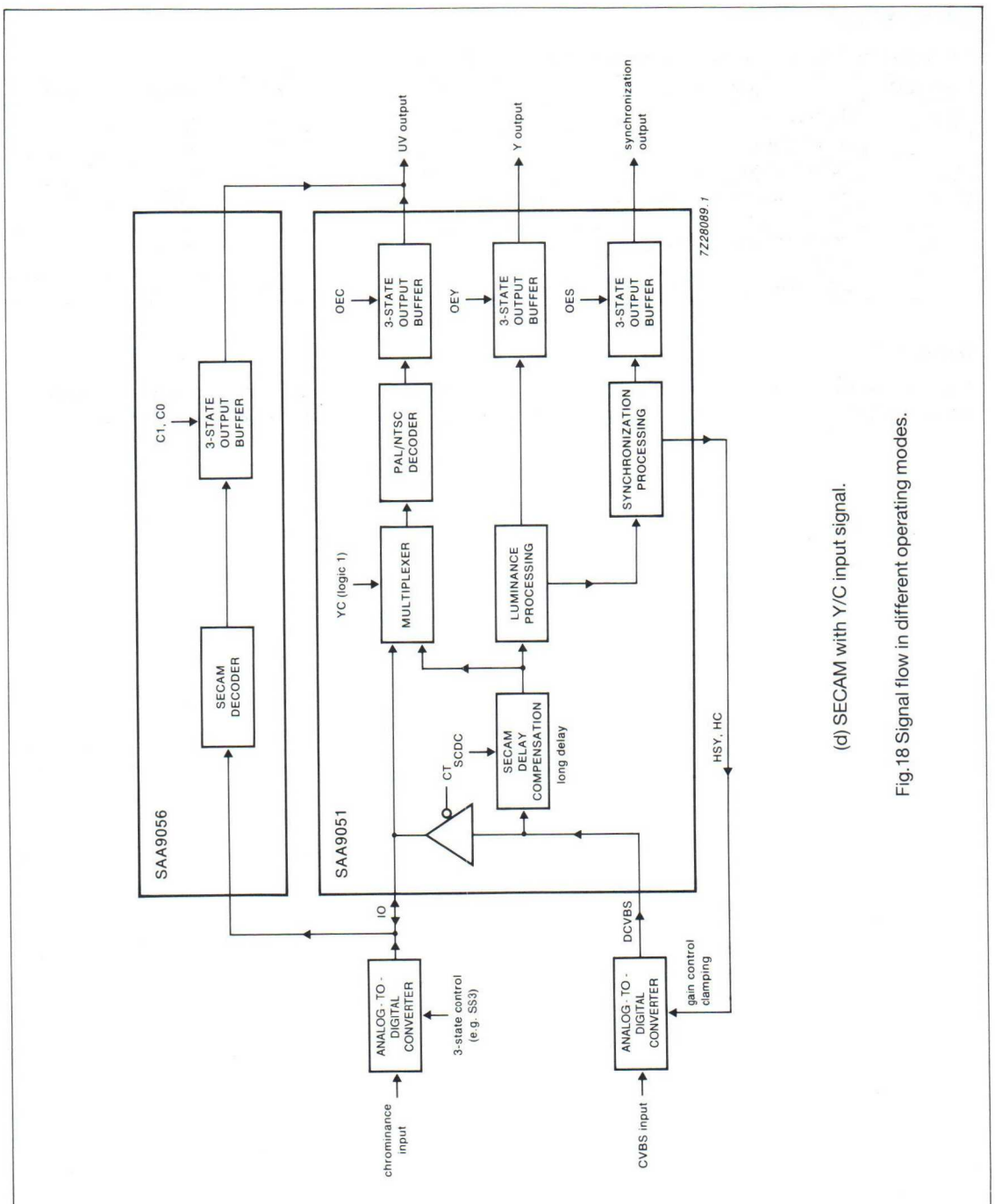
(b) PAL or NTSC with Y/C input signal.

Fig.18 Signal flow in different operating modes.



(c) SECAM with CVBS input signal.

Fig. 18 Signal flow in different operating modes.



(d) SECAM with Y/C input signal.

Fig.18 Signal flow in different operating modes.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	Supply voltage range		−0.5	+ 7.0	V
V_I	Input voltage range		−0.5	+ 7.0	V
V_O	Output voltage range	I_{Omax} = 20 mA	−0.5	+ 7.0	V
P_{tot}	Maximum power dissipation per package		-	3000	mW
T_{amb}	Operating ambient temperature range		0	+ 70	°C
T_{stg}	Storage temperature range		−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 4.5 V to 5.5 V; T_{amb} = 0 to +70 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	Supply voltage		4.5	5.0	5.5	V
I_{DD}	Supply current	note 1	-	380	550	mA
Inputs **Input voltage LOW**						
V_{IL}	pins 2 – 4, 6 – 17, 20 – 23, 43, 56 and 64		–0.5	-	+ 0.8	V
V_{IL}	pins 40 and 41		–0.5	-	+ 1.5	V
Input voltage HIGH						
V_{IH}	pins 2 – 3, 6 – 17, 20 – 23, 43, 56 and 64		2.0	-	V_{DD}	V
V_{IH}	pin 4		2.0	-	V_{DD}	V
V_{IH}	pins 34, 40 and 41		3.0	-	V_{DD}	V
Input leakage current						
I_I	pins 2 – 4, 6 – 17, 20 – 23, 40 – 41, 43 and 64		-	-	10	μA
Input capacitance						
C_I	pin 4		2	-	10	pF
C_I	pins 2 – 3, 14 – 17, 20 – 23, 43 and 64		2	-	7.5	pF
C_I	pins 6 – 13	HIGH-impedance Z-state	2	-	7.5	pF
Outputs **Output voltage LOW**						
V_{OL}	pins 6 – 13, 24 – 26, 29 – 32, 42, 45 -50, 53, 55 – 58, 65 – 66 and 68	I_{OL} = 2.0 mA	0	-	0.6	V
V_{OL}	pin 40 and 41	I_{OL} = 5.0 mA	0	-	0.45	V
Output voltage HIGH						
V_{OH}	pins 6 – 13, 24 – 26, 29 – 33, 42 and 45 – 50, 53, 55 – 58, 65 – 66 and 68	I_{OH} = –0.5 mA	2.2	-	V_{DD}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output capacitance						
C_O	pins 45 – 50, 53 and 55 – 58		-	-	7.5	pF
LFCO output (peak-to-peak value)						
$V_{o(p-p)}$	$R_L \geq 10$ kΩ; $C_L < 15$ pF		1	-	-	V
$V_{o(p-p)}$	$R_L \geq 1$ kΩ; $C_L < 15$ pF		0.5	-	-	V
Timing (see Fig.19)						
t_{C3}	LL3 cycle time		69	-	80	ns
t_{C3H}/t_{C3}	LL3 duty factor		43	-	57	%
t_r, t_f	LL3 rise and fall times	note 3	-	-	6	ns
$t_{SU;\ DAT}$	Input data set-up time		12	-	-	ns
$t_{HD;\ DAT}$	Input data hold time		5	-	-	ns
t_{HD}	Output data hold time		5	-	-	ns
t_D	Output data delay time	except HCY and HS; $C_L = 25$ pF; $I_{OL} =$ 2.0 mA; $V_{OH} = 2.2$ V	-	-	50	ns
t_D	HCY and HS output delay time	$C_L = 25$ pF; $I_{OL} =$ 2.0 mA; $V_{OH} = 2.6$ V	-	-	80	ns
C_L	Output data load capacitance		7.5	-	25	pF
Crystal oscillator (see Fig.20)						
f_n	Nominal frequency	third harmonic	-	24.576	-	MHz
$\Delta f/f_n$	Permissible deviation f_n		-	$\pm 50 \times 10^{-6}$	-	
$\Delta f/f_n$	Temperature deviation from f_n		-	$\pm 20 \times 10^{-6}$	-	
T_{XTAL}	Temperature range		0	-	+ 70	°C
C_{LXTAL}	Load capacitance		8	-	-	pF
R_r	Maximum resonance resistance		-	40	-	Ω
C_1	Motional capacitance		-	1.5 ±20%	-	fF
C_0	Parallel capacitance		-	3.5 ±20%	-	pF

Notes to the characteristics

1. Inputs LOW and outputs not connected, $V_{DD} = 5$ V.
2. 4-bit triangular waveform clocked at 24.576 MHz, AC coupled at pin 36.
3. Rising and falling edges of the clock signal are assumed to be smooth e.g. due to roll-off low-pass filtering.

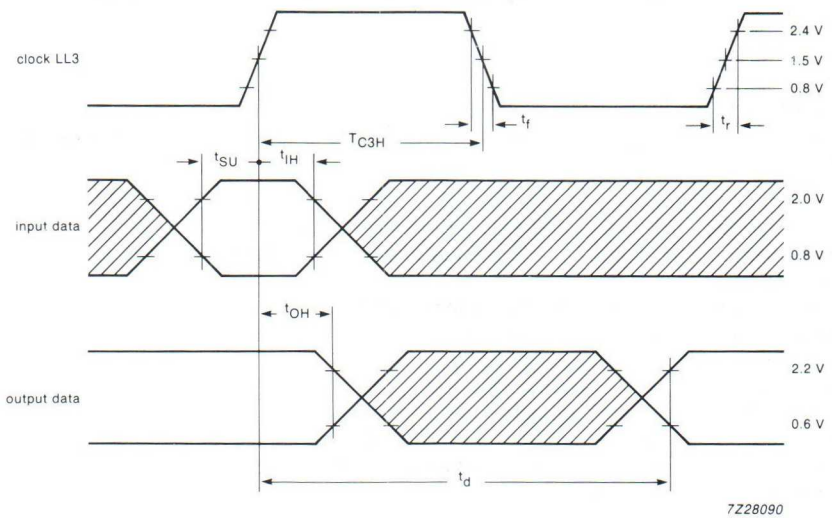


Fig.19 Timing diagram.

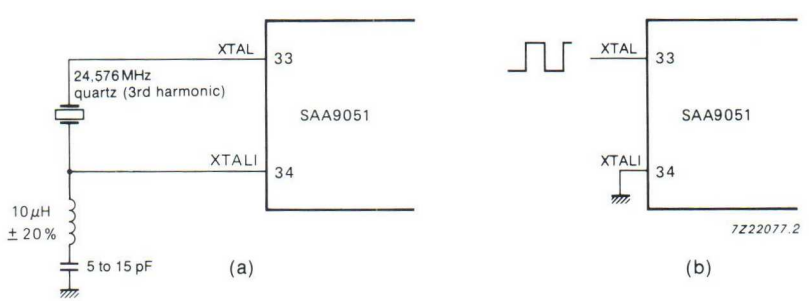


Fig.20 Oscillator circuit requirements; (a) with quartz crystal; (b) with external clock.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

S-VHS DIGITAL SECAM DECODER (SDSD)

GENERAL DESCRIPTION

The SAA9056 is designed to provide colour difference signals for a digital TV signal processing system.

Features

- Phase-linear chrominance bandpass filter for cross-colour improvement
- Programmable filter characteristics for optimum adaption for different IF stages
- Recursive "Cloche" (Bell) filter
- Zero-crossing detection, FM demodulator with high AM rejection
- One demodulator for both carrier frequencies
- Base-band signal adjustment in gain and offset
- De-emphasis with recursive filter structure
- Line delay and cross-over switch for colour difference signals
- Output multiplexer for the UV format of the Digital Multistandard Secam Decoder
- Standard identification circuit with programmable sensitivity
- Programmable I^2C-bus address

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

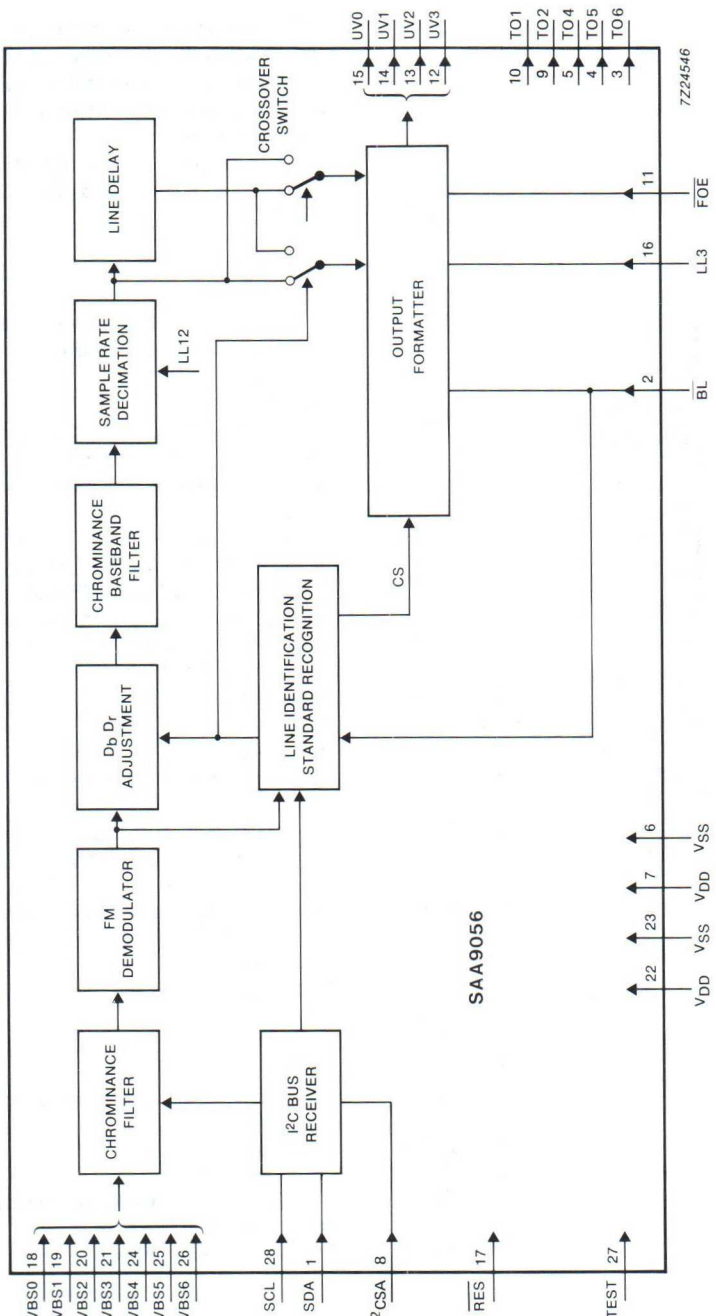


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

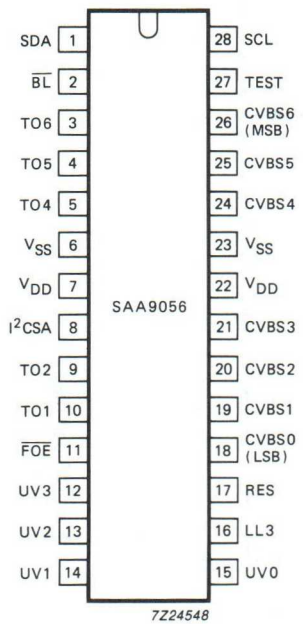


Fig.2 Pinning diagram.

1	SDA	I^2C-bus serial data input, receive only, no data is transmitted from the SDSD
2	$\overline{BL}$	This signal from the digital multistandard decoder indicates the active video and line blanking period
3	TO6	Test output pin, used during test mode only. Do not connect this pin
4	TO5	As pin 3
5	TO4	As pin 3
6	V_{SS}	Ground
7	V_{DD}	+ 5 V supply
8	I^2CSA	I^2C-bus select address. Input to select two different I^2C-bus slave addresses
9	TO2	As pin 3
10	TO1	As pin 3
11	$\overline{FOE}$	Fast output enable signal, forces the UV-outputs to High-Z state
12	UV3	UV colour difference signals, via this port the decoded colour difference signals are transmitted to the DMSD in a mixed parallel/serial format. Additionally the status flag CS (colour in SECAM detected) is encoded in the UV data stream. The output drivers can be set to high impedance (3-state) via the I^2C-bus.
13	UV2	As pin 12
14	UV1	As pin 12
15	UV0	As pin 12
16	LL3	LL3 is the line-locked system clock at 13.5 MHz
17	$\overline{RES}$	The reset signal (active LOW) disables the UV buffers. Minimum LOW-time on this input = 10 LL3-cycles
18	CVBS0	Composite video, blanking and synchronization (LSB) input
19	CVBS1	As pin 18
20	CVBS2	As pin 18
21	CVBS3	As pin 18
22	V_{DD}	As pin 7
23	V_{SS}	As pin 6
24	CVBS4	Composite video, blanking and synchronization
25	CVBS5	As pin 24
26	CVBS6	As pin 24 (MSB)
27	TEST	This signal (active HIGH) enables the scan test mode
28	SCL	I^2C-bus serial clock input

FUNCTIONAL DESCRIPTION

The S-VHS Digital SECAM Decoder (SDSD) forms an integral part of a digital TV signal processing system. The system incorporates a Video Processor and Input Selector (TDA9045), an A/D Converter (SAA9079), a Sample Rate Converter (SAA9058), a Digital Multi-Standard Decoder with separate chrominance and luminance input (SAA9051), a Digital Deflection Controller (SAA9062/3/4)*, a Clock Generator Circuit (SAA9057), a Video Processor with DACs (SAA9060), a Colour Transient Improvement Circuit (TDA4565), a Video Control Combination Circuit (TDA4580), and an Octuple 6-bit DAC and a Feature Box. Figure 9 illustrates the timing of the input and output signals relative to the input clock (LL3).

The S-DMSD (SAA9051) decodes and demodulates the colour information from all TV standards which employ a quadrature modulated colour carrier. The S-DMSD also processes the luminance and synchronization signals and generates auxiliary signals.

The SDSD separates the colour information which it demodulates and decodes to provide the colour difference signals. These signals are subsequently encoded to produce a serial/parallel data stream at the UV outputs. Figure 4 illustrates the formatting and timing of the UV output port.

To enable other sources (eg PIP-CO) to access the digital YUV-bus, a fast output enable signal ($\overline{FOE}$) is provided. Two LL3-cycles after the $\overline{FOE}$ becomes inactive (HIGH), the UV output port of the SDSD is forced to the High-Z state. When the $\overline{FOE}$ signal is active (LOW) again, it needs two LL3-cycles and the UV output port of the SDSD becomes active (see Fig.4).

The chrominance bandpass filter for separating the frequency modulated colour carrier consists of several phase-linear FIR filters which improve the cross-colour behaviour. The non-linear phase (Bell) filter has a recursive structure (IIR filter). Figure 3 illustrates the frequency response of the chrominance band-pass filter and Bell filter. One of the FIR filters can be programmed via the I^2C-bus to provide optimal adaption for the various IF stages. Different responses can be selected by means of a 7-bit control word. Figure 8 illustrates some examples of frequency responses of the programmable adaptive filer.

Only one FM demodulator is used to demodulate the chrominance signal; this accomodates both carrier frequencies regardless of the centre frequency. It is a zero-crossing demodulator with a real time divider which is a pipeline structure. After demodulation the baseband signal is adjusted, line sequentially, to the appropriate colour difference signal. During the clamping period, the demodulated reference carrier is compared with the previous reference signal by the line identification circuit. The identification circuit compares the phase of the two demodulated burst signals and, if the phase relationship is incorrect for several lines (not SECAM), the CS flag (colour in SECAM) will be reset.

The baseband filter consists of a linear phase low-pass filter together with a de-emphasis filter with a recursive structure. Figure 5 illustartes the frequency response of the de-emphasis and band-pass filters for the colour difference signals. After filtering, the sample rate is reduced to a quarter (LL12 = 3.375 MHz). The word length is truncated to seven bits. The resultant signal is delayed by one line period (64 μs = 216 clock periods of 3.375 MHz). The signals, delayed and non-delayed, can be switched either directly or cross-wise to two different outputs which correspond to the colour difference signals.

The cross-over switch is controlled by the line identification circuit. At the end of the chrominance path an output formatter transforms the 14 bits (2 x 7 bits clocked by 3.375 MHz) to a 4-bit wide channel which is clocked by 13.5 MHz (LL3). The bits are separated into odd and even and then serialized.

* The digital TV signal processing system has the option of using one of three Digital Deflection Controllers (SAA9062/3/4). The choice of DDC is dependent on the format of the CRT and the line/field frequency.

The format for the UV output is the same as that of the UV I/O port in the S-DMSD (SAA9051). The timing multiplexer is controlled by the external signal $\overline{BL}$ from the S-DMSD. Signal $\overline{BL}$ is also used as a line-locked synchronization signal to generate several internal burst gate pulses.

The CS flag is transmitted via the chrominance data-stream because the SDSD has no I^2C-bus transmitter. The CS bit is read once per line by the S-DMSD at LL3 clock cycle number 748 (see Fig.6). If no SECAM colour is detected the UV port will be set to zero. After reset the UV lines will be set to high impedance (3-state) and the SDSD must be re-initialized via the I^2C-bus to enable further operation.

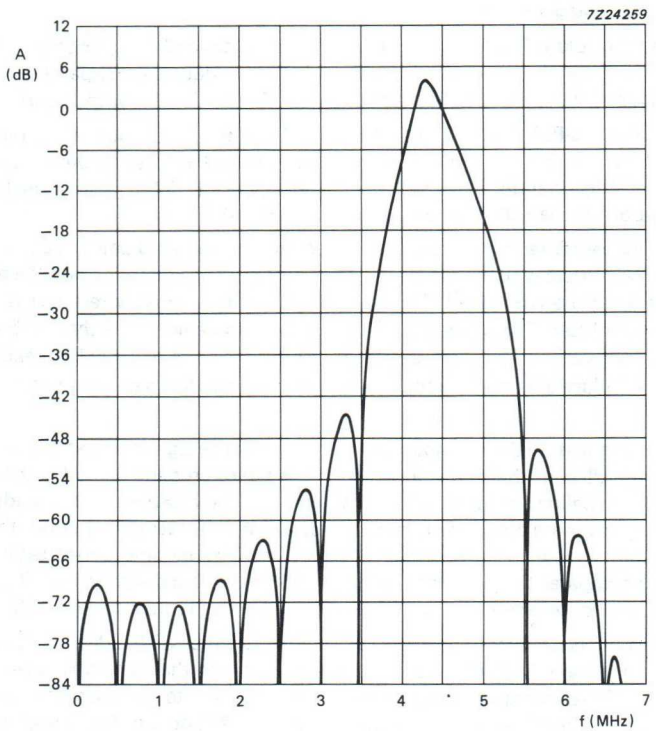


Fig. 3 Frequency response of chrominance bandpass and Bell filter.

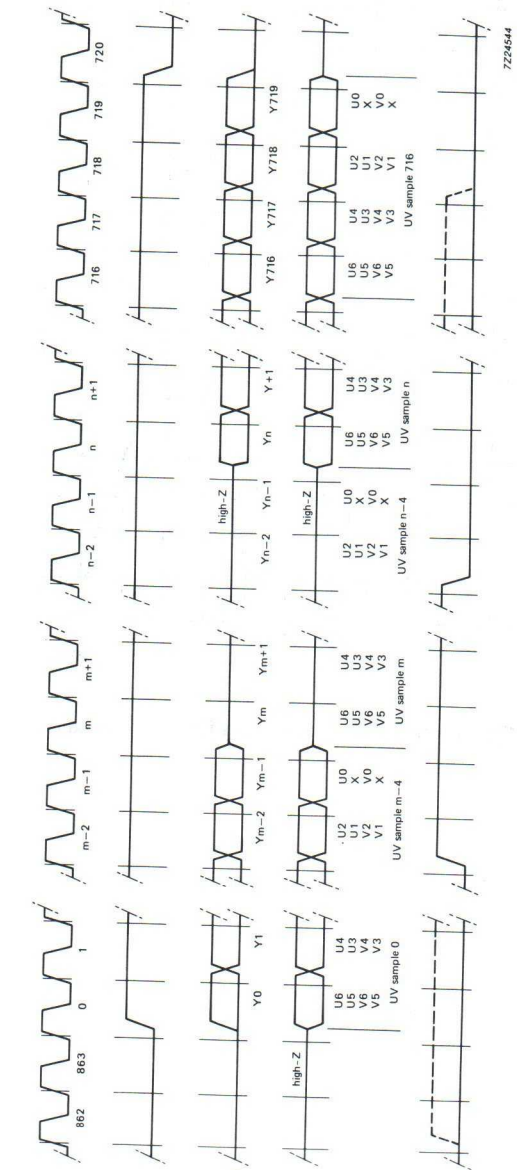


Fig.4 Timing of $\overline{FOE}$ signal.

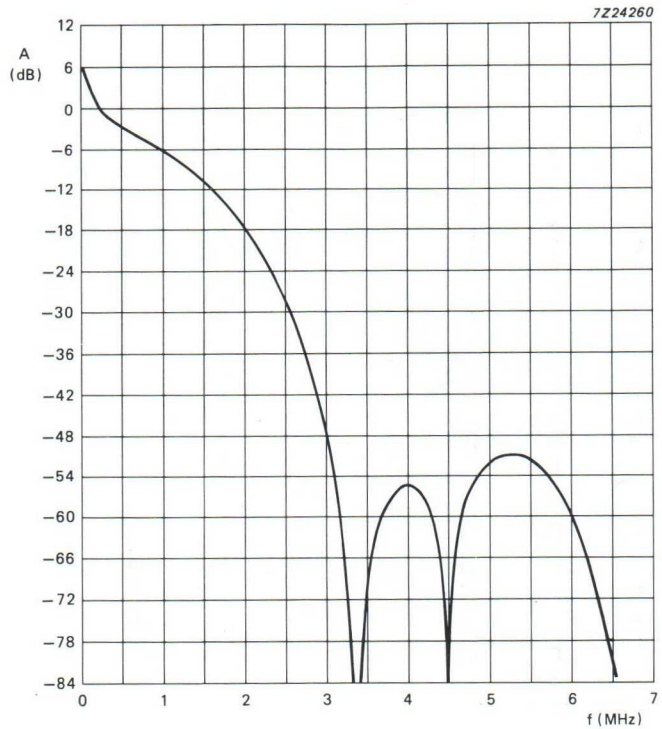
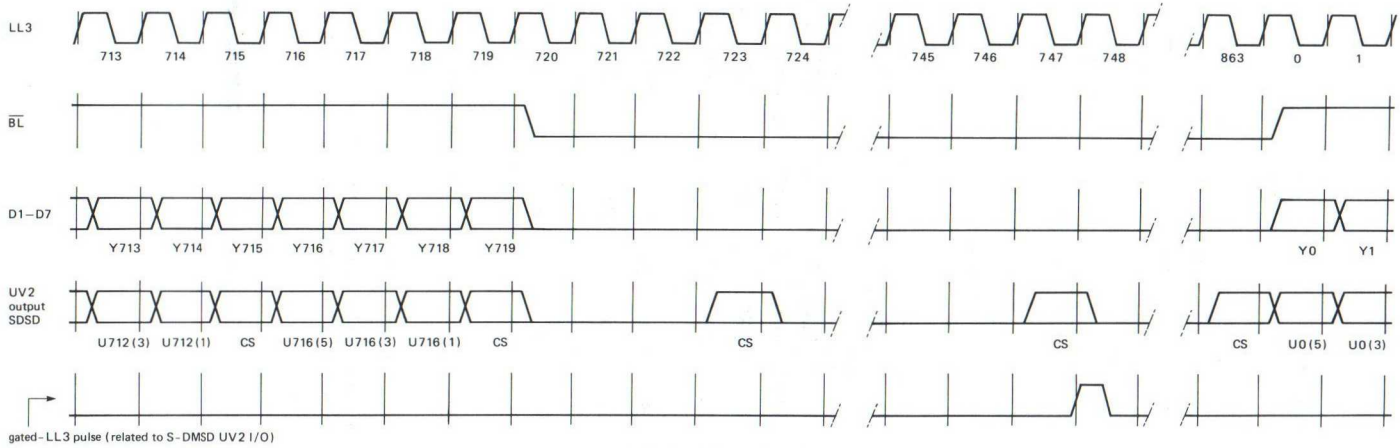
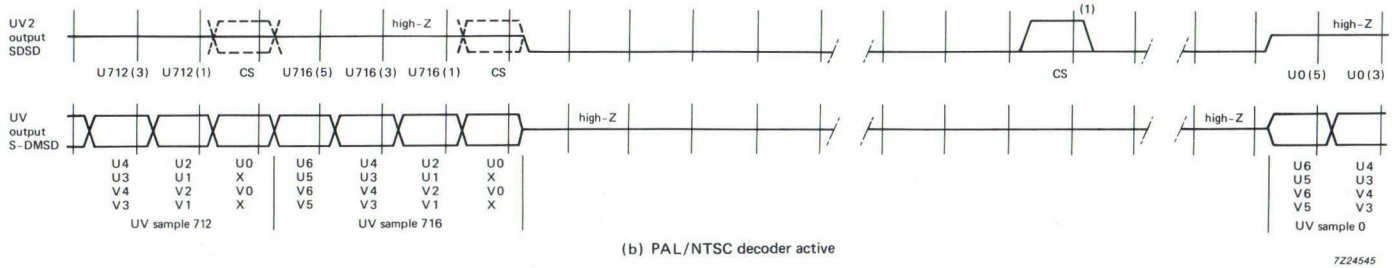


Fig. 5 Frequency response of the de-emphasis and base-band filter for the colour difference signals.

DEVELOPMENT DATA



(a) SECAM decoder active



(b) PAL/NTSC decoder active

7Z24545

(1) The CS signal is active only for ± 64 clock pulses (LL3) around the gate pulse.

Fig.6 Position of CS signal read by S-DMSD.

I²C-BUS PROTOCOL

Slave receiver organization

Two different slave addresses are programmable with the I²CSA input at pin 8

I²CSA	slave receiver addresses							
	A6	A5	A4	A3	A2	A1	A0	*)
0 or unconnected	1	0	0	0	1	0	1	0 (bin) = 8A (hex)
1	1	0	0	0	1	1	1	0 (bin) = 8E (hex)

*) 0 = receiver mode

Fig. 7 Slave receiver format.

Table 1 Subaddress definition

register function	subaddress (HEX)	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
Main counter start address	10	MA1	MA0	X	DT4	DT3	DT2	DT1	DT0
(MA9..... MA0)	11	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2
Burst gate begin	12	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Burst gate end	13	BE7	BE6	BE5	BE4	BE3	BE2	BE1	BE0
Standard recognition sensitivity	14	R7	R6	R5	R4	R3	R2	R1	R0
Programmable adaptive filter	15	X	P6	P5	P4	P3	P2	P1	P0
Control register	16	X	X	X	X	X	C2	C1	C0
Reserved	17–1F	X	X	X	X	X	X	X	X

DEVELOPMENT DATA

Notes to Table 1

1. The subaddress is automatically incremented to enable quick initialization by the I²C-bus controller within one transmission.
2. All eight bits of the subaddress are decoded by the device.
3. The subaddresses shown are acknowledged by the device. Subaddresses 00 to 0F (reserved for the Digital Multi-Standard Decoder) are not acknowledged. The subaddress counter wraps-around from 1F to 00. Subaddresses 20 to FF are not allowed.
4. X = don't care.
5. After power-on-reset the control register (subaddress 16) is set to logic 0, all other registers are undefined.

Subaddress 10 and 11 (HEX)

Main counter start address.

Application dependent.

MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	delay time	
0	1	1	1	1	1	1	1	1	1	+ 511	outside central counter range
–										–	
–										–	
–										–	
–										–	
0	1	1	0	1	0	0	0	1	0	+ 418	
0	1	1	0	1	0	0	0	0	1	+ 417	417 x 74 ns ≈ + 31 μs (maximum positive value)
–										–	
–										–	
–										–	
0	0	0	0	0	0	0	0	0	1	+ 1	+ 74 ns
0	0	0	0	0	0	0	0	0	0	0	reference point*

* Reference point position to be fixed.

MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	delay time	
1	1	1	1	1	1	1	1	1	1	–1	–74 ns
–										–	
–										–	
–										–	
1	0	0	1	0	0	0	0	1	0	–446	–446 x 74 ns ≈ –33 μs (maximum negative value)
1	0	0	1	0	0	0	0	0	1	–447	outside central counter range
–										–	
–										–	
–										–	
–										–	
1	0	0	0	0	0	0	0	0	0	–512	

$$\text{Stepsize} = \frac{1}{13.5\ \text{MHz}} = 74\ \text{ns}$$

Internal counter range: –446 to + 417

Subaddress 12 (HEX)

Burst gate begin (start time)

Application dependent.

BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0	dec	delay time
0	0	0	0	0	0	0	0	0	zero reference point
0	0	0	0	0	0	0	1	1	74 ns
–	–	–	–	–	–	–	–	–	
–	–	–	–	–	–	–	–	–	
1	1	1	1	1	1	1	1	255	18.89 μs

$$\text{Stepsize} = \frac{1}{13.5\ \text{MHz}} = 74\ \text{ns}$$

Subaddress 13 (HEX)

Burst gate end (stop time)

Application dependent.

BE7	BE6	BE5	BE4	BE3	BE2	BE1	BE0	dec	delay time
0	0	0	0	0	0	0	0	0	zero reference point
0	0	0	0	0	0	0	0	1	74 ns
–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–
1	1	1	1	1	1	1	1	255	18.89 μs

$$\text{Stepsize} = \frac{1}{13.5\ \text{MHz}} = 74\ \text{ns}$$

The stop time must be greater than the start time.

The reference point position of the burst gate start/stop time is identical with the main counter zero position.

DEVELOPMENT DATA

Subaddress 14 (HEX)

Standard recognition sensitivity

Application dependent

R7	R6	R5	R4	R3	R2	R1	R0	function
								relationship between the number of line identification errors related to a window of 312 lines
0	0	0	0	0	0	0	0	0 : 312 theoretical highest sensitivity
0	0	0	0	0	0	0	1	1 : 312
0	0	0	1	1	0	0	1	25 : 312
1	1	1	1	1	1	1	1	255 : 312 theoretical lowest sensitivity

For programmed numbers from 0 to approximately 25 (dec) the colour signal is switched off. With the value 25 (dec) the colour signal will be enabled only when extremely good signal quality is present. If the colour signal quality is reduced, i.e. VCR signal source, bad S/N ratio, bad quantization, diminished colour carrier and insufficient IF adaption, the sensitivity should be set lower (higher programmed number up to 255 (dec) in order to prevent excessive switching and thus ensure constant colour.

DEVELOPMENT DATA

Subaddress 15 (HEX)

Programmable adaptive filter PAF (P6–P0)

Application (IF stage) dependent

The programmable adaptive filter, together with the cloche and linear bandpass filter, forms a filter-curve that treats the chrominance frequency spectra with different gain but linear phase. The frequency characteristic is a system of sinusoidal waveforms which are described by:

- Reference "knots" of constant gain (0 dB)
- Frequency points ("tops") with maximum gain
- The amount of maximum gain
  (There is also a switchable pre-amplifier in another stage of the bandpass filter).

The components of the PAF can be programmed via the I^2C-bus by using device address 8A (or 8E) and subaddress 15 thereby producing 57 different transfer functions. An example of some transfer functions is given in Figure 8 (a) to (d).

MSB	P6	P5	P4	P3	P2	P1	P0	function			
								maximum gain at tops			
–	X	X	X	X	1	1	1	19 dB			
–	X	X	X	X	1	1	0	14 dB			
–	X	X	X	X	1	0	1	9.5 dB			
–	X	X	X	X	1	0	0	6 dB			
–	X	X	X	X	0	1	1	3.5 dB			
–	X	X	X	X	0	1	0	2 dB			
–	X	X	X	X	0	0	1	1 dB			
–	X	X	X	X	0	0	0	0 dB			
								position of tops and knots (MHz)			
								top	knot	top	Figs 8a–d
–	X	1	1	1	X	X	X	3.375	4.5	5.625	+ A/dB (d)
–	X	1	1	0	X	X	X	4.5	5.625	6.75	–A/dB (d)
–	X	1	0	1	X	X	X	4.219	5.063	5.906	–A/dB (c)
–	X	1	0	0	X	X	X	3.375	4.219	5.063	+ A/dB (c)
–	X	0	1	1	X	X	X	4.05	5.4	6.75	–A/dB (b)
–	X	0	1	0	X	X	X	2.7	4.05	5.4	+ A/dB (b)
–	X	0	0	1	X	X	X	2.89	3.86	4.82	+ A/dB (a)
–	X	0	0	0	X	X	X	3.86	4.82	5.79	–A/dB (a)
								additional pre-amplification			
–	1	X	X	X	X	X	X	times two			
–	0	X	X	X	X	X	X	times one			
*	X	X	X	X	X	X	X	* MSB not used			

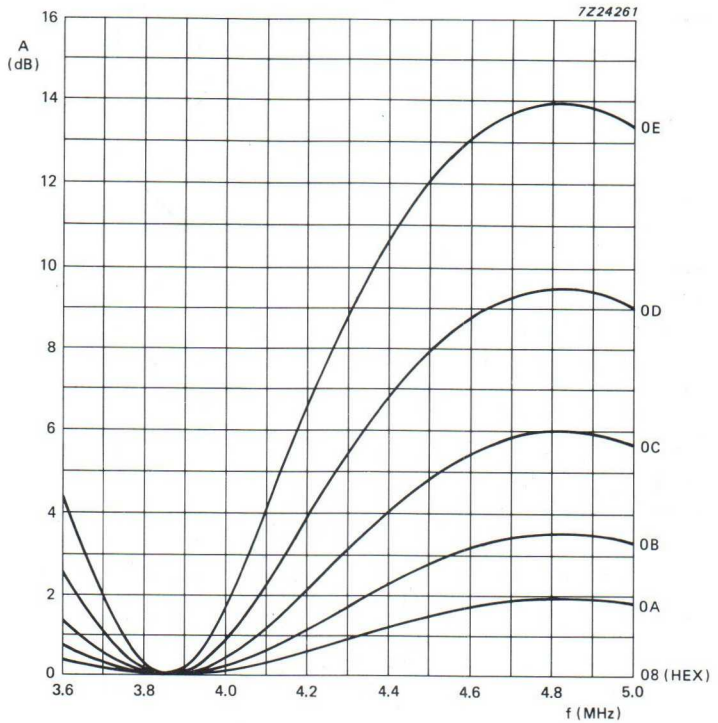


Fig. 8(a) Examples of frequency response for the programmable adaptive filter; from 08 to 0E (HEX).

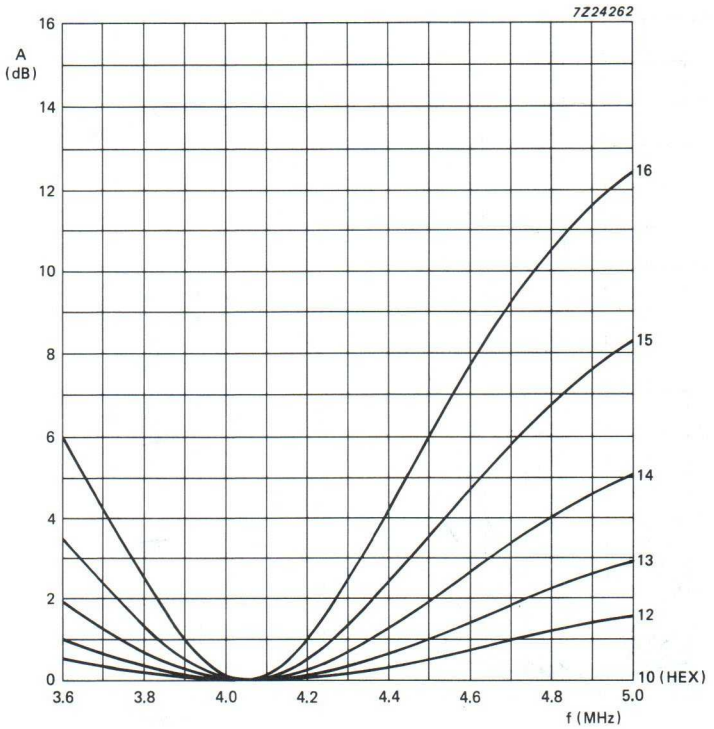


Fig. 8(b) Example of frequency response for the programmable adaptive filter; from 10 to 16 (HEX).

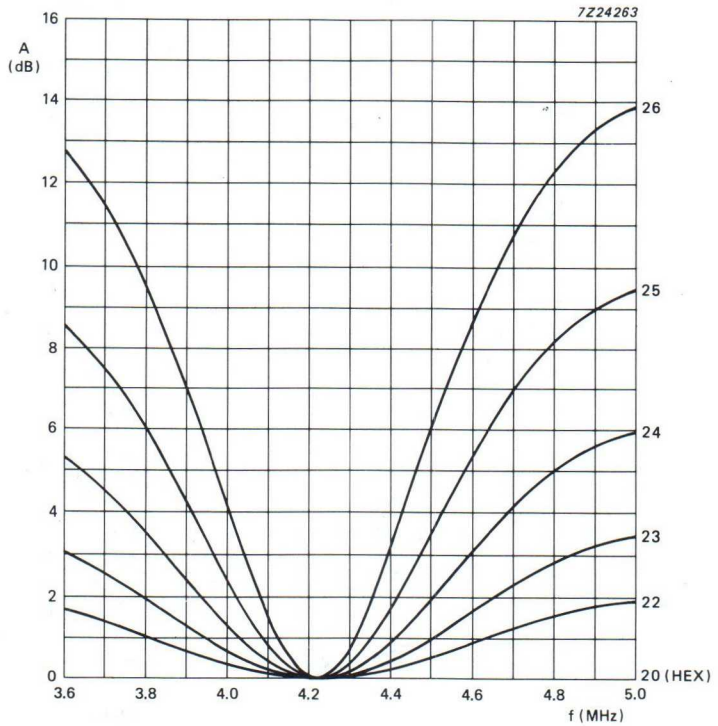


Fig. 8(c) Example of frequency response for the programmable adaptive filter; from 20 to 26 (HEX).

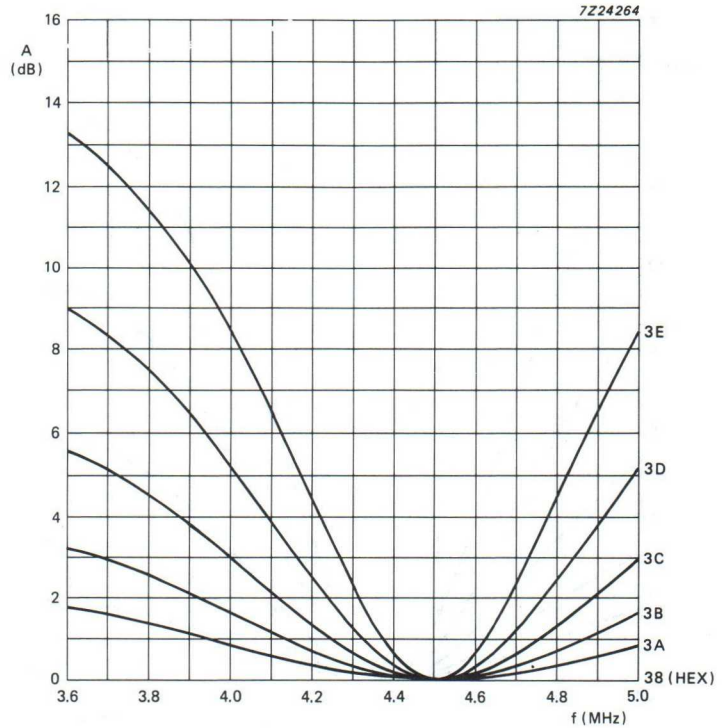


Fig. 8(d) Example of frequency response for the programmable adaptive filter; from 38 to 3E (HEX).

Subaddress 16 (HEX)

DSD control 3 register

C2	C1	C0	UV-output
X	0	1	active zero whole line
X	1	0	colour enable (if CS flag then colour on)
X	1	1	colour forced on (independent of CS flag)
0	X	X	positive UV
1	X	X	negative UV
0	0	0	3-state
1	0	0	UV2-output active during horizontal blanking period (CS-bit* transmission); high impedance in active line negative UV

After power-on reset the control register is set to logic 0.

* The position of the CS transmission is dependent on the start value of the main counter (Reg 10 and 11).



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_{DD}	−0.5	7.0	V
Voltage input		V_I	−0.5	7.0	V
Voltage output	I_{max} = 20 mA	V_O	−0.5	7.0	V
Total power dissipation		P_{tot}	−	1.2	W
Operating ambient temperature range		T_{amb}	0	70	°C
Storage temperature range		T_{stg}	−65	150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified. All voltages are referenced to ground (pins 6 and 23) unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	4.5	–	5.5	V
Supply current (f_{nom})	V_{DD} = 5.5 V					
Inputs LOW; outputs with maximum load		I_{DD}	–	–	180	mA
Inputs						
Input voltage LOW (clock data) pins 2, 16, 17 to 21; and 24 to 27		V_{IL}	0	–	0.8	V
Input voltage LOW (I^2C) pins 1 and 28		V_{IL}	0	–	1.5	V
Input voltage HIGH (data) pins 2, 17 to 21; and 24 to 27		V_{IH}	2	–	V_{DD}	V
Input voltage HIGH (LL3) pin 16		V_{IH}	2.4	–	V_{DD}	V
Input voltage HIGH (I^2C) pins 1 and 28		V_{IH}	3	–	V_{DD}	V
Input leakage current pins 1, 2, 12 to 21; and 24 to 27		I_{LI}	−10	–	+ 10	μA
Input current pins 8 and 11		I_I	−10	–	+ 60	μA
Input capacitance (data) pins 2, 18 to 21; and 24 to 27		C_I	2	–	7.5	pF
Input capacitance (clock) pin 16		C_I	5	–	10	pF
Input capacitance (reset) pin 17		C_I	2	–	10	pF
Outputs						
Output voltage LOW pins 3 to 5; 8 to 15	I_{OL} = 2 mA	V_{OL}	0	–	0.4	V
Output voltage LOW SDA pin 1	I_{OL} = 5 mA	V_{OL}	0	–	0.45	V
Output voltage HIGH pins 3 to 5; 8 to 15	I_{OL} = −0.5 mA	V_{OH}	2.4	–	V_{DD}	V
Capacitive load of outputs in high impedance pins 12 to 15		C_Z	2	–	15	pF

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified. All voltages are referenced to ground (pins 6 and 23) unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Clock timing (LL3)						
Cycle time	note 1	t_{C3}	69	–	80	ns
Duty factor		δ	43	–	57	%
Rise time	note 2	t_r	–	–	6	ns
Fall time	note 2	t_f	–	–	6	ns
Input timing						
Data set up time		t_{SU}	12	–	–	ns
Data hold time	note 3	t_{IH}	5	–	–	ns
Output timing						
Data load capacitance		C_L	7.5	–	50	pF
Data hold time	V_{IH}(CLK) = 3 V	t_{OH}	5	–	–	ns
Data delay time	C_L = 25 pF	t_{OD}	–	–	45	ns

Notes to the characteristics

1. Static deviation = ±2%; dynamic deviation = ±7% for signal path CVBS-DCVBS (this is required for the running-in of the DMSD sync processor).
2. The rising and falling edges of the clock signal are assumed to be smooth due to roll-off low-pass filtering.
3. Matches to SAA9058 for V_{IH}(LL3) ⩾ 3 V.

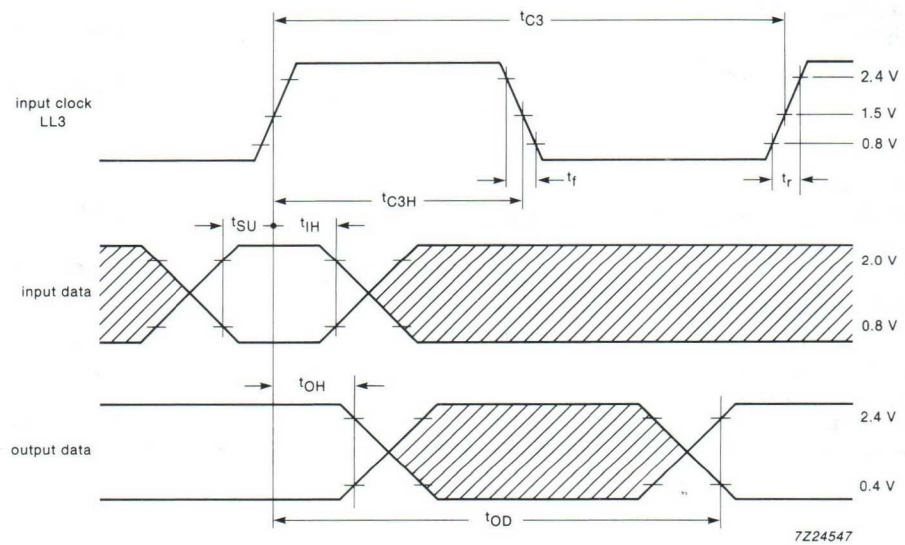


Fig. 9 Timing diagram.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	May 1992

SAA9057B

Clock signal generator circuit for digital TV systems (CGC)

FEATURES

- Clock generation suitable for digital TV systems (line-locked)
- PLL frequency multiplier to generate 4 times of input frequency
- Dividers to generate clocks LL1.5, LL3 and LL3T (4th and 2nd multiples of input frequency)
- Reset control and power fail detection

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8, 17)	4.5	5.0	5.5	V
I_{DDA}	analog supply current	3	-	9	mA
I_{DDD}	digital supply current	10	-	40	mA
V_{LFCO}	LFCO input voltage (peak-to-peak value)	1	-	V_{DDA}	V
f_i	input frequency range	6.25	-	7.25	MHz
V_I	input voltage LOW input voltage HIGH	0 2.4	- -	0.8 V_{DDD}	V V
V_O	output voltage LOW output voltage HIGH	0 2.6	- -	0.6 V_{DDD}	V V
T_{amb}	operating ambient temperature range	0	-	70	°C

GENERAL DESCRIPTION

The SAA9057B generates all clock signals required for a digital TV system suitable for the SAA90xx family. Optional extras (feature box etc.) can be driven via external buffers, advantageous for a digital TV system based on display standard conversion concepts.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9057B	20	DIL	plastic	SOT146
SAA9057BT	20	mini-pack (SO20)	plastic	SOT163A

Clock signal generator circuit for digital TV systems (CGC)

SAA9057B

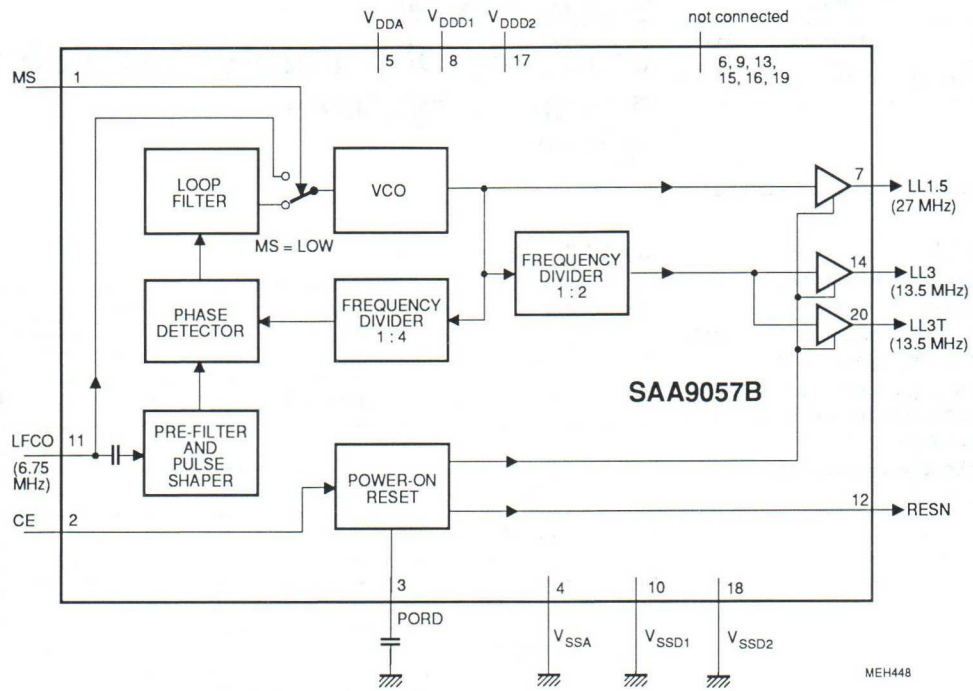


Fig.1 Block diagram.

FUNCTION DESCRIPTION

The SAA9057B generates all clock signals required for a digital TV system suitable for the SAA90xx family. Optional extras (feature box etc.) can be driven via external buffers, advantageous for a digital TV system based on display standard conversion concepts.
The 6.75 MHz input signal LFCO, coming from SAA 9051, is multiplied to 27 MHz by the PLL (including phase detector, loop filter, VCO and frequency divider) and output on LL1.5 (pin7). 13.5 MHz frequency is also generated by 1:2 divider and output on LL3 and LL3T (pins 14 and 20).
The rectangular output signals have 50 % duty factor.

Mode select MS

The LFCO input signal is directly connected to the VCO at MS = HIGH. The circuit operates as an oscillator and frequency divider. MS function is not tested.

Chip enable CE

The buffer outputs are enabled and power-on reset is set to HIGH by CE = HIGH (Fig.4).
CE = LOW sets the clock outputs HIGH and RESN output LOW.

Power-on reset

Power-on reset is activated at power-on, when the supply voltage decreases below 3.5 V (Fig.4) or when chip enable is done. The indicator output RESN is LOW for a time determined by capacitor on pin 3. The RESN signal can be applied to reset other circuit of this digital TV system.
The LFCO input signal has to be applied before RESN becomes HIGH.

Clock signal generator circuit for digital TV systems (CGC)

SAA9057B

PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	mode select input (LOW = PLL mode)
CE	2	chip enable /reset (HIGH = outputs enabled)
PORD	3	power-on reset delay dependent on external capacitor
V_{SSA}	4	analog ground (0 V)
V_{DDA}	5	analog supply voltage (+5 V)
n.c.	6	not connected
LL1.5	7	line-locked clock output signal (4 times f_{LFCO})
V_{DDD1}	8	digital supply voltage 1 (+5 V)
n.c.	9	not connected
V_{SSD1}	10	digital ground 1 (0 V)
LFCO	11	line-locked input frequency
RESN	12	reset output (active-LOW)
n.c.	13	not connected
LL3	14	line-locked clock output signal (2 times f_{LFCO})
n.c.	15	not connected
n.c.	16	not connected
V_{DDD2}	17	digital supply voltage 2 (+5 V)
V_{SSD2}	18	digital ground 2 (0 V)
n.c.	19	not connected
LL3T	20	line-locked clock output signal (2 times f_{LFCO})

PIN CONFIGURATION

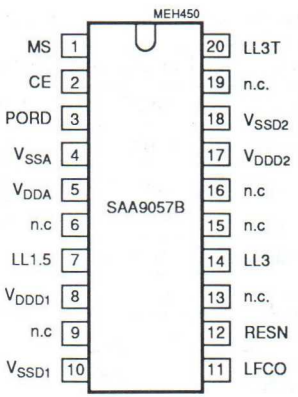


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	–0.5	7.0	V
V_{DDD}	digital supply voltage (pins 8 and 17)	–0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{DDA} - V_{DDD}$	-	±100	mV
V_O	output voltage (I_{OM} = 20 mA)	–0.5	V_{DDD}	V
P_{tot}	total power dissipation	0	1.1	W
T_{stg}	storage temperature range	–65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	tbf	V

* Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal handling precautions appropriate to "Handling MOS devices ".

CHARACTERISTICS

$V_{DDA} = V_{DDD} = 4.5$ to 5.5 V; $f_{LFCO} = 6.25$ to 7.25 MHz and $T_{amb} = 0$ to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8 and 17)		4.5	5.0	5.5	V
I_{DDA}	analog supply current (pin 5)		3	-	9	mA
I_{DDD}	digital supply current ($I_8 + I_{17}$)	note 1	10	-	40	mA
V_{reset}	power-on reset threshold voltage	Fig.4	-	3.5	-	V
Input LFCO (pin 11)						
V_{11}	DC input voltage		0	-	V_{DDA}	V
V_i	input signal (peak-to-peak value)		1	-	V_{DDA}	V
f_{LFCO}	input frequency range		6.25	-	7.25	MHz
C_{11}	input capacitance		-	-	10	pF
Inputs MS and CE (pins 1 and 2)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}	V
I_{LI}	input leakage current		-	-	10	µA
C_I	input capacitance		-	-	5	pF
Output RESN (pin 12)						
V_{OL}	output voltage LOW	$I_{OL} = 2$ mA	0	-	0.4	V
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.4	-	V_{DDD}	V
I_{LI}	output leakage current		-	-	±10	µA
t_d	RESN delay time	$C_3 = 0.1$µF; Fig.4	20	-	200	ms
Output signals LL1.5, LL3 and LL3T (pins 7, 14 and 20)						
V_{OL}	output voltage LOW	$I_{OL} = 2$ mA	0	-	0.6	V
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.6	-	V_{DDD}	V
I_{LI}	output leakage current	high-impedance	-	-	±10	µA
t_{comp}	composite rise time	note 1; note 2	-	-	9	ns
f_{LL}	output frequency LL1.5	Figures 3 and 6	-	4 f_{LFCO}	-	MHz
	output frequency LL3		-	2 f_{LFCO}	-	MHz
	output frequency LL3T		-	2 f_{LFCO}	-	MHz
t_{LL}	duty factor LL1.5	note 1; Fig.3	40	50	60	%
	duty factor LL3 and LL3T	note 1; Fig.3	43	50	57	%
t_r, t_f	rise and fall times	note 1; Fig.3	-	-	6	ns

Notes to the characteristics

1. f_{LFCO} = 7.0 MHz and output load 40 pF. V_{SSA} and V_{SSD} connected together.
2. t_{comp} is the rise time from LOW of all clocks to HIGH of all clocks (Fig.3) including rise time, skew and jitter components. Measurements taken between 0.6 V and 2.6 V.
3. MS function is not tested.

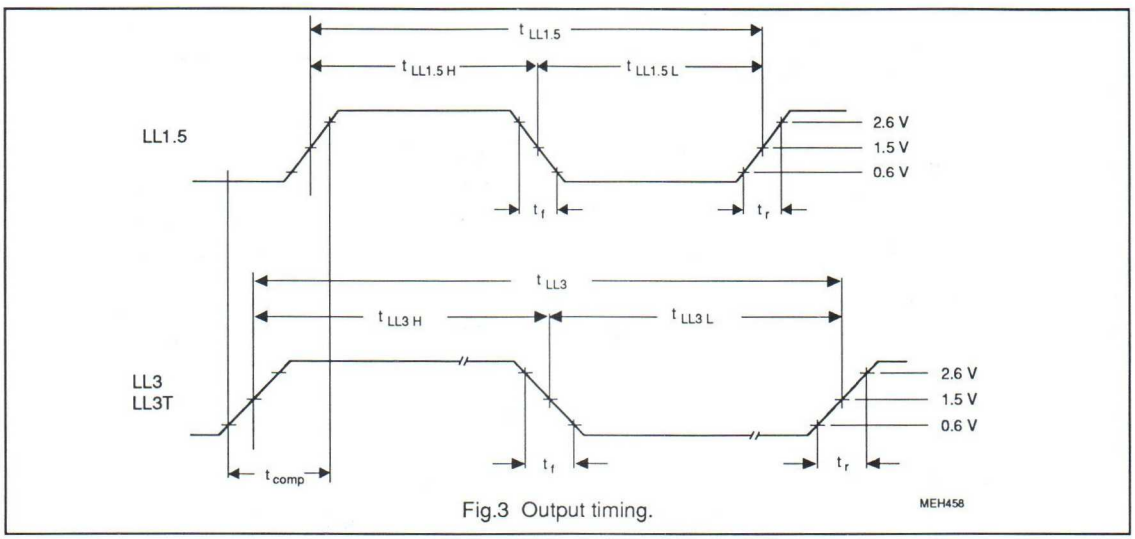


Fig.3 Output timing.

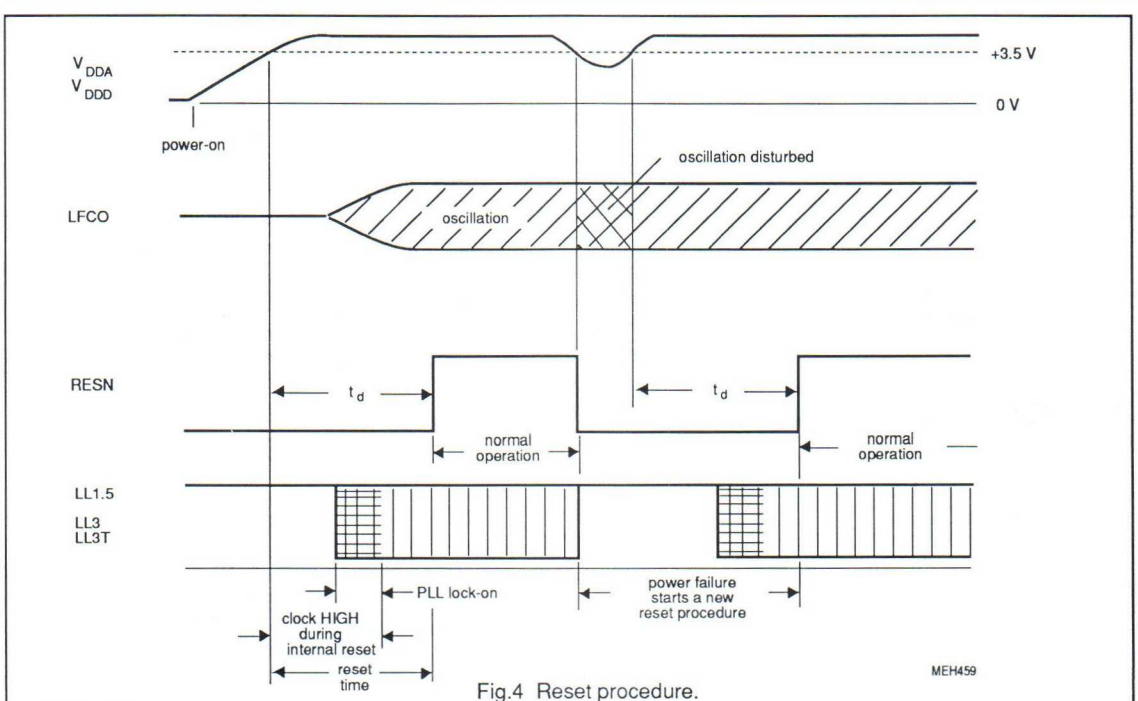
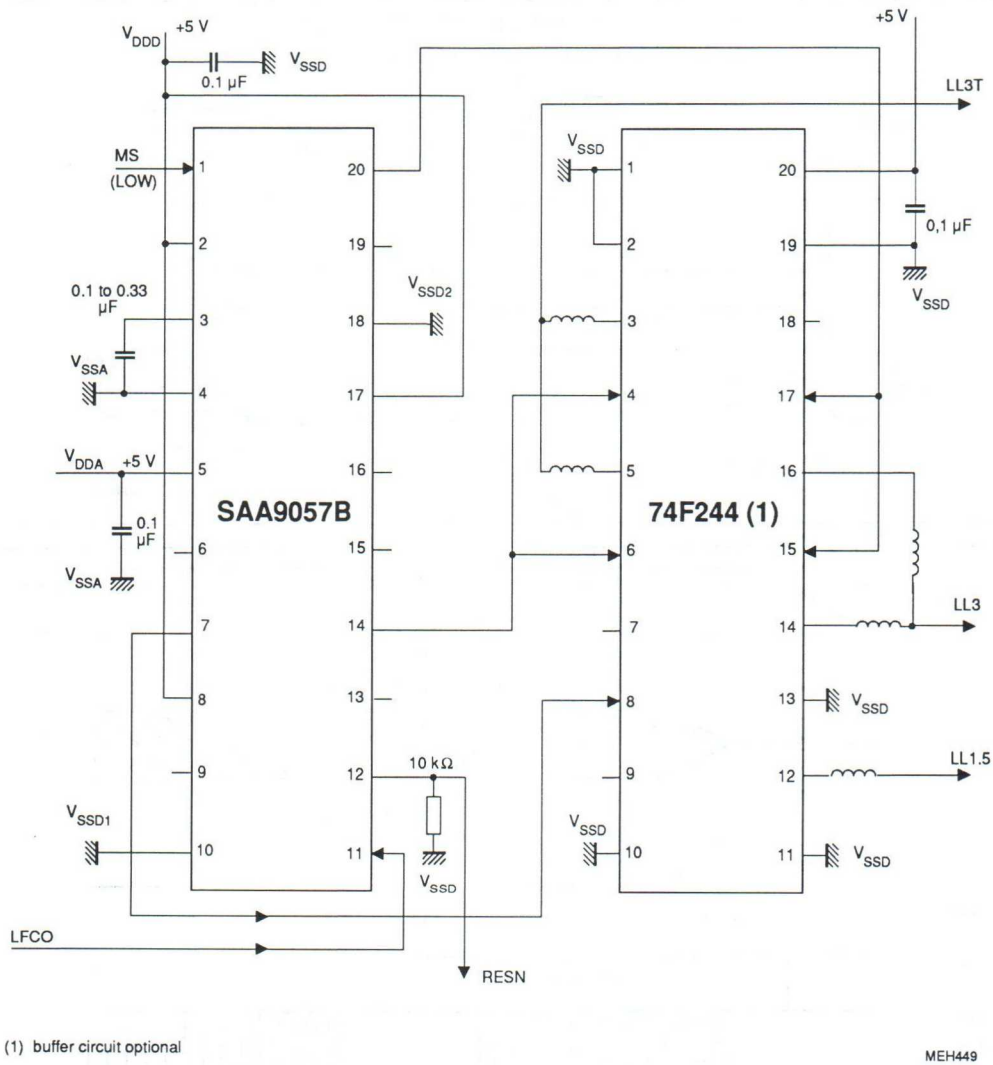


Fig.4 Reset procedure.



(1) buffer circuit optional

MEH449

Fig.5 Application circuit.

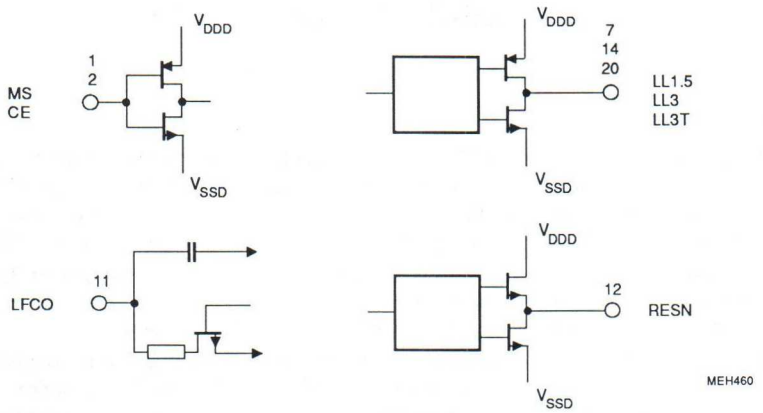


Fig.6 Internal circuit.

SAMPLE-RATE CONVERTER

GENERAL DESCRIPTION

The SAA9058 sample-rate converter (SRC) is for use in digital TV receiver applications. It converts the sampling rate of digital signals by a factor of 2/3, e.g. from 20,25 to 13,5 MHz, using a phase-linear, finite impulse response (FIR) filter with time-varying coefficients. Only two clocks are required; the data format is two's complement, and the word length at both input and output is seven bits.

The FIR filter creates a filter-algorithm to interpolate digitized composite video signals (DCVBS) into a slower sample rate that is suitable for video decoding. The circuit gives low attenuation of colour subcarrier, gives high rejection of aliasing components and has unity DC gain.

It is intended for use with the 7-bit analogue-to-digital converter PNA7509 and the digital multistandard decoder SAA9050, with DCVBS in PAL, NTSC or SECAM. Other applications are digital anti-aliasing filtering, rejection of harmonics caused by analogue-to-digital conversion and data reduction.

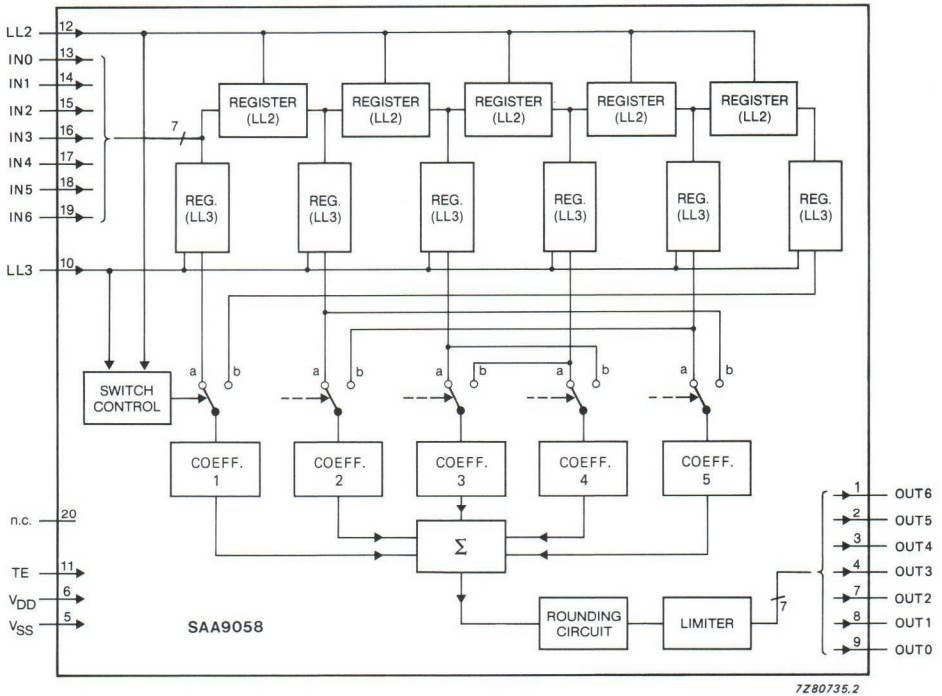


Fig. 1 Block diagram (see Fig. 3 for switch timing).

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

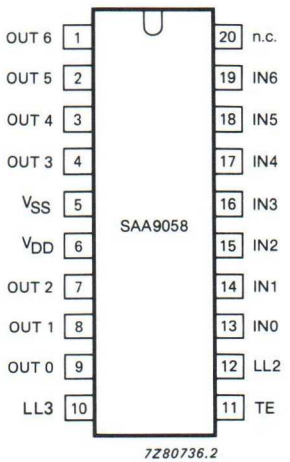


Fig. 2 Pinning diagram.

PINNING

1	OUT6	output data
2	OUT5	
3	OUT4	
4	OUT3	
5	V_{SS}	ground (0 V)
6	V_{DD}	positive supply voltage (+5 V)
7	OUT2	output data
8	OUT1	
9	OUT0	
10	LL3	output clock
11	TE	production test input; V_{SS} for all applications
12	LL2	input clock
13	IN0	input data
14	IN1	
15	IN2	
16	IN3	
17	IN4	
18	IN5	
19	IN6	
20	n.c.	not connected

OPERATION

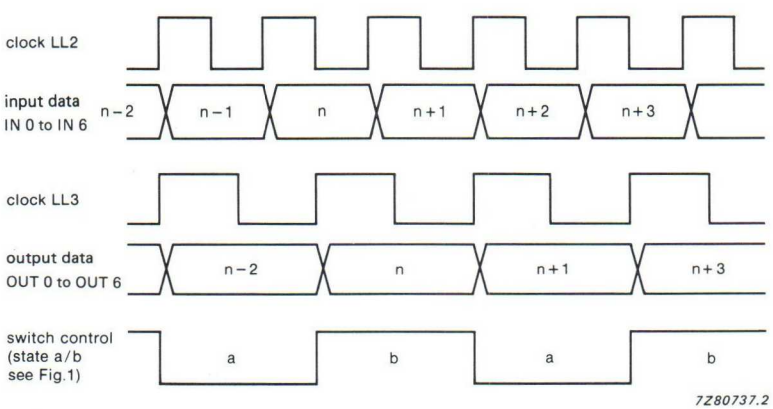


Fig. 3 Relationship of inputs to outputs.

Frequency response

The virtual frequency response in the 2 x LL2 (40,5 MHz) domain is interpreted as the characteristic of the interpolation filter directly before conversion to the LL3 (13,5 MHz) sample rate and the spectral components beyond LL3/2 are aliased into the baseband.

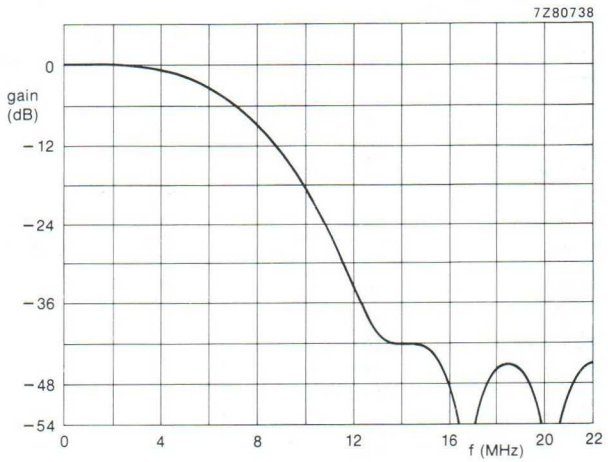


Fig. 4 Frequency response.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to + 7 V
Input voltage range	V_I	−0,5 to + 7 V
Output voltage range to $I_{O\,max}$ = 20 mA	V_O	−0,5 to + 7 V
Maximum power dissipation	P_{tot}	0,5 W
Operating ambient temperature range	T_{amb}	0 to + 70 °C
Storage temperature range	T_{stg}	−65 to + 150 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

T_{amb} = 0 to +70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range	V_{DD}	4,5	5,0	5,5	V
Supply current at V_{DD} = 5,5 V, data outputs not connected, data inputs LOW and frequency nominal	I_{DD}	–	< 100*	65	mA
Inputs					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH (except LL2, LL3)	V_{IH}	2,0	–	V_{DD}	V
Input voltage HIGH (LL2, LL3)	V_{IH}	2,4	–	V_{DD}	V
Input leakage current	I_I	–	–	10	μA
Input capacitance (LL2)	C_I	–	–	10	pF
Input capacitance (LL3)	C_I	–	–	10	pF
Input capacitance (D0 to D6)	C_I	–	–	5	pF
Outputs					
Output voltage HIGH at I_{OH} = −0,5 mA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OH} = 2,0 mA	V_{OL}	0	–	0,6	V
Timing (Fig. 5)					
LL2 cycle time	t_{C2}	46	–	53	ns
LL2 duty factor t_{C2H}/t_{C2}	–	45	–	55	%
LL2 rise and fall time	t_r, t_f	–	–	6**	ns
LL3 cycle time	t_{C3}	69	–	80	ns
LL3 duty factor t_{C3H}/t_{C3}	–	45	–	55	%
LL3 rise and fall time	t_r, t_f	–	–	6**	ns
Skew time	t_{skew}	−2	–	+ 2	ns
Input data set-up time	t_{SU}	12	–	–	ns
Input data hold time	t_{HD}	3	–	–	ns
Output data load capacitance	C_L	7,5	–	15	pF
Output data hold time	t_{OH}	3	–	–	ns
Output data delay time	t_{OD}	–	–	33	ns

* For digital TV application.

** Difference between t_r, t_f of LL2 and t_r, t_f of LL3 shall be less than 2 ns. Rising and falling edges of clocks are assumed to be smooth due to low pass filtering.

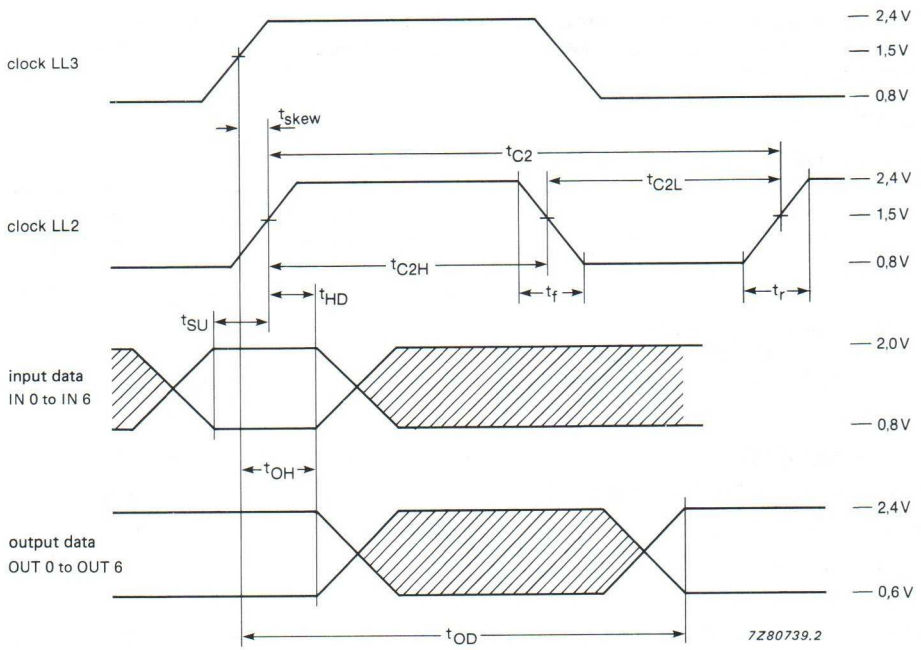


Fig. 5 Timing diagram.

Video enhancement and D/A processor (VEDA)

SAA9065

1. FEATURES

- CMOS circuit to enhance video data and to convert luminance and colour-difference signals from digital-to-analog
- 16-bit parallel input for 4:1:1 and 4:2:2 YUV data
- Data clock input LLC (line-locked clock) for a data rate up to 30 MHz
- 8-bit luminance and 8-bit multiplexed colour-difference formats (optional 7-bit formats)
- MC input to support various clock and pixel rates
- Formatter for YUV input data; 4:2:2 format, 4:1:1 format and filter characteristics selectable
- HREF input to determine the active line (number of pixels)
- Controllable peaking of luminance signal
- Coring stage with controllable threshold to eliminate noise in luminance signal
- Interpolation filter suitable for both formats to increase the data rate in chrominance path
- Polarity of colour-difference signals selectable
- Separate digital-to-analog converters (9-bit resolution for Y; 8-bit for colour-difference signals)
- 1 V (p-p)/ 75 Ω outputs realized by two resistors
- No external adjustments
- All functions controlled via I^2C-bus

2. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage digital part	4.5	5	5.5	V
V_{DDA}	supply voltage analog part	4.75	5	5.25	V
I_{DD}	total supply current	-	tbf	-	mA
V_{IL}	input voltage LOW on YUV-bus	−0.5	-	0.8	V
V_{IH}	input voltage HIGH on YUV-bus	2	-	V_{DDD}+0.5	V
f_{LLC}	input data rate	-	-	30	MHz
$V_{o\ Y,CD}$	output signal Y, ±(R–Y) and ±(B–Y) (peak-to-peak value)	-	2	-	V
$R_{L\ Y,CD}$	output load resistance	125	-	-	Ω
ILE	DC integral linearity error in output signal (8-bit data)	-	-	1	LSB
DLE	DC differential error in output signal (8-bit data)	-	-	0.5	LSB
T_{amb}	operating ambient temperature range	0	-	70	°C

3. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9065	44	PLCC	plastic	SOT187

4. BLOCK DIAGRAM

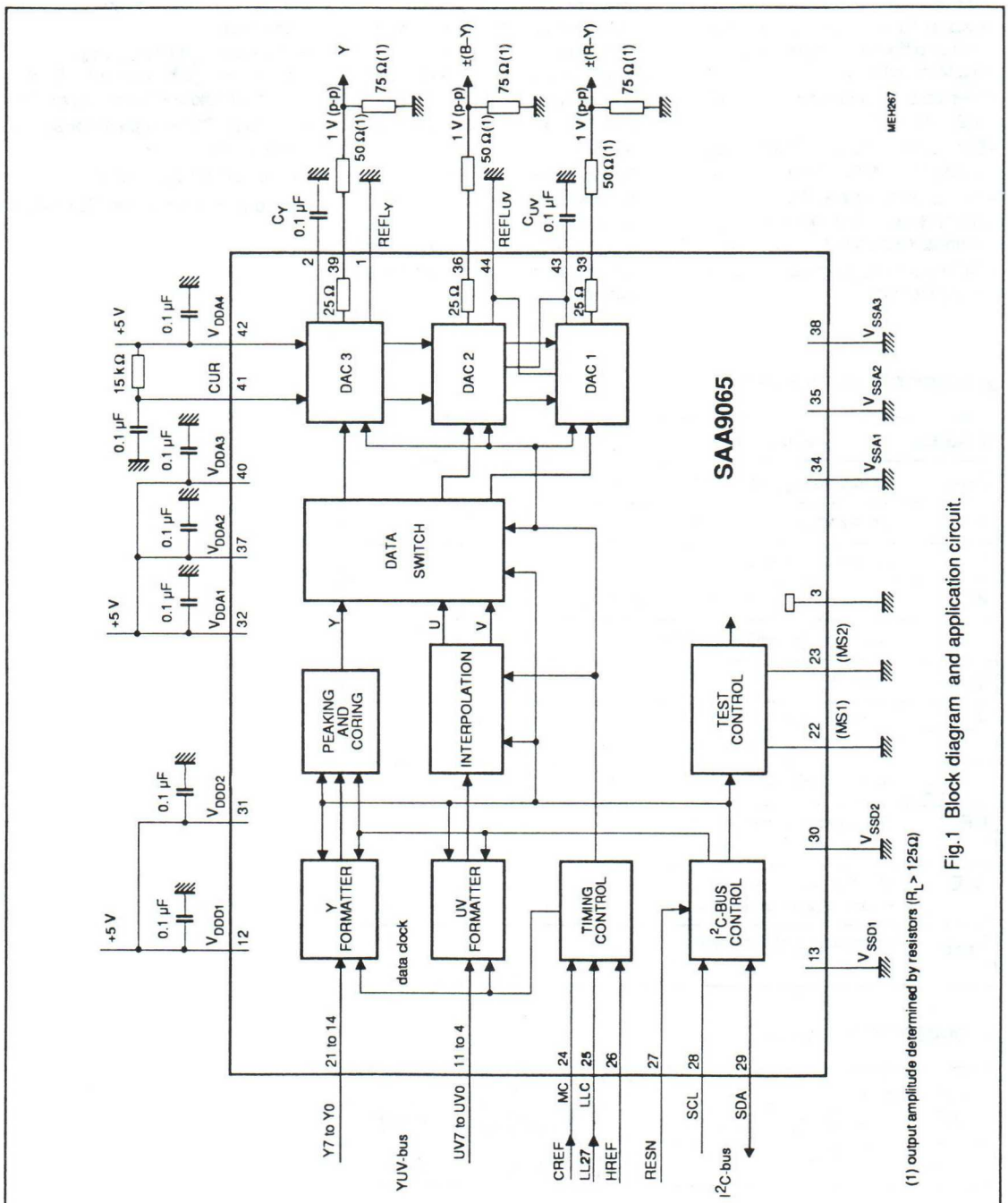


Fig.1 Block diagram and application circuit.

5. PINNING

SYMBOL	PIN	DESCRIPTION
$REFL_Y$	1	low reference of luminance DAC (connected to V_{SSA1})
C_Y	2	capacitor for luminance DAC (high reference)
SUB	3	substrate (connected to V_{SSA1})
UV0	4	UV signal input bits UV7 to UV0 (digital colour-difference signal)
UV1	5	
UV2	6	
UV3	7	
UV4	8	
UV5	9	
UV6	10	
UV7	11	
V_{DDD1}	12	+5 V digital supply voltage 1
V_{SSD1}	13	digital ground 1 (0 V)
Y0	14	Y signal input bits Y7 to Y0 (digital luminance signal)
Y1	15	
Y2	16	
Y3	17	
Y4	18	
Y5	19	
Y6	20	
Y7	21	
MS2	22	mode select 2 input for testing chip
MS1	23	mode select 1 input for testing chip
MC	24	data clock CREF (13.5 MHz e. g.); at MC = HIGH the LLC divider-by-two is inactive
LLC	25	line-locked clock signal (LL27 = 27 MHz)
HREF	26	data clock for YUV data inputs (for active line 768Y or 640Y long)
RESN	27	reset input (active LOW)
SCL	28	I^2C-bus clock line
SDA	29	I^2C-bus data line
V_{SSD2}	30	digital ground 2 (0 V)
V_{DDD2}	31	+5 V digital supply voltage 2
V_{DDA1}	32	+5 V analog supply voltage for buffer of DAC 1
(R–Y)	33	±(R–Y) output signal (analog signal)
V_{SSA1}	34	analog ground 1 (0 V)

SYMBOL	PIN	DESCRIPTION
V_{SSA2}	35	analog ground 2 (0 V)
(B–Y)	36	±(B–Y) output signal (analog colour-difference signal)
V_{DDA2}	37	+5 V analog supply voltage for buffer of DAC 2
V_{SSA3}	38	analog ground 3 (0 V)
Y	39	Y output signal (analog luminance signal)
V_{DDA3}	40	+5 V analog supply voltage for buffer of DAC 3
CUR	41	current input for analog output buffers
V_{DDA4}	42	supply and reference voltage for the three DACs
C_{UV}	43	capacitor for chrominance DACs (high reference)
$REFL_{UV}$	44	low reference of chrominance DACs (connected to V_{SSA1})

PIN CONFIGURATION

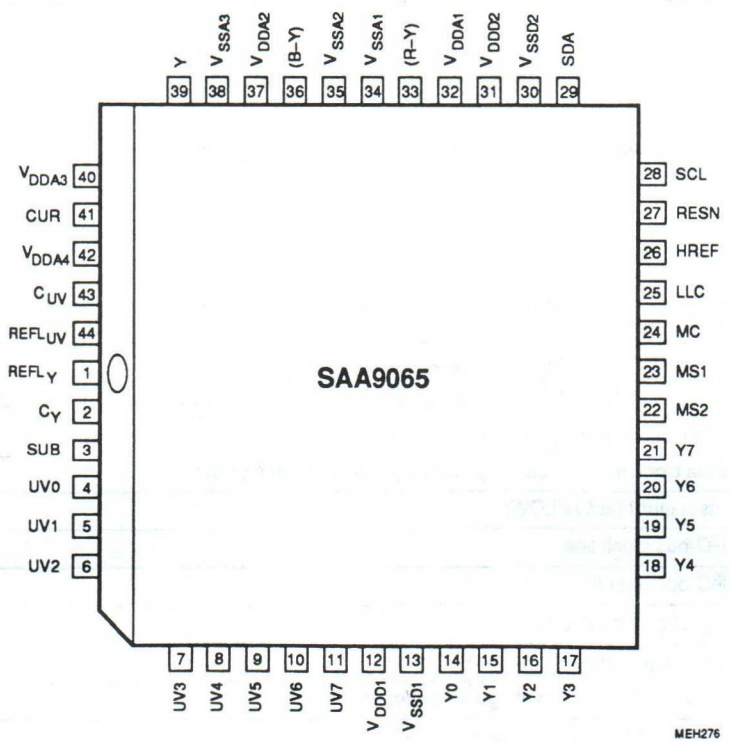


Fig.2 Pin configuration.

6. FUNCTIONAL DESCRIPTION

The CMOS circuit SAA9065 processes digital YUV-bus data up to a data rate of 30 MHz. The data inputs Y7 to Y0 and UV7 to UV0 (Fig.1) are provided with 8-bit data. The data of digital colour-difference signals U and V are in a multiplexed state (serial in 4:2:2 or 4:1:1 format; Tables 2 and 3).

Data is read with the rising edge of LLC (line-locked clock) to achieve a data rate of LLC at MC = HIGH only. If MC is supplied with the frequency CREF (LLC/2 for example), data is read only at every second rising edge (Fig.3).The 7-bit YUV input data are also supported by means of the R78-bit (R78 = 0). Additionally, the luminance data format is converted for internal use into a two´s complement format by inverting MSB. The Y input byte (bits Y7 to Y0) represent luminance information; the UV input byte (bits UV7 to UV0) one of the two digital colour-difference signals in 4:2:2 format (Table 2).

The HREF input signal (HREF = HIGH) determines the start and the end of an active line (Fig.3) the number of pixels respectively . The analog output Y is blanked at HREF = LOW, the (B–Y) and (R–Y) outputs are in a colourless state. The blanking level can be set by the BLV-bit.
The SAA9065 is controllable via the I²C-bus.

Y and UV formatters

The input data formats are formatted into the internally used processing formats (separate for 4:2:2 and 4:1:1 formats). The IFF, IFC and IFL bits control the input data format and determine the right interpolation filter (Figures 10 to 13).

Peaking and coring

Peaking is applied to the Y signal to compensate several bandwidth reductions of the external pre-processing. Y signals can be improved to obtain a better sharpness.
There are the two switchable bandpass filters BF1 and BF 2 controlled via the I²C-bus by the bits BP1, BP0 and BFB. Thus, a frequency response is achieved in combination with the peaking factor K (Figures 5 to 9; K is determined by the bits BFB, WG1 and WG0).

The coring stage with controllable threshold (4 states controlled by CO1 and CO0 bits) reduces noise disturbances (generated by the bandpass gain) by suppressing the amplitude of small high-frequent signal components. The remaining high-frequent peaking component is available for a weighted addition after coring.

Table 1 LLC and MC configuration modes in DMSD applications

PIN	INPUT SIGNAL	COMMENT
LLC MC	LLC (LL27) CREF	The data rate on YUV-bus is half the clock rate on pin LLC, e. g. in SAA7151B, SAA7191 and SAA7191B single scan operation.
LLC MC	LLC (LL27) MC = HIGH	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e. g. in double scan applications.
LLC MC	LLC2/LL3 MC = HIGH	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e. g. SAA9051 single scan operation.
Note: YUV data are only latched with the rising edge of LLC at MC = HIGH.		

Table 2 Data format 4 : 2 : 2. (Fig.3)

INPUT	PIXEL BYTE SEQUENCE					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7(MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Interpolation

The chrominance interpolation filter consists of various filter stages, multiplexers and de-multiplexers to increase the data rate of the colour-difference signals by a factor of 2 or 4. The switching of the filters by the bits IFF, IFC and IFL is described previously. Additional signal samples with significant amplitudes between two consecutive signal samples of the low data rate are generated. The time-multiplexed U and V samples are stored in parallel for converting.

Data switch

The digital signals are adapted to the conversation range. U and V data have 8-bit formats again; Y can have 9 bits dependent on peaking. Blanking and switching to colourless level is applied here. Bits can be inverted by INV-bit to change the polarity of colour-difference output signals.

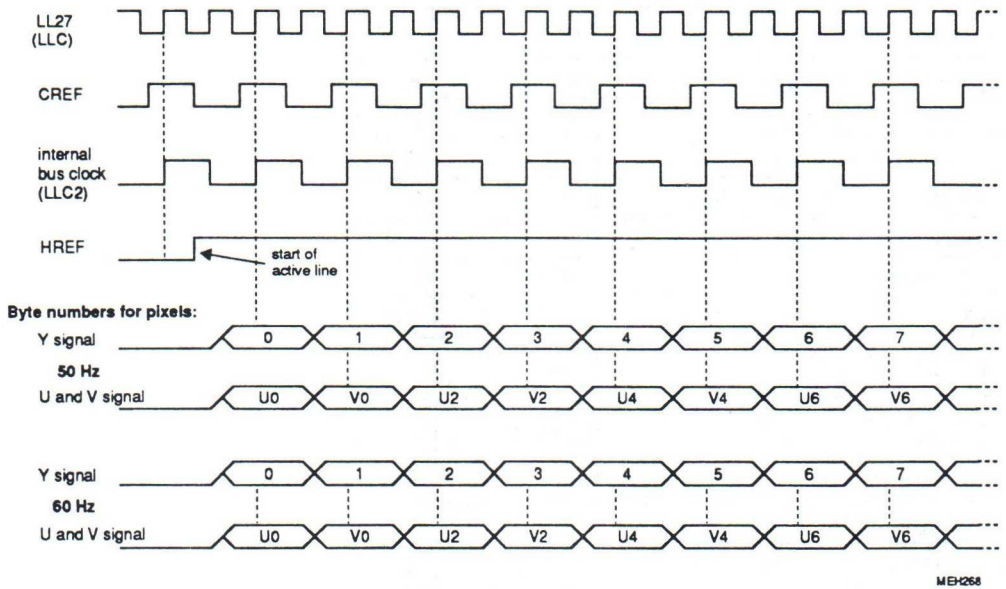
Digital-to-analog converters

Conversion is separate for Y, U and V. The converters use resistor chains with low-impedance output buffers. The minimum output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V floating. An application for 1 V/ 75 Ω on outputs is shown in Fig.1.

Each digital-to-analog converter has its own supply and ground pins suitable for decoupling. The reference voltage, supplying the resistor chain of all three DACs, is the supply voltage V_{DDA4}. The current into pin 41 is 0.3 mA ; a larger current improves the bandwidth but increases the integral non-linearity.

Table 3 Data format 4 : 1 : 1

INPUT	PIXEL BYTE SEQUENCE							
Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			



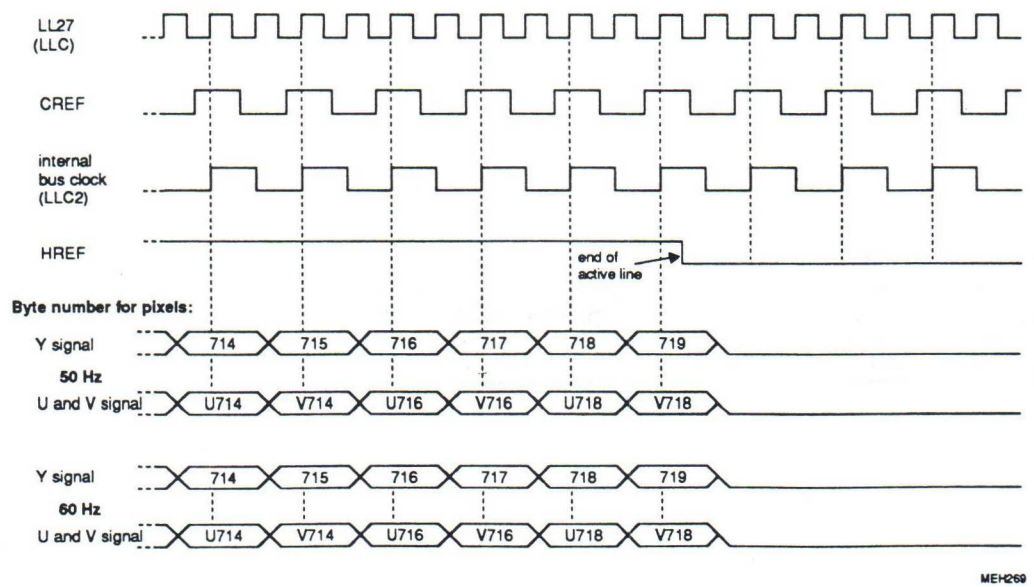


Fig.3 Line control by HREF for 4 : 2 : 2 format, CREF = 13.5 MHz; HREF = 720 pixel; 50 Hz and 60 Hz field.

7. LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD1}	supply voltage range (pin 12)	−0.3	7	V
V_{DDD2}	supply voltage range (pin 31)	−0.3	7	V
V_{DDA1}	supply voltage range (pin 32)	−0.3	7	V
V_{DDA2}	supply voltage range (pin 37)	−0.3	7	V
V_{DDA3}	supply voltage range (pin 40)	−0.3	7	V
V_{DDA4}	supply voltage range (pin 42)	−0.3	7	V
$V_{diff\ GND}$	difference voltage $V_{SSD} - V_{SSA}$	-	±100	mV
V_n	voltage on all input pins 4 to 11, 14 to 27 and 41	−0.3	V_{DDD}	V
V_n	voltage on analog output pins 33, 36 and 39	−0.3	V_{DDD}	V
P_{tot}	total power dissipation	0	tbf	mW
T_{stg}	storage temperature range	−55	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	±2000	-	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

8. THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction-to-ambient in free air	46 K/W

9. CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; LLC = LL27; MC = CREF = 13.5 MHz; T_{amb} = 0 to 70 °C; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD1}	supply voltage range (pin 12)	for digital part	4.5	5	5.5	V
V_{DDD2}	supply voltage range (pin 31)	for digital part	4.5	5	5.5	V
V_{DDA1}	supply voltage range (pin 32)	for buffer of DAC 1	4.75	5	5.25	V
V_{DDA2}	supply voltage range (pin 37)	for buffer of DAC 2	4.75	5	5.25	V
V_{DDA3}	supply voltage range (pin 40)	for buffer of DAC 3	4.75	5	5.25	V
V_{DDA4}	supply voltage range (pin 42)	DAC reference voltage	4.75	5	5.25	V
I_{DDD}	supply current (I_{DDD1} + I_{DDD2})	for digital part	-	tbf	tbf	mA
I_{DDA}	supply current (I_{DDA1} to I_{DDA4})	for DACs and buffers	-	tbf	tbf	mA
YUV-bus inputs (pins 4 to 11 and 14 to 21)		Figures 3 and 4				
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance	V_I = HIGH	-	-	10	pF
I_{LI}	input leakage current		-	-	4.5	µA
Inputs MS1, MS2, MC, LLC, HREF and RESN (pins 22 to 27)						
V_{IL}	input voltage LOW		−0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}+0.5	V
C_I	input capacitance	V_I = HIGH	-	-	10	pF
I_{LI}	input leakage current		-	-	4.5	µA
V_{24}	MC input voltage for LL27	27 MHz data rate	2.0	-	V_{DDD}+0.5	V
	CREF signal on MC input	CREF data rate; note 1	-	-	-	V
I²C-bus SCL and SDA (pins 28 and 29)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3.0	-	V_{DDD}+0.5	V
I_I	input current	V_I = LOW or HIGH	-	-	±10	µA
V_{OL}	SDA output voltage LOW (pin 29)	I_{29} = 3 mA	-	-	0.4	V
I_{29}	output current	during acknowledge	3	-	-	mA
Digital-to-analog converters (pins 1, 2, 41, 42, 43 and 44)						
V_{DAC}	input reference voltage for internal resistor chains (pin 42)		4.75	5	5.25	V
I_{CUR}	input current (pin 41)	R_{41-42} = 15 kΩ	-	300	-	µA
$V_{1,44}$	reference voltage LOW	pin connected to V_{SSA1}	-	0	-	V
C_L	external blocking capacitor to V_{SSA1} for reference voltage HIGH (pins 2 and 43)		-	0.1	-	µF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{LLC}	data conversation rate (clock)	Fig.3	-	-	30	MHz
Res	resolution	luminance DAC	-	9	-	bit
		chrominance DACs	-	8	-	bit
ILE	DC integral linearity error	8-bit data	-	-	1.0	LSB
DLE	DC differential error	8-bit data	-	-	0.5	LSB
Y, ±(R–Y) and ±(B–Y) analog outputs (pins 39, 33 and 36)						
V_o	output signal voltage (peak-to-peak value)	without load	-	2	-	V
$V_{33,36,39}$	output voltage range	without load; note 2	0.2	-	2.2	V
V_{39}	output blanking level	Y output; note 3	-	16	-	LSB
$V_{33,36}$	output no-colour level	±(R–Y), ±(B–Y); note 4	-	128	-	LSB
$R_{33,36,39}$	internal serial output resistance		-	25	-	Ω
$R_{L\ 33,36,39}$	output load resistance	external load	125	-	-	Ω
B	output signal bandwidth	-3 dB	20	-	-	MHz
t_d	signal delay from input to Y output		-	tbf	-	ns
LLC timing (pins 25)		LLC; Fig.3				
t_{LLC}	cycle time		33	37	41	ns
$t_{p\,H}$	pulse width		40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
YUV-bus timing (pins 4 to 11 and 14 to 21)		Fig.5				
t_{SU}	input data set-up time		11	-	-	ns
t_{HD}	input data hold time		3	-	-	ns
MC timing (pin24)		Fig.5				
t_{SU}	input data set-up time		11	-	-	ns
t_{HD}	input data hold time		3	-	-	ns
RESN timing (pin 27)						
t_{SU}	set-up time after power-on or failure	active LOW; note 5	4 x t_{LLC}	-	-	ns

Notes to the characteristics

1. YUV-bus data is read at MC = HIGH (pin 24) clocked with LLC (Fig.5) . Data is read only with every second rising edge of LLC when CREF = LLC/2 on MC-pin 24.
2. 0.2 to 2.2 V ouput voltage range at 8-bit DAC input data. The data word can increase to 9-bit dependent on peaking factor.
3. The luminance signal is set to the digital black level: 16 LSB for BLV-bit = 0; 0 LSB for BLV-bit = 1.
4. The chrominance amplitudes are set to the digital colourless level of 128 LSB.
5. The circuit is prepared for a new data initialization.

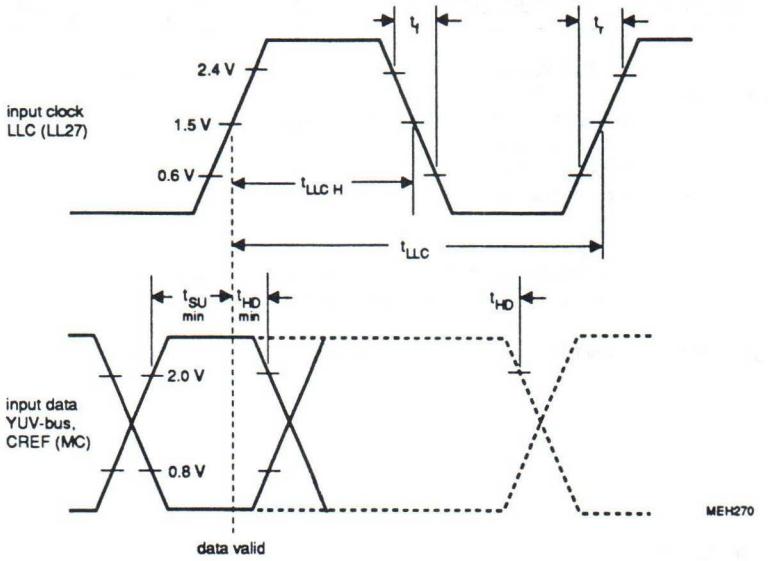


Fig.4 YUV-bus data and CREF timing.

PROCESSING DELAY	LLC CYCLES	REMARKS
YUV digital input to YUV analog output	44 88	at MC = "1" at MC = LLC/2

10. I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = **1011 111X**
A = acknowledge, generated by the slave
SUBADDRESS* = subadress byte (Table 4)
DATA = data byte (Table 4)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 4 I²C-bus transmission

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Peaking and coring	01	0	CO1	CO0	BP1	BP0	BFB	WG1	WG0
Input formats; interpolation	02	IFF	IFC	IFL	0	0	0	0	0
Input/output setting	03	0	0	0	0	DRP	BLV	R78	INV

Bit functions in data bytes:

CO1 to CO0 — Control of coring threshold:

CO1	CO0	
0	0	coring off
0	1	small noise reduction
1	0	medium noise reduction
1	1	high noise reduction

BP1, BP0 and BFB — Bandpass filter selection:

BP1	BP0	BFB	
0	0	0	characteristic Fig.5
0	1	0	characteristic Fig.6
1	0	0	characteristic Fig.7
1	1	0	characteristic Fig.8
0	0	1	BF1 filter bypassed Fig.9
X	X	1	not recommended

BFB, WG1 and WG0	Peaking factor K:	BFB	WG1	WG0	
		0	0	0	K = 1/8; minimum peaking
		0	0	1	K = 1/4
		0	1	0	K = 1/2
		0	1	1	K = 1; maximum peaking
		1	0	0	K = 0; peaking off
		1	0	1	K = 1/4; minimum peaking
		1	1	0	K = 1/2
		1	1	1	K = 1; maximum peaking
IFF, IFC, IFL	Input format and filter control at 13.5 MHz data rate:	IFF	IFC	IFL	
		0	0	0	4 : 1 : 1 format; –3 dB attenuation at 1.6 MHz video frequency; Fig.10
		0	0	1	4 : 1 : 1 format; –3 dB attenuation at 600 kHz video frequency; Fig.11
		0	1	0	4 : 1 : 1 format; –3 dB attenuation at 1.2 MHz video frequency; Fig.12
		1	0	0	4 : 2 : 2 format; –3 dB attenuation at 1.6 MHz video frequency; Fig.10
		1	0	1	4 : 2 : 2 format; –3 dB attenuation at 600 kHz video frequency; Fig.11
		1	1	X	4 : 2 : 2 format; –3 dB attenuation at 2.5 MHz video frequency; Fig.13
DRP	UV input data code:	0 = two´s complement; 1 = offset binary			
BLV	Blanking level on Y output:	0 = 16 LSB; 1 = 0 LSB			
R78	YUV input data solution:	0 = 7-bit data; 1 = 8-bit data			
INV	Polarity of colour-difference output signals:	0 = normal polarity equal to input signal 1 = inverted polarity			

Purchase of Philips´ I²C components conveys a license under the Philips´ I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

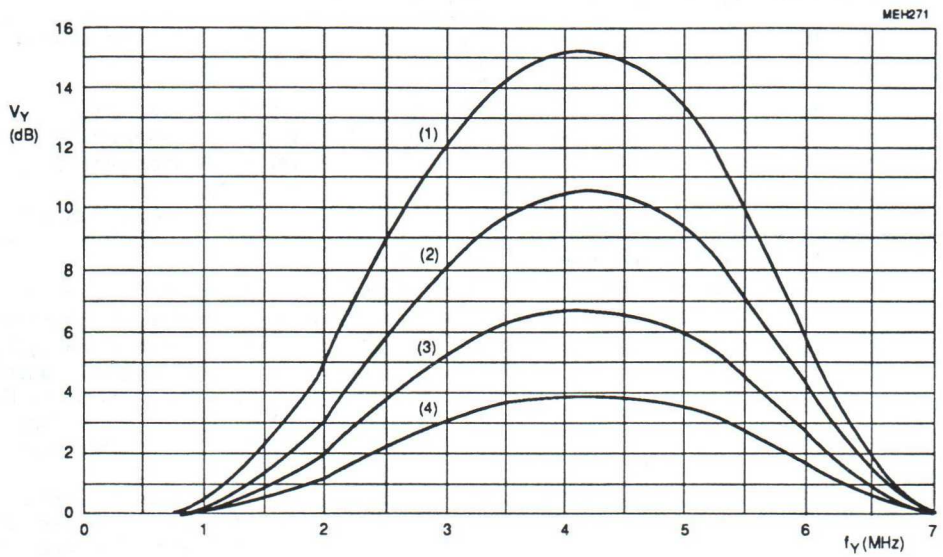


Fig.5 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 0 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

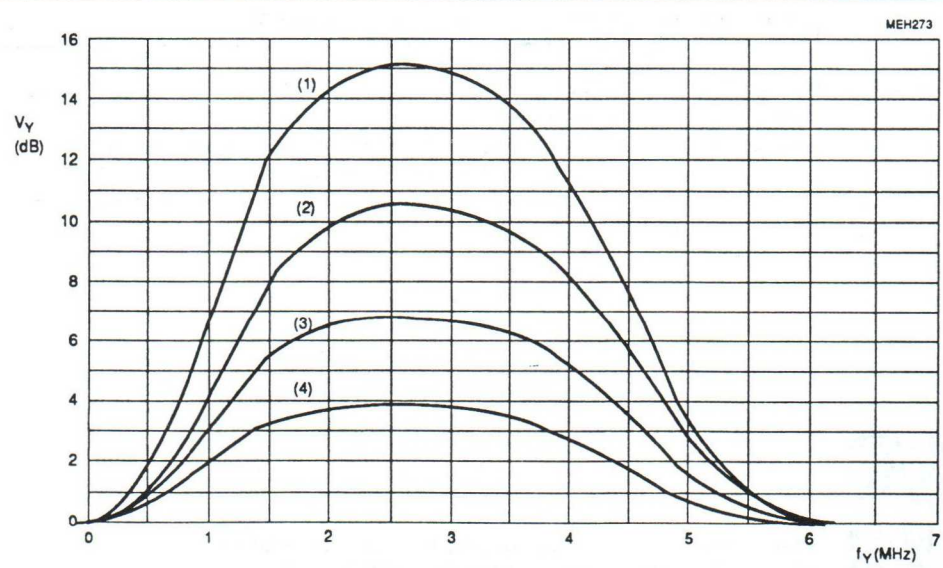


Fig.6 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 1 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

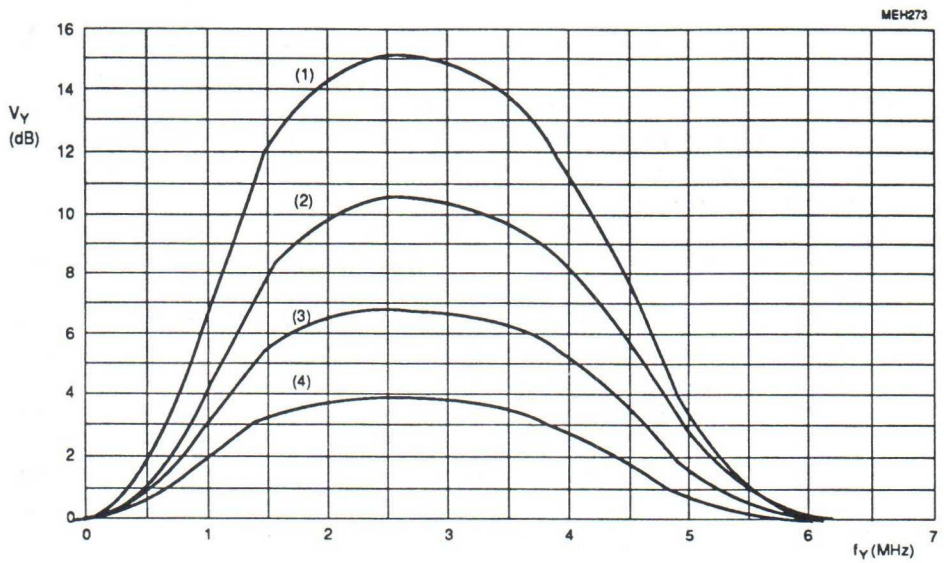


Fig.7 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 0 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

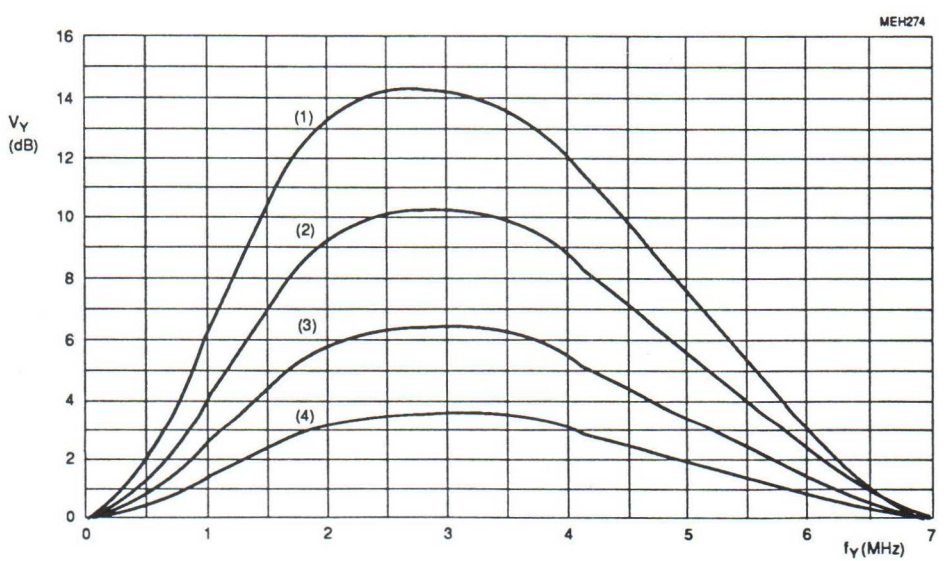


Fig.8 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 1 and BFB = 0: (1) K = 1; (2) K = 1/2; (3) K = 1/4 and (4) K = 1/8.

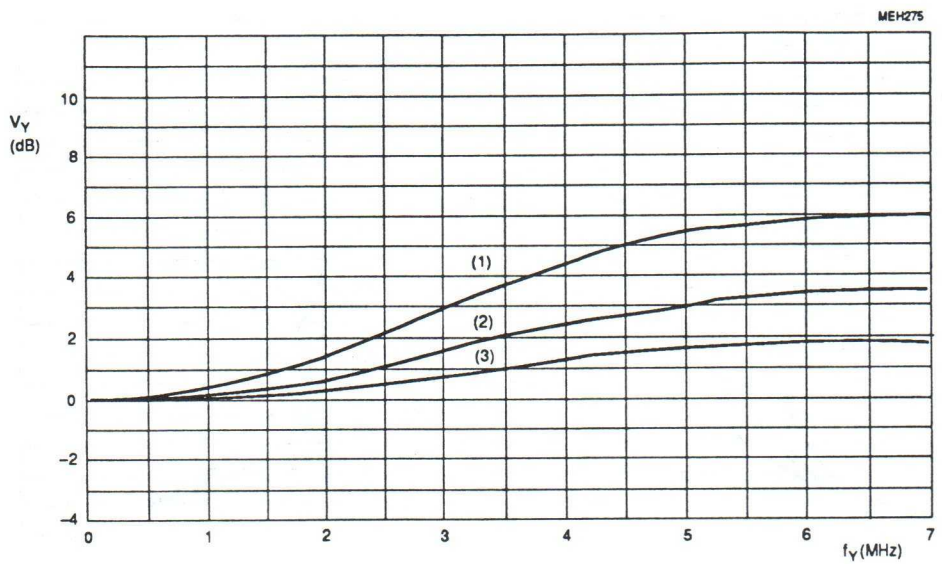


Fig.9 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 0 and BFB = 1; bandpass filter BF1 bypassed and peaking off; (1) K = 1; (2) K = 1/2; (3) K = 1/4.

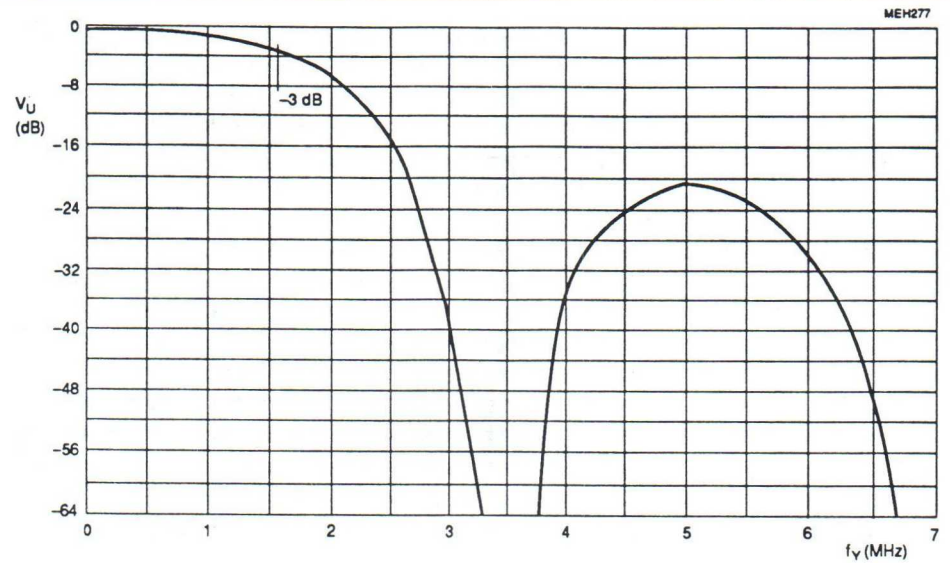


Fig.10 Interpolation filter with I²C-bus control bits IFF = 0; IFC = 0 and IFL = 0 in 4:1:1 format, and control bits IFF = 1; IFC = 0 and IFL = 0 in 4:2:2 format; 13.5 MHz data rate.

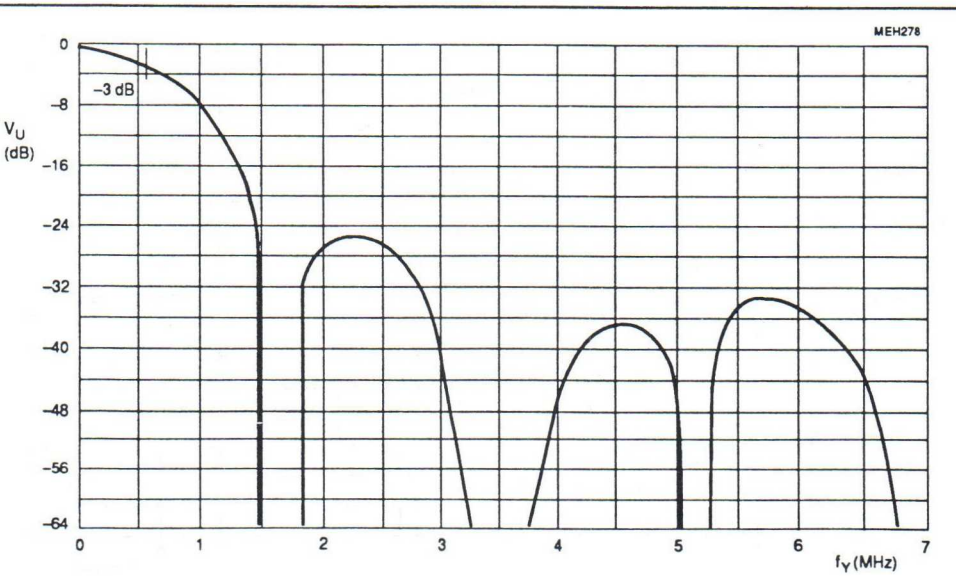


Fig.11 Interpolation filter with I²C-bus control bits IFF = 0; IFC = 0 and IFL = 1 in 4:1:1 format, and control bits IFF = 1; IFC = 0 and IFL = 1 in 4:2:2 format; 13.5 MHz data rate.

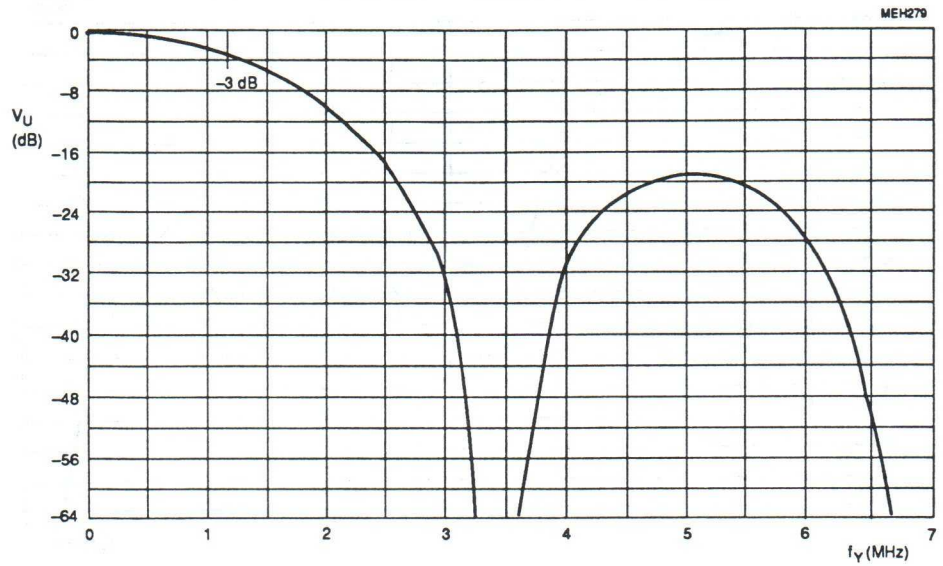


Fig.12 Interpolation filter with I²C-bus control bits IFF = 0; IFC = 1 and IFL = 0 in 4:1:1 format; 13.5 MHz data rate.

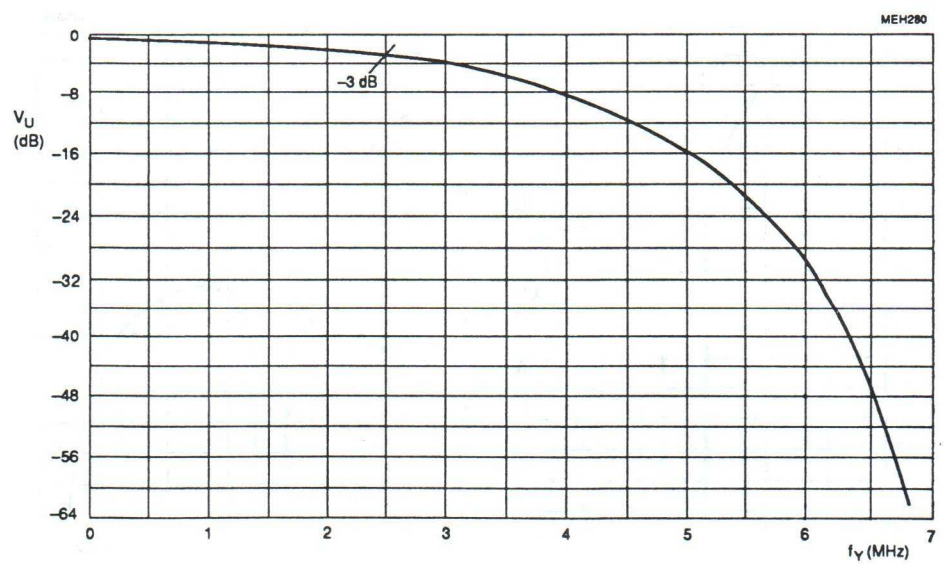


Fig.13 Interpolation filter with I²C-bus control bits IFF = 1; IFC = 1 and IFL = X in 4:2:2 format; 13.5 MHz data rate.

7-BIT ANALOGUE-TO-DIGITAL CONVERTER (ADC 7)

GENERAL DESCRIPTION

The SAA9079 is a monolithic NMOS 7-bit analogue-to-digital converter (ADC) designed for video applications. The device converts the analogue input signal into 7-bit binary coded digital words at a sampling rate of 22 MHz.

The circuit comprises 129 comparators, a reference resistor chain, combining logic, transcoder stages, and TTL output buffers which are positive edge triggered and can be switched into 3-state mode. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

Features

- 7-bit resolution
- No external sample and hold required
- High input impedance
- Binary or two's complement 3-state TTL outputs
- Overflow and underflow 3-state TTL outputs
- All outputs positive-edge triggered
- Standard 24-pin package

Applications

- High-speed A/D conversion
- Video signal digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research

QUICK REFERENCE DATA

Measured over full voltage and temperature range unless otherwise specified

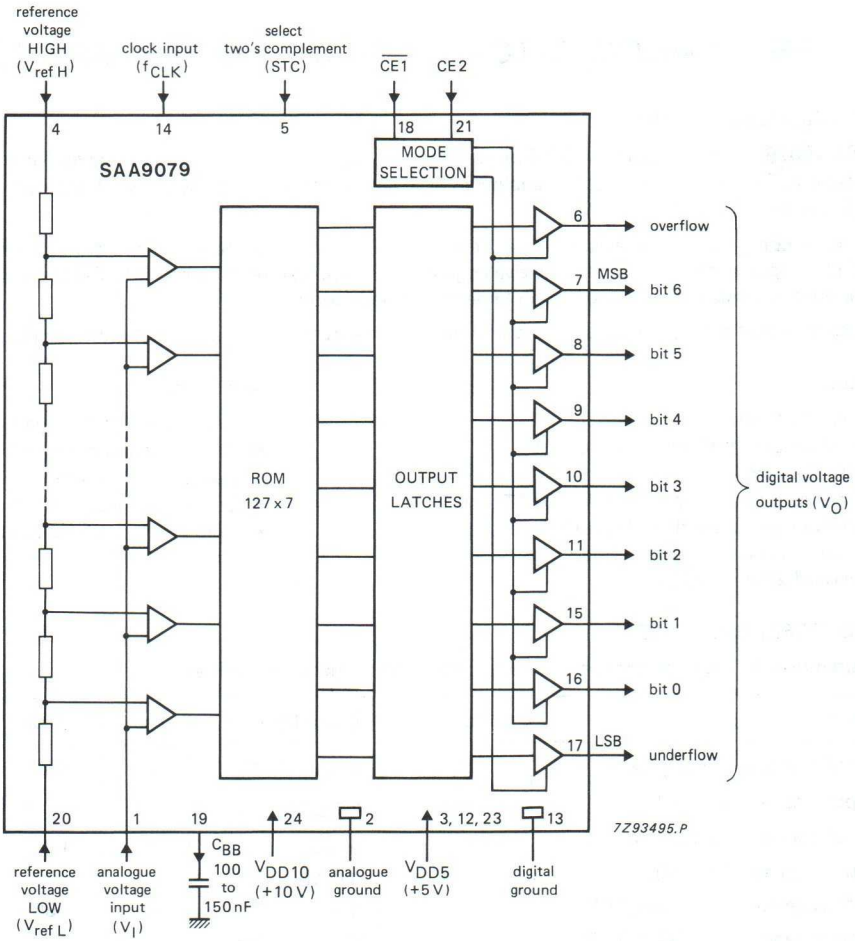
parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pins 3, 12, 23)		V_{DD5}	4.5	–	5.5	V
Supply voltage (pin 24)		V_{DD10}	9.5	–	10.5	V
Supply current (pins 3, 12, 23)	note 1	I_{DD5}	–	–	65	mA
Supply current (pin 24)	note 1	I_{DD10}	–	–	13	mA
Reference current (pins 4, 20)		I_{ref}	150	–	450	μA
Reference voltage LOW (pin 20)		V_{refL}	2.4	2.5	2.6	V
Reference voltage HIGH (pin 4)		V_{refH}	5.0	5.1	5.2	V
Non-linearity	f_i = 1.1 kHz					
integral		INL	–	–	± ½	LSB
differential		DNL	–	–	± ½	LSB
–3 dB Bandwidth		B	11	–	–	MHz
Clock frequency (pin 14)		f_{CLK}	1	–	22	MHz
Total power dissipation	note 1	P_{tot}	–	–	500	mW

Note to quick reference data

1. Measured under nominal conditions: V_{DD5} = 5 V; V_{DD10} = 10 V; T_{amb} = 22 °C.

PACKAGE OUTLINES

24-lead DIL; plastic (SOT101A).
24-lead mini-pack; plastic (SO24; SOT137A).



Note

All three pins 3, 12 and 23 must be connected to positive supply voltage + 5 V.

Fig. 1 Block diagram.

DEVELOPMENT DATA

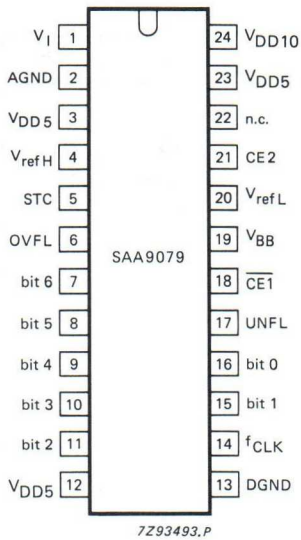


Fig. 2 Pinning diagram.

PINNING

1	V_I	analogue voltage input
2	AGND	analogue ground
3	V_{DD5}	positive supply voltage (+ 5 V)
4	V_{refH}	reference voltage HIGH
5	STC	select two's complement
6	OVFL	overflow
7	bit 6	most-significant bit (MSB)
8	bit 5	
9	bit 4	
10	bit 3	
11	bit 2	
12	V_{DD5}	positive supply voltage (+ 5 V)
13	DGND	digital ground
14	f_{CLK}	clock input
15	bit 1	
16	bit 0	least-significant bit (LSB)
17	UNFL	underflow
18	$\overline{CE1}$	chip enable input 1
19	V_{BB}	back bias output
20	V_{refL}	reference voltage LOW
21	CE2	chip enable input 2
22	n.c.	not connected
23	V_{DD5}	positive supply voltage (+ 5 V)
24	V_{DD10}	positive supply voltage (+ 10 V)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pins 3, 12, 23)	V_{DD5}	−0.5	+ 7.0	V
Supply voltage range (pin 24)	V_{DD10}	−0.5	+ 12.0	V
Input voltage range	V_I	−0.5	+ 7.0	V
Output current	I_O	–	5	mA
Total power dissipation	P_{tot}	–	1	W
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

$V_{DD5} = V_{3, 12, 23-13} = 4.5$ to 5.5 V; $V_{DD10} = V_{24-2} = 9.5$ to 10.5 V; $C_{BB} = 100$ nF; $T_{amb} = 0$ to + 70 °C

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pins 3, 12, 23)	V_{DD5}	4.5	–	5.5	V
Supply voltage (pin 24)	V_{DD10}	9.5	–	10.5	V
Supply current (pins 3, 12, 23)	I_{DD5}	–	–	85	mA
Supply current (pin 24)	I_{DD10}	–	–	18	mA
Reference voltages					
Reference voltage LOW (pin 20)	V_{refL}	2.4	2.5	2.6	V
Reference voltage HIGH (pin 4)	V_{refH}	5.0	5.1	5.2	V
Reference current	I_{ref}	150	–	450	μA
Inputs					
Clock input (pin 14)					
Input voltage LOW	V_{IL}	−0.3	–	0.8	V
Input voltage HIGH (note 1)	V_{IH}	3.0	–	V_{DD5}	V
Digital input levels (pins 5,18,21; note 2)					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD5}	V
Input current					
at $V_5 = 0$ V; V_{13} = GND	$-I_5$	15	–	70	μA
at $V_{18} = 5$ V; V_{13} = GND	I_{18}	15	–	70	μA
at $V_{21} = 0$ V; V_{13} = GND	$-I_{21}$	15	–	120	μA
Input leakage current (except pins 5, 18 and 21)	I_{LI}	–	–	10	μA
Analogue input levels (pin 1) at $V_{refL} = 2.5$ V; $V_{refH} = 5.1$ V					
Input voltage amplitude (peak-to-peak value)	$V_{I(p-p)}$	–	2.6	–	V
Input capacitance (note 3)	C_{1-2}	–	–	30	pF

Notes to characteristics

1. Maximum input voltage must not exceed 5.0 V.
2. If pin 5 is LOW binary coding is selected.
   If pin 5 is HIGH two's complement is selected.
   If pin 5, 18 and 21 are open-circuit, pin 5, 21 are HIGH and pin 18 is LOW.
   For output coding see Table 1 and mode selection see Table 2.
3. Tested on sample base.

parameter	symbol	min.	max.	unit
Outputs				
Digital voltage outputs (pins 6 to 11 and 15 to 17)				
Output voltage LOW at I_O = 2 mA	V_{OL}	0	+0.4	V
Output voltage HIGH at $-I_O$ = 0.5 mA	V_{OL}	2.4	V_{DD5}	V

Table 1 Output coding (V_{refL} = 2.50 V; V_{refH} = 5.08 V)

step	V_{1-2} note 1	UNFL	OVFL	binary bit 6 – bit 0	two's complement bit 6 – bit 0
underflow	< 2.51	1	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
0	2.51	0	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
1	2.53	0	0	0 0 0 0 0 0 1	1 0 0 0 0 0 1
.	.	.	.	. . . .	. . . .
.	.	.	.	. . . .	. . . .
.	.	.	.	. . . .	. . . .
126	5.03	0	0	1 1 1 1 1 1 0	0 1 1 1 1 1 0
127	5.05	0	0	1 1 1 1 1 1 1	0 1 1 1 1 1 1
overflow	⩾ 5.07	0	1	1 1 1 1 1 1 1	0 1 1 1 1 1 1

steps 2-125

DEVELOPMENT DATA

Note to Table 1

1. Approximate values.

Table 2 Mode selection

$\overline{CE1}$	CE2	bit 0 to bit 6	UNFL, OVFL
X	0	HIGH impedance	HIGH impedance
0	1	active	active
1	1	HIGH impedance	active

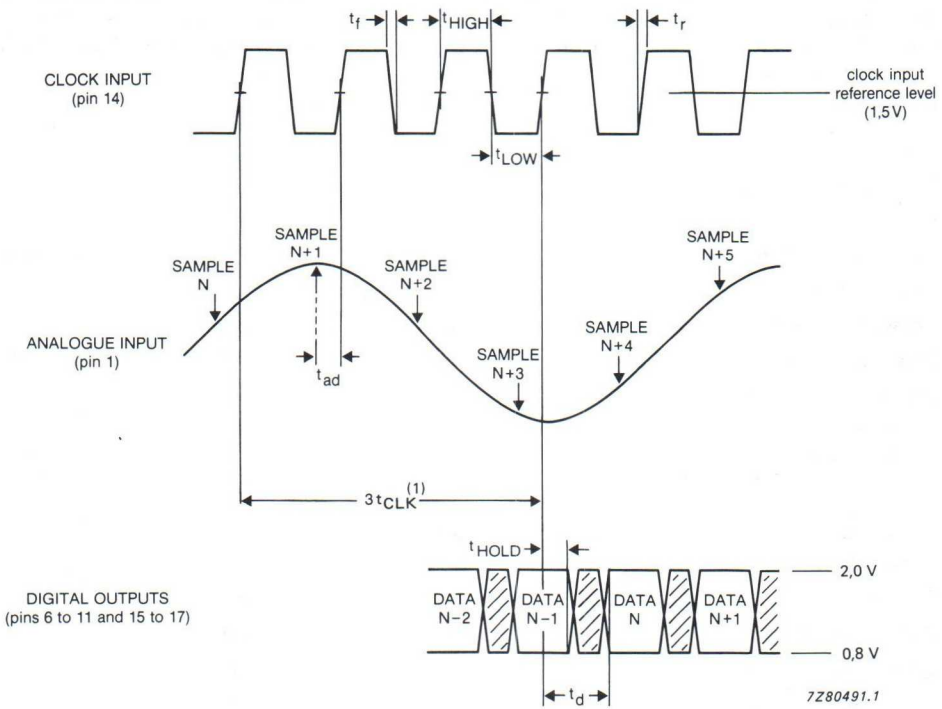
CHARACTERISTICS (continued)

$V_{DD5} = V_{3, 12, 23-13} = 4.5$ V to 5.5 V; $V_{DD10} = V_{24-2} = 9.5$ V to 10.5 V; $V_{refL} = 2.5$ V; $V_{refH} = 5.1$ V; $f_{CLK} = 22$ MHz; $C_{BB} = 100$ nF; $T_{amb} = 0$ to + 70 °C

parameter	symbol	min.	max.	unit
Timing characteristics (see also Fig. 3)				
Clock input (pin 14)				
Clock frequency	f_{CLK}	1	22	MHz
Clock cycle time LOW	t_{LOW}	20	–	ns
Clock cycle time HIGH	t_{HIGH}	20	–	ns
Input rise and fall times (pin 1)				
rise time	t_r	–	5	ns
fall time	t_f	–	5	ns
Analogue input (note 1)				
Bandwidth (–3 dB)	B	11	–	MHz
Non-harmonic noise		–	–36	dB
Peak error (non-harmonic noise)		–	3	LSB
Harmonics (full scale)				
fundamental	f_0	–	0	dB
RMS (2nd and 3rd harmonic)	$f_{2.3}$	–	–28	dB
RMS (4th + 5th + 6th + 7th harmonic)	f_{4-7}	–	–35	dB
Digital outputs (notes 1 and 2)				
Output hold time	t_{HOLD}	6	–	ns
Output delay time at $C_L = 15$ pF	t_d	–	38	ns
Output delay time at $C_L = 50$ pF	t_d	–	48	ns
3-state delay time	t_{dt}	–	25	ns
Capacitive output load	C_{OL}	0	15	pF
Transfer function				
Non-linearity at $f_i = 1.1$ kHz				
integral	INL	–	± ½	LSB
differential	DNL	–	± ½	LSB

Notes to timing characteristics

1. Clock input rise and fall times are at the maximum clock frequency (10% and 90% levels).
2. The timing values of the digital outputs at pins 6 to 11 and 15 to 17 are measured with the clock input reference level at 1.5 V.



(1) There is a delay of 3 clock cycles between sampling of an analogue input signal and the corresponding digital output.

Fig. 3 Timing diagram.

APPLICATION INFORMATION

The minimum and maximum values provided in the data sheet are guaranteed over the whole voltage and temperature range. This note gives additional information to the data sheet where the typical values indicate the behaviour under nominal conditions; V_{DD5} = 5 V, V_{DD10} = 10 V, T_{amb} = 22 °C.

parameter	symbol	typ.	unit
Supply			
Supply current (pins 3, 12, 23)	I_{DD5}	51	mA
Supply current (pin 24)	I_{DD10}	11	mA
Maximum clock frequency	f_{CLK}	25	MHz
Bandwidth (−3 dB)	B	20	MHz
Total power dissipation	P_{tot}	365	mW
Peak error (non-harmonic noise)		1.5	LSB
Suppression of harmonics			
sum of:			
$f_{2nd} + f_{3rd}$		31	dB
$f_{4th} + f_{5th} + f_{6th} + f_{7th}$		39	dB
Non-linearity			
integral	INL	± 1/4	LSB
differential	DNL	± 1/3	LSB
Differential gain	dG	± 3	%
Differential phase	dP	± 1	%
Large signal phase error	P_e	10	deg
Non-harmonic noise		40	dB
Duty factor (20.25 MHz)		50 ± 10	%

Typical values are measured on sample base.

Application recommendation

Spikes at the 10 V supply input must be avoided (e. g. overshoots during switching).
Even a spike duration of less than 1 μs can destroy the device.

Test philosophy

Fig. 4 is a block diagram showing analogue-to-digital testing with a phase locked signal source. The signal generator provides a 5 MHz sinewave for the device under test (except for the linearity test). The 22 MHz clock input is provided by the clock generator. The phase relationship between signal and clock generator is shifted by 100 pico sec. each signal period to provide an effective clock rate of 10 GHz for analysis.

Most calculations are carried out in the spectral domain using Fast Fourier Transformation (FFT) and the inverse FFT to return to time domain.

The successive processing completes the specific measurement (Fig. 5 and 6).

The non-linearities of the converter, integral (INL) and differential (DNL), are measured using a low frequency ramp signal. Within a general uncertain range of conversion between two steps the output signal of the converter randomly switches.

After low-pass filtering the different step width is used for calculating the line of least squares to obtain integral non-linearity.

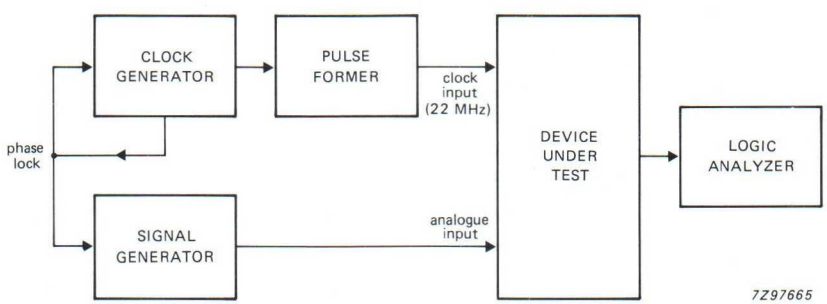
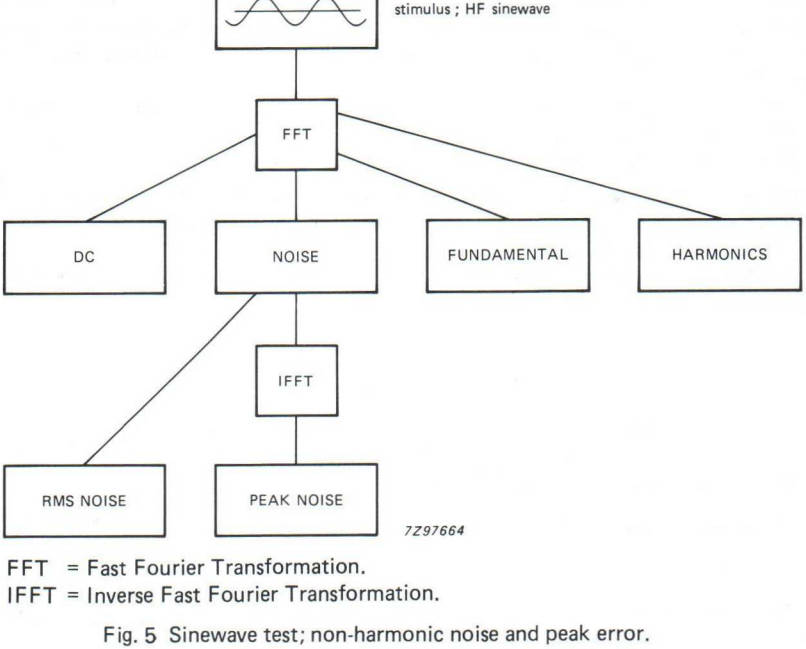


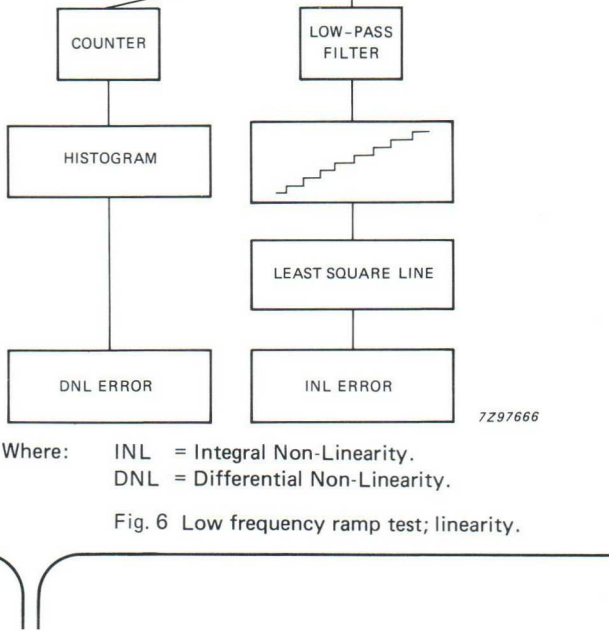
Fig. 4 Analogue-to-digital converter testing with locked signal source.

APPLICATION INFORMATION (continued)



Where: FFT = Fast Fourier Transformation.
IFFT = Inverse Fast Fourier Transformation.

Fig. 5 Sinewave test; non-harmonic noise and peak error.



Where: INL = Integral Non-Linearity.
DNL = Differential Non-Linearity.

Fig. 6 Low frequency ramp test; linearity.

SENSITIVE 1 GHz DIVIDE-BY-64/DIVIDE-BY-256 SWITCHABLE PRESCALER

GENERAL DESCRIPTION

The SAB6456/SAB6456T is a prescaler for UHF/VHF tuners. It can be switched to divide-by-64 or divide-by-256 by the mode-control (MC) pin. The circuit has an input frequency range of 70 MHz to 1 GHz, has high input sensitivity and good harmonic suppression.

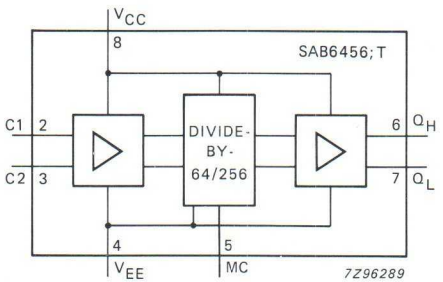


Fig. 1 Block diagram.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 8 to pin 4	V_{CC}	4,5	5,0	5,5	V
Supply current	pin 8	I_{CC}	–	21	–	mA
Input frequency range	pins 2 and 3	f_i	70	–	1000	MHz
Sensitivity to input voltage (r.m.s. value)		$V_{i(rms)}$	–	–	10	mV
Output voltage (peak-to-peak value)	pins 6 and 7	$V_{o(p-p)}$	–	1	–	V
Operating ambient temperature range		T_{amb}	0	–	80	°C

PACKAGE OUTLINES

SAB6456 : 8-lead DIL; plastic (SOT97).
SAB6456T: 8-lead mini-pack (SO8; SOT96A).

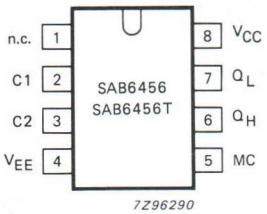


Fig. 2 Pinning diagram.

PINNING

1.	n.c.	not connected
2.	C1	differential inputs
3.	C2	
4.	V_{EE}	ground (0 V)
5.	MC	mode control
6.	Q_H	complementary outputs
7.	Q_L	
8.	V_{CC}	positive supply voltage

FUNCTIONAL DESCRIPTION

The circuit comprises an input amplifier, a divider stage with selectable division ratio and an output stage.

The input amplifier is driven by a sinusoidal signal from the local oscillator of a television tuner. The inputs (C1, C2) are differential and are biased internally to permit capacitive coupling. When driven asymmetrically the unused input should be connected to ground via a capacitor.

The mode-control (MC) input to the divider stage is intended for static control of the division ratio, selection is made as follows:

divide-by-64 : MC pin open-circuit

divide-by-256: MC pin connected to ground

The divider stage may oscillate during no-signal conditions but this oscillation is suppressed when input signals are received.

Two complementary signals (Q_H, Q_L) are provided by the output differential amplifier stage. The voltage-edges of the output signals are slowed internally to reduce harmonics in the television intermediate frequency band.

ELECTROSTATIC DISCHARGE PROTECTION

Inputs and outputs have electrostatic discharge protection according to specification MIL-883C, class B.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC-134)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 8 to pin 4	V_{CC}	–	–	7,0	V
Input voltage		V_i	–	–	V_{CC}	V
Storage temperature range		T_{stg}	−55	–	+150	°C
Junction temperature		T_j	–	–	+150	°C

THERMAL RESISTANCE

From junction to ambient

8-lead DIL; plastic (SOT-97A)	$R_{th\ j\text{-}a}$	120 K/W
8-lead mini-pack (SO-8; SOT-96A)		
on printed circuit board	$R_{th\ j\text{-}a}$	260 K/W
on ceramic substrate	$R_{th\ j\text{-}a}$	170 K/W

D.C. CHARACTERISTICS

V_{CC} = 5 V; V_{EE} = 0 V; T_{amb} = 25 °C; test IC mounted in a test socket or on a printed circuit board; measurements taken after thermal equilibrium is established

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW		V_{OL}	–	–	V_{CC} −0,8	V
Supply current		I_{CC}	–	21	28	mA
Mode-control (MC)						
Input voltage LOW (divide-by-256)		V_{IL}	0	–	0,2	V
Input current LOW		$-I_L$	–	25	60	μA
Input voltage HIGH (divide-by-64)	pin 5 open-circuit	V_{IH}	1,4	–	3,0	V

A.C. CHARACTERISTICS

V_{CC} = 4,5 to 5,5 V; V_{EE} = 0 V; T_{amb} = 0 to +80 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Sensitivity to input voltage (r.m.s. value)	50 Ω system					
	f_i = 70 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 150 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 300 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 500 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 900 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 1000 MHz	$V_{i(rms)}$	–	–	10	mV
Input overload voltage (r.m.s. value)	50 Ω system f_i = 70 MHz to 1000 MHz	V_i	300	–	–	mV
Input parallel resistance	f_i = 70 MHz	R_i	–	560	–	Ω
	f_i = 1000 MHz	R_i	–	30	–	Ω
Input capacitance	f_i = 70 MHz	C_i	–	5	–	pF
	f_i = 1000 MHz	C_i	–	1,5	–	pF
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW		V_{OL}	–	–	V_{CC} –0,8	V
Output voltage swing (peak-to-peak value)	f_i = 70 MHz	$V_{o(p\text{-}p)}$	0,8	1,0	1,2	V
	f_i = 1000 MHz; R_L = 820 Ω; C_L = 60 pF	$V_{o(p\text{-}p)}$	0,17	–	–	V
Attenuation of third harmonic at output	f_i = 800 MHz; R_L = 820 Ω; C_L = 60 pF		–15	–23	–	dB
Output unbalance	see Fig. 3	ΔV_o	–	–	0,1	V
Output resistance		R_o	–	500	–	Ω

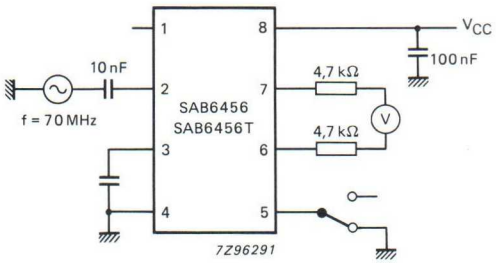


Fig. 3 Test circuit for output unbalance measurement.

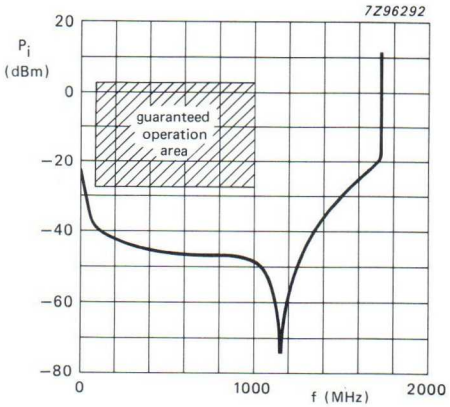


Fig. 4 Typical input sensitivity curve: V_{CC} = 5 V; T_{amb} = 25 °C.

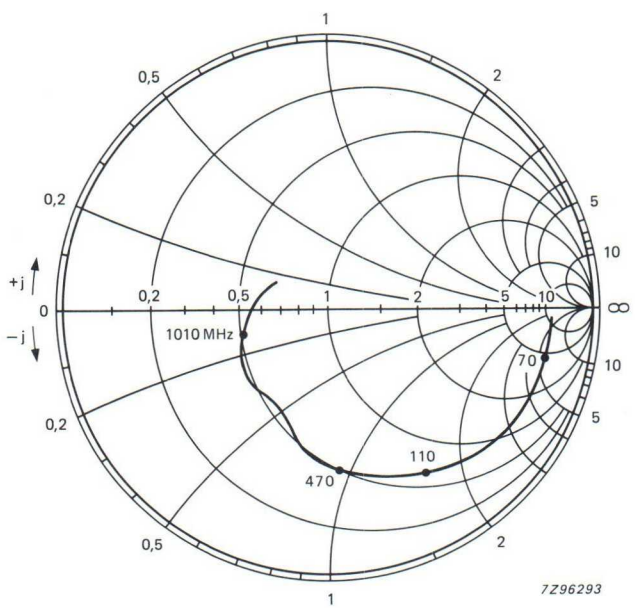


Fig. 5 Smith chart of typical input impedance: $V_{i(rms)}$ = 25 mV; V_{CC} = 5 V; reference value = 50 Ω.

SENSITIVE 2.6 GHz DIVIDE-BY-2 PRESCALER

GENERAL DESCRIPTION

The SAB8726 is a prescaler for satellite television applications. It has an input frequency range of 1 GHz to 2.6 GHz with high input sensitivity.

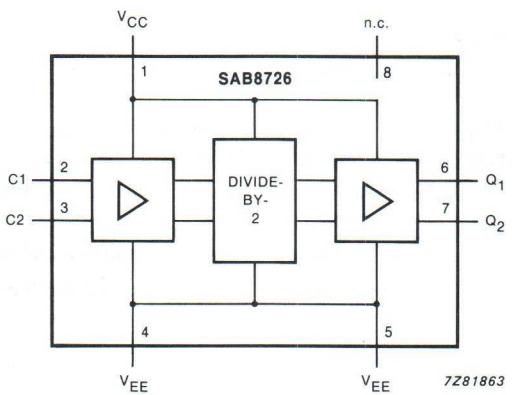


Fig. 1 Block diagram.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 1 to pins 4, 5	V_{CC}	4.5	5.0	5.5	V
Supply current	pin 1	I_{CC}	–	35	–	mA
Input frequency range	pins 2 and 3	f_i	1	–	2.6	GHz
Input sensitivity						
Input voltage (RMS value)		$V_{i(rms)}$	–	–	70	dBm/mV
Output voltage (RMS value)	pins 6 and 7	$V_{o(rms)}$	–	90	–	dBm/mV
Operating ambient temperature range		T_{amb}	0	–	80	°C

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

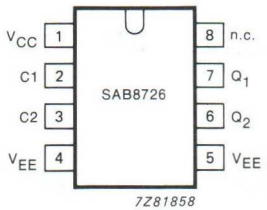


Fig. 2 Pinning diagram.

PINNING

1	V_{CC}	positive supply voltage
2	C1	differential inputs
3	C2	
4	V_{EE}	ground (0 V)
5	V_{EE}	ground (0 V)
6	Q_1	complementary outputs
7	Q_2	
8	n.c.	not connected

FUNCTIONAL DESCRIPTION

This IC is designed to be driven by a sinusoidal 1 GHz to 2.6 GHz signal from the local-oscillator of a satellite TV tuner.

The inputs (C1, C2) are differential and are internally biased to permit capacitive coupling (Fig. 5a). When driven asymmetrically the unused input should be connected to ground via a capacitor (Fig. 5b).

The divider stage will oscillate without an input signal but this oscillation will be suppressed when an input signal within the specified range is applied.

Two complementary signals (Q_1, Q_2) are provided by the output differantial amplifier stage (Fig. 5c).

For asymmetrical output, the unused output should be connected to ground via a 50 Ω resistor and a capacitor (Fig. 5d).

ELECTROSTATIC DISCHARGE PROTECTION

Inputs and outputs have electrostatic discharge protection in accordance with specification MIL-STD-883C, class A.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (DC)	V_{CC}	–	7.0	V
Input voltage	V_i	0	V_{CC}	V
Storage temperature range	T_{stg}	–55	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 80	°C
Junction temperature	T_j	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 120 K/W

DC CHARACTERISTICS

V_{CC} = 5 V ± 10%; V_{EE} = 0 V; T_{amb} = 0 to 80 °C; test IC mounted in a test socket or on a printed circuit board; measurements taken after thermal equilibrium is established; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply current		I_{CC}	–	35	45	mA
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW		V_{OL}	–	–	V_{CC}–0.4	V

DEVELOPMENT DATA

AC CHARACTERISTICS

V_{CC} = 5 V ± 10%; T_{amb} = 0 to + 80 °C; f_{in} = 1 to 2.6 GHz; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Input						
Input frequency range		f_i	1	–	2.6	GHz
Input sensitivity						
Input voltage (RMS value)	50 Ω system					
	f_i = 1 GHz	$V_{i(rms)}$	–	–	–10/70	dBm/mV
	f_i = 2.6 GHz	$V_{i(rms)}$	–	–	–10/70	dBm/mV
Input overload voltage (RMS value)	50 Ω system					
	f_i = 1 GHz	$V_{i(rms)}$	7/500	–	–	dBm/mV
	f_i = 2.6 GHz	$V_{i(rms)}$	7/500	–	–	dBm/mV
Output						
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW		V_{OL}	–	–	V_{CC}–0.4	V
Output voltage level	V_i = 0 dBm; f_i = 2 GHz; R_L = 50 Ω	V_o	–	–8/90	–	dBm/mV
Output resistance		R_o	–	50	–	Ω

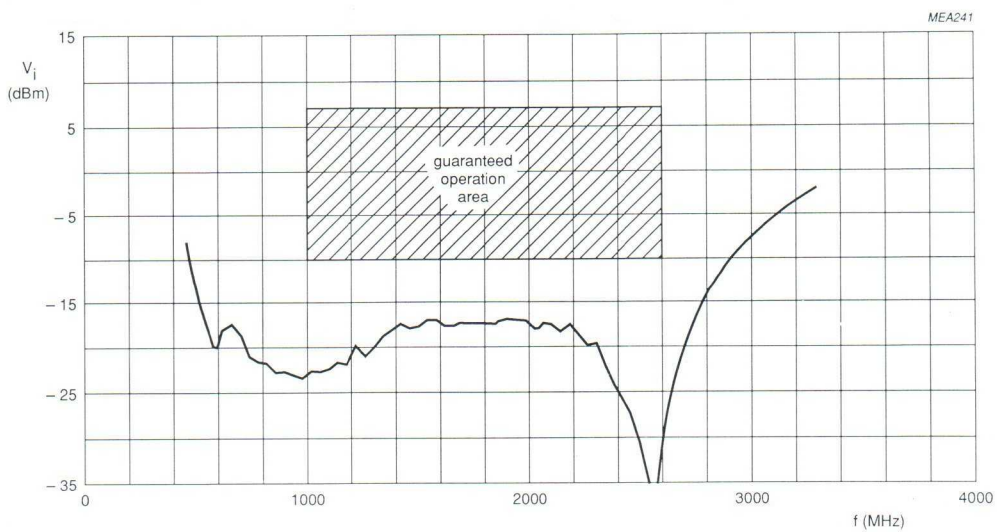


Fig.3 Typical input sensitivity curve: V_{CC} = 5 V; T_{amb} = 25 °C.

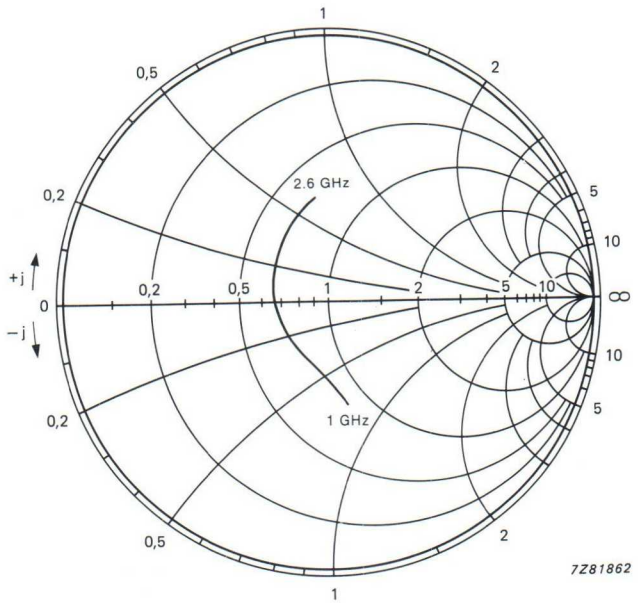
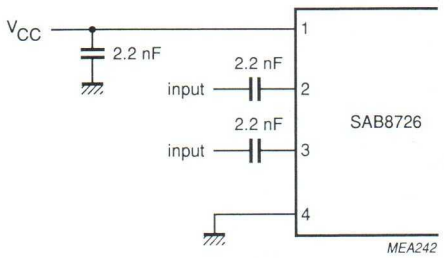


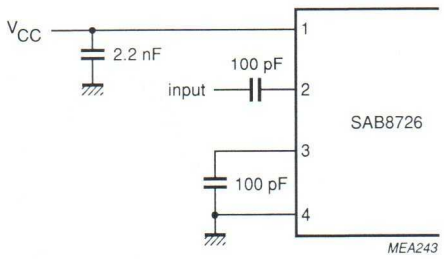
Fig. 4 Smith chart of typical input impedance: input level = −10 dBm; V_{CC} = 5 V; reference value = 50 Ω.

DEVELOPMENT DATA

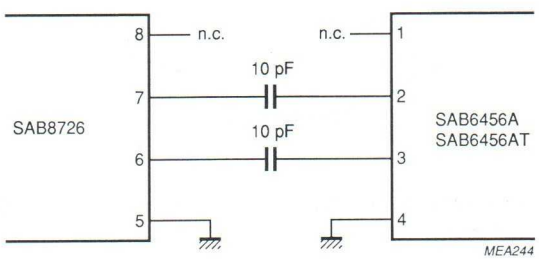
APPLICATION INFORMATION



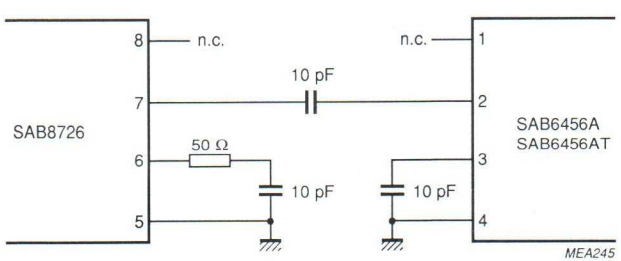
(a) Symmetrical input.



(b) Asymmetrical input.



(c) Symmetrical output.



(d) Asymmetrical output.

Fig. 5 Pin configurations for symmetrical/asymmetrical input and output.

Note to Fig. 5

To minimize possible harmonics the symmetrical output is preferred.

Picture-in-Picture (PIP) controller for NTSC SAB9075H

FEATURES

Display

- One or two live pictures can be displayed simultaneously
- Wide range of multi-Picture-In-Picture (PIP) modes available
- Six 6-bit Analog-to-Digital Converters (ADC) with clamping circuit
- Enhanced vertical resolution at most modes for live pictures
- Two Phase-Locked-Loops (PLL) with Voltage Controlled Oscillator (VCO) to generate the line-locked clocks
- Three 7-bit Digital-to-Analog Converters (DAC)
- 4 : 1 : 1 data format
- Data reduction factors 1 to 4, 1 to 9 and 1 to 16.

I²C-bus programmable

- Different single, double and multi-PIP modes can be set
- Several aspect ratios can be handled
- Reduction factors can be set automatically and manually
- Selection of vertical filtering type
- Freeze of live pictures
- Single-PIP display position, four corners on-screen
- Multi-PIP display position, left or right on-screen
- Fine tuned display position, H (6-bit), V (6-bit)
- Fine tuned acquisition area, H (4-bit), V (4-bit)
- Channel-border and live PIP selectable
- Eight main-border, sub-border, channel-border and background colours selectable
- Border and background brightness adjustable, 30%, 50%, 70% and 100% IRE
- Several types of decoder input signals can be set
- 6-bit HUE and SAT signals (0 to 5 V) adjustable by I²C-bus
- Main and sub-audio mute controllable by I²C-bus.

GENERAL DESCRIPTION

The SAB9075H is a picture-in-picture controller for the NTSC environment in combination with the Integrated NTSC decoder and sync processor TDA8315.

The device inserts one or two live video channels with reduced sizes into a live video signal. All video signals are expected to be analog baseband signals. The conversion into the digital environment and back to the analog environment is carried out on-chip. Internal clocks are generated by two PLLs.

Due to the two PIP channels and a large external memory, a wide range of PIP modes are offered. The emphasis is put on double-PIP and multi-PIP modes. In combination with the different border colours and some external software the IC concept can be used as an excellent channel selection tool.

Some of the I²C-bus registers are for controlling the saturation and HUE of the colours. There are also outputs for the mute function of main and sub-channel.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAB9075H	QFP100[1]	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	all positive supply pins	4.5	5.0	5.5	V
I_{tot}	total supply current	note 1	tbf	220	tbf	mA
f_{sys}	system frequency	note 2	–	27	30	MHz
f_{loop}	loop bandwidth frequency		4	–	–	kHz
t_{jitter}	short term stability time	jitter during 1 line (64 µs)	–	–	4	ns
ς	damping factor		–	0.7	–	–

Notes

1. Digital clocks are silent and analog bias current is zero.
2. The internal system frequencies are 1728 times the input frequency. For more detailed information about the clock generation see Section "PLLs and clock generation".

BLOCK DIAGRAM

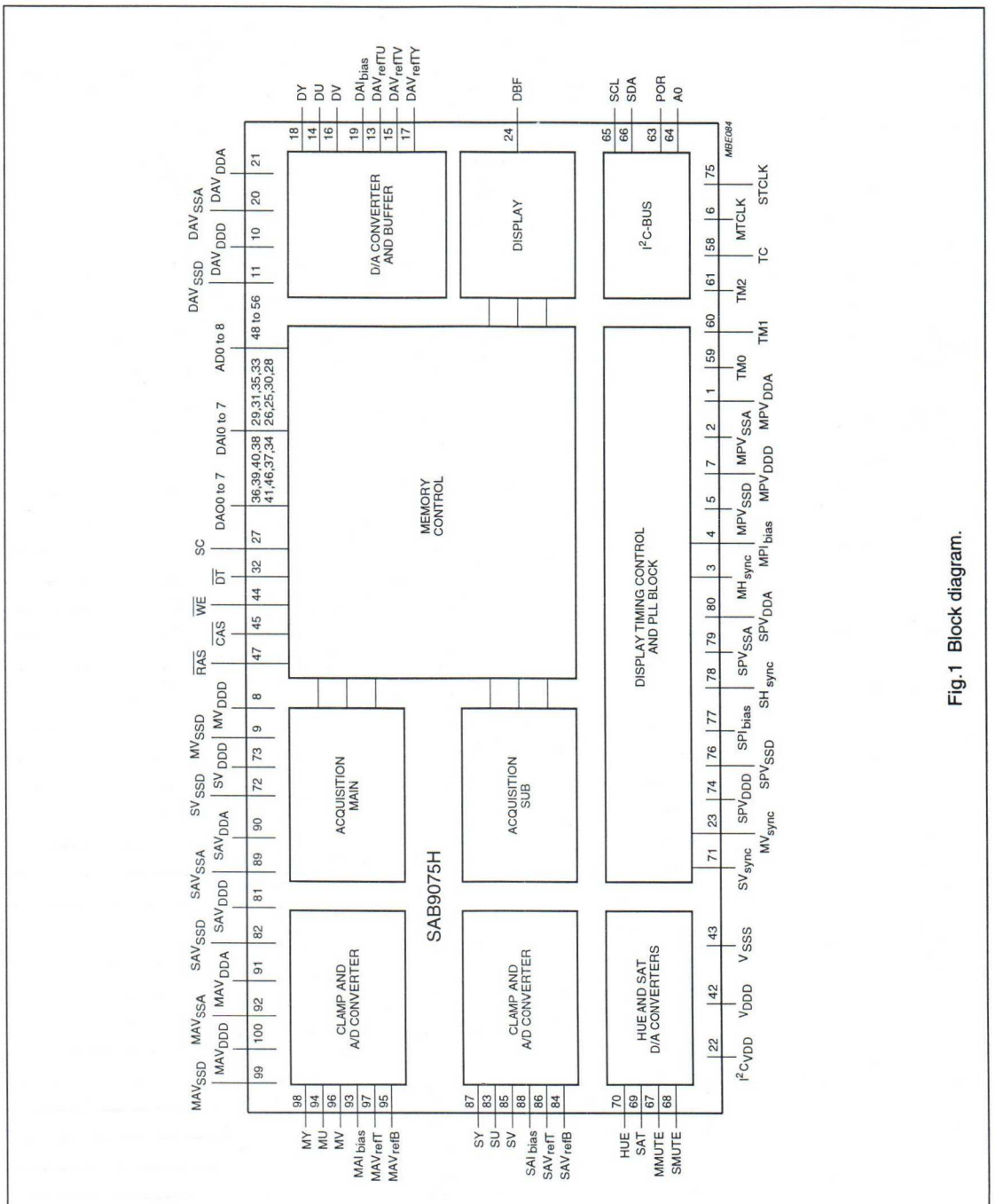


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
MPV_{DDA}	1	I/O	E030	analog positive power supply for PLL main-channel
MPV_{SSA}	2	I/O	E009	analog negative power supply for PLL main-channel
MH_{sync}	3	I	E027	horizontal synchronization for main-channel
MPI_{bias}	4	I	E027	analog bias reference current for PLL main-channel
MPV_{SSD}	5	I/O	E009	digital negative power supply for PLL main-channel
MTCLK	6	I	HPP01	test clock for main-channel
MPV_{DDD}	7	I/O	E030	digital positive power supply for PLL main-channel
MV_{DDD}	8	I/O	E030	digital positive power supply for main-channel core
MV_{SSD}	9	I/O	E009	digital negative power supply for main-channel core
DAV_{DDD}	10	I/O	E030	digital positive power supply for DACs
DAV_{SSD}	11	I/O	E009	digital negative power supply for DACs
n.c.	12	–	–	not connected
DAV_{refTU}	13	I/O	E027	analog reference voltage for top U DAC
DU	14	O	E027	analog U output
DAV_{refTV}	15	I/O	E027	analog reference voltage for top V DAC
DV	16	O	E027	analog V output
DAV_{refTY}	17	I/O	E027	analog reference voltage for top Y DAC
DY	18	O	E027	analog Y output
DAI_{bias}	19	I	E027	analog bias reference current for DACs
DAV_{SSA}	20	I/O	E009	analog negative power supply for DACs
DAV_{DDA}	21	I/O	E030	analog positive power supply for DACs
I^2CV_{DD}	22	I/O	E030	positive supply for HUE and SAT decoders
MV_{sync}	23	I	HPP01	vertical synchronization for main-channel
DBF	24	O	SPF20	fast blanking control output signal
DAI5	25	I	HPP01	data bus input from memory; bit 5
DAI4	26	I	HPP01	data bus input from memory; bit 4
SC	27	O	OPF20	memory shift clock
DAI7	28	I	HPP01	data bus input from memory; bit 7
DAI0	29	I	HPP01	data bus input from memory; bit 0
DAI6	30	I	HPP01	data bus input from memory; bit 6
DAI1	31	I	HPP01	data bus input from memory; bit 1
$\overline{DT}$	32	O	OPF20	memory data transfer; active LOW
DAI3	33	I	HPP01	data bus input from memory; bit 3
DAO7	34	O	OPF20	data bus output to memory; bit 7
DAI2	35	I	HPP01	data bus input from memory; bit 2
DAO0	36	O	OPF20	data bus output to memory; bit 0
DAO6	37	O	OPF20	data bus output to memory; bit 6
DAO3	38	O	OPF20	data bus output to memory; bit 3
DAO1	39	O	OPF20	data bus output to memory; bit 1
DAO2	40	O	OPF20	data bus output to memory; bit 2

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
DAO4	41	O	OPF20	data bus output to memory; bit 4
V_{DDD}	42	I/O	E030	digital positive power supply for peripherals
V_{SSS}	43	I/O	E009	digital negative power supply for peripherals
$\overline{WE}$	44	O	OPF20	memory write enable; active LOW
$\overline{CAS}$	45	O	OPF20	memory column address strobe; active LOW
DAO5	46	O	OPF20	data bus output to memory; bit 5
$\overline{RAS}$	47	O	OPF20	memory row address strobe; active LOW
AD0	48	O	OPF20	memory address bus; bit 0
AD8	49	O	OPF20	memory address bus; bit 8
AD1	50	O	OPF20	memory address bus; bit 1
AD6	51	O	OPF20	memory address bus; bit 6
AD2	52	O	OPF20	memory address bus; bit 2
AD5	53	O	OPF20	memory address bus; bit 5
AD3	54	O	OPF20	memory address bus; bit 3
AD4	55	O	OPF20	memory address bus; bit 4
AD7	56	O	OPF20	memory address bus; bit 7
n.c.	57	–	–	not connected
TC	58	I	HPP01	test control
TM0	59	I	HPP01	test mode 0
TM1	60	I	HPP01	test mode 1
TM2	61	I	HPP01	test mode 2
n.c.	62	–	–	not connected
POR	63	I	HUP07	power-on reset
A0	64	I	HPF01	I^2C-bus address 0 selection pin
SCL	65	I	HPF01	shift clock for I^2C-bus
SDA	66	I/O	IOI41	shift I^2C-bus input data; acknowledge I^2C-bus output data
MMUTE	67	O	SPF20	mute output for main-channel
SMUTE	68	O	SPF20	mute output for sub-channel
SAT	69	O	E027	analog output for SAT decoder
HUE	70	O	E027	analog output for HUE decoder
SV_{sync}	71	I	HPP01	vertical synchronization for sub-channel
SV_{SSD}	72	I/O	E009	digital negative power supply for sub-channel core
SV_{DDD}	73	I/O	E030	digital positive power supply for sub-channel core
SPV_{DDD}	74	I/O	E030	digital positive power supply for PLL sub-channel
STCLK	75	I	HPP01	test clock for sub-channel
SPV_{SSD}	76	I/O	E009	digital negative power supply for PLL sub-channel
SPI_{bias}	77	I	E027	analog bias reference current for PLL sub-channel
SH_{sync}	78	I	E027	horizontal synchronization for sub-channel
SPV_{SSA}	79	I/O	E009	analog negative power supply for PLL sub-channel
SPV_{DDA}	80	I/O	E030	analog positive power supply for PLL sub-channel
SAV_{DDD}	81	I/O	E030	digital positive power supply for ADC sub-channel

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
SAV_{SSD}	82	I/O	E009	digital negative power supply for ADC sub-channel
SU	83	I	E027	analog U input for sub-channel
SAV_{refB}	84	I/O	E027	analog reference voltage for bottom ADC sub-channel
SV	85	I	E027	analog V input for sub-channel
SAV_{refT}	86	I/O	E027	analog reference voltage for top ADC sub-channel
SY	87	I	E027	analog Y input for sub-channel
SAI_{bias}	88	I	E027	analog bias reference current for ADC sub-channel
SAV_{SSA}	89	I/O	E009	analog negative power supply for ADC sub-channel
SAV_{DDA}	90	I/O	E030	analog positive power supply for ADC sub-channel
MAV_{DDA}	91	I/O	E030	analog positive power supply for ADC main-channel
MAV_{SSA}	92	I/O	E009	analog negative power supply for ADC main-channel
MAI_{bias}	93	I	E027	analog bias reference current for ADC main-channel
MU	94	I	E027	analog U input for main-channel
MAV_{refB}	95	I/O	E027	analog reference voltage for bottom ADC main-channel
MV	96	I	E027	analog V input for main-channel
MAV_{refT}	97	I/O	E027	analog reference voltage for top ADC main-channel
MY	98	I	E027	analog Y input for main-channel
MAV_{SSD}	99	I/O	E009	digital negative power supply for ADC main-channel
MAV_{DDD}	100	I/O	E030	digital positive power supply for ADC main-channel

Table 1 Pin type explanation

PIN TYPE	DESCRIPTION
E030	V_{DD} pin; diode to V_{SS}
E009	V_{SS} pin; diode to V_{DD}
E027	analog input pin; diode to V_{DD} and V_{SS}
HPF01	digital input pin; CMOS levels, diode to V_{SS}
HPP01	digital input pin; CMOS levels, diode to V_{DD} and V_{SS}
HUP07	digital input pin; CMOS levels with hysteresis, pull up resistor to V_{DD}, diode to V_{DD} and V_{SS}
IOI41	I^2C-bus pull-down output stage; CMOS input levels
OPF20	digital output pin
SPF20	digital output pin; slew rate controlled

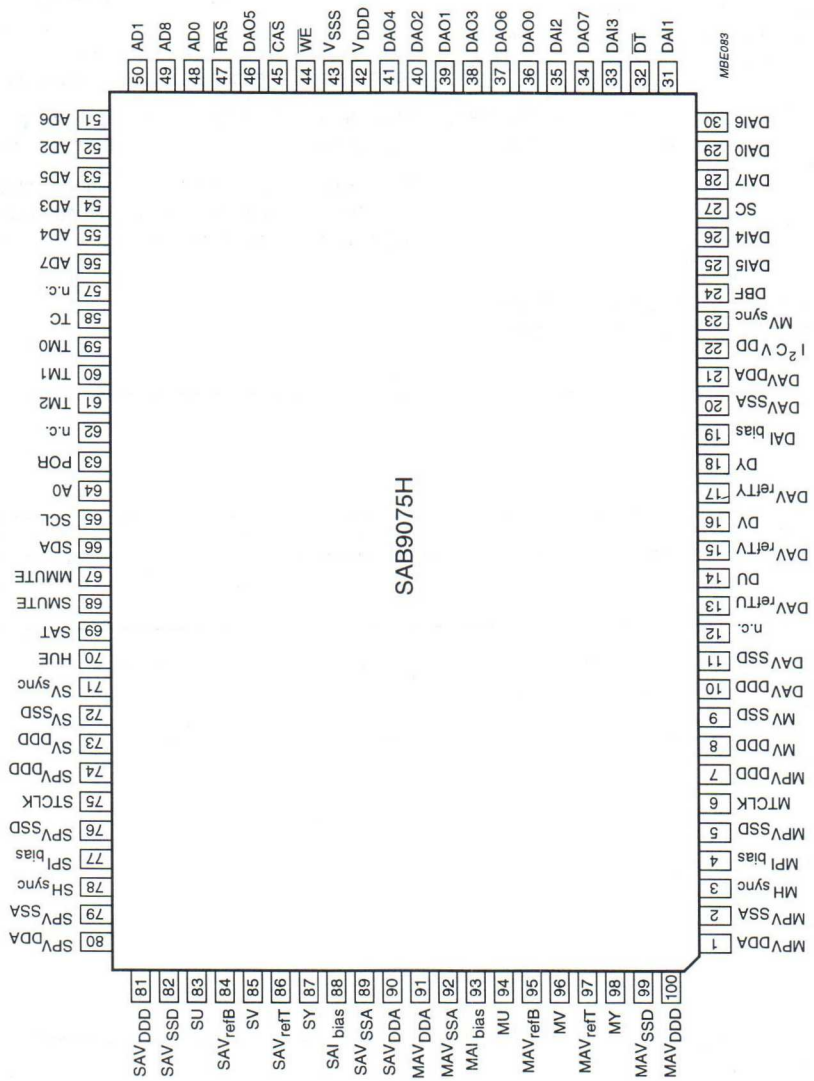


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Acquisition area

The acquisition area is in the centre of the visible screen area. Vertically 228 lines are sampled. Horizontally 672 Y-pixels are processed. The exact active processing area can be fine tuned in horizontal (2 pixels/steps, 16 steps) and vertical (1 line/step, 16 steps) direction for both main and sub-channel by the I²C-bus (see Fig.3). The given numbers are pixel numbers at a 13.5 MHz data rate. The signals, which are dependent on the I²C-bus registers, can also be related to the H_{sync}, in which event they are delayed by 68 pixels.

Chrominance format

The chrominance format is 4 : 1 : 1.

The YUV signals are sampled at a rate of 27 MHz and then filtered and subsampled to a data rate of 13.5 MHz.

It is expected that the input signals do not contain frequencies outside the video bandwidth (Y_{BW} = 4.5 MHz; U_{BW} and V_{BW} = 1.125 MHz).

Display area

The display area is shown in Fig.4. The given numbers are pixels at a data rate of 13.5 MHz. The signals are related to the burstkey and the V_{sync}. Dependent on the I²C-bus registers the signals can also be related to the H_{sync}.

The internal 13.5 MHz data rate is upsampled to the double frequency (27 MHz) and then fed to the DACs.

The display output can be fine positioned by the I²C-bus in 64 steps of 4 pixels in horizontal direction and 64 steps of 1 line/field in vertical direction.

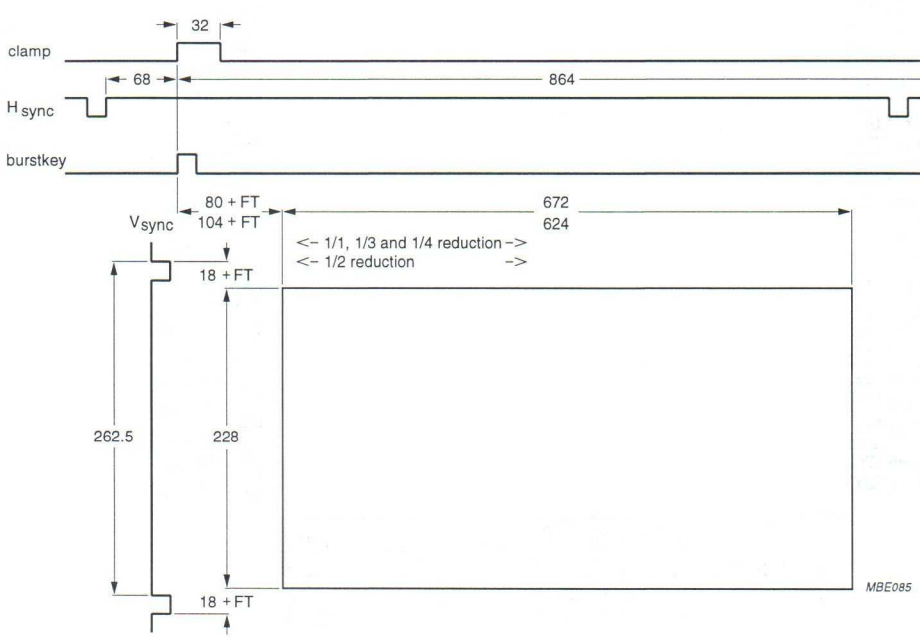


Fig.3 Acquisition area.

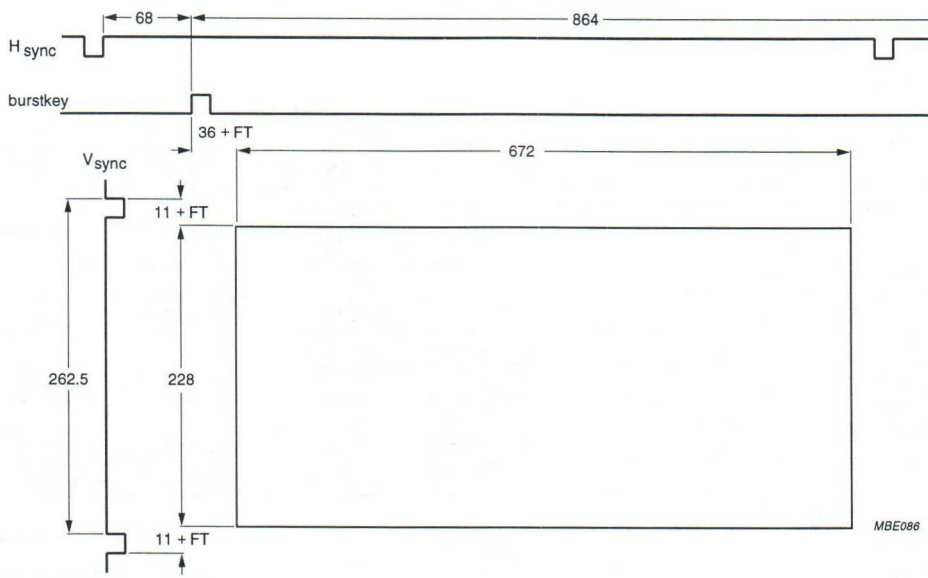


Fig.4 Display area.

PIP modes

The controller contains two independent acquisition-channels which provide the scaling factors to support the range of different modes. With the external memory of 2 Mbit it is possible to select between single, double and multi-PIP modes.

Table 2 gives an overview of the different PIP modes.

Table 2 PIP modes

MODE		SUB	MAIN	SUB SIZE[1]		MAIN SIZE[1]	
				PIXELS	REDUCTION[2]	PIXELS	REDUCTION[2]
4 : 3 main + 4 : 3 sub to 4 : 3 screen or 16 : 9 main + 16 : 9 sub to 16 : 9 screen							
1.1	SPS	1/16	–	160P, 53L	1/4H, 1/4V	–	–
1.2	SPL	1/9	–	216P, 72L	1/3H, 1/3V	–	–
1.3	DP	1/4	1/4	304P, 108L	1/2H, 1/2V	304P, 108L	1/2H, 1/2V
1.4	MP3	3 × 1/16	–	160P, 53L	1/4H, 1/4V	–	–
1.5	MP4	3 × 1/16	1/4	160P, 53L	1/4H, 1/4V	304P, 108L	1/2H, 1/2V
1.6	MP7	7 × 1/16	–	160P, 53L	1/4H, 1/4V	–	–
1.7	MP8	7 × 1/16	1/4	160P, 53L	1/4H, 1/4V	304P, 108L	1/2H, 1/2V
1.8	MP9	8 × 1/9	1/9	216P, 72L	1/3H, 1/3V	216P, 72L	1/3H, 1/3V
16 : 9 sub + 4 : 3 main to 4 : 3 screen							
2.1	SPS	1/16	–	216P, 53L	1/3H, 1/4V	–	–
2.2	SPL	1/9	–	304P, 72L	1/2H, 1/3V	–	–
4 : 3 sub + 16 : 9 main to 16 : 9 screen							
3.1	SPS	1/16	–	160P, 72L	1/4H, 1/3V		
3.2	DP	1/4	1/4	216P, 108L	1/3H, 1/2V	304P, 108L	1/2H, 1/2V

Notes

1. The given sub/main sizes are visible PIP sizes, a border is drawn around these PIPs and does not influence these sizes. The size of the border is 4 pixels wide and 2 lines/fields high.
2. The SAB9075H can be set in automatic mode in which the reduction factors are automatically set by the mode select and aspect ratio select bits of the I²C-bus. If the automatic mode is switched OFF the reduction factors can be set manually. This will give more flexibility to adjust the aspect ratios of incoming signals.

PIP positions

The positions are graphically depicted in Figs 5 to 17.

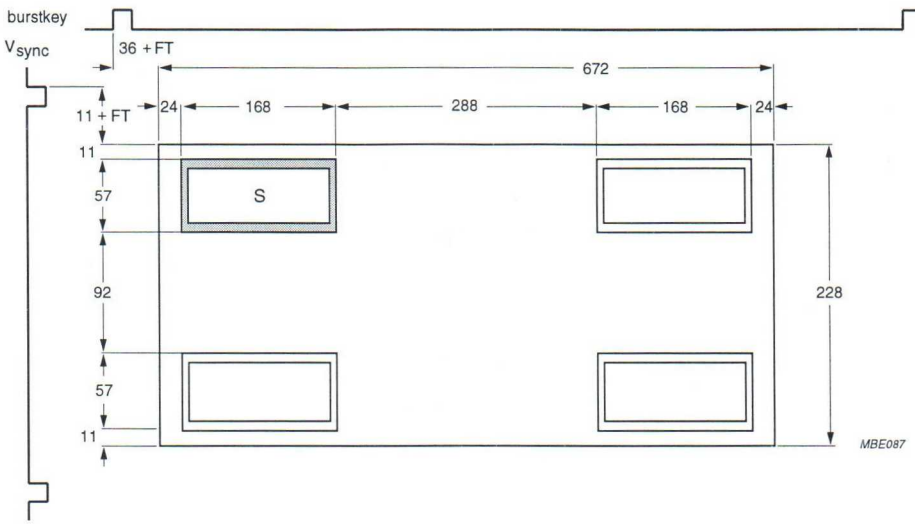


Fig.5 Single-PIP, size $1/16$ (mode SPS).

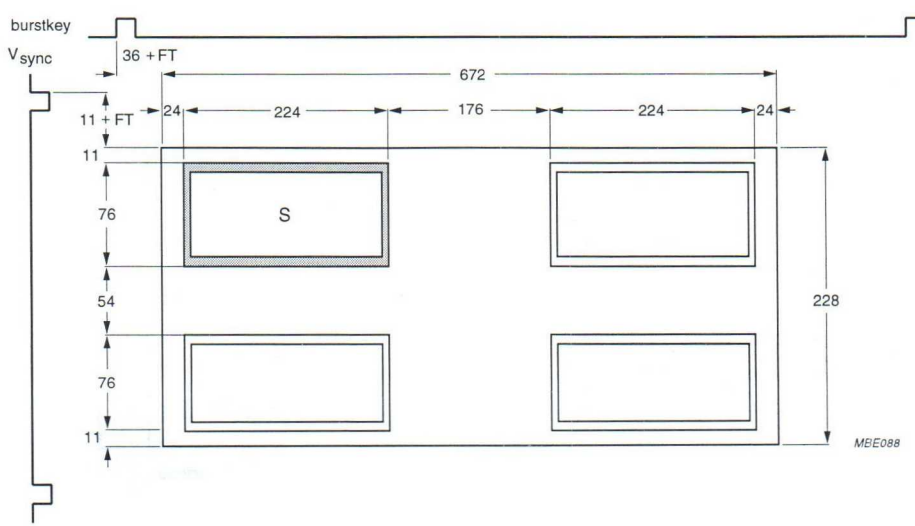


Fig.6 Single-PIP, size $1/9$ (mode SPL).

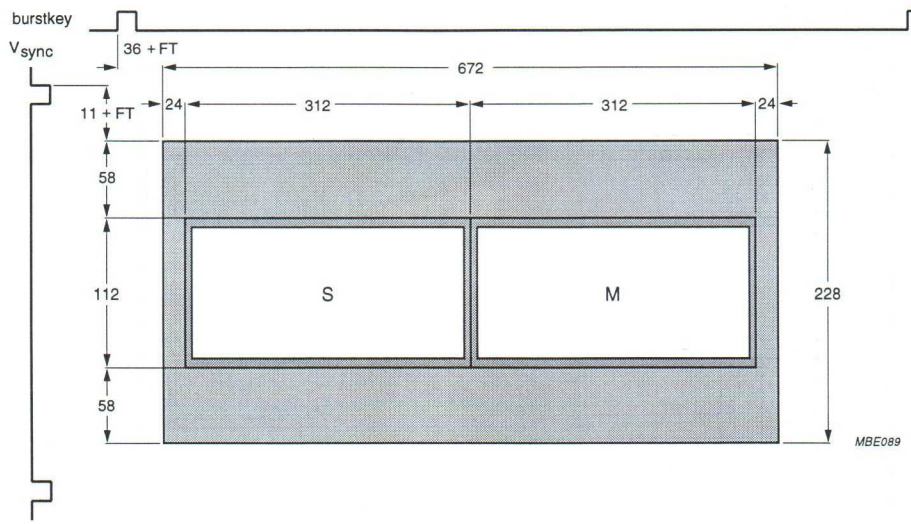


Fig.7 Double-PIP, size $1/16$ (mode DP).

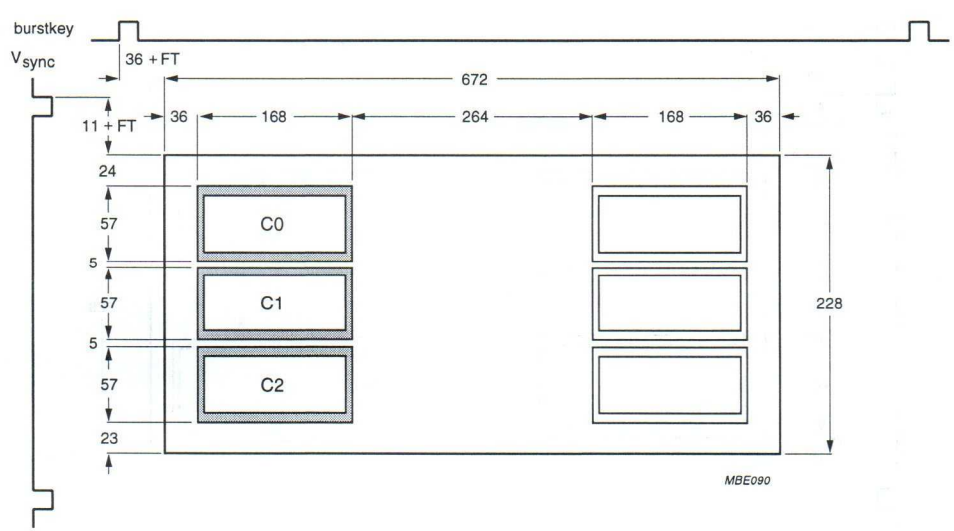


Fig.8 Multi PIP, 3 × sub $1/16$ (mode MP3).

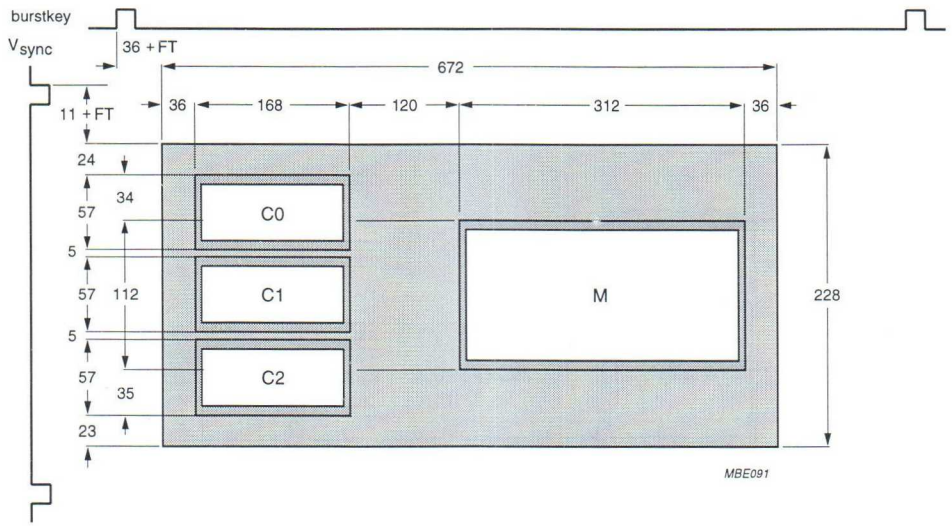


Fig.9 Multi-PIP, 3 × sub 1/16, 1 × main 1/4 (mode MP4).

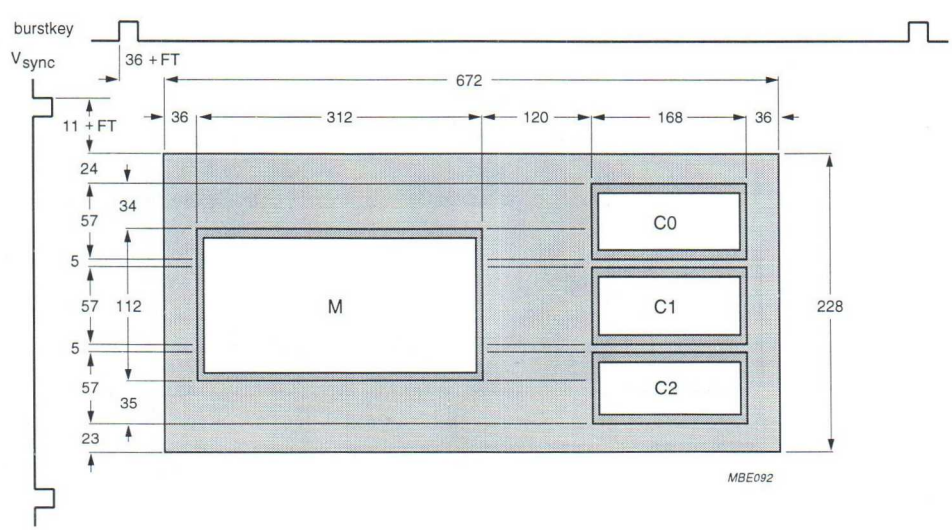


Fig.10 Multi-PIP, 3 × sub 1/16, 1 × main 1/4 (mode MP4, Right).

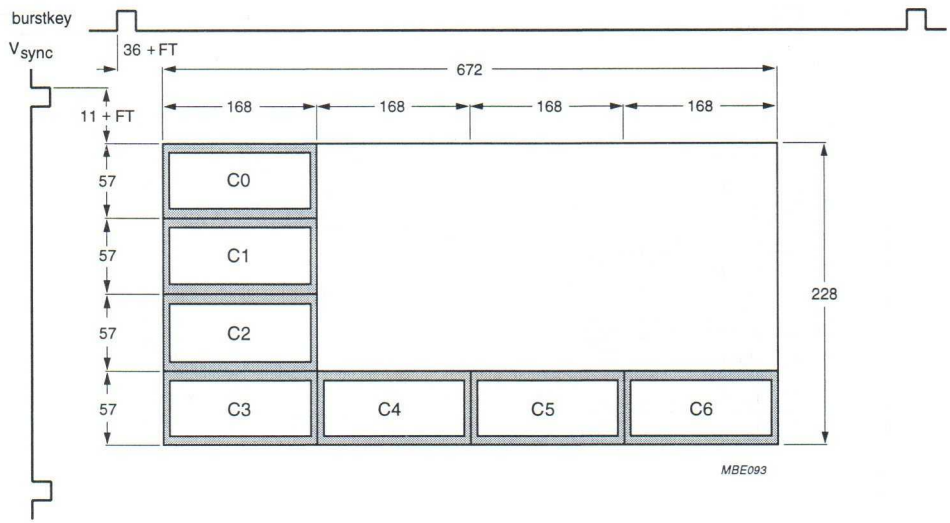


Fig.11 Multi-PIP, 7 × sub 1/16, main life (mode MP7).

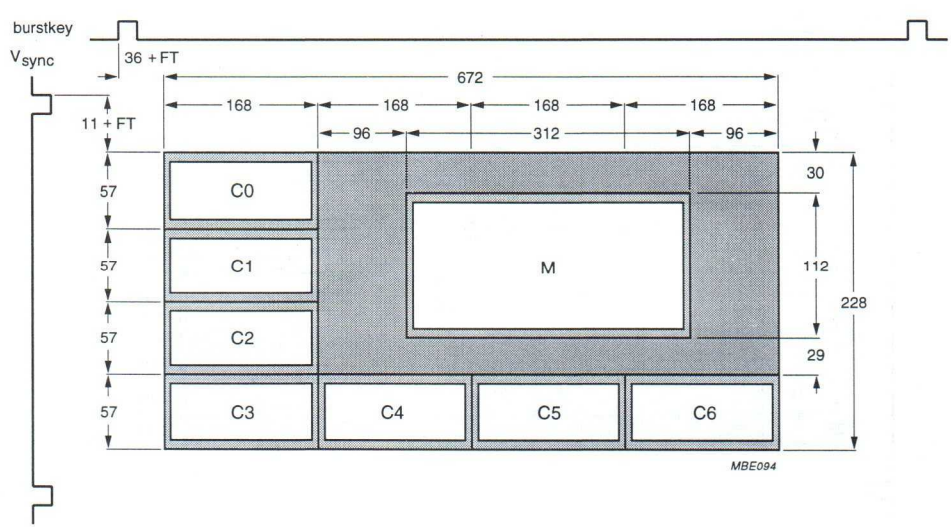


Fig.12 Multi-PIP, 7 × sub 1/16, 1 × main 1/4 (mode MP8).

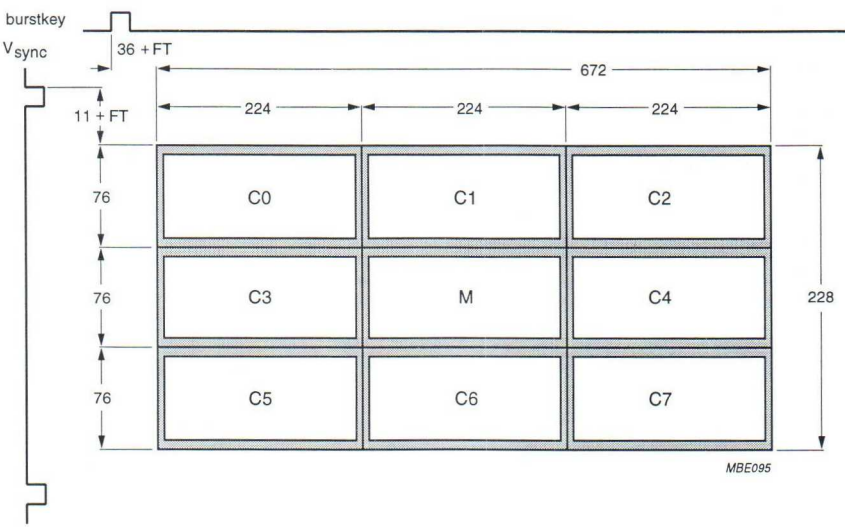


Fig.13 Multi-PIP, 8 × sub 1/9, 1 × main 1/9 (mode MP9).

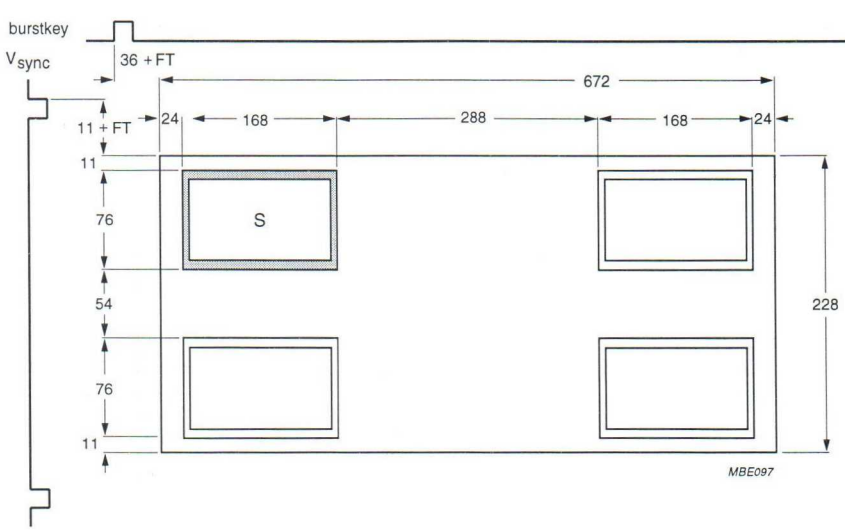


Fig.14 Single-PIP, 4 : 3 sub to 16 : 9 screen (mode SPS).

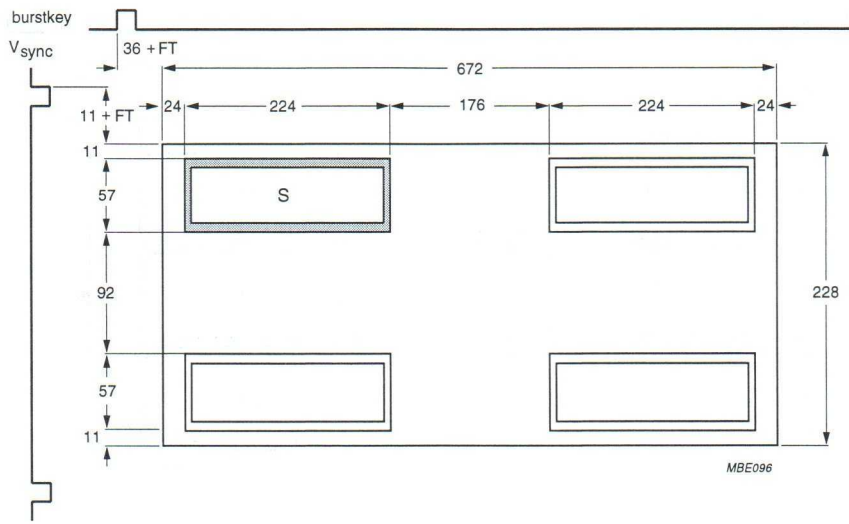


Fig.15 Single-PIP, 16 : 9 sub to 4 : 3 screen (mode SPS).

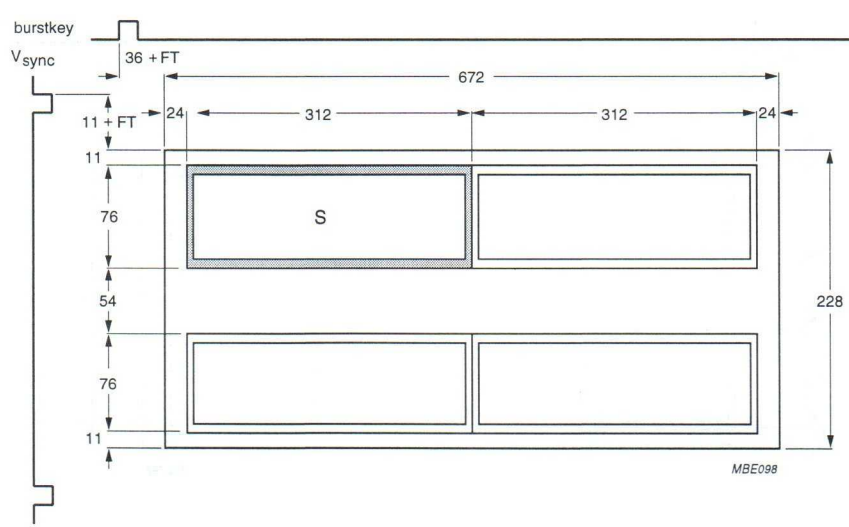


Fig.16 Single-PIP, 16 : 9 sub to 4 : 3 screen (mode SPL).

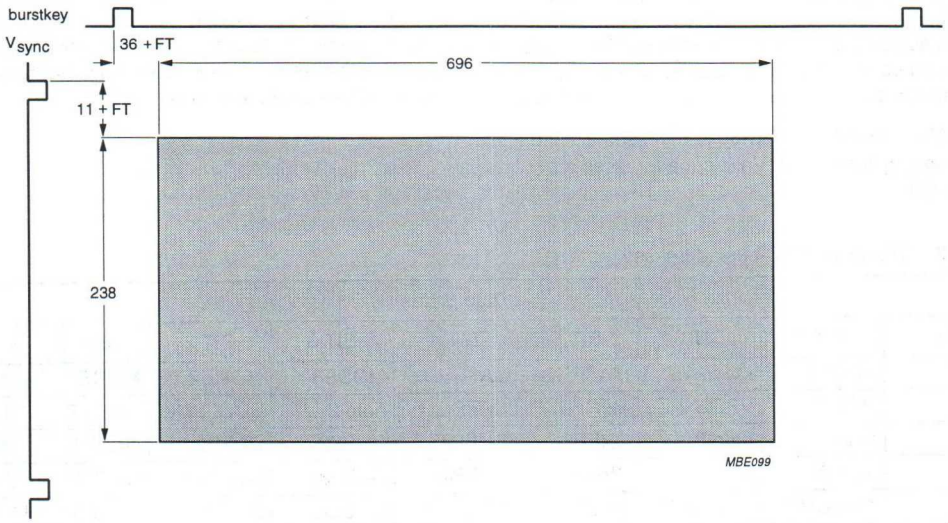


Fig.17 Factory mode.

I²C-bus

The I²C-bus provides bi-directional 2-line communication between different ICs. The SDA line is the Serial Data line and the SCL serves as Serial Clock Line. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

The SAB9075H has the I²C-bus addresses 2C and 2E, switchable by the pin A0. Valid subaddresses are 00H to 0FH.

I²C-bus control is in accordance with the I²C-bus protocol.

First a start sequence must be put on the I²C-bus, then the I²C-bus address 2C or 2E, followed by a subaddress 00 to 0F. After this sequence, the data of the subaddress must be sent. An auto-increment function then gives the option 'send data' of the incremented subaddresses until a stop sequence has been given.

Table 3 Overview of I²C-bus addresses (note 1)

	Data Bytes							
SA	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
00	PIPON	MANRED	MASPECT	SASPECT	MODE3	MODE2	MODE1	MODE0
01	HPOS	VPOS	MFREEZE	SFREEZE	note 2	BCOLPOL	MVFILT	SVFILT
02	note 2	note 2	DHFP5	DHFP4	DHFP3	DHFP2	DHFP1	DHFP0
03	note 2	note 2	DVFP5	DVFP4	DVFP3	DVFP2	DVFP1	DVFP0
04	MREDH1	MREDH0	MREDV1	MREDV0	SREDH1	SREDH0	SREDV1	SREDV0
05	note 2	CBSEL2	CBSEL1	CBSEL0	note 2	SLSEL2	SLSEL1	SLSEL0
06	note 2	MBON	MBBRT1	MBBRT0	note 2	MBCOL2	MBCOL1	MBCOL0
07	note 2	SBON	SBBRT1	SBBRT0	note 2	SBCOL2	SBCOL1	SBCOL0
08	note 2	CBON	CBBRT1	CBBRT0	note 2	CBCOL2	CBCOL1	CBCOL0
09	FACMODE	BGON	BGBRT1	BGBRT0	note 2	BGCOL2	BGCOL1	BGCOL0
0A	MCOLPOL	MVSPOL	MHSYNC	MFPOL	SCOLPOL	SVSPOL	SHSYNC	SFPOL
0B	MAAHFP3	MAAHFP3	MAAHFP3	MAAHFP3	MAAVFP3	MAAVFP3	MAAVFP3	MAAVFP3
0C	SAAHFP3	SAAHFP3	SAAHFP3	SAAHFP3	SAAVFP3	SAAVFP3	SAAVFP3	SAAVFP3
0D	note 2	note 2	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0
0E	note 2	note 2	SAT5	SAT4	SAT3	SAT2	SAT1	SAT0
0F	MMUTE	SMUTE	note 2	note 2	note 2	note 2	note 2	note 2

Notes

1. Table 3 gives an overview of the I²C-bus addresses. They will be explained in more detail in the following pages.
2. Some address spaces are unused but already implemented for future functionality.

Table 4 PIP mode control (note 1)

PIP MODE		ASPECT RATIO		MAIN-REDUCTION(2)		SUB-REDUCTION(2)	
NAME	MODE(3)	MAIN(4)	SUB(4)	HOR	VER	HOR	VER
SPS	0000	0	0	–	–	1/4	1/4
SPS	0000	0	1	–	–	1/3	1/4
SPS	0000	1	0	–	–	1/4	1/3
SPS	0000	1	1	–	–	1/4	1/4
SPL	0001	0	0	–	–	1/3	1/3
SPL	0001	0	1	–	–	1/2	1/3
SPL	0001	1	X	–	–	1/3	1/3
DP	1010	0	X	1/2	1/2	1/2	1/2
DP	1010	1	0	1/2	1/2	1/3	1/2
DP	1010	1	1	1/2	1/2	1/2	1/2
MP3	0110	X	X	–	–	1/4	1/4
MP4	1110	X	X	1/2	1/2	1/4	1/4
MP7	0100	X	X	–	–	1/4	1/4
MP8	1100	X	X	1/2	1/2	1/4	1/4
MP9	1001	X	X	1/3	1/3	1/3	1/3

Notes

1. Table 4 gives an overview of the possible PIP modes and how to set them via the I²C-bus.
2. The columns main and sub-reduction indicate how the PIP pictures appear on the screen.
3. The column mode corresponds to the lower 4 bits of I²C-bus Register 0.
4. The main and sub-aspect ratios correspond to the bits 5 and 6 of I²C-bus Register 0.

Table 5 Register 0; PIP mode control register

BIT	MODE	RESULT
7	PIPON	logic 0 = PIP function is OFF[1]; logic 1 = PIP function is ON
6	MANRED	logic 0 = automatic reduction factors[2]; logic 1 = manual reduction factors[3]
5	MASPECT[4]	main-aspect ratio; 0 = 4 : 3; 1 = 16 : 9
4	SASPECT[4]	sub-aspect ratio; 0 = 4 : 3; 1 = 16 : 9
3	MODE(3)[5]	PIP mode
2	MODE(2)[5]	PIP mode
1	MODE(1)[5]	PIP mode
0	MODE(0)[5]	PIP mode

Notes

1. With PIPON in OFF mode the fast blanking signal is made inactive. All other functions will operate as if the circuit were in operational mode.
2. With MANRED set to logic 0 the reduction factors will be set automatically, dependent on the PIP mode and the aspect ratio bits of main and sub (bits 5 and 4). Table 4 indicates which bits should be set to obtain a certain PIP mode.
3. With MANRED set to logic 1 the calculation of the reduction factors is not carried out and should be set by Register 4 (see Table 9). Only combinations with MANRED set to logic 0 are guaranteed.
4. MASPECT and SASPECT are used in automatic mode (MANRED) to indicate the type of input signals, together with MODE the PIP mode can be set (see Table 4). In manual mode these bits are ignored.
5. The MODE bits set the PIP mode. For the multi-PIP modes the frozen PIPs are set to the 30% grey colour. Once a PIP has been made live it will always display the last video data.

Table 6 Register 1; general control register

BIT	MODE	RESULT
7	HPOS[1]	logic 0 = left; logic 1 = right
6	VPOS[1]	logic 0 = top; logic 1 = bottom
5	MFREEZE[2]	logic 0 = main-freeze is OFF; logic 1 = main-freeze is ON
4	SFREEZE[2]	logic 0 = sub-freeze is OFF; logic 1 = sub-freeze is ON
3	–	not used
2	BCOLPOL[3]	border UV polarity; logic 0 = +(B–Y), +(R–Y); logic 1 = –(B–Y), –(R–Y)
1	MVFILT[4]	main-vertical filter mode; logic 0 = Mode 0; logic 1 = Mode 1
0	SVFILT[4]	sub-vertical filter mode; logic 0 = Mode 0; logic 1 = Mode 1

Notes

1. HPOS and VPOS determine the general location of the sub-PIP on the screen. HPOS only operates in modes SPS, SPL, DP, MP3 and MP4. VPOS only operates in modes SPS and SPL. The default location of the sub-pictures will be left top.
2. MFREEZE will freeze the main-picture, and SFREEZE will freeze the sub-picture selected by the live select bits as in Register 8 (see Table 13).
3. BCOLPOL can invert the border polarity of U and V.
4. MVFILT and SVFILT set the type of vertical filtering for the main and sub-channel. Mode 1 means that diagonal lines are linearized, in Mode 0 this option is switched OFF. This filtering mode only operates with vertical reduction factors $\frac{1}{3}$ and $\frac{1}{4}$.

Table 7 Register 2; display horizontal fine position register

BIT	MODE	DESCRIPTION(1)
7	–	not used
6	–	not used
5	DHFP(5)	horizontal fine position (64 steps)
4	DHFP(4)	horizontal fine position
3	DHFP(3)	horizontal fine position
2	DHFP(2)	horizontal fine position
1	DHFP(1)	horizontal fine position
0	DHFP(0)	horizontal fine position

Note

1. The display position can be set in steps of 4 pixels/lines and 1 line/field. The offsets on the display position are depicted in Fig.4.

Table 8 Register 3; display vertical fine position register

BIT	MODE	DESCRIPTION(1)
7	–	not used
6	–	not used
5	DVFP(5)	vertical fine position (64 steps)
4	DVFP(4)	vertical fine position
3	DVFP(3)	vertical fine position
2	DVFP(2)	vertical fine position
1	DVFP(1)	vertical fine position
0	DVFP(0)	vertical fine position

Note

1. The display position can be set in steps of 4 pixels/lines and 1 line/field. The offsets on the display position are depicted in Fig.4.

Table 9 Register 4; reduction factor register

BIT	MODE	DESCRIPTION(1)
7	MREDH(1)	main-horizontal reduction factor
6	MREDH(0)	main-horizontal reduction factor
5	MREDV(1)	main-vertical reduction factor
4	MREDV(0)	main-vertical reduction factor
3	SREDH(1)	sub-horizontal reduction factor
2	SREDH(2)	sub-horizontal reduction factor
1	SREDV(1)	sub-vertical reduction factor
0	SREDV(0)	sub-vertical reduction factor

Note

1. 01 = $\frac{1}{1}$; 10 = $\frac{1}{2}$; 11 = $\frac{1}{3}$; 00 = $\frac{1}{4}$.

Table 10 Register 5; channel select register

BIT	MODE	DESCRIPTION
7	–	not used
6	CBSEL(2)[1]	channel-border select (maximum 8 channels)
5	CBSEL(1)[1]	channel-border select
4	CBSEL(0)[1]	channel-border select
3	–	not used
2	SLSEL(2)[2]	sub-live select (maximum 8 channels)
1	SLSEL(1)[2]	sub-live select
0	SLSEL(0)[2]	sub-live select

Notes

1. With CBSEL one border of the displayed sub-borders can be selected independently of the SLSEL. This only operates when the channel select-border is ON as in Register 8 (see Table 13) and when the selected channel number is displayed.
2. With SLSEL the active sub-live picture can be selected. This only operates when the SFREEZE is OFF as in Register 1 (see Table 6) and when the selected channel is displayed.

Background and main, sub and channel-border colour and brightness handling

Registers 6 to 9 (see Tables 11 to 14) handle background and main, sub and channel-border colour and brightness. The borders and background can be set ON and OFF.

Background, main and sub-borders are black when they are OFF. The channel-border gets the current sub-border colour when it is switched OFF. The brightness can be set in 4 steps (30%, 50%, 70% and 100%). Eight different colours can be set in accordance with Table 15.

Table 11 Register 6; main-border control register

BIT	MODE	DESCRIPTION
7	–	not used
6	MB0N	logic 0 = MB is OFF; logic 1 =MB is ON
5	MBBRT(1)	main-border brightness (4 steps)
4	MBBRT(0)	main-border brightness
3	–	not used
2	MBCOL(2)	main-border colour (8 colours)
1	MBCOL(1)	main-border colour
0	MBCOL(0)	main-border colour

Table 12 Register 7; sub-border control register

BIT	MODE	DESCRIPTION
7	–	not used
6	SBON	logic 0 = SB is OFF; logic 1 = SB is ON
5	SBBRT(1)	sub-border brightness (4 steps)
4	SBBRT(0)	sub-border brightness
3	–	not used
2	SBCOL(2)	sub-border colour (8 colours)
1	SBCOL(1)	sub-border colour
0	SBCOL(0)	sub-border colour

Table 13 Register 8; channel-border control register

BIT	MODE	DESCRIPTION
7	–	not used
6	CBON	logic 0 = CB is OFF; logic 1 = CB is ON
5	CBBRT(1)	channel-border brightness (4 steps)
4	CBBRT(0)	channel-border brightness
3	–	not used
2	CBCOL(2)	channel-border colour (8 colours)
1	CBCOL(1)	channel-border colour
0	CBCOL(0)	channel-border colour

Table 14 Register 9; background control register

BIT	MODE	DESCRIPTION
7	FACMODE[1]	logic 0 = FM is OFF; logic 1 = FM is ON
6	BGON	logic 0 = BG is OFF; logic 1 = BG is ON
5	BGBRT(1)	background brightness (4 steps)
4	BGBRT(0)	background brightness
3	–	not used
2	BGCOL(2)	background colour (8 colours)
1	BGCOL(1)	background colour
0	BGCOL(0)	background colour

Note

1. The FACMODE bit controls the factory mode which shows an enlarged background colour as depicted in Fig.17 (BGON must be set).

Table 15 Colour table

COLOUR TYPE	BRIGHTNESS (%)[1]							
	0	10	30	50	60	70	80	100
Black/white	40H	50H	60H	70H	47H	57H	67H	77H
Blue	–	–	41H	51H	–	61H	–	71H
Red	–	–	42H	52H	–	62H	–	72H
Magenta	–	–	43H	53H	–	63H	–	73H
Green	–	–	44H	54H	–	64H	–	74H
Cyan	–	–	45H	55H	–	65H	–	75H
Yellow	–	–	46H	56H	–	66H	–	76H

Note

1. The values in are the I²C-bus register values for the Colour Control Registers 6 to 9 (see Tables 11 to 14). The values are hexadecimal values of which the left part indicates the brightness and the right part the colour value.

Table 16 Border display

PIP MODES	MBON	BGON[1]	SBON	CBON	MAIN-BORDER DISPLAY[2]	BACK-GROUND DISPLAY	SUB-BORDER DISPLAY[2]	CHANNEL BORDER DISPLAY
MP4 MP8 MP9 FFS	OFF	OFF	–	–	live BG[3]	live BG[3]	–	–
	OFF	ON	–	–	BGCOL	BGCOL	–	–
	ON	OFF	–	–	MBCOL	live BG[3]	–	–
	ON	ON	–	–	MBCOL	BGCOL	–	–
SPS SPL	–	–	OFF	–	–	–	live BG[3]	–
	–	–	ON	–	–	–	SBCOL	–
DP	OFF	OFF	OFF	–	live BG[3]	live BG[3]	live BG[3]	–
	OFF	ON	OFF	–	BGCOL	BGCOL	BGCOL	–
	ON	OFF	ON	–	MBCOL	live BG[3]	SBCOL	–
	ON	ON	ON	–	MBCOL	BGCOL	SBCOL	–
MP3	–	OFF	OFF	ON	–	live BG[3]	live BG[3]	CBCOL
MP4	–	ON	OFF	ON	–	BGCOL	BGCOL	CBCOL
MP7	–	OFF	ON	ON	–	live BG[3]	SBCOL	CBCOL
MP8	–	ON	ON	ON	–	BGCOL	SBCOL	CBCOL
MP9								

Notes

1. The BGON I²C-bus bit controls the display area outside the PIP and border area, set to ON means that the background gets the BGCOL colour value.
2. The main and sub-border displays are dependent on the I²C-bus switches.
3. 'Live BG' means that the original picture is shown.

Table 17 Register A; decoder format register

BIT	MODE	RESULT
7	MCOLPOL[1]	main-UV polarity; logic 0 = original; logic 1 = inverted
6	MVSPOL[2]	main-vertical sync polarity; logic 0 = positive pulse; logic 1 = negative pulse
5	MHSYNC[3]	main-horizontal sync selection; logic 0 = burst edge; logic 1 = H – sync
4	MFPOL	main-field polarity; inverts field identification window
3	SCOLPOL[1]	sub-UV polarity; logic 0 = original; logic 1 = inverted
2	SVSPOL[2]	sub-vertical sync polarity; logic 0 = positive pulse; logic 1 = negative pulse
1	SHSYNC[3]	sub-horizontal sync selection; logic 0 = burst edge; logic 1 = H – sync
0	SFPOL	sub-field polarity, inverts field identification window

Notes

1. MCOLPOL and SCOPOL invert the UV video data.
2. MVSPOL and SVSPOL determine the active edge of the V_{sync}. If VSPOL is logic 0, the positive edge of the V_{sync} will be taken; if VSPOL is logic 1, the negative edge of the V_{sync} will be taken.
3. MHSYNC and SHSYNC determine whether the H_{sync} signal or the burstkey is used as internal horizontal synchronization.

The exact timing of the V_{sync} in relation to the H_{sync} reference pulse is depicted in Fig.18. A field identification window determines whether a V_{sync} is being handled as a 1st field or a 2nd field. This field identification window can be inverted by the FPOL bit. If FPOL is logic 0 and an active edge of the V_{sync} occurs when the F-ID signal is logic 0, it will be regarded as the 1st field. If FPOL is logic 0 and an active edge of the V_{sync} occurs when the F-ID signal is logic 1, it will be regarded as the 2nd field. If FPOL is logic 1 the 1st and 2nd field IDs are changed over.

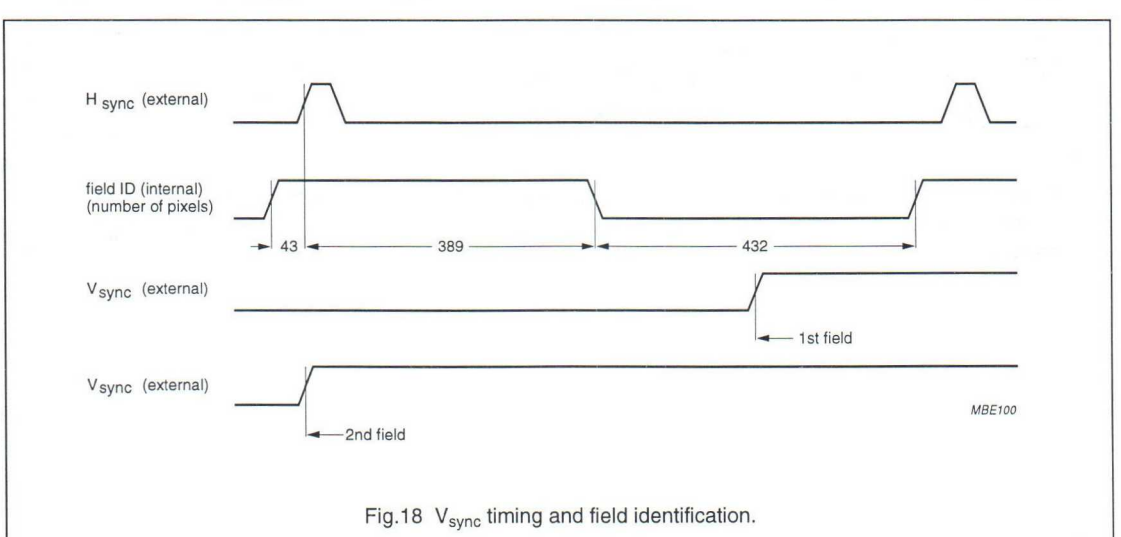


Fig.18 V_{sync} timing and field identification.

Table 18 Register B; main-acquisition area fine position

BIT	MODE	DESCRIPTION[1]
7	MAAHFP(3)	main-acquisition area horizontal fine position
6	MAAHFP(2)	main-acquisition area horizontal fine position
5	MAAHFP(1)	main-acquisition area horizontal fine position
4	MAAHFP(0)	main-acquisition area horizontal fine position
3	MAAVFP(3)[2]	main-acquisition area vertical fine position
2	MAAVFP(2)[2]	main-acquisition area vertical fine position
1	MAAVFP(1)[2]	main-acquisition area vertical fine position
0	MAAVFP(0)[2]	main-acquisition area vertical fine position

Notes

1. The acquisition area can be adjusted in 16 steps of 2 pixels horizontally and 1 line/field vertically.
2. With MAAVFP a complete field must have been processed before the next V_{sync} occurs. This is relevant for non-standard signals.

Table 19 Register C; sub-acquisition area fine position

BIT	MODE	DESCRIPTION [1]
7	SAAHFP(3)	sub-acquisition area horizontal fine position
6	SAAHFP(2)	sub-acquisition area horizontal fine position
5	SAAHFP(1)	sub-acquisition area horizontal fine position
4	SAAHFP(0)	sub-acquisition area horizontal fine position
3	SAAVFP(3)[2]	sub-acquisition area vertical fine position
2	SAAVFP(2)[2]	sub-acquisition area vertical fine position
1	SAAVFP(1)[2]	sub-acquisition area vertical fine position
0	SAAVFP(0)[2]	sub-acquisition area vertical fine position

Notes

1. The acquisition area can be adjusted in 16 steps of 2 pixels horizontally and 1 line/field vertically.
2. With SAAVFP a complete field must have been processed before the next V_{sync} occurs. This is relevant for non-standard signals.

Auxiliary registers

The Auxiliary Registers D to F (see Tables 20 to 22) are implemented to generate I²C-bus controlled signals for circuits which do not have an on-board I²C-bus.

Table 20 Register D; Auxiliary Control Register 1

BIT	MODE	DESCRIPTION
7	–	not used
6	–	not used
5	HUE(5)	hue control (output pin HUE)
4	HUE(4)	hue control
3	HUE(3)	hue control
2	HUE(2)	hue control
1	HUE(1)	hue control
0	HUE(0)	hue control

Table 21 Register E; Auxiliary Control Register 2

BIT	MODE	DESCRIPTION
7	–	not used
6	–	not used
5	SAT(5)	saturation control (output pin SAT)
4	SAT(4)	saturation control
3	SAT(3)	saturation control
2	SAT(2)	saturation control
1	SAT(1)	saturation control
0	SAT(0)	saturation control

Table 22 Register F; Auxiliary Control Register 3

BIT	MODE	DESCRIPTION
7	MMUTE	data bit directly to output pin MMUTE
6	SMUTE	data bit directly to output pin SMUTE
5	–	not used
4	–	not used
3	–	not used
2	–	not used
1	–	not used
0	–	not used

External memory

For the external memory two VDRAMS of type Mitsubishi M5442256 are used. They have a storage capacity of 262144 words of 4-bit each and will be used in parallel.

An overview of the timing to the VDRAM is depicted in Fig.19. Three different timing modes are shown. If the SAB9075 is not in one of these three modes, it is in idle mode in which all the control signals are HIGH. An idle mode takes at least 4 clock periods. Switching from one mode to another is always carried out via this idle mode.

The clock signal shown is an internal clock derived from the PLLs and is approximately 27 MHz.

Main and sub-ADCs

Both main and sub-channels convert the analog input signals to digital signals by three ADCs for each channel.

The input levels of the ADCs are equal and can set by the MAV_{refT}, SAV_{refT}, MAV_{refB}, and SAV_{refB} pins.The reference levels are made internally by a resistor network which divides the analog V_{DD} to a default set of preferred signal levels of 1.5 V. If the application requires a different set of levels the internal resistors can be shunted. External capacitors are required to filter AC components on the reference levels.

The resolution of the ADCs is 6-bit and the sampling is carried out at the system frequency of 27 MHz. The bias current I_{bias} is made internally but can be increased or decreased.

The inputs should be AC-coupled and an internal clamping circuit will clamp the input to MAV_{refB} and SAV_{refB} for the luminance channels and to

$$\frac{MAV_{refT} + MAV_{refB}}{2} + \frac{LSB}{2}$$

$$\frac{SAV_{refT} + SAV_{refB}}{2} + \frac{LSB}{2}$$

for the chrominance channels. The clamping starts at the active edge of the burstkey.

For more information see chapter "Test and application information".

Output DACs

The digital processed signals are converted to analog signals by means of three DACs. The output voltages of these DACs are default set by the DAV_{refTU}, DAV_{refTV} and DAV_{refTY} pins for the TOP-levels. Default signal levels are 1.5 V. The output buffer after each DAC is a PMOS source follower.

For more information see chapter "Test and application information".

HUE and SAT DACs

The HUE and SAT DACs are resistor DACs based on a R2R network. They have a direct control from their I^2C-bus register and therefore their sample frequency is limited by the I^2C-bus frequency. The output voltage is linear with the I^2CV_{DD}. Therefore the V_{DD} of this block is a separate pin.

PLLs and clock generation

The SAB9075H has two PLLs on-board, one for the sub-channel and one for the main-channel and the display part. The PLLs lock to the input signals MH_{sync} and SH_{sync}. The internal clock frequency is 1 728 times higher which is approximately 27 MHz in a standard NTSC system.

The positive edges of the H_{sync} signals are the driving timing points. For good short term stability they have to be noise/jitter free.

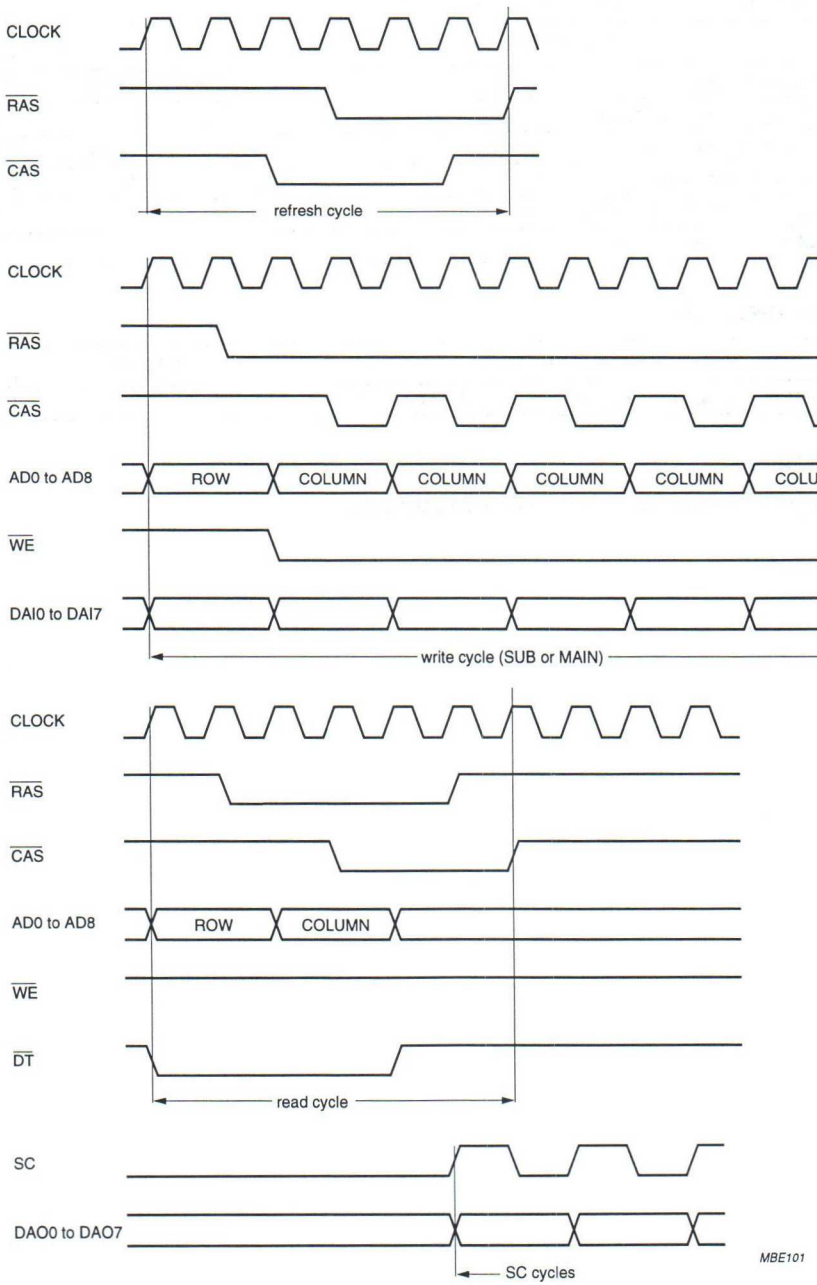


Fig.19 VDRAM timing.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
ΔV_{DD}	supply voltage variation	–	0.2	V
T_{stg}	storage temperature	−25	+150	°C
T_{amb}	operating ambient temperature	0	70	°C
V_{esd}	electrostatic discharge handling	–	–	V
P_{tot}	total power dissipation	–	1.5	W

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R_{thj-a}	thermal resistance from junction to ambient in free air	38	K/W

QUALITY SPECIFICATION

In accordance with SNW-FQ-611, Part E, dated 14 December 1992.

CHARACTERISTICS

V_{DD} = 5.0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	positive supply voltage		4.5	5.0	5.5	V
V_{SS}	negative supply voltage		–	0	–	V
ΔV_{DD}	maximum voltage difference between all positive supply pins		–	0	100	mV
ΔV_{SS}	maximum voltage difference between all negative supply pins		–	0	100	mV
I_{DDQ}	quiescent current digital positive supply pins	note 1	–	2	tbf	µA
$MPIV_{DDA}$	supply current PLL main		–	2.5	tbf	mA
$SPIV_{DDA}$	supply current PLL sub		–	2.5	tbf	mA
$MAIV_{DDA}$	supply current 3 main-ADCs		–	36	tbf	mA
$SAIV_{DDA}$	supply current 3 sub-ADCs		–	36	tbf	mA
DIV_{DDA}	supply current 3 display DACs		–	18	tbf	mA
I^2CV_{DD}	supply current HUE and SAT DACs	note 2	–	2.5	5	mA
I_{tot}	total supply current		tbf	220	tbf	mA
Converter and clamping						
AV_{refT}	top reference voltage	note 3	1.0	1.9	2.0	V
AV_{refB}	bottom reference voltage	note 3	0	0.4	1.0	V
Rin_{ref}	input resistance V_{refT} to V_{refB}	note 3; 1 ADC	tbf	860	tbf	Ω
V_I	DC input voltage		V_{refB}	–	V_{refT}	V
V_i	AC input voltage (peak-to-peak value)		1.0	1.5	–	V
R_i	input resistance	clamping OFF	1	–	–	MΩ
R_{iY}	input resistance for Y channel	clamping ON	–	200	–	Ω
R_{iV}	input resistance for V channel	clamping ON	–	800	–	Ω
R_{iU}	input resistance for U channel	clamping ON	–	800	–	Ω
C_i	input capacitance		–	15	–	pF
Res	resolution		–	6	–	bit
f_s	sample frequency rate	note 4	–	27	–	MHz
DNL	differential non-linearity		–1.0	–	+1.0	LSB
INL	integral non-linearity		–1.0	–	+1.0	LSB
V_{os}	input offset voltage		–1.0	–	+1.0	LSB
α_{cs}	channel separation	within channel	tbf	40	–	dB
		to other channel	tbf	40	–	dB
PSRR	power supply rejection ratio		tbf	40	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TD_{clamp}	delay burstkey edge to clamping start		–	0	–	µs
T_{clamp}	duration of clamping		–	2.33	–	µs
V_{clampY}	clamping voltage level Y	AD_{out} = 0H	–	V_s	–	V
V_{clampU}	clamping voltage level U	AD_{out} = 20H	–	0.5 V_{T+B}	–	V
V_{clampV}	clamping voltage level V	AD_{out} = 20H	–	0.5 V_{T+B}	–	V
Digital-to-analog converter						
V_{refT}	top reference voltage (Y, U and V)	note 3	1.0	1.5	2.0	V
Rin_{ref}	input resistance V_{refT} to V_{refB}	note 3; 1 DAC	tbf	1.0	tbf	kΩ
$V_{o(max)}$	maximum output voltage		V_{refB}	–	V_{refT}	V
$R_{L(min)}$	minimum load resistance		10	–	–	kΩ
$C_{L(max)}$	maximum load capacitance		–	50	–	pF
Res	resolution		–	7	–	bit
f_s	sample frequency rate	note 4	–	27	–	MHz
DNL	differential non-linearity		–0.5	–	+0.5	LSB
INL	integral non-linearity		–1.0	–	+1.0	LSB
α_{cs}	channel separation		tbf	40	–	dB
PSRR	power supply rejection ratio		tbf	40	–	dB
Digital-to-analog converter HUE/SAT						
V_o	output voltage		V_{SS}	–	V_{DD}	V
$R_{L(min)}$	minimum load resistance	note 2	100	–	–	kΩ
$C_{L(max)}$	maximum load capacitance		–	50	–	pF
Res	resolution		–	6	–	bit
DNL	differential non-linearity		–1.0	–	+1.0	LSB
INL	integral non-linearity		–1.0	–	+1.0	LSB
PSRR	power supply rejection ratio	note 2	–	0	–	dB
PLL and clock generation; note 4						
V_{TOP}	TOP-level input voltage		2.5	–	PV_{DD}	V
V_{LOW}	LOW-level input voltage		–	–	0.5	V
V_{slice}	slicing voltage level below TOP		0.45	1.0	2.0	V
f_{PLL}	input frequency		14750	15734	17250	Hz

Notes

1. Digital clocks are silent and analog bias current is zero.
2. The HUE and SAT DACs are based on a R2R ladder network as describe in the section "HUE and SAT DACs". The maximum output sample frequency is determined by the I^2C-bus.
3. The input configuration of the ADCs is depicted in Fig.20. The minimum difference $AV_{refT} - AV_{refB}$ should be larger than 1.0 V. The reference voltages can be calculated as follows:

$$V_{refT} = AV_{DD} \times \left(\frac{1.9}{5.0}\right) V \; ; \; V_{refB} = AV_{DD} \times \left(\frac{0.4}{5.0}\right) V$$

4. The internal system frequencies are 1728 times the input frequency. For more detailed information about the clock generation see section "PLLs and clock generation".

DC CHARACTERISTICS FOR DIGITAL PART

All V_{DD} pins = 4.5 to 5.5 V; T_{amb} = –20 to +75 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH level input voltage	HPF01	70	–	–	$\%V_{DD}$
		HPP01	70	–	–	$\%V_{DD}$
		HUP07	80	–	–	$\%V_{DD}$
V_{IL}	LOW level input voltage	IOI41	70	–	–	$\%V_{DD}$
		HPF01	–	–	30	$\%V_{DD}$
		HPP01	–	–	30	$\%V_{DD}$
		HUP07	–	–	20	$\%V_{DD}$
		IOI41	–	–	30	$\%V_{DD}$
V_{hys}	hysteresis voltage	HUP07	–	33	–	$\%V_{DD}$
V_{OH}	HIGH level output voltage	OPF20; I_{OL} = –2 mA; V_{DD} = 4.5 V	4.4	–	–	V
		SPF20; I_{OL} = –2 mA; V_{DD} = 4.5 V	4.4	–	–	V
V_{OL}	LOW level output voltage	IOI41; I_{OL} = +2 mA; V_{DD} = 4.5 V	–	–	0.15	V
		OPF20; I_{OL} = +2 mA; V_{DD} = 4.5 V	–	–	0.15	V
		SPF20; I_{OL} = +2 mA; V_{DD} = 4.5 V	–	–	0.15	V
I_{LI}	input leakage current	HPF01	–	0.1	1	µA
		HPP01	–	0.1	1	µA
I_{LOZ}	three-state output leakage current	IOI41; V_{DD} = 5.5 V	–	0.2	5.0	µA
R_{pu}	internal pull up resistor	HUP07	17	–	134	kΩ

AC CHARACTERISTICS FOR DIGITAL PART

V_{DD} = 4.5 5.5 V; T_{amb} = –20 to +75 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{sys}	system frequency	note 1	–	27	30	MHz
t_r	rise time	V_{DD} = 4.5 V	–	6	25	ns
t_f	fall time	V_{DD} = 4.5 V	–	6	25	ns

Note

1. The internal system frequencies are 1728 times the input frequency. For more detailed information about the clock generation see section "PLLs and clock generation".

TEST AND APPLICATION INFORMATION

Fig.20 shows how the ADCs and the DACs can be connected in the application.

The generation of the reference voltages is carried out internally and they have to be externally decoupled for AC signals.

For all ADCs and DACs the internal resistor division is such that a maximum signal voltage level of 1.5 V is obtained. For the ADCs there is a DC offset voltage of 0.4 V.

A modification of these reference voltages can be achieved by external shunting.

The ADC reference voltages are the same for all Y/U/V channels which means that their input levels need to be the same. The DAC voltage references can be set separately for Y/U/V channels. These reference voltages can be modified by shunting.

The output buffers of the DACS are PMOS source followers with a minimum output load of 10 kΩ.

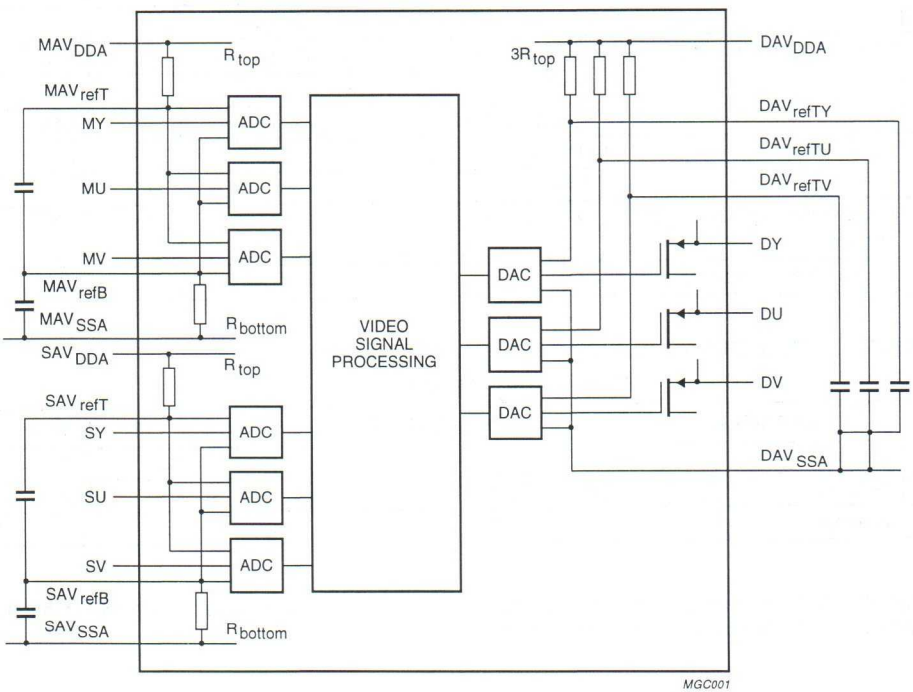


Fig.20 Analog application diagram ADCs and DACs.

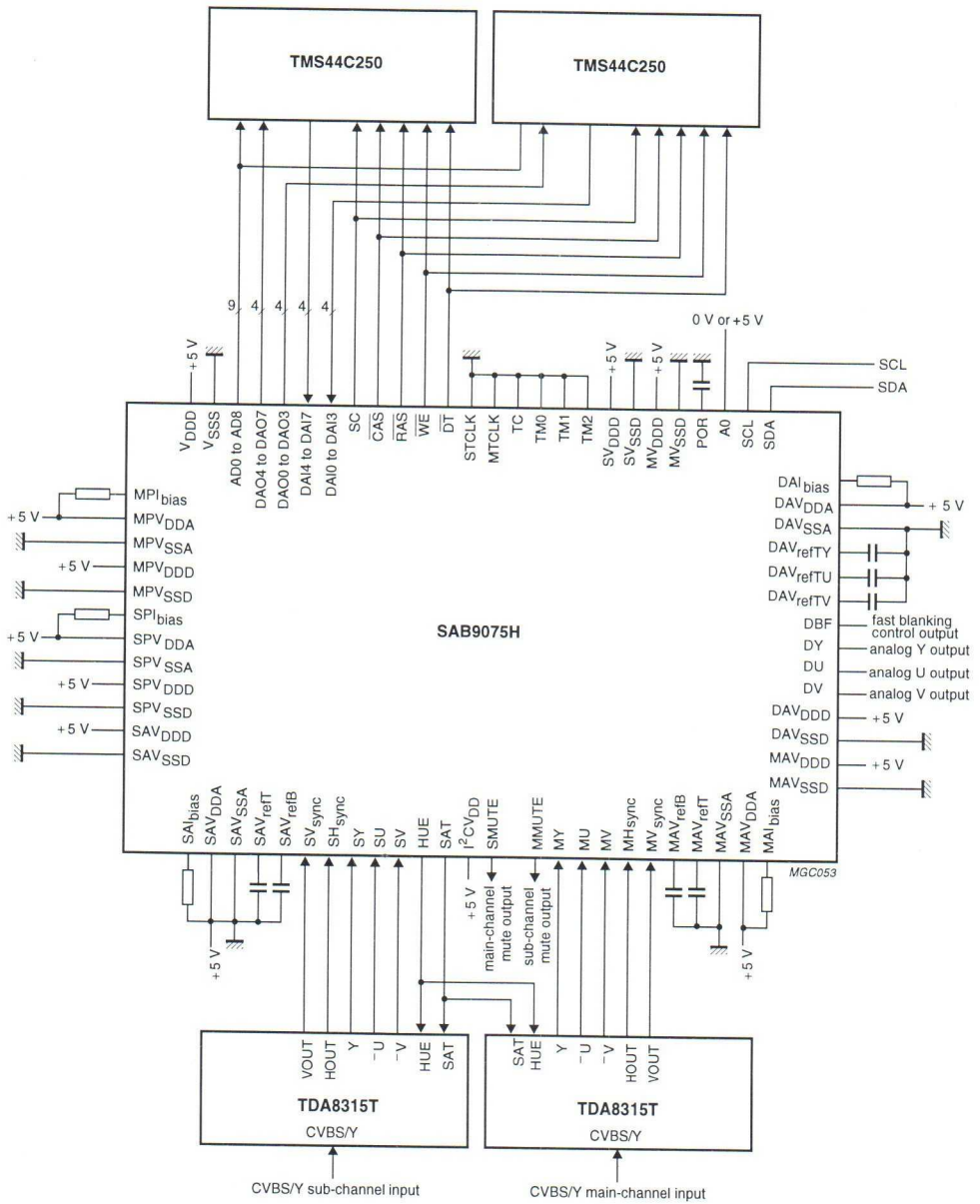


Fig.21 Application diagram.

UNIVERSAL DAC (UDAC)

GENERAL DESCRIPTION

The SAD1009 is intended as a peripheral to a microcontroller-based servo system in video cassette recorders. The device relieves the microcontroller of some of the real time functions. These functions include; generation of programmable pulse width signals (duty factor etc.) and accurate measurement of time period signals (tacho signal etc.). The SAD1009 has nine programmable output ports. All functions of the UDAC are programmable. Commands and data from the microcontroller are loaded via a bidirectional bus using a 16-bit format. Data from the time period measurement is transferred to the microcontroller via the same bidirectional bus, also using a 16-bit format. The clock signal for this device is provided by the quartz oscillator of the microcontroller.

Features

- Generation of programmable pulse width signals
- Measurement of time period signals
- All functions are programmable

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	4,75	5,0	5,25	V
Inputs						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,4	–	–	V
Input leakage current		$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	–	7,5	pF
Outputs						
Output voltage						
LOW	I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V
HIGH	I_{OH} = –1,0 mA	V_{OH}	V_{DD} –0,4	–	–	V
Output sink current		I_O	–	–	1,6	mA
Output source current		$-I_O$	–	–	1,0	mA

PACKAGE OUTLINES

SAD1009P: 24-lead DIL; plastic (SOT101A).
SAD1009T: 24-lead mini-pack; plastic (SO24; SOT137A).

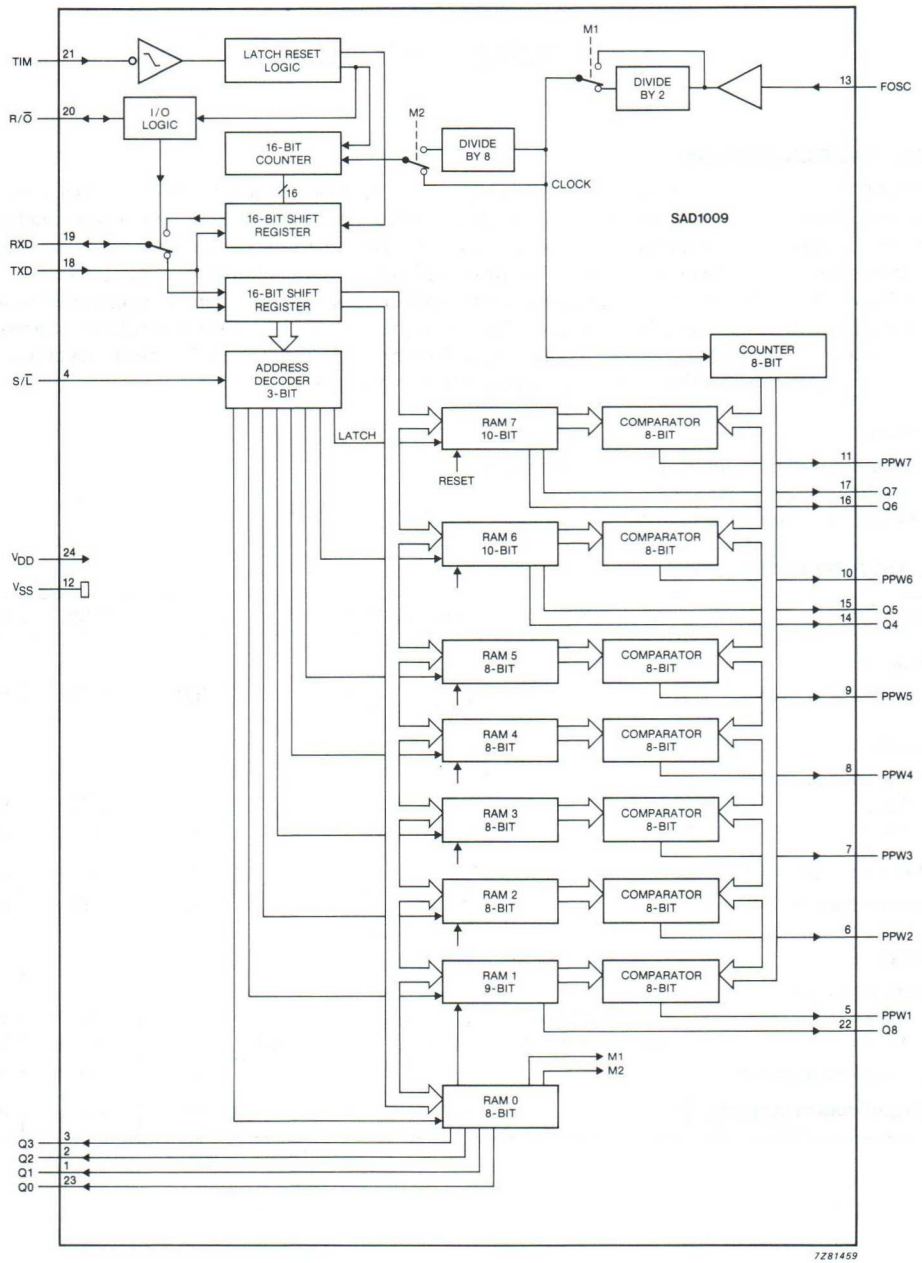


Fig. 1 Block diagram.

PINNING

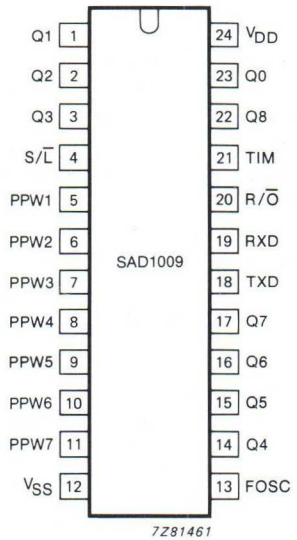


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

Power supply

V_{DD}	positive supply voltage (+5 V)
V_{SS}	ground (0 V)

Inputs

S/$\overline{L}$	shift/$\overline{\text{latch}}$ input
FOSC	oscillator input
TXD	serial clock

Special inputs

TIM	timer input

Outputs

Q0 to Q8	programmable output ports
PPW1 to PPW7	programmable pulse width outputs

Input/outputs

RXD	serial data
R/$\overline{O}$	handshake

FUNCTIONAL DESCRIPTION

Loading data

All commands and data are loaded into the SAD1009 via the bidirectional bus (TXD, RXD). The bidirectional bus is compatible with the serial interface of the '8051' microcontroller, using mode 0.

A 16-bit word is used to program a function of the UDAC. The first 3-bits received from the RAM constitute the address and the remaining 13-bits are data (LSB first, MSB last). None of the functions require all 13-bits of data, therefore, 16-bit words contain a number of immaterial bits (x). The programming format is shown in Table 1.

To shift a program word into the input buffer of the UDAC the S/$\overline{L}$ line (shift/latch not) must be HIGH. The contents of the input buffer are transferred to the appropriate RAM on the HIGH-to-LOW transition of the S/$\overline{L}$ signal. When S/$\overline{L}$ is LOW the input buffer is disabled and cannot accept new incoming information. Fig. 3 illustrates the program reception cycle.

Table 1 Programming format

bit	status	PPW1	PPW2	PPW3	PPW4	PPW5	PPW6	PPW7
1	L	H	L	H	L	H	L	H
2	L	L	H	H	L	L	H	H
3	L	L	L	L	H	H	H	H
4	$\overline{\text{RESET}}$	Q8	X	X	X	X	Q4	Q6
5	X	X	X	X	X	X	Q5	Q7
6	X	X	X	X	X	X	X	X
7	X	X	X	X	X	X	X	X
8	X	X	X	X	X	X	X	X
9	Q0	D8	D8	D8	D8	D8	D8	D8
10	Q1	D7	D7	D7	D7	D7	D7	D7
11	Q2	D6	D6	D6	D6	D6	D6	D6
12	Q3	D5	D5	D5	D5	D5	D5	D5
13	X	D4	D4	D4	D4	D4	D4	D4
14	X	D3	D3	D3	D3	D3	D3	D3
15	M1	D2	D2	D2	D2	D2	D2	D2
16	M2	D1	D1	D1	D1	D1	D1	D1

Where:

X : don't care
D1 to D8: data for programming pulse width, D1 = MSB and D8 = LSB

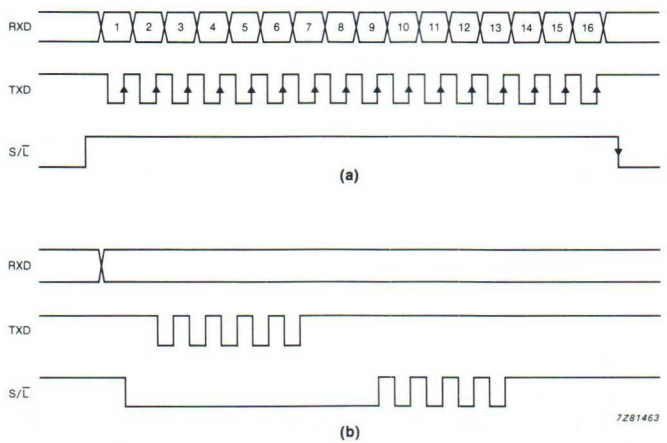


Fig. 3 Program reception cycle: a) normal reception cycle; b) no information is loaded into the input buffer, the RAMs contents remain unchanged.

Pulse width modulated outputs

The UDAC has seven pulse width modulated outputs (PPW1 to PPW7). The output PPW1 is slightly different to outputs PPW2 to PPW7, the difference is explained below. Each output produces a pulse width modulated signal with a duty factor programmable in steps of 1/256 and has a repetition frequency of approximately 23 kHz. These pseudo analogue signals are used to control the capstan and reel drives. Motor control can be performed in the following ways:

- convert the pulse width modulated signal into an analogue signal using filtering and analogue power amplification
- by feeding the pulse width modulated signal to the motor via a power switch and a switch mode filter

To conserve power use the second method for control of the capstain and reel motors. For the scanner control two outputs are available, so that by weighted addition a higher resolution can be achieved.

PPW1 is also an 8-bit programmable output, with a repetition frequency of 23 kHz. The difference is the low frequency contents of the signal are reduced by changing the distribution of the HIGH and LOW level portions. This redistribution means that a filter with two poles; each at 43 μs, is sufficient to reduce the peak-to-peak ripple to less than 1 LSB. This output is for use in applications where long filter delays are not tolerated.

Clock frequency

The clock signal of the UDAC is derived from the quartz oscillator of the microcontroller. The clock frequency should not exceed 6 MHz. The device also contains a programmable 'divide by two' circuit which allows these frequencies to be doubled, thus 6 MHz or 12 MHz microcontrollers can be used. The FOSC signal can be divided by two using bit M1 of RAM 0 (see Table 2).

Table 2 UDAC adjustment

bit M1	quartz frequency (MHz)
L	12
H	6

Programmable output ports

A total of nine output ports can be programmed to supply a HIGH or LOW level signal. Four of these outputs (Q4 to Q7) are intended to supply information about the breaking and direction of the capstan and reel motors, therefore these output ports must be programmed at the same time as the pulse widths of PPW6 and PPW7. Output port Q8 is programmed at the same time as PPW1. The other four output ports (Q0 to Q3) are programmed by RAM 0.

Measurement of the time period

To facilitate accurate measurement of the time period (falling edge to falling edge) of a signal applied to TIM, the UDAC contains a 16-bit counter and a buffer to store the contents of the previous counter measurement. The counter operates at a frequency of $f_{CLOCK}/2$ or $f_{CLOCK}/16$, the counter can be programmed using bit M2 of RAM 0. This timer can record periods of up to 21,8 ms and 175 ms respectively (see Table 3). When the time period is too long and the timer overflows, the microcontroller is loaded with a hex 'FFFF' when it reads the time period after the next pulse.

Table 3 Counter frequency

M2	division ratio	time period (max.)	frequency	resolution
L	2	21,8 ms	46 Hz	333 ns
H	6	175 ms	5,7 Hz	2,67 μs

Data from the timer can be transferred to the microcontroller via a bidirectional bus when the handshaking signal pin R/$\overline{O}$ is pulled LOW by the microcontroller. The LSB is transferred first and the MSB last. After the data has been transferred pin R/$\overline{O}$ remains in a LOW state (pulled down by the UDAC) until a new measurement of the time period is concluded. Note that each measurement of a time period can only be read once. After the next input pulse the 'data ready' state is signalled to the microcontroller by releasing the R/$\overline{O}$ pin, so that the microcontroller reads a HIGH level on this pin.

Note

During the 'data not ready' state the R/$\overline{O}$ is in a low impedance state and during the 'data ready' state the R/$\overline{O}$ is in a high impedance state (= HIGH). To speed up the transition from LOW-to-HIGH, the high impedance state is preceded by a short period of low impedance HIGH state.

Reset

The device can be reset by software by loading a LOW into the $\overline{\text{RESET}}$ bit of RAM 0. The effect of this reset is as follows:

- RAM 0; not influenced
- RAM 1; duty factor = 50%, Q8 = LOW
- RAM 2 to 5; duty factor = 50%
- RAM 6 to 7; duty factor = 0 and Q4 to Q7 = LOW

The reset is de-activated automatically on the next LOW-to-HIGH transition of S/$\overline{L}$. This allows new program information to be loaded and transferred to any RAM without having finished the reset. Due to RAM 0 not being influenced by the reset, the data required after the reset can be loaded along with the reset command.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	–	7	V
Input voltage range	note 1	V_I	−0,5	V_{DD} + 0,5	V
Input voltage at S/$\overline{L}$		$V_{4\text{-}12}$	−0,5	V_{DD} + 2,0	V
D.C. current into any input		$\pm I_I$	–	10	mA
D.C. current from any output		$\pm I_O$	–	10	mA
D.C. current into V_{DD}		$\pm I_I$	–	25	mA
D.C. current into V_{SS}		$\pm I_I$	–	25	mA
Total power dissipation	note 2	P_{tot}	–	200	mW
Storage temperature range		T_{stg}	−55	+150	°C
Operating ambient temperature range		T_{amb}	−20	+70	°C

Notes to ratings

1. Input voltage should not exceed 7 V unless otherwise specified.
2. Diminishes by 5 mW/K from 60 °C.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 4,75 to 5,25 V; T_{amb} = −20 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	4,75	5,0	5,25	V
Supply current range	$V_O = V_{DD}$, I_O = 0 mA on all outputs; $V_I = V_{SS}$ on all inputs	I_{DD}	–	100	–	μA
TXD, RXD, S/$\overline{L}$, R/$\overline{O}$						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,4	–	–	V
Input leakage current	note 1	$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	–	7,5	pF
RXD, R/$\overline{O}$, Q0 to Q7						
Output voltage	note 2					
LOW	I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V
HIGH	I_{OH} = −1,0 mA	V_{OH}	V_{DD}−0,4	–	–	V
Output sink current		I_O	–	–	1,6	mA
Output source current		$-I_O$	–	–	1,0	mA
FOSC						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,4	–	–	V
Input leakage current		$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	–	7,5	pF

D.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
RXD	used as input					
Input leakage current		$\pm I_I$	–	–	10	μA
TIM						
Input voltage						
LOW		V_{IL}	–	–	$0{,}3 \times V_{DD}$	V
LOW	V_{DD} = 5 V at 20 °C	V_{IL}	–	1,8	–	V
HIGH		V_{IH}	$0{,}7 \times V_{DD}$	–	–	V
HIGH	V_{DD} = 5 V at 20 °C	V_{IH}	–	2,9	–	V
Hysteressis	used as input	V_{hys}	–	730	–	mV
R/$\overline{O}$	used as input					
Output resistance		R_O	500	–	1000	Ω
Input leakage current		$\pm I_I$	–	–	10	μA
R/$\overline{O}$	used as output; open drain output; note 3; see Fig. 7					
Output voltage						
LOW	I_{OL} = 0,4 mA	V_{OL}	–	–	0,8	V
HIGH	I_{OH} = –0,4 mA	V_{OH}	$V_{DD}-0{,}8$	–	–	V
PPW1 to PPW7						
Output voltage						
LOW	I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
HIGH	I_{OH} = –4 mA	V_{OH}	$V_{DD}-0{,}4$	–	–	V
Output sink current		I_O	–	–	4	mA
Output source current		$-I_O$	–	–	4	mA

Notes to the d.c. characteristics

1. This value applies to TXD and S/$\overline{L}$, the input leakage current for RXD and R/$\overline{O}$ is shown above.
2. This value applies to RXD and Q0 to Q7, the output voltage for R/$\overline{O}$ is shown above.
3. After a LOW-to-HIGH transition of the R/$\overline{O}$ output, the port is held HIGH for approximately one clock cycle. This low impedance HIGH period is followed by the high impedance OFF-state.

DEVELOPMENT DATA

A.C. CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
RXD, R/$\overline{O}$, Q0 to Q7						
Output transition time	C_L = 50 pF					
LOW-to-HIGH		t_{TLH}	–	–	30	ns
HIGH-to-LOW		t_{THL}	–	–	30	ns
FOSC						
Maximum pulse frequency	M1 = L	f_{max}	–	–	12	MHz
	M1 = H	f_{max}	–	–	6	MHz
Minimum pulse width						
LOW		t_{WL}	20	–	–	ns
HIGH		t_{WH}	20	–	–	ns
TXD						
Pulse frequency		f_{max}	–	–	6	MHz
Pulse width						
LOW		t_{WL}	50	–	–	ns
HIGH		t_{WH}	50	–	–	ns
RXD	used as input; see Fig. 5					
Set-up time RXD to TXD		t_{SURXD}	50	–	–	ns
Hold time RXD to TXD		t_{HDRXD}	50	–	–	ns
RXD	used as output; see Fig. 6					
Propagation delay						
TXD to RXD		t_{PRXD}	–	–	50	ns
R/$\overline{O}$ to RXD		$t_{PR/O}$	–	–	50	ns
S/$\overline{L}$	see Fig. 7					
Pulse width LOW						
Set-up time TXD to S/$\overline{L}$		t_{SUTXD}	50	–	–	ns
Hold time TXD to S/$\overline{L}$		t_{HDTXD}	50	–	–	ns
Propagation delay S/$\overline{L}$ to Q0 - Q7		t_p	–	–	50	ns
TIM						
Pulse width						
LOW	M2 = LOW	t_{WL}	700	–	–	ns
LOW	M2 = HIGH	t_{WL}	5,4	–	–	μs
HIGH		t_{WH}	100	–	–	ns

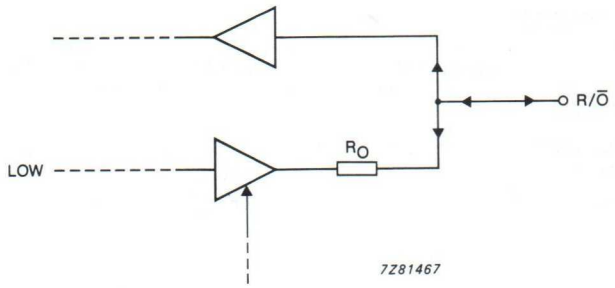


Fig. 4 Equivalent R/$\overline{O}$ output port.

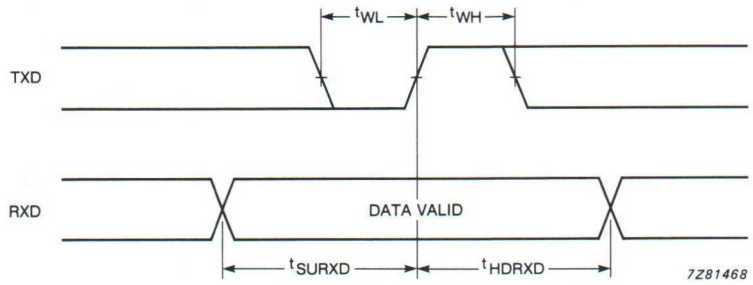


Fig. 5 RXD input waveform.

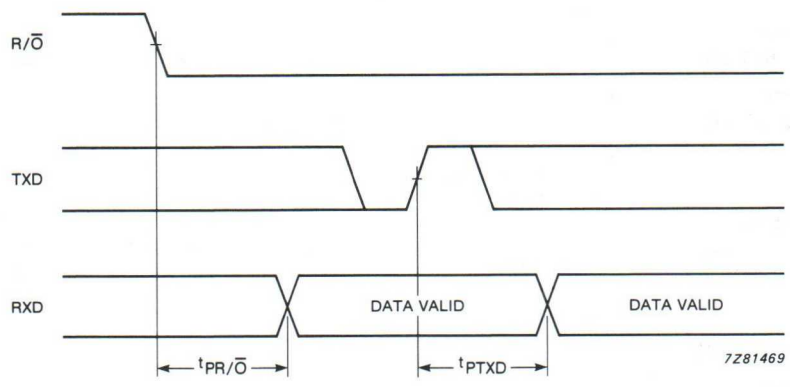


Fig. 6 RXD output waveform.

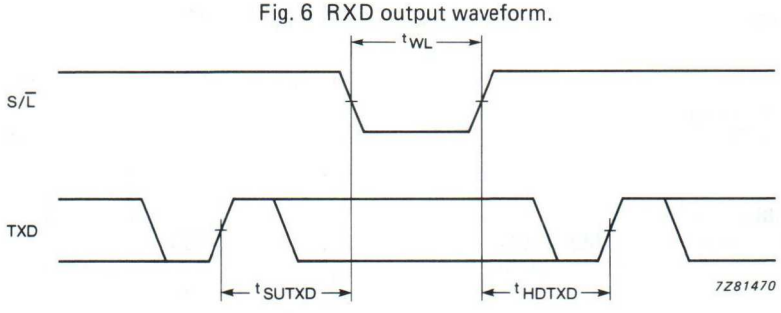


Fig. 7 S/$\overline{L}$ input waveform.

MULTI-NORM PULSE-PATTERN GENERATOR

GENERAL DESCRIPTION

The SAD1019 is part of a frame transfer image sensor camera system which uses the NXA series of frame transfer image sensors. The device provides the vertical transport pulses necessary, for the operation of the frame transfer image sensors and a start-stop signal for the horizontal clock generator. The drive pulses and clock signals for the SAD1019 are provided by the universal sync generator (SAA1043).

Features

- Vertical transport pulses for the image region and storage region of the image sensor during field blanking (ϕ_A and ϕ_B pulses)
- Colour separation and transport of one line of sensor information to the output register during line blanking (ϕ_B, TG and ϕ_C pulses)
- Other additional pulses required for the control and processing in the frame transfer image sensor camera

PACKAGE OUTLINES

SAD1019: 24-lead DIL; plastic (SOT101B).
SAD1019T: 24-lead mini-pack; plastic (SO24; SOT137A).

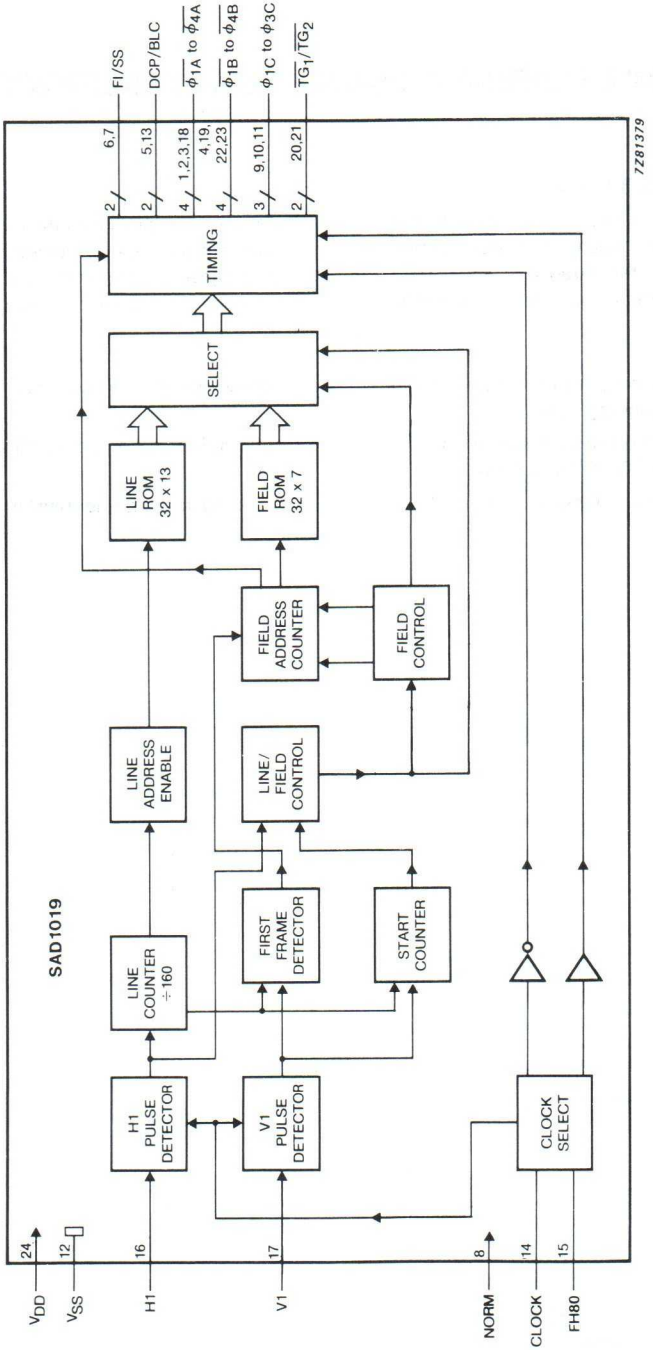


Fig.1 Block diagram.

PINNING

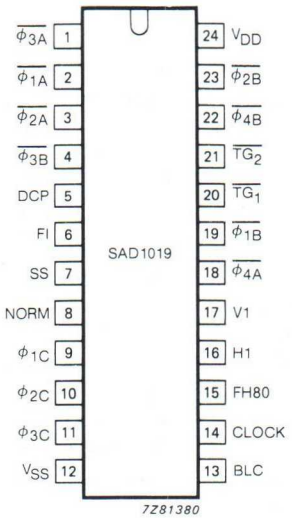


Fig.2 Pinning diagram.

Power supplies

V_{DD}	positive supply voltage (+ 5 V)
V_{SS}	ground (0 V)

Inputs (CMOS)

CLOCK	clock input from SAA1043, typ. 2.5 MHz (625 lines) or typ. 2.51748 MHz (525 lines). 5 MHz mode, typ. 5 MHz (625 lines) or 5.03496 MHz (525 lines)
FH80	clock input from SAA1043, typ. 1.25 MHz (625 lines) or 1.25874 MHz (525 lines)
H1	H1 input from SAA1043, typ. 15.625 kHz (625 lines) or typ. 15.734 kHz (525 lines)
V1	V1 input from SAA1043, typ. 50 Hz (625 lines) or 59.94 Hz (525 lines)
NORM	norm-selection input, 625 lines = LOW, 525 lines = HIGH

Outputs (CMOS push-pull)

$\overline{\phi 1A}$ to $\overline{\phi 4A}$	sensor image section control to drivers
$\overline{\phi 1B}$ to $\overline{\phi 4B}$	sensor storage section control to drivers
$\phi 1C$ to $\phi 3C$	low frequency outputs for transport pulses to pixel oscillator
DCP	DC clamp pulse
FI	frame identification
SS	start/stop for pixel generator
BLC	black-level clamping
$\overline{TG_1}$ and $\overline{TG_2}$	transfer gate control to drivers

FUNCTIONAL DESCRIPTION

625 line mode (NORM = LOW, see Figs 3 to 7)

One complete cycle of the multi-norm pulse-pattern generator (MNPPG) occurs after a command from the synchronization pulse generator (SYN). This cycle consists of 294 line cycles which are used to read out the sensor information followed by transport of the integrated information from the image area to the storage area of the sensor. Once this cycle has been completed the device enters into a 'wait' status period which lasts until the device receives a start command from the SYN.

The cycle is restarted with a V-pulse from the SYN. The falling edge of this pulse is detected in the MNPGG and results in a reset of the start counter as well as providing the field information (field 1/2). The start counter counts 11 lines and then the line cycle information is read from the line ROM. The start of the line cycle occurs at line 22 in frame 1 and line 335 in frame 2. The H1 pulse of the SYN controls the position of the line cycle with respect to the SYN pulses. The H1 pulse sets the correct value in the line counter of the MNPPG.

The control counter counts the number of line cycles and switches the line cycle to field cycle after 294 lines (in both fields), then the field cycle information is read from the field ROM. The control counter was reset before the switch over had taken place, it now counts the field cycles. The field cycle lasts for 294 cycles of the $\overline{\phi 4B}$ pulse and then the device enters the wait status period again.

The device will continue to operate in the manner described, until the overall system is switched off.

525 line mode (NORM = HIGH)

The basic operation is identical except for variations in the start points and number of transports (see Figs 8 to 12).

Operating modes

Synchronization generator (SAA1043)

The H1 pulse from the SAA1043, due to internal delays, is out of phase with the MNPPG clock signal. The following method is used to obtain the correct phase relationship between the H1 pulse and the MNPPG output. The H1 pulse and the FH80 are clocked into a flip-flop, at the output of the flip-flop the timing of the H1 and FH80 signals are in phase. The output of the flip-flop is sampled with that of the CLOCK, which is in phase with the FH80. In this way a reliable fixed phase relationship between SYN and MNPPG is obtained.

Other operating modes

- single 2.5 MHz operation:
  If another synchronization pulse generator is used, in which an H1 pulse is in phase with the CLOCK, a single 2.5 MHz clock signal can be used.

  Connect the 2.5 MHz to the CLOCK and with delay circuitry (RC elements, 50 ns approx.) to FH80.
- single 5 MHz operation:
  If another synchronization pulse generator is used, in which an H1 pulse is in phase with the CLOCK, a single 5 MHz clock signal can be used.

  Connect the 5 MHz to the CLOCK and connect FH80 to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 24)	V_{DD}	−0.5	+ 7.0	V
Supply current (pin 24)	I_{DD}	–	50	mA
Supply current (pin 12)	I_{SS}	–	50	mA
Input voltage range	V_I	−0.5	V_{DD} + 0.5*	V
Input current	$\pm I_I$	–	10	mA
Output current	$\pm I_O$	–	10	mA
Total power dissipation per package	P_{tot}	–	500	mW
Power dissipation per output	P_O	–	25	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* V_{DD} + 0.5 V not to exceed 7.0 V.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 25 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Current						
Supply current	on all outputs; I_O = 0 mA	I_{DD}	–	–	10	μA
Inputs H1, V1, NORM, CLOCK and FH80						
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	–	V
Input voltage LOW	CMOS compatible	V_{IL}	–	–	$0.3V_{DD}$	V
Outputs						
Output voltage HIGH	all outputs except BLC; $-I_O$ = 0.8 mA; V_{DD} = 5 V	V_{OH}	–	–	$V_{DD}-0.5$	V
Output voltage LOW	all outputs except BLC; I_O = 2.9 mA; V_{DD} = 5 V	V_{OL}	–	–	0.5	V
Black level clamping (BLC)						
Output voltage HIGH	$-I_O$ = 2.6 mA; V_{DD} = 5 V	V_{OH}	–	–	$V_{DD}-0.5$	V
Output voltage LOW	I_O = 2.9 mA; V_{DD} = 5 V	V_{OL}	–	–	0.5	V

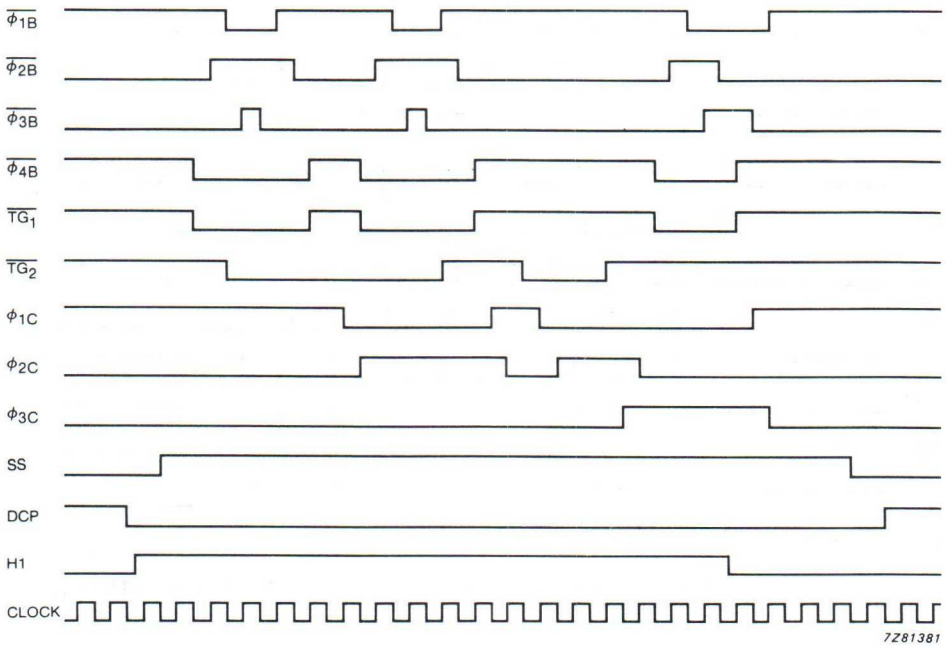
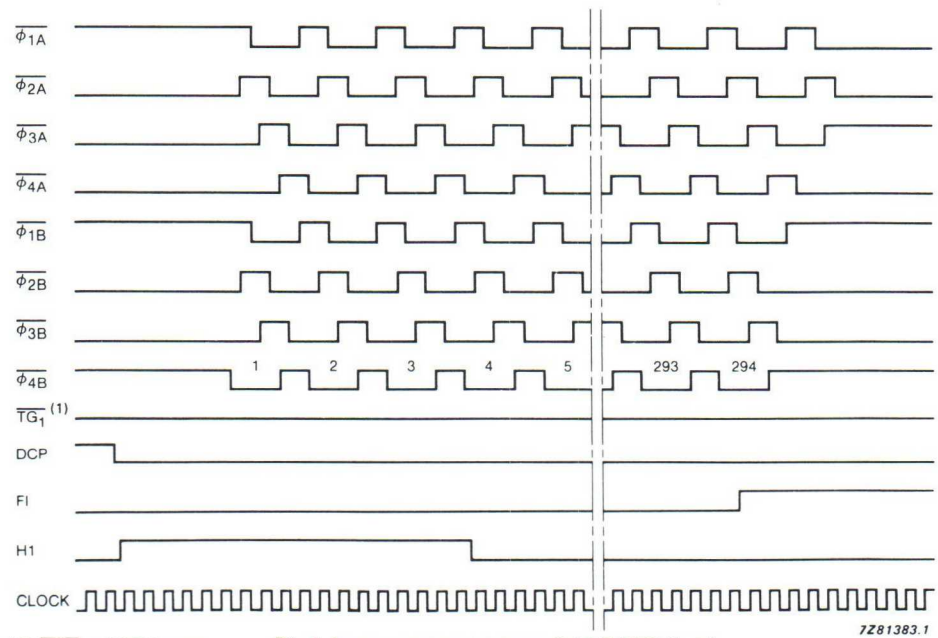
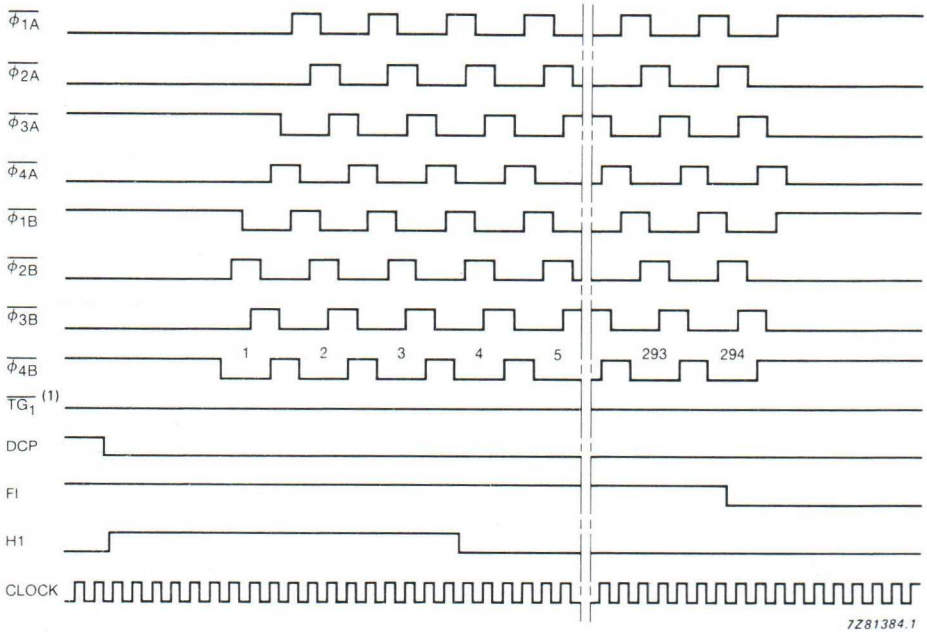


Fig.3 Line transport (625 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.4 Image sensor transport, field 2 (625 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.5 Image sensor transport, field 1 (625 lines).

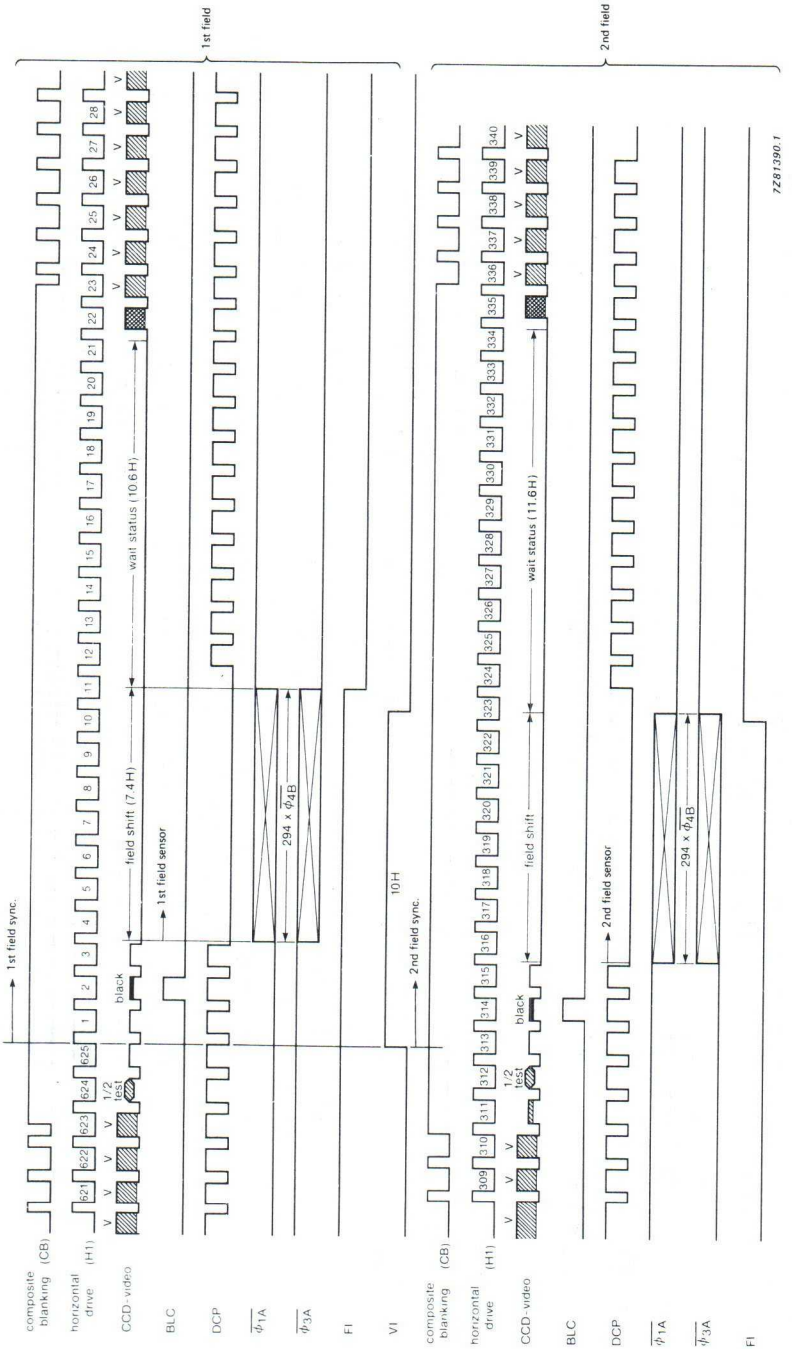


Fig.6 Pulse pattern during field blanking (625 lines).

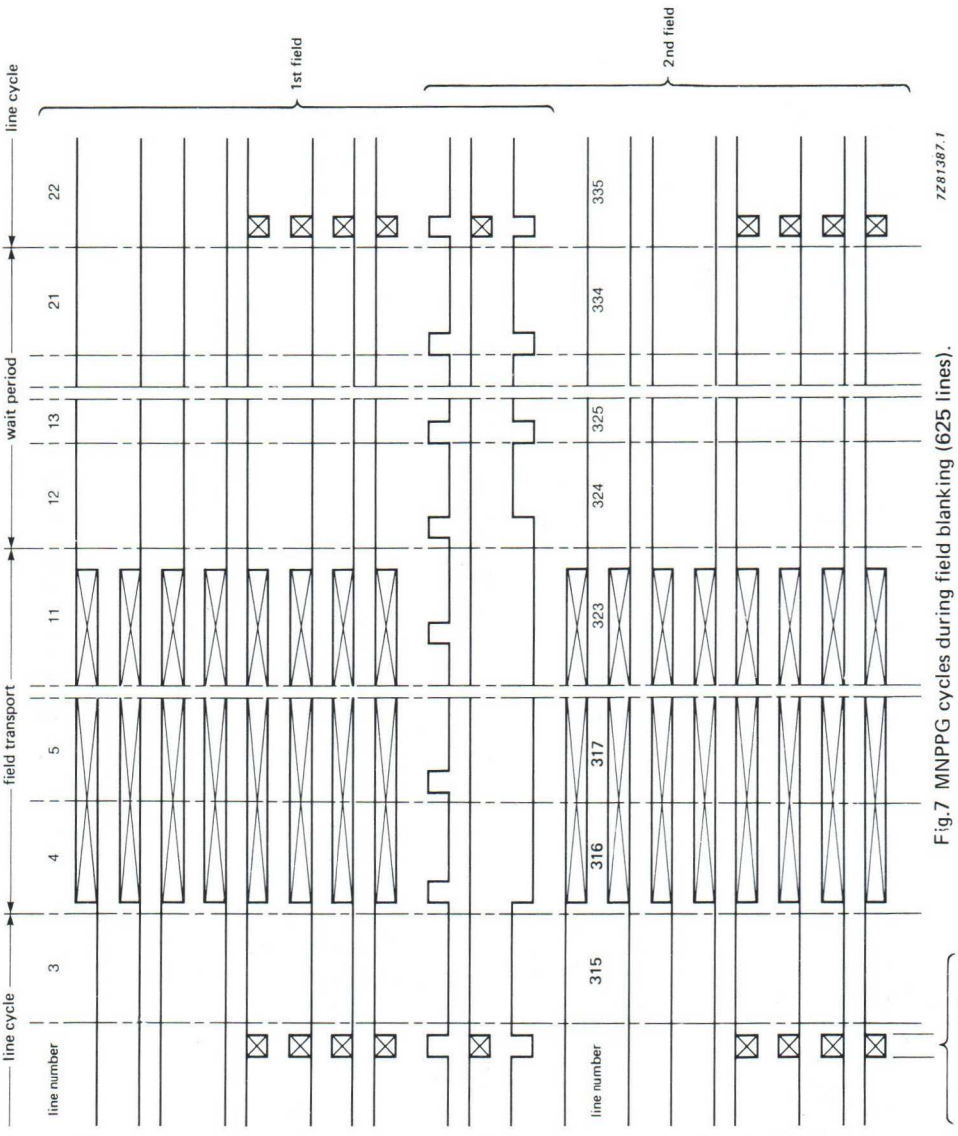


Fig.7 MNPPG cycles during field blanking (625 lines).

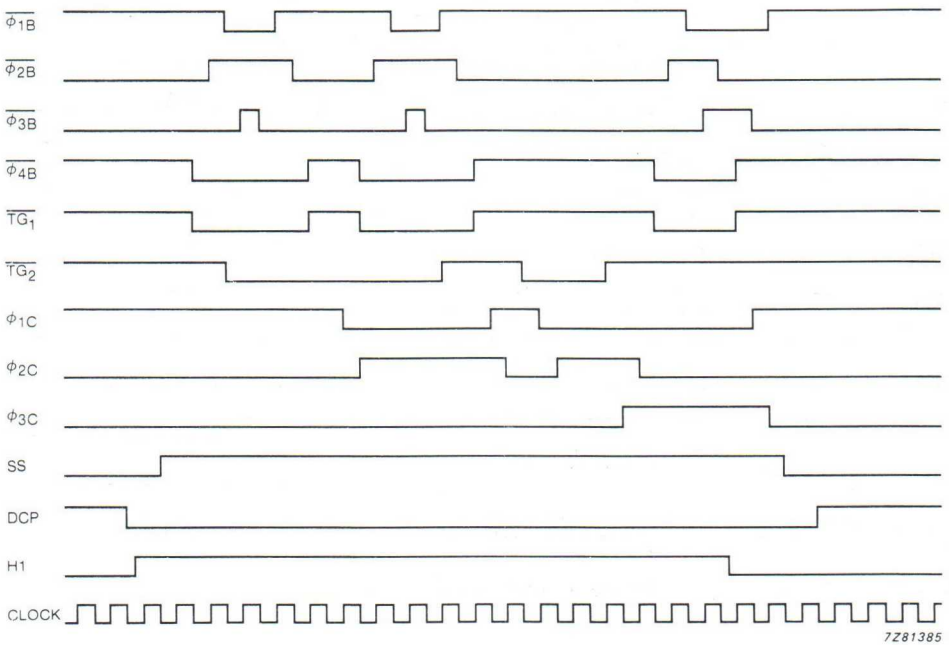
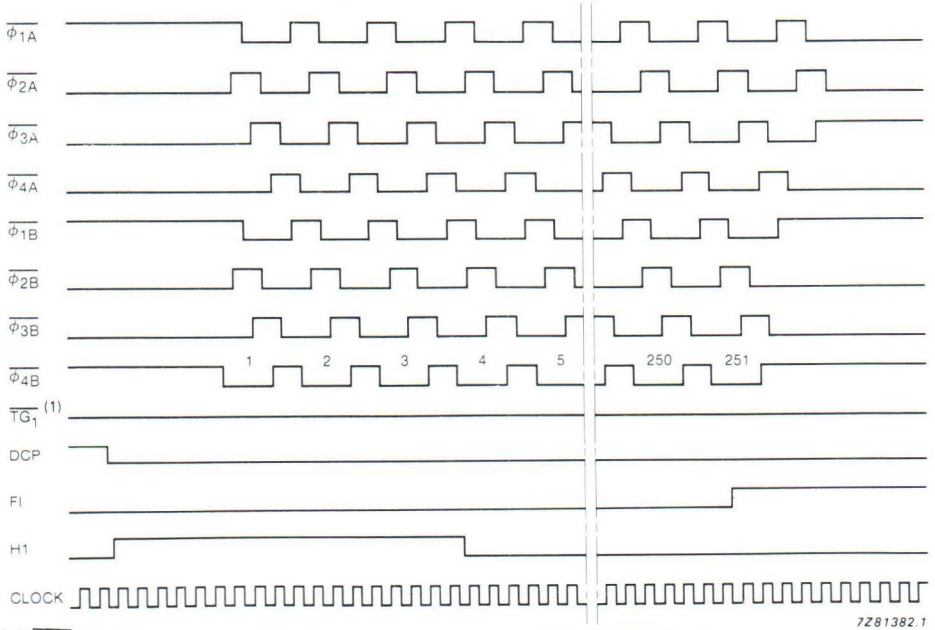
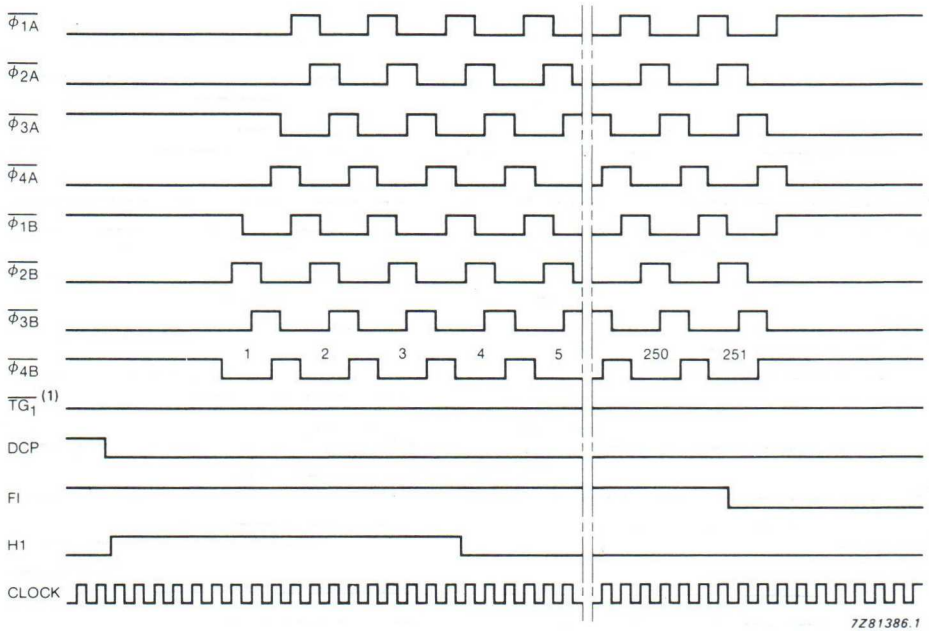


Fig.8 Line transport (525 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.9 Image sensor transport, field 2 (525 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.10 Image sensor transport, field 1 (525 lines).

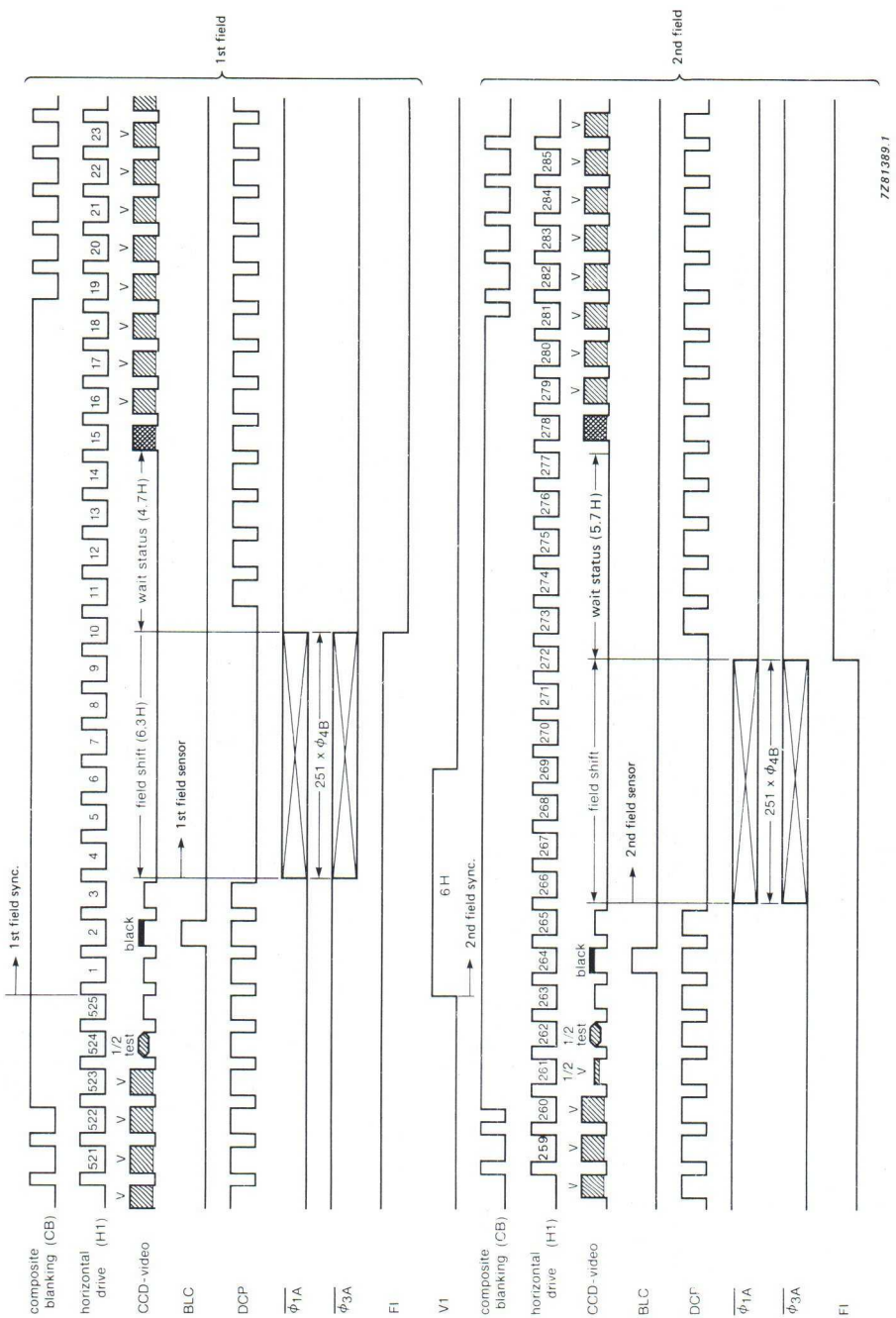


Fig.11 Pulse pattern during field blanking (525 lines

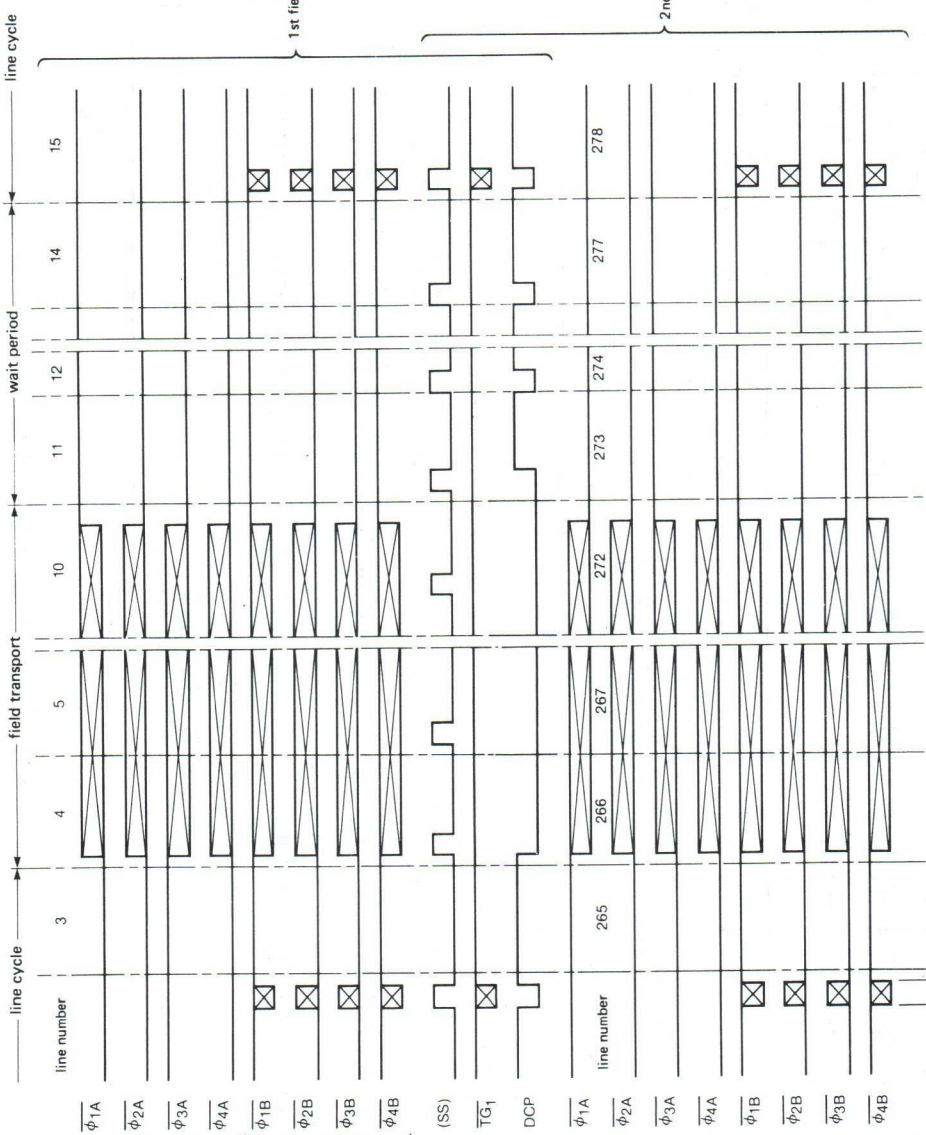


Fig.12 MNPPG cycles during field blanking (525 lines).

DATA LINE DECODER

GENERAL DESCRIPTION

The SAF1135 is a data line decoder, designed in CMOS technology, which operates in conjunction with the data line processor (SAA5235) to form a data line receiver system.

This system receives and decodes binary data that is transmitted in line 16 of every first field of a standard television signal. The decoded information is accessed via the built-in I^2C bus interface. This information can be used to program a video tape recorder to start and stop the recording of a television program at the correct time, regardless of a delay or extension in the transmission time of the required television program.

Valid Video Programming System (VPS) data is transmitted in line 16 only. There is no VPS information in line 329.

The data transmission is biphase modulated and the bit transfer rate is 2,5 Mbit/s.

Features

- Field selection
- Line 16 decoding
- Start code check
- Biphase check
- Storage of data line information
- Generation of data reset pulse
- I^2C bus transmitter

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 14)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 14)	I_{DD}	–	1	–	mA
Bit transfer rate at input DLD (pin 8)	BR_{DLD}	–	2,5	–	Mbits/s
Clock frequency at input DLCL (pin 11)	f_{DLCL}	–	5	–	MHz
Storage temperature range	T_{stg}	−65	–	+150	°C
Operating ambient temperature range	T_{amb}	0	–	70	°C

PACKAGE OUTLINES

14-lead DIL; plastic (SOT27).

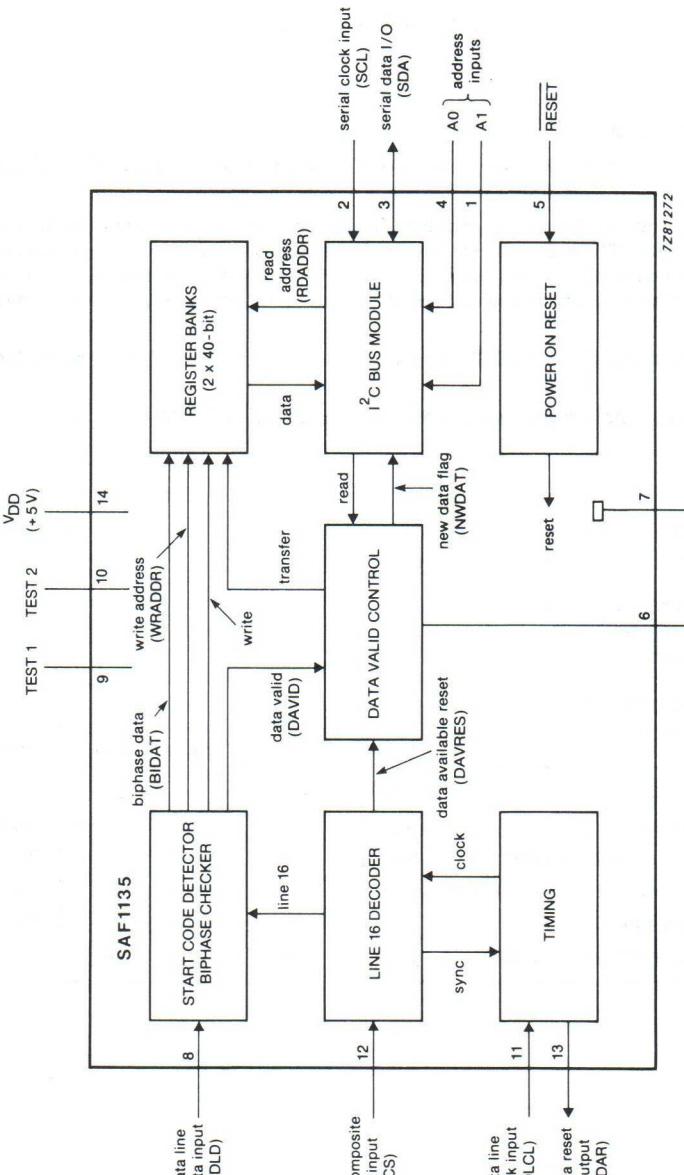


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The SAF1135 is designed to receive and decode Video Tape Recorder (VTR) control information which is transmitted in line 16 of every first field of a standard television signal. The following description refers to the block diagram Fig. 1 unless otherwise stated.

Data line 16

The total information of data line 16 consists of fifteen 8-bit words. The contents of the information is shown in Fig. 2, a timing diagram of the data line in Fig. 3 and a survey of VTR control labels in Fig. 4.

From the total fifteen 8-bit words, the SAF1135 extracts words 5, 11, 12, 13 and 14. The contents of these words can be requested via the built-in I^2C bus interface (see Fig. 9). The circuit is fully transparent, thus each bit is transferred without modification. Only the sequence of the words is changed; words 11 to 14 being transmitted first followed by word 5.

By evaluation of the Video Composite Sync (VCS) signal at pin 12 the SAF1135 identifies the beginning of line 16 in the first field. The line 16 decoder stage releases the start code detector. When a correct start code is detected (for timing of start code detection, see Fig. 5) words 5 and 11 to 14 are decoded, checked for biphase errors and stored in register bank R (Receive). If no biphase error has occurred, the contents of register bank R are transferred to register bank T (Transmit) by the data valid control signal (DAVID). If the system has been addressed, this transfer is delayed until the next start or stop condition of the I^2C bus has been received.

The last correct data line information remains available until it is read via the I^2C bus. After it is read once the stored information is no longer considered to be valid, the internal new data flag (NWDAT) is reset and if the circuit is addressed, the only VPS data sent back is "FFF...F". The same conditions apply after power-up. Then no data can be read out.

New data is available after reception of another error-free line 16.

Power-on Reset

Reset pulses applied externally to pin 5 ($\overline{\text{RESET}}$; active LOW) are latched internally by the power-on reset circuit.

$\overline{\text{RESET}}$ = LOW influences:

- I^2C bus logic to no acknowledge
- NWDAT flag and internal timing to reset
- Data available output ($\overline{\text{DAV}}$; active LOW) at pin 6 forced to LOW
- Data reset output (DAR) at pin 13 forced to HIGH
- Serial data (SDA) input/output at pin 3 released

When $\overline{\text{RESET}}$ changes to HIGH the reset period is terminated with the next negative-going transition of the data line clock (DLCL) input at pin 11. Then, the data available ($\overline{\text{DAV}}$) output at pin 6 will go HIGH.

When an external reset is not used pin 5 is connected to V_{DD}. If an external reset is required, the rise time (t_r) of $\overline{\text{RESET}}$ voltage must be greater than 50 μs. An external 10 kΩ resistor connected between pin 5 and V_{DD} and an external 2,7 nF capacitor connected to V_{SS} will result in $t_r \geqslant 50$ μs.

FUNCTIONAL DESCRIPTION (continued)

Word	Content
1	Run in
2	Start code
3	Program source identification (binary coded)
4	Program source identification (ASCII sequential)
5	Sound and VTR control information
6	Program/Test picture identification
7	Internal information exchange
8	Address assignment of signal distribution
9	
10	Messages/Commands
11	VTR Control Information
12	
13	
14	
15	Reserve

Fig. 2 Total information of data line 16.

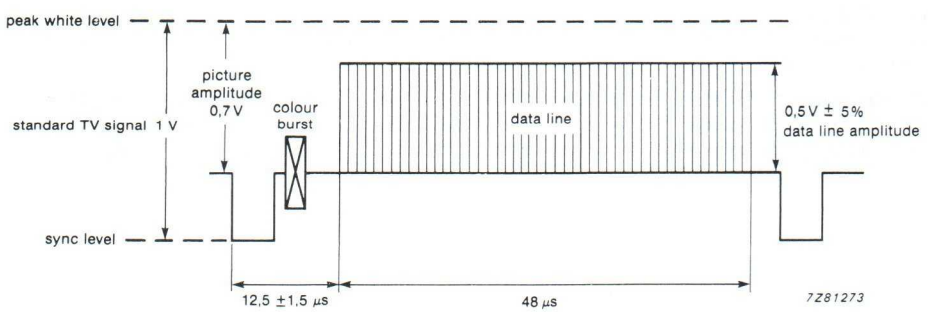


Fig. 3 Timing diagram of data line 16; modulation depth 71,4%.

| | VTR Control Information | | |

FUNCTIONAL DESCRIPTION (continued)

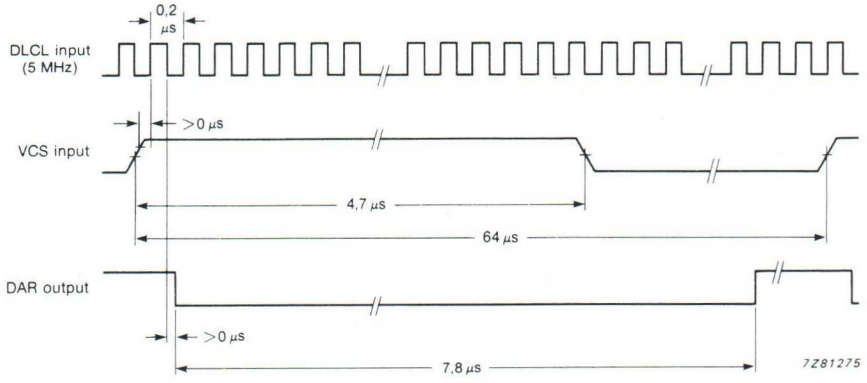


Fig. 6 Timing diagram of the data reset pulse generation.

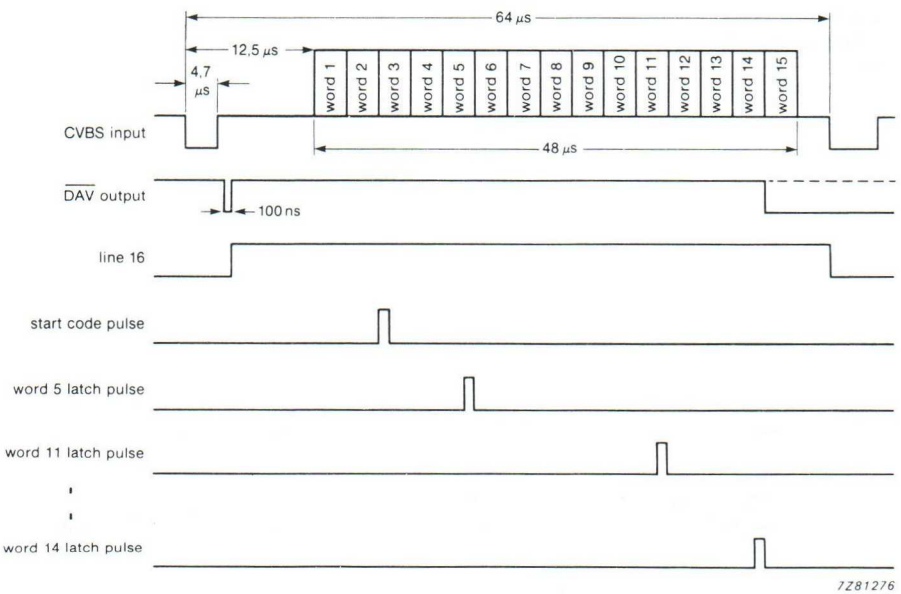


Fig. 7 Timing diagram of the data available output and word latch pulses.

Data line data and clock inputs (DLD; DLCL)

The data line data and clock signals from the SAA5235 are input at pins 8 and 11 respectively. The data transmission is biphase modulated, the bit transfer rate is 2,5 Mbit/s and the clock frequency is 5 MHz.

Input DLD incorporates an internal active clamping circuit. DLCL is internally a.c. coupled.

Video composite sync input (VCS)

The VCS input pulse at pin 12 is used for:

- Generation of the data reset pulse (DAR)
- Identification of the first field
- Selection of line 16

The timing of the data reset pulse generation is shown in Fig. 6.

I^2C bus address inputs (A0; A1)

The two I^2C address inputs at pins 4 and 1 respectively, provide the four different addresses 20H, 22H, 24H and 26H.

Data reset output (DAR)

The DAR output at pin 13 is a line frequency pulse with a 0,88 duty factor derived from the VCS pulse. The DAR pulse is fed to the SAA5235 to reset the data slicer circuit and the clock phase detector circuit.

Data available output ($\overline{DAV}$)

The $\overline{DAV}$ active LOW output at pin 6 is set to LOW after reception of one error-free data line 16. $\overline{DAV}$ returns to HIGH after at the beginning of the next first field.

If no valid data is available $\overline{DAV}$ remains HIGH. However, a short duration (100 ns) pulse inserted at the beginning of line 16 ensures that a HIGH-to-LOW transition occurs, which can be used for triggering.

The timing of $\overline{DAV}$ output and word latch pulses is shown in Fig. 7.

I^2C bus

The internally latched data from words 5 and 11 to 14 can be clocked out via the I^2C interface by a bus master. The lines are the serial clock input (SCL) at pin 2 and the serial data input/output (SDA) at pin 3.

The SAF1135 can operate only as a slave transmitter on the bus.
Data format is shown in Fig. 8.

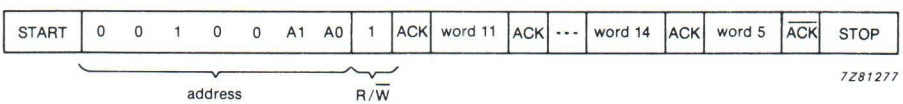


Fig. 8 I^2C bus data format.

- The MSB of each word is transmitted first.
- There is no restriction on the number of words to be transmitted, but if more than five words are requested, word 5 will be repeated.
- Noise pulses less than 200 ns duration are ignored on the bus lines.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 14)	V_{DD}		−0,5 to +7,0	V
Supply current (pin 14)	I_{DD}	max.	20	mA
Supply current (pin 7)	I_{SS}	max.	20	mA
Input voltage (pins 8 and 11)	V_I		−0,5 to +12	V
Input voltage on all other pins	V_I		−0,5 to V_{DD} +0,5*	V
Input current	$\pm I_I$	max.	10	mA
Output current	$\pm I_O$	max.	10	mA
Power dissipation per package**	P_{tot}	max.	400	mW
Power dissipation per output	P	max.	100	mW
Storage temperature range	T_{stg}		−65 to +150	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

* V_{DD} +0,5 not to exceed 7,0 V.

** Above +60 °C: derate linearly with 8 mW/K.

D.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 14)						
Supply voltage	–	V_{DD}	4,5	5	5,5	V
Supply current	Quiescent at 25 °C All inputs at V_{DD} or V_{SS} $\overline{RESET}$ at V_{SS} TEST 1 and $\overline{TEST\ 2}$ at V_{DD} I_O = 0 mA	I_{DD}	–	–	10	μA
	During normal operation (without LED at $\overline{DAV}$, V_{DD} = 5 V)	I_{DD}	–	1	–	mA
Inputs						
A0, A1, TEST 1, TEST 2, SCL						
Input voltage LOW		V_{IL}	–	–	$0{,}2V_{DD}$	V
Input voltage HIGH		V_{IH}	$0{,}7V_{DD}$	–	–	V
Leakage current		I_{LI}	–	–	1	μA
DLCL						
Input voltage	Clock internally a.c. coupled	V_I	–	–	12	V
Leakage current	V_I = 0 to 10 V	I_{LI}	–	–	10	μA
$\overline{RESET}$	During normal operation pin 5 connected to V_{DD}					
Input voltage LOW		V_{IL}	–	–	$0{,}3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0{,}9V_{DD}$	–	–	V
Input current HIGH		I_{IH}	–	–	15	μA
Leakage current		I_{LI}	–	–	10	μA
VCS						
Input voltage LOW		V_{IL}	–	–	0,8	V
Input voltage HIGH		V_{IH}	2,0	–	–	V
Leakage current		I_{LI}	–	–	1	μA

D.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs/Outputs						
DLD	Internal active clamping circuit, open drain output					
Input voltage LOW		V_{IL}	–	–	0,9	V
Input voltage HIGH		V_{IH}	2,0	–	12	V
Leakage current		I_{LI}	–	–	1	μA
Output voltage LOW	I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
SDA	open drain output					
Input voltage LOW		V_{IL}	–	–	0,9	V
Input voltage HIGH		V_{IH}	3,15	–	–	V
Leakage current	V_{DD} = 6 V; V_I = 0 or V_{DD}	I_{LI}	–	–	6	μA
Output voltage LOW	I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
Outputs						
DAR						
Output voltage LOW	I_{OL} = 1 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH	$-I_{OH}$ = 400 μA	V_{OH}	V_{DD}–0,5 V	–	–	V
$\overline{DAV}$						
Output voltage LOW	I_{OL} = 10 mA	V_{OL}	–	–	1,0	V
Output voltage HIGH	$-I_{OH}$ = 400 μA	V_{OH}	V_{DD}–0,5 V	–	–	V

A.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs						
Input capacitance		C_I	–	–	10	pF
A0, A1, TEST 1, TEST 2, SCL						
Rise time	$V_{IL(max)}$ to $V_{IH(min)}$	t_r	50	–	–	µs
DLCL						
Clock frequency	sinusoidal input signal	f_{DLCL}	–	5	–	MHz
Input voltage	peak-to-peak value	$V_{I(p-p)}$	1	–	–	V
DLD						
Coupling capacitor		C_{EXT}	—	1	4,7	nF
Set-up time	relative to rising edge of DLCL	t_{SU}	40	–	–	ns
Hold-up time	relative to rising edge of DLCL	t_{HD}	40	–	–	ns
Outputs						
DAR, $\overline{DAV}$						
Rise and fall times	C_L = 50 pF	t_r, t_f	–	–	50	ns
DAR-time LOW		$t_{DAR,L}$	–	7,8	–	µs
SDA						
Fall time	C_L = 400 pF	t_f	–	–	300	ns
I²C bus - Input/Output						
Input current HIGH	For both SDA and SCL valid 0,9 V_{DD}, including I_{LI} of possible output stage	I_{IH}	–	–	10	µA
Input capacitance		C_I	–	–	10	pF
Rise time		t_r	–	–	1	µs
Fall time		t_f	–	–	0,3	µs
Clock frequency		f_{CL}	–	–	100	kHz
Pulse duration LOW		t_{LOW}	4,7	–	–	µs
Pulse duration HIGH		t_{HIGH}	4,0	–	–	µs



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

APPLICATION INFORMATION

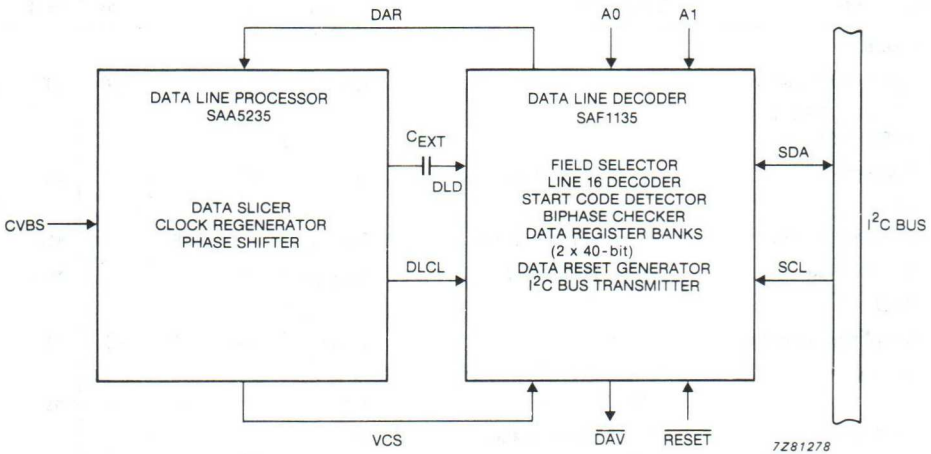


Fig. 9 Data line receiver.

SOUND I.F. AMPLIFIER/DEMODULATOR FOR TV

The TBA120U is an i.f. amplifier with a symmetrical FM demodulator and an a.f. amplifier with adjustable output voltage. The a.f. amplifier is also provided with an output for volume control and an input for VCR operation.

The input and output of the TBA120U are especially designed for LC-circuits, but the input can also be used with a ceramic filter.

QUICK REFERENCE DATA

Supply voltage (pin 11)	V_P	typ.	12 V
Supply current	I_P	typ.	13,5 mA
I.F. voltage gain at f = 5,5 MHz	$G_{v\ if}$	typ.	68 dB
Input voltage starting limiting	V_i	typ.	30 μV
AM suppression at $\Delta f = \pm 50$ kHz	α	typ.	60 dB
A.F. output voltage adjustment range (pin 8)	$\Delta V_{o\ af}$	typ.	85 dB
A.F. output voltage at $\Delta f = \pm 50$ kHz (r.m.s. value)			
at pin 8	$V_{o\ af(rms)}$	typ.	1,2 V
at pin 12	$V_{o\ af(rms)}$	typ.	1,0 V

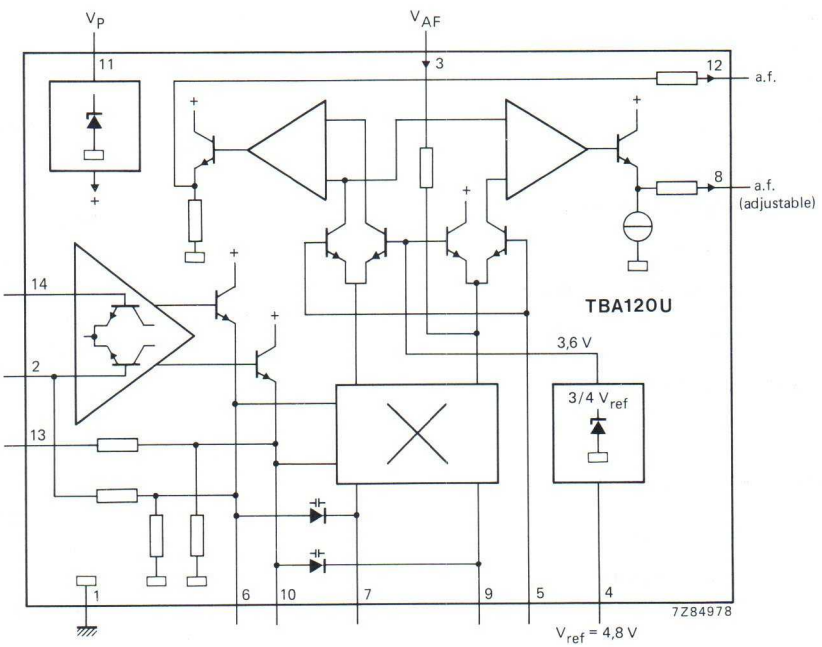


Fig. 1 Block diagram.

PACKAGE OUTLINE

14-lead DIL; plastic (SOT27).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	$V_P = V_{11-1}$	max.	18 V*
Adjustment voltage (pin 5)	V_{5-1}	max.	6 V
Total power dissipation	P_{tot}	max.	400 mW
By-pass resistance	R_{13-14}	max.	1 kΩ
Storage temperature range	T_{stg}		−40 to + 125 °C
Operating ambient temperature range	T_{amb}		0 to + 70 °C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; f = 5,5 MHz

I.F. voltage gain	$G_{v\ if\ 6-14}$	typ.	68 dB
Input voltage starting limiting at Δf = ± 50 kHz; f_m = 1 kHz	V_i	typ. <	30 μV 60 μV
I.F. output voltage at limiting (peak-to-peak value)	$V_{o\ if\ (p-p)}$	typ.	250 mV
AM suppression at Δf = ± 50 kHz; V_i = 500 μV; f_m = 1 kHz; m = 30%	α	> typ.	50 dB 60 dB
I.F. residual voltage without de-emphasis at pin 12	$V_{if\ 12}$	typ.	30 mV
at pin 8	$V_{if\ 8}$	typ.	20 mV
A.F. voltage gain	$G_{v\ af\ 8-3}$	typ.	7,5
A.F. adjustment at R_{4-5} = 5 kΩ; R_{5-1} = 13 kΩ	$\Delta V_{o\ af}$	 typ.	20 to 36 dB 28 dB
A.F. output voltage control range	$\Delta V_{o\ af}$	> typ.	70 dB 85 dB
Adjustment resistor**	R_{4-5}		1 to 10 kΩ
D.C. voltage portion at the a.f. outputs pin 12	V_{12-1}	typ.	5,6 V
pin 8	V_{8-1}	typ.	4,0 V
Output resistance of the a.f. outputs pin 12	$R_{o\ 12-1}$	typ.	1,1 kΩ
pin 8	$R_{o\ 8-1}$	typ.	1,1 kΩ
Input resistance of the a.f. input	$R_{i\ 3-1}$	typ.	2 kΩ
Stabilized reference voltage	$V_{4-1} = V_{ref}$	 typ.	4,2 to 5,3 V 4,8 V
Source resistance of reference voltage source	R_{4-1}	typ.	12 Ω

* Supply voltage operating range is 10 to 18 V.

** Pin 5 must be connected to pin 4, when volume control adjustment is not applicable.

Hum suppression			
at pin 12	V_{12}/V_{11}	typ.	30 dB
at pin 8	V_8/V_{11}	typ.	35 dB
Supply current (pin 11)	$I_P = I_{11}$		9,5 to 17,5 mA
		typ.	13,5 mA
I.F. input impedance	$\|Z_i\|$	typ.	40 kΩ/4,5 pF
		>	15 kΩ/< 6 pF
A.F. output voltage at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $V_i = 10$ mV; $Q_o = 45$; r.m.s. value			
at pin 12	$V_{o\,af\,(rms)}$	typ.	1,0 V
at pin 8	$V_{o\,af\,(rms)}$	typ.	1,2 V
Distortion at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $V_i = 10$ mV; $Q_o = 20$	d_{tot}	typ.	1 %

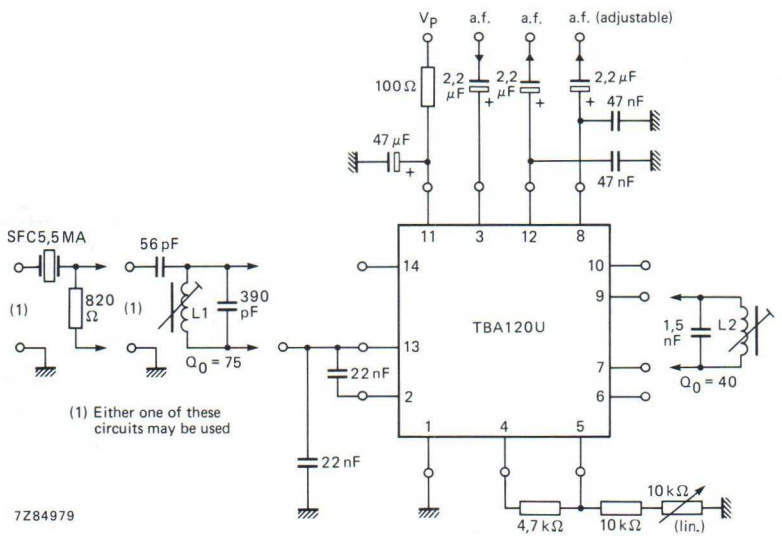


Fig. 2 Application example using TBA120U.

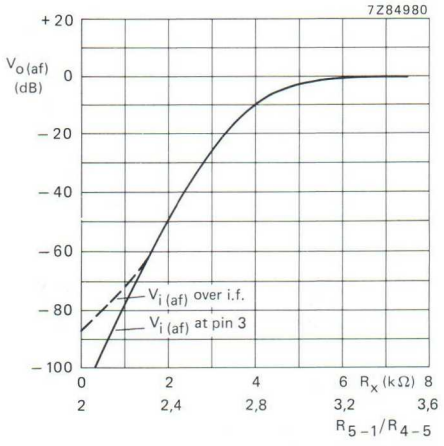


Fig. 3 The a.f. output voltage at pin 8 as a function of the resistance values as shown in Fig. 4.

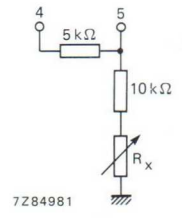
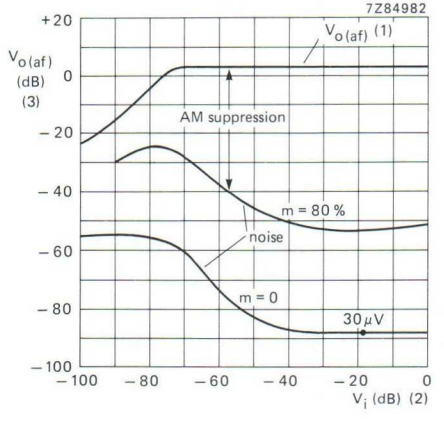


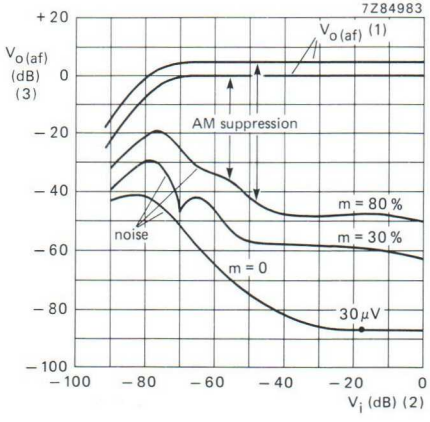
Fig. 4 Resistor conditions for curves in Fig. 3.



(1) $V_{o\,af}$ with de-emphasis at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $d_{tot} = 1{,}5\%$; 0 dB ≙ 770 mV.

(2) V_i: 0 dB ≙ 200 mV at 60 Ω.

Fig. 5 The a.f. output voltage at pin 8 as a function of the input voltage with SFC 5,5 MA at the input (see Fig. 2).



(1) $V_{o\,af}$ with de-emphasis at $f_m = 1$ kHz; 0 dB ≙ 770 mV;
curve a: $\Delta f = \pm 50$ kHz; $d_{tot} = 3\%$;
curve b: $\Delta f = \pm 25$ kHz; $d_{tot} = 1\%$.

(2) V_i: 0 dB ≙ 200 mV at pin 14.

Fig. 6 The a.f. output voltage at pin 8 as a function of the input voltage with broadband input (60 Ω).

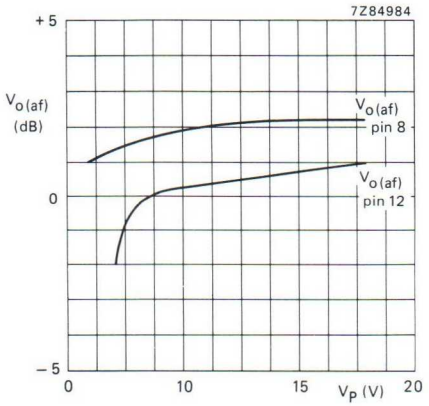


Fig. 7 The a.f. output voltages at pins 8 and 1 as a function of the supply voltage; 0 dB ≙ 770 mV.

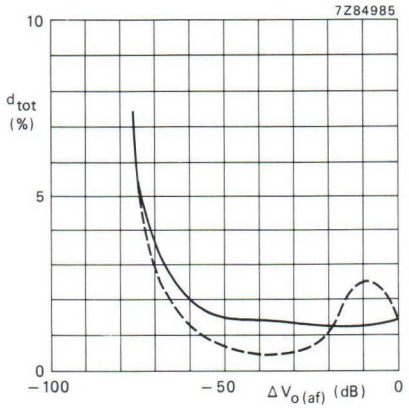


Fig. 8 Total distortion as a function of the a.f. output voltage change.
——— 0 dB ≙ 900 mV over i.f. (pin 8)
– – – – 0 dB ≙ 1,15 V (pin 8)

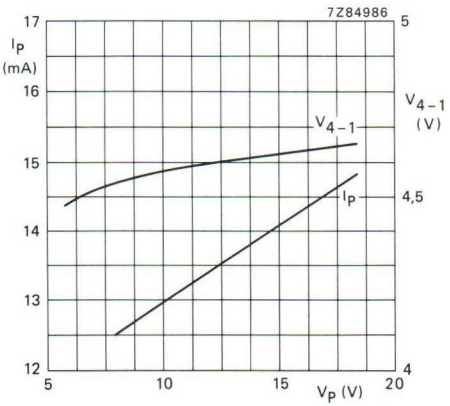


Fig. 9 Supply current and the reference voltage at pin 4 as a function of supply voltage.

4 W AUDIO POWER AMPLIFIER WITH DC VOLUME CONTROL

GENERAL DESCRIPTION

The TDA1013B is an integrated audio amplifier circuit with DC volume control, encapsulated in a 9-lead single in-line (SIL) plastic package. The wide supply voltage range makes this circuit ideal for applications in mains and battery-fed apparatus such as television receivers and record players.

The DC volume control stage has a logarithmic control characteristic with a range of more than 80 dB; control is by means of a DC voltage variable between 2 and 6.5 V.

The audio amplifier has a well defined open loop gain and a fixed integrated closed loop. This device requires only a few external components and offers stability and performance.

Features

- Few external components
- Wide supply voltage range
- Wide control range
- Pin compatible with TDA1013A
- Fixed gain
- High signal-to-noise ratio
- Thermal protection

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10	18	40	V
Repetitive peak output current		I_{ORM}	–	–	1.5	A
Total sensitivity	P_o = 2.5 W; DC control at max. gain	V_i	44	55	69	mV
Audio amplifier						
Output power	THD = 10%; R_L = 8 Ω	P_o	4.0	4.2	–	W
Total harmonic distortion	P_o = 2.5 W; R_L = 8 Ω	THD	–	0.15	0.1	%
Sensitivity	P_o = 2.5 W	V_i	100	125	160	mV
DC volume control unit						
Gain control range		$\lvert\Delta G_v\rvert$	80	–	–	dB
Signal handling	THD < 1%; DC control = 0 dB	V_i	1.2	1.7	–	V
Sensitivity (pin 6)	V_o = 125 mV; max. voltage gain	V_i	39	45	55	mV
Input impedance (pin 8)		$\lvert Z_i\rvert$	23	29	35	kΩ

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

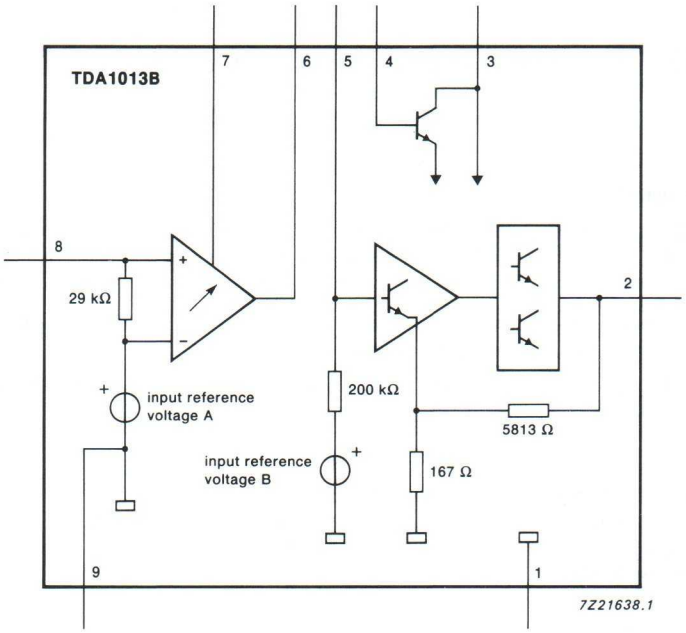


Fig.1 Block diagram.

PINNING

1 power ground
2 amplifier output
3 supply voltage
4 electronic filter
5 amplifier input
6 control unit output
7 control voltage
8 control unit input
9 signal ground (substrate)

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

1 TO 4 W AUDIO POWER AMPLIFIER

The TDA1015 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P	3,6 to 18	V
Peak output current	I_{OM}	max. 2,5	A
Output power at d_{tot} = 10%			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ. 0,3	%
Input impedance			
preamplifier (pin 8)	$\|Z_i\|$	> 100	kΩ
power amplifier (pin 6)	$\|Z_i\|$	typ. 20	kΩ
Total quiescent current	I_{tot}	typ. 14	mA
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Storage temperature	T_{stg}	−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

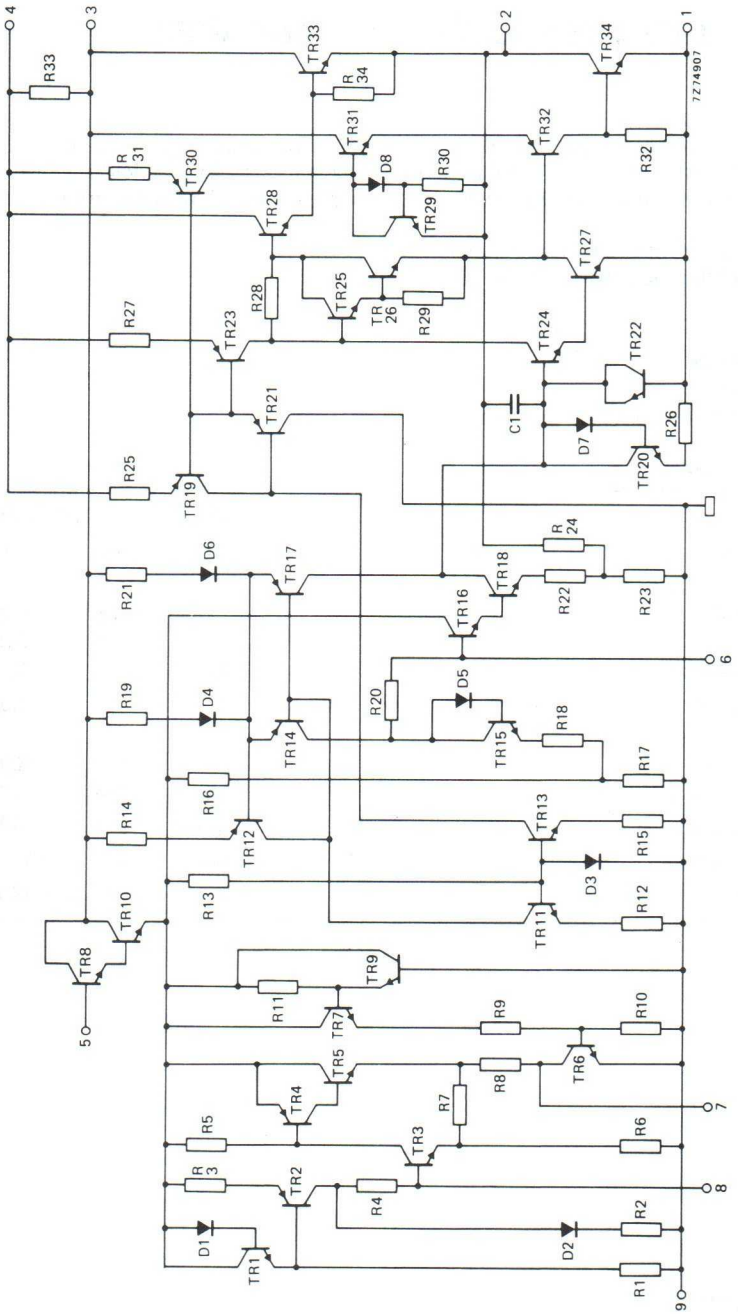


Fig. 1 Circuit diagram.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

0,5 W AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1015T is a low-cost audio amplifier which can deliver up to 0,5 W output power into a 16 Ω load impedance at a supply voltage of 9 V. The amplifier is specially designed for portable applications such as radios and recorders. The IC has a very low supply voltage requirement (3,6 V min.).

Features

- High input impedance
- Separated preamplifier and power amplifier
- Limited noise behaviour at radio frequencies
- Short-circuit protected
- Miniature encapsulation

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 12	V
Peak output current	I_{OM}	max.	1	A
Output power	P_o	typ.	0,5	W
Voltage gain power amplifier	G_{v1}	typ.	29	dB
Voltage gain preamplifier	G_{v2}	typ.	23	dB
Total quiescent current	I_{tot}	max.	22	mA
Operating ambient temperature range	T_{amb}		−25 to +150	°C
Storage temperature range	T_{stg}		−55 to +150	°C

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

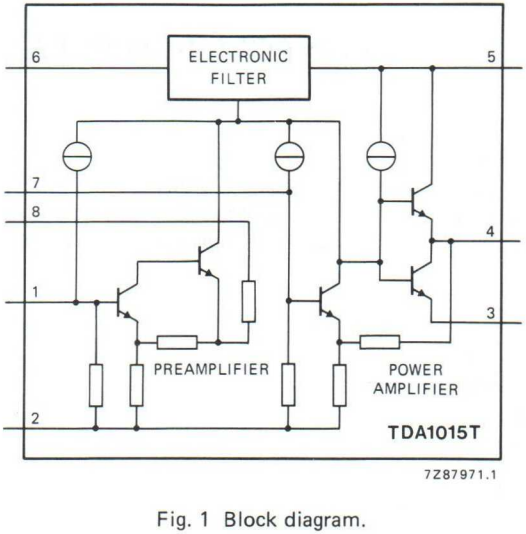


Fig. 1 Block diagram.

Proportional-control triac triggering circuit

TDA1023/T

FEATURES

- Adjustable width of proportional range
- Adjustable hysteresis
- Adjustable width of trigger pulse
- Adjustable repetition timing of firing burst
- Control range translation facility
- Fail safe operation
- Supplied from the mains
- Provides supply for external temperature bridge

APPLICATIONS

- Panel heaters
- Temperature control

GENERAL DESCRIPTION

The TDA1023 is a bipolar integrated circuit for controlling triacs in a proportional time or burst firing mode. Permitting precise temperature control of heating equipment it is especially suited to the control of panel heaters. It generates positive-going trigger pulses but complies with regulations regarding mains waveform distortion and RF interference.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage (derived from mains voltage)	-	13.7	-	V
V_Z	stabilized supply voltage for temperature bridge	-	8	-	V
$I_{16(AV)}$	supply current (average value)	-	10	-	mA
t_w	trigger pulse width	-	200	-	µs
T_b	firing burst repetition time at C_T = 68 µF	-	41	-	s
$-I_{OH}$*	output current	-	-	150	mA
T_{amb}	operating ambient temperature range	−20	-	+75	°C

Note

*Negative current is defined as conventional current flow out of a device. A negative output current is suited for positive triac triggering.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1023	16	DIL	plastic	SOT38
TDA1023T	16	mini-pack	plastic	SO16; SOT109A

Proportional-control triac triggering circuit

TDA1023/T

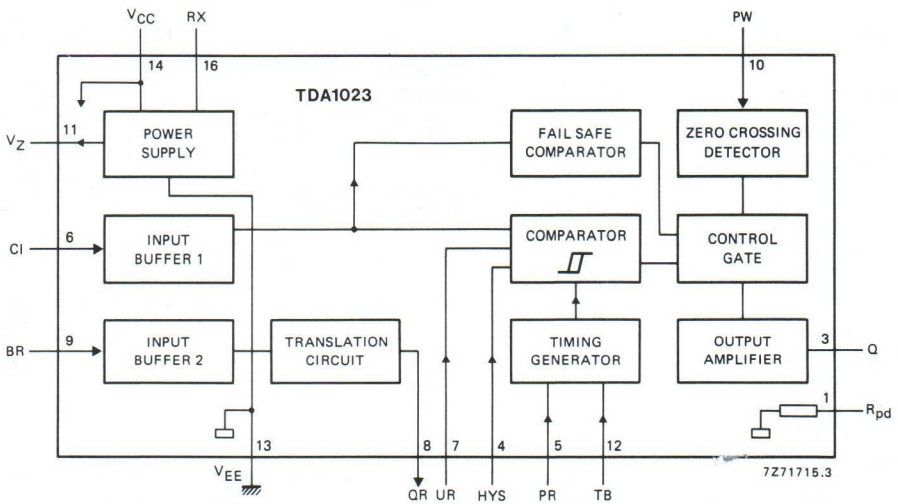


Fig.1 Block diagram.

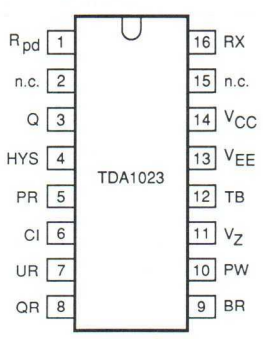


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
R_{pd}	1	internal pull-down resistor
n.c.	2	not connected
Q	3	output
HYS	4	hysteresis control input
PR	5	proportional range control input
CI	6	control input
UR	7	unbuffered reference input
QR	8	output of reference buffer
BR	9	buffered reference input
PW	10	pulse width control input
V_Z	11	reference supply output
TB	12	firing burst repetition time control input
V_{EE}	13	ground
V_{CC}	14	positive supply
n.c.	15	not connected
RX	16	external resistor connection

FUNCTIONAL DESCRIPTION

The TDA1023 generates pulses to trigger a triac. These pulses coincide with the zero excursions of the mains voltage, thus minimizing RF interference and mains supply transients. In order to gate the load on and off, the trigger pulses occur in bursts thus further reducing mains supply pollution. The average power in the load is varied by modifying the duration of the trigger pulse burst in accordance with the voltage difference between the control input CI and the reference input, either UR or BR.

Power supply: V_{CC}, RX and V_z (pins 14, 16 and 11)

The TDA1023 is supplied from the AC mains via a resistor R_D to the RX connection (pin 16); the V_{EE} connection (pin 13) is linked to the neutral line (see Fig.4a). A smoothing capacitor C_S should be coupled between the V_{CC} and V_{EE} connections.

A rectifier diode is included between the RX and V_{CC} connections whilst the DC supply voltage is limited by a chain of stabilizer diodes between the RX and V_{EE} connections (see Fig.3).

A stabilized reference voltage (V_Z) is available at pin 11 to power an external temperature sensing bridge.

Supply operation

During the positive mains half-cycles the current through the external voltage dropping resistor R_D charges the external smoothing capacitor C_S until RX attains the stabilizing potential of the internal stabilizing diodes. R_D should be selected to be capable of supplying the current I_{CC} for the TDA1023, the average output current $I_{3(AV)}$, recharge the smoothing capacitor C_S and provide the supply for an external temperature bridge. (see Figs 9 to 12). Any excess current is by-passed by the internal stabilizer diodes. The maximum rated supply current, however, must not be exceeded.

During the negative mains half-cycles external smoothing capacitor C_S supplies the sum of the current demand described above. Its capacitance must be sufficiently high to maintain the supply voltage above the specified minimum.

Dissipation in resistor R_D is halved by connecting a diode in series (see Fig.4b and 9 to 12). A further reduction in dissipation is possible by using a high quality dropping capacitor C_D in series with a resistor R_{SD} (see Figs 4c and 14). Protection of the TDA1023 and the triac against mains-borne transients can be provided by connecting a suitable VDR across the mains input.

Control and reference inputs CI, BR and UR (pins 6, 9 and 7)

For the control of room temperature (5 °C to 30 °C) optimum performance is obtained by using the translation circuit. The buffered reference input BR (pin 9) is used as a reference input whilst the output reference buffer QR (pin 8) is connected to the unbuffered reference input UR (pin 7). This ensures that the range of room temperature is encompassed in most of the rotation of the potentiometer to give a linear temperature scale with accurate setting.

Should the translation circuit not be required, the unbuffered reference input UR (pin 7) is used as a reference input. The buffered reference input BR (pin 9) must then be connected to the reference supply output V_Z (pin 11).

For proportional power control the unbuffered reference input UR (pin 7) must be connected to the firing burst repetition time control input TB (pin 12).The buffered reference input BR (pin 9), which is in this instance inactive, must then be connected to the reference supply output V_Z (pin 11).

Proportional range control input PR (pin 5)

The output duty factor changes from 0% to 100% by a variation of 80 mV at the control input CI (pin 6) with the proportional range control input PR open. For temperature control this corresponds to a temperature difference of 1 K.

By connecting the proportional range control input PR (pin 5) to ground the range may be increased to 400 mV, i.e. 5 K. Intermediate values may be obtained by connecting the PR input to ground via a resistor R5 (see Table 1).

Hysteresis control input HYS (pin 4)

With the hysteresis control input HYS (pin 4) open, the device has a built-in hysteresis of 20 mV. For temperature control this corresponds with 0.25 K.

Hysteresis is increased to 320 mV, corresponding to 4 K, by grounding HYS (pin 4). Intermediate values are obtained by connecting pin 4 via resistor R4 to ground. Table 1 provides a set of values for R4 and R5 giving a fixed ratio between hysteresis and proportional range.

Trigger pulse width control input PW (pin 10)

The width of the trigger pulse may be adjusted to the value required for the triac by choosing the value of the external synchronization resistor

R_S between the trigger pulse width control input PW (pin 10) and the AC mains. The pulse width is inversely proportional to the input current (see Fig.13).

Output Q (pin 3)

Since the circuit has an open-emitter output it is capable of sourcing current. It is thus suited for generating positive-going trigger pulses. The output is current-limited and short-circuit protected. The maximum output current is 150 mA and the output pulses are stabilized at 10 V for output currents up to that value.

To minimize the total supply current and power dissipation, a gate resistor R_G must be connected between the output Q and the triac gate to limit the output current to the minimum required by the triac (see Figs 5 to 8).

Pull-down resistor R_{pd} (pin 1)

The TDA1023 includes a 1.75 kΩ pull-down resistor R_{pd} between pins 1 and 13 (V_{EE}, ground connection) intended for use with sensitive triacs.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage	-	16	V
Supply current				
$I_{16(AV)}$	average	-	30	mA
$I_{16(RM)}$	repetitive peak	-	100	mA
$I_{16(SM)}$	non-repetitive peak (tp < 50 μs)	-	2	A
V_I	input voltage, all inputs	-	16	V
$I_{6, 7, 9, 10}$	input current	-	10	mA
V_1	voltage on R_{pd} connection	-	16	V
$V_{3, 8, 11}$	output voltage, Q, QR, V_Z	-	16	V
Output current				
$-I_{OH(AV)}$	average	-	30	mA
$-I_{OH(M)}$	peak max. 300 μs	-	700	mA
P_{tot}	total power dissipation	-	500	mW
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−20	+75	°C

CHARACTERISTICS

V_{CC} = 11 to 16 V; T_{amb} = −20 to +75 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	internally stabilized supply voltage at I_{16} = 10mA		12	13.7	15	V
$\Delta V_{CC}/\Delta I_{16}$	variation with I_{16}		-	30	-	mV/mA
I_{16}	supply current at V_{16-13} = 11 to 16 V I_{10} = 1mA; f = 50 Hz; pin 11 open; $V_{6-13} > V_{7-13}$	pins 4 and 5 open	-	-	6	mA
		pins 4 and 5 grounded	-	-	7.1	mA
Reference supply output V_z (pin 11) for external temperature bridge						
V_{11-13}	output voltage		-	8	-	V
$-I_{11}$	output current		-	-	1	mA
Control and reference inputs CI, BR and UR (pins 6, 9 and 7)						
V_{6-13}	input voltage to inhibit the output		-	7.6	-	V
$I_{6, 7, 9}$	input current	V_1 = 4 V	-	-	2	µA
Hysteresis control input HYS (pin 4)						
ΔV_6	hysteresis	pin 4 open	9	20	40	mV
ΔV_6	hysteresis	pin 4 grounded	-	320	-	mV
Proportional control range input PR (pin 5)						
ΔV_6	proportional range	pin 5 open	50	80	130	mV
ΔV_6	proportional range	pin 5 grounded	-	400	-	mV
Pulse width control input PW (pin 10)						
t_w	pulse width	$I_{10(RMS)}$ = 1mA; f = 50 Hz	100	200	300	µs
Firing burst repetition time control input TB (pin 12)						
T_bC_T	firing burst repetition time, ratio to capacitor C_T		320	600	960	ms/µF
Output of reference buffer QR (pin 8)						
	output voltage at input voltage:					
V_{8-13}		V_{9-13} = 1.6 V	-	3.2	-	V
V_{8-13}		V_{9-13} = 4.8 V	-	4.8	-	V
V_{8-13}		V_{9-13} = 8 V	-	6.4	-	V
Output Q (pin 3)						
V_{OH}	output voltage HIGH	$-I_{OH}$ = 150 mA	10	-	-	V
$-I_{OH}$	output current HIGH		-	-	150	mA
Internal pull-down resistor R_{pd} (pin 1)						
R_{pd}	resistance to V_{EE}		1	1.75	3	kΩ

Table 1 Adjustment of proportional range and hysteresis. Combinations of resistor values giving hysteresis > $^1/_4$ proportional range.

Proportional range	Proportional range resistor	Minimum hysteresis	Maximum hysteresis resistor
	R5		R4
mV	kΩ	mV	kΩ
80	open	20	open
160	3.3	40	9.1
240	1.1	60	4.3
320	0.43	80	2.7
400	0	100	1.8

Table 2 Timing capacitor values C_T

Effective DC value	Marked AC specification		Catalogue number*
µF	µF	V	
68	47	25	2222 016 90129
47	33	40	- - 90131
33	22	25	- 015 90102
22	15	40	- - 90101
15	10	25	- - 90099
10	6.8	40	- - 90098

Note

*Special electrolytic capacitors recommended for use with the TDA1023.

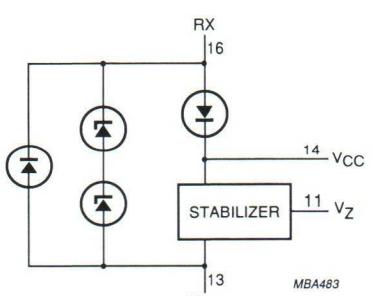
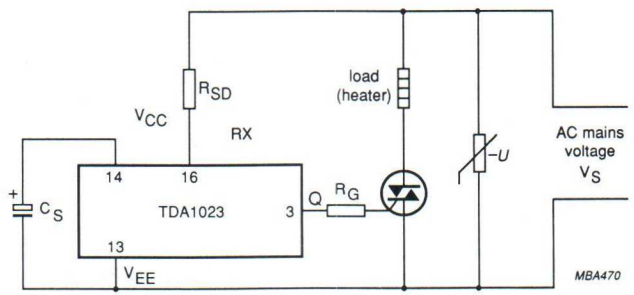
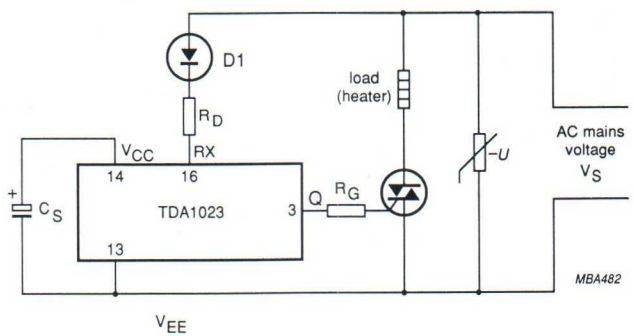


Fig.3 Internal supply connections.





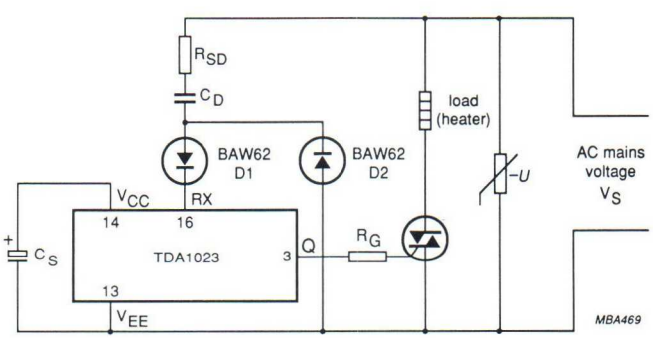


Fig.4 Alternative supply arrangements.

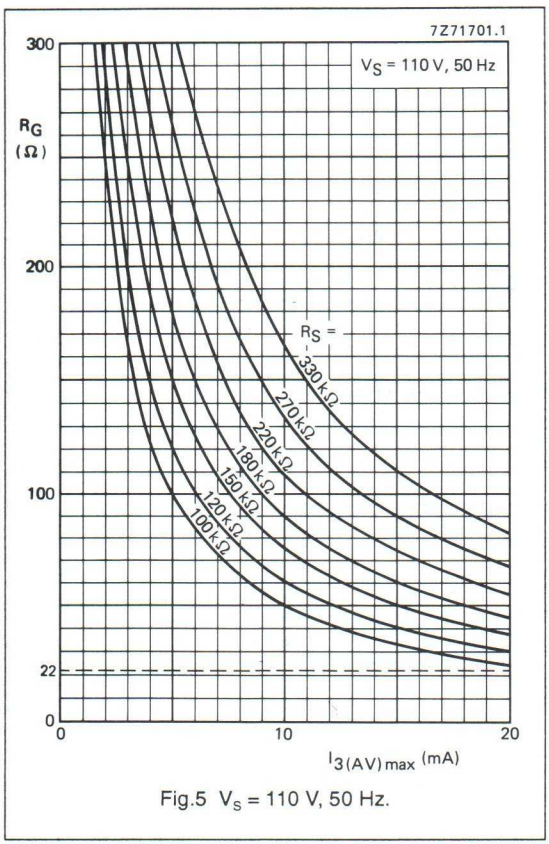


Fig.5 V_S = 110 V, 50 Hz.

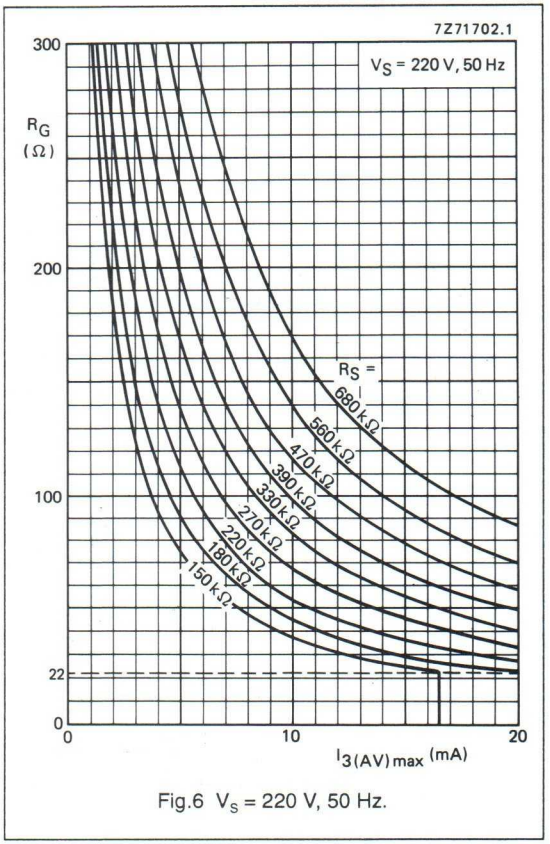


Fig.6 V_S = 220 V, 50 Hz.

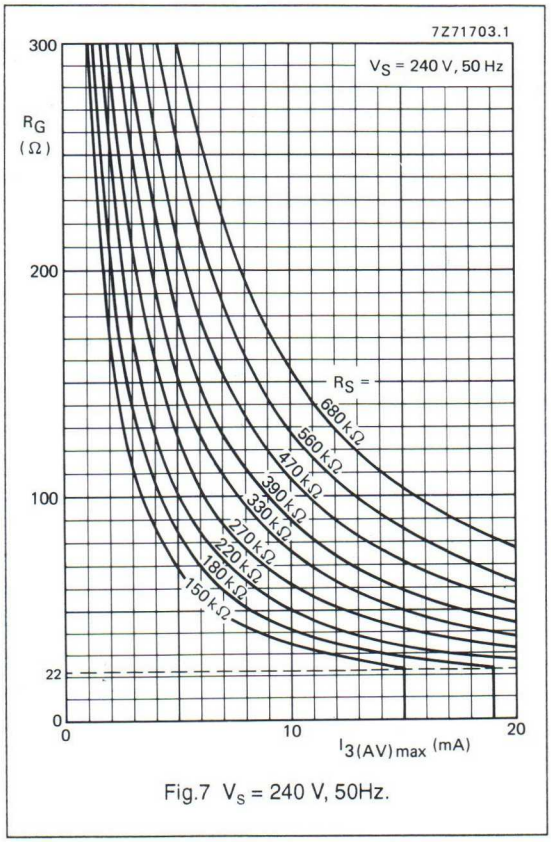


Fig.7 V_S = 240 V, 50Hz.

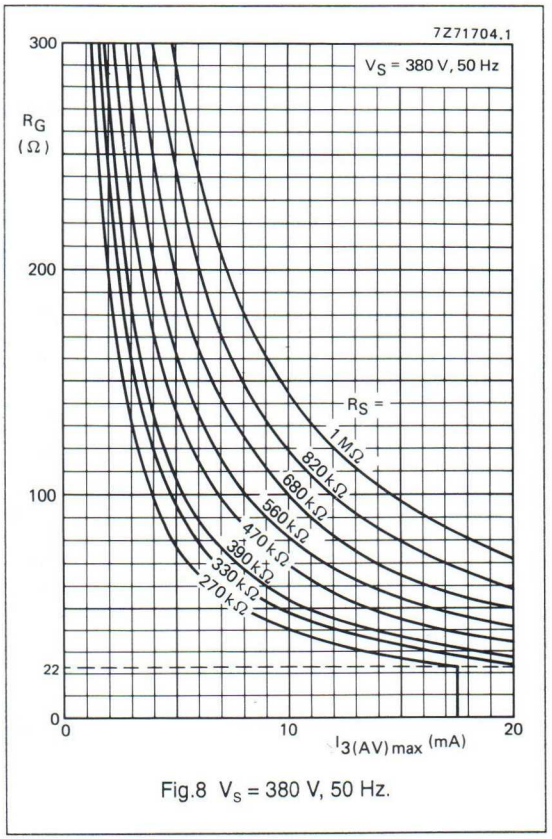


Fig.8 V_S = 380 V, 50 Hz.

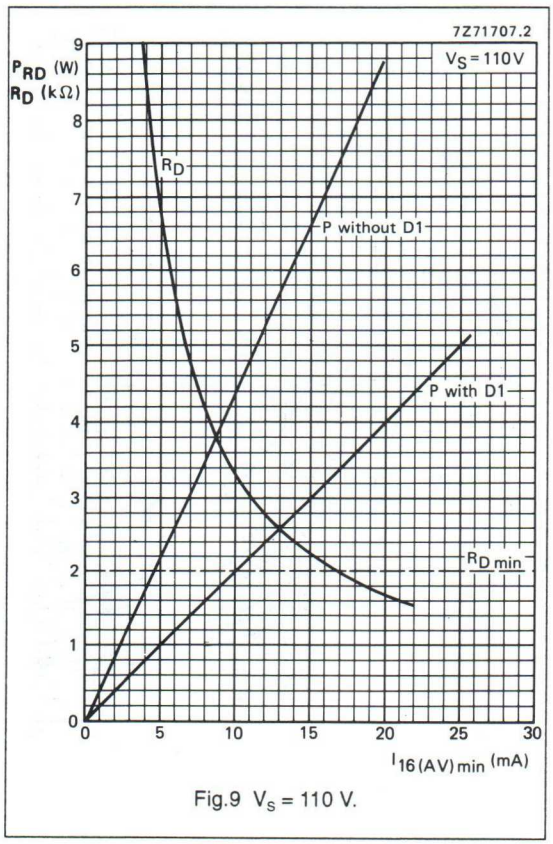


Fig.9 V_S = 110 V.

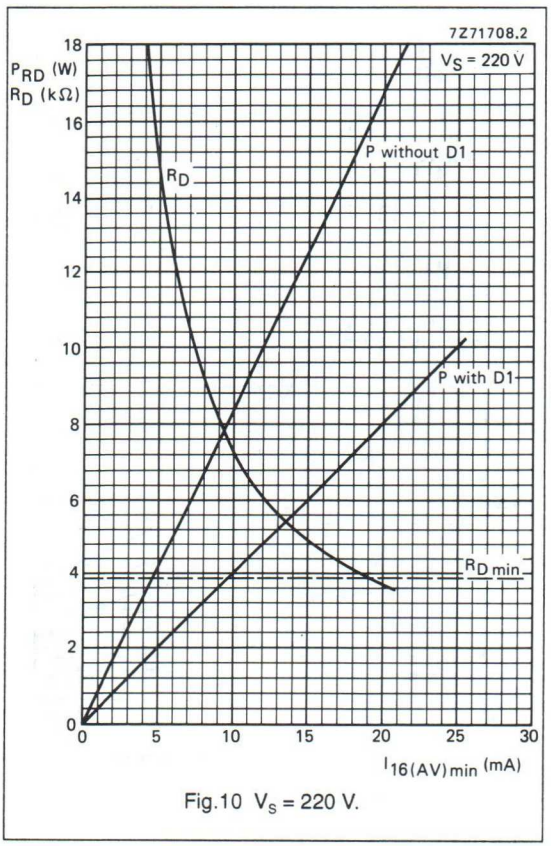


Fig.10 V_S = 220 V.

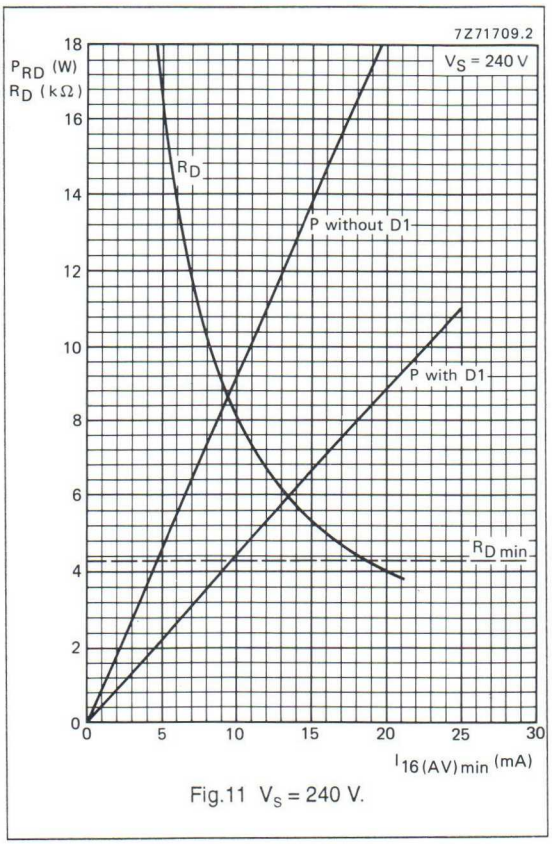


Fig.11 V_S = 240 V.

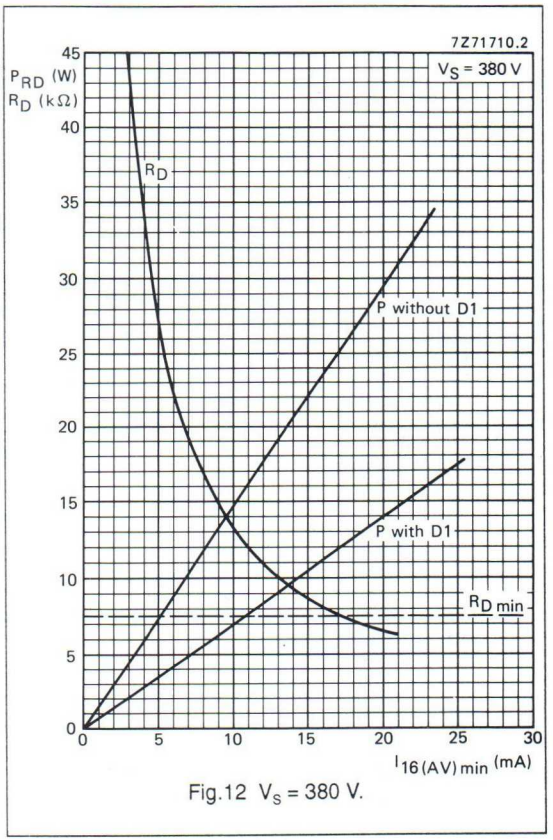


Fig.12 V_S = 380 V.

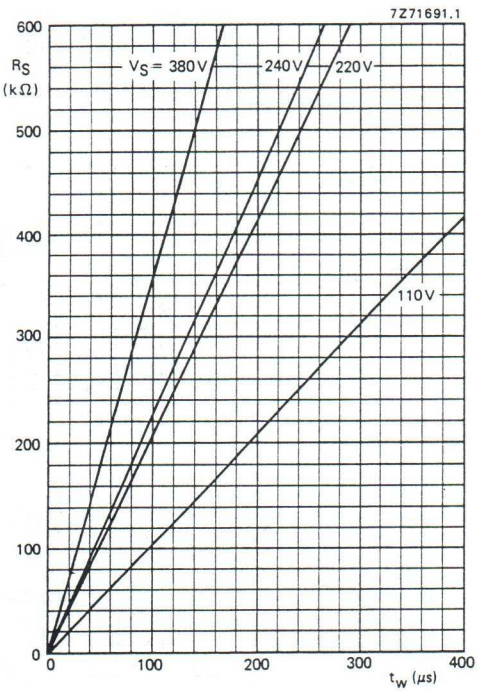


Fig.13 Synchronization resistor R_S as a function of required trigger pulse width t_w with a mains voltage V_S as a parameter.

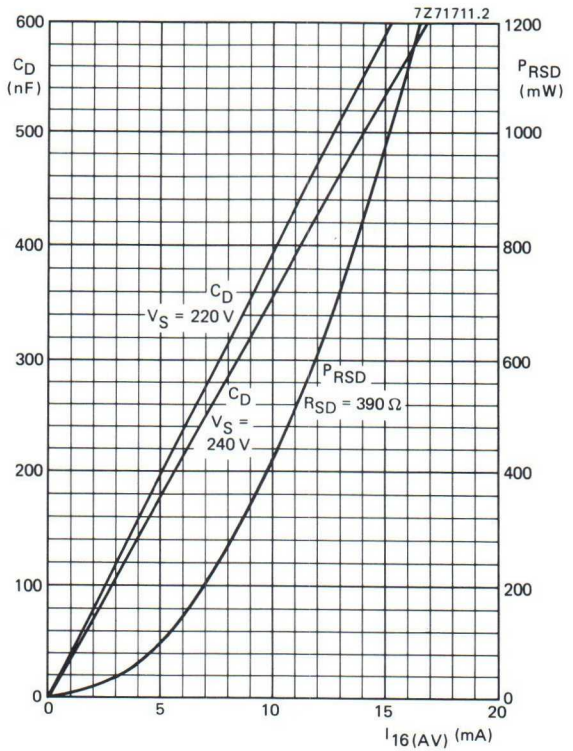
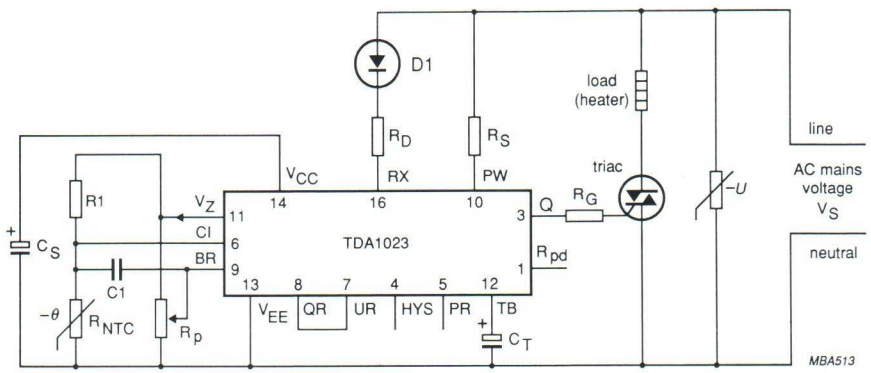


Fig.14 Nominal value of voltage dropping capacitor C_D and power P_{RSD} dissipated in a voltage dropping resistor R_{SD} as a function of average supply current $I_{16\ (AV)}$ with the mains supply voltage V_S as a parameter.



Conditions:- Mains supply; V_S = 220 V; Temperature range = 5 to 30 °C.
BT139 data at T_j = 25 °C; V_{gt} < 1.5 V; I_{gt} > 70 mA; I_L < 60 mA

Fig.15 The TDA1023/T used in a 1200 to 2000 W heater with triac BT139. For component values see Table 3.

Table 3 Temperature controller component values (see Fig. 15).

SYMBOL	PARAMETER	REMARKS	VALUE
t_w	trigger pulse width	see BT139 data sheet	75 µs
R_S	synchronization resistor	see Fig. 13	180 kΩ
R_G	gate resistor	see Fig. 6	110 Ω
$I_{3(AV)}$	max. average gate current	see Fig.8	4.1 mA
R4	hysteresis resistor	see Table 1	n.c.
R5	proportional band resistor	see Table 1	n.c.
$I_{16(AV)}$	min. required supply current		11.1 mA
R_D	mains dropping resistor	see Fig. 10	6.2 kΩ
P_{RD}	power dissipated in R_D	see Fig.10	4.6 W
C_T	timing capacitor (eff. value)	see Table 2	68 µF
VDR	voltage dependent resistor	cat. no. 2322 593 62512	250 V AC
D1	rectifier diode		BYW56
R1	resistor to pin 11	1% tolerance	18.7 kΩ
R_{NTC}	NTC thermistor (at 25 °C)	B = 4200 K cat no. 2322 642 12223	22 kΩ
R_p	potentiometer		22 kΩ
C1	capacitor between pins 6 and 9		47 nF
C_S	smoothing capacitor		220 µF; 16 V
If R_D and D1 are replaced by C_D and R_{SD}			
C_D	mains dropping capacitor		470 nF
R_{SD}	series dropping resistor		390 Ω
P_{RSD}	power dissipated in R_{SD}	see Fig.14	0.6 W
VDR	voltage dependent resistor	cat. no. 2322 594 62512	250 V AC

Notes

1. ON/OFF control: pin 12 connected to pin 13.
2. If translation circuit is not required: slider of R_p to pin 7; pin 8 open; pin 9 connected to pin 11.

SIGNAL-SOURCES SWITCH

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers.

QUICK REFERENCE DATA

Supply voltage range (pin 14)	V_P		6 to 23 V
Operating ambient temperature	T_{amb}		−30 to + 80 °C
Supply voltage (pin 14)	V_P	typ.	20 V
Current consumption	I_{14}	typ.	3,5 mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ.	6 V
Voltage gain	G_v	typ.	1
Total harmonic distortion	d_{tot}	typ.	0,01 %
Crosstalk	α	typ.	70 dB
Signal-to-noise ratio	S/N	typ.	120 dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

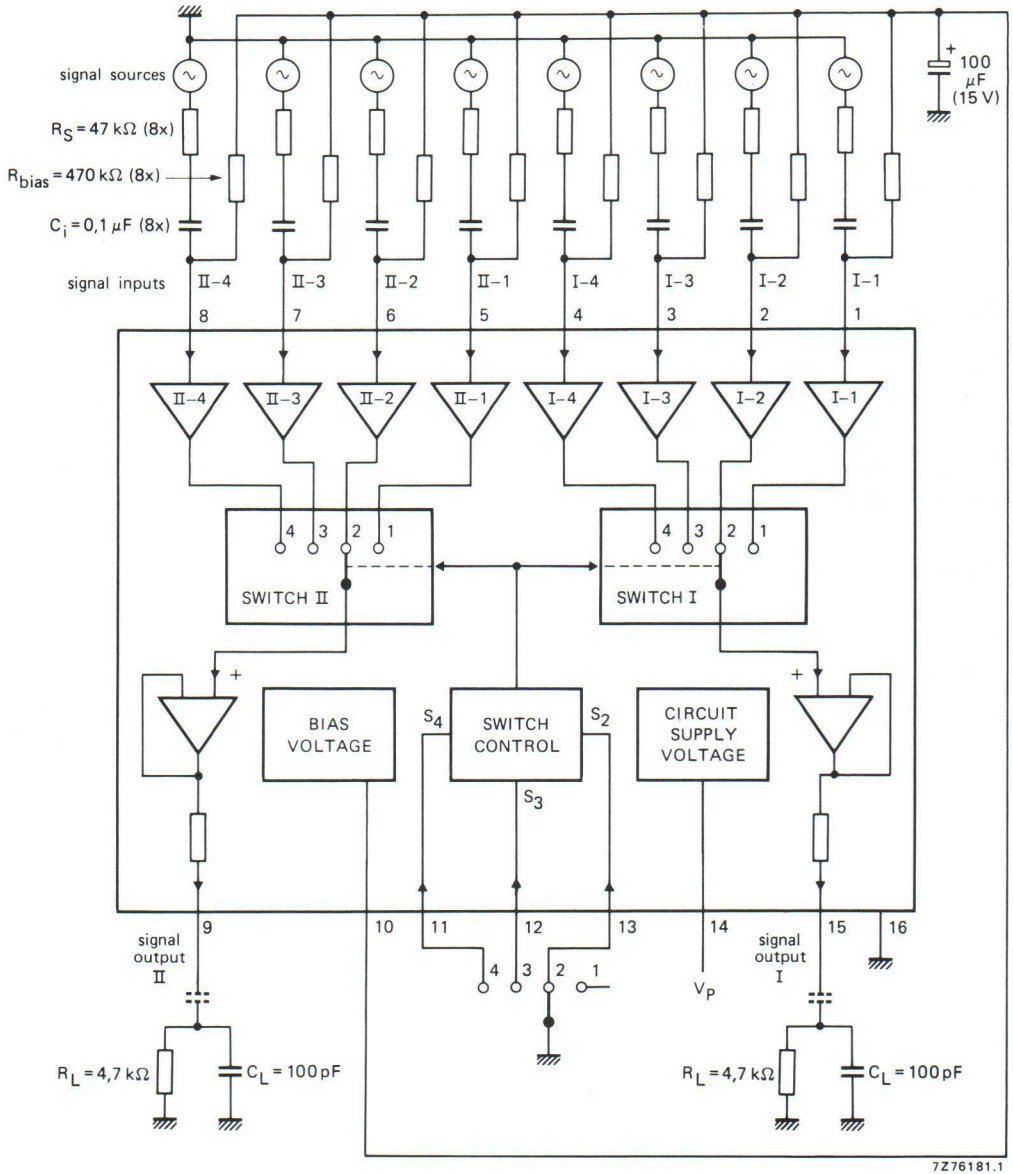


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 14)	V_P	max.	23	V
Input voltage (pins 1 to 8)	V_I	max.	V_P	
	$-V_I$	max.	0,5	V
Switch control voltage (pins 11, 12 and 13)	V_S		0 to 23	V
Input current	$\pm I_I$	max.	20	mA
Switch control current	$-I_S$	max.	50	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 80	°C

CHARACTERISTICS

V_P = 20 V; T_{amb} = 25 °C; unless otherwise specified

Current consumption				
without load; $I_9 = I_{15} = 0$	I_{14}	typ.	3,5	mA
			2 to 5	mA
Supply voltage range (pin 14)	V_P		6 to 23	V
Signal inputs				
Input offset voltage of switched-on inputs				
$R_S \leqslant 1$ kΩ	V_{io}	typ.	2	mV
		<	10	mV
Input offset current of switched-on inputs	I_{io}	typ.	20	nA
		<	200	nA
Input offset current of a switched-on input with respect to a non-switched-on input of a channel	I_{io}	typ.	20	nA
		<	200	nA
Input bias current independent of switch position	I_i	typ.	250	nA
		<	950	nA
Capacitance between adjacent inputs	C	typ.	0,5	pF
D.C. input voltage range	V_I		3 to 19	V
Supply voltage rejection ratio; $R_S \leqslant 10$ kΩ	SVRR	typ.	100	μV/V
Equivalent input noise voltage $R_S = 0$; f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	3,5	μV
Equivalent input noise current f = 20 Hz to 20 kHz (r.m.s. value)	$I_{n(rms)}$	typ.	0,05	nA
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at R_S = 1 kΩ; f = 1 kHz	α	typ.	100	dB

CHARACTERISTICS (continued)

Signal amplifier

Voltage gain of a switched-on input at $I_g = I_{15} = 0$; $R_L = \infty$	G_v	typ.	1
Current gain of a switched-on amplifier	G_i	typ.	10^5

Signal outputs

Output resistance (pins 9 and 15)	R_o	typ.	400 Ω
Output current capability at V_P = 6 to 23 V	$\pm I_g$; $\pm I_{15}$	typ.	5 mA
Frequency limit of the output voltage $V_{i(p-p)}$ = 1 V; R_S = 1 kΩ; R_L = 10 MΩ; C_L = 10 pF	f	typ.	1,3 MHz
Slew rate (unity gain); $\Delta V_{9\text{-}16}/\Delta t$; $\Delta V_{15\text{-}16}/\Delta t$ R_L = 10 MΩ; C_L = 10 pF	S	typ.	2 V/μs

Bias voltage

D.C. output voltage	$V_{10\text{-}16}$	typ. 10,2 to 11,8 V	11 V *
Output resistance	$R_{10\text{-}16}$	typ.	8,2 kΩ

Switch control

switched-on inputs	interconnected pins	control voltages		
		$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
I-1, II-1	1-15, 5-9	H	H	H
I-2, II-2	2-15, 6-9	H	H	L
I-3, II-3	3-15, 7-9	H	L	H
I-4, II-4	4-15, 8-9	L	H	H
I-4, II-4	4-15, 8-9	L	L	H
I-4, II-4	4-15, 8-9	L	H	L
I-4, II-4	4-15, 8-9	L	L	L
I-3, II-3	3-15, 7-9	H	L	L

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at $V_{SL} \leqslant 1{,}5$ V.

Control inputs (pins 11, 12 and 13)

Required voltage			
HIGH	V_{SH}	>	3,3 V **
LOW	V_{SL}	<	2,1 V
Input current			
HIGH (leakage current)	I_{SH}	<	1 μA
LOW (control current)	$-I_{SL}$	<	250 μA

* $V_{10\text{-}16}$ is typically $0{,}5 \cdot V_{14\text{-}16} + 1{,}5 \cdot V_{BE}$.

** Or control inputs open ($R_{11,12,13-16} > 33$ MΩ).

APPLICATION INFORMATION

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 1; R_S = 47 kΩ; C_i = 0,1 μF; R_{bias} = 470 kΩ; R_L = 4,7 kΩ; C_L = 100 pF (unless otherwise specified)

Voltage gain	G_v	typ.	−1,5 dB
Output voltage variation when switching the inputs	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	typ. <	10 mV 100 mV
Total harmonic distortion			
over most of signal range (see Fig. 4)	d_{tot}	typ.	0,01 %
V_i = 5 V; f = 1 kHz	d_{tot}	typ.	0,02 %
V_i = 5 V; f = 20 Hz to 20 kHz	d_{tot}	typ.	0,03 %
Output signal handling			
d_{tot} = 0,1%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	> typ.	5,0 V 5,3 V
Noise output voltage (unweighted)			
f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	5 μV
Noise output voltage (weighted)			
f = 20 Hz to 20 kHz (in accordance with DIN 45405)	V_n	typ.	12 μV
Amplitude response	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	<	0,1 dB *
V_i = 5 V; f = 20 Hz to 20 kHz; C_i = 0,22 μF			
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz	α	typ.	75 dB **
Crosstalk between switched-on inputs and the outputs of the other channels	α	typ.	90 dB **

* The lower cut-off frequency depends on values of R_{bias} and C_i.

** Depends on external circuitry and R_S. The value will be fixed mostly by capacitive crosstalk of the external components.

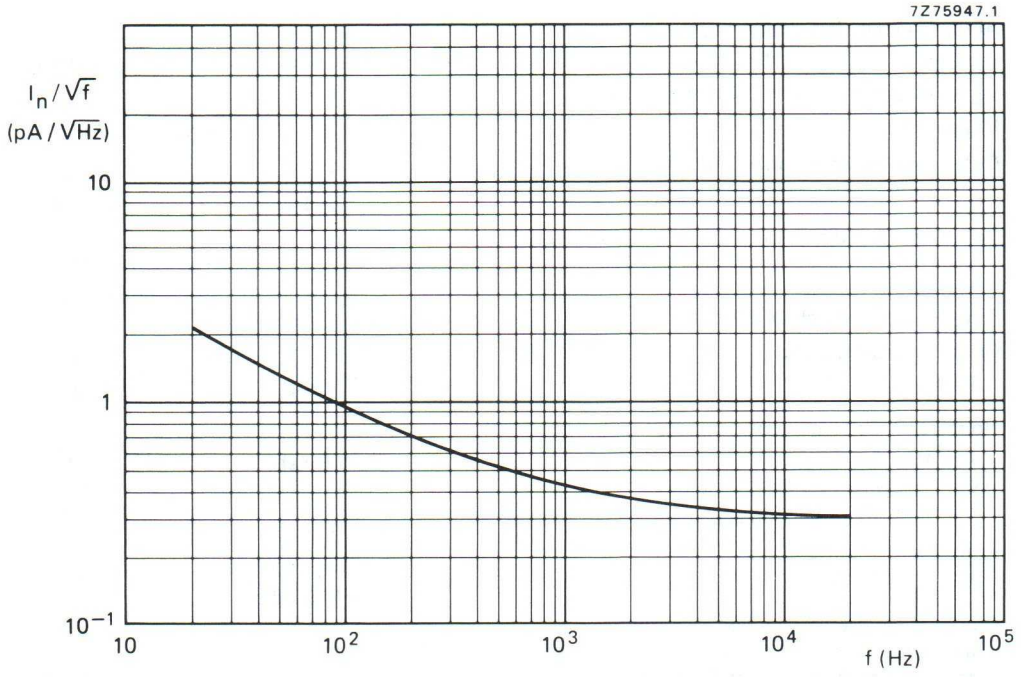


Fig. 2 Equivalent input noise current.

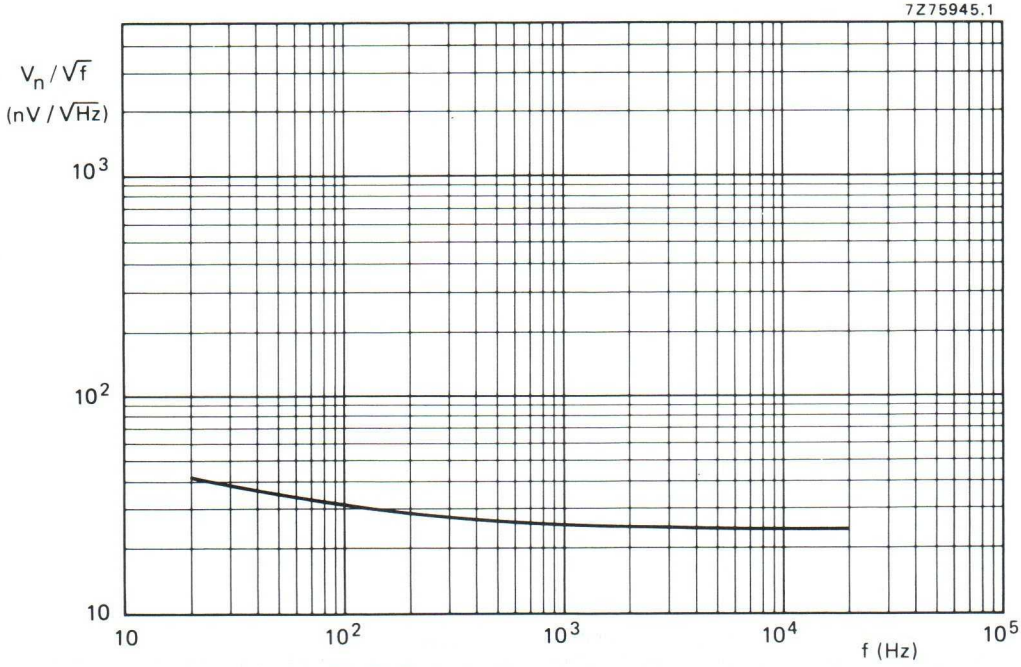


Fig. 3 Equivalent input noise voltage.

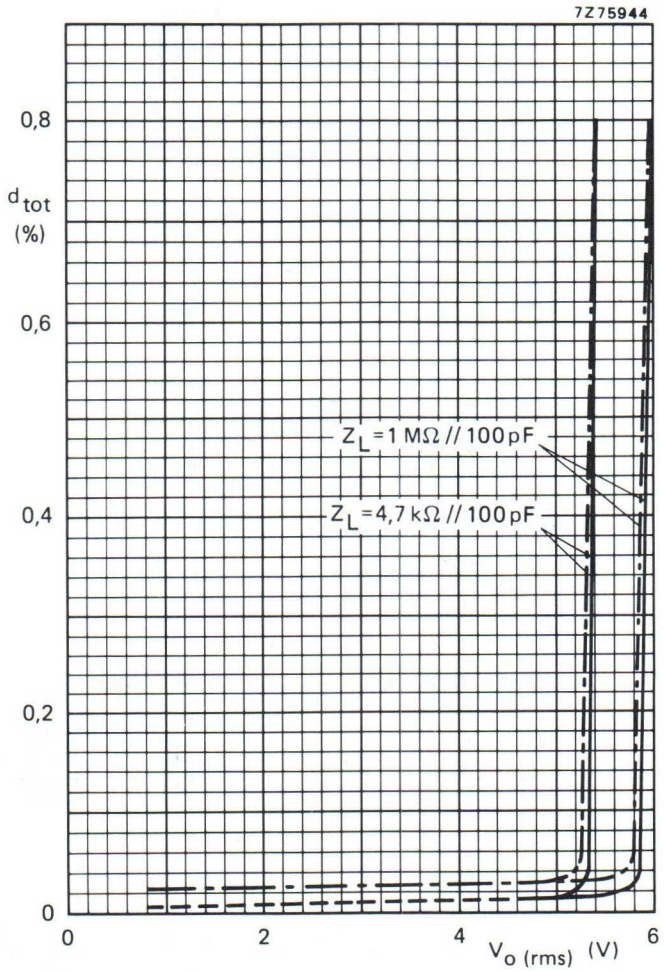


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; — · — · f = 20 kHz.

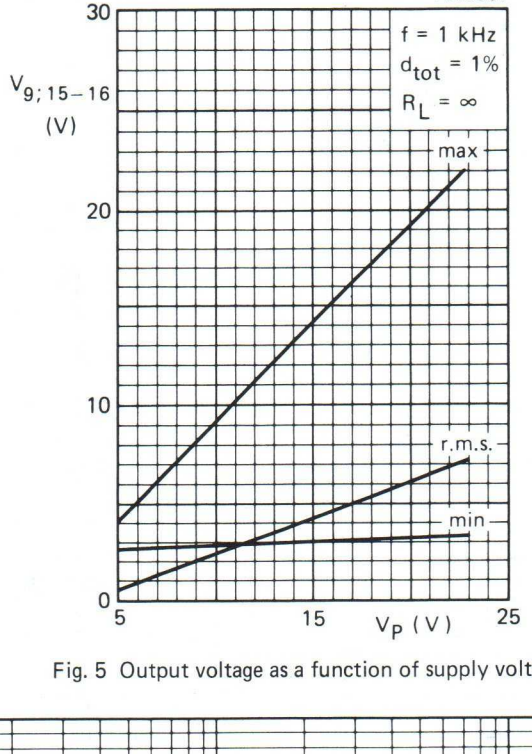


Fig. 5 Output voltage as a function of supply voltage.

Fig. 6 Noise output voltage as a function of input resistance; G_V = 1; f = 20 Hz to 20 kHz.
—— V_n (output); – – – V_n (R_S).

APPLICATION NOTES

Input protection circuit and indication

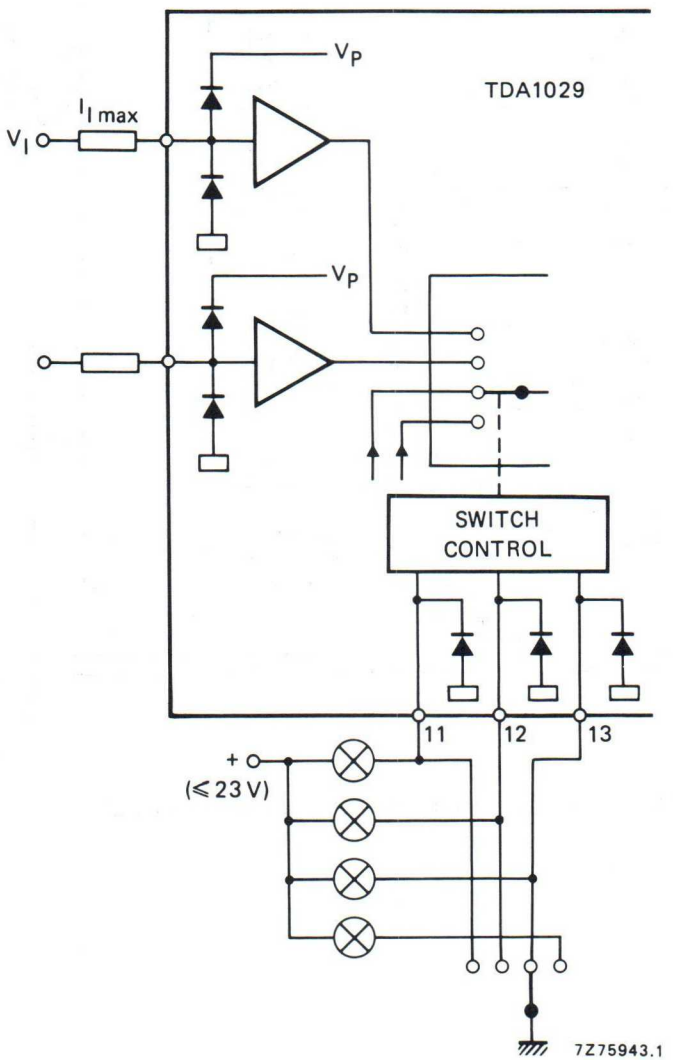


Fig. 7 Circuit diagram showing input protection and indication.

Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range; e.g. unused inputs can be connected directly to pin 10.

Circuits with standby operation

The control inputs (pins 11, 12 and 13) are high-ohmic at $V_{SH} \leqslant 20$ V ($I_{SH} \leqslant 1\ \mu A$), as well as, when the supply voltage (pin 14) is switched off.

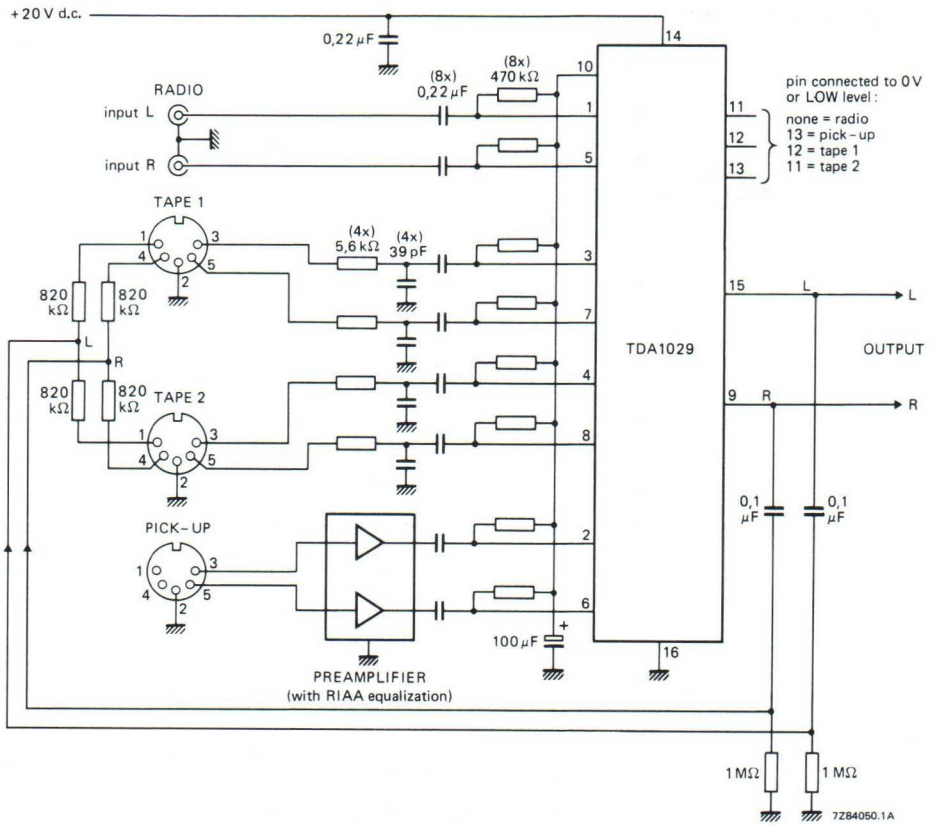


Fig. 8 TDA1029 connected as a four input stereo source selector.

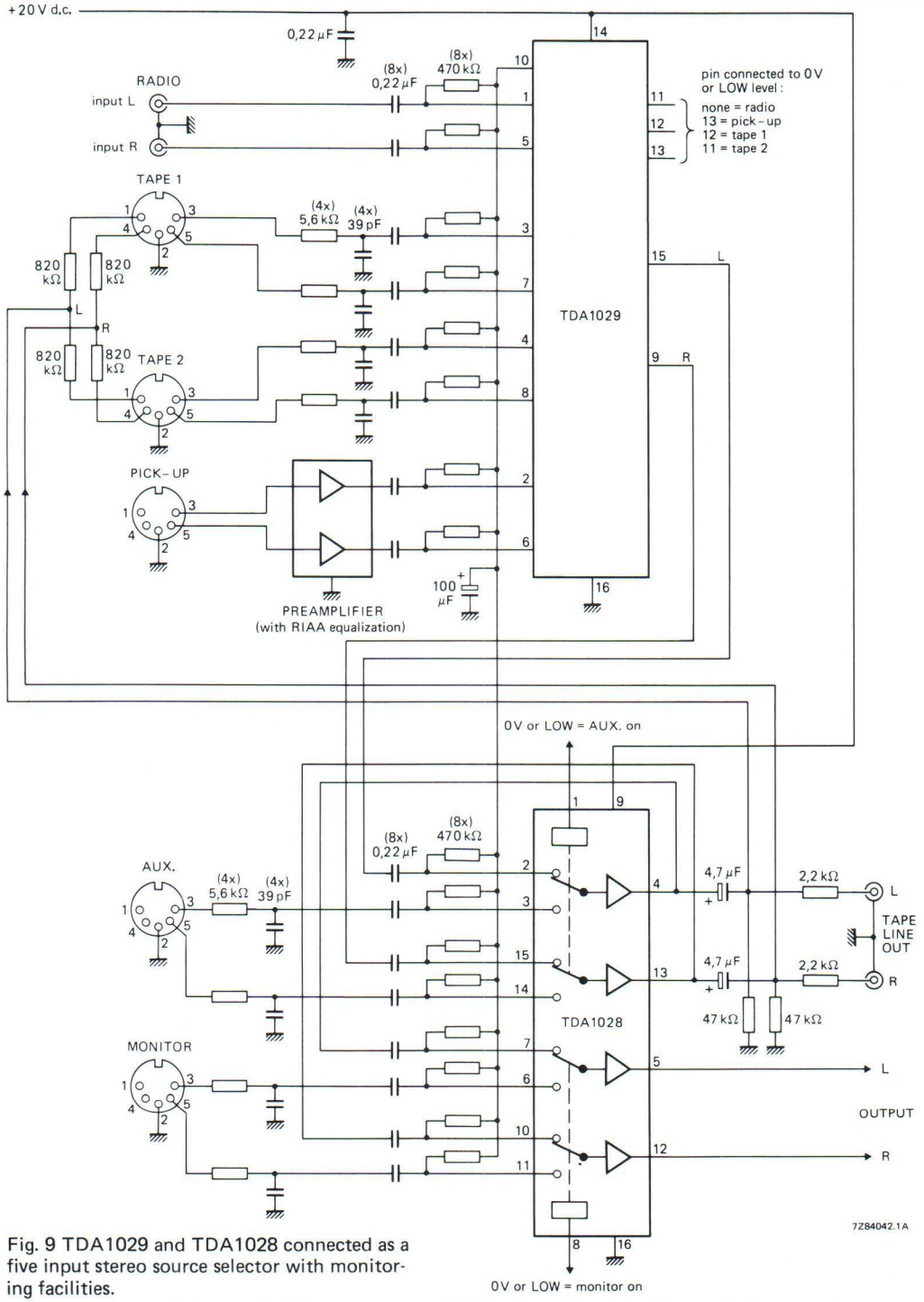


Fig. 9 TDA1029 and TDA1028 connected as a five input stereo source selector with monitoring facilities.

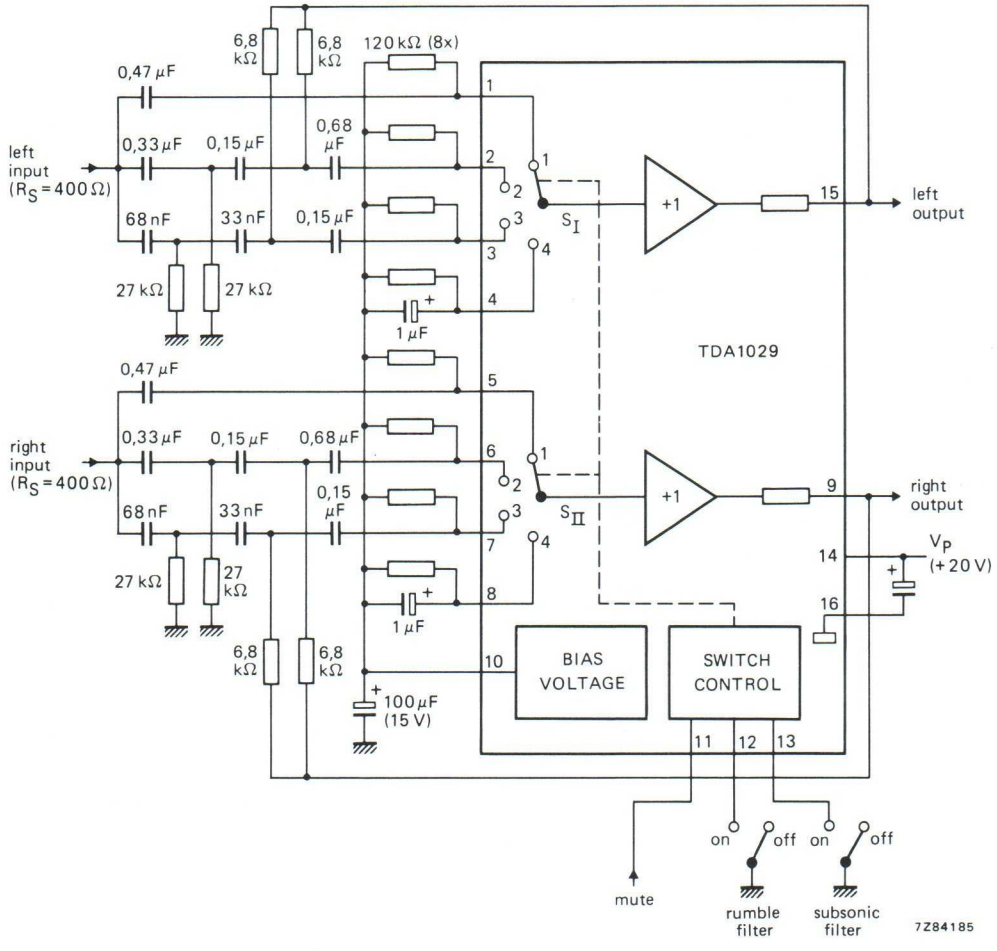


Fig. 10 TDA1029 connected as a third-order active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant. It is a four-function circuit which can select mute, rumble filter, subsonic filter and linear response.

Switch control

function	$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
linear	H	H	H
subsonic filter 'on'	H	H	L
rumble filter 'on'	H	L	X
mute 'on'	L	X	X

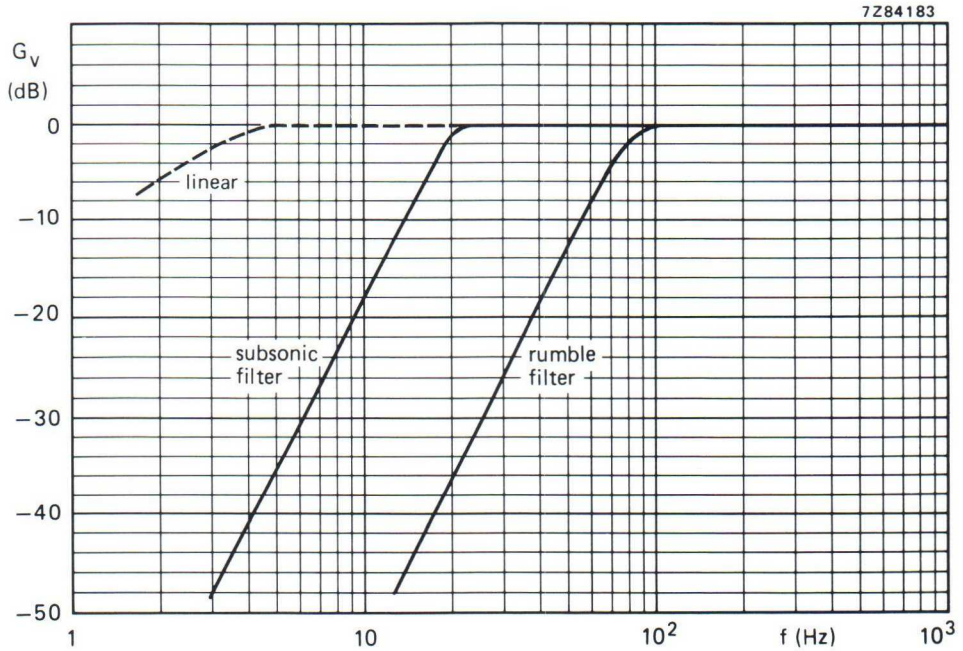


Fig. 11 Frequency response curves for the circuit of Fig. 10.

EAST-WEST CORRECTION DRIVER CIRCUIT

The TDA1082 is a monolithic integrated circuit driving east-west correction of colour tubes in television receivers. The circuit can be used for class-A and class-D operation and incorporates the following functions:

- differential input amplifier
- squaring stage
- differential output amplifier with driver stage
- protection stage with threshold
- switching off the correction during flyback
- voltage stabilizer

QUICK REFERENCE DATA

Supply voltage (pin 1)	V_P	typ.	12 V
Current consumption	I_P	typ.	17 mA
Total power dissipation	P_{tot}	max.	600 mW
Operating ambient temperature range	T_{amb}		0 to + 70 °C
Collector voltage drift external transistor	ΔV_C	typ.	0,7 V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

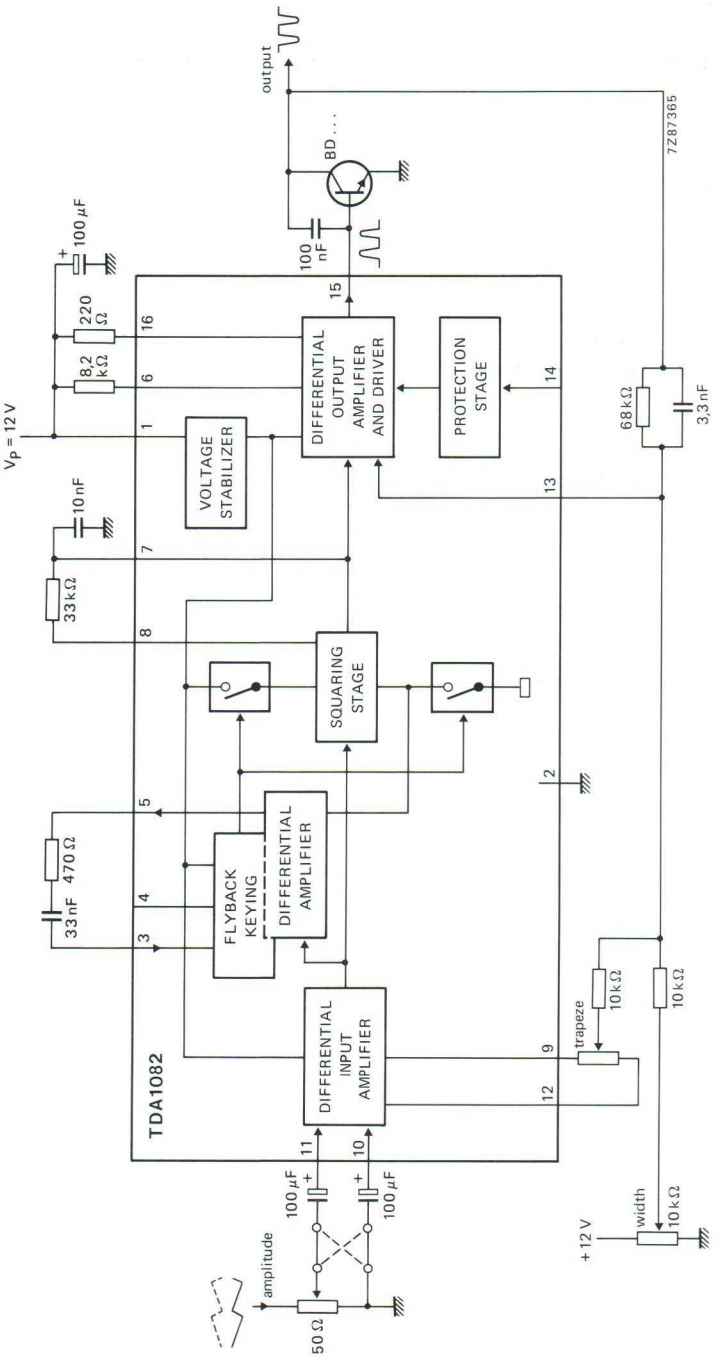


Fig. 1 Block diagram with external components (class-A operation). Also used as test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	V_P	max.	16	V
Output current (pin 15)	$-I_O$	max.	50	mA
Total power dissipation	P_{tot}	max.	600	mW
Storage temperature range	T_{stg}	−25 to +	150	°C
Operating ambient temperature range	T_{amb}	0 to +	70	°C

Voltages

with respect to ground (pin 2)	min.	max.	
Pins 1, 5, 7, 8, 9, 12, 13 and 16	0	16	V
Pins 3 and 4	0	–	V
Pins 10, 11 and 15	0	5	V

Currents

Pins 3, 4 and 6	–	5	mA
Pin 14	0	1,5	mA
Pins 15 and 16 ($-I_{15}$ and $+I_{16}$)	0	50	mA

CHARACTERISTICS

V_P = 12 V (range 10,5 to 14 V); T_{amb} = 25; measured in circuit Fig. 1 with colour tube A66-500X; unless otherwise specified

Supply

Voltage range	V_P	10,5	to	14	V
Voltage peak value	V_{PM}	max.		15	V
Current range	I_P	11	to	30	mA
Current typical value	I_P	typ.		17	mA

Sawtooth signal (pin 10 or 11)

Input voltage d.c. value	V_i	typ.	2,5	V
Input resistance	R_i	typ.	5,6	kΩ
		<	7,0	kΩ

Correcting signals (pin 13)

Input voltage d.c. value	V_{13}	typ.	0,6	V
Input current	I_{13}	typ.	0,5	mA

Flyback keying (pin 3)

Input current range	I_3	0,05	to	5	mA
Peak value, d = 5%	I_3	typ.		20	mA

Threshold (pin 14)

Input voltage at I_{14} = 200 μA for switching off the driver stage	V_i	typ.		8	V
		7,2	to	8,8	V

Output stage (pin 6)			
Generator current	I_6	typ.	1 mA
Flyback differential amplifier (pin 5)			
D.C. value output voltage	V_5	typ.	6 V
Output resistance	R_5	typ.	5,6 kΩ
Squaring stage (pin 7)			
D.C. value output voltage	V_7	typ.	6 V
Peak to peak value output voltage	$V_{7(p\text{-}p)}$	typ.	1,5 V
Output resistance	R_7	5,6 to typ.	9,4 kΩ 7,5 kΩ
Correction trapezoidal deformation (pins 9 and 12)			
D.C. voltage	$V_{9,12}$	typ.	5 V
Output resistance	$R_{9,12}$	typ.	7,5 kΩ
Driver output (pin 15)			
Output current	$-I_{15}$	<	50 mA
Drift of d.c. collector voltage			
Of external transistor in closed loop T_{amb} = 15 to 70 °C; V_{CO} = 8 V	ΔV_C	typ.	0,7 V

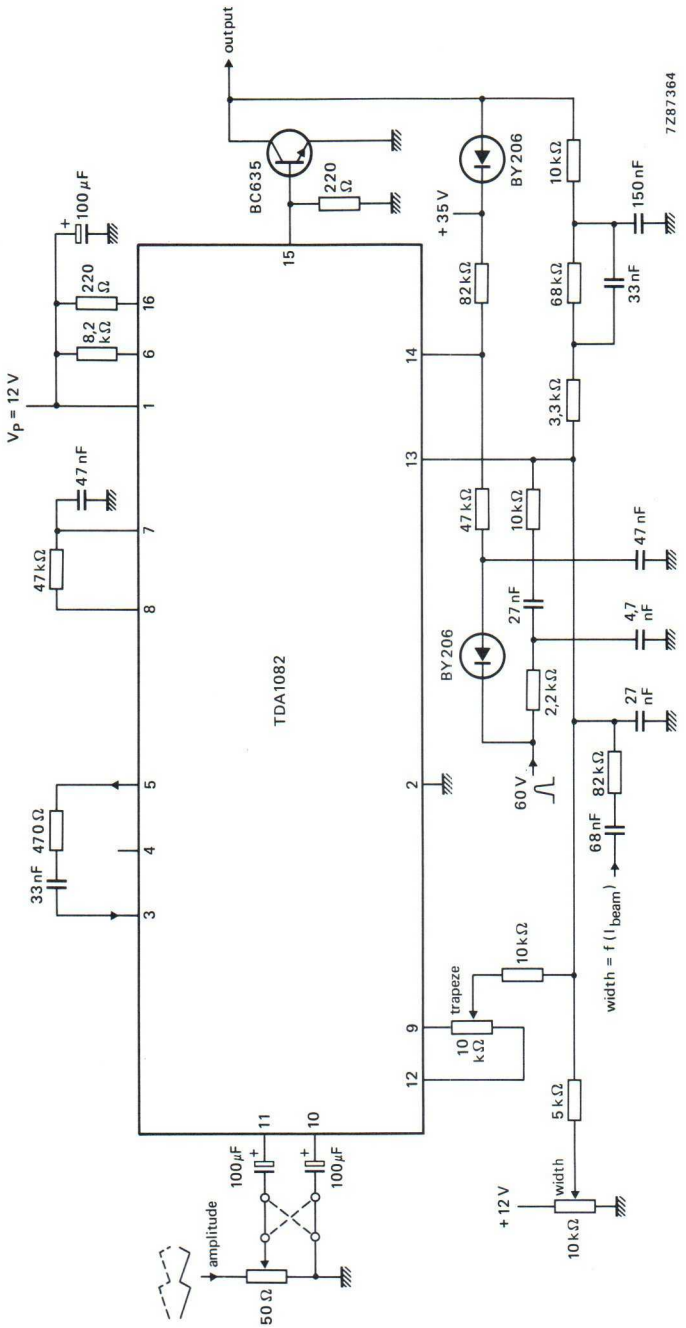


Fig. 2 Application circuit E-W-correction (class-D operation).

50 W HIGH- PERFORMANCE HI-FI AMPLIFIER

GENERAL DESCRIPTION

The TDA1514A integrated circuit is a hi-fi power amplifier for use as a building block in radio, tv and other audio applications. The high performance of the IC meets the requirements of digital sources (e.g. Compact Disc equipment).
The circuit is totally protected, the two output transistors both having thermal and SOAR protection (see Fig.3). The circuit also has a mute function that can be arranged for a period after power-on with a delay time fixed by external components.
The device is intended for symmetrical power supplies but an asymmetrical supply may also be used.

Features

- High output power
- Low harmonic distortion
- Low intermodulation distortion
- Low offset voltage
- Good ripple rejection
- Mute/stand-by facilities
- Thermal protection
- Protected against electrostatic discharge
- No switch-on or switch-off clicks
- Very low thermal resistance
- Safe Operating Area (SOAR) protection

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6 to pin 4)		V_P	± 10	–	± 30	V
Total quiescent current	V_P = ± 27.5 V	I_{tot}	–	56	–	mA
Output power	THD = –60 dB; V_P = ± 27.5 V; R_L = 8 Ω	P_o	–	40	–	W
	V_P = ± 23 V; R_L = 4 Ω	P_o	–	48	–	W
Closed loop voltage gain	determined externally	G_c	–	30	–	dB
Input resistance	determined externally	R_i	–	20	–	kΩ
Signal plus noise-to-noise ratio	P_o = 50 mW	(S+N)/N	–	83	–	dB
Supply voltage ripple rejection	f = 100 Hz	SVRR	–	64	–	dB

PACKAGE OUTLINE

9-lead SIL, plastic power (SOT131R).

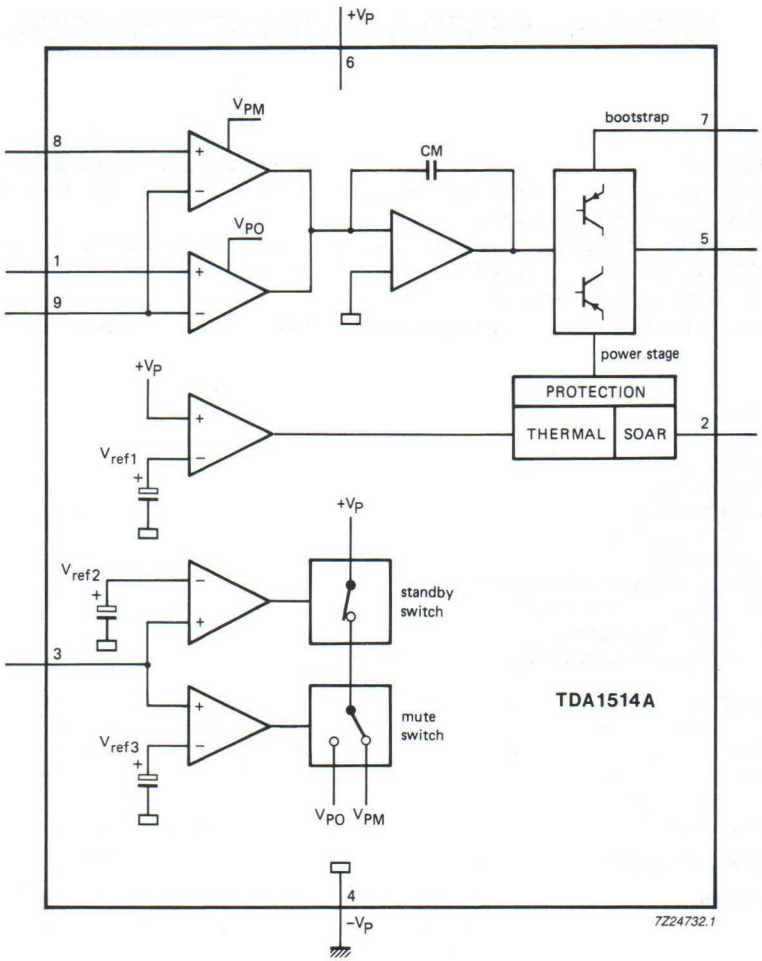


Fig.1 Block diagram.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

2 x 12 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1521/TDA1521Q is a dual hi-fi audio power amplifier encapsulated in a 9-lead plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Stereo applications			
Supply voltage range	V_P	± 7,5 to ± 21,0	V
Output power at THD = 0,5%, V_P = ± 16 V	P_O	typ. 12	W
Voltage gain	G_V	typ. 30	dB
Gain balance between channels	ΔG_V	typ. 0,2	dB
Ripple rejection	SVRR	typ. 60	dB
Channel separation	α	typ. 70	dB
Noise output voltage	$V_{no(rms)}$	typ. 70	μV

PACKAGE OUTLINES

TDA1521: 9-lead single in-line; plastic power (SOT131).
TDA1521Q: 9-lead SIL-bent-to-DIL; plastic power (SOT157).

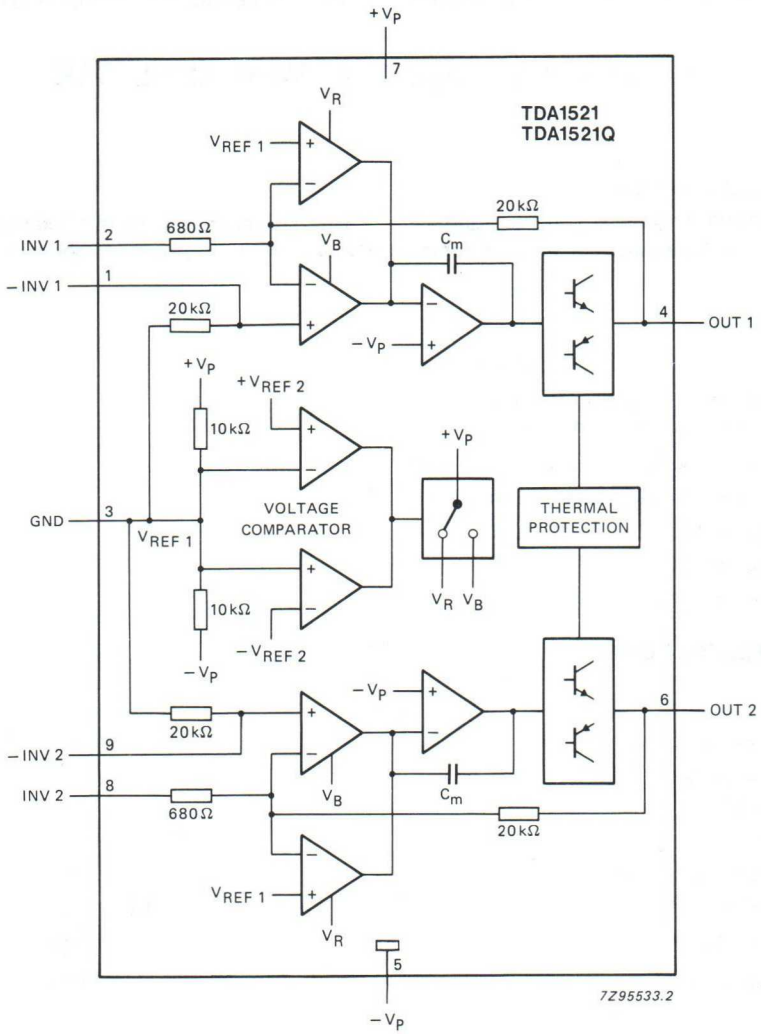


Fig. 1 Block diagram.

PINNING

1	–INV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (symmetrical) / ½ V_P (asymmetrical)
4	OUT1	output 1
5	$-V_P$	negative supply (symmetrical) / ground (asymmetrical)
6	OUT2	output 2
7	+ V_P	positive supply
8	INV2	inverting input 2
9	–INV2	non-inverting input 2

2 x 6 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1521A is a dual hi-fi audio power amplifier encapsulated in a 9-lead plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Stereo applications			
Supply voltage range	V_P	± 7,5 to ± 21,0	V
Output power at THD = 0,5%, V_P = ± 12 V	P_O	typ. 6	W
Voltage gain	G_V	typ. 30	dB
Gain balance between channels	ΔG_V	typ. 0,2	dB
Ripple rejection	SVRR	typ. 60	dB
Channel separation	α	typ. 70	dB
Noise output voltage	$V_{no(rms)}$	typ. 70	μV

PACKAGE OUTLINE

TDA1521A: 9-lead single in-line; plastic power (SOT 110B).

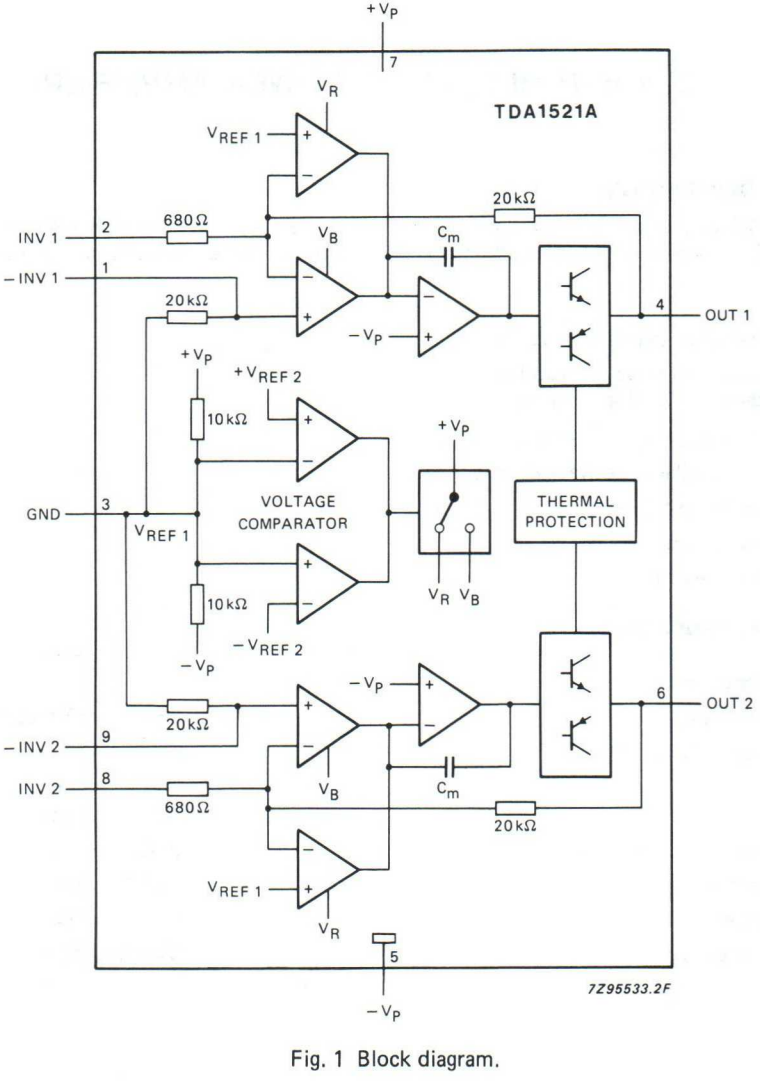


Fig. 1 Block diagram.

PINNING

1	–INV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (symmetrical) / ½ VP (asymmetrical)
4	OUT1	output 1
5	–VP	negative supply (symmetrical) / ground (asymmetrical)
6	OUT2	output 2
7	+ VP	positive supply
8	INV2	inverting input 2
9	–INV2	non-inverting input 2

STEREO-TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by d.c. voltages or by single linear potentiometers.

Features

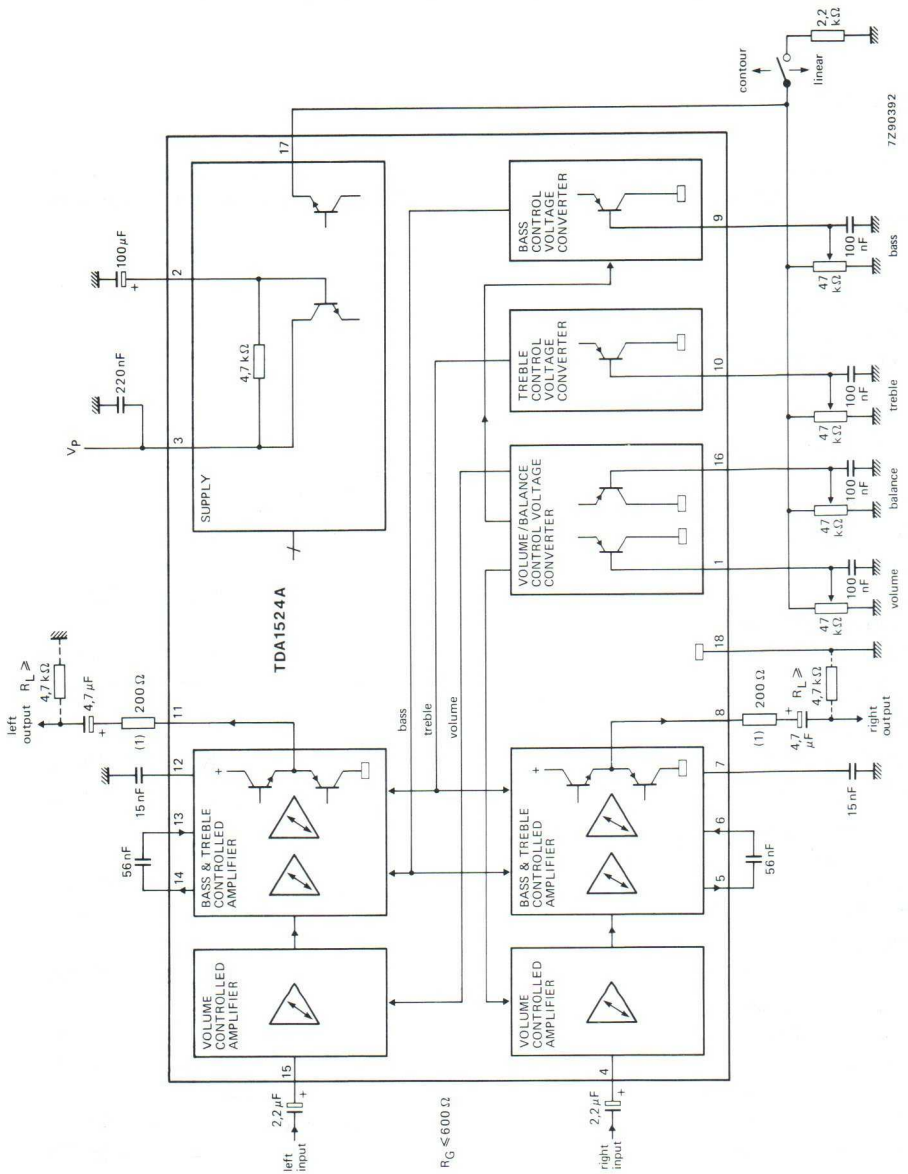
- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

QUICK REFERENCE DATA

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	typ.	12 V
Supply current (pin 3)	$I_P = I_3$	typ.	35 mA
Maximum input signal with d.c. feedback (r.m.s. value)	$V_{i(rms)}$	typ.	2,5 V
Maximum output signal with d.c. feedback (r.m.s. value)	$V_{o(rms)}$	typ.	3 V
Volume control range	G_v		−80 to + 21,5 dB
Bass control range at 40 Hz	ΔG_v		−19 to + 17 dB
Treble control range at 16 kHz	ΔG_v	typ.	± 15 dB
Total harmonic distortion	THD	typ.	0,3 %
Output noise voltage (unweighted; r.m.s. value) at f = 20 Hz to 20 kHz; V_P = 12 V;			
for max. voltage gain	$V_{no(rms)}$	typ.	310 μV
for voltage gain G_v = −40 dB	$V_{no(rms)}$	typ.	100 μV
Channel separation at G_v = −20 to + 21,5 dB	α_{cs}	typ.	60 dB
Tracking between channels at G_v = −20 to + 26 dB	ΔG_v	max.	2,5 dB
Ripple rejection at 100 Hz	RR	typ.	50 dB
Supply voltage range (pin 3)	$V_P = V_{3\text{-}18}$		7,5 to 16,5 V
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig. 1 Block diagram and application circuit with single-pole filter.

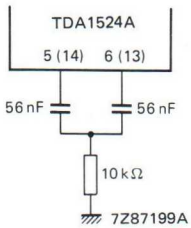


Fig. 2 Double-pole low-pass filter for improved bass-boost.

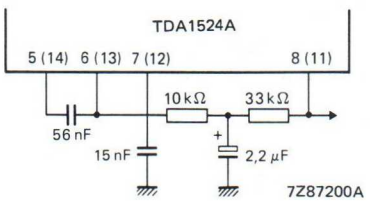


Fig. 3 D.C. feedback with filter network for improved signal handling.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	max.	20 V
Total power dissipation	P_{tot}	max.	1200 mW
Storage temperature range	T_{stg}	−55 to + 150	°C
Operating ambient temperature range	T_{amb}	−30 to + 80	°C

D.C. CHARACTERISTICS

$V_P = V_{3-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	$V_P = V_{3-18}$	7,5	–	16,5	V
Supply current					
at V_P = 8,5 V	$I_P = I_3$	19	27	35	mA
at V_P = 12 V	$I_P = I_3$	25	35	45	mA
at V_P = 15 V	$I_P = I_3$	30	43	56	mA
D.C. input levels (pins 4 and 15)					
at V_P = 8,5 V	$V_{4,15-18}$	3,8	4,25	4,7	V
at V_P = 12 V	$V_{4,15-18}$	5,3	5,9	6,6	V
at V_P = 15 V	$V_{4,15-18}$	6,5	7,3	8,2	V
D.C. output levels (pins 8 and 11) under all control voltage conditions with d.c. feedback (Fig. 3)					
at V_P = 8,5 V	$V_{8,11-18}$	3,3	4,25	5,2	V
at V_P = 12 V	$V_{8,11-18}$	4,6	6,0	7,4	V
at V_P = 15 V	$V_{8,11-18}$	5,7	7,5	9,3	V
Pin 17					
Internal potentiometer supply voltage at V_P = 8,5 V	V_{17-18}	3,5	3,75	4,0	V
Contour on/off switch (control by I_{17})					
contour (switch open)	$-I_{17}$	–	–	0,5	mA
linear (switch closed)	$-I_{17}$	1,5	–	10	mA
Application without internal potentiometer supply voltage at $V_P \geqslant 10{,}8$ V (contour cannot be switched off)					
Voltage range forced to pin 17	V_{17-18}	4,5	–	$V_P/2-V_{BE}$	V
D.C. control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively)					
at V_{17-18} = 5 V	$V_{1,9,10,16}$	1,0	–	4,25	V
using internal supply	$V_{1,9,10,16}$	0,25	–	3,8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	–	–	5	μA

A.C. CHARACTERISTICS

$V_P = V_{3-18} = 8{,}5$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Control range					
Max. gain of volume (Fig. 5)	$G_{V\ max}$	20,5	21,5	23	dB
Volume control range; $G_{V\ max}/G_{V\ min}$	ΔG_V	90	100	–	dB
Balance control range; $G_V = 0$ dB (Fig. 6)	ΔG_V	–	−40	–	dB
Bass control range at 40 Hz (Fig. 7)	ΔG_V	–	−19 to + 17 ± 3		dB
Treble control range at 16 kHz (Fig. 8)	ΔG_V	–	± 15 ± 3	–	dB
Contour characteristics		see Figs 9 and 10			
Signal inputs, outputs					
Input resistance; pins 4 and 15 (note 1)					
at gain of volume control: $G_V = 20$ dB	$R_{i4,15}$	10	–	–	kΩ
$G_V = -40$ dB	$R_{i4,15}$	–	160	–	kΩ
Output resistance (pins 8 and 11)	$R_{o8,11}$	–	–	300	Ω
Signal processing					
Power supply ripple rejection					
at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; $G_V = 0$ dB	RR	35	50	–	dB
Channel separation (250 Hz to 10 kHz)					
at $G_V = -20$ to + 21,5 dB	α_{cs}	46	60	–	dB
Spread of volume control with					
constant control voltage $V_{1-18} = 0{,}5\ V_{17-18}$	ΔG_V	–	–	± 3	dB
Gain tolerance between left and right					
channel $V_{16-18} = V_{1-18} = 0{,}5\ V_{17-18}$	$\Delta G_{V,L-R}$	–	–	1,5	dB
Tracking between channels					
for $G_V = 21{,}5$ to −26 dB					
f = 250 Hz to 6,3 kHz; balance adjusted at					
$G_V = 10$ dB	ΔG_V	–	–	2,5	dB

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal handling with d.c. feedback (Fig. 3)					
Input signal handling					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 8,5 V; THD = 0,7%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,8	2,4	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 12 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 15 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
Output signal handling (note 2 and note 3)					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	1,8	2,0	–	V
at V_P = 8,5 V; THD = 10%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	–	2,2	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	2,5	3,0	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	–	3,5	–	V
Noise performance (V_P = 8,5 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	260	–	μV
for G_V = −3 dB (note 4)	$V_{no(rms)}$	–	70	140	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	890	–	μV
for maximum emphasis of bass and treble (contour off; G_V = −40 dB)	$V_{no(m)}$	–	360	–	μV
Noise performance (V_P = 12 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	310	–	μV
for G_V = −16 dB (note 4)	$V_{no(rms)}$	–	100	200	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	940	–	μV
for maximum emphasis of bass and treble (contour off; G_V = −40 dB)	$V_{no(m)}$	–	400	–	μV

parameter	symbol	min.	typ.	max.	unit
Noise performance (V_P = 15 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	350	–	μV
for G_V = 16 dB (note 4)	$V_{no(rms)}$	–	110	220	μV
Output noise voltage; weighted as DIN 45405					
of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	980	–	μV
for maximum emphasis of bass and treble					
(contour off; G_V = −40 dB)	$V_{no(m)}$	–	420	–	μV

Notes to characteristics

1. Equation for input resistance (see also Fig. 4)

$$R_i = \frac{160\ k\Omega}{1 + G_V}\ ;\ G_{V\ max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. Linear frequency response.
5. For peak values add 4,5 dB to r.m.s. values.

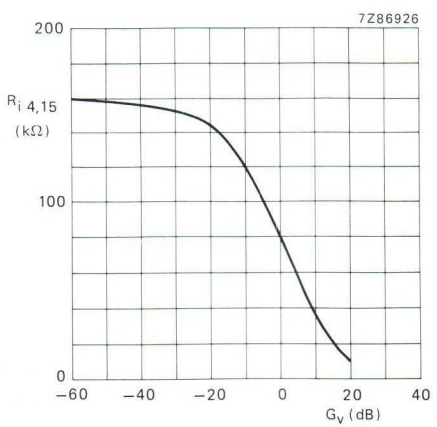


Fig. 4 Input resistance (R_i) as a function of gain of volume control (G_V). Measured in Fig. 1.

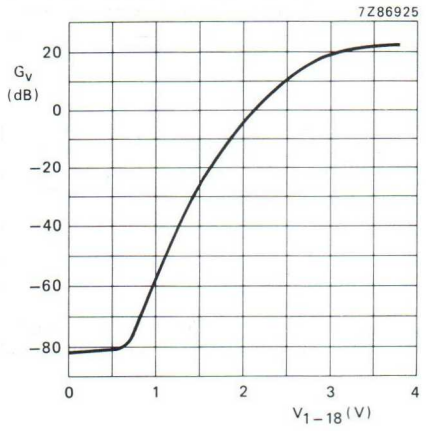


Fig. 5 Volume control curve; voltage gain (G_v) as a function of control voltage (V_{1-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 1 kHz.

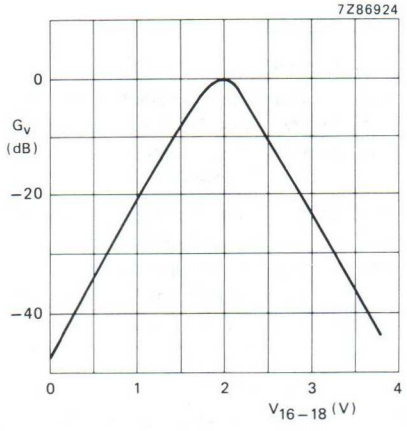


Fig. 6 Balance control curve; voltage gain (G_v) as a function of control voltage (V_{16-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V.

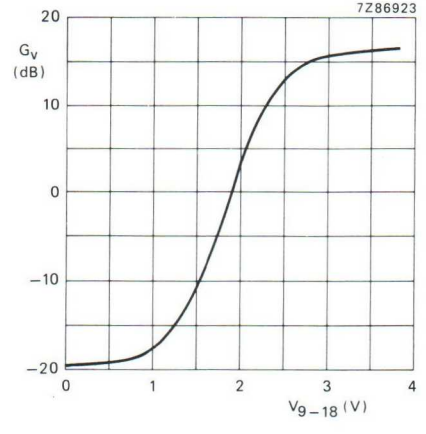


Fig. 7 Bass control curve; voltage gain (G_v) as a function of control voltage (V_{9-18}). Measured in Fig. 1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 40 Hz.

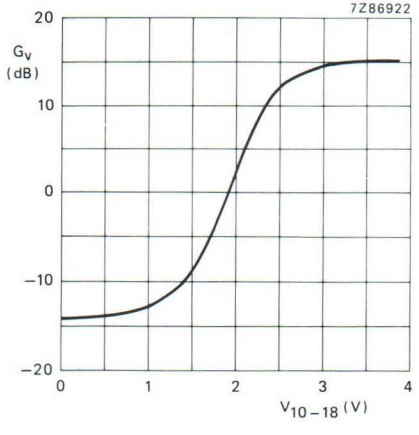


Fig. 8 Treble control curve; voltage gain (G_v) as a function of control voltage (V_{10-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 16 kHz.

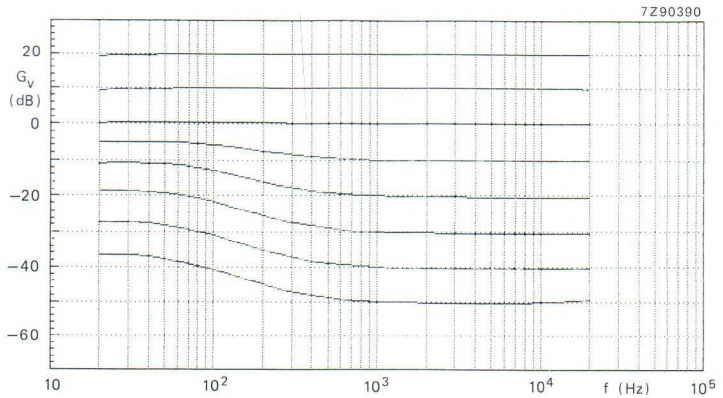


Fig. 9 Contour frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

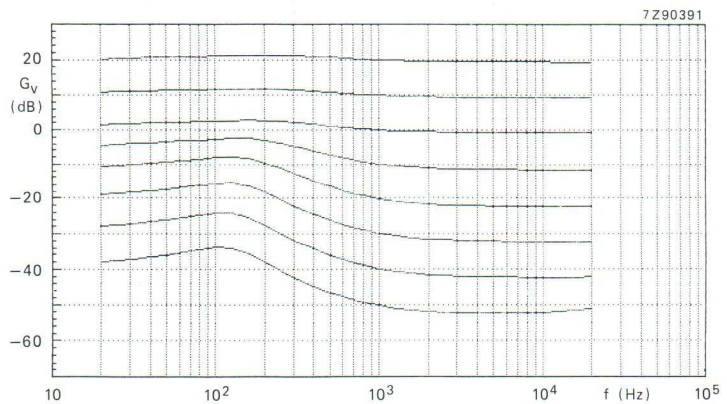


Fig. 10 Contour frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

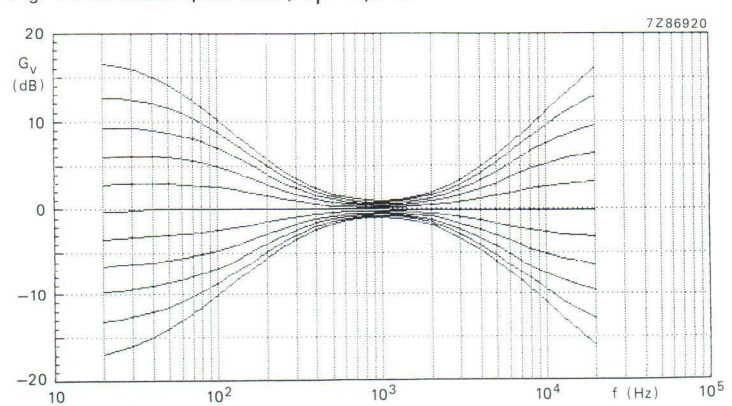


Fig. 11 Tone control frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

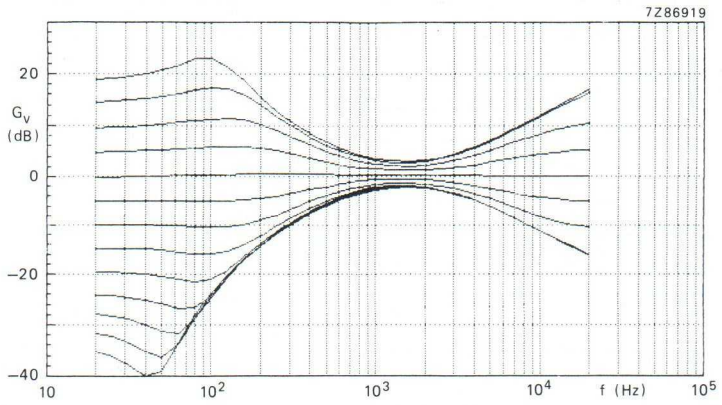


Fig. 12 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

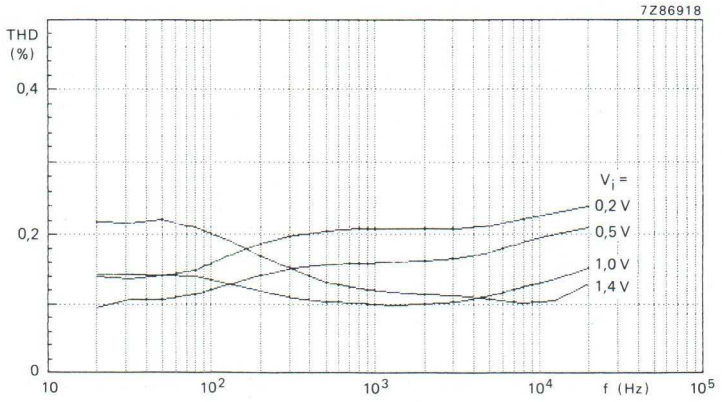


Fig. 13 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig. 1; V_P = 8,5 V; volume control voltage gain at

$$G_V = 20 \log \frac{V_o}{V_i} = 0 \text{ dB}.$$

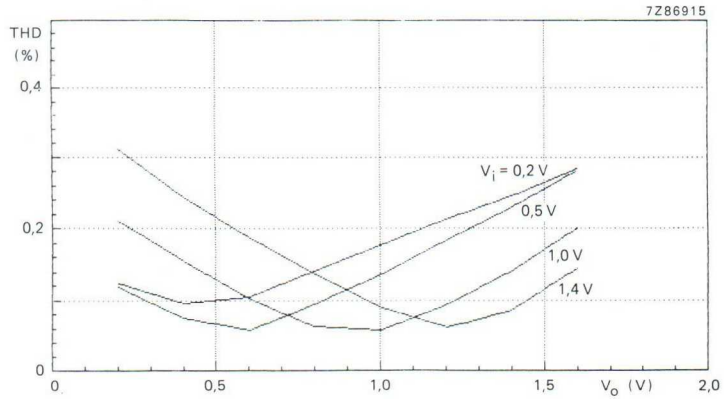
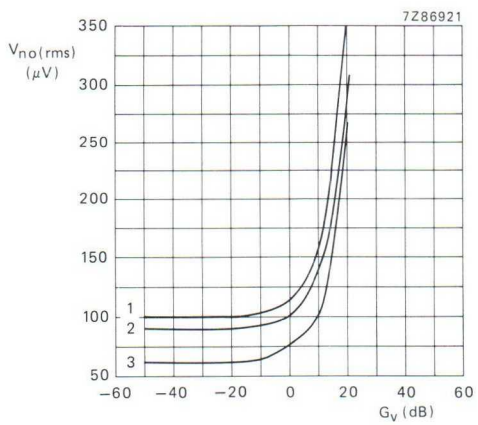


Fig. 14 Total harmonic distortion (THD); as a function of output voltage (V_O). Measured in Fig. 1; V_P = 8,5 V; f_i = 1 kHz.



(1) V_P = 15 V.
(2) V_P = 12 V.
(3) V_P = 8,5 V.

Fig. 15 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain (G_V). Measured in Fig. 1; f = 20 Hz to 20 kHz.

STEREO-TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by DC voltages or by single linear potentiometers.

Features

- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

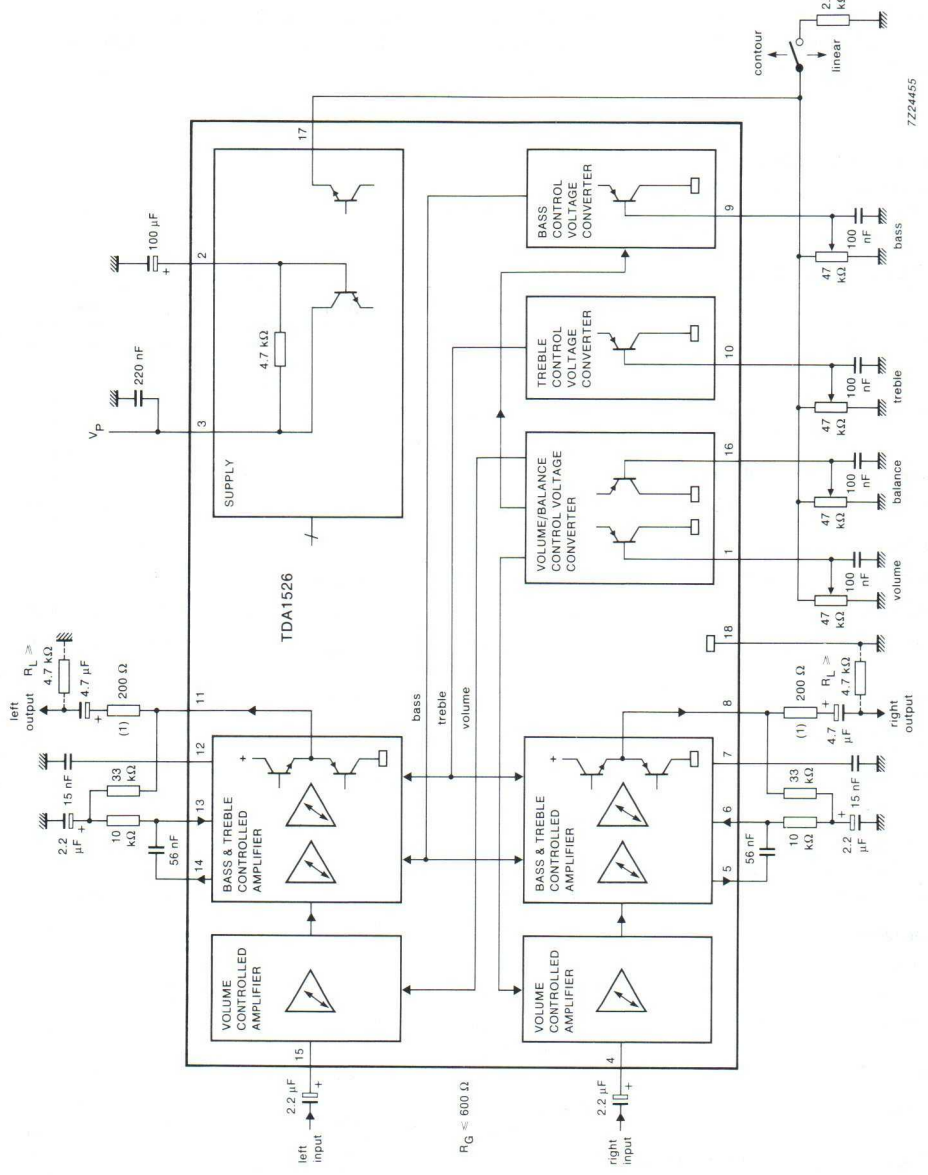
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		V_P	7.5	12	16.5	V
Supply current (pin 3)	V_P = 12 V	I_P	25	35	45	mA
Signal handling with DC feedback	V_P = 8.5 to 15 V; THD = 0.7%; f = 1 kHz					
Input signal handling (RMS value)		$V_{i(rms)}$	1.8	2.0	–	V
Output signal handling (RMS value)	notes 2 and 3	$V_{o(rms)}$	1.8	2.0	–	V
Control range						
Maximum gain of volume	see Fig. 4	$G_{v\,max}$	20.5	21.5	23	dB
Volume control range	$G_{v\,max}/G_{v\,min}$	ΔG_v	90	100	–	dB
Balance control range	G_v = 0 dB; see Fig. 5	ΔG_v	–	–40	–	dB
Bass control range	at 40 Hz; see Fig. 6	ΔG_v	–	–19 to +17 ±3	–	dB
Treble control range	at 16 kHz; see Fig. 7	ΔG_v	–	±15 ±3	–	dB
Total harmonic distortion		THD	–	–	0.5	%
Noise performance	V_P = 12 V					
Output noise voltage (unweighted) at f = 20 Hz to 20 kHz for G_v = –16 dB	RMS value; note 4 note 5	$V_{no(rms)}$	–	100	200	μV
Signal processing						
Channel separation at G_v = –20 to 21.5 dB	f = 250 Hz to 10 kHz	α_{cs}	46	60	–	dB
Tracking between channels for G_v = 21.5 to –26 dB	f = 250 Hz to 6.3 kHz; balance at G_v = 10 dB	ΔG_v	–	–	2.5	dB
Ripple rejection	$V_{P(rms)} = \leqslant 200$ mV; f = 100 Hz; G_v = 0 dB	RR	35	50	–	dB
Operating ambient temperature range		T_{amb}	–30	–	+85	°C

For explanation of notes see **Notes to the characteristics.**

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig.1 Block diagram and application circuit with single-pole filter.

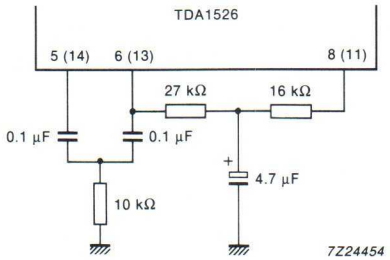


Fig.2 Double-pole low-pass filter for improved bass-boost.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	V_P	–	20	V
Total power dissipation	P_{tot}	–	1200	mW
Storage temperature range	T_{stg}	–55	+ 150	°C
Operating ambient temperature range	T_{amb}	–30	+ 80	°C

DC CHARACTERISTICS

$V_P = V_{3-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4.7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	$V_P = V_{3-18}$	7.5	–	16.5	V
Supply current					
at $V_P = 8.5$ V	$I_P = I_3$	19	27	35	mA
at $V_P = 12$ V	$I_P = I_3$	25	35	45	mA
at $V_P = 15$ V	$I_P = I_3$	30	43	56	mA
DC input levels (pins 4 and 15)					
at $V_P = 8.5$ V	$V_{4,15-18}$	3.8	4.25	4.7	V
at $V_P = 12$ V	$V_{4,15-18}$	5.3	5.9	6.6	V
at $V_P = 15$ V	$V_{4,15-18}$	6.5	7.3	8.2	V
DC output levels (pins 8 and 11) under all control voltage conditions with DC feedback					
at $V_P = 8.5$ V	$V_{8,11-18}$	3.3	4.25	5.2	V
at $V_P = 12$ V	$V_{8,11-18}$	4.6	6.0	7.4	V
at $V_P = 15$ V	$V_{8,11-18}$	5.7	7.5	9.3	V
Pin 17					
Internal potentiometer supply voltage at $V_P = 8.5$ V	V_{17-18}	3.5	3.75	4.0	V
Contour on/off switch (control by I_{17})					
contour (switch open)	$-I_{17}$	–	–	0.5	mA
linear (switch closed)	$-I_{17}$	1.5	–	10	mA
Application without internal potentiometer supply voltage at $V_P \geqslant 10.8$ V (contour cannot be switched off)					
Voltage range forced to pin 17	V_{17-18}	4.5	–	$V_P/2-V_{BE}$	V
DC control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively)					
at $V_{17-18} = 5$ V	$V_{1,9,10,16}$	1.0	–	4.25	V
using internal supply	$V_{1,9,10,16}$	0.25	–	3.8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	–	–	5	μA

AC CHARACTERISTICS

$V_P = V_{3-18} = 8.5$ V; $T_{amb} = 25$ °C; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4.7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Control range					
Maximum gain of volume (Fig. 4)	$G_{V\,max}$	20.5	21.5	23	dB
Volume control range; $G_{V\,max}/G_{V\,min}$	ΔG_V	90	100	–	dB
Balance control range; G_V = 0 dB (Fig. 5)	ΔG_V	–	−40	–	dB
Bass control range at 40 Hz (Fig. 6)	ΔG_V	–	−19 to +17 ±3		dB
Treble control range at 16 kHz (Fig. 7)	ΔG_V	–	±15 ±3	–	dB
Contour characteristics			see Figs 9 and 10		
Signal inputs, outputs					
Input resistance; pins 4 and 15 (note 1)					
at gain of volume control: G_V = 20 dB	$R_{i4,15}$	10	–	–	kΩ
G_V = −40 dB	$R_{i4,15}$	–	160	–	kΩ
Output resistance (pins 8 and 11)	$R_{o8,11}$	–	–	300	Ω
Signal processing					
Power supply ripple rejection at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; G_V = 0 dB	RR	35	50	–	dB
Channel separation (250 Hz to 10 kHz) at G_V = −20 to +21.5 dB	α_{cs}	46	60	–	dB
Spread of volume control with constant control voltage $V_{1-18} = 0.5\,V_{17-18}$	ΔG_V	–	–	±3	dB
Gain tolerance between left and right channel $V_{16-18} = V_{1-18} = 0.5\,V_{17-18}$	$\Delta G_{V,L-R}$	–	–	1.5	dB
Tracking between channels for G_V = 21.5 to −26 dB f = 250 Hz to 6.3 kHz; balance adjusted at G_V = 10 dB	ΔG_V	–	–	2.5	dB

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal handling with DC feedback					
Input signal handling at V_P = 8.5 V – 15 V; THD = 0.7%; f = 1 kHz (RMS value)	$V_{i(rms)}$	1.8	2.0	–	V
Output signal handling (note 2 and note 3) at V_P = 8.5 V; THD = 0.7%; f = 1 kHz (RMS value)	$V_{o(rms)}$	1.8	2.0	–	V
Noise performance (V_P = 12 V)					
Output noise voltage (unweighted; Fig. 14) at f = 20 Hz to 20 kHz (RMS value; note 4) for G_V = –16 dB (note 5)	$V_{no(rms)}$	–	100	200	μV

Notes to characteristics

1. Equation for input resistance (see also Fig. 3)

$$R_i = \frac{160\,k\Omega}{1 + G_V}; G_{V\,max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. For peak values add 4.5 dB to RMS values.
5. Linear frequency response.

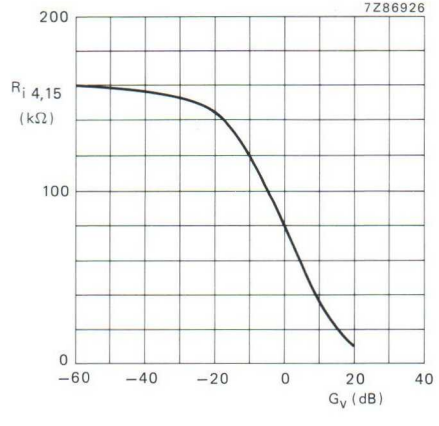


Fig.3 Input resistance (R_i) as a function of gain of volume control (G_V). Measured in Fig.1.

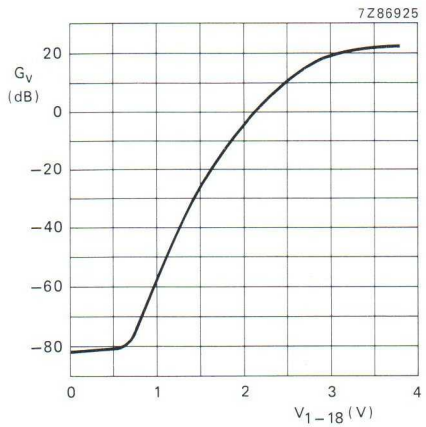


Fig.4 Volume control curve; voltage gain (G_v) as a function of control voltage (V_{1-18}). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 1 kHz.

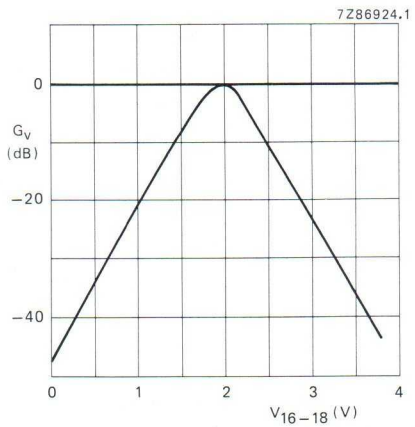


Fig.5 Balance control curve; voltage gain (G_v) as a function of control voltage (V_{16-18}). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V.

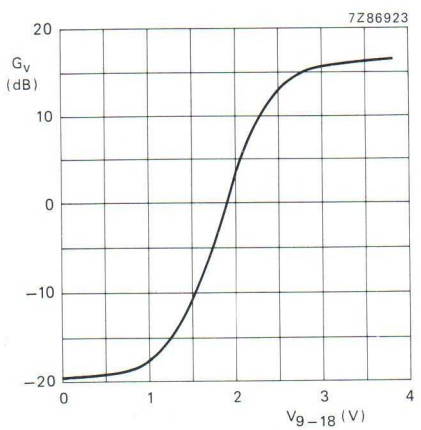


Fig.6 Bass control curve; voltage gain (G_v) as a function of control voltage (V_{9-18}). Measured in Fig.1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 40 Hz.

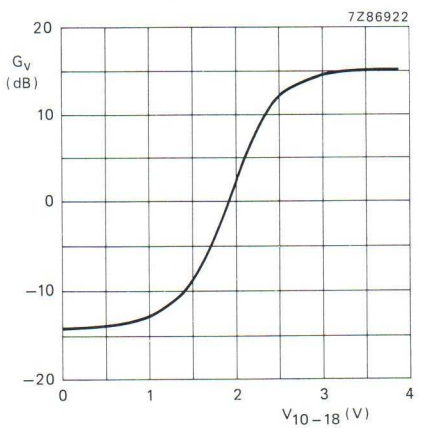


Fig.7 Treble control curve; voltage gain (G_v) as a function of control voltage (V_{10-18}). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 16 kHz.

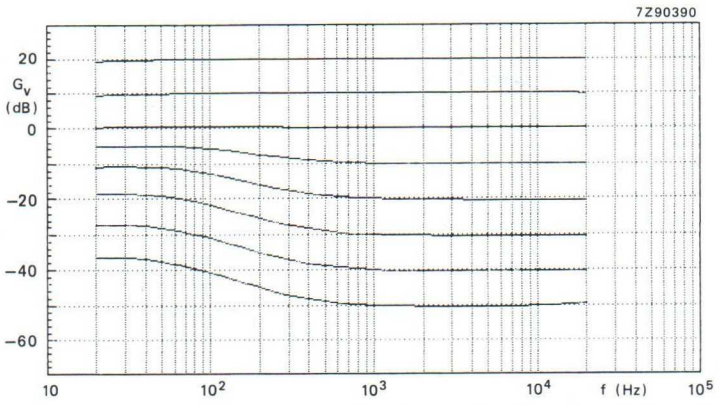


Fig.8 Contour frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig.1 with single-pole filter; V_P = 8.5 V.

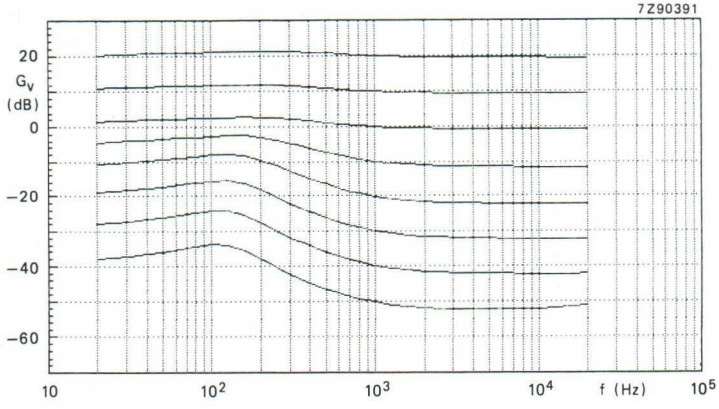


Fig.9 Contour frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig.1 with double-pole filter; V_P = 8.5 V.

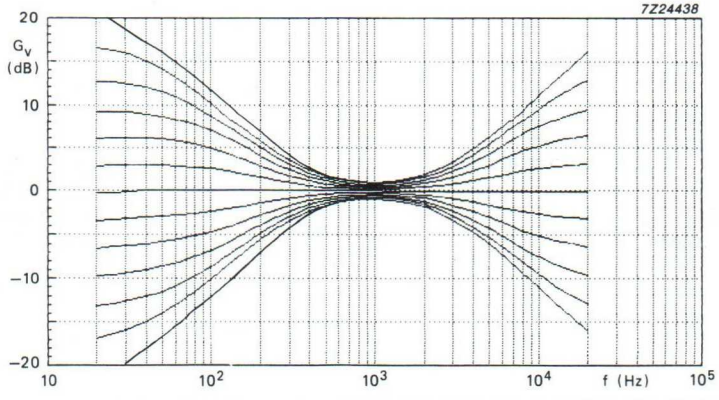


Fig.10 Tone control frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig.1 with single-pole filter; V_P = 8.5 V.

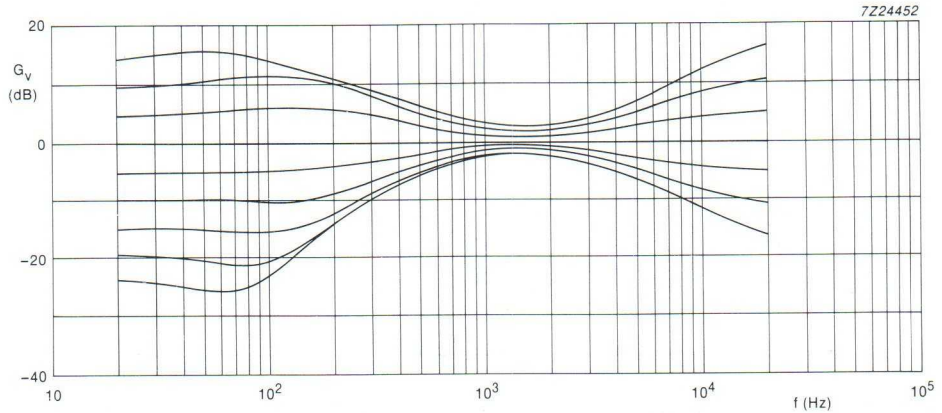


Fig.11 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig.1 with double-pole filter; V_P = 8.5 V.

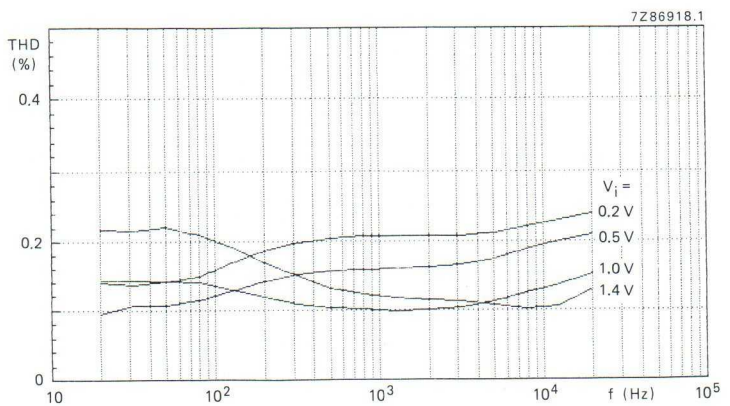


Fig.12 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig.1; V_P = 8.5 V; volume control voltage gain at

$$G_V = 20 \log \frac{V_O}{V_i} = 0 \text{ dB}.$$

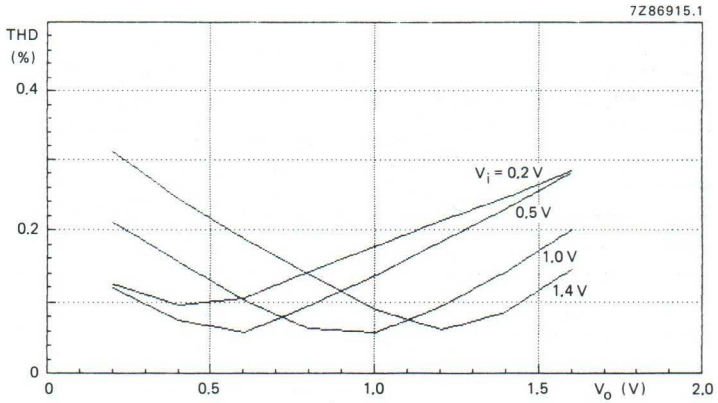


Fig.13 Total harmonic distortion (THD); as a function of output voltage (V_O). Measured in Fig.1; V_P = 8.5 V; f_i = 1 kHz.

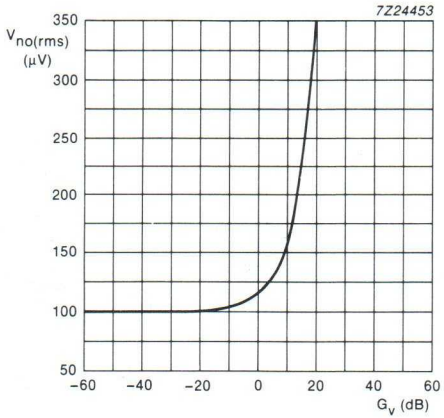


Fig.14 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain (G_v). Measured in Fig.1; V_P = 15 V; f = 20 Hz to 20 kHz.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	February 1991

TDA1541A

Stereo high performance 16-bit DAC

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATASHEET

FEATURES

- High sound quality
- High performance: low noise and distortion, wide dynamic range
- 4 x or 8 x oversampling possible
- Selectable two-channel input format
- TTL compatible inputs

GENERAL DESCRIPTION

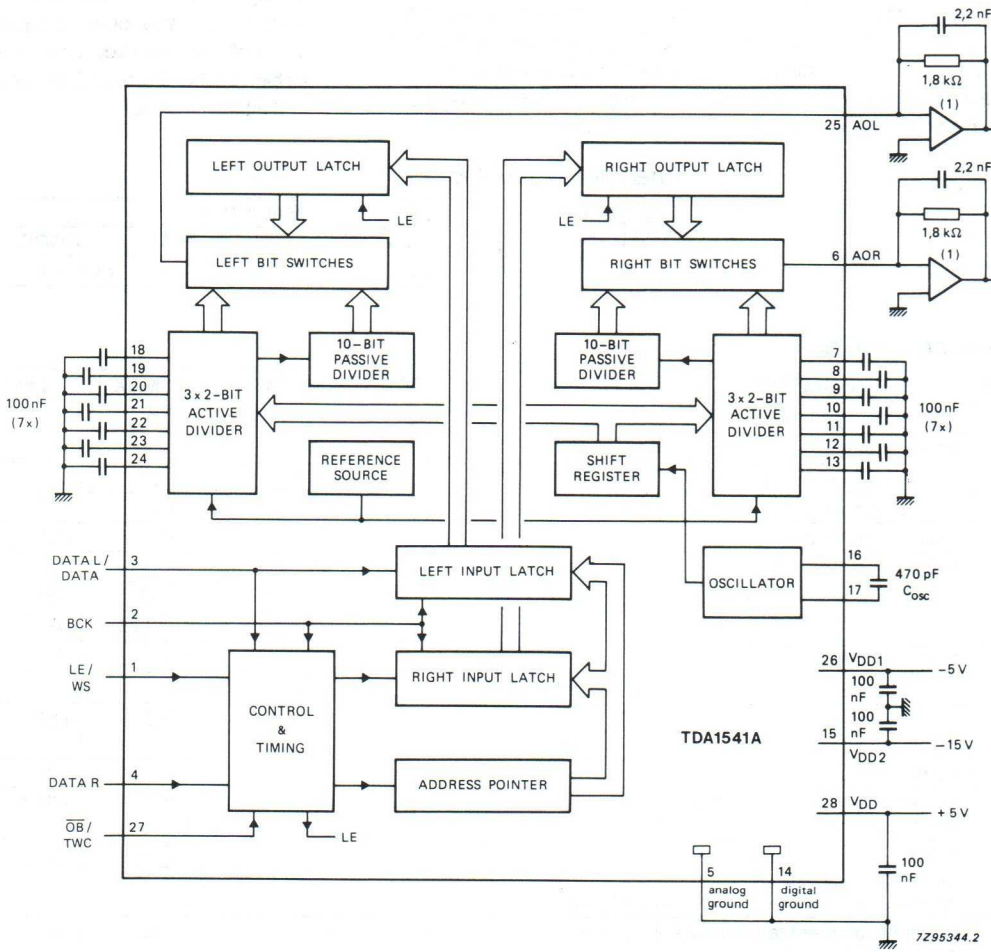
The TDA1541A is a stereo 16-bit digital-to-analog converter (DAC). The ingenious design of the electronic circuit guarantees a high performance and superior sound quality. The TDA1541A is therefore extremely suitable for use in top-end high-fi digital audio equipment such as high quality Compact Disc players or digital amplifiers.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1541A	28	DIL	plastic	SOT117

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage; pin 28		4.5	5.0	5.5	V
$-V_{DD1}$	supply voltage; pin 26		4.5	5.0	5.5	V
$-V_{DD2}$	supply voltage; pin 15		14.0	15.0	16.0	V
I_{DD}	supply current; pin 28		-	27	40	mA
$-I_{DD1}$	supply current; pin 26		-	37	50	mA
$-I_{DD2}$	supply current; pin 15		-	25	35	mA
THD	total harmonic distortion	including noise	-	−95	−90	dB
		at 0 dB	-	0.0018	0.0032	%
THD	total harmonic distortion	including noise	-	−42	-	dB
		at −60 dB	-	0.79	-	%
NL	non-linearity	at T_{amb} = −20 to +85 °C	-	0.5	1.0	LSB
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input; (pin 3 and 4)		-	-	6.4	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	6.4	MHz
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 200 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−40	-	+85	°C
P_{tot}	total power dissipation		-	700	-	mW



(1) TDA1542
(2) 2 x NE5534 or equivalent

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LE/WS	1	latch enable input / word select input
BCK	2	bit clock input
DATA L /DATA	3	data left channel input / data input (selected format)
DATA R	4	data right channel input
GND(A)	5	analog ground
AOR	6	right channel output
DECOU	7 to 13	decoupling
GND (D)	14	digital ground
V_{DD2}	15	−15 V supply voltage
COSC	16,17	oscillator
DECOU	18 to 24	decoupling
AOL	25	left channel output
V_{DD1}	26	−5 V supply voltage
$\overline{OB}$/TWC	27	mode select input
V_{DD}	28	+5 V supply voltage

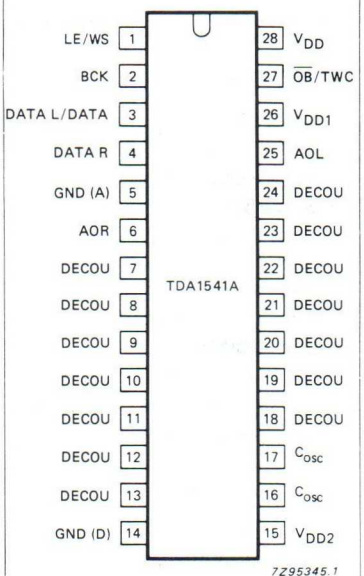


Fig.2 Pin configuration

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	February 1991

TDA1543

Dual 16-bit DAC (economy version) (I^2S input format)

FEATURES

- Low distortion
- 16-bit dynamic range
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- I^2S input format: time multiplexed, two's complement, TTL

GENERAL DESCRIPTION

The TDA1543 is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders, digital sound in TV sets and in digital amplifiers.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1543	8	DIL	plastic	SOT97
TDA1543T	16	mini-pack	plastic	SO16L;SOT162A

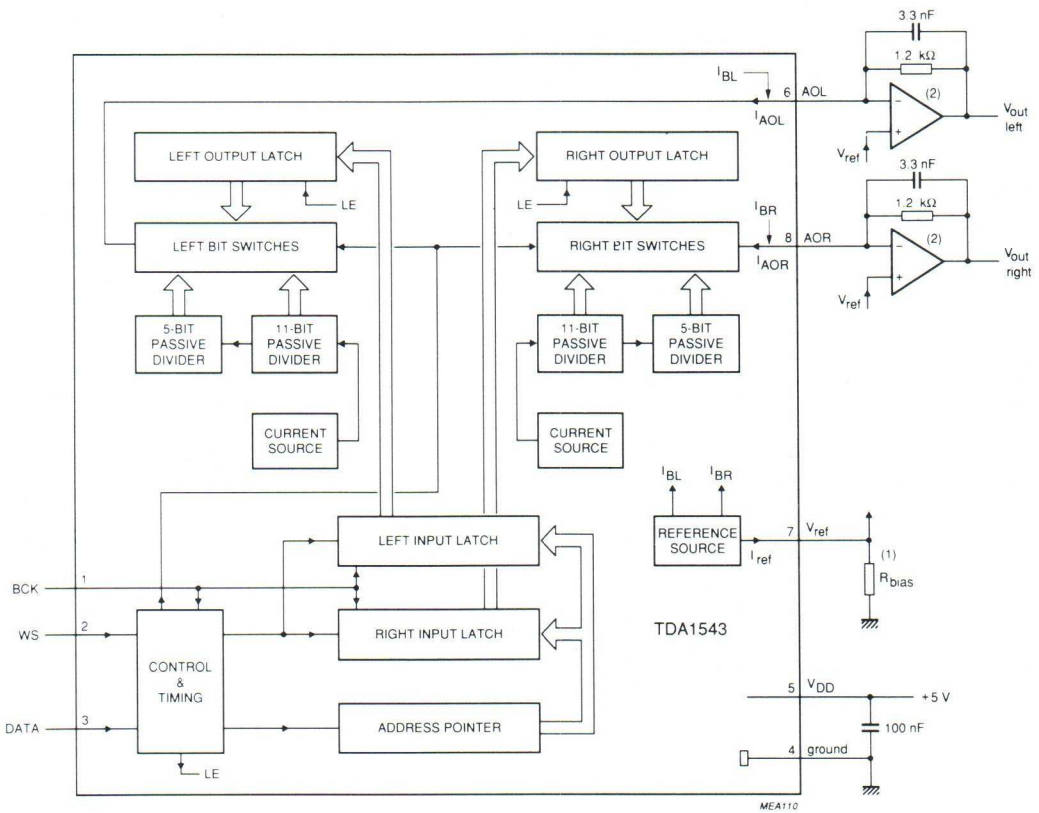
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		-	50	60	mA
I_{FS}	full scale output current		1.95	2.30	2.65	mA
THD	total harmonic distortion	including noise	-	−75	−70	dB
		at 0 dB	-	0.018	0.032	%
THD	total harmonic distortion	including noise	-	−30	−23	dB
		at −60 dB	-	3.2	7.9	%
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input		-	-	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	9.2	MHz
S/N	signal-to-noise ratio	at bipolar zero	90	96	-	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 500 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−30	-	+85	°C
P_{tot}	total power dissipation		-	250	-	mW
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

Dual 16-bit DAC (economy version) (I^2S input format)

TDA1543



(1) Optional
(2) 2 x 1/2 NE5532

Fig.1 Block diagram.

Dual 16-bit DAC (economy version) (I^2S input format)

TDA1543

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	+5 V supply voltage
AOL	6	left channel voltage output
V_{ref}	7	reference voltage output
AOR	8	right channel output

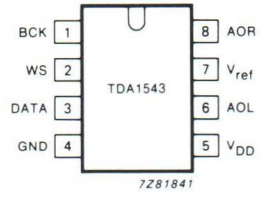


Fig.2(a) Pin configuration TDA1543.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
BCK	3	bit clock input
WS	4	word select input
DATA	5	data input
GND	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DD}	11	+5 V supply voltage
AOL	12	left channel output
V_{ref}	13	reference voltage output
AOR	14	right channel output
n.c.	15	not connected
n.c.	16	not connected

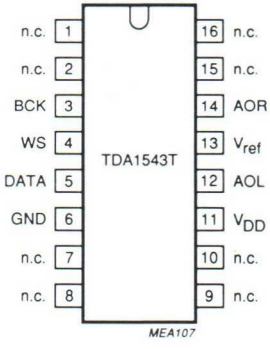


Fig.2(b) Pin configuration TDA1543T.

Stereo continuous calibration DAC TDA1545A

FEATURES

- Space saving package (SO8 or DIL8)
- Low power consumption
- Low total harmonic distortion
- Wide dynamic range (16-bit resolution)
- Continuous calibration concept
- Easy application: single 3 to 5.5 V rail power supply and output- and bias current are proportional to the supply voltage
- Fast settling time permits 2 x, 4 x and 8 x oversampling (serial input) or double speed operation at 4 x oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range of −40 °C to +85 °C
- Compatible with most of the Japanese input formats: time multiplexed, two's complement and TTL
- No zero crossing distortion.

GENERAL DESCRIPTION

The TDA1545A is the first device of a new generation of the digital-to-analog convertors which embodies the innovative technique of continuous calibration. The largest bit-currents are repeatedly generated by one single current reference source. This duplication is based upon an internal charge storage principle having an accuracy insensitive to ageing, temperature and process variations.

The device is fabricated in a 1.0 μm CMOS process and features an extremely low power dissipation, small package size and easy application. Furthermore, the accuracy of the high coarse current combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensures high quality audio reproduction. Therefore, the continuous calibration digital-to-analog convertor is eminently suitable for use in (portable) digital audio equipment.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1545A	8	DIL	plastic	SOT97
TDA1545AT	8	mini-pack	plastic	SO8; SOT96A

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3	5	5.5	V
I_{DD}	supply current	V_{DD} = 5 V; at code 0000H	–	3.0	4.0	mA
I_{FS}	full scale output current					
		V_{DD} = 5 V	0.9	1.0	1.1	mA
		V_{DD} = 3 V	–	0.6	–	mA
THD	total harmonic distortion	including noise				
		at 0 dB	–	–88	–78	dB
		at 0 dB	–	0.004	0.01	%
		at –60 dB	–	–33	–24	dB
		at –60 dB	–	2.2	6	%
		at –60 dB; A-weighting	–	–35	–	dB
		at –60 dB; A-weighting	–	1.7	–	%
		at –60 dB; A-weighting; R3 = R4 = 11 kΩ; I_{FS} = 2 mA	–	1.4	–	%
S/N	signal-to-noise ratio at bipolar zero					
		A-weighting; at code 0000H	86	98	–	dB
		R3 = R4 = 11 kΩ; I_{FS} = 2 mA	–	101	–	dB
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
BR	input bit rate at data input		–	–	18.4	Mbits/s
f_{BCK}	clock frequency at clock input		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (IOL; IOR)		–	±400	–	ppm
P_{tot}	total power dissipation	at code 0000H				
		V_{DD} = 5 V	–	15	20	mW
		V_{DD} = 3 V	–	6	–	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C

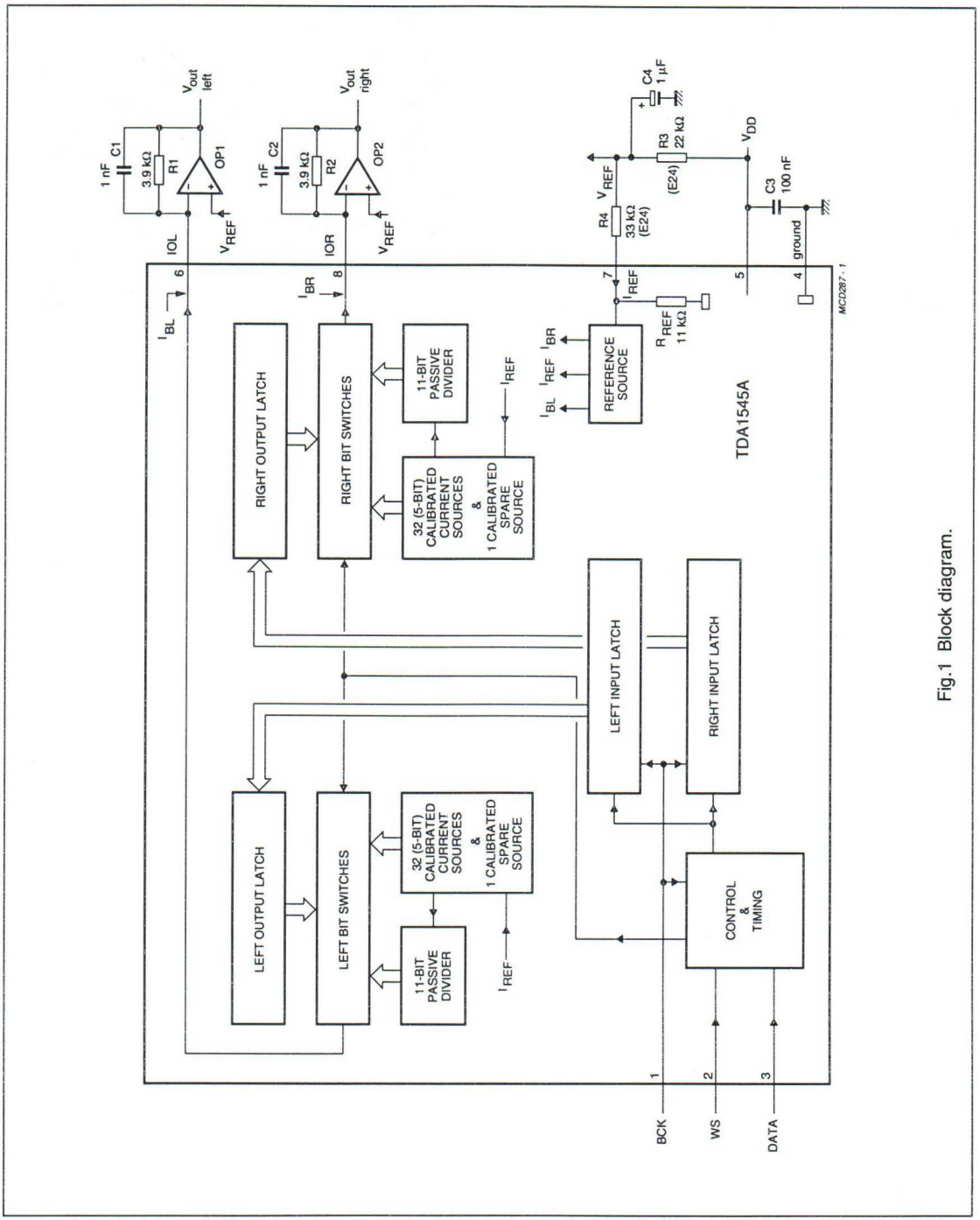


Fig.1 Block diagram.

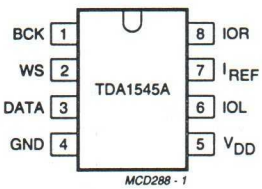


Fig.2 Pin configuration.

PINNING

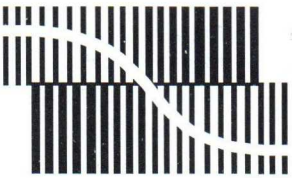
SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	positive supply voltage
IOL	6	left channel output
I_{REF}	7	reference current input
IOR	8	right channel output

Bitstream Continuous Calibration DAC with digital sound processing (BCC-DAC)

TDA1546T

CONTENTS

1 FEATURES
1.1 Easy application
1.2 High performance
1.3 Digital sound processing features
1.3.1 Volume control features
1.3.2 Sound processing features
1.3.3 Sound monitor features
2 ORDERING INFORMATION
3 QUICK REFERENCE DATA
4 GENERAL DESCRIPTION
5 BLOCK DIAGRAM
6 PINNING
7 FUNCTIONAL DESCRIPTION
7.1 Clock generation and distribution
7.2 Power-on reset
7.3 Microprocessor interface
7.3.1 Address mode
7.3.2 Data transfer mode
7.3.3 Organization and programming of the internal register file
7.3.3.1 Volume control register bits: BAL3 to BAL0 and BAR3 to BAR0
7.3.3.2 Volume control register bits: VC7 to VC0 and FT3 to FT0
7.3.3.3 Volume control register bit: MUTE
7.3.3.4 Volume control register bit: RUNFA
7.3.3.5 Sound monitor register bits: FP2 to FP0
7.3.3.6 Sound monitor register bits: OVER3 to OVER0
7.3.3.7 Sound monitor register bits: SIL3 to SIL0 and SILT3 to SILT0
7.3.3.8 Sound monitor register bit SPOS
7.3.3.9 Sound processing register bit: DSS
7.3.3.10 Sound processing register bits: SCT3 to SCT0
7.3.3.11 Sound processing register bits: SCB3 to SCB0
7.3.3.12 Sound processing register bits: SCBB3 to SCBB0
7.3.3.13 Sound processing register bits: DEMC1 and DEMC0
7.3.3.14 Sound processing register bit: DSM
7.3.3.15 Miscellaneous register bits: ED3 to ED0
7.3.3.16 Miscellaneous register bits: EA2 to EA0
7.3.3.17 Miscellaneous register bits: INS1 and INS0
7.3.3.18 Miscellaneous register bits: PVIV1, PVIV0 and PINM1, PINM0
7.3.3.19 Miscellaneous register bit: CLRM
7.3.3.20 Miscellaneous register bits: OUTS1 and OUTS0
7.3.3.21 Miscellaneous register bit: LONLY
7.3.3.22 Miscellaneous register bits: FSO1, FSO0, TRI, ACDT, DCDT, CLKIV, CLKON, DYC1 and DYC0
7.4 Multiple format input interface
7.4.1 Synchronization
7.5 Normal-speed mode
7.6 Double-speed mode
7.6.1 Double-speed mode features
7.6.2 Low-power option using double-speed mode
7.7 Volume control features
7.7.1 Digital balance
7.7.2 Digital volume control with fade function
7.7.3 Digital soft-mute
7.7.4 Scaling and polarity of the digital up-sampling filter
7.8 Sound processing related features
7.8.1 De-emphasis filter
7.8.2 Treble
7.8.3 Bass
7.8.4 Bass boost
7.8.5 Digital dynamic bass boost, digital loudness and other dynamic applications of tone control
7.8.6 Digital speaker system mode
7.9 Sound monitor block
7.9.1 Spectrum analyzer
7.9.2 dB converter
7.9.3 Peak detection
7.9.4 Silence detection
7.9.5 Overload detection
7.9.6 Versatile outputs
7.10 Noise shaper
7.11 Continuous calibration digital-to-analog converter
7.12 Operational amplifiers
7.13 Internal reference circuitry
8 LIMITING VALUES
9 THERMAL CHARACTERISTICS
10 QUALITY SPECIFICATION
11 CHARACTERISTICS
12 ANALOG CHARACTERISTICS



BITSTREAM CONVERSION

13 APPLICATION INFORMATION
13.1 Digital filter characteristics (theoretical values)
13.2 Example application circuit
14 PACKAGE OUTLINE
15 SOLDERING
15.1 Plastic small-outline packages
15.1.1 By wave
15.1.2 By solder paste reflow
15.1.3 Repairing soldered joints (by hand-held soldering iron or pulse-heated solder tool)
16 DEFINITIONS
17 LIFE SUPPORT APPLICATIONS
18 PURCHASE OF PHILIPS I²C COMPONENTS

Bitstream Continuous Calibration DAC with digital sound processing (BCC-DAC)

TDA1546T

1 FEATURES

1.1 Easy application

- Voltage output 1.5 V (RMS)
- Operational amplifiers and cascaded 4-stage digital FIR filter integrated
- Master and slave mode clock system with selectable system clock (f_{sys}) $256f_s$ or $384f_s$
- I^2S-bus serial input format or Japanese 16, 18 or 20 bits serial input mode
- All features are accessible under remote control
- Simple 3-line serial microcontroller command interface
- Power-on reset
- 28 lead small outline package.

1.2 High performance

- Superior signal-to-noise ratio
- Low total harmonic distortion
- Wide dynamic range
- No zero crossing distortion
- Continuous calibration digital-to-analog conversion combined with noise shaping techniques
- Second-order noise shaper
- 128 times oversampling in normal-speed mode
- 64 times oversampling in double-speed mode.

1.3 Digital sound processing features

1.3.1 VOLUME CONTROL FEATURES

- Smoothed transitions before and after digital mute (soft mute)
- Fade function: duration-programmable (6 ms to 22.4 s at 44.1 kHz) digital volume control (attenuation as well as gain): +6 dB to −90 dB in steps of 0.375 dB with automatic soft mute
- Digital balance: 0 dB to −22.5 dB in steps of −1.5 dB (maximum overall attenuation combined with volume control: −90 dB)

1.3.2 SOUND PROCESSING FEATURES

- Digital de-emphasis filter for three sample rates (32 kHz, 44.1 kHz or 48 kHz)
- Digital treble: −10.5 dB to +12 dB at 20 kHz; 16 steps spaced at 1.5 dB
- Digital bass: −9 dB to +13.5 dB at 20 Hz; 16 steps spaced at 1.5 dB
- Distortion-free digital dynamic bass boost: 0 dB to +37 dB at 10 Hz; 15 steps spaced at 2 dB
- Can be used for loudness or dynamic digital bass boost
- Double-speed mode (e.g. for high-speed dubbing)
- Pseudo double-speed mode (for power saving application)
- Digital speaker system mode including digital crossover filter.

1.3.3 SOUND MONITOR FEATURES

- Spectrum analyzer for seven different frequency ranges
- Digital silence detection. Level (−48 dB to ∞ dB, in steps of 3 dB) and duration (200 ms to 3.2 s, in steps of 200 ms at 44.1 kHz) programmable. Output via versatile pins.
- Peak level detection and readout to microcontroller (dB linear, 0 dB to −90 dB in steps of 1.5 dB)
- Digital overload detection. Level-programmable (dB linear, −1.5 dB to −46.5 dB, in steps of 3 dB). Output via versatile pins.
- Digital spectrum analyzer by combination of peak detection and 7-band selective filter
- Optional combination spectrum analyzer and overload detection for frequency-dependent overload detection.

2 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1546T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

3 QUICK REFERENCE DATA

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	note 1	3.8	5.0	5.5	V
I_{DDD}	digital supply current	note 2	–	40	–	mA
I_{DDA}	analog supply current	note 2	–	5.5	–	mA
I_{DDO}	operational amplifier supply current	note 2	–	6.5	–	mA
I_{DDX}	clock circuitry supply current	note 2	–	1	–	mA
$V_{FS(rms)}$	full-scale output voltage (RMS value)	V_{DD} = 5 V	1.425	1.5	1.575	V
(THD+N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level	–	–88	–81	dB
			–	0.004	0.009	%
		at –60 dB signal level; A-weighted	–	–44	–40	dB
S/N	signal-to-noise ratio at bipolar zero	A-weighted; at code 00000H	100	108	–	dB
t_{dg}	group delay	f_s = sample rate; normal-speed	–	$\frac{24}{f_s}$	–	s
BR	input bit rate at data input	f_s = 48 kHz; normal-speed	–	–	3.072	Ms^{-1}
		f_s = 48 kHz; double-speed	–	–	6.144	Ms^{-1}
f_{sys}	system clock frequency		6.4	–	18.432	MHz
TC_{FS}	full-scale temperature coefficient at analog outputs (V_{OL} and V_{OR})		–	$\pm 100 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–20	–	+70	°C

Notes

1. All V_{DD} and V_{SS} pins must be connected to the same supply or ground respectively.
2. Measured at input code 00000H and V_{DD} = 5 V.

4 GENERAL DESCRIPTION

The TDA1546T is the first Bitstream Continuous Calibration digital-to-analog converter (BCC-DAC) to feature unique signal processing functions. In addition to the basic functions of digital filtering and digital-to-analog conversion, it offers such advanced digital signal processing functions as volume control, tone control, bass boost, peak or spectrum analyzer readout and many more convenient functions. The digital processing features are of high sound quality due to the wide dynamic range of the bitstream conversion technique.

The TDA1546T accepts I²S-bus data input formats with word lengths of up to 20 bits and various Japanese serial data input formats with word lengths of 16, 18 and 20 bits. The circuit can operate as a master or slave with different system clocks ($256f_s$ or $384f_s$) and is therefore, eminently suitable for use in various applications such as DCC, CD, DAT and MD.

The range of applications is further extended by an incorporated Digital Speaker System mode (DSS) with digital crossover filter.

Four cascaded FIR filters and a sample-and-hold function increase the oversampling rate from $1f_s$ to $96f_s$ ($384f_s$ system clock) or $128f_s$ ($256f_s$ system clock). A second-order noise shaper converts this oversampled data to a bitstream for the 5-bit DACs.

The DACs are of the continuous calibration type and incorporate a special data coding technique, which contributes to a high signal-to-noise ratio and dynamic range.

On-board amplifiers convert the output current to a voltage signal capable of driving a line output. Externally connected capacitors perform the required first-order filtering. Additional post filtering is not required.

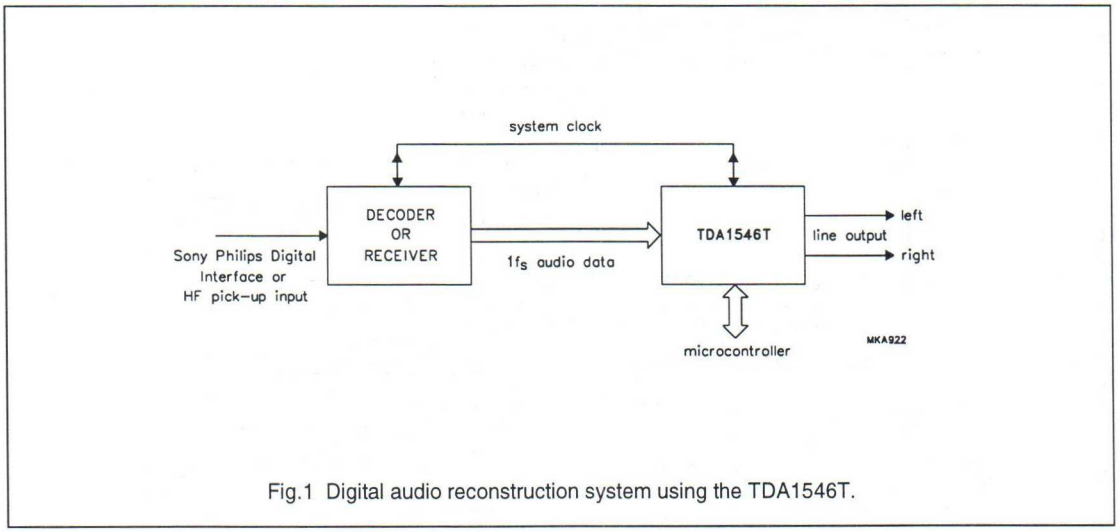


Fig.1 Digital audio reconstruction system using the TDA1546T.

5 BLOCK DIAGRAM

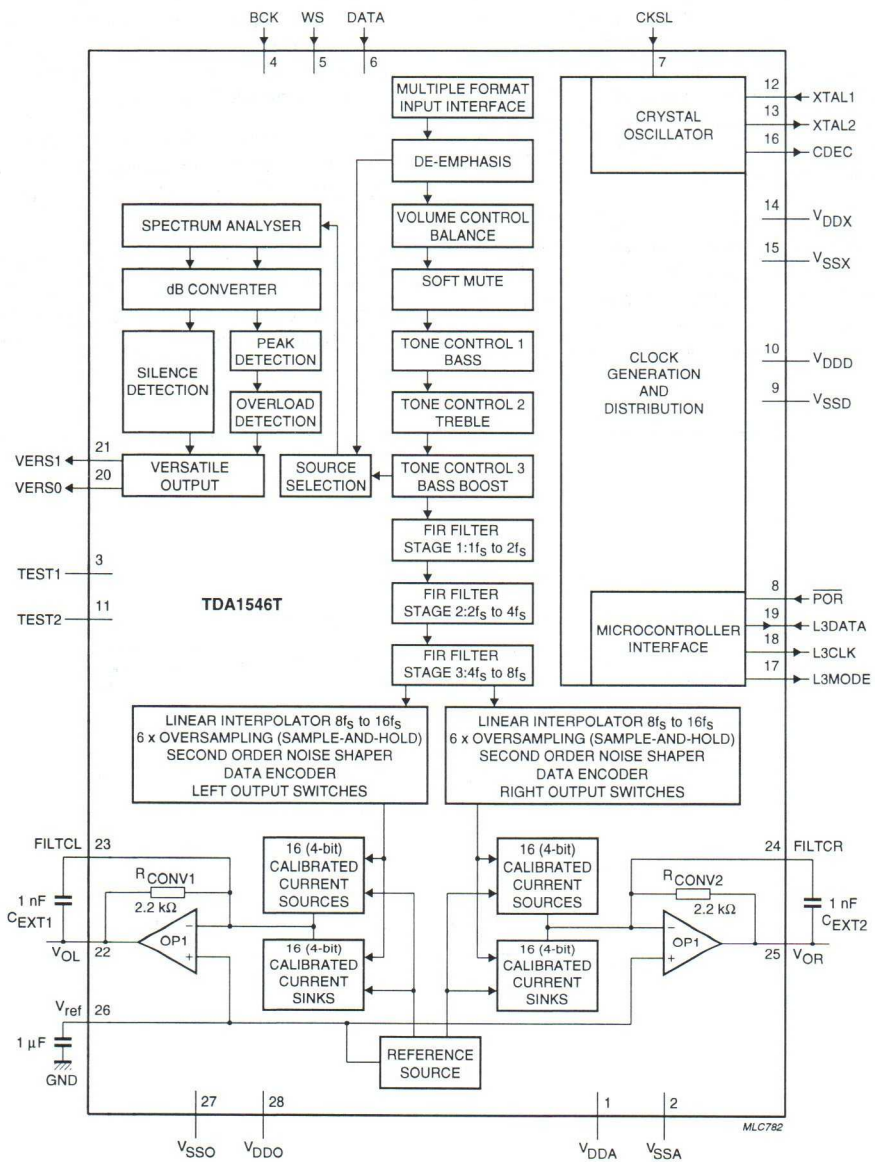


Fig.2 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
V_{DDA}	1	Analog supply voltage
V_{SSA}	2	Analog ground
TEST1	3	Test input 1. This pin should be connected to ground.
BCK	4	Bit clock input
WS	5	Word select input
DATA	6	Data input
CKSL	7	System clock frequency selection input
$\overline{POR}$	8	Power-on reset (active LOW). Internal pull-up resistor allows timed operation in combination with external capacitor.
V_{SSD}	9	Digital ground
V_{DDD}	10	Digital supply voltage
TEST2	11	Test input 2. This pin should be connected to ground.
XTAL1	12	Crystal oscillator input in master mode or external clock input in slave mode
XTAL2	13	Crystal oscillator drive output to crystal
V_{DDX}	14	Crystal oscillator supply voltage
V_{SSX}	15	Crystal oscillator ground
CDEC	16	System clock output
L3MODE	17	Identification of the L3-bus operation mode
L3CLK	18	Bit clock for synchronization of microcontroller data transfer
L3DATA	19	Bidirectional data line intended for control data from the microcontroller and peak data from the TDA1546T
VERS0	20	Versatile output 0 for silence or overload detection. Can be used to drive an LED.
VERS1	21	Versatile output 1 for silence or overload detection. Can be used to drive an LED.
V_{OL}	22	Left channel audio voltage output
FILTCL	23	Capacitor for left channel first-order filter function should be connected between this pin and V_{OL} (pin 22).
FILTCR	24	Capacitor for right channel first-order filter function should be connected between this pin and V_{OR} (pin 25).
V_{OR}	25	Right channel audio voltage output
V_{ref}	26	Decoupling pin for internal reference voltage, $\frac{1}{2}V_{DDA}$ (typ)
V_{SSO}	27	Internal operational amplifier ground
V_{DDO}	28	Internal operational amplifier supply voltage

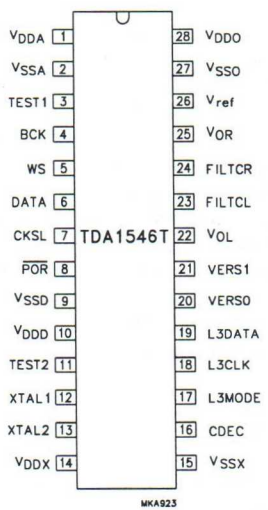


Fig.3 Pin configuration.

7 FUNCTIONAL DESCRIPTION

The TDA1546T CMOS digital-to-analog bitstream converter incorporates an up-sampling digital filter and noise shaper which increase the oversample rate of $1f_s$ input data to $128f_s$ in the normal-speed mode. This high-rate oversampling, together with the 5-bit DAC, enables the filtering required for waveform smoothing and out-of-band noise reduction to be achieved by simple first-order analog post-filtering.

In the double-speed mode, the input sample frequency is twice that of the normal-speed mode, as is the signal bandwidth. The TDA1546T is able to distinguish between the two modes (by means of a special programming bit), so that in the double-speed mode, only half the amount of oversampling is applied, and digital filtering is applied over double the bandwidth compared to normal-speed. Thus in the double-speed mode, the input sample rate of 1fs input data is up-sampled by a factor $64f_s$, achieving the same absolute output sample frequency as in normal-speed mode.

In the block diagram, Fig.2, a general subdivision into main functional Sections is illustrated. The actual signal processing takes place in the digital signal processing block. The two blocks named microcontroller interface and clock generation and distribution fulfil a general auxiliary function to the audio data processing path. The microcontroller interface provides access to all the blocks that require, or allow, configuration or selection and processes the data readout from the peak detection block, all via a simple three-line interface. The clock generation and distribution section, which is driven by the external system clock or crystal oscillator, provides the data processing blocks with time bases and controls the system mode dependent frequency settings. The following sections give detailed explanations of the operation of each block and their setting options processed by the microcontroller interface, the use of the microcontroller interface and of the operation of the clock section with its various system settings.

7.1 Clock generation and distribution

The TDA1546T has an internal clock generator that may be used by connecting a crystal of 11.2896 MHz ($256f_s$) or 16.9344 MHz ($384f_s$) between pins XTAL1 and XTAL2. This mode is used when the TDA1546T is the master in the system. The circuit diagram of Fig.4 shows the typical connection of the external oscillator circuitry for master mode operation.

Alternatively, the TDA1546T can also operate in slave mode. Figure 5 shows how to connect for slave mode operation. In this mode, pin XTAL1 receives an input clock of 256 or $384f_s$ (f_s = 32, 44.1 or 48 kHz) and voltage levels of 0 V to 5 V by AC coupling and attenuation.

The CDEC output (pin 16) contains a buffered version of the system clock for external use. The clock selection pin CKSL is used to select between system clock frequency ratios. Its effect is shown in Table 1.

Table 1 System clock selection

PIN CKSL	SYSTEM CLOCK	CDEC OUTPUT
0	$256f_s$	$256f_s$
1	$384f_s$	$384f_s$

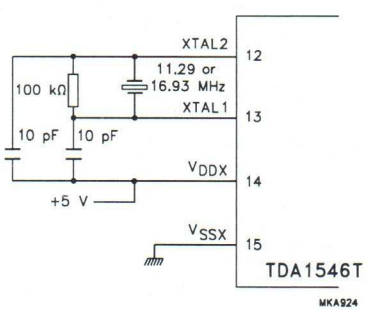


Fig.4 External crystal oscillator circuit.

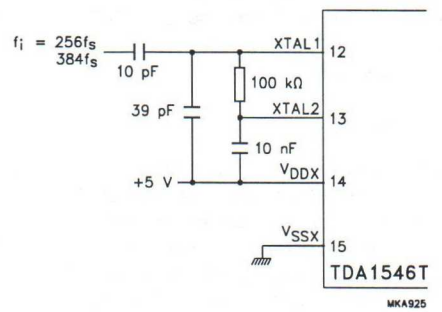


Fig.5 External clock input connection.

7.2 Power-on reset

The internal register file of the TDA1546T is initialized by a power-on reset sequence which can be instigated via the $\overline{POR}$ input pin 8. A LOW input on $\overline{POR}$ causes the reset sequence to be active. This input has an internal resistance to V_{DD} to allow for passive use with only an external capacitor connected between this pin and ground. For correct detection by the TDA1546T internal controller, the system clock must be running, and $\overline{POR}$ should remain LOW for at least one audio sample period before being returned HIGH. Following detection another audio sample period is needed to complete the initialization procedure, after which the values of the various control bits in the internal register file are at their predefined initial values (see Section 7.3).

7.3 Microprocessor interface

The exchange of data and control information between the TDA1546T and a microcontroller is accomplished through a serial hardware interface comprising the following pins:

L3DATA: microcontroller interface bidirectional data line.

L3CLK: microcontroller interface clock line.

L3MODE microcontroller interface mode line.

Information transfer through the microcontroller bus is organized according to the so-called 'L3' format, in which two different modes of operation can be distinguished; address mode and data transfer mode.

The address mode is required to select a device communicating via the L3-bus and to determine the direction of data transfer in data transfer mode. Data transfer for the TDA1546T can be in two directions, input to the TDA1546T to program its sound processing and other functional features, and output from the TDA1546T for transfer of audio peak data, which it has acquired and processed, to the system microcontroller.

7.3.1 Address mode

The address mode is used to select a device for subsequent data transfer and to define the direction of that transfer as well as the source or destination registers. The address mode is characterized by L3MODE being LOW and a burst of 8 clock pulses on L3CLK, accompanied by 8 data bits. The fundamental timing is shown in Fig.6.

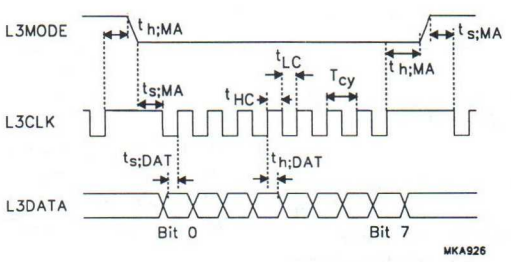


Fig.6 Timing address mode.

Data bits 0 to 1 indicate the type of the subsequent data transfer as shown below in Table 2. The direction of the channel status and user data transfers depends on the transmit/receive mode.

Table 2 Selection of data exchange

BIT 1[1]	BIT 0	TRANSFER	DIRECTION
X	0	data to TDA1546T	input
X	1	data from TDA1546T	output

Note

1. Where X = don't care.

Data bits 2 to 7 represent a 6-bit device address, with bit 7 being the MSB and bit 2 the LSB. The address of the TDA1546T is 000100 (bit 7 to bit 2). In the event that the TDA1546T receives a different address, it immediately 3-states the L3DATA pin and deselects its microcontroller interface logic. A dummy address of 000000 is defined for the deselection of all devices that are connected to the serial microcontroller bus.

7.3.2 Data transfer mode

The selection performed in the address mode remains active during subsequent data transfers, until the TDA1546T receives a new address command. The fundamental timing of data transfers is shown in Fig.7, where L3DATA denotes the data from the TDA1546T to the microcontroller (L3DATA write). The timing for the opposite direction is essentially the same as in the address mode (L3DATA read). The maximum input clock and data rate is $64f_s$ (or $32f_s$ when in the double-speed mode).

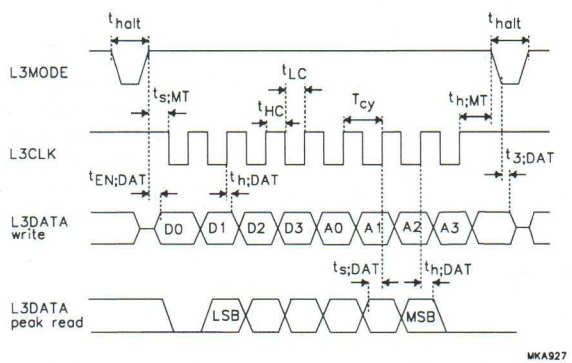


Fig.7 Timing for data transfer mode.

All transfers are bytewise, i.e. they are based on groups of 8 bits. Data will be stored in the TDA1546T after the eighth bit of a byte has been received.

A multi-byte transfer is illustrated in Fig.8. The definition of the L3 protocol allows for a so-called "halt" mode, as some devices which are expected to connect to the same microcontroller bus lines may require an indication of when 8 bits have been transferred. This halt mode option is implemented in the TDA1546T, meaning that subsequent byte transfers must be separated by a period identified as halt mode. A halt mode period is characterized by the following conditions:
L3MODE = LOW, L3DATA = 3-state and L3CLK = HIGH.

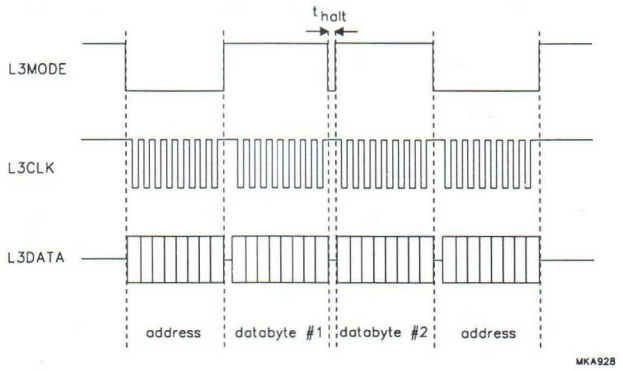


Fig.8 Multibyte transfer.

7.3.3 Organization and programming of the internal register file

Command data received from the microcontroller is stored in an internal register file (see Table 3) which is organized as a page of 16 registers, each containing a 4-bit command data word (D3 to D0).

Access to the words in the register file involves selection of the address of a register location (by means of A3, A2, A1 and A0). A second page of 4 registers is accessible by means of the extended address register bits (EA2, EA1 and EA0) and extended data register bits (ED3, ED2, ED1 and ED0).

Table 3 Microcontroller control register file

ADDRESS				D3	D2	D1	D0	INITIAL STATE	USED FOR
A3	A2	A1	A0						
0	0	0	0	BAL3	BAL2	BAL1	BAL0	1 1 1 1	balance left
		0	1	BAR3	BAR2	BAR1	BAR0	1 1 1 1	balance right
		1	0	VC3	VC2	VC1	VC0	1 1 1 1	volume control
		1	1	VC7	VC6	VC5	VC4	1 1 1 0	volume control
0	1	0	0	FT3	FT2	FT1	FT0	0 0 0 0	fade time
		0	1	DSS	FP2	FP1	FP0	0 0 0 0	digital speaker system; 3 × band-pass
		1	0	OVER3	OVER2	OVER1	OVER0	1 1 1 1	overload
		1	1	SIL3	SIL2	SIL1	SIL0	0 0 0 0	silence level
1	0	0	0	SILT3	SILT2	SILT1	SILT0	0 0 0 0	silence time
		0	1	MUTE	OUTS1	OUTS0	SPOS	0 0 0 0	mute; 2 × output scaling; peak source
		1	0	SCT3	SCT2	SCT1	SCT0	0 1 1 1	treble
		1	1	SCB3	SCB2	SCB1	SCB0	0 1 1 0	bass
1	1	0	0	SCBB3	SCBB2	SCBB1	SCBB0	0 0 0 0	bass boost
		0	1	FSO1	FSO0	DEMC1	DEMC0	0 0 0 0	2 × reserved; 2 × de-emphasis
		1	0	ED3	ED2	ED1	ED0	1 1 1 1	extended data
		1	1	RUNFA	EA2	EA1	EA0	1 1 1 1	run fade; extended address

Table 4 Extended microcontroller control register file

EXTENDED ADDRESS			ED3	ED2	ED1	ED0	INITIAL STATE	USED FOR
EA2	EA1	EA0						
0	0	0	INS1	INS0	DSM	CLRM	0 0 0 0	input format; double-speed mode; clear memory
0	0	1	PVIV1	PVIV0	PINM1	PINM0	0 0 1 0	polarity and function versatile output pins
0	1	0	LONLY	TRI	ACDT	DCDT	0 0 1 1	left only; 3 × reserved
0	1	1	CLKIV	CLKON	DYC1	DYC0	0 0 0 0	4 × reserved

The following programming values for the various control words in the register file are given below.

7.3.3.1 Volume control register bits: BAL3 to BAL0 and BAR3 to BAR0

Balance: a 4-bit value to program left channel attenuation (BAL3 to BAL0) and a 4-bit value to program right channel attenuation (BAR3 to BAR0). The range is 0 dB to −22.5 dB in steps of 1.5 dB (see Section 7.7.1).

7.3.3.2 Volume control register bits: VC7 to VC0 and FT3 to FT0

Volume control set number: an 8-bit value to program volume control coefficient set (6 dB to −90 dB, in steps of 0.375 dB, VC7 to VC0); a 4-bit value to program fade time (6 ms to 22.4 s, FT3 to FT0) (see Section 7.7.2).

7.3.3.3 Volume control register bit: MUTE

Digital soft mute control bit: logic 1 to activate mute and logic 0 to deactivate (see Section 7.7.3).

7.3.3.4 Volume control register bit: RUNFA

Function control bit: logic 1 to activate the volume control (after new fade time and/or volume control setting) (see Section 7.7.2.).

7.3.3.5 Sound monitor register bits: FP2 to FP0

Frequency range control bits (see Section 7.9.1).

7.3.3.6 Sound monitor register bits: OVER3 to OVER0

Overload detection level (dB linear; 0 dB to −45 dB, in steps of −3 dB) (see Section 7.9.5).

7.3.3.7 Sound monitor register bits: SIL3 to SIL0 and SILT3 to SILT0

Digital silence set numbers: a 4-bit value to program digital silence detection level −48 dB to ∞ dB (SIL3 to SIL0) and a 4-bit value to program digital silence duration 0.2 s to 3.2 s (SILT3 to SILT0) (see Section 7.9.4).

7.3.3.8 Sound monitor register bit SPOS

This bit controls the position of the spectrum analyzer. When SPOS = 1 the position of spectrum analyzer precedes the tone control sections. When SPOS = 0 the position of the spectrum analyzer succeeds the tone control sections.

7.3.3.9 Sound processing register bit: DSS

Digital speaker system programming bit (see Section 7.8.6).

7.3.3.10 Sound processing register bits: SCT3 to SCT0

Treble coefficient set number: a 4-bit value to program digital treble coefficient set (see Section 7.8.2).

7.3.3.11 Sound processing register bits: SCB3 to SCB0

Bass coefficient set number: a 4-bit value to program digital bass coefficient set (see Section 7.8.3).

7.3.3.12 Sound processing register bits: SCBB3 to SCBB0

Bass boost coefficient set number: a 4-bit value to program digital bass boost coefficient set (see Section 7.8.4). This is also used for digital speaker system configuration (see Section 7.8.6).

7.3.3.13 Sound processing register bits: DEMC1 and DEMC0

De-emphasis function enable and f_s selection bits (see Section 7.8.1).

7.3.3.14 Sound processing register bit: DSM

Double-speed mode control bit: logic 1 to activate double-speed mode, logic 0 to deactivate (see Section 7.6).

7.3.3.15 Miscellaneous register bits: ED3 to ED0

Extended microcontroller control data (see Table 4).

7.3.3.16 Miscellaneous register bits: EA2 to EA0

Extended microcontroller register address (see Table 4).

7.3.3.17 Miscellaneous register bits: INS1 and INS0

Input format selection control bits (see Section 7.4).

7.3.3.18 Miscellaneous register bits: PVIV1, PVIV0 and PINM1, PINM0

These bits control the polarity (PVIV1 and PVIV0) and the output mode (PINM1 and PINM0) of the versatile output pins VERS1 and VERS0 (see Section 7.9.6).

7.3.3.19 Miscellaneous register bit: CLRM

Clear memory register bit: logic 1 to clear entire filter delay line (approximately 2 audio samples).

7.3.3.20 Miscellaneous register bits: OUTS1 and OUTS0

Output scaling factor control bits (see Table 10).

7.3.3.21 Miscellaneous register bit: LONLY

"Left Only" programming bit for use with digital speaker system mode (see Section 7.8.6).

7.3.3.22 Miscellaneous register bits: FSO1, FSO0, TRI, ACDT, DCDT, CLKIV, CLKON, DYC1 and DYC0

Register bits reserved for future use.

7.4 Multiple format input interface

Data input to the TDA1546T is accepted in four possible formats, I²S-bus (with word lengths of up to 20 bits), and LSB fixed formats of word lengths 16, 18 and 20 bits. As the resolution of the TDA1546T is 18 bits, input beyond this number does not affect the audio data processing. The general appearance of the permitted formats is given in Fig.9. The selection of a format is achieved through programming of the appropriate bits in the microcontroller register file. The truth table for these bits, INS1 and INS0, is given in Table 5. Characteristic timing for the input interface is given in the diagram of Fig.9.

Table 5 Input format programming

INS1	INS0	DATA INPUT FORMAT
0	0	I²S-bus format
0	1	LSB-justified format, 16 bits
1	0	LSB-justified format, 18 bits
1	1	LSB-justified format, 20 bits

7.4.1 Synchronization

For correct data input to reach the central controller of the TDA1546T, synchronization must be achieved on the incoming $1f_s$ I²S-bus or LSB justified format input signals. The incoming WS signal is sampled to detect whether its phase transitions belonging to left channel input occur at the correct synchronous timing instants. This sampling occurs at the TDA1546T internal clock rate. A correct phase transition of WS is expected after a fixed delay time of a previous correct transition, if not, the input will be regarded as out-of-lock. When such a condition occurs, the internal controller is instructed to wait for a period of 16 system clock cycles during which the expected WS transition must occur to achieve synchronization. The wait action is repeated as often as necessary until synchronization is achieved.

To allow for slight disturbances, which would otherwise cause unnecessarily frequent resets, the critical WS transitions are expected within a tolerance window (rather than at one particular timing instant) of 32 system clock cycles. The phase, however, may vary according to the instant upon which synchronization has been achieved. The word select phase transition marking the start of right channel input data is expected after a fixed delay of the left channel synchronized WS transition, meaning that the input WS signal should be symmetrical in time (50% duty cycle measured in units of system clock cycles).

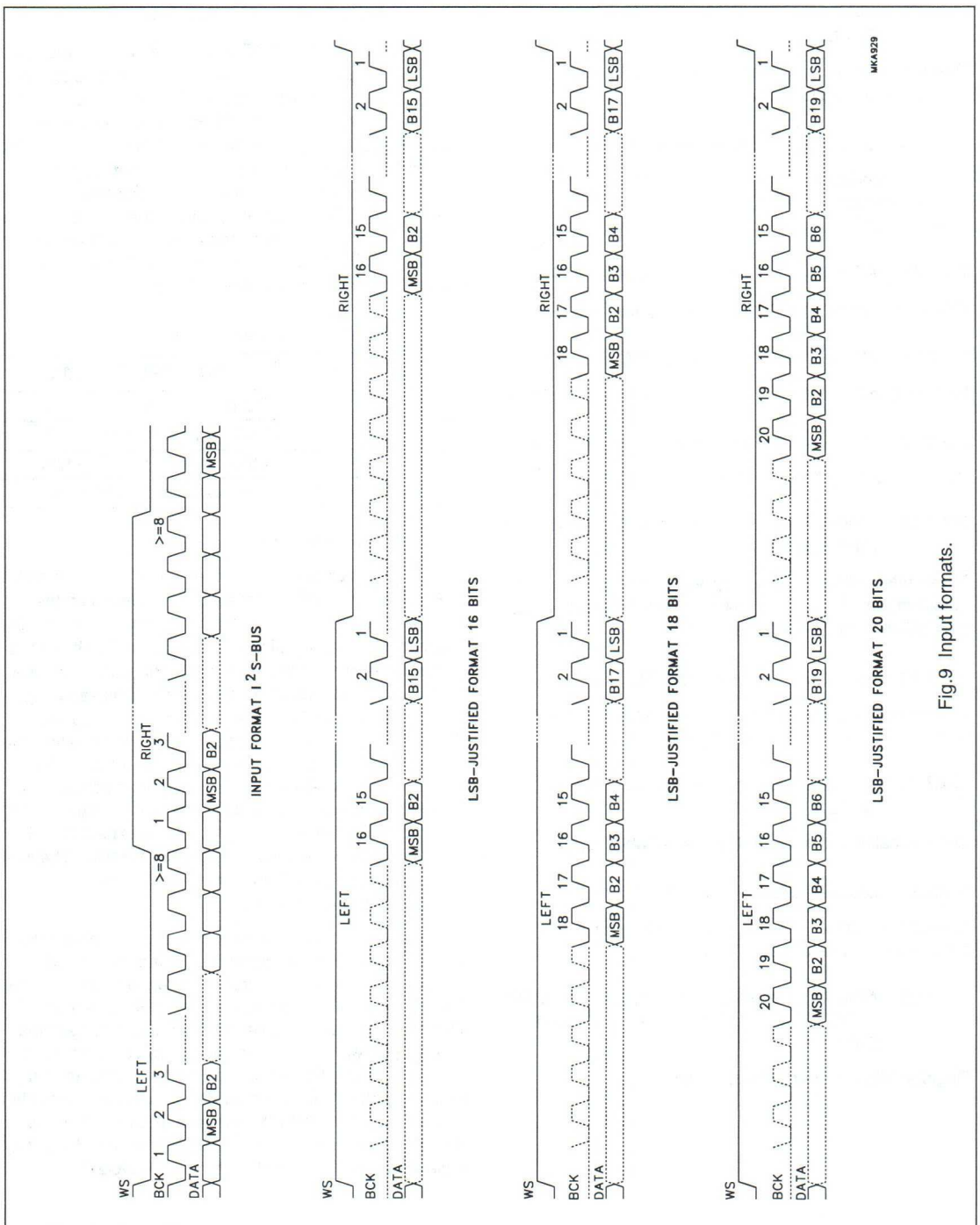


Fig.9 Input formats.

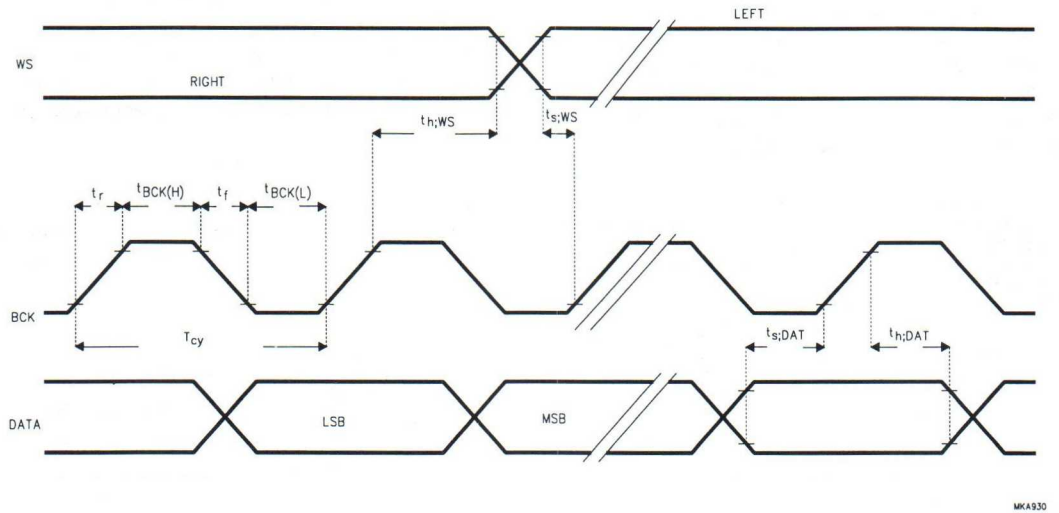


Fig.10 Timing of input signals.

7.5 Normal-speed mode

In the normal-speed mode the oversampling filter consists of:

- A 75th-order half-band low-pass FIR filter which increases the oversampling rate from 1 time to 2 times.
- An 11th-order half-band low-pass FIR filter which increases the oversampling rate from 2 times to 4 times.
- An 7th-order half-band low-pass FIR filter which increases the oversampling rate from 4 times to 8 times.
- A linear interpolation section which increases the oversampling rate to 16 times. This removes the spectral components around $8f_s$.
- A sample-and-hold section which provides another 6 times oversampling to 96 times. The zero-order hold characteristic of this sample-and-hold section plus the first-order analog filtering remove the spectral components around $16f_s$.

7.6 Double-speed mode

The double-speed is controlled by the register control bit DSM. When this bit is active HIGH the device operates in the double-speed mode. In the double-speed mode the oversampling filter consists of:

- A 51st-order half-band low-pass FIR filter which increases the oversampling rate from 1 time to 2 times.
- A 7th-order half-band low-pass FIR filter which increases the oversampling rate from 2 times to 4 times.
- A linear interpolation section which increases the oversampling rate to 8 times. This removes the spectral components around $4f_s$.
- A sample-and-hold section which provides another 6 times oversampling to 48 times. The zero-order hold characteristic of this sample-and-hold section plus the first-order analog filtering removes the spectral components around $8f_s$.

7.6.1 DOUBLE-SPEED MODE FEATURES

In the normal-speed mode all of the sound processing features such as those listed in the "Features" are available. However, the use of double-speed mode cuts down on the number of options due to the fact that a smaller cycle budget is available to the internal feature controller. Table 6 gives the availability of the different features in the double-speed mode.

Table 6 Feature status in double-speed mode

FEATURE	AVAILABLE	REMARKS
Balance	yes	
Volume	yes	adapted scale: range from –96 dB to 0 dB
Fade	no	volume change will be instantaneous
Band-pass filter	no	fixed to flat response
Overload detection	no	
Silence detection	no	
Mute	yes	
Peak position	no	fixed to before
Treble, Bass	no	
Bass boost	yes	
De-emphasis	yes	
Clear memory	yes	
Versatile pins	yes	although no detection takes place these pins respond to polarity setting
Peak readout	yes	

Because of the shift in scale of the volume control between normal and double-speed mode, a step in volume of 6 dB on switchover in either way should be compensated for by adjusting the volume during a preferably muted transition period.

7.6.2 LOW-POWER OPTION USING DOUBLE-SPEED MODE

The double-speed mode feature can also be used to cut down on power requirements. When the TDA1546T is switched to the double-speed mode using control bit DSM, and the system clock frequency is halved simultaneously, the filters will operate correctly on data input at normal-speed. The same feature restrictions as in the double-speed mode apply, as does the filter performance specified for double-speed mode. The current consumption of the digital supply voltage is halved because of the lower absolute clock speed. In terms of conversion accuracy of the digital-to-analog converter section, some performance will however be sacrificed.

7.7 Volume control features

Features related to volume control are the digital balance control, digital volume control with fade function and the digital soft-mute. Their operation is described below.

7.7.1 DIGITAL BALANCE

Table 7 Digital balance

BAL3 TO BAL0 BAR3 TO BAR0	LEVEL (dB)
1 1 1 1	0
1 1 1 0	–1.5
....	...
0 0 0 1	–21.0
0 0 0 0	–22.5

The balance value from 1111 to 0000 can be obtained using the following equation;
Balance = –1.5 dB × (15 – balance setting)

At extremely low volume settings (see Section 7.7.2) the range of effect of the balance control will be limited. The balance control effect will not go beyond an overall attenuation of 89.55 dB (balance plus volume control).

7.7.2 DIGITAL VOLUME CONTROL WITH FADE FUNCTION

One of the features of the TDA1546T is an advanced digital volume control with inherent fading function. Only the desired volume and the fade speed need to be instructed to the TDA1546T, via the microcontroller interface. The single-bit flag RUNFA can then be used to inhibit or execute the volume change operation. When RUNFA = 0, the volume control settings can be changed without effect on the output. When RUNFA is then set to 1, the TDA1546T autonomously performs an automatic fade-in or fade-out to the desired volume by a natural, exponential approach. It allows for volume control to an accuracy of 0.375 dB from a gain of 6 dB of full-scale to –90 dB in normal-speed, and a range of 0 dB of full-scale to –96 dB in double-speed mode (see Tables 8 and 9).

In normal-speed operation the fade time can be set over a wide range, varying from 6 ms to over 20 seconds for a complete fade. The fade time is completely determined by the fade time setting and is independent of the amount of volume change programmed. This means that a smaller volume step will take the same amount of time but using a less steep slope than a larger volume change with the same fade time setting.

In the double-speed mode the fade option is not available. Regardless of the current fade speed setting, a volume change in double-speed mode will take effect immediately, i.e. the next audio sample instant. Volume control data is in 2 nibbles and can be set in 256 steps. The relationship between command and output is shown in Tables 8 and 9.

Table 8 Volume control

VC7 TO VC0	VC (DEC)	VOLUME LEVEL	
		NS	DS
1111 1111	255	6.02	0
1111 1110	254	5.64	−0.37
....	...	....	....
1111 0000	240	0.37	−5.64
1110 1111	239	0.00	−6.02
....	...	....	....
0000 0001	1	−89.55	−95.57
0000 0000	0	−∞	−∞

Table 9 Fade control

FT3 TO FT0	FT (DEC)	FADE TIME AT 44.1 kHz (s)
0000	0	0.006
0001	1	0.2
0010	2	0.6
....	...	....
1110	14	19.6
1111	15	22.4

The gain value ranging from 1111 1111 to 0000 000 can be converted to its logarithmic counterpart by the following equations:

Normal-speed mode:

$$G = (\text{volume setting} - 239) \times \left[\frac{5 \times (\log 2)}{4}\right]$$

Example: attenuate data for 1111 11110:

$$A = (254 - 239) \times \left[\frac{5 \times \log 2}{4}\right] = 5.64 \text{ dB}$$

Double speed mode:

$$G = (\text{volume setting} - 255) \times \left[\frac{5 \times (\log 2)}{4}\right]$$

Example: attenuate data for 1111 11110:

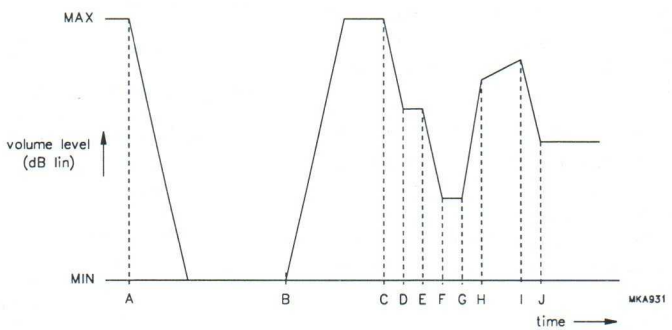
$$A = (254 - 255) \times \left[\frac{5 \times \log 2}{4}\right] = -0.37 \text{ dB}$$

The fade time from 0000 to 1111 can be converted by using the following equation:

$$\text{Fade time} = \left\{\frac{[(FT + 1) \times (FT \times 16 + 1)] \times 256}{f_s}\right\}$$

Example: fade time for 0010 at f_s = 44.1 kHz;
fade time = 3 × 33 × 256/44100 = 0.57 s

In Fig.11, a few fading examples illustrate the operation of the TDA1546T advanced digital volume control.



(1) A = fade-out to zero volume (VC = 0; RUNFA = 1).
(2) B = fade-in to maximum volume (RUNFA = 0; VC = 256; RUNFA = 1).
(3) C = volume decrease (RUNFA = 0; VC = XXX; RUNFA = 1).
(4) D = volume regulation override by resetting RUNFA to 0.
(5) E = volume regulation resumed by resetting RUNFA to 1.
(6) F = volume regulation stops at programmed level XXX.
(7) G = fade-in to maximum level (RUNFA = 0; VC = 256; RUNFA = 1).
(8) H = change in fade time (RUNFA = 0; FT = xxx; RUNFA = 1).
(9) I = fade-out to lower volume level and fade time change (RUNFA = 0; new VC; new FT; RUNFA = 1).
(10) J = volume regulation stops at programmed level.
Note: for illustration only, axes vary in scale.

Fig.11 Volume control example.

7.7.3 Digital soft-mute

Soft mute is controlled by the microcontroller register file bit MUTE. When the bit is active HIGH the value of the samples is decreased smoothly to zero following a cosine curve. To step down the value of the data 32 coefficients are used, each one being used 32 times before stepping onto the next. This amounts to a mute transition time of 23 ms at f_s = 44.1 kHz. When the MUTE bit is LOW, the samples are returned to the full level again following the same cosine curve in reverse order. Mute is synchronized to the sample clock, so that operation always takes place on complete samples.

7.7.4 Scaling and polarity of the digital up-sampling filter

The scaling factor of the digital up-sampling filter can be selected by means of register file bits OUTS1 and OUTS0. Only those modes controlled by bit OUTS0 are actually useful, the other two are reserved modes and should not be used.

In the configuration with the default initialization (OUTS0 = 0), the TDA1546T is inverting, meaning that a positive pulse contained in the digital input data is converted to a negative pulse on the analog outputs. This polarity and scaling is identical to that used in TDA1305T. The TDA1546T can be made non-inverting by setting bit OUTS0 in the microcontroller register file. The complete truth table for these bits is shown in Table 10.

Table 10 Special control register bits

OUTS1	OUTS0	MODE	SCALING
0	0	TDA1305T equivalent	−0.9
0	1	non-inverting	+0.9
1	0	reserved	−0.66
1	1	reserved	−0.99

7.8 Sound processing related features

7.8.1 De-emphasis filter

The TDA1546T incorporates selectable digital de-emphasis filters, dimensioned to produce the de-emphasis frequency characteristics for each of the three possible sample rates 32, 44.1 and 48 kHz. With its 18-bit dynamic range, the digital de-emphasis of the TDA1546T is a convenient and component-saving alternative to analog de-emphasis.

Selection of the de-emphasis filters is performed via the microcontroller interface, bits DEMC1 and DEMC0. The programming is given in Table 11.

Table 11 De-emphasis mode programming

DEMC1	DEMC0	DE-EMPHASIS FUNCTION
0	0	de-emphasis disabled
0	1	de-emphasis for f_s = 32.0 kHz
1	0	de-emphasis for f_s = 44.1 kHz
1	1	de-emphasis for f_s = 48.0 kHz

7.8.2 Treble

A digital treble gain (up to 12 dB in steps of 1.5 dB or cut down to −10.5 dB in steps of 1.5 dB) can be applied to boost or attenuate high-range signal content. The microcontroller bits SCT3 to SCT0 select the treble characteristic to be applied, the effect of which is shown in Table 12. The programmable treble filter is a first-order shelving type with a fixed corner frequency of 2.1 kHz. In the "flat" position the treble stage has no influence on the audio signal path. Because of the possibility of treble boost beyond the available digital headroom causing overload of high frequency range signals, the higher positive treble boost values should generally be used in conjunction with an approximately corresponding attenuation using the volume control function.

7.8.3 Bass

Digital bass control can be applied under control from the microcontroller via control bits SCB3 to SCB0 (see Table 12) to achieve a moderate bass enforcement or attenuation. The programmable bass filter is a first-order shelving type with a fixed corner frequency of 500 Hz. In the "flat" position the bass stage has no influence on the audio signal path. Higher bass settings should generally be compensated by approximately equal attenuation using the volume control to avoid digital overload of basses.

7.8.4 Bass boost

A strong bass boost effect, which is useful in compensating for poor bass response of portable headphone sets, is implemented digitally in the TDA1546T and can be controlled in 14 steps using the microcontroller bits SCBB3 to SCBB0. Valid settings range from "flat" (no influence on audio) to +37 dB with step sizes varying from 3 dB (lower boosts) to 2.5 dB to 2 dB (higher boosts). The SCBB value 15 is a reserved value and should not be used. (see Table 12). The programmable bass boost filter is a second-order shelving type with a fixed corner frequency of 250 Hz and has a Butterworth characteristic. Because of the exceptional amount of programmable gain, bass boost should be used in conjunction with adequate prior attenuation, using the volume control. The bass stage and the bass boost stage operate independently so that the ultimately attainable gain for low frequencies may reach a total boost of approximately 50 dB.

7.8.5 Digital dynamic bass boost, digital loudness and other dynamic applications of tone control

Because of the integration of volume control, tone control and level monitoring functions in the TDA1546T, a wide range of dynamic tone and level control applications is made available. These can be defined in software by the user, thereby replacing and improving on components formerly used to perform these functions in the analog domain. Among these applications the most popular are dynamic bass boost and loudness. Because the volume setting is known in the system controller, it can, for instance, be used directly to determine an appropriate amount of bass boost. This avoids the signal level dependent 'sighing', 'pumping' and distortion effects typical of analog dynamic bass boost circuits. Depending on the headroom made available by the current volume setting, applying a bass boost of up to 30 dB, combined with a slight treble boost (up to 6 dB) will achieve a typical dynamic bass boost effect of high sound quality.

Digital loudness can be realized using the current volume setting to determine a suitable moderate bass gain (up to approximately 15 dB is typical of loudness) and treble gain (up to approximately 6 dB).

A further enhancement in dynamic tone control and signal adaptation can be achieved by using the peak monitoring function (either with a flat response or using the band-pass filters) or overload detection (which can also be made frequency-selective) in your dynamic tone control algorithm.

Table 12 Sound processing parameters

REGISTER BITS	TREBLE SCT3 TO SCT0 (dB)	BASS SCB3 TO SCB0 (dB)	BASS BOOST SCBB3 TO SCBB0 (dB)
0 0 0 0	−10.5	−9	flat
0 0 0 1	−9	−7.5	3
0 0 1 0	−7.5	−6	6
0 0 1 1	−6	−4.5	9
0 1 0 0	−4.5	−3	12
0 1 0 1	−3	−1.5	15
0 1 1 0	−1.5	flat	18
0 1 1 1	flat	1.5	21
1 0 0 0	1.5	3	23.5
1 0 0 1	3	4.5	26
1 0 1 0	4.5	6	28.5
1 0 1 1	6	7.5	31
1 1 0 0	7.5	9	33
1 1 0 1	9	10.5	35
1 1 1 0	10.5	12	37
1 1 1 1	12	13.5	reserved

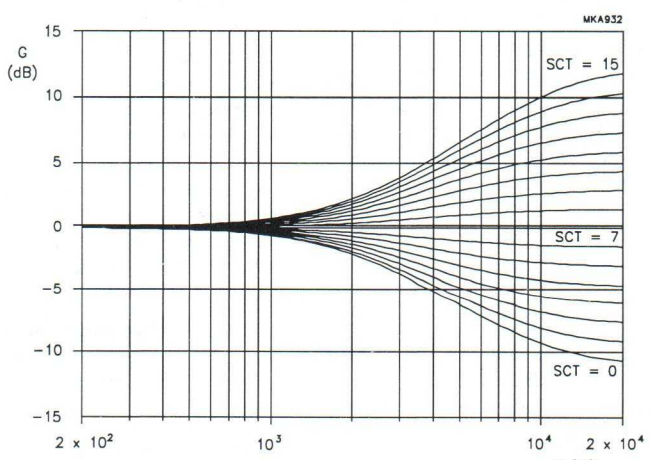


Fig.12 Treble frequency response.

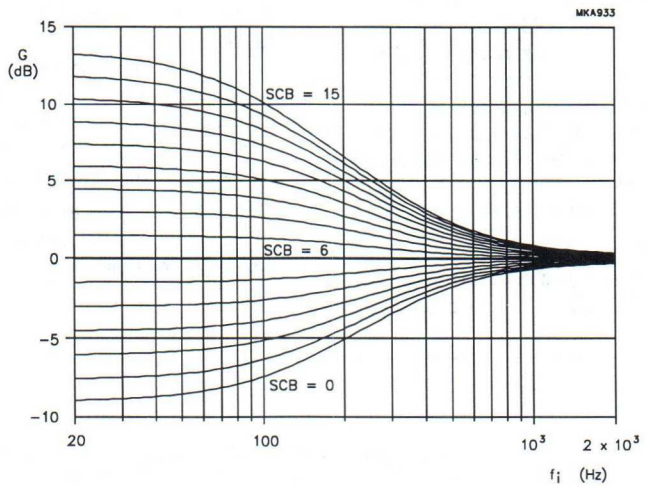


Fig.13 Bass frequency response.

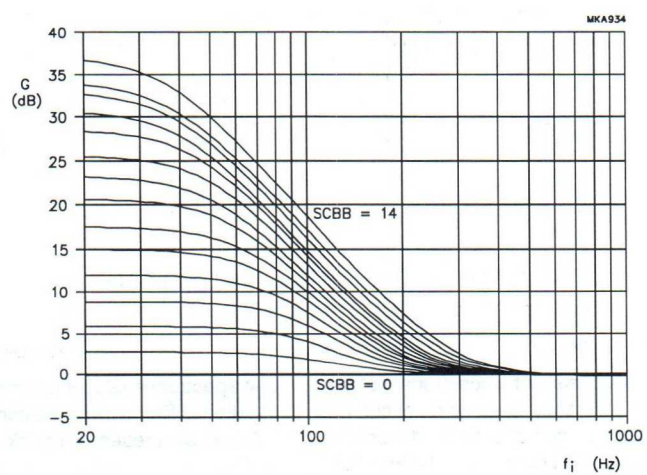


Fig.14 Bass boost frequency response.

7.8.6 DIGITAL SPEAKER SYSTEM MODE

The TDA1546T can be used as a two-way digital crossover filter and digital preamplifier in a digital speaker system. In the DSS mode, one TDA1546T is used per loudspeaker channel. The left channel of TDA1546T drives the amplifier for the low frequency transducer and the right channel drives the high-frequency power amplifier. The digital crossover filter is activated by setting the control bit DSS to 1 and the 4-bit bass boost value to its reserved value of 15. Figure 15 shows the frequency transfer function of the digital crossover filter.

The auxiliary bit LONLY (left only) can be set to enable a special internal channel-copying mode. The left-channel data input is copied internally to the right channel via the input data bus and the incoming right channel data is 'don't care'. This simplifies interfacing at the input data bus level. Direct connection of the WS line to the TDA1546T appoints the TDA1546T as the left channel processor, and placing an inverter in series with the WS input results in the processing of the right channel data only, thereby appointing the TDA1546T as right channel processor. Consequently, by using LONLY, the normal time-multiplexed I²S-bus or other format can be used rather than a dedicated left or right channel bus.

Due to the nature of the digital crossover filter, the digital speaker mode must be used with volume set to –0.375 dB (one unit step below 0 dB) to preclude any occurrence of digital clipping.

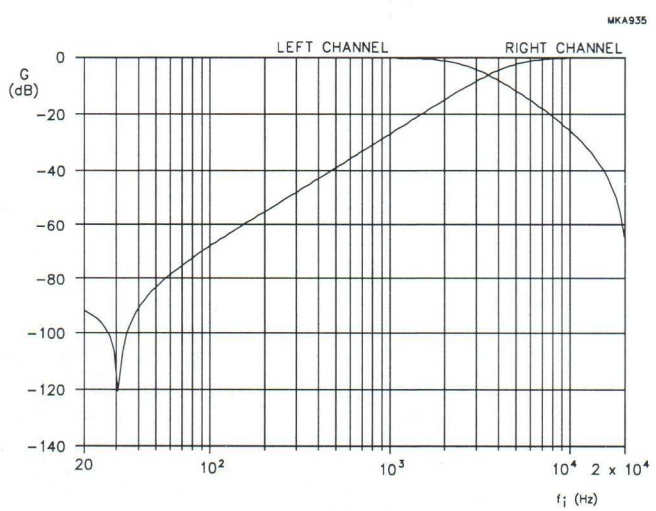


Fig.15 Digital crossover filter frequency response.

7.9 Sound monitor block

The sound monitor block consists of a spectrum analyzer, silence detection, peak detection, overload detection and versatile output pins. The position of the sound monitor block can be programmed using microcontroller bit SPOS. When SPOS = 1 the sound monitor block precedes the tone control sections. When SPOS = 0 the sound monitor block succeeds the tone control sections.

7.9.1 SPECTRUM ANALYZER

The spectrum analyzer is constructed of a second-order band-pass filter (where the centre frequency is selectable) followed by a resettable peak detector, silence detector and overload detector. The band-pass filter can be set to 7 different frequency bands plus one flat response. The 7 bands are equally spaced in the audio band with a ratio of 1:2.3, which is slightly wider than octave bands. The centre frequencies are given in Table 13.

Table 13 Spectrum analyzer frequency band

FP2	FP1	FP0	FREQUENCY BAND	SETTLING TIME TO –40 dB OR 1% (ms)
0	0	0	flat	–
0	0	1	0 to 99 Hz	30
0	1	0	189 Hz	16
0	1	1	435 Hz	5.6
1	0	0	1000 Hz	2.4
1	0	1	2300 Hz	1.1
1	1	0	5290 Hz	0.5
1	1	1	12200 Hz	0.2

To scan the whole audio band with one filter, the filter must be switched between the 7 bands. This switching causes a transient which takes time to settle. The settling time is dependent on the bandwidth and is slowest for the low frequency bands, e.g. the 189 Hz band takes approximately 16 ms to settle to 1% or –40 dB (i.e. the settling rate is 8 ms per 20 dB). For all bands except the 99 Hz band, the settling rate is inversely proportional to the bandwidth and therefore to the centre frequency. The 99 Hz filter behaves differently because it is, in essence, a first-order low-pass filter.

The settling time of the switchable band-pass filter calls for attention to waiting times when used in a spectrum analyzer application. A waiting time is necessary to allow the switching transient to settle. A "dummy" peak readout will then reset the peak detection register to zero, after which instant new frequency-dependent peak data can be accumulated. The time needed to accumulate valid peak information depends on the centre frequency and bandwidth of the band involved, thus a second waiting time will need to be implemented. A peak read action performed after this second waiting time will return an accurate output value.

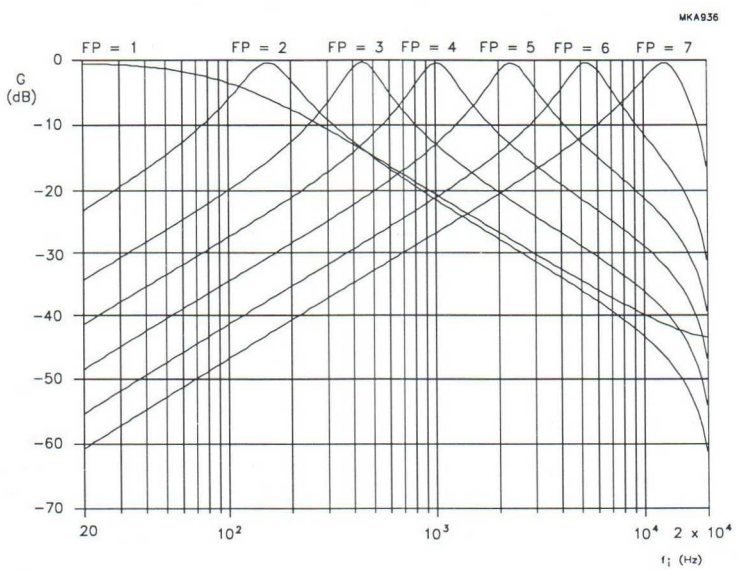


Fig.16 Spectrum analyzer frequency response.

7.9.2 dB CONVERTER

Before peak data is output, the detected value is converted from linear to a dB scale internally by the TDA1546T. This has the following advantages:

- ease calculation load on the system microcontroller
- optimal use of dynamic range of the readout
- facilitate manipulation of sound processing control levels in combination with peak readout levels, to allow for e.g. dynamic tone control.

The internal linear peak detection occurs with a resolution of 16 bits on the incoming left and right audio samples individually. This linearly acquired value is converted to dB's as shown in Table 14. Because of quantization of the linear code, accuracy is lower for the very lowest detected peak values. Some values in the lower range of the dB scale have no counterpart in the linear scale, consequently these values never occur as output peak words. This is also illustrated in Table 14). The dB conversion block converts only positive linear values to a a useful dB value. All negative input values will be converted to an output value of 3 for recognition.

Table 14 Peak readout linear-to-dB conversion (note 1)

PEAK DATA	PEAK VALUE (dB)	PEAK DATA	PEAK VALUE (dB)	PEAK DATA	PEAK VALUE (dB)	PEAK DATA	PEAK VALUE (dB)
000000	$-\infty$	000001	n.a.	000010	n.a.	000011	−90.31
000100	n.a.	000101	n.a.	000110	n.a.	000111	−84.29
001000	n.a.	001001	n.a.	001010	−80.77	001011	−78.27
001100	n.a.	001101	−76.33	001110	−74.75	001111	−72.25
010000	−71.22	010001	−69.48	.....	.....	.....	.....
.....	.....	111101	−2.87	111110	−1.48	111111	0.00

Note

1. The peak level dB conversion block relates according to the following transfer formula from linear to dB scale:
   a) Peak value (dB) = (peak data − 63.5) × 5 × log 2
   b) The table should be read as follows. The maximum value of 63 (111111) is returned when the detected value resides between −1.48 dB and 0 dB, the next lower value of 62 is returned when the detected value resides between −2.87 dB and −1.48 dB etc. Only true digital silence will return a peak readout value of 000000.
   c) For peak data > 010011 (= 19) the error in peak level is $<(11 \times \log 2)/4$
   d) For peak data <010100 (= 20) the error will be larger due to 16 bits accuracy.

7.9.3 PEAK DETECTION

The TDA1546T provides a convenient way to monitor the peak value of the audio data, for left and right channels individually, by way of readout via the microcontroller interface. Peak value monitoring has its applications mainly in digital volume unit measurement and display, and in automatic recording level control. The peak level measurement of the TDA1546T occurs with a resolution of 16 bits thus providing a dynamic range amply suitable for all practical applications.

The output of the peak detection block is a register of two 6-bit words (one for each channel) which represents the dB linear value of the positive peak value and is accessible via the microcontroller interface. The peak detection block continuously monitors the audio information arriving from the spectrum analyzer, comparing its actual dB value to the value currently stored in the peak register. Any new value greater than the currently held peak value will cause the register to assume the new, greater value. On a peak request (see Section 7.3) the contents of the peak register are transferred to the microcontroller interface. After a read action the peak register will be reset and the collection of new peak data started. The end of a peak read action should be marked by an address mode sequence so that the output peak register is able to latch new data.

The peak detection block receives data that has been processed by the de-emphasis block, so if peak data is read when applying digital de-emphasis, the de-emphasis frequency characteristic will be noticeable in the peak output value.

The peak data readout protocol is illustrated in Fig.7. A peak request is performed by activating the address mode of the microcontroller interface (see Table 2). Upon the peak request, the microcontroller will commence collecting data from the internal peak data output register (dB linear, 6-bit left, 6-bit right) on the LOW-to-HIGH transition of L3CLK by sending a clock onto the L3CLK line. The first and last bits of the byte (bit 0 and bit 7 in Fig.7) are padding bits with default set to zero. The first peak bit (bit 1), is the LSB of the channel peak value. The contents of the peak data output register will not change during the peak request. The peak data readout procedure may be aborted at any instant by returning to the address mode, thereby marking the end of the peak request.

7.9.4 Silence detection

The TDA1546T is designed to detect silence conditions in the left and right channels, separately or combined, and report this via the versatile outputs VERS1 and VERS0 (see Section 7.9.6). The function is programmable in silence level (dB linear via microcontroller register bits SIL3 to SIL0) and silence duration (SILT3 to SILT0) and is implemented to allow external manipulation of the audio signal upon absence of program material, such as muting or recorder control. The silence levels and silence duration timings are given in Table 15.

Table 15 Silence detection parameters

SILENCE LEVEL		SILENCE DURATION	
SIL3 TO SIL0	SILENCE LEVEL (dB)	SILT3 TO SILT0	SILENCE DURATION AT 44.1 kHz (s)
0 0 0 0	$-\infty$	0 0 0 0	0.2
0 0 0 1	–90.3	0 0 0 1	0.4
0 0 1 0	–87.3	0 0 1 0	0.6
....	...	....	...
1 1 1 0	–51.2	1 1 1 0	3.0
1 1 1 1	–48.2	1 1 1 1	3.2

The silence level and silence duration from 0000 to 1111 can be obtained using the following equations:

silence if: sample $< (2 \times SIL - 62) \times 5\log 2$

Example: silence for 1110:

$(2 \times 14 - 62) \times 5\log 2 = -51.2$ dB

$$\text{silence duration} = \frac{[(SILT + 1) \times 241] \times 256}{(f_s \times 7)}$$

Example: silence for 1110 at

$$f_s = 44.1 \text{ kHz} = \frac{[(14 + 1) \times 241] \times 256}{(44100 \times 7)}$$

The TDA1546T itself does not influence the audio signal as a result of digital silence. The sole function of this block is detection, and any further treatment must be accomplished by other means. Silence detected is TRUE when the corresponding channel carries samples smaller than the programmed value for at least the duration of the programmed time. As a separated left/right digital silence detection is not always needed, the logic "AND" function of both left and right digital detection circuits can be logically combined to a mono digital silence indication on pin VERS0, programmed via register control bits PINM1 and PINM0.

7.9.5 Overload detection

A level programmable overload detection is present to facilitate applications in digital volume unit measurement and display, and in automatic recording level control. The overload condition of the audio data for left and right channels, individually or combined, is reported via the versatile outputs VERS1 and VERS0 (see Section 7.9.6). The overload levels are given in Table 16.

Table 16 Overload detection level

OVER3 TO OVER0	DETECTION LEVEL (dB)
0 0 0 0	–46.7
0 0 0 1	–43.6
....	...
1 1 1 0	–4.5
1 1 1 1	–1.5

The overload detection level from 0000 to 1111 can be obtained using the following equation:

Overload if peak level $> (2 \times OVER - 31) \times 5\log 2$

Overload detected is TRUE when the corresponding channel carries samples greater than the programmed value. A condition of detected overload will be held until peak data is read out from the TDA1546T. This implies that a continuous overload indication (also via the versatile outputs) will function properly only with periodic peak readout taking place. As a separated left/right digital overload detection is not always needed, the logic "OR" function of both left and right digital detection circuits can be logically combined to a mono digital overload indication on pin VERS1, programmed via register control bits PINM1 and PINM0.

7.9.6 VERSATILE OUTPUTS

Table 17 Versatile output pin control

REGISTER BIT		OUTPUT MODE	
PINM1	**PINM0**	**VERS1**	**VERS0**
0	0	mono overload detection	mono silence detection
0	1	left overload detection	right overload detection
1	0	left digital silence detection	right digital silence detection
1	1	no detection	no detection
PVIV1 = 0		VERS1 is active HIGH	
PVIV1 = 1		VERS1 is active LOW	
PVIVO = 0		VERS0 is active HIGH	
PVIV0 = 1		VERS0 is active LOW	

7.10 Noise shaper

In the normal-speed mode the second-order noise shaper operates at $96f_s$ ($f_{sys} = 384f_s$) or $128f_s$ ($f_{sys} = 256f_s$). In the double-speed mode the noise shaper operates at $48f_s$ ($f_{sys} = 384f_s$) or $64f_s$ ($f_{sys} = 256f_s$). It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique used in combination with a special data coding enables extremely high signal-to-noise ratios to be achieved. The noise shaper outputs a 5-bit PDM bitstream signal to the DAC.

7.11 Continuous calibration digital-to-analog converter

The dual 5-bit DAC uses the continuous calibration technique. This method, based on charge storage, involves exact duplication of a single reference current source. In the TDA1546T, 32 such current sources plus one spare source are continuously calibrated. The spare source is included to allow continuous converter operation.

The DAC receives a 5-bit data bitstream from the noise shaper. This data is then converted so that only small currents are switched to the output during digital silence (input 00000H). In this way extremely high-noise performance is achieved.

7.12 Operational amplifiers

The operational amplifiers and the internal conversion resistors R_{CONV1} and R_{CONV2} convert the DAC current to an output voltage which is made available at pins V_{OL} and V_{OR} (typ 1.5 V RMS). Connecting an external capacitor between FILTCL and V_{OL}, FILTCR and V_{OR} respectively provides the required first-order post filtering for the left and right channels.

7.13 Internal reference circuitry

The Internal reference circuitry ensures that the output voltage signal is proportional to the supply voltage, thereby maintaining maximum dynamic range for supply voltages from 3.8 to 5.5 V. The reference voltage output (pin 26) is intended for external decoupling of the reference voltage. It is a high-impedance output and should not be used to drive external loads, otherwise the performance of the TDA1546T's analog circuitry will be impaired. The voltage at V_{ref} is typically 50% of the analog supply voltage (V_{DDA}).

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–	7.0	V
T_{xtal}	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		–65	+125	°C
T_{amb}	operating ambient temperature		–20	+70	°C
V_{es}	electrostatic handling	note 1	–3500	+3500	V
		note 2	–350	+350	V

Notes

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
2. Equivalent to discharging a 200 pF capacitor through a 2.5 μH inductor.

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	75	K/W

10 QUALITY SPECIFICATION

In accordance with *SNW-FQ-611*. The numbers of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9398 510 63011.

11 CHARACTERISTICS

T_{amb} = –20 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD}	digital supply voltage	note 1	3.8	5.0	5.5	V
I_{DDD}	digital supply current	V_{DDD} = 5 V; at code 00000H	–	40	–	mA
V_{DDA}	analog supply voltage	note 1	3.8	5.0	5.5	V
I_{DDA}	analog supply current	V_{DDA} = 5 V; at code 00000H	–	5.5	–	mA
V_{DDO}	operational amplifier supply voltage	note 1	3.8	5.0	5.5	V
I_{DDO}	operational amplifier supply current	V_{DDO} = 5 V; at code 00000H	–	6.5	–	mA
V_{DDX}	clock circuitry supply voltage	note 1	3.8	5.0	5.5	V
I_{DDX}	clock circuitry supply current	V_{DDX} = 5 V; at code 00000H	–	1	–	mA
RR	ripple rejection to V_{DDA}	note 2	–	25	–	dB
System clock input						
f_{xtal}	crystal frequency	$f_{sys} = 384f_s$	9.6	16.93	18.4	MHz
		$f_{sys} = 256f_s$	6.4	11.29	12.28	MHz
T_{cy}	system clock duty cycle	note 3	40	–	60	%
I_{LI}	input leakage current	note 4	–	–	10	µA
C_I	input capacitance		–	–	10	pF
Master clock mode (see Fig.4)						
G_m	mutual conductance	f_i = 100 kHz	–	6.2	–	mS
G_v	small signal voltage gain	$G_v = G_m \times G_o$	–	41	–	V/V
Slave clock mode (see Fig.5)						
VI_L	LOW level input voltage	note 5	–0.5	–	$0.2V_{DD}$	V
V_{IH}	HIGH level input voltage	note 5	$0.8V_{DD}$	–	V_{DD} + 0.5	V
Digital inputs; WS, BCK, DATA, TEST1, TEST2, L3DATA, L3CLK, L3MODE and CKSL						
V_{IL}	LOW level input voltage	note 5	–0.5	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 5	$0.7V_{DD}$	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	note 4	–	–	10	µA
C_I	input capacitance		–	–	10	pF
Power-on reset; $\overline{\text{POR}}$						
V_{IL}	LOW level input voltage	note 5	–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 5	$0.7V_{DD}$	–	V_{DD} + 0.5	V
C_I	input capacitance		–	–	10	pF
R_I	input resistance		17	–	203	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital outputs; CDEC, VERS0 and VERS1						
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = –4 mA	V_{DD} – 0.5	–	V_{DD}	V
t_r	output rise time	note 3	–	–	20	ns
t_f	output fall time	note 3	–	–	20	ns
MSR_{CDEC}	mark-space ratio	output CDEC; note 6	45	50	55	%
C_L	load capacitance		–	–	30	pF
Serial input data timing (see Fig.10)						
f_{BCK}	bit clock input = data input rate	$f_{sys} = 384f_s$	–	–	$48f_s$	MHz
		$f_{sys} = 256f_s$	–	–	$64f_s$	MHz
f_{WS}	word select input frequency	normal-speed	25	44.1	48	kHz
		double-speed	50	88.2	96	kHz
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{BCK(H)}$	bit clock time HIGH		55	–	–	ns
$t_{BCK(L)}$	bit clock time LOW		55	–	–	ns
$t_{s;DAT}$	data set-up time		40	–	–	ns
$t_{h;DAT}$	data hold time		10	–	–	ns
$t_{s;WS}$	word select set-up time		40	–	–	ns
$t_{h;WS}$	word select hold time		10	–	–	ns

Notes

1. All V_{DD} and V_{SS} pins must be connected externally to the same supply.
2. V_{ripple} = 1% of the supply voltage; f_{ripple} = 100 Hz.
3. Reference levels = 10% and 90%.
4. Minimum I_{LI} measured at V_i = 0 V; maximum I_{LI} measured at V_i = 5.5 V.
5. Minimum V_{IL} and maximum V_{IH} are peak values to allow for transients.
6. Specified duty cycle valid only when used in crystal oscillator applications.

12 ANALOG CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference values						
V_{ref}	reference voltage level		2.45	2.5	2.55	V
R_{CONV}	current-to-voltage conversion resistor		1.6	2.2	2.8	kΩ
Analog outputs						
RES	resolution		–	–	18	bit
t_{dg}	group delay	f_s = sample rate; normal-speed	–	$\frac{24}{f_s}$	–	s
$V_{FS(rms)}$	full-scale output voltage (pins 22 and 25) (RMS value)	at 0 dB input level	1.425	1.5	1.575	V
$V_{DC(os)}$	output voltage DC offset with respect to reference voltage level V_{ref}	at code 00000H	–80	–65	–50	mV
TC_{FS}	full-scale temperature coefficient		–	$\pm 100 \times 10^{-6}$	–	
(THD+N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB input level; note 1	–	–88	–81	dB
			–	0.004	0.009	%
		at –60 dB input level; A-weighted; note 1	–	–44	–40	dB
		at 0 dB input level; (20 Hz to 20 kHz); note 2	–	–85	–80	dB
			–	0.006	0.01	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted; at code 00000H	100	108	–	dB
α_{cs}	channel separation		85	100	–	dB
$\lvert\delta V_O\rvert$	imbalance between outputs		–	0.2	0.3	dB
$\lvert Z_O\rvert$	dynamic output impedance		–	10	–	Ω
R_{OL}	output load resistance		3	–	–	kΩ
C_{OL}	output load capacitance		–	–	200	pF

Notes

1. Measured with a 1 kHz sine wave generated at a sampling rate of 48 kHz.
2. Measured with a sine wave swept from 20 Hz to 20 kHz, generated at a sampling rate of 48 kHz.

13 APPLICATION INFORMATION

13.1 Digital filter characteristics (theoretical values)

Table 18 Normal-speed filter characteristics

ITEMS	SAMPLE FREQUENCY	RANGE	CHARACTERISTICS	
Pass band	44.1 kHz	0 to 20 kHz	0 ±0.025 dB	
	32 kHz	14.5 to 15 kHz	> –0.15 dB	
Stop band	44.1 kHz	24.1 to 150 kHz	typical	<–60 dB
			worst case	<–57 dB
		>150 kHz	typical	<–57 dB
			worst case	<–47 dB
	32 kHz	17 to 17.5 kHz	< –40 dB	

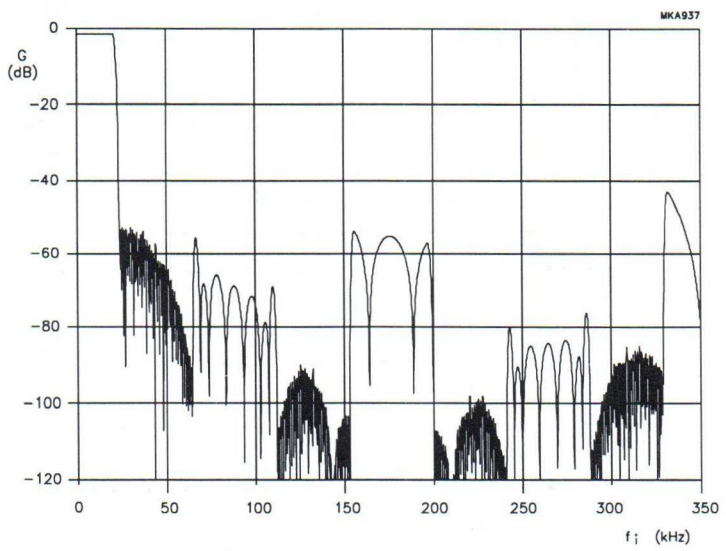


Fig.17 Digital filter overall frequency response.

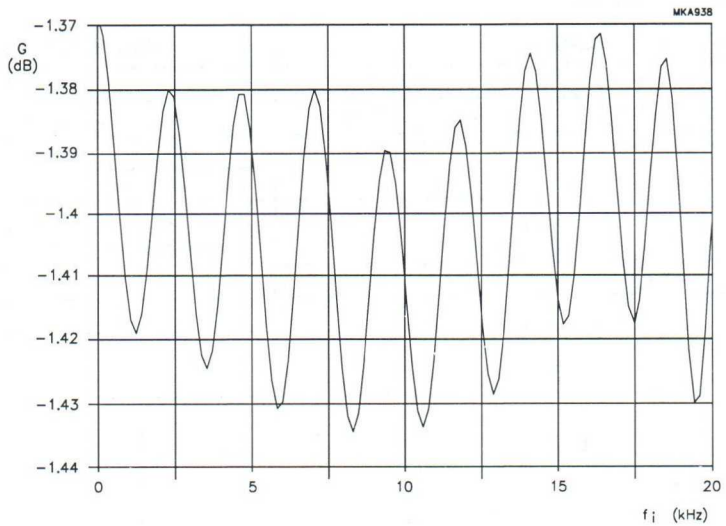


Fig.18 Digital filter pass band ripple.

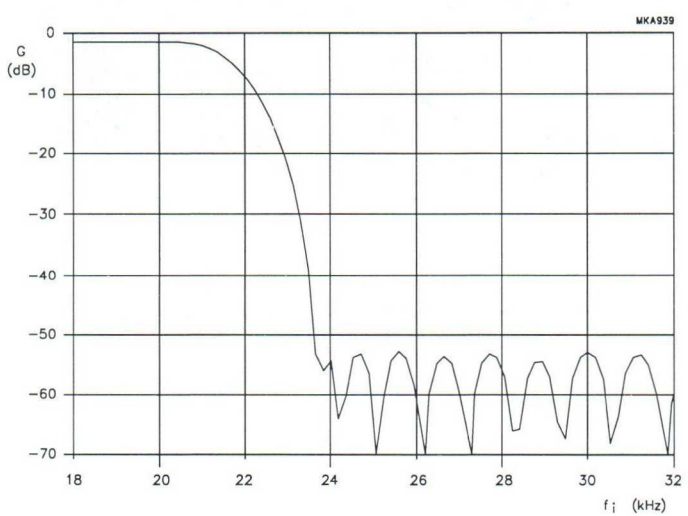


Fig.19 Digital filter transition band.

Table 19 Double-speed filter characteristics

ITEM	RANGE	CHARACTERISTICS	
Pass band	0 to 17 kHz	0 ±0.075 dB	
	17 to 20 kHz	> −0.3 dB	
Stop band	24.1 to 150 kHz	typical	< −47 dB
		worst case	< −45 dB
	>150 kHz	typical	< −33 dB
		worst case	< −25 dB

Table 20 De-emphasis: deviation from ideal 50 ms to 15 ms characteristic

ITEM	SAMPLE FREQUENCY	RANGE	CHARACTERISTICS
Gain deviation	44.1 and 48 kHz	0 to 18 kHz	0 ±0.05 dB
		18 to 20 kHz	<0.12 dB
	32 kHz	0 to 13 kHz	0 ±0.06 dB
		13 to 15 kHz	<0.22 dB
Phase deviation	44.1 and 48 kHz	0 to 15 kHz	<10 deg
		15 to 20 kHz	<15 deg
	32 kHz	0 to 9 kHz	<10 deg
		9 to 15 kHz	<16 deg

13.2 Example application circuit

An example of an application circuit, the schematic for a printed-circuit board available for evaluation, is shown in Fig.20. The following are shown:

- the typical connection of the power-on reset pin using a timing capacitor
- circuitry surrounding the XTAL1 and XTAL2 pins which can be configured to either crystal oscillator mode (master mode) or external system clock input mode (slave mode)
- an example connection for LED indication of digital silence and overload detection (the inverters are optional, used as buffers. The polarity of the versatile output pins programmed via PVIV1 and PVIV0 should reflect the connection polarity of the indicator LEDs)
- typical decoupling connection for the V_{ref} pin
- typical low component count stereo line output stage (no additional filtering and therefore no external operational amplifiers needed).

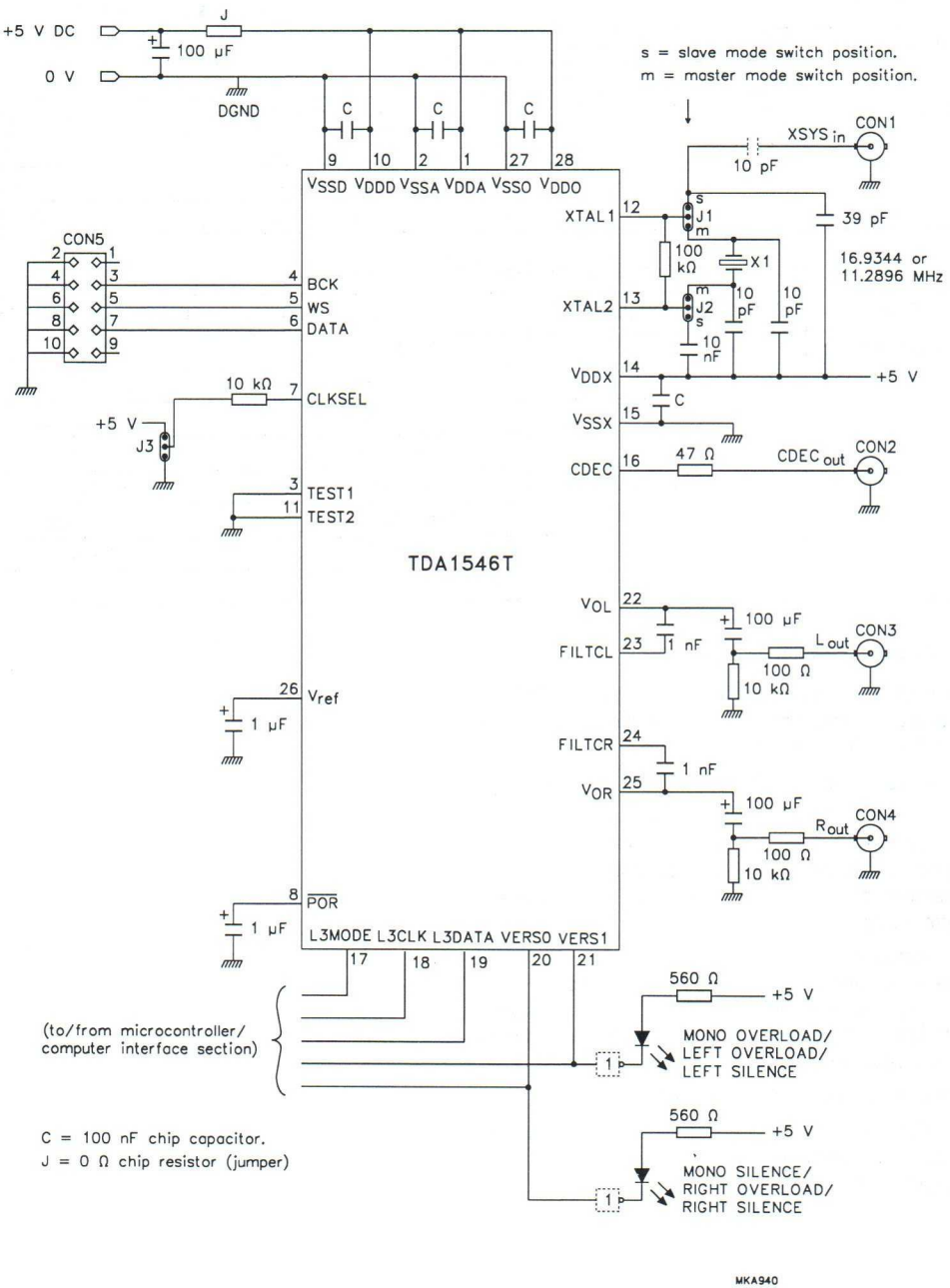


Fig.20 Application diagram (demonstration printed-circuit board).

QUASI-SPLIT-SOUND CIRCUIT

GENERAL DESCRIPTION

The TDA2545A is a monolithic integrated circuit for quasi-split-sound processing in television receivers.

Features

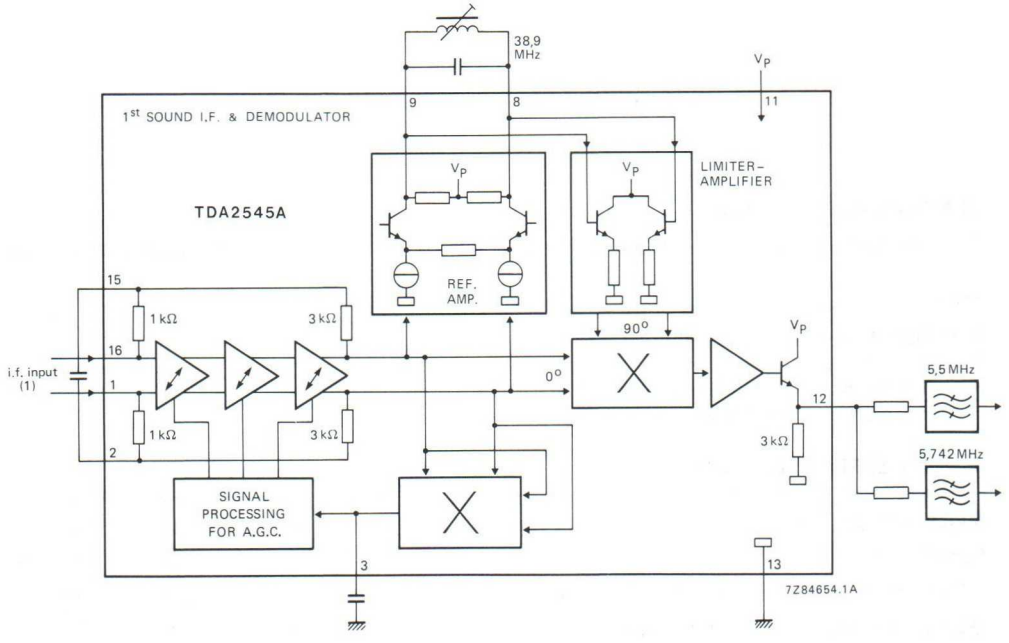
- 3-stage gain controlled i.f. amplifier
- A.G.C. circuit
- Reference amplifier and limiter amplifier for vision carrier (V.C.) processing
- Linear multiplier for quadrature demodulation

QUICK REFERENCE DATA

Supply voltage (pin 11)	$V_P = V_{11\text{-}13}$	typ.	12 V
Supply current (pin 11)	$I_P = I_{11}$	typ.	45 mA
Minimum i.f. vision carrier input voltage (r.m.s. value)	$V_{VC1\text{-}16(rms)}$	typ.	150 μV
Output voltage; 5,5 MHz (r.m.s. value)	$V_{12\text{-}13(rms)}$	typ.	100 mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{12\text{-}13(rms)}$	typ.	45 mV
I.F. control range	ΔG_v	typ.	64 dB
Signal-to-weighted-noise ratio (rel. to 1 kHz; 30 kHz deviation)			
at 5,5 MHz } for 2T/20T pulses with white bars	S + W/W	typ.	58 dB
at 5,742 MHz } for 2T/20T pulses with white bars	S + W/W	typ.	56 dB

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38).



(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.).

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	$V_P = V_{11-13}$	max.	13,2	V
Storage temperature range	T_{stg}	−25 to	+150	°C
Operating ambient temperature range	T_{amb}	0 to	+70	°C

CHARACTERISTICS

$V_P = V_{11-13} = 12$ V; $T_{amb} = 25$ °C; measured at $f_{VC} = 38{,}9$ MHz, $f_{SC1} = 33{,}4$ MHz, $f_{SC2} = 33{,}158$ MHz:

Vision carrier (V.C.) modulated with different video signals (see below); modulation depth 100% (proportional to 10% residual carrier).

Vision carrier amplitude (r.m.s. value) is $V_{VC} = 10$ mV.
Vision-to-sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB.

Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation $\Delta f = \pm 30$ kHz.
For measuring circuit see Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 11)					
Supply voltage	$V_P = V_{11-13}$	10,8	12	13,2	V
Supply current	$I_P = I_{11}$	33	45	55	mA
I.F. amplifier					
Input voltage for start of gain control (intercarrier signals −3 dB)	$V_{VC1-16(rms)}$	–	150	200	μV
Input voltage for end of gain control (intercarrier signals + 1 dB)	$V_{VC1-16(rms)}$	100	250	–	mV
I.F. gain control range	ΔG_v	60	64	–	dB
Control voltage range (see Fig. 3)	V_{3-13}	4	–	V_p	V
Input resistance	R_{1-16}	–	2,5	–	kΩ
Input capacitance	C_{1-16}	–	1,5	–	pF
Intercarrier generation					
Output voltage; 5,5 MHz (r.m.s. value)	$V_{12-13(rms)}$	60	100	140	mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{12-13(rms)}$	27	45	63	mV
D.C. output voltage	V_{12-13}	–	5,9	–	V
Allowable d.c. load resistance at the output	R_{12-13}	7	–	–	kΩ
Allowable output current	$-I_{12}$	–	–	1	mA
Intercarrier signal-to-noise (see note 1) (measured behind the FM demodulators) weighted according to CCIR 468-2, quasi-peak					
a. 2T/20T pulses with white bars (see also Fig. 4)					
at 5,5 MHz	S+W/W	53	58	–	dB
at 5,742 MHz	S+W/W	51	56	–	dB
b. 6 kHz sinewave					
at 5,5 MHz	S+W/W	50	53	–	dB
at 5,742 MHz	S+W/W	50	53	–	dB
c. black level (sync pulses only)					
at 5,5 MHz	S+W/W	60	65	–	dB
at 5,742 MHz	S+W/W	58	63	–	dB

Note 1.
Incidental phase on the vision carrier, caused by TV transmitter, has to be less than 0,5 degrees for black to white transient (equivalent to S+W/W = 56 dB for 6 kHz sinewave).

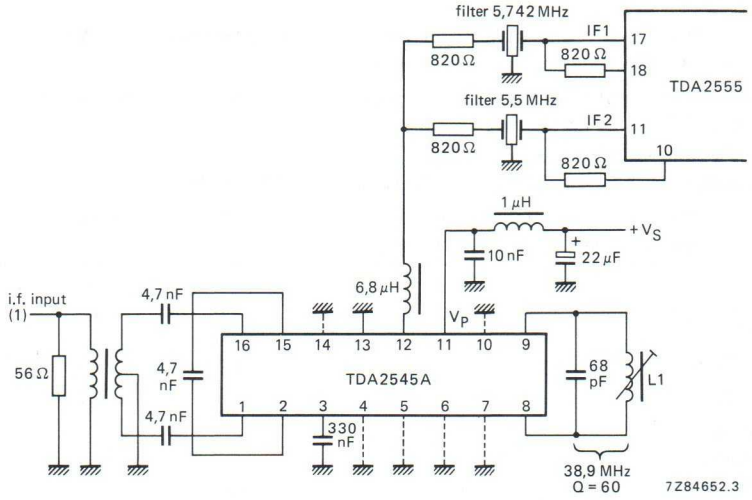


Fig. 2 Measuring circuit for TDA2545A.

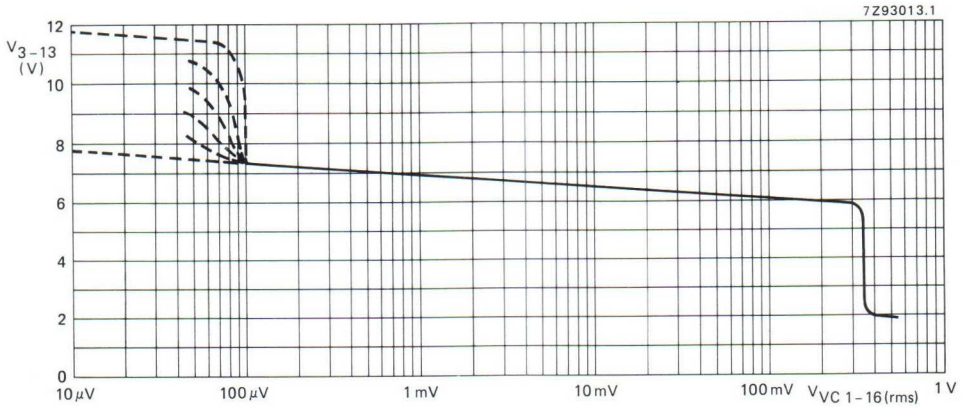


Fig. 3 Control voltage at pin 3 as a function of the input voltage V_{VC1-16}(rms).

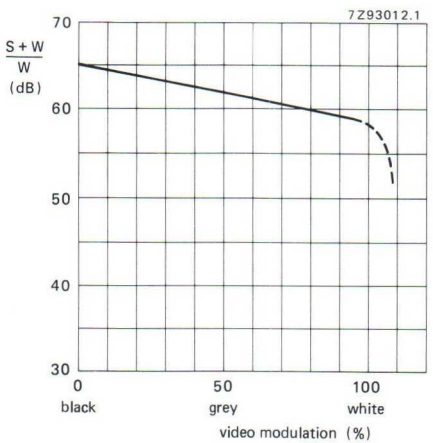


Fig. 4 Signal-to-weighted-noise ratio depending on video modulation.

QUASI-SPLIT-SOUND CIRCUIT WITH 5,5 MHz DEMODULATION

GENERAL DESCRIPTION

The TDA2546A is a monolithic integrated circuit for quasi-split-sound processing, including 5,5 MHz demodulation, in television receivers.

Features

1st i.f. (V.C.: vision carrier plus S.C.: sound carrier)

- 3-stage gain controlled i.f. amplifier
- A.G.C. circuit
- Reference amplifier and limiter amplifier for vision carrier (V.C.) processing
- Linear multiplier for quadrature demodulation

2nd i.f. (5,5 MHz signal)

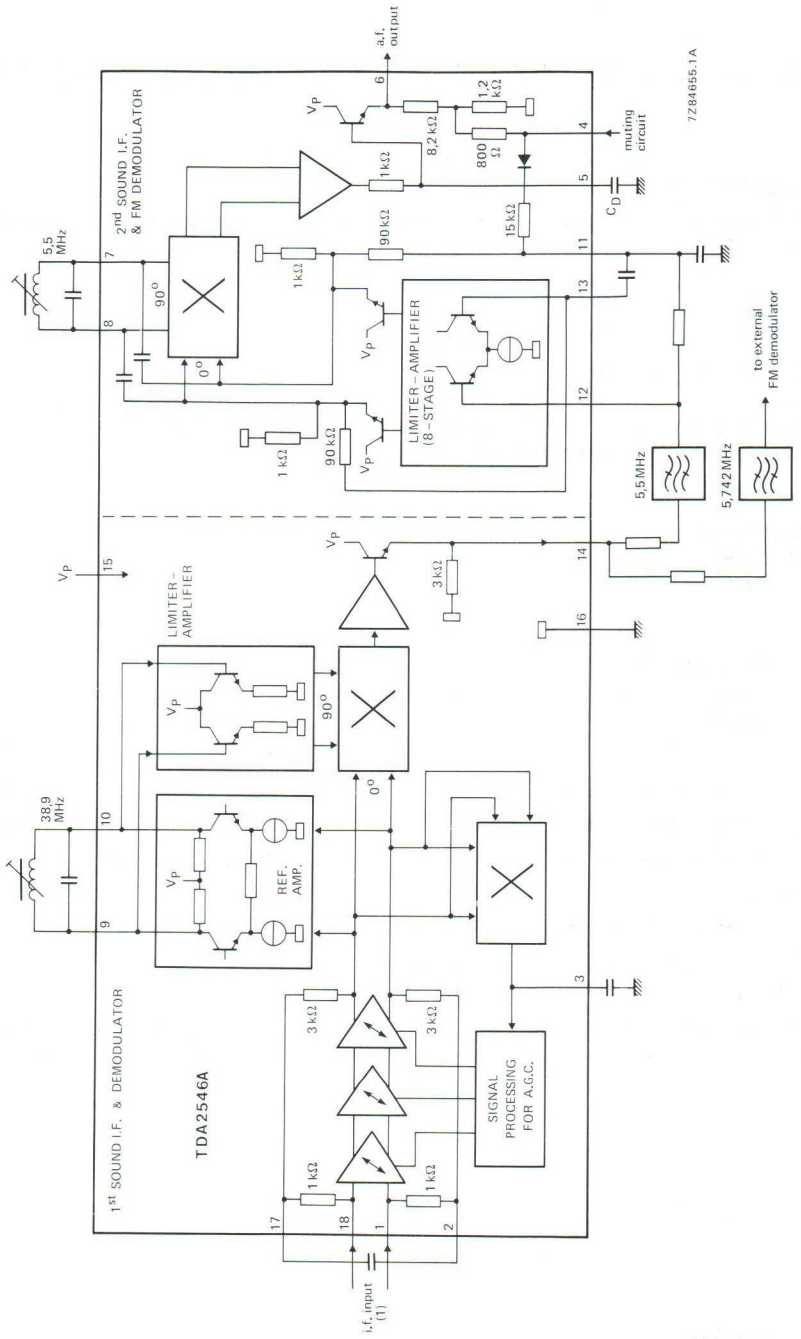
- 8-stage limiter amplifier
- Quadrature demodulator
- A.F. amplifier with de-emphasis
- AV switch

QUICK REFERENCE DATA

Supply voltage (pin 15)	$V_P = V_{15\text{-}16}$	typ.	12 V
Supply current (pin 15)	$I_P = I_{15}$	typ.	57 mA
Minimum i.f. vision carrier input voltage (r.m.s. value)	$V_{VC1\text{-}18(rms)}$	typ.	150 μV
Output voltage; 5,5 MHz (r.m.s. value)	$V_{14\text{-}16(rms)}$	typ.	100 mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{14\text{-}16(rms)}$	typ.	45 mV
I.F. control range	ΔG_v	typ.	64 dB
Signal-to-weighted-noise ratio (rel. to 1 kHz; 30 kHz deviation)			
at 5,5 MHz for 2T/20T pulses with white bars	S + W/W	typ.	58 dB
at 5,742 MHz for 2T/20T pulses with white bars	S + W/W	typ.	56 dB
A.F. output voltage (r.m.s. value)	$V_{o6\text{-}16(rms)}$	typ.	0,6 V

PACKAGE OUTLINES

18-lead DIL; plastic (SOT102).



(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.)

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_P = V_{15-16}$	max.	13,2	V
Input current (pin 4)	I_4	max.	7	mA
Storage temperature range	T_{stg}	−25 to	+150	°C
Operating ambient temperature range	T_{amb}	0 to	+70	°C

CHARACTERISTICS

$V_P = V_{15-16} = 12$ V; $T_{amb} = 25$ °C; measured at $f_{VC} = 38{,}9$ MHz, $f_{SC1} = 33{,}4$ MHz, $f_{SC2} = 33{,}158$ MHz:

Vision carrier (V.C.) modulated with different video signals (see below); modulation depth 100% (proportional to 10% residual carrier).

Vision carrier amplitude (r.m.s. value) is $V_{VC} = 10$ mV.
Vision-to-sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB.

Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation $\Delta f = \pm 30$ kHz.
For measuring circuit see Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 15)					
Supply voltage	$V_P = V_{15-16}$	10,8	12	13,2	V
Supply current	$I_P = I_{15}$	40	57	75	mA
I.F. amplifier					
Input voltage for start of gain control (intercarrier signals −3 dB)	$V_{VC1-18(rms)}$	–	150	200	μV
Input voltage for end of gain control (intercarrier signals + 1 dB)	$V_{VC1-18(rms)}$	100	250	–	mV
I.F. gain control range	ΔG_V	60	64	–	dB
Control voltage range (see Fig. 3)	V_{3-16}	4	–	V_p	V
Input resistance	R_{1-18}	–	2,5	–	kΩ
Input capacitance	C_{1-18}	–	1,5	–	pF
Intercarrier generation					
Output voltage; 5,5 MHz (r.m.s. value)	$V_{14-16(rms)}$	60	100	140	mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{14-16(rms)}$	27	45	63	mV
D.C. output voltage	V_{14-16}	–	5,9	–	V
Allowable d.c. load resistance at the output	R_{14-16}	7	–	–	V
Allowable output current	$-I_{14}$	–	–	1	mA
Frequency demodulator (measured at f = 5,5 MHz)					
Input voltage vor start of limiting (r.m.s. value)	$V_{12-16(rms)}$	–	–	100	μV
Maximum input voltage (r.m.s. value)	$V_{12-16(rms)}$	–	200	–	mV
D.C. output voltage	$V_{11,12,13-16}$	–	2,2	–	V

parameter	symbol	min.	typ.	max.	unit
A.F. output voltage (r.m.s. value)	$V_{6\text{-}16(rms)}$	450	600	810	mV
D.C. output voltage	$V_{6\text{-}16}$	–	4	–	V
Allowable d.c. load resistance at the output	$R_{6\text{-}16}$	27	–	–	kΩ
Allowable a.c. load impedance at the output	$Z_{6\text{-}16}$	10	–	–	kΩ
Total harmonic distortion	THD	–	–	1	%
Internal de-emphasis resistance	$R_{i5\text{-}16}$	–	1	–	kΩ
Switching voltage (pin 4)					
for mute	$V_{4\text{-}16}$	9	–	–	V
for a.f. on	$V_{4\text{-}16}$	–	–	2,5	V
Intercarrier signal-to-noise (measured behind the FM demodulators)					
Signal-to-weighted-noise ratio according to CCIR 468-2, quasi-peak 2T/20T pulses with white bars (see also Fig. 4)					
at 5,5 MHz	S+W/W	53	58	–	dB
at 5,742 MHz	S+W/W	51	56	–	dB
6 kHz sine wave					
at 5,5 MHz	S+W/W	50	53	–	dB
at 5,742 MHz	S+W/W	50	53	–	dB
with black level (vision carrier modulated with sync pulses only)					
at 5,5 MHz	S+W/W	60	65	–	dB
at 5,742 MHz	S+W/W	58	63	–	dB

NOTES TO THE CHARACTERISTICS

1. Incidential phase on the vision carrier, caused by TV-transmitter, has to be less than 0,5 degrees for black to white transient.
   (Equivalent to S+W/W = 56 dB for 6 kHz sine wave).

(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.)

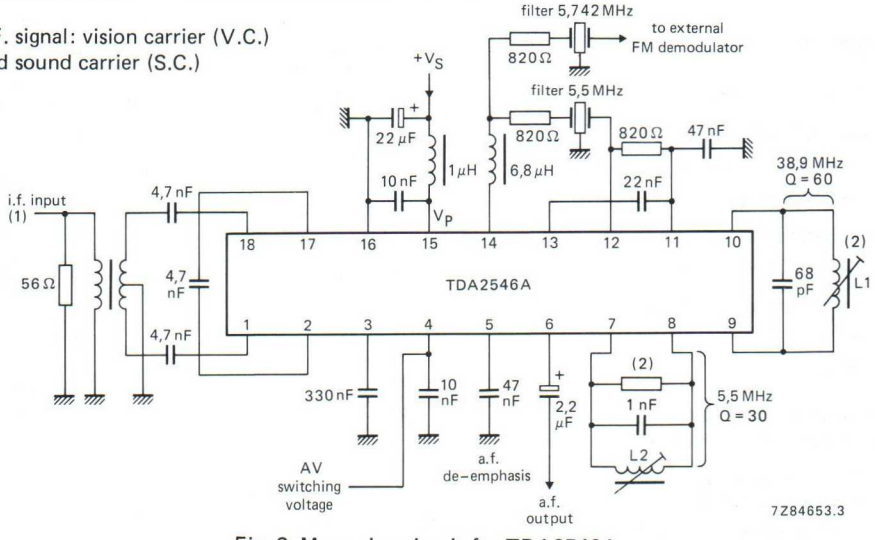


Fig. 2 Measuring circuit for TDA2546A.

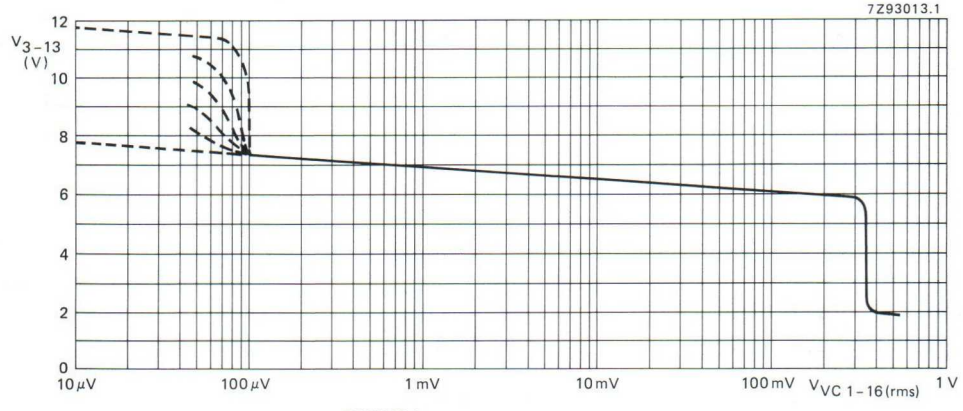


Fig. 3 Control voltage at pin 3 as a function of the input voltage $V_{VC1-18(rms)}$.



Fig. 4 Signal-to-weighted-noise ratio depending on video modulation.

I.F. AMPLIFIER AND DEMODULATOR FOR MULTISTANDARD TV RECEIVERS

GENERAL DESCRIPTION

The TDA2549 is a complete i.f. circuit with a.f.c., a.g.c., demodulation and video preamplification facilities for multistandard television receivers. It is capable of handling positively and negatively modulated video signals in both colour and black/white receivers.

Features

- Gain-controlled wide-band amplifier providing complete i.f. gain
- Synchronous demodulator for positive and negative modulation
- Video preamplifier with noise protection for negative modulation
- Auxiliary video input and output (75 Ω)
- Video switch to select between auxiliary video input signal and demodulated video signal
- A.F.C. circuit with on/off switch and inverter switch
- A.G.C. circuit for positive modulation (mean level) and negative modulation (noise gate)
- A.G.C. output for controlling MOSFET tuners

QUICK REFERENCE DATA

Supply voltage (pins 13 and 21)	$V_P = V_{13;21-3}$	typ.	12 V
Supply current (pins 13 and 21)	$I_P = I_{13;21-3}$	typ.	82 mA
I.F. input signal at V_o = 2 V (between pins 6 and 7)	$V_i = V_{6-7}$	typ.	50 μV
Video output voltage at V_i = 0 V (between pins 22 and 3)			
positive modulation	$V_o = V_{22-3}$	typ.	2 V
negative modulation	$V_o = V_{22-3}$	typ.	4 V
Gain control range	G_v	typ.	74 dB
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	57 dB
A.F.C. output voltage swing (pin 15)	V_{15-3}	min.	10 V
Max. tuner a.g.c. output current (pin 10)	I_{10}	min.	0,3 mA
Video bandwidth (3 dB)	B	typ.	5,5 MHz
Auxiliary video input voltage (pin 12) at V_o = 2 V (peak-to-peak value)	$V_{12-3(p-p)}$	typ.	1 V
Auxiliary video output impedance (pin 14)	$\lvert Z_{14-3}\rvert$	typ.	7 Ω
Auxiliary video output voltage (pin 14)	V_{14-3}	typ.	2 V

PACKAGE OUTLINE

24-lead DIL; plastic (SOT101A).

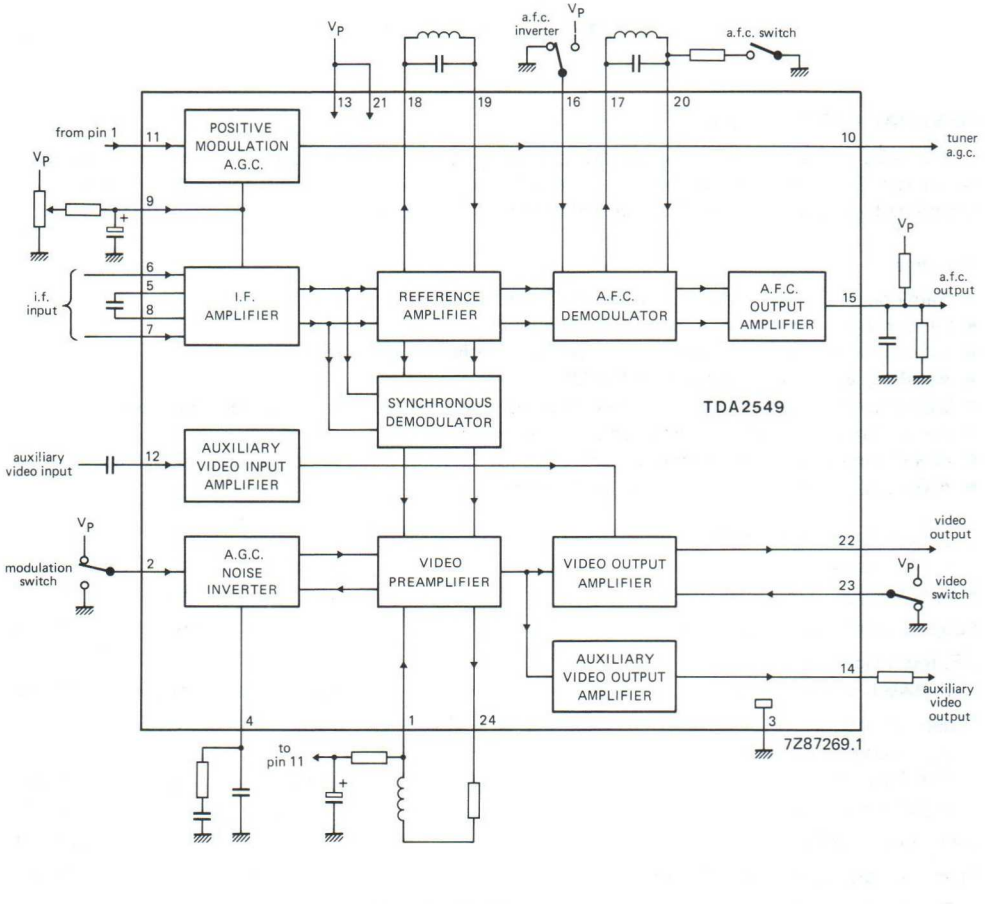


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pins 13 and 21)	V_P	13,8 V
Storage temperature range	T_{stg}	−25 to +125 °C
Operating ambient temperature range	T_{amb}	−25 to +70 °C

CHARACTERISTICS (measured in Fig. 5)

V_P = 12 V; T_{amb} = 25 °C

paramater	symbol	min.	typ.	max.	unit
Supply voltage range	V_P	10,8	12	13,2	V
Supply current (pins 13 and 21)	I_P	–	82	–	mA
I.F. input signal for V_o = 2 V (between pins 6 and 7)	$V_i = V_{6-7}$	–	50	150	μV
Input impedance (differential)	$\lvert Z_{6-7} \rvert$	–	2	–	kΩ
Input capacitance (differential)	C_{6-7}	–	2	–	pF
Zero signal output level					
positive modulation	V_{22-3}	1,6	2	2,3	V
negative modulation	V_{22-3}	3,7	4	4,3	V
Top sync output level	V_{22-3}	1,7	2	2,3	V
Gain control range	G_v	50	74	–	dB
Signal-to-noise ratio at V_i = 10 mV (note 1)	S/N	50	57	–	dB
Maximum video output amplitude for positive modulation (peak-to-peak value)	$V_{22-3(p-p)}$	4,5	–	–	V
Bandwidth of video amplifier (3 dB)	B	–	5,5	–	MHz
Differential gain at V_o = 2 V	dG	–	4	10	%
Differential phase at V_o = 2 V	$d\varphi$	–	2	10	%
Residual carrier signal (r.m.s. value)	$V_{24-3(rms)}$	–	10	20	mV
Residual second harmonic of carrier signal (r.m.s. value)	$V_{24-3(rms)}$	–	20	60	mV

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
A.F.C. output voltage swing	V_{15-3}	10	–	–	V
Change of frequency required for a.f.c. output voltage swing of 10 V	Δf	–	70	200	kHz
A.F.C. switch off for a voltage lower than:	V_{17-3}	–	–	1,5	V
A.F.C. inverter switch					
positive a.f.c. (Fig. 2)	V_{16-3}	0	–	1,5	V
negative a.f.c. (Fig. 3)	V_{16-3}	4	–	12	V
Tuner A.G.C.					
Leakage current	I_{10}	–	–	15	μA
Saturation voltage					
I_{10} = 0,3 mA	V_{10-3}	–	0,1	0,3	V
take-over point LOW	V_i	–	–	3	mV
take-over point HIGH	V_i	10	–	–	mV
Signal expansion at G_v = 50 dB	ΔV_{22-3}	–	–	0,5	dB
Negative modulation (Fig. 4)					
white spot inverter threshold level	V_{22-3}	–	4,6	–	V
white spot insertion level	V_{22-3}	–	3,2	–	V
noise inverter threshold level	V_{22-3}	–	0,9	–	V
noise insertion level	V_{22-3}	–	2,5	–	V
Positive modulation a.g.c. detector reference level	V_{11-3}	3,0	3,2	3,4	V
Auxiliary video input signal for $V_{o(p-p)}$ = 2 V	V_{12-3}	0,7	1	1,4	V
Auxiliary video output					
output signal (note 2)	V_{14-3}	–	1	–	V
top sync level	V_{14-3}	1	2	3	V
output impedance	$\lvert Z_{14-3} \rvert$	–	7	–	Ω
Levels for video switches					
positive video	V_{2-3}	–	–	1	V
negative video	V_{2-3}	3	–	–	V
internally demodulated signal	V_{23-3}	–	–	1	V
auxiliary video signal	V_{23-3}	3	–	–	V

Notes to the characteristics

1. Signal-to-noise ratio $S/N = \dfrac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}$.
2. Measured in application of Fig. 5.

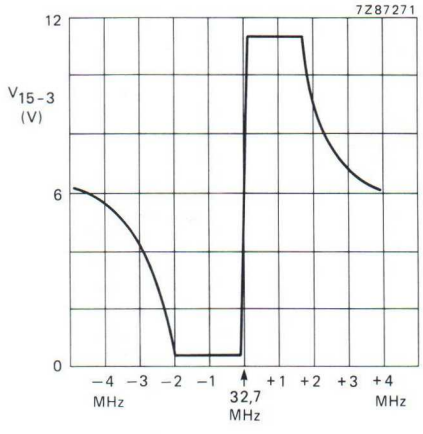


Fig. 2 A.F.C. output voltage V_{15-3} for positive a.f.c.

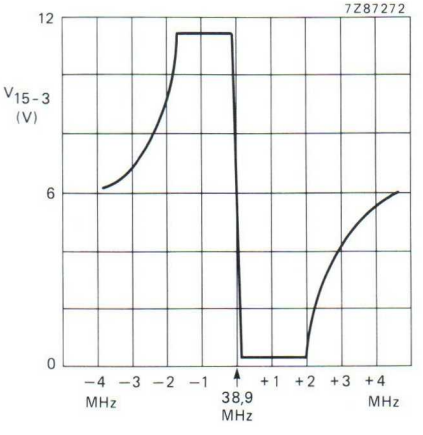


Fig. 3 A.F.C. output voltage V_{15-3} for negative a.f.c.

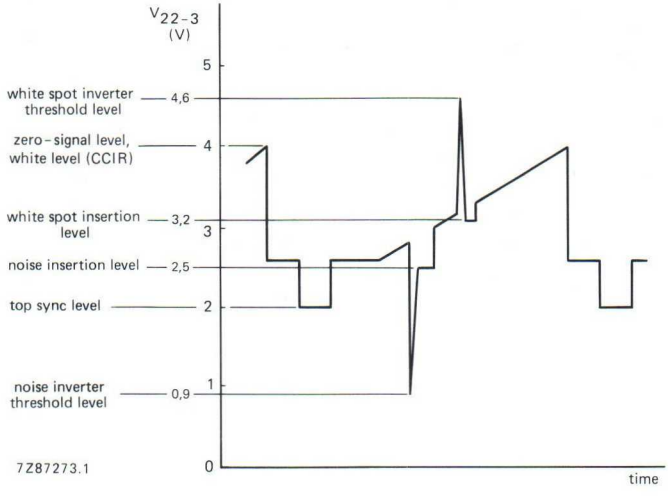


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

APPLICATION INFORMATION

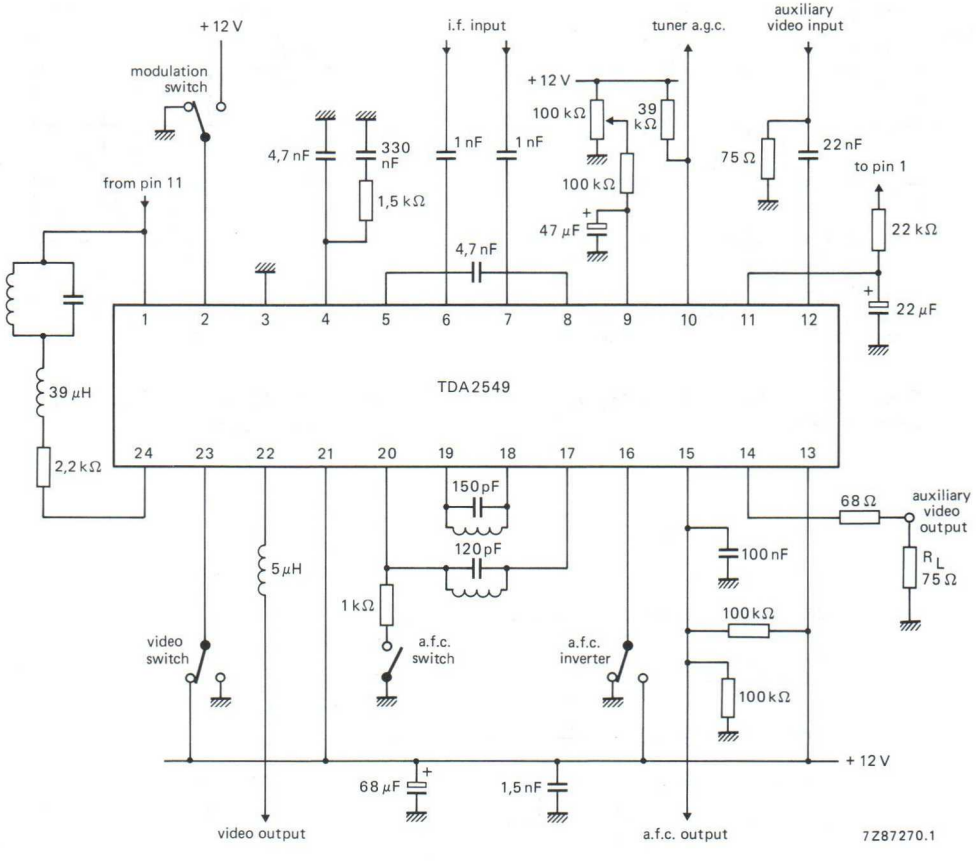


Fig. 5 Application diagram.

DUAL TV SOUND DEMODULATOR CIRCUITS

GENERAL DESCRIPTION

The circuits incorporate two FM demodulator systems to perform the demodulator functions required in a dual sound carrier TV system for demodulating the sound carriers.
The difference between TDA2555 and TDA2557 is the number of stages of the limiting amplifier.

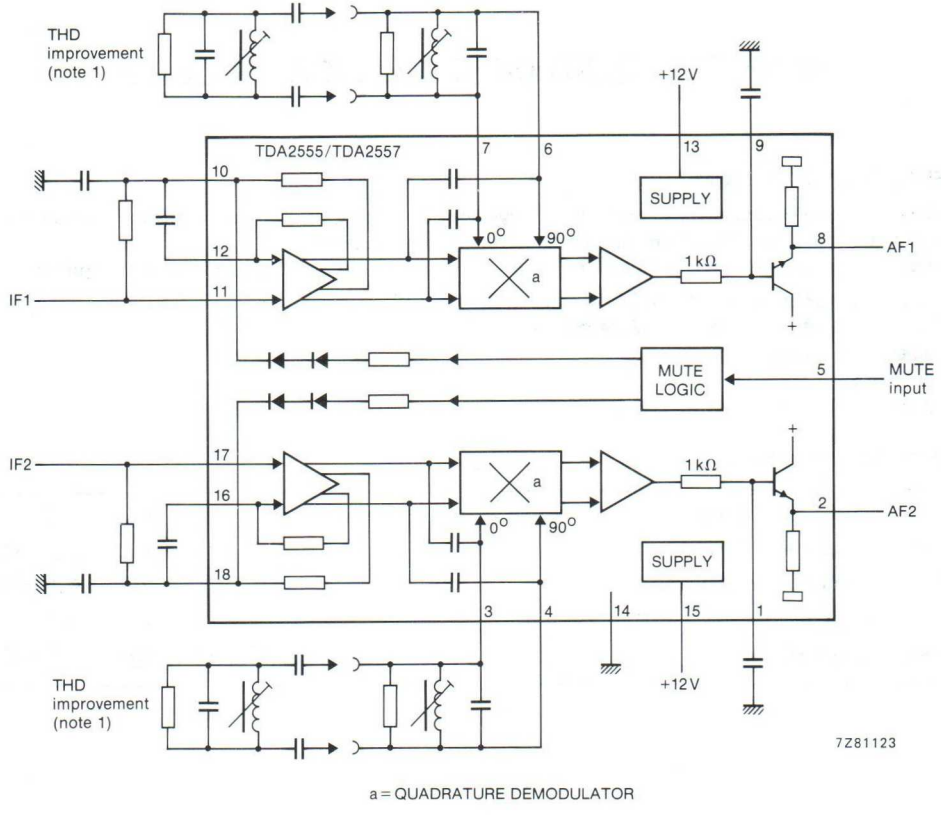
- **Eight** (TDA2555) or **five** (TDA2557) stage limiting amplifier
- Quadrature demodulator for FM detection
- De-emphasis stage
- Output amplifier
- Mute function for each FM demodulator

QUICK REFERENCE DATA

Supply voltage (pins 13 and 15)	V_P	typ.	12	V
Supply current (pins 13 and 15)	I_P	typ.	24,5	mA
AF output voltage (pins 2 and 8)	$V_{o(rms)}$	typ.	600	mV
Total harmonic distortion (note 1)	THD	<	0,1	%
Signal to weighted noise ratio	(S + N)/N	typ.	70	dB

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



a = QUADRATURE DEMODULATOR

Fig. 1 Block diagram.
TDA2555 with 8-stage limiting amplifier;
TDA2557 with 5-stage limiting amplifier.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pins 13 and 15)	V_P	max.	13,2 V
Total power dissipation	P_{tot}	max.	400 mW
Storage temperature range	T_{stg}	−40 to + 150	°C
Operating ambient temperature	T_{amb}	0 to + 70	°C

CHARACTERISTICS

$V_P = V_{13,\ 15\text{-}14} = 12$ V; $T_{amb} = 25$ °C; $f_{IF1} = 5{,}5$ MHz; $f_{IF2} = 5{,}74$ MHz; $f_{m1} = 1$ kHz;
$\Delta f = \pm 30$ kHz;
$V_{i(rms)} = 5$ mV for TDA2555;
$V_{i(rms)} = 10$ mV for TDA2557;
see test circuit Fig. 3, voltages with respect to ground (pin 14), unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Total current consumption	$I_{13,15}$	18	24,5	30	mA
LIMITING AMPLIFIER					
Maximum input voltage	$V_{11\text{-}12(rms)}$ $V_{16\text{-}17(rms)}$	–	200	–	mV
Input voltage for start of limiting (3 dB AF signal reduction)					
TDA2555	$V_{11\text{-}12(rms)}$ $V_{16\text{-}17(rms)}$	–	50	100	μV
TDA2557	$V_{11\text{-}12(rms)}$ $V_{16\text{-}17(rms)}$	–	250	500	μV
DC voltage (input limiting amplifier) pins 11, 12, 16, 17 to 14	V_i	–	2,0	–	V
DC voltage (feedback loop)	$V_{10,18\text{-}14}$	–	2,0	–	V
FM DEMODULATOR					
IF reference signal voltage	$V_{3\text{-}4(rms)}$ $V_{6\text{-}7(rms)}$	–	200	–	mV
DC voltage	$V_{3,4,6,7\text{-}14}$	–	3,1	–	V
AF output voltage	$V_{2\text{-}14(rms)}$	450	600	750	mV
Difference of output signals	$\frac{V_{2\text{-}14}}{V_{8\text{-}14}}$	–	± 0,1	± 0,5	dB
Total harmonic distortion at outputs AF1 and AF2 (note 1)	THD	–	–	0,5	%
A.M. suppression at outputs AF1 and AF2, $f_{FM} = 70$ Hz; $\Delta f = \pm 50$ kHz; $f_{AM} = 1$ kHz; m = 0,3	AMS	50	–	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
FM DEMODULATOR (continued)					
Signal to noise ratio at outputs AF1 and AF2 (CCIR weighted, quasi peak)	$(S+N)/N$	65	70	–	dB
Residual IF-signal without deemphasis	$V_{2,8\text{-}14(rms)}$	–	30	–	mV
Ripple rejection at outputs AF1 and AF2 f = 50 Hz to 20 kHz; $V_{i(rms)}$ = 200 mV	RR	–	40	–	dB
AUDIO OUTPUT STAGE					
emitter follower with 1,0 mA bias current					
DC output voltage	$V_{2,8\text{-}14}$	3,0	4,0	5,0	V
External DC load resistance	$R_{2,8\text{-}14}$	2	–	–	kΩ
AC output current (note 2)	$-I_{2,8\text{-}14(p\text{-}p)}$	–	–	0,5	mA
Deemphasis input resistance (note 3)	$R_{1,9\text{-}14}$	0,8	1,0	1,2	kΩ
DC voltage (deemphasis)	$V_{1,9\text{-}14}$	3,7	4,7	5,7	V
Crosstalk attenuation f = 1 kHz (note 4)	$\alpha_{12,21}$	60	–	–	dB
Crosstalk attenuation f = 10 kHz (note 4)	$\alpha_{12,21}$	60	–	–	dB
Output impedance	$R_{2,8\text{-}14}$	–	25	–	Ω
AF output level (Fig. 2, note 5) MUTE function $V_{i(rms)} < 60$ mV	α	60	–	–	dB
Switching input current $V_{5\text{-}14} = 0$ V	$-I_5$	–	–	500	μA
$V_{5\text{-}14} = V_P$	I_5	–	–	500	μA
Internal d.c. voltage no mute (pin 5 not connected)	$V_{5\text{-}14}$	–	6,2	–	V

Notes to the characteristics

1. THD < 0,1% requires a double tuned demodulator circuit (Q_L = 20). With a single tuned circuit a THD of < 0,5% is possible (see Figs 1 and 3).
2. If higher a.c. output current is required an external resistor must be applied from output (pins 2 and 8) to ground (min. 2 kΩ) in order to improve the THD performance ($-I_{2,8} < 4$ mA).
3. The deemphasis time constant is 50 μs.
4. Crosstalk attenuation is defined as:

$$o_{12} = \frac{V_{2\text{-}14} \text{ unmodulated}}{V_{8\text{-}14}} \qquad o_{21} = \frac{V_{8\text{-}14} \text{ unmodulated}}{V_{2\text{-}14}}.$$

5. In the MUTE state the a.f. output level attenuation is more than 60 dB. The MUTE function is only guaranteed for an r.m.s. value of the input voltage lower than 60 mV. See also Fig. 2.

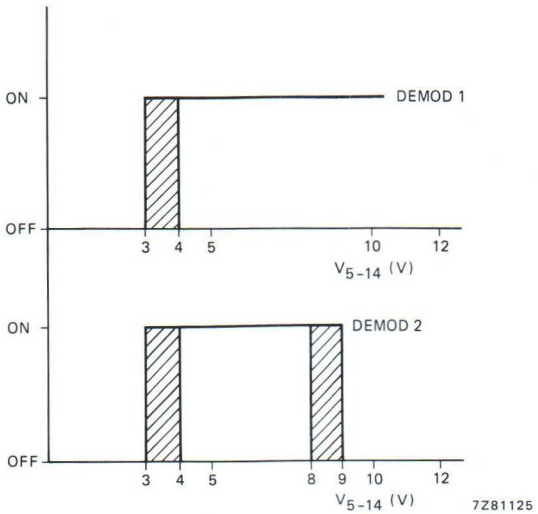


Fig. 2 Mute function.

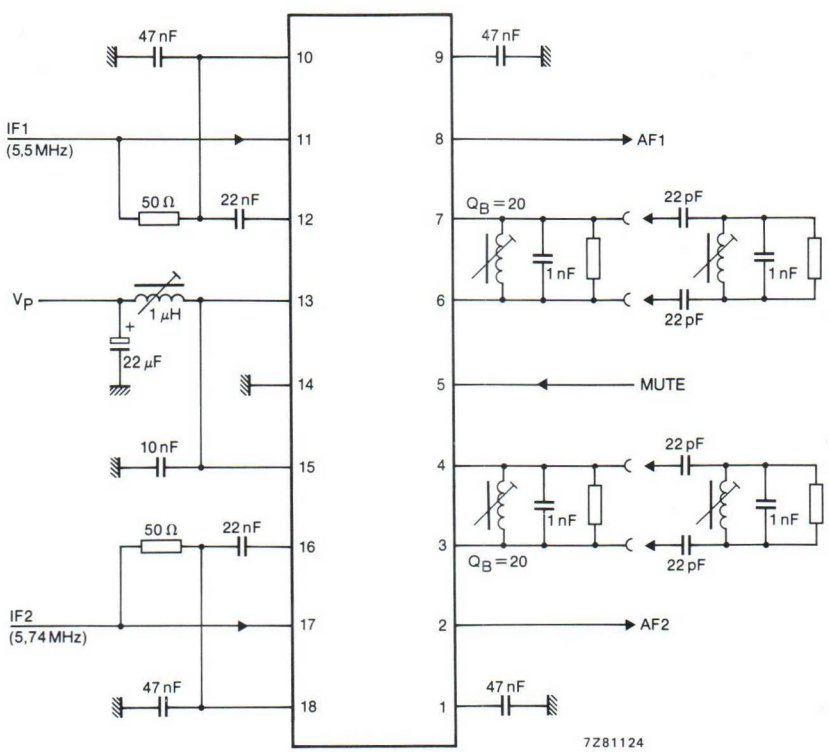


Fig. 3 Test and application circuit.

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