NTEGRATED CIRCUITS

Semiconductors for Wired Telecom Systems

Data Handbook IC03a
1998



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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

PREFACE

Thank you for your interest in wired telecom products from Philips Semiconductors. As a leading supplier to the telephony market, we offer a wide range of discrete and integrated semiconductor telecom components.

A DETAILED REFERENCE SOURCE

This wired telecom handbook includes information on Philips Semiconductors' current integrated circuits and discrete products for wired applications. The products offer a comprehensive solution for wired telephony terminals, from line-interfaces, tone and pulse diallers and discrete devices, though to caller-identification decoders, digital answering-machine processors, hands-free circuits and LCD drivers.

To make selection easier, information is grouped into sections, each accompanied by a product selection guide, which describes the most significant product features. Each section contains detailed product descriptions in the form of data sheets. A new section entitled 'DSP-based solutions' has been added, consolidating the existing product portfolio and extending its range to highly-integrated multi-function telephone terminals.

Relevant application notes are published in the Application Handbook for Wired Telecom Systems (IC03b). Together IC03 part a) and b) provides a comprehensive reference source for wired telephony, including not only details about Philips Semiconductors' products, but also how best to apply them.

COMPREHENSIVE SOLUTIONS

Philips Semiconductors is a recognised leader in enabling technologies, system-level know-how, silicon, software and product development resources to help customers take full advantage of one of the fastest-growing markets in the world. Specifically the company is a leading innovator of products for:

- Caller Identification
- DSP-based solutions: digital answering machine processors, offering full-duplex speakerphone and the highest speech-compression rates on the market.
- Speech and Transmission circuits.
- Listening-in and hands-free circuits.
- Diallers and DTMF generators.
- Derivative telephony-specific micro-controllers (PCD33xx-family); the largest range of configurations and performance options, including low-voltage devices operating down to 1.8V.
- Low-voltage one-time-programmable (OTP) devices, including the PCD3755/56 series, still the lowest-voltage OTPs available.
- Bipolar transistors, regulators and protection diodes.
- LCD display drivers (available additionally as naked die or as chip-on-glass module assemblies).

TECHNOLOGY LEADER

Implementation of cost-effective Telecom terminals demands a broad knowledge, not only at the systems level, but also at the interconnection and component level. Philips Semiconductors' state-of-the art fabrication and packaging expertise provides the technology needed for today's demanding applications, together with the reliability and quality levels customers have come to rely upon from one of the world's top-ten semiconductor companies.

UNRIVALLED RESOURCES

Philips Semiconductors has one of the widest portfolios of technology in semiconductors to meet the needs of the wired telephony market. World-class designs, advanced fabrication processes and up-to-date manufacturing plans and logistics have established Philips Semiconductors as a world supplier. Quality Assurance is based on internationally-accepted quality standards such as ISO9000 and QA9000, as well as customer-specific standards such as Ford's TQE and AT&T's "Partner in Excellence.

CUSTOMER CO-OPERATION

Co-operation with customers is vital for securing market acceptance of customers' products and our own. In addition, we believe that technical partnerships are extremely important for stimulating further development of advanced Telecom technology, and have successful

partnerships with major Telecom systems suppliers and terminal makers.

WORLD-WIDE RESEARCH AND DESIGN-IN SUPPORT

Over 12 per cent of our turnover is invested back into research and development, covering process technology, design, system innovation, type/product development and assembly technology. The result is over 300 new devices per year, along with new technology and process developments, software and services.

We have our own System Laboratories, which explore new uses and applications; act as design and development laboratories to uncover potential problems from customers and help them develop their products faster through shared development; and replicate customer engineering efforts in-house.

Product Development Teams located at our manufacturing and development sites are technology-oriented. Many of our new products are the direct result of work done by the Development Teams, working alone, or in conjunction with groups in the Research or Systems Laboratories.

Philips Corporate Research Labs

Eindhoven, The Netherlands

Redhill, UK

Limeil-BrÈvannes, France

Aachen/Hamburg, Germany

Briarcliff Manor, USA

Philips Semiconductors' System Labs

Eindhoven, The Netherlands

TV, Telephony, Micro-controllers

Southampton, UK

Teletext, digital audio, software for TV and CD-ROM

Hamburg, Germany

Automotive, identification, DSP in radio and TV, Multimedia

Sunnyvale, USA

Multimedia, datacom, automotive

Product Development Teams

Caen, France

Speech and Transmission circuits, hands-free Ics

Zürich, Switzerland

DSP-based solutions, Caller-Identification, Telecom Microcontrollers, LCD drivers, peripheral Ics

Hamburg, Germany

Nijmegen, The Netherlands

Stadskanaal, The Netherlands

Discrete semiconductors and regulators

Semiconductors for Wired Telecom Systems

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2N7002	N-channel vertical D-MOS transistor	x
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BC546; BC547; BC548	NPN general purpose transistors	x
BC556; BC557; BC558	PNP general purpose transistors	x
BC846; BC847; BC848	NPN general purpose transistors	x
BC856; BC857;BC857	PNP general purpose transistors	x
BR211 series	Breakover diodes	x
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BS107A	N-channel enhancement mode vertical D-MOS transistor	x
BS108	N-channel enhancement mode vertical D-MOS transistor	x
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BSN10; BSN10A	N-channel enhancement mode vertical D-MOS transistor	x
BSN20	N-channel enhancement mode vertical D-MOS transistor	x
BSN254; BSN254A	N-channel enhancement mode vertical D-MOS transistors	x
BSN274; BSN274A	N-channel enhancement mode vertical D-MOS transistors	x
BSN304; BSN304A	N-channel enhancement mode vertical D-MOS transistors	x
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BSP304; BSP304A	P-channel enhancement mode vertical D-MOS transistors	x
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TEA1066T	Versatile telephone transmission circuit with dialler interface	171
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P83CL887_P87CL887	12k low-power CT0 microcontroller	840
PCA3351C/52C/53C, PCD3351A/52A/53A	8-bit microcontroller with DTMF generator and 128 bytes EEPROM	845
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REPLACEMENT/WITHDRAWAL TYPES

The following type numbers were in the previous issue of IC03a, but not in the current version:

TYPE NUMBER	REASON FOR DELETION	REPLACEMENT TYPE
PCD3344A	Obsolete	PCD3349A
PCD3356A; PCD3357A	Replaced by new products	
PCD3360	Obsolete per 1998 Jan 01	
PCD4440T	Obsolete per 1998 Jan 01	
PCF84C22A; PCF84C42A	Obsolete per 1999 Jan 01	
TEA1060; TEA1061		TEA1067
TEA1068	Obsolete per1999 Jan 01	TEA1067, TEA1110A
TEA1096; TEA1096A	Obsolete per1999 Jan 01	TEA1097, UBA1707

OVERVIEW OF LISTENING-IN ICs

Type	Details	Supply voltage (V)	Speech part	Line powered	Current consumpt. (mA)	PD[1]
TDA7050	loudspeaker amplifier	1.6 to 6.0	no	no	3.2	no
TDA7052	loudspeaker amplifier	3 to 18	no	no	4	no
TEA1083	call-progress monitor	3.0	no	yes	2.5	no
TEA1083A	TEA1083 with PD	3.0	no	yes	2.5	yes
TEA1085	TEA1083A with dynamic limiter, Larsen level limiter and volume control	3.6 adjustable	no	yes	4.2	yes
TEA1085A	TEA1085 with logic MUTE function instead of toggling function	3.6 adjustable	no	yes	4.2	yes
TEA1097	speech and loudspeaker amplifier IC with auxiliary I/Os and switches	3.0 to 5.3[2] 3.0 to 6.0[3]	yes	yes	3.5[4] 5.5[5]	yes
UBA1707	programmable line interface with loudspeaker amplifier and electronic hook switch	3.0 to 5.5	yes	no	2.2	yes (via bus)

Notes

1. PD = power-down input.
2. Line-powered.
3. Mains-powered.
4. In speech mode.
5. In digital handsfree mode.

Type	Loudspeaker gain (dB)	R_{xout}[1]	Package	Corded	Cordless	Answer machine/fax	Combi fax
TDA7050	26	BTL	DIP8, SO8	no	yes	yes	no
TDA7052	39	BTL	DIP8	no	yes	yes	no
TEA1083	35	SEL	DIP8	yes	yes	no	yes
TEA1083A	35	SEL	DIP16, SO16	yes	yes	no	yes
TEA1085	41	BTL	DIP24, SO24	yes	yes	no	yes
TEA1085A	41	BTL	DIP24, SO24	yes	yes	no	yes
TEA1097	0 to 35	SEL	VSO40	yes	yes	yes	yes
UBA1707	28	SEL	SO28, SSOP28	no	yes	yes	yes

Note

1. BTL = Bridge-Tied Load; SEL = Single-Ended Load.

OVERVIEW OF HANDSFREE ICs

Type	Details	Supply voltage (V)	Speech part	Line powered	Current consumpt. (mA)	PD[1]	$G_{v(Tx)}$ (dB)
TEA1093	includes on-chip power supply	3.6 adjustable	no	yes	5.5	yes	5 to 25
TEA1094	for use with external supply	3.3 to 12	no	no	3.1	no	0 to 31
TEA1094A	TEA1094 with power- down	3.3 to 12	no	no	3.1	yes	0 to 31
TEA1095	TEA1094A without loudspeaker drive capability	2.9 to 12	no	no	2.7	yes	0 to 40
TEA1098	speech + handsfree IC	3.0 to 5.3	yes	yes	3.5[4] 5.5[5]	yes	0 to 31
TEA1099	TEA1098 with auxiliary I/Os and analog switch matrix	3.0 to 5.3[2] 3.0 to 6.0[3]	yes	yes	3.5[4] 5.5[5]	yes	0 to 31

Notes

1. PD = power-down input.
2. Line-powered.
3. Mains-powered.
4. In speech mode.
5. In handsfree mode.

Type	Switching range (dB)	$G_{v(Rx)}$ (dB)	R_{xout}[1]	Package	Corded	Cordless	Answer machine /fax	Combi fax
TEA1093	0 to 52	3 to 39	BTL	DIP28, SO28	yes	yes	no	yes
TEA1094	0 to 52	0 to 33	SEL	DIP28, SO28	yes	yes	no	yes
TEA1094A	0 to 52	0 to 33	SEL	DIP24, SO24, SSOP24	yes	yes	no	yes
TEA1095	0 to 52	−14 to +26	–	DIP24, SO24, SSOP24	yes	yes	no	yes
TEA1098	0 to 52	0 to 35	SEL	VSO40	yes	no	no	no
TEA1099	0 to 52	0 to 35	SEL	QFP44	yes	yes	yes	yes

Notes

1. BTL = Bridge-Tied Load; SEL = Single-Ended Load.

OVERVIEW OF SPEECH/TRANSMISSION ICs

Type	Details	Typ. V_{LN} at 15 mA (V)	Parallel operation	Typ. I_{CC} (mA)	PD[1]	$G_{v(mic)}$ (dB)	Micro MUTE
PCA1070	fully programmable line interface	4.83 (at 12 mA)	yes	2.3	yes	30 to 51	yes
TEA1062	simplified TEA1067 (no power down, single ended receiver)	4.0	yes	0.9	no	44 to 52	no
TEA1062A	TEA1062 with inverted MUTE polarity	4.0	yes	0.9	no	44 to 52	no
TEA1064A	improved TEA1067 with dynamic limiter and powerful DC supply for peripherals	3.6	yes	1.3	yes	44 to 52	yes
TEA1064B	TEA1064A with single ground reference	3.5	yes	1.3	yes	44 to 52	yes
TEA1067	optimized for parallel phones operation	3.9	yes	1	yes	44 to 52	no
TEA1110A	EMC optimized, on-chip default settings	3.65	yes	1.15	no	44	no
TEA1112	EMC optimized, on-chip default settings, LED on-hook/off-hook indication	3.65	yes	1.15	no	39 to 52	yes
TEA1112A	TEA1112 with inverted MUTE polarity	3.65	yes	1.15	no	39 to 52	yes
TEA1113	TEA1112A with Tx Dynamic limiter	4.0	yes	1.3	no	39 to 52	yes
TEA1114A	with 3.3 V stabilized strong supply point	4.35	Yes	1.25	no	44	no
TEA1118	interface for cordless, answering machine and modem	3.65	Yes	1.15	no	0 to 11	no
TEA1118A	TEA1118 with DTMF input	3.65	Yes	1.15	no	11	yes

Note

1. PD = Power Down input.

Type	$G_{v(Rx)}$ (dB)	R_{xout}[1]	Typ. $\Delta G_{v(AGC)}$ (dB)	Package	Corded	Cordless	Answer machine /fax	Combi -fax
PCA1070	−25 to +11	BTL	via software	DIP24, SO24	yes	no	no	yes
TEA1062	20 to 31	SEL	−5.8	DIP16, SO16	yes	no	no	yes
TEA1062A	20 to 31	SEL	−5.8	DIP16, SO16	yes	no	no	yes
TEA1064A	20 to 45	BTL	−6.1	DIP20, SO20	yes	no	no	yes
TEA1064B	20 to 45	BTL	−6.1	DIP20, SO20	yes	no	no	yes
TEA1067	20 to 45	BTL	−5.9	DIP18, SO20	yes	no	no	yes
TEA1110A	19 to 33	SEL	−5.8	DIP14, SO14	yes	no	no	yes
TEA1112	19 to 31	SEL	−5.8	DIP16, SO16	yes	no	yes	yes
TEA1112A	19 to 31	SEL	−5.8	DIP16, SO16	yes	no	yes	yes
TEA1113	19 to 31	SEL	−5.8	DIP16, SO16	yes	no	yes	yes
TEA1114A	19 to 45	SEL	−6.0	DIP16, SO16	yes	no	yes	yes
TEA1118	19 to 31	SEL	−5.8	SSOP16, SO14	no	yes	yes	yes
TEA1118A	19 to 31	SEL	−5.8	SSOP16, SO14	no	yes	yes	yes

Note

1. BTL = Bridge-Tied Load, SEL = Single-Ended Load.

OVERVIEW OF TELECOM MICROCONTROLLERS AND CALLER-ID

TYPE	ROM (kbytes)	RAM (bytes)	EEPROM (bytes)	I/O	OPERATING VOLTAGE (V)	SPECIAL FEATURES	PACKAGE	MAX. SPEED (MHz)	CATEGORY
33xx family (8048-core)									
PCD3349A	4	224	–	20	1.8 to 6.0[1]	DTMF	DIP28, SO28	16	33xx
PCD3350A	8	256	256	34	1.8 to 6.0[1]	DTMF, Melody output, Real-Time Clock, EEPROM	QFP44	16	33xx
PCD3351A	2	64	128	20	1.8 to 6.0[1]	DTMF, Melody output, EEPROM	DIP28, SO28, LQFP32	16	33xx
PCD3352A	4	128	128	20	1.8 to 6.0[1]	DTMF, Melody output, EEPROM	DIP28, SO28, LQFP32	16	33xx
PCD3353A	6	128	128	20	1.8 to 6.0[1]	DTMF, Melody output, EEPROM	DIP28, SO28, LQFP32	16	33xx
PCA3351C	2	64	128	20	1.8 to 6.0[1]	as PCD3351A, 0 to 50 °C, V_{POR} = 2.0 V ±300 mV	DIP28, SO28, LQFP32	16	33xx
PCA3352C	4	128	128	20	1.8 to 6.0[1]	as PCD3352A, 0 to 50 °C, V_{POR} = 2.0 V ±300 mV	DIP28, SO28, LQFP32	16	33xx
PCA3353C	6	128	128	20	1.8 to 6.0[1]	as PCD3353A, 0 to 50 °C, V_{POR} = 2.0 V ±300 mV	DIP28, SO28, LQFP32	16	33xx
PCD3354A	8	256	256	36	1.8 to 6.0[1]	DTMF, Melody output, EEPROM	QFP44	16	33xx
PCA3354C	8	256	256	36	1.8 to 6.0[1]	as PCD3354A, 0 to 50 °C, V_{POR} = 2.0 V ±300 mV	QFP44	16	33xx
PCD3359A	2	64	128	20	1.8 to 6.0[1]	as PCD3351A plus Keyboard Interrupt; Tone disabled during ringing	DIP28, SO28, LQFP32	16	33xx
PCD3755A/E/F	8 (OTP)	128	128	20	1.8 to 6.0[1]	OTP version of 3351A/52A/53A	DIP28, SO28, LQFP32	16	33xx
PCD3756A	8 (OTP)	128	128	20	1.8 to 6.0[1]	OTP version of PCD3359A	DIP28, SO28, LQFP32	16	33xx
84Cxx family (8048-core)									
PCF84C12A	1	64	–	13	2.5 to 5.5	8048-based microcontroller, use external DTMF generator	DIP20, SO20	16	84Cxx
PCF84C81A	8	256	–	20	2.5 to 5.5	8048-based microcontroller with I^2C-bus	DIP28, SO28	16	84Cxx

TYPE	ROM (kbytes)	RAM (bytes)	EEPROM (bytes)	I/O	OPERATING VOLTAGE (V)	SPECIAL FEATURES	PACKAGE	MAX. SPEED (MHz)	CATEGORY
Caller-ID									
PCD3316	–	–	–	–	2.5 to 3.6	Caller-ID decoder (level 2)	SO16	3.58	CIDCW
80CL51 family									
P80CL51	4	128	–	32	1.8 to 6.0	low-voltage 80C51	DIP40, VSO40, QFP44	16	80CL51
P83CL580	6	256	–	40	2.5 to 6.0	ADC, PWM, Watchdog, Timer2, UART, I²C-bus	VSO56, QFP64	12	80CL51
TELX (80CL51-core based, optimized for telecom)									
P87CL881	63	2 kbytes	–	32	2.7 to 3.6	OTP memory, UART, 400 kHz I²C-bus, low-voltage detection	LQFP44	10[2]	TELX
P83CL883	8	256	–	18	2.7 to 3.6	UART, MSK modem, 400 kHz I²C-bus, DTMF, low-voltage detection, In System programming	SO28	3.58[3]/10[2]	TELX
P87CL883	8 (OTP)	256	–	18	2.7 to 3.6	OTP version of P83CL883	SO28	3.58[3]/10[2]	TELX
P83CL884	8	256	128	18	2.7 to 3.6	same as P83CL883 but with additional 128 bytes EEPROM	SO28	3.58[3]/10[2]	TELX
P87CL884	8 (OTP)	256	128	18	2.7 to 3.6	OTP version of P83CL884	SO28	3.58[3]/10[2]	TELX
P83CL886	16	512	–	18	2.7 to 3.6	same as P83CL883, but larger program memory size	SO28	3.58[3]/10[2]	TELX
P87CL886	16 (OTP)	512	–	18	2.7 to 3.6	OTP version of P83CL886	SO28	3.58[3]/10[2]	TELX
P83CL887	12	512	–	18	2.7 to 3.6	same as P83CL883, but larger program memory size	SO28	3.58[3]/10[2]	TELX
P87CL887	12 (OTP)	512	–	18	2.7 to 3.6	OTP version of P83CL887	SO28	3.58[3]/10[2]	TELX

Notes

1. DTMF tone output and/or EEPROM erase/write from 2.5 V.
2. TELX core is twice as fast as the standard 80C51, i.e. 10 MHz clock corresponds to 20 MHz clock on standard 80C51 with the same performance.
3. For DTMF.

OVERVIEW OF LCD DRIVERS

Overview of LCD segment drivers (part 1)

TYPE	SEGMENT @ MULTIPLEX RATE						LOGIC VOLTAGE RANGE (V)	LCD VOLTAGE $V_{OP(MAX)}$ (V)	ON-CHIP BIAS VOLTAGE GENERATOR	INTERFACE
	1:1	1:2	1:3	1:4	1:8	1:16				
PCF2100C		40					2.25-6.5	6.5	X	I^2C-bus
PCF2111C		64					2.25-6.5	6.5	X	I^2C-bus
PCF2112C	32						2.25-6.5	6.5	X	I^2C-bus
PCF8566 (OM4085)[1]	24	48	72	96			2.5-6.0	6.0	X	I^2C-bus
PCF8576 PCF8576C	40	80	120	160			2.5-9.0 2.5-6.0	9.0 6.0	X	I^2C-bus
PCF8577C	32	64					2.5-6.0	6.0	X	I^2C-bus
PCF8578					256	384	2.5-6.0	9.0	X	I^2C-bus
OM4068	32	64	96				2.5-5.5	6.5		2 MHz serial
PCF8533 slim chip	80	160	240	320			2.5-5.5	6.5	X	400 KHz I^2C-bus

Overview of LCD segment drivers (part 2)

TYPE	SPECIAL FEATURES	PACKAGE	APPLICATIONS			
			CORDED	CORDLESS	ANSWER MACH./FAX	COMBI-PHONE
PCF2100C		DIL28, SO28	X		X	
PCF2111C		DIL40, VSO40	X		X	
PCF2112C		VSO40	X		X	
PCF8566 (OM4085)[1]	cascadable with PCF8566/76(C)	DIL40, VSO40	X	X	X	X
PCF8576 PCF8576C	cascadable with PCF8566/76(C)	VSO56, LQFP64	X	X	X	X
PCF8577C		DIL40, VSO40	X		X	
PCF8578	easy blinking, scratch pad RAM	VSO56, LQFP64		X	X	X
OM4068	cascadable	QFP44, DIP40	X	X	X	X
PCF8533 slim chip	cascadable up to 5120	-	X	X	X	X

Note

1. V_{dd} = 2.00 V

Overview of LCD graphic and character drivers (part 1)

TYPE	ROWS	COLUMNS	MATRIX SIZE (LINES × CHARS OR MATRIX SIZE)	LOGIC VOLTAGE RANGE (V)	LCD VOLTAGE $V_{OP(MAX)}$ (V)	ON-CHIP BIAS GEN.	ON-CHIP VOLTAGE MULTIPLIER
Character drivers							
PCF2116	16, 32	60	1 or 2 lines by 24 or 4 lines by 12	2.5-6.0	9	X	X
PCF2104	16, 32	60	1 or 2 lines by 24 or 4 lines by 12	2.5-6.0	9	X	
PCF2105	16, 32	60	1 or 2 lines by 24 or 4 lines by 12	2.5-6.0	9	X	
PCF2113	18	60	2 lines by 12 + icons or 1 line by 24 + icons	1.8-5.5	6.5	X	X
PCF2103	18	60	2 lines by 12 + icons or 1 line by 24 + icons	1.8-5.5	6.5	X	
PCF2119 slim chip	9, 18	80	1 line by 32 or 2 lines by 16 + icons	1.5-4.0	6.5	X	X
Graphic drivers							
PCF8558 slim chip	40	101	40 × 101	2.5-6.0	9	X	
PCF8578	8, 16, 24, 32	32, 24, 16, 8	any	2.5-6.0	9		
PCF8579		40	any	2.5-6.0	9		
OM6202	65	102	65 × 102	2.5-3.5	16	X	X
PCF8549, OM6204	65	102	65 × 102	1.5-6.0	16	X	X

Overview of LCD graphic and character drivers (part 2)

TYPE	INTERFACES	TEMP. COMP.	PACKAGES	XTAL/ BUMPS	APPLICATIONS				
					MOBILE PHONE	CORDED CALLER ID	CORDLESS	ANSWER MACH./FAX	COMBI-PHONE
Character drivers									
PCF2116	I²C-bus and parallel 4/8bit		LQFP128	X/X	X	X			X
PCF2104	I²C-bus and parallel 4/8bit		-	X/X	X				X
PCF2105	400 kHz I²C-bus and parallel 4/8bit		-	X/X	X				X
PCF2113	400 kHz I²C-bus and parallel 4/8bit	X	LQFP100	X/X	X			X	X
PCF2103	400 kHz I²C-bus and parallel 4/8bit		-	X/X	X		X	X	X
PCF2119 slim chip	400 kHz I²C-bus and parallel 4/8bit	X	-	X	X	X	X	X	X
Graphic drivers									
PCF8558 slim chip	400 kHz I²C-bus		-	X	X		X		X
PCF8578	I²C-bus		VSO56, LQFP64	X/X			X	X	X
PCF8579	I²C-bus		VSO56, LQFP64	X/X			X	X	X
OM6202	parallel	X	TCP	X	X				X
PCF8549, OM6204	400 kHz I²C-bus	X	TCP tray	X	X		X		

LF Small-signal Transistors — Selection guide

MAX. V_{CEO}/I_C	DESCRIPTION	POL.	PACKAGE				
			SOT23	SOT89	SOT143	SOT223	SOT323/SC-70
10 V/3 A	BISS transistors (breakthrough in small-signal transistors)	npn				BDL31	
10 V/3 A		pnp				BDL32	
40 V/1 A		npn	PMMT491A				
40 V/1 A		pnp	PMMT591A				
15 V/100 mA	high speed switching	npn	PMBT2369			PZT2369A	PMST2369
40 V/800 mA		npn	PMBT2222A	PXT2222A		PZT2222A	PMST2222A
60 V/600 mA		pnp	PMBT2907A	PXT2907A		PZT2907A	PMST2907A
50 V/100 mA	resistor-equipped transistors for switching purposes	npn	PDTC114TT				PDTC114TU
50 V/100 mA		npn					
50 V/100 mA		pnp	PDTA114TT				PDTA114TU
50 V/100 mA		npn	PDTC114ET				PDTC114EU
50 V/100 mA		npnp					
50 V/100 mA		pnp	PDTA114ET				PDTA114EU
50 V/100 mA		npn					
50 V/100 mA		npn					
50 V/100 mA		pnp					
50 V/100 mA		npn	PDTC124ET				PDTC124EU
50 V/100 mA		npnp					
50 V/100 mA		pnp	PDTA124ET				PDTA124EU
50 V/100 mA		npn					
50 V/100 mA		pnp					
50 V/100 mA		npn	PDTC143ET				PDTC143EU
50 V/100 mA		pnp	PDTA143ET				PDTA143EU
50 V/100 mA		npn	PDTC144ET				PDTC144EU
50 V/100 mA		pnp	PDTA144ET				PDTA144EU
20 V/1 A	high current transistors	npn		BC868		BCP68	
20 V/1 A		pnp		BC869		BCP69	
150 V/300 mA	high voltage transistors	pnp	PMBT5401			PZT5401	PMST5401
160 V/300 mA		npn	PMBT5550			PZT5551	PMST5550
300 V/500 mA		pnp	PMBTA92	PXTA92		PZTA92	PMSTA92
300 V/500 mA		npn	PMBTA42	PXTA42		PZTA42	PMSTA42
350 V/300 mA		npn				PZTA44	

MAX. V_{CEO}/I_C	PACKAGE			FEATURES
	SC-59	SC-88	SC-75	
10 V/3 A				very low V_{CEsat}: 180 mV at I_C = 1 A; I_B = 20 mA
10 V/3 A				very low V_{CEsat}: 250 mV at I_C = 1 A; I_B = 20 mA
40 V/1 A				very low V_{CEsat}: < 350 mV at I_C = 500 mA; I_B = 50 mA
40 V/1 A				very low V_{CEsat}: < 300 mV at I_C = 500 mA; I_B = 50 mA
15 V/100 mA				t_{on}: 10 ns at 10 mA/3 mA/–1.5 mA
40 V/800 mA				t_{on}: 35 ns at 150 mA/15 mA/–15 mA
60 V/600 mA				t_{on}: 40 ns at –150 mA/–15 mA/15 mA
50 V/100 mA	PDTC114TK			R1/R2: 10 kΩ/-
50 V/100 mA			PDTC114TE	R1/R2: 10 kΩ/-
50 V/100 mA	PDTA114TK	PUMB4		R1/R2: 10 kΩ/-
50 V/100 mA	PDTC114EK	PUMH11	PDTC114EE	R1/R2: 10 kΩ/10 kΩ
50 V/100 mA		PUMD3		R1/R2: 10 kΩ/10 kΩ
50 V/100 mA	PDTA114EK		PDTA114EE	R1/R2: 10 kΩ/10 kΩ
50 V/100 mA			PDTC114YE	R1/R2: 10 kΩ/47 kΩ
50 V/100 mA			PDTC123JE	R1/R2: 22 kΩ/47 kΩ
50 V/100 mA			PDTA123JE	R1/R2: 22 kΩ/47 kΩ
50 V/100 mA	PDTC124EK	PUMH1	PDTC124EE	R1/R2: 22 kΩ/22 kΩ
50 V/100 mA		PUMD2		R1/R2: 22 kΩ/22 kΩ
50 V/100 mA	PDTA124EK		PDTA124EE	R1/R2: 22 kΩ/22 kΩ
50 V/100 mA			PDTC124XE	R1/R2: 22 kΩ/47 kΩ
50 V/100 mA			PDTA124XE	R1/R2: 22 kΩ/47 kΩ
50 V/100 mA	PDTC143EK		PDTC143EE	R1/R2: 4.7 kΩ/4.7 kΩ
50 V/100 mA	PDTA143EK		PDTA143EE	R1/R2: 4.7 kΩ/4.7 kΩ
50 V/100 mA	PDTC144EK		PDTC144EE	R1/R2: 47 kΩ/47 kΩ
50 V/100 mA	PDTA144EK		PDTA144EE	R1/R2: 47 kΩ/47 kΩ
20 V/1 A				medium power
20 V/1 A				medium power
150 V/300 mA				low capacitance: C_c < 6 pF
160 V/300 mA				low capacitance: C_c < 6 pF
300 V/500 mA				
300 V/500 mA				
350 V/300 mA				

LF Small-signal Transistors — Selection guide

MAX. V_{CEO}/I_C	DESCRIPTION	POL.	PACKAGE				
			SOT23	SOT89	SOT143	SOT223	SOT323/SC-70
45 V/100 mA	general purpose transistors	pnp					2PA1576[1]
45 V/500 mA		pnp	BC807				BC807W
45 V/500 mA		npn	BC817				BC817W
45 V/100 mA		pnpn					
45 V/100 mA		npnp					
50 V/100 mA		npn					2PC4081[1]
65 V/100 mA		npn	BC847		BCV61/63		BC847W
65 V/100 mA		pnp	BC857		BCV62/64		BC857W

Note

1. Only available in tight DC current gain groups.

MAX. V_{CEO}/I_C	PACKAGE			FEATURES
	SC-59	SC-88	SC-75	
45 V/100 mA	2PB709A[1]	PUMT1	2PA1774[1]	
45 V/500 mA	2PD602A			high amplification at high currents
45 V/500 mA	2PB710A			high amplification at high currents
45 V/100 mA		PUMZ1		
45 V/100 mA		BC847BPN		tight h_{FE} matching
50 V/100 mA	2PD601A[1]	PUMX1	2PC4617[1]	
65 V/100 mA		BC847BS	BC847T	SOT143: current mirror; SC88: tight h_{FE} matching
65 V/100 mA		BC857BS	BC857T	SOT143: current mirror; SC88: tight h_{FE} matching

Note

1. Only available in tight DC current gain groups.

N-CHANNEL MOS-FETS

TYPE NUMBER	PACKAGE	RATINGS			CHARACTERISTICS						
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	V_{GSth} (V)	R_{DSon} (Ω)		at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
						typ.	max.				
BS107	SOT54/TO-92var	200	150	830	0.8 to 2.4	20	28	20	2.6	10/20	
BS107A	SOT54/TO-92	200	250	600	1 to 3	4.5	6.4	250	10	5/15	
BS108	SOT54/TO-92	200	250	1000	0.4 to 1.8	5	8	100	2.8	10/30	
BS170	SOT54/TO-92var	60	500	830	0.8 to 3	2.5	5	200	10	10/10	
BSN10	SOT54/TO-92	50	175	830	0.4 to 1.8	8	15	100	10	5/10	
BSN10A	SOT54/TO-92	50	175	830	0.4 to 1.8	8	15	100	10	5/10	
BSN20	SOT23	50	100	250	0.4 to 1.8	8	15	100	10	5/10	
BSN254	SOT54/TO-92var	250	300	1000	0.8 to 2	5	10	20	2.4	10/30	
BSN254A	SOT54/TO-92var	250	300	1000	0.8 to 2	5	10	20	2.4	10/30	
BSN274	SOT54/TO-92var	270	250	1000	0.8 to 2	9	14	20	2.4	10/30	
BSN274A	SOT54/TO-92var	270	250	1000	0.8 to 2	9	14	20	2.4	10/30	
BSN304	SOT54/TO-92var	300	250	1000	0.8 to 2	7.9	14	20	2.4	10/30	
BSN304A	SOT54/TO-92var	300	250	1000	0.8 to 2	7.9	14	20	2.4	10/30	
BSP126	SOT223	250	350	1500	0.8 to 2	5	10	20	2.4	10/30	
BSP130	SOT223	300	300	1500	0.8 to 2	6.7	8	250	10	10/30	
BSS89	SOT54/TO-92var	200	300	1000	0.8 to 2.8	4.5	6	400	10	5/15[1]	
BST74A	SOT54/TO-92var	200	250	1000	0.8 to 2.8	6	12	250	10	10/25	
PMBF107	SOT23	200	100	250	0.8 to 2.4	20	28	20	2.6	10/20	
PMBF170	SOT23	60	250	300	0.8 to 3	2.5	5	200	10	10/15	
2N7000	SOT54/TO-92var	60	280	830	0.8 to 3	3.5	5.3	75	4.5	10/10	
2N7002	SOT23	60	180	300	0.8 to 3	3.5	5.3	75	4.5	10/15	

Note

1. Typical values.

P-CHANNEL MOS-FETS

TYPE NUMBER	PACKAGE	RATINGS			CHARACTERISTICS						
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	V_{GSth} (V)	R_{DSon} (Ω) typ.	R_{DSon} (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
BSP92	SOT223	240	180	1500	0.8 to 2	10	20	180	10	10/30	
BSP225	SOT223	250	225	1500	0.8 to 2.8	10	15	200	10	10/30	
BSP254	SOT54/TO-92var	250	200	1000	0.8 to 2.8	10	15	200	10	10/30	
BSP254A	SOT54/TO-92var	250	200	1000	0.8 to 2.8	10	15	200	10	10/30	
BSP255	SOT223	300	325	4000	0.8 to 2	–	17	160	10	4/25[1]	
BSP304	SOT54/TO-92var	300	170	1000	1.95 to 2.8	–	17	170	10	10/30	
BSP304A	SOT54/TO-92var	300	170	1000	1.95 to 2.8	–	17	170	10	10/30	
BSS92	SOT54/TO-92var	240	150	1000	0.8 to 2.8	10	20	100	10	5/20[1]	

Note

1. Typical values.

N-CHANNEL / P-CHANNEL / COMPLEMENTARY MULTI-CHIP POWERMOS

TYPE NUMBER	PACKAGE	CHANNEL	RATINGS			CHARACTERISTICS						
			V_{DS} (V)	I_D (mA)	P_{tot} (mW)	V_{GSth} (V)	R_{DSon} (Ω) typ.	R_{DSon} (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
PHC2300	SOT96-1 (SO8)	N	300	340	1600	0.8 to 2	–	8	175	10	10/30	
		P	300	235	1600	0.8 to 2	–	17	115	10	10/35	

VOLTAGE REGULATOR DIODE

TYPE NUMBER	RATINGS						CHARACTERISTICS		PACKAGE (not to scale)
	P_{tot} @ T_{tp} max.		P_{ZSM} @ T_j and t_p max.			P_{RSM} max.	V_Z nom. E24 range	V_R[1] min.	
	(W)	(°C)	(W)	(°C)	(ms)	(W)	(V)	(V)	
LEADED TYPE									
BZW03 series	6.0	25	1000	25	0.1	500	7.5 to 270	6.2 to 430	 SOD64

Note

1. Device used as a voltage suppressor diode.

Breakover Diodes

The Philips BreakOver Diode (BOD) is a two terminal, transient over-voltage suppressor which operates in either an 'off' (non-conducting) or an 'on' (conducting) state. The BOD will remain in the off-state until a transient voltage exceeding the maximum breakover voltage is applied across its terminals. Provided sufficient current is available to switch the device on, it will then switch to the on-state, and conduct with a low on-state voltage. It will remain in the on-state until the transient decays away and the current falls below the holding current.

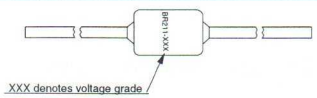
The device is available in either a conventional leaded axial package or an axial surface mounted package.

The main area of application for breakover diodes is over-voltage protection in line based telecommunications equipment (telephones, faxes, modems, internet terminals etc) and also in telephone exchange line cards. Their main features are:-

1. 40 Amp surge capability, (10/700µs impulse).
2. Breakover voltages 140 V to 280 V.
3. Low on-state voltage ≤ 2.5 V.
4. Low leakage current in the off-state ≤ 10 µA.
5. High holding current ≥ 150 mA.



Symbol



SOD84 Axial package



SOD106 Surface mount package

Avalanche voltage I_D = 10mA	Breakover voltage	Peak pulse current 10/700µs pulse	Holding current	Switching current	Type number	
V_{BR} (V)	V_{BO} (V)	I_{TSM} (A)	I_H (mA)	I_S (A)		
MIN	MAX	MAX	MIN	MAX		
123	157	40	150	1	BR211-140	BR211SM-140
140	180	40	150	1	BR211-160	BR211SM-160
158	202	40	150	1	BR211-180	BR211SM-180
176	224	40	150	1	BR211-200	BR211SM-200
193	247	40	150	1	BR211-220	BR211SM-220
211	269	40	150	1	BR211-240	BR211SM-240
228	292	40	150	1	BR211-260	BR211SM-260
246	314	40	150	1	BR211-280	BR211SM-280

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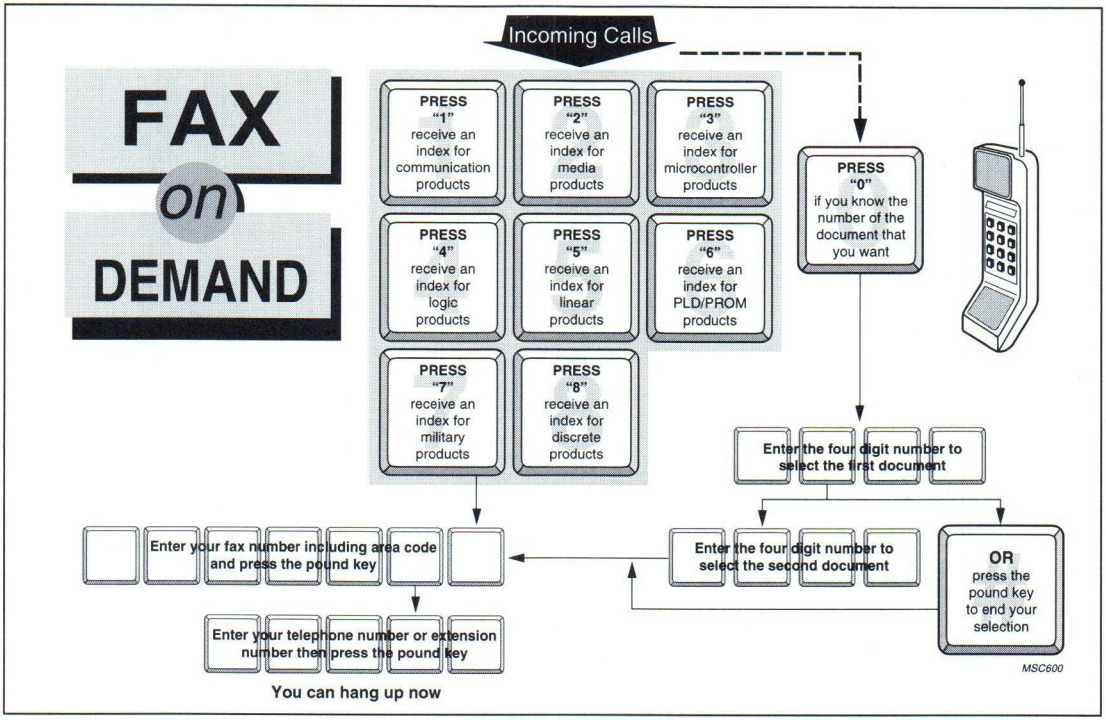
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FAX-ON-DEMAND PHONE NUMBERS

United Kingdom, Ireland	44-181-730-5020
France	33-1-40-996060
Italy	39-167-295502
North America	1-800-282-2000

LOCATIONS SOON TO BE IN OPERATION

- Hong Kong
- Japan
- The Netherlands.

GENERAL

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TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

DISCRETE SEMICONDUCTORS

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A Germanium or other material with a band gap of 0.6 to 1 eV

B Silicon or other material with a band gap of 1 to 1.3 eV

C Gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more

R Compound materials, e.g. cadmium sulphide.

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.

In the following list low power types are defined by $R_{th\ j\text{-}mb} > 15$ K/W and power types by $R_{th\ j\text{-}mb} \leq 15$ K/W.

A Diode; signal, low power

B Diode; variable capacitance

C Transistor; low power, audio frequency

D Transistor; power, audio frequency

E Diode; tunnel

F Transistor; low power, high frequency

G multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter, see under "Serial number/special third letter"

H Diode; magnetic sensitive

L Transistor; power, high frequency

N Photocoupler

P Radiation detector; e.g. high sensitivity photo-transistor; with special third letter

Q Radiation generator; e.g. LED, laser; with special third letter

R Control or switching device; e.g. thyristor, low power; with special third letter

S Transistor; low power, switching

T Control and switching device; e.g. thyristor, power; with special third letter

U Transistor; power, switching

W Surface acoustic wave device

X Diode; multiplier, e.g. varactor, step recovery

Y Diode; rectifying, booster

Z Diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER/SPECIAL THIRD LETTER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.(1) The letter has no fixed meaning, except in the following cases:

A For triacs, after second letter 'R' or 'T'

F For emitters and receivers in fibre-optic communication, after second letter 'G', 'P' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

L For lasers in non-fibre-optic applications, after second letter 'G' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

O For opto-triacs, after second letter 'R'

T For 3-state bicolour LEDs, after second letter 'Q'

W For transient voltage suppressor diodes, after second letter 'Z'.

EXAMPLES OF BASIC TYPE NUMBERS

AA112 Germanium, low power signal diode (consumer type)

ACY32 Germanium, low power AF transistor (industrial type)

BD232 Silicon, power AF transistor (consumer type)

CQY17 GaAs, light-emitting diode (industrial type)

RPY84 CdS, photo-conductive cell (industrial type).

Version letter(s)

One or two letters may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type. The letters never have a fixed meaning, except that the letter 'R' indicates reverse polarity and the letter 'W' indicates a surface mounted device (SMD).

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

Suffix

Sub-classification can be used for devices supplied in a wide range of variants, called associated types. The following sub-coding suffixes are in use:

VOLTAGE REFERENCE AND VOLTAGE REGULATOR DIODES

One letter and one number, preceded by a hyphen (-). The letter, if required, indicates the nominal tolerance of the Zener voltage.

A 1%
B 2%
C 5%
D 10%
E 20%.

In the case of a 3% tolerance, the letter 'F' is used.

The number denotes the typical operating (Zener) voltage, related to the nominal current rating for the entire range. The letter 'V' is used in place of the decimal point.

Example: BZY74-C6V3 or -C10.

TRANSIENT VOLTAGE SUPPRESSOR DIODES

One number, preceded by a hyphen (-). The number indicates the maximum recommended continuous reversed (stand-off) voltage, V_R. The letter 'V' is used in place of the decimal point.

Example: BZW70-9V1 or –39.

The letter 'B' may be used immediately after the last number, to indicate a bidirectional suppressor diode.

Example: BZW10-15B.

CONVENTIONAL AND CONTROLLED AVALANCHE RECTIFIER DIODES AND THYRISTORS

One number, preceded by a hyphen (-). The number indicates the rated maximum repetitive peak reverse voltage, V_{RRM}, or the rated repetitive peak off-state voltage, V_{DRM}, whichever is the lower. Reversed polarity with respect to the case is indicated by the letter 'R' immediately after the number.

Example: BYT-100 or -100R.

RADIATION DETECTORS

One number, preceded by a hyphen (-). The number indicates the depletion layer in micrometres (μm). The resolution is indicated by a version letter.

Example: BPX10-2A.

ARRAY OF RADIATION DETECTORS AND GENERATORS

One number, preceded by a hyphen (-). The number indicates the number of basic devices assembled into the array.

Examples: BPW50-6, BPW50-9, BPW50-12.

HIGH FREQUENCY POWER TRANSISTORS

One number, preceded by a hyphen (-). The number indicates the supply voltage.

Example: BLU80-24.

INTEGRATED CIRCUITS

Basic type number

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

FIRST AND SECOND LETTERS

Digital family circuits

The first two letters identify the family.(1)

Solitary circuits

The first letter divides solitary circuits into:

S Solitary digital circuits
T Analog circuits
U Mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(2)

Microprocessors

The first two letters identify microprocessors and related circuits:

MA Microcomputer or central processing unit
MB Slice processor (functional slice of microprocessor)

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.
(2) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

MD Related memories

ME Other related circuits such as interfaces, clocks, peripheral controllers, etc.

Charge-transfer devices and switched capacitors

The first two letters identify:

NH Hybrid circuits

NL Logic circuits

NM Memories

NS Analog signal processing using switched capacitors

NT Analog signal processing using charge-transfer devices

NX Imaging devices

NY Other related circuits.

THIRD LETTER

The third letter indicates the operating ambient temperature range:

A temperature range not specified below

B 0 to + 70 °C

C −55 to +125 °C

D −25 to + 70 °C

E −25 to + 85 °C

F −40 to + 85 °C

G −55 to + 85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

Serial number

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

Version letter

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C Cylindrical

D Ceramic dual in-line (CERDIL, CERDIP)

F Flat pack (two leads)

G Flat pack (four leads)

H Quad flat pack (QFP)

L Chip on tape (foil)

P Plastic dual in-line (DIL)

Q Quad in-line (QUIL)

T Mini pack (SOL, SO, VSO)

U Uncased chip.

Two-letter suffix

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

FIRST LETTER (GENERAL SHAPE)

C Cylindrical

D Dual in-line (DIL)

E Power DIL (with external heatsink)

F Flat pack (leads on two sides)

G Flat pack (leads on four sides)

H Quad flat pack (QFP)

K Diamond (TO-3 family)

M Multiple in-line (except dual, triple and quad)

Q Quad in-line (QUIL)

R Power QUIL (with external heatsink)

S Single in-line (SIL)

T Triple in-line

W Leaded chip carrier (LCC)

X Leadless chip carrier (LLCC)

Y Pin grid array (PGA).

SECOND LETTER (MATERIAL)

C Metal-ceramic

G Glass-ceramic

M Metal

P Plastic.

Examples

PCF1105WP: digital IC; PC family; operating temperature range –40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range –55 to +125 °C; serial number 2000.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor.
- All mains-powered electrical equipment should be connected via an earth leakage switch.
- Equipment cases should be earthed.
- Relative humidity should be maintained between 50 and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

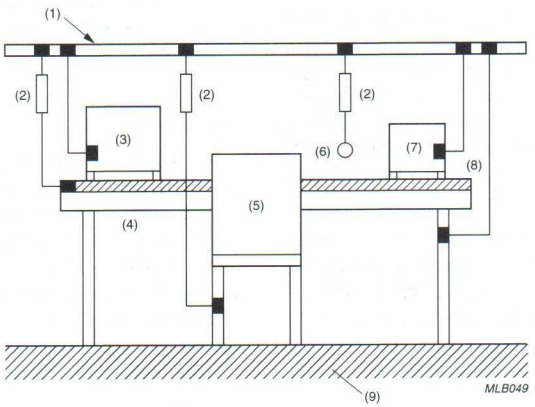
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.
(9) Antistatic floor.

Fig.1 Protected work station.

SPEECH/TRANSMISSION CIRCUITS

Multistandard programmable analog CMOS transmission IC

PCA1070

FEATURES

- Line interface with:
  - Voltage regulator with programmable DC voltage drop
  - Programmable set impedance
  - Output to control an external switching MOS transistor for pulse dialling
  - Programmable DC voltage during pulse dialling
  - Circuitry for short DC settling time
- Interface to peripheral circuits with:
  - Supply for microcontroller and DTMF diallers
  - Input to sense supply voltage of microcontroller and output for reset of microcontroller
  - I²C-bus (programming of parameters, control of all logic signals)
  - High impedance DTMF signal input
  - Input for external oscillator signal with on-chip DC blocking
  - Power-down via the I²C-bus
  - Stabilized supply for electret microphone
- Microphone and DTMF amplifiers:
  - Low-noise microphone preamplifier suitable for various types of microphones
  - Symmetrical high impedance microphone preamplifier inputs
  - Programmable gain for microphone and DTMF channels
  - Sending mute via the I²C-bus to disable microphone amplifier and enable DTMF amplifier
  - Sending mute also to be used as privacy switch
  - Dynamic limiting (speech controlled) to prevent distortion of line signal and sidetone; programmable maximum sending level
- Receiving amplifier:
  - Suitable for various types of earpieces (including piezo)
  - Programmable gain and hearing protection level
  - Receiving mute via the I²C-bus to disable receiving amplifier and enable DTMF confidence tone
  - On-chip anti-sidetone circuit with programmable sidetone balance
  - Confidence tone in the earpiece during DTMF dialling



- Facility to regulate parameters with line current:
  - Value of DC line current (bit code) readable via the I²C-bus
  - Line loss compensation with fully software programmable characteristics (control range, stop current) of microphone/earpiece/DTMF amplifiers
  - Fully software programmable control of sidetone balance and DC voltage drop as a function of line length.

APPLICATIONS

- Wired telephony (basic till feature phones)
- Combi-terminals (e.g. telephone and answering machine or FAX)
- Modems and base units of cordless telephones.

GENERAL DESCRIPTION

The PCA1070 is a CMOS integrated circuit performing all speech and line interface functions in fully electronic telephone sets. The device requires a minimum of external components. The transmission parameters are programmable via the I²C-bus. This makes the IC adaptable to nearly all worldwide country requirements and to a various range of speech transducers, without changing the (few) external components.

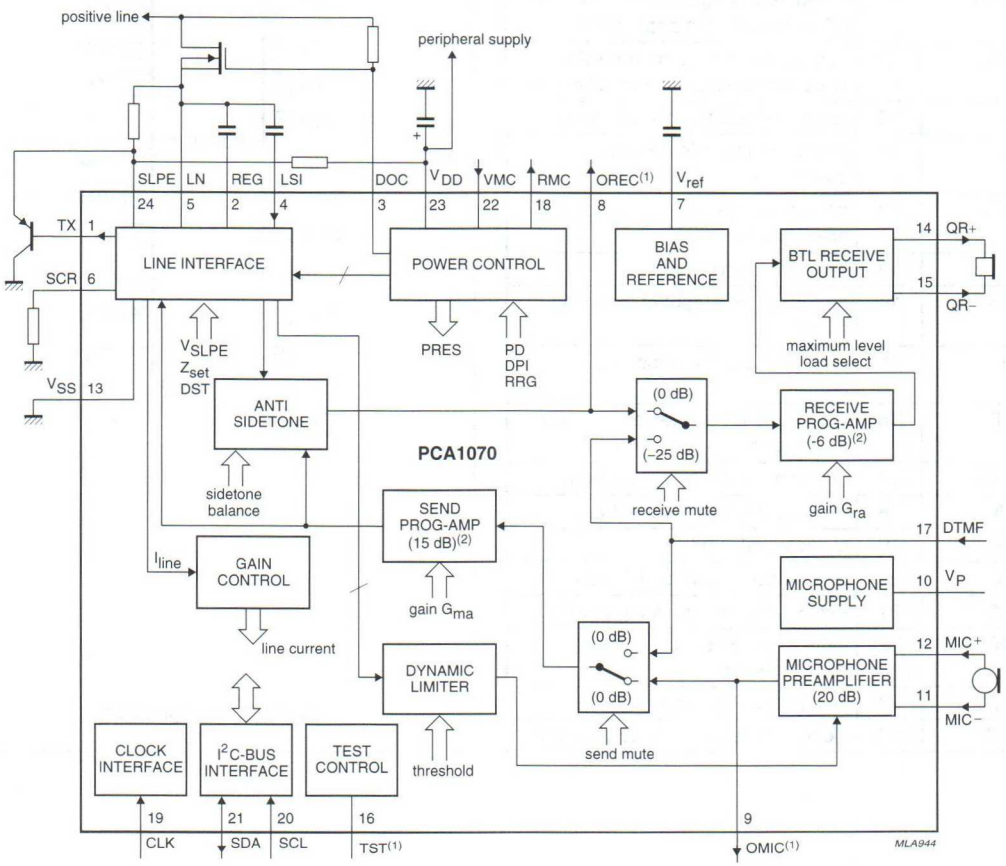
The parameters are stored in the EEPROM of a microcontroller and are loaded into the PCA1070 during the start-up phase of the transmission IC after hook-off.

The PCA1070 also allows adaptation to the connected telephone line by reading the line current via the I²C-bus and processing it in the microcontroller.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA1070P	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
PCA1070T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM



(1) Test pins.
(2) Default value.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TX	1	drive output
REG	2	voltage regulator decoupling
DOC	3	dial output connection
LSI	4	line signal input
LN	5	positive line terminal
SCR	6	sending current resistor
V_{ref}	7	voltage reference decoupling
OREC	8	output receiving preamplifier; to be left open-circuit in application
OMIC	9	output microphone preamplifier; to be left open-circuit in application
V_P	10	supply for electret microphones
MIC–	11	inverting input microphone preamplifier
MIC+	12	non-inverting input microphone preamplifier
V_{SS}	13	negative line terminal
QR+	14	non-inverting output of receiving amplifier
QR–	15	inverting output of receiving amplifier
TST	16	test pin; to be connected to V_{SS} in application
DTMF	17	dual tone multi-frequency input
RMC	18	reset output for microcontroller
CLK	19	clock signal input
SCL	20	serial clock line input; I^2C-bus
SDA	21	serial data line input/output; I^2C-bus
VMC	22	input to sense supply voltage microcontroller
V_{DD}	23	positive supply decoupling
SLPE	24	slope (DC resistance) adjustment

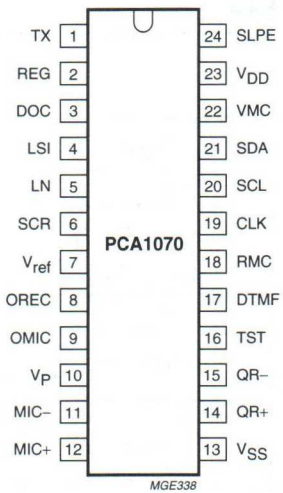


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

All values in the Chapter "Functional description" are typical unless stated otherwise.

Line interface

DC VOLTAGE DROP

Power for the PCA1070 and its peripheral circuits is obtained from the telephone line. The IC develops its own supply voltage at V_{DD} and regulates its DC voltage drop between pins SLPE and V_{SS}. This voltage (V_{SLPE}) can be programmed via the I²C-bus interface between 3.1 to 5.9 V and is default at 4.7 V (see Table 8).

The DC line voltage at pin LN can be calculated using the following equation:

$$V_{LN} = V_{SLPE} + (I_{line} - I_{LN}) \times R_{LN\text{-}SLPE}$$

where:

I_{LN} = DC bias current flowing into pin LN (≈3 mA if I_{line} > 17 mA)

$R_{LN\text{-}SLPE}$ = external 20 Ω resistor between LN and SLPE.

At line currents below 6 mA the DC voltage V_{SLPE} is automatically adjusted to a lower value. This means that the operation of more sets, connected in parallel, is possible with reduced sending and receiving levels and relaxed performance. At line currents below 16 mA the DC bias current I_{LN} is reduced from ≈3 mA to a lower value to ensure maximum possible transmit level capability under all line current conditions.

SET IMPEDANCE

In normal conditions $I_{line} >> I_{LN}$ and the static behaviour is equivalent to a voltage regulator diode with a series resistor $R_{LN\text{-}SLPE}$. In the audio frequency range the dynamic impedance Z_{LN} is determined mainly by the internal component $Z_{set} = R_a + (R_b // C)$. The equivalent impedance Z_{LN} is shown in Fig.3. The values of R_a, R_b and C can be programmed via the I²C-bus interface (see Tables 9, 10 and 11).

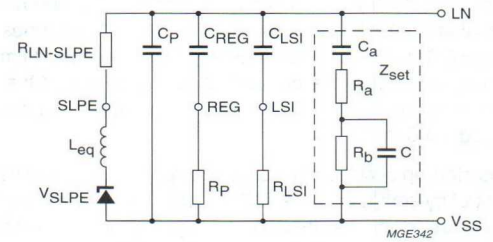


Fig.3 Equivalent impedance Z_{LN}.

where:

C_a = DC blocking capacitor (influence negligible at f ≥ 300 Hz for given value of C_{LSI})

C_{LSI} = capacitor at pin LSI (100 nF)

C_P = internal capacitor (12 nF)

C_{REG} = capacitor at pin REG (470 nF)

L_{eq} = artificial inductor (= $R_P \times R_{LN\text{-}SLPE} \times C_{REG}$ = 10.1 H at V_{SLPE} = 4.7 V)

$R_{LN\text{-}SLPE}$ = DC slope resistance (20 Ω)

R_P = internal resistor (1075 kΩ at V_{SLPE} = 4.7 V)

R_{LSI} = internal resistor (240 kΩ).

SUPPLY FOR PERIPHERAL CIRCUITS

The supply voltage V_{DD} can be used for peripheral circuitry. The supply capabilities depend on the programmed DC voltage drop V_{SLPE} and on several other parameters as given in the following equation:

$$V_{DD} = V_{SLPE} - (I_{DD} + I_p + I_{VP}) \times R_{SLPE\text{-}VDD}$$

where:

I_{DD} = internal current consumption PCA1070 (2.3 mA)

I_p = current to peripheral circuitry

I_{VP} = current taken from V_P for electret microphone

$R_{SLPE\text{-}VDD}$ = external resistor between SLPE and V_{DD}.

DC STARTING AND SETTLING TIME

The IC is equipped with circuitry for fast DC start-up. This circuit is automatically activated as soon as V_{DD} reaches 3 V after hook-off, and is deactivated when V_{SLPE} drops below 5.9 V. This ensures that only a relatively short time is needed to reach the default DC setting (V_{SLPE}) of the circuit and that V_{DD} will not exceed the maximum permitted voltage of 6 V.

The start-up circuit can also be activated under software control by setting bit code DST to logic 1 via the I^2C-bus. The start-up time can be optimized by programming the bit code DST to logic 1 during the start-up procedure.
In practice this is possible as soon as the microcontroller has become operational. The DST bit can also be used to quickly restore the DC settings (V_{SLPE}) after long line breaks or during reprogramming of V_{SLPE}.

It should be noted that the AC impedance into pin LN is reduced considerably when DST = 1.

Power control

INTERNAL RESET PCA1070

The PCA1070 has an internal reset circuit that monitors the supply voltage V_{DD}. If V_{DD} is below the threshold level (1.2 V) then the circuit is in reset-mode. In this mode the current consumption is low and the internal reset is active and writes the default values into all registers. The status bit PRES will be set to logic 1. The microcontroller can read this bit via the I^2C-bus interface; once read it will be set to logic 0 again.

When V_{DD} passes the threshold (increasing V_{DD}), the circuit becomes partly active and the internal ring/speech detector will be activated (see Section "Start-up and switch-off behaviour").

RESET OUTPUT FOR MICROCONTROLLER

The voltage at pin VMC (microcontroller supply voltage) is monitored by a reset circuit. If V_{VMC} is below the threshold level the output RMC is set to logic 1. This threshold level is 2 V in the normal operating and power-down mode and 2.1 V in the standby mode (see Fig.4).

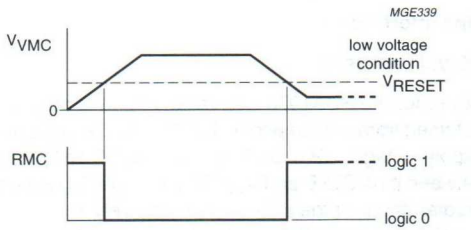


Fig.4 VMC timing diagram.

POWER-DOWN/STANDBY MODES

The circuit can be set in power-down or standby mode. These modes are intended for use with pulse dialling during long line breaks and applications with memory retention.

With control bits PDx = 01, the circuit is in the power-down mode; the typical current consumption at pin V_{DD} is reduced from I_{DD} = 2.3 mA to 30 µA; the typical current consumption at pin VMC is 4 µA. When PDx = 11 the circuit is in the standby mode and I_{DD} and I_{VMC} are reduced to 2 µA. In both conditions (power-down and standby) the voltage stabilizer will be disabled.

START-UP AND SWITCH-OFF BEHAVIOUR

This description refers to the basic application where V_{DD} and VMC are connected together and one supply capacitor is used (see Fig.8).

Speech condition

After hook-off, line current will be applied to the line input LN and the supply capacitor connected to V_{DD} and VMC will be charged.

The internal reset signal will change from logic 1 to logic 0 when V_{DD} passes the threshold level (1.2 V) and the circuit becomes partly active [the line interface part is kept in power-down mode, so that all of the line current is available to charge the supply capacitor(s)];
The PCA1070 can receive data via the I^2C-bus (standard I^2C specifications are fulfilled for $V_{DD} \geq 2.5$ V; relaxed performance for $V_{DD} = 1.8$ to 2.5 V).

When V_{VMC} passes the microcontroller reset level of 2 V (2.1 V in standby mode) the output RMC changes from logic 1 to logic 0 and the circuit is switched to the normal operating mode.

After hook-on V_{VMC} decreases and the output RMC will change from logic 0 to logic 1 when V_{VMC} passes the threshold level, however the PCA1070 will stay in the normal operating mode until the internal reset at 1.2 V takes place.

By decreasing V_{DD} the internal reset signal will change from logic 0 to logic 1 when V_{DD} passes 1.2 V and the circuit will go into the reset mode (line interface part in power-down and all programmable parameters reset to default values).

Ringer condition

In this condition the supply capacitor connected to V_{DD} and VMC is charged by the rectified ringer signal; no line current is applied to pin LN.

V_{DD} and V_{VMC} are increasing and when V_{DD} passes the internal reset threshold level (1.2 V), the internal ring/speech-detector will be activated and the circuit will switch to the standby condition ($I_{DD} < 5$ µA; $I_{VMC} < 5$ µA) before the voltage at VMC reaches the threshold level for microcontroller reset. When V_{VMC} passes this threshold level (2.1 V) output RMC changes from logic 1 to logic 0 and the circuit will stay in the standby mode until line current is applied to pin LN. By setting the 'Reset Ring' control bit (RRG) to logic 1 via the I^2C-bus interface, the ring/speech detector will be disabled.

DIAL PULSE INPUT (DPI)

The DPI bit controls output DOC (open-drain) that drives the gate of an external MOS interrupter transistor. DPI is controlled via the I^2C-bus interface.

If DPI is set to logic 1, pin DOC will be pulled down to switch-off the MOSFET to generate a line break. If DPI = 0 pin DOC is high-ohmic and the interrupter transistor will conduct the line current.

Sending channel

The PCA1070 has symmetrical microphone inputs and accepts input signals of maximum 70 mV (peak) for THD = 2% ($V_{DD} \geq 2.5$ V). Its input impedance is 100 kΩ and its gain is default 41 dB. Dynamic, magnetic, piezoelectric and electret (with built-in FET source follower) microphones can be used. Some possible microphone arrangements are shown in Fig.5.

The gain of the sending channel can be programmed between 30 dB and 51 dB in 1 dB steps using bit code GMAx (6 bits). The gain of the microphone preamplifier is 20 dB (with dynamic limiter not active) and GMAx sets the gain of the 'sending prog-amp' (allowed range G_{ma} = 4 to 25 dB). The gain of the line interface is 6 dB.

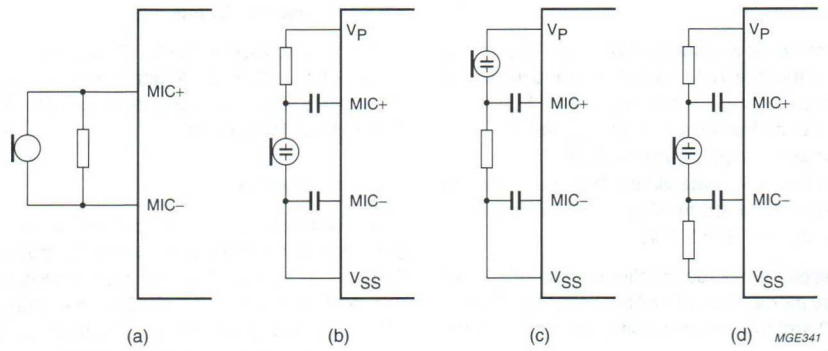
Thus the total gain of the sending channel (G_M) is as follows:

$G_M = 20 + G_{ma} + 6$ (dB)

Default: $G_M = 20 + 15 + 6 = 41$ dB

Where G_{ma} = 'gain sending prog-amp'.

Programming the gain of the 'sending prog-amp' is given in Table 13.



(a) Dynamic or piezo.
(b) Low impedance electret with built-in pre-amplifier.
(c) High impedance electret with built-in pre-amplifier.
(d) Symmetrical connection of electret.

Fig.5 Microphone arrangements.

Dynamic limiter

To prevent distortion of the transmitted speech signal, the gain of the microphone amplifier is reduced rapidly when signal peaks on the line exceed an internally determined threshold level. The time in which the gain is reduced, the attack time, is very short. The circuit stays in this gain-reduced condition until the peaks of the sending signal remain below the threshold level. The sending gain then returns to normal after a time also determined on the chip, the release time. The threshold level of the AC peak-to-peak line voltage on pin LN is default at 3.5 V (p-p). A level of 2.6 V (p-p) can be programmed by setting bit code DLT to logic 1.

The internal threshold level is lowered automatically if the DC voltage setting of the circuit (V_{SLPE}) is not high enough to reach the programmed level. Also when the DC current in the transmit output stage is insufficient to drive the line load, the internal threshold level is lowered automatically.

Dynamic limiting considerably improves sidetone performance in over-drive conditions (less distortion and limited sidetone level).

DTMF channel

The PCA1070 has an asymmetrical DTMF input. Its input impedance is 200 kΩ // 45 pF and its gain is default at 21 dB. DTMF signals can be sent to the line by setting control bit 'Sending Mute' (SM) to logic 1 (default SM = 0); by setting 'Receiving Mute' (RM) also to logic 1 (default RM = 0), the dialling tones are also sent to the receiving output to generate a confidence tone in the earpiece.

The gain between the DTMF input and the line LN can be programmed between 1 dB and 21 dB in 1 dB steps using bit code GMAx (6 bits). The confidence tone gain (between DTMF input and earpiece outputs QR) can be programmed between –40 dB and –19 dB (symmetrical drive of earpiece) using bit code GRAx (6 bits). GMAx sets the gain of the 'sending prog-amp' (recommended range in DTMF mode for G_{ma} = –5 to 15 dB) and GRAx sets the gain of the 'rec prog-amp' (allowed range G_{ra} = –25 to 0 dB).

The total gain of the DTMF channel between the DTMF input and the line LN is as follows:

$G_{DTMF} = G_{ma} + 6$ (dB)

Default $G_{DTMF} = 15 + 6 = 21$ dB

The confidence tone gain (DTMF to QR outputs) is:

With symmetrical drive of earpiece $G_{CTs} = G_{ra} - 19$ (dB)

Default $G_{CTss} = -6 - 19 = -25$ dB.

At low gain settings ($G_{ra} < -10$ dB), the confidence tone gain will be slightly higher than the calculated value. This is caused by a residual signal.

Programming the gain of the 'sending prog-amp' and the 'rec prog-amp' is given in Table 13.

Receiving channel

The gain of the receiving channel is defined between the line connection LN and the earpiece outputs QR+ and QR–. Its voltage gain is default –6 dB (differential drive). The LN terminal accepts receiving signals up to 1 V (RMS) for THD = 2%. The outputs may be used to connect dynamic, magnetic or piezoelectric earpieces with single-ended or differential drive. The load select bit RFC is set default to logic 1 to guarantee stable operation in case of a capacitive load (piezoelectric earpiece). With a resistive load (dynamic capsule) RFC should be set to logic 0 via the I²C-bus interface to obtain optimum performance with respect to distortion and bandwidth.

Two levels for hearing protection can be selected via the I²C-bus interface with control bit HPL.

The earpiece arrangements are illustrated in Fig.6.

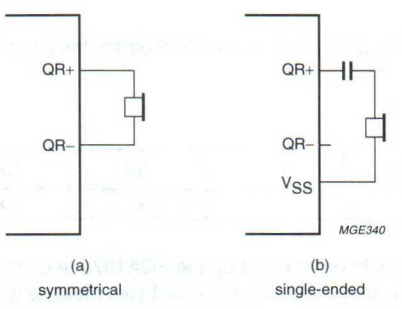


Fig.6 Earpiece arrangements.

The gain of the receiving channel can be programmed between –19 dB and +11 dB (symmetrical drive) in 1 dB steps using bit code GRAx (6 bits).

GRAx sets the gain of the 'rec prog-amp' (allowed range $G_{ra} = -19$ dB to +11 dB; default $G_{ra} = -6$ dB).

The total gain of the receiving channel is as follows:

Symmetrical drive $G_{RS} = G_{ra}$ (dB)

Default $G_{RS} = -6$ dB.

Asymmetrical or single-ended drive $G_{RA} = G_{RS} - 6$ (dB)

Default $G_{ra} = -6 - 6$ (dB) = –12 dB.

Programming the gain G_{ra} of the 'rec prog-amp' is given in Table 13.

Sidetone balance

The PCA1070 has an on-chip anti-sidetone circuit. An internal balance impedance Z_{oss} can be programmed via the I²C-bus interface to match the external line impedance Z_{line} to give optimum sidetone suppression. $Z_{oss} = R_{sa} + (R_{sb} // C_s)$.

Programming the sidetone balance impedance is given in Tables 14, 15 and 16.

Line current control

The DC line current can be read via the I²C-bus interface. This information can be used for the adaptation of transmission parameters (for example line loss compensation, sidetone balance and DC characteristic).

The bit code LCx as a function of line current is given in Table 17.

I²C-BUS PROGRAMMING

Table 1 Programmable parameters

The following parameters (see Fig.1) can be programmed by means of a bit code via the I²C-bus:

SYMBOL	PARAMETER	BLOCK	BITS	DESCRIPTION
VDCx	V_{SLPE}	line interface	3	DC voltage SLPE-V_{SS}
ZSAx	set impedance	line interface	3	R_a of set impedance
ZSBx		line interface	3	R_b of set impedance
ZSPx		line interface	4	f_p (pole frequency) of set impedance
DST	DST	line interface	1	DC Start Time
PDx	PD	power control	2	Power-Down
DPI	DPI	power control	1	Dial Pulse Input
RRG	RRG	power control	1	Reset RinG detector
HPL	maximum receiving level	BTL receiving output	1	Hearing Protection Level
RFC	load select	BTL receiving output	1	Resistive/Capacitive load
ZOSAx	sidetone impedance	anti-sidetone	4	R_{sa} of sidetone impedance
ZOSBx		anti-sidetone	4	R_{sb} of sidetone impedance
ZOSPx		anti-sidetone	4	C_s of sidetone impedance
RM	receiving mute	receiving mute	1	Receiving Mute
GRAx	gain G_{ra}	receiving prog-amp	6	Gain receiving prog-amp
GMAx	gain G_{ma}	sending prog-amp	6	Gain sending prog-amp
SM	sending mute	sending mute	1	Sending Mute
DLT	threshold	dynamic limiter	1	Dynamic Limiter Threshold

Table 2 Readable parameters

The following parameters (see also Fig.1) can be read as a bit code via the I²C-bus:

SYMBOL	PARAMETER	BLOCK	BITS	DESCRIPTION
PRES	PRES	power control	1	PCA1070 Reset
LCx	line current	gain control	5	Line Current

I²C interface

The I²C-bus interface (see *"The I²C-bus and how to use it"* 12NC: 9398 393 40011) is used to program the transmission parameters and control functions.

Table 3 Device address

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
0	1	0	0	0	1	0	X

All functions can be accessed by writing an 8-bit word to the PCA1070. In order to set up the PCA1070, a control message consisting of the device address, a R/$\overline{W}$ bit, a subaddress byte and one or more data bytes must be written to the PCA1070. If more than one data byte follows the subaddress, these bytes are stored in the successive registers by the automatic increment feature.

Table 4 The control word format for the slave receiver

	DEVICE ADDRESS								SUB ADDRESS									DATA/CONTROL BYTE									
S	0	1	0	0	0	1	0	0[1]	A	I7	I6	I5	I4	I3	I2	I1	I0	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P

Note

1. This bit is R/$\overline{W}$.

Table 5 Bit arrangement of each data byte used in the control word: PCA1070 receive (see note 1)

FUNCTION	SUB ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
DC voltage	H00		VDC2	VDC1	VDC0				DST
Sidetone and set impedance	H01	ZOSB3	ZOSB2	ZOSB1	ZOSB0	ZOSA3	ZOSA2	ZOSA1	ZOSA0
	H02	ZOSP3	ZOSP2	ZOSP1	ZOSP0		ZSA2	ZSA1	ZSA0
	H03		ZSB2	ZSB1	ZSB0	ZSP3	ZSP2	ZSP1	ZSP0
Sending channel	H04	DLT		GMA5	GMA4	GMA3	GMA2	GMA1	GMA0
Receiving channel	H05	RFC	HPL	GRA5	GRA4	GRA3	GRA2	GRA1	GRA0
Control	H06	PD1	PD0		RRG	RM	SM		DPI

Note

1. The bits that are not indicated must be set to logic 0.

Table 6 The control word format for the slave transmitter

	DEVICE ADDRESS									DATA/STATUS BYTE										
S	0	1	0	0	0	1	0	1[1]	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P

Note

1. Change in direction of R/$\overline{W}$ bit.

Table 7 PCA1070 send

FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
PCA1070 status	PRES[1]	–	–	LC4[2]	LC3[2]	LC2[2]	LC1[2]	LC0[2]

Notes

1. Indicates if PCA1070 has received internal reset; PRES will be set to logic 1 with internal reset and is set to logic 0 after reading the register via the I^{2}C-bus.
2. Information about value of line current.

WRITE AND READ TABLES

DC voltages

Table 8 DC voltage at pin SLPE

VDC2	VDC1	VDC0	V_{SLPE} (V)	REMARK
0	0	0	3.1	
0	0	1	3.5	
0	1	0	3.9	
0	1	1	4.3	
1	**0**	**0**	**4.7**	**default**
1	0	1	5.1	
1	1	0	5.5	
1	1	1	5.9	

Set impedance

Programming the impedance in the audio frequency range seen at pin LN: $R_a + (R_b // C)$

Table 9 Programming R_a

ZSA2	ZSA1	ZSA0	R_a (Ω)	REMARK
0	0	0	0	
0	0	1	100	
0	**1**	**0**	**200**	**default**
0	1	1	300	
1	0	0	400	
1	0	1	500	note 1
1	1	X	600	notes 1 and 2

Notes

1. For Z_{set} combinations where $R_a = 0$ only $R_b = 600\ \Omega$ is allowed. If $R_a \geq 500\ \Omega$ it is obligatory that $R_b = 0$. This is to safeguard stable operation of the line interface under all practical conditions. If Z_{ref} requires $R_a = 0$ and $R_b \neq 600\ \Omega$ use $R_a = 100\ \Omega$ instead and reduce the original R_b by 100 Ω.
2. X = don't care.

Table 10 Programming R_b

ZSB2	ZSB1	ZSB0	R_b (Ω)	REMARK
0	0	0	0	note 1
0	0	1	600	
0	1	0	700	
0	**1**	**1**	**800**	**default**
1	X	0	900	note 2
1	X	1	1000	note 2

Notes

1. For Z_{set} combinations where $R_a = 0$ only $R_b = 600\ \Omega$ is allowed. If $R_a \geq 500\ \Omega$ it is obligatory that $R_b = 0$. This is to safeguard stable operation of the line interface under all practical conditions. If Z_{ref} requires $R_a = 0$ and $R_b \neq 600\ \Omega$ use $R_a = 100\ \Omega$ instead and reduce the original R_b by 100 Ω.
2. X = don't care.

Table 11 Programming pole frequency:

ZSP3	ZSP2	ZSP1	ZSP0	f_p (Hz)	CORRESPONDING VALUE OF C (nF)[1]					REMARK
					R_b (600 Ω)	R_b (700 Ω)	R_b (800 Ω)	R_b (900 Ω)	R_b (1000 Ω)	
0	0	0	0	828	320	275	240	214	192	
0	0	0	1	1095	242	207	182	161	145	
0	0	1	0	1448	183	157	137	122	110	
0	**0**	**1**	**1**	**1915**	**139**	**119**	**104**	**92**	**83**	**default**
0	1	0	0	2533	105	90	79	70	63	
0	1	0	1	3350	79	68	59	53	48	
0	1	1	0	4430	60	51	45	40	36	
0	1	1	1	5859	45	39	34	30	27	
1	X	X	X	12000	22	19	17	15	13	note 2

Notes

1. $C = \dfrac{1}{2\pi \times R_b \times f_p}$
2. X = don't care.

Reset functions

Monitoring of internal reset PCA1070.

Table 12 Status bit PRES

PRES	DESCRIPTION
1	internal reset has occurred; default values in all registers
0	register has been read via the I^2C-bus interface

Programmable amplifier (prog-amp)

An identical programmable amplifier called 'prog-amp' is used both in the sending and receiving channel. The bit codes GMAx and GRAx are given in Table 13. The permitted adjustment range differs for the two amplifiers and is also different for DTMF and speech mode. This is indicated in the corresponding sections.

Table 13 Bit code prog-amp

GAIN (dB)	GMA5 GRA5	GMA4 GRA4	GMA3 GRA3	GMA2 GRA2	GMA1 GRA1	GMA0 GRA0
−25	1	1	1	0	0	1
−24	1	1	1	0	0	0
−23	1	1	0	1	1	1
−22	1	1	0	1	1	0
−21	1	1	0	1	0	1
−20	1	1	0	1	0	0
−19	1	1	0	0	1	1
−18	1	1	0	0	1	0
−17	1	1	0	0	0	1
−16	1	1	0	0	0	0
−15	1	0	1	1	1	1
−14	1	0	1	1	1	0
−13	1	0	1	1	0	1
−12	1	0	1	1	0	0
−11	1	0	1	0	1	1
−10	1	0	1	0	1	0
−9	1	0	1	0	0	1
−8	1	0	1	0	0	0
−7	1	0	0	1	1	1
−6[1]	**1**	**0**	**0**	**1**	**1**	**0**
−5	1	0	0	1	0	1
−4	1	0	0	1	0	0
−3	1	0	0	0	1	1
−2	1	0	0	0	1	0
−1	1	0	0	0	0	1
−0	1	0	0	0	0	0

GAIN (dB)	GMA5 GRA5	GMA4 GRA4	GMA3 GRA3	GMA2 GRA2	GMA1 GRA1	GMA0 GRA0
+0	0	0	0	0	0	0
+1	0	0	0	0	0	1
+2	0	0	0	0	1	0
+3	0	0	0	0	1	1
+4	0	0	0	1	0	0
+5	0	0	0	1	0	1
+6	0	0	0	1	1	0
+7	0	0	0	1	1	1
+8	0	0	1	0	0	0
+9	0	0	1	0	0	1
+10	0	0	1	0	1	0
+11	0	0	1	0	1	1
+12	0	0	1	1	0	0
+13	0	0	1	1	0	1
+14	0	0	1	1	1	0
+15[2]	**0**	**0**	**1**	**1**	**1**	**1**
+16	0	1	0	0	0	0
+17	0	1	0	0	0	1
+18	0	1	0	0	1	0
+19	0	1	0	0	1	1
+20	0	1	0	1	0	0
+21	0	1	0	1	0	1
+22	0	1	0	1	1	0
+23	0	1	0	1	1	1
+24	0	1	1	0	0	0
+25	0	1	1	0	0	1

Notes

1. Default value 'rec prog-amp' GRAx.
2. Default value 'sending prog-amp' GMAx.

Sidetone balance impedance

Internal balance impedance Z_{oss} to match the external line impedance Z_{line} to give optimum sidetone suppression. $Z_{oss} = R_{sa} + (R_{sb} // C_s)$.

The optimum setting of R_{sa} depends on the value of the set impedance. To safeguard stable operation of the anti-sidetone circuit under all practical conditions, the following condition must be fulfilled: $R_{sa} \geq 0.5R_a$.

Table 14 Programming R_{sa}

ZOSA3	ZOSA2	ZOSA1	ZOSA0	R_{sa} (Ω)
0	0	0	0	134
0	0	0	1	153
0	0	1	0	193
0	0	1	1	221
0	1	0	0	246
0	1	0	1	277
0	1	1	0	295
0	1	1	1	341
1	0	0	0	369
1	0	0	1	443
1	**0**	**1**	**0**	**492**(1)
1	0	1	1	–
1	1	0	0	–
1	1	0	1	–
1	1	1	0	–
1	1	1	1	–

Note

1. Default value.

Table 15 Programming R_{sb}

ZOSB				R_{sb} (Ω)
MSB			LSB	
0	0	0	0	465
0	0	0	1	637
0	0	1	0	710
0	0	1	1	803
0	1	0	0	893
0	1	0	1	1003
0	**1**	**1**	**0**	**1259**(1)
0	1	1	1	1410
1	0	0	0	1572
1	0	0	1	1773
1	0	1	0	1978
1	0	1	1	2216
1	1	0	0	–
1	1	0	1	–
1	1	1	0	–
1	1	1	1	–

Note

1. Default value.

Table 16 Programming C_s

ZOSP				C_s (nf)
MSP			LSP	
0	0	0	0	5
0	0	0	1	55
0	0	1	0	58
0	0	1	1	69
0	1	0	0	76
0	1	0	1	85
0	1	1	0	96
0	1	1	1	105
1	0	0	0	121
1	**0**	**0**	**1**	**134**(1)
1	0	1	0	145
1	0	1	1	166
1	1	0	0	186
1	1	0	1	207
1	1	1	0	232
1	1	1	1	259

Note

1. Default value.

Line current control

Table 17 Bit code LCx and DC line current

LC4	LC3	LC2	LC1	LC0	I_{line} (typ.) (mA)
0	0	0	0	0	<12.5
0	0	0	0	1	15.0
0	0	0	1	0	17.5
0	0	0	1	1	20.0
0	0	1	0	0	22.5
0	0	1	0	1	25.0
0	0	1	1	0	27.5
0	0	1	1	1	30.0
0	1	0	0	0	32.5
0	1	0	0	1	35.0
0	1	0	1	0	37.5
0	1	0	1	1	40.0
0	1	1	0	0	42.5
0	1	1	0	1	45.0
0	1	1	1	0	47.5
0	1	1	1	1	50.0
1	0	0	0	0	52.5
1	0	0	0	1	55.0
1	0	0	1	0	58.0
1	0	0	1	1	61.0
1	0	1	0	0	64.0
1	0	1	0	1	66.5
1	0	1	1	0	69.0
1	0	1	1	1	71.5
1	1	0	0	0	74.0
1	1	0	0	1	77.5
1	1	0	1	0	80.0
1	1	0	1	1	82.5
1	1	1	0	0	85.0
1	1	1	0	1	88.0
1	1	1	1	0	91.0
1	1	1	1	1	>94.0

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{LN}	positive line voltage at pin LN	−0.8	+12	V
V_i	input voltage on pins SLPE, DOC, REG, TX and LSI	−0.8	+12	V
V_{DD}	supply voltage	−0.8	+7.0	V
V_n	voltage on all other pins	−0.8	+7.0	V
I_i	input current	−10	+10	mA
P_{tot}	total power dissipation	−	250	mW
T_{stg}	storage temperature	−40	+125	°C
T_{amb}	operating ambient temperature	−10	+60	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	DIP24	54	K/W
	SO24	74	K/W

TEST CONDITIONS AND PARAMETER SETTINGS FOR THE CHARACTERISTICS

Table 18 Test conditions

SYMBOL	VALUE	UNIT
I_{line}	20	mA
V_{SS}	0	V
f	1000	Hz
I_p	0	A
I_{VP}	0	A
f_{clk}	3.597545	MHz
T_{amb}	25	°C
Z_{line}	220 Ω + 820 Ω // 115 nF	
R_m	150	Ω
R_t	150	Ω

Table 19 Test settings and control bits. All values, except RFC, are default. Programmable via the I²C-bus; bit codes are given in Chapter "I²C-bus programming".

SYMBOL	VALUE
VDCx	100
ZSAx	010
ZSBx	011
ZSPx	0011
GMAx	001111
GRAx	100110
ZOSAx	1010
ZOSBx	0110
ZOSPx	1001
DST	0
DLT	0
RFC	0
HPL	0
PDx	00
RRG	0
RM	0
SM	0
DPI	0

CHARACTERISTICS

All parameters are measured in the test circuit of Fig.7 under the conditions specified in Tables 18 and 19; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC line interface: LN, TX, SLPE and REG						
I_{line}	line current operating range		17	–	140	mA
		reduced sending level	12	–	17	mA
V_{SLPE}	DC voltage at SLPE	with or without clock	4.3	4.7	5.1	V
$V_{SLPE(min)}$	minimum selectable value	VDCx = 000	2.8	3.1	3.4	V
$V_{SLPE(max)}$	maximum selectable value	VDCx = 111	5.4	5.9	6.4	V
$V_{SLPE(step)}$	step resolution		–	0.4	–	V
V_{SLPE}	DC voltage at SLPE	with or without clock; fast start-up; DST = 1	–	4.7	–	V
$V_{SLPE(min)}$	minimum selectable value	fast start-up; DST = 1; VDCx = 000	–	3.1	–	V
$V_{SLPE(max)}$	maximum selectable value	fast start-up; DST = 1; VDCx = 111	–	5.9	–	V
$V_{SLPE(step)}$	step resolution	fast start-up; DST = 1	–	0.4	–	V
ΔV_{SLPE}	variation with temperature	at T_{amb} = −10 °C to +60 °C with respect to 25 °C	–	±20	–	mV
V_{LN}	DC line voltage at LN	with or without clock	4.6	5.0	5.4	V
		I_{line} = 12 mA		4.83		V
		I_{line} = 120 mA	6.5	7.0	7.5	V
V_{LN}	DC line voltage at LN at low line current	with or without clock; I_{line} = 0.25 mA	–	1	–	V
		I_{line} = 2 mA	–	1.9	–	V
		I_{line} = 4 mA	–	3.4	–	V
		I_{line} = 7 mA	–	4.73	5.2	V
t_{DC}	DC start-up time	C_{VDD} = 470 µF; no clock; note 1	–	145	–	ms
TX: DRIVE OUTPUT FOR EXTERNAL PNP						
V_{TX}	output voltage at TX	external PNP disconnected; V_{SLPE} = 2 V; V_{REG} = 1.5 V; $V_{DD} = V_{VMC}$ = 2.5 V; I_{TX} = 0 mA	–	1.45	–	V
		V_{SLPE} = 3 V; V_{REG} = 2.5 V; $V_{DD} = V_{VMC}$ = 2.5 V; I_{TX} = 1.6 mA	–	2.2	–	V
t_{SW}	switching time DC voltage at SLPE	V_{SLPE} steps from 3.1 V to 5.9 V; note 2	–	65	–	ms
		V_{SLPE} steps from 5.9 V to 3.1 V; note 2	–	65	–	ms
		fast start-up; DST = 1; V_{SLPE} steps from 3.1 V to 5.9 V; note 2	–	0.5	–	ms
		fast start-up; DST = 1; V_{SLPE} steps from 5.9 V to 3.1 V; note 2	–	1	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies: V_{DD}, VMC, V_P and SLPE						
V_{DD}	operating supply voltage	note 3	2.5	–	6	V
		relaxed performance; note 4	1.8	–	2.5	V
V_{DD}; SUPPLY PIN						
I_{DD}	internal current consumption	V_{DD} = 2.5 V	–	2.3	–	mA
		power-down; PDx = 01; SCL = 1; SDA = 1	–	30	100	µA
		standby; PDx = 11; SCL = 1; SDA = 1	–	2	5	µA
V_{DD}: PERIPHERAL SUPPLY						
I_p	current available for peripheral circuitry	V_{DD} = 2.9 V; RM = 1; SM = 1	–	4.9	–	mA
		V_{DD} = 2.5 V; RM = 1; SM = 1	–	6.5	–	mA
VMC: SENSE INPUT MICROCONTROLLER SUPPLY VOLTAGE						
I_{VMC}	input current	V_{VMC} = 2.5 V	–	4	10	µA
		power-down; PDx = 01; V_{VMC} = 2.5 V; SCL = 1; SDA = 1	–	4	10	µA
		standby; PDx = 11; V_{VMC} = 2.5 V; SCL = 1; SDA = 1	–	2	5	µA
V_P: SUPPLY OUTPUT FOR ELECTRET MICROPHONE						
V_P	output voltage	I_{VP} = 500 µA	1.6	1.9	–	V
Z_{VP}	output impedance	f = 300 Hz	–	40	–	Ω
PSR_{VP}	power supply rejection	f = 300 Hz; note 5	–	65	–	dB
Reset functions: V_{DD}, VMC and RMC						
INTERNAL RESET						
$V_{DD(sw)}$	switching level of V_{DD} below which internal reset is active	T_{amb} = −10 to +60 °C; note 6	1.0	1.2	1.4	V
RMC: RESET OUTPUT FOR MICROCONTROLLER						
$V_{VMC(sw)}$	voltage level at pin VMC where RMC changes state	note 7	1.8	2.0	2.2	V
		power-down; PDx = 01; note 7	1.8	2.0	2.2	V
		standby; PDx = 11; note 7	1.8	2.1	2.4	V
$\Delta V_{VMC}/\Delta T$	voltage variation with ambient temperature	T_{amb} = −10 to +60 °C	–	0	–	mV/°C
		power-down; PDx = 01; T_{amb} = −10 to +60 °C	–	0	–	mV/°C
		standby; PDx = 11; T_{amb} = −10 to +60 °C	–	+3	–	mV/°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sending channel: MIC+, MIC–, DTMF, OMIC, LN, SCR, REG and LSI						
MIC+ AND MIC–: MICROPHONE INPUTS						
Z_{MIC}	input impedance	differential	60	100	–	kΩ
		single-ended	30	50	–	kΩ
$CMRR_{MIC}$	common mode rejection ratio	note 8	–	72	–	dB
$V_{MIC(peak)}$	allowed input signal voltage level (peak value)		–	–	70	mV
G_M	gain MIC+/MIC– to LN		39.5	41	42.5	dB
$G_{M(min)}$	minimum selectable gain	GMAx = 000100	28.5	30	31.5	dB
$G_{M(max)}$	maximum selectable gain	GMAx = 011001	49.5	51	52.5	dB
$G_{M(step)}$	step resolution		–	1	–	dB
ΔG_M	gain variation with frequency	at f = 300 Hz and 3400 Hz with respect to 1 kHz; note 9	–	–	+0.3/–0.7	dB
	gain variation with ambient temperature	at T_{amb} = –10 to +60 °C with respect to 25 °C	–	±0.2	–	dB
	gain variation with line current	at I_{line} = 100 mA with respect to 20 mA; note 9	–	0	±0.5	dB
t_{ACM}	AC start-up time	C_{VDD} = 470 µF; note 10	–	150	–	ms
Sending mute/privacy switch						
ΔG_M	reduction of G_M	SM = 1	–	100	–	dB
DTMF: DUAL TONE MULTI-FREQUENCY INPUT						
R_{DTMF}	parallel input resistance	SM = 1	100	200	–	kΩ
C_{DTMF}	parallel input capacitance	SM = 1	–	45	–	pF
G_{DTMF}	gain from DTMF to LN	SM = 1	20	21	22	dB
$G_{DTMF(min)}$	minimum selectable gain	SM = 1; GMAx = 100101	0	1	2	dB
$G_{DTMF(max)}$	maximum selectable gain	SM = 1; GMAx = 001111	20	21	22	dB
$G_{DTMF(step)}$	step resolution	SM = 1	–	1	–	dB
ΔG_{DTMF}	gain variation with frequency	SM = 1; at f = 300 Hz and 3400 Hz with respect to 1 kHz; note 9	–	–	+0.3/–0.7	dB
	gain variation with ambient temperature	SM = 1; at T_{amb} = –10 to +60 °C with respect to 25 °C	–	±0.2	–	dB
	gain variation with line current	SM = 1; at I_{line} = 100 mA with respect to 20 mA; note 9	–	0	±0.5	dB
Confidence tone						
G_{CTS}	gain from DTMF to QR+/QR–;	RM = 1; SM = 1; notes 11 and 12	–	–25	–	dB
$G_{CTS(min)}$	minimum selectable gain	RM = 1; SM = 1; GRAx = 111001	–	–40	–	dB
$G_{CTS(max)}$	maximum selectable gain	RM = 1; SM = 1; GRAx = 100000	–	–19	–	dB
$G_{CTS(step)}$	step resolution	RM = 1; SM = 1	–	0.5 to 1	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OMIC: MICROPHONE PREAMPLIFIER OUTPUT						
Z_{OMIC}	output impedance		–	400	–	Ω
G_{OMIC}	gain from MIC+/MIC– to OMIC	dynamic limiter not active; note 13	–	20	–	dB
LN: SENDING CHANNEL OUTPUT; notes 14 and 15						
BRL	balance return loss Z_{LN} with Z_{ref} = 220 Ω + (820 Ω // 115 nF)	Z_{line} = ∞ Ω; f = 300 Hz	20	37	–	dB
		Z_{line} = ∞ Ω; f = 1 kHz	20	35	–	dB
		Z_{line} = ∞ Ω; f = 3.4 kHz	20	25	–	dB
Selectable values for $Z_{set} = R_a + (R_b // C)$ with $C = 1/(2\pi \times R_b \times f_p)$; note 16						
R_a	non-shunted resistance of Z_{set}		–	200	–	Ω
$R_{a(min)}$	minimum selectable value for R_a	ZSAx = 001; note 17	–	0	–	Ω
$R_{a(max)}$	maximum selectable value for R_a	ZSAx = 11x	–	600	–	Ω
$R_{a(step)}$	step resolution for R_a		–	100	–	Ω
R_b	shunted resistance of Z_{set}		–	800	–	Ω
$R_{b(min)}$	minimum selectable value for R_b	ZSBx = 001; notes 17 and 18	–	600	–	Ω
$R_{b(max)}$	maximum selectable value for R_b	ZSBx = 1x1	–	1000	–	Ω
$R_{b(step)}$	step resolution for R_b		–	100	–	Ω
f_p	pole frequency determining shunt capacitance C		–	1915	–	Hz
$f_{p(min)}$	minimum selectable f_p	ZSPx = 0000	–	828	–	Hz
$f_{p(max)}$	maximum selectable f_p	ZSPx = 0111; note 19	–	5859	–	Hz
n	multiplication factor for f_p	$f_p(x + 1) = n \times [f_p(x)]$	–	1.322	–	
$V_{LN(noise)}$	noise output voltage	psophometrically weighted (O41 curve)	–	–76	–	dBmp
Dynamic limiter						
$V_{LN(p-p)}$	threshold of dynamic limiter (peak-to-peak)		3.1	3.5	3.9	V
		DLT = 1	2.2	2.6	3.0	V
		low voltage condition; V_{SLPE} = 3.1 V	–	2.4	–	V
		low current condition; I_{line} = 9 mA	–	2.6	–	V
THD	total harmonic distortion	V_i = 12 mV (RMS) + 10 dB	–	2.5	5.0	%
Dynamic behaviour of limiter; note 20						
t_{att}	attack time	V_i steps from 12 to 38 mV (RMS)	–	1.5	–	ms
t_{rel}	release time	V_i steps from 38 to 12 mV (RMS)	–	90	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCR: PIN FOR SENDING CURRENT RESISTOR						
V_{SCR}	voltage at pin SCR		–	0.28	–	V
		reduced sending gain; G_M = 30 dB; GMAx = 000100	–	0.26	–	V
		I_{line} = 12 mA	–	0.22	–	V
		I_{line} = 7 mA	–	0.13	–	V
Receiving channel: LN, LSI, OREC, QR+ and QR–						
QR+, QR–: RECEIVING AMPLIFIER OUTPUTS						
Z_{QR+}, Z_{QR-}	output impedance	single-ended	–	4	–	Ω
G_{RS}	gain from LN to QR+/QR-	note 21	–7.5	-6	–4.5	dB
$G_{RS(min)}$	minimum selectable gain	GRAx = 110011	–20.5	–19	–17.5	dB
$G_{RS(max)}$	maximum selectable gain	GRAx = 001011	9.5	11.0	12.5	dB
$G_{RS(step)}$	gain step resolution		–	1	–	dB
ΔG_{RS}	gain variation with frequency	at f = 300 Hz and 3400 Hz with respect to 1 kHz; note 9	–	–	±0.5	dB
ΔG_{RS}	gain variation with temperature	at T_{amb} = –10 to +60 °C with respect to 25 °C	–	±0.2	–	dB
ΔG_{RS}	gain variation with line current	at I_{line} = 100 mA with respect to 20 mA; note 9	–	0	±0.5	dB
t_{ACR}	AC start-up time	C_{VDD} = 470 µF; note 10	–	140	–	ms
$v_{QR(p-p)}$	maximum output voltage swing (peak-to-peak)	V_{DD} = 5 V; GRAx = 001011; $R_t = \infty$ Ω; RFC = 1; V_{LN} = 2 V (RMS)	–	2.3	–	V
		HPL = 1; V_{DD} = 5 V; GRAx = 001011; $R_t = \infty$ Ω; RFC = 1; V_{LN} = 2 V (RMS)	–	5.9	–	V
$v_{QR(rms)}$	output voltage (RMS value); THD = 2%	HPL = 1; GRAx = 000011; note 22	0.45	–	–	V
		HPL = 1; R_t = 450 Ω; GRAx = 000011; note 22	0.84	–	–	V
		RFC = 1; C_t = 80 nF; f = 3.4 kHz; GRAx = 000011; note 22	0.9	–	–	V
		single-ended; HPL = 1; Z_t = 150 Ω + 100 µF at QR–; GRAx = 001001; note 22	0.45	–	–	V
$v_{QR(noise)}$	noise output voltage	psophometrically weighted (O41 curve)	–	–82	–	dBmp
$V_{QR(offset)}$	DC offset voltage between QR+/QR–		–	–	±100	mV
OREC: OUTPUT RECEIVE PREAMPLIFIER						
Z_{OREC}	output impedance		–	1000	–	Ω
G_{OREC}	gain from LN to OREC	note 13	–	–6	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Selectable values for $Z_{oss} = R_{sa}$ (R_{sb} // C_s); note 23						
R_{sa}	non-shunted resistance of Z_{oss}		–	492	–	Ω
$R_{sa(min)}$	minimum selectable value R_{sa}	ZOSAx = 0000	–	134	–	Ω
$R_{sa(max)}$	maximum selectable value for R_{sa}	ZOSAx = 1010; note 24	–	492	–	Ω
R_{sb}	shunted resistance of Z_{oss}		–	1259	–	Ω
$R_{sb(min)}$	minimum selectable value for R_{sb}	ZOSBx = 0000	–	465	–	Ω
$R_{sb(max)}$	maximum selectable value for R_{sb}	ZOSBx = 1011; note 24	–	2216	–	Ω
C_s	shunt capacitance of Z_{oss}		–	134	–	nF
$C_{s(min)}$	minimum selectable value for C_s	ZOSPx = 0001; note 25	–	55	–	nF
$C_{s(max)}$	maximum selectable value for C_s	ZOSPx = 1111; note 24	–	259	–	nF
Sidetone suppression; note 26						
G_{STS}	gain from MIC+/MIC– to QR+/QR–	Z_{line} = 492 Ω + (1259 Ω // 134 nF); f = 300 Hz	–	11	15	dB
		Z_{line} = 492 Ω + (1259 Ω // 134 nF); f = 1 kHz	–	5	10	dB
		Z_{line} = 492 Ω + (1259 Ω // 134 nF); f = 3.4 kHz	–	9	15	dB
Dial output connection: DOC (open-drain output)						
I_{DOC}	output sink current	V_{DOC} = 12 V	–	0	100	nA
		DPI = 1; V_{DOC} = 0.4 V; V_{DD} = 2.5 V	200	400	–	µA
Line current control: LN and SLPE						
$I_{line(min)}$	minimum value of DC line current that can be read as a bit code via the I²C-bus	LCx = 00001	–	15	–	mA
$I_{line(max)}$	maximum value of DC line current that can be read as a bit code via the I²C-bus	LCx = 11110	–	91	–	mA
$I_{line(step)}$	DC line current step resolution	note 27	–	≈2.5	–	mA
I²C-bus inputs/outputs: SDA and SCL						
	in accordance with standard	note 28	–	–	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock input: CLK						
$V_{CLK(p-p)}$	input signal voltage level (peak-to-peak value)		200	–	$V_{VMC} - V_{SS}$	mV
$\Delta f_{CLK}/f_{CLK}$	frequency tolerance	note 29	–	–	±0.5	%
R_{CLK}	input series resistance		–	800	–	kΩ
C_{CLK}	input series capacitance		–	4	–	pF

Notes

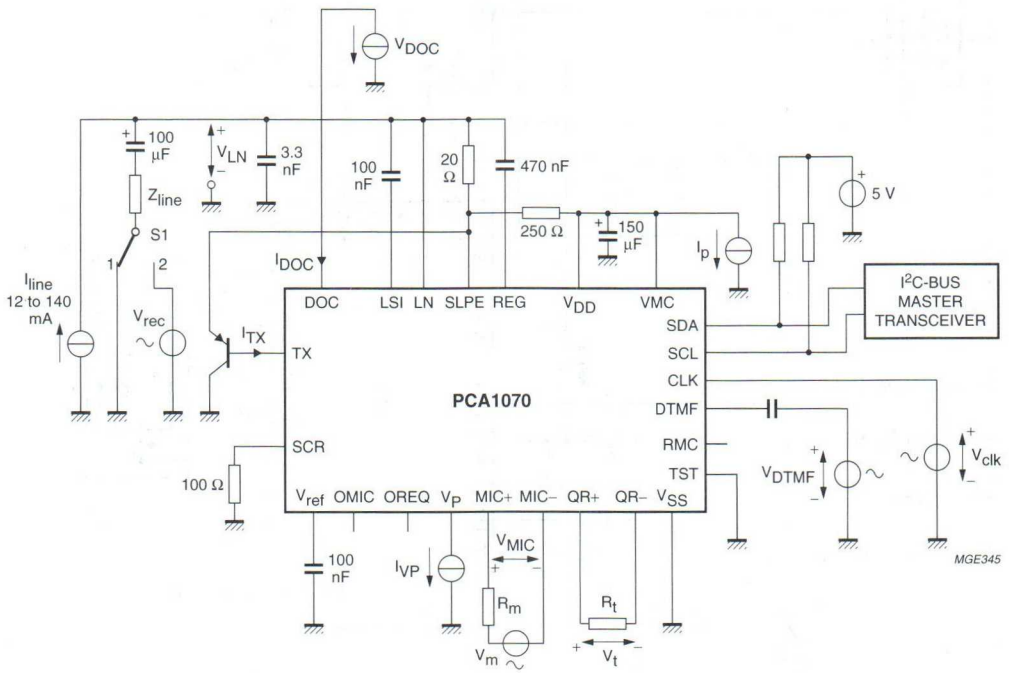
1. Time needed to reach at start-up the default DC voltage V_{SLPE} (±10% from its final value):
   a) Time depends strongly on the value of the capacitor(s) at V_{DD} and VMC; with a lower value of C_{VDD} the DC start-up time decreases.
   b) The start-up time can be reduced considerably by programming the bit code DST = 1 during the start-up procedure. In practice this is possible as soon as the microcontroller has become operational.
2. Time needed to reach the DC voltage V_{SLPE} within ±10% from its final value) after reprogramming VDCx.
3. The supply voltage V_{DD} is determined by the regulated DC voltage at pin SLPE and by the voltage drop between pin SLPE and V_{DD}; see Chapter "Functional description".
4. Relaxed performance means: parameters can deviate from their specified values.
5. Rejection between supply pin V_{DD} and V_P. Rejection between pin LN and V_P can be calculated by adding the attenuation of the first-order low-pass filter (R = 250 Ω, C = 150 μF) between SLPE and V_{DD}.
6. If V_{DD} is above this level, the default values have been loaded into the internal registers.
7. RMC changes from logic 1 to logic 0 when voltage on pin VMC is increasing; RMC changes from logic 0 to logic 1 when voltage on pin VMC is decreasing; see Fig.4.
8. Common mode signal is applied via 2 × 470 Ω external resistors connected to pins MIC+ and MIC–.
9. Not tested, guaranteed by design.
10. Time needed to reach default settings (±3 dB).
11. At low gain settings the confidence tone gain will be slightly higher than the specified value due to a residual signal.
12. G_{CTA}, the confidence tone gain for asymmetrical drive, equals G_{CTS} –6 (in dB).
13. To be left open-circuit in application.
14. The AC set impedance between pin LN and V_{SS} consists of $R_a + (R_b \,//\, C)$ in parallel with an artificial inductor L_{eq} and internal resistors R_p and R_{LSI} and internal capacitor C_p. See Chapter "Functional description".
15. Balance Return Loss indicates the deviation of an impedance with respect to a reference impedance. $BRL = 20 \log |(Z_{LN} + Z_{ref})/(Z_{LN} - Z_{ref})|$ where $Z_{LN} \approx R_a + (R_b \,//\, C)$ is the impedance seen into pin LN $Z_{ref} = R_{a(ref)} + (R_{b(ref)} \,//\, C_{ref})$ is the reference impedance.
16. Without clock the set impedance is automatically set to Z_{set} = 600 Ω (typical).
17. The combination $R_a = 0$ and $R_b = 0$ is not allowed (see Tables 9 and 10, note 1).
18. Value logic 0 can also be programmed.
19. Value f_p = 12 kHz can also be programmed.
20. Attack and release times are also valid under low current and voltage conditions.
21. G_{RA}, the receiving channel gain for asymmetrical drive equals G_{RS} –6 (in dB).
22. The maximum possible output swing depends on the DC conditions (the programmed voltage V_{SLPE} and the load on the supply pin V_{DD}) and on the gain setting of the receiving channel.

23. The internal balance impedance Z_{oss} to match the external load impedance at pin LN ($Z_{line} = Z_{oss}$) for optimum sidetone suppression; $Z_{oss} = R_{sa} + (R_{sb} // C_s)$; without clock the sidetone balance impedance is automatically set to $Z_{oss} = 600\ \Omega$ (typical).
24. Other values can be found in Tables 14, 15 and 16.
25. Value $C_s = 5$ nF can also be programmed.
26. Gain sending channel G_M = default (typical 41 dB); gain receiving channel G_{rec} = default (typical –6 dB); sidetone gain G_{STS} minimum sidetone suppression at f = 300 Hz and 3400 Hz is: $G_M + G_R - G_{st(max)} = 41 - 6 - 15 = 20$ dB. G_{STA}, the sidetone gain for asymmetrical drive equals G_{STS} –6 (in dB).
27. Indication only; exact values can be found in Table 16.
28. Standard I^2C-bus specifications are valid for $V_{DD} \geq 2.5$ V. Relaxed specifications for $V_{DD} = 1.8$ to 2.5 V.
29. Recommended accuracy of input frequency; a higher tolerance will cause parameters to deviate from their specified values; note that all parameters are specified with the reference input clock frequency $f_{clk} = 3.579545$ MHz.

TEST AND APPLICATION INFORMATION

The test circuit is illustrated in Fig.7. The basic application circuit is illustrated in Fig.8. An interrupter with an N-channel depletion MOS transistor (e.g. BSD254A or BSP124) is shown. It is intended for applications where a low DC line voltage is required. An interrupter with an N-channel enhancement MOS transistor (e.g. BSN304A or BSP130) can be used for applications where a relatively high DC line voltage is allowed.

An application circuit for applications where a low DC line voltage and long line interrupts are required, is illustrated in Fig.9 (interrupter with an N-channel depletion MOS transistor).



Definitions:

Gain sending channel $G_M = 20 \log (V_{LN}/V_{MIC})$ with S1 in position 1; $V_{DTMF} = 0$.

Gain DTMF amplifier $G_{DTMF} = 20 \log (V_{LN}/V_{DTMF})$ with S1 in position 1; $V_m = 0$.

Gain receiving channel $G_{rec} = 20 \log (V_T/V_{LN})$ with S1 in position 2; $V_m = 0$.

Sidetone gain $G_{st} = 20 \log (V_T/V_{MIC})$ with S1 in position 1; $V_{DTMF} = 0$.

Fig.7 Test circuit of the PCA1070.

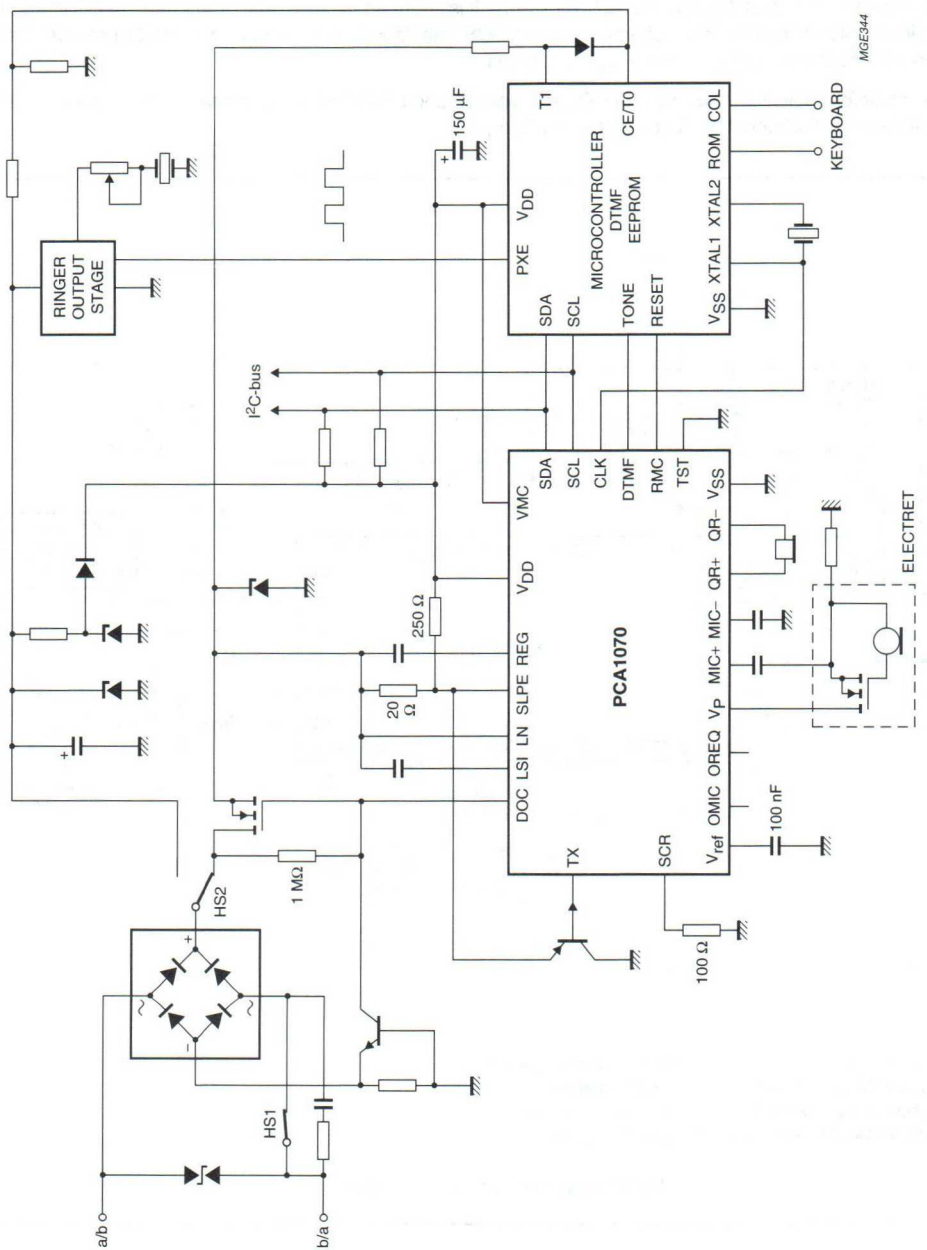


Fig.8 Basic application diagram.

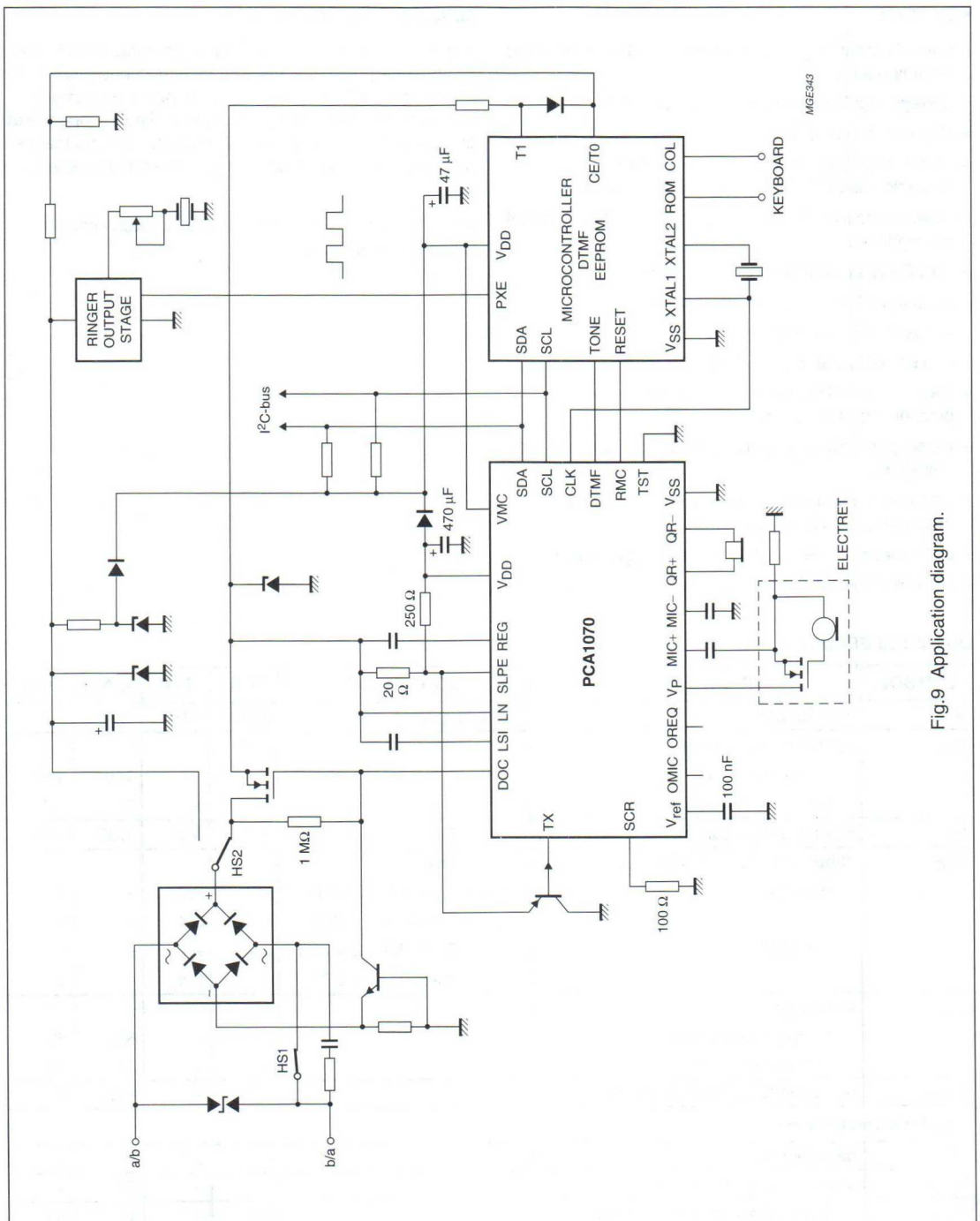


Fig.9 Application diagram.

Low voltage transmission circuits with dialler interface

TEA1062; TEA1062A

FEATURES

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable static resistance
- Provides a supply for external circuits
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
  - TEA1062: active HIGH (MUTE)
  - TEA1062A: active LOW ($\overline{\text{MUTE}}$)
- Receiving amplifier for dynamic, magnetic or piezoelectric earpieces
- Large gain setting ranges on microphone and earpiece amplifiers
- Line loss compensation (line current dependent) for microphone and earpiece amplifiers
- Gain control curve adaptable to exchange supply
- DC line voltage adjustment facility.

GENERAL DESCRIPTION

The TEA1062 and TEA1062A are integrated circuits that perform all speech and line interface functions required in fully electronic telephone sets. They perform electronic switching between dialling and speech. The ICs operate at line voltage down to 1.6 V DC (with reduced performance) to facilitate the use of more telephone sets connected in parallel.

All statements and values refer to all versions unless otherwise specified.

MAINTENANCE TYPE
Not recommended for new designs

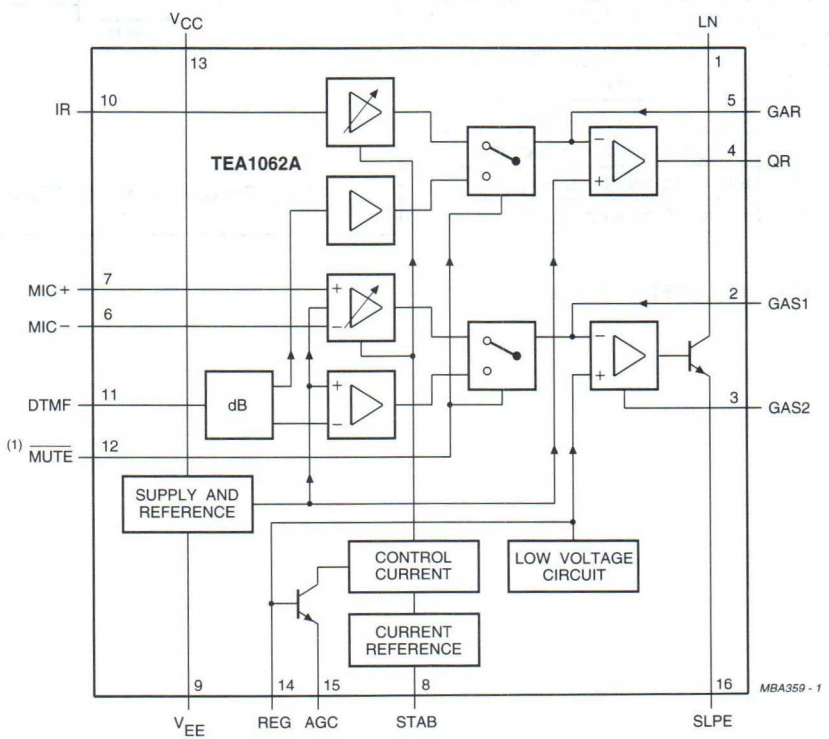
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	line voltage	I_{line} = 15 mA	3.55	4.0	4.25	V
I_{line}	operating line current					
	normal operation		11	–	140	mA
	with reduced performance		1	–	11	mA
I_{CC}	internal supply current	V_{CC} = 2.8 V	–	0.9	1.35	mA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA				
	TEA1062	I_p = 1.2 mA; MUTE = HIGH	2.2	2.7	–	V
		I_p = 0 mA; MUTE = HIGH	–	3.4	–	V
	TEA1062A	I_p = 1.2 mA; $\overline{\text{MUTE}}$ = LOW	2.2	2.7	–	V
		I_p = 0 mA; $\overline{\text{MUTE}}$ = LOW	–	3.4	–	V
G_v	voltage gain					
	microphone amplifier		44	–	52	dB
	receiving amplifier		20	–	31	dB
T_{amb}	operating ambient temperature		–25	–	+75	°C
Line loss compensation						
ΔG_v	gain control		–	5.8	–	dB
V_{exch}	exchange supply voltage		36	–	60	V
R_{exch}	exchange feeding bridge resistance		0.4	–	1	kΩ

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1062	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
TEA1062M1	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4 or SOT38-9
TEA1062A	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
TEA1062AM1	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4 or SOT38-9
TEA1062T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TEA1062AT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM



(1) Pin 12 is active HIGH (MUTE) for TEA1062.

Fig.1 Block diagram for TEA1062A.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
GAS1	2	gain adjustment; transmitting amplifier
GAS2	3	gain adjustment; transmitting amplifier
QR	4	non-inverting output; receiving amplifier
GAR	5	gain adjustment; receiving amplifier
MIC–	6	inverting microphone input
MIC+	7	non-inverting microphone input
STAB	8	current stabilizer
V_{EE}	9	negative line terminal
IR	10	receiving amplifier input
DTMF	11	dual-tone multi-frequency input
$\overline{MUTE}$	12	mute input (see note 1)
V_{CC}	13	positive supply decoupling
REG	14	voltage regulator decoupling
AGC	15	automatic gain control input
SLPE	16	slope (DC resistance) adjustment

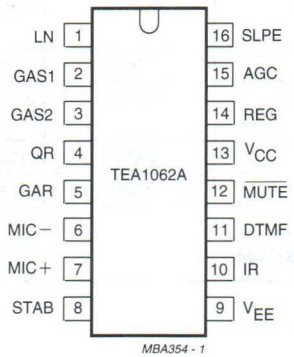


Fig.2 Pin configuration for TEA1062A.

Note

1. Pin 12 is active HIGH (MUTE) for TEA1062.

FUNCTIONAL DESCRIPTION

Supplies V_{CC}, LN, SLPE, REG and STAB

Power for the IC and its peripheral circuits is usually obtained from the telephone line. The supply voltage is derived from the line via a dropping resistor and regulated by the IC. The supply voltage V_{CC} may also be used to supply external circuits e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V_{EE}. The internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch} and the DC resistance of the telephone line R_{line}.

The circuit has an internal current stabilizer operating at a level determined by a 3.6 kΩ resistor connected between STAB and V_{EE} (see Fig.9). When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p) the excess current is shunted to V_{EE} via LN.

The regulated voltage on the line terminal (V_{LN}) can be calculated as:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9$$

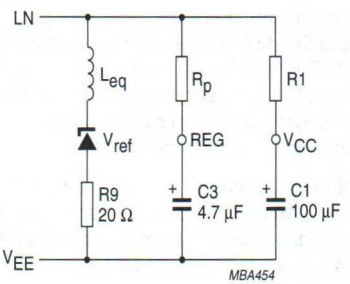
$$V_{LN} = V_{ref} + \{(I_{line} - I_{CC} - 0.5 \times 10^{-3}\ A) - I_p\} \times R9$$

V_{ref} is an internally generated temperature compensated reference voltage of 3.7 V and R9 is an external resistor connected between SLPE and V_{EE}.

In normal use the value of R9 would be 20 Ω.

Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics, sidetone level, maximum output swing on LN and the DC characteristics (especially at the lower voltages).

Under normal conditions, when $I_{SLPE} >> I_{CC} + 0.5\ mA + I_p$, the static behaviour of the circuit is that of a 3.7 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1. Fig.3 shows the equivalent impedance of the circuit.



$L_{eq} = C3 \times R9 \times R_p$.
$R_p = 16.2\ k\Omega$.

Fig.3 Equivalent impedance circuit.

At line currents below 9 mA the internal reference voltage is automatically adjusted to a lower value (typically 1.6 V at 1 mA). This means that more sets can be operated in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. At line currents below 9 mA the circuit has limited sending and receiving levels. The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor when connected between LN and REG will decrease the internal reference voltage and when connected between REG and SLPE will increase the internal reference voltage.

Current (I_p) available from V_{CC} for peripheral circuits depends on the external components used. Fig.10 shows this current for $V_{CC} > 2.2$ V. If MUTE is LOW (TEA1062) or $\overline{MUTE}$ is HIGH (TEA1062A) when the receiving amplifier is driven, the available current is further reduced. Current availability can be increased by connecting the supply IC (TEA1081) in parallel with R1 as shown in Fig.19 and Fig.20, or by increasing the DC line voltage by means of an external resistor (R_{VA}) connected between REG and SLPE (Fig.18).

Microphone inputs MIC+ and MIC− and gain pins GAS1 and GAS2

The circuit has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 × 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ, see Figures 14 and 15). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) can be used. Microphone arrangements are illustrated in Fig.11.

The gain of the microphone amplifier can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer in use. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2.

Stability is ensured by two external capacitors, C6 connected between GAS1 and SLPE and C8 connected between GAS1 and V_{EE}. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The value of C8 is 10 times the value of C6. The cut-off frequency corresponds to the time constant R7 × C6.

Input MUTE (TEA1062)

When MUTE is HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when MUTE is LOW or open-circuit. MUTE switching causes only negligible clicking on the line and earpiece output. If the number of parallel sets in use causes a drop in line current to below 6 mA the speech amplifiers remain active independent to the DC level applied to the MUTE input.

Input $\overline{\text{MUTE}}$ (TEA1062A)

When $\overline{\text{MUTE}}$ is LOW or open-circuit, the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when $\overline{\text{MUTE}}$ is HIGH. $\overline{\text{MUTE}}$ switching causes only negligible clicking on the line and earpiece output. If the number of parallel sets in use causes a drop in line current to below 6 mA the DTMF amplifier becomes active independent to the DC level applied to the $\overline{\text{MUTE}}$ input.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled dialling tones may be sent on to the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier IR, QR and GAR

The receiving amplifier has one input (IR) and a non-inverting output (QR). Earpiece arrangements are illustrated in Fig.12. The IR to QR gain is typically 31 dB (when R4 = 100 kΩ). It can be adjusted between 20 and 31 dB to match the sensitivity of the transducer in use. The gain is set with the value of R4 which is connected between GAR and QR. The overall receive gain, between LN and QR, is calculated by subtracting the anti-sidetone network attenuation (32 dB) from the amplifier gain. Two external capacitors, C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 times the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 × C4.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

Automatic Gain Control input AGC

Automatic line loss compensation is achieved by connecting a resistor (R6) between AGC and V_{EE}.

The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.8 dB which corresponds to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and average attenuation of 1.2 dB/km). Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.13 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line-loss compensation is required the AGC pin may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

Sidetone suppression

The anti-sidetone network, R1//Z_{line}, R2, R3, R8, R9 and Z_{bal}, (see Fig.4) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R9 \times R2 = R1 \times \left(R3 + \frac{R8 \times Z_{bal}}{R8 + Z_{bal}} \right) \quad (1)$$

$$\frac{Z_{bal}}{Z_{bal} + R8} = \frac{Z_{line}}{Z_{line} + R1} \quad (2)$$

If fixed values are chosen for R1, R2, R3 and R9, then condition (1) will always be fulfilled when $|R8//Z_{bal}| << R3$.

To obtain optimum sidetone suppression, condition (2) has to be fulfilled which results in:

$$Z_{bal} = \frac{R8}{R1} \times Z_{line} = k \times Z_{line}$$

Where k is a scale factor; $k = \frac{R8}{R1}$

The scale factor k, dependent on the value of R8, is chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| << R3$ fulfilling condition (a) and thus ensuring correct anti-sidetone bridge operation
- $|Z_{bal} + R8| >> R9$ to avoid influencing the transmit gain.

In practise Z_{line} varies considerably with the line type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.

EXAMPLE

The balance impedance Z_{bal} at which the optimum suppression is present can be calculated by:

Suppose Z_{line} = 210 Ω + (1265 Ω//140 nF) representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).

When k = 0.64 then R8 = 390 Ω;
Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig.4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier.
The attenuation is almost constant over the whole audio-frequency range.

Figure 5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances. (More information on the balancing of anti-sidetone bridges can be obtained in our publication *"Applications Handbook for Wired telecom systems, IC03b"*, order number 9397 750 00811.)

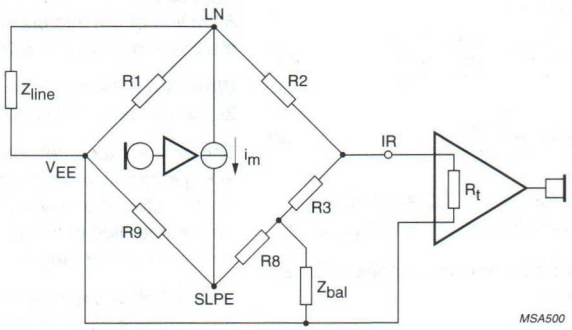


Fig.4 Equivalent circuit of TEA1060 family anti-sidetone bridge.

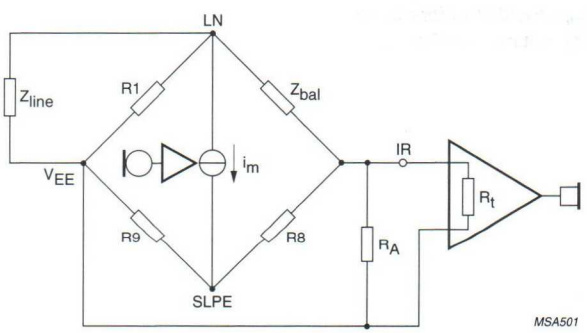


Fig.5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		–	12	V
$V_{LN(R)}$	repetitive line voltage during switch-on or line interruption		–	13.2	V
$V_{LN(RM)}$	repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω; see Fig.18	–	28	V
I_{line}	line current	R9 = 20 Ω; note 1	–	140	mA
V_I	input voltage on all other pins	positive input voltage	–	V_{CC} + 0.7	V
		negative input voltage	–	−0.7	V
P_{tot}	total power dissipation	R9 = 20 Ω; note 2			
	TEA1062; TEA1062A		–	666	mW
	TEA1062M1; TEA1062AM1		–	617	mW
	TEA1062T; TEA1062AT		–	454	mW
T_{amb}	operating ambient temperature		−25	+75	°C
T_{stg}	storage temperature		−40	+125	°C
T_j	junction temperature		–	125	°C

Notes

1. Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE (see Figs 6, 7 and 8).
2. Calculated for the maximum ambient temperature specified (T_{amb} = 75 °C) and a maximum junction temperature of 125 °C.

HANDLING

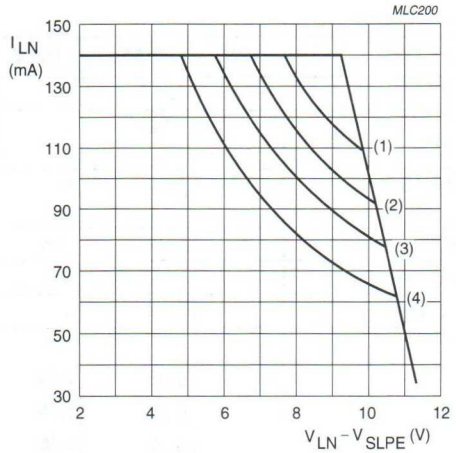
This device meets class 2 ESD test requirements [Human Body Model (HBM)], in accordance with *"MIL STD 883C - method 3015"*.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1062; TEA1062A	75	K/W
	TEA1062M1; TEA1062AM1	81	K/W
	TEA1062T; TEA1062AT (note 1)	110	K/W

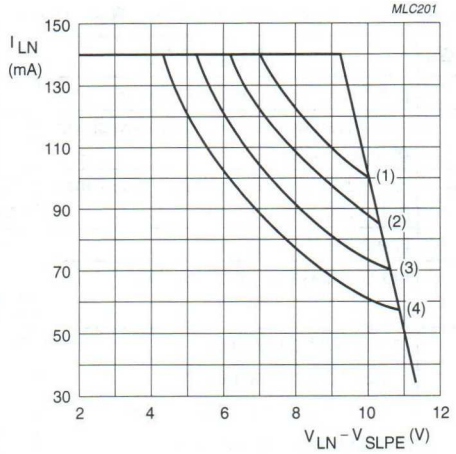
Note

1. Mounted on glass epoxy board 28.5 × 19.1 × 1.5 mm.



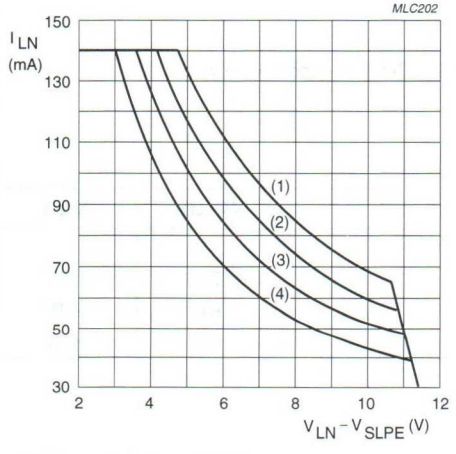
(1) T_{amb} = 45 °C; P_{tot} = 1068 mW.
(2) T_{amb} = 55 °C; P_{tot} = 934 mW.
(3) T_{amb} = 65 °C; P_{tot} = 800 mW.
(4) T_{amb} = 75 °C; P_{tot} = 666 mW.

Fig.6 TEA1062 and TEA1062A safe operating area.



(1) T_{amb} = 45 °C; P_{tot} = 988 mW.
(2) T_{amb} = 55 °C; P_{tot} = 864 mW.
(3) T_{amb} = 65 °C; P_{tot} = 741 mW.
(4) T_{amb} = 75 °C; P_{tot} = 617 mW.

Fig.7 TEA1062M1 and TEA1062AM1 safe operating area.



(1) T_{amb} = 45 °C; P_{tot} = 727 mW.
(2) T_{amb} = 55 °C; P_{tot} = 636 mW.
(3) T_{amb} = 65 °C; P_{tot} = 545 mW.
(4) T_{amb} = 75 °C; P_{tot} = 454 mW.

Fig.8 TEA1062T and TEA1062AT safe operating area.

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies LN and V_{CC} (pins 1 and 13)						
V_{LN}	voltage drop over circuit between LN and V_{EE}	MIC inputs open-circuit				
		I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	1.9	–	V
		I_{line} = 15 mA	3.55	4.0	4.25	V
		I_{line} = 100 mA	4.9	5.7	6.5	V
		I_{line} = 140 mA	–	–	7.5	V
$\Delta V_{LN}/\Delta T$	variation with temperature	I_{line} = 15 mA	–	–0.3	–	mV/K
V_{LN}	voltage drop over circuit between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA				
		R_{VA} (LN to REG) = 68 kΩ	–	3.5	–	V
		R_{VA} (REG to SLPE) = 39 kΩ	–	4.5	–	V
I_{CC}	supply current	V_{CC} = 2.8 V	–	0.9	1.35	mA
V_{CC}	supply voltage available for peripheral circuitry	I_{line} = 15 mA; MUTE = HIGH				
	TEA1062	I_p = 1.2 mA	2.2	2.7	–	V
		I_p = 0 mA	–	3.4	–	V
V_{CC}	supply voltage available for peripheral circuitry	I_{line} = 15 mA; $\overline{\text{MUTE}}$ = LOW				
	TEA1062A	I_p = 1.2 mA	2.2	2.7	–	V
		I_p = 0 mA	–	3.4	–	V
Microphone inputs MIC– and MIC+ (pins 6 and 7)						
$\lvert Z_i \rvert$	input impedance					
	differential	between MIC– and MIC+	–	64	–	kΩ
	single-ended	MIC– or MIC+ to V_{EE}	–	32	–	kΩ
CMRR	common mode rejection ratio		–	82	–	dB
G_v	voltage gain MIC+ or MIC– to LN	I_{line} = 15 mA; R7 = 68 kΩ	50.5	52.0	53.5	dB
ΔG_{vf}	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
ΔG_{vT}	gain variation with temperature referenced to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 and +75 °C	–	±0.2	–	dB
DTMF input (pin 11)						
$\lvert Z_i \rvert$	input impedance		–	20.7	–	kΩ
G_v	voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	24.0	25.5	27.0	dB
ΔG_{vf}	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
ΔG_{vT}	gain variation with temperature referenced to 25 °C	I_{line} = 50 mA; T_{amb} = –25 and +75 °C	–	±0.2	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Gain adjustment inputs GAS1 and GAS2 (pins 2 and 3)						
ΔG_v	transmitting amplifier gain variation by adjustment of R7 between GAS1 and GAS2		−8	−	0	dB
Sending amplifier output LN (pin 1)						
$V_{LN(rms)}$	output voltage (RMS value)	THD = 10%				
		I_{line} = 4 mA	−	0.8	−	V
		I_{line} = 15 mA	1.7	2.3	−	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC− and MIC+; psophometrically weighted (P53 curve)	−	−69	−	dBmp
Receiving amplifier input IR (pin 10)						
$\lvert Z_i \rvert$	input impedance		−	21	−	kΩ
Receiving amplifier output QR (pin 4)						
$\lvert Z_o \rvert$	output impedance		−	4	−	Ω
G_v	voltage gain from IR to QR	I_{line} = 15 mA; R_L = 300 Ω (from pin 9 to pin 4)	29.5	31	32.5	dB
ΔG_{vf}	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	−	±0.2	−	dB
ΔG_{vT}	gain variation with temperature referenced to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 and +75 °C	−	±0.2	−	dB
$V_{o(rms)}$	output voltage (RMS value)	THD = 2%; sine wave drive; R4 = 100 kΩ; I_{line} = 15 mA; I_p = 0 mA				
		R_L = 150 Ω	0.22	0.33	−	V
		R_L = 450 Ω	0.3	0.48	−	V
$V_{o(rms)}$	output voltage (RMS value)	THD = 10%; R4 = 100 kΩ; R_L = 150 Ω; I_{line} = 4 mA	−	15	−	mV
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted (P53 curve); R_L = 300 Ω	−	50	−	μV
Gain adjustment input GAR (pin 5)						
ΔG_v	receiving amplifier gain variation by adjustment of R4 between GAR and QR		−11	−	0	dB
Mute input (pin 12)						
V_{IH}	HIGH level input voltage		1.5	−	V_{CC}	V
V_{IL}	LOW level input voltage		−	−	0.3	V
I_{MUTE}	input current		−	8	15	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reduction of gain						
ΔG_v	MIC+ or MIC– to LN					
	TEA1062	MUTE = HIGH	–	70	–	dB
	TEA1062A	$\overline{MUTE}$ = LOW	–	70	–	dB
G_v	voltage gain from DTMF to QR	R4 = 100 kΩ; R_L = 300 Ω				
	TEA1062	MUTE = HIGH	–	–17	–	dB
	TEA1062A	$\overline{MUTE}$ = LOW	–	–17	–	dB
Automatic gain control input AGC (pin 15)						
ΔG_v	controlling the gain from IR to QR and the gain from MIC+, MIC– to LN gain control range	R6 = 110 kΩ (between AGC and V_{EE}) I_{line} = 70 mA	–	–5.8	–	dB
I_{lineH}	highest line current for maximum gain		–	23	–	mA
I_{lineL}	lowest line current for minimum gain		–	61	–	mA

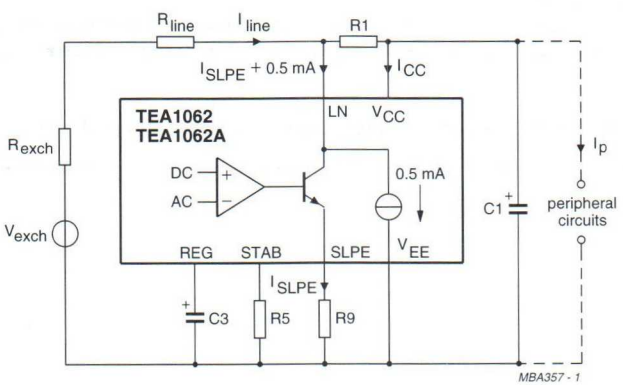
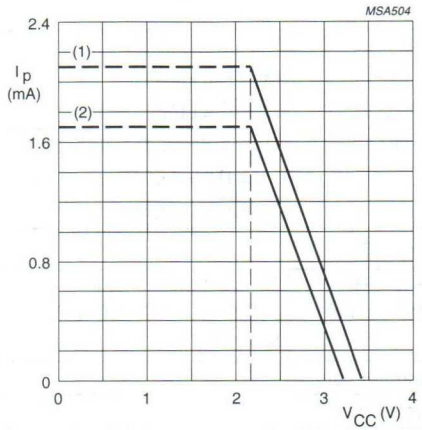


Fig.9 Supply arrangement.



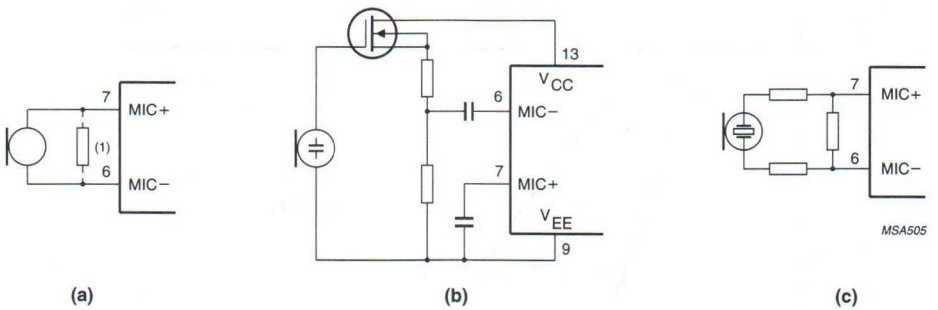
The supply possibilities can be increased by setting the voltage drop over the circuit V_{LN} to a higher value by resistor R_{VA} connected between REG and SLPE.

$V_{CC} > 2.2$ V; $I_{line} = 15$ mA at $V_{LN} = 4$ V; R1 = 620 Ω; R9 = 20 Ω.

(1) $I_p = 2.1$ mA. Is valid when the receiving amplifier is not driven or when MUTE = HIGH (TEA1062), $\overline{\text{MUTE}}$ = LOW (TEA1062A).

(2) $I_p = 1.7$ mA. Is valid when MUTE = LOW (TEA1062), $\overline{\text{MUTE}}$ = HIGH (TEA1062A) and the receiving amplifier is driven; $V_{o(rms)} = 150$ mV, $R_L = 150$ Ω.

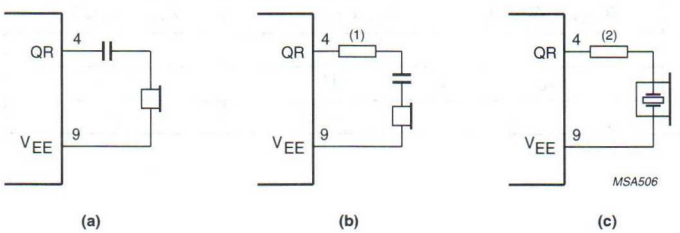
Fig.10 Typical current I_p available from V_{CC} for peripheral circuitry.



(a) Magnetic or dynamic microphone.
(b) Electret microphone.
(c) Piezoelectric microphone.

(1) Resistor may be connected to reduce the terminating impedance.

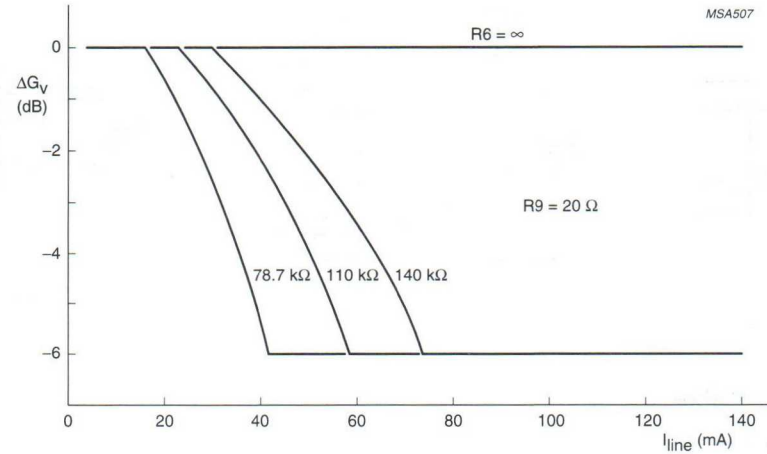
Fig.11 Alternative microphone arrangements.



(a) Dynamic earpiece.
(b) Magnetic earpiece.
(c) Piezoelectric earpiece.

(1) Resistor may be connected to prevent distortion (inductive load).
(2) Resistor is required to increase the phase margin (capacitive load).

Fig.12 Alternative receiver arrangements.

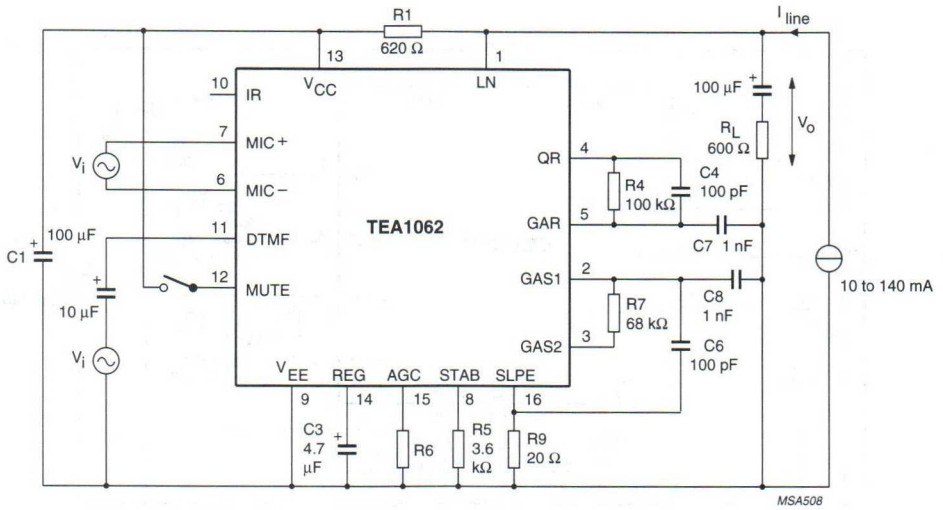


R9 = 20 Ω.

Fig.13 Variation of gain as a function of line current with R6 as a parameter.

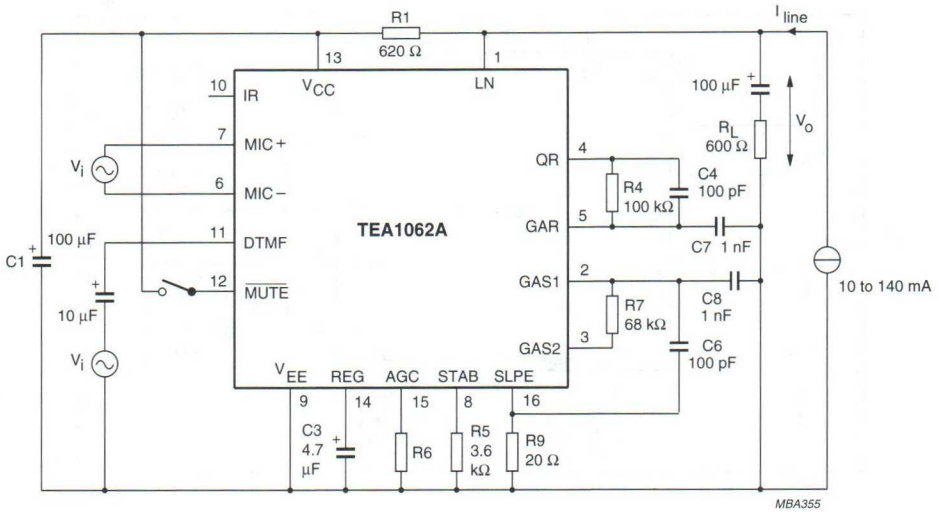
Table 1 Values of resistor R6 for optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

V_{exch} (V)	R6 (kΩ)			
	R_{exch} = 400 Ω	R_{exch} = 600 Ω	R_{exch} = 800 Ω	R_{exch} = 1000 Ω
36	100	78.7	–	–
48	140	110	93.1	82
60	–	–	120	102



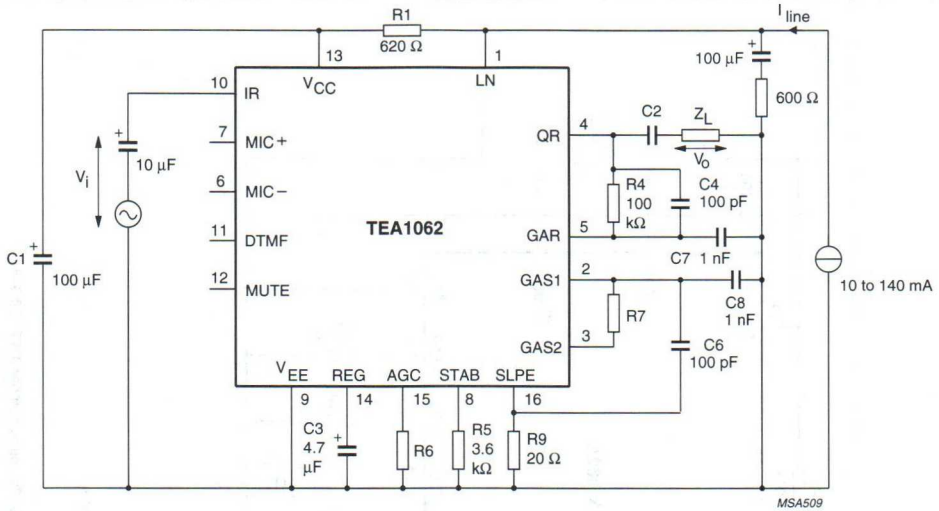
Voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.
For measuring gain from MIC+ and MIC− the MUTE input should be LOW or open-circuit.
For measuring the DTMF input, the MUTE input should be HIGH.
Inputs not being tested should be open-circuit.

Fig.14 Test circuit for defining TEA1062 voltage gain of MIC+, MIC− and DTMF inputs.



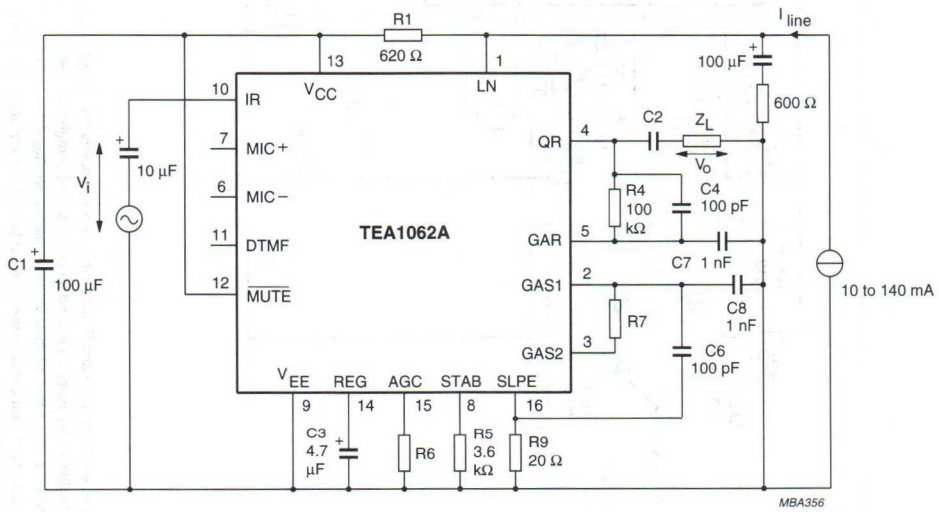
Voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.
For measuring gain from MIC+ and MIC− the $\overline{\text{MUTE}}$ input should be HIGH.
For measuring the DTMF input, the $\overline{\text{MUTE}}$ input should be LOW or open-circuit.
Inputs not being tested should be open-circuit.

Fig.15 Test circuit for defining TEA1062A voltage gain of MIC+, MIC− and DTMF inputs.



Voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.

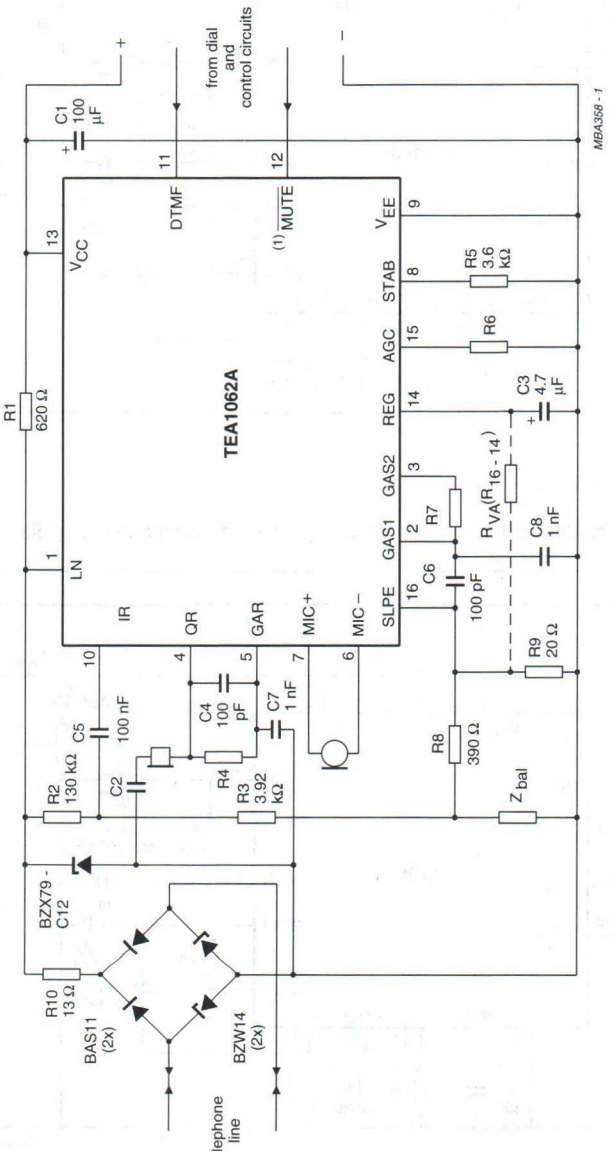
Fig.16 Test circuit for defining TEA1062 voltage gain of the receiving amplifier.



Voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.

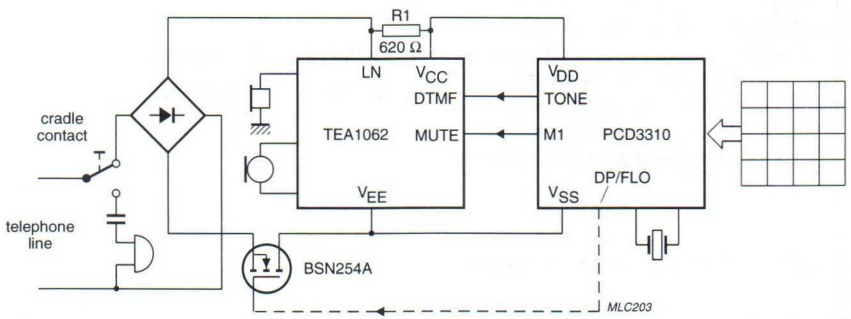
Fig.17 Test circuit for defining TEA1062A voltage gain of the receiving amplifier.

APPLICATION INFORMATION



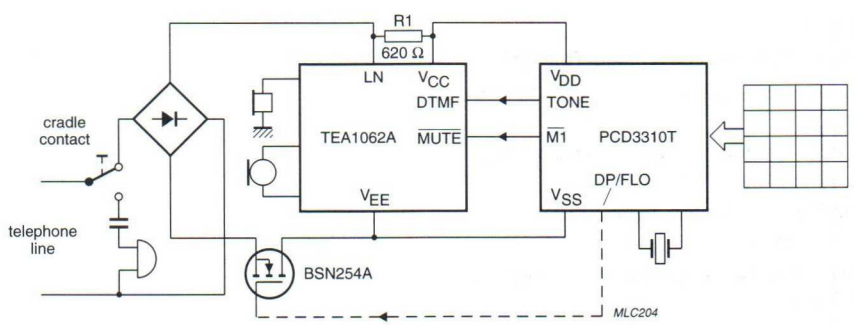
The diode bridge, the Zener diode and R10 limit the current into, and the voltage across, the circuit during line transients.
A different protection arrangement is required for pulse dialling or register recall.
The DC line voltage can be set to a higher value by the resistor R_{VA} (REG to SLPE).
Further application information can be found in our publication *"Applications Handbook for Wired telecom systems, IC03b"*, order number 9397 750 00811.
(1) Pin 12 is active HIGH (MUTE) for TEA1062.

Fig.18 Typical application of TEA1062A, with piezoelectric earpiece and DTMF dialling.



(a) DTMF pulse set with CMOS bilingual dialling circuit PCD3310. The dashed line shows an optional flash (register recall by timed loop break).

Fig.19 Typical simplified application of the TEA1062.



(a) DTMF pulse set with CMOS bilingual dialling circuit PCD3310T. The dashed line shows an optional flash (register recall by timed loop break).

Fig.20 Typical simplified application of the TEA1062A.

Low voltage versatile telephone transmission circuit with dialler interface and transmit level dynamic limiting

TEA1064A

GENERAL DESCRIPTION

The TEA1064A is a bipolar integrated circuit that performs all the speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech and has a powerful DC supply for peripheral circuits. The IC operates at line voltages down to 1.8 V DC (with reduced performance) to facilitate the use of more telephone sets connected in parallel. The transmit signal on the line is dynamically limited (speech-controlled) to prevent distortion at high transmit levels of both the sending signal and the sidetone.

FEATURES

- Low DC line voltage; operates down to 1.8 V (excluding polarity guard)
- Voltage regulator with low voltage drop and adjustable static resistance
- DC line voltage adjustment facility
- Provides a supply for external circuits in two options:
  - unregulated supply, regulated line voltage;
  - stabilized supply, line voltage varies with supply current
- Dynamic limiting (speech-controlled) in transmit direction prevents distortion of line signal and sidetone
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- DTMF signal input
- Confidence tone in the earpiece during DTMF dialling
- Mute input for disabling speech during pulse or DTMF dialling
- Power-down input for improved performance during pulse dial or register recall (flash)
- Receiving amplifier for magnetic, dynamic or piezo-electric earpieces
- Large amplification setting ranges on microphone and earpiece amplifiers
- Line loss compensation (line current dependent) for microphone and earpiece amplifiers (not used for DTMF amplifier)
- Gain control curve adaptable to exchange supply
- Automatic disabling of the DTMF amplifier in extremely-low voltage conditions
- Microphone MUTE function available with switch

PACKAGE OUTLINES

TEA1064A :20-lead DIL; plastic (SOT146).[1]

TEA1064AT:20-lead mini-pack; plastic (SO20; SOT163A).[2]

Notes

1. SOT146-1; 1998 Jun 18.
2. SOT163-1; 1998 Jun 18.

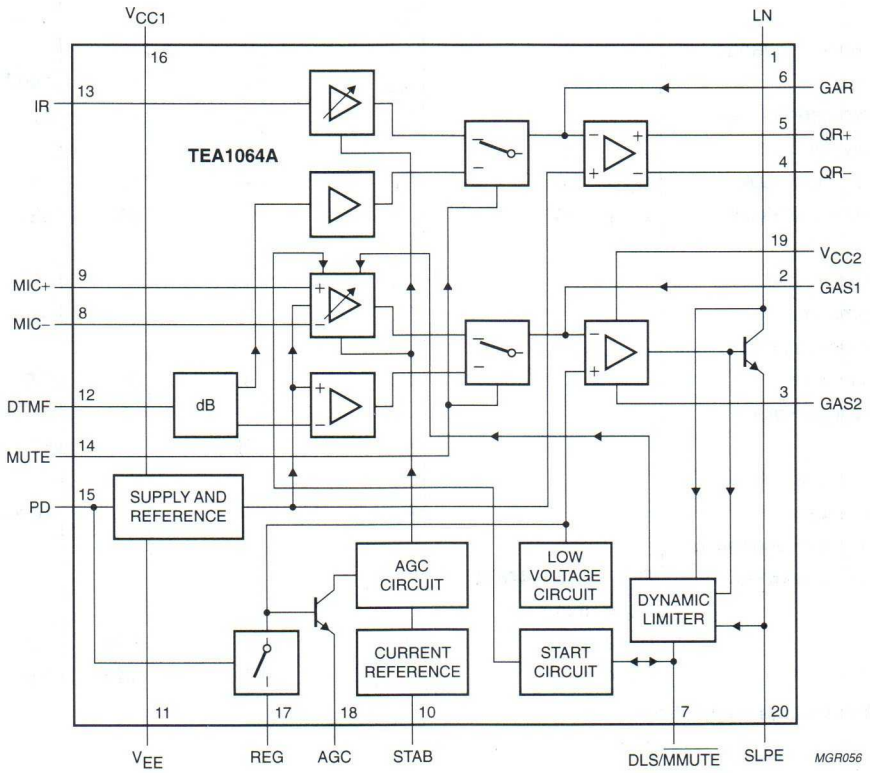


Fig.1 Block diagram.

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating ambient temperature range		T_{amb}	−25	–	+ 75	°C
Line current operating range:						
normal operation		I_{line}	11	–	140[1]	mA
with reduced performance		I_{line}	2	–	11	mA
Internal supply current:						
power-down input LOW	V_{CC1} = 2.8 V	I_{CC1}	–	1.3	1.6	mA
power-down input HIGH	V_{CC1} = 2.8 V	I_{CC1}	–	60	82	µA
Voltage gain range:						
microphone amplifier		G_v	44	–	52	dB
receiving amplifier		G_v	20	–	45	dB
Line loss compensation:						
gain control range		G_v	5.7	6.1	6.5	dB
exchange supply voltage range		V_{exch}	36	–	60	V
exchange feeding bridge resistance range		R_{exch}	400	–	1000	Ω
Maximum output voltage swing on LN (peak-to-peak value)	R15 + R16 = 448 Ω					
	I_{line} = 15 mA					
	I_p = 2 mA	$V_{LN(p-p)}$	3.7	3.95	4.2	V
	I_p = 4 mA	$V_{LN(p-p)}$	3.0	3.25	3.5	V
Regulated line voltage application						
	R15 = 0 Ω;					
	R16 = 392 Ω					
Supply for peripherals	I_{line} = 15 mA					
	I_p = 1.4 mA	V_p	2.5	–	–	V
	I_p = 2.7 mA;					
	$R_{REG-SLPE}$ = 20 kΩ	V_p	2.9	–	–	V
DC line voltage	I_{line} = 15 mA					
	without $R_{REG-SLPE}$	V_{LN}	–	3.57	–	V
	$R_{REG-SLPE}$ = 20 kΩ	V_{LN}	–	4.57	–	V

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Stabilized supply voltage application						
	R15 = 392 Ω; R16 = 56 Ω					
Supply for peripherals	I_{line} = 15 mA					
	I_p = 0 to 4 mA	$V_{CC2-SLPE}$	3.05	3.3	3.55	V
DC line voltage	I_{line} = 15 mA					
	I_p = 2 mA	V_{LN}	4.2	4.4	4.8	V
	I_p = 4 mA	V_{LN}	4.9	5.1	5.5	V

Note

1. For TEA1064AT the maximum line current depends on the heat dissipating qualities of the mounted device.

PINNING

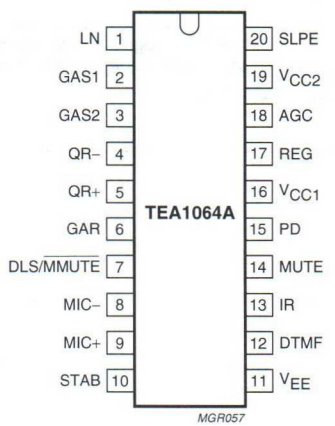


Fig.2 Pinning diagram.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	$\overline{\text{DLS}}$/$\overline{\text{MMUTE}}$	decoupling for transmit amplifier dynamic and microphone MUTE input
8	MIC–	inverting microphone input
9	MIC+	non-inverting microphone input
10	STAB	current stabilizer
11	V_{EE}	negative line terminal
12	DTMF	dual-tone multi-frequency input
13	IR	receiving amplifier input
14	MUTE	mute input
15	PD	power-down input
16	V_{CC1}	internal supply decoupling
17	REG	voltage regulator decoupling
18	AGC	automatic gain control input
19	V_{CC2}	reference voltage with respect to SLPE
20	SLPE	slope adjustment for DC curve/reference for peripheral circuits.

FUNCTIONAL DESCRIPTION

Supplies V_{CC1}, V_{CC2}, LN, SLPE, REG and STAB (Fig.3)

Power for the TEA1064A and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply voltage at V_{CC1} and regulates its voltage drop. The internal supply requires a decoupling capacitor between V_{CC1} and V_{EE}. The internal current stabilizer is set by a 3.6 kΩ resistor between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the subscriber line DC resistance R_{line} and the DC voltage (including polarity guard) on the subscriber set (see Fig.3).

The internal voltage regulator generates a temperature-compensated reference voltage that is available between V_{CC2} and SLPE [$V_{ref} = V_{CC2-SLPE} = 3.3$ V (typ.)]. This internal voltage regulator requires decoupling by a capacitor between REG and V_{EE} (C3).

The reference voltage can be used to:

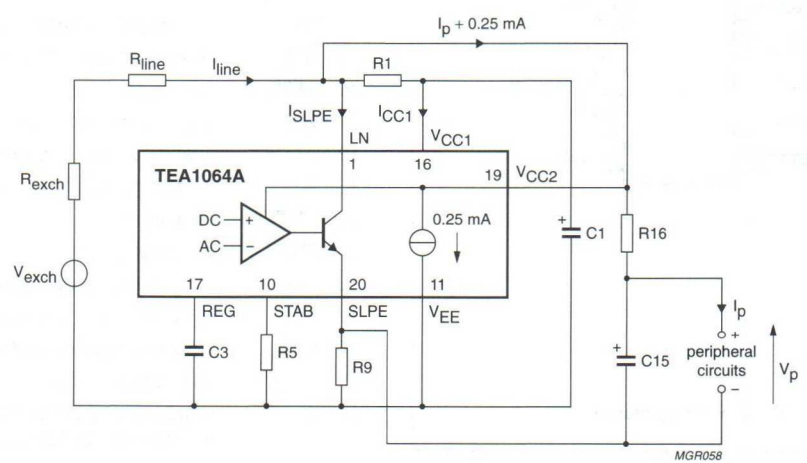
- regulate directly the line voltage (stabilized $V_{LN-SLPE} = V_{CC2-SLPE}$)(1)
- to stabilize the supply voltage for peripherals.

Regulated line voltage

In this application the V_{CC2} pin is connected to the LN pin as shown in Fig.3. This configuration gives a stabilized voltage across pins LN and SLPE which, applied via the low-pass filter R16, C15, provides a supply to the peripherals that is independent of the line current and depends only on the peripheral supply current.

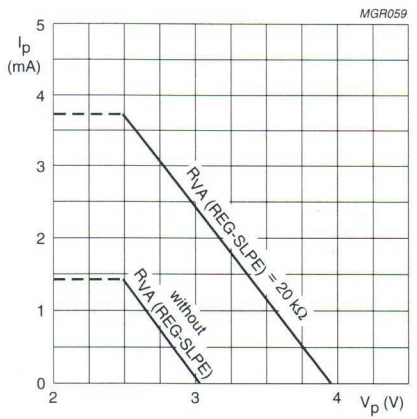
The value of R16 and the level of the DC voltage $V_{LN-SLPE}$ determine the supply capabilities. In the basic application R16 = 392 Ω and C15 = 220 µF. The worst-case peripheral supply current as a function of supply voltage is shown in Fig.4. To increase the supply capabilities, the DC voltage $V_{LN-SLPE}$ can be increased by using $R_{VA(REG-SLPE)}$ or by decreasing the value of R16.

(1) The TEA1064A application with regulated line voltage is the same as is used for TEA1060/TEA1061, TEA1067 and TEA1068 integrated circuits.



The voltage $V_{LN-SLPE}$ is fixed to $V_{ref} = 3.3 \pm 0.25$ V. Resistor R16 together with the line current determine the supply capabilities and the maximum output swing on the line (no loop damping is necessary).
The line voltage $V_{LN} = V_{ref} + ([I_{line} - 1.55\ mA] \times R9)$.

Fig.3 Application with regulated line voltage (stabilized $V_{LN-SLPE}$).



I_{line} = 15 mA; R16 = 392 Ω; R15 = 0 Ω; valid for MUTE = 0 and 1. Line current has very little influence

Fig.4 Minimum supply current for peripherals (I_p) as a function of the peripheral supply voltage (V_p).

The maximum AC output swing on the line at low line currents is influenced by R16 (limited by current) and the maximum output swing on the line at high line currents is influenced by the DC voltage $V_{LN-SLPE}$ (limited by voltage). In both these situations, the internal dynamic limiter in the sending channel prevents distortion when the microphone input is overdriven. The maximum AC output swing on LN is shown in Fig.5; practical values for R16 are from 200 to 600 Ω and this influences both the maximum output swing at low line currents and the supply capabilities.

The SLPE pin is the ground reference for peripheral circuits, therefore inputs MUTE, PD and DTMF are also referenced to SLPE.

Active microphones can be supplied between V_{CC1} and V_{EE}. Low-power circuits that provide only MUTE and/or PD inputs to the TEA1064A also can be powered from V_{CC1}. However V_{CC1} cannot be used for circuits that provide DTMF signals to the TEA1064A because V_{CC1} is referred to ground.

If the line current I_{line} exceeds I_{CC1} + 0.25 mA, the voltage converter shunts the excess current to SLPE via LN; where $I_{CC1} \approx 1.3$ mA, the value required by the IC for normal operation.

The DC line voltage on LN is:

$$V_{LN} = V_{LN-SLPE} + (I_{SLPE} \times R9)$$

$$V_{LN} = V_{ref} + ([I_{line} - I_{CC1} - 0.25 \times 10^{-3}\ A] \times R9)$$

in which

V_{ref} = 3.3 V ± 0.25 V is the internal reference voltage between V_{CC2} and SLPE; its value can be adjusted by external resistor R_{VA}

R9 = external resistor between SLPE and V_{EE} (20 Ω in basic application).

With R9 = 20 Ω, this results in:

V_{LN} = 3.57 ± 0.25 V at I_{line} = 15 mA

V_{LN} = 4.17 ± 0.3 V at I_{line} = 15 mA, $R_{VA(REG-SLPE)}$ = 33 kΩ

V_{LN} = 4.57 ± 0.35 V at I_{line} = 15 mA, $R_{VA(REG-SLPE)}$ = 20 kΩ

The preferred value for R9 is 20 Ω. Changing R9 influences microphone gain, DTMF gain, the gain control characteristics, sidetone, and the DC characteristics (especially the low voltage characteristics).

In normal conditions, $I_{SLPE} >> (I_{CC1} + 0.25\ mA)$ and the static behaviour is equivalent to a voltage regulator diode with an internal resistance of R9. In the audio frequency range the dynamic impedance is determined mainly by R1. The equivalent impedance of the circuit in the audio frequency range is shown in Fig.6.

The internal reference voltage $V_{CC2-SLPE}$ can be increased by external resistor $R_{VA(REG-SLPE)}$ connected between REG and SLPE. The supply voltage $V_{CC2-SLPE}$ is shown as a function of $R_{VA(REG-SLPE)}$ in Fig.7. Changing the reference voltage influences the output swing of both sending and receiving amplifiers.

At line currents below 8 mA (typ.), the DC voltage dropped across the circuit is adjusted to a lower level automatically (approximately 1.8 V at 2 mA). This gives the possibility of operating more telephone sets in parallel with DC line voltages (excluding polarity guard) down to an absolute minimum of 1.8 V. At line currents below 8 mA (typ.), the circuit has limited sending and receiving levels.

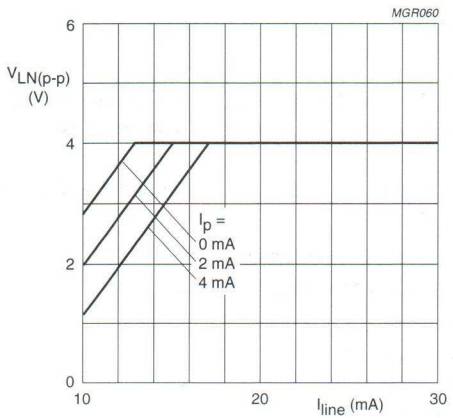


Fig.5 Maximum AC output swing on the line as a function of line current with peripheral supply current as a parameter: R15 = 0 Ω; R16 = 392 Ω.

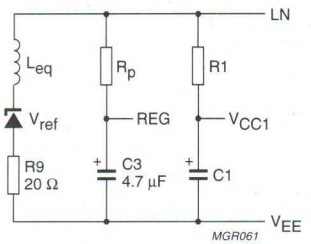


Fig.6 Equivalent impedance between LN and V_{EE} in the application with stabilized $V_{LN-SLPE}$:
R15 = 0 Ω
$L_{eq} = C3 \times R9 \times R_p$
R_p = 15 kΩ

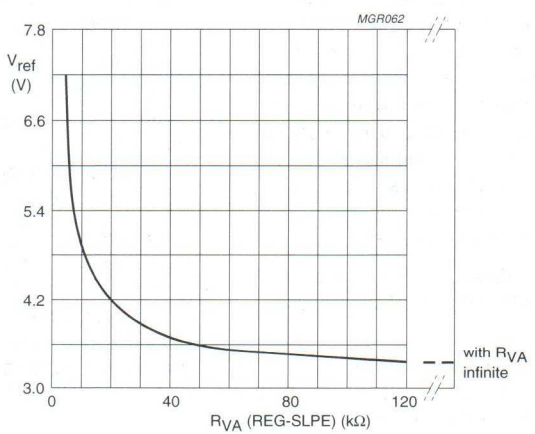


Fig.7 Internal reference voltage $V_{CC2-SLPE}$ as a function of resistor $R_{VA(REG-SLPE)}$ for line currents between 11 and 140 mA.

In the stabilized supply application:
$V_{LN} = V_{CC2-SLPE} + ([I_p + 0.25 \times 10^{-3}\ A] \times R15) + ([I_{line} - 1.55 \times 10^{-3}\ A] \times R9)$
In the unregulated supply application (R15 = 0 Ω):
$V_{LN} = V_{CC2-SLPE} + ([I_{line} - 1.55 \times 10^{-3}\ A] \times R9)$

Stabilized peripheral supply voltage

The configuration shown in Fig.8 provides a stabilized voltage across pins V_{CC2} and SLPE for peripheral circuits (such as dialling and control circuits); the DC voltage V_{LN} now varies with the peripheral supply current.

The $V_{CC2\text{-}SLPE}$ supply must be decoupled by capacitor C15. For stable loop operation, resistor R16 ($\approx 50\ \Omega$) is connected between V_{CC2} and SLPE in series with C15. The voltage regulator control loop is completed by resistor R15 between LN and V_{CC2}.

For sets with an impedance of 600 Ω, practical values are: R15 = 200 to 600 Ω; C15 = 220 µF; C3 = 470 nF. The ratio R15/R16 ≤ 8 is for stable loop operation with sufficient phase margin, and R15/R16 ≥ 6 is for satisfactory set impedance in the audio frequency range.

For sets with complex impedance, the value of C3 and the ratio R15/R16 are different (further information is given in the TEA1064A Application Report(1)).

The peripheral supply capability depends mainly on the available line current, the required AC output swing on the line, the maximum permitted DC voltage on the line and the values of external components (especially R15). With R15 = 392 Ω and R16 = 56 Ω (basic application) the maximum possible AC output swing on the line as a function of line current is as shown in Fig.9, the curve parameter is the peripheral supply current (I_p). Different values for R15 (from 200 to 600 Ω) maintaining $6 < R15/R16 < 8$ give different results (these are described in the TEA1064A Application Report (1).

(1) Supplied on request.

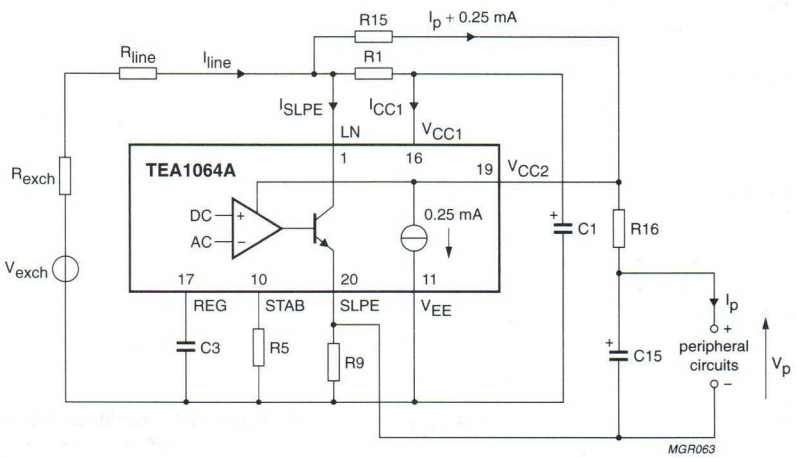


Fig.8 Application with stabilized supply voltage for peripheral circuits: R15 = 392 Ω; R16 = 56 Ω.

The DC line voltage on LN is

$$V_{LN} = V_{LN\text{-}SLPE} + (I_{SLPE} \times R9).$$

Therefore

$$V_{LN} = V_{ref} + ([I_p + 0.25 \times 10^{-3}\ A] \times R15) + ([I_{line} - I_{CC1} - 0.25 \times 10^{-3}\ A] \times R9)$$

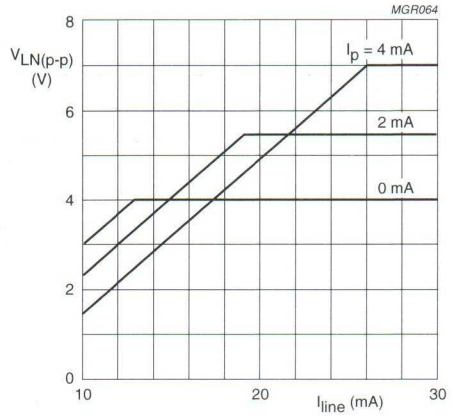
in which:

V_{ref} is the internal reference voltage between V_{CC2} and SLPE (the value of V_{ref} can be adjusted by an external resistor, R_{VA}). V_{ref} = 3.3 V (typ.) without R_{VA}

I_p is the supply current used by peripheral circuits

R15 is an external resistor between LN and V_{CC2} (392 Ω in the basic application)

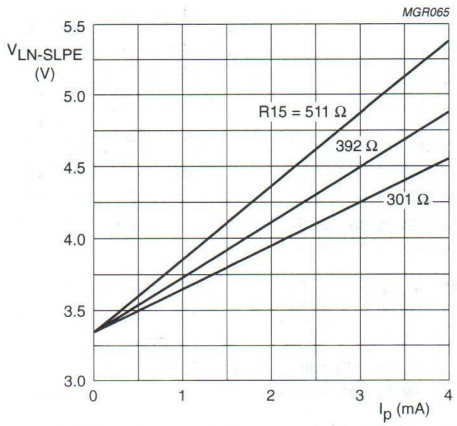
R9 is an external resistor between SLPE and V_{EE} (20 Ω in the basic application)



As different values of R15 and R16 are allowed, different curves would then apply

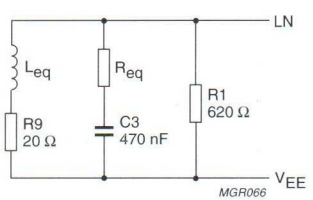
Fig.9 Maximum output swing on line as a function of line current with the peripheral supply current as a parameter; R15 = 392 Ω; R16 = 56 Ω.

The DC voltage $V_{LN\text{-}SLPE}$ as a function of I_p with R15 as a parameter is shown in Fig.10. In the audio frequency range, the dynamic impedance is determined mainly by R1. The equivalent impedance in the audio range of the circuit (Fig.8) is shown in Fig.11.



$V_{CC2\text{-}SLPE}$ can be adjusted between approximately 3.3 and 4.3 V by changing the value of R_{VA}, this results in a parallel-shift of the curves. The total voltage drop $V_{LN} \approx V_{LN\text{-}SLPE} + ([I_{line} - 1.55\ mA] \times R9)$.

Fig.10 Curves showing the typical voltage drop between LN and SLPE as a function of the supply current for peripherals with R15 as a parameter: $V_{CC2\text{-}SLPE}$ = 3.3 V (R_{VA} not connected).



$$R_{eq} = R_p \left(\frac{R15}{R16} + 1 \right)$$

$$L_{eq} = C3 \times R9 \times R_{eq} \text{ with } R_p = 15\ k\Omega$$

Fig.11 Equivalent impedance between LN and V_{EE} at f > 300 Hz in the application with stabilized supply voltage for peripheral circuits.

Microphone inputs MIC+ and MIC− and gain pins GAS1 and GAS2

The TEA1064A has symmetrical microphone inputs, its input impedance is 64 kΩ (2 × 32 kΩ) and its voltage amplification is typ. 52 dB with R7 = 68 kΩ. Either dynamic, magnetic or piezo-electric microphones can be used, or an electret microphone with a built-in FET buffer. Arrangements for the microphone types are shown in Fig.12.

The gain of the microphone amplifier is proportional to external resistor R7 connected between GAS1 and GAS2 and with this it can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer.

An external 100 pF capacitor (C6) is required between GAS1 and SLPE to ensure stability. A larger value of C6 may be chosen to obtain a first-order low-pass filter with a cut-off frequency corresponding to the time constant R7 × C6.

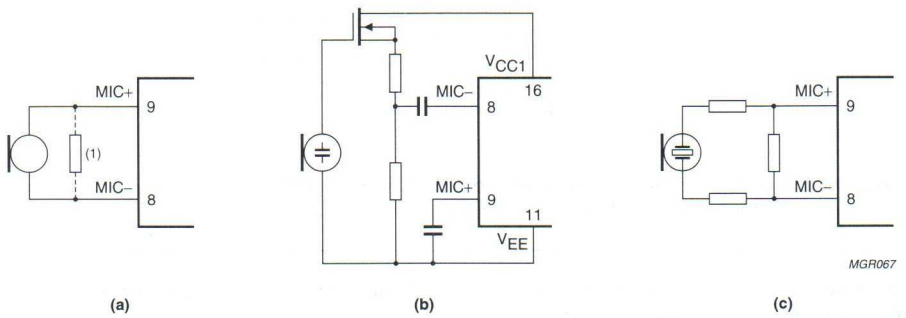


Fig.12 Microphone arrangements: a) magnetic or dynamic microphone, the resistor (1) may be connected to reduce the terminating impedance, or for sensitive types a resistive attenuator can be used to prevent overloading the microphone inputs; b) electret microphone; c) piezo-electric microphone.

Dynamic limiter (microphone) pin DLS/$\overline{\text{MMUTE}}$

A low level at the DLS/$\overline{\text{MMUTE}}$ pin inhibits the microphone inputs MIC+ and MIC− but has no influence on the receiving and DTMF amplifiers.
Removing the low level at the DLS/$\overline{\text{MMUTE}}$ pin provides the normal function of the microphone amplifier after a short time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ pin. The microphone mute function can be realised by a simple switch as shown in Fig.13.

To prevent distortion of the transmitted signal, the gain of the sending amplifier is reduced rapidly when peaks of the signal on the line exceed an internally-determined threshold. The time in which gain reduction is effected (attack time) is very short. The circuit stays in the gain-reduced condition until the peaks of the sending signal remain below the threshold level. The sending gain then returns to normal after a time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ (release time).

The internal threshold adapts automatically to the DC voltage setting of the circuit (voltage $V_{LN\text{-}SLPE}$). This means that the maximum output swing on the line will be higher if the DC voltage dropped across the circuit is increased.

Fig.14 shows the maximum possible output swing on the line as a function of the DC voltage drop ($V_{LN\text{-}SLPE}$) with $I_{line} - I_p$ as a parameter.

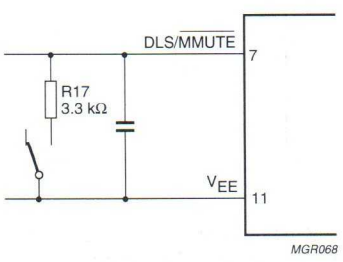


Fig.13 Microphone-mute function.

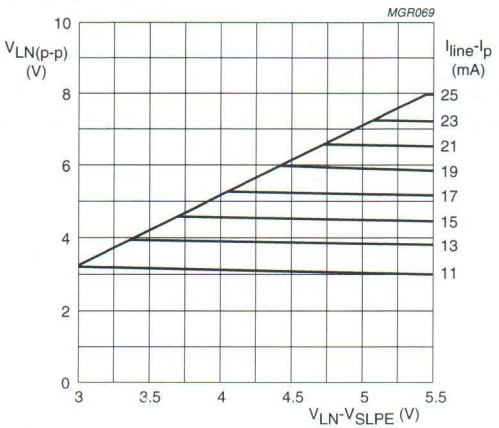


Fig.14 Maximum output swing on line as a function of the DC voltage drop $V_{LN-SLPE}$ with $I_{line} - I_p$ as a parameter: R15 = 392 Ω; R16 = 56 Ω; or R15 = 0 Ω and R16 = 392 + 56 = 448 Ω.

The internal threshold level is lowered automatically if the DC current in the transmit output stage is insufficient. This prevents distortion of the sending signal in applications using parallel-connected telephones or telephones operating over long lines, for example.

Dynamic limiting also considerably improves sidetone performance in over-drive conditions (less distortion; limited sidetone level).

Receiving amplifier IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, QR+ (non-inverting) and QR− (inverting). These outputs may be used for single-ended or differential drive, depending on the type and sensitivity of the earpiece used (see Fig.15). Gain from IR to QR+ is typically 31 dB with R4 = 100 kΩ, sufficient for low-impedance magnetic or dynamic earpieces which are suitable for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB. Differential drive can be used when the earpiece impedance exceeds 450 Ω as with high-impedance dynamic, magnetic or piezo-electric earpieces.

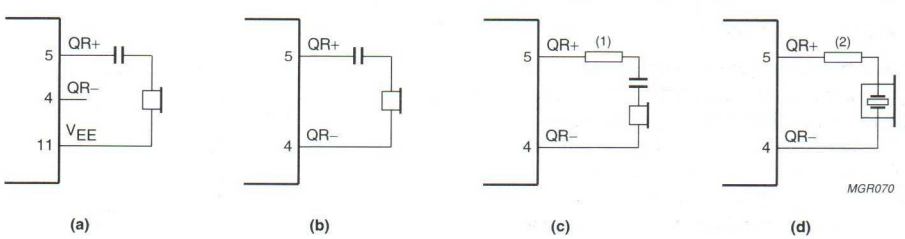
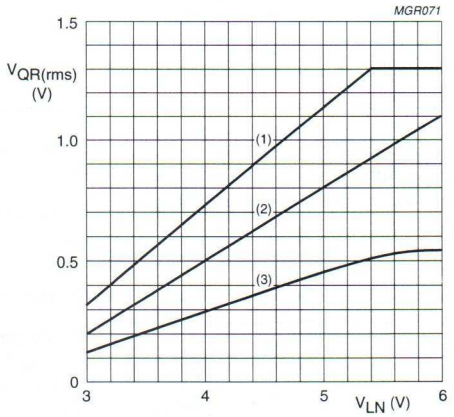


Fig.15 Alternative receiver arrangements: a) dynamic earpiece with an impedance less than 450 Ω; b) dynamic earpiece with an impedance more than 450 Ω; c) magnetic earpiece with an impedance more than 450 Ω, resistor (1) may be connected to prevent distortion (inductive load); d) piezo-electric earpiece, resistor (2) is required to increase the phase margin (stability with capacitive load).

The output voltage of the receiving amplifier is specified for continuous-wave drive. Fig.16 shows the maximum output swing of the receiving amplifier as a function of the DC voltage drop (V_{LN}). The maximum output voltage will be higher under speech conditions, where the ratio of the peak to the RMS value is higher.

The gain of the receiving amplifier can be adjusted to suit the sensitivity of the transducer used. The adjustment range is between 20 dB and 39 dB with single-ended drive and between 26 dB and 45 dB with differential drive. The gain is proportional to the external resistor R4 connected between GAR and QR+. The overall gain between LN and QR+ can be found by subtracting the attenuation of the anti-sidetone network (32 dB) from the amplifier gain.

Two external capacitors (C4 =100 pF and C7 = 10 × C4 = 1 nF) ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R4 × C4. The relationship C7 = 10 × C4 must be maintained.



Curve (1) is for a differential load of 47 nF (series resistance = 100 Ω); f = 3400 Hz.
Curve (2) is for a differential load of 450 Ω; f = 1 kHz.
Curve (3) is for a single-ended load of 150 Ω; f = 1 kHz.

Fig.16 Maximum output swing of the receiving amplifier as a function of DC voltage drop V_{LN} with the load at the receiver output as parameter: valid for both supply options; THD = 2%; I_{line} = 15 mA.

Automatic gain control input AGC

Automatic compensation of line loss is obtained by connecting a resistor (R6) between AGC and V_{EE}. This automatic gain control varies the gain of the microphone amplifier and receiving amplifier in accordance with the DC line current. The control range is 6.1 dB; this corresponds to a 5 km line of 0.5 mm diameter copper twisted-pair cable (DC resistance = 176 Ω/km, average attenuation = 1.2 dB/km). The DTMF gain is not affected by this feature.

The value of R6 must be chosen with reference to the exchange supply voltage and its feeding bridge resistance (see Fig.17 and Table 1). Different values of R6 give the same line current ratios at the start and the end of the control range. If automatic line-loss compensation is not required the AGC pin can be left open, the amplifiers then give their maximum gain.

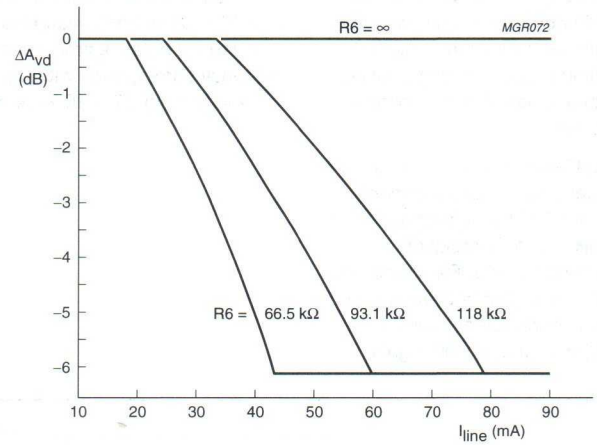


Fig.17 Variation of gain as a function of line current with R6 as a parameter; R9 = 20 Ω.

Table 1 Values of R6 giving optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	36	84.5	66.5	X	X
	48	118	93.1	77.8	66.5
	60	X	X	97.6	84.5

MUTE input (see notes 1. and 2.)

MUTE = HIGH enables the DTMF input and inhibits the microphone and receiving amplifier inputs.

MUTE = LOW or open-circuit disables the DTMF input and enables the microphone and receiving amplifier inputs.

Switching MUTE gives negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF (see note 1.)

When the DTMF input is enabled, dialling tones may be sent on to the line. The voltage gain between DTMF-SLPE and LN-V_{EE} is typ. 26 dB less than the gain of the microphone amplifier and varies with R7 in the same way as the gain of the microphone amplifier. This means that the tone level at the DTMF input has to be adjusted after setting the gain of the microphone amplifier. With R7 = 68 kΩ the gain is typically 26 dB.

The signalling tones can be heard in the earpiece at a low level (confidence tone).

Power-down input PD (see notes 1. and 2.)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted; as a consequence it provides no supply for the transmission circuit connected to V_{CC1} or for the peripherals between V_{CC2} and SLPE. These supply gaps are bridged by the charges in the capacitors C1 and C15. The requirements on these capacitors are eased by applying a HIGH level to the PD input during the time of the loop break. This reduces the internal supply current I_{CC1} from (typ.) 1.3 mA to (typ.) 60 μA and switches off the voltage regulator to prevent discharge via LN and V_{CC2}.

A HIGH level at PD also internally disconnects the capacitor at REG so that the voltage stabilizer has no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall.

When the power-down facility is not required, the PD pin can be left open-circuit or connected to SLPE.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising R1//Z_{line},

R2, R3, R8, R9 and Z_{bal} (see Fig.18). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9 \times R2 = R1 \times (R3 + [R8//Z_{bal}])$

b) $(Z_{bal}/[Z_{bal} + R8]) = (Z_{line}/[Z_{line} + R1])$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) is always fulfilled provided $|R8//Z_{bal}| << R3$.

To obtain optimum sidetone suppression, condition b) has to be fulfilled, resulting in:

$$Z_{bal} = (R8/R1) \times Z_{line} = k \times Z_{line}$$

where k is a scale factor; k = (R8/R1).

The scale factor k (value of R8) is chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal};
- $|Z_{bal}//R8| << R3$ to fulfil condition a) and thus ensure correct anti-sidetone bridge operation;
- $|Z_{bal} + R8| >> R9$ to avoid influencing the transmit gain.

In practice Z_{line} varies considerably with the line length and line type. Therefore the value chosen for Z_{bal} should be for an average line length giving satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

Example

The line impedance for which optimum suppression is to be obtained can be represented by 210 Ω + (1265 Ω // 140 nF). This represents a 5 km line of 0.5 mm diameter copper twisted-pair cable matched with 600 Ω (176 Ω/km; 38 nF/km).

With k = 0.64 this results in: R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω // 220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig.18 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Alternatively a conventional Wheatstone bridge can be used as an anti-sidetone circuit (Fig.19). Both bridge types can be used with either resistive or complex set impedances. (More information on the balancing of anti-sidetone bridges can be obtained in our publication *"Versatile speech transmission ICs for electronic telephone sets"*, order number 9398 341 10011).

Notes

1. The reference used for the MUTE, DTMF and PD inputs is SLPE.
2. A LOW level for any of these pins is defined by connection to SLPE, a HIGH level is defined as a voltage greater than V_{SLPE} + 1.5 V and smaller than V_{CC1} + 0.4 V.

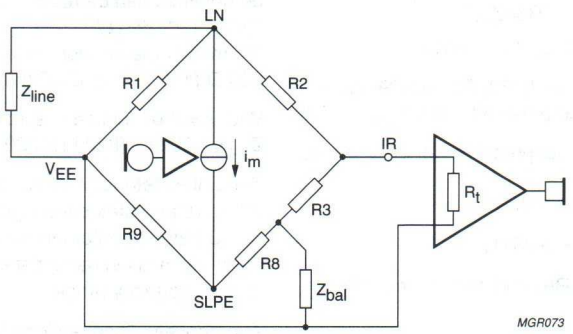


Fig.18 Equivalent circuit of TEA1060 family anti-side-tone bridge.

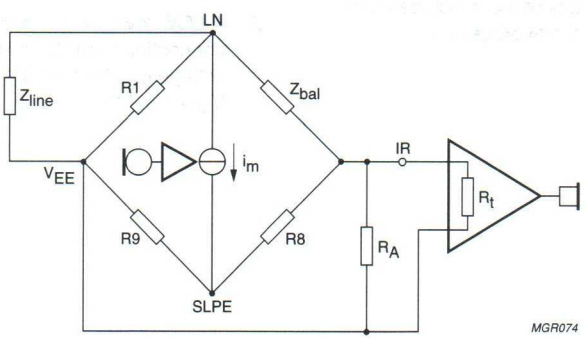


Fig.19 Equivalent circuit of an anti-sidetone network in the Wheatstone bridge configuration.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Positive line voltage continuous		V_{LN}	–	12	V
Repetitive line voltage during switch-on line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage one 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig.24)	V_{LN}	–	28	V
Line current TEA1064A (note 1)	R9 = 20 Ω	I_{LN}	–	140	mA
Line current TEA1064AT (note 1)	R9 = 20 Ω	I_{LN}	–	140	mA
Input voltage on pins other than LN and V_{CC2}		V_i	V_{EE}–0.7	V_{CC1} + 0.7	V
Total power dissipation (note 2)	R9 = 20 Ω				
TEA1064A		P_{tot}	–	714	mW
TEA1064AT		P_{tot}	–	555	mW
Storage temperature range		T_{stg}	–40	+ 125	°C
Operating ambient temperature range		T_{amb}	–25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

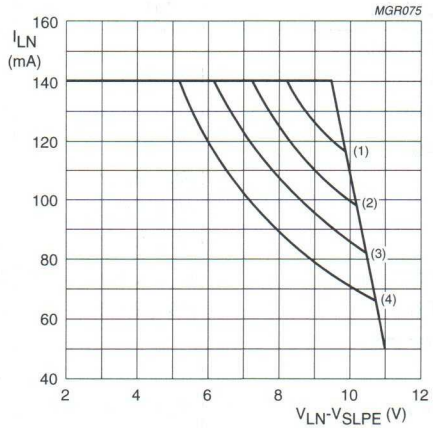
Notes

1. Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs 20 and 21 to determine the current as a function of the required voltage and the temperature.
2. Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

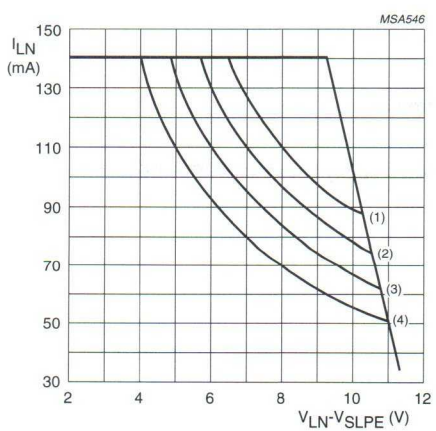
From junction to ambient in free air

TEA1064A	$R_{th\ j\text{-}a}$	=	70 K/W
TEA1064AT mounted on glass epoxy board 41 × 19 × 1.5 mm	$R_{th\ j\text{-}a}$	=	90 K/W



	T_{amb}	P_{tot}
(1)	45 °C	1143 mW
(2)	55 °C	1000 mW
(3)	65 °C	857 mW
(4)	75 °C	714 mW

Fig.20 TEA1064A safe operating area.



	T_{amb}	P_{tot}
(1)	45 °C	888 mW
(2)	55 °C	777 mW
(3)	65 °C	666 mW
(4)	75 °C	555 mW

Fig.21 TEA1064AT safe operating area.

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; R_L = 600 Ω; tested in the circuit of Fig.22 or 23); unless otherwise specified

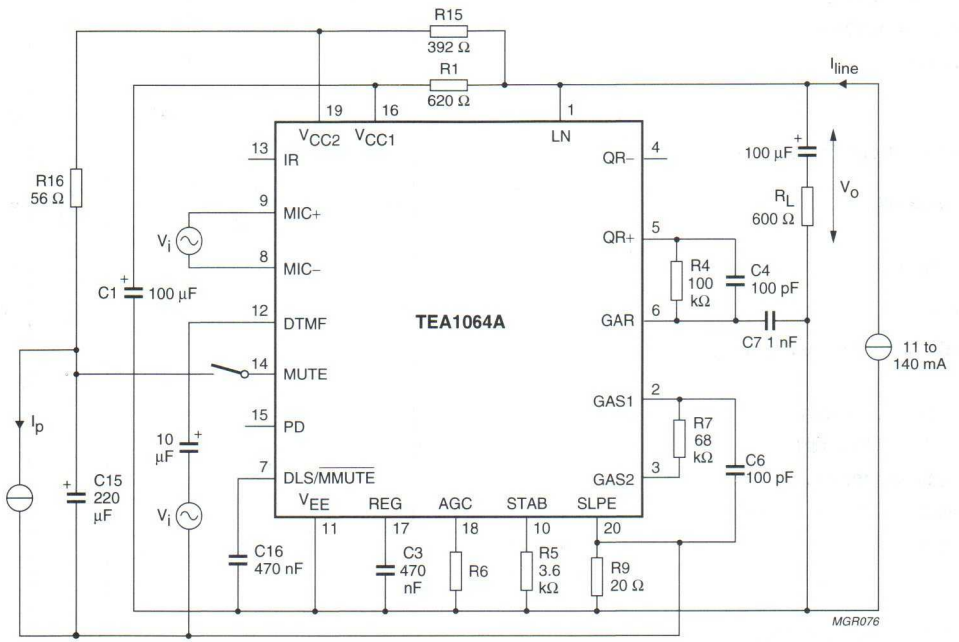
PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supplies LN, V_{CC1}, V_{CC2} (pins 1, 16, 19)						
Reference DC voltage between						
V_{CC2} and SLPE	I_{line} = 15 mA					
	I_p = 0; 4 mA					
R_{VA} not connected		$V_{CC2\text{-}SLPE}$	3.05	3.3	3.55	V
Variation with temperature	I_{line} = 15 mA	$V_{CC2\text{-}SLPE}/\Delta T$	−3.0	−1.0	1.0	mV/K
Variation with line current referred						
to 15 mA	I_{line} = 100 mA	$\Delta V_{CC2\text{-}SLPE}$	–	60	–	mV
With R_{VA} connected between						
REG and SLPE	R_{VA} = 33 kΩ	$V_{CC2\text{-}SLPE}$	3.6	3.8	4.2	V
	R_{VA} = 20 kΩ	$V_{CC2\text{-}SLPE}$	3.95	4.2	4.65	V
DC line voltage:						
voltage drop between LN and V_{EE}	MIC−, MIC+ inputs open; R15 = 392 Ω; without R_{VA}					
at I_{line} = 15 mA	I_p = 0 mA	V_{LN}	3.4	3.6	4.0	V
	I_p = 2 mA	V_{LN}	4.2	4.4	4.8	V
	I_p = 4 mA	V_{LN}	4.9	5.1	5.5	V
at I_{line} = 100 mA	I_p = 2 mA	V_{LN}	–	6.1	7.0	V
at I_{line} = 140 mA	Ip = 2 mA	V_{LN}	–	7.0	7.8	V
Voltage drop under low current						
conditions	I_p = 0 mA					
	I_{line} = 2 mA	V_{LN}	–	1.8	–	V
	I_{line} = 4 mA	V_{LN}	–	2.2	–	V
	I_{line} = 7 mA	V_{LN}	–	3.2	–	V
	I_{line} = 11 mA	V_{LN}	–	3.5	–	V
Internal supply current I_{CC1}:						
current into pin V_{CC1}	V_{CC1} = 2.8 V					
	PD = LOW	I_{CC1}	–	1.3	1.6	mA
	PD = HIGH	I_{CC1}	–	60	82	µA
Microphone inputs MIC−, MIC+ (pins 8, 9)						
Input impedance:						
differential		Z_i	51	64	77	kΩ
single-ended		Z_i	25.5	32.0	38.5	kΩ
Common mode rejection ratio		CMRR	–	82	–	dB

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Voltage gain (see Fig.22)	I_{line} = 15 mA;					
	R7 = 68 kΩ	G_v	51	52	53	dB
Variation of G_v with frequency,						
referred to 0.8 kHz	f = 300 and 3400 Hz	$\Delta G_v f$	−0.5	± 0.1	+ 0.5	dB
Variation of G_v with temperature,						
referred to 25 °C	without R6;					
	I_{line} = 50 mA;					
	T_{amb} = −25 to + 75 °C	$\Delta G_v T$	–	± 0.2	–	dB
DTMF input (pin 12)						
Input impedance		Z_i	16.8	20.7	24.6	kΩ
Voltage gain (see Fig.22)	I_{line} = 15 mA;					
	R7 = 68 kΩ	G_v	25	26	27	dB
Variation of G_v with frequency,						
referred to 0.8 kHz	f = 300 and 3400 Hz	$\Delta G_v f$	−0.5	± 0.1	+ 0.5	dB
	f = 697 and 1633 Hz	$\Delta G_v f$	−0.2	± 0.05	+ 0.2	dB
Variation of G_v with temperature,						
referred to 25 °C	I_{line} = 50 mA;					
	T_{amb} = −25 to + 75°C	$\Delta G_v T$	–	± 0.2	0.5	dB
Gain adjustment inputs GAS1, GAS2 (pins 2, 3)						
Transmitting amplifier,						
gain adjustment range		ΔG_v	−8	–	+ 0	dB
Sending amplifier output LN (pin 1)						
Dynamic limiter						
Output voltage swing						
(peak-to-peak value)	I_{line} = 15 mA;					
	R7 = 68 kΩ;					
	I_p = 0 mA;					
	$V_{i(rms)}$ = 3.6 mV	$V_{LN(p-p)}$	3.6	4.0	4.5	V
Total harmonic distortion	V_i = 3.6 mV + 10 dB	THD	–	1.5	2.0	%
	V_i = 3.6 mV + 15 dB	THD	–	2.8	10.0	%
Output voltage swing						
(peak-to-peak value)	V_i = 3.6 mV + 10 dB					
	I_p = 2 mA	$V_{LN(p-p)}$	3.7	3.95	4.2	V
	I_p = 4 mA	$V_{LN(p-p)}$	3.0	3.25	3.5	V
	I_p = 0 mA;					
	I_{line} = 7 mA	$V_{LN(p-p)}$	–	2	–	V
	I_p = 0 mA;					
	I_{line} = 4 mA	$V_{LN(p-p)}$	–	1	–	V

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Dynamic behaviour of limiter	C16 = 470 nF					
attack time, V_{mic} jumps from 2 mV to 40 mV		t_{att}	–	1.5	5.0	ms
release time, V_{mic} jumps from 40 mV to 2 mV		t_{rel}	50	150	–	ms
Noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–72	–	dBmp
Receiving amplifier input IR (pin 13)						
Input impedance		Z_i	17	21	25	kΩ
Receiving amplifier outputs QR– QR+ (pins 4, 5)						
Output impedance	single-ended	Z_o	–	4	–	Ω
Voltage gain	Fig.23; I_{line} = 15 mA; R4 = 100 kΩ					
single-ended; R_T = 300 Ω		G_v	30	31	32	dB
differential; R_T = 600 Ω		G_v	36	37	38	dB
Variation with frequency, referred to 0.8 kHz	f = 300 and 3400 Hz	$\Delta G_v f$	–0.5	–0.2	0	dB
Variation with temperature, referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 to +75 °C	$\Delta G_v T$	–	± 0.2	–	dB
Output voltage (RMS value)	THD = 2%; sinewave drive; R4 = 100 kΩ; I_{line} = 15 mA					
single-ended; R_T = 150 Ω	I_p = 0 mA	$V_{o(rms)}$	–	0.22	–	V
	I_p = 2 mA	$V_{o(rms)}$	–	0.35	–	V
differential; R_T = 450 Ω	I_p = 0 mA	$V_{o(rms)}$	–	0.39	–	V
	I_p = 2 mA	$V_{o(rms)}$	–	0.64	–	V
differential; C_T = 47 nF; (100 Ω series resistor); f = 3400 Hz	I_p = 0 mA	$V_{o(rms)}$	–	0.57	–	V
	I_p = 2 mA	$V_{o(rms)}$	–	0.9	–	V

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Output voltage (RMS value)	I_p = 0 mA; THD = 10%; sinewave drive; R4 = 100 kΩ; single-ended; R_T = 150 Ω;					
	I_{line} = 4 mA	$V_{o(rms)}$	–	25	–	mV
	I_{line} = 7 mA	$V_{o(rms)}$	–	160	–	mV
Noise output voltage (RMS value)	I_{line} = 15 mA; R_4 = 100 kΩ; psophometrically weighted (P53 curve); pin IR open single-ended;					
	R_T = 300 Ω;	$V_{no(rms)}$	–	45	–	μV
	differential;					
	R_T = 600 Ω	$V_{no(rms)}$	–	90	–	μV
Noise output voltage (RMS value)	in circuit of Fig.23; S1 in position 2; 200 Ω between MIC+ and MIC–; single-ended;					
	R_T = 300 Ω					
	R_7 = 68 kΩ	$V_{no(rms)}$	–	100	–	μV
	R_7 = 24.9 kΩ	$V_{no(rms)}$	–	65	–	μV
Gain adjustment input GAR (pin 6)						
Receiving amplifier, gain adjustment range		ΔG_v	–11	–	+8	dB
MUTE INPUT (pin 14)						
Input voltage HIGH		V_{IH}	1.5 + V_{SLPE}	–	V_{CC1} + 0.4	V
Input voltage LOW		V_{IL}	0	–	0.3 + V_{SLPE}	V
Input current		I_{mute}	–	11	20	μA
Change of microphone amplifier gain at mute-ON	MUTE = HIGH	$-\Delta G_v$	–	100	–	dB

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Voltage gain from input DTMF-SLPE to QR+ output with mute-ON	MUTE = HIGH; single-ended load; R_L = 300 Ω	G_v	–	−18	–	dB
Power-down input PD (pin 15)						
Input voltage HIGH		V_{IH}	1.5 + V_{SLPE}	–	V_{CC1} + 0.4	V
Input voltage LOW		V_{IL}	0	–	0.3 + V_{SLPE}	V
Input current		I_{PD}	–	5	10	μA
Automatic gain control input AGC (pin 18)						
Controlling the gain from IR (pin 13) to QR+, QR− (pins 4, 5) and the gain from MIC+, MIC− (pins 8, 9) to LN (pin 1)	R6 = 93.1 kΩ (between pins 18 and 11)					
gain control range with respect to I_{line} = 15 mA	I_{line} = 75 mA	$-G_v$	5.7	6.1	6.5	dB
Highest line current for maximum gain		I_{line}	–	24	–	mA
Lowest line current for minimum gain		I_{line}	–	61	–	mA
Change of gain between I_{line} = 15 and 35 mA		$-\Delta G_v$	0.9	1.4	1.9	dB
Microphone mute input DLS/$\overline{\text{MMUTE}}$ (pin 7)						
Input voltage low		V_{IL}	V_{EE}	–	V_{EE} + 0.3	V
Input current at low input voltage		I_{IL}	−85	−60	−35	μA
Release time after a low level on pin 7	C16 = 470 nF	t_{rel}	–	30	–	ms
Change of microphone amplifier gain at low input voltage on pin 7		$-\Delta G_v$	–	100	–	dB



For measuring the gain from MIC+ and MIC− the MUTE input should be LOW or open-circuit; for measuring the DTMF input, the MUTE input should be HIGH. Inputs not being tested should be open-circuit.

Fig.22 Test circuit for defining voltage gain of MIC−, MIC+ and DTMF inputs; voltage gain (G_v) is defined as $20 \log |V_o / V_i|$.

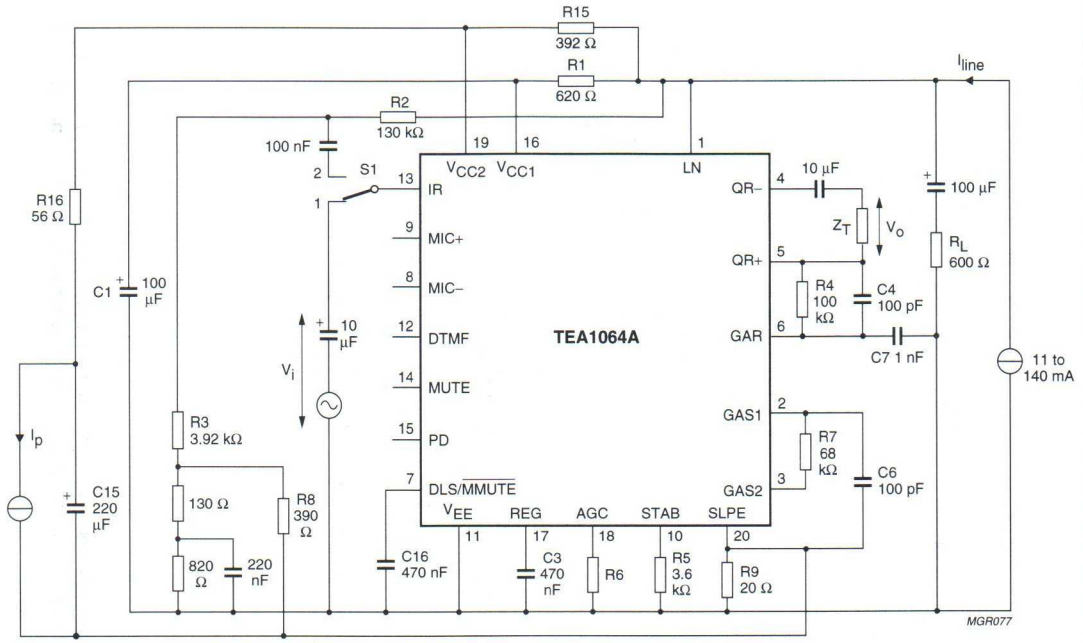


Fig.23 Test circuit for defining voltage gain of the receiving amplifier, voltage gain (G_v) is defined as $20 \log |V_o / V_i|$ (with S1 in position 1).

APPLICATION INFORMATION

The basic application circuit is shown in Fig.24 and some typical applications are shown in Figs 25, 26 and 27.

In the basic application, the circuit provides two possibilities for supplies to peripheral circuits:

- regulated line voltage V_{LN} (stabilized $V_{LN\text{-}SLPE}$) and unregulated supply voltage for peripheral circuits, the supply voltage is dependent only on the peripheral supply current. This application is the same as that used for TEA1060/TEA1061, TEA1067 and TEA1068;
- stabilized supply voltage for peripherals ($V_{CC2\text{-}SLPE}$), the DC line voltage depends on the current flowing to the peripheral circuits.

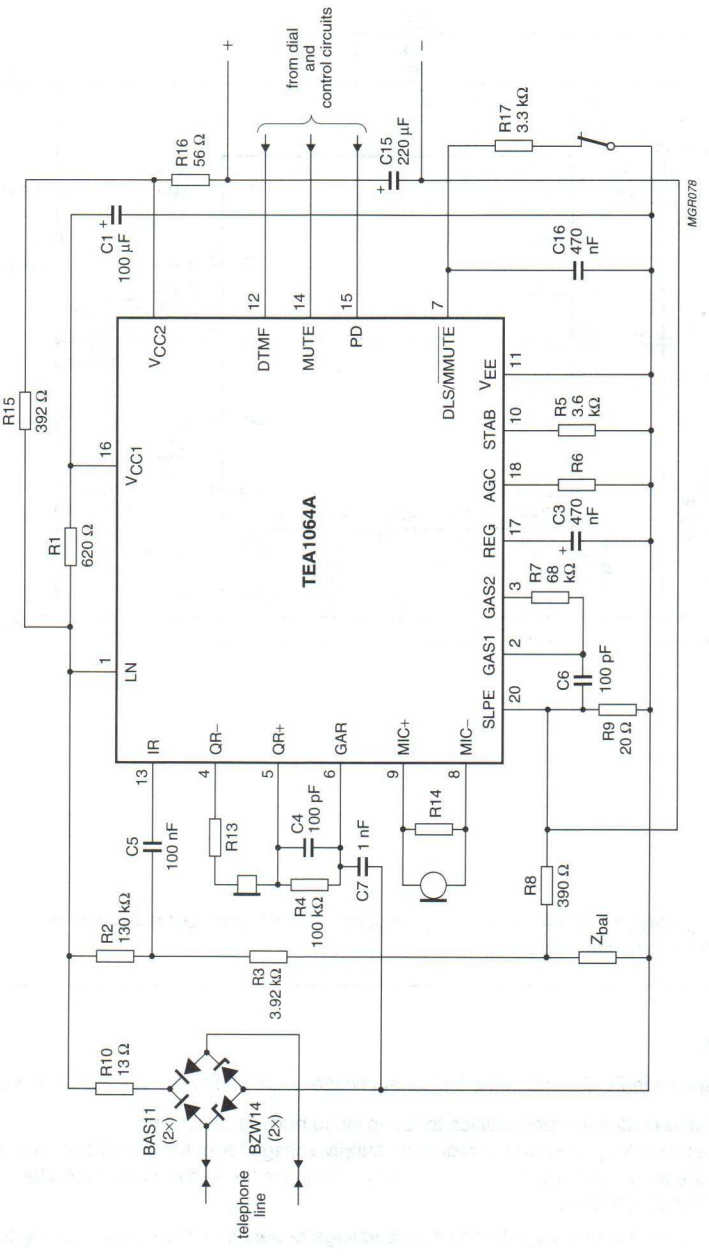


Fig.24 Basic application of the TEA1064A with stabilized supply for peripherals, shown here with a piezo-electric earpiece and DTMF dialling. The diode bridge and R10 limit the current into, and the voltage across, the circuit during line transients. A different protection arrangement is required for pulse dialling or register recall.

For the basic application giving regulated line voltage the above circuit is changed as follows:

- R15 must be short-circuited;
- the value of R16 is changed to 392 Ω;
- the value of C3 is changed to 4.7 μF.

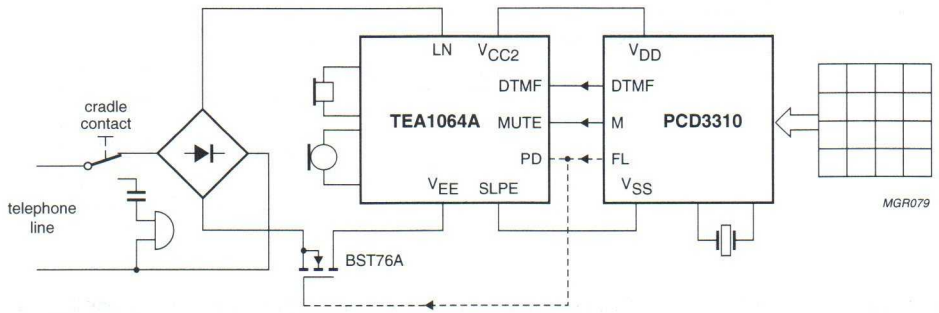


Fig.25 Typical DTMF-pulse set application circuit (simplified) showing the TEA1064A with the CMOS bilingual dialling circuit PCD3310; the broken line indicates optional flash (register recall by timed loop break).

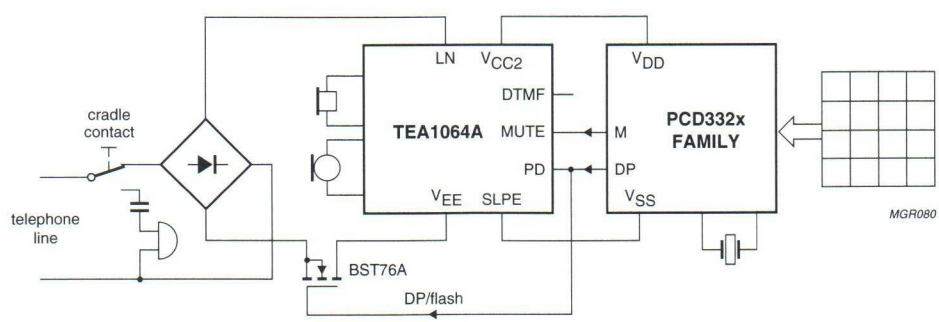


Fig.26 Typical pulse dial set application circuit (simplified) showing the TEA1064A with one of the PCD332X family of CMOS interrupted current-loop dialling circuits.

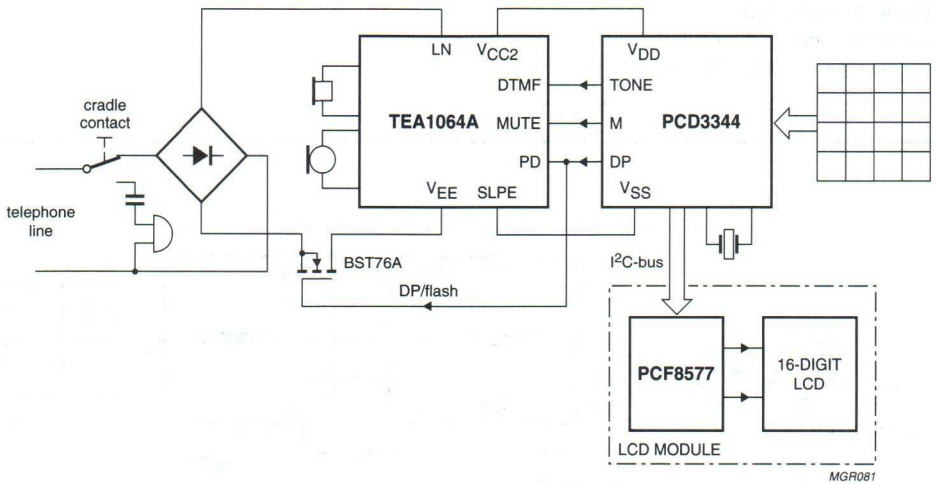


Fig.27 Typical dual-standard (pulse and DTMF) feature phone application circuit (simplified) showing the TEA1064A and the PCD3344 CMOS telephone microcontroller with on-chip DTMF generator plus I²C-bus.

Low voltage versatile telephone transmission circuit with dialler interface and transmit level dynamic limiting

TEA1064B

FEATURES

- Low DC line voltage; operates down to 1.8 V (excluding polarity guard)
- Voltage regulator with low voltage drop and adjustable static resistance
- DC line voltage adjustment facility
- Provides a supply for external circuits
- Dynamic limiting (speech-controlled) in transmit direction prevents distortion of line signal and sidetone
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- DTMF signal input
- Confidence tone in the earpiece during DTMF dialling
- Mute input for disabling speech during pulse or DTMF dialling
- Power-down input for improved performance during pulse dial or register recall (flash)
- Receiving amplifier for dynamic, magnetic or piezo-electric earpieces
- Large amplification setting ranges on microphone and earpiece amplifiers
- Line loss compensation (line current dependent) for microphone and earpiece amplifiers (not used for DTMF amplifier)
- Gain control curve adaptable to exchange supply
- Automatic disabling of the DTMF amplifier in extremely-low voltage conditions
- Microphone MUTE function available with switch
- MUTE, POWER-DOWN and DTMF input reference (pin V_{EE2}) can be connected either to V_{EE1} or SLPE.

GENERAL DESCRIPTION

The TEA1064B is a bipolar integrated circuit that performs all the speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech. The IC operates at line voltages down to 1.8 V DC (with reduced performance) to facilitate the use of more telephone sets connected in parallel. The transmit signal on the line is dynamically limited (speech-controlled) to prevent distortion at high transmit levels of both the sending signal and the sidetone.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1064B	20	DIL	plastic	SOT146[1]
TEA1064BT	20	mini-pack	plastic	SO20; SOT163A[2]

Notes

1. SOT146-1; 1998 Jun 18.
2. SOT163-1; 1998 Jun 18.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range					
	normal operation	note 1	11	–	140	mA
	with reduced performance		2	–	11	mA
I_{CC}	internal supply current	V_{CC} = 2.8 V				
	power-down input LOW		–	1.3	1.6	mA
	power-down input HIGH		–	60	82	µA
G_v	voltage gain range					
	microphone amplifier		44	–	52	dB
	receiving amplifier		20	–	45	dB
	line loss compensation ranges					
G_v	gain control		5.7	6.1	6.5	dB
V_{exch}	exchange supply voltage		36	–	60	V
R_{exch}	exchange feeding bridge resistance		400	–	1000	Ω
$V_{LN(p-p)}$	maximum output voltage swing on LN (peak-to-peak value)	R16 = 392 Ω; I_{line} = 15 mA				
		I_p = 1.4 mA	3.55	3.80	4.05	V
		I_p = 2.7 mA	3.25	3.50	3.75	V
V_p	supply for peripherals	I_{line} = 15 mA				
		I_p = 1.4 mA	2.5	2.7	–	V
		I_p = 2.7 mA; $R_{REG-SLPE}$ = 20 kΩ	2.9	3.1	–	V
V_{LN}	DC line voltage	I_{line} = 15 mA				
		without $R_{REG-SLPE}$	3.25	3.5	3.75	V
		$R_{REG-SLPE}$ = 20 kΩ	4.05	4.4	4.75	V
T_{amb}	operating ambient temperature range		–25	–	+75	°C

Note

1. For the TEA1064BT the maximum line current depends on the heat dissipating qualities of the mounted device.

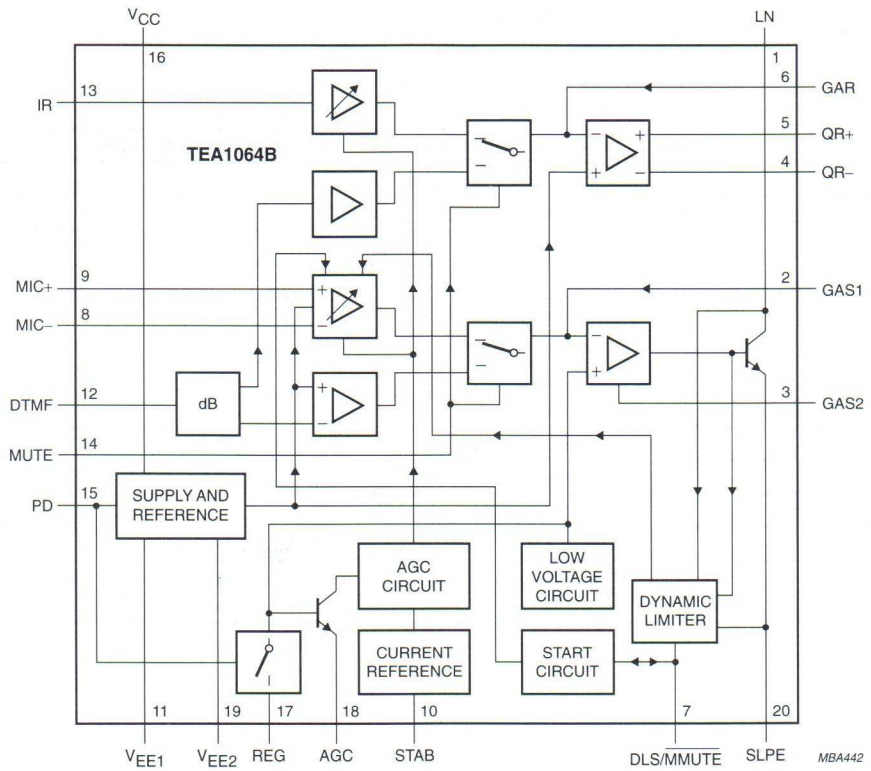


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
GAS1	2	gain adjustment; transmitting amplifier
GAS2	3	gain adjustment; transmitting amplifier
QR–	4	inverting output; receiving amplifier
QR+	5	non-inverting output; receiving amplifier
GAR	6	gain adjustment; receiving amplifier
DLS/$\overline{\text{MMUTE}}$	7	decoupling for transmit amplifier dynamic and microphone MUTE input
MIC–	8	inverting microphone input
MIC+	9	non-inverting microphone input
STAB	10	current stabilizer
V_{EE1}	11	negative line terminal
DTMF	12	dual-tone multi-frequency input
IR	13	receiving amplifier input
MUTE	14	mute input
PD	15	power-down input
V_{CC}	16	internal supply decoupling
REG	17	voltage regulator decoupling
AGC	18	automatic gain control input
V_{EE2}	19	reference for POWER-DOWN (PD), MUTE and DTMF
SLPE	20	slope adjustment for DC curve/reference for peripheral circuits

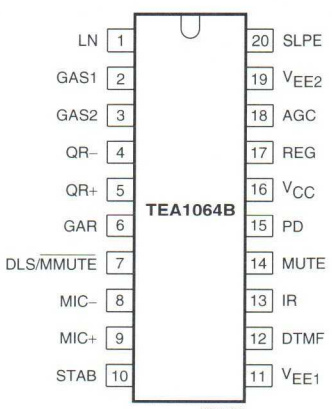


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Supplies V_{CC}, V_{EE2}, LN, SLPE, REG and STAB (Figs 3 and 5)

Power for the TEA1064B and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply voltage at V_{CC} and regulates its voltage drop. The internal supply requires a decoupling capacitor between V_{CC} and V_{EE1}. The internal current stabilizer is set by a 3.6 kΩ resistor between STAB and V_{EE1}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the subscriber line DC resistance R_{line} and the DC voltage (including polarity guard) on the subscriber set (see Fig.3).

The internal voltage regulator generates a temperature-compensated reference voltage that is available between LN and SLPE ($V_{ref} = V_{LN-SLPE} = 3.23$ V typ.). This internal voltage regulator requires decoupling by a capacitor between REG and V_{EE1} (C3).

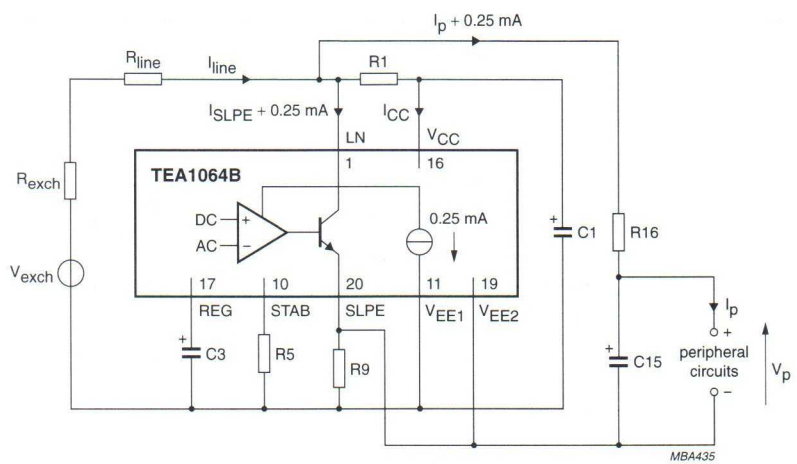
The configuration shown in Fig.3, gives a stabilized voltage across pins LN and SLPE which, applied via the low-pass filter R16, C15, provides a supply to the peripherals that is independant of the line current and depends only on the peripheral supply current.

The value of R16 and the level of the DC voltage $V_{LN-SLPE}$ determine the supply capabilities. In the basic application R16 = 392 Ω and C15 = 220 µF. The worst-case peripheral supply current as a function of supply voltage is shown in Fig.4.

To increase the supply capabilities, the value of R16 can be decreased or the DC voltage $V_{LN-SLPE}$ can be increased by using $R_{VA(REG-SLPE)}$.

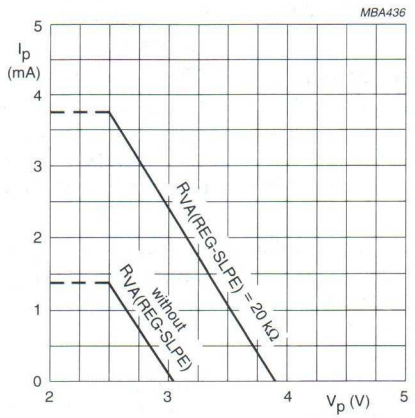
Note

The TEA1064B application is the same as is used for TEA1060/TEA1061, TEA1067 and TEA1068 integrated circuits.



The voltage $V_{LN-SLPE}$ is fixed to $V_{ref} = 3.323 \pm 0.25$ V.
Resistor R16 together with the line current determine the supply capabilities and the maximum output swing on the line (no loop damping is necessary).
The line voltage $V_{LN} = V_{ref} + (\{I_{line} - 1.55\ mA\} \times R9)$.

Fig.3 Supply arrangement with reference to SLPE.



I_{line} = 15 mA; R16 = 392 Ω; valid for MUTE = 0 and 1.
Line current has very little influence.

Fig.4 Maximum supply current with respect to Fig.3 for peripherals (I_p) as a function of the peripheral supply voltage (V_p).

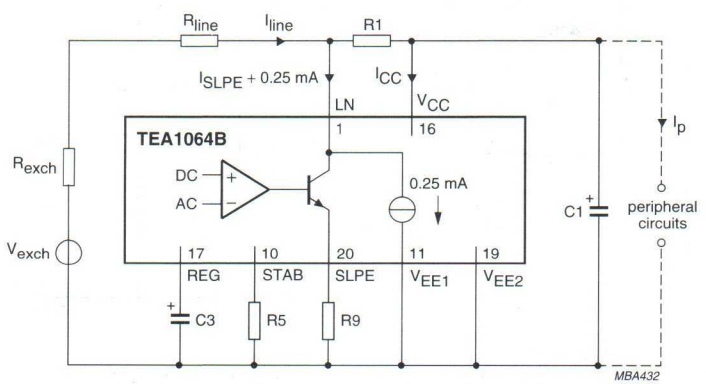
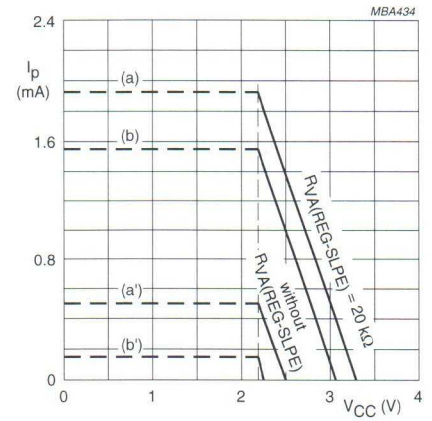


Fig.5 Supply arrangement with reference to V_{EE1}.



(a) I_p = 1.94 mA
(b) I_p = 1.54 mA
(a') I_p = 0.54 mA
(b') I_p = 0.16 mA
I_{line} = 15 mA
R1 = 620 Ω and R9 = 20 Ω
Curve (a) and (a') are valid when the receiving amplifier is not driven or when MUTE = HIGH.
Curve (b) and (b') are valid when the receiving amplifier is driven and when MUTE = LOW.
$V_{o(RMS)}$ = 150 mV, R_T = 150 Ω.

Fig.6 Maximum current I_p with respect to Fig.5 available from V_{cc} for peripheral circuitry with V_{CC} > 2.2 V.

The maximum AC output swing on the line at low currents is influenced by R16 (limited by current) and the maximum output swing on the line at high currents is influenced by DC voltage $V_{LN-SLPE}$ (limited by voltage). In both these situations, the internal dynamic limiter in the sending channel prevents distortion when the microphone is overdriven. The maximum AC output swing on LN is shown in Fig.7; practical values for R16 are from 200 Ω to 600 Ω and this influences both maximum output swing at low line currents and the supply capabilities.

When the SLPE pin is the reference for peripheral circuits, inputs MUTE, PD and DTMF must be referenced to SLPE. This is achieved by connecting pin V_{EE2} to pin SLPE; V_{EE2} being the reference of MUTE, PD and DTMF input stages.

Active microphones can be supplied between V_{CC} and V_{EE1} as shown in Fig.5. Low power circuits that provide MUTE, PD and DTMF inputs to the TEA1064B can also be powered from V_{CC} (see Fig.6 for the supply capability of V_{CC}). MUTE, PD and DTMF are then referenced to V_{EE1} and the pin V_{EE2} must therefore be connected to V_{EE1}.

If the line current I_{line} exceeds I_{CC} + 0.25 mA, the voltage converter shunts the excess current to SLPE via LN; where $I_{CC} \approx$ 1.3 mA, the value required by the IC for normal operation.

The DC line voltage on LN is:

- $V_{LN} = V_{LN-SLPE} + (I_{SLPE} \times R9)$
- $V_{LN} = V_{ref} + (\{I_{line} - I_{CC} - 0.25 \times 10^{-3}\ A\} \times R9)$

in which:

- V_{ref} = 3.23 V ± 0.25 V is the internal reference voltage between LN and SLPE; its value can be adjusted by external resistor R_{VA}.
- R9 = external resistor between SLPE and V_{EE1} (20 Ω in basic operation).

With R9 = 20 Ω, this results in:

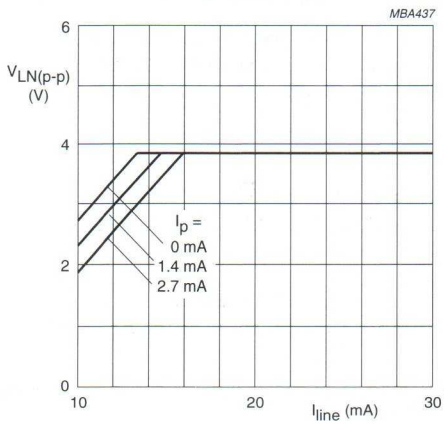
- V_{LN} = 3.3 ± 0.25 V at I_{line} = 15 mA
- V_{LN} = 4.1 ± 0.3 V at I_{line} = 15 mA, $R_{VA(REG-SLPE)}$ = 33 kΩ
- V_{LN} = 4.4 ± 0.35 V at I_{line} = 15mA, $R_{VA(REG-SLPE)}$ = 20 kΩ

The preferred value for R9 is 20 Ω. Changing R9 influences microphone gain, DTMF gain, the gain control characteristics, sidetone and the DC characteristics (especially the low voltage characteristics).

In normal conditions, $I_{SLPE} >> (I_{CC} + 0.25\ mA)$ and the static behaviour is equivalent to a voltage regulator diode with an internal resistance of R9. In the audio frequency range the dynamic impedance is determined mainly by R1. The equivalent impedance of the circuit in audio frequency range is shown in Fig.8.

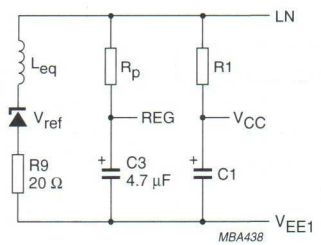
The internal reference voltage $V_{LN-SLPE}$ can be increased by external resistor $R_{VA(REG-SLPE)}$ connected between REG and SLPE. The voltage $V_{LN-SLPE}$ is shown as a function of $R_{VA(REG-SLPE)}$ in Fig.9. Changing the reference voltage influences the output swing of both sending and receiving amplifiers.

At line currents below 8 mA (typ.), the DC voltage dropped across the circuit is adjusted to a lower level automatically (approximately 1.8 V at 2 mA). This gives the possibility of operating more telephone sets in parallel with DC line voltages (excluding polarity guard) down to an absolute minimum of 1.8 V. At line currents below 8 mA (typ.), the circuit has limited sending and receiving levels.



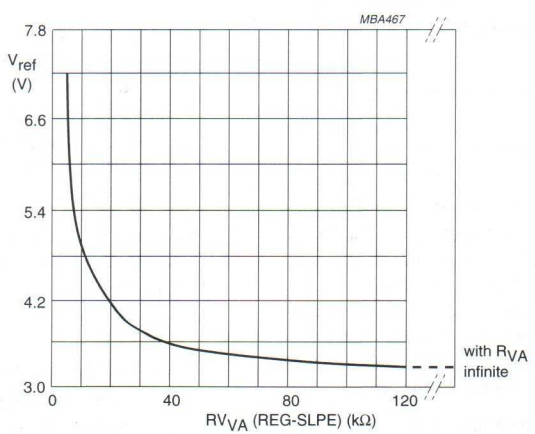
R16 = 392 Ω; I_p with respect to Fig.3.

Fig.7 Typical AC output swing at total harmonic distortion (THD) = 2% on the line as a function of line current with peripheral supply current as a parameter.



$L_{eq} = C3 \times R9 \times R_p$
R_p = 15 kΩ

Fig.8 Equivalent impedance between LN and V_{EE}.



$V_{LN} = V_{LN\text{-}SLPE} + (\{I_{line} - 1.55 \times 10^{-3}\ A\} \times R9)$.

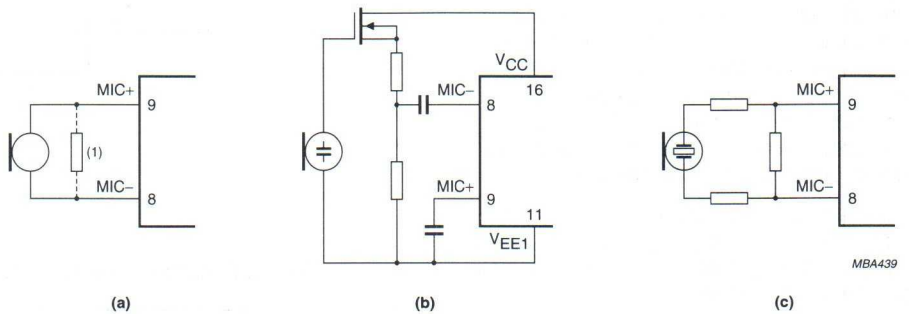
Fig.9 Internal reference voltage $V_{LN\text{-}SLPE}$ as a function of resistor $R_{VA(REG\text{-}SLPE)}$ for line currents between 11 mA and 140 mA.

Microphone inputs MIC+ and MIC− and gain pins GAS1 and GAS2

The TEA1064B has symmetrical microphone inputs, its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage amplification is typically 52 dB with R7 = 68 kΩ. Either dynamic, magnetic or piezo-electric microphones can be used, or an electret microphone with a built-in FET buffer. Arrangements for the microphone types are shown in Fig.10.

The gain of the microphone amplifier is proportional to external resistor R7 connected between GAS1 and GAS2 and with this it can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer.

An external 100 pF capacitor (C6) is required between GAS1 and SLPE to ensure stability. A larger value of C6 may be chosen to obtain a first-order low-pass filter with a cut-off frequency corresponding to the time constant R7 x C6.



Resistor (1) may be connected to reduce the terminating impedance, or for sensitive types a resistive attenuator can be used to prevent overloading the microphone inputs.

Fig.10 Microphone arrangements (a) magnetic or dynamic microphone (b) electret microphone (c) piezo-electric microphone currents.

Dynamic limiter (microphone) pin DLS/$\overline{\text{MMUTE}}$

A low level at the DLS/$\overline{\text{MMUTE}}$ pin inhibits the microphone inputs MIC+ and MIC– but has no influence on the receiving and DTMF amplifiers.

Removing the low level at the DLS/$\overline{\text{MMUTE}}$ pin provides the normal function of the microphone amplifier after a short time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ pin. The microphone mute function can be realised by a simple switch as shown in Fig.11.

To prevent distortion of the transmitted signal, the gain of the sending amplifier is reduced rapidly when peaks of the signal on the line exceed an internally-determined threshold. The time in which gain reduction is effected (attack time) is very short. The circuit stays in the gain-reduced condition until the peaks of the sending signal remain below the threshold level. The sending gain then returns to normal after a a time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ (release time).

The internal threshold adapts automatically to the DC voltage setting of the circuit ($V_{LN-SLPE}$). This means that the maximum output swing on the line will be higher if the DC voltage dropped across the circuit is increased. Fig.12 shows the maximum possible output swing on the line as a function of the DC voltage drop ($V_{LN-SLPE}$) with $I_{line} - I_p$ as a parameter.

The internal threshold level is lowered automatically if the DC current in the transmit output stage is insufficient. This prevents distortion of the sending signal in applications using parallel-connected telephones or telephones operating over long lines, for example.

Dynamic limiting also considerably improves sidetone performance in over-drive conditions (less distortion; limited sidetone level).

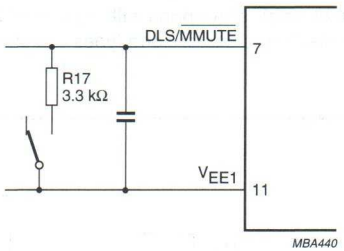
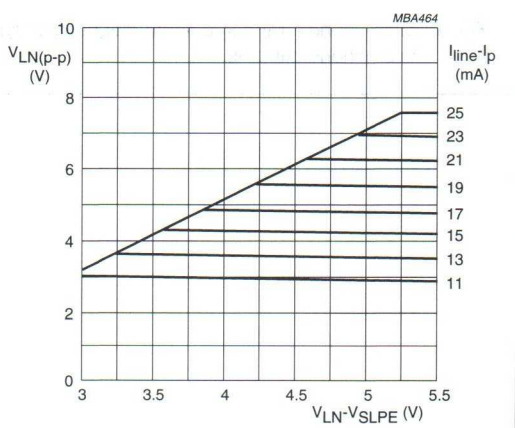


Fig.11 Microphone-mute function.

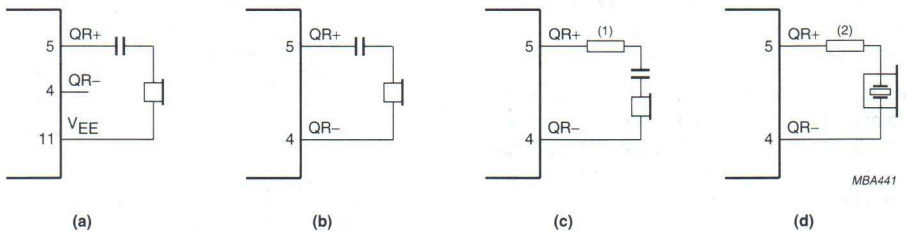


R16 = 392 Ω.

Fig.12 Typical output swing on line as a function of the DC voltage drop $V_{LN-SLPE}$ with $I_{line} - I_p$ as a parameter.

Receiving amplifier IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complimentary outputs, QR+ (non-inverting) and QR− (inverting). These outputs may be used for single-ended or differential drive, depending on the type and sensitivity of the earpiece used (see Fig.13). Gain from IR to QR+ is typically 31 dB with R4 = 100 kΩ, sufficient for low-impedance magnetic or dynamic earpieces which are suitable for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB. Differential drive can be used when the earpiece impedance exceeds 450 Ω as with high-impedance dynamic, magnetic or piezo-electric earpieces.



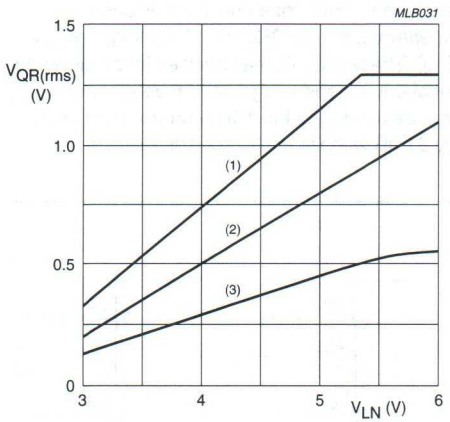
Resistor (1) may be connected to prevent distortion (inductive load).
Resistor (2) is required to increase the phase margin (stability with capacitive load).

Fig.13 Alternative receiver arrangements (a) dynamic earpiece with an impedance less than 450 Ω
(b) dynamic earpiece with an impedance more than 450 Ω
(c) magnetic earpiece with an impedance more than 450 Ω
(d) piezo-electric earpiece.

The output voltage of the receiving amplifier is specified for continuous-wave drive. Fig.14 shows the maximum output swing of the receiving amplifier as a function of the DC voltage drop (V_{LN}). The maximum output voltage will be higher under speech conditions, where the ratio of the peak to the RMS value is higher.

The gain of the receiving amplifier can be adjusted to suit the sensitivity of the transducer used. The adjustment range is between 20 dB and 39 dB with single-ended drive and between 26 dB and 45 dB with differential drive. The gain is proportional to the external resistor R4 connected between GAR and QR+. The overall gain between LN and QR+ can be found by subtracting the attenuation of the anti-sidetone network (32 dB) from the amplifier gain.

Two external capacitors (C4 = 100 pF and C7 = 10 x C4 = 1 nF) ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with time constant R4 x C4. The relationship C7 = 10 x C4 must be maintained.



Valid for both options; THD = 2%, I_{line} = 15 mA.
Curve (1) is for a differential load of 47 nf (series resistance = 100 Ω; f = 3400 Hz.
Curve (2) is for a differential load of 450 Ω; f = 1 kHz.
Curve (3) is for a single-ended load of 150 Ω; f = 1 kHz.

Fig.14 Typical output swing of the receiving amplifier as a function of DC voltage drop V_{LN} with the load at the receiver output as parameter.

Automatic gain control input AGC

Automatic compensation of line loss is obtained by connecting a resistor (R6) between AGC and V_{EE1}.

This automatic gain control varies the gain of the microphone amplifier and receiving amplifier in accordance with the DC line current. The control range is 6.1 dB; this corresponds to a 5 km line of 0.5 dB diameter copper twisted-pair cable (DC resistance = 176 Ω/km, average attenuation = 1.2 dB/km). The DTMF gain is not affected by this feature.

The value of R6 must be chosen with reference to the exchange supply voltage and its feeding bridge resistance (see Fig.15 and Table 1). Different values of R6 give the same line current ratios at the start and the end of the control range. If automatic line-loss compensation is not required the AGC pin can be left open-circuit, the amplifiers then provide their maximum gain.

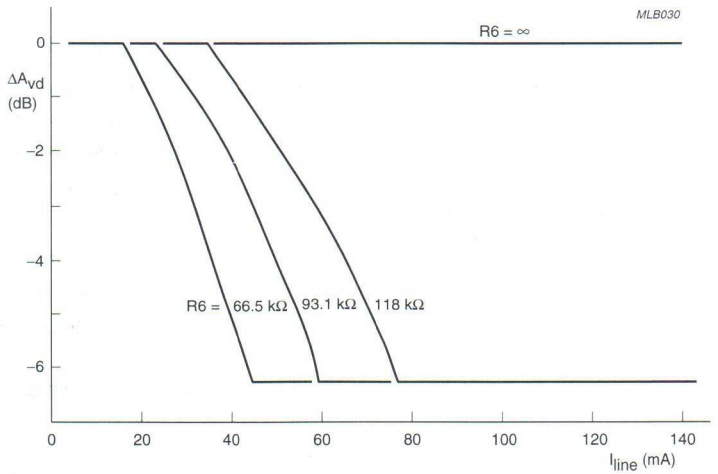


Fig.15 Variation of gain as a function of line current with R6 as a parameter; R9 = 20 Ω.

Table 1 Values of R6 giving optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	35	84.5	66.5	x	x
	48	118	93.1	77.8	66.5
	60	x	x	97.6	84.5

V_{EE2} input

V_{EE2} is the reference for MUTE, POWER-DOWN and DTMF inputs. These signals are referenced to V_{EE1} when generated by peripherals powered between V_{CC} and V_{EE1}, but they can also be referenced to SLPE when peripherals are powered as shown in Fig.3. In the first instance (reference to V_{EE1}), V_{EE2} has to be connected to V_{EE1}. In the second instance (reference to SLPE), V_{EE2} has to be connected to SLPE.

MUTE input (see notes 1 and 2)

MUTE = HIGH enables the DTMF input and inhibits the microphone and receiving amplifier inputs.

MUTE = LOW or open-circuit disables the DTMF input and enables the microphone and receiving amplifier inputs.

Switching MUTE gives negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF (see note 1)

When the DTMF input is enabled, dialling tones may be sent on the line. The voltage gain between DTMF-V_{EE2} and LN-V_{EE1} is typically 26.5 dB less than the gain of the microphone amplifier and varies with R7 in the same way as the gain of the microphone amplifier. This means that the tone level at the DTMF input has to be adjusted after setting the gain of the microphone amplifier.

With R7 = 68 kΩ the gain is typically 25.5 dB.

The signalling tones can be heard in the earpiece at a low level (confidence tone).

Power-down input PD (see notes 1. and 2.)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted; as a consequence it provides no supply for the transmission circuit connected to V_{CC} or for the peripherals between V_{LN} and SLPE.

These supply gaps are bridged by the charges in the capacitors C1 and C15. The requirements on these capacitors are eased by an applied HIGH level to the PD input during the time of the loop break. This reduces the internal supply current I_{CC1} from 1.3 mA (typ.) to 60 μA (typ.) and switches off the voltage regulator to prevent discharge via LN to V_{CC2}.

A HIGH level at PD also internally disconnects the capacitor at REG so that the voltage stabilizer has no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall.

When the power-down facility is not required, the PD pin can be left open-circuit or connected to V_{EE2}.

Sidetone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising R1//Z_{line}, R2, R3, R8, R9 and Z_{bal} (see Fig.16). Maximum compensation is obtained when the following conditions are fulfilled:

(a) $R9 \times R2 = R1 \times (R3 + \{R8//Z_{bal}\})$

(b) $(Z_{bal}/\{Z_{bal} + R8\}) = (Z_{line}/\{Z_{line} + R1\})$

If fixed values are chosen for R1, R2, R3 and R9, then condition (a) is always fulfilled provided $|R8//Z_{bal}| << R3$

To obtain optimum sidetone suppression, condition (b) has to be fulfilled, resulting in:

$$Z_{bal} = (R8/R1) \times Z_{line} = k \times Z_{line}$$

Where k is a scale factor; k = (R8/R1).

The scale factor k (value of R8) is chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| << R3$ to fulfil condition (a) and thus ensure correct anti-sidetone bridge operation
- $|Z_{bal} + R8| >> R9$ to avoid influencing the transmit gain

In practise Z_{line} varies considerably with the line length and line type. Therefore the value chosen for Z_{bal} should be for an average line length giving satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

EXAMPLE

The line impedance for which optimum suppression is to be obtained can be represented by 210 Ω + (1265 Ω //140 nF). This represents a 5 km line of 0.5 mm diameter copper twisted-pair cable matched with 600 Ω (176 Ω/km; 38 nF/km).

With k = 0.64 this results in : R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig.16 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Alternatively a conventional Wheatstone bridge can be used as an anti-sidetone circuit (see Fig.17). Both bridge types can be used with either resistive or complex set impedances. (More information on the balancing of anti-sidetone bridges can be obtained in our publication *"Versatile speech transmission ICs for electronic telephone sets"*, order number 9398 341 10011).

Notes

1. The reference level used for the MUTE, DTMF and PD inputs is V_{EE2}.
2. A LOW level for any of these pins is defined by connection to V_{EE2}, a HIGH level is defined as a voltage greater than V_{EE2} + 1.5 V and smaller than V_{CC} + 0.4 V.

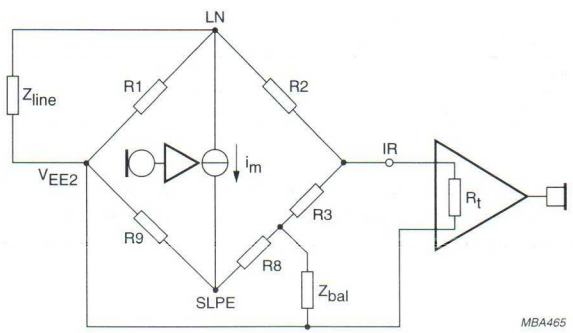


Fig.16 Equivalent circuit of TEA1060 family anti-sidetone bridge.

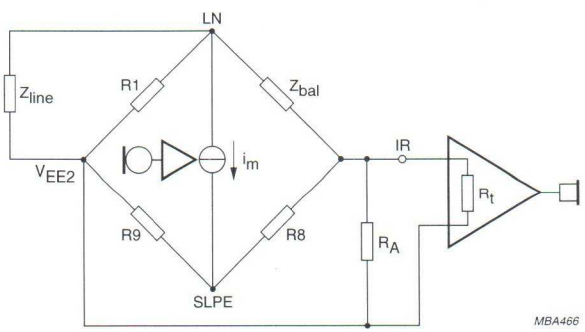


Fig.17 Equivalent circuit of an anti-sidetone network in the Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive line voltage continuous		–	12	V
V_{LN}	repetitive line voltage during switch-on line interruption		–	13.2	V
V_{LN}	repetitive peak line voltage one 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω; see Fig.22	–	28	V
I_{LN}	line current	R9 = 20 Ω			
	TEA1064B	note 1	–	140	mA
	TEA1064BT	note 1	–	140	mA
V_i	input voltage on pins other than LN		V_{EE1}–0.7	V_{CC}+0.7	V
P_{tot}	total power dissipation	R9 = 20 Ω; note 2			
	TEA1064B		–	717	mW
	TEA1064BT		–	555	mW
T_{amb}	operating ambient temperature		–25	+75	°C
T_{stg}	storage temperature		–40	+125	°C
T_j	junction temperature		–	+125	°C

Notes

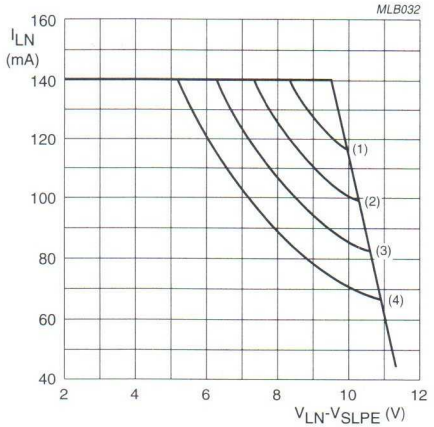
1. Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs 18 and 19 to determine the current as a function of the required voltage and the temperature.
2. Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT146	70 K/W
	SOT163A (note 1)	90 K/W

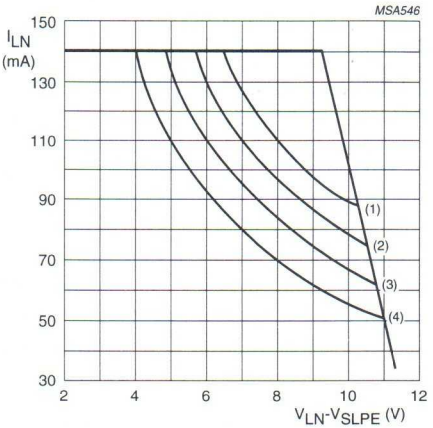
Note

1. Mounted on glass epoxy board 41 × 19 × 1.5 mm.



(1) T_{amb} = 45 °C; P_{tot} = 1143 mW.
(2) T_{amb} = 55 °C; P_{tot} = 1000 mW.
(3) T_{amb} = 65 °C; P_{tot} = 857 mW.
(4) T_{amb} = 75 °C; P_{tot} = 714 mW.

Fig.18 TEA1064B safe operating area.



(1) T_{amb} = 45 °C; P_{tot} = 888 mW.
(2) T_{amb} = 55 °C; P_{tot} = 777 mW.
(3) T_{amb} = 65 °C; P_{tot} = 666 mW.
(4) T_{amb} = 75 °C; P_{tot} = 555 mW.

Fig.19 TEA1064BT safe operating area.

CHARACTERISTICS

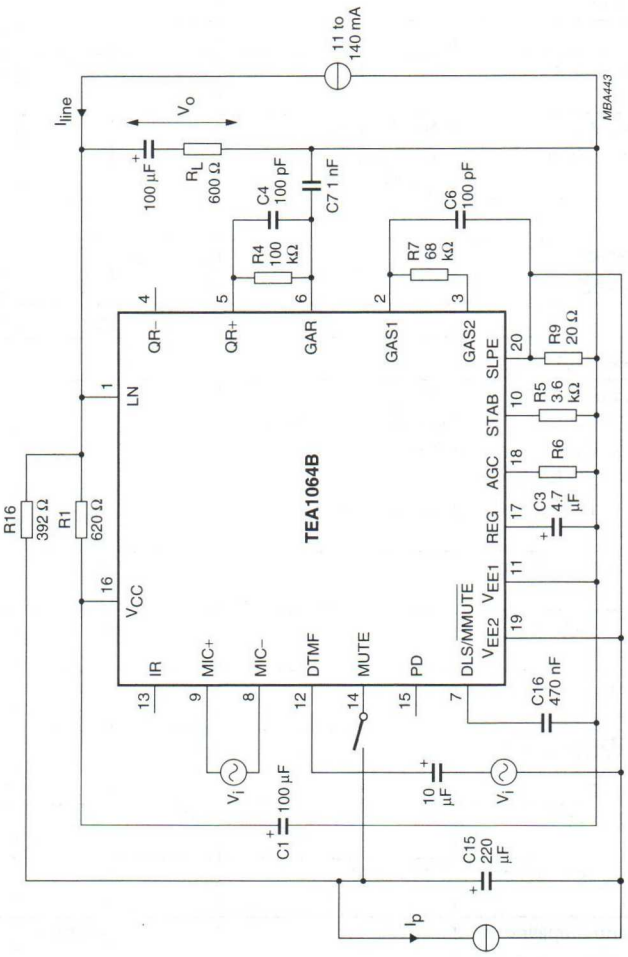
I_{line} = 11 to 140 mA; V_{EE1} = 0 V; f = 800 Hz; T_{amb} = 25 °C; R_L = 600 Ω; tested in the circuits of Fig.20 or Fig.21; V_{EE2} connected to SLPE; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies LN and V_{CC} (pins 1 and 16)						
V_{LN}	DC line voltage: voltage drop between LN and V_{EE1}	MIC–, MIC+ inputs open-circuit; without R_{VA}				
		I_{line} = 2 mA	–	1.8	–	V
		I_{line} = 4 mA	–	2.2	–	V
		I_{line} = 7 mA	–	3.2	–	V
		I_{line} = 11 mA	–	3.4	–	V
		I_{line} = 15 mA	3.25	3.5	3.75	V
		I_{line} = 100 mA	–	5.25	6.05	V
		I_{line} = 140 mA	–	6.1	7.0	V
$\Delta V_{LN}/\Delta T$	variation with temperature	I_{line} = 15 mA	–3	–1	+1	mV/K
V_{LN}	voltage drop over circuit with R_{VA} connected between REG and SLPE					
		R_{VA} = 33 kΩ	3.8	4.1	4.4	V
		R_{VA} = 20 kΩ	4.05	4.4	4.75	V
I_{CC}	internal supply current into pin 16	V_{CC} = 2.8 V				
		PD = LOW	–	1.3	1.6	mA
		PD = HIGH	–	60	82	µA
V_{CC}	supply voltage available for peripheral circuitry V_{EE2} connected to V_{EE1}	I_{line} = 15 mA; MUTE = HIGH; see Fig.5				
		I_p = 0.54 mA	2.2	2.4	–	V
		I_p = 0 mA	2.5	2.7	–	V
V_p	supply voltage available for peripheral circuitry	I_{line} = 15 mA				
		I_p = 1.4 mA	2.5	2.7	–	V
		I_p = 2.7 mA; $R_{REG-SLPE}$ = 20 kΩ	2.9	3.1	–	V
Microphone inputs MIC– and MIC+ (pins 8 and 9)						
Z_i	input impedance					
	differential		51	64	77	kΩ
	single-ended		25.5	32.0	38.5	kΩ
CMRR	common mode rejection ratio		–	82	–	dB
G_v	voltage gain (see Fig.20)	I_{line} = 15 mA; R7 = 68 kΩ	51	52	53	dB
$\Delta G_v f$	variation of G_v with frequency referred to 0.8 kHz	f = 300 and 3400 Hz	–0.5	±0.1	+0.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta G_v T$	variation of G_v with temperature referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 to +75 °C	–	±0.2	–	dB
DTMF input (pin 12)						
Z_i	input impedance		16.8	20.7	24.6	kΩ
G_v	voltage gain (see Fig.20)	I_{line} = 15 mA; R7 = 68 kΩ	24.5	25.5	26.5	dB
$\Delta G_v f$	variation of G_v with frequency referred to 0.8 kHz					
		f = 300 and 3400 Hz	−0.5	±0.01	+0.5	dB
		f = 697 and 1633 Hz	−0.2	±0.05	+0.2	dB
$\Delta G_v T$	variation of G_v with temperature referred to 25 °C	I_{line} = 50 mA; T_{amb} = −25 to +75 °C	–	±0.2	0.5	dB
Gain adjustment inputs GAS1 and GAS2 (pins 2 and 3)						
ΔG_v	transmitting amplifier gain adjustment range		−8	–	+0	dB
Sending amplifier output LN (pin 1)						
DYNAMIC LIMITER						
$V_{LN(p-p)}$	output voltage swing (peak-to-peak value)	I_{line} = 15 mA; R7 = 68 kΩ; $V_{i(RMS)}$ = 3.6 mV	3.4	3.8	4.2	V
THD	total harmonic distortion					
		V_i = 3.6 mV +10 dB	–	1.5	–	%
		V_i = 3.6 mV +15 dB	–	2.8	–	%
$V_{LN(p-p)}$	output voltage swing (peak-to-peak value)	V_i = 3.6 mV +10 dB				
		I_p = 1.4 mA	3.55	3.8	4.05	V
		I_p = 2.7 mA	3.25	3.5	3.75	V
		I_p = 0 mA; I_{line} = 7 mA	–	1.8	–	V
		I_p = 0 mA; I_{line} = 4 mA	–	0.9	–	V
	dynamic behaviour of limiter	C16 = 470 nF				
t_{att}	attack time V_{mic} jumps from 2 mV to 40 mV		–	1.5	5.0	ms
t_{rel}	release time V_{mic} jumps from 40 mV to 2 mV		50	150	–	ms
$V_{no(RMS)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC− and MIC+; psophometrically weighted (P53 curve)	–	−72	–	dBmp

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiving amplifier input IR (pin 13)						
Z_i	input impedance		17	21	25	kΩ
Receiving amplifier outputs QR− and QR+ (pins 4 and 5)						
Z_o	output impedance	single-ended	–	4	–	Ω
G_v	voltage gain (see Fig.21)	I_{line} = 15 mA; R4 = 100 kΩ				
	single-ended	R_T = 300 Ω	30	31	32	dB
	differential	R_T = 600 Ω	36	37	38	dB
$\Delta G_v f$	variation of G_v with frequency referred to 0.8 kHz	f = 300 and 3400 Hz	−0.5	−0.2	0	dB
$\Delta G_v T$	variation of G_v with temperature referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 to +75 °C	–	±0.2	–	dB
$V_{o(RMS)}$	output voltage (RMS value)	TDA = 2%; sinewave drive; R4 = 100 kΩ; I_{line} = 15 mA				
	single-ended	R_T = 150 Ω	–	0.2	–	V
	differential	R_T = 450 Ω	–	0.37	–	V
	differential	C_T = 47 nF; R_s = 100 Ω; f = 3400 Hz	–	0.52	–	V
$V_{o(RMS)}$	output voltage (RMS value)	I_p = 0 mA; TDA = 10%; sinewave drive; R4 = 100 kΩ; R_T = 150 Ω				
		I_{line} = 4 mA	–	20	–	mV
		I_{line} = 7 mA	–	160	–	mV
$V_{no(RMS)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; psophometrically weighted (P53 curve); pin IR open-circuit				
	single-ended	R_T = 300 Ω	–	45	–	μV
	differential	R_T = 600 Ω	–	90	–	μV
$V_{no(RMS)}$	noise output voltage (RMS value)	see Fig.21; S1 in position 2; 200 Ω between MIC− and MIC+; single-ended; R_T = 300 Ω				
		R7 = 68 kΩ	–	100	–	μV
		R7 = 24.9 kΩ	–	65	–	μV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Gain adjustment input GAR (pin 6)						
ΔG_v	receiving amplifier gain adjustment range		−11	–	+8	dB
MUTE input (pin 14)						
V_{IH}	HIGH level input voltage		1.5 +V_{EE2}	–	V_{CC} +0.4	V
V_{IL}	LOW level input voltage		0	–	0.3 +V_{EE2}	V
I_{mute}	input current		–	11	20	μA
ΔG_v	change of microphone amplifier gain at mute on	MUTE = HIGH	–	−100	–	dB
G_v	voltage gain from input DTMF-SLPE to QR+ output with mute on	MUTE = HIGH; single-ended load; R_L = 300 Ω	–	−18	–	dB
Power-down input PD (pin 15)						
V_{IH}	HIGH level input voltage		1.5 +V_{EE2}	–	V_{CC1} +0.4	V
V_{IL}	LOW level input voltage		0	–	0.3 +V_{EE2}	V
I_{PD}	input current		–	5	10	μA
Automatic gain control input AGC (pin 18)						
	controlling the gain from IR (pin 13) to QR+, QR− (pins 4, 5) and the gain from MIC+, MIC− (pins 8, 9) to LN (pin 1)	R6 = 93.1 kΩ (between pins 18 and 11)				
G_v	gain control range with respect to I_{line} = 15 mA	I_{line} = 75 mA	−5.7	−6.1	−6.5	dB
I_{line}	highest line current for maximum gain		–	24	–	mA
I_{line}	lowest line current for minimum gain		–	61	–	mA
ΔG_v	change of gain between I_{line} = 15 and 35 mA		−0.9	−1.4	−1.9	dB
Microphone mute input DLS/$\overline{\text{MMUTE}}$ (pin 7)						
V_{IL}	LOW level input voltage		V_{EE1}	–	V_{EE1} +0.3	V
I_{IL}	input current at LOW level input voltage		−85	−60	−35	μA
t_{rel}	release time after a LOW level on pin 7	C16 = 470 nF	–	30	–	ms
ΔG_v	change of microphone amplifier gain at LOW level input voltage on pin 7		–	−100	–	dB



For measuring gain from MIC+ and MIC− the MUTE input should be LOW or open-circuit.
For measuring the DTMF input, the MUTE input should be HIGH.
Inputs not being tested should be open-circuit.

Fig.20 Test circuit for defining voltage gain of MIC−, MIC+ and DTMF inputs; voltage gain (G_v) is defined as 20log $|V_o/V_i|$.

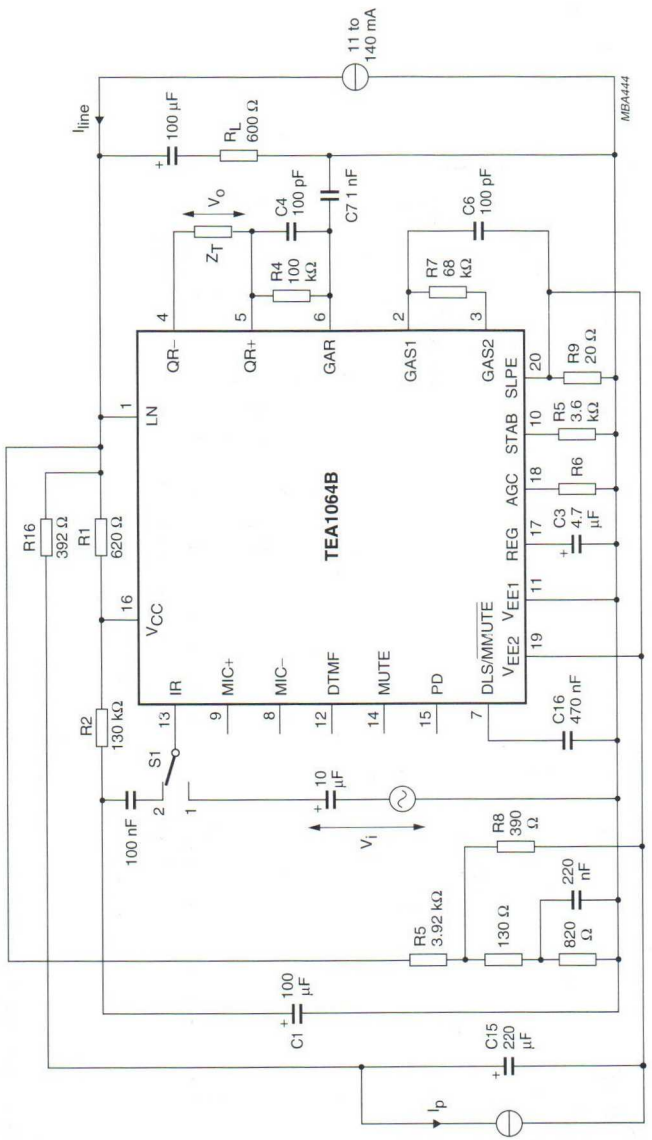
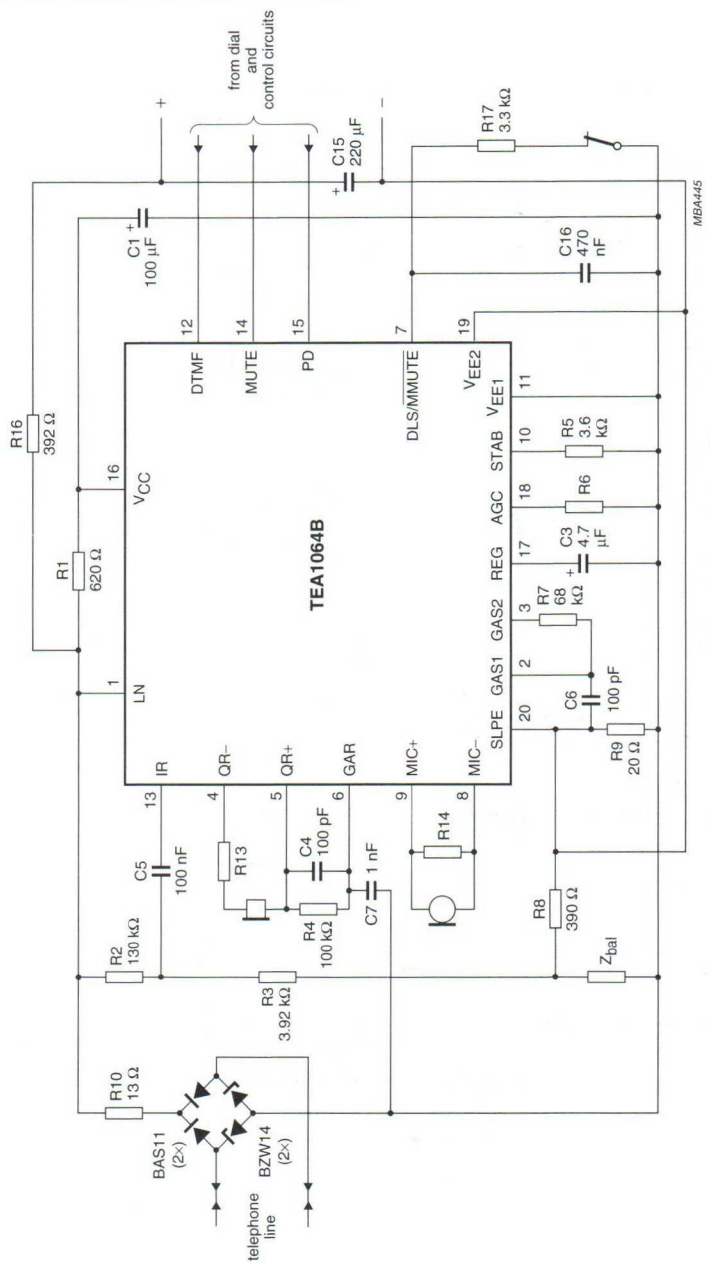


Fig.21 Test circuit for defining voltage gain of the receiving amplifier; voltage gain (G_v) is defined as $20\log |V_o/V_i|$ (with S1 in position 1).

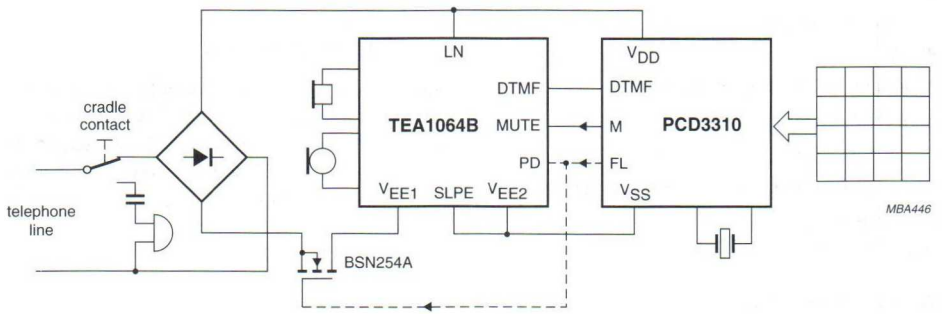
APPLICATION INFORMATION

The basic application circuit is shown in Fig.22 and some typical application are shown in Fig.23



The diode bridge and R10 limit the current into, and the voltage across, the circuit during line transients.
A different protection arrangement is required for pulse dialling or register recall.

Fig.22 Basic application of TEA1064B with SLPE as supply reference for peripherals, shown here with piezo-electric earpiece and DTMF dialling.



The broken line indicates optional flash (register recall by timed loop break).

Fig.23 Typical DTMF-pulse set application circuit (simplified) showing the TEA1064B with the CMOS bilingual dialling circuit PCD3310.

Versatile telephone transmission circuit with dialler interface

TEA1065

FEATURES

- Current and voltage regulator mode with adjustable static resistances
- Provides supply for external circuitry
- Symmetrical high-impedance inputs for piezoelectric microphone
- Asymmetrical high-impedance input for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power-down input for pulse dial or register recall
- Digital pulse input to drive an external switch transistor
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (on microphone and earpiece amplifiers)
- Adjustable gain control
- DC line voltage adjustment facility

GENERAL DESCRIPTION

The TEA1065 is a bipolar integrated circuit which performs all speech and line interface functions that are required in fully electronic telephone sets with adjustable DC mask. The circuit performs electronic switching between dialling and speech internally.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1065	24	DIL	plastic	SOT101L
TEA1065T	24	SO24	plastic	SOT137A

Notes

1. SOT101-1; 1998 Jun 18.
2. SOT137-1; 1998 Jun 18.

MAINTENANCE TYPE
Not recommended for new designs

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	line voltage	I_{line} = 15 mA	4.25	4.45	4.65	V
I_{line}	normal operation line current range		10	–	150	mA
I_{CC}	internal supply consumption					
	power-down input LOW		–	1.14	1.5	mA
	power-down input HIGH		–	73	105	µA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA; MUTE input HIGH				
		I_P = 1.2 mA	2.7	–	–	V
		I_P = 1.55 mA	2.5	–	–	V
G_V	voltage gain range					
	microphone amplifier		30	–	46	dB
	earpiece amplifier		20	–	45	dB
ΔG_V	line loss compensation					
	gain control range		–5.5	–5.9	–6.3	dB
T_{amb}	operating ambient temperature range		–25	–	+75	°C

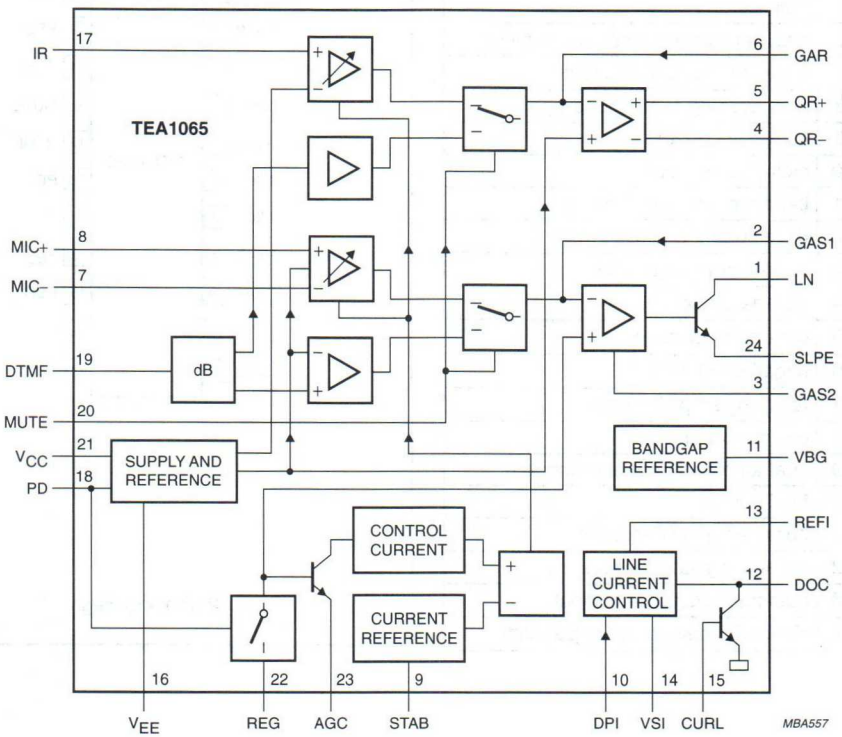


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
GAS1	2	gain adjustment; sending amplifier
GAS2	3	gain adjustment; sending amplifier
QR–	4	inverting output; receiving amplifier
QR+	5	non-inverting output; receiving amplifier
GAR	6	gain adjustment; receiving amplifier
MIC–	7	inverting microphone input
MIC+	8	non-inverting microphone input
STAB	9	current stabilizer
DPI	10	digital pulse input
VBG	11	bandgap output reference
DOC	12	drive current output
REFI	13	reference voltage input
VSI	14	voltage sense input
CURL	15	current limitation input
V_{EE}	16	negative line terminal
IR	17	receiving amplifier input
PD	18	power-down input
DTMF	19	dual-tone multifrequency input
MUTE	20	MUTE input
V_{CC}	21	positive supply decoupling
REG	22	voltage regulator decoupling
AGC	23	automatic gain control input
SLPE	24	slope (DC resistance) adjustment

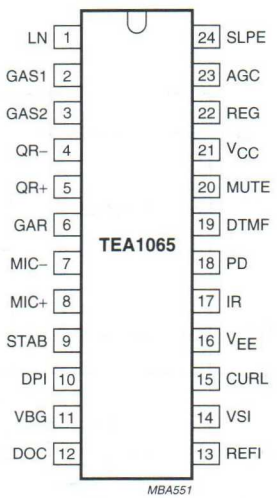


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripherals are usually supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} (pin 21) and regulates its voltage drop between LN and SLPE (pins 1 and 24). The internal supply requires a decoupling capacitor between V_{CC} and V_{EE} (pin 16); the internal voltage regulator has to be decoupled by a capacitor from REG (pin 22) to V_{EE}. The internal current stabilizer is set by a 3.6 kΩ resistor connected between STAB (pin 9) and V_{EE}.

The TEA1065 can be set either in a DC voltage regulator mode or in a DC current regulator mode. The DC mask can be selected by connecting the appropriate external components to the dedicated pins (VSI, REFI, DOC, VBG).

When the DC current regulator mode is not required it can be cancelled by connecting pin VSI to V_{EE}; pins REFI, VBG and DOC are left open-circuit.

Voltage regulator mode

The voltage regulator mode is achieved when the line current is less than the current I_{knee} as illustrated in Fig.3. With R13 = R14 = 30 kΩ, the current I_{knee} = 30 mA (I_P = 0 mA).

This line current value will be reached when the voltage on pin VSI (almost equal to the voltage on pin SLPE) exceeds the voltage on pin REFI (equal to the voltage on pin VBG divided by the resistor tap R13, R14). For other values of R13 and R14, the I_{knee} current is given by the following formula:

$$I_{knee} = I_{CC} + I_P + (VBG/R9) \times \{R14/(R14 + R13)\} - (R15/R9) \times I_O(VSI)$$

I_{CC} is the current required by the circuit itself (typ. 1.14 mA). I_P is the current required by the peripheral circuits connected between V_{CC} and V_{EE}. $I_{O(VSI)}$ is the output current from pin VSI (typ. 2.5 μA).

The DC slope of the V_{line}/I_{line} curve is, in this mode, determined by R9 (R9 = R9a + R9b) in series with the r_{ds} of the external line current control transistor (see Fig.4; $r_{ds} = \partial V_{GS}/\partial I_D$ at $V_{GS} = V_{DS}$).

Current regulator mode

The current regulator mode is achieved when the line current is greater than I_{knee}. In this mode, the slope of the V_{line}/I_{line} curve is approximately 1300 Ω with R9 = 20 Ω, R16 = 1 MΩ, R13 = R14 = 30 kΩ. For other values of these resistances, the slope value can be approximated by the following formula:

$$R9 \times \{1 + R16 \times (1/R13 + 1/R14)\}$$

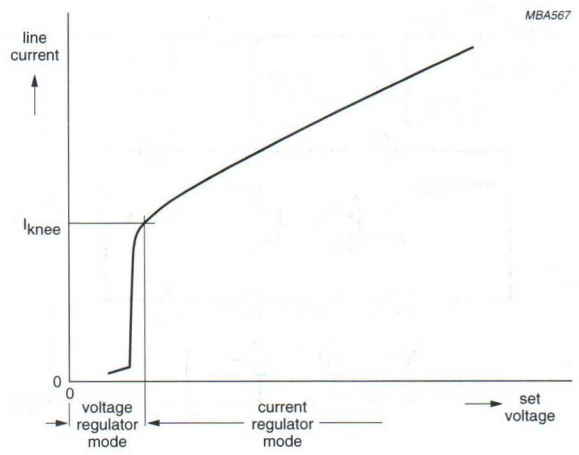


Fig.3 Voltage and current regulator mode.

The DC current flowing into the set is determined by the exchange supply voltage (V_{exch}), the DC resistance of the subscriber line (R_{line}) and the DC voltage on the subscriber set (see Fig.4).
If the line current exceeds $I_{CC} + 0.3$ mA, required by the circuit itself ($I_{CC} \approx 1.14$ mA), plus the current I_p required by the peripheral circuits connected to V_{CC} then the voltage regulator will divert the excess current via LN.

$$V_{LN} = V_{ref} + I_{SLPE} \times R9 =$$
$$V_{ref} + (I_{line} - I_{CC} - 0.3 \times 10^{-3} - I_p) \times R9$$

where: V_{ref} is an internally generated temperature compensated reference voltage of 4.18 V and R9 is an external resistor connected between SLPE and V_{EE}.

The preferred value of R9 is 20 Ω. Changing R9 will influence the microphone gain, gain control characteristics, sidetone and the maximum output swing on LN. In this instance, the voltage on the line (excluding the diode rectifier bridge; see Fig.4) is:

$$V_{line} = V_{LN} + V_{GS} + R16 \times I_{DOC}$$

where: V_{GS} is the voltage drop between the gate and source terminal of the external line current control transistor and I_{DOC} is the current sunk by pin DOC ($I_{DOC} = 0$ in the voltage regulator mode and increases with I_{line} in the current regulator mode).
Under normal conditions $I_{SLPE} >> I_{CC} + 0.3$ mA $+ I_p$ and for the voltage regulator mode ($I_{line} < I_{knee}$), the static behaviour of the circuit is equal to a 4.18 V voltage regulator diode with an internal resistance of R9 in series with the V_{GSon} of the external line current control transistor. For the current regulator mode ($I_{line} > I_{knee}$), the static behaviour of the circuit is equal to a 4.18 V voltage regulator diode with an internal resistance of R9 in series with the V_{GSon} of the external line current control transistor and also in series with a DC voltage source R16 $\times I_{DOC}$ (the preferred value of R16 is 1 MΩ at this value the current I_{DOC} is negligible compared to I_{line}).

In the audio frequency range the dynamic impedance between LN and V_{EE} is equal to R1 (see Fig.8). The internal reference voltage V_{ref} can be adjusted by means of an external resistor R_{VA}. This resistor, connected between LN and REG, will decrease the internal reference voltage. When R_{VA} is connected between REG and SLPE the internal reference voltage will increase.
The maximum allowed line current is given in Figs 5 and 6, where the current is shown as a function of the required reference voltage, ambient temperature and applied package.

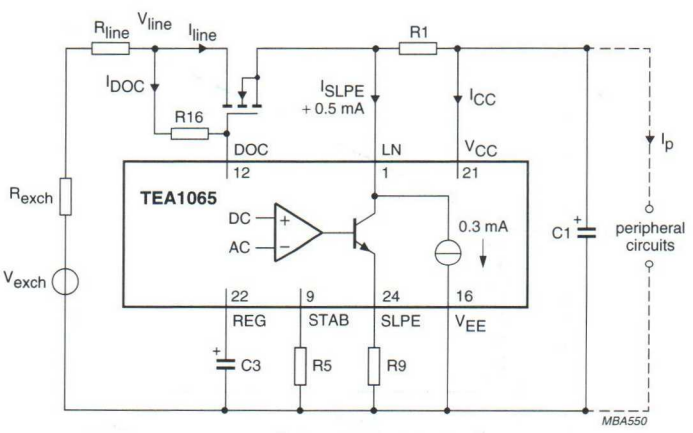
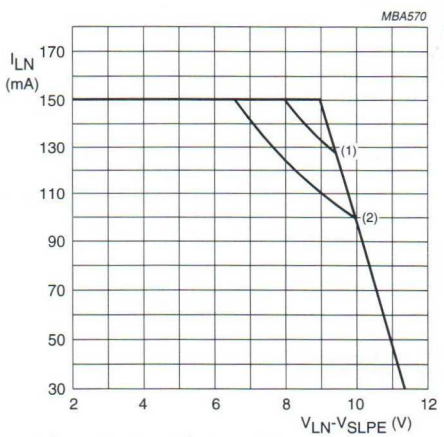


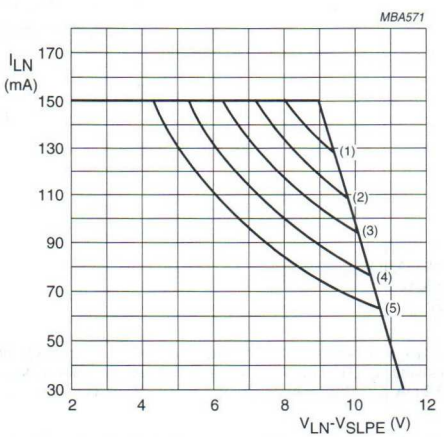
Fig.4 Supply arrangement.

The current I_p, available from V_{CC} for supplying peripheral circuits, depends on the external components and on the line current. Fig.7 shows this current for $V_{CC} > 2.2$ V and for $V_{CC} > 3$ V, where 3 V is the minimum supply voltage for most CMOS circuits including a diode voltage drop for a back-up diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven (earpiece amplifier supplied from V_{CC}).



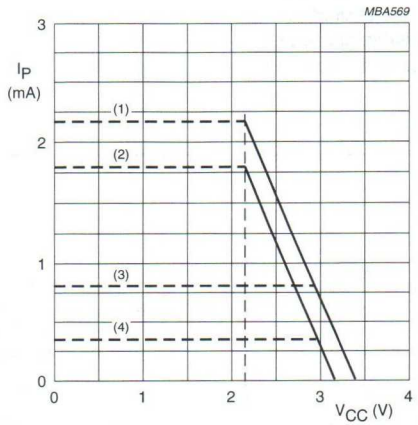
	T_{amb}	P_{tot}
(1)	65 °C	1.2 W
(2)	75 °C	1.0 W

Fig.5 TEA1065 safe operating area.



	T_{amb}	P_{tot}
(1)	35 °C	1.2 W
(2)	45 °C	1.07 W
(3)	55 °C	0.93 W
(4)	65 °C	0.8 W
(5)	75 °C	0.67 W

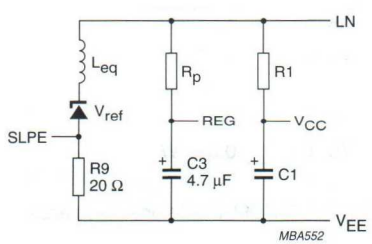
Fig.6 TEA1065T safe operating area.



I_{line} = 15 mA at V_{LN} = 4.45 V
R1 = 620 Ω
R9 = 20 Ω

Curve (1) and (3) are valid when the receiving amplifier is not driven or when MUTE = HIGH, curves (2) and (4) are valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)}$ = 150 mV, R_L = 150 Ω (asymmetrical).
(1) = 2.2 mA; (2) = 1.77 mA; (3) = 0.78 mA and (4) = 0.36 mA.

Fig.7 Maximum current I_p available from V_{CC} for external (peripheral) circuitry with V_{CC} > 2.2 V and V_{CC} > 3 V.



$L_{eq} = C3 \times R9 \times R_p$
R_p = 17.5 kΩ

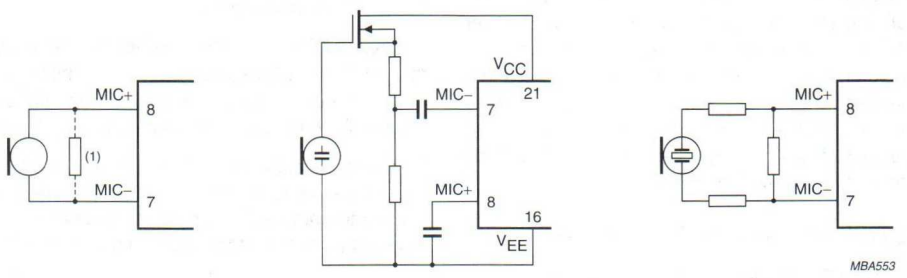
Fig.8 Equivalent circuit impedance between LN and V_{EE}.

Microphone inputs MIC+ and MIC− and gain adjustment connections GAS1 and GAS2

The TEA1065 has symmetrical microphone inputs, its input impedance is 40.8 kΩ (2 × 20.4 kΩ) and its voltage gain is typ. 38 dB with R7 = 68 kΩ. Either dynamic, magnetic or piezoelectric microphones can be used, or an electret microphone with a built-in FET buffer. Arrangements for the microphones types are illustrated in Fig.9.

The gain of the microphone amplifier is proportional to external resistor R7, connected between GAS1 and GAS2, which can be adjusted between 30 dB and 46 dB to suit the sensitivity of the transducer.

An external 100 pF capacitor (C6) is required between GAS1 and SLPE to ensure stability. A larger value of C6 may be chosen to obtain a first-order low-pass filter. The "cut-off" frequency corresponds with the time constant R7 × C6.



(a) magnetic or dynamic microphone, the resistor (1) may be connected to reduce the terminating impedance, or for sensitive types a resistive attenuator can be used to prevent overloading the microphone inputs;

(b) electret microphone;

(c) piezoelectric microphone.

Fig.9 Microphone arrangements.

MUTE input

When MUTE = HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. When MUTE = LOW or open-circuit the DTMF input is inhibited and the microphone and receiving amplifier inputs are enabled. Switching the MUTE input will cause negligible clicks at the earpiece outputs and on the line. An electrostatic discharge protection diode is connected between pin MUTE and pin V_{CC} (pins 20 and 21).

Dual-tone multifrequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typ. 12.5 dB less than the gain of the microphone amplifier and varies with R7 in the same way as the gain of the microphone amplifier. This means that the tone level at the DTMF input has to be adjusted after setting the gain of the microphone amplifier. When R7 = 68 kΩ the gain is typically 25.5 dB. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifiers: IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, QR+ (non-inverting) and QR− (inverting). These outputs may be used for single-ended or differential drive, depending on the type and sensitivity of the earpiece used (see Fig.10). Gain from IR to QR+ is typically 31 dB with R4 = 100 kΩ, which is sufficient for low-impedance magnetic or dynamic earpieces which are suitable for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB. Differential drive can be used when earpiece impedance exceeds 450 Ω as with high impedance dynamic, magnetic or piezoelectric earpieces.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the ratio of peak and RMS value is higher.

The gain of the receiving amplifier can be adjusted over a range of −11 dB to +8 dB to suit the sensitivity of the transducer that is used. The gain is proportional to external resistor R4 connected between GAR and QR+.

Two external capacitors, C4 = 100 pF and C7 = 1 nF, are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order low-pass filter. The "cut-off" frequency corresponds with the time constant R4 × C4.

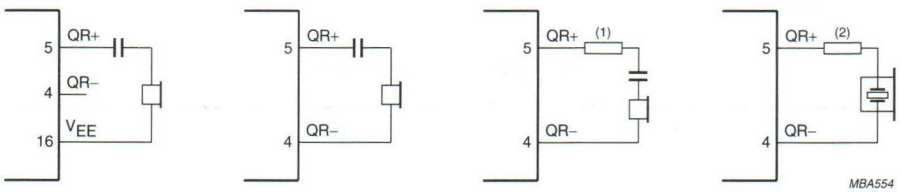


Fig.10 Alternative receiver arrangements:
(a) dynamic earpiece with an impedance less than 450 Ω;
(b) dynamic earpiece with an impedance more than 450 Ω;
(c) magnetic earpiece with an impedance more than 450 Ω, resistor (1) may be connected to prevent distortion (inductive load);
(d) piezoelectric earpiece, resistor (2) is required to increase the phase margin (stability with capacitive load).

Automatic gain control

Automatic compensation of line loss is obtained by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and receiving amplifier in accordance with the DC line current (see Fig.12). The control range is 5.9 dB; this corresponds to a line length of 3.5 km of twisted pair cable (see Fig.11). The DTMF gain is not affected by this feature.

If automatic line loss compensation is not required the AGC pin can be left open-circuit, the amplifiers then give their maximum gain.

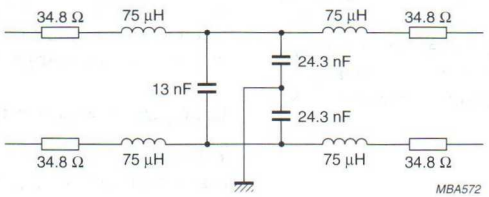


Fig.11 Typical 0.5 km line cell model used for automatic gain control optimization.

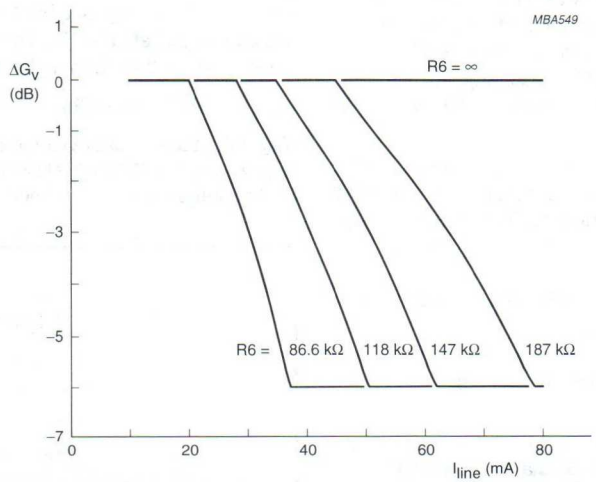


Fig.12 Variation of gain as a function of line current with R6 as a parameter; R9 = 20 Ω.

Power-down input PD

During pulse dialling or register recall (timed-loop-break) the telephone line is interrupted, consequently it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirement on this capacitor is relaxed by applying a HIGH level to the PD input during the loop-break. This reduces the internal supply current from typ. 1.14 mA to 73 μA.

A HIGH level at PD also disconnects the capacitor at REG which results in the voltage stabilizer having no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required PD may be left open-circuit or connected to V_{EE}. An electrostatic discharge protection diode is connected between pin PD and V_{CC}.

Digital pulse input DPI

A HIGH level at DPI creates a current which flows from pin DOC to V_{EE} in order to interrupt the line current by the external line current control transistor (see Fig.18; MOSFET BUK554). A LOW level (or pin left open-circuit) disables this current to provide the normal DC regulation (voltage or current). A simple application without regulation of current in pulse dialling mode is given in Fig.18.

When DPI is activated (HIGH level), the external line current control transistor is switched off resulting in no current in the TEA1065. The voltage on pin SLPE becomes zero and capacitor C15 discharges cancelling the current regulation when DPI becomes inactive (LOW level).

To provide a constant regulation (in speech mode and pulse mode), an external transistor is required to keep C15 charged during DPI active (see Fig.19 in which the Field Effect Transistor BSJ177 is directly driven by the DPI signal).
An electrostatic discharge protection diode is connected between pin DPI and pin V_{CC}.

Voltage sense input and reference voltage input VSI and REFI

The voltage on pin VSI represents the DC voltage of pin SLPE. The RC filter (R15 × C15) is also intended to disable the DC regulation when C15 is shunted or not yet charged (especially directly after hook-off). The time constant R15 × C15 determines approximately the time when no regulation (except CURL pin limitation) is activated.
The voltage applied on pin REFI represents a fraction of the bandgap reference voltage given by pin VBG (resistor tap R13 and R14) in order to determine I_{knee}.

Drive current output DOC

Pin DOC drives the external line current control transistor in order to achieve line interruption during pulse dialling (or register recall) and also the DC slope when $I_{line} > I_{knee}$.
The current sunk by pin DOC is determined by the voltage on pin VSI in comparison with the voltage on pin VBG divided by the resistor tap R13 and R14.
When pin DPI is activated, pin DOC changes to a low voltage (by trying to sink typ. 900 μA to V_{EE}) to switch off the external line current control transistor.

Bandgap reference output VBG

This output provides a voltage reference to set the knee line current with the following formula:

$$I_{knee} = I_{CC} + I_P + (VBG/R9) \times \{R14/(R14 + R13)\} - (R15/R9) \times 2.5 \times 10^{-6}$$

In order to improve stability, a capacitive load is not allowed on this output.

Current limit input CURL

This input is applied to the base of an internal NPN transistor which has its collector connected to pin DOC and its emitter to V_{EE} (see Fig.13). The transistor limits the line current just after hook-off or during line transients to a value given by the following formula:

$$I_{hook\text{-}off} = I(R1) + V_{BE}/R9b$$

V_{BE} is the base-emitter voltage of the transistor (typ. 700 mV at 25 °C). I(R1) is the current flowing through R1 to charge C1 just after hook-off.

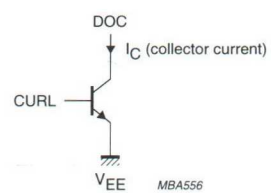


Fig.13 Internal current limiting transistor.

The maximum hook-off current then becomes:

$I_{hook\text{-}off} = V_Z/R1 + V_{BE} \times (R9a + R9b + R1)/(R1 \times R9b)$

where V_Z is the Zener voltage of diode D5 (see Fig.18).

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising $R1//Z_{line}$, R2, R3, R9 and Z_{bal} (see Fig.18). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9 \times R2 = R1 \times (R3 + R8)$
b) $k = R3 \times (R8 + R9)/(R2 \times R9)$
c) $Z_{bal} = k \times Z_{line}$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice Z_{line} varies considerably with the line length and line type. Therefore, the value chosen for Z_{bal} should be for an average line length giving satisfactory sidetone suppression with long and short times. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

Example

With k = 1, R1 = 619 Ω, R9 = 20 Ω and an average line impedance represented by 270 Ω + (120 nF // 1100 Ω), the calculation results in:

- R2 = 130 kΩ
- R3 = 3650 Ω
- R8 = 715 Ω

The anti-sidetone network for the TEA1060 family, shown in Fig.15, attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Note

More information on the balancing of the anti-sidetone bridges can be obtained in our publication *"Versatile speech transmission ICs for electronic telephone sets"*, order number 9398 341 10011.

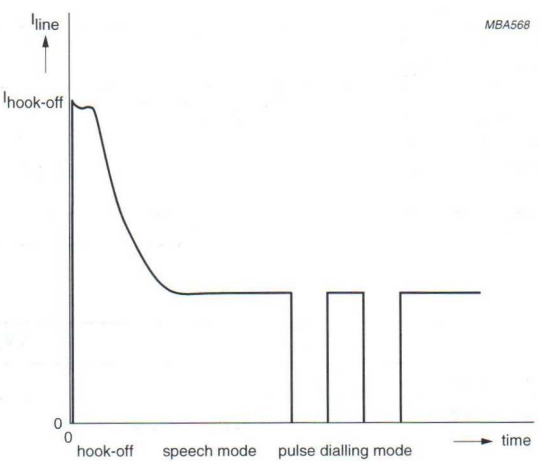


Fig.14 Example of line current shape in pulse dialling mode (see also Fig.18).

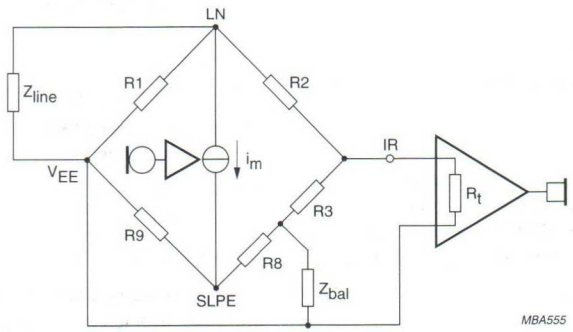


Fig.15 Equivalent circuit of TEA1060 family anti-sidetone bridge.

LIMITING VALUES

In accordance with the absolute maximum system (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive line voltage continuous		–	12	V
V_{DOC}	positive DOC voltage continuous		–	12	V
V_{LN}	repetitive line voltage during switch-on or line interruption		–	13.2	V
I_{LN}	line current (see also Fig.5 and 6)		–	150	mA
V_I	input voltage on pins other than LN, DOC, VSI, REFI and CURL		$V_{EE} - 0.7$	$V_{CC} + 0.7$	V
P_{tot}	total power dissipation	see Figs 5 and 6			
T_{stg}	storage temperature range		–40	+ 125	°C
T_{amb}	operating ambient temperature range		–25	+75	°C
T_j	junction temperature		–	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air; TEA1065	–	50	K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air; TEA1065T (1)	–	75	K/W

Note

1. TEA1065T is mounted on glassy epoxy board 28.5 × 19.1 × 1.5 mm

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2, method 3015 (HBM 1500 Ω, 100 pF, 3 positive pulses and 3 negative pulses on each pin as a function of pin V_{EE}.

CHARACTERISTICS

I_{LN} = 10 to 150 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; R9 = 20 Ω; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply LN and V_{CC} (pins 1 and 21)						
V_{LN}	voltage drop over circuit	I_{line} = 5 mA	3.95	4.25	4.55	V
		I_{line} = 15 mA	4.25	4.45	4.65	V
		I_{line} = 100 mA	5.4	6.1	6.7	V
		I_{line} = 140 mA	–	–	7.5	V
$\Delta V_{LN}/\Delta T$	variation with temperature	I_{line} = 15 mA	–3	–1	+1	mV/K
V_{LN}	voltage drop over circuit	I_{line} = 15 mA				
		$R_{VA} = R_{1\text{-}22}$ = 68 kΩ	3.6	3.9	4.15	V
		$R_{VA} = R_{22\text{-}24}$ = 39 kΩ	4.7	5.0	5.3	V
I_{CC}	supply current	PD = LOW; V_{CC} = 2.8 V	–	1.14	1.5	mA
		PD = HIGH; V_{CC} = 2.8 V	–	73	105	µA
Microphone inputs MIC+ and MIC– (pins 8 and 7)						
$\|Z_I\|$	input impedance		18.5	20.4	24.3	kΩ
G_v	voltage gain	I_{line} = 15 mA; R7 = 68 kΩ	37	38	39	dB
$\Delta G_v f$	variation with frequency referred to 800 Hz	I_{line} = 15 mA; f = 300 to 3400 Hz	–0.5	±0.2	+0.5	dB
$\Delta G_v T$	variation with temperature referred to 25 °C	I_{line} = 50 mA; T_{amb} = –25 to 75 °C; without R6	–	±0.5	–	dB
Dual-tone multi-frequency input DTMF (pin 19)						
$\|Z_I\|$	input impedance		16.8	20.7	24.6	kΩ
G_v	voltage gain	I_{line} = 15 mA; R7 = 68 kΩ	24.5	25.5	26.5	dB
$\Delta G_v f$	variation with frequency referred to 800 Hz	I_{line} = 15 mA f = 300 to 3400 Hz	–0.5	±0.2	+0.5	dB
$\Delta G_v T$	variation with temperature referred to 25 °C	I_{line} = 50 mA; T_{amb} = –25 to +75 °C	–	±0.5	–	dB
Gain adjustment GAS1 and GAS2 (pin 2 and 3)						
ΔG_v	gain variation with R7 connected between pins 2 and 3; transmitting amplifier		–8	–	+8	dB

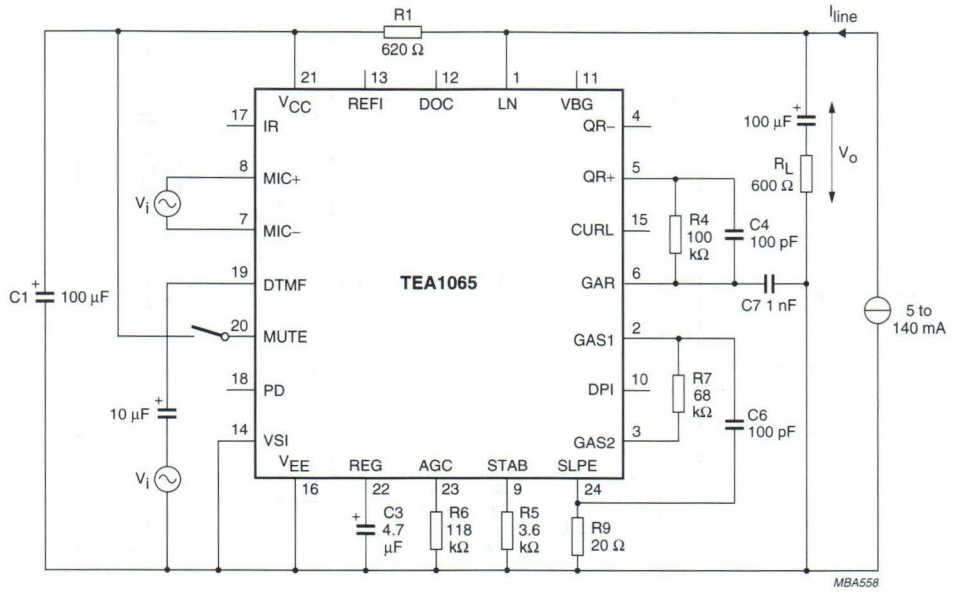
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmitting amplifier output LN (pin 1)						
$V_{LN(rms)}$	output voltage (RMS value)	I_{line} = 15 mA				
		d_{tot} = 2%	1.9	2.3	–	V
		d_{tot} = 10%	–	2.6	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; pin 7 and 8 open-circuit psophometrically weighted (P53 curve); control transistor included (MOS BUK554 type see Fig.18)	–	–68	–	dBmp
Receiving amplifier input IR (pin 17)						
Z_I	input impedance		17	21	25	kΩ
Receiving amplifier outputs QR+ and QR– (pin 5 and 4)						
Z_O	output impedance		–	4	–	Ω
G_v	voltage gain	I_{line} = 15 mA; R4 = 100 kΩ				
		single-ended; RT = 300 Ω	30	31	32	dB
		differential; RT = 600 Ω	36	37	38	dB
$\Delta G_v f$	variation with frequency referred to 800 Hz	f = 300 to 3400 Hz	–0.5	±0.2	+0.5	dB
$\Delta G_v T$	variation with temperature referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 to +75 °C	–	±0.2	–	dB
$V_{O(rms)}$	output voltage (RMS value)	I_{line} = 15 mA; THD = 2%; sinewave drive; R4 = 100 kΩ				
		single-ended; RT = 150 Ω	0.3	0.38	–	V
		differential; RT = 450 Ω	0.56	0.72	–	V
		differential; CT = 60 nF; (1500 Ω series resistor); f = 3400 Hz	0.87	1.07	–	V
		I_{line} = 30 mA; differential; CT = 60 nF; (1500 Ω series resistor); f = 3400 Hz	1.02	1.22	–	V
$V_{O(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ				
		single-ended; RT = 300 Ω	–	50	–	μV
		differential; RT = 600 Ω	–	100	–	μV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Gain adjustment GAR (pin 6)						
ΔG_v	receiving amplifier, gain adjustment range		−11	–	+8	dB
Mute input MUTE (pin 20)						
V_{IH}	input voltage HIGH		1.5	–	V_{CC}	V
V_{IL}	input voltage LOW		–	–	0.3	V
I_{MUTE}	input current		–	8	15	µA
ΔG_v	change of microphone amplifier gain	MUTE = HIGH	–	−70	–	dB
G_v	voltage gain from DTMF input to QR+ or QR−	MUTE = HIGH; R4 = 100 kΩ single-ended; RT = 300 Ω	−19	−17	−15	dB
Power-down input PD (pin 18)						
V_{IH}	input voltage HIGH		1.5	-	V_{CC}	V
V_{IL}	input voltage LOW		-	-	0.3	V
I_{PD}	input current		-	2.5	5.0	µA
Automatic gain control input AGC (pin 23)						
ΔG_v	controlling the gain from IR to QR+, QR− and the gain from MIC+, MIC− to LN; gain control range with respect to I_{line} = 15 mA	R6 = 118 kΩ	−5.5	−5.9	−6.3	dB
I_{line}	highest line current for maximum gain		–	28	–	mA
I_{line}	lowest line current for minimum gain		–	50	–	mA
ΔG_v	change of gain between I_{line} = 15 and 35.5 mA		–	-1.5	–	dB
Current limiting input CURL (pin 15)						
V_{BE}	base-emitter voltage drop of internal transistor	see Fig.13; I_C = 50 µA = I_{DOC}	–	0.7	–	V
H_{FE}	current gain of internal transistor	see Fig.13; I_C = 50 µA = I_{DOC}	60	120	–	
$I_{C(max)}$	maximum collector current of internal transistor	see Fig.13	–	–	2	mA
Bandgap reference voltage output VBG (pin 12)						
V_{BG}	reference voltage		–	1.22	–	V
I_{BG}	output drive capability	note 1	−100	-	+50	µA
Z_O	output impedance		–	12	–	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage sense input VSI (pin 14)						
I_O	output current	pin VSI connected to V_{EE}	–	–2.5	–	μA
Reference input REFI (pin 13)						
I_O	output current		–	–	2.0	mA
Drive current output DOC (pin 11)						
I_O	output current	REFI connected to V_{EE}; VSI not connected; DPI = LOW	120	300	–	μA
		REFI not connected; VSI connected to V_{EE}; DPI = HIGH	200	900	–	μA
Digital pulse input DPI (pin 10)						
V_{IH}	input voltage HIGH		1.5	–	V_{CC}	V
V_{IL}	input voltage LOW		–	–	0.3	V
I_{DPI}	input current		–	2.5	5	μA

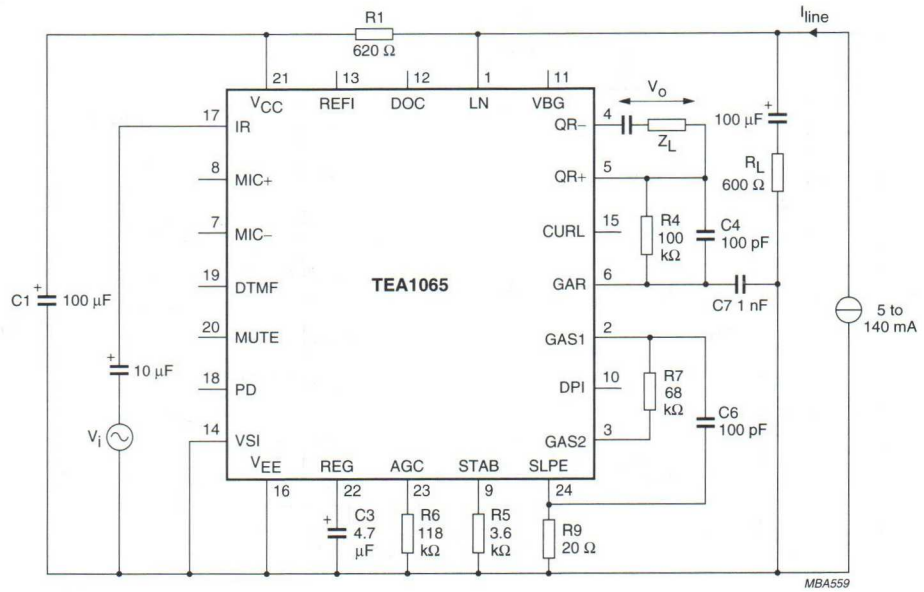
Note

1. No capacitive load on the V_{BG} output. Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.



Voltage gain is defined as $G_v = 20 \text{ Log } |V_o/V_i|$. For measuring the gain from MIC+ and MIC– the MUTE input should be LOW or open-circuit, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open-circuit except VSI that should be connected to V_{EE}.

Fig.16 Test circuit for defining voltage gain of MIC+, MIC– and DTMF inputs.



Voltage gain is defined as $G_v = 20 \text{ Log } |V_o/V_i|$.

Fig.17 Test circuit for defining voltage gain of the receiving amplifier.

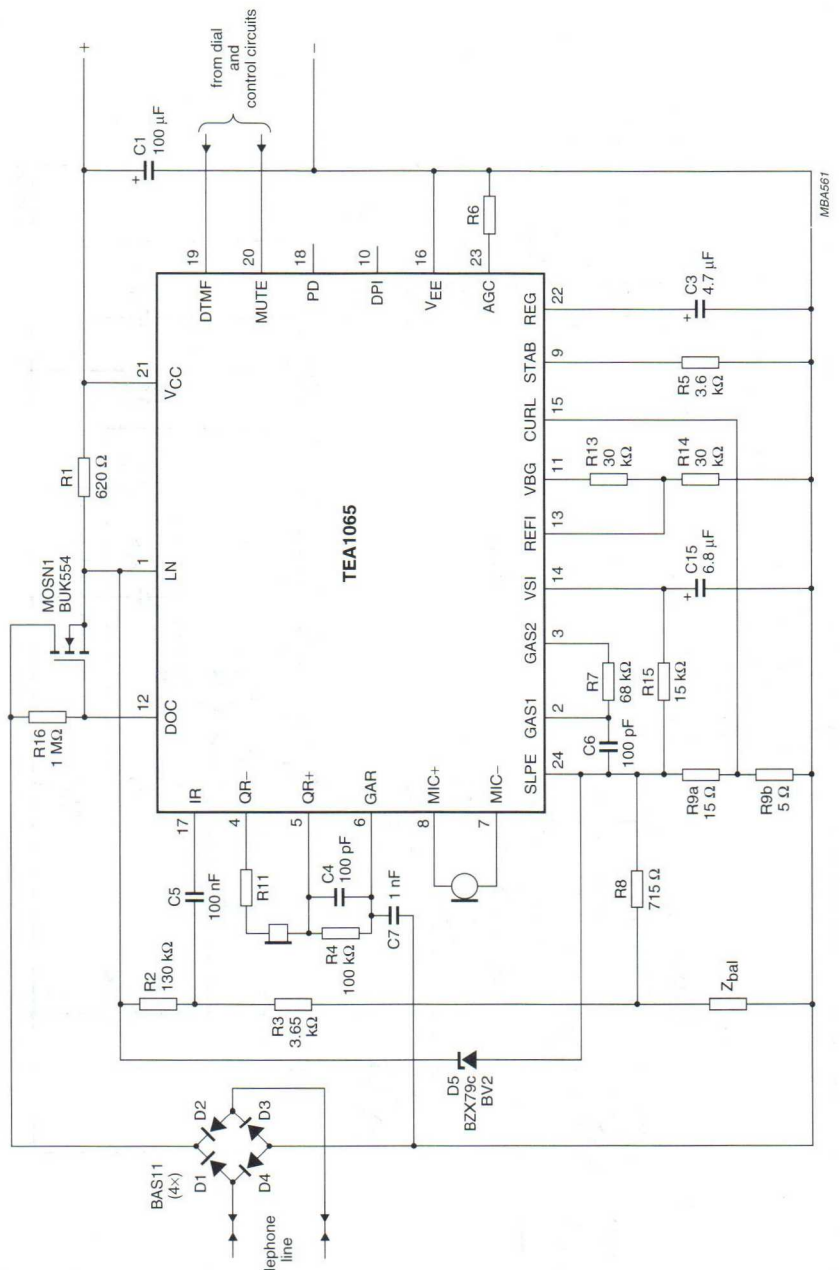
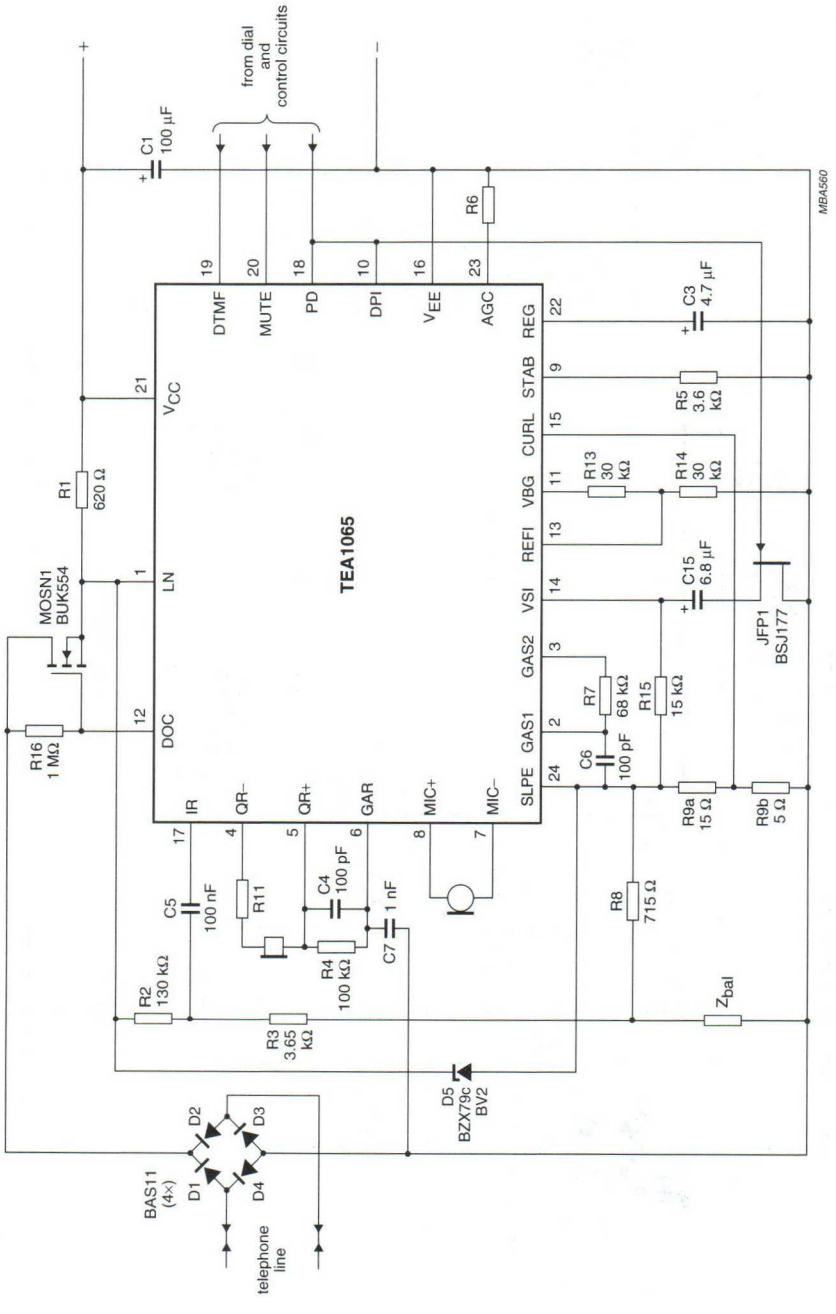


Fig.18 Typical application of the TEA1065, with a piezoelectric earpiece and DTMF dialling.



DTMF dialling requires a different protection arrangement.

Fig.19 Typical application of the TEA1065, with a piezoelectric earpiece and pulse dialling.

Versatile telephone transmission circuit with dialler interface

TEA1066T

FEATURES

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical low-impedance inputs for dynamic and magnetic microphones
- Symmetrical high-impedance inputs for piezoelectric microphone
- Asymmetrical high-impedance input for electret microphone
- Dual-tone multi-frequency (DTMF) signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (microphone and earpiece amplifiers)
- Gain control adaptable to exchange supply
- DC line voltage adjustment facility.

GENERAL DESCRIPTION

The TEA1066T is a bipolar integrated circuit that performs all speech and line interface functions required in fully electronic telephone sets. The circuit performs electronic switching between dialling and speech.

QUICK REFERENCE DATA

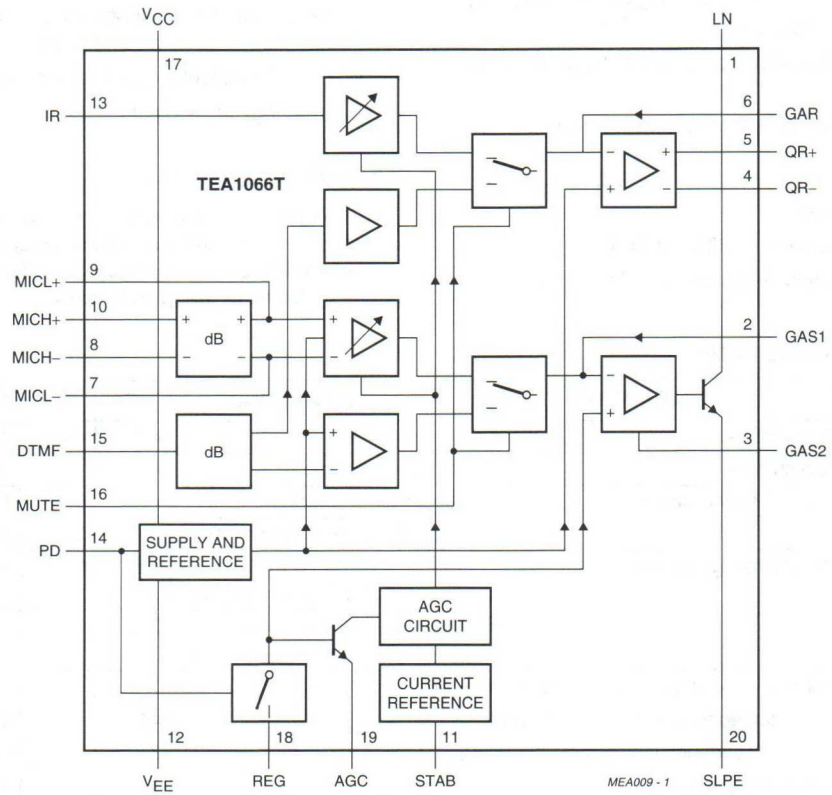
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	line voltage	I_{line} = 15 mA	4.25	4.45	4.65	V
I_{line}	line current	normal operation	10	–	140	mA
I_{CC}	internal supply current	power down input LOW	–	0.96	1.3	mA
		power down input HIGH	–	55	82	µA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA; MUTE input HIGH; I_p = 1.2 mA	2.8	3.05	–	V
		I_{line} = 15 mA; MUTE input HIGH; I_p = 1.7 mA	2.5	–	–	V
G_v	voltage gain range for microphone amplifier					
	low impedance inputs (pins 7 and 9)		44	–	60	dB
	high impedance inputs (pins 8 and 10)		30	–	46	dB
	receiving amplifier		17	–	39	dB
T_{amb}	operating ambient temperature		–25	–	+75	°C
Line loss compensation						
ΔG_v	gain control		5.5	5.9	6.3	dB
V_{exch}	exchange supply voltage		24	–	60	V
R_{exch}	exchange feeding bridge resistance		400	–	1000	Ω

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1066T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

MAINTENANCE TYPE
Not recommended for new designs

BLOCK DIAGRAM



The blocks marked 'dB' are attenuators.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
GAS1	2	gain adjustment transmitting amplifier
GAS2	3	gain adjustment transmitting amplifier
QR–	4	inverting output receiving amplifier
QR+	5	non-inverting output receiving amplifier
GAR	6	gain adjustment receiving amplifier
MICL–	7	inverting microphone input, low impedance
MICH–	8	inverting microphone input, high impedance
MICL+	9	non-inverting microphone input, low impedance
MICH+	10	non-inverting microphone input, high impedance
STAB	11	current stabilizer
V_{EE}	12	negative line terminal
IR	13	receiving amplifier input
PD	14	power-down input
DTMF	15	dual-tone multi-frequency input
MUTE	16	mute input
V_{CC}	17	supply voltage decoupling
REG	18	voltage regulator decoupling
AGC	19	automatic gain control input
SLPE	20	slope (DC resistance) adjustment

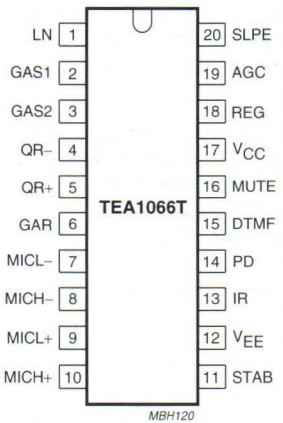


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Supplies: V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1066T and its peripheral circuits is usually obtained from the telephone line. The TEA1066T develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3.6 kΩ between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistance of the telephone line (R_{line}) and the DC voltage on the subscriber set (see Fig.7).

If the line current I_{line} exceeds the current I_{CC} + 0.5 mA required by the circuit itself (approximately 1 mA) plus the current I_p required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9$$

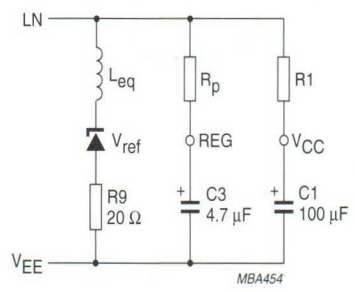
or

$$V_{LN} = V_{ref} + (I_{line} - I_{CC} - 0.5 \times 10^{-3}A - I_p) \times R9$$

where V_{ref} is an internally generated temperature compensated reference voltage of 4.2 V and R9 is an external resistor connected between SLPE and V_{EE}.

The preferred value for R9 is 20 Ω. Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics, side-tone level and the maximum output swing on LN.

Under normal conditions, when $I_{SLPE} >> I_{CC} + 0.5$ mA + I_p, the static behaviour of the circuit is that of a 4.2 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range, the dynamic impedance is largely determined by R1 (see Fig.3).



$R_p = 17.5$ kΩ
$L_{eq} = C3 \times R9 \times R_p$

Fig.3 Equivalent impedance circuit.

The internal reference voltage can be adjusted by means of an external resistor R_{VA}. This resistor, connected between LN and REG (pins 1 and 18), will decrease the internal reference voltage; when connected between REG and SLPE (pins 18 and 20) it will increase the internal reference voltage.

Current I_p, available from V_{CC} for supplying peripheral circuits, depends on external components and on the line current. Figure 8 shows this current for $V_{CC} > 2.2$ V and > 3 V, this being the minimum supply voltage for most CMOS circuits, including voltage drop for an enable diode. If MUTE is LOW, the available current is further reduced when the receiving amplifier is driven.

Microphone inputs MICL+, MICH+, MICL− and MICH− and amplification adjustment connections GAS1 and GAS2

The TEA1066T has symmetrical microphone inputs. The MICL+ and MICL− inputs are intended for low-sensitivity, low-impedance dynamic or magnetic microphones. The input impedance is 8.2 kΩ (2 × 4.1 kΩ) and its voltage gain is typically 52 dB. The MICH+ and MICH− inputs are intended for a piezoelectric microphone or an electret microphone with a built-in FET source follower. Its input impedance is 40.8 kΩ (2 × 20.4 kΩ) and its voltage gain is typical 38 dB.

The arrangements with the microphone types mentioned are shown in Fig.9.

The gain of the microphone amplifier in both types can be adjusted over a range of ±8 dB to suit the sensitivity of the transducer used. The gain is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 × C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier; a LOW level or an open circuit has the reverse effect. Switching the mute input will cause negligible clicks at the earpiece outputs and on the line.

Dual-tone multi frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typically 25.5 dB and varies with R7 in the same way as the gain of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR−.

These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig.10). Gain from IR to QR+ is typically 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces, which are suited for single-ended drive. By using both outputs (differential drive), the gain is increased by 6 dB and differential drive becomes possible. This feature can be used when the earpiece impedance exceeds 450 Ω (high-impedance dynamic, magnetic or piezoelectric earpieces).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak to RMS value is higher.

The receiving amplifier gain can be adjusted over a range of ±8 dB to suit the sensitivity of the transducer used. The gain is set by the external resistor R4 connected between GAR and QR+.

Two external capacitors, C4 = 100 pF and $C7 = 10 \times C4 = 1$ nF, are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order, low-pass filter. The 'cut-off' frequency corresponds with the time constant $R4 \times C4$.

Automatic gain control input AGC

Automatic line loss compensation is obtained by connecting a resistor R6 between AGC and V_{EE}. This automatic gain control varies the microphone amplifier gain and the receiving amplifier gain in accordance with the DC line current.

The control range is 6 dB. This corresponds with a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.11 and Table 1). Different values of R6 give the same ratio of line currents for start and end of the control range.

If automatic line loss compensation is not required, AGC may be left open. The amplifiers then all give their maximum gain as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input during the time of the loop break, which reduces the supply current from typically 1 mA to typically 55 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required PD may be left open.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal} (see Fig.14). Maximum compensation is obtained when the following conditions are fulfilled:

$$R9 \times R2 = R1\,(R3 + [R8//Z_{bal}]) \quad (1)$$

$$Z_{bal}/(Z_{bal} + R8) = Z_{line}/(Z_{line} + R1) \quad (2)$$

If fixed values are chosen for R1, R2, R3, and R9, then condition (1) will always be fulfilled, provided that $|R8//Z_{bal}| < R3$. To obtain optimum side-tone suppression, condition (2) has to be fulfilled, resulting in:

$Z_{bal} = (R8/R1)\,Z_{line} = k \times Z_{line}$, where k is a scale factor: $k = (R8/R1)$.

Scale factor k (dependent on the value of R8) must be chosen to meet the following criteria:

1. Compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
2. $|Z_{bal}//R8| << R3$
3. $|Z_{bal} + R8| >> R9$.

In practice, Z_{line} varies greatly with line length and cable type; consequently, an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal}/k equals the average line impedance.

Example: The balanced line impedance $|Z_{bal}|$ at which the optimum suppression is preset can be calculated by:

Assume Z_{line} = 210 Ω + (1265 Ω/140 nF), representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km). When k = 0.64, then R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-side-tone network for the TEA1060 family shown in Fig.4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier.

The attenuation is almost constant over the whole audio frequency range. Figure 5 shows a conventional Wheatstone bridge anti-side-tone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

The anti-side-tone network as used in the standard application (see Fig.13) attenuates the signal from the line with 32 dB. The attenuation is nearly flat over the audio-frequency range.

Instead of the previously-described special TEA1066 bridge, the conventional Wheatstone bridge configuration can be used as an alternative anti-side-tone circuit. Both bridge types can be used with either a resistive set impedance or a complex set impedance.

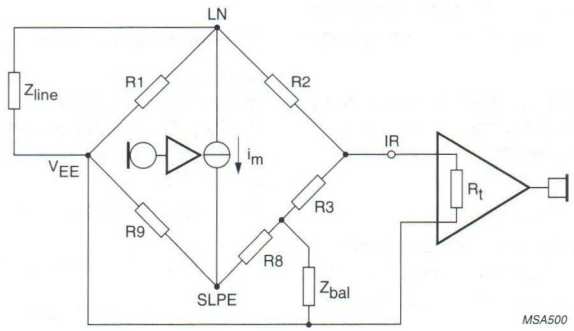


Fig.4 Equivalent circuit of TEA1060 family anti-side-tone bridge.

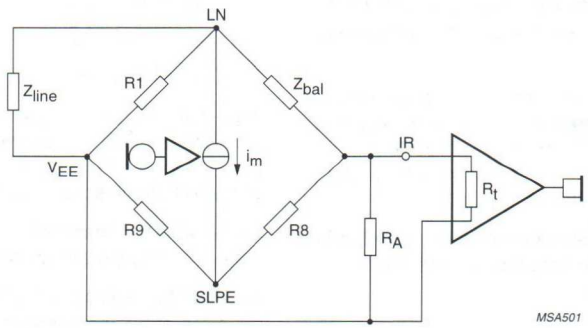


Fig.5 Equivalent circuit of an anti-side-tone network in a Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

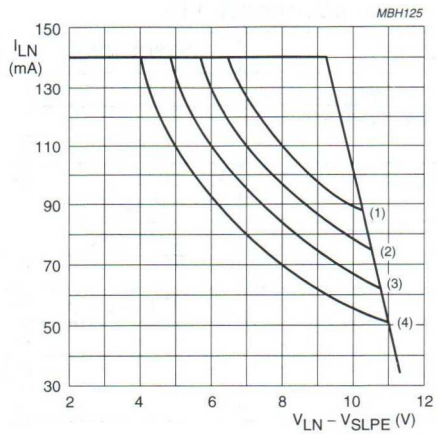
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		–	12	V
$V_{LN(R)}$	repetitive line voltage during switch-on or line interruption		–	13.2	V
$V_{LN(RM)}$	repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω; (Fig.10)	–	28	V
I_{line}	line current	R9 = 20 Ω; note 1	–	140	mA
V_n	voltage on any other pin		V_{EE} – 0.7	V_{CC} + 0.7	V
P_{tot}	total power dissipation	R9 = 20 Ω; note 2	–	555	mW
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C
T_j	junction temperature		–	125	°C

Notes

1. Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE (see Fig.6).
2. Calculated for the maximum ambient temperature specified, T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air mounted on glass epoxy board 41 × 19 × 1.5 mm	90	K/W



(1) T_{amb} = 45 °C; P_{tot} = 888 mW.
(2) T_{amb} = 55 °C; P_{tot} = 777 mW.
(3) T_{amb} = 65 °C; P_{tot} = 666 mW.
(4) T_{amb} = 75 °C; P_{tot} = 555 mW.

Fig.6 Safe operating area.

CHARACTERISTICS

I_{line} = 10 to 100 mA; V_{EE} = 0 V; f = 800 Hz; R9 = 20 Ω; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies: LN and V_{CC} (pins 1 and 17)						
V_{LN}	voltage drop over circuit between LN and V_{EE}	I_{line} = 5 mA	3.95	4.25	4.55	V
		I_{line} = 15 mA	4.25	4.45	4.65	V
		I_{line} = 100 mA	5.40	6.10	6.70	V
		I_{line} = 140 mA	–	–	7.50	V
$\Delta V_{LN}/\Delta T$	voltage drop variation with temperature	I_{line} = 15 mA	−4	−2	0	mV/K
V_{LN}	voltage drop over circuit between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA; R_{VA} = R1-18 = 68 kΩ	3.50	3.80	4.05	V
		I_{line} = 15 mA; R_{VA} = R18-20 = 39 kΩ	4.70	5	5.30	V
I_{CC}	supply current	PD = LOW; V_{CC} = 2.8 V	–	0.96	1.30	mA
		PD = HIGH; V_{CC} = 2.8 V	–	55	82	µA
V_{CC}	supply voltage available for peripheral circuits	I_{line} = 15 mA; MUTE = HIGH; I_p = 0 mA	3.50	3.75	–	V
		I_{line} = 15 mA; MUTE = HIGH; I_p = 1.2 mA	2.80	3.05	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Microphone inputs MICL+ and MICL–; MICH+ and MICH–						
$\|Z_i\|$	input impedance					
	MICL+ (pin 9); MICL– (pin 7)		3.3	4.1	4.9	kΩ
	MICH+ (pin 10); MICH– (pin 8)		16.5	20.4	24.5	kΩ
CMRR	common mode rejection ratio		–	82	–	dB
G_v	voltage gain	I_{line} = 15 mA; R7 = 68 Ω				
	MICL+/MICL– to LN		51	52	53	dB
	MICH+/MICH– to LN		37	38	39	dB
ΔG_{vf}	gain variation with frequency at f = 300 Hz and 3400 Hz	with respect to 800 Hz	–0.5	±0.2	+0.5	dB
ΔG_{vT}	gain variation with temperature at T_{amb} = –25 °C and +75 °C	I_{line} = 50 mA; with respect to 800 Hz	–	±0.2	–	dB
Dual-tone multi-frequency input DTMF (pin 15)						
$\|Z_i\|$	input impedance		16.8	20.7	24.6	kΩ
G_v	voltage gain from DTMF to LN	I_{line} = 15 mA; R7= 68 kΩ	24.5	25.5	26.5	dB
ΔG_{vf}	gain variation with frequency at f = 300 Hz and 3400 Hz	with respect to 800 Hz	–0.5	±0.2	+0.5	dB
ΔG_{vT}	gain variation with temperature at T_{amb} = –25 °C and +75 °C	I_{line} = 50 mA; with respect to 25 °C	–	±0.2	–	dB
Gain adjustment connections GAS1 and GAS2 (pins 2 and 3)						
ΔG_v	gain variation with R7, transmitting amplifier		–8	–	+8	dB
Transmitting amplifier output LN (pin 1)						
$V_{LN(rms)}$	output voltage (RMS value)	I_{line} = 15 mA; THD = 2%	1.9	2.3	–	V
		I_{line} = 15 mA; THD = 10%	–	2.6	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; microphone inputs open; psophometrically weighted (P53 curve)	–	–70	–	dBmp
Receiving amplifier input IR (pin 13)						
$\|Z_i\|$	input impedance		17	21	25	kΩ
Receiving amplifier outputs QR+ and QR– (pins 5 and 4)						
$\|Z_o\|$	output impedance	single-ended	–	4	–	Ω
G_v	voltage gain from IR to QR+ or QR–	I_{line} = 15 mA; R4 = 100 kΩ				
		single-ended; R_L = 300 Ω	24	25	26	dB
		differential; R_L = 600 Ω	30	31	32	dB
ΔG_{vf}	gain variation with frequency at f = 300 Hz and 3400 Hz	with respect to 800 Hz	–0.5	±0.2	+0.5	dB
ΔG_{vT}	gain variation with temperature at T_{amb} = –25 °C and +75 °C	I_{line} = 50 mA; with respect to 25 °C	–	±0.2	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{o(rms)}$	output voltage (RMS value)	sine-wave drive; I_{line} = 15 mA; I_p = 0 mA; THD = 2%; R4 = 100 kΩ				
		single-ended; R_L = 150 Ω	0.30	0.38	–	V
		single-ended; R_L = 450 Ω	0.40	0.52	–	V
		differential; C_L = 47 nF; R_{series} = 100 Ω; f = 3400 Hz	0.80	1.0	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; pin 13 (IR) open; psophometrically weighted (P53 curve)				
		single-ended; R_L = 300 Ω	–	50	–	μV
		differential; R_L = 600 Ω	–	100	–	μV
Gain adjustment GAR (pin 6)						
ΔG_v	gain variation with R4 connected between pin 6 and pin 5 receiving amplifier		–8	–	+8	dB
MUTE input (pin 16)						
V_{IH}	HIGH level input voltage		1.50	–	V_{CC}	V
V_{IL}	LOW level input voltage		–	–	0.3	V
I_{MUTE}	input current		–	5	10	μA
ΔG_v	voltage gain reduction between MICL+ (pin 9) and MICL– (pin 7) to LN (pin 1)	MUTE = HIGH	–	70	–	dB
G_v	voltage gain from DTMF to QR+ or QR–	MUTE = HIGH; R4 = 100 kΩ; single-ended; R_L = 300 Ω	–21	–19	–17	dB
Power-down input PD (pin 14)						
V_{IH}	HIGH level input voltage		1.5	–	V_{CC}	V
V_{IL}	LOW level input voltage		–	–	0.3	V
I_{PD}	input current in power-down condition		–	5	10	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic gain control input AGC (pin 19)						
ΔG_v	gain control range from IR to QR+/QR– and from MIC+/MIC– to LN	I_{line} = 70 mA; R6 = 110 kΩ between AGC and V_{EE}	–5.5	–5.9	–6.3	dB
$I_{line(H)}$	highest line current for maximum gain	R6 = 110 kΩ between AGC and V_{EE}	–	23	–	mA
$I_{line(L)}$	lowest line current for minimum gain	R6 = 110 kΩ between AGC and V_{EE}	–	61	–	mA
ΔG_v	voltage gain variation	between I_{line} = 15 mA and I_{line} = 35 mA; R6 = 110 kΩ between AGC and V_{EE}	–1.0	–1.5	–2.0	dB

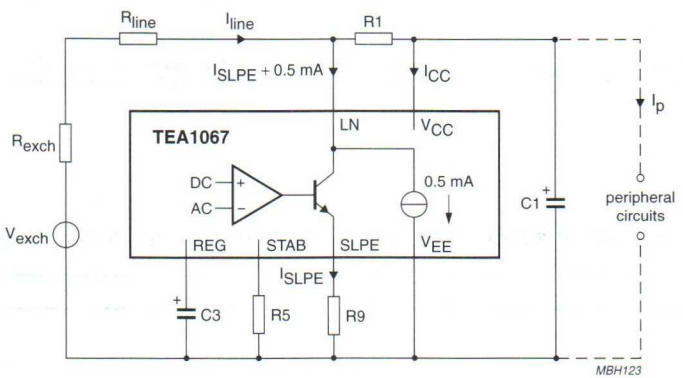
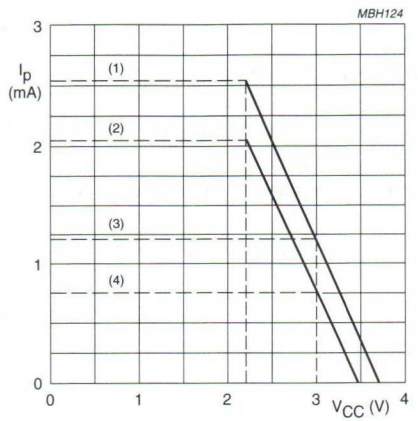


Fig.7 Supply arrangement.



Curves (1) and (3) are valid when the receiving amplifier is not driven or when MUTE = HIGH. Curves (2) and (4) are valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)}$ = 150 mV, R_L = 150 Ω (asymmetrical). I_{line} = 15 mA; V_{LN} = 4.45 V; R1 = 620 Ω and R9 = 20 Ω.

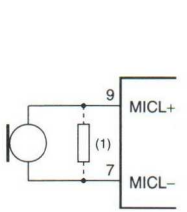
(1) I_p = 2.55 mA.

(2) I_p = 2.1 mA.

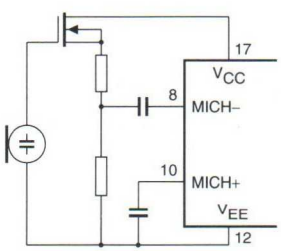
(3) I_p = 1.2 mA.

(4) I_p = 0.75 mA.

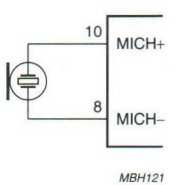
Fig.8 Typical current I_p available from V_{CC} for external (peripheral) circuitry with V_{CC} > 2.2 V and V_{CC} > 3 V.



a. Magnetic or dynamic microphone.



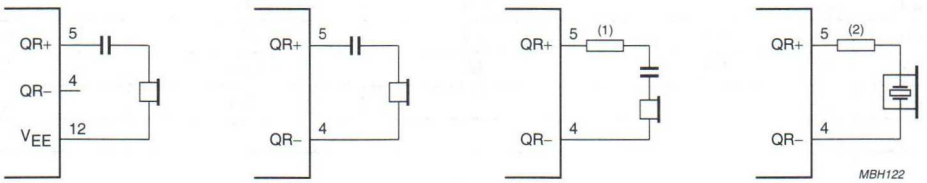
b. Electret microphone.



c. piezoelectric microphone.

(1) May be connected to lower the terminating impedance.

Fig.9 Alternative microphone arrangements.



a. Dynamic earpiece with less than 450 Ω impedance.

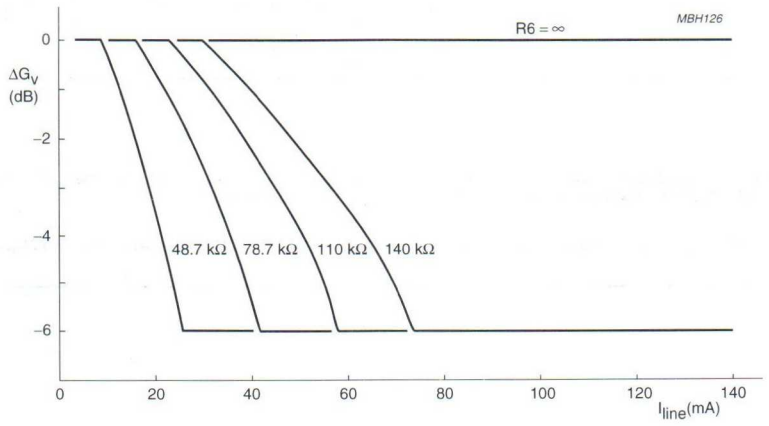
b. Dynamic earpiece with more than 450 Ω impedance.

c. Magnetic earpiece with more than 450 Ω impedance.

d. piezoelectric earpiece.

(1) May be connected to prevent distortion (inductive load).
(2) Required to increase the phase margin (capacitive load).

Fig.10 Alternative receiver arrangements.

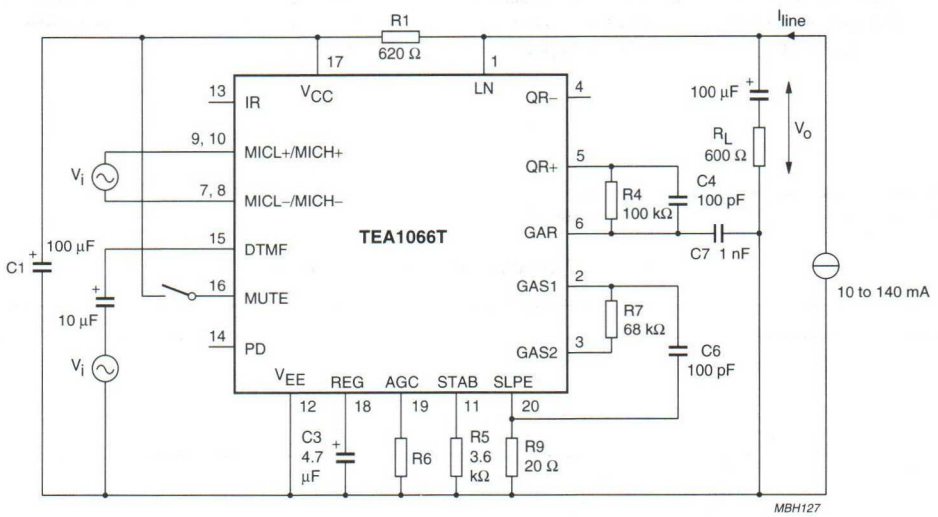


R9 = 20 Ω.

Fig.11 Variation of gain with line current, with R6 as a parameter.

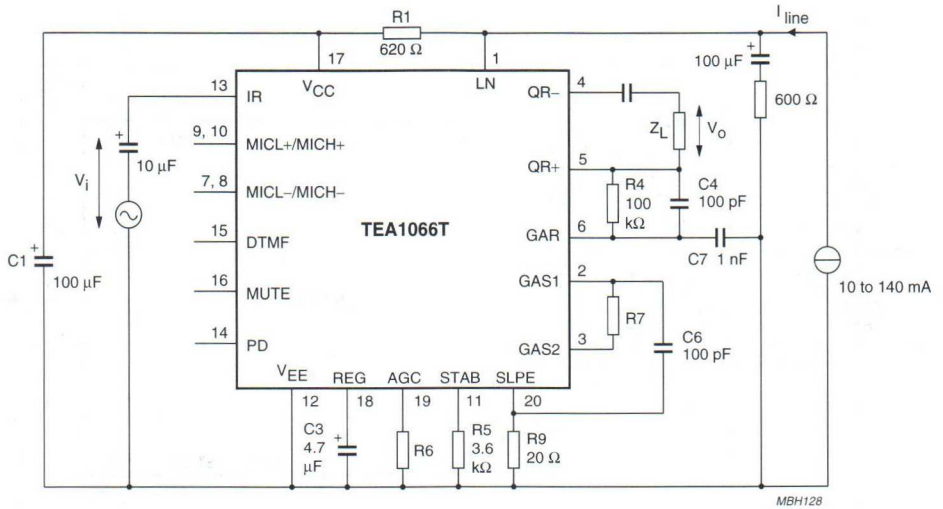
Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}; R9 = 20 Ω

V_{exch} (V)	R6 (kΩ)			
	R_{exch} = 400 Ω	R_{exch} = 600 Ω	R_{exch} = 800 Ω	R_{exch} = 1000 Ω
24	61.9	48.7	X	X
36	100	78.7	68	60.4
48	140	110	93.1	82
60	X	X	120	102



Voltage gain is defined as: $G_v = 20 \log |V_o/V_i|$. For measuring the gain from MICL+, MICL− or MICH+ and MICH−, the MUTE input should be LOW or open; for measuring the DTMF input, MUTE should be HIGH. Inputs not under test should be open.

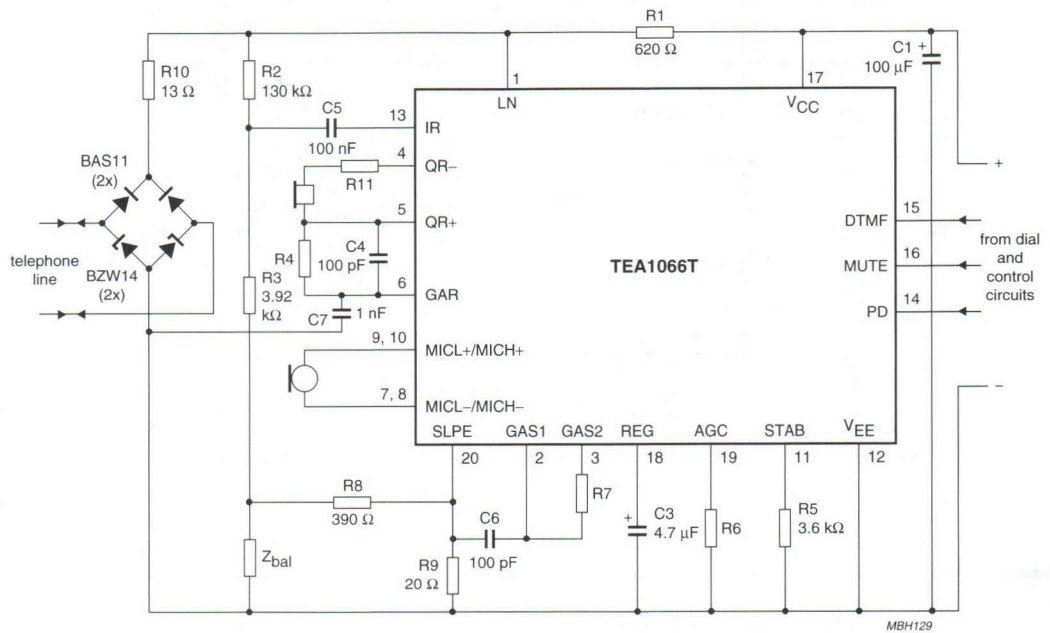
Fig.12 Test circuit for defining voltage gain of MICL+, MICL−, MICH+ and MICH− DTMF inputs.



Voltage gain is defined as: $G_v = 20 \log |V_o/V_i|$.

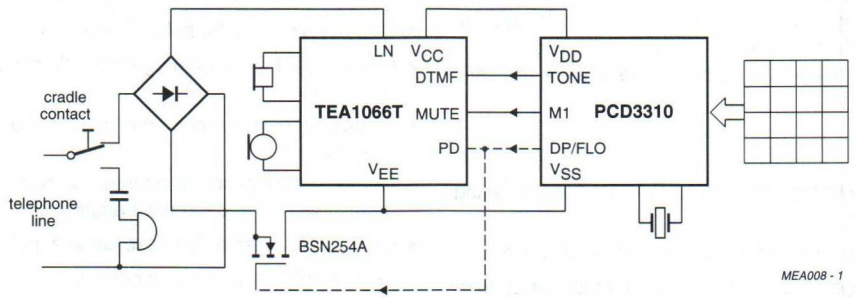
Fig.13 Test circuit for defining voltage gain of the receiving amplifier.

APPLICATION INFORMATION



Typical application of the TEA1066, shown with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

Fig.14 Application diagram.



The dashed lines show an optional flash (register recall by timed loop break).

Fig.15 DTMF pulse set with CMOS PCD3310 dialling circuit.

Low voltage versatile telephone transmission circuit with dialler interface

TEA1067

GENERAL DESCRIPTION

The TEA1067 is a bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech. The circuit is able to operate down to a DC line voltage of 1.6 V (with reduced performance) to facilitate the use of more telephone sets in parallel.

Features

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable static resistance
- Provides supply with limited current for external circuitry
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line current dependent line loss compensation facility for microphone and earpiece amplifiers
- Gain control adaptable to exchange supply
- DC line voltage adjustment capability

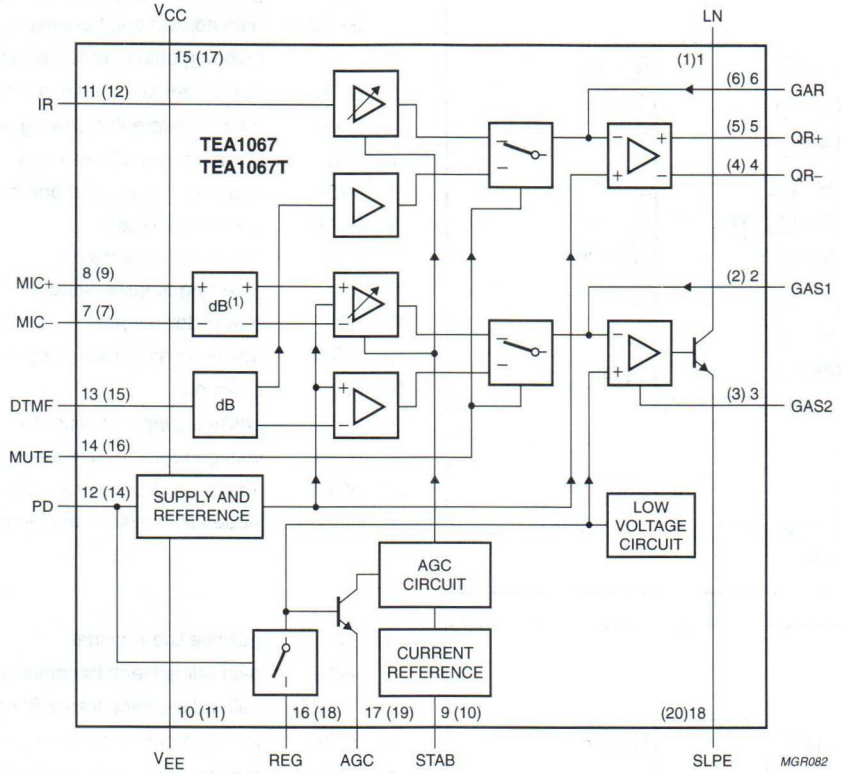
QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Line voltage	I_{line} = 15 mA	V_{LN}	3.65	3.9	4.15	V
Line current operating range	normal operation					
TEA1067		I_{line}	11	–	140	mA
TEA1067T		I_{line}	11	–	140	mA
with reduced performance		I_{line}	1	–	11	mA
Internal supply current	power down					
	input LOW	I_{CC}	–	1	1.35	mA
	input HIGH	I_{CC}	–	55	82	μA
Supply voltage for peripherals	I_{line} = 15 mA; I_p = 1.4 mA;					
	mute input HIGH	V_{CC}	2.2	2.4	–	V
	I_{line} = 15 mA; I_p = 0.9 mA;					
	mute input HIGH	V_{CC}	2.5	–	–	V
Voltage gain range						
microphone amplifier		G_v	44	–	52	dB
receiving amplifier		G_v	20	–	45	dB
Line loss compensation						
gain control range		ΔG_v	5.5	5.9	6.3	dB
Exchange supply voltage range		V_{exch}	36	–	60	V
Exchange feeding bridge						
resistance range		R_{exch}	0.4	–	1	kΩ

PACKAGE OUTLINES

TEA1067: 18-lead DIL; plastic (SOT102). SOT102-1; 1998 Jun 18.

TEA1067T: 20-lead mini-pack; plastic (SO20; SOT163A). SOT163-1; 1998 Jun 18.



Figures in parenthesis refer to TEA1067T.

Fig.1 Block diagram.

Low voltage versatile telephone transmission circuit with dialler interface

TEA1067

PINNING

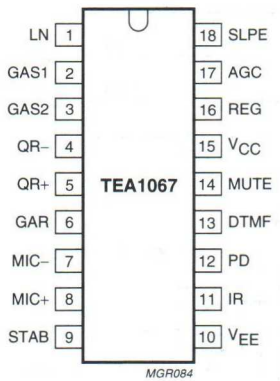


Fig.2 Pinning diagram for TEA1067 18-lead DIL version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (DC resistance) adjustment

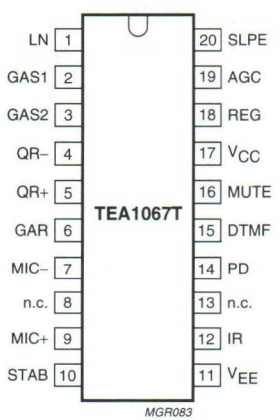


Fig.3 Pinning diagram for TEA1067T 20-lead mini-pack version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment, receiving amplifier
7	MIC–	inverting microphone input
8	n.c.	not connected
9	MIC+	non-inverting microphone input
10	STAB	current stabilizer
11	V_{EE}	negative line terminal
12	IR	receiving amplifier input
13	n.c.	not connected
14	PD	power-down input
15	DTMF	dual-tone multi-frequency input
16	MUTE	mute input
17	V_{CC}	positive supply decoupling
18	REG	voltage regulator decoupling
19	AGC	automatic gain control input
20	SLPE	slope (DC resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1067 and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external circuits e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V_{EE} while the internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current drawn by the device will vary in accordance with varying values of the exchange voltage (V_{exch}), the feeding bridge resistance (R_{exch}), and the DC resistance of the telephone line (R_{line}).

The TEA1067 has an internal current stabilizer working at a level determined by a 3.6 kΩ resistor connected between STAB and V_{EE} (see Fig.7). When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p) the excess current is shunted to V_{EE} via LN.
The regulated voltage on the line terminal (V_{LN}) can be calculated as:

$V_{LN} = V_{ref} + I_{SLPE} \times R9$; or
$V_{LN} = V_{ref} + [(I_{line} - I_{CC} - 0.5 \times 10^{-3}\ A) - I_p] \times R9$

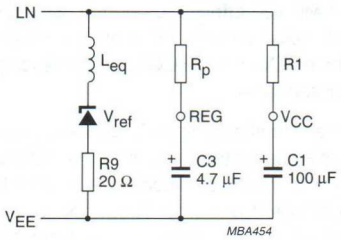
Where V_{ref} is an internally generated temperature compensated reference voltage of 3.6 V and R9 is an external resistor connected between SLPE and V_{EE}.

In normal use the value of R9 would be 20 Ω. Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics, side-tone level and maximum output swing on LN, and the DC characteristics (especially at the lower voltages).

Under normal conditions, when $I_{SLPE} >> I_{CC} + 0.5\ mA + I_p$, the static behaviour of the circuit is that of a 3.6 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1. Fig.4 shows the equivalent impedance of the circuit.

At line currents below 9 mA the internal reference voltage is automatically adjusted to a lower value (typically 1.6 V at 1 mA). This means that the operation of more sets in parallel is possible with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. With line currents below 9 mA the circuit has limited sending and receiving levels. The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor connected between LN and REG will decrease the internal reference voltage, connected between REG and SLPE it will increase the internal reference voltage.

Current (I_p) available from V_{CC} for peripheral circuits depends on the external components used. Fig.10 shows this current for $V_{CC} > 2.2$ V. If MUTE is LOW when the receiving amplifier is driven the available current is further reduced. Current availability can be increased by connecting the supply IC (TEA1081) in parallel with R1, as shown in Fig.17 (c), or by increasing the DC line voltage by means of an external resistor (R_{VA}) connected between REG and SLPE.



$R_p = 16.2\ k\Omega$
$L_{eq} = C3 \times R9 \times R_p$

Fig.4 Equivalent impedance circuit.

Microphone inputs (MIC+ and MIC–) and gain adjustment pins (GAS1 and GAS2)

The TEA1067 has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 × 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ, see Fig.14). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) microphones can be used. Microphone arrangements are shown in Fig.11.

The gain of the microphone amplifier can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer in use. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2. Stability is ensured by the external capacitor C6 which is connected between GAS1 and SLPE. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The cut-off frequency corresponds to the time constant R7 × C6.

Mute input (MUTE)

When MUTE is HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when MUTE is LOW or open-circuit. MUTE switching causes only negligible clicking on the earpiece outputs and line. If the number of parallel sets in use causes a drop in line current to below 6 mA the speech amplifiers remain active independent to the DC level applied to the MUTE input.

Dual-tone multi-frequency input (DTMF)

When the DTMF input is enabled dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving Amplifier (IR, QR+, QR– and GAR)

The receiving amplifier has one input (IR), one non-inverting complementary output (QR+) and an inverting complementary output (QR–). These outputs may be used for single-ended or differential drive depending on the sensitivity and type of earpiece used (see Fig.12). IR to QR + gain is typically 31 dB (when R4 = 100 kΩ), this is sufficient for low-impedance magnetic or dynamic microphones which are suited for single-ended drive. Using both outputs for differential drive gives an additional gain of 6 dB. This feature can be used when the earpiece impedance exceeds 450 Ω (high-impedance dynamic or piezoelectric types).

The receiving amplifier gain can be adjusted between 20 and 39 dB with single-ended drive and between 26 and 45 dB with differential drive, to match the sensitivity of the transducer in use. The gain is set with the value of R4 which is connected between GAR and QR+. Overall receive gain between LN and QR+ is calculated by substracting the anti-sidetone network attenuation (32 dB) from the amplifier gain. Two external capacitors C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 × the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 × C4.
The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

Automatic gain control input (AGC)

Automatic line loss compensation is achieved by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.9 dB. This corresponds to a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation 1.2 dB/km. Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.13 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line loss compensation is required the AGC may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

Power-down input (PD)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted. During these interruptions the telephone line provides no power for the transmission circuit or circuits supplied by V_{CC}. The charge held on C1 will bridge these gaps. This bridging is made easier by a HIGH level on the PD input which reduces the typical supply current from 1 mA to 55 µA and switches off the voltage regulator preventing discharge through LN. When PD is HIGH the capacitor at REG is disconnected with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required PD may be left open-circuit.

Side-tone suppression

The anti-sidetone network, $R1//Z_{line}$, R2, R3, R9 and Z_{bal}, (see Fig.5) suppresses transmitted signal in the earpiece. Compensation is maximum when the following conditions are fulfilled:

(a) $R9 \times R2 = R1\ (R3 + [R8//Z_{bal}])$;

(b) $(Z_{bal} / [Z_{bal} + R8]) = (Z_{line} / [Z_{line} + R1])$

If fixed values are chosen for R1, R2, R3, and R9 then condition (a) will always be fulfilled when $|R8//Z_{bal}| << R3$. To obtain optimum side-tone suppression condition (b) has to be fulfilled resulting in:

$Z_{bal} = (R8/R1)\ Z_{line} = k.Z_{line}$ where k is a scale factor; $k = (R8/R1)$

The scale factor (k), dependent on the value of R8, is chosen to meet the following criteria:

(a) Compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}

(b) $|Z_{bal}//R8| << R3$ to fulfil condition (a) and thus ensuring correct anti-sidetone bridge operation

(c) $|Z_{bal} + R8| >> R9$ to avoid influencing the transmitter gain

In practice Z_{line} varies considerably with the line type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.

Example

The line balance impedance (Z_{bal}) at which the optimum suppression is present can be calculated by:
suppose Z_{line} = 210 Ω + (1265 Ω//140 nF), representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).
When k = 0.64 then R8 = 390 Ω;
Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig.5 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. Fig.6 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

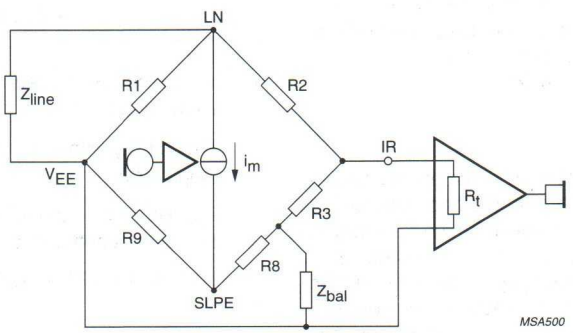


Fig.5 Equivalent circuit of TEA1060 anti-sidetone bridge.

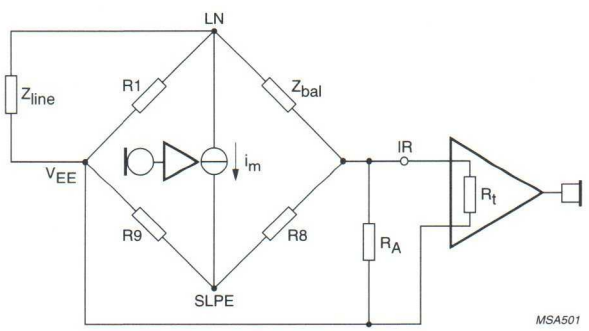


Fig.6 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

More information can be found in the designer guide; 9398 341 10011

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Positive continuous line voltage		V_{LN}	–	12	V
Repetitive line voltage during switch-on line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig.16)	V_{LN}	–	28	V
Line current TEA1067 (note 1)	R9 = 20 Ω	I_{line}	–	140	mA
Line current TEA1067T (note 1)	R9 = 20 Ω	I_{line}	–	140	mA
Voltage on all other pins		V_i	–	V_{CC} + 0.7	V
		$-V_i$	–	0.7	V
Total power dissipation (note 2)	R9 = 20 Ω				
TEA1067		P_{tot}	–	769	mW
TEA1067T		P_{tot}	–	550	mW
Storage temperature range		T_{stg}	−40	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

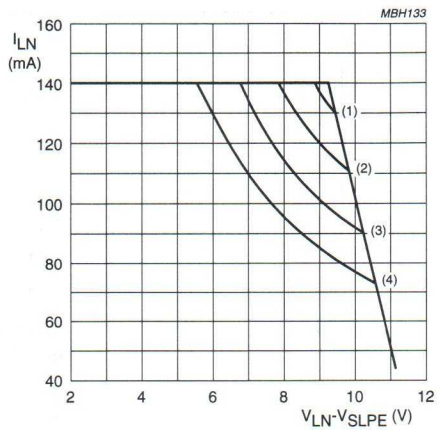
Notes

1. Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs 7 and 8 to determine the current as a function of the required voltage and the temperature.
2. Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

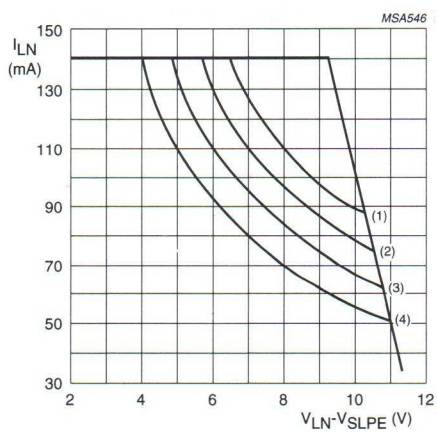
From junction to ambient in free air

TEA1067	$R_{th\ j\text{-}a}$	typ.	65	K/W
TEA1067T mounted on glass epoxy board 41 × 19 × 1.5 mm	$R_{th\ j\text{-}a}$	typ.	90	K/W



	T_{amb}	P_{tot}
(1)	45 °C	1231 mW
(2)	55 °C	1077 mW
(3)	65 °C	923 mW
(4)	75 °C	769 mW

Fig.7 TEA1067 safe operating area.



	T_{amb}	P_{tot}
(1)	45 °C	888 mW
(2)	55 °C	777 mW
(3)	65 °C	666 mW
(4)	75 °C	555 mW

Fig.8 TEA1067T safe operating area.

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified

PARAMETER	CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply; LN and V_{CC}						
Voltage drop over circuit, between LN and V_{EE}	microphone inputs open					
	I_{line} = 1 mA	V_{LN}	–	1.6	–	V
	I_{line} = 4 mA	V_{LN}	1.75	2.0	2.25	V
	I_{line} = 7 mA	V_{LN}	2.25	2.8	3.35	V
	I_{line} = 11 mA	V_{LN}	3.55	3.8	4.05	V
	I_{line} = 15 mA	V_{LN}	3.65	3.9	4.15	V
	I_{line} = 100 mA	V_{LN}	4.9	5.6	6.5	V
	I_{line} = 140 mA	V_{LN}	–	–	7.5	V
Variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	–3	–1	1	mV/K
Voltage drop over circuit, between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA; R_{VA} (LN to REG) = 68 kΩ		3.1	3.4	3.7	V
	I_{line} = 15 mA; R_{VA} (REG to SLPE) = 39 kΩ		4.2	4.5	4.8	V
Supply current	PD = LOW; V_{CC} = 2.8 V	I_{CC}	–	1.0	1.35	mA
Supply current	PD = HIGH; V_{CC} = 2.8 V	I_{CC}	–	55	82	µA
Supply voltage available for peripheral circuitry	I_{line} = 15 mA; MUTE = HIGH					
	I_p = 1.4 mA	V_{CC}	2.2	2.4	–	V
	I_p = 0 mA	V_{CC}	2.95	3.2	–	V
Microphone inputs MIC+ and MIC–						
Input impedance (differential) between MIC– and MIC+		$\|Z_i\|$	51	64	77	kΩ
Input impedance (single-ended) MIC– or MIC+ to V_{EE}		$\|Z_i\|$	25.5	32	38.5	kΩ
Common mode rejection ratio		k_{CMR}	–	82	–	dB
Voltage gain MIC+/MIC– to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	51	52	53	dB

PARAMETER	CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t 800 Hz	ΔG_{vf}	−0.5	± 0.2	+0.5	dB
Gain variation with temperature at −25 °C and + 75 °C	w.r.t. 25 °C without R6; I_{line} = 50 mA	ΔG_{vT}	–	± 0.2	–	dB
Dual-tone multi-frequency input DTMF						
Input impedance		$\lvert Z_i \rvert$	16.8	20.7	24.6	kΩ
Voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	24.5	25.5	26.5	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	±0.2	+0.5	dB
Gain variation with temperature at −25 °C and +75 °C	w.r.t. 25 °C I_{line} = 50 mA	ΔG_{vT}	–	±0.2	–	dB
Gain adjustment GAS1 and GAS2						
Gain variation of the transmitting amplifier by varying R7 between GAS1 and GAS2		ΔG_v	−8	–	0	dB
Sending amplifier output LN						
Output voltage	I_{line} = 15 mA					
	THD = 2%	$V_{LN(rms)}$	–	1.9	–	V
	THD = 10%	$V_{LN(rms)}$	1.9	2.2	–	V
	I_{line} = 4 mA; THD = 10%	$V_{LN(rms)}$	–	0.8	–	V
	I_{line} = 7 mA; THD = 10%	$V_{LN(rms)}$	–	1.4	–	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC− and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	−72	–	dBmp
Receiving amplifier input IR						
Input impedance		$\lvert Z_i \rvert$	17	21	25	kΩ

PARAMETER	CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Receiving amplifier outputs QR+ and QR–						
Output impedance (single-ended)		$\|Z_o\|$	–	4	–	Ω
Voltage gain from IR to QR+ or QR–	I_{line} = 15 mA; R4 = 100 kΩ					
single-ended	R_L (from QR+ or QR–) = 300 Ω	G_v	30	31	32	dB
differential	R_L (from QR+ or QR–) = 600 Ω	G_v	36	37	38	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	–0.5	–0.2	0	dB
Gain variation with temperature at –25 °C and +75 °C	w.r.t. 25 °C without R6; I_{line} = 50 mA	ΔG_{vT}	–	±0.2	–	dB
Output voltage	sinewave drive; I_{line} = 15 mA; I_p = 0 mA; THD = 2%; R4 = 100 kΩ					
single-ended	RL = 150 Ω	$V_{o(rms)}$	0.25	0.29	–	V
	RL = 450 Ω	$V_{o(rms)}$	0.45	0.55	–	V
differential	f = 3400 Hz; series R = 100 Ω; C_L = 47 nF	$V_{o(rms)}$	0.65	0.80	–	V
Output voltage	THD = 10%; RL = 150 Ω; R4 = 100 kΩ					
	I_{line} = 4 mA	$V_{o(rms)}$	–	15	–	mV
	I_{line} = 7 mA	$V_{o(rms)}$	–	130	–	mV
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted; (P53 curve)					
single-ended	RL = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential	RL = 600 Ω	$V_{no(rms)}$	–	100	–	μV

PARAMETER	CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Gain adjustment GAR						
Gain variation of receiving amplifier achievable by varying R4 between GAR and QR		ΔG_v	−11	–	+8	dB
Mute input						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{MUTE}	–	8	15	μA
Gain reduction MIC+ or MIC− to LN	MUTE = HIGH	ΔG_v	–	70	–	dB
Voltage gain from DTMF to QR+ or QR−	MUTE = HIGH; R4 = 100 kΩ; single-ended; R_L = 300 Ω	G_v	−21	−19	−17	dB
Power-down input PD						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{PD}	–	5	10	μA
Automatic gain control input AGC						
Controlling the gain from IR to QR+/QR− and the gain from MIC+/MIC− to LN; R6 between AGC and V_{EE}	R6 = 110 kΩ					
Gain control range	I_{line} = 70 mA	ΔG_v	−5.5	−5.9	−6.3	dB
Highest line current for maximum gain		I_{line}	–	23	–	mA
Minimum line current for minimum gain		I_{line}	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA		ΔG_v	−1.0	−1.5	−2.0	dB

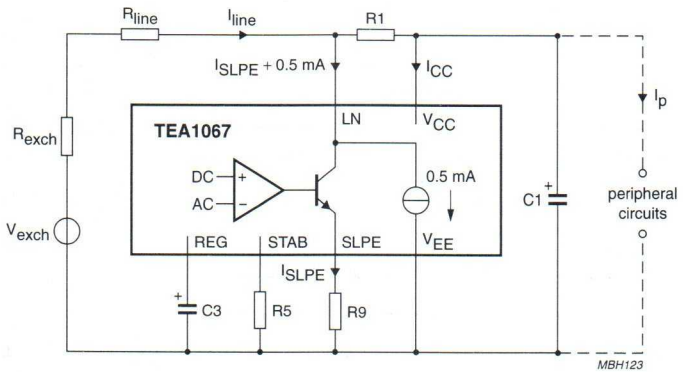
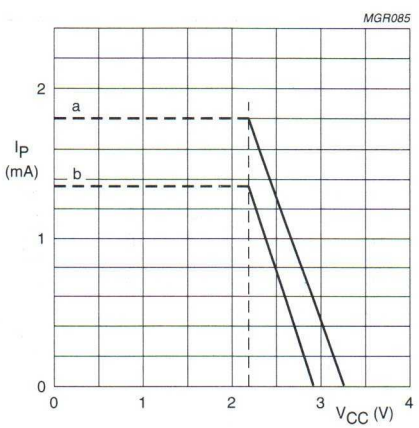


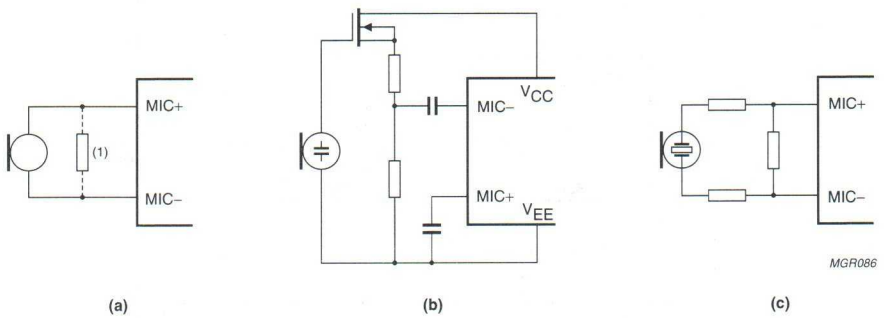
Fig.9 Supply arrangement.



Curve (a) is valid when the receiving amplifier is not driven or when MUTE = HIGH, curve (b) is valid when MUTE = LOW and the receiving amplifier is driven; $V_{o(rms)}$ = 150 mV, R_L = 150 Ω asymmetrical. The supply possibilities can be increased simply by setting the voltage drop over the circuit V_{LN} to a higher value by means of resistor R_{VA} connected between REG and SLPE.

(a) I_p = 1.8 mA
(b) I_p = 1.35 mA
I_{line} = 15 mA at V_{LN} = 3.9 V
R1 = 620 Ω and R9 = 20 Ω.

Fig.10 Typical current I_p available from V_{CC} for peripheral circuitry with $V_{CC} \geq 2.2$ V.

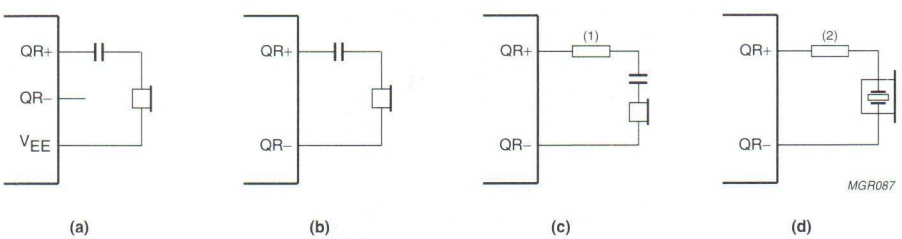


(a) Magnetic or dynamic microphone. The resistor marked (1) may be connected to decrease the terminating impedance.

(b) Electret microphone.

(c) Piezoelectric microphone.

Fig.11 Alternative microphone arrangements.



(a) Dynamic earpiece with less than 450 Ω impedance.

(b) Dynamic earpiece with more than 450 Ω impedance.

(c) Magnetic earpiece with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load).

(d) Piezoelectric earpiece. The resistor marked (2) is required to increase the phase margin (capacitive load).

Fig.12 Alternative receiver arrangements.

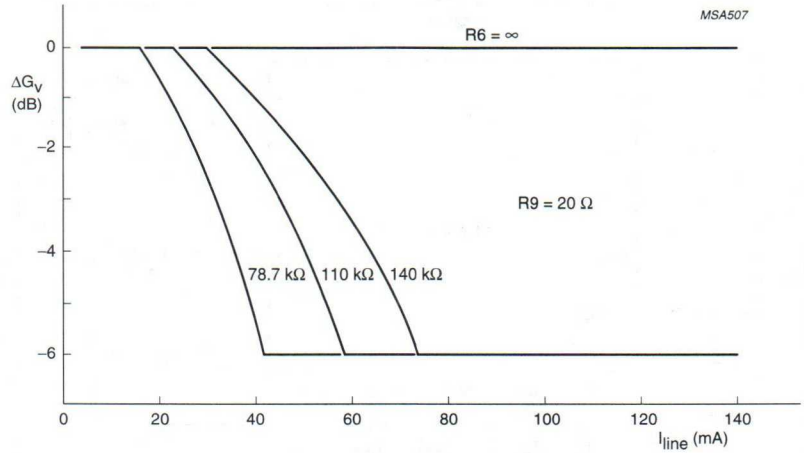
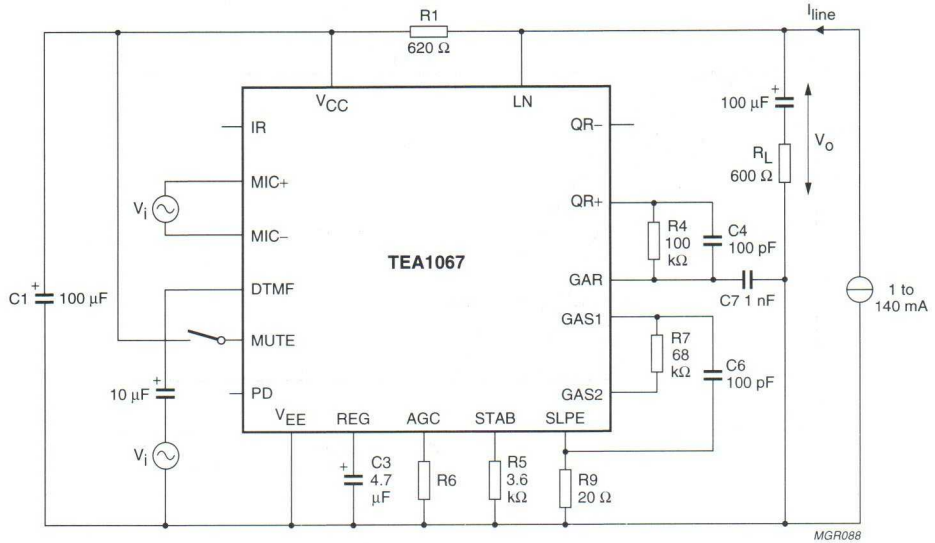


Fig.13 Variation of gain with line current, with R6 as a parameter.

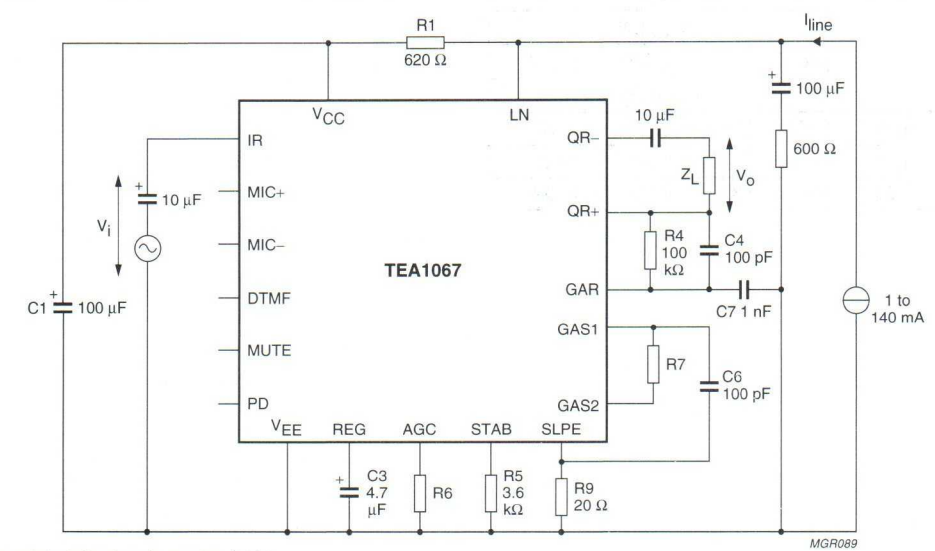
Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	36	100	78.7	X	X
	48	140	110	93.1	82
	60	X	X	120	102



Voltage gain is defined as: $G_v = 20 \log |V_o/V_i|$. For measuring the gain from MIC+ and MIC– the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

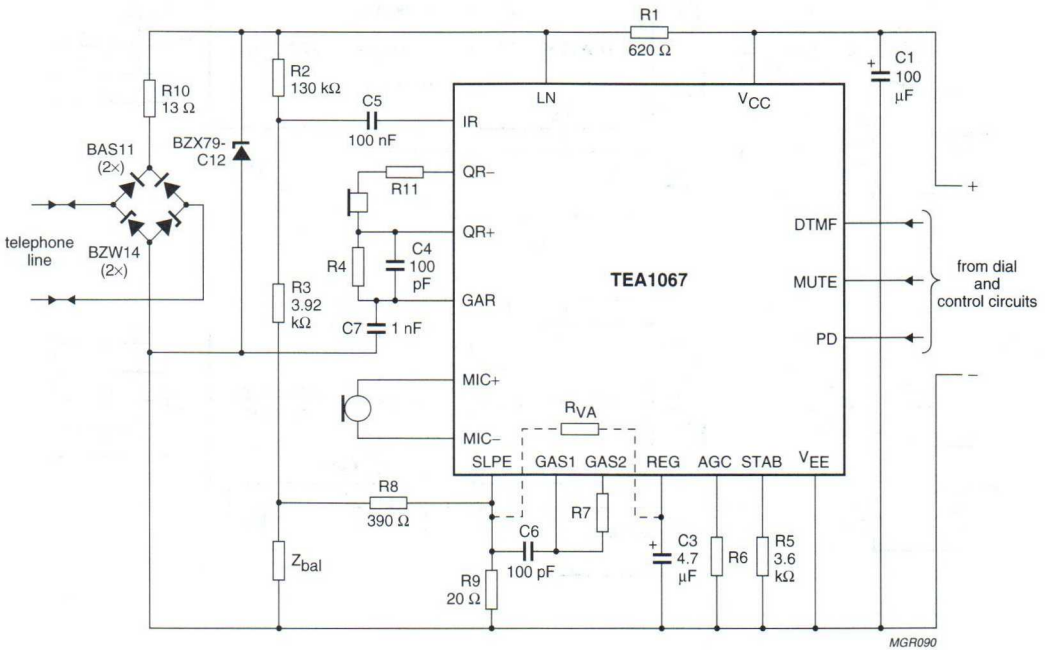
Fig.14 Test circuit for defining voltage gain of MIC+, MIC– and DTMF inputs.



Voltage gain is defined as: $G_v = 20 \log |V_o/V_i|$.

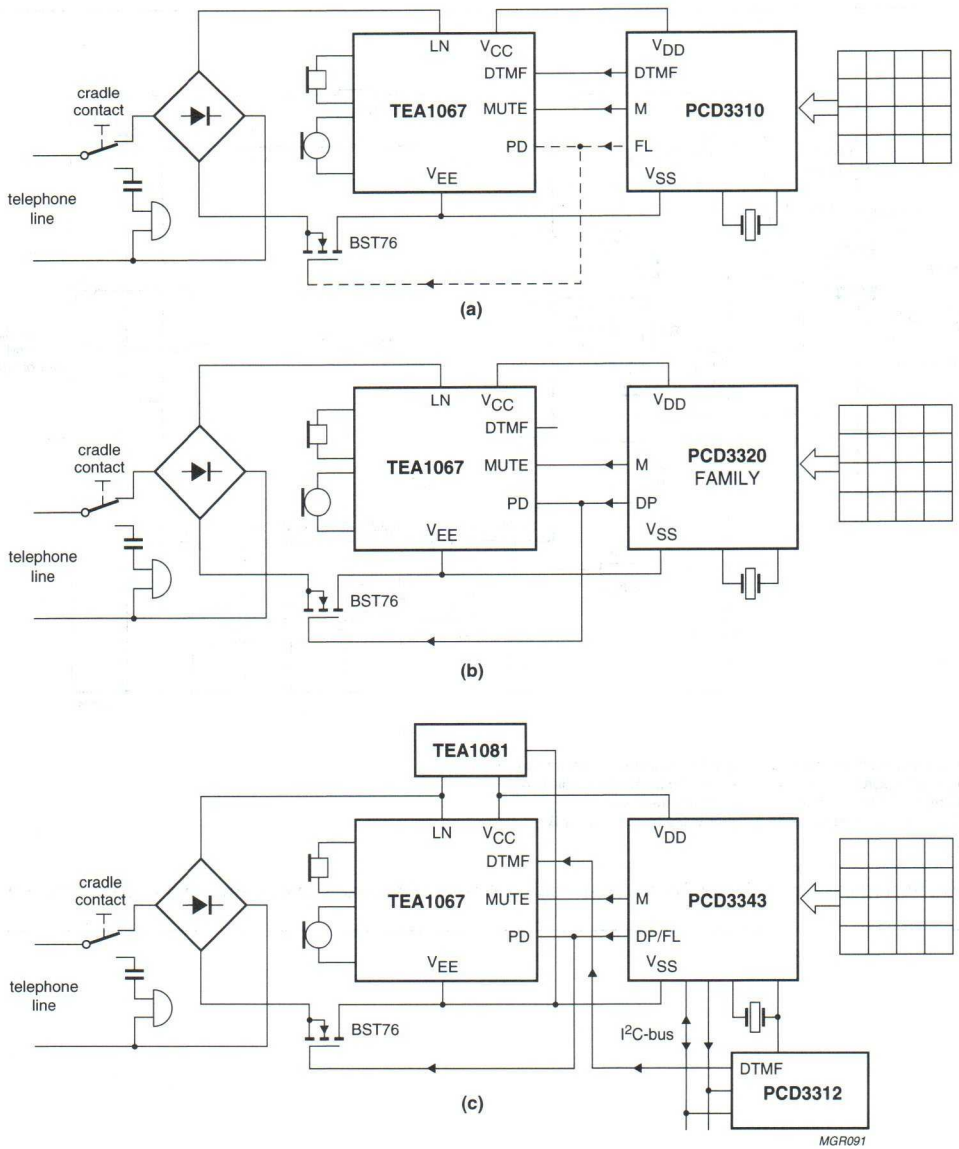
Fig.15 Test circuit for defining voltage gain of the receiving amplifier.

APPLICATION INFORMATION



The bridge to the left, the zener diode and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.
The DC line voltage can be set to a higher value by the resistor R_{VA} (REG to SLPE).

Fig.16 Typical application of the TEA1067, shown here with a piezoelectric earpiece and DTMF dialling.



(a) DTMF-Pulse set with CMOS dialling circuit PCD3310.
The dashed lines show an optional flash (register recall by timed loop break).

(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.

(c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS controller and the PCD3312 CMOS DTMF generator with I^2C-bus. Supply is provided by the TEA1081 supply circuit.

Fig.17 Typical applications of the TEA1067 (simplified).

Low voltage versatile telephone transmission circuit with dialler interface

TEA1110A

FEATURES

- Low DC line voltage; operates down to 1.6 V (excluding voltage drop over external polarity guard)
- Voltage regulator with adjustable DC voltage
- Provides a supply for external circuits
- Symmetrical high impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high impedance input (32 kΩ) for electret microphones
- DTMF input with confidence tone
- $\overline{\text{MUTE}}$ input for pulse or DTMF dialling
- Receiving amplifier for dynamic, magnetic or piezo-electric earpieces
- AGC line loss compensation for microphone and earpiece amplifiers.

APPLICATION

- Line powered telephone sets, cordless telephones, fax machines, answering machines.

GENERAL DESCRIPTION

The TEA1110A is a bipolar integrated circuit that performs all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between speech and dialling. The IC operates at a line voltage down to 1.6 V DC (with reduced performance) to facilitate the use of telephone sets connected in parallel.

All statements and values refer to all versions unless otherwise specified.

QUICK REFERENCE DATA

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; AGC pin connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range	normal operation	11	–	140	mA
		with reduced performance	1	–	11	mA
V_{LN}	DC line voltage		3.35	3.65	3.95	V
I_{CC}	internal current consumption	V_{CC} = 2.9 V	–	1.1	1.4	mA
V_{CC}	supply voltage for peripherals	I_P = 0 mA	–	2.9	–	V
G_{vtrx}	typical voltage gain					
	microphone amplifier (not adjustable)	V_{MIC} = 4 mV (RMS)	–	43.7	–	dB
	receiving amplifier range	V_{IR} = 4 mV (RMS)	19	–	33	dB
ΔG_{vtrx}	gain control range for microphone and receiving amplifiers with respect to I_{line} = 15 mA	I_{line} = 85 mA	–	5.9	–	dB
ΔG_{vtrxm}	gain reduction for microphone and receiving amplifiers	$\overline{\text{MUTE}}$ = LOW	–	80	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1110A	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
TEA1110AT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

BLOCK DIAGRAM

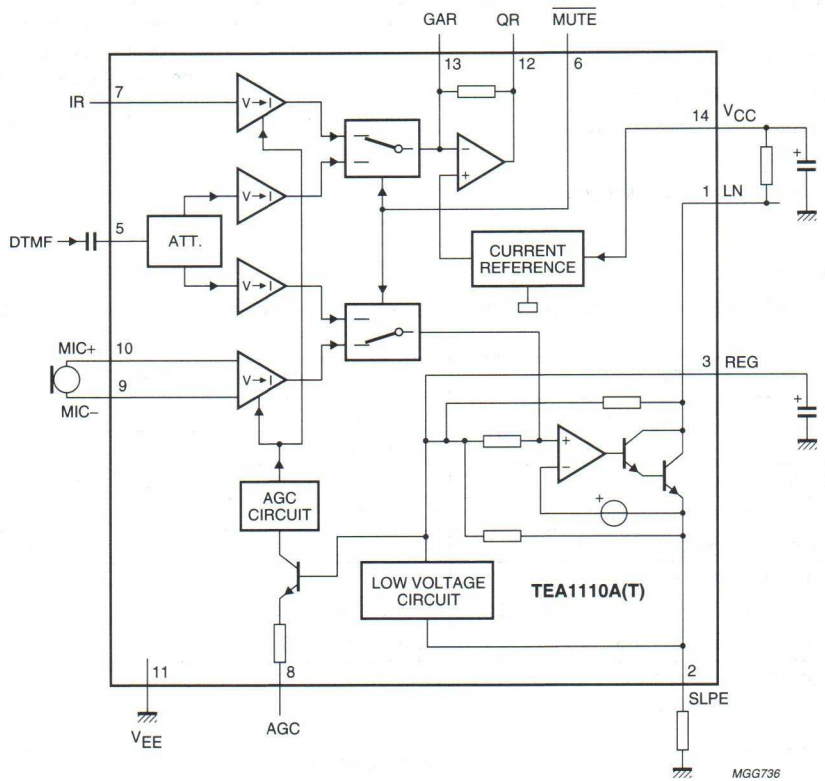


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
SLPE	2	slope (DC resistance) adjustment
REG	3	line voltage regulator decoupling
n.c.	4	not connected
DTMF	5	dual-tone multi-frequency input
$\overline{\text{MUTE}}$	6	mute input to select speech or dialling mode (active LOW)
IR	7	receiving amplifier input
AGC	8	automatic gain control/ line loss compensation
MIC–	9	inverting microphone amplifier input
MIC+	10	non-inverting microphone amplifier input
V_{EE}	11	negative line terminal
QR	12	receiving amplifier output
GAR	13	receive gain adjustment
V_{CC}	14	supply voltage for speech circuit and peripherals

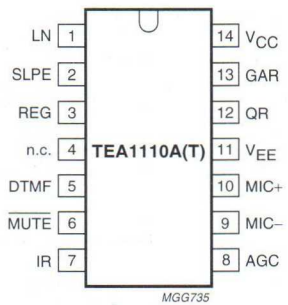


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supply (pins LN, SLPE, V_{CC} and REG)

The supply for the TEA1110A and its peripherals is obtained from the telephone line. See Fig.3.

The IC generates a stabilized reference voltage (V_{ref}) between pins LN and SLPE. V_{ref} is temperature compensated and can be adjusted by means of an external resistor (R_{VA}). V_{ref} equals 3.35 V and can be increased by connecting R_{VA} between pins REG and SLPE (see Fig.4), or decreased by connecting R_{VA} between pins REG and LN. The voltage at pin REG is used by the internal regulator to generate V_{ref} and is decoupled by C_{REG}, which is connected to V_{EE}. This capacitor, converted into an equivalent inductance (see Section "Set impedance"), realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (R_{CC} in the audio-frequency range). The voltage at pin SLPE is proportional to the line current.

The voltage at pin LN is:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I_{CC} - I_P - I^*$$

Where:

I_{line} = line current

I_{CC} = current consumption of the IC

I_P = supply current for peripheral circuits

I^* = current consumed between LN and V_{EE}.

The preferred value for R_{SLPE} is 20 Ω. Changing R_{SLPE} will affect more than the DC characteristics; it also influences the microphone and DTMF gains, the gain control characteristics, the sidetone level and the maximum output swing on the line.

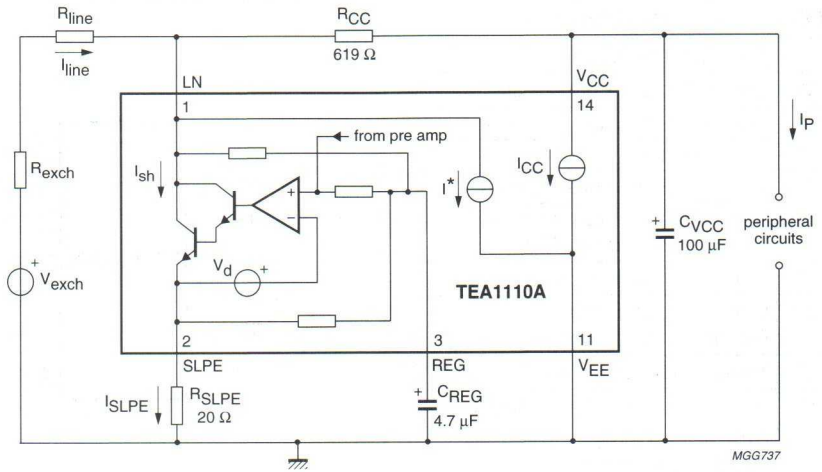


Fig.3 Supply configuration.

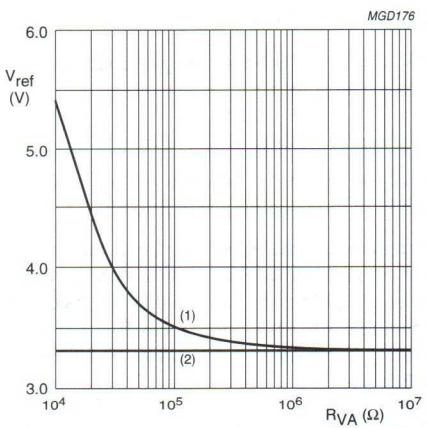
The internal circuitry of the TEA1110A is supplied from pin V_{CC}. This voltage supply is derived from the line voltage by means of a resistor (R_{CC}) and must be decoupled by a capacitor C_{VCC}. It may also be used to supply peripheral circuits such as dialling or control circuits. The V_{CC} voltage depends on the current consumed by the IC and the peripheral circuits as shown by the formula:

$$V_{CC} = V_{CC0} - R_{CCint} \times (I_P - I_{rec})$$

$$V_{CC0} = V_{LN} - R_{CC} \times I_{CC}$$ (see also Figs 5 and 6).

R_{CCint} is the internal equivalent resistance of the voltage supply, and I_{rec} is the current consumed by the output stage of the earpiece amplifier.

The DC line current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistance of the telephone line (R_{line}) and the reference voltage (V_{ref}). With line currents below 7.5 mA, the internal reference voltage (generating V_{ref}) is automatically adjusted to a lower value. This means that more sets can operate in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. At currents below 7.5 mA, the circuit has limited sending and receiving levels. This is called the low voltage area.



(1) Influence of R_{VA} on V_{ref}.
(2) V_{ref} without influence of R_{VA}.

Fig.4 Reference voltage adjustment by R_{VA}.

Set impedance

In the audio frequency range, the dynamic impedance is mainly determined by the R_{CC} resistor. The equivalent impedance of the circuit is illustrated in Fig.7.

Microphone amplifier (pins MIC+ and MIC−)

The TEA1110A has symmetrical microphone inputs. The input impedance between pins MIC+ and MIC− is 64 kΩ (2 × 32 kΩ). The voltage gain from pins MIC+/MIC− to pin LN is set at 43.7 dB (typ).

Automatic gain control is provided on this amplifier for line loss compensation.

Receiving amplifier (pins IR, GAR and QR)

The receiving amplifier has one input (IR) and one output (QR). The input impedance between pin IR and pin V_{EE} is 20 kΩ. The voltage gain from pin IR to pin QR is set at 33 dB (typ). The gain can be decreased by connecting an external resistor R_{GAR} between pins GAR and QR; the adjustment range is 14 dB. Two external capacitors C_{GAR} (connected between GAR and QR) and C_{GARS} (connected between GAR and V_{EE}) ensure stability. The C_{GAR} capacitor provides a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAR} \times (R_{GARint} // R_{GAR})$. R_{GARint} is the internal resistor which sets the gain with a typical value of 125 kΩ. The condition $C_{GARS} = 10 \times C_{GAR}$ must be fulfilled to ensure stability.

The output voltage of the receiving amplifier is specified for continuous wave drive. The maximum output swing depends on the DC line voltage, the R_{CC} resistor, the I_{CC} current consumption of the circuit, the I_P current consumption of the peripheral circuits and the load impedance.

Automatic gain control is provided on this amplifier for line loss compensation.

Automatic gain control (pin AGC)

The TEA1110A performs automatic line loss compensation. The automatic gain control varies the gain of the microphone amplifier and the gain of the receiving amplifier in accordance with the DC line current. The control range is 5.9 dB (which corresponds approximately to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km). The IC can be used with different configurations of feeding bridge (supply voltage and bridge resistance) by connecting an external resistor R_{AGC} between pins AGC and V_{EE}. This resistor enables the I_{start} and I_{stop} line currents to be increased (the ratio between I_{start} and I_{stop} is not affected by the resistor). The AGC function is disabled when pin AGC is left open-circuit.

Mute function (pin $\overline{\text{MUTE}}$)

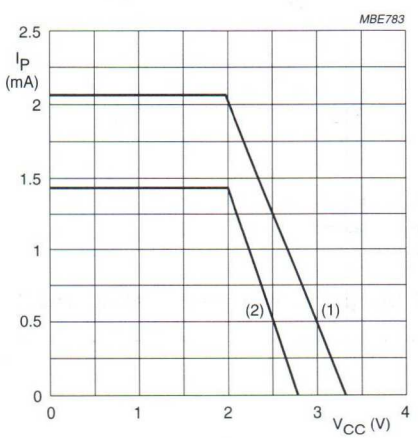
The mute function performs the switching between the speech mode and the dialling mode. When $\overline{\text{MUTE}}$ is LOW, the DTMF input is enabled and the microphone and receiving amplifiers inputs are disabled. When $\overline{\text{MUTE}}$ is HIGH, the microphone and receiving amplifiers inputs are enabled while the DTMF input is disabled. A pull-up resistor is included at the input.

DTMF amplifier (pin DTMF)

When the DTMF amplifier is enabled, dialling tones may be sent on line. These tones can be heard in the earpiece at a low level (confidence tone).

The TEA1110A has an asymmetrical DTMF input. The input impedance between DTMF and V_{EE} is 20 kΩ. The voltage gain from pin DTMF to pin LN is 25.3 dB.

The automatic gain control has no effect on the DTMF amplifier.



(1) With R_{VA} resistor.
(2) Without R_{VA} resistor.

Fig.5 Typical current I_P available from V_{CC} for peripheral circuits at I_{line} = 15 mA.

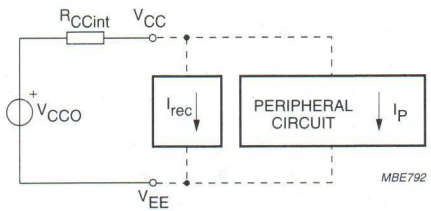
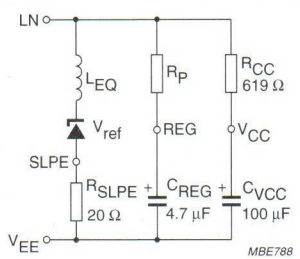


Fig.6 V_{CC} supply voltage for peripherals.



$L_{eq} = C_{REG} \times R_{SLPE} \times R_P$.
R_P = internal resistance.
R_P = 15.5 kΩ.

Fig.7 Equivalent impedance between LN and V_{EE}.

SIDETONE SUPPRESSION

The TEA1110A anti-sidetone network comprising $R_{CC}//Z_{line}$, R_{ast1}, R_{ast2}, R_{ast3}, R_{SLPE} and Z_{bal} (see Fig.8) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = R_{CC} \times (R_{ast2} + R_{ast3})$$

$$k = \frac{(R_{ast2} \times (R_{ast3} + R_{SLPE}))}{(R_{ast1} \times R_{SLPE})}$$

$$Z_{bal} = k \times Z_{line}$$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice, Z_{line} varies considerably with the line type and the line length. Therefore, the value of Z_{bal} should be for an average line length which gives satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

The anti-sidetone network for the TEA1110A (as shown in Fig.12) attenuates the receiving signal from the line by 32 dB before it enters the receiving amplifier.
The attenuation is almost constant over the whole audio frequency range.

A Wheatstone bridge configuration (see Fig.9) may also be used.

More information on the balancing of an anti-sidetone bridge can be obtained in our publication *"Applications Handbook for Wired Telecom Systems, IC03b"*, order number 9397 750 00811.

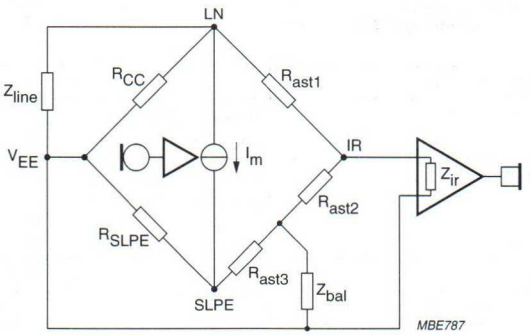


Fig.8 Equivalent circuit of TEA1110A family anti-sidetone bridge.

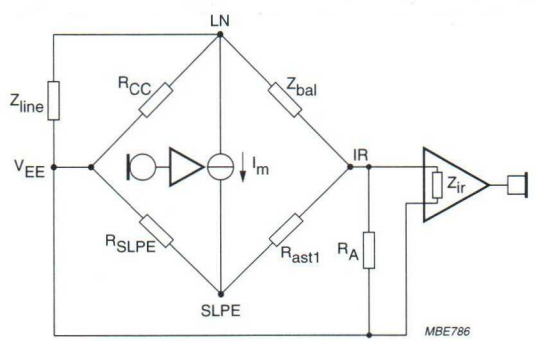


Fig.9 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

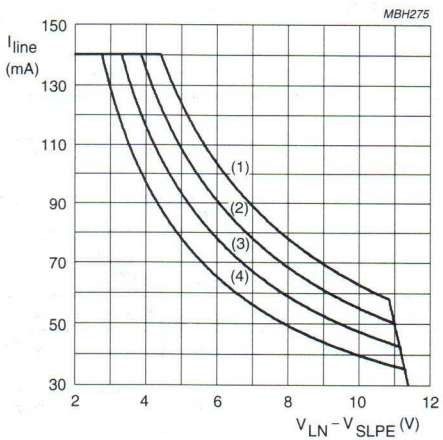
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		V_{EE} – 0.4	12	V
	repetitive line voltage during switch-on or line interruption		V_{EE} – 0.4	13.2	V
$V_{n(max)}$	maximum voltage on all pins		V_{EE} – 0.4	V_{CC} + 0.4	V
I_{line}	line current	R_{SLPE} = 20 Ω; see Figs 10 and 11	–	140	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C; see Figs 10 and 11			
	TEA1110A		–	588	mW
	TEA1110AT		–	384	mW
T_{stg}	storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

HANDLING

This device meets class 2 ESD test requirements [Human Body Model (HBM)], in accordance with *"MIL STD 883C - method 3015"*.

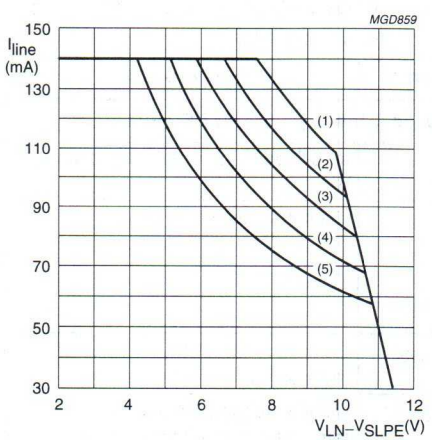
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air; mounted on epoxy board 40.1 × 19.1 × 1.5 mm (TEA1110A)	85	K/W
	thermal resistance from junction to ambient in free air; mounted on epoxy board 40.1 × 19.1 × 1.5 mm (TEA1110AT)	130	K/W



(1) T_{amb} = 45 °C; P_{tot} = 0.615 W.
(2) T_{amb} = 55 °C; P_{tot} = 0.538 W.
(3) T_{amb} = 65 °C; P_{tot} = 0.461 W.
(4) T_{amb} = 75 °C; P_{tot} = 0.384 W.

Fig.10 SO14 Safe operating area (TEA1110AT).



(1) T_{amb} = 35 °C; P_{tot} = 1.058 W.
(2) T_{amb} = 45 °C; P_{tot} = 0.941 W.
(3) T_{amb} = 55 °C; P_{tot} = 0.823 W.
(4) T_{amb} = 65 °C; P_{tot} = 0.705 W.
(5) T_{amb} = 75 °C; P_{tot} = 0.588 W.

Fig.11 DIP14 Safe operating area (TEA1110A).

CHARACTERISTICS

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; AGC pin connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies (pins V_{LN}, V_{CC}, SLPE and REG)						
V_{ref}	stabilized voltage between LN and SLPE		3.1	3.35	3.6	V
V_{LN}	DC line voltage	I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	2.3	–	V
		I_{line} = 15 mA	3.35	3.65	3.95	V
		I_{line} = 140 mA	–	–	6.9	V
$V_{LN(exR)}$	DC line voltage with an external resistor R_{VA}	$R_{VA(SLPE-REG)}$ = 27 kΩ	–	4.4	–	V
$\Delta V_{LN(T)}$	DC line voltage variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C	–	±30	–	mV
I_{CC}	internal current consumption	V_{CC} = 2.9 V	–	1.1	1.4	mA
V_{CC}	supply voltage for peripherals	I_P = 0 mA	–	2.9	–	V
R_{CCint}	equivalent supply voltage resistance	I_P = 0.5 mA	–	550	620	Ω
Microphone amplifier (pins MIC+ and MIC−)						
$\lvert Z_i \rvert$	input impedance					
	differential between pins MIC+ and MIC−		–	64	–	kΩ
	single-ended between pins MIC+/MIC− and V_{EE}		–	32	–	kΩ
G_{vtx}	voltage gain from MIC+/MIC− to LN	V_{MIC} = 4 mV (RMS)	42.7	43.7	44.7	dB
$\Delta G_{vtx(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vtx(T)}$	gain variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C	–	±0.3	–	dB
CMRR	common mode rejection ratio		–	80	–	dB
$V_{LN(max)(rms)}$	maximum sending signal (RMS value)	I_{line} = 15 mA; THD = 2%	1.4	1.7	–	V
		I_{line} = 4 mA, THD = 10%	–	0.8	–	V
V_{notx}	noise output voltage at pin LN; pins MIC+/MIC− shorted through 200 Ω	psophometrically weighted (P53 curve)	–	−78.5	–	dBmp
Receiving amplifier (pins IR, QR and GAR)						
$\lvert Z_i \rvert$	input impedance		–	20	–	kΩ
G_{vrx}	voltage gain from IR to QR	V_{IR} = 4 mV (RMS)	32	33	34	dB
$\Delta G_{vrx(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vrx(T)}$	gain variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C	–	±0.3	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_{vrxr}	gain voltage reduction range	external resistor connected between GAR and QR	–	–	14	dB
$V_{o(rms)}$	maximum receiving signal (RMS value)	I_P = 0 mA sine wave drive; R_L = 150 Ω; THD = 2%	–	0.25	–	V
		I_P = 0 mA sine wave drive; R_L = 450 Ω; THD = 2%	–	0.35	–	V
$V_{norx(rms)}$	noise output voltage at pin QR (RMS value)	G_{vrx} = 33 dB; IR open-circuit; R_L = 150 Ω; psophometrically weighted (P53 curve)	–	–87	–	dBVp
Automatic gain control (pin AGC)						
ΔG_{vtrx}	gain control range for microphone and receiving amplifiers with respect to I_{line} = 15 mA	I_{line} = 85 mA	–	5.9	–	dB
I_{start}	highest line current for maximum gain		–	23	–	mA
I_{stop}	lowest line current for minimum gain		–	56	–	mA
DTMF amplifier (pin DTMF)						
$\lvert Z_i \rvert$	input impedance		–	20	–	kΩ
G_{vdtmf}	voltage gain from DTMF to LN	V_{DTMF} = 20 mV (RMS); $\overline{MUTE}$ = LOW	24.1	25.3	26.5	dB
$\Delta G_{vdtmf(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vdtmf(T)}$	gain variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±0.4	–	dB
G_{vct}	voltage gain from DTMF to QR (confidence tone)	V_{DTMF} = 20 mV (RMS); R_L = 150 Ω	–	–15	–	dB
Mute function (pin $\overline{MUTE}$)						
V_{IL}	LOW level input voltage		V_{EE} – 0.4	–	V_{EE} + 0.3	V
V_{IH}	HIGH level input voltage		V_{EE} + 1.5	–	V_{CC} + 0.4	V
$I_{\overline{MUTE}}$	input current			1.5		µA
ΔG_{vtrxm}	gain reduction for microphone and receiving amplifiers	$\overline{MUTE}$ = LOW		80		dB

APPLICATION INFORMATION

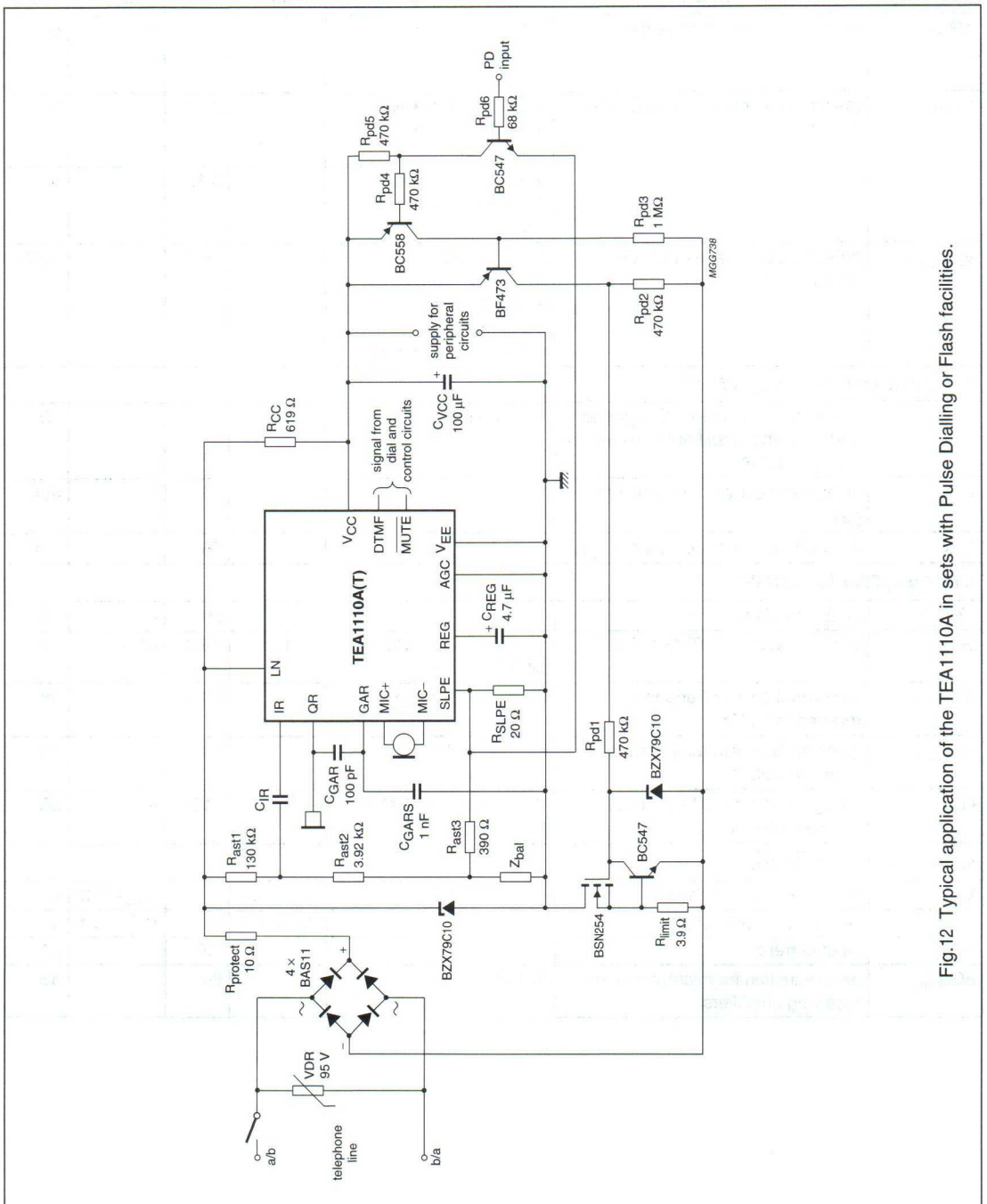


Fig.12 Typical application of the TEA1110A in sets with Pulse Dialling or Flash facilities.

Low voltage versatile telephone transmission circuits with dialler interface

TEA1112; TEA1112A

FEATURES

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable DC voltage
- Provides a supply for external circuits
- Symmetrical high impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high impedance input (32 kΩ) for electret microphones
- DTMF input with confidence tone
- Mute input for pulse or DTMF dialling (MUTE for TEA1112 and $\overline{\text{MUTE}}$ for TEA1112A)
- Receiving amplifier for dynamic, magnetic or piezo-electric earpieces
- AGC line loss compensation for microphone and earpiece amplifiers
- LED on-hook/off-hook status indication
- Microphone mute function (MMUTE for TEA1112 and $\overline{\text{MMUTE}}$ for TEA1112A).

APPLICATION

- Line powered telephone sets, cordless telephones, fax machines and answering machines.

GENERAL DESCRIPTION

The TEA1112; TEA1112A are bipolar integrated circuits that perform all speech and line interface functions required in fully electronic telephone sets. They perform electronic switching between speech and dialling. The ICs operate at a line voltage down to 1.6 V DC (with reduced performance) to facilitate the use of telephone sets connected in parallel.

A current (proportional to the line current and internally limited to a typical value of 19.5 mA) is available to drive an LED which indicates the on-hook/off-hook status.

The microphone amplifier can be disabled during speech condition by means of a microphone mute function.

All statements and values refer to all versions unless otherwise specified.

QUICK REFERENCE DATA

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; AGC pin connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range	normal operation	11	–	140	mA
		with reduced performance	1	–	11	mA
$I_{LED(max)}$	maximum supply current available	I_{line} = 18 mA	–	0.5	–	mA
		I_{line} > 76 mA	–	19.5	–	mA
V_{LN}	DC line voltage		3.35	3.65	3.95	V
I_{CC}	internal current consumption	V_{CC} = 2.9 V	–	1.15	1.4	mA
V_{CC}	supply voltage for peripherals	I_p = 0 mA	–	2.9	–	V
G_{vtrx}	typical voltage gain range					
	microphone amplifier	V_{MIC} = 2 mV (RMS)	38.8	–	51.8	dB
	receiving amplifier	V_{IR} = 6 mV (RMS)	19.2	–	31.2	dB
ΔG_{vtrx}	gain control range for microphone and receiving amplifiers with respect to I_{line} = 15 mA	I_{line} = 85 mA	–	5.8	–	dB
ΔG_{vtxm}	microphone amplifier gain reduction		–	80	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1112	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
TEA1112A	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
TEA1112T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TEA1112AT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

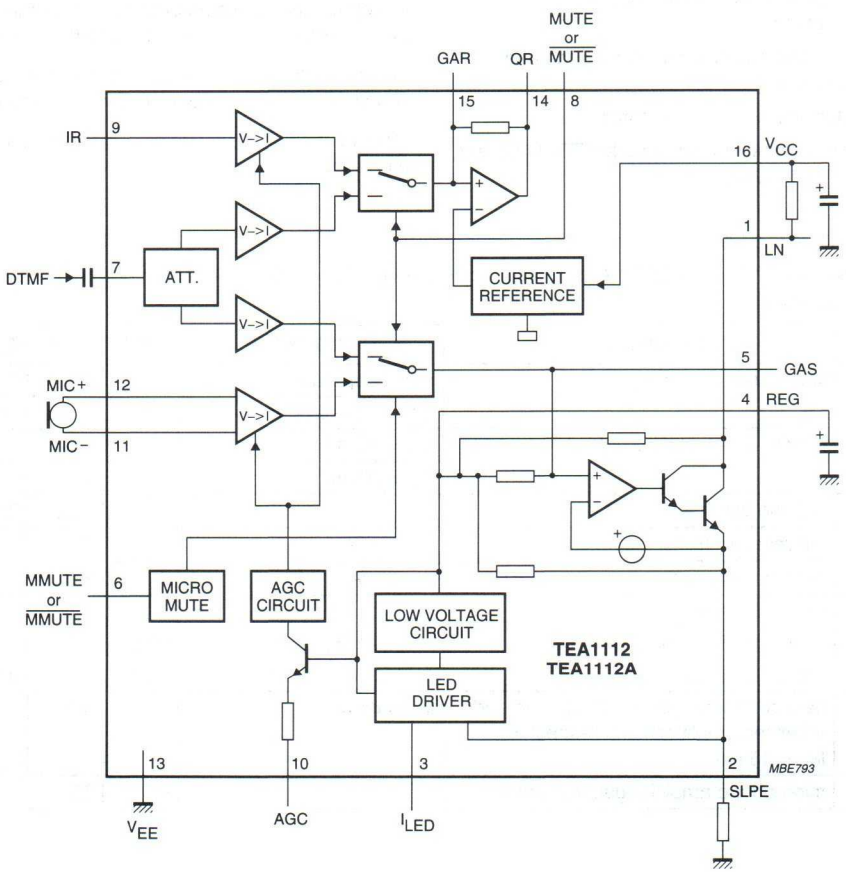


Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	TEA1112	TEA1112A	
LN	1	1	positive line terminal
SLPE	2	2	slope (DC resistance) adjustment
I_{LED}	3	3	available output current to drive a LED
REG	4	4	line voltage regulator decoupling
GAS	5	5	sending gain adjustment
MMUTE	6	–	microphone mute input
$\overline{\text{MMUTE}}$	–	6	microphone mute input (active LOW)
DTMF	7	7	dual-tone multi-frequency input
MUTE	8	–	mute input to select speech or dialling mode
$\overline{\text{MUTE}}$	–	8	mute input to select speech or dialling mode (active LOW)
IR	9	9	receiving amplifier input
AGC	10	10	automatic gain control/line loss compensation
MIC–	11	11	inverting microphone amplifier input
MIC+	12	12	non-inverting microphone amplifier input
V_{EE}	13	13	negative line terminal
QR	14	14	receiving amplifier output
GAR	15	15	receive gain adjustment
V_{CC}	16	16	supply voltage for speech circuit and peripherals

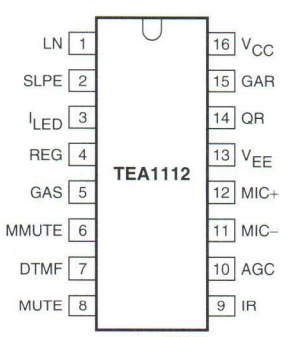


Fig.2 Pin configuration (TEA1112).

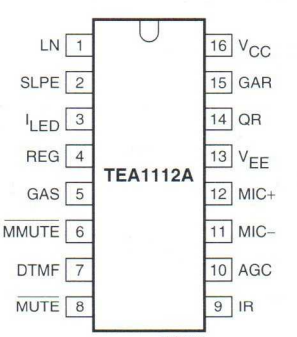


Fig.3 Pin configuration (TEA1112A).

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supply (pins LN, SLPE, V_{CC} and REG)

The supply for the TEA1112; TEA1112A and their peripherals is obtained from the telephone line.

The ICs generate a stabilized reference voltage (V_{ref}) between pins LN and SLPE. This reference voltage is equal to 3.35 V, is temperature compensated and can be adjusted by means of an external resistor (R_{VA}). It can be increased by connecting the R_{VA} resistor between pins REG and SLPE (see Fig.5), or decreased by connecting the R_{VA} resistor between pins REG and LN. The voltage at pin REG is used by the internal regulator to generate the stabilized reference voltage and is decoupled by a capacitor (C_{REG}) which is connected to V_{EE}. This capacitor, converted into an equivalent inductance (see Section "Set impedance"), realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (R_{CC} in the audio-frequency range). The voltage at pin SLPE is proportional to the line current. Figure 4 illustrates the supply configuration.

The ICs regulate the line voltage at pin LN, and can be calculated as follows:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I_{CC} - I_p - I^* = I_{LED} + I_{sh}$$

Where:

I_{line} = line current

I_{CC} = current consumption of the IC

I_p = supply current for peripheral circuits

I^* = current consumed between LN and V_{EE}

I_{LED} = supply current for the LED component

I_{sh} = the excess line current shunted to SLPE (and V_{EE}) via LN.

The preferred value for R_{SLPE} is 20 Ω. Changing R_{SLPE} will affect more than the DC characteristics; it also influences the microphone and DTMF gains, the LED supply current characteristic, the gain control characteristics, the sidetone level and the maximum output swing on the line.

The internal circuitry of the TEA1112; TEA1112A is supplied from pin V_{CC}. This voltage supply is derived from the line voltage by means of a resistor (R_{CC}) and must be decoupled by a capacitor C_{VCC}. It may also be used to supply peripheral circuits such as dialling or control circuits. The V_{CC} voltage depends on the current consumed by the IC and the peripheral circuits as shown by the formula (see also Figs.6 and 7). R_{CCint} is the internal impedance of the voltage supply point, and I_{rec} is the current consumed by the output stage of the earpiece amplifier.

$$V_{CC} = V_{CC0} - R_{CCint} \times (I_p - I_{rec})$$

$$V_{CC0} = V_{LN} - R_{CC} \times I_{CC}$$

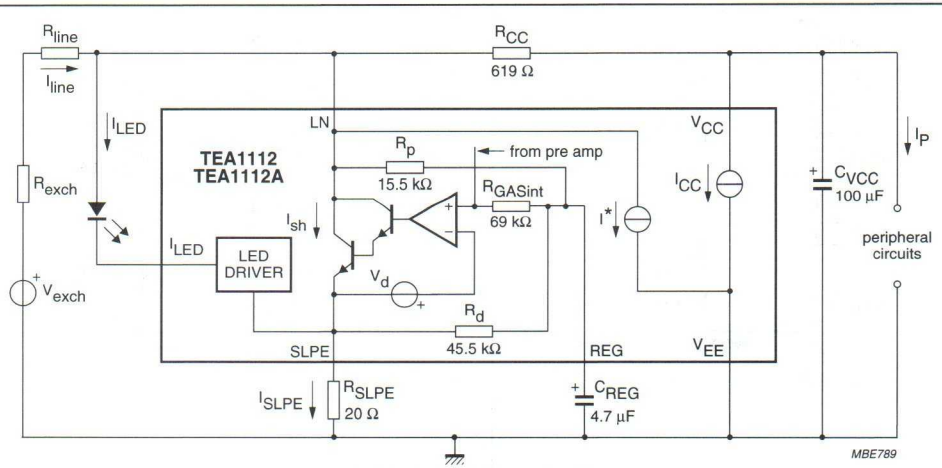
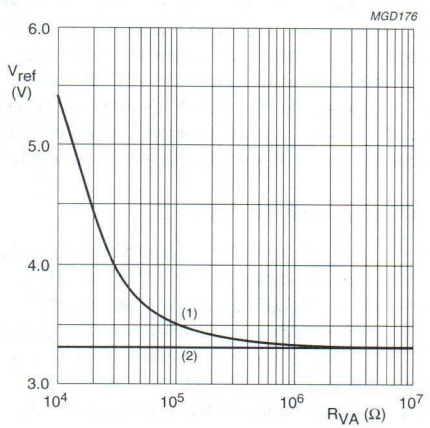


Fig.4 Supply configuration.



(1) Influence of R_{VA} on V_{ref}.
(2) V_{ref} without influence of R_{VA}.

Fig.5 Reference voltage adjustment by R_{VA}.

The DC line current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistance of the telephone line (R_{line}) and the reference voltage (V_{ref}). With line currents below 7.5 mA, the internal reference voltage (generating V_{ref}) is automatically adjusted to a lower value. This means that more sets can operate in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. At currents below 7.5 mA, the circuit has limited sending and receiving levels. This is called the low voltage area.

Set impedance

In the audio frequency range, the dynamic impedance is mainly determined by the R_{CC} resistor. The equivalent impedance of the circuits is illustrated in Fig.8.

LED supply (pin I_{LED})

The TEA1112; TEA1112A give an on-hook/off-hook status indication. This is achieved by a current made available to drive an LED connected between pins I_{LED} and LN. In the low voltage area, which corresponds to low line current conditions, no current is available for this LED.

For line currents higher than a threshold, $I_{LEDstart}$, the I_{LED} current increases proportionally to the line current (with a ratio of one third). The I_{LED} current is internally limited to 19.5 mA (see Fig.9). If no LED device is used in the application, the I_{LED} pin should be shorted to pin SLPE.

For 17 mA < I_{line} < 77 mA: $I_{LED} = \frac{I_{line} - 17}{3}$

This LED driver is referenced to SLPE. Consequently, all the I_{LED} supply current will flow through the R_{SLPE} resistor. The AGC characteristics are not disturbed (see Fig.4).

Microphone amplifier (pins MIC+, MIC– and GAS)

The TEA1112; TEA1112A have symmetrical microphone inputs. The input impedance between pins MIC+ and MIC– is 64 kΩ (2 × 32 kΩ). The voltage gain from pins MIC+/MIC– to pin LN is set at 51.8 dB (typ). The gain can be decreased by connecting an external resistor R_{GAS} between pins GAS and REG. The adjustment range is 13 dB. A capacitor C_{GAS} connected between pins GAS and REG can be used to provide a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAS} \times (R_{GASint} // R_{GAS})$. R_{GASint} is the internal resistor which sets the gain with a typical value of 69 kΩ.

Automatic gain control is provided on this amplifier for line loss compensation.

Microphone mute (pin MMUTE; TEA1112)

The microphone amplifier can be disabled by activating the microphone mute function. When MMUTE is LOW, the normal speech mode is entered, depending on the level on MUTE (see Table 1). When MMUTE is HIGH, the microphone amplifier inputs are disabled while the DTMF input is enabled (no confidence tone is provided). The voltage gain between LN and MIC+/MIC– is attenuated; the gain reduction is 80 dB (typ).

Microphone mute (pin $\overline{\text{MMUTE}}$; TEA1112A)

The microphone amplifier can be disabled by activating the microphone mute function. When $\overline{\text{MMUTE}}$ is LOW, the microphone amplifier inputs are disabled while the DTMF input is enabled (no confidence tone is provided). The voltage gain between LN and MIC+/MIC– is attenuated; the gain reduction is 80 dB (typ). When $\overline{\text{MMUTE}}$ is HIGH, the normal speech mode is entered, depending on the level on MUTE (see Table 1).

Receiving amplifier (pins IR, GAR and QR)

The receiving amplifier has one input (IR) and one output (QR). The input impedance between pin IR and pin V_{EE} is 20 kΩ. The voltage gain from pin IR to pin QR is set at 31.2 dB (typ). The gain can be decreased by connecting an external resistor R_{GAR} between pins GAR and QR; the adjustment range is 12 dB. Two external capacitors C_{GAR} (connected between GAR and QR) and C_{GARS} (connected between GAR and V_{EE}) ensure stability. The C_{GAR} capacitor provides a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAR} \times (R_{GARint} // R_{GAR})$. R_{GARint} is the internal resistor which sets the gain with a typical value of 100 kΩ. The relationship $C_{GARS} = 10 \times C_{GAR}$ must be fulfilled to ensure stability.

The output voltage of the receiving amplifier is specified for continuous wave drive. The maximum output swing depends on the DC line voltage, the R_{CC} resistor, the I_{CC} current consumption of the circuit, the I_p current consumption of the peripheral circuits and the load impedance.

Automatic gain control is provided on this amplifier for line loss compensation.

Automatic gain control (pin AGC)

The TEA1112; TEA1112A perform automatic line loss compensation. The automatic gain control varies the gain of the microphone amplifier and the gain of the receiving amplifier in accordance with the DC line current. The control range is 5.8 dB (which corresponds approximately to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km). The ICs can be used with different configurations of feeding bridge (supply voltage and bridge resistance) by connecting an external resistor R_{AGC} between pins AGC and V_{EE}. This resistor enables the I_{start} and I_{stop} line currents to be increased (the ratio between I_{start} and I_{stop} is not affected by the resistor). The AGC function is disabled when pin AGC is left open-circuit.

Mute function (pin MUTE; TEA1112)

The mute function performs the switching action between the speech mode and the dialling mode. When MUTE is LOW or open-circuit, the microphone and receiving amplifiers inputs are enabled while the DTMF input is disabled, depending on the MMUTE level (see Table 1). When MUTE is HIGH, the DTMF input is enabled and the microphone and receiving amplifiers inputs are disabled.

Mute function (pin $\overline{\text{MUTE}}$; TEA1112A)

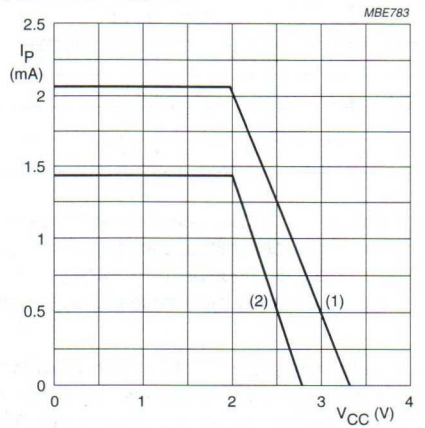
The mute function performs the switching between the speech mode and the dialling mode. When $\overline{\text{MUTE}}$ is LOW or open-circuit, the DTMF input is enabled and the microphone and receiving amplifiers inputs are disabled. When $\overline{\text{MUTE}}$ is HIGH, the microphone and receiving amplifiers inputs are enabled while the DTMF input is disabled, depending on the MMUTE level (see Table 1).

DTMF amplifier (pin DTMF)

When the DTMF amplifier is enabled, dialling tones may be sent on line. These tones can be heard in the earpiece at a low level (confidence tone).

The TEA1112; TEA1112A have an asymmetrical DTMF input. The input impedance between DTMF and V_{EE} is 20 kΩ. The voltage gain from pin DTMF to pin LN is 25.5 dB. When an external resistor is connected between pins REG and GAS to decrease the microphone gain, the DTMF gain varies in the same way (the DTMF gain is 26.3 dB lower than the microphone gain with no AGC control).

The automatic gain control has no effect on the DTMF amplifier.



(1) With R_{VA} resistor.
(2) Without R_{VA} resistor.

Fig.6 Typical current I_p available from V_{CC} for peripheral circuits at I_{line} = 15 mA.

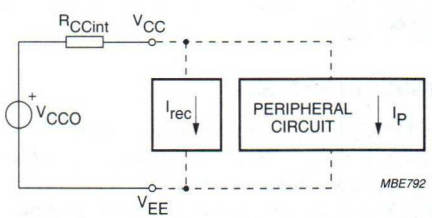
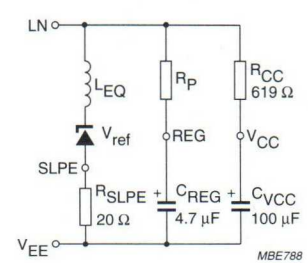


Fig.7 V_{CC} supply voltage for peripherals.



$L_{EQ} = C_{REG} \times R_{SLPE} \times R_P$.
R_P = internal resistance.
R_P = 15.5 kΩ.

Fig.8 Equivalent impedance between LN and V_{EE}.

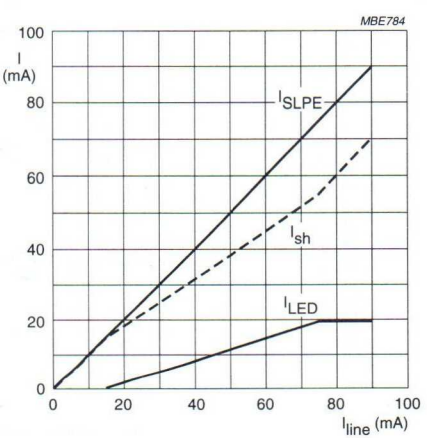


Fig.9 Available current to drive an LED.

MUTE and MMUTE levels for different modes

Table 1 Required MUTE and MMUTE levels to enable the different possible modes

IC	TEA1112		TEA1112A	
Mode	MUTE	MMUTE	$\overline{\text{MUTE}}$	$\overline{\text{MMUTE}}$
Speech	L	L	H	H
DTMF dialling	H	X	L	X
Microphone mute	L	H	H	L

SIDETONE SUPPRESSION

The TEA1112; TEA1112A anti-sidetone network comprising R_{CC} // Z_{line}, R_{ast1}, R_{ast2}, R_{ast3}, R_{SLPE} and Z_{bal} (see Fig.10) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = R_{CC} \times (R_{ast2} + R_{ast3})$$

$$k = \frac{(R_{ast2} \times (R_{ast3} + R_{SLPE}))}{(R_{ast1} \times R_{SLPE})}$$

$$Z_{bal} = k \times Z_{line}$$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice, Z_{line} varies considerably with the line type and the line length. Therefore, the value chosen for Z_{bal} should be for an average line length which gives satisfactory sidetone suppression with short and long lines.
The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

The anti-sidetone network for the TEA1112; TEA1112A (as shown in Fig.14) attenuates the receiving signal from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. A Wheatstone bridge configuration (see Fig.11) may also be used.

More information on the balancing of an anti-sidetone bridge can be obtained in our publication *"Applications Handbook for Wired Telecom Systems, IC03b"*, order number 9397 750 00811.

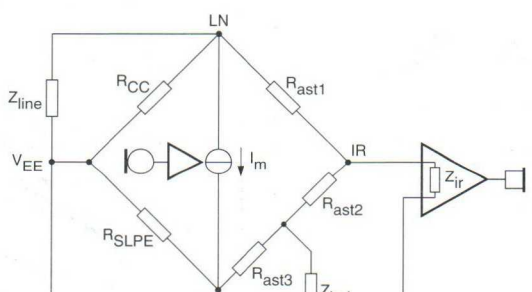


Fig.10 Equivalent circuit of TEA1112; TEA1112A family anti-sidetone bridge.

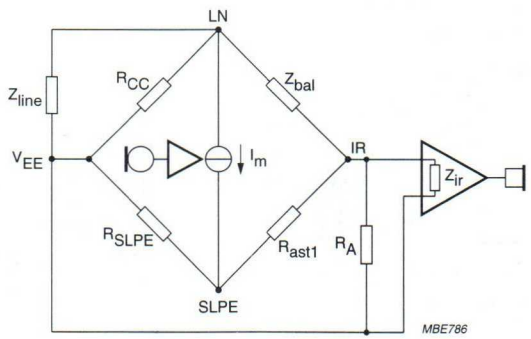


Fig.11 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

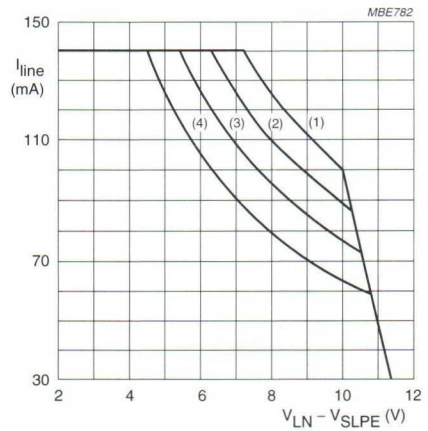
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		$V_{EE} - 0.4$	12	V
	repetitive line voltage during switch-on or line interruption		$V_{EE} - 0.4$	13.2	V
$V_{n(max)}$	maximum voltage on pins I_{LED}, SLPE		$V_{EE} - 0.4$	$V_{LN} + 0.4$	V
	maximum voltage on all other pins		$V_{EE} - 0.4$	$V_{CC} + 0.4$	V
I_{line}	line current	R_{SLPE} = 20 Ω; see Figs 12 and 13	–	140	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C; see Figs 12 and 13			
	TEA1112; TEA1112A		–	625	mW
	TEA1112T; TEA1112AT		–	416	mW
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

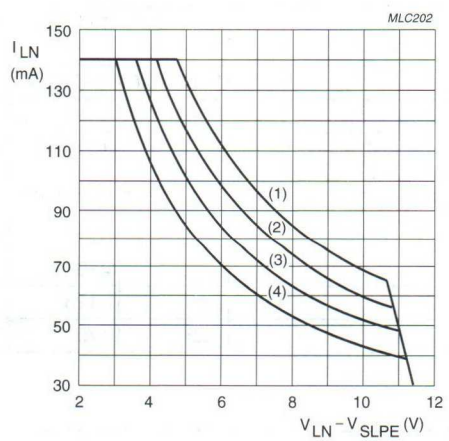
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air (TEA1112; TEA1112A)	80	K/W
	thermal resistance from junction to ambient in free air mounted on epoxy board 40.1 × 19.1 × 1.5 mm (TEA1112T; TEA1112AT)	130	K/W



LINE	T_{amb} (°C)	P_{tot} (W)
(1)	45	1.000
(2)	55	0.875
(3)	65	0.750
(4)	75	0.625

Fig.12 Safe operating area (TEA1112; TEA1112A).



LINE	T_{amb} (°C)	P_{tot} (W)
(1)	45	0.666
(2)	55	0.583
(3)	65	0.500
(4)	75	0.416

Fig.13 Safe operating area (TEA1112T; TEA1112AT).

CHARACTERISTICS

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; AGC pin connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins V_{LN}, V_{CC}, SLPE and REG)						
V_{ref}	stabilized voltage between LN and SLPE		3.1	3.35	3.6	V
V_{LN}	DC line voltage	I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	2.45	–	V
		I_{line} = 15 mA	3.35	3.65	3.95	V
		I_{line} = 140 mA	–	–	6.9	V
$V_{LN(exR)}$	DC line voltage with an external resistor R_{VA}	$R_{VA(SLPE-REG)}$ = 27 kΩ	–	4.4	–	V
$\Delta V_{LN(T)}$	DC line voltage variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C	–	±30	–	mV
I_{CC}	internal current consumption	V_{CC} = 2.9 V	–	1.15	1.4	mA
V_{CC}	supply voltage for peripherals	I_p = 0 mA	–	2.9	–	V
R_{CCint}	equivalent supply voltage impedance	I_p = 0.5 mA	–	550	620	Ω
LED supply (pin I_{LED})						
$I_{line(h)}$	highest line current for I_{LED} < 0.5 mA		–	18	–	mA
$I_{line(l)}$	lowest line current for maximum I_{LED}		–	76	–	mA
$I_{LED(max)}$	maximum supply current available		–	19.5	–	mA
Microphone amplifier (pins MIC+, MIC− and GAS)						
$\lvert Z_i \rvert$	input impedance					
	differential between pins MIC+ and MIC−		–	64	–	kΩ
	single-ended between pins MIC+/MIC− and V_{EE}		–	32	–	kΩ
G_{vtx}	voltage gain from MIC+/MIC− to LN	V_{MIC} = 2 mV (RMS)	50.6	51.8	53	dB
$\Delta G_{vtx(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vtx(T)}$	gain variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C	–	±0.3	–	dB
CMRR	common mode rejection ratio		–	80	–	dB
ΔG_{vtxr}	gain voltage reduction range	external resistor connected between GAS and REG	–	–	13	dB
$V_{LN(max)}$	maximum sending signal (RMS value)	I_{line} = 15 mA; THD = 2%	1.4	1.7	–	V
		I_{line} = 4 mA; THD = 10%	–	0.8	–	V
V_{notx}	noise output voltage at pin LN; pins MIC+/ MIC− shorted through 200 Ω	psophometrically weighted (P53 curve)	–	−70.5	–	dBmp

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Microphone mute (pins MMUTE; TEA1112 and $\overline{\text{MMUTE}}$; TEA1112A)						
ΔG_{vtxm}	gain reduction in microphone MUTE mode		–	80	–	dB
V_{IL}	LOW level input voltage		V_{EE} – 0.4	–	V_{EE} + 0.3	V
V_{IH}	HIGH level input voltage		V_{EE} + 1.5	–	V_{CC} + 0.4	V
I_{MMUTE}	input current	input level = HIGH	–	1.25	3	µA
Receiving amplifier (pins IR, QR and GAR)						
$\lvert Z_i \rvert$	input impedance		–	20	–	kΩ
G_{vrx}	voltage gain from IR to QR	V_{IR} = 6 mV (RMS)	29.7	31.2	32.7	dB
$\Delta G_{vrx(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vrx(T)}$	gain variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
ΔG_{vrxr}	gain voltage reduction range	external resistor connected between GAR and QR	–	–	12	dB
$V_{o(rms)}$	maximum receiving signal (RMS value)	I_p = 0 mA sine wave drive; R_L = 150 Ω; THD = 2%	–	0.25	–	V
		I_p = 0 mA sine wave drive; R_L = 450 Ω; THD = 2%	–	0.35	–	V
$V_{norx(rms)}$	noise output voltage at pin QR (RMS value)	IR open-circuit; R_L = 150 Ω; psophometrically weighted (P53 curve)	–	–86	–	dBVp
Automatic gain control (pin AGC)						
ΔG_{vtrx}	gain control range for microphone and receiving amplifiers with respect to I_{line} = 15 mA	I_{line} = 85 mA	–	5.8	–	dB
I_{start}	highest line current for maximum gain		–	26	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{stop}	lowest line current for minimum gain		–	61	–	mA
DTMF amplifier (pin DTMF)						
$\|Z_i\|$	input impedance		–	20	–	kΩ
G_{vdtmf}	voltage gain from DTMF to LN in DTMF dialling or microphone MUTE mode	V_{DTMF} = 20 mV (RMS)	24.3	25.5	26.7	dB
$\Delta G_{vdtmf(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vdtmf(T)}$	gain variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C	–	±0.4	–	dB
G_{vct}	voltage gain from DTMF to QR (confidence tone)	V_{DTMF} = 20 mV (RMS); R_L = 150 Ω	–	−18	–	dB
Mute function (pins MUTE; TEA1112 and $\overline{\text{MUTE}}$; TEA1112A)						
V_{IL}	LOW level input voltage		V_{EE} − 0.4	–	V_{EE} + 0.3	V
V_{IH}	HIGH level input voltage		V_{EE} + 1.5	–	V_{CC} + 0.4	V
I_{MUTE}	input current	input level = HIGH	–	1.25	3	µA
ΔG_{trxm}	gain reduction for microphone and receiving amplifiers in DTMF dialling mode		–	80	–	dB

APPLICATION INFORMATION

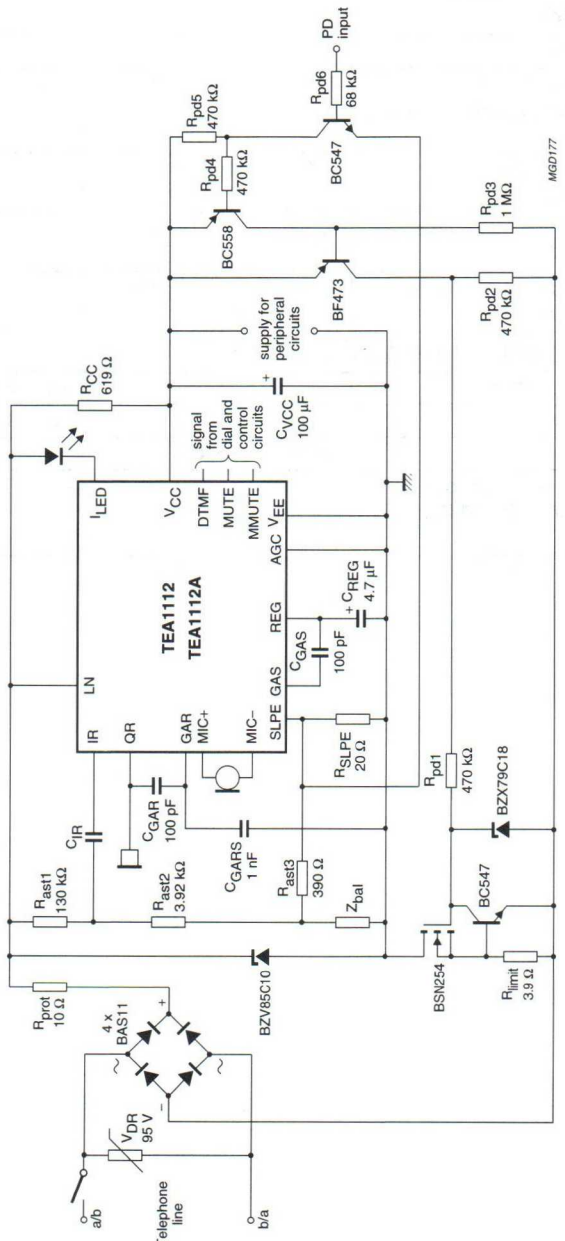


Fig.14 Typical application of the TEA1112; TEA1112A in sets with Pulse Dialling or Flash facilities.

Low voltage versatile telephone transmission circuit with dialler interface

TEA1113

FEATURES

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable DC voltage
- Provides a supply for external circuits
- Symmetrical high impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high impedance input (32 kΩ) for electret microphones
- DTMF input with confidence tone
- $\overline{\text{MUTE}}$ input for pulse or DTMF dialling
- Receiving amplifier for dynamic, magnetic or piezo-electric earpieces
- Dynamic limitation in the transmit direction to prevent distortion of the transmit line and sidetone signals
- AGC line loss compensation for microphone and earpiece amplifiers
- LED on-hook/off-hook status indication
- Microphone mute function available with switch.

APPLICATION

- Line powered telephone sets, cordless telephones, fax machines and answering machines.

GENERAL DESCRIPTION

The TEA1113 is a bipolar integrated circuit that performs all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between speech and dialling. The IC operates at a line voltage down to 1.6 V DC (with reduced performance) to facilitate the use of telephone sets connected in parallel.

A current (proportional to the line current and internally limited to 19.5 mA) is available to drive an LED which indicates the on-hook/off-hook status.

The transmit signal on the line is dynamically limited to prevent distortion at high transmit levels for both the sending line and sidetone signals. The microphone amplifier can be disabled during speech condition by means of a microphone mute function.

All statements and values refer to all versions unless otherwise specified.

QUICK REFERENCE DATA

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; C_{DLS} = 470 nF; AGC pin connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range	normal operation	11	–	140	mA
		with reduced performance	1	–	11	mA
$I_{LED(max)}$	maximum supply current available	I_{line} = 18 mA	–	0.6	–	mA
		I_{line} > 76 mA	–	19.5	–	mA
V_{LN}	DC line voltage		3.7	4.0	4.3	V
$V_{LN(max)(p-p)}$	maximum output voltage swing (peak-to-peak value)		3.8	4.65	–	V
I_{CC}	internal current consumption	V_{CC} = 3.2 V	–	1.3	1.6	mA
V_{CC}	supply voltage for peripherals	I_p = 0 mA	2.8	3.2	–	V
G_{vtrx}	typical voltage gain range					
	microphone amplifier	V_{MIC} = 2 mV (RMS)	38.8	–	51.8	dB
	receiving amplifier	V_{IR} = 4 mV (RMS)	19.3	–	31.3	dB
ΔG_{vtrx}	gain control range for microphone and receiving amplifiers with respect to I_{line} = 15 mA	I_{line} = 85 mA	–	5.8	–	dB
ΔG_{vtxm}	microphone amplifier gain reduction		–	80	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1113	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
TEA1113T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

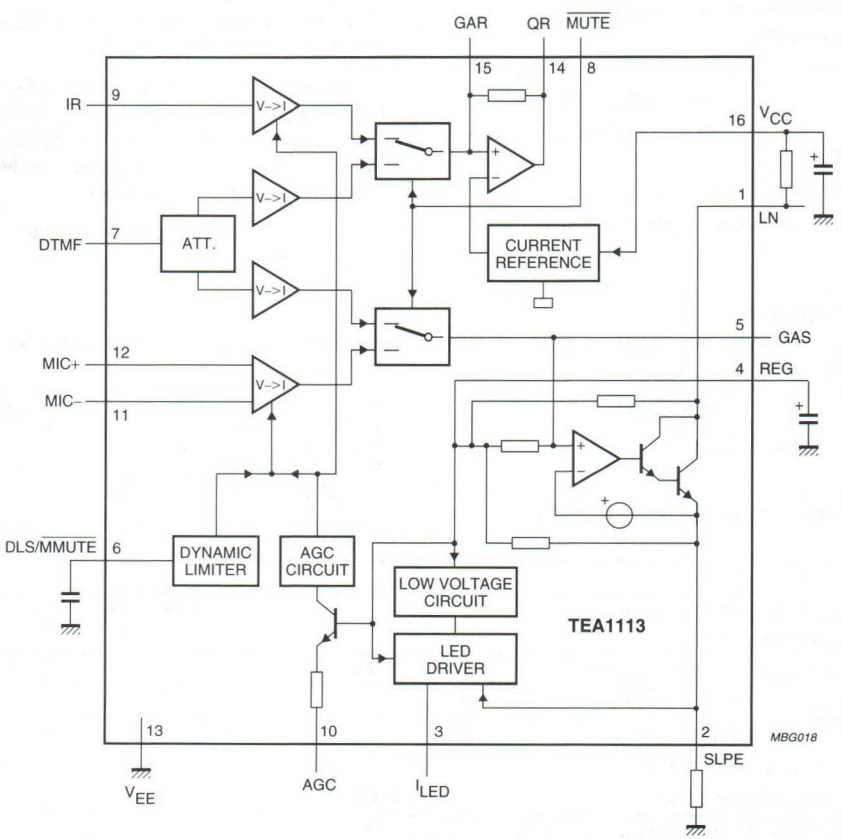


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
SLPE	2	slope (DC resistance) adjustment
I_{LED}	3	available output current to drive an LED
REG	4	line voltage regulator decoupling
GAS	5	sending gain adjustment
DLS/$\overline{\text{MMUTE}}$	6	dynamic limiter timing adjustment and microphone mute input
DTMF	7	dual-tone multi-frequency input
$\overline{\text{MUTE}}$	8	mute input to select speech or dialling mode (active LOW)
IR	9	receiving amplifier input
AGC	10	automatic gain control - line loss compensation
MIC–	11	inverting microphone amplifier input
MIC+	12	non-inverting microphone amplifier input
V_{EE}	13	negative line terminal
QR	14	receiving amplifier output
GAR	15	receive gain adjustment
V_{CC}	16	supply voltage for speech circuit and peripherals

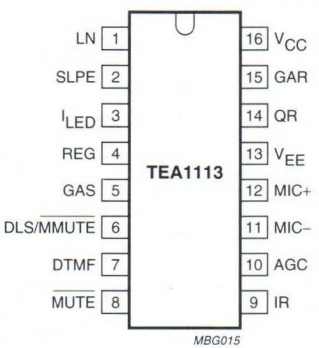


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supply (pins LN, SLPE, V_{CC} and REG)

The supply for the TEA1113 and its peripherals is obtained from the telephone line.

The ICs generate a stabilized reference voltage (V_{ref}) between pins LN and SLPE. This reference voltage is equal to 3.7 V, is temperature compensated and can be adjusted by means of an external resistor (R_{VA}). It can be increased by connecting the R_{VA} resistor between pins REG and SLPE, or decreased by connecting the R_{VA} resistor between pins REG and LN. The voltage at pin REG is used by the internal regulator to generate the stabilized reference voltage and is decoupled by a capacitor (C_{REG}) which is connected to V_{EE}. This capacitor, converted into an equivalent inductance (see Section "Set impedance"), realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (R_{CC} in the audio-frequency range). The voltage at pin SLPE is proportional to the line current. Figure 3 illustrates the supply configuration.

The IC regulates the line voltage at the pin LN, and it can be calculated as follows:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I_{CC} - I_p - I^* = I_{LED} + I_{sh}$$

I_{line}: line current

I_{CC}: current consumption of the IC

I_p: supply current for peripheral circuits

I^*: current consumed between LN and V_{EE}

I_{LED}: supply current for the LED component

I_{sh}: the excess line current shunted to SLPE (and V_{EE}) via LN.

The preferred value for R_{SLPE} is 20 Ω. Changing R_{SLPE} will affect more than the DC characteristics; it also influences the microphone and DTMF gains, the LED supply current characteristic, the gain control characteristics, the sidetone level and the maximum output swing on the line.

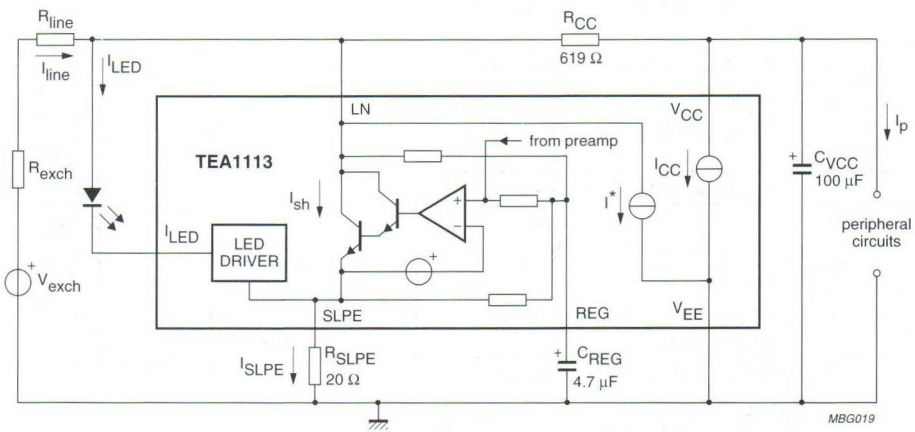
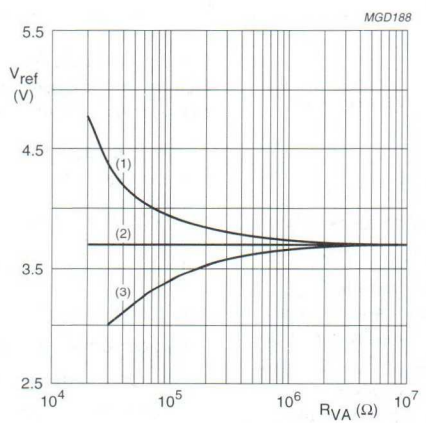


Fig.3 Supply configuration.



(1) R_{VA} between REG and SLPE.
(2) No R_{VA}.
(3) R_{VA} between REG and LN.

Fig.4 Reference voltage adjustment by a R_{VA} resistor.

The internal circuitry of the TEA1113 is supplied from pin V_{CC}. This voltage supply is derived from the line voltage by means of a resistor (R_{CC}) and must be decoupled by a capacitor C_{VCC}. It may also be used to supply peripheral circuits such as dialling or control circuits. The V_{CC} voltage depends on the current consumed by the IC and the peripheral circuits as shown by the formula (see also Figs 5 and 6). R_{CCint} is the internal impedance of the voltage supply point, and I_{rec} is the current consumed by the output stage of the earpiece amplifier.

$$V_{CC} = V_{CCO} - R_{CCint} \times (I_p - I_{rec})$$

$$V_{CCO} = V_{LN} - R_{CC} \times I_{CC}$$

The DC line current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistance of the telephone line (R_{line}) and the reference voltage (V_{ref}). With line currents below 8 mA, the internal reference voltage (generating V_{ref}) is automatically adjusted to a lower value. This means that more sets can operate in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. At currents below 8 mA, the circuit has limited sending and receiving levels. This is called the low voltage area.

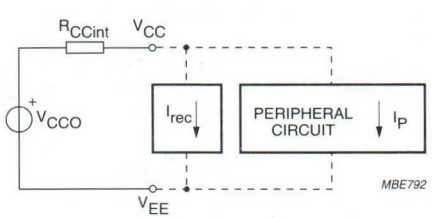


Fig.5 V_{CC} voltage supply for peripherals.

Set impedance

In the audio frequency range, the dynamic impedance is mainly determined by the R_{CC} resistor. The equivalent impedance of the circuits is illustrated in Fig.7.

LED supply (pin I_{LED})

The TEA1113 gives an on-hook/off-hook status indication. This is achieved by a current made available to drive an LED connected between pins I_{LED} and LN. In the low voltage area, which corresponds to low line current conditions, no current is available for this LED. For line currents higher than a threshold current, the I_{LED} current increases proportionally to the line current (with a ratio of one third).The I_{LED} current is internally limited to 19.5 mA (see Fig.8).

For 17 mA < I_{line} < 77 mA:

$$I_{LED} = \frac{I_{line} - 17}{3}$$

This LED driver is referenced to SLPE. Consequently, all the I_{LED} supply current will flow through the R_{SLPE} resistor. The AGC characteristics are not disturbed (see Fig.3 for the supply configuration).

Microphone amplifier (pins MIC+, MIC− and GAS)

The TEA1113 has symmetrical microphone inputs. The input impedance between pins MIC+ and MIC− is 64 kΩ (2 × 32 kΩ). The voltage gain from pins MIC+/MIC− to pin LN is set to 51.8 dB (typ). The gain can be decreased by connecting an external resistor R_{GAS} between pins GAS and REG. The adjustment range is 13 dB. A capacitor C_{GAS} connected between pins GAS and REG can be used to provide a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAS} \times (R_{GASint} // R_{GAS})$. R_{GASint} is the internal resistor which sets the gain with a typical value of 69 kΩ.

Automatic gain control is provided on this amplifier for line loss compensation.

Dynamic limiter and microphone mute (pin DLS/$\overline{\text{MMUTE}}$)

The dynamic limiter only acts on the microphone channel, this is to prevent clipping of the line signal. To prevent distortion, the microphone gain is rapidly reduced when peaks on the line signal exceed an internally determined threshold level or when the current in the transmit output stage is insufficient. The time in which the gain reduction is realized is very short (attack time). The microphone channel stays in the reduced gain condition until the peaks

on the line signal remain below the threshold level. The microphone gain then returns to its nominal value after a time determined by the capacitor C_{DLS} (release time).

The maximum output swing on the line depends on the DC voltage setting (V_{ref}). The internal threshold level is automatically adapted.

A LOW level on pin DLS/$\overline{\text{MMUTE}}$ inhibits the microphone inputs MIC+ and MIC– without affecting the DTMF and receiving inputs. Removing the LOW level from pin DLS/$\overline{\text{MMUTE}}$ provides the normal function of the microphone amplifier after a short time which is determined by capacitor C_{DLS}. With the value of the capacitor at 470 nF, the release time is in the order of a few tenths of a millisecond. The microphone mute function can be realized by a simple switch as illustrated in Fig.9.

Receiving amplifier (pins IR, GAR and QR)

The receiving amplifier has one input (IR) and one output (QR). The input impedance between pin IR and pin V_{EE} is 20 kΩ. The voltage gain from pin IR to pin QR is fixed to 31.3 dB (typ). The gain can be decreased by connecting an external resistor R_{GAR} between pins GAR and QR; the adjustment range is 12 dB. Two external capacitors C_{GAR} (connected between GAR and QR) and C_{GARS} (connected between GAR and V_{EE}) ensure stability. The C_{GAR} capacitor provides a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAR} \times (R_{GARint} // R_{GAR})$. R_{GARint} is the internal resistor which sets the gain with a typical value of 100 kΩ. The relationship $C_{GARS} = 10 \times C_{GAR}$ must be fulfilled to ensure stability.

The output voltage of the receiving amplifier is specified for continuous wave drive. The maximum output swing depends on the DC line voltage, the R_{CC} resistor, the I_{CC} current consumption of the circuit, the I_p current consumption of the peripheral circuits and the load impedance.

Automatic gain control is provided on this amplifier for line loss compensation.

Automatic gain control (pin AGC)

The TEA1113 performs automatic line loss compensation. The automatic gain control varies the gain of the microphone amplifier and the gain of the receiving amplifier in accordance with the DC line current. The control range is 5.8 dB (which corresponds approximately to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km).

The IC can be used with different configurations of feeding bridge (supply voltage and bridge resistance) by connecting an external resistor R_{AGC} between pins AGC and V_{EE}. This resistor enables the I_{start} and I_{stop} line currents to be increased (the ratio between I_{start} and I_{stop} is not affected by the resistor). The AGC function is disabled when pin AGC is left open-circuit.

Mute function (pin $\overline{\text{MUTE}}$)

The mute function performs the switching between the speech mode and the dialling mode. When $\overline{\text{MUTE}}$ is LOW or open-circuit, the DTMF input is enabled and the microphone and receiving amplifiers inputs are disabled. When $\overline{\text{MUTE}}$ is HIGH, the microphone and receiving amplifiers inputs are enabled while the DTMF input is disabled.

DTMF amplifier (pin DTMF)

When the DTMF amplifier is enabled, dialling tones may be sent on line. These tones can be heard in the earpiece at a low level (confidence tone).

The TEA1113 has an asymmetrical DTMF input. The input impedance between DTMF and V_{EE} is 20 kΩ. The voltage gain from pin DTMF to pin LN is 25.4 dB. When the resistor R_{GAS} is connected, to decrease the microphone gain, the DTMF gain varies in the same way (the DTMF gain is 26.4 dB lower than the microphone gain with no AGC control).

The automatic gain control has no effect on the DTMF amplifier.

Sidetone suppression

The TEA1113 anti-sidetone network comprising $R_{CC} // Z_{line}$, R_{ast1}, R_{ast2}, R_{ast3}, R_{SLPE} and Z_{bal} (see Fig.10) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = R_{CC} \times (R_{ast2} + R_{ast3})$$

$$k = \frac{(R_{ast2} \times (R_{ast3} + R_{SLPE}))}{(R_{ast1} \times R_{SLPE})}$$

$$Z_{bal} = k \times Z_{line}$$

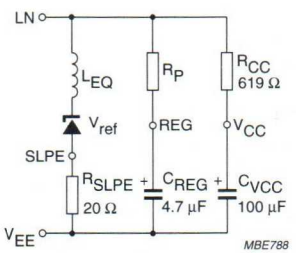
The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice, Z_{line} varies considerably with the line type and the line length. Therefore, the value chosen for Z_{bal} should be for an average line length which gives satisfactory sidetone suppression with short and long lines.
The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

The anti-sidetone network for the TEA1113 (as shown in Fig.14) attenuates the receiving signal from the line by 32 dB before it enters the receiving amplifier.
The attenuation is almost constant over the whole audio frequency range.

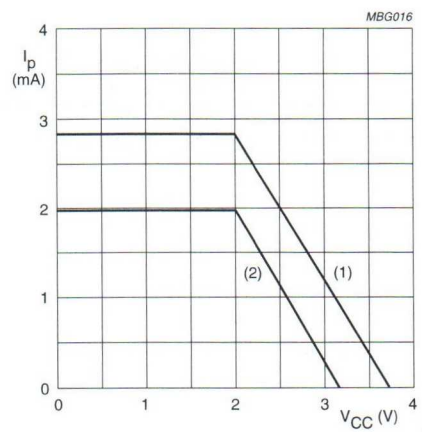
A Wheatstone bridge configuration (see Fig.11) may also be used.

More information on the balancing of an anti-sidetone bridge can be obtained in our publication *"Applications Handbook for Wired Telecom Systems, IC03b"*, order number 9397 750 00811.



$L_{eq} = C_{REG} \times R_{SLPE} \times R_P$; R_P = internal resistance; R_P = 15.5 kΩ.

Fig.7 Equivalent impedance between LN and V_{EE}.



(1) With R_{VA} resistor.
(2) Without R_{VA} resistor.

Fig.6 Typical current I_P available from V_{CC} for peripheral circuits at I_{line} = 15 mA.

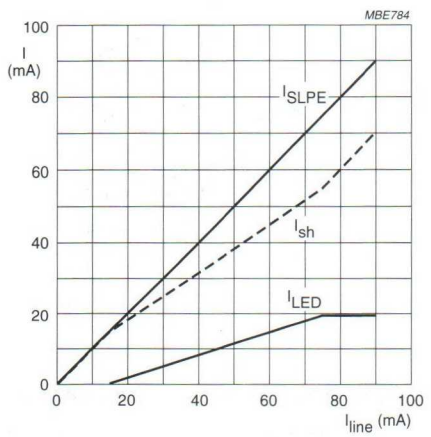


Fig.8 Available current to drive an LED.

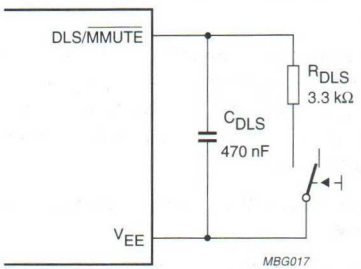


Fig.9 Microphone mute function.

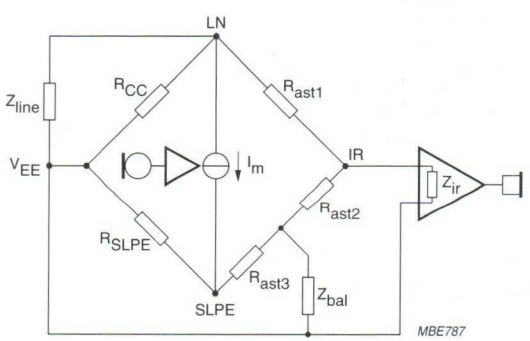


Fig.10 Equivalent circuit of TEA1113 anti-sidetone bridge.

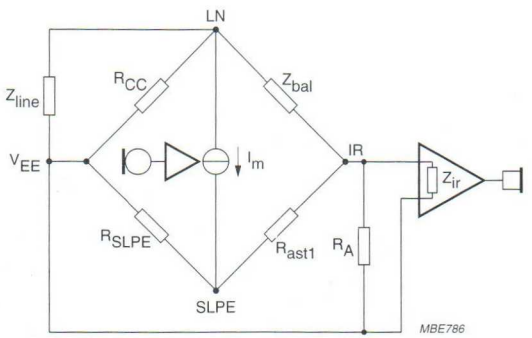


Fig.11 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

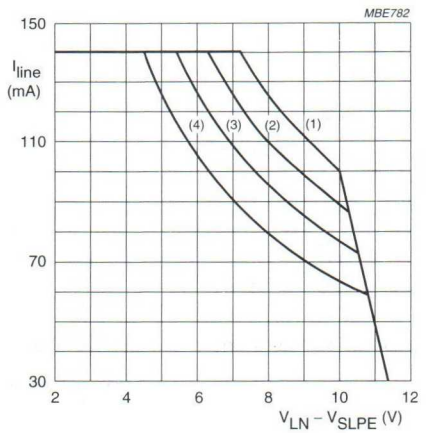
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		V_{EE} – 0.4	12.0	V
	repetitive line voltage during switch-on or line interruption		V_{EE} – 0.4	13.2	V
$V_{n(max)}$	maximum voltage on pins I_{LED}, SLPE		V_{EE} – 0.4	V_{LN} + 0.4	V
	maximum voltage on all other pins		V_{EE} – 0.4	V_{CC} + 0.4	V
I_{line}	line current	R_{SLPE} = 20 Ω; see Figs 12 and 13	–	140	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C; see Figs 12 and 13			
	TEA1113		–	625	mW
	TEA1113T		–	416	mW
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

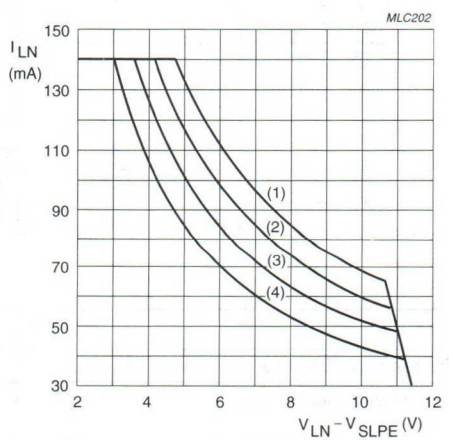
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air (TEA1113)	80	K/W
	thermal resistance from junction to ambient in free air mounted on epoxy board 40.1 × 19.1 × 1.5 mm (TEA1113T)	130	K/W



LINE	T_{amb} (°C)	P_{tot} (mW)
(1)	45	1000
(2)	55	875
(3)	65	750
(4)	75	625

Fig.12 Safe operating area (TEA1113).



LINE	T_{amb} (°C)	P_{tot} (mW)
(1)	45	666
(2)	55	583
(3)	65	500
(4)	75	416

Fig.13 Safe operating area (TEA1113T).

CHARACTERISTICS

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; C_{DLS} = 470 nF; AGC pin connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins V_{LN}, V_{CC}, SLPE and REG)						
V_{ref}	stabilized voltage between LN and SLPE		3.45	3.7	3.95	V
V_{LN}	DC line voltage	I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	2.5	–	V
		I_{line} = 15 mA	3.7	4	4.3	V
		I_{line} = 140 mA	–	–	7.0	V
$V_{LN(exR)}$	DC line voltage with an external resistor R_{VA}	$R_{VA(LN-REG)}$ = 82 kΩ	–	3.6	–	V
		$R_{VA(SLPE-REG)}$ = 27 kΩ	–	4.75	–	V
$\Delta V_{LN(T)}$	DC line voltage variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C	–	±30	–	mV
I_{CC}	internal current consumption	V_{CC} = 3.2 V	–	1.3	1.6	mA
V_{CC}	supply voltage for peripherals	I_p = 0 mA	2.8	3.2	–	V
R_{CCint}	equivalent supply voltage impedance	I_p = 0.5 mA	–	550	620	Ω
LED supply (pin I_{LED})						
$I_{line(h)}$	highest line current for I_{LED} < 0.6 mA		–	18	–	mA
$I_{line(l)}$	lowest line current for maximum I_{LED}		–	76	–	mA
$I_{LED(max)}$	maximum supply current available		–	19.5	–	mA
Microphone amplifier (pins MIC+, MIC− and GAS)						
$\|Z_i\|$	input impedance					
	differential between pins MIC+ and MIC−		–	64	–	kΩ
	single-ended between pins MIC+/MIC− and V_{EE}		–	32	–	kΩ
G_{vtx}	voltage gain from MIC+/MIC− to LN	V_{MIC} = 2 mV (RMS)	50.6	51.8	53	dB
$\Delta G_{vtx(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vtx(T)}$	gain variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C	–	±0.3	–	dB
CMRR	common mode rejection ratio		–	80	–	dB
ΔG_{vtxr}	gain voltage reduction range	external resistor connected between GAS and REG	–	–	13	dB
V_{notx}	noise output voltage at pin LN; pins MIC+ / MIC− shorted through 200 Ω	psophometrically weighted (P53 curve)	–	−70.5	–	dBmp

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Dynamic limiter and microphone mute (pin DLS/$\overline{\text{MMUTE}}$)						
DYNAMIC LIMITER BEHAVIOUR						
$V_{LN(max)(p-p)}$	maximum output voltage swing on the line (peak-to-peak value)	I_{line} = 15 mA; V_{ref} = 3.7 V	3.8	4.65	–	V
		I_{line} = 4 mA	–	1.6	–	
THD	total harmonic distortion	V_{MIC} = 4 mV (RMS) + 10 dB	–	–	2	%
		V_{MIC} = 4 mV (RMS) + 15 dB	–	–	10	%
t_{att}	attack time, V_{MIC} jumps from 2 mV up to 20 mV	C_{DLS} = 470 nF	–	1.5	5	ms
t_{rel}	release time, V_{MIC} jumps from 20 mV down to 2 mV	C_{DLS} = 470 nF	50	150	–	ms
MICROPHONE MUTE INPUT						
ΔG_{vtxm}	gain reduction	DLS/$\overline{\text{MMUTE}}$ = LOW	–	80	–	dB
V_{IL}	LOW level input voltage		V_{EE} – 0.4	–	V_{EE} + 0.3	V
I_{IL}	LOW level input current		40	60	–	µA
t_{rel}	release time after a LOW level on pin DLS/$\overline{\text{MMUTE}}$	C_{DLS} = 470 nF	–	30	–	ms
Receiving amplifier (pins IR, QR and GAR)						
$\lvert Z_i \rvert$	input impedance		–	20	–	kΩ
G_{vrx}	voltage gain from IR to QR	V_{IR} = 4 mV (RMS)	30.3	31.3	32.3	dB
$\Delta G_{vrx(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vrx(T)}$	gain variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
ΔG_{vrxr}	gain voltage reduction range	external resistor connected between GAR and QR	–	–	12	dB
$V_{o(rms)}$	maximum output voltage (RMS value)	I_p = 0 mA sine wave drive; R_L = 150 Ω; THD = 2%	240	290	–	mV
		I_p = 0 mA sine wave drive; R_L = 450 Ω; THD = 2%	350	410	–	mV
$V_{norx(rms)}$	noise output voltage at pin QR (RMS value)	R_L = 150 Ω; IR open-circuit; psophometrically weighted (P53 curve)	–	–86	–	dBVp
Automatic gain control (pin AGC)						
ΔG_{vtrx}	gain control range for microphone and receiving amplifiers with respect to I_{line} = 15 mA	I_{line} = 85 mA	–	5.8	–	dB
I_{start}	highest line current for maximum gain		–	25	–	mA
I_{stop}	lowest line current for minimum gain		–	59	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DTMF amplifier (pin DTMF)						
$\|Z_i\|$	input impedance		–	20	–	kΩ
G_{vdtmf}	voltage gain from DTMF to LN	V_{DTMF} = 25 mV (RMS); $\overline{MUTE}$ = LOW	24.2	25.4	26.6	dB
$\Delta G_{vdtmf(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vdtmf(T)}$	gain variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C	–	±0.5	–	dB
G_{vct}	voltage gain from DTMF to QR (confidence tone)	R_L = 150 Ω; V_{DTMF} = 25 mV (RMS)	–	−18	–	dB
Mute function (pin $\overline{MUTE}$)						
V_{IL}	LOW level input voltage		V_{EE} − 0.4	–	V_{EE} + 0.3	V
V_{IH}	HIGH level input voltage		V_{EE} + 1.5	–	V_{CC} + 0.4	V
I_{MUTE}	input current	$\overline{MUTE}$ = HIGH	–	1.25	3	μA
ΔG_{vtrxm}	gain reduction for microphone and receiving amplifiers	$\overline{MUTE}$ = LOW	–	80	–	dB

APPLICATION INFORMATION

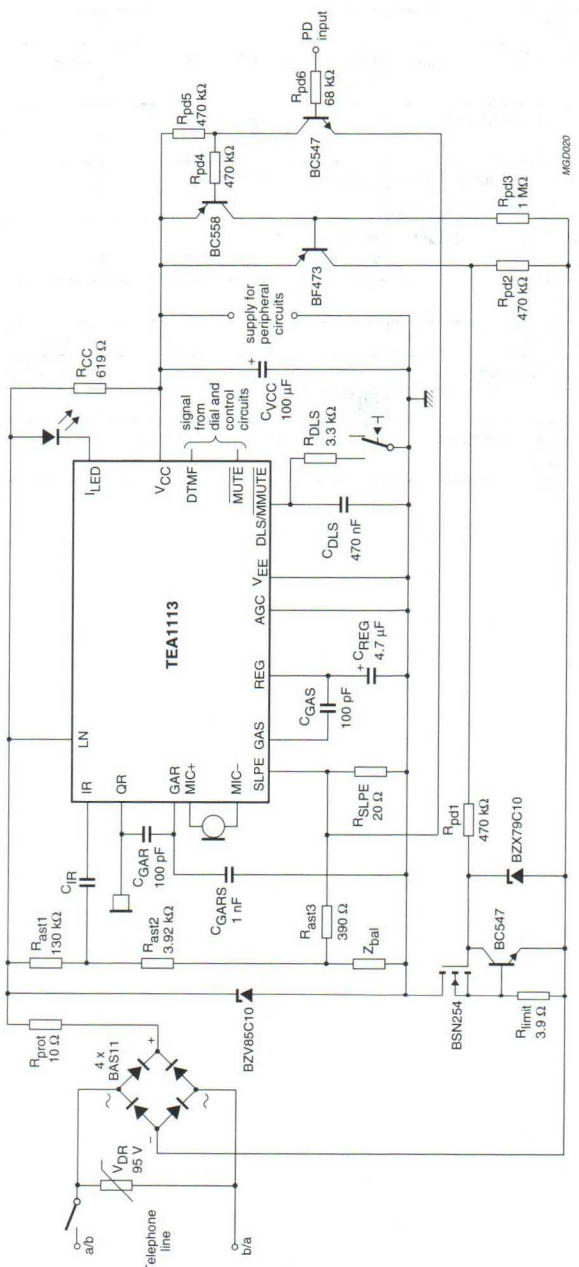


Fig.14 Typical application of the TEA1113 in sets with Pulse Dialling or Flash facilities.

Low voltage telephone transmission circuit with dialler interface and regulated strong supply

TEA1114A

FEATURES

- Low DC line voltage; operates down to 1.6 V (excluding voltage drop over external polarity guard)
- Line voltage regulator with adjustable DC voltage
- 3.3 V regulated strong supply point for peripheral circuits compatible with:
  - Speech mode
  - Ringer mode
  - Trickle mode
- Transmit stage with:
  - Microphone amplifier with symmetrical high impedance inputs
  - DTMF amplifier with confidence tone on receive output
- Receive stage with:
  - Receive amplifier with asymmetrical output
  - Earpiece amplifier with adjustable gain (and gain boost facility) for all types of earpieces
- $\overline{\text{MUTE}}$ input for pulse or DTMF dialling
- AGC line loss compensation for microphone and receive amplifiers.

APPLICATIONS

- Line powered telephone sets with LCD module
- Cordless telephones
- Fax machines
- Answering machines.

GENERAL DESCRIPTION

The TEA1114A is a bipolar integrated circuit that performs all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between speech and dialling. The IC operates at a line voltage down to 1.6 V DC (with reduced performance) to facilitate the use of telephone sets connected in parallel.

When the line current is high enough, a fixed amount of current is derived from the LN pin in order to create a strong supply point at pin V_{DD}. The voltage at pin V_{DD} is regulated to 3.3 V to supply peripherals such as dialler, LCD module and microcontroller.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1114A	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
TEA1114AT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

QUICK REFERENCE DATA

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; AGC pin connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; measured according to test circuits given in Figs 14, 15 and 16; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range	normal operation	11	–	140	mA
		with reduced performance	1	–	11	mA
V_{LN}	DC line voltage		4.05	4.35	4.65	V
I_{CC}	internal current consumption	V_{CC} = 3.7 V	–	1.25	1.5	mA
V_{CC}	supply voltage for internal circuitry (unregulated)	I_P = 0 mA	–	3.6	–	V
V_{DD}	regulated supply voltage for peripherals					
	speech mode	I_{DD} = −2.5 mA	3.0	3.3	3.6	V
	ringer mode	I_{DD} = 75 mA	3.0	3.3	3.6	V
I_{DD}	available supply current for peripherals		–	–	−2.5	mA
$G_{v(TX)}$	typical voltage gain for microphone amplifier	V_{MIC} = 4 mV (RMS)	43.2	44.2	45.2	dB
$G_{v(RX)}$	typical voltage gain for receiving amplifier	V_{IR} = 4 mV (RMS)	32.4	33.4	34.4	dB
$\Delta G_{v(QR)}$	gain setting range for earpiece amplifier	R_{E1} = 100 kΩ	−14	–	+12	dB
$\Delta G_{v(trx)}$	gain control range for microphone and receive amplifiers with respect to I_{line} = 15 mA	I_{line} = 85 mA	–	6.0	–	dB
$\Delta G_{v(trx)(m)}$	gain reduction for microphone and receive amplifiers	$\overline{MUTE}$ = LOW	–	80	–	dB

BLOCK DIAGRAM

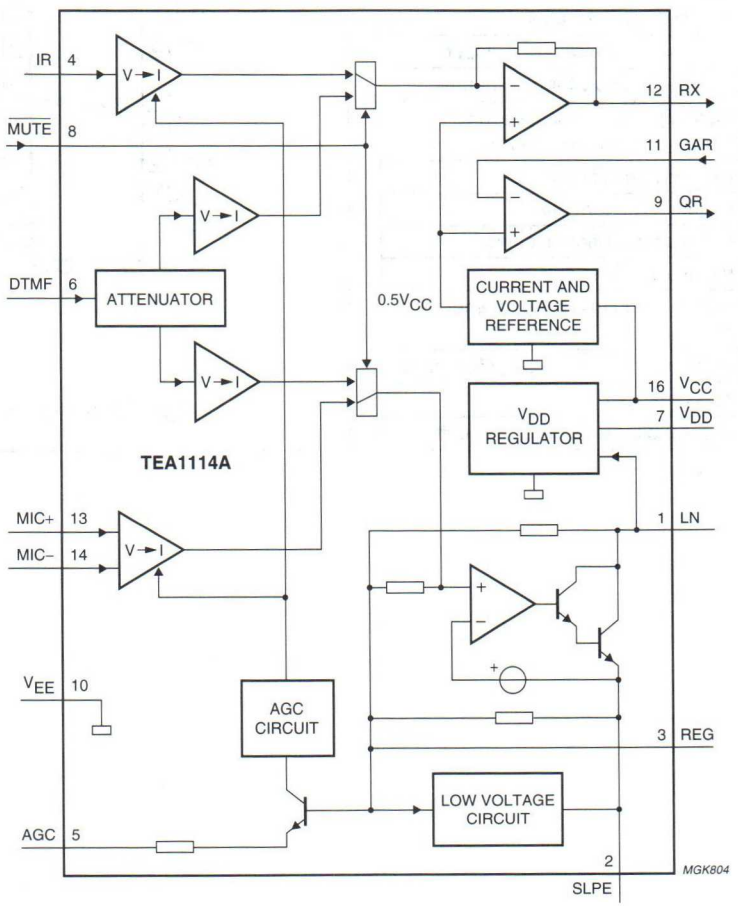


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
SLPE	2	slope (DC resistance) adjustment
REG	3	line voltage regulator decoupling
IR	4	receive amplifier input
AGC	5	automatic gain control/ line loss compensation
DTMF	6	dual-tone multi-frequency input
V_{DD}	7	regulated supply for peripherals
$\overline{MUTE}$	8	mute input to select speech or dialling mode (active LOW)
QR	9	earpiece amplifier output
V_{EE}	10	negative line terminal
GAR	11	earpiece amplifier inverting input
RX	12	receive amplifier output
MIC+	13	non-inverting microphone amplifier input
MIC–	14	inverting microphone amplifier input
n.c.	15	not connected
V_{CC}	16	supply voltage for internal circuit

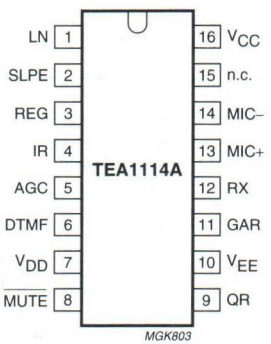


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supply (pins LN, SLPE, REG, V_{CC} and V_{DD})

The supply for the TEA1114A and its peripherals is obtained from the telephone line (see Fig.3).

THE LINE INTERFACE (PINS LN, SLPE AND REG)

The IC generates a stabilized reference voltage (V_{ref}) between pins LN and SLPE. V_{ref} is temperature compensated and can be adjusted by means of an external resistor (R_{VA}). V_{ref} equals 4.15 V and can be increased by connecting R_{VA} between pins REG and SLPE or decreased by connecting R_{VA} between pins REG and LN. The voltage at pin REG is used by the internal regulator to generate V_{ref} and is decoupled by C_{REG}, which is connected to V_{EE}.
This capacitor, converted into an equivalent inductance (see Section "Set impedance") realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (R_{CC} in the audio-frequency range). The voltage at pin SLPE is proportional to the line current.

The voltage at pin LN is:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I_{CC} - I_P - I_{SUP}$$

where:

I_{line} = line current

I_{CC} = current consumption of the IC

I_P = supply current for external circuits

I_{SUP} = current consumed between LN and V_{EE} by the V_{DD} regulator.

The preferred value for R_{SLPE} is 20 Ω. Changing R_{SLPE} will affect more than the DC characteristics; it also influences the microphone and DTMF gains, the gain control characteristics, the sidetone level and the maximum output swing on the line.

The DC line current flowing into the set is determined by the exchange supply voltage (V_{EXCH}), the feeding bridge resistance (R_{EXCH}), the DC resistance of the telephone line (R_{line}) and the reference voltage (V_{ref}). With line currents below 9 mA, the internal reference voltage (generating V_{ref}) is automatically adjusted to a lower value. This means that more sets can operate in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. At currents below 9 mA, the circuit has limited sending and receiving levels. This is called the low voltage area.

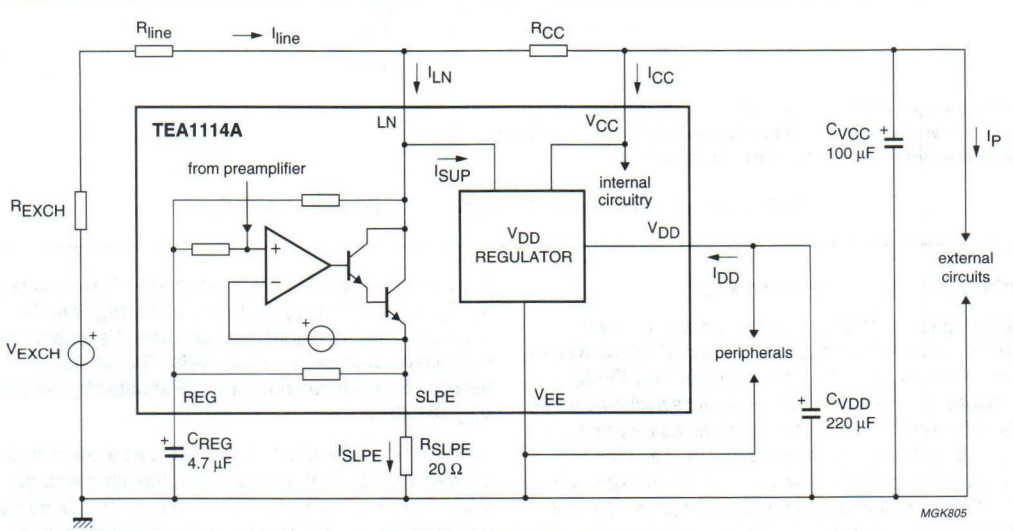


Fig.3 Supply configuration.

THE INTERNAL SUPPLY POINT (PIN V_{CC})

The internal circuitry of the TEA1114A is supplied from pin V_{CC}. This voltage supply is derived from the line voltage by means of a resistor (R_{CC}) and must be decoupled by a capacitor C_{VCC}. It may also be used to supply some external circuits. The V_{CC} voltage depends on the current consumed by the IC and the peripheral circuits as:

$$V_{CC0} = V_{LN} - R_{CC} \times I_{CC}$$

$$V_{CC} = V_{CC0} - R_{CC} \times (I_P + I_{rec})$$

(see also Figs 4 and 5). I_{rec} is the current consumed by the output stage of the earpiece amplifier.

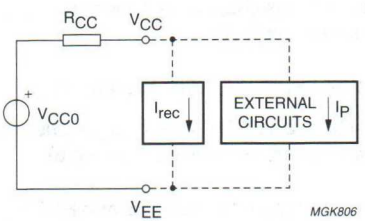
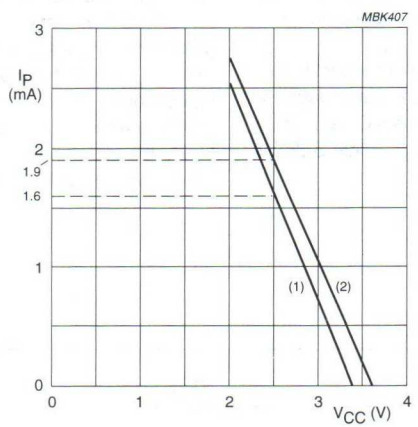


Fig.4 V_{CC} used as supply voltage for external circuits.



$V_{CC} \geq 2.5$ V; $V_{LN} = 4.35$ V at $I_{line} = 15$ mA; $R_{CC} = 619\ \Omega$; $R_{SLPE} = 20\ \Omega$
Curve (1) is valid when the receiving amplifier is driven: $V_{QR(rms)} = 150$ mV; $R_{L1} = 150\ \Omega$.
Curve (2) is valid when the receiving amplifier is not driven.

Fig.5 Typical current I_P available from V_{CC} for peripheral circuitry.

THE REGULATED SUPPLY POINT (PIN V_{DD})

The V_{DD} regulator delivers a stabilized voltage for the peripherals in transmission mode (nominal V_{LN}) as well as in ringer mode ($V_{LN} = 0$ V). The regulator (see Fig.6) consists of a sense input circuit, a current switch and a V_{DD} output stabilizer. The regulator operates as a current source at the LN input in transmission mode; it takes a constant current of 3.7 mA (at nominal conditions) from pin LN. The current switch reduces the distortion on the line at large signal swings. Output V_{DD} follows the DC voltage at pin LN (with typically 0.35 V difference) up to $V_{DD} = 3.3$ V. The input current of the regulator is constant while the output (source) current is determined by the consumption of the peripherals. The difference between input and output current is shunted by the internal V_{DD} stabilizer.

In ringer mode, the stabilizer operates as a shunt stabilizer to keep V_{DD} at 3.3 V. In this mode, the input voltage $V_{LN} = 0$ V while the input current into pin V_{DD} is delivered by the ringing signal. V_{DD} has to be decoupled by a capacitor C_{VDD}.

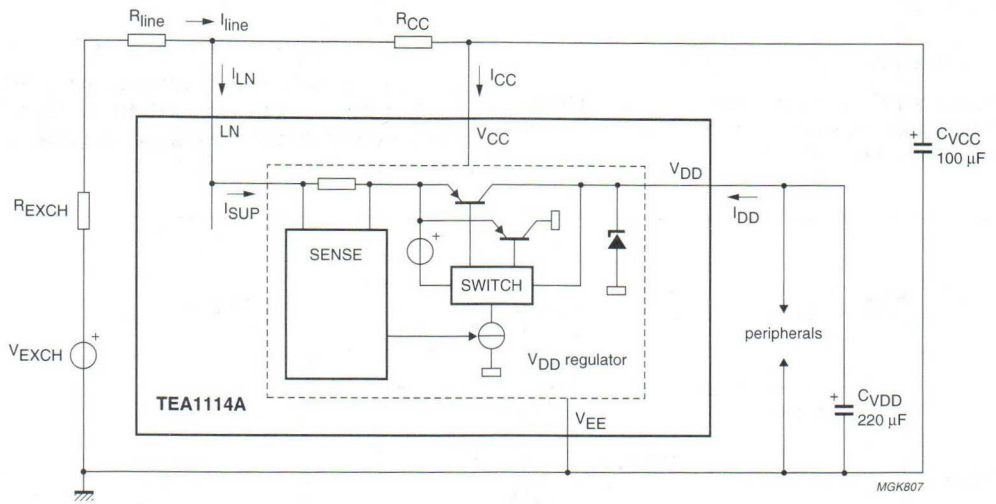


Fig.6 V_{DD} regulator configuration.

Set impedance

In the audio frequency range, the dynamic impedance is mainly determined by the R_{CC} resistor. The equivalent impedance of the circuit is illustrated in Fig.7.

Transmit stage (pins MIC+, MIC– and DTMF)

MICROPHONE AMPLIFIER (PINS MIC+ AND MIC–)

The TEA1114A has symmetrical microphone inputs. The input impedance between pins MIC+ and MIC– is 64 kΩ (2 × 32 kΩ). The voltage gain from pins MIC+/MIC– to pin LN is set at 44.2 dB (typically).

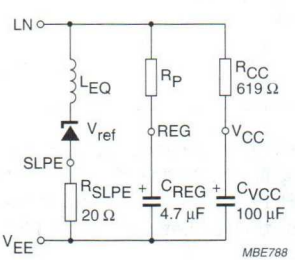
Automatic gain control is provided on this amplifier for line loss compensation.

DTMF AMPLIFIER (PIN DTMF)

When the DTMF amplifier is enabled, dialling tones may be sent on line. These tones are also sent to the receive output RX at a low level (confidence tone).

The TEA1114A has an asymmetrical DTMF input. The input impedance between DTMF and V_{EE} is 20 kΩ. The voltage gain from pin DTMF to pin LN is set at 26 dB.

Automatic gain control has no effect on the DTMF amplifier.



$L_{EQ} = C_{REG} \times R_{SLPE} \times R_P$.
R_P = internal resistance.
R_P = 17.5 kΩ.

Fig.7 Equivalent impedance between LN and V_{EE}.

Receiving stage (pins IR, RX, GAR and QR)

The receive part consists of a receive amplifier and an earpiece amplifier.

THE RECEIVE AMPLIFIER (PINS IR AND RX)

The receive amplifier transfers the receive signal from input IR to output RX. The input impedance of the receive amplifier, between pins IR and V_{EE}, is 20 kΩ.

The voltage gain from pin IR to RX is set at 33.4 dB. RX output is intended to drive high ohmic (real) loads. Automatic gain control is provided on the receive amplifier.

THE EARPIECE AMPLIFIER (PINS GAR AND QR)

The earpiece amplifier is an operational amplifier having its output (QR) and inverting input (GAR) available. It can be used in conjunction with two resistors to get some extra gain or attenuation.

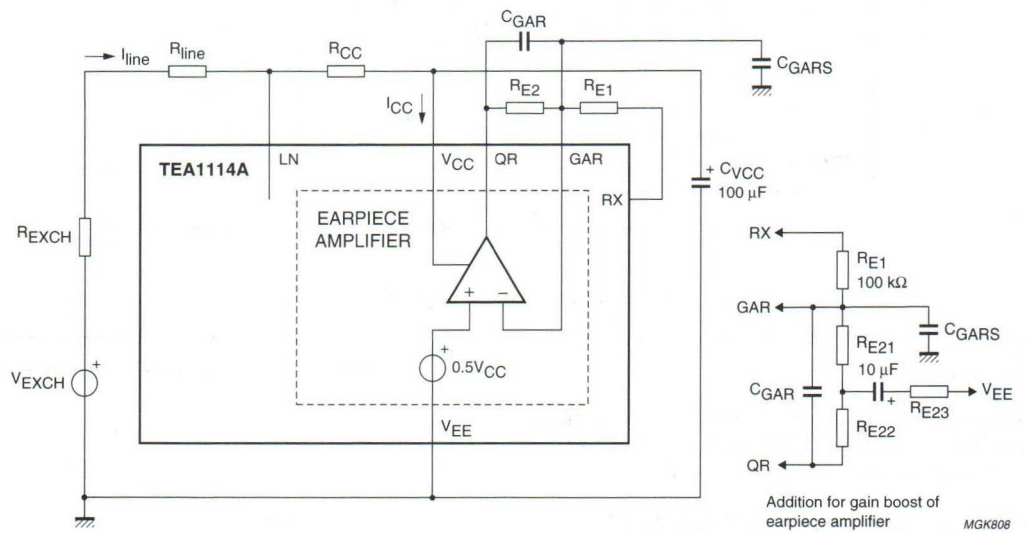


Fig.8 Earpiece amplifier configuration.

In an usual configuration (see Fig.8), output RX drives the earpiece amplifier by means of R_{E1} connected between RX and GAR. Feedback resistor R_{E2} of the earpiece amplifier is connected between QR and GAR. Output QR drives the earpiece.

The gain of the earpiece amplifier (from RX to QR) can be set between +12 and −14 dB by means of resistor R_{E2}. The preferred value of R_{E1} is 100 kΩ.

The earpiece amplifier offers a gain boost facility relative to the initial gain. Resistor R_{E2} has to be replaced by the network of R_{E21}, R_{E22} and R_{E23} as shown in Fig.8.

The initial gain is defined by: $-\frac{R_{E21} + R_{E22}}{R_{E1}}$

which corresponds to $R_{E23} = \infty$. The gain boost is realized by a defined value of R_{E23} and is:

$$-\frac{R_{E21} + R_{E22}}{R_{E1}} \times \left(1 + \frac{R_{E21} \,//\, R_{E22}}{R_{E23}}\right)$$

Two external capacitors C_{GAR} (connected between GAR and QR) and C_{GARS} (connected between GAR and V_{EE}) ensure stability. The C_{GAR} capacitor provides a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAR} \times R_{E2}$. The relationship $C_{GARS} = 10 \times C_{GAR}$ must be fulfilled to ensure stability.

The output voltages of both amplifiers are specified for continuous wave drive. The maximum output swing depends on the DC line voltage V_{LN}, the R_{CC} resistor, the I_{CC} current consumption of the circuit, the I_P current consumption of the peripheral circuits and the load impedance.

Automatic gain control (pin AGC)

The TEA1114A performs automatic line loss compensation. The automatic gain control varies the gain of the microphone amplifier and the gain of the receive amplifier in accordance with the DC line current.

The control range is 6.0 dB (which corresponds approximately to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km).

The IC can be used with different configurations of feeding bridge (supply voltage and bridge resistance) by connecting an external resistor R_{AGC} between pins AGC and V_{EE}. This resistor enables the I_{start} and I_{stop} line currents to be increased (the ratio between I_{start} and I_{stop} is not affected by the resistor). The AGC function is disabled when pin AGC is left open-circuit.

Mute function (pin $\overline{\text{MUTE}}$)

The mute function performs the switching between the speech mode and the dialling mode.

When $\overline{\text{MUTE}}$ is LOW, the DTMF input is enabled and the microphone and receive amplifier inputs are disabled. In this mode, the DTMF tones are sent to the receive output at a low level (confidence tone).

When $\overline{\text{MUTE}}$ is HIGH, the microphone and receiving amplifiers inputs are enabled while the DTMF input is disabled. The $\overline{\text{MUTE}}$ input is provided with an internal pull-up current source to V_{CC}.

SIDETONE SUPPRESSION

The TEA1114A anti-sidetone network comprising R_{CC} // Z_{line}, R_{ast1}, R_{ast2}, R_{ast3}, R_{SLPE} and Z_{bal} (see Fig.9) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = R_{CC} \times (R_{ast2} + R_{ast3})$$

$$k = \frac{R_{ast2} \times (R_{ast3} + R_{SLPE})}{R_{ast1} \times R_{SLPE}}$$

$$Z_{bal} = k \times Z_{line}$$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice, Z_{line} varies considerably with the line type and the line length. Therefore, the value of Z_{bal} should be for an average line length which gives satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

The anti-sidetone network for the TEA1114A attenuates the receiving signal from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range.

A Wheatstone bridge configuration (see Fig.10) may also be used.

More information on the balancing of an anti-sidetone bridge can be obtained in our publication *"Semiconductors for Wired Telecom Systems; Application Handbook, IC03b"*. For ordering information please contact the Philips Semiconductors sales office.

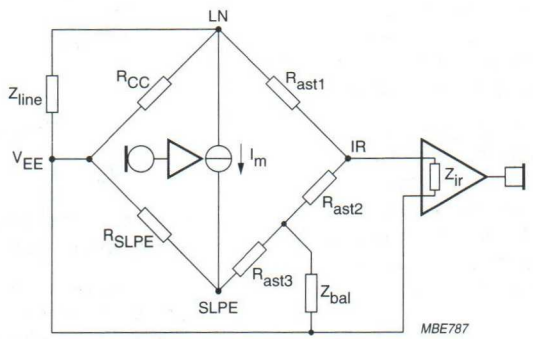


Fig.9 Equivalent circuit of TEA1114A anti-sidetone bridge.

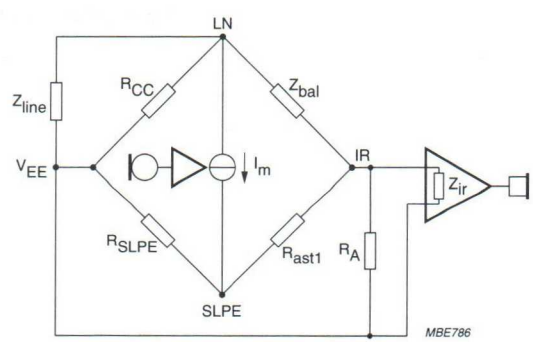


Fig.10 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

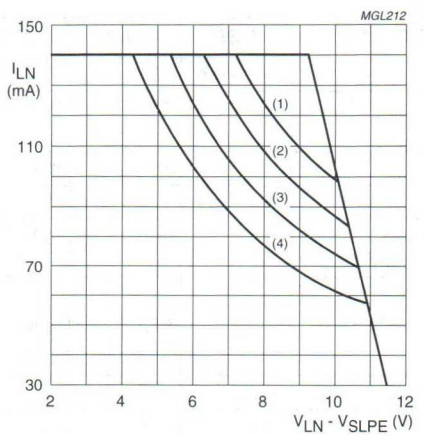
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		$V_{EE} - 0.4$	12	V
	repetitive line voltage during switch-on or line interruption		$V_{EE} - 0.4$	13.2	V
I_{DD}	maximum input current at pin V_{DD}		–	75	mA
$V_{n(max)}$	maximum voltage on all pins except pin V_{DD}		$V_{EE} - 0.4$	$V_{CC} + 0.4$	V
I_{line}	line current	$R_{SLPE} = 20\ \Omega$; see Figs 11 and 12	–	140	mA
P_{tot}	total power dissipation	$T_{amb} = 75\ °C$; see Figs 11 and 12			
	TEA1114A		–	625	mW
	TEA1114AT		–	416	mW
T_{stg}	storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; note 1		
	TEA1114A		70	K/W
	TEA1114AT		115	K/W

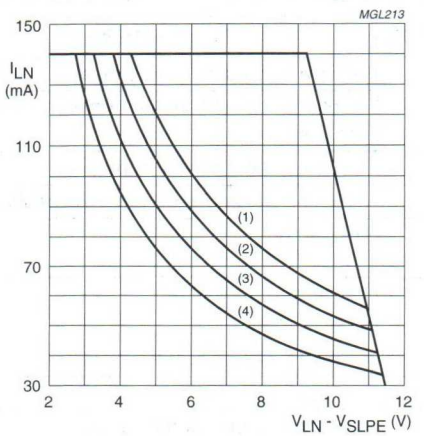
Note

1. Mounted on epoxy board 40.1 × 19.1 × 1.5 mm.



(1) T_{amb} = 45 °C; P_{tot} = 1.000 W.
(2) T_{amb} = 55 °C; P_{tot} = 0.875 W.
(3) T_{amb} = 65 °C; P_{tot} = 0.750 W.
(4) T_{amb} = 75 °C; P_{tot} = 0.625 W.

Fig.11 DIP16 safe operating area (TEA1114A).



(1) T_{amb} = 45 °C; P_{tot} = 0.666 W.
(2) T_{amb} = 55 °C; P_{tot} = 0.583 W.
(3) T_{amb} = 65 °C; P_{tot} = 0.500 W.
(4) T_{amb} = 75 °C; P_{tot} = 0.416 W.

Fig.12 SO16 safe operating area (TEA1114AT).

CHARACTERISTICS

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; pin AGC connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; measured according to test circuits given in Figs 14, 15 and 16; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins V_{LN}, V_{CC}, SLPE, REG and V_{DD})						
THE LINE INTERFACE (PINS LN, SLPE AND REG)						
V_{ref}	stabilized reference voltage between pins LN and SLPE		3.9	4.15	4.4	V
V_{LN}	DC line voltage	I_{line} = 1 mA	–	1.45	–	V
		I_{line} = 4 mA	–	2.7	–	V
		I_{line} = 15 mA	4.05	4.35	4.65	V
		I_{line} = 140 mA	–	7.1	7.55	V
$V_{LN(Rext)}$	DC line voltage with an external resistor R_{VA}	R_{VA} = 44.2 kΩ (between pins LN and REG)	–	3.6	–	V
$\Delta V_{LN(T)}$	DC line voltage variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±40	–	mV
THE INTERNAL SUPPLY POINT (PIN V_{CC})						
I_{CC}	internal current consumption	V_{CC} = 3.6 V	–	1.25	1.5	mA
V_{CC}	supply voltage for internal circuitry	I_P = 0 mA	–	3.6	–	V
THE REGULATED SUPPLY POINT (PIN V_{DD})						
I_{SUP}	input current of the V_{DD} regulator (current from pin LN not flowing through pin SLPE)	I_{line} = 1 mA	–	0	–	mA
		I_{line} = 4 mA	–	0.9	–	mA
		$I_{line} \geq$ 11 mA	–	3.7	–	mA
V_{DD}	regulated supply voltage in:					
	speech mode	I_{DD} = –2.5 mA; V_{LN} > 3.6 V + 0.25 V (typ.); $I_{line} \geq$ 11 mA	3.0	3.3	3.6	V
	speech mode at reduced performance	I_{line} = 4 mA	–	V_{LN} – 0.35	–	V
	ringer mode	I_{line} = 0 mA; I_{DD} = 75 mA	3.0	3.3	3.6	V
I_{DD}	regulated supply current available in:					
	speech mode	$I_{line} \geq$ 11 mA	–	–	–2.5	mA
	speech mode at reduced performance	I_{line} = 4 mA	–	–0.5	–	mA
	trickle mode	I_{line} = 0 mA; V_{CC} discharging; V_{DD} = 1.2 V	–	–	100	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit stage (pins MIC+, MIC– and DTMF)						
MICROPHONE AMPLIFIER (PINS MIC+ AND MIC–)						
$\|Z_i\|$	input impedance differential between pins MIC+ and MIC– single-ended between pins MIC+/MIC– and V_{EE}		– –	64 32	– –	kΩ kΩ
$G_{v(TX)}$	voltage gain from pins MIC+/MIC– to pin LN	V_{MIC} = 4 mV (RMS)	43.2	44.2	45.2	dB
$\Delta G_{v(TX)(f)}$	voltage gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{v(TX)(T)}$	voltage gain variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
CMRR	common mode rejection ratio		–	80	–	dB
$V_{LN(max)(rms)}$	maximum sending signal (RMS value)	I_{line} = 15 mA; THD = 2%	1.8	2.15	–	V
		I_{line} = 4 mA; THD = 10%	–	0.4	–	V
$V_{no(LN)}$	noise output voltage at pin LN	psophometrically weighted (P53 curve); pins MIC+/ MIC– shorted through 200 Ω	–	–78	–	dBmp
DTMF AMPLIFIER (PIN DTMF)						
$\|Z_i\|$	input impedance		–	20	–	kΩ
$G_{v(DTMF)}$	voltage gain from pin DTMF to pin LN	V_{DTMF} = 20 mV (RMS); $\overline{MUTE}$ = LOW	25	26	27	dB
$\Delta G_{v(DTMF)(f)}$	voltage gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{v(DTMF)(T)}$	voltage gain variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±0.4	–	dB
$G_{v(ct)}$	voltage gain from pin DTMF to pin RX (confidence tone)	V_{DTMF} = 20 mV (RMS); R_{L2} = 10 kΩ; $\overline{MUTE}$ = LOW	–	–9.2	–	dB
Receiving stage (pins IR, RX, GAR and QR)						
THE RECEIVE AMPLIFIER (PINS IR AND RX)						
$\|Z_i\|$	input impedance		–	20	–	kΩ
$G_{v(RX)}$	voltage gain from pin IR to pin RX	V_{IR} = 4 mV (RMS)	32.4	33.4	34.4	dB
$\Delta G_{v(RX)(f)}$	voltage gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{v(RX)(T)}$	voltage gain variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
$V_{RX(max)(rms)}$	maximum receiving signal on pin RX (RMS value)	I_P = 0 mA; sine wave drive; R_{L2} = 10 kΩ; THD = 2%	0.4	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert I_{RX(max)} \rvert$	maximum source and sink current on pin RX (peak value)	I_P = 0 mA; sine wave drive	50	–	–	µA
$V_{no(RX)(rms)}$	noise output voltage at pin RX (RMS value)	pin IR open-circuit; R_{L2} = 10 kΩ; psophometrically weighted (P53 curve)	–	–86	–	dBVp
THE EARPIECE AMPLIFIER (PINS GAR AND QR)						
$G_{v(QR)}$	voltage gain from pin RX to pin QR	V_{IR} = 4 mV (RMS); $R_{E1} = R_{E2}$ = 100 kΩ	–1	0	+1	dB
$\Delta G_{v(QR)}$	voltage gain setting	R_{E1} = 100 kΩ	–14	–	+12	dB
$V_{QR(max)(rms)}$	maximum receiving signal on pin QR (RMS value)	I_P = 0 mA; sine wave drive; R_{L1} = 150 Ω; THD = 2%	0.3	0.38	–	V
		I_P = 0 mA; sine wave drive; R_{L1} = 450 Ω; THD = 2%	0.46	0.56	–	V
$V_{no(QR)(rms)}$	noise output voltage at pin QR (RMS value)	IR open-circuit; R_{L1} = 150 Ω; $R_{E1} = R_{E2}$ = 100 kΩ psophometrically weighted (P53 curve)	–	–86	–	dBVp
		R_{E1} = 100 kΩ; R_{E2} = 25 kΩ	–	–100	–	dBVp
Automatic gain control (pin AGC)						
$\Delta G_{v(trx)}$	voltage gain control range for microphone and receive amplifiers with respect to I_{line} = 20 mA	I_{line} = 85 mA	–	6.0	–	dB
I_{start}	highest line current for maximum gain		–	23	–	mA
I_{stop}	lowest line current for minimum gain		–	59	–	mA
Mute function (pin $\overline{\text{MUTE}}$)						
V_{IL}	LOW-level input voltage		V_{EE} – 0.4	–	V_{EE} + 0.3	V
V_{IH}	HIGH-level input voltage		V_{EE} + 1.5	–	V_{CC} + 0.4	V
I_{MUTE}	input current		–	2	10	µA
$\Delta G_{v(trx)(m)}$	voltage gain reduction for:					
	microphone amplifier	$\overline{\text{MUTE}}$ = LOW	–	80	–	dB
	receive amplifier	$\overline{\text{MUTE}}$ = LOW	–	80	–	dB
	earpiece amplifier	$\overline{\text{MUTE}}$ = LOW	–	80	–	dB
	DTMF amplifier	$\overline{\text{MUTE}}$ = HIGH	–	80	–	dB

TEST AND APPLICATION INFORMATION

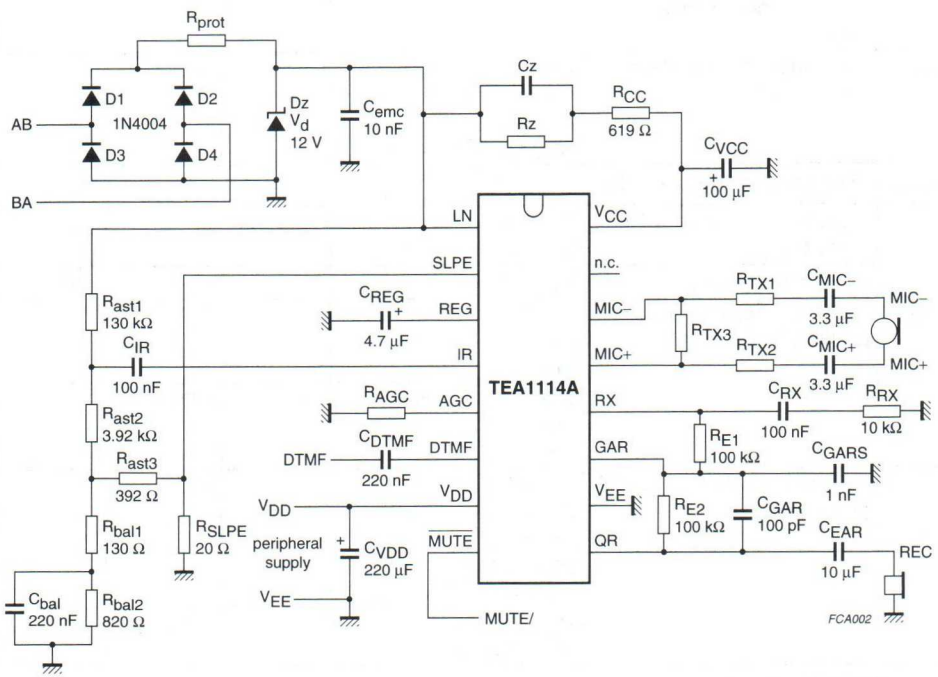
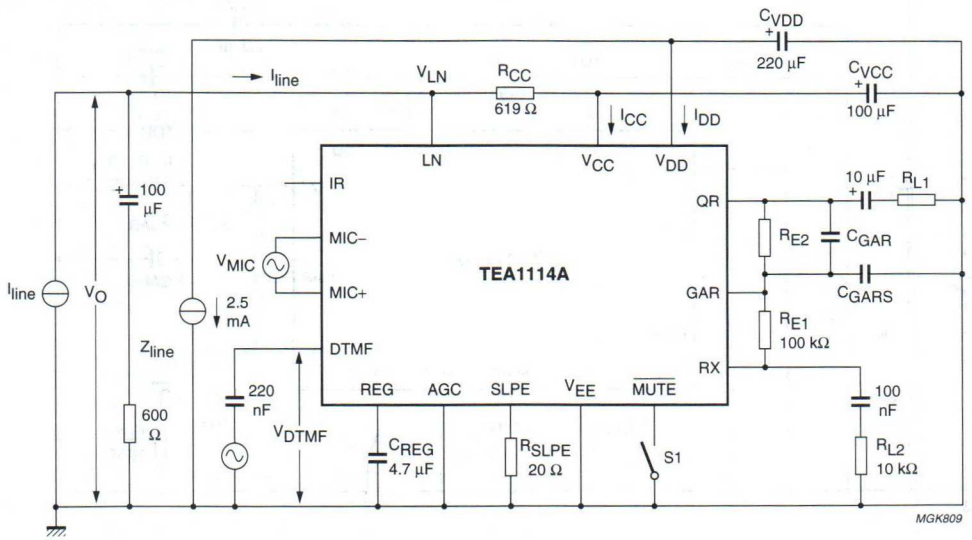


Fig.13 Basic application of the TEA1114A IC



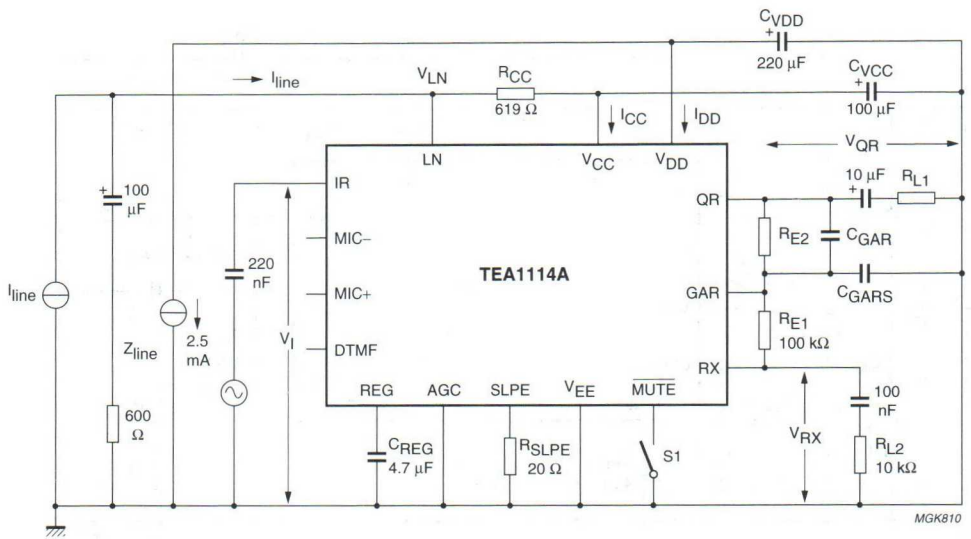
Voltage gain defined as $G_v = 20 \log \left|\frac{V_O}{V_I}\right|$; $V_I = V_{MIC}$ or V_{DTMF}.

Microphone gain: S1 = open.

DTMF gain and confidence tone: S1 = closed.

Inputs not being tested should be open-circuit.

Fig.14 Test figure for defining transmit gains.

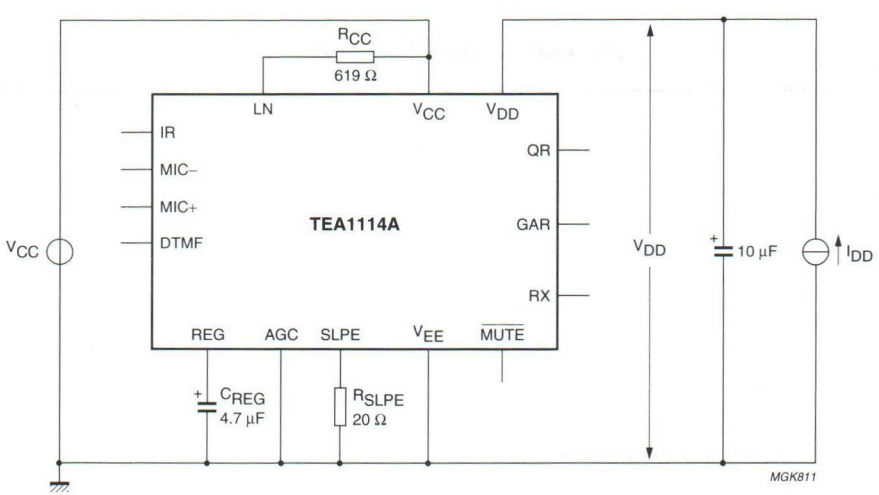


Voltage gain defined as $G_v = 20 \log \left|\frac{V_O}{V_I}\right|$; $V_O = V_{QR}$ or V_{RX}.

Receive and earpiece gains: S1 = open.

Inputs not being tested should be open-circuit.

Fig.15 Test figure for defining receive gains.



Inputs not being tested should be open-circuit.

Fig.16 Test figure for defining regulated supply (V_{DD}) performance in ringer and trickle mode.

Versatile cordless transmisssion circuit TEA1118; TEA1118A

FEATURES

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable DC voltage
- Provides a supply for external circuits
- Symmetrical high impedance transmit inputs (62.5 kΩ) with large signals handling capabilities [up to 1 V (RMS value) with less than 2% THD]
- Receive amplifier for dynamic, magnetic or piezoelectric earpieces
- AGC line loss compensation for transmit and earpiece amplifiers
- DTMF input with confidence tone (TEA1118A only)
- MUTE input for pulse or DTMF dialling (TEA1118A only)
- Transmit mute function, also enabling the DTMF input (TEA1118A only).

GENERAL DESCRIPTION

The TEA1118 and TEA1118A are bipolar integrated circuits that perform all speech and line interface functions required in cordless telephone base stations. The ICs operate at a line voltage down to 1.6 V DC (with reduced performance) to facilitate the use of telephone sets connected in parallel.

The TEA1118A offers in addition to the TEA1118 electronic switching between speech and dialling. Moreover the transmit amplifier can be disabled during speech condition by means of a transmit mute function.

All statements and values refer to all versions unless otherwise specified.

APPLICATIONS

- Cordless telephone base stations
- Fax machines
- Answering machines.

QUICK REFERENCE DATA

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; AGC pin connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range	normal operation	11	–	140	mA
		with reduced performance	1	–	11	mA
V_{LN}	DC line voltage		3.35	3.65	3.95	V
I_{CC}	internal current consumption	V_{CC} = 2.9 V	–	1.15	1.4	mA
V_{CC}	supply voltage for peripherals	I_P = 0 mA	–	2.9	–	V
G_{vtrx}	typical voltage gain range					
	transmit amplifier (TEA1118A only)	V_{TX} = 200 mV (RMS)	–	–	11.3	dB
	transmit amplifier (TEA1118 only)	V_{TX} = 200 mV (RMS)	5.3	–	11.3	dB
	receive amplifier	V_{IR} = 4 mV (RMS)	19	–	31	dB
ΔG_{vtrx}	gain control range for transmit and receive amplifiers with respect to I_{line} = 15 mA	I_{line} = 75 mA	–	5.8	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1118M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TEA1118T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TEA1118AM	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TEA1118AT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

BLOCK DIAGRAMS

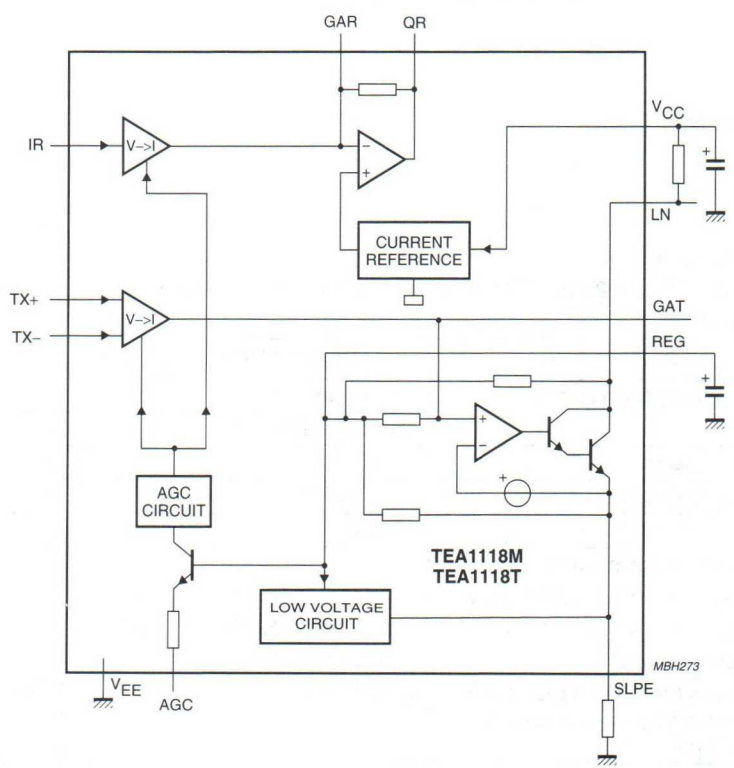


Fig.1 Block diagram (TEA1118).

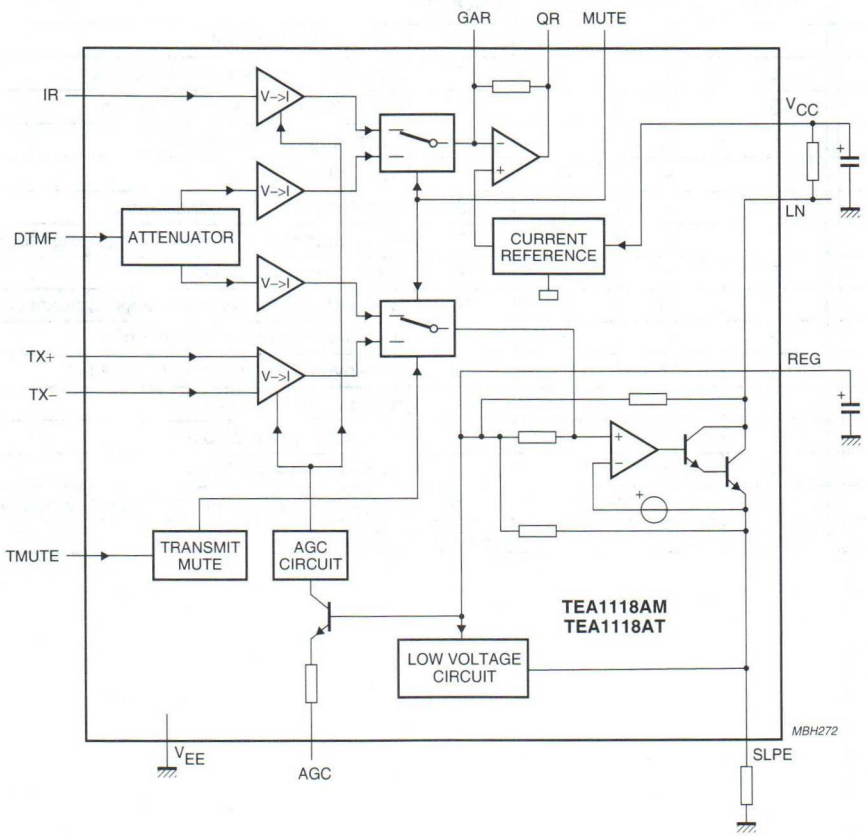


Fig.2 Block diagram (TEA1118A).

PINNING

SYMBOL	TEA1118		TEA1118A		DESCRIPTION
	SO14	SSOP16	SO14	SSOP16	
LN	1	1	1	1	positive line terminal
SLPE	2	2	2	2	slope (DC resistance) adjustment
REG	3	3	3	3	line voltage regulator decoupling
GAT	4	4	–	–	transmit gain adjustment
TMUTE	–	–	4	5	transmit mute input
DTMF	–	–	5	6	dual-tone multi-frequency input
MUTE	–	–	6	8	mute input to select speech or dialling mode
IR	7	9	7	9	receive amplifier input
AGC	8	10	8	10	automatic gain control/line loss compensation
TX–	9	11	9	11	inverting transmit amplifier input
TX+	10	12	10	12	non-inverting transmit amplifier input
V_{EE}	11	13	11	13	negative line terminal
QR	12	14	12	14	receive amplifier output
GAR	13	15	13	15	receive gain adjustment
V_{CC}	14	16	14	16	supply voltage for speech circuit and peripherals
n.c.	5 and 6	5 to 8	–	4 and 7	not connected

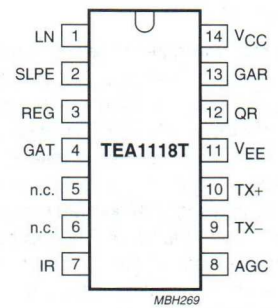


Fig.3 Pin configuration (TEA1118T).

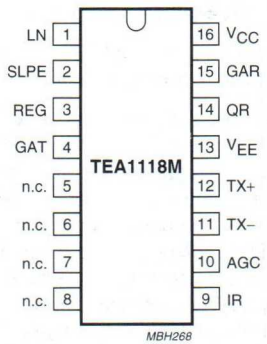


Fig.4 Pin configuration (TEA1118M).

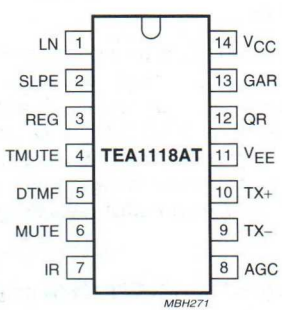


Fig.5 Pin configuration (TEA1118AT).

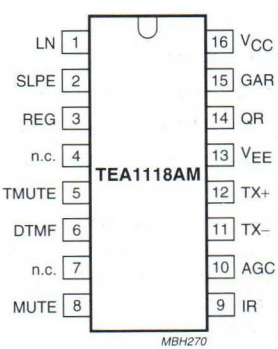


Fig.6 Pin configuration (TEA1118AM).

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supplies (pins LN, SLPE, V_{CC} and REG)

The supply for the TEA1118 and TEA1118A and their peripherals is obtained from the telephone line.

The ICs generate a stabilized reference voltage (V_{ref}) between pins LN and SLPE. This reference voltage is equal to 3.35 V, is temperature compensated and can be adjusted by means of an external resistor (R_{VA}). It can be increased by connecting the R_{VA} resistor between pins REG and SLPE (see Fig.11), or decreased by connecting the R_{VA} resistor between pins REG and LN. The voltage at pin REG is used by the internal regulator to generate the stabilized reference voltage and is decoupled by a capacitor (C_{REG}) which is connected to V_{EE}. This capacitor, converted into an equivalent inductance (see Section "Set impedance"), realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (R_{CC} in the audio-frequency range). The voltage at pin SLPE is proportional to the line current. Figure 7 illustrates the supply configuration.

The ICs regulate the line voltage at pin LN, and it can be calculated as follows:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I_{CC} - I_P - I^* = I_{sh}$$

where:

I_{line}: line current

I_{CC}: current consumption of the IC

I_P: supply current for peripheral circuits

I^*: current consumed between LN and V_{EE}

I_{sh}: the excess line current shunted to SLPE (and V_{EE}) via LN.

The preferred value for R_{SLPE} is 20 Ω. Changing R_{SLPE} will affect more than the DC characteristics; it also influences the transmit gain and the DTMF gain (TEA1118A only), the gain control characteristics, the sidetone level and the maximum output swing on the line.

The internal circuitry of the TEA1118 and TEA1118A is supplied from pin V_{CC}. This voltage supply is derived from the line voltage by means of a resistor (R_{CC}) and must be decoupled by a capacitor C_{VCC}. It may also be used to supply peripheral circuits such as dialling or control circuits. The V_{CC} voltage depends on the current consumed by the IC and the peripheral circuits as shown by the formula (see also Figs 8 and 9). R_{CCint} is the internal equivalent resistance of the voltage supply point, and I_{rec} is the current consumed by the output stage of the earpiece amplifier.

$$V_{CC} = V_{CC0} - R_{CCint} \times (I_P - I_{rec})$$

$$V_{CC0} = V_{LN} - R_{CC} \times I_{CC}$$

The DC line current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistance of the telephone line (R_{line}) and the reference voltage (V_{ref}). With line currents below 7.5 mA, the internal reference voltage (generating V_{ref}) is automatically adjusted to a lower value. This means that more sets can operate in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. At currents below 7.5 mA, the circuit has limited transmit and receive levels. This is called the low voltage area.

Set impedance

In the audio frequency range, the dynamic impedance is mainly determined by the R_{CC} resistor. The equivalent impedance of the circuits is illustrated in Fig.10.

Transmit amplifier (pins TX+, TX− and GAT)

The TEA1118 and TEA1118A have symmetrical transmit inputs. The input impedance between pins TX+ and TX− is equal to 62.5 kΩ; the input impedance between pins TX+/TX− and V_{EE} is equal 36.5 kΩ. The voltage gain from pins TX+/TX− to pin LN is set at 11.3 dB.

Automatic gain control is provided on this amplifier for line loss compensation.

The gain of the TEA1118 can be decreased by connecting an external resistor R_{GAT} between pins GAT and REG. The adjustment range is equal to 6 dB. A capacitor C_{GAT} connected between pins GAT and REG can be used to provide a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAT} \times (R_{GATint} // R_{GAT})$. R_{GATint} is the internal resistor which sets the gain with a typical value of 27 kΩ.

Transmit mute (pin TMUTE; TEA1118A only)

The transmit amplifier can be disabled by activating the transmit mute function. When TMUTE is LOW, the normal speech mode is entered, depending on the level on MUTE. When TMUTE is HIGH, the transmit amplifier inputs are disabled while the DTMF input is enabled (no confidence tone is provided). The voltage gain between LN and TX+/TX− is attenuated; the gain reduction is 80 dB.

Receive amplifier (pins IR, GAR and QR)

The receive amplifier has one input (IR) and one output (QR). The input impedance between pins IR and V_{EE} is 20 kΩ. The voltage gain from pin IR to pin QR is set at 31 dB. The gain can be decreased by connecting an external resistor R_{GAR} between pins GAR and QR; the adjustment range is 12 dB. Two external capacitors C_{GAR} (connected between GAR and QR) and C_{GARS} (connected between GAR and V_{EE}) ensure stability.

The C_{GAR} capacitor provides a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAR} \times (R_{GARint} // R_{GAR})$. R_{GARint} is the internal resistor which sets the gain with a typical value of 100 kΩ. The condition $C_{GARS} = 10 \times C_{GAR}$ must be fulfilled to ensure stability.

Automatic gain control is provided on this amplifier for line loss compensation.

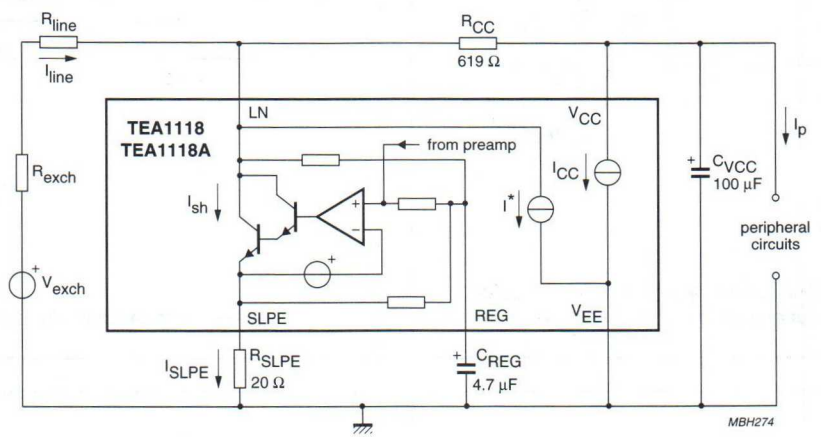
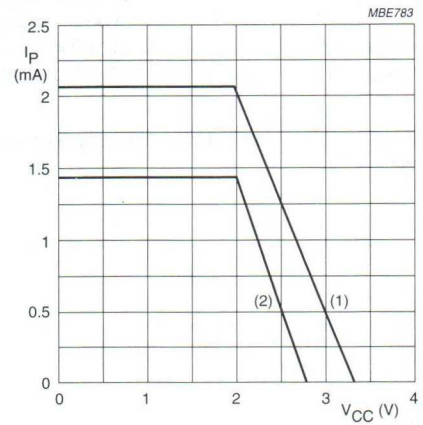


Fig.7 Supply configuration.



(1) With R_{VA} resistor.
(2) Without R_{VA} resistor.

Fig.8 Typical current I_P available from V_{CC} for peripheral circuits at I_{line} = 15 mA.

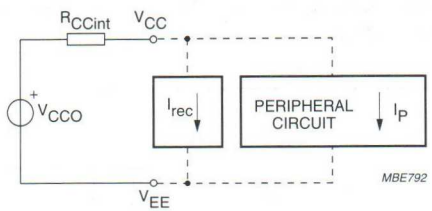
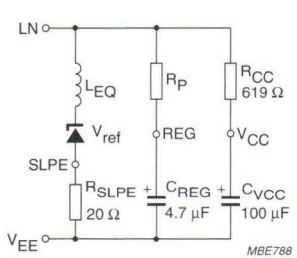
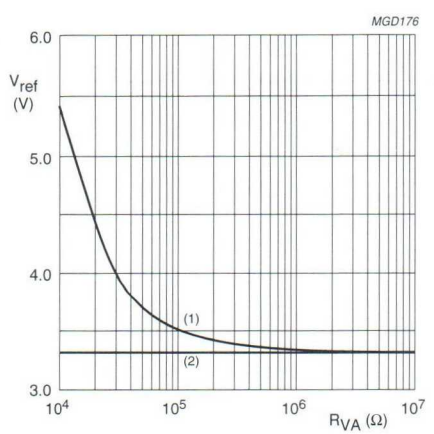


Fig.9 V_{CC} voltage supply for peripheral.



$L_{EQ} = C_{REG} \times R_{SLPE} \times R_P$.
R_P = internal resistance (15.5 kΩ).

Fig.10 Equivalent impedance between LN and V_{EE}.



(1) Influence of R_{VA} on V_{ref}.
(2) V_{ref} without influence of R_{VA}.

Fig.11 Reference voltage adjustment by R_{VA}.

Automatic Gain Control (pin AGC)

The TEA1118 and TEA1118A perform automatic line loss compensation. The automatic gain control varies the gain of the transmit amplifier and the gain of the receive amplifier in accordance with the DC line current.
The control range is 5.8 dB (which corresponds approximately to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km).
The ICs can be used with different configurations of feeding bridge (supply voltage and bridge resistance) by connecting an external resistor R_{AGC} between pins AGC and V_{EE}. This resistor enables the I_{start} and I_{stop} line currents to be increased (the ratio between I_{start} and I_{stop} is not affected by the resistor). The AGC function is disabled when pin AGC is left open-circuit.

DTMF amplifier (pin DTMF; TEA1118A only)

When the DTMF amplifier is enabled, dialling tones may be sent on line. These tones can be heard in the earpiece at a low level (confidence tone).

The TEA1118A has an asymmetrical DTMF input.
The input impedance between DTMF and V_{EE} is 20 kΩ.
The voltage gain from pin DTMF to pin LN is 17.4 dB.

The automatic gain control has no effect on the DTMF amplifier.

Mute function (pin MUTE; TEA1118A only)

The mute function performs the switching action between the speech mode and the dialling mode. When MUTE is LOW or open-circuit, the transmit and receive amplifiers inputs are enabled while the DTMF input is disabled, depending on the TMUTE level. When MUTE is HIGH, the DTMF input is enabled and the transmit and receive amplifiers inputs are disabled.

Sidetone suppression

The TEA1118 and TEA1118A anti-sidetone network comprising $R_{CC}//Z_{line}$, R_{ast1}, R_{ast2}, R_{ast3}, R_{SLPE} and Z_{bal} (see Fig.12) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = R_{CC} \times (R_{ast2} + R_{ast3})$$

$$k = \frac{[R_{ast2} \times (R_{ast3} + R_{SLPE})]}{(R_{ast1} \times R_{SLPE})}$$

$$Z_{bal} = k \times Z_{line}$$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice, Z_{line} varies considerably with the line type and the line length. Therefore, the value chosen for Z_{bal} should be for an average line length which gives satisfactory sidetone suppression with short and long lines.
The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

The anti-sidetone network for the TEA1118 and TEA1118A (as shown in Fig.16) attenuates the receive signal from the line by 32 dB before it enters the receive amplifier.
The attenuation is almost constant over the whole audio frequency range.

A Wheatstone bridge configuration (see Fig.13) may also be used.

More information on the balancing of an anti-sidetone bridge can be obtained in our publication *"Applications Handbook for Wired Telecom Systems, IC03b"*, order number 9397 750 00811.

MUTE and TMUTE levels for different modes (TEA1118A only)

Table 1 Required MUTE and TMUTE levels to enable the different possible modes

MODE	CHANNEL				MUTE	TMUTE
	TRANSMIT	RECEIVE	DTMF	CONFIDENCE TONE		
Speech	on	on	off	off	LOW	LOW
DTMF dialling	off	off	on	on	HIGH	X[1]
Transmit mute	off	on	on	off	LOW	HIGH

Note

1. X = don't care.

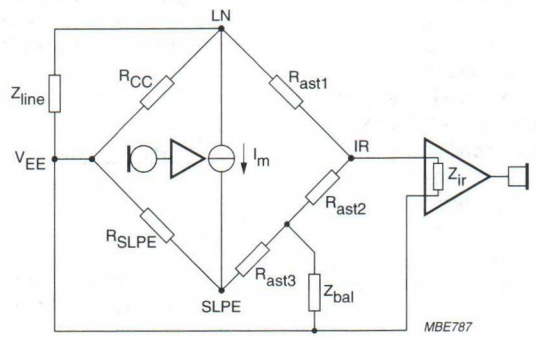


Fig.12 Equivalent circuit of TEA1118 and TEA1118A family anti-sidetone bridge.

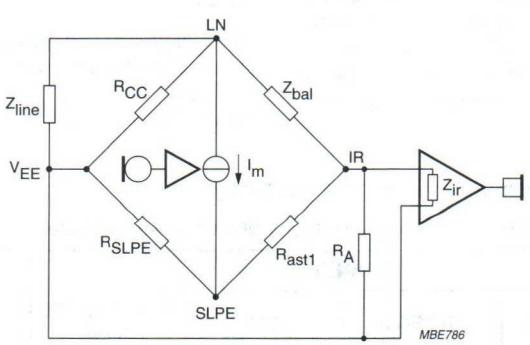


Fig.13 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

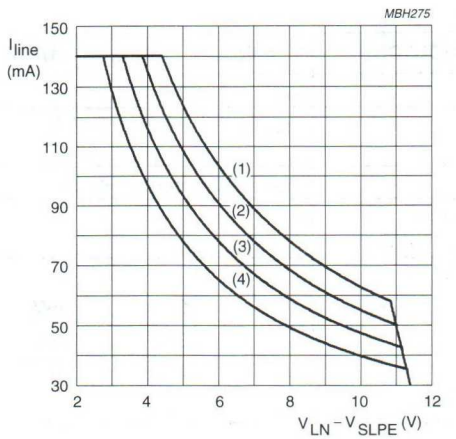
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		V_{EE} – 0.4	12	V
	repetitive line voltage during switch-on or line interruption		V_{EE} – 0.4	13.2	V
$V_{n(max)}$	maximum voltage on all pins		V_{EE} – 0.4	V_{CC} + 0.4	V
I_{line}	line current	R_{SLPE} = 20 Ω; see Figs 14 and 15	–	140	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C; see Figs 14 and 15			
	TEA1118T; TEA1118AT		–	384	mW
	TEA1118M; TEA1118AM		–	312	mW
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

HANDLING

This device meets class 2 ESD test requirements [Human Body Model (HBM)], in accordance with *"MIL STD 883C - method 3015"*.

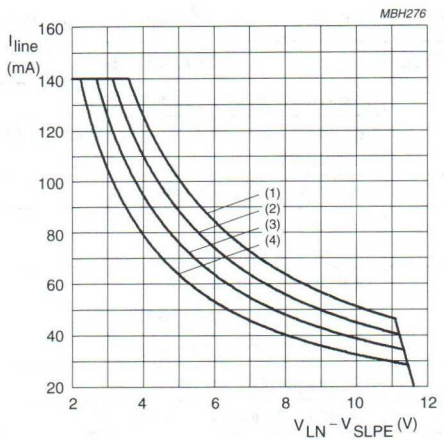
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air			
	TEA1118T; TEA1118AT		130	K/W
	TEA1118M; TEA1118AM	mounted on epoxy board 40.1 × 19.1 × 1.5 mm	160	K/W



(1) T_{amb} = 45 °C; P_{tot} = 615 mW.
(2) T_{amb} = 55 °C; P_{tot} = 538 mW.
(3) T_{amb} = 65 °C; P_{tot} = 461 mW.
(4) T_{amb} = 75 °C; P_{tot} = 384 mW.

Fig.14 SO14 safe operating area.



(1) T_{amb} = 45 °C; P_{tot} = 500 mW.
(2) T_{amb} = 55 °C; P_{tot} = 437 mW.
(3) T_{amb} = 65 °C; P_{tot} = 375 mW.
(4) T_{amb} = 75 °C; P_{tot} = 312 mW.

Fig.15 SSOP16 safe operating area.

CHARACTERISTICS

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; AGC pin connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies (pins V_{LN}, V_{CC}, SLPE and REG)						
V_{ref}	stabilized voltage between LN and SLPE		3.1	3.35	3.6	V
V_{LN}	DC line voltage	I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	2.45	–	V
		I_{line} = 15 mA	3.35	3.65	3.95	V
		I_{line} = 140 mA	–	–	6.9	V
$V_{LN(exR)}$	DC line voltage with an external resistor R_{VA}	$R_{VA(SLPE-REG)}$ = 27 kΩ	–	4.4	–	V
$\Delta V_{LN(T)}$	DC line voltage variation with temperature referenced to 25 °C	T_{amb} = −25 to +75 °C	–	±30	–	mV
I_{CC}	internal current consumption	V_{CC} = 2.9 V	–	1.15	1.4	mA
V_{CC}	supply voltage for peripherals	I_P = 0 mA	–	2.9	–	V
R_{CCint}	equivalent supply voltage resistance	I_P = 0.5 mA	–	550	620	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit amplifier (pins TX+, TX– and GAT)						
$\|Z_i\|$	input impedance					
	differential between pins TX+ and TX–		–	62.5	–	kΩ
	single-ended between pins TX+/TX– and V_{EE}		–	36.5	–	kΩ
G_{vtx}	voltage gain from TX+/TX– to LN	V_{TX} = 200 mV (RMS)	10.1	11.3	12.5	dB
$\Delta G_{vtx(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vtx(T)}$	gain variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
CMRR	common mode rejection ratio		–	60	–	dB
ΔG_{vtxr}	gain voltage reduction range (TEA1118 only)	external resistor connected between GAT and REG	–	–	6	dB
$V_{LN(max)}$	maximum sending signal (RMS value)	I_{line} = 15 mA; THD = 2%	1.4	1.7	–	V
		I_{line} = 4 mA; THD = 10%	–	0.8	–	V
$V_{TX(max)}$	maximum transmit input voltage (RMS value)	I_{line} = 15 mA; THD = 2%	–	0.45	–	V
		I_{line} = 75 mA; THD = 2%	–	0.9	–	V
V_{notx}	noise output voltage at pin LN; pins TX+/TX– shorted through 200 Ω	psophometrically weighted (P53 curve)	–	–84	–	dBmp
Transmit mute (pin TMUTE; TEA1118A only)						
ΔG_{vtxm}	gain reduction	TMUTE = HIGH	–	80	–	dB
V_{IL}	LOW level input voltage		V_{EE} – 0.4	–	V_{EE} + 0.3	V
V_{IH}	HIGH level input voltage		V_{EE} + 1.5	–	V_{CC} + 0.4	V
I_{TMUTE}	input current	input level = HIGH	–	1.25	3	μA
Receive amplifier (pins IR, QR and GAR)						
$\|Z_i\|$	input impedance		–	20	–	kΩ
G_{vrx}	voltage gain from IR to QR	V_{IR} = 4 mV (RMS)	29.8	31	32.2	dB
$\Delta G_{vrx(f)}$	gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vrx(T)}$	gain variation with temperature referenced to 25 °C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
ΔG_{vrxr}	gain voltage reduction range	external resistor connected between GAR and QR	–	–	12	dB
$V_{o(rms)}$	maximum receive signal (RMS value)	I_P = 0 mA sine wave drive; R_L = 150 Ω; THD = 2%	–	0.25	–	V
		I_P = 0 mA sine wave drive; R_L = 450 Ω; THD = 2%	–	0.35	–	V
$V_{norx(rms)}$	noise output voltage at pin QR (RMS value)	IR open-circuit; R_L = 150 Ω; psophometrically weighted (P53 curve)				
	TEA1118		–	–89	–	dBVp
	TEA1118A		–	–86	–	dBVp

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic gain control (pin AGC)						
ΔG_{vtrx}	gain control range for transmit and receive amplifiers with respect to I_{line} = 15 mA	I_{line} = 75 mA;	–	5.8	–	dB
I_{start}	highest line current for maximum gain		–	26	–	mA
I_{stop}	lowest line current for minimum gain		–	61	–	mA
DTMF amplifier (pin DTMF; TEA1118A only)						
$\lvert Z_i \rvert$	input impedance		–	20	–	kΩ
G_{vdtmf}	voltage gain from DTMF to LN	V_{DTMF} = 100 mV (RMS); MUTE or TMUTE = HIGH	16.2	17.4	18.6	dB
$\Delta G_{vdtmf(f)}$	gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vdtmf(T)}$	gain variation with temperature referenced to 25 °C	T_{amb} = −25 to + 75 °C	–	±0.4	–	dB
G_{vct}	voltage gain from DTMF to QR (confidence tone)	V_{DTMF} = 100 mV (RMS); R_L = 150 Ω	–	−18	–	dB
Mute function (pin MUTE; TEA1118A only)						
V_{IL}	LOW level input voltage		V_{EE} − 0.4	–	V_{EE} + 0.3	V
V_{IH}	HIGH level input voltage		V_{EE} + 1.5	–	V_{CC} + 0.4	V
I_{MUTE}	input current	input level = HIGH	–	1.25	3	µA
ΔG_{trxm}	gain reduction for transmit and receive amplifiers	MUTE = HIGH	–	80	–	dB

APPLICATION INFORMATION

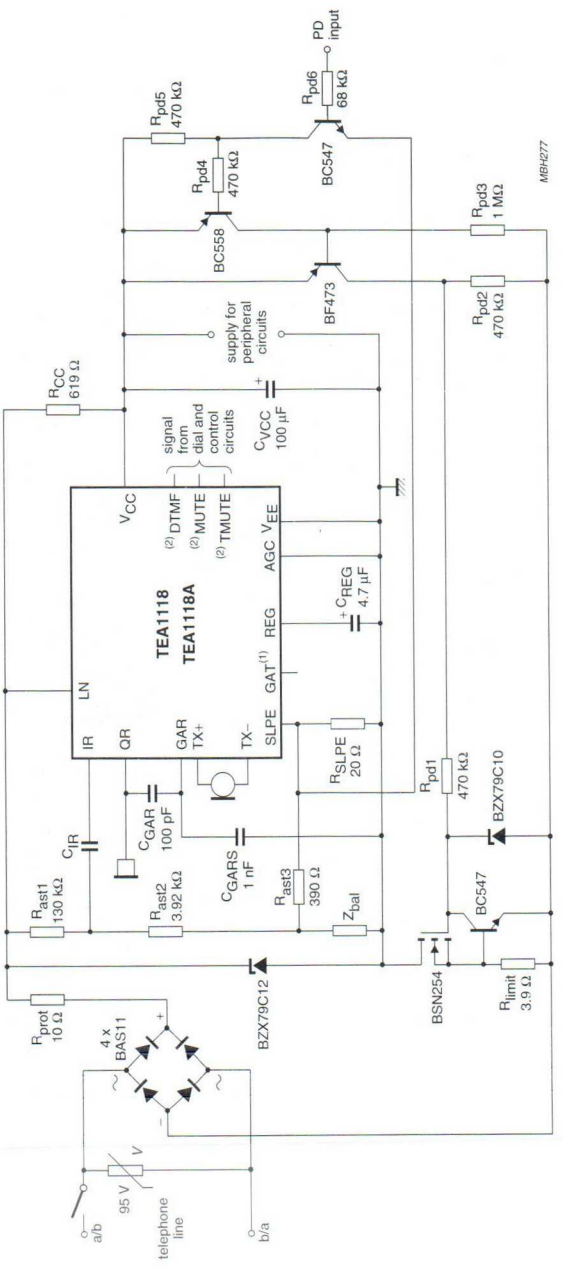


Fig.16 Typical application of the TEA1118 and TEA1118A in sets with pulse dialling or flash facilities.

(1) TEA1118 only.
(2) TEA1118A only.

LISTENING-IN CIRCUITS

Low voltage mono/stereo power amplifier TDA7050

GENERAL DESCRIPTION

The TDA7050 is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0 V	
Total quiescent current (at V_P = 3 V)	I_{tot}	typ.	3,2 mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω			
V_P = 3 V; d_{tot} = 10%	P_o	typ.	140 mW
D.C. output offset voltage between the outputs	$\lvert\Delta V\rvert$	max.	70 mV
Noise output voltage (r.m.s. value)			
at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	140 μV
Stereo application			
Output power at R_L = 32 Ω			
d_{tot} = 10%; V_P = 3 V	P_o	typ.	35 mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ.	75 mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ.	40 dB
Noise output voltage (r.m.s. value)			
at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	100 μV

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97); SOT97-1; 1996 July 23.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig.1		
Storage temperature range	T_{stg}		−55 to + 150 °C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration			
at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

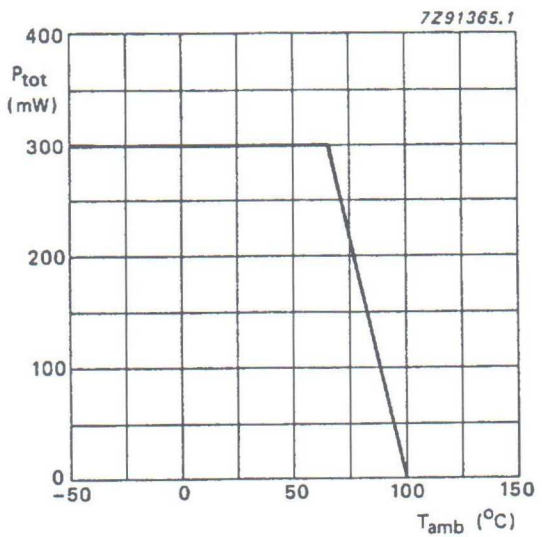


Fig.1 Power derating curve.

THERMAL RESISTANCE

From junction to ambient R_{thj-a} = 110 K/W

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig.4					
Output power; note 1					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig.5					
Output power; note 1					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

Note

1. Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig.2 (BTL application) and Fig.3 (stereo application).

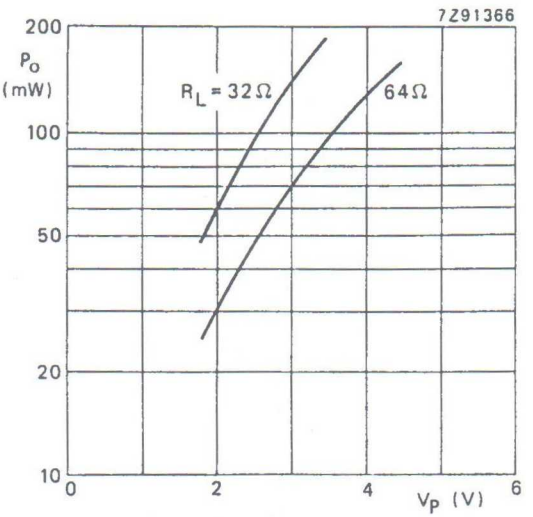


Fig.2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

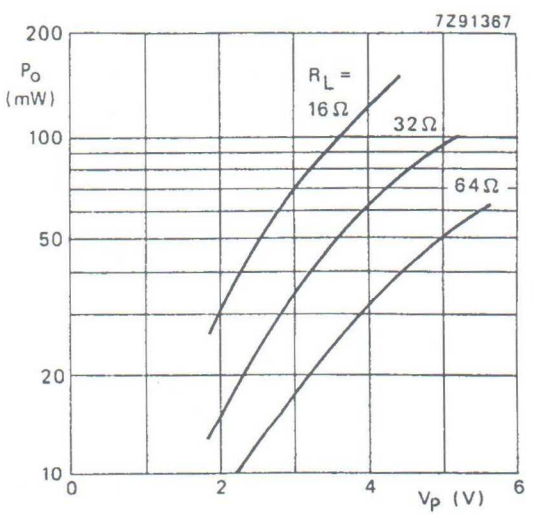


Fig.3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

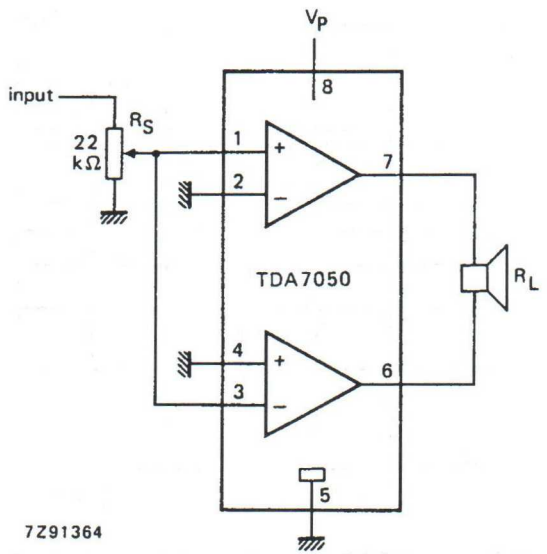


Fig.4 Application diagram (BTL); also used as test circuit.

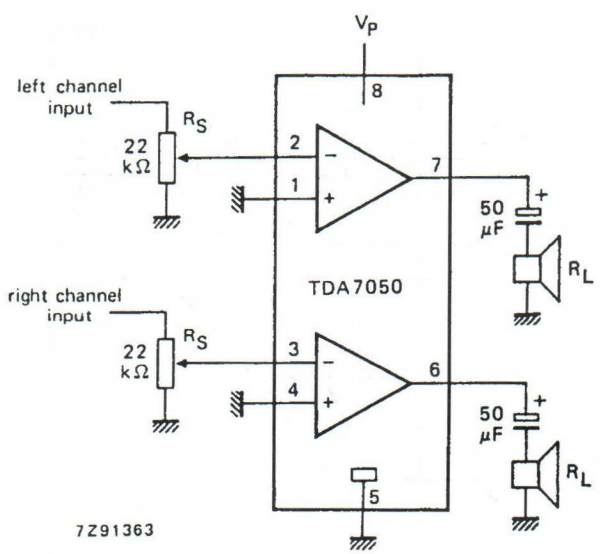


Fig.5 Application diagram (stereo); also used as test circuit.

Low voltage mono/stereo power amplifier TDA7050T

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example).

QUICK REFERENCE DATA

Supply voltage range	V_P		1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ.	3,2	mA
Bridge tied load application (BTL)				
Output power at R_L = 32 Ω				
V_P = 3 V; d_{tot} = 10%	P_o	typ.	140	mW
D.C. output offset voltage between the outputs	$\lvert\Delta V\rvert$	max.	70	mV
Noise output voltage (r.m.s. value)				
at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	140	μV
Stereo application				
Output power at R_L = 32 Ω				
d_{tot} = 10%; V_P = 3 V	P_o	typ.	35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ.	75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ.	40	dB
Noise output voltage (r.m.s. value)				
at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	100	μV

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A); SOT96-1; 1996 July 24.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig.1		
Storage temperature range	T_{stg}		−55 to + 150 °C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration			
at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

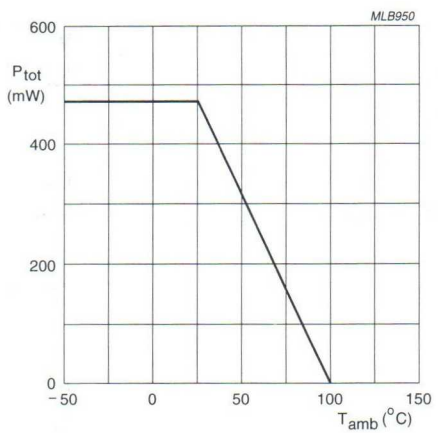


Fig.1 Power derating curve.

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\,max} - T_{amb}}{R_{th\,j\text{-}a}} = \frac{100 - 60}{160} = 0.25\ W$$

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig.4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig.5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig.2 (BTL application) and Fig.3 (stereo application).

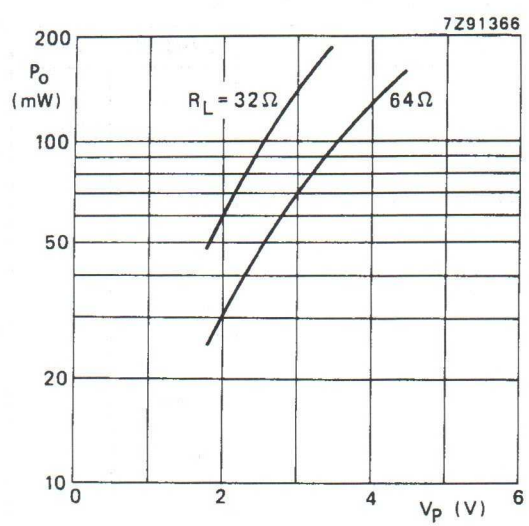


Fig.2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

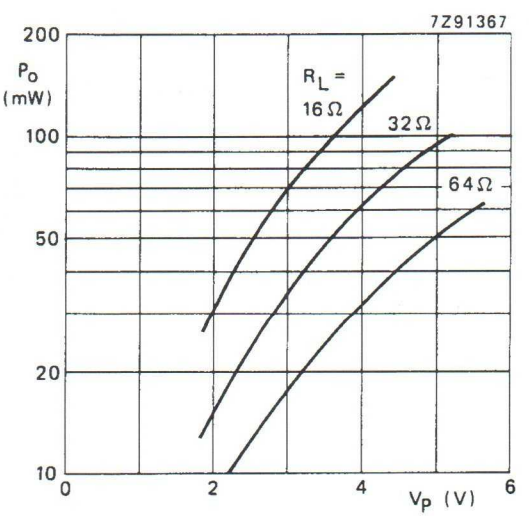


Fig.3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

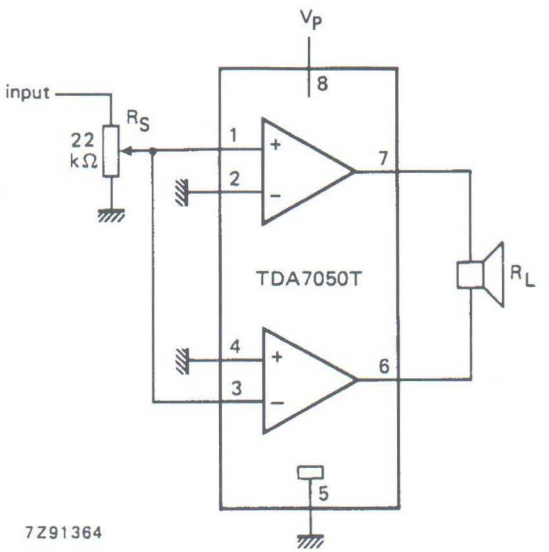


Fig.4 Application diagram (BTL); also used as test circuit.

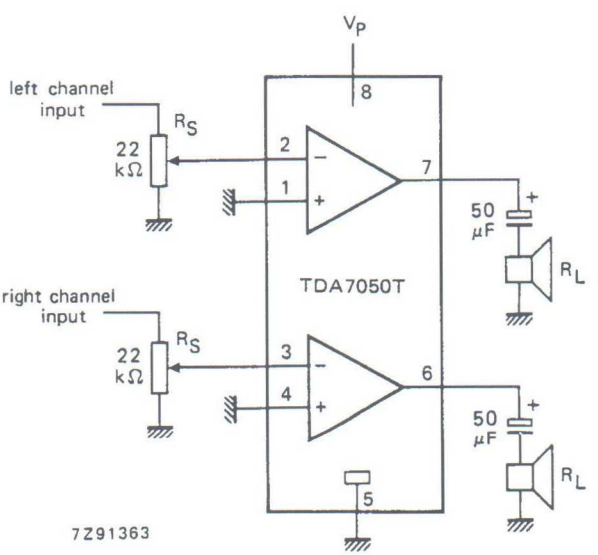


Fig.5 Application diagram (stereo); also used as test circuit.

1 W BTL mono audio amplifier with DC volume control

TDA7052A/AT

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7052A/AT are mono BTL output amplifiers with DC volume control. They are designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
P_O	output power					
	TDA7052A	$R_L = 8\ \Omega$; $V_P = 6$ V	1.0	1.1	–	W
	TDA7052AT	$R_L = 16\ \Omega$; $V_P = 6$ V	0.5	0.55	–	W
G_v	maximum total voltage gain		34.5	35.5	36.5	dB
ϕ	gain control range		75	80	–	dB
I_P	total quiescent current	$V_P = 6$ V; $R_L = \infty$	–	7	12	mA
THD	total harmonic distortion					
	TDA7052A	$P_O = 0.5$ W	–	0.3	1	%
	TDA7052AT	$P_O = 0.25$ W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7052A	8	DIL	plastic	SOT97[1]
TDA7052AT	8	mini-pack	plastic	SOT96A[2]

Notes

1. SOT97-1; 1996 September 10.
2. SOT96-1; 1996 September 10.

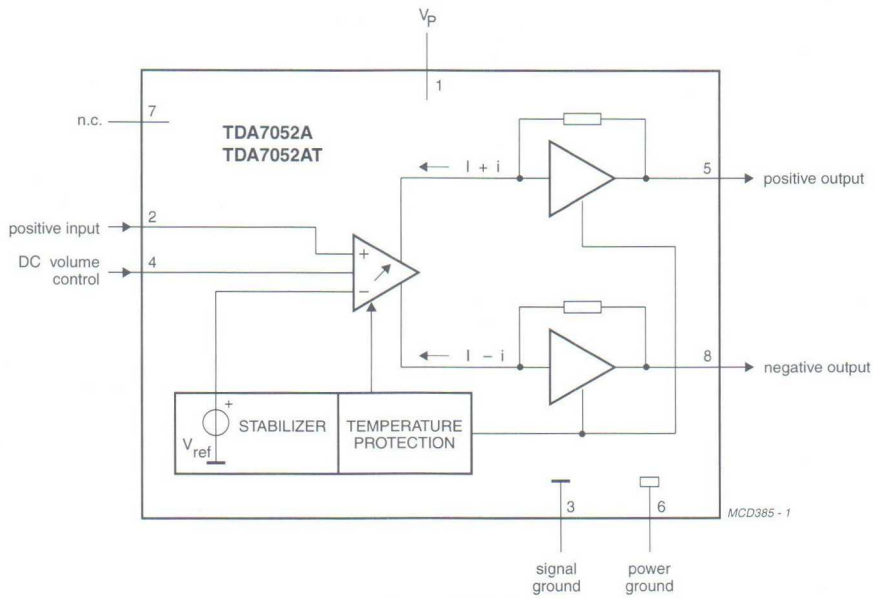


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
IN+	2	positive input
GND1	3	signal ground
VC	4	DC volume control
OUT+	5	positive output
GND2	6	power ground
n.c	7	not connected
OUT−	8	negative output

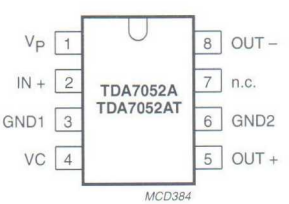


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA7052A/AT are mono BTL output amplifiers with DC volume control, designed for use in TV and monitors but also suitable for battery fed portable recorders and radios.

In conventional DC volume circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.

In the TDA7052A/AT the DC volume control stage is integrated into the input stage so that no coupling capacitors are required and yet a low offset voltage is maintained. At the same time the minimum supply remains low.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Thus a reduced power supply with smaller capacitors can be used which results in cost savings.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 35.5 dB. The DC volume control stage has a logarithmic control characteristic.

The total gain can be controlled from 35.5 dB to −44 dB. If the DC volume control voltage is below 0.3 V, the device switches to the mute mode.

The amplifier is short-circuit proof to ground, V_P and across the load. Also a thermal protection circuit is implemented. If the crystal temperature rises above +150 °C the gain will be reduced, so the output power is reduced.

Special attention is given to switch on and off clicks, low HF radiation and a good overall stability.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage range		–	18	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\%$			
	TDA7052A		–	1.25	W
	TDA7052AT		–	0.8	W
T_{amb}	operating ambient temperature range		−40	+85	°C
T_{stg}	storage temperature range		−55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time		–	1	hr
V_2	input voltage pin 2		–	8	V
V_4	input voltage pin 4		–	8	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	TDA7052A	100 K/W
	TDA7052AT	155 K/W

Notes to the thermal resistance

TDA7052A: $V_P = 6$ V; $R_L = 8\ \Omega$. The maximum sine-wave dissipation is 0.9 W.
Therefore $T_{amb(max)} = 150 - 100 \times 0.9 = 60$ °C.

TDA7052AT: $V_P = 6$ V; $R_L = 16\ \Omega$. The maximum sine-wave dissipation is 0.46 W.
Therefore $T_{amb(max)} = 150 - 155 \times 0.46 = 78$ °C.

CHARACTERISTICS

V_P = 6 V; T_{amb} = 25 °C; f = 1 kHz; TDA7052A: R_L = 8 Ω; TDA7052AT: R_L = 16 Ω; unless otherwise specified (see Fig.6).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
I_P	total quiescent current	V_P = 6 V; R_L = ∞ note 1	–	7	12	mA
Maximum gain; V_4 = 1.4 V						
P_O	output power TDA7052A TDA7052AT	THD = 10%	 1.0 0.5	 1.1 0.55	 – –	 W W
THD	total harmonic distortion TDA7052A TDA7052AT	 P_O = 0.5 W P_O = 0.25 W	 – –	 0.3 0.3	 1 1	 % %
G_v	voltage gain		34.5	35.5	36.5	dB
V_I	input signal handling	V_4 = 0.8 V; THD < 1%	0.5	0.65	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	f = 500 kHz; note 2	–	210	–	μV
B	bandwidth	−1 dB	–	20 Hz to 300 kHz	–	
SVRR	supply voltage ripple rejection	note 3	38	46	–	dB
$\|V_{off}\|$	DC output offset voltage		–	0	150	mV
Z_I	input impedance (pin 2)		15	20	25	kΩ
Minimum gain; V_4 = 0.5 V						
G_v	voltage gain		–	−44	–	dB
$V_{no(rms)}$	noise output voltage (RMS value)	note 4	–	20	30	μV
Mute position						
V_O	output voltage in mute position	$V_4 \leq 0.3$ V; V_I = 600 mV	–	–	30	μV
DC volume control						
ϕ	gain control range		75	80	–	dB
I_4	control current	V_4 = 0.4 V	60	70	80	μA

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage dividend by R_L.
2. The noise output voltage (RMS value) at f = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
3. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV, (RMS value) is applied to the positive supply rail.
4. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

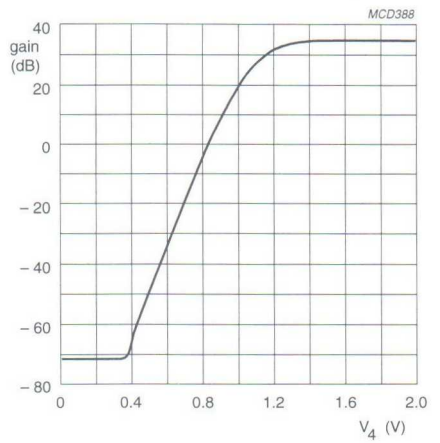


Fig.3 Gain control as a function of DC volume control.

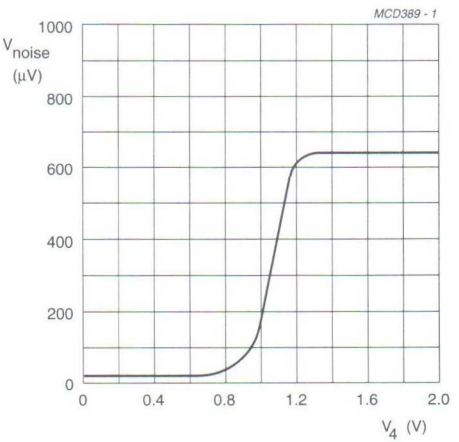


Fig.4 Noise output voltage as a function of DC volume control.

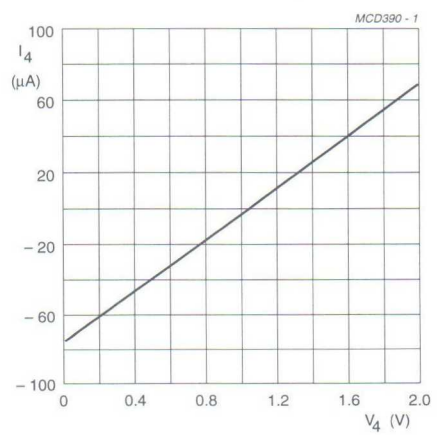
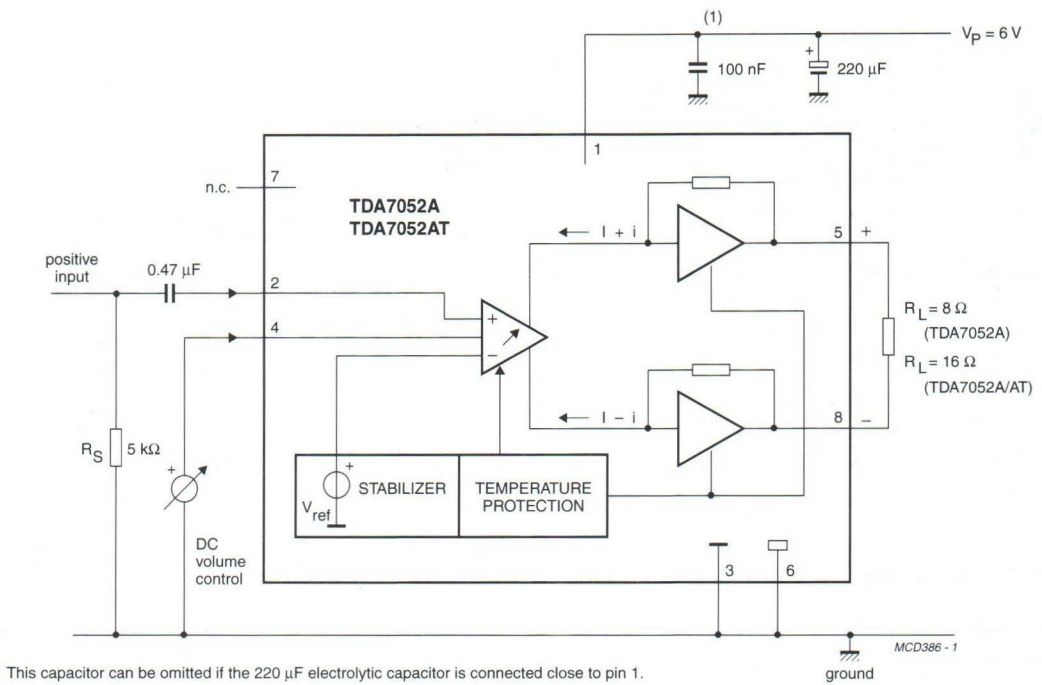


Fig.5 Control current as a function of DC volume control.

APPLICATION INFORMATION



This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 1.

Fig.6 Test and application diagram.

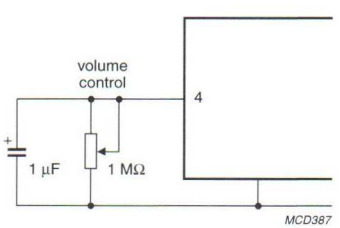


Fig.7 Application with potentiometer as volume control; maximum gain = 30 dB.

Call progress monitor for line powered telephone sets

TEA1083; TEA1083A

FEATURES

- Internal supply
  - Optimum current split-up
  - Low constant current (adjustable) in transmission IC
  - Nearly all line current available for monitoring
  - Stabilized supply voltage
- Loudspeaker amplifier with a fixed gain of 35 dB
- Volume controlled by potentiometer
- Power-down input (TEA1083A only)
- Loudspeaker enable input.

GENERAL DESCRIPTION

The TEA1083/83A is a bipolar IC which has been designed for use in line powered telephone sets. It is intended to offer a monitoring facility of the line signal via a loudspeaker during on-hook dialling. The TEA1083/83A is intended for use in conjunction with a transmission circuit of the TEA1060 family. The device uses a part of the available line current via the internal supply circuit.

The loudspeaker amplifier, which consists of a preamplifier and a power amplifier, amplifies the received line signals from the transmission circuit when enabled via the LSE input. The loudspeaker amplifier can also be used to amplify dialling tones from the dialler IC. The power amplifier contains a push-pull output stage to drive the loudspeaker in a Single Ended Load (SEL) configuration.

The internal voltage stabilizer can be used to supply external devices. By activating the power-down (PD) input of the TEA1083A, the current consumption of the circuit will be reduced, this enables pulse dialling or flash (register recall).

An internal start circuit ensures normal start-up of the transmission IC.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{SUP}	input current range		3.0	–	120	mA
V_{BB}	stabilized supply current		–	2.95	–	V
I_{SUP}	current consumption	PD = HIGH; TEA1083A only	–	50	–	µA
G_v	voltage gain of loudspeaker amplifier		–	35	–	dB
I_{SUP}	minimum input current	P_O = 10 mW (typ) into 50 Ω	–	10	–	mA
T_{amb}	operating ambient temperature range		–25	–	+75	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1083	8	DIL	PLASTIC	SOT97D[1]
TEA1083A	16	DIL	PLASTIC	SOT38[2]
TEA1083AT	16	SOL	PLASTIC	SOT162AG[3]

Notes

1. SOT97-1; 1998 Jun 18.
2. SOT38-1; 1998 Jun 18.
3. SOT162-1; 1998 Jun 18.

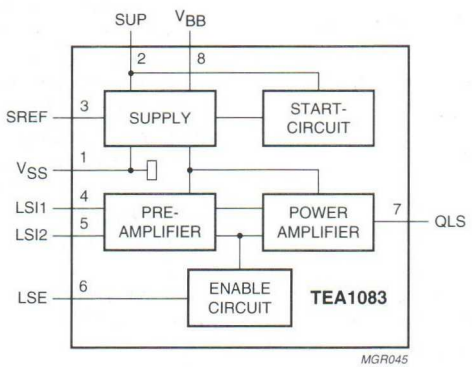


Fig.1 Block diagram (TEA1083).

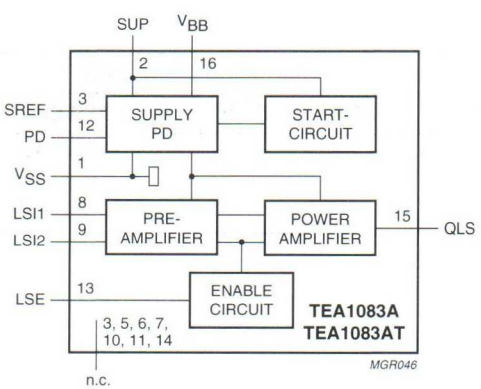


Fig.2 Block diagram (TEA1083A/AT).

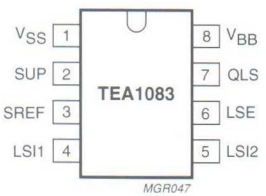


Fig.3 Pin configuration (TEA1083).

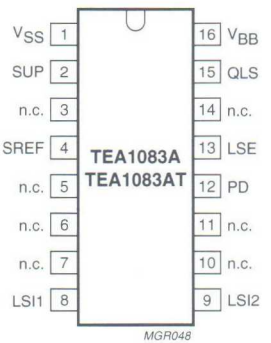


Fig.4 Pin configuration (TEA1083A/AT).

PINNING

SYMBOL	PIN DIL16	PIN DIL8	DESCRIPTION
V_{SS}	1	1	negative supply terminal
SUP	2	2	positive supply terminal
n.c.	3	–	not connected
SREF	4	3	supply reference input
n.c.	5	–	not connected
n.c.	6	–	not connected
n.c.	7	–	not connected
LSI1	8	4	loudspeaker amplifier input 1
LSI2	9	5	loudspeaker amplifier input 2
n.c.	10	–	not connected
n.c.	11	–	not connected
PD	12	–	power-down input
LSE	13	6	loudspeaker enable input
n.c.	14	–	not connected
QLS	15	7	loudspeaker amplifier output
V_{BB}	16	8	stabilized supply voltage

Table 1 Comparison of the TEA108X family.

PRODUCT	CONDITIONS	TEA1083	TEA1083A	TEA1085/85A
Application area	note 1	call progress monitoring		listening-in
PD facility		–	X	X
MUTE or LSE facility	note 2	X	X	X
Dynamic limiter		–	–	X
Howling limiter		–	–	X
V_{BB} setting		–	–	X
SEL	note 3	X	X	X
BTL	note 3	–	–	X
Number of pins	note 4	8	16	24

Notes

1. A call progress monitor is recommended by the European Telecommunications Standards Institute (ETSI) for telephone sets with automatic on-hook dialling facilities so that audible, or visual, progress of a call attempt can be monitored. In accordance with the ETSI (at a frequency of 440 Hz and a line level of 20 dBm (600 Ω)), a minimum level of 50 dBA shall be guaranteed at a distance of 50 cm from the set. This corresponds to a minimum level of approximately 100 mV (RMS) ($P_O \geq 0.2$ mW) across a loudspeaker; Philips type AD2071/Z50.

   A listening-in set has to offer the user more facilities e.g. howling limiting to reduce annoying loudspeaker and line signals. Dynamic limiting of the loudspeaker signal, with respect to supply conditions, can also be required. Acoustic output levels for listening-in sets are approximately 70 to 75 dBA. This corresponds to a loudspeaker level of approximately 1 mV (RMS) ($P_O \approx 20$ mW).
2. The MUTE function of the TEA1085A has a logic input; the MUTE function of the TEA1085 has a toggle input.
3. SEL: loudspeaker connected in a single-ended-load configuration
   BTL: loudspeaker connected in a bridge-tied-load configuration
4. Consult the product specification for the package outline/s.

FUNCTIONAL DESCRIPTION

The TEA1083/83A is normally used in conjunction with a transmission circuit of the TEA1060 family. The circuit must be connected between the positive line terminal (pin 2) and pin SLPE of the transmission IC. The transmission characteristics (impedance, gain settings, etc.) are not affected.
An interconnection between the TEA1083/83A and a member of the TEA1060 family is illustrated in Fig.5.

Supplies SUP, SREF, V_{BB} and V_{SS}

In Fig.6 the line current is divided into I_{TR} for the transmission IC and I_{SUP} for the monitoring circuit TEA1083/83A.

I_{TR} is constant:

$$I_{TR} = V_{int} / R20$$

$$I_{SUP} = I_{line} - I_{CC} - I_{TR}$$

Where:

- V_{int} is an internal temperature compensated reference voltage of 500 mV (typ) between pins SUP and SREF
- R20 is a resistor connected between SUP and SREF
- I_{CC} is the internal current consumption of the TEA106X (approximately 1 mA).

A practical value for resistor R20 is 150 Ω; this produces a current of approximately 3.3 mA (typ) for I_{TR} and I_{SUP} is approximately equal to $I_{line} - 4.3$ mA.

The circuit stabilizes its own supply voltage at V_{BB}. Transistor TR1 provides the supplies for the internal circuits. Transistor TR2 is used to minimize signal distortion on the line by momentarily diverting the input current to V_{SS} whenever the instantaneous value of the voltage at V_{SUP} drops below the supply voltage V_{BB}. V_{BB} is fixed to a typical value of 2.95 V.
The supply at V_{BB} is decoupled with respect to V_{SS} by a 220 μF capacitor (C20).

The DC voltage ($V_{SUP} - V_{SS}$) is determined by the transmission IC and V_{int}; thus
$V_{SUP} - V_{SS} = V_{LN-SLPE} + V_{int}$.
The reference voltage of the transmission IC has to be adjusted to a level where $V_{SUP} - V_{BB\,(max)}$ is greater than 400 mV. The minimum voltage space between SUP and V_{BB} (400 mV) is required to maintain a 'high' efficiency of the internal supply for mean speech levels. $V_{BB\,(max)}$ is the specified maximum level.

The internal current consumption of the TEA1083/83A (I_{SUP0}) is typically 2.5 mA (where $V_{SUP} - V_{SS} = 3.6$ V). The current I_{SUP0} consists of currents I_{BIAS} (approximately 0.4 mA) for the circuitry connected to SUP and I_{BB0} (approximately 2.1 mA) for the internal circuitry connected to V_{BB} (see Fig.6).

LOUDSPEAKER AMPLIFIER (LSI1/LSI2 and QLS)

The TEA1083/83A has symmetrical inputs at LSI1 and LSI2. The input signal is normally taken from the earpiece output of the transmission circuit (see Fig.5) and/or from the signal output of the DTMF generator via a resistive attenuator.
The attenuation factor must be chosen in accordance with the output levels from the transmission IC and/or DTMF generator and, in accordance with the required output power and permitted signal distortion from the loudspeaker signal.

The output QLS drives the loudspeaker as a single-ended load. The output stage has been optimized for use with a 50 Ω loudspeaker (e.g. Philips type AD2071). The loudspeaker amplifier is enabled when the LSE input goes HIGH. The gain of the amplifier is fixed at 35 dB.

Volume control of the loudspeaker signal can be obtained by using a level control at the input (see Fig.5).

The maximum voltage swing at the QLS output is $V_{O(p-p)} = 2.5$ V (typical with 50 Ω load). The input level V_{LSI} is approximately 16 mV(rms) and the supply current $I_{SUP} > 11$ mA. In this condition the signal is limited by the available voltage space (V_{BB}). Higher input levels and/or lower supply currents will result in an increase of the harmonic distortion due to signal clipping.

With a limit of 2.5 V (p-p), the maximum output swing is dependent on the supply current and loudspeaker impedance. It can be approximated, for low distortions, by the following equation:

$$V_{O(p-p)} = 2 \times (I_{SUP} - I_{SUPO}) \times \pi \times R_{LS}$$

Where;

- $V_{O(p-p)}$ = the peak-to-peak level of the loudspeaker
- R_{LS} = the loudspeaker impedance
- I_{SUPO} = 2.5 mA (typ.)

POWER-DOWN INPUT (PD)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, thereby breaking the supply current to the transmission IC. The capacitor connected to V_{BB} provides the supply for the TEA1083/83A during the supply breaks.

By making the PD input HIGH during the loop break, the requirement on the capacitor is eased and, consequently, the internal current consumption I_{BB0} (see Fig.5) is reduced from 2.1 mA to 400 μA typically. Transistors TR1 and TR2 are inhibited during power-down and the bias current is reduced from approximately 400 μA to approximately 50 μA with $V_{SUP} = 3.6$ V in the following equation:

$$I_{SUP(PD)} = I_{BIAS(PD)} = (V_{SUP} - 2V_d)/Ra$$

Where $3.6 < V_{SUP} < V_{BB} + 3$ V

$2V_d$ is the voltage drop across 2 internal diodes (approximately 1.3 V)

Ra is an internal resistor (typical 50 kΩ)

LOUDSPEAKER ENABLE INPUT (LSE)

The LSE input has a pull-down structure. It switches the loudspeaker amplifier, in the monitoring condition, by applying a HIGH level at the input. The amplifier is in the standby condition when LSE is LOW (input open-circuit or connected to V_{SS}).

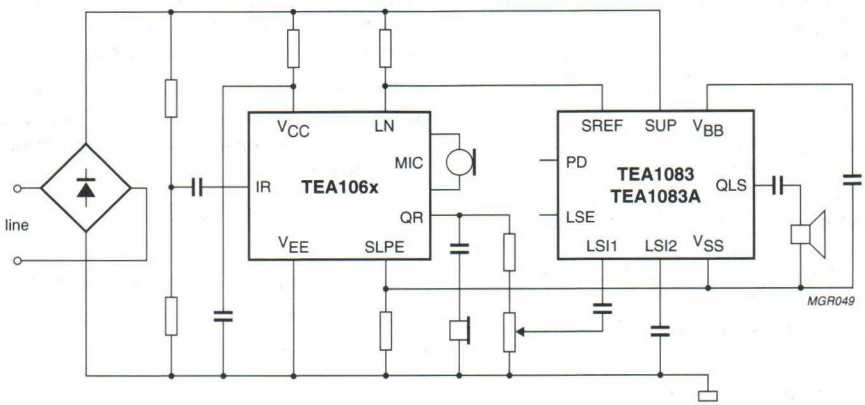


Fig.5 Interconnection with a transmission IC of the TEA106X family.

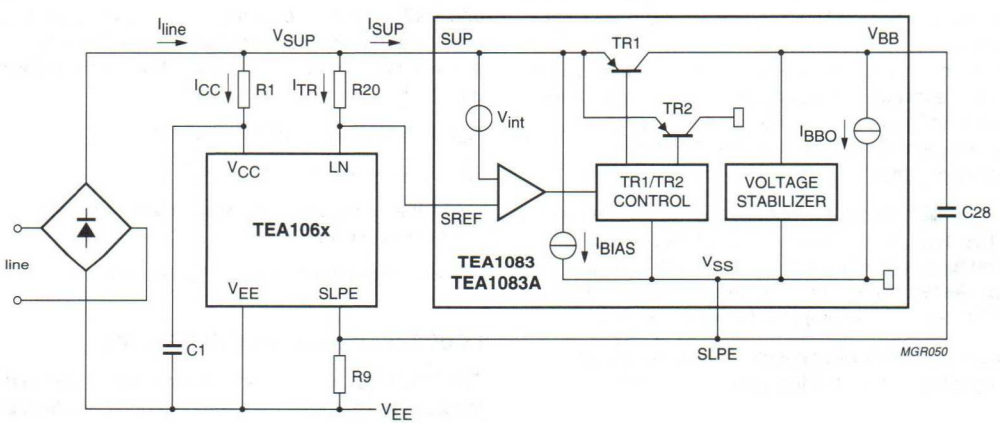


Fig.6 Supply arrangement.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{SUP}	Supply voltage				
	continuous		–	12	V
	during switch-on or line interruption		–	13.2	V
V_{SUP}	Repetitive supply voltage from 1 ms to 5 s with 12 Ω current limiting resistor in series with supply		–	28	V
V_{SREF}	Supply reference voltage		V_{SS} – 0.5	V_{SUP} + 0.5	V
V	Voltage on all other pins		V_{SS} – 0.5	V_{BB} + 0.5	V
I_{SUP}	Supply current	see Fig.6	–	120	mA
P_{tot}	Total power dissipation	T_{amb} = 75 °C; T_j = 125 °C			
	TEA1083		–	500	mW
	TEA1083A		–	769	mW
	TEA1083AT		–	555	mW
T_{stg}	Storage temperature range		–40	+125	°C
T_{amb}	Operating ambient temperature range		–25	+75	°C
T_j	Junction temperature		–	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air (TEA1083)	100 K/W
	from junction to ambient in free air (TEA1083A)	65 K/W
	from junction to ambient in free air (TEA1083AT)	90 K/W

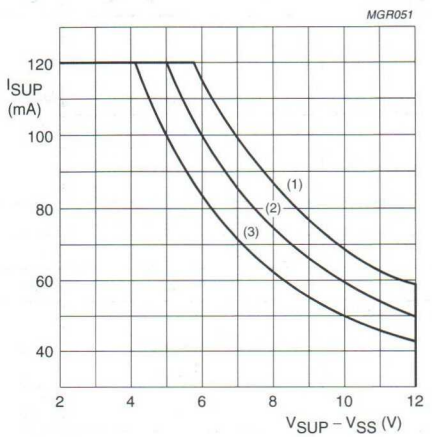


Fig.7 Safe operating area; see Table 2 (TEA1083).

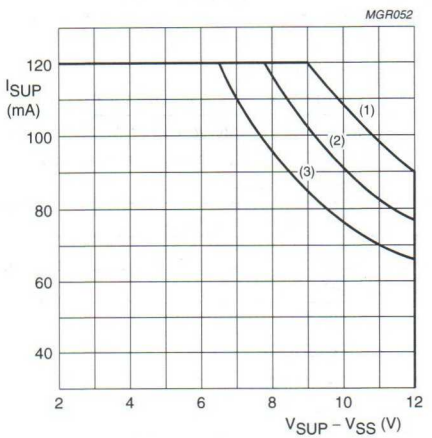


Fig.8 Safe operating areas see Table 3 (TEA1083A).

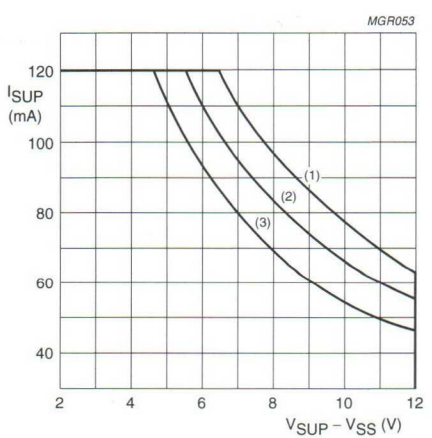


Fig.9 Safe operating area; see Table 4 (TEA1083AT).

Table 2

CURVE	T_{amb}	P_{tot}
1	55 °C	700 mW
2	65 °C	600 mW
3	75 °C	500 mW

Table 3

CURVE	T_{amb}	P_{tot}
1	55 °C	1077 mW
2	65 °C	923 mW
3	75 °C	769 mW

Table 4

CURVE	T_{amb}	P_{tot}
1	55 °C	777 mW
2	65 °C	666 mW
3	75 °C	555 mW

CHARACTERISTICS

V_{SUP} = 3.6 V; V_{SS} = 0 V; I_{SUP} = 15 mA; V_{SUP} = 0 V (RMS); f = 800 Hz; T_{amb} = 25 °C; PD = LOW; LSE = HIGH; loudspeaker amplifier load = 50 Ω; all measurements taken in test circuit Fig.10; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{SUP}	Minimum DC input voltage		–	V_{BB} + 0.6	–	V
$V_{SUP-SREF}$	Internal reference voltage		400	500	600	mV
V_{BB}	Stabilized supply voltage	I_{SUP} = 15 mA	2.75	2.95	3.15	V
ΔV_{BB}	Variation of supply voltage	from I_{SUP} = 15 to 120 mA	–	15	–	mV
$\Delta V_{BB}/\Delta T$	Variation of supply voltage with temperature, referred to 25 °C	T_{amb} = –25 to +75 °C; I_{sup} = 15 mA	–	±0.2	–	mV/K
I_{SUP}	Minimum operating current		–	2.5	4.0	mA
THD	Distortion of AC signal between SUP and V_{EE}	$V_{SUP(RMS)}$ = 1 V	–	0.3	–	%
$V_{no(RMS)}$	Noise between SUP and V_{EE} (RMS value)	psophometrically weighted (P53 curve)	–	–71	–	dBmp
	Current consumption in power-down condition	PD = HIGH				
I_{SUP}	V_{SUP} = 3.6 V		–	50	75	µA
I_{BB}	V_{BB} = 2.95 V		–	400	550	µA
Loudspeaker amplifier inputs LSI1 and LSI2						
Z_i	input impedance (LSI1 and LSI2)	single ended	7.5	9.5	11.5	kΩ
		differential (LSI1 to LSI2)	15	19	23	kΩ
G_v	Voltage gain from LSI1/2 to QLS	I_{SUP} = 15 mA; V_i = 2 mV (RMS)	34	35	36	dB
ΔG_v	Total gain variation with input signal from 2 mV(RMS) to 10 mV(RMS)		–	0.2	–	dB
$\Delta G/\Delta T$	Total gain variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±0.4	–	dB
Output capabilities						
$V_{O(p-p)}$	Maximum output voltage (peak-to-peak value)	THD = 3%; 50 Ω load	2.0	2.5	–	V
$V_{O(p-p)}$	Output voltage (peak-to-peak value)	V_i = 10 mV(RMS); I_{SUP} = 15 mA; V_{SUP}–V_{EE} = 1 V (RMS)	–	1.6	–	V
$V_{no(RMS)}$	Noise output voltage (RMS value)	1 kΩ between inputs LSI1 and LSI2; psophometrically weighted (P53 curve)	–	250	–	µV
Power-down input (PD) (TEA1083A only)						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}	V
I_{PD}	Input current	PD = HIGH	–	2.3	2.8	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LSE input						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}	V
I_I	Input current	LSE = HIGH	–	5	10	μA
ΔG	Reduction of gain from LSI1/LSI2 to QLS	LSE = LOW	60	80	–	dB

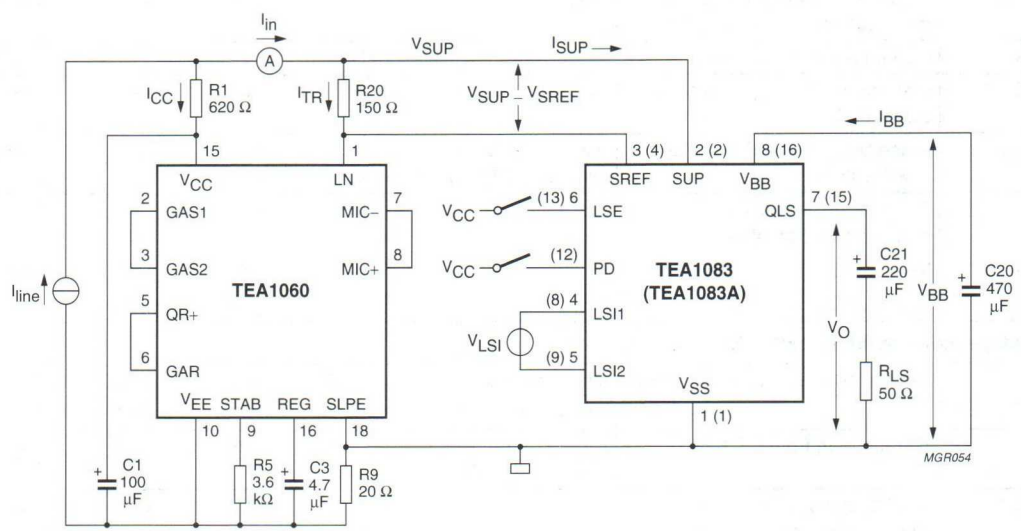


Fig.10 Test circuit.

Notes to figure 10

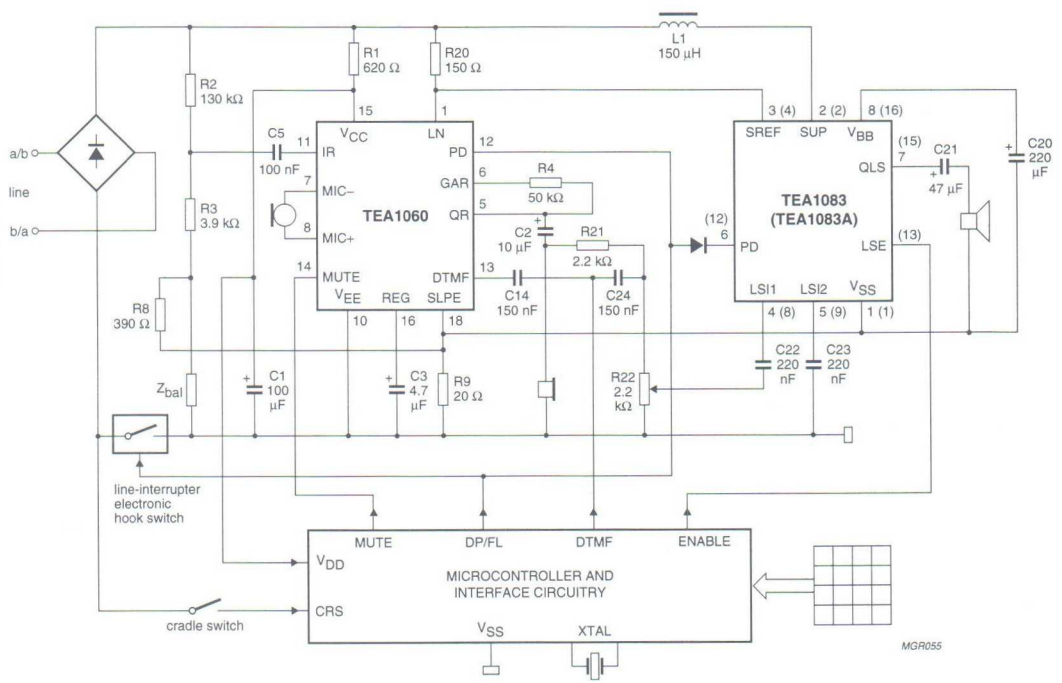
1. $I_{SUP} = I_{IN} - I_{TR}$
2. $G_v = 20 \log \left| \frac{V_o}{V_{LSI}} \right|$
3. $I_{TR} = \frac{V_{SUP-SREF}}{R20}$
4. The pin numbers in parenthesis refer to the TEA1083A/AT
5. LSE has to be HIGH to measure the voltage gain
6. PD has to be HIGH to measure in PD conditions
7. The pins not shown in the TEA1060 are left open-circuit
8. An impedance in series with pin SUP (e.g. an ammeter) should be avoided as it interferes with the values of I_{TR} and I_{SUP}.

APPLICATION INFORMATION

An application of the TEA1083/83A, in conjunction with a member of the TEA1060 family, is illustrated in figure 11. The TEA1083/83A is used for call progress monitoring during on-hook dialling. The dialling facilities are performed by a microcontroller (e.g. PCD3344, PCD3349).

Only the most important components have been shown. For detailed information refer to a data sheet of the TEA1060 family.

The electronic hook switch can be replaced by a mechanical system (hook switch) with a hold/release function which is intended for on-hook dialling.



Pin numbers in parenthesis refer to the TEA1083A/AT.

Fig.11 Application example when the TEA1083/83A is used in conjunction with the TEA1060.

Listening-in circuit for line-powered telephone sets

TEA1085; TEA1085A

FEATURES

- Internal supply

  optimum current split-up
  - low constant current (adjustable) in transmission IC
  - nearly all line current available for listening-in

  adjustable supply voltage
- Loudspeaker amplifier

  dynamic limiter providing low distortion and the highest possible output power
  SE or BTL drive for loudspeaker volume control by potentiometer and/or logic inputs (e.g. microcontroller drive)
  fixed gain of 35 dB
- Larsen level limiter

  low sensitivity for own speech due to 3rd-order filter and attack delay
  adjustable voltage thresholds
- Power down input
- MUTE input

  TEA1085/TEA1085A
  - clickfree switching between listening-in mode and standby mode

  TEA1085
  - toggle function
  - start-up in standby condition

  TEA1085A
  - logic level input

GENERAL DESCRIPTION

The TEA1085 and TEA1085A are bipolar ICs which have been designed for use in line-powered telephone sets and provide a listening-in facility for the received line signal via a loudspeaker. Nearly all the line current can be used for powering the loudspeaker.
The circuits incorporate a supply circuit, loudspeaker amplifier dynamic limiter, MUTE circuit, power-down facility and logic inputs for gain setting. The devices also incorporate a Larsen Level Limiter to reduce howling effects.
The ICs are intended for use in conjunction with a transmission circuit of the TEA1060 family.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1085/TEA1085A	24	DIL	plastic	SOT101B[1]
TEA1085T/TEA1085AT	24	SO24	plastic	SOT137A[2]

Notes

1. SOT101-1; 1998 Jun 18.
2. SOT137-1; 1998 Jun 18.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{SUP}	input current range		4	–	120	mA
V_{BB}	stabilized supply voltage		–	3.6	–	V
I_{SUP}	current consumption	PD = HIGH	–	55	–	µA
G_v	voltage gain loudspeaker amplifier					
		SE	–	35	–	dB
		BTL	–	41	–	dB
ΔG_v	maximum gain reduction with logic inputs (3 steps)		–	18	–	dB
I_{SUP}	minimum input current					
		P_{OUT} = 20 mW typ. into 50 Ω SE	–	15	17	mA
		P_{OUT} = 40 mW typ. into 50 Ω BTL	–	–	32	mA
$t_{ad(RMS)}$	Larsen limiter attack delay time V_{DTI} jumps from 0 to ≥ 100 mV (RMS value)		100	–	200	ms
$V_{DTI(RMS)}$	Larsen limiter threshold level	Larsen mode	–	7	–	mV
G_v	Larsen limiter preamplifier gain setting range		30	–	52	dB
T_{amb}	operating ambient temperature range		–25	–	+75	°C

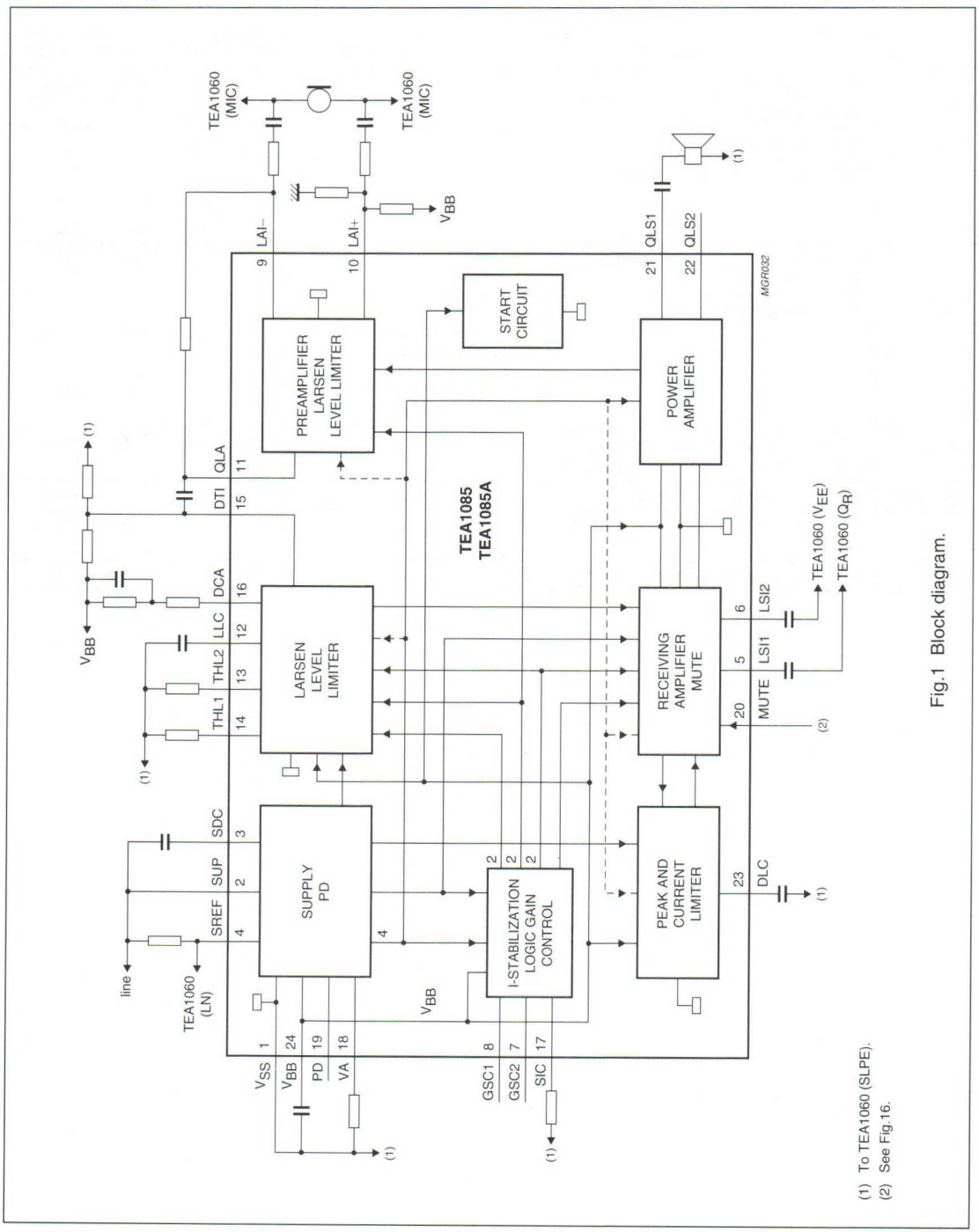


Fig.1 Block diagram.

(1) To TEA1060 (SLPE).
(2) See Fig.16.

PIN CONFIGURATION

SYMBOL	PIN	DESCRIPTION
V_{SS}	1	negative supply
SUP	2	positive supply
SDC	3	supply amplifier decoupling
SREF	4	supply reference input
LSI1	5	loudspeaker amplifier input 1
LSI2	6	loudspeaker amplifier input 2
GSC2	7	logic input 2 for gain select
GSC1	8	logic input 1 for gain select
LAI−	9	Larsen limiter preamplifier inverting input
LAI+	10	Larsen limiter preamplifier non-inverting input
QLA	11	Larsen limiter preamplifier output
LLC	12	Larsen limiter capacitor
THL2	13	Larsen limiter residual threshold level
THL1	14	Larsen limiter attack delay threshold level
DTI	15	Larsen limiter detector input
DCA	16	Larsen limiter detector current adjustment
SIC	17	Larsen limiter current stabilizer
VA	18	V_{BB} voltage adjustment
PD	19	power-down input
MUTE	20	MUTE input
QLS1	21	loudspeaker amplifier output 1
QLS2	22	loudspeaker amplifier output 2
DLC	23	dynamic limiter capacitor
V_{BB}	24	stabilized supply decoupling

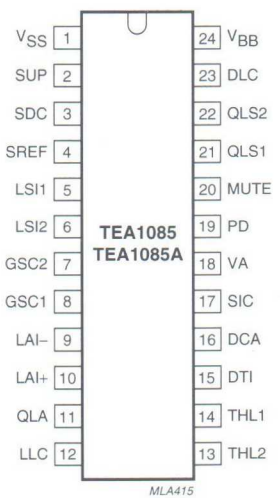


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Figure 1 illustrates a block diagram of the TEA1085/TEA1085A with external components and connections to the transmission IC.

The TEA1085/TEA1085A are bipolar ICs which have been designed for use in line-powered telephone sets and provide a listening-in facility for the received line signal via a loudspeaker. Nearly all the line current can be used for powering the loudspeaker.

The loudspeaker amplifier consists of a preamplifier, to amplify the earpiece signal from the transmission circuit and, a double push-pull output stage to drive the loudspeaker in the BTL (bridge tied load) or SE (single ended) configuration. The gain of the preamplifier is controlled by a dynamic limiter which prevents high distortion of the loudspeaker signal. This is achieved by preventing clipping of the loudspeaker signal, with respect to the supply voltage, and at too low supply current. Two logic inputs can be used to reduce the gain in 3 steps.

Because of acoustic feedback from the loudspeaker to the microphone, howling signals (Larsen effect) can occur on the telephone line and in the loudspeaker. When the Larsen signal exceeds a voltage and time duration threshold the Larsen level limiter (LLL) will reduce the Larsen signal to a low level within a short period of time by reducing the gain of the receiving preamplifier. This is achieved by using the microphone signal as an input signal which is processed in the LLL via a preamplifier and 3rd-order filter.

The MUTE input can be used to enable or disable the loudspeaker amplifier.

The MUTE function of the TEA1085 has a toggle input to permit the use of a simple push-button switch.

The MUTE function of the TEA1085A has a logic input to operate with a microcontroller.

By activating the power-down input the current consumption of the circuit will be reduced, this enables pulse dialling or flash (register recall).

An internal start circuit ensures normal start-up of the transmission IC and start-up of the listening-in IC in the standby mode.

The TEA1085/TEA1085A are intended for use in conjunction with a member of the TEA1060 family and should be connected between LINE and SLPE of the transmission IC. The transmission characteristics (impedance, gain settings, for example) are not affected. The interconnection between the two ICs is illustrated in Fig.3.

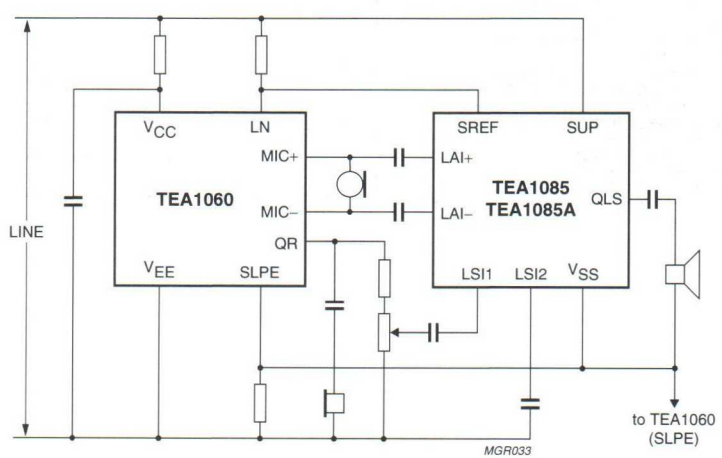
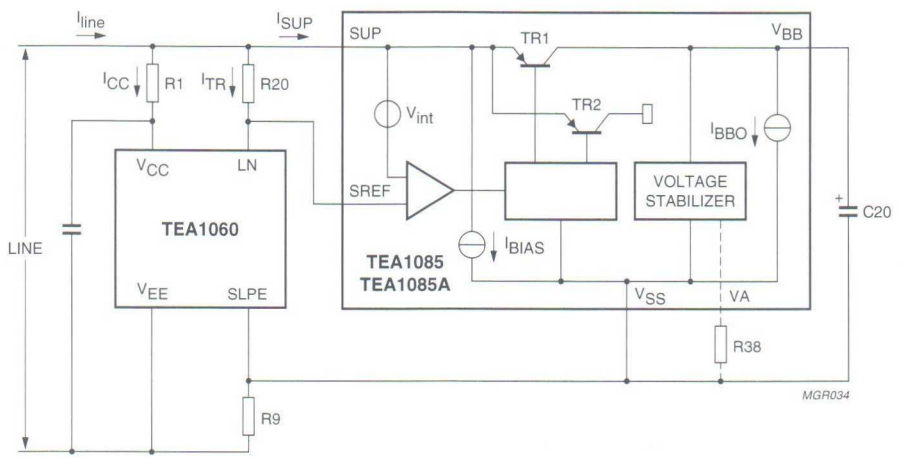


Fig.3 Interconnection of the TEA1085/TEA1085A with the TEA1060.

Supply; SUP, SREF, V_{BB}, V_{SS} and VA

The line current is divided into I_{TR} for the TEA1060 and I_{SUP} for the TEA1085/TEA1085A. The supply arrangement is illustrated in Fig.4.



I_{TR} is constant: $I_{TR} = V_{int} / R20$; $I_{SUP} = I_{line} - I_{CC} - I_{TR}$

Fig.4 Supply arrangement.

Where:

V_{int}	is an internal temperature compensated reference voltage with a typical value of 315 mV between SUP and SREF
R20	is a resistor between SUP and SREF
I_{CC}	is the internal current consumption of the TEA106X (≈ 1 mA)

A practical value for R20 is 150 Ω. This value of resistance produces a value for I_{TR} = 2 mA and $I_{SUP} = I_{line} - 3$ mA.

The TEA1085/TEA1085A stabilizes its own supply voltage at V_{BB}. Transistor TR1 provides the supplies for the internal circuits. TR2 is used to minimize the signal distortion on the line by momentarily diverting the input current to V_{SS} whenever the instantaneous value of the voltage V_{SUP} drops below the supply voltage V_{BB}. V_{BB} is fixed to a typical value of 3.6 V but can be increased by means of an external resistor (R38) connected between VA and V_{SS} or decreased by connecting this resistor between VA and V_{BB}. The minimum level on V_{BB} is restricted to 3.0 V; the level of the V_{BB} limiter is also affected (see application report for further information). The supply at V_{BB} is decoupled by a 470 µF capacitor.

The DC voltage ($V_{SUP} - V_{SS}$) is determined by the transmission IC ($V_{LN-SLPE}$); thus:
$V_{SUP} - V_{SS} = V_{LN-SLPE} + V_{int}$.
The minimum DC voltage that can be applied to this input is $V_{BB(max)} + 0.4$ V.

Where: $V_{BB(max)}$ is the worst case supply voltage (this depends on the setting of R38, which is connected between VA and V_{SS}).

The internal current consumption of the TEA1085/TEA1085A (I_{SUP0}) is typically 4.2 mA (where $V_{SUP} - V_{SS}$ = 4.5 V, MUTE off). Thus the current available for powering the loudspeaker is $I_{SUP} - I_{SUP0}$.
The current I_{SUP0} consists of a bias current of ≈ 0.4 mA for the circuitry connected to SUP and current I_{BB0} of ≈ 3.8 mA which is used for the circuitry connected to V_{BB} (see Fig.4).

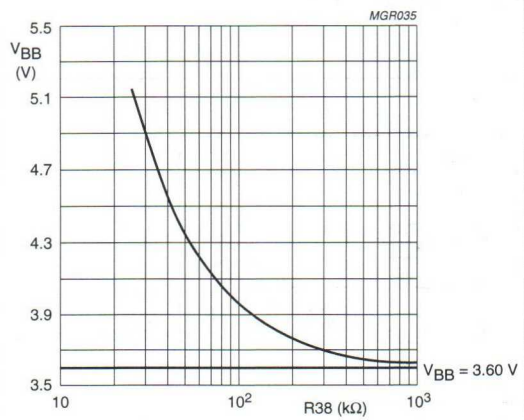


Fig.5 Stabilized supply voltage as a function of R38.

Supply amplifier stability (SDC) pin 3

To ensure stability of the TEA1085/TEA1085A, in combination with a transmission IC of the TEA1060 family, a 47 pF capacitor connected between SDC and SUP and a 150 μH coil connected between SUP and the positive line terminal (Fig.16) is required.

Loudspeaker amplifier (LSI1/LSI2 and QLS1/QLS2) pins 5/6, 21/22

The TEA1085/TEA1085A have symmetrical inputs at LSI1 and LSI2. The input signal is normally taken from the earpiece output of the transmission circuit via a resistive attenuator (see Fig.3). The amount of attenuation must be chosen in accordance with the receive gain of the transmission IC (which depends on the sensitivity of the earpiece transducer). The maximum input signal level is 450 mV(RMS) at T_{amb} = +25 °C.
The outputs QLS1 and QLS2 can be used for single ended drive (SE) or bridge tied load drive (BTL). The output stages have been optimized for use with a 50 Ω loudspeaker (e.g. Philips type AD2071).
The gain of the amplifier is fixed to ≈ 35 dB for the SE drive and ≈ 41 dB for the BTL drive (when the inputs for logic control are left open-circuit or are connected to V_{SS}).
The volume control can be obtained by using a potentiometer at the input and/or by the logic control function.

Logic gain control (GSC1 and GSC2) pins 7 and 8

The logic inputs GSC1 and GSC2 can be used to reduce the gain of the loudspeaker amplifier by means of the logic gain control function in 3 steps of 6 dB.

Table 1 Data for microcontroller drive of logic inputs

GSC2	GSC1	gain (dB)	gain reduction (dB)
0	0	35	0
0	1	28.7	6.3
1	0	22.2	12.2
1	1	17	18

Where:

0 = connection to V_{SS} or left open-circuit
1 = applying a voltage ≥ V_{SS} + 1.5 V

Dynamic limiter (DLC) pin 23

To prevent distortion of the signal at the loudspeaker outputs the gain of the amplifier is reduced rapidly when:

- the peaks of the signal at the loudspeaker outputs exceed an internally determined threshold (voltage limiter)
- the DC current into SUP is insufficient (current limiter)
- the voltage at V_{BB} decreases below an internally determined threshold, typically 2.9 V (V_{BB} limiter)

The time in which the gain reduction is effected is the 'attack time'; this is very short in the first and third instance and relatively long in the second instance. The circuit will remain in the gain-reduced condition until the peaks of the output signal remain below the threshold level. The gain will then return to a nominal level after a time determined by the capacitor connected to DLC (release time).

MUTE input (MUTE) pin 20; TEA1085A

This MUTE is provided with a logic input to operate with a microcontroller for instance.
The loudspeaker amplifier is disabled when the MUTE input is LOW (connected to V_{SS} or open input). A HIGH level at the MUTE input enables the amplifier in the listening-in mode.

MUTE input (MUTE) pin 20; TEA1085

The MUTE function is provided with a toggle input and is designed to switch between the standby condition and the listening-in condition on the rising edge of the input MUTE signal (see Fig.6).
In the basic application the MUTE input must be LOW (connected to V_{SS}). A simple push-button can be used to operate the MUTE toggle (see Fig.7). Debouncing can be realized by means of a small capacitor connected between MUTE and V_{SS}.
An internal start circuit ensures that the circuit always starts up in the standby condition.

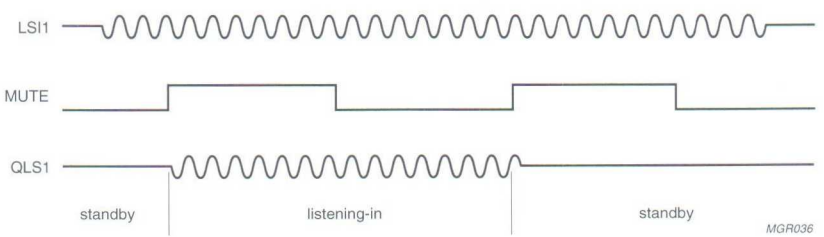
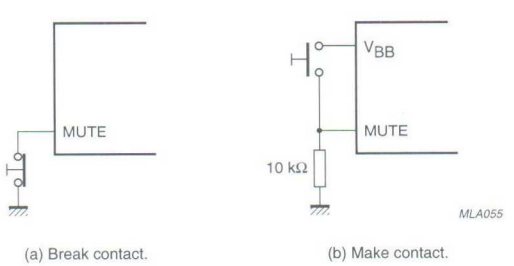


Fig.6 Mute toggle function of the TEA1085.



(a) Break contact. (b) Make contact.

Fig.7 Mute switch alternatives with the TEA1085.

Power down input (PD) pin 19

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, thereby breaking the supply to the transmission and listening-in circuits. The capacitor connected to V_{BB} provides the supply for the listening-in circuit during the supply breaks.
By making the PD input HIGH during the loop break the requirement on the capacitor is eased and, consequently, the internal (standby) current consumption I_{BBO} (Fig.4) at V_{BB} is reduced from 3.8 mA to 400 μA typical. So that the transmission circuit is not affected transistors TR1 and TR2 are inhibited and the bias current is reduced from ≈ 0.4 mA to ≈ 55 μA with V_{SUP} = 4.5 V in the following equation:

$I_{SUP(PD)} = I_{BIAS(PD)} = (V_{SUP} - 2V_d) / Ra$

(where $4.2\ V < V_{SUP} < V_{BB} + 3\ V$)

$2V_d$ = the voltage drop across 2 internal diodes (≈ 1.3 V)
Ra = an internal resistor of typical 60 kΩ

Larsen limiter current stabilizer (SIC) pin 17

A current reference is set by resistor R36 between SIC and V_{SS}. The preferred value is 120 kΩ. The internal reference current is given by the following equation:

$I_{SIC} = 1.25 / R36$; when R36 = 120 kΩ, I_{SIC} = 10.5 μA

Changing the value of R36 will affect the timing of the Larsen level limiter system.

Larsen limiter preamplifier (LAI1/LAI2 and QLA) pins 9/10 and 11

This circuit amplifies the microphone signal to a level suitable for the Larsen limiter detector. The gain is set by external components (see Fig.8).
Normally the gain is set to the same level as the microphone amplifier of the transmission circuit, this ensures that the output signal level at output QLA is equal to the line signal level.

The gain between QLA and the microphone input is given by the following equation (the high-pass filter is not taken into account):

$A_{pre} = V_{QLA} / V_M = R29 / R26$; in the basic application R25 = R26 = 10 kΩ

The gain can be adjusted between 30 dB (R29 = 316 kΩ) and 52 dB (R29 = 4 MΩ). The impedance result of R28 and R27 in parallel must be equal to R29 (e.g. R27 = R28 = 2 × R29).

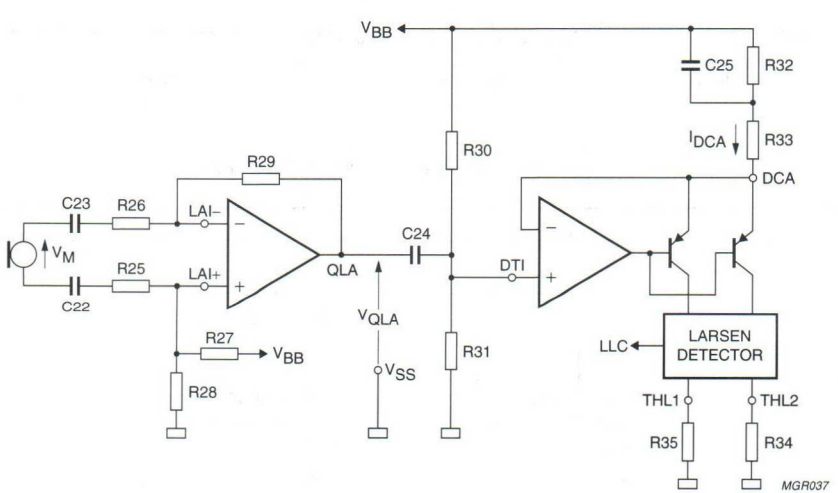


Fig.8 Larsen limiter preamplifier and voltage/current converter.

Larsen limiter detector (DTI and DCA) pins 15 and 16

The QLA output signal is AC coupled to the detector input DTI. DTI is biased by potential divider R30 and R31. The voltage applied to DTI of the Larsen level limiter is converted into a current for further processing in this circuit. Current adjustment is achieved using the network connected between DCA and V_{BB} (see Fig.8).

The equation for DC current is:

$$I_{DCA} = \frac{R30}{R30 + R31} \times V_{BB} \times \frac{1}{R32 + R33}$$

The equation for AC current is:

$$i_{DCA} = \frac{V_{DTI}}{R33} \text{ for } f > \frac{1}{2}\pi \text{ R33 C25}$$

In the basic application:

R30 = 100 kΩ, R31 = 220 kΩ, R33 = 500 Ω, R32 = 100 kΩ and C25 = 330 nF

This results in I_{DCA} = 11 μA and the equation:

$$\frac{i_{DCA}}{V_{DTI}} = 2 \text{ (mA/V)}$$

High-pass filter

A third order high-pass filter is created between the microphone input voltage and the current flowing into DCA. The cut-off frequencies (see Fig.9) of the three sections are:

$$f1 = \frac{1}{2\pi R_{eg} C24} \text{ where } R_{eq} = \frac{R30 \times R31}{R30 + R31}$$

$$f2 = \frac{1}{2\pi R33 C24}$$

$$f3 = \frac{1}{2\pi R26 C23} = 1/(2\pi R25 C22)$$

Where: R25 = R26 and C22 = C23

The filter reduces the sensitivity of the system to own speech.
Normal speech is in the frequency range 300 Hz to 3400 Hz, however, the Larsen signal normally occurs at a frequency > 3 kHz.
With the component values as used in the basic application (see Fig.16); f1 = 500 Hz, f2 = 1 kHz and f3 = 3 kHz

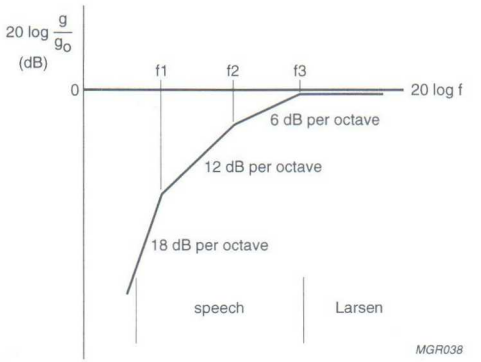


Fig.9 Third-order high-pass filter.

Where: $g = \frac{i_{DCA}}{V_m}$ $g_o = \frac{A_{pre}}{R33}$

Larsen limiter capacitor (LLC) pin 12

A 1 μF capacitor (C26) is connected externally between V_{SS} and LLC to determine the attack and release timing of the Larsen level limiter in the listen-in and Larsen mode. The timing is also dependent on the value of the resistor connected between SIC and V_{SS}.

Larsen level limiter threshold (THL1 and THL2) pins 13 and 14

When the signal at DTI exceeds the first threshold level the capacitor connected to LLC will start to discharge. The first threshold level is determined by the value of the resistor, R35, connected to THL1 and V_{SS}. The amount of discharge of C26 depends on how much the level of the signal at DTI exceeds the first threshold level (for normal speech the discharge is small).
The Larsen effect is generally defined as a signal level of ≥ 100 mV(RMS), on line, for a period of more than 100 ms. The Larsen signal must be reduced to a low level within 200 ms. For Larsen signal levels (f > f3 in Fig.9) of ≥ 100 mV(RMS) at DTI and, with the component values of Fig.16, the system will switch from the listen-in mode to the Larsen mode in a time period of 100 ms to 200 ms; consequently, the initial Larsen effect will last only for a short period of time.

This reaction time is the 'attack delay time' and ensures minimum sensitivity of the system for own speech.

The first threshold level at DTI is determined by the equation:

$$V_{DTI1} = \left(\frac{1.25}{R25} - \frac{I_{DCA}}{2}\right) \times 2 \times R33 \quad \text{(if f > f3 in Fig.9)}$$

Where: I_{DCA} = the DC current into DCA

With the component values given in Fig.16, I_{DCA} = 11 μA thus V_{DTI1} = 18.8 mV.

Listen-in mode

During normal speech the discharge of the capacitor connected to LLC is not sufficient to reach the threshold level whereby the system switches to the Larsen mode. This is because normal speech is not continuous, the discharge of C26 is slow (attack delay) and the charge is fast.
The slope of V_{LLC} during charge is given in the equation:

$$S_{1i} = \frac{\Delta V_{LLC}}{\Delta_\tau} = \frac{1.25}{C26 \times R36} \quad (V/s)$$

With C26 = 1 μF and R36 = 120 kΩ this results in S_{1i} = 10 V/s.

Discharge of the capacitor at LLC occurs when the signal at DTI exceeds V_{DTI1}, thus for a continuous signal at DTI the attack delay time t_{ad} (see Fig.10) is determined by the equation:

$$t_{ad} = \frac{C26 \times R36}{2 \times (3 \times k - 1)}$$

Where $k = t_1 / T$

The duty cycle is determined by the time in which the first threshold level (V_{DTI1}) is exceeded by the signal level at DTI (see Fig.11) thus for large signals; $k \leq 0.5$.
With the component values given in Fig.16; $k \geq 0.457$ for signals ≥ 100 mV(RMS).
Consequently 120 ms ≤ t_{ad} ≤ 160 ms, for V_{DTI} ≥ 100 mV(RMS)

Larsen mode

After the 'attack delay time' the circuit switches from the listen-in mode to the Larsen mode. The gain of the loudspeaker amplifier is reduced quickly to a value (t_{LAa} = Larsen attack time, see Fig.10) whereby the residual Larsen signal is determined by a second threshold level. This level can be set by resistor R34 connected between THL2 and V_{SS}. The second threshold level must always be selected at a lower level than the first threshold level thus R34 > R35.
The time taken to effect gain reduction is very short. In the Larsen mode the circuit acts as a dynamic limiter with peak detector and regulates the gain so that the signal level at DTI is determined by the second threshold level V_{DTI2}.
The second threshold level at DTI is determined by the equation:

$$V_{DTI2} = \left(\frac{1.25}{R34} - \frac{I_{DCA}}{2}\right) \times 2 \times R33 \quad \text{(if f > f3 in Fig.9)}$$

Where: I_{DCA} = the DC current into DCA

With the component values given in Fig.16, V_{DTI2} = 6.9 mV.

The charge current in the Larsen mode is reduced to half the charge current in the listen-in mode.

The slope of V_{LLC} during charge (see Fig.10) is given in the equation:

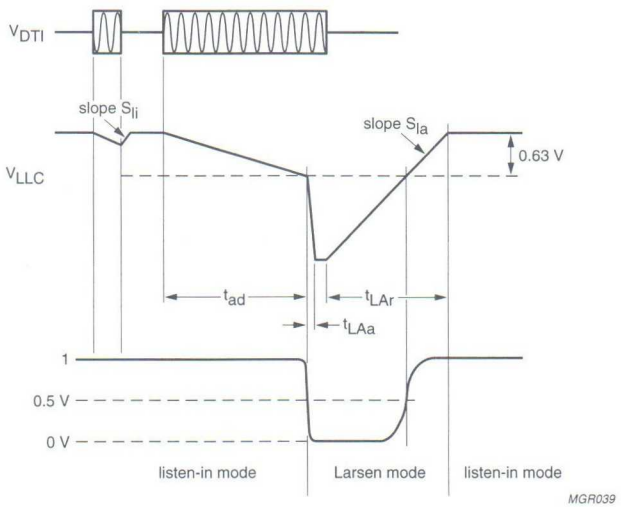
$$S_{1a} = \frac{\Delta V_{LLC}}{\Delta_\tau} = \frac{1.25}{2 \times C26 \times R34} \quad (V/s)$$

Where: C26 = 1 μF and R36 = 100 kΩ, S_{1a} = 5 V/s

When the Larsen effect stops (total open-loop gain < 1) the gain of the loudspeaker amplifier will return to its normal value in a time period known as the 'Larsen release time' (t_{LAr}). This time period is determined by capacitor C26 connected to LLC and resistor R36 connected to SIC.

Where: C26 = 1 μF and R36 = 120 kΩ, t_{LAr} = 250 ms

In practice the choice of the threshold levels (determined by R35 and R34) depends on the sensitivity of the microphone and loudspeaker, the send and receive gains, sidetone suppression and the acoustical properties which are determined by the cabinet of the telephone set.

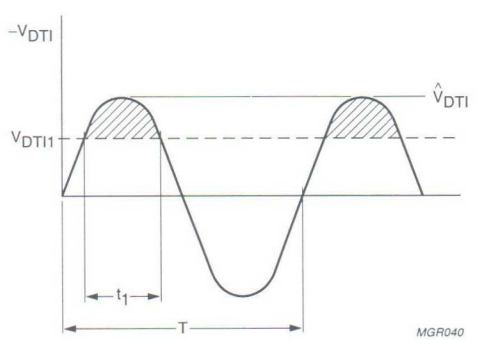


Where:

Change of receive gain $= \frac{G_v}{G_{vo}}$

Nominal receive gain $= 20 \log G_{vo} = 35$ dB

Fig.10 Dynamic behaviour of Larsen limiter (in open-loop condition).



Where:

$k = \frac{t_1}{T}$

$$k = 0.5 - \frac{\arcsin\left(\frac{V_{DTI1}}{\hat{V}_{DTI}}\right)}{\pi}$$

Fig.11 Definition of duty cycle k.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

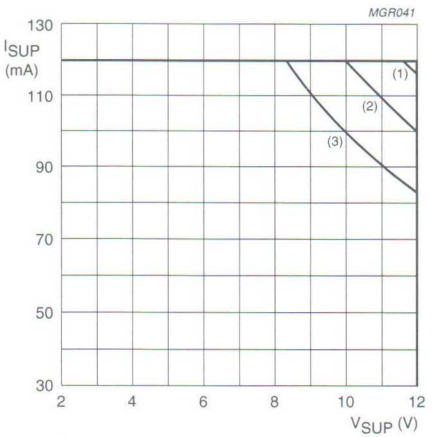
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{SUP}	positive supply voltage				
	continuous		–	12	V
	during switch-on or line interruption		–	13.2	V
	repetitive supply voltage from 1 ms to 5 s	with 12 Ω current limiting resistor in series with supply	–	28	V
V_{SREF}	supply reference voltage		V_{SS} – 0.5	V_{SUP} + 0.5	V
V_n	voltage on all other pins		V_{SS} – 0.5	V_{BB} + 0.5	V
I_{SUP}	supply current				
	TEA1085/TEA1085A	see Fig.12	–	120	mA
	TEA1085T/TEA1085AT	see Fig.13	–	120	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C; T_j = 125 °C			
	TEA1085/TEA1085A		–	1	W
	TEA1085T/TEA1085AT		–	666	mW
T_{amb}	operating ambient temperature range		–25	+75	°C
T_{stg}	storage temperature range		–40	+125	°C
T_j	junction temperature		–	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air		
	TEA1085/TEA1085A		50 K/W
	TEA1085T/TEA1085AT	note 1	75 K/W

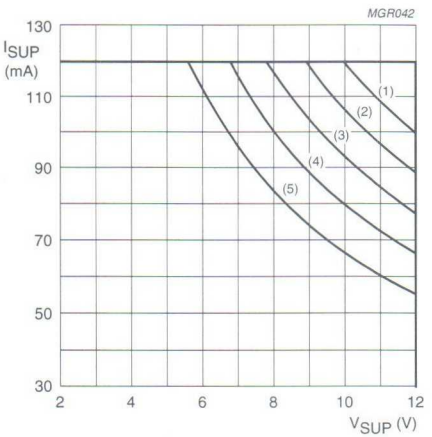
Note

1. Device mounted on a glass epoxy board 40.1 × 19.1 × 1.5 mm.



(1) T_{amb} = 55 °C; P_{tot} = 1.4 W.
(2) T_{amb} = 65 °C; P_{tot} = 1.2 W.
(3) T_{amb} = 75 °C; P_{tot} = 1.0 W.

Fig.12 TEA1085/TEA1085A safe operating area.



(1) T_{amb} = 35 °C; P_{tot} = 1.2 W.
(2) T_{amb} = 45 °C; P_{tot} = 1.07 W.
(3) T_{amb} = 55 °C; P_{tot} = 0.93 W.
(4) T_{amb} = 65 °C; P_{tot} = 0.8 W.
(5) T_{amb} = 75 °C; P_{tot} = 0.666 W.

Fig.13 TEA1085T/TEA1085AT safe operating area.

CHARACTERISTICS

V_{SREF} = 4.2 V; V_{SS} = 0 V; I_{SUP} = 15 mA; V_{SUP} = 0 V(RMS); f = 800 Hz; T_{amb} = 25 °C; PD = LOW; MUTE (TEA1085) = OFF (listening-in mode); MUTE (TEA1085A) = HIGH (listening-in mode); GSC1 = GSC2 = LOW; 50 Ω loudspeaker; no R38; test circuit Fig.14; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{SUP}	minimum DC input voltage		–	V_{BB} + 0.7	–	V
$V_{SUP-SREF}$	internal reference voltage		275	315	355	mV
V_{BB}	stabilized supply voltage	no R38; I_{SUP} = 15 mA	3.4	3.6	3.8	V
ΔV_{BB}	variation from I_{SUP} = 15 to 120 mA		–	10	–	mV
		R38 = 39.2 kΩ between pins V_{SS} and VA; V_{SREF} = 5.2 V; I_{SUP} = 15 mA	4.2	4.45	4.7	V
$\Delta V_{BB}/\Delta T$	variation with temperature	no R38; I_{SUP} = 15 mA	tbf	–0.2	tbf	V
I_{SUP}	minimum operating current		–	4.2	5.5	mA
THD	distortion of AC signal on SUP	$V_{SUP(RMS)}$ = 1 V	–	0.3	–	%
$V_{no(RMS)}$	noise between SUP and V_{EE}		–	–72	–	dBmp
	current consumption in power-down condition	PD = HIGH				
I_{SUP}		V_{SUP} = 4.5 V	–	55	75	µA
I_{BB}		V_{BB} = 3.6 V	–	400	550	µA
Loudspeaker amplifier inputs LSI1 and LSI2						
$\|Z_i\|$	input impedance					
		single ended	7.5	9.5	11.5	kΩ
		differential	15	19	23	kΩ
G_v	voltage gain with 50 Ω load	I_{SUP} = 15 mA; V_i = 1.8 mV(RMS)				
		single ended	34	35	36	dB
		BTL output	39.9	40.9	41.9	dB
ΔG_v	variation with signal level	I_{SUP} = 50 mA; V_i = 1.8 mV(RMS) and 14 mV(RMS)				
		single ended	–	+0.1	0.4	dB
		BTL output	–	+0.2	0.6	dB
ΔG_v	variation with frequency referred to 1 kHz	f = 300 Hz and 3400 Hz; V_i = 1.8 mV(RMS)				
		single ended	–	± 0.1	–	dB
		BTL output	–	± 0.1	–	dB
ΔG_v	variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C				
		single ended	–	± 0.4	–	dB
		BTL output	–	± 0.5	–	dB

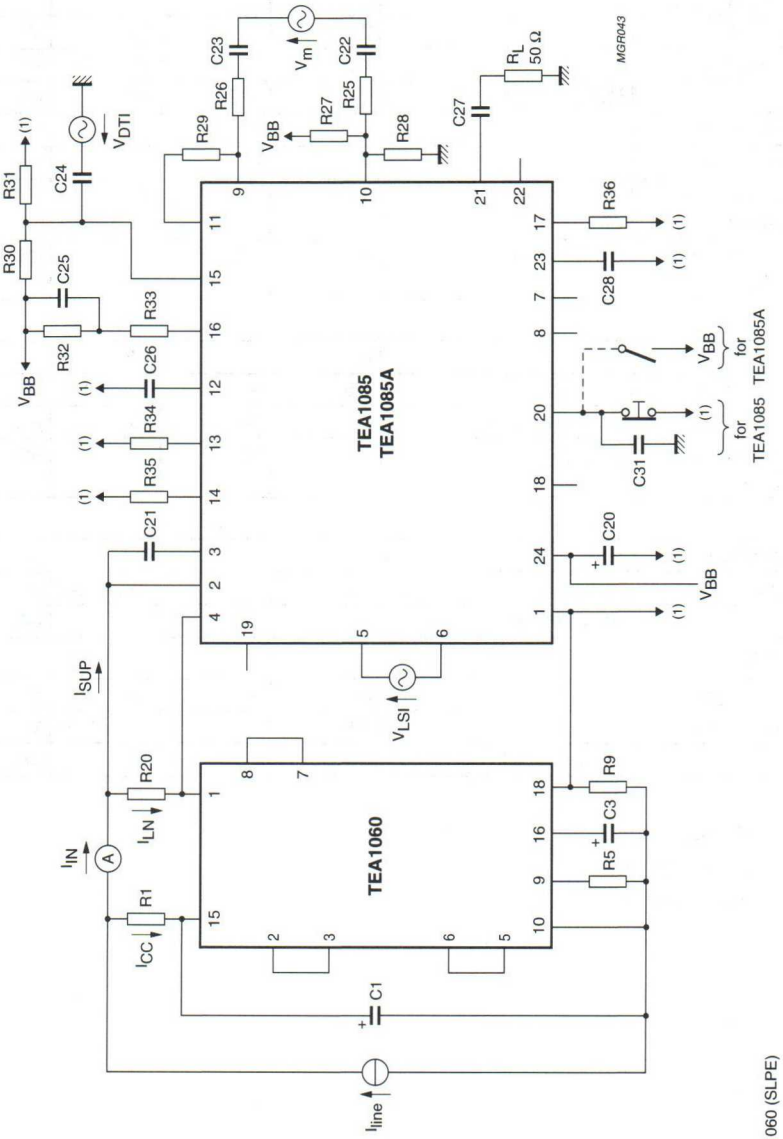
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Loudspeaker outputs QLS1 and QLS2						
$V_{o(p-p)}$	output voltage (peak-to-peak value)	V_i = 22 mV(RMS)				
	single ended	I_{SUP} = 9 mA; note 1	1.2	1.45	–	V
		I_{SUP} = 17 mA; note 2	2.5	2.9	–	V
	bridge tied load	I_{SUP} = 23.5 mA; note 2	2.5	2.9	–	V
		I_{SUP} = 32 mA; note 3	3.5	4.0	–	V
THD	total harmonic distortion	V_i = 22 mV(RMS)				
	single ended	I_{SUP} = 9 mA	–	0.4	2	%
		I_{SUP} = 17 mA	–	0.7	2	%
	bridge tied load	I_{SUP} = 23.5 mA	–	0.4	2	%
$V_{o(p-p)}$	output voltage (peak-to-peak value)	V_i = 22 mV(RMS)				
	single ended	I_{SUP} = 17 mA; $V_{SUP} - V_{EE}$ = 1 V(RMS)	1.75	2.15	–	V
Dynamic limiter						
THD	total harmonic distortion	V_i = 22 mV(RMS) +10 dB				
	single ended	I_{SUP} = 9 mA	–	0.5	10	%
		I_{SUP} = 17 mA	–	1.2	10	%
	bridge tied load	I_{SUP} = 23.5 mA	–	0.6	10	%
t_{att}	dynamic behaviour of limiter attack time; V_i jumps from 10 mV(RMS) to 65 mV(RMS)	single ended load				
	voltage limiter	I_{SUP} = 17 mA	–	2	5	ms
	current limiter	I_{SUP} = 12 mA	–	500	tbf	ms
	V_{BB} limiter	I_{SUP} = 9 mA	–	10	–	ms
t_{rel}	release time; V_i jumps from 65 mV(RMS) to 10 mV(RMS)	I_{SUP} = 17 mA	tbf	75	tbf	ms
V_{BBO}	threshold V_{BB} limiter below which gain reduction starts	I_{SUP} = 9 mA	tbf	2.95	tbf	V
$V_{no(RMS)}$	noise output voltage	1 kΩ between inputs LSI1, LSI2; psophometrically weighted (P53 curve)				
	single ended		–	170	–	μV
	bridge tied load		–	350	–	μV
Logic gain control						
ΔG_v	reduction of voltage gain	V_i = 1.8 mV(RMS)				
	GSC2 = 0, GSC1 = 1		5.8	6.3	6.8	dB
	GSC2 = 1, GSC1 = 0		11.7	12.2	12.7	dB
	GSC2 = 1, GSC1 = 1		17	18	19	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Larsen limiter preamplifier						
	operational amplifier					
G_{v0}	open-loop gain		–	92	–	dB
f_{p1}	1st pole		–	120	–	Hz
f_{p2}	2nd pole		–	3.3	–	MHz
G_B	unity gain bandwidth		–	4	–	MHz
G_v	voltage gain	f = 3 kHz; R26 = 10 kΩ; R29 = 4 MΩ	51	52	53	dB
G_v	gain adjustment range		30	–	52	dB
Larsen limiter detector						
	voltage to current convertor					
V_{DCA}-V_{DTI}	DC offset voltage	$V_{BB} - V_{DTI}$ = 1 V	–25	1	+25	mV
G_v	voltage gain from DTI to DCA	V_{DTI} = 100 mV(RMS); f = 3 kHz	tbf	–0.8	tbf	dB
V_{THL1}	DC voltage at THL1	R35 = 51 kΩ	1.8	1.25	1.33	V
V_{THL2}	DC voltage at THL2	R34 = 100 kΩ	1.8	1.25	1.33	V
	dynamic behaviour with a burst at DTI	f = 3 kHz; see Fig.15				
t_{LIr}	listen-in release time	see Fig.15(a)	tbf	40	tbf	ms
t_{ad}	attack delay time	see Fig.15(b)				
	V_{DTI} jumps from 0 to 100 mV (RMS value)		–	160	200	ms
	V_{DTI} jumps from 0 to 1 V (RMS value)		100	120	–	ms
t_{LAa}	Larsen attack time	see Fig.15(b); V_{DTI} = 100 mV(RMS)	–	20	tbf	ms
t_{LAr}	Larsen release time	see Fig.15(b)				
	V_{DTI} jumps from 100 mV to 0 mV (RMS value)		tbf	250	tbf	ms
V_{LLC}	DC voltage at LLC	V_{DTI} = 0 V	1.75	1.9	2.0	V
$-\Delta V_{LLC}$	reduction of V_{LLC} to attack Larsen mode		0.59	0.63	0.68	V
ΔG_v	gain reduction	V_{LLC} = 0.7 V	60	tbf	tbf	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MUTE input; TEA1085						
	(toggle function, positive edge triggered set-reset flip-flop)					
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	$V_{BB}+0.4$	V
I_{MUTE}	input current	MUTE = LOW	–	–22	–28	μA
t_W	minimum input pulse width		–	50	–	μs
P_R	minimum pulse repetition time		–	2	–	ms
$V_{BB(MUTE)}$	supply voltage below which MUTE toggle is reset		tbf	2	tbf	V
ΔG_v	reduction of gain from LSI1, LSI2 to QLS1, QLS2	MUTE = ON	60	100	–	dB
MUTE input; TEA1085A						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	$V_{BB}+0.4$	V
I_{MUTE}	input current	MUTE = HIGH	–	10	20	μA
ΔG_v	reduction of gain from LSI1, LSI2 to QLS1, QLS2	MUTE = HIGH	60	100	–	dB
Power down input						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	$V_{BB}+0.4$	V
I_{PD}	input current	PD = HIGH	–	2.3	2.8	μA
Logic inputs GSC1 and GSC2						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	$V_{BB}+0.4$	V
I_{GSC}	input current	GSC = HIGH	–	6	8	μA

Notes

1. Typical output power is 5 mW into 50 Ω
2. Typical output power is 20 mW into 50 Ω
3. Typical output power is 40 mW into 50 Ω



(1) To TEA1060 (SLPE)

The DC current is divided as follows:

$$I_{SUP} = I_{IN} - \frac{V_{SUP-SREF}}{R20}$$

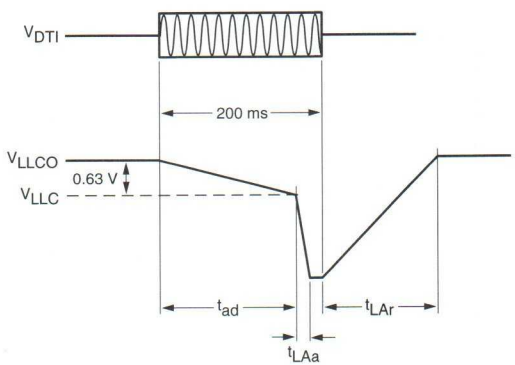
$$I_{LN} = \frac{V_{SUP-SREF}}{R20}$$

The pins not shown in the TEA1060 are left open. An impedance in series with pin SUP (e.g. an ammeter) should be avoided as it interferes with the value of I_{LN}.

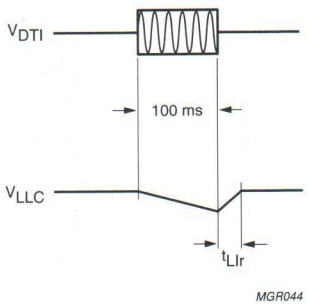
Fig.14 Test circuit.

Table 2 Component values in test circuit Fig.14

COMPONENT	CONDITION	VALUE	UNIT
Resistor			
R1		620	Ω
R5		3.6	kΩ
R9		20	Ω
R20		150	Ω
R25		10	kΩ
R26		10	kΩ
R27		8	MΩ
R28		8	MΩ
R29		4	MΩ
R30		100	kΩ
R31		220	kΩ
R32		100	kΩ
R33		500	Ω
R34		100	kΩ
R35		51	kΩ
R36		120	kΩ
Capacitor			
C1		100	µF
C3		4.7	µF
C20		470	µF
C21		68	pF
C22		2.2	µF
C23		2.2	µF
C24		100	nF
C25		330	nF
C26		1	µF
C27		220	µF
C28		330	nF
C31	TEA1085 only	10	nF



(b) Attack delay (t_{ad}), Larsen attack time (t_{LAa}), Larsen release time (t_{LAr});
V_{DTI} = 100 mV(RMS) and 1 V(RMS); f = 3 kHz.



(a) Listen-in release time (t_{LIr});
V_{DTI} = 100 mV(RMS); f = 3 kHz.

Fig.15 Test signals for Larsen level limiter.

APPLICATION INFORMATION

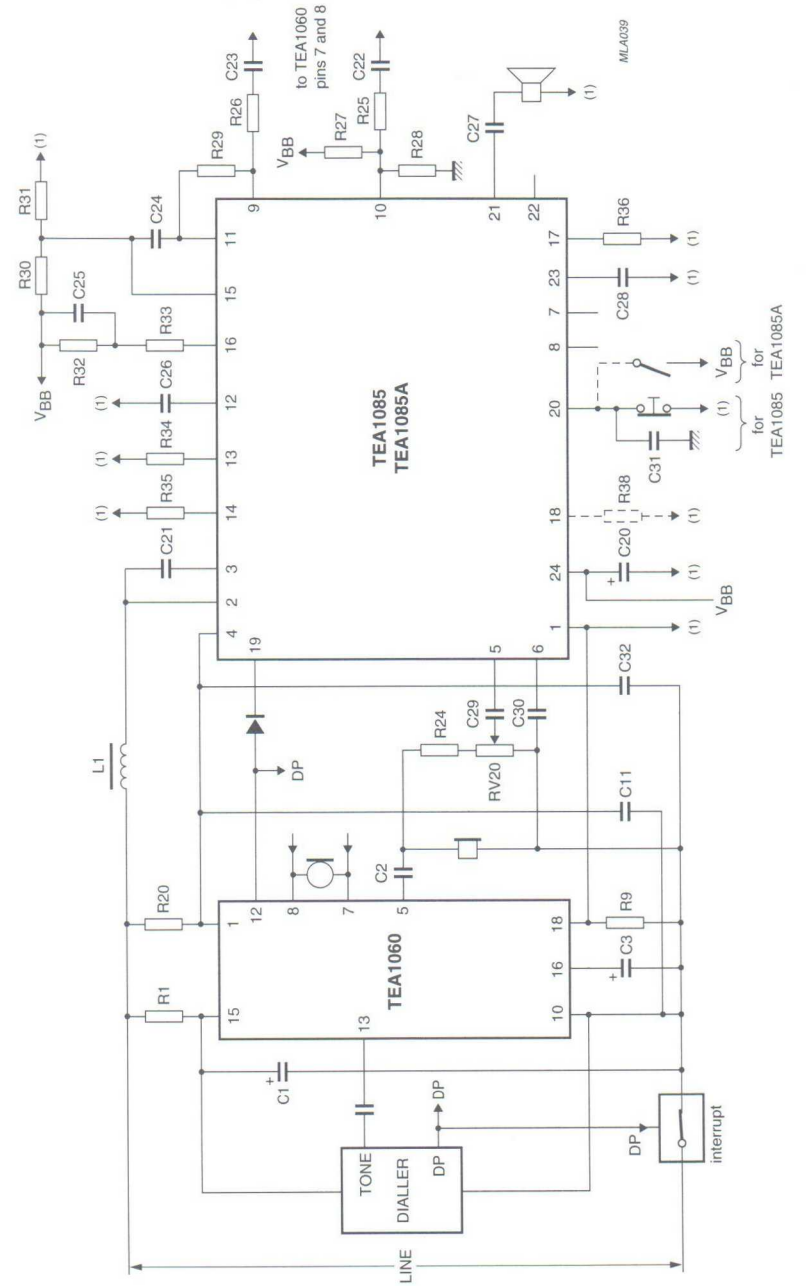


Fig.16 Basic application of TEA1085/TEA1085A and TEA1060.

The basic application circuit of the TEA1085/TEA1085A is illustrated in Fig.16. Only the most important components of the TEA1060 part are shown, other components and their values are given in the TEA1060 Data sheet.
The supply pin (V_{BB}) of the TEA1085/TEA1085A can also be used to supply peripheral circuits (e.g. microcontrollers, diallers etc.). Further information will be published in the TEA1085 application report.

Table 3 Component values in application circuit Fig.16

COMPONENT	CONDITION	VALUE	UNIT
Resistor			
R20		150	Ω
R24	note 1	1	kΩ
R25		10	kΩ
R26		10	kΩ
R27	note 1	3.3	MΩ
R28	note 1	3.3	MΩ
R29	note 1	1.65	MΩ
R30		100	kΩ
R31		220	kΩ
R32		100	kΩ
R33		500	Ω
R34		100	kΩ
R35		51	kΩ
R36		120	kΩ
RV20	note 1	1	kΩ
Capacitor			
C11		4.7	nF
C20		470	μF
C21		47	pF
C22		4.7	nF
C23		4.7	nF
C24		4.7	nF
C25		330	nF
C26		1	μF
C27		47	μF
C28		330	nF
C29		220	nF
C30		220	nF
C31	TEA1085 only	10	nF
Coil			
L1		150	μH

Note

1. Value depends on the gain setting of the transmission circuit.

Speech and loudspeaker amplifier IC with auxiliary inputs/outputs and analog multiplexer

TEA1097TV

FEATURES

Line interface

- Low DC line voltage
- Voltage regulator with adjustable DC voltage
- Symmetrical high impedance inputs (70 kΩ) for dynamic, magnetic or electret microphones
- DTMF input with confidence tone on earphone and/or loudspeaker
- Receive amplifier for dynamic, magnetic or piezo-electric earpieces (with externally adjustable gain)
- AGC: automatic gain control for true line loss compensation.

Supplies

- Provides a strong 3.35 V regulated supply for micro-controller or dialler
- Provides filtered power supply, optimized according to line current and compatible with external voltage or current sources
- Filtered 2 V power supply output for electret microphone
- Compatible with a ringer mode
- $\overline{PD}$ logic input for power down.

Loudspeaker amplifier

- Single-ended rail-to-rail output
- Externally adjustable gain
- Dynamic limiter to prevent distortion
- Logarithmic volume control via linear potentiometer.

Auxiliary interfaces

- Asymmetrical high input impedance for electret microphone
- General purpose auxiliary output for transmit and receive
- Auxiliary transmit input with high signal level capability dedicated to line transmission
- Auxiliary receive input with high signal level capability
- Integrated multiplexer for channels selection.

APPLICATIONS

- Telephone answering machines
- Telephones with digital handsfree
- Line powered telephone sets
- Cordless telephones
- Fax machines.

GENERAL DESCRIPTION

The TEA1097TV is an analog bipolar circuit dedicated for telephony applications. It includes a line interface, handset microphone and earpiece amplifiers, base microphone and loudspeaker amplifiers, some specific auxiliary inputs/outputs (I/Os) and an analog multiplexer to enable the right transmit and/or receive channels. The multiplexer is controlled by a logic circuitry decoding four logic inputs provided by a micro-controller. Twelve different application modes have been defined and can be accessed by selecting the right logic inputs.

This IC can be supplied by the line and/or by the mains if available (in a cordless telephone or a telephone answering machine for example). It provides a 3.35 V supply for a micro-controller and a 2 V filtered voltage supply for electret microphones. The IC is designed to facilitate the use of the loudspeaker amplifier during ringing phase.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1097TV	VSO40	plastic very small outline package; 40 leads	SOT158-1

QUICK REFERENCE DATA

I_{line} = 15 mA; R_{slpe} = 20 Ω; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; AGC pin connected to LN; $\overline{PD}$ = HIGH; HFC = LOW; AUXC = LOW; $\overline{MUTT}$ = HIGH; $\overline{MUTR}$ = HIGH; measured according to test circuits; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range	normal operation	11	–	130	mA
		with reduced performance	1	–	11	mA
V_{SLPE}	stabilized voltage between SLPE and GND	I_{line} = 15 mA	tbf	3.7	tbf	V
		I_{line} = 70 mA	tbf	6.15	tbf	V
V_{BB}	regulated supply voltage for internal circuitry	I_{line} = 15 mA	tbf	3.0	tbf	V
		I_{line} = 70mA	tbf	5.35	tbf	V
V_{DD}	regulated supply voltage on pin V_{DD}	V_{BB} > 3.35 V + 0.25 V (typ.)	–	3.35	3.6	V
		otherwise	–	V_{BB} – 0.25	–	V
V_{ESI}	external voltage supply allowed on pin ESI		–	–	6	V
I_{ESI}	external current supply allowed on pin ESI		–	–	140	mA
I_{BB}	current available on pin V_{BB}					
	in speech mode		–	11.5	–	mA
	in digital handsfree application	HFC = HIGH	–	9.5	–	mA
$I_{BB(PD)}$	current consumption on V_{BB} during power down phase	$\overline{PD}$ = LOW; AUXC = LOW	–	500	–	µA
$G_{v(MIC-LN)}$	voltage gain from pin MIC+/MIC– to LN	V_{MIC} = 4 mV (RMS)	tbf	44.6	tbf	dB
$G_{v(IR-RECO)}$	voltage gain from pin IR (referred to LN) to RECO	V_{IR} = 15 mV (RMS)	tbf	29.7	tbf	dB
$\Delta G_{v(QR)}$	gain voltage range between pins RECO and QR		–3	–	+15	dB
$G_{v(TXIN-TXOUT)}$	voltage gain from pin TXIN to TXOUT	V_{TXIN} = 8 mV (RMS); R_{GATX} = 30.1 kΩ; note 1	–	15.2	–	dB
$G_{v(TXAUX-LN)}$	voltage gain from pin TXAUX to LN	V_{TXAUX} = 0.1 V (RMS); note 1	–	12.6	–	dB
$G_{v(HFRX-LSAO)}$	voltage gain from pin HFRX to LSAO	V_{HFRX} = 20 mV(RMS); R_{GALS} = 255 kΩ; note 1	–	27.8	–	dB
$\Delta G_{v(trx)}$	gain control range for transmit and receive amplifiers affected by the AGC; with respect to I_{line} = 15 mA	I_{line} = 70 mA $G_{v(MIC-LN)}$, $G_{v(IR-RECO)}$ and $G_{v(IR-AUXO)}$	tbf	6.2	tbf	dB

Note

1. When the channel is enabled according to Table 1.

BLOCK DIAGRAM

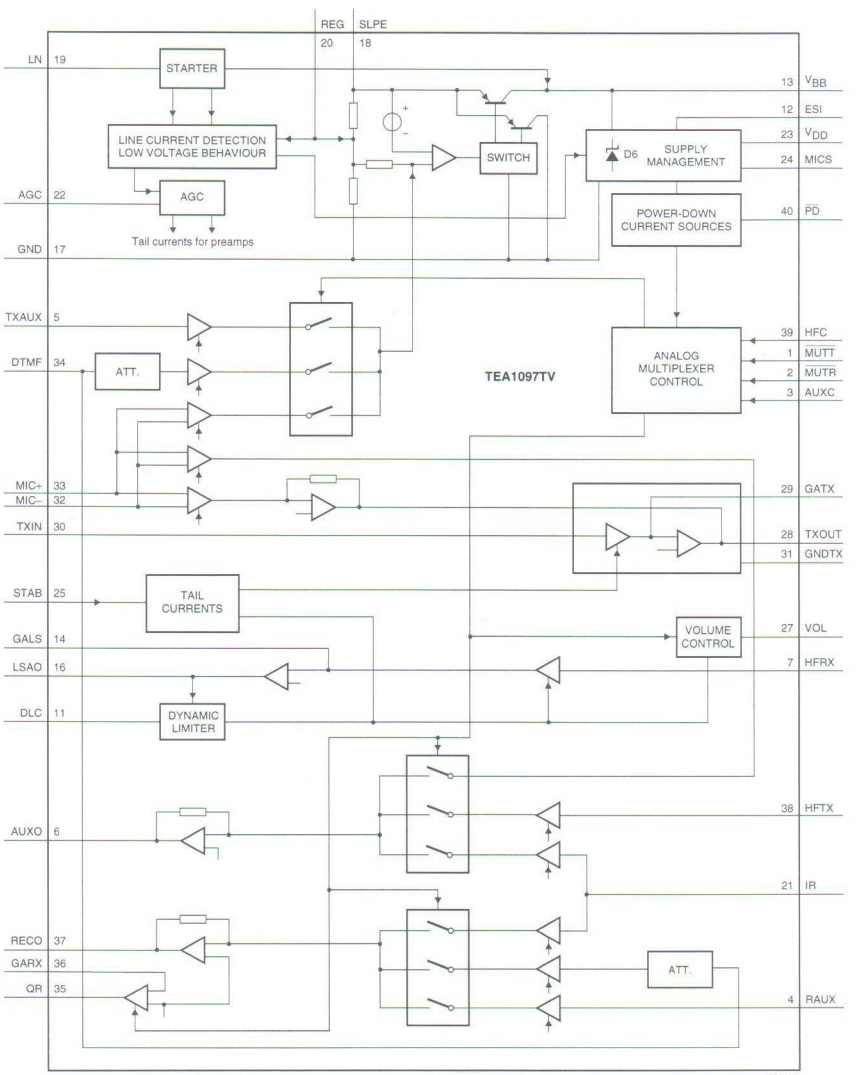


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{MUTT}$	1	logic input
$\overline{MUTR}$	2	logic input
AUXC	3	logic input
RAUX	4	auxiliary receive amplifier input
TXAUX	5	auxiliary transmit amplifier input
AUXO	6	auxiliary amplifier output
HFRX	7	receive input for loudspeaker amplifier
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
DLC	11	dynamic limiter capacitor for the loudspeaker amplifier
ESI	12	external supply input
V_{BB}	13	stabilized supply for internal circuitry
GALS	14	loudspeaker amplifier gain adjustment
n.c.	15	not connected
LSAO	16	loudspeaker amplifier output
GND	17	ground reference
SLPE	18	line current sense
LN	19	positive line terminal
REG	20	line voltage regulator decoupling
IR	21	receive amplifier input
AGC	22	automatic gain control / line loss compensation
V_{DD}	23	3.3 V regulated voltage supply for microcontrollers
MICS	24	microphone supply
STAB	25	reference current adjustment
n.c.	26	not connected
VOL	27	loudspeaker volume adjustment
TXOUT	28	base microphone amplifier output
GATX	29	base microphone amplifier gain adjustment
TXIN	30	base microphone amplifier input
GNDTX	31	ground reference for microphone amplifiers
MIC–	32	negative handset microphone amplifier input
MIC+	33	positive handset microphone amplifier input
DTMF	34	dual tone multi-frequency input
QR	35	earpiece amplifier output
GARX	36	earpiece amplifier gain adjustment
RECO	37	receive amplifier output
HFTX	38	transmit input for auxiliary receive amplifier
HFC	39	logic input
$\overline{PD}$	40	power-down input

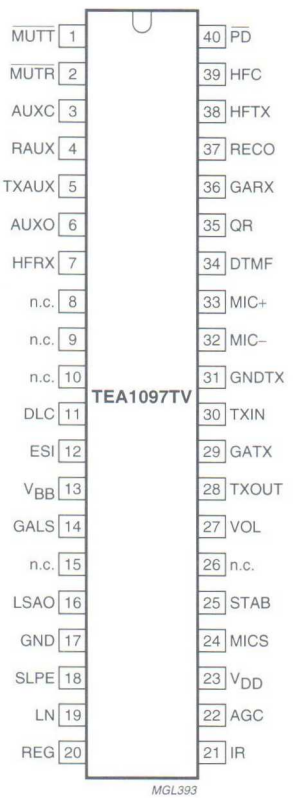


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supplies

LINE INTERFACE AND INTERNAL SUPPLY (PINS LN, SLPE, REG AND V_{BB})

The supply for the TEA1097TV and its peripherals is obtained from the line. The IC generates a stabilized reference voltage (V_{ref}) between pins SLPE and GND. This reference voltage is equal to 3.7 V for line currents lower than 18 mA. It than increases linearly with the line current and reaches the value of 6.15 V for line currents higher than 46 mA. For line currents below 9 mA, the internal reference voltage generating V_{ref} is automatically adjusted to a lower value. This is the so-called low voltage area and the TEA1097TV has limited performances in this area (see "Low voltage behaviour" section). This reference voltage is temperature compensated.

The voltage between pins SLPE and REG is used by the internal regulator to generate the stabilized reference voltage and is decoupled by means of a capacitor between pins LN and REG. This capacitor converted into an equivalent inductance realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (done by an external impedance).

The IC regulates the line voltage at pin LN and it can be calculated as follows:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I^{x}$$

where:

I_{line} = line current

I^{x} = current consumed on pin LN (approximately a few μA)

I_{SLPE} = current flowing through the R_{SLPE} resistor

The preferred value for R_{SLPE} is 20 Ω. Changing this value will affect more than the DC characteristics; it also influences the transmit gains to the line, the gain control characteristic, the sidetone level and the maximum output swing on the line.

As can be seen from Fig.4, the internal circuitry is supplied by pin V_{BB}, which is a strong supply point combined with the line interface. The line current is flowing through the R_{SLPE} resistor and is sunk by the V_{BB} voltage stabilizer, becoming available for a loudspeaker amplifier or any peripheral IC. Its voltage is equal to 3.0 V for line currents

lower than 18 mA. It than increases linearly with the line current and reaches the value of 5.35 V for line currents greater than 46 mA. It is temperature compensated.

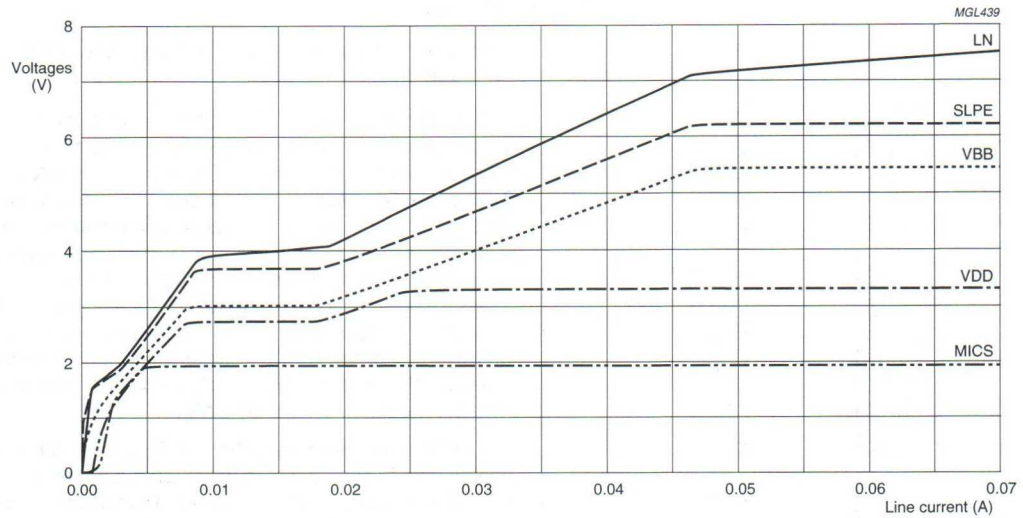


Fig.3 Main voltages versus line current.

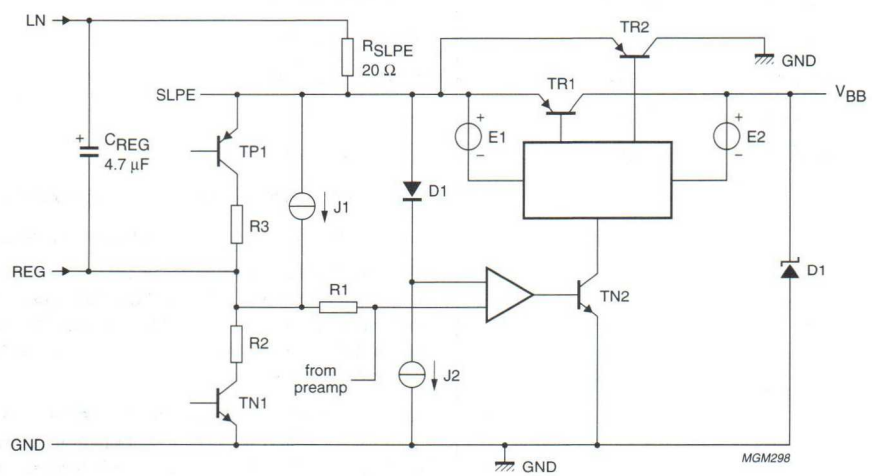


Fig.4 Line interface principle.

The aim of the current switch TR1-TR2 is to reduce distortion of large AC line signals. Current I_{SLPE} is supplied to V_{BB} via TR1 when the voltage on SLPE is greater than V_{BB} + 0.25 V. When the voltage on SLPE is lower than this value, the current I_{SLPE} is shunted to GND via TR2.

The reference voltage V_{ref} can be increased by connecting an external resistor between pins REG and SLPE. For large line currents, this increase can slightly affect some dynamic performances such as maximum signal level on the line for 2% THD. The voltage on pin V_{BB} is not affected by this external resistor.

External supply (pins ESI and V_{BB})

The TEA1097TV can be supplied by the line as well as by external power sources (voltage or current sources) that must be connected at pin ESI.

The IC will choose which supply to use according to the voltage it can provide. A voltage supply on ESI is efficient only if its value is greater than the working voltage of the internal V_{BB} voltage stabilizer. Otherwise the IC continues to be line powered. The current consumed on this source is at least equal to the internal consumption. It depends on the voltage difference between the value forced on ESI and the working voltage of the internal stabilizer. The current required increases with the voltage difference to manage. The excess current compared to the internal consumption becomes then available for other purposes such as supplying a loudspeaker amplifier. The voltage source should not exceed 6 V. If the value of the external voltage source can be lower than the working voltage of the internal stabilizer, an external diode is required to avoid reverse current flowing into the external power supply.

In case of current source, the voltage on V_{BB} and ESI depends on the current available. It is internally limited to 6.6 V. The current source should not exceed 140 mA.

V_{DD} supply for micro-controller (pin V_{DD})

The voltage on V_{DD} supply point follows the voltage on V_{BB} with a difference typically equal to 250 mV and is internally limited to 3.35 V. This voltage is temperature compensated. This supply point can provide a current up to 3 mA typically. Its internal consumption stays low (a few 10 nA) as long as V_{DD} does not exceed 1.5 V.

An external voltage can be connected on V_{DD} with limited extra consumption on V_{DD} (typically 120 µA). This voltage source should not be lower than 3.5 V and higher than 6 V.

V_{BB} and V_{DD} can supply external circuits in the limits of currents provided either from the line or from ESI, taking into account the internal current consumption.

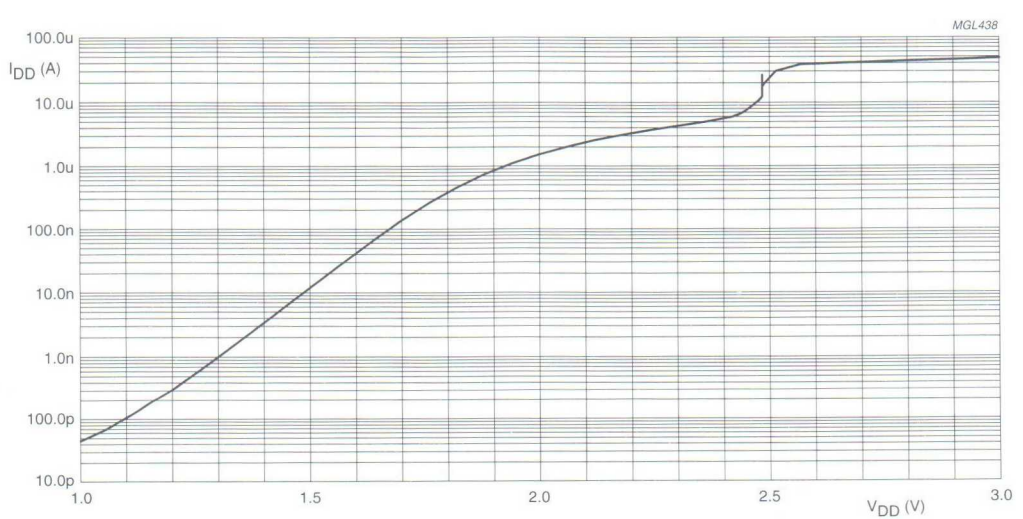


Fig.5 Current consumption on V_{DD}.

Supply for microphone (pins MICS and GNDTX)

The MICS output can be used as a supply for an electret microphone. Its voltage is equal to 2 V; it can source current up to 1 mA and has an output impedance equal to 200 Ω.

Low voltage behaviour

For line currents below 9 mA, the reference voltage is automatically adjusted to a lower value; the V_{BB} voltage follows the SLPE voltage with 250 mV difference. The excess current available for other purposes than DC biasing of the IC becomes small. In this low voltage area, the IC has limited performances.

When the V_{BB} voltage reaches 2.7 V, the V_{BB} detector of the receive dynamic limiter on LSAO acts continuously, discharging the DLC capacitor. In DC condition, the loudspeaker is automatically disabled below this voltage.

When V_{BB} becomes lower than 2.5 V, the TEA1097TV is forced in a low voltage mode whatever the levels on the logic inputs are. It is a speech mode with reduced performances only enabling the microphone channel (between the MIC inputs and LN) and the earpiece amplifier. These two channels are able to deliver signals for line currents as small as 3 mA. The HFC input is tied to GND sinking a current typically equal to 300 μA

Power-down mode (pins $\overline{PD}$ and AUXC)

To reduce consumption during dialling or register recall (flash), the TEA1097TV is provided with a power-down input ($\overline{PD}$). When the voltage on both pins $\overline{PD}$ and AUXC is LOW, the current consumption from V_{BB} and V_{DD} is reduced to 500 μA. Therefore a capacitor of 470 μF on V_{BB} is sufficient to power the TEA1097TV during pulse dialling or flash. The $\overline{PD}$ input has a pull-up structure, while AUXC has a pull-down structure. In this mode, the capacitor C_{REG} is internally disconnected.

Ringer mode (pins ESI, V_{BB}, AUXC and $\overline{PD}$)

The TEA1097TV is designed to be activated during the ringing phase. The loudspeaker amplifier can be used for the melody signal. The IC must be powered by an external supply on ESI, while applying a 'high' level on the logic input AUXC and a 'low' level on $\overline{PD}$ input. Only the HFRX input and the LSAO output are activated, in order to limit the current consumption. Some dynamic limitation is provided to prevent V_{BB} from being discharged below 2.7 V.

Transmit channels (pins MIC+, MIC−, DTMF, TXAUX, and LN)

Handset microphone amplifier (pins MIC+, MIC− and LN)

The TEA1097TV has symmetrical microphone inputs. The input impedance between MIC+ and MIC− is typically equal to 70 kΩ. The voltage gain between pins MIC+/MIC− and LN is set to 44.6 dB. Without limitation from the output, the microphone input stage can accommodate signals up to 18 mV (RMS) at room temperature for 2% of total harmonic distortion (THD). The microphone inputs are biased at one diode voltage.

Automatic gain control is provided for line loss compensation.

DTMF amplifier (pins DTMF, LN and RECO)

The TEA1097TV has an asymmetrical DTMF input. The input impedance between DTMF and GND is typically equal to 20 kΩ. The voltage gain between pins DTMF and LN is set to 25.7 dB. Without limitation from the output, the input stage can accommodate signals up to 180 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

When the DTMF amplifier is enabled, dialling tones may be sent on the line. These tones can be heard in the earpiece or in the loudspeaker at a low level. This is called the confidence tone. The voltage attenuation between pins DTMF and RECO is typically equal to −16.5 dB.

The DC biasing of this input is 0 V.

The automatic gain control has no effect on these channels.

Auxiliary Transmit amplifier (pins TXAUX and LN)

The TEA1097TV has an asymmetrical auxiliary input TXAUX. The input impedance between TXAUX and GND is typically equal to 20 kΩ. The voltage gain between pins TXAUX and LN is set to 12 dB. Without limitation from the output, the input stage can accommodate signals up to 1.2 V (RMS) at room temperature for 2% of total harmonic distortion (THD). The TXAUX input is biased at two diodes voltage.

Automatic gain control is provided for line loss compensation.

MICROPHONE MONITORING ON TXOUT (PINS MIC+, MIC– AND TXOUT)

The voltage gain between the microphone inputs MIC+/MIC– and the output TXOUT is set to 49.8 dB. This channel gives an image of the signal sent on the line while speaking in the handset microphone. Using an external circuitry, this signal can be used for several purposes such as sending dynamic limitation or anti-howling in a listening-in application. The TXOUT output is biased at two diodes voltage.

The automatic gain control has no effect on these channels.

Receive channels (pins IR, RAUX, RECO, GARX and QR)

RX AMPLIFIER (PINS IR AND RECO)

The receive amplifier has one input IR which is referred to the line. The input impedance between pins IR and LN is typically equal to 20 kΩ and the DC biasing between these pins is equal to one diode voltage. The gain between pins IR (referred to LN) and RECO is typically equal to 29.7 dB. Without limitation from the output, the input stage can accommodate signals up to 50 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

This receive amplifier has a rail-to-rail output RECO, which is designed for use with high ohmic (real) loads (larger than 5 kΩ). This output is biased at two diodes voltage.

Automatic gain control is provided for line loss compensation.

EARPIECE AMPLIFIER (PINS GARX AND QR)

The earpiece amplifier is an operational amplifier having its output (QR) and its inverting input (GARX) available. Its input signal comes, via a decoupling capacitor, from the receive RECO output. It is used in combination with two resistors to get the required gain or attenuation compared to the receive gain. It can be chosen between –3 dB and 15 dB.

Two external capacitors C_{GAR} (connected between GAR and QR) and C_{GARS} (connected between GAR and GND) ensure stability. The C_{GAR} capacitor provides a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAR} \times R_{E2}$. The relationship $C_{GARS} >= 10 \times C_{GAR}$ must be fulfilled.

The earpiece amplifier has a rail-to-rail output QR, biased at two diodes voltage. It is designed for use with low ohmic (real) loads (150 Ω) or capacitive loads (100 nF in series with 100 Ω).

When the amplifier is turned off, the signal present on the earpiece is equal to the ratio between the load on QR and $R_{E1} + R_{E2}$

AUXILIARY RECEIVE AMPLIFIER (PINS RAUX AND RECO)

The auxiliary receive amplifier has an asymmetrical input RAUX; it uses the RECO output. Its input impedance between pins RAUX and GND is typically equal to 20 kΩ. The voltage gain between pins RAUX and RECO is equal to –2.3 dB. Without any limitation from the output, the input stage can accommodate signals up to 0.9 V (RMS) at room temperature for 2% of total harmonic distortion (THD).

This auxiliary amplifier has a rail-to-rail output RECO, which is designed for use with high ohmic (real) loads (larger than 5 kΩ). This output is biased at two diodes voltage.

The automatic gain control has no effect on this channel.

Auxiliary amplifiers using AUXO (pins MIC+, MIC–, HFTX, IR and AUXO)

The TEA1097TV has an auxiliary output AUXO, biased at two diodes voltage. This output stage is a rail-to-rail one, designed for use with high ohmic (real) loads (larger than 5 kΩ). The AUXO output amplifier is used in three different channels, two transmit channels and one receive channel.

AUXILIARY AMPLIFIERS USING THE MICROPHONE INPUTS (PINS MIC+, MIC– AND AUXO)

The auxiliary transmit amplifier using the microphone MIC+/MIC– inputs has a gain of 25.2 dB referred to AUXO. Without limitation from the output, the input stage can accommodate signals up to 18 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

The automatic gain control has no effect on this channel.

AUXILIARY AMPLIFIERS USING HFTX (PINS HFTX AND AUXO)

The auxiliary transmit amplifier using the HFTX input has a gain of 15.2 dB referred to AUXO. The input stage is designed to achieve less than 2% at room temperature of total harmonic distortion (THD) for maximum output signal on AUXO.

The automatic gain control has no effect on this channel.

RX AMPLIFIER USING IR (PINS IR AND AUXO)

The auxiliary receive amplifier uses pin IR as input. The input is referred to LN and the DC biasing between these

two pins is one diode voltage. The voltage gain between the input IR (referred to LN) and the output AUXO is typically equal to 32.8 dB, which compensates typically the attenuation provided by the anti-sidetone network.

The input stage is designed to achieve less than 2% at room temperature of total harmonic distortion (THD) for maximum output signal on AUXO.

Automatic gain control is provided for line loss compensation.

AGC (pin AGC)

The TEA1097TV performs automatic line loss compensation, which fits well with the true line attenuation. The automatic gain control varies the gain of some transmit and receive amplifiers in accordance with the DC line current. The control range is 6.2 dB for $G_{v(MIC-LN)}$, $G_{v(IR-RECO)}$, $G_{v(IR-AUXO)}$ and 6.6dB for $G_{v(TXAUX-LN)}$, which corresponds approximately to a line length of 5.5 km for a 0.5 mm twisted-pair copper cable.

To enable this gain control, the pin AGC must be shorted to pin LN. The start current for compensation corresponds to a line current equal to typically 23 mA and the stop current to 57 mA. The start current can be increased by connecting an external resistor between pins AGC and LN. It can be increased up to 40 mA (using a resistor typically equal to 80 kΩ). The start and stop current will be maintained in a ratio equal to 2.5. By leaving the AGC pin opened, the gain control is disabled and no line loss compensation is performed.

Base microphone channel: pins TXIN, GATX, TXOUT and GNDTX (see Fig.6)

The TEA1097TV has an asymmetrical base microphone input TXIN with an input resistance of 20 kΩ. The DC biasing of the input is 0 V.

The output TXOUT is biased at two diodes voltage and has a current capability equal to 20 μA (RMS). The gain of the microphone amplifier (from pins TXIN to TXOUT) can be adjusted from 0 dB up to 31 dB to suit specific application requirements. The gain is proportional to the value of R_{GATX} and equals 15.2 dB with R_{GATX} = 30.1 kΩ. Without limitation from the output, the microphone input stage can accommodate signals up to 18 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

A capacitor can be connected in parallel with R_{GATX} to provide a first-order low-pass filter.

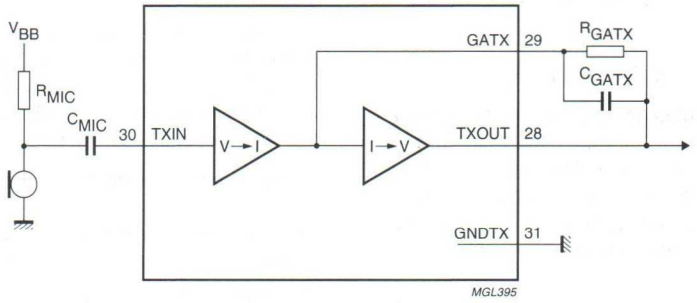


Fig.6 Base microphone channel.

Loudspeaker channel

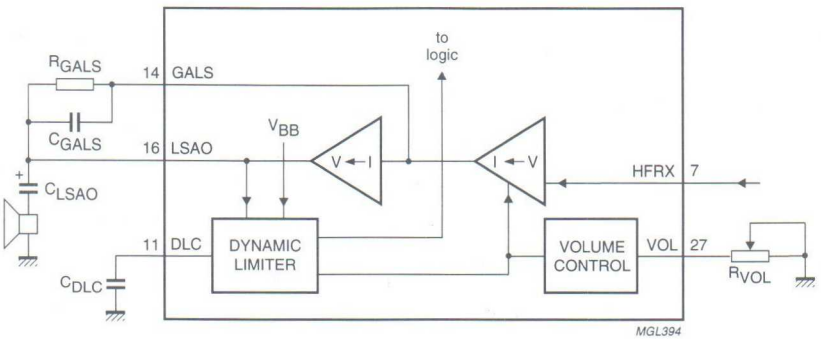


Fig.7 Loudspeaker channel.

LOUDSPEAKER AMPLIFIER: PINS HFRX, GALS AND LSAO

The TEA1097TV has an asymmetrical input for the loudspeaker amplifier with an input resistance of 20 kΩ between HFRX and GND. It is biased at two diodes voltage. The input stage can accommodate signals up to 580 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

The rail-to-rail output stage is designed to power a loudspeaker down to 8Ω connected as a single-ended load (between LSAO and GND). When the circuit is externally supplied, the maximum output power is typically equal to 280mW for 6V applied on ESI.

The gain of the loudspeaker amplifier can be adjusted from 0 dB up to 35 dB to suit specific application requirements. The gain from HFRX to LSAO is proportional to the value of R_{GALS} and equals 27.8 dB with R_{GALS} = 255 kΩ. A capacitor connected in parallel with R_{GALS} can be used to provide a first-order low-pass filter.

VOLUME CONTROL: PIN VOL

The loudspeaker amplifier gain can be adjusted with the potentiometer R_{VOL}. A linear potentiometer can be used to obtain logarithmic control of the gain at the loudspeaker amplifier. Each 1.9 kΩ increase of R_{VOL} results in a gain loss of 3 dB.

DYNAMIC LIMITER: PIN DLC

The dynamic limiter of the TEA1097TV prevents clipping of the loudspeaker output stage and protects the operation of the circuit when the supply voltage at V_{BB} falls below 2.7 V.

Hard clipping of the loudspeaker output stage is prevented by rapidly reducing the gain when the output stage starts to saturate. The time in which gain reduction is effected (clipping attack time) is approximately a few milliseconds. The circuit stays in the reduced gain mode until the peaks of the loudspeaker signals no longer cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time (typically 100 ms). Both attack and release times are proportional to the value of the capacitor C_{DLC}. The total harmonic distortion of the loudspeaker output stage, in reduced gain mode, stays below 1% up to 10 dB (minimum) of input voltage overdrive [providing V_{HFRX} is below 580 mV (RMS)].

When the supply voltage drops below an internal threshold voltage of 2.7 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). When the supply voltage exceeds 2.7 V, the gain of the loudspeaker amplifier is increased again.

By forcing a level lower than 0.2 V on pin DLC, the loudspeaker amplifier is muted.

Logic inputs

Table 1 Selection of transmit and receive channels for 12 different application modes

LOGIC INPUTS					FEATURES	APPLICATION EXAMPLES
$\overline{PD}$	HFC	$\overline{MUTT}$	$\overline{MUTR}$	AUXC		
0	X	X	X	1	HFRX to LSAO	ringer mode
0	X	X	X	0		flash, DC dialling
1	0	0	0	0	DTMF to LN; DTMF to RECO; QR and MICS are active	DTMF dialling (telephone set)
1	0	0	1	0	MIC to AUXO; RAUX to RECO; QR and MICS are active	cordless intercom with handset
1	0	1	1	0	MIC to LN; IR to RECO; IR to AUXO; MIC to TXOUT; QR and MICS are active	handset conversation (telephone set)
1	0	1	0	1	TXAUX to LN; IR to AUXO	conversation using auxiliary I/O; cordless: digital handsfree in mobile
1	1	0	1	1	RAUX to RECO; HFRX to LSAO	listening on the loudspeaker
1	1	0	0	1	TXAUX to LN; IR to AUXO; RAUX to RECO; HFRX to LSAO	answering machine: play and record messages; listen the recorded message on the loudspeaker
1	1	0	0	0	DTMF to LN; DTMF to RECO; HFRX to LSAO; QR and MICS are active	DTMF dialling in handsfree or group listening modes
1	1	1	0	1	TXAUX to LN; IR to AUXO; IR to RECO; HFRX to LSAO	answering machine: play and record messages while listening in the loudspeaker
1	1	0	1	0	TXIN to TXOUT; HFTX to AUXO; RAUX to RECO; HFRX to LSAO; MICS is active	cordless intercom with base
1	1	1	1	0	TXIN to TXOUT; TXAUX to LN; IR to RECO; IR to AUXO; HFRX to LSAO; MICS is active	digital handsfree conversation
1	1	1	0	0	MIC to LN; IR to RECO; IR to AUXO; HFRX to LSAO; MIC to TXOUT; QR and MICS are active	handset conversation with listening-in

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		GND – 0.4	12	V
	repetitive line voltage during switch-on or line interruption		GND – 0.4	13.2	V
V_{ESI}	positive continuous voltage on pin ESI		GND – 0.4	6	V
I_{ESI}	input current at pin ESI		–	140	mA
$V_{n(max)}$	maximum voltage on pins REG, SLPE, IR, AGC		GND – 0.4	V_{LN} + 0.4	V
	maximum voltage on all other pins except V_{DD}		GND – 0.4	V_{BB} + 0.4	V
I_{line}	maximum line current		–	130	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C	–	400	mW
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	115	K/W

CHARACTERISTICS

I_{line} = 15 mA; R_{slpe} = 20 Ω; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; AGC pin connected to LN; $\overline{PD}$ = HIGH; HFC = LOW; AUXC = LOW; $\overline{MUTT}$ = HIGH; $\overline{MUTR}$ = HIGH; measured according to test circuits; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
LINE INTERFACE AND INTERNAL SUPPLY (PINS LN, SLPE, REG AND V_{BB})						
V_{SLPE}	stabilized voltage between SLPE and GND	I_{line} = 15 mA	tbf	3.7	tbf	V
		I_{line} = 70 mA	tbf	6.15	tbf	V
V_{BB}	regulated supply voltage for internal circuitry	I_{line} = 15 mA	tbf	3.0	tbf	V
		I_{line} = 70 mA	tbf	5.35	tbf	V
I_{line}	line current for voltage increase					
	start current		–	18	–	mA
	stop current		–	46	–	mA
$\Delta V_{SLPE(T)}$	stabilized voltage variation with temperature referred to 25°C	T_{amb} = −25 to +75 °C	–	±60	–	mV
$\Delta V_{BB(T)}$	regulated voltage variation with temperature referred to 25°C	T_{amb} = −25 to +75 °C	–	±30	–	mV
I_{BB}	current available on pin V_{BB}					
	in speech mode		–	11.5	–	mA
	in digital handsfree application	HFC = HIGH	–	9.5	–	mA
V_{LN}	line voltage	I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	2.4	–	V
		I_{line} = 15 mA	tbf	4	tbf	V
		I_{line} = 130 mA	–	8.5	9.3	V
EXTERNAL SUPPLY (PIN ESI)						
V_{ESI}	external voltage supply allowed on pin ESI		–	–	6	V
I_{ESI}	input current on pin ESI	V_{ESI} = 3.5 V	–	3.1	–	mA
I_{ESI}	external current supply allowed on pin ESI		–	–	140	mA
V_{ESI}	voltage on pin ESI when supplied by a current source	I_{ESI} = 140 mA	–	6.6	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SUPPLY FOR PERIPHERALS (PIN V_{DD})						
V_{DD}	regulated supply voltage on V_{DD}	V_{BB} > 3.35 V + 0.25 V (typ.)	–	3.35	3.6	V
		otherwise	–	V_{BB} – 0.25	–	V
$\Delta V_{DD(T)}$	regulated voltage variation with temperature referred to 25°C	T_{amb} = –25 to +75°C; V_{BB} > 3.35 V + 0.25 V (typ.)	–	±30	–	mV
I_{DD}	current consumption on V_{DD}	in trickle mode; I_{line} = 0 mA; V_{DD} = 1.5 V; V_{BB} discharging	–	15	150	nA
		V_{DD} > 3.35 V	–	120	–	µA
$I_{DD(o)}$	current available for peripherals	V_{DD} = 3.35 V	–	–	–3	mA
SUPPLY FOR MICROPHONE (PIN MICS)						
V_{MICS}	supply voltage for a microphone		–	2	–	V
I_{MICS}	current available on MICS		–	–	–1	mA
POWER DOWN INPUT (PIN $\overline{PD}$)						
V_{IL}	low level input voltage		GND–0.4	–	GND+0.3	V
V_{IH}	high level input voltage		GND+1.8	–	V_{BB} +0.4	V
$I_{\overline{PD}}$	input current		–	–3	–6	µA
$I_{BB(PD)}$	current consumption on V_{BB} during power down phase	$\overline{PD}$ = LOW; AUXC = LOW	–	500	–	µA
RINGER MODE (PINS $\overline{PD}$, AUXC, HFRX, LSAO)						
I_{ESI}	input current on pin ESI	$\overline{PD}$ = LOW; AUXC = HIGH; V_{ESI} = 3.5 V	–	3.2	–	mA
$G_{v(HFRX-LSAO)}$	voltage gain from pin HFRX to LSAO	$\overline{PD}$ = LOW; AUXC = HIGH; V_{ESI} = 3.5 V V_{HFRX} = 20 mV (RMS); R_{GALS} = 255 kΩ	–	28	–	dB
Preamplifier inputs (pins MIC+, MIC–, IR, DTMF, TXIN, HFTX, HFRX, TXAUX, RAUX)						
$\lvert Z_{i(MIC)} \rvert$	input impedance					
	differential between pins MIC+ and MIC–		–	70	–	kΩ
	single-ended between pins MIC+/MIC– and GNDTX		–	35	–	kΩ
$\lvert Z_{i(IR)} \rvert$	input impedance between pins IR and LN		–	20	–	kΩ
$\lvert Z_{i(DTMF)} \rvert$	input impedance between pins DTMF and GND		–	20	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Z_{i(TXIN)} \rvert$	input impedance between pins TXIN and GNDTX		–	20	–	kΩ
$\lvert Z_{i(HFTX)} \rvert$	input impedance between pins HFTX and GND		–	20	–	kΩ
$\lvert Z_{i(HFRX)} \rvert$	input impedance between pins HFRX and GND		–	20	–	kΩ
$\lvert Z_{i(TXAUX)} \rvert$	input impedance between pins TXAUX and GND		–	20	–	kΩ
$\lvert Z_{i(RAUX)} \rvert$	input impedance between pins RAUX and GND		–	20	–	kΩ
TX amplifiers; see note 1						
TX HANDSET MICROPHONE AMPLIFIER (PINS MIC+, MIC– AND LN)						
$G_{v(MIC-LN)}$	voltage gain from pin MIC+/MIC– to LN	V_{MIC} = 5 mV (RMS)	tbf	44.6	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75 °C	–	±0.25	–	dB
CMRR	common mode rejection ratio		–	80	–	dB
THD	total harmonic distortion at LN	V_{LN} = 1.4 V (RMS)	–	–	2	%
		I_{line} = 4 mA; V_{LN} = 0.12 V (RMS)	–	–	10	%
$V_{no(LN)}$	noise output voltage at pin LN; pins MIC+/MIC– shorted through 200 Ω	psophometrically weighted (p53 curve)	–	–77.5	–	dBmp
$\Delta G_{v(m)}$	gain reduction if not activated	$\overline{HFC}$ = LOW; $\overline{MUTT}$ = LOW; $\overline{MUTR}$ = LOW; AUXC = LOW	60	80	–	dB
DTMF AMPLIFIER (PINS DTMF, LN AND RECO)						
$G_{v(DTMF-LN)}$	voltage gain from pin DTMF to LN	V_{DTMF} = 50 mV (RMS)	tbf	25.7	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75 °C	–	±0.25	–	dB
$\Delta G_{v(m)}$	gain reduction if not activated	HFC = LOW; MUTT = HIGH; MUTR = HIGH; AUXC = LOW	60	80	–	dB
$G_{v(DTMF-RECO)}$	voltage gain from pin DTMF to RECO	V_{DTMF} = 50 mV (RMS)	–	–16.5	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TX AUXILIARY AMPLIFIER USING TXAUX (PINS TXAUX AND LN)						
$G_{v(TXAUX-LN)}$	voltage gain from pin TXAUX to LN	V_{TXAUX} = 0.1 V (RMS)	tbf	12.6	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75 °C	–	±0.25	–	dB
THD	total harmonic distortion at LN	V_{LN} = 1.4 V (RMS)	–	–	2	%
$V_{TXAUX(rms)}$	Maximum input voltage at TXAUX (RMS value)	I_{line} = 70 mA; THD = 2%	1	1.2	–	V
$V_{no(LN)}$	noise output voltage at pin LN; pin TXAUX shorted to GND through 200 Ω in series with 10 μF	psophometrically weighted (p53 curve)	–	–80.5	–	dBmp
$\Delta G_{v(m)}$	gain reduction if not activated	HFC = LOW; $\overline{MUTT}$ = HIGH; $\overline{MUTR}$ = HIGH; AUXC = LOW	60	80	–	dB
MICROPHONE MONITORING ON TXOUT (PINS MIC+, MIC– AND TXOUT)						
$G_{v(MIC-TXOUT)}$	voltage gain from pin MIC+/MIC– to TXOUT	V_{MIC} = 2 mV (RMS)	tbf	49.8	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.1	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75 °C	–	±0.35	–	dB
RX amplifiers; see note 1						
RX AMPLIFIERS USING IR (PINS IR AND RECO)						
$G_{v(IR-RECO)}$	voltage gain from pin IR (referred to LN) to RECO	V_{IR} = 15 mV (RMS)	tbf	29.7	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
$V_{IR/LN(rms)}$	Maximum input voltage on IR (referred to LN) (RMS value)	I_{line} = 70 mA; THD = 2%	40	50	–	mV
$V_{RECO(rms)}$	Maximum output voltage on RECO (RMS value)	THD = 2%	0.75	0.9	–	V
$V_{no(RECO)(rms)}$	noise output voltage at pin RECO; pin IR is an open circuit (RMS value)	psophometrically weighted (p53 curve)	–	–88	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	HFC = LOW; $\overline{MUTT}$ = HIGH; $\overline{MUTR}$ = HIGH; AUXC = LOW	60	80	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RX EARPIECE AMPLIFIER (PINS GARX AND QR)						
$\Delta G_{v(QR)}$	gain voltage range between pins RECO and QR		−3	–	+15	dB
$V_{QR(rms)}$	maximum output voltage on QR (RMS value)	sine wave drive; R_L = 150 Ω; THD < 2%	0.75	0.9	–	V
$V_{no(QR)(rms)}$	noise output voltage at pin QR; pin IR is an open circuit (RMS value)	$G_{v(QR)}$ = 0 dB; psophometrically weighted (p53 curve)	–	−88	–	dBVp
RX AMPLIFIER USING RAUX (PINS RAUX AND RECO)						
$G_{v(RAUX-RECO)}$	voltage gain from pin RAUX to RECO	V_{RAUX} = 0.4 V (RMS)	tbf	−2.3	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = −25 to +75 °C	–	±0.25	–	dB
$V_{RAUX(rms)}$	Maximum input voltage on RAUX (RMS value)	THD = 2%	0.8	0.95	–	V
$V_{no(RECO)(rms)}$	noise output voltage at pin RECO; pin RAUX shorted to GND through 200 Ω in series with 10 µF (RMS value)	psophometrically weighted (p53 curve)	–	−100	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	HFC = LOW; $\overline{MUTT}$ = HIGH; $\overline{MUTR}$ = HIGH; AUXC = LOW	60	80	–	dB
Auxiliary amplifiers using AUXO; see note 1						
TX AUXILIARY AMPLIFIER USING MIC+ AND MIC− (PINS MIC+, MIC− AND AUXO)						
$G_{v(MIC-AUXO)}$	voltage gain from pin MIC+/MIC− to AUXO	V_{MIC} = 10 mV (RMS)	tbf	25.2	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.1	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = −25 to +75°C	–	±0.3	–	dB
$V_{MIC(rms)}$	Maximum input voltage on MIC+/MIC- (RMS value)	THD = 2%	–	18	-	mV
$V_{no(AUXO)}$	noise output voltage at pin AUXO; pins MIC+/MIC− shorted to GNDTX through 200 Ω in series with 10 µF (RMS value)	psophometrically weighted (p53 curve)	–	−91	–	dBVp

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TX AUXILIARY AMPLIFIER USING HFTX (PINS HFTX AND AUXO)						
$G_{v(HFTX-AUXO)}$	voltage gain from pin HFTX to AUXO	V_{HFTX} = 100 mV (RMS)	tbf	15.2	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.1	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.1	–	dB
$V_{AUXO(rms)}$	Maximum output voltage on AUXO (RMS value)	THD = 2%	0.8	0.9	–	V
$V_{no(AUXO)}$	noise output voltage at pin AUXO; pin HFTX shorted to GND through 200 Ω in series with 10 μF (RMS value)	psophometrically weighted (p53 curve)	–	–91.5	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	HFC = LOW; MUTT =LOW ; MUTR = HIGH; AUXC = LOW	60	80	–	dB
RX AMPLIFIER USING IR (PINS IR AND AUXO)						
$G_{v(IR-AUXO)}$	voltage gain from pin IR (referred to LN) to AUXO	V_{IR} = 8 mV (RMS)	tbf	32.8	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.1	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.3	–	dB
$V_{AUXO(rms)}$	Maximum output voltage on AUXO (RMS value)	THD = 2%	0.8	0.9	–	V
$V_{no(AUXO)(rms)}$	noise output voltage at pin AUXO; pin IR is an open circuit (RMS value)	psophometrically weighted (p53 curve)	–	–85	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	HFC = HIGH; MUTT = LOW; MUTR = HIGH; AUXC = HIGH	60	80	–	dB
Automatic Gain Control (pin AGC)						
$\Delta G_{v(trx)}$	gain control range for transmit and receive amplifiers affected by the AGC; with respect to I_{line} = 15 mA	I_{line} = 70 mA; $G_{v(MIC-LN)}$; $G_{v(IR-RECO)}$; $G_{v(IR-AUXO)}$	tbf	6.2	tbf	dB
		I_{line} = 70 mA; $G_{v(TXAUX-LN)}$	tbf	6.6	tbf	dB
I_{start}	highest line current for maximum gain		–	23	–	mA
I_{stop}	lowest line current for maximum gain		–	57	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logic inputs (pins HFC, AUXC, $\overline{\text{MUTT}}$, $\overline{\text{MUTR}}$)						
V_{IL}	low level input voltage		GND–0.4	–	GND+0.3	V
V_{IH}	high level input voltage		GND+1.8	–	V_{BB}+0.4	V
I	input current					
	for pins HFC and AUXC		–	3	6	µA
	for pins $\overline{\text{MUTT}}$ and $\overline{\text{MUTR}}$		–	–2.5	–6	µA
Base microphone amplifier (pins TXIN, TXOUT and GATX); see note 1						
$G_{v(TXIN-TXOUT)}$	voltage gain from pin TXIN to TXOUT	V_{TXIN} = 8 mV (RMS); R_{GATX} = 30.1 kΩ	–	15.2	–	dB
ΔG_v	voltage gain adjustment with R_{GATX}		–15	–	+16	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.1	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.15	–	dB
$V_{no(TXOUT)(rms)}$	noise output voltage at pin TXOUT; pin TXIN is shorted through 200 Ω in series with 10 µF to GNDTX (RMS value)	psophometrically weighted (p53 curve)	–	–101	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	HFC =HIGH; MUTT = LOW; MUTR = LOW; AUXC = LOW	60	80	–	dB
Loudspeaker amplifier (pins HFRX, LSAO, GALS and VOL); see note 1						
$G_{v(HFRX-LSAO)}$	voltage gain from pin HFRX to LSAO	V_{HFRX} = 20 mV (RMS); R_{GALS} = 255 kΩ	tbf	27.8	tbf	dB
ΔG_v	voltage gain adjustment with R_{GALS}		–28	–	+7	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.3	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
$\Delta G_{v(vol)}$	voltage gain variation related to ΔR_{VOL} = 1.9 kΩ		–	–3	–	dB
$V_{HFRX(rms)}$	maximum input voltage at pin HFRX (RMS value)	I_{line} = 70 mA; R_{GALS} = 33 kΩ; for 2% THD in the input stage	450	580	–	mV
$V_{no(LSAO)(rms)}$	noise output voltage at pin LSAO; pin HFRX is open circuit (RMS value)	psophometrically weighted (p53 curve)	–	–79	–	dBVp

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{LSAO(rms)}$	output voltage (RMS value)	I_{BB} = 0 mA; I_{DD} = 1 mA				
		I_{line} = 18 mA	–	0.9	–	V
		I_{line} = 30 mA	–	1.2	–	V
		I_{line} > 50 mA	–	1.6	–	V
$I_{LSAO(max)}$	maximum output current at pin LSAO (peak value)	external supply on ESI	150	300	–	mA
Dynamic limiter (pins LSAO and DLC); see note 1						
t_{att}	attack time	when V_{HFRX} jumps from 20 mV rms to 20 mV rms + 10 dB	–	–	5	ms
		when V_{BB} jumps below $V_{BB(th)}$	–	1	–	ms
t_{rel}	release time	when V_{HFRX} jumps from 20 mV rms + 10 dB to 20 mV rms	–	100	–	ms
THD	Total Harmonic Distortion at V_{HFRX} = 20 mV + 10 dB	$t > t_{att}$	–	0.1	2	%
$V_{BB(th)}$	V_{BB} limiter threshold		–	2.7	–	V
Mute Loudspeaker (pin DLC); see note 1						
$V_{DLC(th)}$	threshold voltage required on pin DLC to obtain mute receive condition		GND–0.4	–	GND+0.2	V
$I_{DLC(th)}$	threshold current sourced by pin DLC in mute receive condition	V_{DLC} = 0.2 V	–	100	–	µA
$\Delta G_{vrx(m)}$	voltage gain reduction in mute receive condition	V_{DLC} = 0.2 V	60	80	–	dB

Note

1. When the channel is enabled according to Table 1.

TEST AND APPLICATION INFORMATION

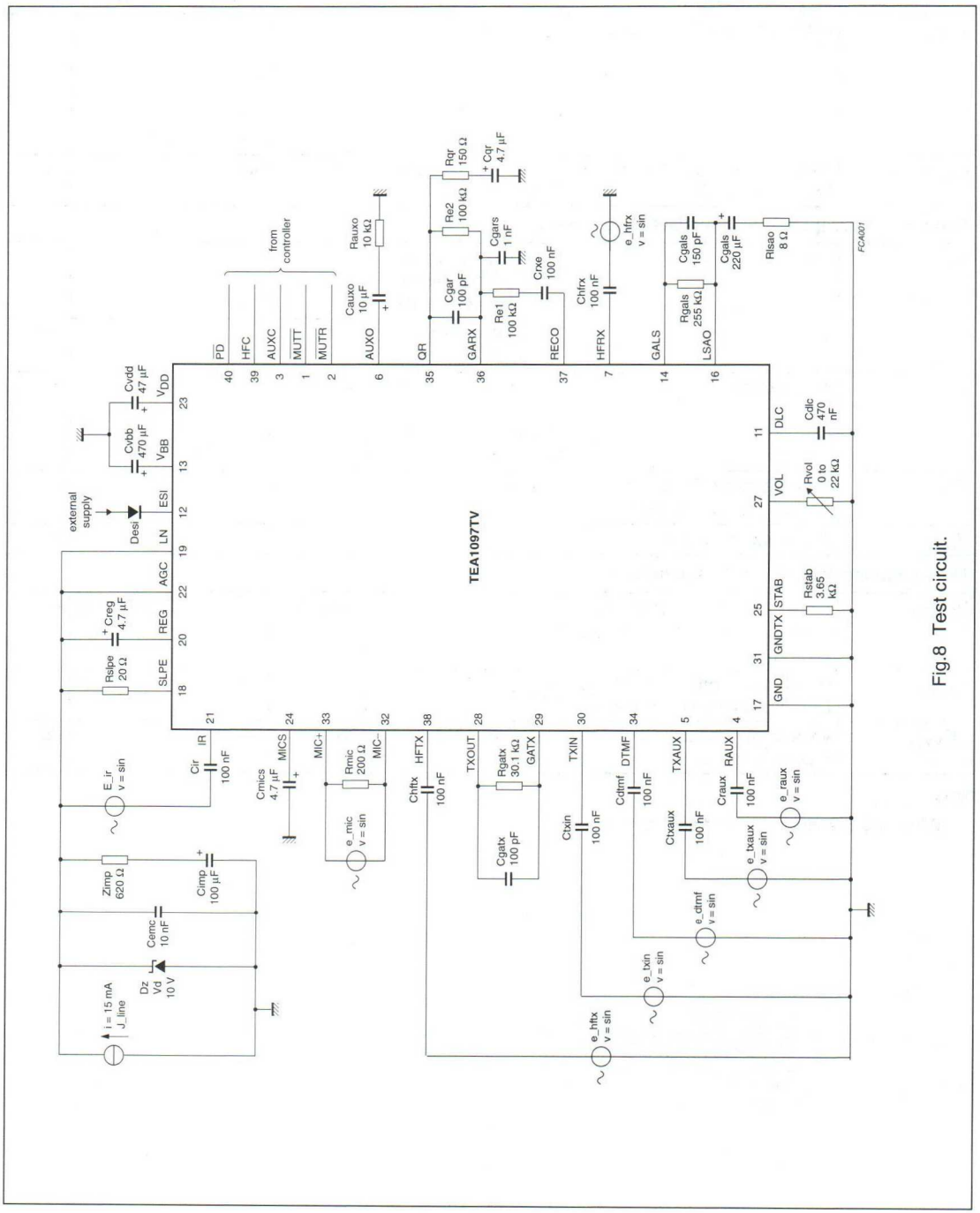


Fig.8 Test circuit.

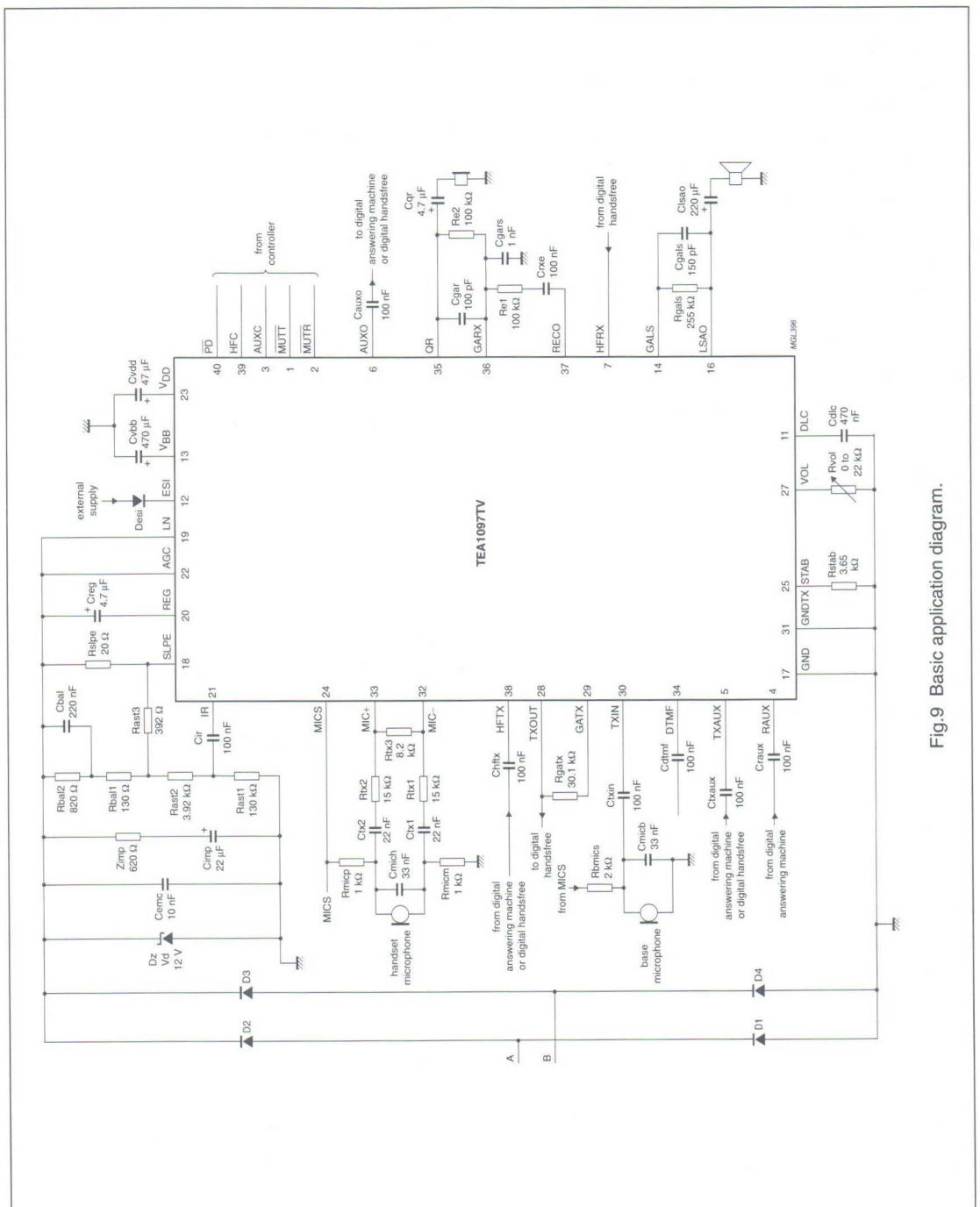


Fig.9 Basic application diagram.

Cordless telephone, answering machine line interface

UBA1707

FEATURES

Line interface

- Low DC line voltage; operates down to 1.2 V (excluding polarity guard)
- Voltage regulator with adjustable DC voltage
- DC mask for voltage and current regulation
- Line current limitation for protection
- Electronic hook switch control input
- Transmit amplifier with:
  - Symmetrical inputs
  - Fixed gain
  - Large signals handling capability.
- Receive amplifier with fixed gain
- Transmit and receive amplifiers AGC for line loss compensation.

Auxiliary amplifier

- Fixed gain.

Loudspeaker channel

- Dual inputs
- Rail-to-rail output stage for single-ended load drive
- High output current capability
- Dynamic limiter to prevent distortion
- Digital volume control
- Fixed maximum gain.

General purpose switches

- Three switches with open-collector.

3-wires serial bus interface

Allows to control:

- DC mask (voltage or current regulation)
- Receive amplifier mute function
- AGC:
  - On/off
  - Slope
  - I_{start} line current.
- Auxiliary amplifier mute function
- Loudspeaker channel:
  - Input selection
  - Volume setting
  - Dynamic limiter inhibition
  - Power-down mode.
- General purpose switches state
- Global power-down mode.

Supply

Operates with external supply voltage from 3.0 to 5.5 V.

APPLICATIONS

- Cordless base stations
- Answering machines
- Mains or battery-powered telephone sets.

GENERAL DESCRIPTION

The UBA1707 is a BiCMOS integrated circuit intended for use in mains-powered telecom terminals. It performs all speech and line interface functions, DC mask for voltage or current regulation and electronic hook switch control. The device includes an auxiliary amplifier, a loudspeaker channel and general purpose switches.

Most of the characteristics are programmable via a 3-wire serial bus interface.

ORDERING INFORMATION

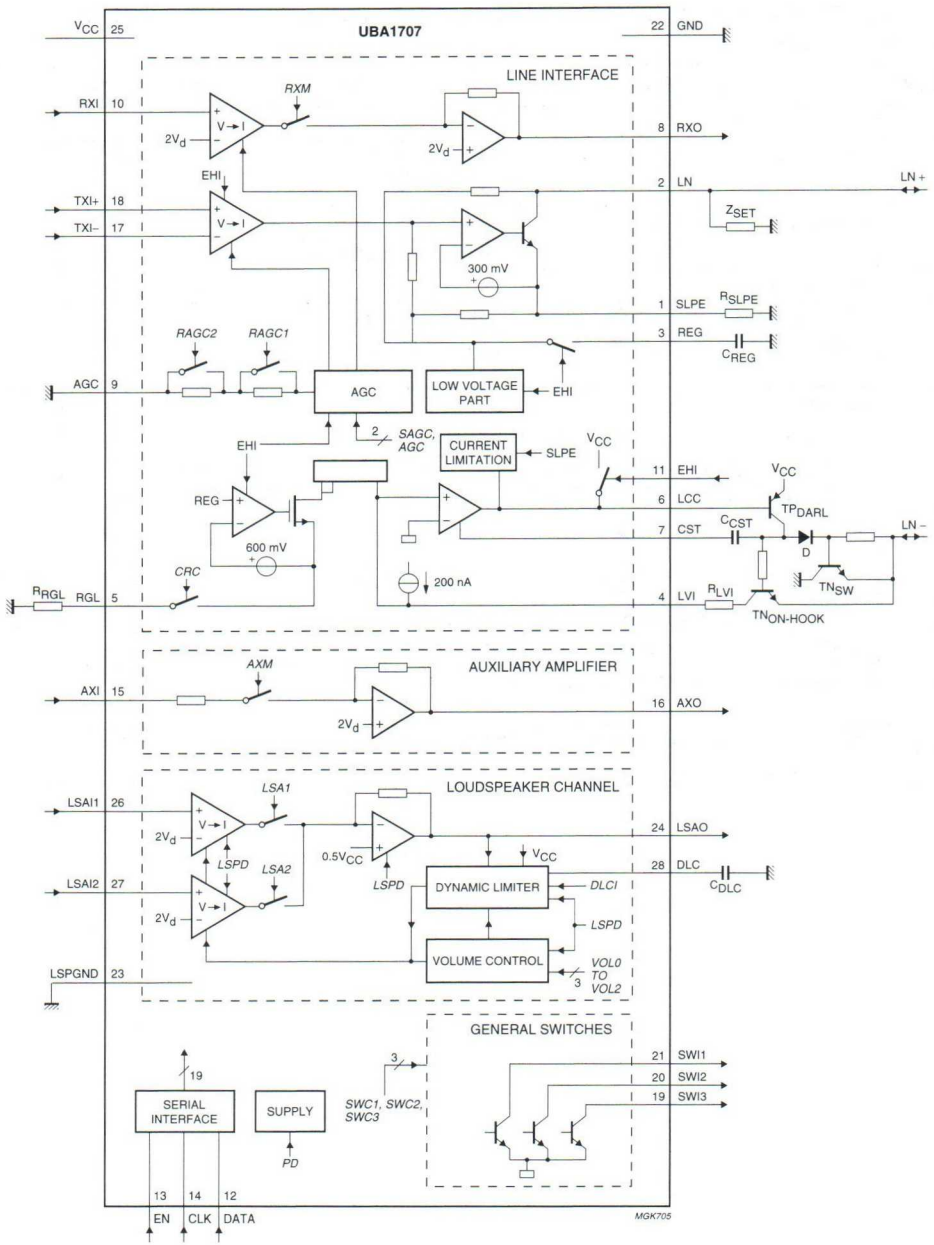
TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UBA1707T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
UBA1707TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

QUICK REFERENCE DATA

I_{line} = 15 mA; V_{CC} = 3.3 V; R_{SLPE} = 10 Ω; AGC pin connected to GND; Z_{line} = 600 Ω; Z_{SET} = 619 Ω; EHI = HIGH; f = 1 kHz; T_{amb} = 25 °C; bit AGC at logic 1, all other configuration bits at logic 0; measured in test circuit of Fig.17; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	operating voltage range		3.0	–	5.5	V
I_{CC}	current consumption from pin V_{CC}	normal operation; bit PD = 0	–	2.2	3.2	mA
		power-down mode; bit PD = 1	–	110	150	μA
I_{line}	line current operating range	normal operation	11	–	140	mA
		with reduced performance	3	–	11	mA
V_{LN}	DC line voltage		2.7	3.0	3.3	V
R_{REGC}	DC mask slope in current regulation mode	I_{line} > 35 mA (typical); R_{LVI} = 1 MΩ; R_{RGL} = 7.15 kΩ; bit CRC = 1	–	1.4	–	kΩ
$G_{v(trx)}$	voltage gain					
	transmit amplifier from TXI to LN	V_{TXI} = 50 mV (RMS)	10.7	11.7	12.7	dB
	receive amplifier from RXI to RXO	V_{RXI} = 2 mV (RMS)	36.9	37.9	38.9	dB
$\Delta G_{v(trx)}$	gain control range for transmit and receive amplifiers with respect to I_{line} = 15 mA	I_{line} = 90 mA	–	6.5	–	dB
$G_{v(AX)}$	voltage gain from AXI to AXO	V_{AXI} = 2 mV (RMS)	30.8	31.8	32.8	dB
$G_{v(LSA)}$	voltage gain from LSAI1 or LSAI2 to LSAO for maximum volume	V_{LSAI} = 8 mV (RMS); bits LSA1 = 1 and LSA2 = 1	26.5	28	29.5	dB
$\Delta G_{v(LSA)}$	voltage gain adjustment range for loudspeaker channel	bits (VOL0, VOL1 and VOL2) from (0, 0, 0) to (1, 1, 1)	–	21	–	dB
$\Delta G_{v(LSA)s}$	voltage gain adjustment step for loudspeaker channel	VOL0 from 0 to 1	–	3	–	dB

BLOCK DIAGRAM



Bit names are given in italics.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SLPE	1	connection for slope resistor
LN	2	positive line terminal
REG	3	line voltage regulator decoupling
LVI	4	negative line voltage sense input
RGL	5	reference for current regulation mode
LCC	6	line current control output
CST	7	input for stability capacitor
RXO	8	receive amplifier output
AGC	9	automatic gain control/line loss compensation adjustment
RXI	10	receiver amplifier input
EHI	11	electronic hook switch control input
DATA	12	serial bus data input
EN	13	programming serial bus enable input
CLK	14	serial bus clock input
AXI	15	auxiliary amplifier input
AXO	16	auxiliary amplifier output
TXI–	17	inverted transmit amplifier input
TXI+	18	non-inverted transmit amplifier input
SWI3	19	NPN open-collector output 3
SWI2	20	NPN open-collector output 2
SWI1	21	NPN open-collector output 1
GND	22	ground reference
LSPGND	23	ground reference for the loudspeaker amplifier
LSAO	24	loudspeaker amplifier output
V_{CC}	25	supply voltage
LSAI1	26	loudspeaker amplifier input 1
LSAI2	27	loudspeaker amplifier input 2
DLC	28	dynamic limiter timing adjustment

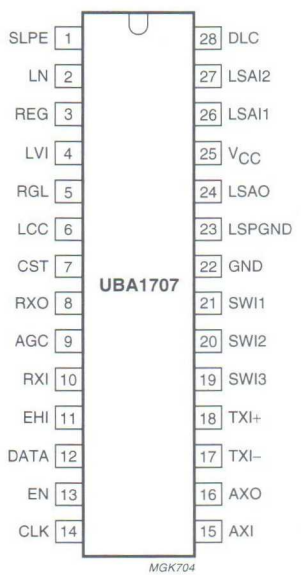


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supply (pins V_{CC} and GND; bits PD and LSPD)

The UBA1707 must be supplied with an external stabilized voltage source between pins V_{CC} and GND.

Pins GND and LSPGND must be connected together.

Without any signal, with the loudspeaker channel enabled at minimum volume and without any general purpose switch selected, the internal current consumption is 2.2 mA at V_{CC} = 3.3 V. Each selected switch (pins SWI1, SWI2, or SWI3) increases the current consumption by 600 µA.

The supply current can be reduced when the loudspeaker channel is not used by switching it off (bit LSPD at logic 1). The current consumption is then decreased by approximately 800 µA at minimum volume.

To drastically reduce current consumption, the UBA1707 is provided with a power-down mode controlled by bit PD. When bit PD is at logic 1, the current consumption from V_{CC} becomes 110 µA. In this mode, the serial interface is the only function which remains active.

Line interface

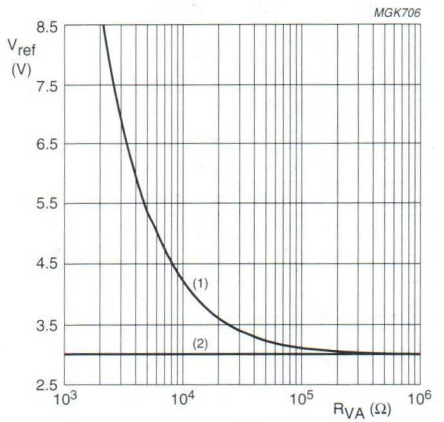
DC CHARACTERISTICS (PINS LN, SLPE, REG, CST, LVI, LCC, RGL AND GND; BIT CRC)

The IC generates a stabilized reference voltage (V_{ref}) between pins LN and SLPE. This reference voltage is equal to 2.9 V, is temperature compensated and can be adjusted by means of an external resistor (R_{VA}). It can be increased by connecting the R_{VA} resistor between pins REG and SLPE (see Fig.3).

The voltage at pin REG is used by the internal regulator to generate the stabilized reference voltage and is decoupled by a capacitor (C_{REG}) which is connected to GND. This capacitor, converted into an equivalent inductance (see Section "Set impedance") realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (Z_{SET} in the audio-frequency range). Figure 4 illustrates the reference voltage supply configuration. As can be seen from Fig.4, part of the line current flows into the Z_{SET} impedance network and is not sensed by the UBA1707. Therefore using the R_{VA} resistor to change value of the reference voltage will also modify all parameters related to the line current such as:

- The automatic gain control
- The DC mask management
- The low voltage area characteristics.

In the same way, changing the value of Z_{SET} also affects the characteristics. The IC has been optimized for V_{ref} = 2.9 V and Z_{SET} = 619 Ω.



(1) Influence of R_{VA} on V_{ref}.
(2) V_{ref} without influence of R_{VA}.

Fig.3 Reference voltage adjustment with R_{VA}.

The IC regulates the line voltage at pin LN which can be calculated as follows:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I_{ZSET} - I^* \cong I_{line} - I_{ZSET}$$

Where:

I_{line} = line current

I_{ZSET} = current flowing through Z_{SET}

I^* = current consumed between LN and GND (approximately 100 µA).

The preferred value for R_{SLPE} is 10 Ω. Changing R_{SLPE} will affect more than the DC characteristics; it also influences the transmit gain, the gain control characteristics, the sidetone level and the maximum output swing on the line.

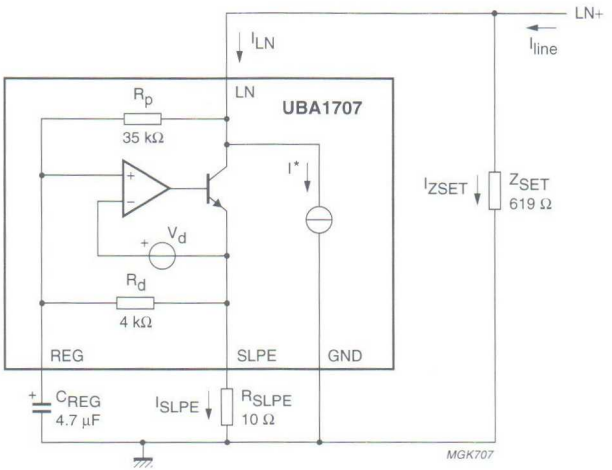


Fig.4 Reference voltage supply configuration.

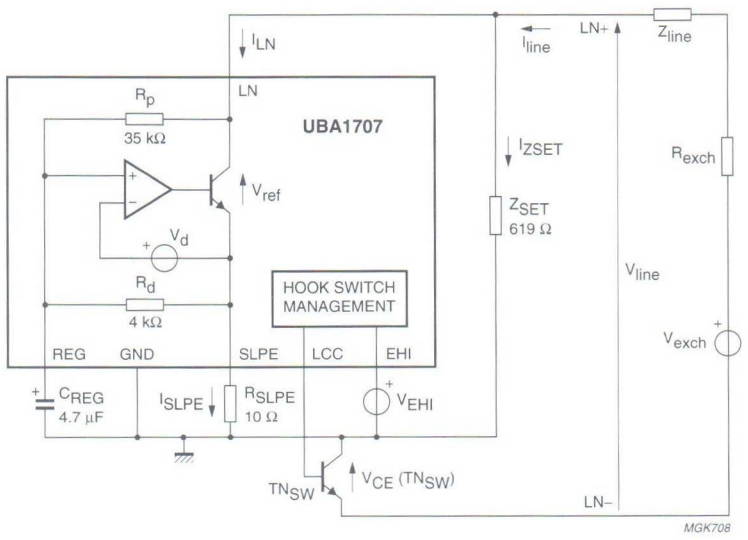


Fig.5 Line current settling simplified configuration.

The DC line current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistors of the telephone line (R_{line}) and the set (R_{SET}), the reference voltage (V_{ref}) and the voltage introduced by the transistor (TN_{SW}) used as line interrupter (see Fig.5). With a line current below I_{low} (8 mA with Z_{SET} = 619 Ω), the internal reference voltage (V_{ref}) is automatically adjusted to a lower value. This means that more sets can operate in parallel with DC line voltages (excluding the polarity guard) down to 1.2 V. At line current below I_{low}, the circuit has limited transmit and receive levels. This is called the low voltage area.

Figure 6 shows in more details how the UBA1707, in association with some external components, manages the line interrupter (TN_{SW} external transistor).

In on-hook conditions (voltage at pin EHI is LOW), the voltage at pin LCC is pulled-up to the supply voltage level (V_{CC}) to turn off the TP_{DARL} transistor. As a result, because of the R_{PLD} resistor, the TN_{SW} and $TN_{ON\text{-}HOOK}$ transistors are switched off. The $TN_{ON\text{-}HOOK}$ transistor disconnects the R_{LVI} resistor from the LN– line terminal in order to guarantee a high on-hook impedance.

In off-hook conditions (voltage at pin EHI is HIGH), an operational amplifier drives (at pin LCC) the base of TP_{DARL} which forms a current amplifier structure in association with TN_{SW}. The line current flows through TN_{SW} transistor. The $TN_{ON\text{-}HOOK}$ transistor is forced into deep saturation. A virtual ground is created at pin LVI because of the operational amplifier. A DC current (I_{LVI}) is sourced from pin LVI into the R_{LVI} resistor in order to generate a voltage source. Thus the voltage between pin GND and the negative line terminal (LN–) becomes:

$$V_{CE}\,(TN_{SW}) = R_{LVI} \times I_{LVI} + V_{CE}\,(TN_{ON\text{-}HOOK}) \cong R_{LVI} \times I_{LVI}$$

The voltage V_{line} between the line terminals LN+ and LN– can be calculated as follows:

$$V_{line} \cong V_{ref} + R_{SLPE} \times (I_{line} - I_{ZSET}) + V_{CE}\,(TN_{SW})$$

Where:

I_{line} = line current

I_{ZSET} = current flowing through Z_{SET}.

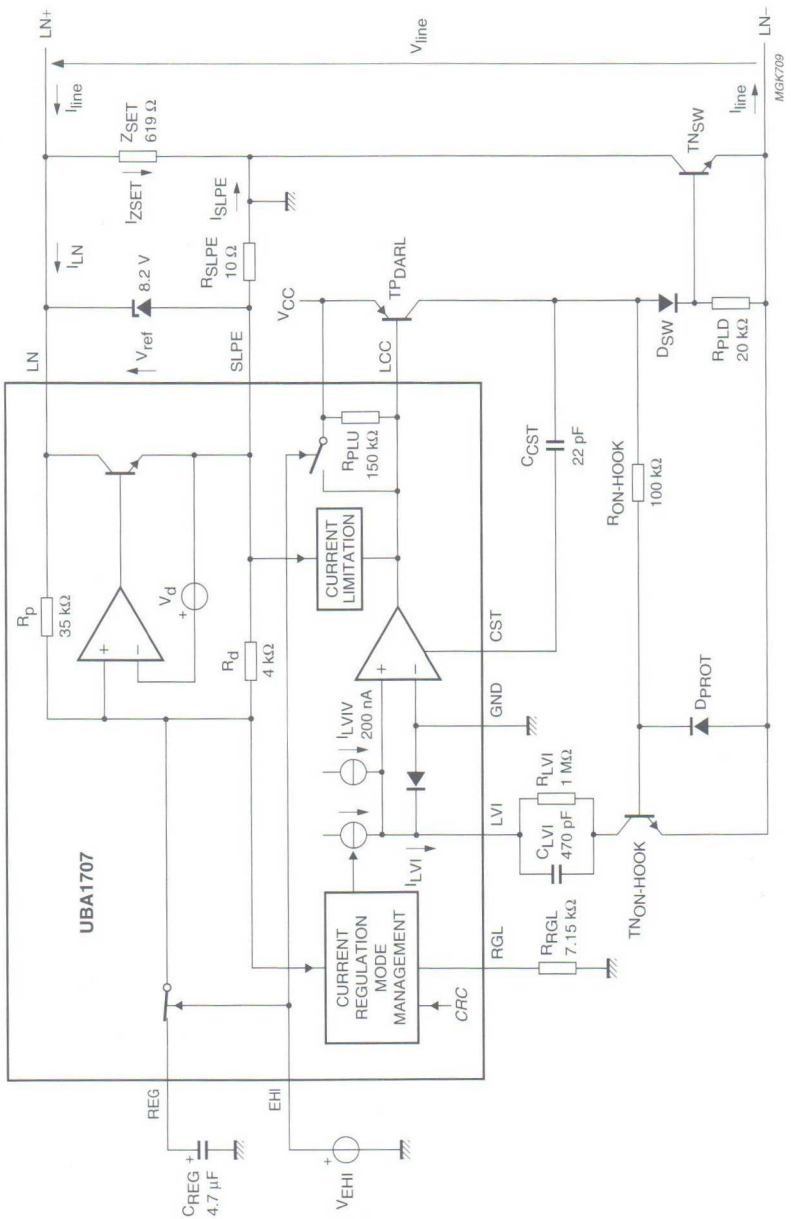
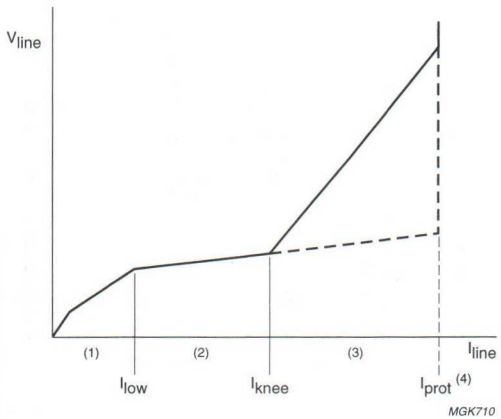


Fig.6 Line interrupter management and DC mask regulation configuration.

Bit names are given in italics.

The UBA1707 offers the possibility to choose two kinds of regulations for the DC characteristic between the line terminals LN+ and LN– (see Fig.7):

- Voltage regulation mode
- Current regulation mode.



(1) Low voltage area.
(2) Small slope (determined by R_{SLPE}).
(3) Small slope (dashed line; determined by R_{SLPE}) in voltage regulation mode.
High slope (full line; determined by R_{SLPE}, R_{LVI} and R_{RGL}) in current regulation mode.
(4) Current limitation.

Fig.7 General form of the DC mask as a function of regulation mode.

The regulation mode is selected by the bit CRC via the serial interface.

The DC mask regulation is realised by adjusting the DC voltage V_{CE} (TN_{SW}) between pin GND and line terminal LN– as a function of the line current.

Voltage regulation mode

In voltage regulation mode (bit CRC at logic 0), V_{CE} (TN_{SW}) voltage is fixed by means of a 200 nA DC constant current I_{LVIV} flowing through R_{LVI}.

Therefore V_{CE} (TN_{SW}) $\cong R_{LVI} \times I_{LVIV}$ = 200 mV in typical application (see Fig.18).

The slope $\Delta V_{line}/\Delta I_{line}$ of the V_{line}, I_{line} characteristic is $R_{REGV} \cong R_{SLPE}$.

Current regulation mode

In current regulation mode (bit CRC at logic 1), when the line current is lower than I_{knee} = 35 mA (with Z_{SET} = 619 Ω), V_{CE} (TN_{SW}) is fixed by means of a 200 nA DC constant current I_{LVIV} flowing through R_{LVI}. When the line current is higher than 35 mA, an additional current (proportional to the line current) flows through R_{LVI}. As a result, TN_{SW} works as a DC voltage source increasing with the line current. V_{CE} (TN_{SW}) can be calculated as follows:

$$V_{CE}(TN_{SW}) \cong R_{LVI} \times \left(\frac{R_{SLPE}}{R_{RGL}} \times (I_{line} - I_{knee}) + I_{LVIV} \right)$$

Where:

I_{line} = line current

R_{RGL} = resistor connected at pin RGL.

The slope $\Delta V_{line}/\Delta I_{line}$ of the V_{line}, I_{line} characteristic is determined by the ratio of resistors connected at pins SLPE, LVI and RGL, as follows:

$$R_{REGC} \cong R_{SLPE} + R_{LVI} \times \frac{R_{SLPE}}{R_{RGL}} = 1400\ \Omega \text{ in typical}$$

application (see Fig.18).

Current limitation

Whatever the selected mode is, the line current is limited to approximately 145 mA. This current is sensed on SLPE, for this purpose the external zener diode must be connected between pins LN and SLPE. The speech function no longer operates in this condition.

Electronic hook switch control (pin EHI)

The electronic hook switch input (EHI) controls the state of TP_{DARL} transistor. When the voltage applied at pin EHI is LOW, TP_{DARL} transistor is turned off. Voltage at pin LCC is pulled up to supply voltage (V_{CC}). TN_{SW} and $TN_{ON\text{-}HOOK}$ transistors are also turned off by means of a pull-down resistor (R_{PLD}). When the voltage applied at pin EHI is HIGH, TP_{DARL} transistor is driven by the operational amplifier at pin LCC and the regulation mode selected is operating. An internal 165 kΩ pull-up resistor is connected between pins LCC and V_{CC}.

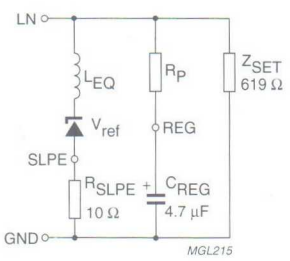
The EHI input can also be used for pulse dialling or register recall (timed loop break). During line breaks (voltage at pin EHI is LOW or open-circuit), the voltage regulator is switched off and the capacitor at pin REG is internally disconnected to prevent its discharge. As a result, the voltage stabilizer will have negligible switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall.

When the UBA1707 is in power-down mode (bit PD at logic 1), the TP_{DARL} transistor is forced to be turned off whatever the voltage applied at pin EHI.

Set impedance

In the audio frequency range, the dynamic impedance between pins LN and GND (illustrated in Fig.8) is mainly determined by the Z_{SET} impedance.

The impedance introduced by the external TN_{SW} transistor connected between pin GND and the negative line terminal (LN–) is negligible.



$L_{eq} = C_{REG} \times R_{SLPE} \times R_P$
R_P = internal resistance = 35 kΩ.

Fig.8 Equivalent impedance between LN and GND.

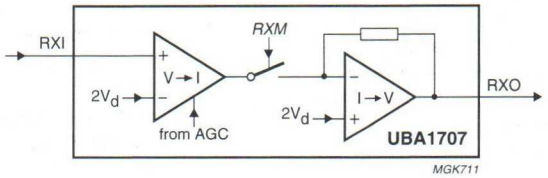
Transmit amplifier (pins TXI+ and TXI–)

The UBA1707 has symmetrical transmit inputs TXI+ and TXI–. The input impedance between pins TXI+ or TXI– and GND is 21 kΩ. The voltage gain from pins TXI+ or TXI– to pin LN is set at 11.7 dB with 600 Ω line load (Z_{line}) and 619 Ω set impedance. The inputs are biased at $2 \times V_d \cong 1.4$ V, with V_d representing the diode voltage. Automatic gain control is provided on this amplifier for line loss compensation.

Receive amplifier (pins RXI and RXO; bit RXM)

The receive amplifier (see Fig.9) has one input (RXI) and one output (RXO). The input impedance between pins RXI and GND is 21 kΩ. The rail-to-rail output stage is designed to drive a 500 µA peak current. The output impedance at pin RXO is approximately 100 Ω.

The voltage gain from pin RXI to pin RXO is set at 37.9 dB. This gain value compensates typically the attenuation of the anti-sidetone network (see Fig.10). The output as well as the input are biased at $2 \times V_d \cong 1.4$ V. Automatic gain control is provided on this amplifier for line loss compensation. This amplifier can be muted by activating the receive mute function (bit RXM at logic 1).



Bit names are given in italics.

Fig.9 Receive amplifier.

SIDETONE SUPPRESSION

The UBA1707 anti-sidetone network comprising $Z_{SET}//Z_{line}$, R_{ast1}, R_{ast2}, R_{ast3}, R_{SLPE} and Z_{bal} (see Fig.10) suppresses the transmitted signal in the received signal. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = Z_{SET} \times (R_{ast2} + R_{ast3})$$

$$k = \frac{(R_{ast2} \times (R_{ast3} + R_{SLPE}))}{(R_{ast1} \times R_{SLPE})}$$

$$Z_{bal} = k \times Z_{line}$$

The scale factor 'k' is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice, Z_{line} varies considerably with the line type and the line length.

Therefore, the value chosen for Z_{bal} should be for an average line length which gives satisfactory sidetone suppression with short and long lines.

The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

The anti-sidetone network for the UBA1707 (see Fig.18) attenuates the receiving signal from the line by 38 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. A Wheatstone bridge configuration (see Fig.11) may also be used.

More information on the balancing of an anti-sidetone bridge can be obtained in our publication *"Applications Handbook for Wired Telecom Systems, IC03b"*, order number 9397 750 00811.

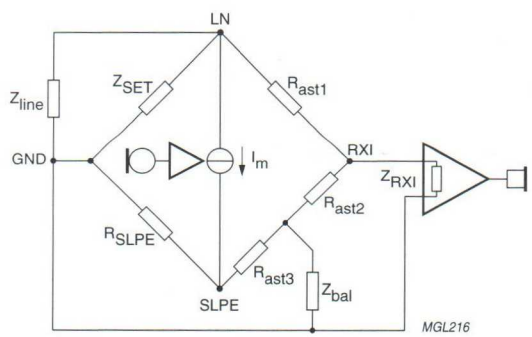


Fig.10 Equivalent circuit of UBA1707 anti-sidetone bridge.

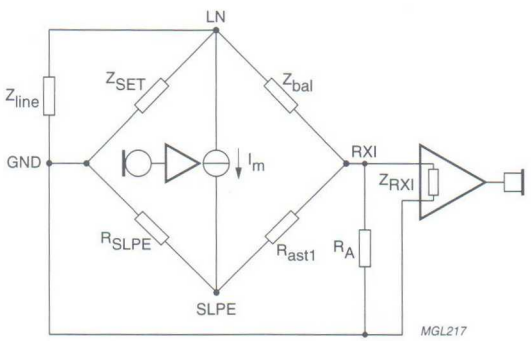


Fig.11 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

AUTOMATIC GAIN CONTROL (PIN AGC; BITS RAGC1, RAGC2, SAGC AND AGC)

The UBA1707 performs automatic line loss compensation. The automatic gain control varies the gain of the transmit amplifier and the gain of the receive amplifier in accordance with the DC line current. The control range is 6.5 dB (which roughly corresponds to a line length of 5.5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km).

When the line current is greater than I_{stop}, the voltage gains are minimum. When the line current is less than I_{start}, the voltage gains are maximum. When the AGC pin is connected to pin GND, the start line current (I_{start}) can be chosen between 22.5 and 29.5 mA via bits RAGC1 and RAGC2 through the serial interface. Two values for the I_{stop}/I_{start} ratio (slope of the AGC) are possible via the bit SAGC through the serial interface. When bit SAGC is at logic 0 then $I_{stop} = 2.7 \times I_{start}$ (optimized for voltage regulation mode). When SAGC is at logic 1 then $I_{stop} = 1.9 \times I_{start}$ (optimized for current regulation mode).

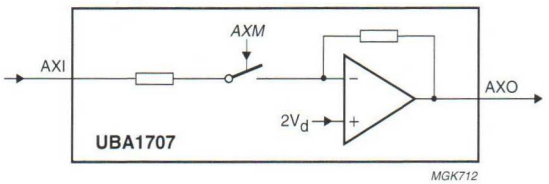
An external resistor R_{AGC} (connected between pins GND and AGC) enables the I_{start} and I_{stop} line currents to be increased (the ratio between I_{start} and I_{stop} is not affected by this external resistor). So internal and external adjustments of the automatic gain control allow optimization of the IC for many configurations of exchange supply voltage and feeding bridge resistance. Part of the line current flows into the Z_{SET} impedance network. The IC has been optimized for $Z_{SET} = 619\ \Omega$. Changing this 619 Ω value slightly modifies I_{stop} and I_{start} line currents as well as the value of the two AGC slopes.

The automatic gain control function can be disabled by setting the AGC bit to logic 0 via the serial interface or when pin AGC is left open-circuit. In this case both of the voltage gains are maximum.

Auxiliary amplifier (pins AXI and AXO; bit AXM)

The auxiliary amplifier (see Fig.12) has one input (AXI) and one output (AXO). The input impedance between pins AXI and GND is 3.8 kΩ. The rail-to-rail output stage is designed to drive a 500 μA peak current. The output impedance at pin AXO is approximately 100 Ω.

The output as well as the input are biased at $2 \times V_d \cong 1.4$ V DC voltage. The voltage gain from pin AXI to pin AXO is set at 31.8 dB.The amplifier can be muted by setting bit AXM at logic 1 via the serial interface. In this case, the input impedance between pins AXI and GND is infinite.



Bit names are given in italics.

Fig.12 Auxiliary amplifier.

Loudspeaker channel (see Fig.13)

LOUDSPEAKER AMPLIFIER (PINS LSAI1, LSAI2, LSAO AND LSPGND; BITS LSPD, LSA1 AND LSA2)

The loudspeaker amplifier has two symmetrical inputs LSAI1 and LSAI2 selectable independently by the bits LSA1 and LSA2 respectively. The input impedance between pins LSAI1or LSAI2 and GND is typically 21 kΩ. Each of these two inputs stages can accommodate signals up to 500 mV (RMS) at room temperature for less than 2% of Total Harmonic Distortion (THD) at minimum voltage gain.

The inputs are biased at $2 \times V_d \cong 1.4$ V DC voltage (whatever the state of bits LSA1 and LSA2).

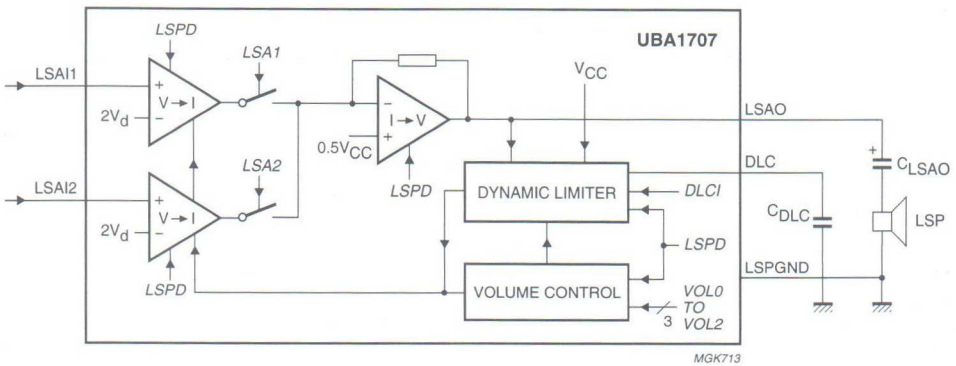
The rail-to-rail output stage is designed to power a loudspeaker connected as a single-ended load (between pins LSAO and LSPGND). The output LSAO is able to drive at least a 150 mA peak current.

As a result, it can drive loudspeaker loads down to 8 Ω at V_{CC} = 4.0 V and 16 Ω at V_{CC} = 5.5 V. The output is biased at $\frac{1}{2}V_{CC}$. Its output voltage capability is specified for continuous wave drive and depends on the value of V_{CC}.

In order to avoid crosstalk from the loudspeaker to other amplifiers, the loudspeaker current flows via pin LSPGND. This pin must be externally connected to pin GND.

The nominal value of the voltage gain for maximum volume from pins LSAI1 or LSAI2 to pin LSAO is set at 28 dB.

This amplifier is no longer supplied by setting the LSPD bit at logic 1 via the serial interface.



Bit names are given in italics.

Fig.13 Loudspeaker channel.

Dynamic limiter (pin DLC; bit DLCI)

The dynamic limiter of the UBA1707 prevents clipping of the loudspeaker output stage and protects the operation of the circuit when the supply voltage at V_{CC} falls below 2.7 V.

Hard clipping of the loudspeaker output stage is prevented by rapidly reducing the gain when the output stage starts to saturate. The time in which gain reduction is effected (clipping attack time) is approximately a few milliseconds. The circuit stays in the reduced gain mode until the peaks of the loudspeaker signals no longer cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time (typically 250 ms). Both attack and release times are proportional to the value of the capacitor C_{DLC}. The total harmonic distortion of the loudspeaker output stage, in reduced gain mode, stays below 5% up to 10 dB (minimum) of input voltage overdrive [providing V_{LSAI} is below 500 mV (RMS)].

When the supply voltage drops below an internal threshold voltage of 2.7 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). When the supply voltage exceeds 2.7 V, the gain of the loudspeaker amplifier is increased again.

The hard clipping of the dynamic limiter can be inhibited by setting the DLCI bit at logic 1, via the serial interface.

The dynamic limiter is no longer supplied by setting the LSPD bit at logic 1. In this case, the C_{DLC} capacitor charge is maintained to allow the gain of the loudspeaker amplifier to return to its nominal value as soon as the loudspeaker channel is supplied again.

Volume control (bits VOL0, VOL1 and VOL2)

The loudspeaker amplifier voltage gain can be reduced in steps of 3 dB via the serial interface (via bits VOL0, VOL1 and VOL2). These bits provide 7 steps of voltage gain adjustment. The voltage gain is maximum when all bits are at logic 1 and is reduced by 21 dB when all bits are at logic 0.

General purpose switches (pins SWI1, SWI2 and SWI3; bits SWC1, SWC2 and SWC3)

The UBA1707 is equipped with 3 general purpose open-collector switches which short the pins SWI1, SWI2 and SWI3 to ground. They are respectively controlled by bits SWC1, SWC2 and SWC3 and have an operating voltage limited to 12 V. The outputs have to be current biased.

For a bias current between 2 and 20 mA, the AC impedance is 30 Ω maximum.

Serial interface (pins DATA, CLK and EN)

A simple 3-wire unidirectional serial bus is used to program the circuit. The 3 wires of the bus are EN, CLK and DATA. The data sent to the device is loaded in bursts framed by EN. Programming clock edges (falling edges) and their appropriate data bits are ignored until EN goes active HIGH. The programmed information is loaded into the addressed register when EN returns inactive (LOW) or left open-circuit.

During normal operation, EN should be kept LOW. Only the last 8 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored and no check is made on the number of clock pulses. It can always capture new programming data even during global power-down (bit PD at logic 1).

Data is entered with the most significant bit first. The leading 6 bits make up the data field (bits D0 to D5) while the trailing 2 bits are the address field (bits ADO and AD1). The first bit entered is D5, the last bit AD0. This organisation allows to send only the number of bits of the addressed register.

Figure 16 shows the serial timing diagram. Table 1 gives the list of registers.

When the supply voltage V_{CC} drops below 2.5 V, all register files are set in the initial state (see Table 1) defined by the power-up reset. At start-up, the circuit is in power-down mode.

In the event that the IC is used in a noisy environment, it is advised to periodically refresh the content of registers.

Table 1 Register description

BIT NAME	FUNCTION	POLARITY	DATA	ADDRESS	STATE AT POWER-UP RESET
Register 0: general purpose switches state and DC mask regulation mode					
SWC1	SWI1 output connection	0: SWI1 switched-off	D0	(AD1, AD0) = (0,0)	0
		1: SWI1 switched-on			
SWC2	SWI2 output connection	0: SWI2 switched-off	D1		0
		1: SWI2 switched-on			
SWC3	SWI3 output connection	0: SWI3 switched-off	D2		0
		1: SWI3 switched-on			
un	unused	must be set to logic 0	D3		0
CRC	current regulation mode	0: voltage regulation	D4		0
		1: current regulation			
Register 1: automatic gain control					
RAGC1	AGC range selection 1		D0	(AD1, AD0) = (0,1)	0
RAGC2	AGC range selection 2		D1		0
SAGC	AGC slope selection	0: 2.7 type slope; note 1	D2		0
		1: 1.9 type slope; note 1			
AGC	line loss compensation mode	0: AGC inhibited	D3		0
		1: AGC enabled			
Register 2: loudspeaker channel					
LSA1	loudspeaker channel input 1 selection	0: LSAI1 unselected	D0	(AD1, AD0) = (1,0)	0
		1: LSAI1 selected			
LSA2	loudspeaker channel input 2 selection	0: LSAI2 unselected	D1		0
		1: LSAI2 selected			
LSPD	loudspeaker channel power-down	0: channel on	D2		0
		1: channel in power-down			
VOL0	volume control (least significant bit)		D3		0
VOL1	volume control		D4		0
VOL2	volume control (most significant bit)		D5		0
Register 3: mute functions and power-down					
AXM	auxiliary amplifier mute	0: amplifier enabled	D0	(AD1, AD0) = (1,1)	0
		1: amplifier muted			
RXM	receive amplifier mute	0: amplifier enabled	D1		0
		1: amplifier muted			
PD	reduced consumption mode	0: normal operating mode	D2		1
		1: power-down mode			
DLCI	dynamic limiter inhibit	0: limiter enabled	D3		0
		1: limiter inhibited			

Note

1. See Section "Automatic gain control (pin AGC; bits RAGC1, RAGC2, SAGC and AGC)".

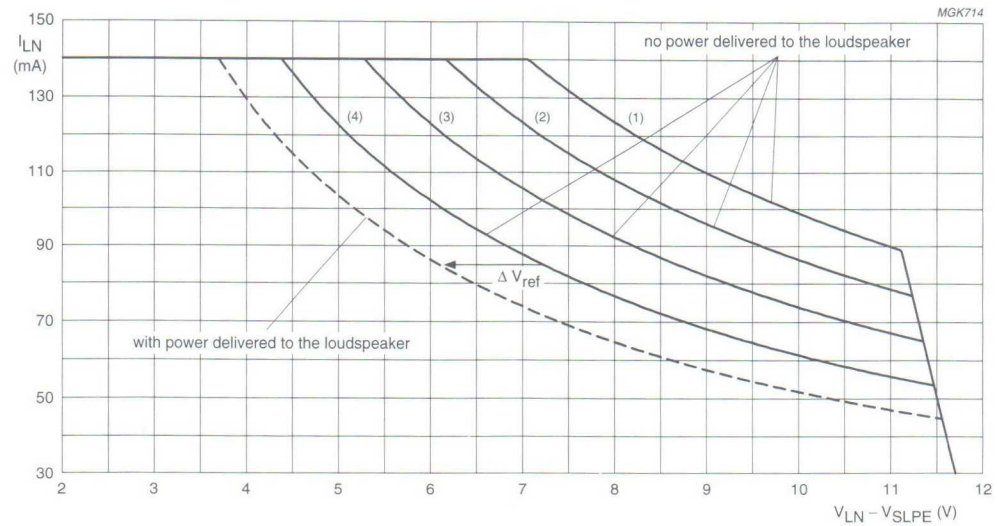
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage on pin V_{CC}		GND – 0.4	5.5	V
V_{LN}	positive continuous line voltage on pin LN		GND – 0.4	12.0	V
	repetitive line voltage during switch-on or line interruption		GND – 0.4	13.2	V
V_{SWIn}	voltage on pins SWI1, SWI2, and SWI3	continuous	GND – 0.4	12.0	V
		during switching	GND – 0.4	13.2	V
$V_{n(max)}$	maximum voltage on all other pins		GND – 0.4	V_{CC} + 0.4	V
I_{LN}	current sunk by pin LN	see Figs 14 and 15	–	150	mA
I_{SWIn}	continuous current sunk by pins SWI1, SWI2, and SWI3	bit SWCn = 1	–	20	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C; see Figs 14 and 15			
	UBA1707T		–	625	mW
	UBA1707TS		–	416	mW
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air		
	UBA1707T		70	K/W
	UBA1707TS		104	K/W



LINE	T_{amb} (°C)	P_{tot} (mW)
(1)	45	1000
(2)	55	875
(3)	65	750
(4)	75	625

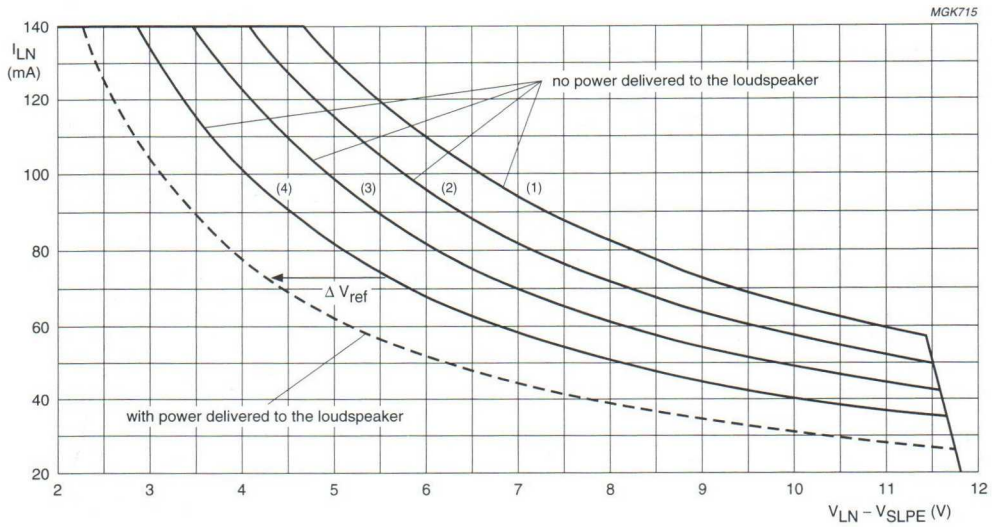
The line current value can be calculated from I_{LN} value as follows:

$$I_{line} = \frac{I_{LN} \times (R_{SET} + R_{SLPE}) + V_{LN} - V_{SLPE}}{R_{SET}}$$ where R_{SET} is the resistive part of Z_{SET}.

When power is delivered to a loudspeaker with R_L impedance, the curves must be shifted to the left by:

$$\Delta V_{ref} = \frac{V_{CC}^2}{2 \times \pi^2 \times R_L \times I_{LN}}$$ with maximum power dissipated by the loudspeaker amplifier (dotted line given for V_{CC} = 5.5 V, R_L = 16 Ω).

Fig.14 Safe operating area (UBA1707T).



LINE	T_{amb} (°C)	P_{tot} (mW)
(1)	45	666
(2)	55	583
(3)	65	500
(4)	75	416

The line current value can be calculated from I_{LN} value as follows:

$$I_{line} = \frac{I_{LN} \times (R_{SET} + R_{SLPE}) + V_{LN} - V_{SLPE}}{R_{SET}}$$ where R_{SET} is the resistive part of Z_{SET}.

When power is delivered to a loudspeaker with R_L impedance, the curves must be shifted to the left by:

$$\Delta V_{ref} = \frac{V_{CC}^2}{2 \times \pi^2 \times R_L \times I_{LN}}$$ with maximum power dissipated by the loudspeaker amplifier (dotted line given for V_{CC} = 5.5 V, R_L = 16 Ω).

Fig.15 Safe operating area (UBA1707TS).

CHARACTERISTICS

I_{line} = 15 mA; V_{CC} = 3.3 V; R_{SLPE} = 10 Ω; AGC pin connected to GND; Z_{line} = 600 Ω; Z_{SET} = 619 Ω; EHI = HIGH; f = 1 kHz; T_{amb} = 25 °C; bit AGC at logic 1, all other configuration bits at logic 0; measured in test circuit of Fig.17; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins V_{CC} and GND; bit PD)						
V_{CC}	operating supply voltage		3.0	–	5.5	V
I_{CC}	current consumption from pin V_{CC}		–	2.2	3.2	mA
$I_{CC(pd)}$	current consumption from pin V_{CC} in power-down mode	bit PD = 1	–	110	150	μA
Line interface (pins LN, SLPE and REG)						
DC CHARACTERISTICS						
V_{ref}	stabilized voltage between pins LN and SLPE	I_{line} = 11 to 140 mA	2.6	2.9	3.2	V
V_{LN}	DC line voltage between pins LN and GND	I_{line} = 2 mA	–	1.2	–	V
		I_{line} = 4 mA	–	1.8	–	V
		I_{line} = 15 mA	2.7	3.0	3.3	V
		I_{line} = 140 mA	–	4.35	–	V
$V_{LN(Rext)}$	DC line voltage between pins LN and GND with an external resistor R_{VA}	$R_{VA(SLPE-REG)}$ = 8 kΩ	–	4.5	–	V
$\Delta V_{LN(T)}$	DC line voltage variation with temperature referenced to 25 °C	T_{amb} = −25 to +75 °C	–	8.0	–	mV
Masks regulation (pins LCC, LVI, CST and RGL; bit CRC)						
DC CHARACTERISTICS						
$I_{LCC(max)}$	maximum current sunk by pin LCC		500	–	–	μA
$R_{int(LCC)}$	internal resistance between pins V_{CC} and LCC		–	165	–	kΩ
Voltage regulation mode						
I_{LVIV}	current sourced from pin LVI	bit CRC = 0	–	200	–	nA
Current regulation mode						
I_{knee}	start line current for current regulation mode	bit CRC = 1	–	35	–	mA
R_{REGC}	DC mask slope in current regulation mode	$I_{line} > I_{knee}$; R_{LVI} = 1 MΩ; R_{RGL} = 7.15 kΩ; bit CRC = 1	–	1.4	–	kΩ
Current limitation						
I_{prot}	current limitation level		–	145	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Electronic hook-switch control (pin EHI)						
V_{IH}	HIGH-level input voltage		2.3	–	V_{CC} + 0.4	V
V_{IL}	LOW-level input voltage	V_{CC} = 3.0 to 5.5 V	GND – 0.4	–	$0.3V_{CC}$	V
I_{bias}	input bias current	input level = HIGH	0	2	5	µA
Transmit amplifier (pins TXI+, TXI– and LN)						
$\|Z_i\|$	input impedance	between pins TXI+ and GND or TXI– and GND	–	21	–	kΩ
		between pins TXI+ and TXI–	–	36	–	kΩ
$G_{v(TX)}$	voltage gain from TXI+/TXI– to LN	V_{TXI} = 50 mV (RMS)	10.7	11.7	12.7	dB
$\Delta G_{v(TX)(f)}$	voltage gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.3	–	dB
$\Delta G_{v(TX)(T)}$	voltage gain variation with temperature referenced to 25 °C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
CMRR	common mode rejection ratio		–	65	–	dB
PSRR	power supply rejection ratio		–	36	–	dB
$V_{LN(max)(rms)}$	maximum sending signal (RMS value)	I_{line} = 15 mA; THD = 2%	1.2	1.4	–	V
		I_{line} = 4 mA; THD = 10%	–	0.26	–	V
$V_{iTX(max)(rms)}$	maximum transmit input voltage (RMS value) for 2% THD on pin LN	I_{line} = 15 mA	–	0.35	–	V
		I_{line} = 90 mA	–	0.75	–	V
$V_{no(LN)}$	noise output voltage at pin LN	pins TXI+ and TXI– short-circuited through 200 Ω in series with 10 µF; psophometrically weighted (P53 curve)	–	–74	–	dBm p
Receive amplifier (pins RXI and RXO; bit RXM)						
$\|Z_i\|$	input impedance between pins RXI and GND		–	21	–	kΩ
$G_{v(RX)}$	voltage gain from RXI to RXO	V_{RXI} = 2 mV (RMS)	36.9	37.9	38.9	dB
$\Delta G_{v(RX)(f)}$	voltage gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{v(RX)(T)}$	voltage gain variation with temperature referenced to 25 °C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
PSRR	power supply rejection ratio		–	68	–	dB
THD	total harmonic distortion	V_{RXI} = 2 mV (RMS)	–	0.03	–	%
		V_{RXI} = 12.5 mV (RMS)	–	2	–	%
		V_{RXI} = 19.5 mV (RMS); I_{line} = 90 mA	–	2	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{no(RXO)(rms)}$	noise output voltage at pin RXO (RMS value)	RXI open-circuit; psophometrically weighted (P53 curve)	–	–81	–	dBVp
$\Delta G_{v(RX)(m)}$	voltage gain reduction from pin RXI to RXO when muted	V_{RXI} = 10 mV (RMS); bit RXM = 1	–	80	–	dB
Automatic gain control (pin AGC; bits RAGC1, RAGC2, SAGC and AGC)						
$\Delta G_{v(trx)}$	gain control range for transmit and receive amplifiers with respect to I_{line} = 15 mA	I_{line} = 90 mA	–	6.5	–	dB
I_{start}	highest line current for maximum gain	bits RAGC1 = 1; RAGC2 = 1	–	22.5	–	mA
		bits RAGC1 = 1; RAGC2 = 0	–	25	–	mA
		bits RAGC1 = 0; RAGC2 = 1	–	27	–	mA
		bits RAGC1 = 0; RAGC2 = 0	–	29.5	–	mA
I_{stop}	lowest line current for minimum gain when I_{start} = 23 mA	bits SAGC = 0; RAGC1 = 1; RAGC2 = 1	–	62	–	mA
		bits SAGC = 1; RAGC1 = 1; RAGC2 = 1	–	43	–	mA
$\Delta G_{v(trxoff)}$	gain variation for transmit and receive amplifiers when AGC is off	bit AGC = 0; I_{line} = 15 to 140 mA	–	–	±0.2	dB
Amplifiers						
AUXILIARY AMPLIFIER (PINS AXI AND AXO; BIT AXM)						
$\|Z_i\|$	input impedance between pins AXI and GND		–	3.8	–	kΩ
$G_{v(AX)}$	voltage gain from pin AXI to AXO	V_{AXI} = 2 mV (RMS)	30.8	31.8	32.8	dB
$\Delta G_{v(AX)(f)}$	voltage gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{v(AX)(T)}$	voltage gain variation with temperature referenced to 25 °C	T_{amb} = –25 to +75 °C	–	±0.2	–	dB
PSRR	power supply rejection ratio		–	79	–	dB
$V_{no(AXO)(rms)}$	noise output voltage at pin AXO (RMS value)	pin AXI connected to pin GND through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	–	–83	–	dBVp
$\Delta G_{v(AX)(m)}$	voltage gain reduction from pin AXI to AXO when amplifier muted	V_{AXI} = 10 mV (RMS); bit AXM = 1	–	80	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LOUDSPEAKER CHANNEL (PINS LSAI1, LSAI2, LSAO, DLC AND LSPGND; BITS LSA1, LSA2, LSPD, VOL0, VOL1, VOL2 AND DLCI)						
Loudspeaker amplifier						
$\|Z_i\|$	input impedance between pins LSAI1 or LSAI2 and GND	bits LSA1 = 1, LSA2 = 1	–	21	–	kΩ
$G_{v(LSA)}$	voltage gain from LSAI1 or LSAI2 to LSAO for maximum volume	V_{LSAI} = 8 mV (RMS); bits LSA1 = 1, LSA2 = 1	26.5	28	29.5	dB
$\Delta G_{v(LSA)(f)}$	voltage gain variation with frequency referenced to 1 kHz	V_{LSAI} = 8 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
$\Delta G_{v(LSA)(T)}$	voltage gain variation with temperature referenced to 25 °C	T_{amb} = −25 to +75 °C	–	±0.3	–	dB
$V_{LSAI(rms)}$	maximum input voltage between pins LSAI1 or LSAI2 and GND (RMS value)	V_{CC} = 5.0 V; $G_{v(LSA)}$ = 7 dB; for 2% of THD in input stage	–	500	–	mV
$V_{no(LSAO)(rms)}$	noise output voltage at pin LSAO (RMS value)	pin LSAI1 (with bits LSA1 = 1, LSA2 = 0) or pin LSAI2 (with bits LSA1 = 0, LSA2 = 1) connected to pin GND through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	–	−80	–	dBVp
Output capability						
$V_{LSAO(p-p)}$	output voltage capability at pin LSAO (peak-to-peak value)	V_{CC} = 5.0 V; $G_{v(LSA)}$ = 28 dB; V_{LSAI} = 100 mV (RMS); R_L = 16 Ω	3.0	3.6	–	V
		V_{CC} = 3.3 V; $G_{v(LSA)}$ = 28 dB; V_{LSAI} = 100 mV (RMS); R_L = 8 Ω	–	2.0	–	V
$\|I_{LSAO(max)}\|$	maximum current capability at pin LSAO (peak value)		150	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Dynamic limiter						
t_{att}	attack time	V_{CC} = 3 V; $G_{v(LSA)}$ = 28 dB				
		when V_{LSAI} jumps from 20 mV (RMS) to 20 mV (RMS) + 10 dB; bit DLCI = 0	–	–	5	ms
		when V_{CC} drops below 2.7 V; bit DLCI = don't care	–	1	–	ms
t_{rel}	release time	V_{CC} = 3 V; $G_{v(LSA)}$ = 28 dB; when V_{LSAI} jumps from 20 mV (RMS) + 10 dB to 20 mV (RMS); bit DLCI = 0	–	250	–	ms
THD	total harmonic distortion at V_{LSAI} = 20 mV (RMS) + 10 dB	V_{CC} = 3 V; $G_{v(LSA)}$ = 28 dB; $t > t_{att}$	–	0.5	5	%
Volume control						
$\Delta G_{v(LSA)}$	voltage gain adjustment range	bits (VOL0, VOL1, VOL2)from (0, 0, 0) to (1, 1, 1)	–	21	–	dB
$\Delta G_{v(LSA)(s)}$	voltage gain adjustment step	VOL0 from 0 to 1	–	3	–	dB
Switches (pins SWI1, SWI2 and SWI3; bits SWC1, SWC2 and SWC3)						
$\lvert Z_{i(off)} \rvert$	AC impedance between pins SWIn and GND when not selected	bit SWCn = 0	700	–	–	kΩ
$\lvert Z_{i(on)} \rvert$	AC impedance between pins SWIn and GND when selected	2 mA < I_{SWIn} < 20 mA; bit SWCn = 1	–	–	30	Ω
Serial interface (pins DATA, CLK and EN)						
V_{IH}	HIGH-level input voltage		2.3	–	V_{CC} + 0.4	V
V_{IL}	LOW-level input voltage	V_{CC} = 3 to 5.5 V	GND – 0.4	–	0.3V_{CC}	V
I_{bias}	input bias current	input level = HIGH	0	2	5	µA
C_i	input capacitance at pins DATA, CLK and EN		–	4	–	pF

SERIAL BUS TIMING CHARACTERISTICS

V_{CC} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
Serial programming clock; pin CLK				
f_{clk}	clock frequency	0	300	kHz
Enable programming; pin EN				
t_{START}	delay to falling clock edge	1	–	µs
t_{END}	delay from last rising clock edge	0.1	–	µs
$t_{W(min)}$	minimum inactive pulse width	1.5	–	µs
$t_{SU;EN}$	enable set-up time to next clock edge	0.1	–	µs
Serial data; pin DATA				
$t_{SU;DATA}$	input data to clock set-up time	2	–	µs
$t_{HD;DATA}$	input data to clock hold time	2	–	µs

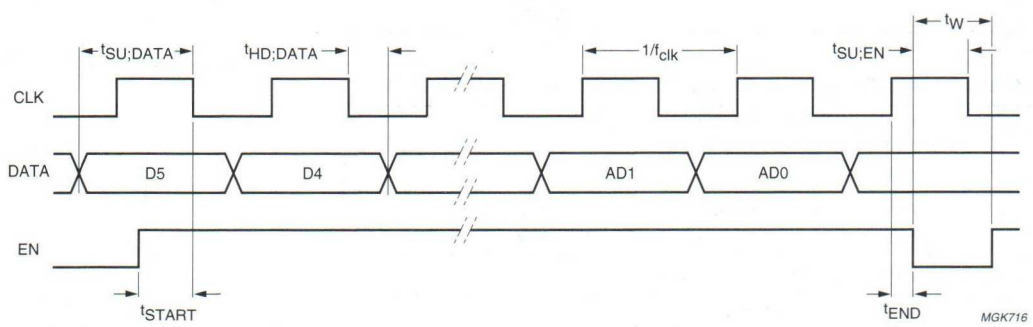


Fig.16 Serial bus timing diagram.

TEST AND APPLICATION INFORMATION

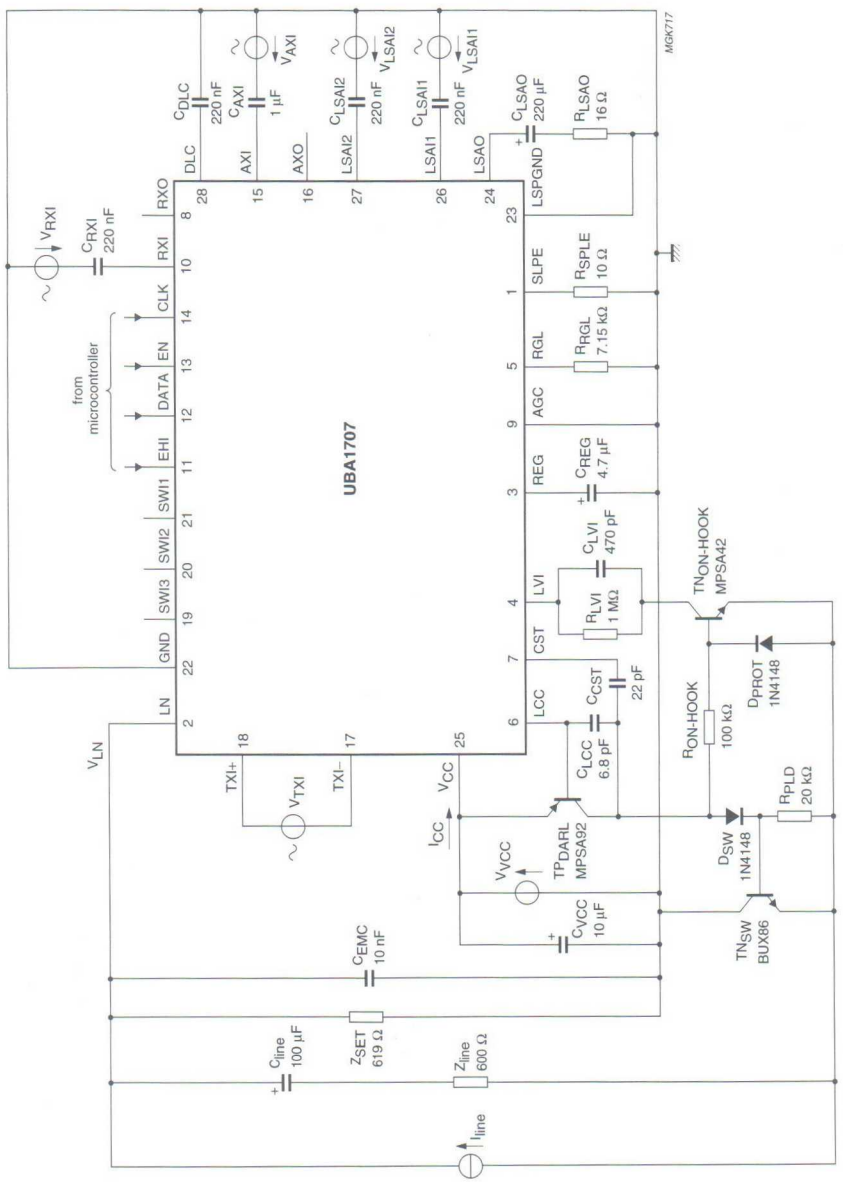


Fig.17 Test circuit.

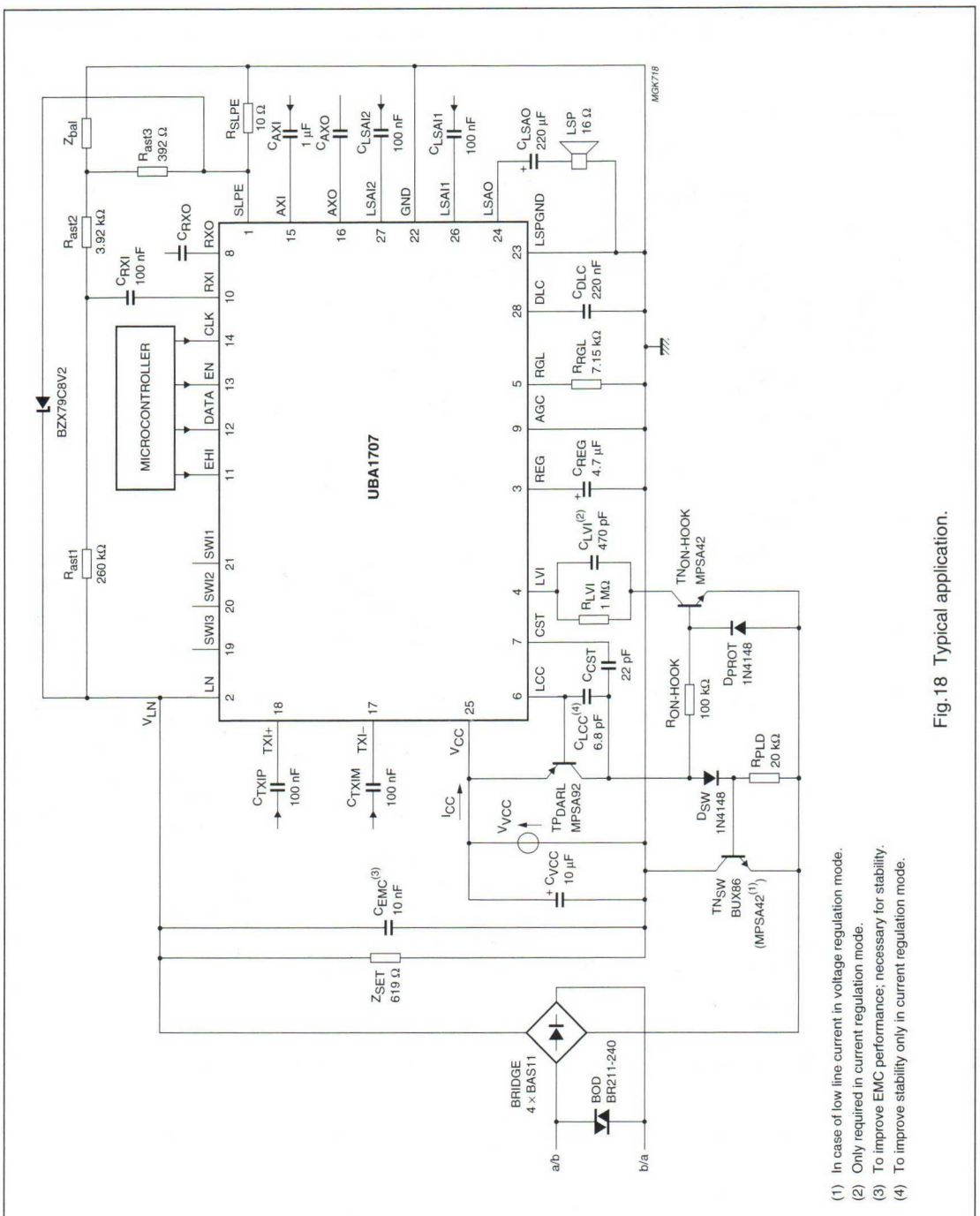


Fig.18 Typical application.

HANDS-FREE CIRCUITS

Hands-free IC TEA1093

FEATURES

- Line powered supply with:
  - adjustable stabilized supply voltage
  - power down function
- Microphone channel with:
  - externally adjustable gain
  - microphone mute function
- Loudspeaker channel with:
  - externally adjustable gain
  - dynamic limiter to prevent distortion
  - rail-to-rail output stages for single-ended or bridge-tied load drive
  - logarithmic volume control via linear potentiometer
  - loudspeaker mute function
- Duplex controller consisting of:
  - signal envelope and noise envelope monitors for both channels with:

    externally adjustable sensitivity

    externally adjustable signal envelope time constant

    externally adjustable noise envelope time constant
  - decision logic with:

    externally adjustable switch-over timing

    externally adjustable idle mode timing

    externally adjustable dial tone detector in receive channel
  - voice switch control with:

    adjustable switching range

    constant sum of gain during switching

    constant sum of gain at different volume settings.

APPLICATIONS

- Line-powered telephone sets with hands-free/listening-in functions.

GENERAL DESCRIPTION

The TEA1093 is a bipolar circuit intended for use in line-powered telephone sets. In conjunction with a member of the TEA1060 family or PCA1070 transmission circuits, the device offers a hands-free function for line powered telephone sets. It incorporates a supply, a microphone channel, a loudspeaker channel and a duplex controller with signal and noise monitors on both channels.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1093	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TEA1093T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

QUICK REFERENCE DATA

V_{SREF} = 4.2 V; V_{GND} = 0 V; I_{SUP} = 15 mA; V_{SUP} = 0 V (RMS); f = 1 kHz; T_{amb} = 25 °C; PD = LOW; MUTET = LOW; R_L = 50 Ω; R_{VOL} = 0 Ω; measured in test circuit of Fig.15; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{SUP}	operating supply current (pin SUP)		7	–	140	mA
V_{BB}	stabilized supply voltage		3.35	3.6	3.85	V
$I_{BB(pd)}$	current consumption from pin V_{BB} in power-down condition	PD = HIGH; V_{BB} = 3.6 V	–	400	550	µA
$I_{SUP(pd)}$	current consumption from pin SUP in power-down condition	PD = HIGH; V_{sup} = 4.5 V	–	55	75	µA
G_{vtx}	voltage gain from pin MIC to pin MOUT in transmit mode	V_{MIC} = 1 mV (RMS); R_{GAT} = 30.1 kΩ	12.5	15	17.5	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAT}		−10	–	+10	dB
G_{vrx}	voltage gain in receive mode	V_{RIN} = 20 mV (RMS); R_{GAR} = 66.5 kΩ; R_L = 50 Ω				
	the difference between RIN1 and RIN2 to LSP1 or LSP2 single-ended load		15.5	18	20.5	dB
	the difference between RIN1 and RIN2 to the difference between LSP1 and LSP2 bridge-tied load		21.5	24	26.5	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		−15	–	+15	dB
$V_{O(p-p)}$	bridge-tied load (peak-to-peak value)	V_{RIN} = 150 mV (RMS); R_L = 33 Ω; note 1	–	5.15	–	V
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment with R_{SWR} referenced to R_{SWR} = 365 kΩ		−40	–	+12	dB
T_{amb}	operating ambient temperature		−25	–	+75	°C

Note

1. Corresponds to 100 mW output power.

BLOCK DIAGRAM

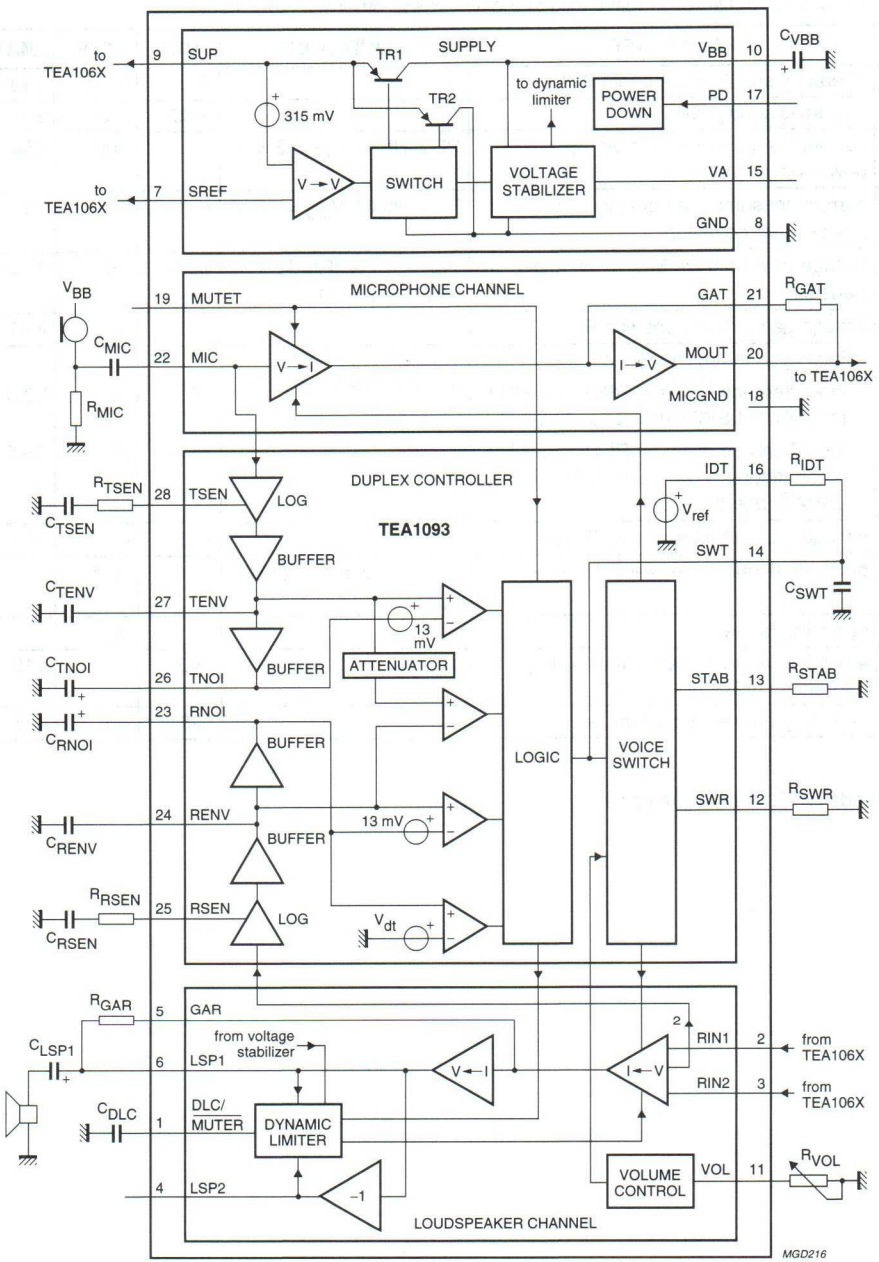


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DLC/$\overline{\text{MUTER}}$	1	dynamic limiter timing adjustment, receiver channel mute input
RIN1	2	receiver amplifier input 1
RIN2	3	receiver amplifier input 2
LSP2	4	loudspeaker amplifier output 2
GAR	5	receiver gain adjustment
LSP1	6	loudspeaker amplifier output 1
SREF	7	supply reference input
GND	8	ground reference
SUP	9	supply input
V_{BB}	10	stabilized supply output
VOL	11	receiver volume adjustment
SWR	12	switching range adjustment
STAB	13	reference current adjustment
SWT	14	switch-over timing adjustment
VA	15	V_{BB} voltage adjustment
IDT	16	idle mode timing adjustment
PD	17	power-down input
MICGND	18	ground reference for the microphone amplifier
MUTET	19	transmit channel mute input
MOUT	20	microphone amplifier output
GAT	21	microphone gain adjustment
MIC	22	microphone input
RNOI	23	receive noise envelope timing adjustment
RENV	24	receive signal envelope timing adjustment
RSEN	25	receive signal envelope sensitivity adjustment
TNOI	26	transmit noise envelope timing adjustment
TENV	27	transmit signal envelope timing adjustment
TSEN	28	transmit signal envelope sensitivity adjustment

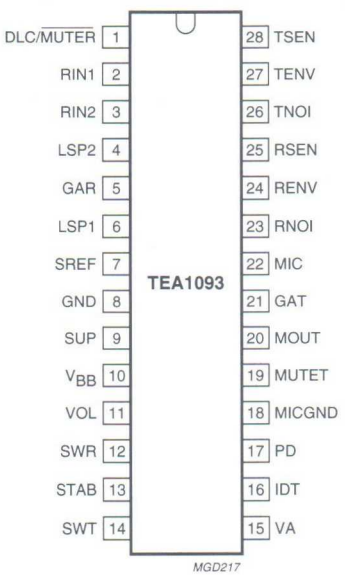


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The values given in the functional description are typical values except when otherwise specified.

A principle diagram of the TEA106X is shown on the left side of Fig.3. The TEA106X is a transmission circuit of the TEA1060 family intended for hand-set operation. It incorporates a receiving amplifier for the earpiece, a transmit amplifier for the microphone and a hybrid. For more details on the TEA1060 family, please refer to *"Data Handbook IC03"*. The right side of Fig.3 shows a principle diagram of the TEA1093, a hands-free add-on circuit with a microphone amplifier, a loudspeaker amplifier and a duplex controller.

As can be seen from Fig.3, a loop is formed via the sidetone network in the transmission circuit and the acoustic coupling between loudspeaker and microphone of the hands-free circuit. When this loop gain is greater than 1, howling is introduced. In a full duplex application, this would be the case. The loop-gain has to be much lower than 1 and therefore has to be decreased to avoid howling. This is achieved by the duplex controller.The duplex controller of the TEA1093 detects which channel has the 'largest' signal and then controls the gain of the microphone amplifier and the loudspeaker amplifier so that the sum of the gains remains constant. As a result, the circuit can be in three stable modes:

1. Transmit mode (Tx mode): the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum.
2. Receive mode (Rx mode): the gain of the loudspeaker amplifier is at its maximum and the gain of the microphone amplifier is at its minimum.
3. Idle mode: the gain of the amplifiers is halfway between their maximum and minimum value.

The difference between the maximum gain and minimum gain is called the switching range.

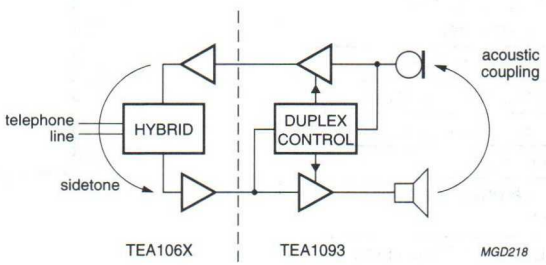


Fig.3 Hands-free telephone set principles.

Supply: pins SUP, SREF, V_{BB}, GND, VA and PD

As can be seen from Fig.4, the line current is divided between the speech-transmission circuit ($I_{TR} + I_{CC}$) and the TEA1093 circuit (I_{SUP}). It can be shown that:

$$I_{SUP} = I_{line} - I_{TR} - I_{CC}$$

Where:

$$I_{TR} = V_{SUP} - V_{SREF}/R_{SREF}$$

$$V_{SUP} - V_{SREF} = 315 \text{ mV}$$

$$R_{SREF} = 100\ \Omega$$

$$I_{CC} \approx 1 \text{ mA}$$

It follows that $I_{SUP} \approx I_{LINE} - 4$ mA.

The TEA1093 stabilizes its own supply voltage of 3.6 V at V_{BB}. The voltage on V_{BB} can be adjusted by means of an external resistor R_{VA}.

When R_{VA} is connected between pin V_A and GND, the voltage on V_{BB} is increased, when connected between pin V_A and V_{BB}, it is decreased. This is shown in Fig.5. Two capacitors of 4.7 nF (C_{SREF} and C_{STAB}) are required to ensure stability of the supply block. When V_{SUP} is greater than V_{BB} + 0.4 V, the current I_{SUP} is supplied to V_{BB} via TR1. When V_{SUP} is less, the current is shunted to GND via TR2, which prevents distortion on the line.

To reduce current consumption during pulse dialling or register recall (flash), the TEA1093 is provided with a power-down (PD) input. When the voltage on PD is HIGH, the current consumption from SUP is 55 µA and from V_{BB} 400 µA. Therefore a capacitor of 470 µF (C_{VBB}) is sufficient to power the TEA1093 during pulse dialling.

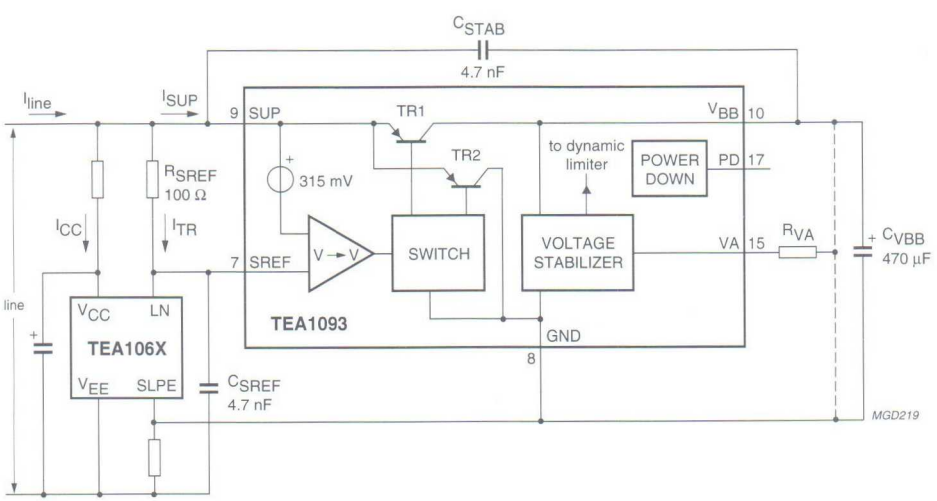


Fig.4 Supply arrangement.

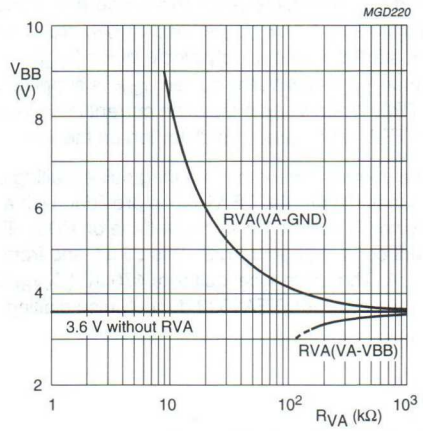


Fig.5 V_{BB} as a function of R_{VA}.

Microphone channel: pin MIC, GAT, MOUT, MICGND and MUTET

The TEA1093 has an asymmetrical microphone input MIC with an input resistance of 20 kΩ. The gain of the input stage varies according to the mode of the TEA1093. In the transmit mode, the gain is at its maximum; in the receive mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The output capability at pin MOUT is 20 μA (RMS).

In the transmit mode, the overall gain of the microphone amplifier (from pin MIC to MOUT) can be adjusted from 5 dB up to 25 dB to suit specific application requirements. The gain is proportional to the value of R_{GAT} and equals 15 dB typical with R_{GAT} = 30.1 kΩ.

A capacitor must be connected in parallel with R_{GAT} to ensure stability of the microphone amplifier. Together with R_{GAT}, it also provides a first-order low-pass filter.

By applying a HIGH level on pin MUTET, the microphone amplifier is muted and the TEA1093 is automatically forced into the receive mode.

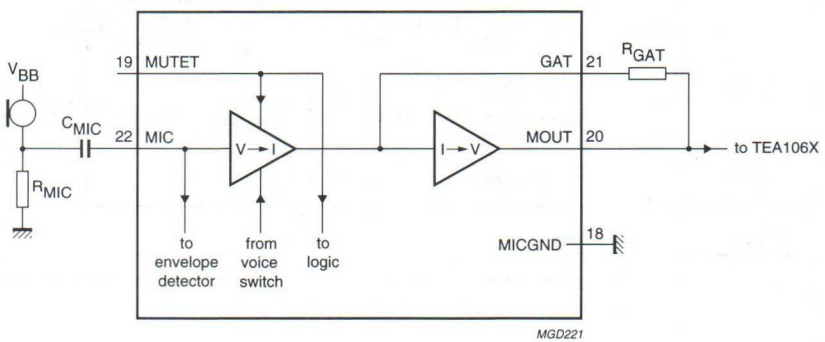


Fig.6 Microphone channel.

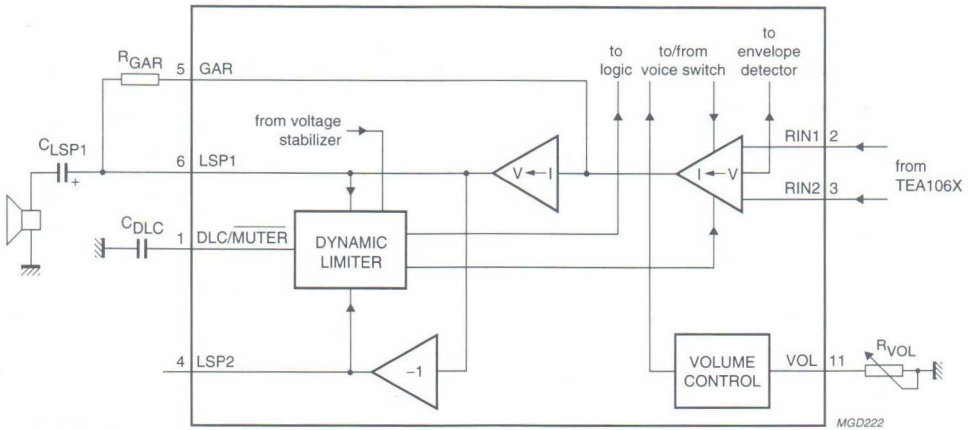


Fig.7 Loudspeaker channel.

Loudspeaker channel

LOUDSPEAKER AMPLIFIER: PINS RIN1, RIN2, GAR, LSP1 AND LSP2

The TEA1093 has symmetrical inputs for the loudspeaker amplifier with an input resistance of 40 kΩ between RIN1 and RIN2 (2 × 20 kΩ). The input stage can accommodate signals up to 390 mV (RMS) at room temperature for 2% of total harmonic distortion (THD). The gain of the input stage varies according to the mode of the TEA1093. In the receive mode, the gain is at its maximum; in the transmit mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The rail-to-rail output stage is designed to power a loudspeaker which is connected as a single-ended load (between LSP1 and GND) or as a bridge-tied load (between LSP1 and LSP2).

In the receive mode, the overall gain of the loudspeaker amplifier can be adjusted from 3 dB up to 39 dB to suit specific application requirements. The gain from RIN1 or RIN2 to LSP1 is proportional to the value of R_{GAR} and equals 18 dB with R_{GAR} = 66.5 kΩ. The second output LSP2 is in opposite phase with LSP1. Therefore, in the basic application, the gain between RIN1-RIN2 to LSP1-LSP2 equals 24 dB typical with R_{GAR} = 66.5 kΩ. A capacitor connected in parallel with R_{GAR} can be used to provide a first-order low-pass filter.

VOLUME CONTROL: PIN VOL

The loudspeaker amplifier gain can be adjusted with the potentiometer R_{VOL}. A linear potentiometer can be used to obtain logarithmic control of the gain at the loudspeaker amplifier. Each 950 Ω increase of R_{VOL} results in a gain loss of 3 dB. The maximum gain reduction with the volume control is internally limited to the switching range.

DYNAMIC LIMITER: PIN DLC/$\overline{\text{MUTER}}$

The dynamic limiter of the TEA1093 prevents clipping of the loudspeaker output stages and protects the operation of the circuit when the supply condition falls below a certain level.

Hard clipping of the loudspeaker output stages is prevented by rapidly reducing the gain when the output stages start to saturate. The time in which gain reduction is effected (clipping attack time) is approximately a few milliseconds. The circuit stays in the reduced gain mode until the peaks of the loudspeaker signals no longer cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time (typical 250 ms). Both attack and release times are proportional to the value of the capacitor C_{DLC}. The total harmonic distortion of the loudspeaker output stages, in reduced gain mode, stays below 5% up to 10 dB (minimum) of input voltage overdrive [providing V_{RIN} is below 390 mV (RMS)].

When the supply conditions drop below the required level, the gain of the loudspeaker amplifier is reduced in order to prevent the TEA1093 from malfunctioning. Only the gain of the loudspeaker amplifier is affected since it is considered to be the major power consuming part of the TEA1093.

When the TEA1093 experiences a loss of current, the supply voltage V_{BB} decreases. In this event, the gain of the loudspeaker amplifiers is slowly reduced (approximately a few seconds). When the supply voltage continues to decrease and drops below an internal voltage threshold of 2.75 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). When normal supply conditions are resumed, the gain of the loudspeaker amplifier is increased again. This system ensures that in the event of large continuous signals, all current is used to power the loudspeaker while the voltage on pin V_{BB} remains at its nominal value.

By forcing a level lower than 0.2 V on pin DLC/$\overline{\text{MUTER}}$, the loudspeaker amplifier is muted and the TEA1093 is automatically forced into the transmit mode.

Duplex controller

SIGNAL AND NOISE ENVELOPE DETECTORS: PINS TSEN, TENV, TNOI, RSEN, RENV AND RNOI

The signal envelopes are used to monitor the signal level strength in both channels. The noise envelopes are used to monitor background noise in both channels. The signal and noise envelopes provide inputs for the decision logic. The signal and noise envelope detectors are shown in Fig.8.

For the transmit channel, the input signal at MIC is 40 dB, amplified to TSEN. For the receive channel, the differential signal between RIN1 and RIN2 is 0 dB amplified to RSEN. The signals from TSEN and RSEN are logarithmically compressed and buffered to TENV and RENV respectively. The sensitivity of the envelope detectors is set with R_{TSEN} and R_{RSEN}. The capacitors connected in series with the two resistors block any DC component and form a first-order high-pass filter. In the basic application, see Fig.16, it is assumed that V_{MIC} = 1 mV (RMS) and V_{RIN} = 100 mV (RMS) nominal and both R_{TSEN} and R_{RSEN} have a value of 10 kΩ. With the value of C_{TSEN} and C_{RSEN} at 100 nF, the cut-off frequency is at 160 Hz.

The buffer amplifiers leading the compressed signals to TENV and RENV have a maximum source current of 120 μA and a maximum sink current of 1 μA. Together with the capacitor C_{TENV} and C_{RENV}, the timing of the signal envelope monitors can be set. In the basic application, the value of both capacitors is 470 nF. Because of the logarithmic compression, each 6 dB signal increase means 18 mV increase of the voltage on the envelopes TENV or RENV at room temperature. Thus, timings can be expressed in dB/ms. At room temperature, the 120 μA sourced current corresponds to a maximum rise-slope of the signal envelope of 85 dB/ms. This is sufficient to track normal speech signals. The 1 μA current sunk by TENV or RENV corresponds to a maximum fall-slope of 0.7 dB/ms. This is sufficient for a smooth envelope and also eliminates the effect of echoes on switching behaviour.

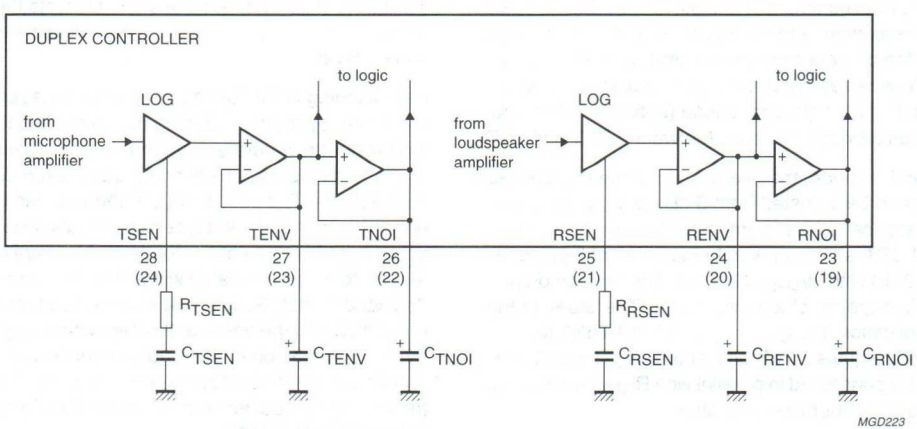


Fig.8 Signal and noise envelope detectors.

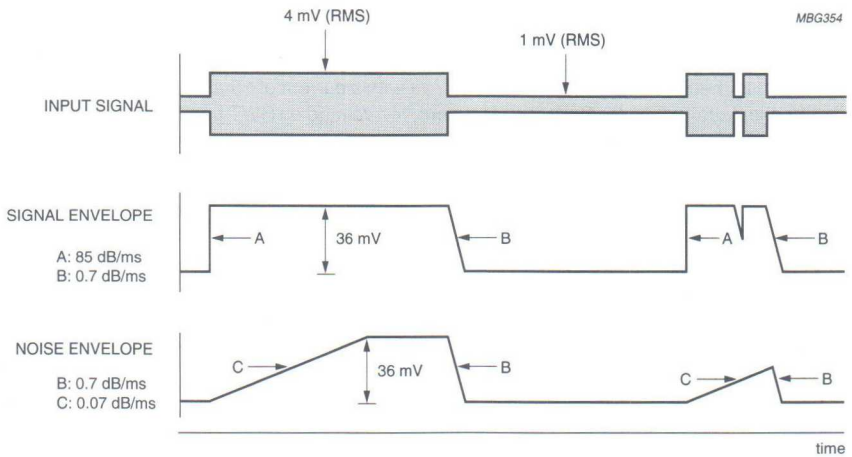
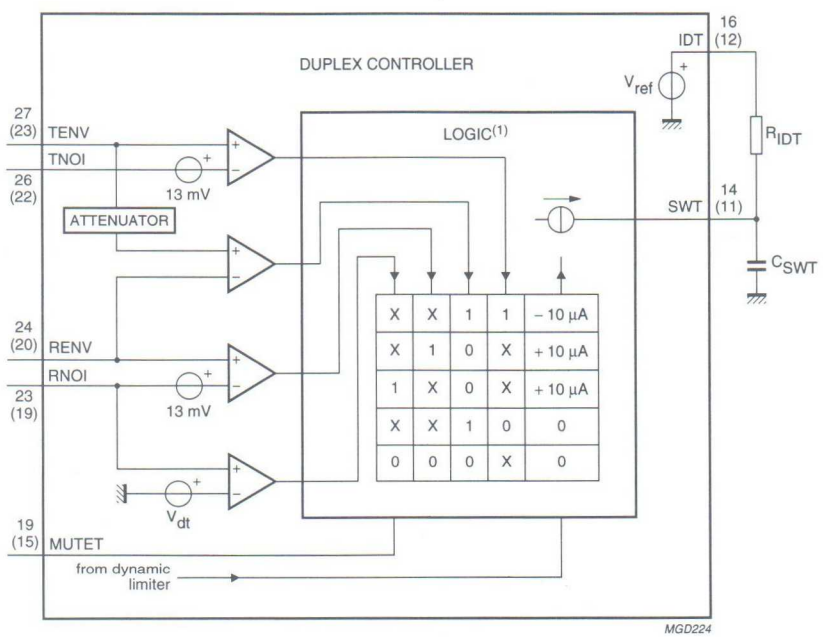


Fig.9 Signal and noise envelope waveforms.



(1) When MUTET = HIGH, +10 µA is forced.
When DLC/MUTER < 0.2 V, −10 µA is forced.

Fig.10 Decision logic.

To determine the noise level, the signal on TENV and RENV are buffered to TNOI and RNOI. These buffers have a maximum source current of 1 μA and a maximum sink current of 120 μA. Together with the capacitors C_{TNOI} and C_{RNOI}, the timing can be set. In the basic application of Fig.16, the value of both capacitors is 4.7 μF. At room temperature, the 1 μA sourced current corresponds to a maximum rise-slope of the noise envelope of approximately 0.07 dB/ms. This is small enough to track background noise and not to be influenced by speech bursts. The 120 μA current that is sunk corresponds to a maximum fall-slope of approximately 8.5 dB/ms. However, during the decrease of the signal envelope, the noise envelope tracks the signal envelope so it will never fall faster than approximately 0.7 dB/ms. The behaviour of the signal envelope and noise envelope monitors is illustrated in Fig.9.

Decision logic: pins IDT and SWT

The TEA1093 selects its mode of operation (transmit, receive or idle mode) by comparing the signal and the noise envelopes of both channels. This is executed by the decision logic. The resulting voltage on pin SWT is the input for the voice-switch.

To facilitate the distinction between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference $V_{ENV}-V_{NOI}$ = 13 mV. This so called speech/noise threshold is implemented in both channels.

The signal on MIC contains both speech and the signal coming from the loudspeaker (acoustic coupling). When receiving, the contribution from the loudspeaker overrules the speech. As a result, the signal envelope on TENV is formed mainly by the loudspeaker signal. To correct this, an attenuator is connected between TENV and the TENV/RENV comparator. Its attenuation equals that applied to the microphone amplifier.

When a dial tone is present on the line, without monitoring, the tone would be recognized as noise because it is a signal with a constant amplitude. This would cause the TEA1093 to go into the idle mode and the user of the set would hear the dial tone fade away. To prevent this, a dial tone detector is incorporated which, in standard applications, does not consider input signals between RIN1 and RIN2 as noise when they have a level greater than 127 mV (RMS). This level is proportional to R_{RSEN}.

As can be seen from Fig.10, the output of the decision logic is a current source. The logic table gives the relationship between the inputs and the value of the current source. It can charge or discharge the capacitor C_{SWT} with a current of 10 μA (switch-over). If the current is zero, the voltage on SWT becomes equal to the voltage on IDT via the high-ohmic resistor R_{IDT} (idling). The resulting voltage difference between SWT and IDT determines the mode of the TEA1093 and can vary between −400 mV and +400 mV.

Table 1 Modes of TEA1093

$V_{SWT} - V_{IDT}$ (mV)	MODE
<−180	transmit mode
0	idle mode
>+180	receive mode

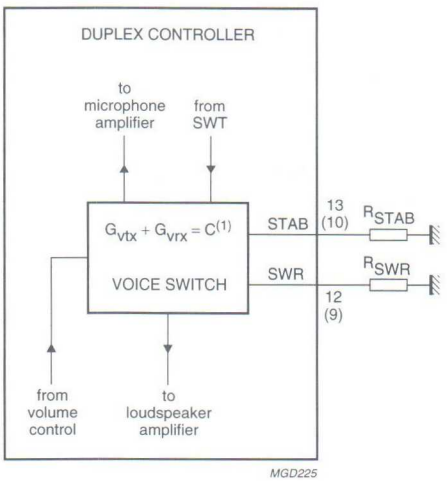
The switch-over timing can be set with C_{SWT}, the idle mode timing with C_{SWT} and R_{IDT}. In the basic application given in Fig.16, C_{SWT} is 220 nF and R_{IDT} is 2.2 MΩ. This enables a switch-over time from transmit to receive mode or vice-versa of approximately 13 ms (580 mV swing on SWT). The switch-over time from idle mode to transmit mode or receive mode is approximately 4 ms (180 mV swing on SWT).

The switch over, from receive mode or transmit mode to idle mode, is equal to $4 \times R_{IDT} \times C_{SWT}$ and is approximately 2 seconds (idle mode time).

The inputs MUTET and DLC/$\overline{\text{MUTER}}$ overrule the decision logic. When MUTET goes HIGH, the capacitor C_{SWT} is charged with 10 μA thus resulting in the receive mode. When the voltage on pin DLC/$\overline{\text{MUTER}}$ goes lower than 0.2 V, the capacitor is discharged with 10 μA thus resulting in the transmit mode.

Voice-switch: pins STAB and SWR

A diagram of the voice-switch is illustrated in Fig.11. With the voltage on SWT, the TEA1093 voice-switch regulates the gains of the transmit and the receive channel so that the sum of both is kept constant.



(1) c - constant.

Fig.11 Voice-switch.

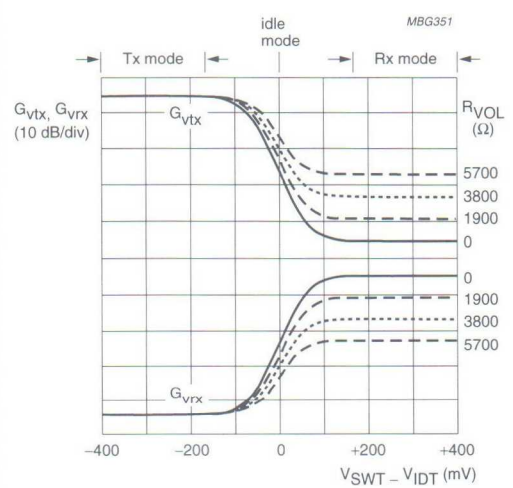


Fig.12 Switch-over behaviour.

In the transmit mode, the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum. In the receive mode, the opposite applies. In the idle mode, both microphone and loudspeaker amplifier gains are halfway. The difference between maximum and minimum is the so called switching range. This range is determined by the ratio of R_{SWR} and R_{STAB} and is adjustable between 0 and 52 dB. R_{STAB} should be 3.65 kΩ and sets an internally used reference current. In the basic application diagram given in Fig.16, R_{SWR} is 365 kΩ which results in a switching range of 40 dB. The switch-over behaviour is illustrated in Fig.12.

In the receive mode, the gain of the loudspeaker amplifier can be reduced using the volume control. Since the voice-switch keeps the sum of the gains constant, the gain of the microphone amplifier is increased at the same time (see dashed curves in Fig.12). In the transmit mode, however, the volume control has no influence on the gain of the microphone amplifier or the gain of the loudspeaker amplifier. Consequently, the switching range is reduced when the volume is reduced. At maximum reduction of volume, the switching range becomes 0 dB.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

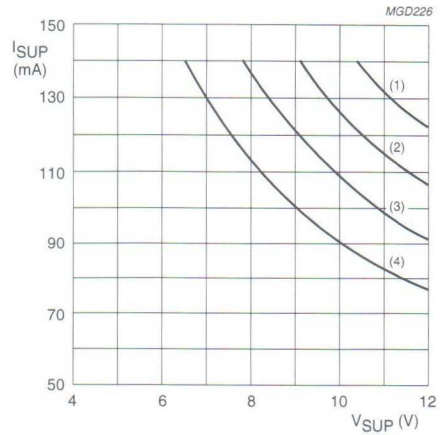
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{n(max)}$	maximum voltage on all pins; except pins SUP, SREF, V_{BB}, RIN1 and RIN2		V_{GND} – 0.4 V	V_{BB} + 0.4 V	V
V_{RINmax}	maximum voltage on pin RIN1 or RIN2		V_{GND} – 1.2 V	V_{BB} + 0.4 V	V
V_{BBmax}	maximum voltage on pin V_{BB}		V_{GND} – 0.4 V	12.0	V
$V_{SREFmax}$	maximum voltage on pin SREF		V_{GND} – 0.4 V	V_{SUP} + 0.4 V	V
V_{SUPmax}	maximum voltage on pin SUP		V_{GND} – 0.4 V	12.0	V
I_{SUPmax}	maximum current on pin SUP	see also Figs 13 and 14	–	140	mA
P_{tot}	total power dissipation	see also Figs 13 and 14; T_{amb} = 75 °C			
	TEA1093		–	910	mW
	TEA1093T		–	670	mW
T_{stg}	storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

HANDLING

ESD in accordance with MIL STD883C; Method 3015 (HBM 1500 Ω, 100 pF); 3 pulses positive and 3 pulses negative on each pin referenced to ground. Class 2: 2000 to 3999 V.

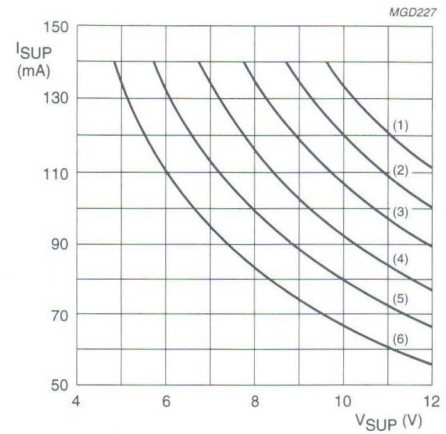
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1093	55	K/W
	TEA1093T	75	K/W



(1) T_{amb} = 45 °C; P_{tot} = 1.45 W.
(2) T_{amb} = 55 °C; P_{tot} = 1.27 W.
(3) T_{amb} = 65 °C; P_{tot} = 1.09 W.
(4) T_{amb} = 75 °C; P_{tot} = 0.91 W.

Fig.13 TEA1093 safe operating area.



(1) T_{amb} = 25 °C; P_{tot} = 1.33 W.
(2) T_{amb} = 35 °C; P_{tot} = 1.20 W.
(3) T_{amb} = 45 °C; P_{tot} = 1.07 W.
(4) T_{amb} = 55 °C; P_{tot} = 0.93 W.
(5) T_{amb} = 65 °C; P_{tot} = 0.80 W.
(6) T_{amb} = 75 °C; P_{tot} = 0.67 W.

Fig.14 TEA1093T safe operating area.

CHARACTERISTICS

V_{SREF} = 4.2 V; V_{GND} = 0 V; I_{SUP} = 15 mA; V_{SUP} = 0 V (RMS); f = 1 kHz; T_{amb} = 25 °C; PD = LOW; MUTET = LOW; R_L = 50 Ω; R_{VOL} = 0 Ω; measured in test circuit of Fig.15; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (VA, SREF, SUP, V_{BB}, GND and PD)						
V_{BB}	stabilized supply voltage		3.35	3.6	3.85	V
$\Delta V_{BB(ISUP)}$	V_{BB} variation with I_{SUP}	I_{SUP} = 15 to 140 mA	–	20	–	mV
$\Delta V_{BB(T)}$	V_{BB} variation with temperature referenced to 25 °C	T_{amb} = −25 to + 75 °C	–	±20	–	mV
$\Delta V_{BB(RVA)}$	V_{BB} adjustment with R_{VA}	between VA and V_{BB}; R_{VA} = 180 kΩ	–	3.2	–	V
		between VA and GND; V_{SREF} = 4.9 V; R_{VA} = 56 kΩ	–	4.5	–	V
$I_{SUP(min)}$	minimum operating current		–	5.5	7.0	mA
$V_{SUP} - V_{BB}$	minimum DC voltage drop between pin SUP and V_{BB}		0.4	–	–	V
$V_{SUP} - V_{SREF}$	internal reference voltage		275	315	355	mV
THD	total harmonic distortion of AC signal on SUP	V_{SUP} = 1 V (RMS)	–	0.5	–	%
Power-Down input PD						
V_{IL}	LOW level input voltage		V_{GND} − 0.4 V	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4 V	V
I_{PD}	input current in power-down condition	PD = HIGH	–	2.5	5.0	µA
$I_{SUP(PD)}$	current consumption from pin SUP in power-down condition	PD = HIGH; V_{SUP} = 4.5 V	–	55	75	µA
$I_{BB(PD)}$	current consumption from pin V_{BB} in power-down condition	PD = HIGH; V_{BB} = 3.6 V	–	400	550	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Microphone channel (MIC, GAT, MOUT, MUTET and MICGND)						
MICROPHONE AMPLIFIER						
$\|Z_i\|$	input impedance between pin MIC and MICGND		17	20	23	kΩ
G_{vtx}	voltage gain from pin MIC to MOUT in transmit mode	V_{MIC} = 1 mV (RMS)	12.5	15	17.5	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAT}		−10	–	+10	dB
ΔG_{vtxT}	voltage gain variation with temperature referenced to 25 °C	V_{MIC} = 1 mV (RMS); T_{amb} = −25 to +75 °C	–	±0.3	–	dB
ΔG_{vtxf}	voltage gain variation with frequency referenced to 1 kHz	V_{MIC} = 1 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
V_{notx}	noise output voltage at pin MOUT	pin MIC connected to MICGND through 200 Ω in series with 10 µF; psophometrically weighted (P53 curve)	–	−100	–	dBmp
TRANSMIT MUTE INPUT MUTET						
V_{IL}	LOW level input voltage		V_{GND} − 0.4 V	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4 V	V
I_{MUTET}	input current	MUTET = HIGH	–	2.5	5	µA
ΔG_{vtxm}	voltage gain reduction with MUTET active	MUTET = HIGH	–	80	–	dB
Loudspeaker channel (RIN1, RIN2, GAR, LSP1, LSP2 and DLC/$\overline{\text{MUTER}}$)						
LOUDSPEAKER AMPLIFIER						
$\|Z_i\|$	input impedance	between pins RIN1 or RIN2 and GND	17	20	23	kΩ
		between pins RIN1 and RIN2	34	40	46	kΩ
G_{vrx}	voltage gain in receive mode	V_{RIN} = 20 mV (RMS)				
	the difference between RIN1 and RIN2 to the difference between LSP1 and LSP2, bridge-tied load		21.5	24	26.5	dB
	the difference between RIN1 and RIN2 to LSP1 or LSP2, single-ended load		15.5	18	20.5	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		−15	–	+15	dB
ΔG_{vrxT}	voltage gain variation with temperature referenced to 25 °C	V_{RIN} = 20 mV (RMS); T_{amb} = -25 to +75 °C	–	±0.3	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_{vrxf}	voltage gain variation with frequency referenced to 1 kHz	V_{RIN} = 20 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
$V_{RIN(rms)}$	maximum input voltage between RIN1 and RIN2 (RMS value)	for 2% THD in input stage; R_{GAR} = 11.8 kΩ	–	390	–	mV
$V_{norx(rms)}$	noise output voltage at pin LSP1 or LSP2 (RMS value)	inputs RIN1 and RIN2 short-circuited through 200 Ω in series with 10 µF; psophometrically weighted (P53 curve)	–	80	–	µV
CMRR	common mode rejection ratio		–	50	–	dB
ΔG_{vrxv}	voltage gain variation related to ΔR_{VOL} = 950 Ω	when total attenuation does not exceed the switching range	–	3	–	dB
OUTPUT CAPABILITY						
$V_{OSE(p-p)}$	single-ended load (peak-to-peak value)	V_{RIN} = 150 mV (RMS); I_{SUP} = 11 mA; note 1	1.2	1.45	–	V
		V_{RIN} = 150 mV (RMS); I_{SUP} = 16.5 mA; note 2	2.5	2.9	–	V
$V_{OBTL(p-p)}$	bridge-tied load (peak-to-peak value)	V_{RIN} = 150 mV (RMS); I_{SUP} = 27 mA; note 2	2.5	2.9	–	V
		V_{RIN} = 150 mV (RMS); I_{SUP} = 35 mA; note 3	3.5	4.0	–	V
		V_{RIN} = 150 mV (RMS); I_{SUP} = 62 mA; R_L = 33 Ω; note 4	–	5.15	–	V
$\lvert I_{OM(max)} \rvert$	maximum output current at LSP1 or LSP2 (peak value)		150	300	–	mA
DYNAMIC LIMITER						
t_{att}	attack time when V_{RIN} jumps from 20 mV to 20 mV + 10 dB	R_{GAR} = 374 kΩ; I_{SUP} = 20 mA	–	–	5	ms
t_{rel}	release time when V_{RIN} jumps from 20 mV + 10 dB to 20 mV	R_{GAR} = 374 kΩ; I_{SUP} = 20 mA	–	250	–	ms
THD	total harmonic distortion at V_{RIN} = 20 mV + 10 dB	R_{GAR} = 374 kΩ; I_{SUP} = 20 mA; $t > t_{att}$	–	0.9	5	%
$V_{BB(th)}$	V_{BB} limiter threshold		–	2.75	–	V
t_{att}	attack time when V_{BB} jumps below $V_{BB(th)}$		–	1	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MUTE RECEIVE						
$V_{DLC(th)}$	threshold voltage required on pin DLC/$\overline{\text{MUTER}}$ to obtain mute receive condition		V_{GND} – 0.4 V	–	0.2	V
$I_{DLC(th)}$	threshold current sourced by pin DLC/$\overline{\text{MUTER}}$ in mute receive condition	V_{DLC} = 0.2 V	–	80	–	µA
ΔG_{vrxm}	voltage gain reduction in mute receive condition	V_{DLC} < 0.2 V	–	80	–	dB
Envelope and noise detectors (TSEN, TENV, RSEN and RENV)						
PREAMPLIFIERS						
$G_{v(TSEN)}$	voltage gain from MIC to TSEN		38	40	42	dB
$G_{v(RSEN)}$	voltage gain between RIN1 and RIN2 to RSEN.		–2	0	+2	dB
LOGARITHMIC COMPRESSOR AND SENSITIVITY ADJUSTMENT						
$\Delta V_{det(TSEN)}$	sensitivity detection on pin TSEN; voltage change on pin TENV when doubling the current from TSEN	I_{TSEN} = 0.8 to 160 µA	–	18	–	mV
$\Delta V_{det(RSEN)}$	sensitivity detection on pin RSEN; voltage change on pin RENV when doubling the current from RSEN	I_{RSEN} = 0.8 to 160 µA	–	18	–	mV
SIGNAL ENVELOPE DETECTORS						
$I_{source(ENV)}$	maximum current sourced from pin TENV or RENV		–	120	–	µA
$I_{sink(ENV)}$	maximum current sunk by pin TENV or RENV		0.75	1	1.25	µA
ΔV_{ENV}	voltage difference between pin RENV and TENV	when 10 µA is sourced from both RSEN and TSEN; envelope detectors tracking; note 5	–	±3	–	mV
NOISE ENVELOPE DETECTORS						
$I_{source(NOI)}$	maximum current sourced from pin TNOI or RNOI		0.75	1	1.25	µA
$I_{sink(NOI)}$	maximum current sunk by pin TNOI or RNOI		–	120	–	µA
ΔV_{NOI}	voltage difference between pin RNOI and TNOI	when 5 µA is sourced from both RSEN and TSEN; noise detectors tracking; note 5	–	±3	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DIAL TONE DETECTOR						
$V_{RINDT(rms)}$	threshold level at pin RIN1 and RIN2 (RMS value)		–	127	–	mV
Decision logic (IDT and SWT)						
SIGNAL RECOGNITION						
$\Delta V_{Srx(th)}$	threshold voltage between pin RENV and RNOI to switch-over from receive to idle mode	$V_{RIN} < V_{RINDT}$; note 6	–	13	–	mV
$\Delta V_{Stx(th)}$	threshold voltage between pin TENV and TNOI to switch-over from transmit to idle mode	note 6	–	13	–	mV
SWITCH-OVER						
$I_{source(SWT)}$	current sourced from pin SWT when switching to receive mode		7.5	10	12.5	µA
$I_{sink(SWT)}$	current sunk by pin SWT when switching to transmit mode		7.5	10	12.5	µA
$I_{idle(SWT)}$	current sourced from pin SWT in idle mode		–	0	–	µA
Voice switch (STAB and SWR)						
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment with R_{SWR} referenced to 365 kΩ		–40	–	12	dB
$\lvert\Delta G_v\rvert$	voltage gain variation from transmit mode to idle mode on both channels		–	20	–	dB
G_{tr}	gain tracking ($G_{vtx} + G_{vrx}$) during switching, referenced to idle mode		–	±0.5	–	dB

Notes

1. Corresponds to 5 mW output power.
2. Corresponds to 20 mW output power.
3. Corresponds to 40 mW output power.
4. Corresponds to 100 mW output power.
5. Corresponds to ±1 dB tracking.
6. Corresponds to 4.3 dB noise/speech recognition level.

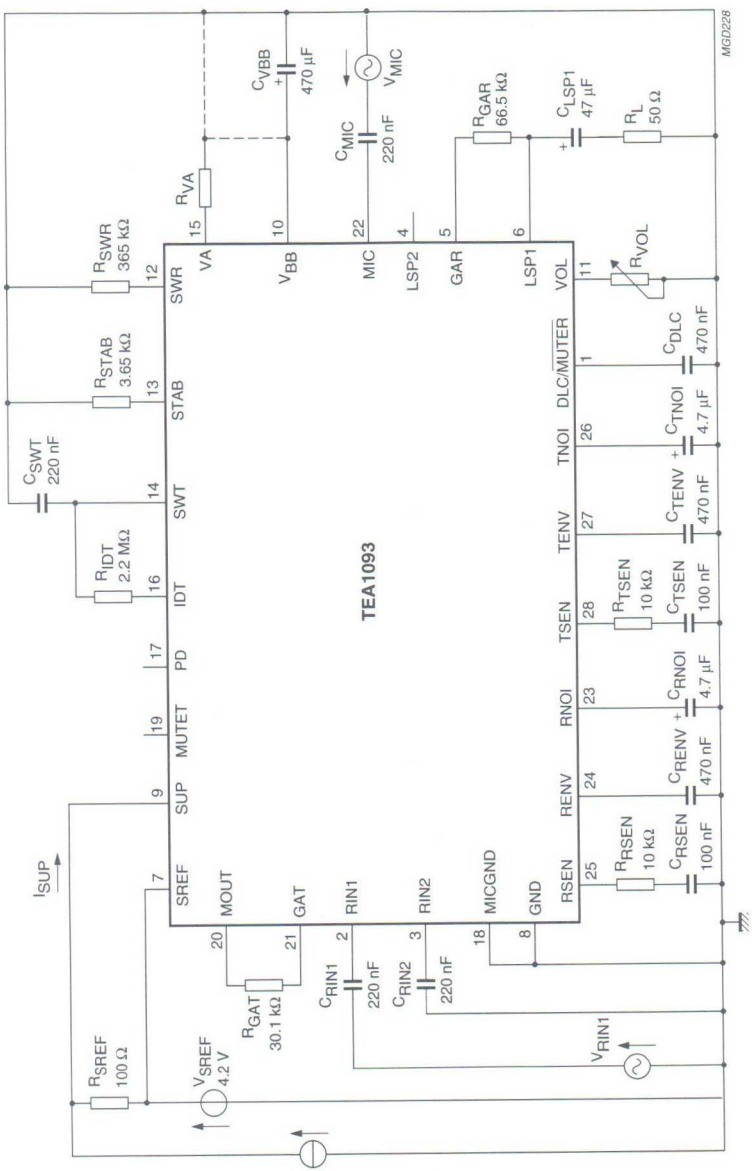


Fig.15 Test circuit.

APPLICATION INFORMATION

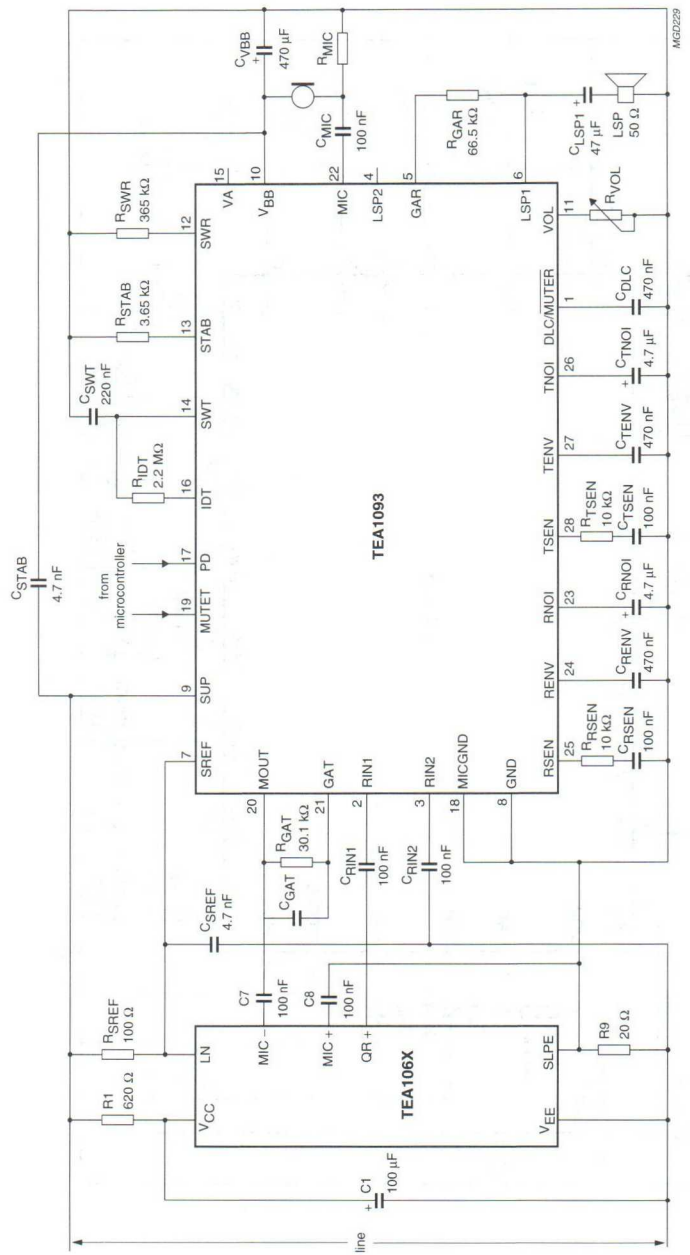


Fig.16 Basic application diagram.

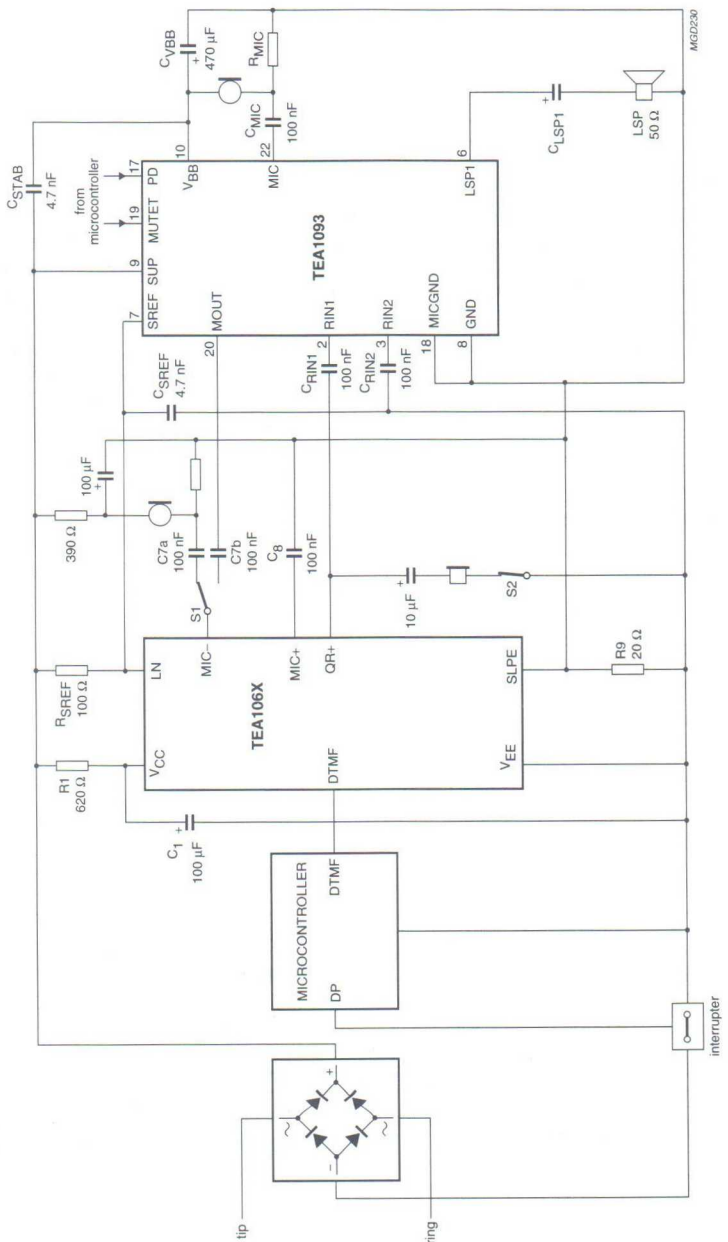


Fig.17 Application proposal.

FEATURES

- Low power consumption
- Power-down function (TEA1094A only)
- Microphone channel with:
  - externally adjustable gain
  - microphone mute function.
- Loudspeaker channel with:
  - externally adjustable gain
  - dynamic limiter to prevent distortion
  - rail-to-rail output stage for single-ended load drive
  - logarithmic volume control via linear potentiometer
  - loudspeaker mute function.
- Duplex controller consisting of:
  - signal envelope and noise envelope monitors for both channels with:
    externally adjustable sensitivity
    externally adjustable signal envelope time constant
    externally adjustable noise envelope time constant
  - decision logic with:
    externally adjustable switch-over timing
    externally adjustable idle mode timing
    externally adjustable dial tone detector in receive channel
  - voice switch control with:
    adjustable switching range
    constant sum of gain during switching
    constant sum of gain at different volume settings.

APPLICATIONS

- Mains, battery or line-powered telephone sets with hands-free/listening-in functions
- Cordless telephones
- Answering machines
- Fax machines.

GENERAL DESCRIPTION

The TEA1094 and TEA1094A are bipolar circuits intended for use in mains, battery or line-powered telephone sets, cordless telephones, answering machines and Fax machines. In conjunction with a member of the TEA106X, TEA111X families of transmission circuits, the devices offer a hands-free function. They incorporate a microphone amplifier, a loudspeaker amplifier and a duplex controller with signal and noise monitors on both channels.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1094	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TEA1094A	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
TEA1094T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TEA1094AT	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TEA1094AM	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

QUICK REFERENCE DATA

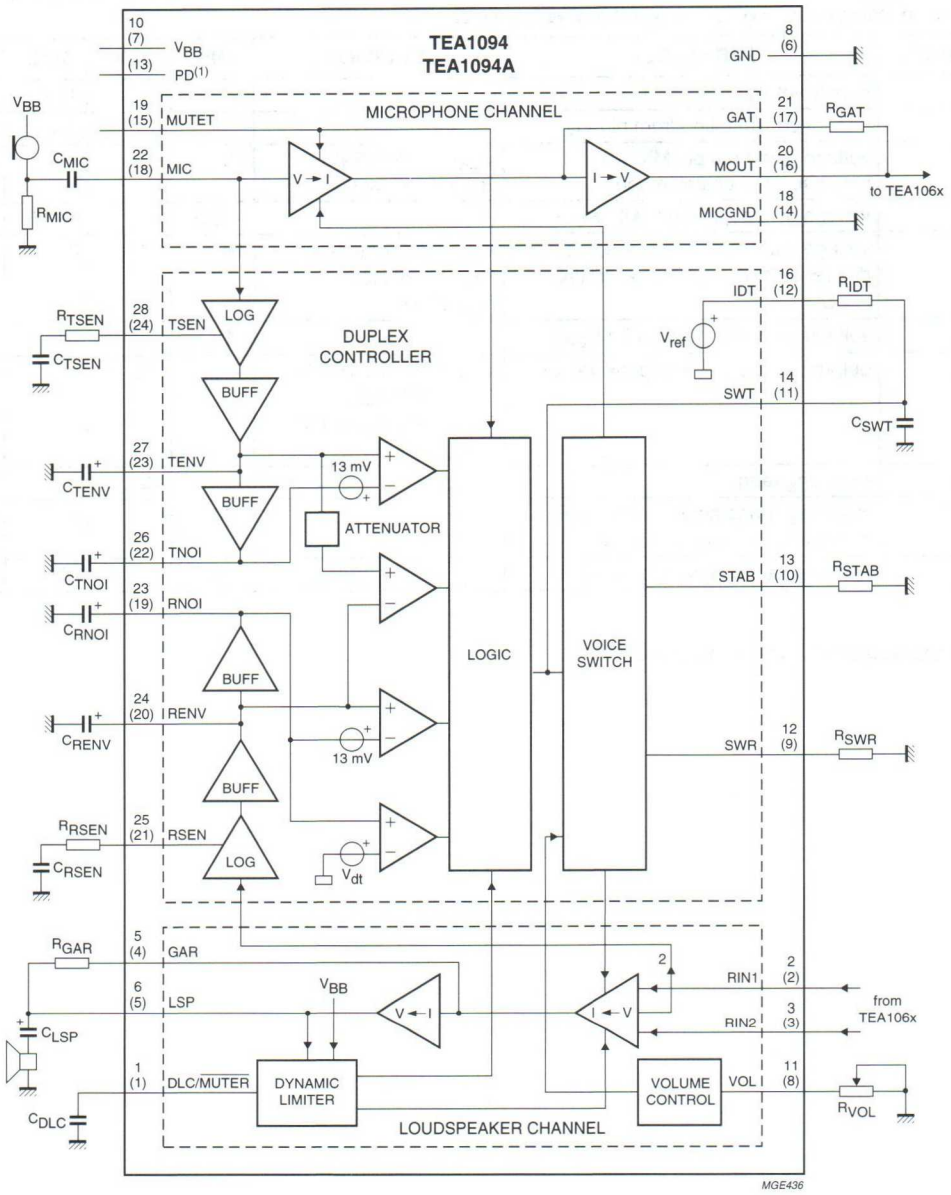
V_{BB} = 5 V; V_{GND} = 0 V; f = 1 kHz; T_{amb} = 25 °C; MUTET = LOW; PD = LOW (TEA1094A only); R_L = 50 Ω; R_{VOL} = 0 Ω; measured in test circuit of Fig.12; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BB}	supply voltage		3.3	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	3.1	4.4	mA
G_{vtx}	voltage gain from pin MIC to pin MOUT in transmit mode	V_{MIC} = 1 mV (RMS); R_{GAT} = 30.1 kΩ	13	15.5	18	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAT}		−15.5	–	+15.5	dB
G_{vrx}	voltage gain in receive mode; the difference between RIN1 and RIN2 to LSP	V_{RIN} = 20 mV (RMS); R_{GAR} = 66.5 kΩ; R_L = 50 Ω	16	18.5	21	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		−18.5	–	+14.5	dB
$V_{O(p-p)}$	output voltage (peak-to-peak value)	V_{RIN} = 150 mV (RMS); R_{GAR} = 374 kΩ; R_L = 33 Ω; V_{BB} = 9.0 V; note 1	–	7.5	–	V
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment with R_{SWR} referenced to R_{SWR} = 365 kΩ		−40	–	+12	dB
T_{amb}	operating ambient temperature		−25	–	+75	°C

Note

1. Corresponds to 200 mW output power.

BLOCK DIAGRAM



The pin numbers given in parenthesis are for the TEA1094A.

(1) TEA1094A only.

Fig.1 Block diagram.

PINNING

SYMBOL	PINS		DESCRIPTION
	TEA1094	TEA1094A	
DLC/$\overline{\text{MUTER}}$	1	1	dynamic limiter timing adjustment; receiver channel mute input
RIN1	2	2	receiver amplifier input 1
RIN2	3	3	receiver amplifier input 2
n.c.	4	–	not connected
GAR	5	4	receiver gain adjustment
LSP	6	5	loudspeaker amplifier output
n.c.	7	–	not connected
GND	8	6	ground reference
n.c.	9	–	not connected
V_{BB}	10	7	supply voltage
VOL	11	8	receiver volume adjustment
SWR	12	9	switching range adjustment
STAB	13	10	reference current adjustment
SWT	14	11	switch-over timing adjustment
n.c.	15	–	not connected
IDT	16	12	idle mode timing adjustment
PD	–	13	power-down input
n.c.	17	–	not connected
MICGND	18	14	ground reference for the microphone amplifier
MUTET	19	15	transmit channel mute input
MOUT	20	16	microphone amplifier output
GAT	21	17	microphone gain adjustment
MIC	22	18	microphone input
RNOI	23	19	receive noise envelope timing adjustment
RENV	24	20	receive signal envelope timing adjustment
RSEN	25	21	receive signal envelope sensitivity adjustment
TNOI	26	22	transmit noise envelope timing adjustment
TENV	27	23	transmit signal envelope timing adjustment
TSEN	28	24	transmit signal envelope sensitivity adjustment

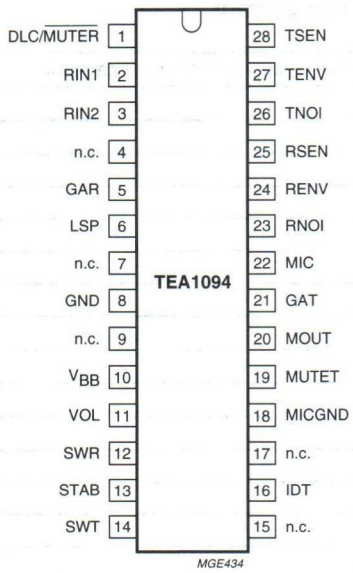


Fig.2 Pin configuration (TEA1094).

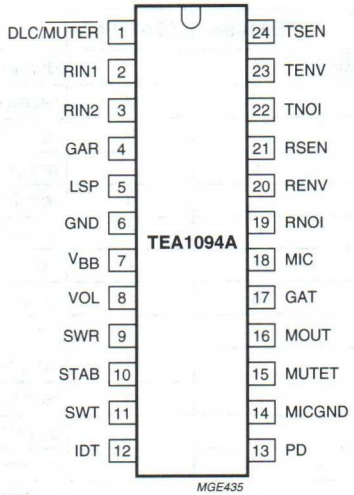


Fig.3 Pin configuration (TEA1094A).

FUNCTIONAL DESCRIPTION

General

The values given in the functional description are typical values unless otherwise specified.

A principle diagram of the TEA106X is shown on the left side of Fig.4. The TEA106X is a transmission circuit of the TEA1060 family intended for hand-set operation.
It incorporates a receiving amplifier for the earpiece, a transmit amplifier for the microphone and a hybrid.
For more details on the TEA1060 family, please refer to *"data Handbook IC03"*. The right side of Fig.4 shows a principle diagram of the TEA1094 and TEA1094A, hands-free add-on circuits with a microphone amplifier, a loudspeaker amplifier and a duplex controller.

As can be seen from Fig.4, a loop is formed via the sidetone network in the transmission circuit and the acoustic coupling between loudspeaker and microphone of the hands-free circuit. When this loop gain is greater than 1, howling is introduced. In a full duplex application, this would be the case.
The loop-gain has to be much lower than 1 and therefore has to be decreased to avoid howling. This is achieved by the duplex controller. The duplex controller of the TEA1094 and TEA1094A detects which channel has the 'largest' signal and then controls the gain of the microphone amplifier and the loudspeaker amplifier so that the sum of the gains remains constant.
As a result, the circuit can be in three stable modes:

1. Transmit mode (Tx mode).

   The gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum.

2. Receive mode (Rx mode).

   The gain of the loudspeaker amplifier is at its maximum and the gain of the microphone amplifier is at its minimum.

3. Idle mode.

   The gain of the amplifiers is halfway between their maximum and minimum value.

The difference between the maximum gain and minimum gain is called the switching range.

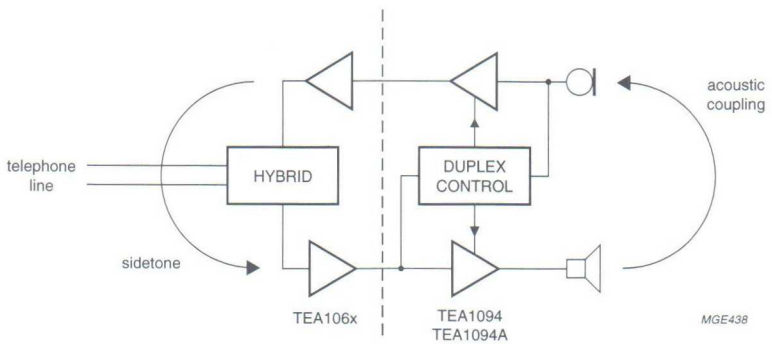


Fig.4 Hands-free telephone set principles.

Supply: pins V_{BB}, GND and PD

The TEA1094 and TEA1094A must be supplied with an external stabilized voltage source between pins V_{BB} and GND. In the idle mode, without any signal, the internal supply current is 3.1 mA at V_{BB} = 5 V.

To reduce the current consumption during pulse dialling or register recall (flash), the TEA1094A is provided with a power-down (PD) input. When the voltage on PD is HIGH the current consumption from V_{BB} is 180 μA.

Microphone channel: pins MIC, GAT, MOUT, MICGND and MUTET (see Fig.5)

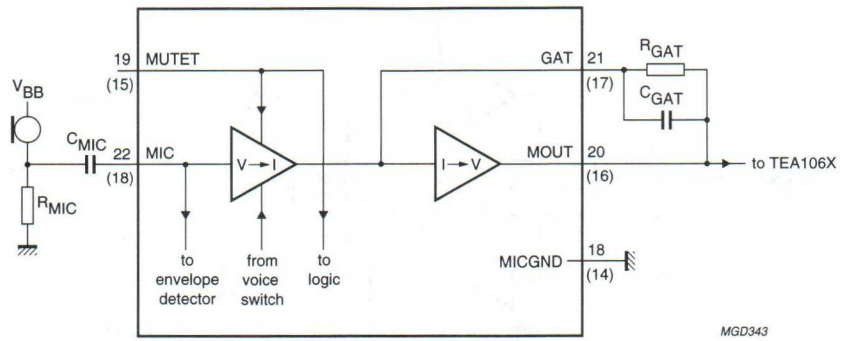
The TEA1094 and TEA1094A have an asymmetrical microphone input MIC with an input resistance of 20 kΩ. The gain of the input stage varies according to the mode of the TEA1094 and TEA1094A. In the transmit mode, the gain is at its maximum; in the receive mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum.

Switch-over from one mode to the other is smooth and click-free. The output capability at pin MOUT is 20 μA (RMS).

In the transmit mode, the overall gain of the microphone amplifier (from pins MIC to MOUT) can be adjusted from 0 dB up to 31 dB to suit specific application requirements. The gain is proportional to the value of R_{GAT} and equals 15.5 dB with R_{GAT} = 30.1 kΩ.

A capacitor must be connected in parallel with R_{GAT} to ensure stability of the microphone amplifier. Together with R_{GAT}, it also provides a first-order low-pass filter.

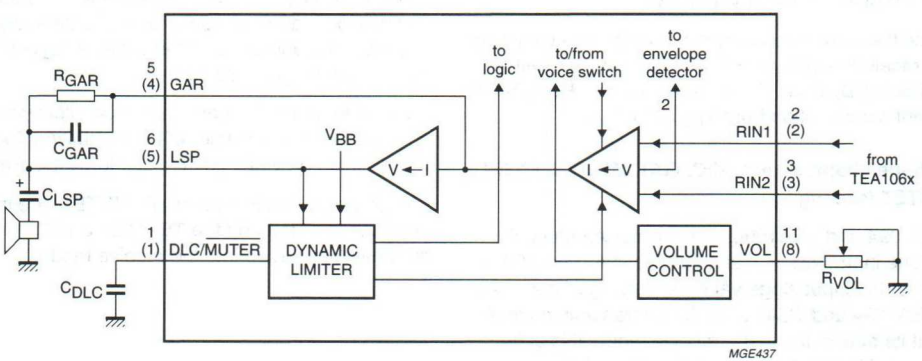
By applying a HIGH level on pin MUTET, the microphone amplifier is muted and the TEA1094 and TEA1094A are automatically forced into the receive mode.



The pin numbers given in parenthesis refer to the TEA1094A.

Fig.5 Microphone channel.

Loudspeaker channel



The pin numbers given in parenthesis refer to the TEA1094A.

Fig.6 Loudspeaker channel.

LOUDSPEAKER AMPLIFIER: PINS RIN1, RIN2, GAR AND LSP

The TEA1094 and TEA1094A have symmetrical inputs for the loudspeaker amplifier with an input resistance of 40 kΩ between RIN1 and RIN2 (2 × 20 kΩ). The input stage can accommodate signals up to 390 mV (RMS) at room temperature for 2% of total harmonic distortion (THD). The gain of the input stage varies according to the mode of the TEA1094 and TEA1094A. In the receive mode, the gain is at its maximum; in the transmit mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The rail-to-rail output stage is designed to power a loudspeaker connected as a single-ended load (between LSP and GND).

In the receive mode, the overall gain of the loudspeaker amplifier can be adjusted from 0 dB up to 33 dB to suit specific application requirements. The gain from RIN1 and RIN2 to LSP is proportional to the value of R_{GAR} and equals 18.5 dB with R_{GAR} = 66.5 kΩ. A capacitor connected in parallel with R_{GAR} can be used to provide a first-order low-pass filter.

VOLUME CONTROL: PIN VOL

The loudspeaker amplifier gain can be adjusted with the potentiometer R_{VOL}. A linear potentiometer can be used to obtain logarithmic control of the gain at the loudspeaker amplifier. Each 950 Ω increase of R_{VOL} results in a gain loss of 3 dB. The maximum gain reduction with the volume control is internally limited to the switching range.

DYNAMIC LIMITER: PIN DLC/$\overline{\text{MUTER}}$

The dynamic limiter of the TEA1094 and TEA1094A prevents clipping of the loudspeaker output stage and protects the operation of the circuit when the supply voltage at V_{BB} falls below 2.9 V.

Hard clipping of the loudspeaker output stage is prevented by rapidly reducing the gain when the output stage starts to saturate. The time in which gain reduction is effected (clipping attack time) is approximately a few milliseconds. The circuit stays in the reduced gain mode until the peaks of the loudspeaker signals no longer cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time (typically 250 ms). Both attack and release times are proportional to the value of the capacitor C_{DLC}. The total harmonic distortion of the loudspeaker output stage, in reduced gain mode, stays below 5% up to 10 dB (minimum) of input voltage overdrive [providing V_{RIN} is below 390 mV (RMS)].

When the supply voltage drops below an internal threshold voltage of 2.9 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). When the supply voltage exceeds 2.9 V, the gain of the loudspeaker amplifier is increased again.

By forcing a level lower than 0.2 V on pin DLC/$\overline{\text{MUTER}}$, the loudspeaker amplifier is muted and the TEA1094 (TEA1094A) is automatically forced into the transmit mode.

Duplex controller

SIGNAL AND NOISE ENVELOPE DETECTORS: PINS TSEN, TENV, TNOI, RSEN, RENV AND RNOI

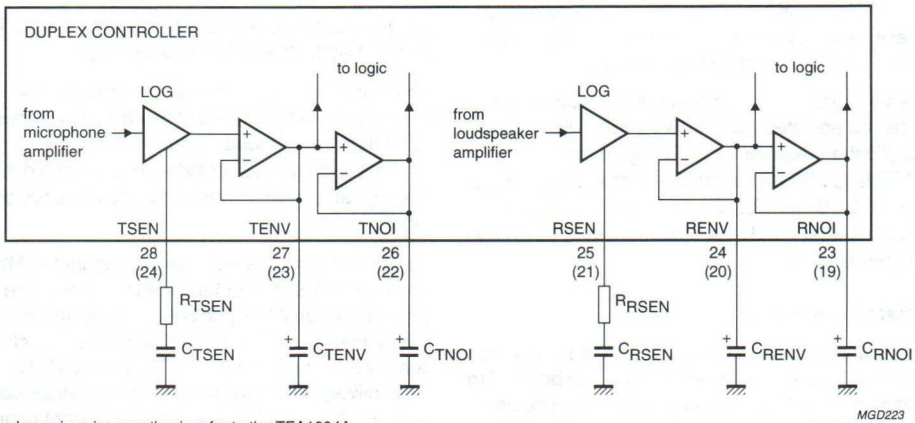
The signal envelopes are used to monitor the signal level strength in both channels. The noise envelopes are used to monitor background noise in both channels. The signal and noise envelopes provide inputs for the decision logic. The signal and noise envelope detectors are shown in Fig.7.

For the transmit channel, the input signal at MIC is 40 dB amplified to TSEN. For the receive channel, the differential signal between RIN1 and RIN2 is 0 dB amplified to RSEN. The signals from TSEN and RSEN are logarithmically compressed and buffered to TENV and RENV respectively. The sensitivity of the envelope detectors is set with R_{TSEN} and R_{RSEN}. The capacitors connected in series with the two resistors block any DC component and form a first-order high-pass filter. In the basic application, see Fig.13, it is assumed that V_{MIC} = 1 mV (RMS) and V_{RIN} = 100 mV (RMS) nominal and both R_{TSEN} and R_{RSEN} have a value of 10 kΩ. With the value of C_{TSEN} and C_{RSEN} at 100 nF, the cut-off frequency is at 160 Hz.

The buffer amplifiers leading the compressed signals to TENV and RENV have a maximum source current of 120 μA and a maximum sink current of 1 μA. Together with the capacitor C_{TENV} and C_{RENV}, the timing of the signal envelope monitors can be set. In the basic application, the value of both capacitors is 470 nF. Because of the logarithmic compression, each 6 dB signal increase means 18 mV increase of the voltage on the envelopes TENV or RENV at room temperature. Thus, timings can be expressed in dB/ms. At room temperature, the 120 μA sourced current corresponds to a maximum rise-slope of the signal envelope of 85 dB/ms. This is sufficient to track normal speech signals. The 1 μA current sunk by TENV or RENV corresponds to a maximum fall-slope of 0.7 dB/ms. This is sufficient for a smooth envelope and also eliminates the effect of echoes on switching behaviour.

To determine the noise level, the signals on TENV and RENV are buffered to TNOI and RNOI. These buffers have a maximum source current of 1 μA and a maximum sink current of 120 μA. Together with the capacitors C_{TNOI} and C_{RNOI}, the timing can be set. In the basic application of Fig.13 the value of both capacitors is 4.7 μF. At room temperature, the 1 μA sourced current corresponds to a maximum rise-slope of the noise envelope of approximately 0.07 dB/ms.

This is small enough to track background noise and not to be influenced by speech bursts. The 120 μA current that is sunk corresponds to a maximum fall-slope of approximately 8.5 dB/ms. However, during the decrease of the signal envelope, the noise envelope tracks the signal envelope so it will never fall faster than approximately 0.7 dB/ms. The behaviour of the signal envelope and noise envelope monitors is illustrated in Fig.8.



The pin numbers given in parenthesis refer to the TEA1094A.

Fig.7 Signal and noise envelope detectors.

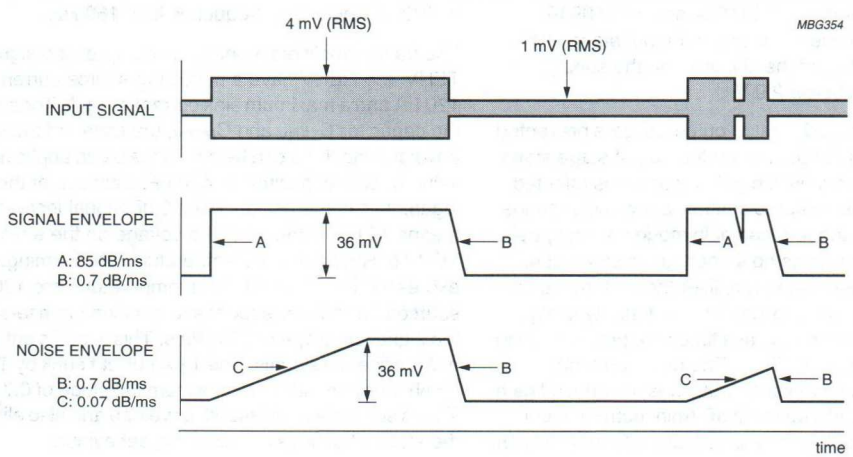
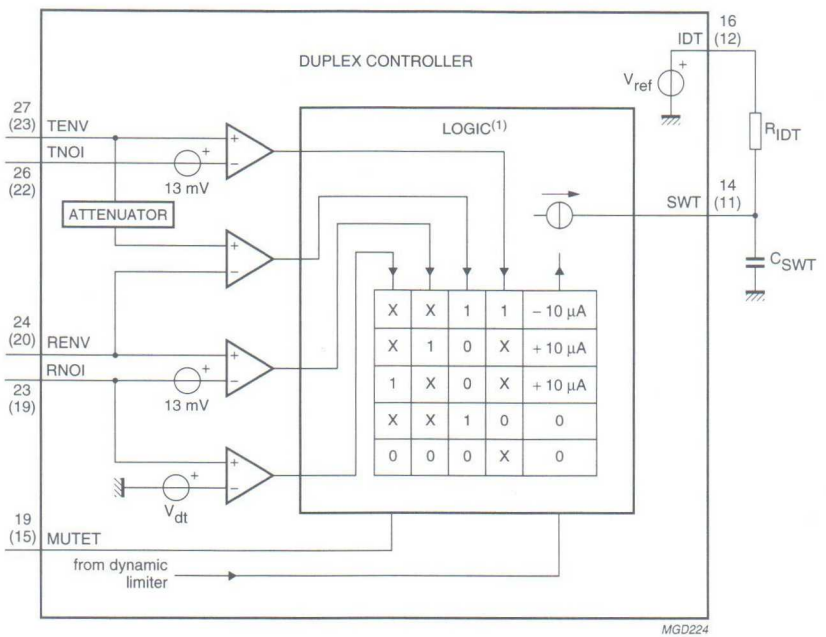


Fig.8 Signal and noise envelope waveforms.

DECISION LOGIC: PINS IDT AND SWT



The pin numbers given in parenthesis refer to the TEA1094A.

(1) When MUTET = HIGH, +10 µA is forced.
When DLC/$\overline{\text{MUTER}}$ < 0.2 V, −10 µA is forced.

Fig.9 Decision logic.

The TEA1094 and TEA1094A select their modes of operation (transmit, receive or idle mode) by comparing the signal and the noise envelopes of both channels. This is executed by the decision logic. The resulting voltage on pin SWT is the input for the voice-switch.

To facilitate the distinction between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference $V_{ENV} - V_{NOI} = 13$ mV. This so called speech/noise threshold is implemented in both channels.

The signal on MIC contains both speech and the signal coming from the loudspeaker (acoustic coupling). When receiving, the contribution from the loudspeaker overrules the speech.

As a result, the signal envelope on TENV is formed mainly by the loudspeaker signal. To correct this, an attenuator is connected between TENV and the TENV/RENV comparator. Its attenuation equals that applied to the microphone amplifier.

When a dial tone is present on the line, without monitoring, the tone would be recognized as noise because it is a signal with a constant amplitude. This would cause the TEA1094 (TEA1094A) to go into the idle mode and the user of the set would hear the dial tone fade away. To prevent this, a dial tone detector is incorporated which, in standard applications, does not consider input signals between RIN1 and RIN2 as noise when they have a level greater than 127 mV (RMS). This level is proportional to R_{RSEN}.

As can be seen from Fig.9, the output of the decision logic is a current source. The logic table gives the relationship between the inputs and the value of the current source. It can charge or discharge the capacitor C_{SWT} with a current of 10 μA (switch-over). If the current is zero, the voltage on SWT becomes equal to the voltage on IDT via the high-ohmic resistor R_{IDT} (idling). The resulting voltage difference between SWT and IDT determines the mode of the TEA1094 (TEA1094A) and can vary between −400 and +400 mV (see Table 1).

Table 1 Modes of TEA1094; TEA1094A

$V_{SWT} - V_{IDT}$ (mV)	MODE
<−180	transmit mode
0	idle mode
>180	receive mode

The switch-over timing can be set with C_{SWT}, the idle mode timing with C_{SWT} and R_{IDT}. In the basic application given in Fig.13, C_{SWT} is 220 nF and R_{IDT} is 2.2 MΩ. This enables a switch-over time from transmit to receive mode or vice-versa of approximately 13 ms (580 mV swing on SWT). The switch-over time from idle mode to transmit mode or receive mode is approximately 4 ms (180 mV swing on SWT).

The switch-over time, from receive mode or transmit mode to idle mode, is equal to $4 \times R_{IDT}C_{SWT}$ and is approximately 2 seconds (idle mode time).

The inputs MUTET and DLC/$\overline{\text{MUTER}}$ overrule the decision logic. When MUTET goes HIGH, the capacitor C_{SWT} is charged with 10 μA thus resulting in the receive mode. When the voltage on pin DLC/$\overline{\text{MUTER}}$ goes lower than 0.2 V, the capacitor C_{SWT} is discharged with 10 μA thus resulting in the transmit mode.

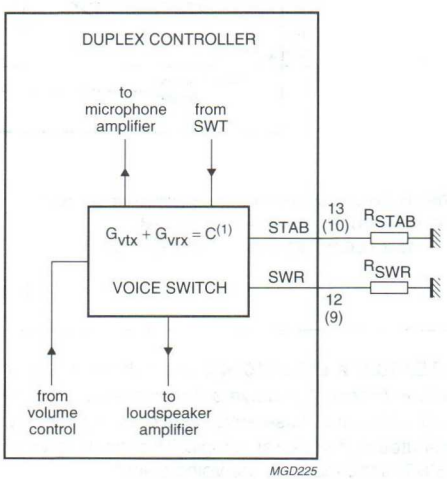
VOICE-SWITCH: PINS STAB AND SWR

A diagram of the voice-switch is illustrated in Fig.10. With the voltage on SWT, the TEA1094 (TEA1094A) voice-switch regulates the gains of the transmit and the receive channel so that the sum of both is kept constant.

In the transmit mode, the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum. In the receive mode, the opposite applies. In the idle mode, both microphone and loudspeaker amplifier gains are halfway.

The difference between maximum and minimum is the so called switching range. This range is determined by the ratio of R_{SWR} and R_{STAB} and is adjustable between 0 and 52 dB. R_{STAB} should be 3.65 kΩ and sets an internally used reference current. In the basic application diagram given in Fig.13, R_{SWR} is 365 kΩ which results in a switching range of 40 dB. The switch-over behaviour is illustrated in Fig.11.

In the receive mode, the gain of the loudspeaker amplifier can be reduced using the volume control. Since the voice-switch keeps the sum of the gains constant, the gain of the microphone amplifier is increased at the same time (see dashed curves in Fig.11). In the transmit mode, however, the volume control has no influence on the gain of the microphone amplifier or the gain of the loudspeaker amplifier. Consequently, the switching range is reduced when the volume is reduced. At maximum reduction of volume, the switching range becomes 0 dB.



The pin numbers given in parenthesis refer to the TEA1094A.

(1) C = constant.

Fig.10 Voice switch.

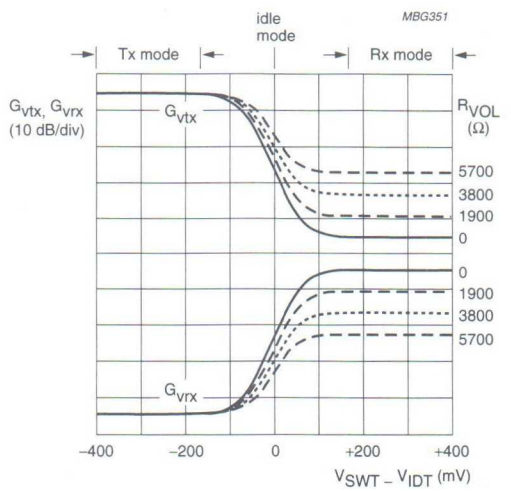


Fig.11 Switch-over behaviour.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{n(max)}$	maximum voltage on all pins; except pins V_{BB}, RIN1 and RIN2		V_{GND} − 0.4	V_{BB} + 0.4	V
$V_{RIN(max)}$	maximum voltage on pins RIN1 and RIN2		V_{GND} − 1.2	V_{BB} + 0.4	V
$V_{BB(max)}$	maximum voltage on pin V_{BB}		V_{GND} − 0.4	12.0	V
P_{tot}	total power dissipation	T_{amb} = 75 °C			
	TEA1094		−	1000	mW
	TEA1094A		−	910	mW
	TEA1094T		−	625	mW
	TEA1094AT		−	590	mW
	TEA1094AM		−	438	mW
T_{stg}	IC storage temperature		−40	+125	°C
T_{amb}	operating ambient temperature		−25	+75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1094	45	K/W
	TEA1094A	50	K/W
	TEA1094T	70	K/W
	TEA1094AT	75	K/W
	TEA1094AM	104	K/W

CHARACTERISTICS

V_{BB} = 5 V; V_{GND} = 0 V; f = 1 kHz; T_{amb} = 25 °C; MUTET = LOW; PD = LOW (TEA1094A only); R_L = 50 Ω; R_{VOL} = 0 Ω; measured in test circuit of Fig.12; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (V_{BB}, GND and PD)						
V_{BB}	supply voltage		3.3	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	3.1	4.4	mA
POWER-DOWN INPUT PD (TEA1094A ONLY)						
V_{IL}	LOW level input voltage		V_{GND} – 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{PD}	input current	PD = HIGH	–	2.5	5	µA
$I_{BB(PD)}$	current consumption from pin V_{BB} in power-down condition	PD = HIGH	–	180	240	µA
Microphone channel (MIC, GAT, MOUT, MUTET and MICGND)						
MICROPHONE AMPLIFIER						
$\|Z_i\|$	input impedance between pins MIC and MICGND		17	20	23	kΩ
G_{vtx}	voltage gain from pin MIC to MOUT in transmit mode	V_{MIC} = 1 mV (RMS)	13	15.5	18	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAT}		−15.5	–	+15.5	dB
ΔG_{vtxT}	voltage gain variation with temperature referenced to 25 °C	V_{MIC} = 1 mV (RMS); T_{amb} = −25 to +75 °C	–	±0.3	–	dB
ΔG_{vtxf}	voltage gain variation with frequency referenced to 1 kHz	V_{MIC} = 1 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
V_{notx}	noise output voltage at pin MOUT	pin MIC connected to MICGND through 200 Ω in series with 10 µF; psophometrically weighted (P53 curve)	–	−100	–	dBmp

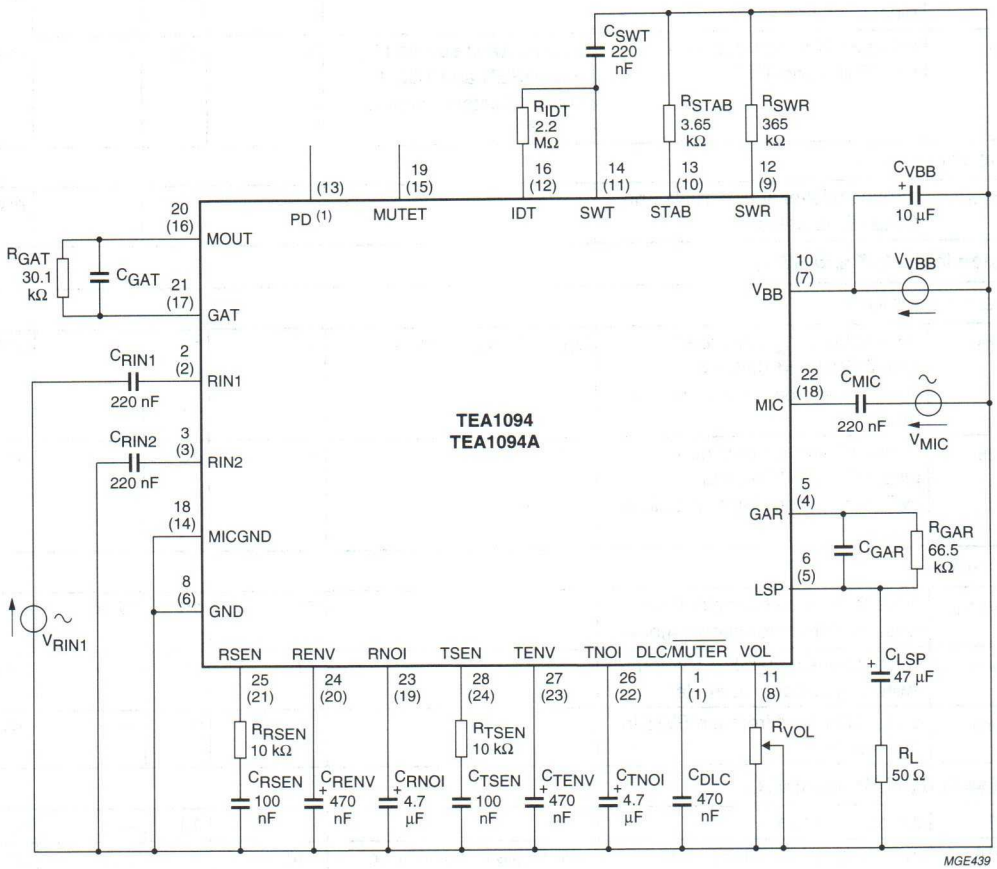
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TRANSMIT MUTE INPUT MUTET						
V_{IL}	LOW level input voltage		V_{GND} – 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{MUTET}	input current	MUTET = HIGH	–	2.5	5	μA
ΔG_{vtxm}	voltage gain reduction with MUTET active	MUTET = HIGH	–	80	–	dB
Loudspeaker channel (RIN1, RIN2, GAR, LSP and DLC/$\overline{\text{MUTER}}$)						
LOUDSPEAKER AMPLIFIER						
$\lvert Z_i \rvert$	input impedance	between pins RIN1 or RIN2 and GND	17	20	23	kΩ
		between pins RIN1 and RIN2	34	40	46	kΩ
G_{vrx}	voltage gain in receive mode; between RIN1 and RIN2 to LSP	V_{RIN} = 20 mV (RMS)	16	18.5	21	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		−18.5	–	+14.5	dB
ΔG_{vrxT}	voltage gain variation with temperature referenced to 25 °C	V_{RIN} = 20 mV (RMS); T_{amb} = −25 to +75 °C	–	±0.3	–	dB
ΔG_{vrxf}	voltage gain variation with frequency referenced to 1 kHz	V_{RIN} = 20 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
$V_{RIN(rms)}$	maximum input voltage between RIN1 and RIN2 (RMS value)	R_{GAR} = 11.8 kΩ; for 2% THD in input stage	–	390	–	mV
$V_{norx(rms)}$	noise output voltage at pin LSP (RMS value)	inputs RIN1 and RIN2 short-circuited through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	–	80	–	μV
CMRR	common mode rejection ratio		–	50	–	dB
ΔG_{vrxv}	voltage gain variation related to ΔR_{VOL} = 950 Ω	when total attenuation does not exceed the switching range	–	3	–	dB
OUTPUT CAPABILITY						
$V_{OSE(p-p)}$	output voltage (peak-to-peak value)	V_{RIN} = 300 mV (RMS); note 1	3.5	4.5	–	V
		V_{RIN} = 150 mV (RMS); R_{GAR} = 374 kΩ; R_L = 33 Ω; V_{BB} = 9.0 V; note 2	–	7.5	–	V
I_{OM}	maximum output current at LSP (peak value)		150	500	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DYNAMIC LIMITER						
t_{att}	attack time when V_{RIN} jumps from 20 mV to 20 mV + 10 dB	R_{GAR} = 374 kΩ	–	–	5	ms
t_{rel}	release time when V_{RIN} jumps from 20 mV + 10 dB to 20 mV	R_{GAR} = 374 kΩ	–	250	–	ms
THD	total harmonic distortion at V_{RIN} = 20 mV + 10 dB	R_{GAR} = 374 kΩ; $t > t_{att}$	–	0.9	5	%
$V_{BB(th)}$	V_{BB} limiter threshold		–	2.9	–	V
t_{att}	attack time when V_{BB} jumps below $V_{BB(th)}$		–	1	–	ms
MUTE RECEIVE						
$V_{DLC(th)}$	threshold voltage required on pin DLC/$\overline{\text{MUTER}}$ to obtain mute receive condition		V_{GND} – 0.4	–	0.2	V
$I_{DLC(th)}$	threshold current sourced by pin DLC/$\overline{\text{MUTER}}$ in mute receive condition	V_{DLC} = 0.2 V	–	100	–	µA
ΔG_{vrxm}	voltage gain reduction in mute receive condition	V_{DLC} < 0.2 V	–	80	–	dB
Envelope and noise detectors (TSEN, TENV, RSEN, RENV, RNOI and TNOI)						
PREAMPLIFIERS						
$G_{v(TSEN)}$	voltage gain from MIC to TSEN		37.5	40	42.5	dB
$G_{v(RSEN)}$	voltage gain between RIN1 and RIN2 to RSEN		–2.5	0	+2.5	dB
LOGARITHMIC COMPRESSOR AND SENSITIVITY ADJUSTMENT						
$\Delta V_{det(TSEN)}$	sensitivity detection on pin TSEN; voltage change on pin TENV when doubling the current from TSEN	I_{TSEN} = 0.8 to 160 µA	–	18	–	mV
$\Delta V_{det(RSEN)}$	sensitivity detection on pin RSEN; voltage change on pin RENV when doubling the current from RSEN	I_{RSEN} = 0.8 to 160 µA	–	18	–	mV
SIGNAL ENVELOPE DETECTORS						
$I_{source(ENV)}$	maximum current sourced from pin TENV or RENV		–	120	–	µA
$I_{sink(ENV)}$	maximum current sunk by pin TENV or RENV		0.75	1	1.25	µA
ΔV_{ENV}	voltage difference between pins RENV and TENV	when 10 µA is sourced from both RSEN and TSEN; envelope detectors tracking; note 3	–	±3	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
NOISE ENVELOPE DETECTORS						
$I_{source(NOI)}$	maximum current sourced from pins TNOI or RNOI		0.75	1	1.25	μA
$I_{sink(NOI)}$	maximum current sunk by pins TNOI or RNOI		–	120	–	μA
ΔV_{NOI}	voltage difference between pins RNOI and TNOI	when 5 μA is sourced from both RSEN and TSEN; noise detectors tracking; note 3	–	±3	–	mV
DIAL TONE DETECTOR						
$V_{RINDT(rms)}$	threshold level at pins RIN1 and RIN2 (RMS value)		–	127	–	mV
Decision logic (IDT and SWT)						
SIGNAL RECOGNITION						
$\Delta V_{Srx(th)}$	threshold voltage between pins RENV and RNOI to switch-over from receive to idle mode	$V_{RIN} < V_{RINDT}$; note 4	–	13	–	mV
$\Delta V_{Stx(th)}$	threshold voltage between pins TENV and TNOI to switch-over from transmit to idle mode	note 4	–	13	–	mV
SWITCH-OVER						
$I_{source(SWT)}$	current sourced from pin SWT when switching to receive mode		7.5	10	12.5	μA
$I_{sink(SWT)}$	current sunk by pin SWT when switching to transmit mode		7.5	10	12.5	μA
$I_{idle(SWT)}$	current sourced from pin SWT in idle mode		–	0	–	μA
Voice switch (STAB and SWR)						
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referenced to 365 kΩ	–40	–	+12	dB
$\lvert\Delta G_v\rvert$	voltage gain variation from transmit mode to idle mode on both channels		–	20	–	dB
G_{tr}	gain tracking ($G_{vtx} + G_{vrx}$) during switching, referenced to idle mode		–	±0.5	–	dB

Notes

1. Corresponds to 50 mW output power.
2. Corresponds to 200 mW output power.
3. Corresponds to ±1 dB tracking.
4. Corresponds to 4.3 dB noise/speech recognition level.



The pin numbers given in parenthesis refer to the TEA1094A.

(1) TEA1094A only.

Fig.12 Test circuit.

APPLICATION INFORMATION

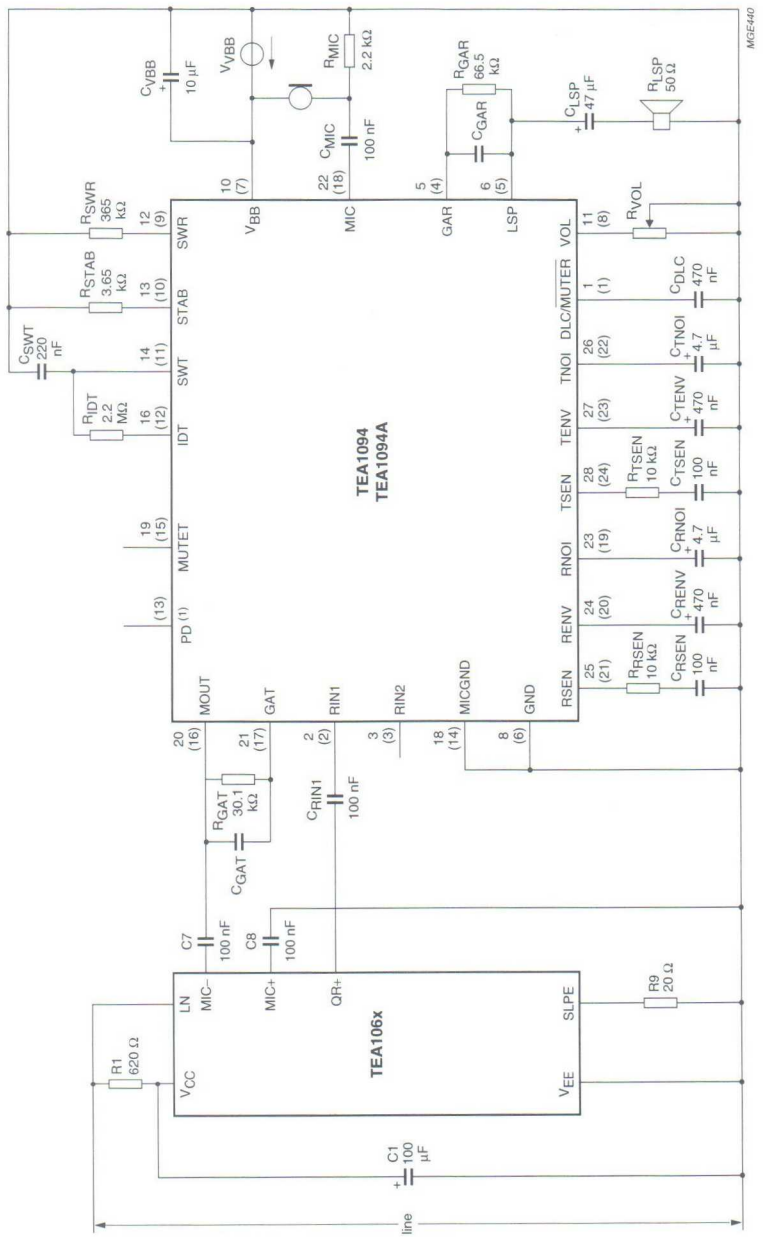


Fig.13 Basic application diagram.

The pin numbers given in parenthesis refer to the TEA1094A.

(1) TEA1094A only.

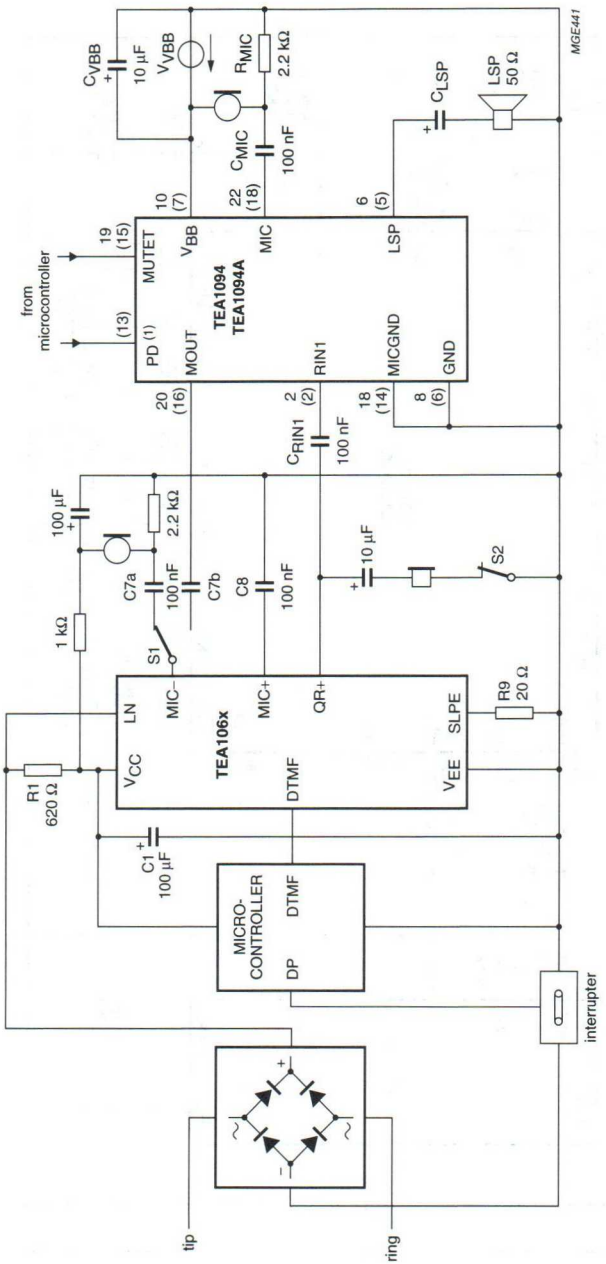


Fig.14 Application example.

The pin numbers given in parenthesis refer to the TEA1094A.
(1) TEA1094A only.

Voice switched speakerphone IC TEA1095

FEATURES

- External power supply with power-down function
- Transmit channel with:
  - externally adjustable gain
  - transmit mute function
- Receive channel with:
  - externally adjustable gain
  - logarithmic volume control via a linear potentiometer
  - receive mute function
- Duplex controller consisting of:
  - signal envelope and noise envelope monitors for both channels with:

    externally adjustable sensitivity

    externally adjustable signal envelope time constant

    externally adjustable noise envelope time constant
  - decision logic with:

    externally adjustable switch-over timing

    externally adjustable idle mode timing

    externally adjustable dial tone detector in receive channel
  - voice switch control with:

    adjustable switching range

    constant sum of gain during switching

    constant sum of gain at different volume settings.

APPLICATIONS

- Mains, battery or line-powered telephone sets
- Cordless telephones
- Answering machines
- Fax machines
- Hands-free car kits.

GENERAL DESCRIPTION

The TEA1095 is a bipolar circuit, that in conjunction with a member of the TEA106X, TEA111X families of transmission or TEA1096 transmission/listening-in circuits offers a hands-free function. It incorporates a transmit amplifier, a receiver channel amplifier and a duplex controller with signal and noise monitors on both channels.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1095	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
TEA1095T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TEA1095TS	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

QUICK REFERENCE DATA

V_{BB} = 5 V; V_{GND} = 0 V; f = 1 kHz; T_{amb} = 25 °C; MUTETX = LOW; MUTERX = LOW; PD = LOW; R_{VOL} = 0 Ω; measured in test circuit of Fig.11; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BB}	supply voltage		2.9	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	2.7	3.8	mA
G_{vtx}	voltage gain from TXIN to TXOUT in transmit mode	V_{TXIN} = 1 mV (RMS); R_{GATX} = 30.1 kΩ	–	15.5	–	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GATX}		−15.5	–	+24.5	dB
G_{vrx}	voltage gain from RXIN to RXOUT in receive mode	V_{RXIN} = 20 mV (RMS); R_{GARX} = 16.5 kΩ	–	6.5	–	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GARX}		−20.5	–	+19.5	dB
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referenced to R_{SWR} = 365 kΩ	−40	–	+12	dB
T_{amb}	operating ambient temperature		−25	–	+75	°C

BLOCK DIAGRAM

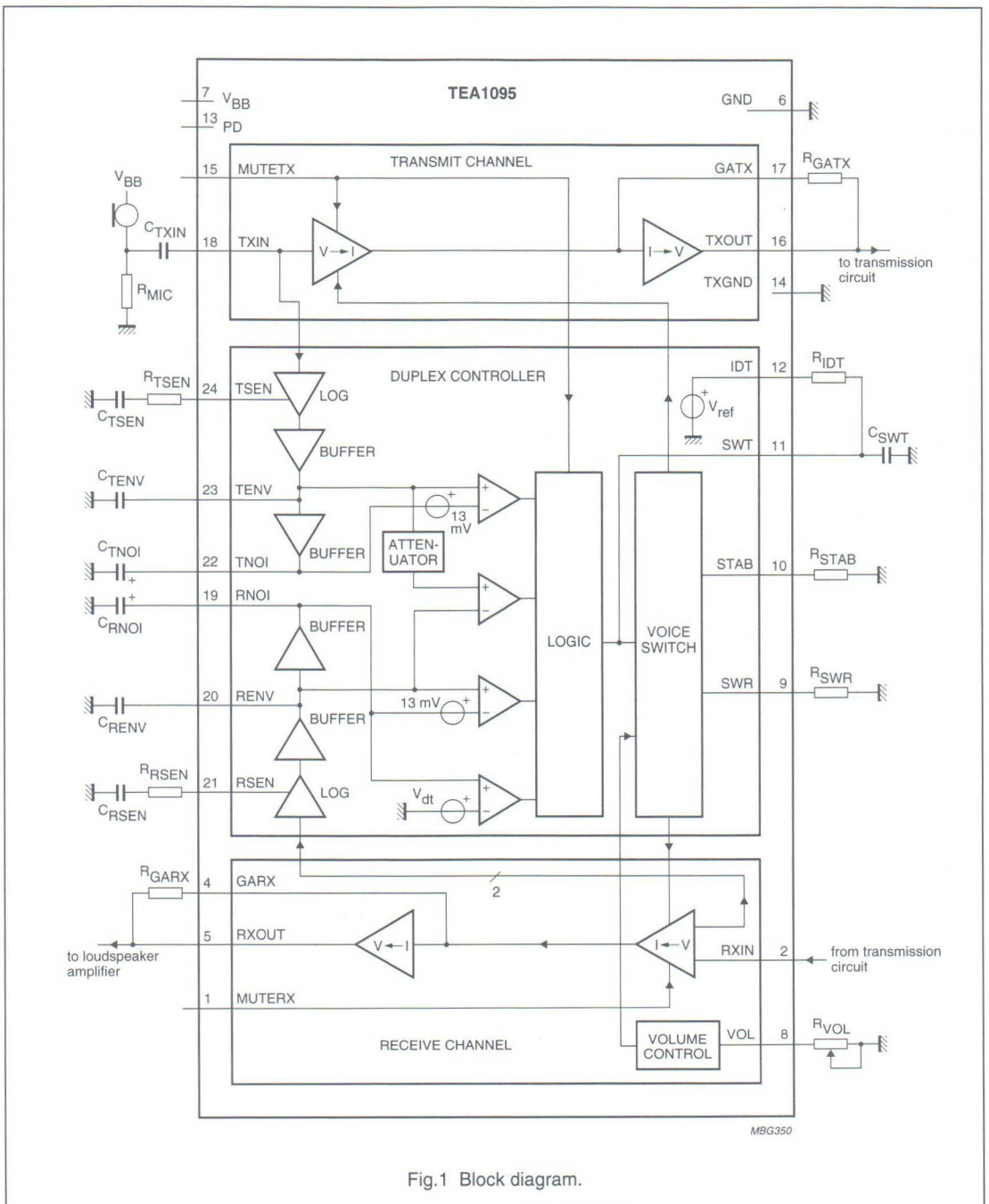


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
MUTERX	1	receiver channel mute input
RXIN	2	receiver amplifier input
n.c.	3	not connected
GARX	4	receiver gain adjustment
RXOUT	5	receiver amplifier output
GND	6	ground reference
V_{BB}	7	supply voltage input
VOL	8	receiver volume adjustment
SWR	9	switching range adjustment
STAB	10	reference current adjustment
SWT	11	switch-over timing adjustment
IDT	12	idle mode timing adjustment
PD	13	power-down input
TXGND	14	ground reference for the transmit channel
MUTETX	15	transmit channel mute input
TXOUT	16	transmit amplifier output
GATX	17	transmit gain adjustment
TXIN	18	transmit amplifier input
RNOI	19	receive noise envelope timing adjustment
RENV	20	receive signal envelope timing adjustment
RSEN	21	receive signal envelope sensitivity adjustment
TNOI	22	transmit noise envelope timing adjustment
TENV	23	transmit signal envelope timing adjustment
TSEN	24	transmit signal envelope sensitivity adjustment

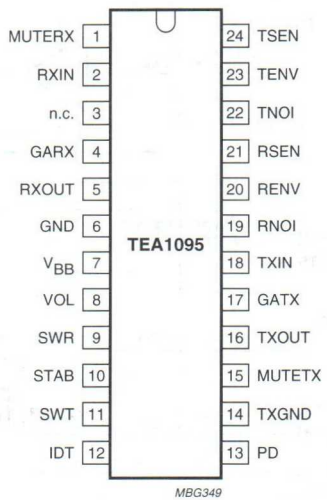


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The values given in the functional description are typical values except when otherwise specified.

A principle diagram of the TEA1096 is shown on the left side of Fig.3. The TEA1096 is a transmission and listening-in circuit. It incorporates a receiving amplifier for the earpiece, a transmit amplifier for the microphone, a loudspeaker amplifier and a hybrid. For more details on the TEA1096 circuit (please refer to *Data Handbook IC03*). The right side of Fig.3 shows a principle diagram of the TEA1095, a hands-free add-on circuit with a transmit amplifier, a receiver amplifier and a duplex controller.

As can be seen from Fig.3, a loop is formed via the sidetone network in the transmission circuit and the acoustic coupling between loudspeaker and microphone of the hands-free circuit. When this loop gain is greater than 1, howling is introduced. In a full duplex application, this would be the case. The loop-gain has to be much lower than 1 and therefore has to be decreased to avoid howling. This is achieved by the duplex controller. The duplex controller of the TEA1095 detects which channel has the 'largest' signal and then controls the gains of the transmit amplifier and the receiver amplifier such that the sum of the gains remains constant. As a result, the circuit can be in three stable modes:

1. Transmit mode (Tx mode): the gain of the transmit amplifier is at its maximum and the gain of the receiver amplifier is at its minimum.
2. Receive mode (Rx mode): the gain of the receiver amplifier is at its maximum and the gain of the transmit amplifier is at its minimum.
3. Idle mode: the gain of the amplifiers is halfway between their maximum and minimum value.

The difference between the maximum gain and minimum gain is called the switching range.

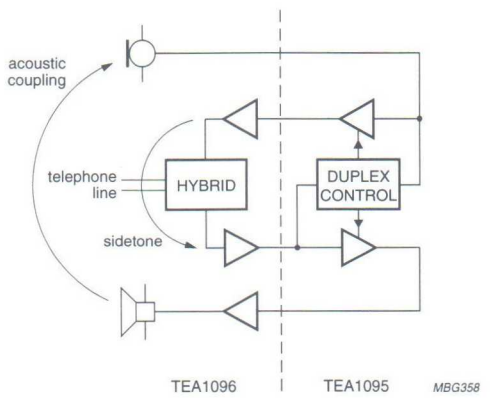


Fig.3 Hands-free telephone set principles.

Supply: pins V_{BB}, GND and PD

The TEA1095 must be supplied with an external stabilized voltage source between pins V_{BB} and GND. In idle mode, without any signal, the internal supply current is 2.7 mA at V_{BB} = 5 V.

To reduce current consumption during pulse dialling or register recall (flash), the TEA1095 is provided with a power-down (PD) input. When the voltage on PD is HIGH, the current consumption from V_{BB} is 140 μA.

Transmit channel: pins TXIN, GATX, TXOUT, TXGND and MUTETX

The TEA1095 has an asymmetrical transmit input (TXIN) with an input resistance of 20 kΩ. The gain of the input stage varies according to the mode of the TEA1095. In the transmit mode, the gain is at its maximum; in the receive mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The output capability at pin TXOUT is 20 μA (RMS).

In the transmit mode, the overall gain of the transmit amplifier (from pin TXIN to TXOUT) can be adjusted from 0 dB to 40 dB to suit application specific requirements. The gain is proportional to the value of R_{GATX} and equals 15.5 dB with R_{GATX} = 30.1 kΩ.

A capacitor must be connected in parallel with R_{GATX} to ensure stability of the transmit amplifier. Together with R_{GATX}, it also provides a first-order low-pass filter.

By applying a HIGH level on pin MUTETX, the transmit amplifier is muted and the TEA1095 is automatically forced into the receive mode.

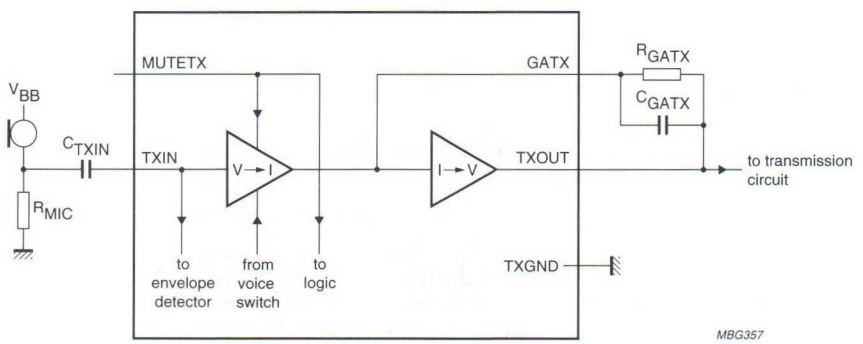


Fig.4 Transmit channel.

Receive channel

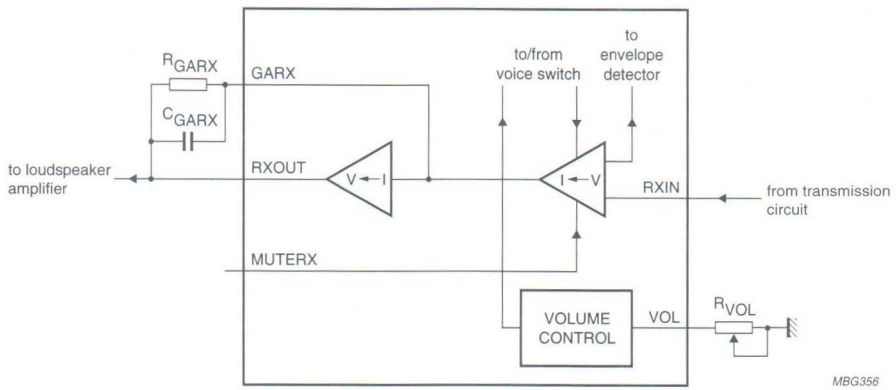


Fig.5 Receive channel.

RECEIVER AMPLIFIER: PINS RXIN, GARX, RXOUT AND MUTERX

The TEA1095 has an asymmetrical input (RXIN) for the receiver amplifier with an input resistance of 20 kΩ. The gain of the input stage varies according to the mode of the TEA1095. In the receive mode, the gain is at its maximum; in the transmit mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free.

In the receive mode, the overall gain of the receive amplifier can be adjusted from −14 dB to +26 dB to suit application specific requirements. The gain from RXIN to RXOUT is proportional to the value of R_{GARX} and equals 6.5 dB with R_{GARX} = 16.5 kΩ. A capacitor connected in parallel with R_{GARX} can be used to provide a first-order low-pass filter.

By applying a HIGH level on pin MUTERX, the receiver amplifier is muted and the TEA1095 is automatically forced into the transmit mode.

VOLUME CONTROL: PIN VOL

The receiver amplifier gain can be adjusted with the potentiometer R_{VOL}. A linear potentiometer can be used to obtain logarithmic control of the gain of the receiver amplifier. Each 950 Ω increase of R_{VOL} results in a gain loss of 3 dB. The maximum gain reduction with the volume control is internally limited to the switching range.

Duplex controller

SIGNAL AND NOISE ENVELOPE DETECTORS: PINS TSEN, TENV, TNOI, RSEN, RENV AND RNOI

The signal envelopes are used to monitor the signal level strength in both channels. The noise envelopes are used to monitor background noise in both channels. The signal and noise envelopes provide inputs for the decision logic. The signal and noise envelopes detectors are shown in Fig.6.

For the transmit channel, the input signal at TXIN is 40 dB amplified to TSEN. For the receive channel, the input signal at RXIN is 0 dB amplified to RSEN. The signals from TSEN and RSEN are logarithmically compressed and buffered to TENV and RENV respectively. The sensitivity of the envelope detectors is set with R_{TSEN} and R_{RSEN}.

The capacitors connected in series with the two resistors block any DC component and form a first order high-pass filter. In the basic application (see Fig.12), it is assumed that V_{TXIN} = 1 mV (RMS) and V_{RXIN} = 100 mV (RMS) nominal and both R_{TSEN} and R_{RSEN} have a value of 10 kΩ. With the value of C_{TSEN} and C_{RSEN} at 100 nF, the cut-off frequency is at 160 Hz.

The buffer amplifiers leading the compressed signals to TENV and RENV have a maximum source current of 120 μA and a maximum sink current of 1 μA. Together with the capacitors C_{TENV} and C_{RENV}, the timing of the signal envelope monitors can be set. In the basic application, the value of both capacitors is 470 nF. Because of the logarithmic compression, each 6 dB signal increase means 18 mV increase of the voltage on the envelopes TENV or RENV at room temperature. Thus, timings can be expressed in dB/ms. At room temperature, the 120 μA sourced current corresponds to a maximum rise-slope of the signal envelope of 85 dB/ms. This is enough to track normal speech signals. The 1 μA current sunk by TENV or RENV corresponds to a maximum fall-slope of 0.7 dB/ms. This is enough for a smooth envelope and also eliminates the effect of echoes on switching behaviour.

To determine the noise level, the signal on TENV and RENV are buffered to TNOI and RNOI. These buffers have a maximum source current of 1 μA and a maximum sink current of 120 μA. Together with the capacitors C_{TNOI} and C_{RNOI}, the timing can be set. In the basic application of Fig.12, the value of both capacitors is 4.7 μF. At room temperature, the 1 μA sourced current corresponds to a maximum rise-slope of the noise envelope of approximately 0.07 dB/ms. This is small enough to track background noise and not to be influenced by speech bursts. The 120 μA current that is sunk corresponds to a maximum fall-slope of approximately 8.5 dB/ms. However, during the decrease of the signal envelope, the noise envelope tracks the signal envelope so it will never fall faster than approximately 0.7 dB/ms. The behaviour of the signal envelope and noise envelope monitors is illustrated in Fig.7.

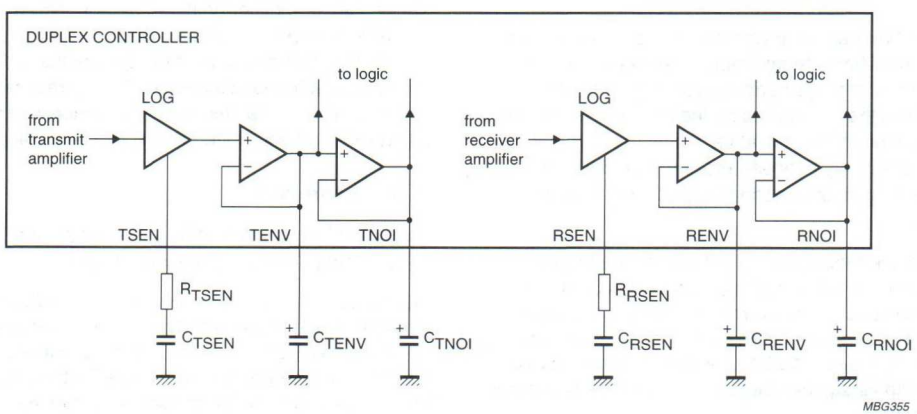


Fig.6 Signal and noise envelope detectors.

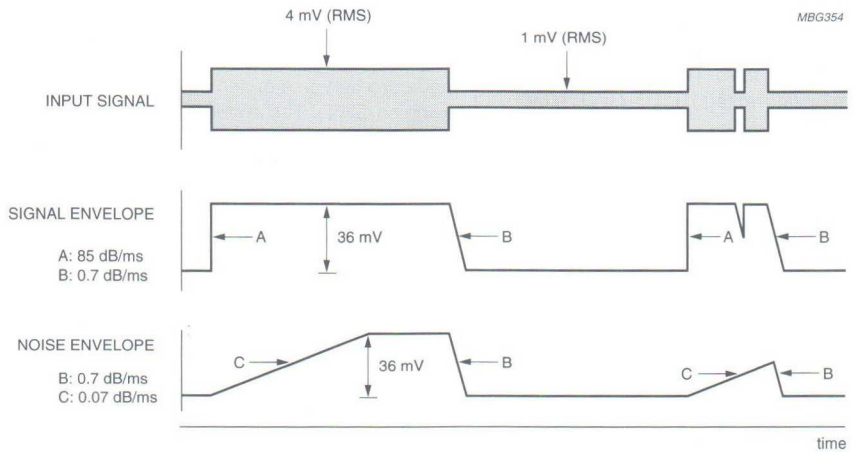
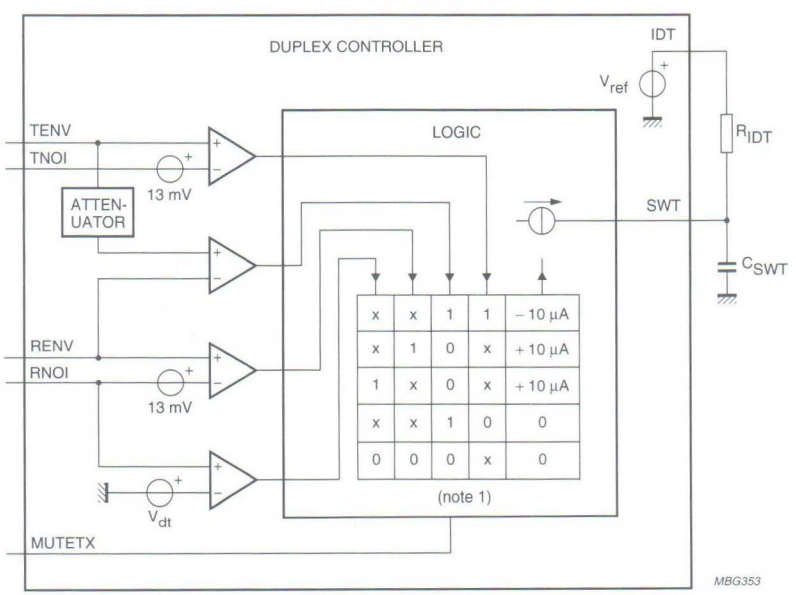


Fig.7 Signal and noise envelope waveforms.



x	x	1	1	− 10 µA
x	1	0	x	+ 10 µA
1	x	0	x	+ 10 µA
x	x	1	0	0
0	0	0	x	0

(1) When MUTETX = HIGH +10 µA is forced. When MUTERX = HIGH −10 µA is forced.

Fig.8 Decision logic.

DECISION LOGIC: PINS IDT AND SWT

The TEA1095 selects its mode of operation (transmit, receive or idle mode) by comparing the signal and the noise envelopes of both channels. This is executed by the decision logic. The resulting voltage on pin SWT is the input for the voice-switch.

To facilitate the distinction between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference $V_{ENV-NOI}$ = 13 mV. This so called speech/noise threshold is implemented in both channels.

The signal on TXIN contains both speech and the signal coming from the loudspeaker (acoustic coupling). When receiving, the contribution from the loudspeaker overrules the speech. As a result, the signal envelope on TENV is formed mainly by the loudspeaker signal. To correct this, an attenuator is connected between TENV and the TENV/RENV comparator. Its attenuation equals that applied to the transmit amplifier.

When a dial tone is present on the line, without monitoring, the tone would be recognized as noise because it is a signal with a constant amplitude. This would cause the TEA1095 to go into the idle mode and the user of the set would hear the dial tone fade away. To prevent this, a dial tone detector is incorporated which, in standard application, does not consider the input signals at RXIN as noise when they have a level greater than 42 mV (RMS). This level is proportional to R_{RSEN}.

As can be seen from Fig.8, the output of the decision logic is a current source. The logic table gives the relationship between the inputs and the value of the current source. It can charge or discharge the capacitor C_{SWT} with a current of 10 μA (switch-over). If the current is zero, the voltage on SWT becomes equal to the voltage on IDT via the high ohmic resistor R_{IDT} (idling). The resulting voltage difference between SWT and IDT determines the mode of the TEA1095 and can vary between −400 mV and +400 mV.

Table 1 Modes of TEA1095

$V_{SWT} - V_{IDT}$ (mV)	MODE
<−180	transmit mode
0	idle mode
>180	receive mode

The switch-over timing can be set with C_{SWT}, the idle mode timing with C_{SWT} and R_{IDT}. In the basic application given in Fig.12, C_{SWT} is chosen at 220 nF and R_{IDT} at 2.2 MΩ. This enables a switch-over time from transmit to receive mode or vice-versa of approximately 13 ms (580 mV swing on SWT). The switch-over time from idle mode to transmit mode or receive mode is approximately 4 ms (180 mV swing on SWT).

The switch-over time from receive mode or transmit mode to idle mode is equal to $4 \times R_{IDT}\ C_{SWT}$ and is approximately 2 s (idle mode time).

The inputs MUTETX and MUTERX overrule the decision logic. When MUTETX goes HIGH, the capacitor C_{SWT} is charged with 10 μA resulting in the receive mode. When the voltage on pin MUTERX goes HIGH, the capacitor C_{SWT} is discharged with 10 μA resulting in the transmit mode.

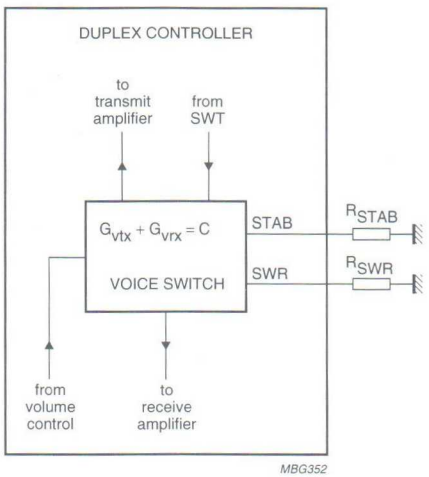
VOICE-SWITCH: PINS STAB AND SWR

A diagram of the voice-switch is illustrated in Fig.9. With the voltage on SWT, the TEA1095 voice-switch regulates the gains of the transmit and the receive channel such that the sum of both is kept constant.

In the transmit mode, the gain of the transmit amplifier is at its maximum and the gain of the receive amplifier is at its minimum. In the receive mode, the opposite applies. In the idle mode, both transmit and receive amplifier gains are halfway.

The difference between maximum and minimum is the so called switching range. This range is determined by the ratio of R_{SWR} and R_{STAB} and is adjustable between 0 and 52 dB. R_{STAB} should be equal to 3.65 kΩ and sets an internally used reference current. In the basic application diagram given in Fig.12, R_{SWR} is equal to 365 kΩ which results in a switching range of 40 dB. The switch-over behaviour is illustrated in Fig.10.

In the receive mode, the gain of the receive amplifier can be reduced using the volume control. Since the voice-switch keeps the sum of the gains constant, the gain of the transmit amplifier is increased at the same time (see dashed curves in Fig.10). In the transmit mode however, the volume control has no influence on the gain of the transmit amplifier or the gain of the receive amplifier. Consequently, the switching range is reduced when the volume is reduced. At maximum reduction of volume, the switching range becomes 0 dB.



Where C = constant.

Fig.9 Voice switch.

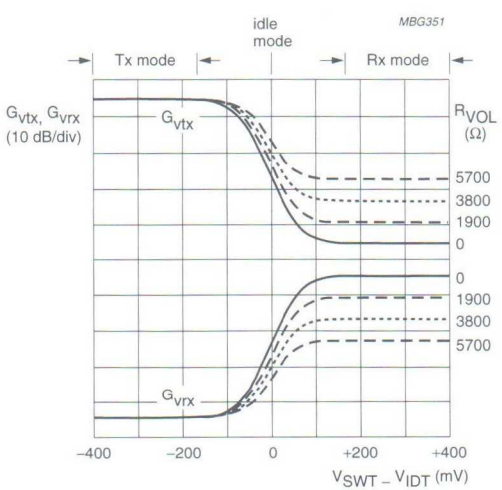


Fig.10 Switch-over behaviour.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{n(max)}$	maximum voltage on all pins; except pins V_{BB} and RXIN		V_{GND} – 0.4	V_{BB} + 0.4	V
$V_{RIN(max)}$	maximum voltage on pin RXIN		V_{GND} – 1.2	V_{BB} + 0.4	V
$V_{BB(max)}$	maximum voltage on pin V_{BB}		V_{GND} – 0.4	12.0	V
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1095	50	K/W
	TEA1095T	75	K/W
	TEA1095TS	104	K/W

CHARACTERISTICS

V_{BB} = 5 V; V_{GND} = 0 V; f = 1 kHz; T_{amb} = 25 °C; MUTETX = LOW; MUTERX = LOW; PD = LOW; R_{VOL} = 0 Ω; measured in test circuit of Fig.11; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (V_{BB}, PD and GND)						
V_{BB}	supply voltage		2.9	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	2.7	3.8	mA
POWER-DOWN INPUT PD						
V_{IL}	LOW level input voltage		V_{GND} – 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{PD}	power-down input current	PD = HIGH	–	2.5	5	µA
$I_{BB(PD)}$	current consumption from pin V_{BB} in power-down mode	PD = HIGH	–	140	190	µA
Transmit channel (TXIN, GATX, TXOUT, MUTETX and TXGND)						
TRANSMIT AMPLIFIER						
$\lvert Z_i \rvert$	input impedance between pins TXIN and TXGND		17	20	23	kΩ
G_{vtx}	voltage gain from TXIN to TXOUT in transmit mode	V_{TXIN} = 1 mV (RMS); R_{GATX} = 30.1 kΩ	–	15.5	–	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GATX}		–15.5	–	+24.5	dB
ΔG_{vtxT}	voltage gain variation with temperature referenced to 25 °C	V_{TXIN} = 1 mV (RMS); T_{amb} = –25 to +75 °C	–	±0.3	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_{vtxf}	voltage gain variation with frequency referenced to 1 kHz	V_{TXIN} = 1 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
V_{notx}	noise output voltage at pin TXOUT	pin TXIN connected to TXGND through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	–	–100	–	dBmp
TRANSMIT MUTE INPUT MUTETX						
V_{IL}	LOW level input voltage		V_{GND} – 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{MUTETX}	input current	MUTETX = HIGH	–	2.5	5	μA
ΔG_{vtxm}	voltage gain reduction with MUTETX active	MUTETX = HIGH	–	80	–	dB
Receive channel (RXIN, GARX, RXOUT and MUTERX)						
RECEIVE AMPLIFIER						
$\|Z_i\|$	input impedance between pins RXIN and GND		17	20	23	kΩ
G_{vrx}	voltage gain from RXIN to RXOUT in receive mode	V_{RXIN} = 20 mV (RMS); R_{GARX} = 16.5 kΩ	–	6.5	–	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GARX}		–20.5	–	+19.5	dB
ΔG_{vrxT}	voltage gain variation with temperature referenced to 25 °C	V_{RXIN} = 20 mV (RMS); T_{amb} = –25 to +75 °C	–	±0.3	–	dB
ΔG_{vrxf}	voltage gain variation with frequency referenced to 1 kHz	V_{RXIN} = 20 mV (RMS); f_i = 300 to 3400 Hz	–	±0.3	–	dB
$V_{norx(rms)}$	noise output voltage at pin RXOUT (RMS value)	input RXIN short-circuited through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	–	20	–	μV
ΔG_{vrxv}	voltage gain variation referenced to ΔR_{VOL} = 950 Ω	when total attenuation does not exceed the switching range	–	3	–	dB
RECEIVE MUTE INPUT MUTERX						
V_{IL}	LOW level input voltage		V_{GND} – 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{MUTERX}	input current	MUTERX = HIGH	–	2.5	5	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_{vrxm}	gain reduction with MUTERX active	MUTERX = HIGH	–	80	–	dB
Envelope and noise detectors (TSEN, TENV, TNOI, RSEN, RENV and RNOI)						
PREAMPLIFIERS						
$G_{v(TSEN)}$	voltage gain from TXIN to TSEN		–	40	–	dB
$G_{v(RSEN)}$	voltage gain between RXIN to RSEN		–	0	–	dB
LOGARITHMIC COMPRESSOR AND SENSITIVITY ADJUSTMENT						
$\varphi_{det(TSEN)}$	sensitivity detection on pin TSEN; voltage change on pin TENV when doubling the current from TSEN	I_{TSEN} = 0.8 to 160 μA	–	18	–	mV
$\varphi_{det(RSEN)}$	sensitivity detection on pin RSEN; voltage change on pin RENV when doubling the current from RSEN	I_{RSEN} = 0.8 to 160 μA	–	18	–	mV
SIGNAL ENVELOPE DETECTORS						
$I_{source(ENV)}$	maximum current sourced from pin TENV or RENV		–	120	–	μA
$I_{sink(ENV)}$	maximum current sunk by pin TENV or RENV		0.75	1	1.25	μA
ΔV_{ENV}	voltage difference between pins RENV and TENV	when 10 μA is sourced from both RSEN and TSEN; envelope detectors tracking; note 1	–	±3	–	mV
NOISE ENVELOPE DETECTORS						
$I_{source(NOI)}$	maximum current sourced from pins TNOI or RNOI		0.75	1	1.25	μA
$I_{sink(NOI)}$	maximum current sunk by pins TNOI or RNOI		–	120	–	μA
ΔV_{NOI}	voltage difference between pins RNOI and TNOI	when 2 μA is sourced from both RSEN and TSEN; noise detectors tracking; note 1	–	±3	–	mV
DIAL TONE DETECTOR						
$V_{RINDT(rms)}$	threshold level at pin RXIN (RMS value)		–	42	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Decision logic (IDT and SWT)						
SIGNAL RECOGNITION						
$\Delta V_{Srx(th)}$	threshold voltage between pins RENV and RNOI to switch-over from receive to idle mode	$V_{RXIN} < V_{RINDT}$; note 2	–	13	–	mV
$\Delta V_{Stx(th)}$	threshold voltage between pins TENV and TNOI to switch-over from transmit to idle mode	note 2	–	13	–	mV
SWITCH-OVER						
$I_{source(SWT)}$	current sourced from pin SWT when switching to receive mode		7.5	10	12.5	μA
$I_{sink(SWT)}$	current sunk by pin SWT when switching to transmit mode		7.5	10	12.5	μA
$I_{idle(SWT)}$	current sourced from pin SWT in idle mode		–	0	–	μA
Voice switch (STAB and SWR)						
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referenced to R_{SWR} = 365 kΩ	−40	–	+12	dB
$\lvert\Delta G_v\rvert$	voltage gain variation from transmit mode to idle mode on both channels		–	20	–	dB
G_{tr}	gain tracking (G_{vtx} + G_{vrx}) during switching, referenced to idle mode		–	±0.5	–	dB

Notes

1. Corresponds to ±1 dB tracking.
2. Corresponds to 4.3 dB noise/speech recognition level.

TEST AND APPLICATION INFORMATION

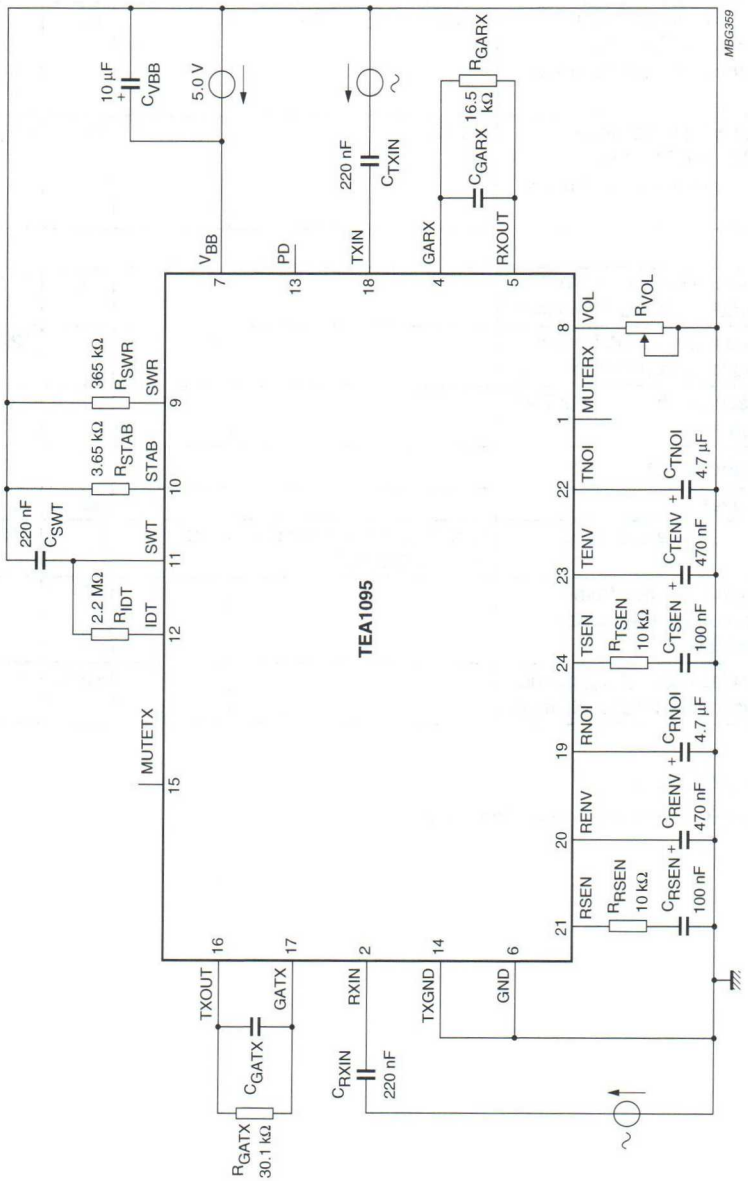


Fig.11 Test circuit.

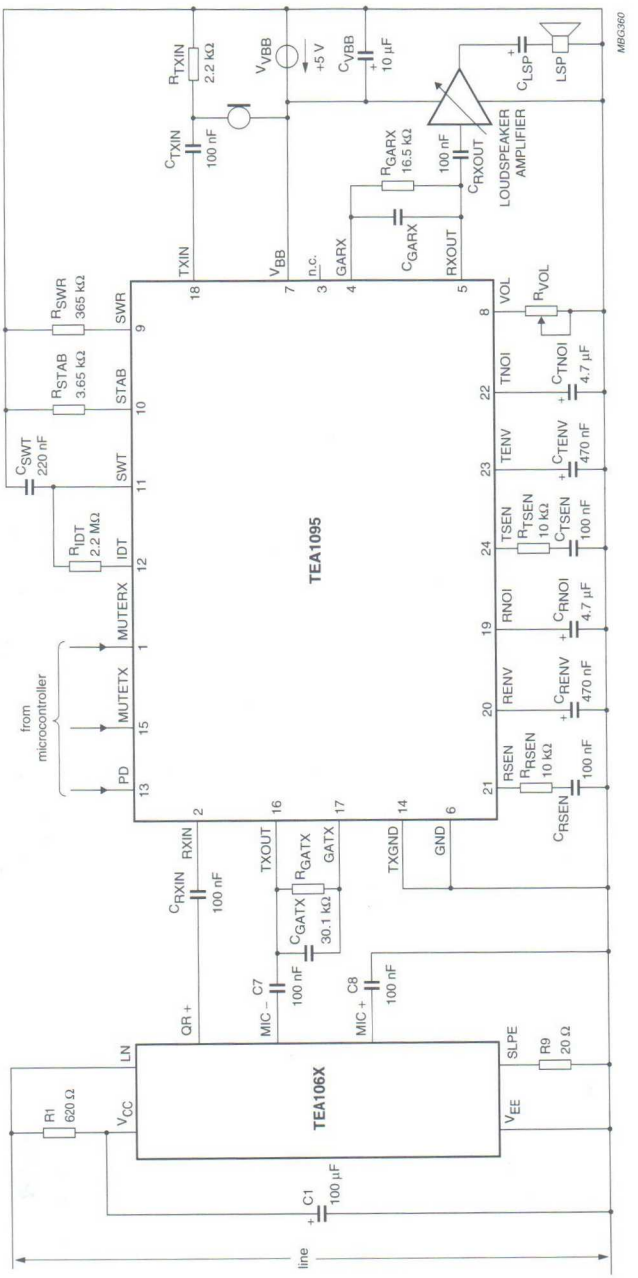
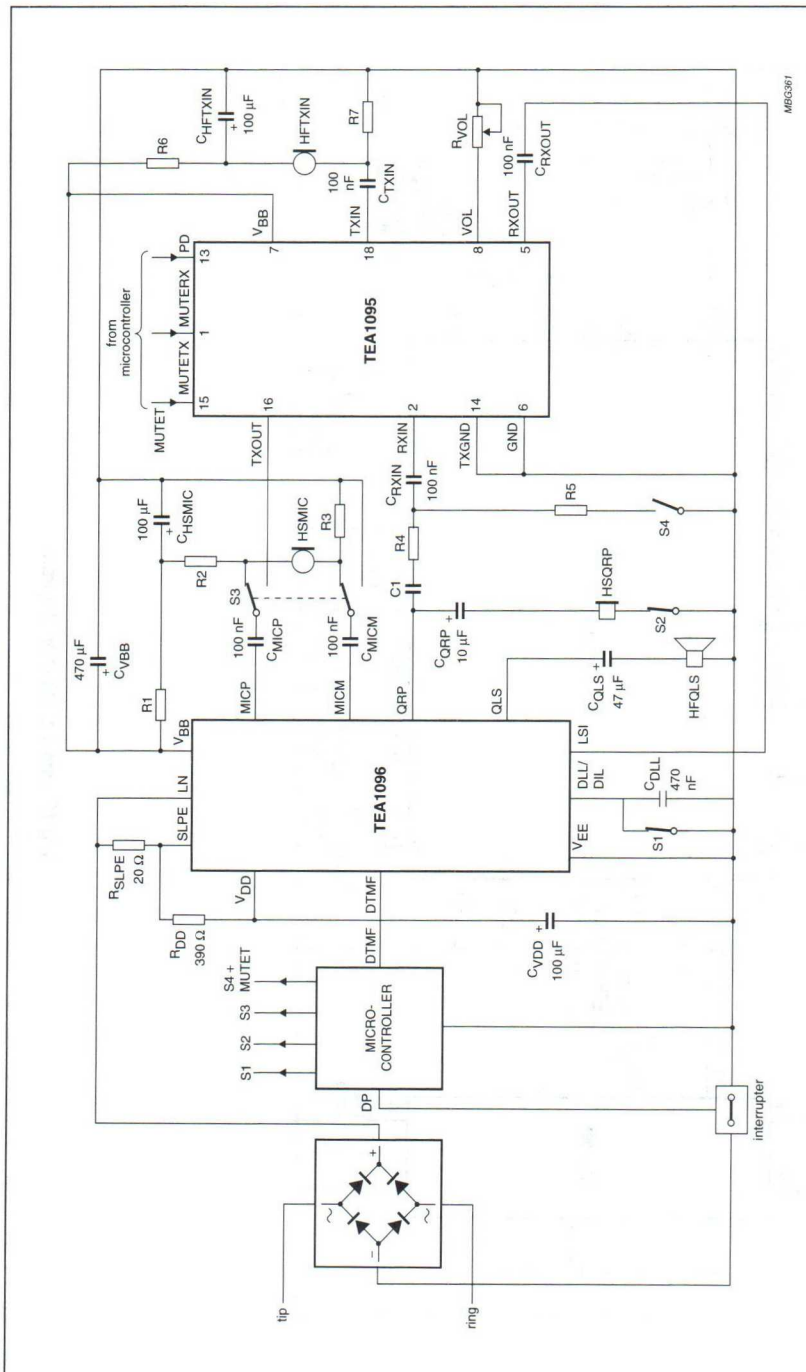


Fig.12 Basic application diagram.



MODE	SWITCH				MUTET
	S1	S2	S3	S4	
Hands-free	OPEN	OPEN	TXOUT	OPEN	LOW
Handset	CLOSED	CLOSED	HSMIC	OPEN	DON'T CARE
Handset plus listening-in	OPEN	CLOSED	HSMIC	CLOSED	HIGH

Fig.13 Application example.

Speech and handsfree IC TEA1098TV

FEATURES

Line interface

- Low DC line voltage
- Voltage regulator with adjustable DC voltage
- Symmetrical high impedance inputs (70 kΩ) for dynamic, magnetic or electret microphones
- DTMF input with confidence tone on earphone and/or loudspeaker
- Receive amplifier for dynamic, magnetic or piezo-electric earpieces (with externally adjustable gain)
- AGC: automatic gain control for true line loss compensation.

Supplies

- Provides a strong 3.35 V regulated supply for micro-controller or dialler
- Provides filtered power supply, optimized according to line current
- Filtered 2 V power supply output for electret microphone
- $\overline{PD}$ logic input for power down.

Handsfree

- Asymmetrical high input impedance for electret microphone
- Loudspeaker amplifier with single-ended rail-to-rail output and externally adjustable gain
- Dynamic limiter on loudspeaker amplifier to prevent distortion
- Logarithmic volume control on loudspeaker amplifier via linear potentiometer
- Duplex controller consisting of:
  - signal and noise envelope monitors for both channels (with adjustable sensitivities and timing)
  - decision logic (with adjustable switch-over and idle-mode timing)
  - voice switch control (with adjustable switching range and constant sum of gain during switching).

APPLICATIONS

- Line powered telephone sets

GENERAL DESCRIPTION

The TEA1098TV is an analog bipolar circuit dedicated for telephony applications. It includes a line interface, handset (HS) microphone and earpiece amplifiers, handsfree (HF) microphone and loudspeaker amplifiers and a duplex controller with signal and noise monitors on both channels.

This IC provides a 3.35 V supply for a micro-controller and a 2 V filtered voltage supply for an electret microphone.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1098TV	VSO40	plastic very small outline package; 40 leads	SOT158-1

QUICK REFERENCE DATA

I_{line} = 15 mA; R_{slpe} = 20 Ω; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; AGC pin connected to LN; $\overline{PD}$ = HIGH; HFC = LOW; $\overline{MUTE}$ = HIGH; measured according to test circuits; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range	normal operation	11	–	130	mA
		with reduced performance	1	–	11	mA
V_{SLPE}	stabilized voltage between SLPE and GND	I_{line} = 15 mA	tbf	3.7	tbf	V
		I_{line} = 70 mA	tbf	6.15	tbf	V
V_{BB}	regulated supply voltage for internal circuitry	I_{line} = 15 mA	tbf	3.0	tbf	V
		I_{line} = 70 mA	tbf	5.35	tbf	V
V_{DD}	regulated supply voltage on pin V_{DD}	V_{BB} > 3.35 V + 0.25 V (typ.)	–	3.35	3.6	V
		otherwise	–	V_{BB} – 0.25	–	V
I_{BB}	current available on pin V_{BB}					
	in speech mode		–	11	–	mA
	in handsfree mode		–	9	–	mA
$I_{BB(PD)}$	current consumption on V_{BB} during power down phase	$\overline{PD}$ = LOW	–	500	–	µA
$G_{v(MIC-LN)}$	voltage gain from pin MIC+/MIC– to LN	V_{MIC} = 5 mV (RMS)	tbf	44.6	tbf	dB
$G_{v(IR-RECO)}$	voltage gain from pin IR (referred to LN) to RECO	V_{IR} = 15 mV (RMS)	tbf	29.7	tbf	dB
$\Delta G_{v(QR)}$	gain voltage range between pins RECO and QR		–3	–	+15	dB
$G_{v(TXIN-TXOUT)}$	voltage gain from pin TXIN to TXOUT	V_{TXIN} = 8 mV (RMS); R_{GATX} = 30.1 kΩ	–	15.2	–	dB
$G_{v(HFTX-LN)}$	voltage gain from pin HFTX to LN	V_{HFTX} = 15 mV (RMS)	–	35	–	dB
$G_{v(HFRX-LSAO)}$	voltage gain from pin HFRX to LSAO	V_{HFRX} = 30 mV (RMS); R_{GALS} = 255 kΩ; I_{line} = 70 mA	–	27.8	–	dB
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referred to 365 kΩ	–40	–	+12	dB
$\Delta G_{v(trx)}$	gain control range for transmit and receive amplifiers affected by the AGC; with respect to I_{line} = 15 mA	I_{line} = 70 mA	–	6.2	–	dB

BLOCK DIAGRAM

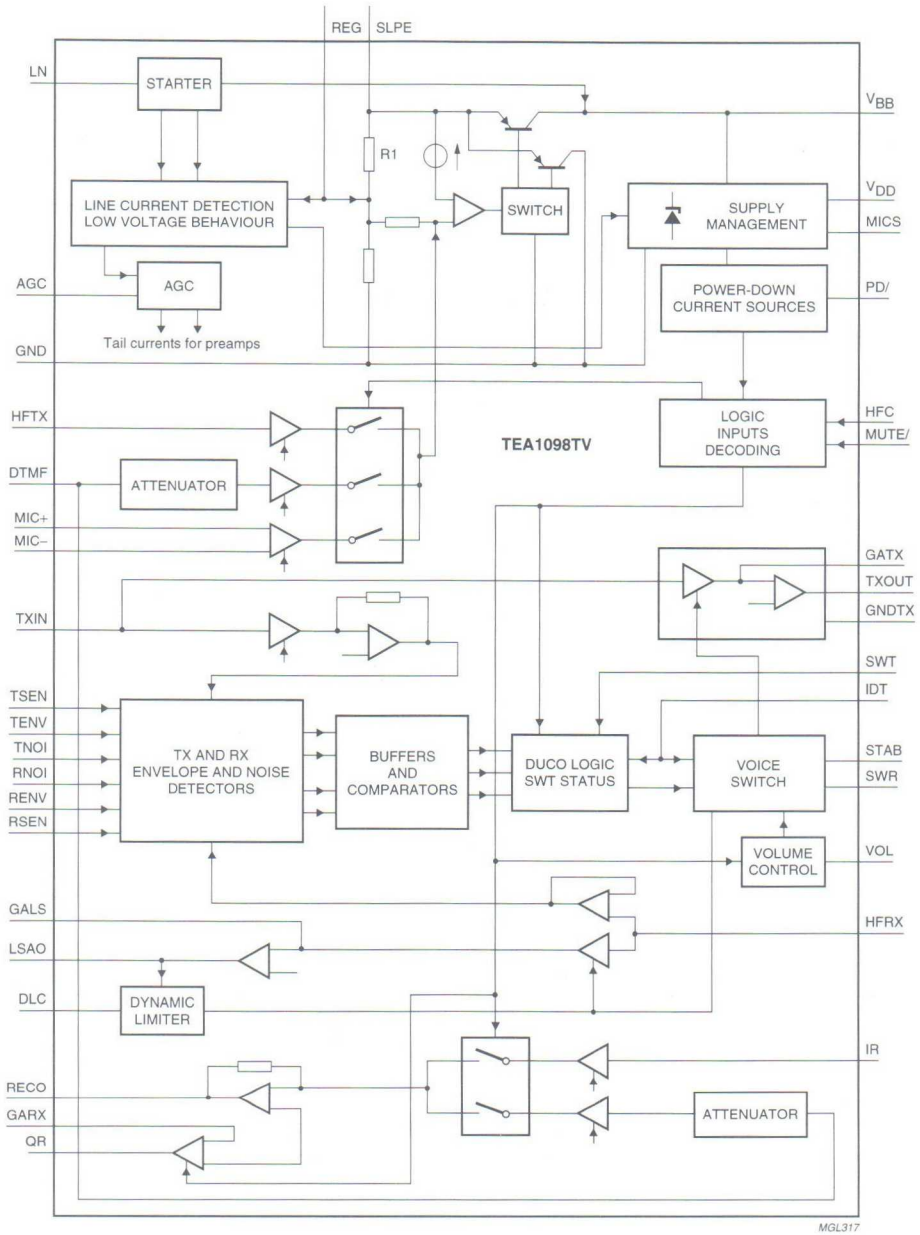


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{PD}$	1	power-down input
$\overline{MUTE}$	2	logic input
n.c.	3	not connected
n.c.	4	not connected
HFRX	5	receive input for loudspeaker amplifier
TNOI	6	transmit noise envelope timing adjustment
TENV	7	transmit signal envelope timing adjustment
TSEN	8	transmit signal envelope sensitivity adjustment
RNOI	9	receive noise envelope timing adjustment
RSEN	10	receive signal envelope sensitivity adjustment
RENV	11	receive signal envelope timing adjustment
DLC	12	dynamic limiter capacitor for the loudspeaker amplifier
V_{BB}	13	stabilized supply for internal circuitry
GALS	14	loudspeaker amplifier gain adjustment
LSAO	15	loudspeaker amplifier output
GND	16	ground reference
SLPE	17	line current sense
LN	18	positive line terminal
REG	19	line voltage regulator decoupling
IR	20	receive amplifier input
AGC	21	automatic gain control / line loss compensation
V_{DD}	22	3.35 V regulated voltage supply for microcontrollers
MICS	23	microphone supply
STAB	24	reference current adjustment
SWR	25	switching range adjustment
VOL	26	loudspeaker volume adjustment
SWT	27	switch-over timing adjustment
IDT	28	idle mode timing adjustment
TXOUT	29	HF microphone amplifier output
GATX	30	HF microphone amplifier gain adjustment
TXIN	31	HF microphone amplifier input
GNDTX	32	ground reference for microphone amplifiers
MIC–	33	negative HS microphone amplifier input
MIC+	34	positive HS microphone amplifier input
DTMF	35	dual tone multi-frequency input
QR	36	earpiece amplifier output
GARX	37	earpiece amplifier gain adjustment
RECO	38	receive amplifier output
HFTX	39	transmit input for line amplifier
HFC	40	logic input

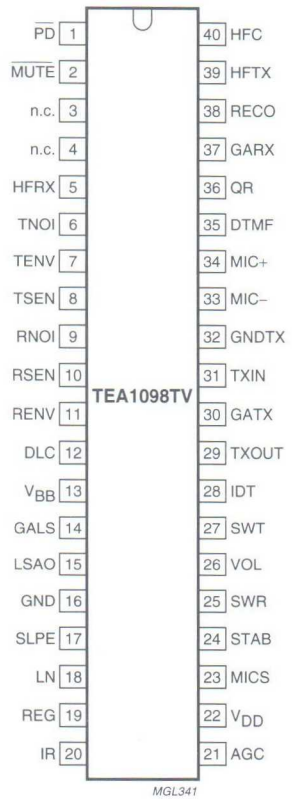


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supplies

LINE INTERFACE AND INTERNAL SUPPLY (PINS LN, SLPE, REG AND V_{BB})

The supply for the TEA1098TV and its peripherals is obtained from the line. The IC generates a stabilized reference voltage (V_{ref}) between pins SLPE and GND.

This reference voltage is equal to 3.7 V for line currents lower than 18 mA. It than increases linearly with the line current and reaches the value of 6.15 V for line currents higher than 46 mA. For line currents below 9 mA, the internal reference voltage generating V_{ref} is automatically adjusted to a lower value. This is the so-called low voltage area and the TEA1098TV has limited performances in this area (see Section "Low voltage behaviour"). This reference voltage is temperature compensated.

The voltage between pins SLPE and REG is used by the internal regulator to generate the stabilized reference voltage and is decoupled by means of a capacitor between pins LN and REG. This capacitor converted into an equivalent inductance realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (done by an external impedance).

The IC regulates the line voltage at pin LN and it can be calculated as follows:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I^{x}$$

where:

I_{line} = line current

I^{x} = current consumed on pin LN (approximately a few μA)

I_{SLPE} = current flowing through the R_{SLPE} resistor

The preferred value for R_{SLPE} is 20 Ω. Changing this value will affect more than the DC characteristics; it also influences the transmit gains to the line, the gain control characteristic, the sidetone level and the maximum output swing on the line.

As can be seen from Fig.3, the internal circuitry is supplied by pin V_{BB}, which is a strong supply point combined with the line interface. The line current is flowing through the R_{SLPE} resistor and is sunk by the V_{BB} voltage stabilizer, becoming available for a loudspeaker amplifier or any peripheral IC. Its voltage is equal to 3.0 V for line currents lower than 18 mA. It than increases linearly with the line current and reaches the value of 5.35 V for line currents greater than 46 mA. It is temperature compensated.

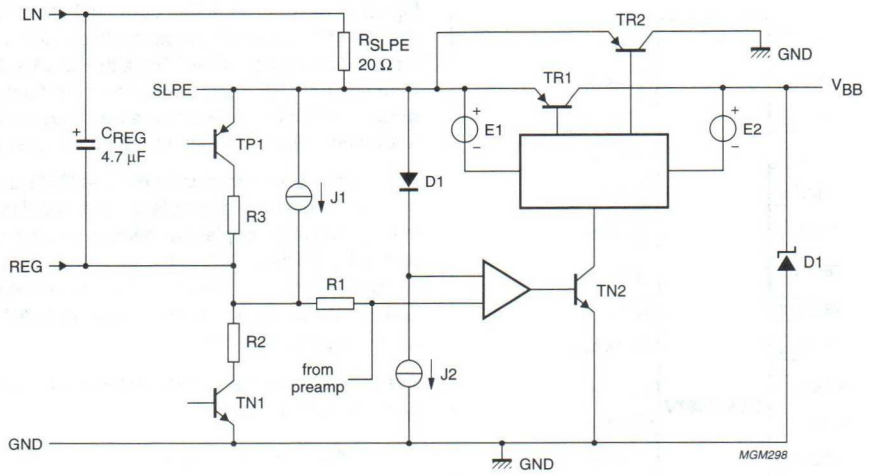


Fig.3 Line interface principle.

The aim of the current switch TR1-TR2 is to reduce distortion of large AC line signals. Current I_{SLPE} is supplied to V_{BB} via TR1 when the voltage on SLPE is greater than V_{BB} + 0.25 V. When the voltage on SLPE is lower than this value, the current I_{SLPE} is shunted to GND via TR2.

The reference voltage V_{ref} can be increased by connecting an external resistor between pins REG and SLPE. For large line currents, this increase can slightly affect some dynamic performances such as maximum signal level on the line for 2% THD. The voltage on pin V_{BB} is not affected by this external resistor. See Fig.4 for the main DC voltages.

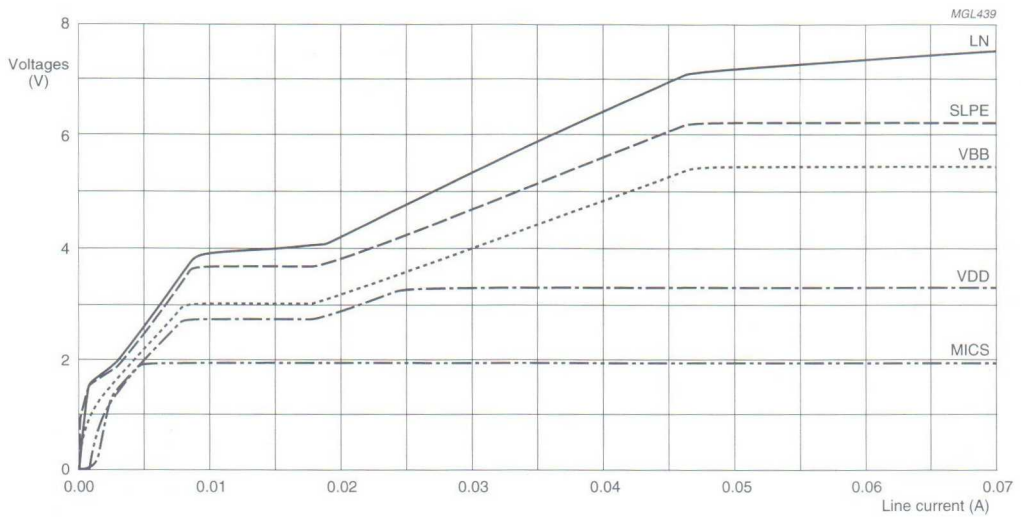


Fig.4 Main DC voltages.

V_{DD} SUPPLY FOR MICRO-CONTROLLER (PIN V_{DD})

The voltage on V_{DD} supply point follows the voltage on V_{BB} with a difference typically equal to 250 mV and is internally limited to 3.35 V. This voltage is temperature compensated. This supply point can provide a current up to 3 mA typically. Its internal consumption stays low (a few 10 nA) as long as V_{DD} does not exceed 1.5 V.

An external voltage can be connected on V_{DD} with limited extra consumption on V_{DD} (typically 120 μA). This voltage source should not be lower than 3.5 V and higher than 6 V.

V_{BB} and V_{DD} can supply external circuits in the limit of currents provided either from the line or from ESI, taking into account the internal current consumption.

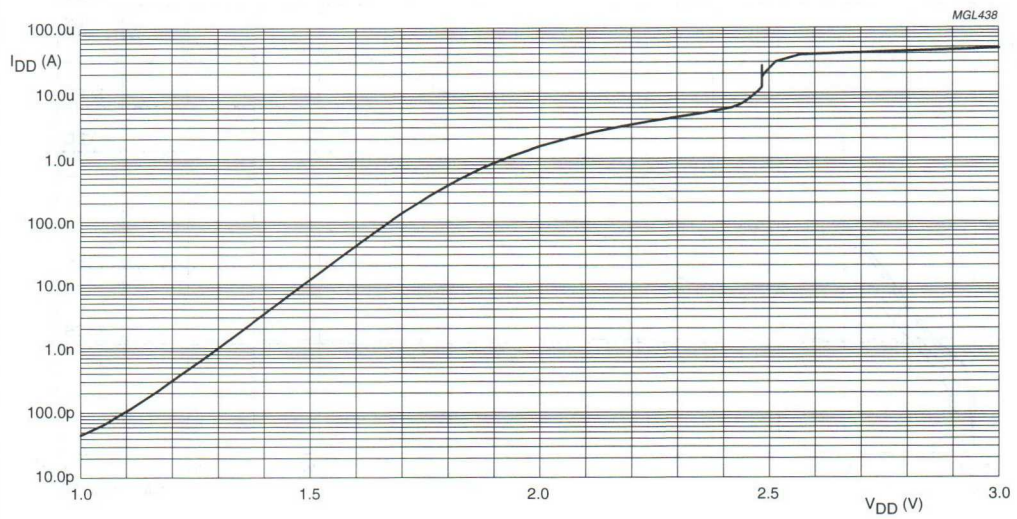


Fig.5 Current consumption on V_{DD}.

Supply for microphone (pins MICS and GNDTX)

The MICS output can be used as a supply for an electret microphone. Its voltage is equal to 2 V; it can source a current up to 1 mA and has an output impedance equal to 200 Ω.

Low voltage behaviour

For line currents below 9 mA, the reference voltage is automatically adjusted to a lower value; the V_{BB} voltage follows the SLPE voltage with 250 mV difference. The excess current available for other purposes than DC biasing of the IC becomes small. In this low voltage area, the IC has limited performances.

When the V_{BB} voltage becomes lower than 2.7 V, the V_{BB} detector of the receive dynamic limiter on LSAO acts continuously, discharging the DLC capacitor. In the DC condition, the loudspeaker is then automatically disabled below this voltage.

When V_{BB} reaches 2.5 V, the TEA1098TV is forced in a low voltage mode whatever the levels on the logic inputs are. It is a speech mode with reduced performances only enabling the microphone channel (between the MIC inputs and LN) and the earpiece amplifier. These two channels are able to deliver signals for line currents as small as 3 mA. The HFC input is tied to GND sinking a current typically equal to 300 μA.

Power-down mode (pin $\overline{PD}$)

To reduce consumption during dialling or register recall (flash), the TEA1098TV is provided with a power-down input ($\overline{PD}$). When the voltage on pin $\overline{PD}$ is LOW, the current consumption from V_{BB} and V_{DD} is reduced to 500 μA. Therefore a capacitor of 470 μF on V_{BB} is sufficient to power the TEA1098TV during pulse dialling or flash. The $\overline{PD}$ input has a pull-up structure. In this mode, the capacitor C_{REG} is internally disconnected.

Transmit channels (pins MIC+, MIC–, DTMF, HFTX and LN)

HANDSET MICROPHONE AMPLIFIER (PINS MIC+, MIC– AND LN)

The TEA1098TV has symmetrical microphone inputs. The input impedance between MIC+ and MIC– is typically equal to 70 kΩ. The voltage gain between pins MIC+/MIC– and LN is set to 44.6 dB. Without limitation from the output, the microphone input stage can accommodate signals up to 18 mV (RMS) at room temperature for 2% of total harmonic distortion (THD). The microphone inputs are biased at one diode voltage.

Automatic gain control is provided for line loss compensation.

DTMF AMPLIFIER (PINS DTMF, LN AND RECO)

The TEA1098TV has an asymmetrical DTMF input. The input impedance between DTMF and GND is typically equal to 20 kΩ. The voltage gain between pins DTMF and LN is set to 25.7 dB. Without limitation from the output, the input stage can accommodate signals up to 180 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

When the DTMF amplifier is enabled, dialling tones may be sent on the line. These tones can be heard in the earpiece or in the loudspeaker at a low level. This is called the confidence tone. The voltage attenuation between pins DTMF and RECO is typically equal to –16.5 dB.

The DC biasing of this input is 0 V.

The automatic gain control has no effect on these channels.

HANDSFREE TRANSMIT OUTPUT STAGE (PINS HFTX AND LN)

The TEA1098TV has an asymmetrical HFTX input, which is mainly intended for use in combination with the TXOUT output. The input impedance between HFTX and GND is typically equal to 20 kΩ. The voltage gain between pins HFTX and LN is set to 35 dB. Without limitation from the output, the input stage can accommodate signals up to 95 mV (RMS) at room temperature for 2% of total harmonic distortion (THD). The HFTX input is biased at two diodes voltage.

Automatic gain control is provided for line loss compensation.

Receive channels (pins IR, RECO, GARX and QR)

RX AMPLIFIER (PINS IR AND RECO)

The receive amplifier has one input IR which is referred to the line. The input impedance between pins IR and LN is typically equal to 20 kΩ and the DC biasing between these pins is equal to one diode voltage. The gain between pins IR (referred to LN) and RECO is typically equal to 29.7 dB. Without limitation from the output, the input stage can accommodate signals up to 50 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

This receive amplifier has a rail-to-rail output RECO, which is designed for use with high ohmic (real) loads (larger than 5 kΩ). This output is biased at two diodes voltage.

Automatic gain control is provided for line loss compensation.

EARPIECE AMPLIFIER (PINS GARX AND QR)

The earpiece amplifier is an operational amplifier having its output (QR) and its inverting input (GARX) available. Its input signal comes, via a decoupling capacitor, from the receive output RECO. It is used in combination with two resistors to get the required gain or attenuation compared to the receive gain. It can be chosen between –3 dB and 15 dB.

Two external capacitors C_{GAR} (connected between GAR and QR) and C_{GARS} (connected between GAR and GND) ensure stability. The C_{GAR} capacitor provides a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAR} \times R_{E2}$. The relationship $C_{GARS} >= 10 \times C_{GAR}$ must be fulfilled.

The earpiece amplifier has a rail-to-rail output QR, biased at two diodes voltage. It is designed for use with low ohmic (real) loads (150 Ω) or capacitive loads (100 nF in series with 100 Ω).

AGC (pin AGC)

The TEA1098TV performs automatic line loss compensation, which fits well with the true line attenuation. The automatic gain control varies the gain of some transmit and receive amplifiers in accordance with the DC line current. The control range is 6.2 dB for $G_{v(MIC-LN)}$, $G_{v(IR-RECO)}$ and $G_{v(IR-RECO)}$ and 6.65 dB for the other affected channels, which corresponds approximately to a line length of 5.5 km for a 0.5 mm twisted-pair copper cable.

To enable this gain control, the pin AGC must be shorted to pin LN. The start current for compensation corresponds to a line current equal to typically 23 mA and the stop current to 57 mA. The start current can be increased by connecting an external resistor between pins AGC and LN. It can be increased up to 40 mA (using a resistor typically equal to 80 kΩ). The start and stop current will be maintained in a ratio equal to 2.5. By leaving the AGC pin opened, the gain control is disabled and no line loss compensation is performed.

Handsfree application

As can be seen from Fig.3, a loop is formed via the sidetone network in the line interface part and the acoustic coupling between loudspeaker and microphone of the handsfree part. When this loop gain is greater than 1, howling occurs. In a full duplex application, this would be the case. The loop-gain has to be much lower than 1 and therefore has to be decreased to avoid howling. This is achieved by the duplex controller. The duplex controller of the TEA1098TV detects which channel has the 'largest' signal and then controls the gain of the microphone loudspeaker amplifiers so that the sum of the gains remains constant.

As a result, in handsfree application the circuit can be in three stable modes:

1. Transmit mode (Tx mode).

   The gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum.

2. Receive mode (RX mode).

   The gain of the loudspeaker amplifier is at its maximum and the gain of the microphone amplifier is at its minimum.

3. Idle mode.

   The gain of the amplifiers is halfway between their maximum and minimum value.

The difference between the maximum gain and minimum gain is called the switching range.

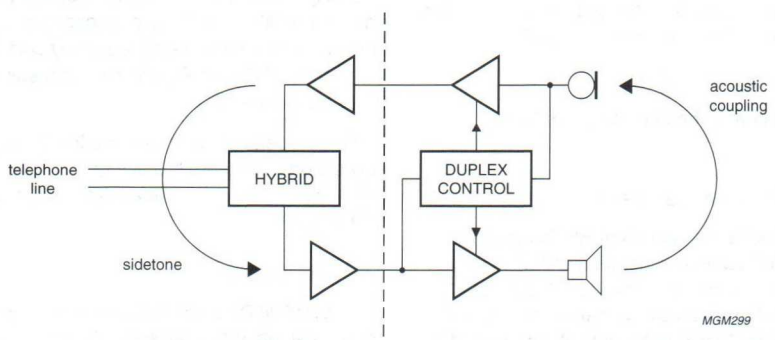


Fig.6 Handsfree telephone set principles.

HANDSFREE MICROPHONE CHANNEL: PINS TXIN, GATX, TXOUT AND GNDTX (see Fig.7)

The TEA1098TV has an asymmetrical handsfree microphone input TXIN with an input resistance of 20 kΩ. The DC biasing of the input is 0 V. The gain of the input stage varies according to the mode of the TEA1098TV. In the transmit mode, the gain is at its maximum; in the receive mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum.

Switch-over from one mode to the other is smooth and click-free. The output TXOUT is biased at two diodes voltage and has a current capability equal to 20 μA (RMS).

In the transmit mode, the overall gain of the microphone amplifier (from pins TXIN to TXOUT) can be adjusted from 0 dB up to 31 dB to suit specific application requirements. The gain is proportional to the value of R_{GATX} and equals 15.2 dB with R_{GATX} = 30.1 kΩ. Without limitation from the output, the microphone input stage can accommodate signals up to 18 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

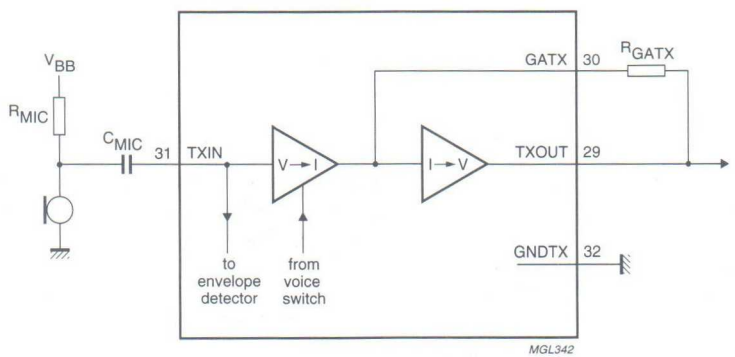


Fig.7 Handsfree microphone channel.

LOUDSPEAKER CHANNEL

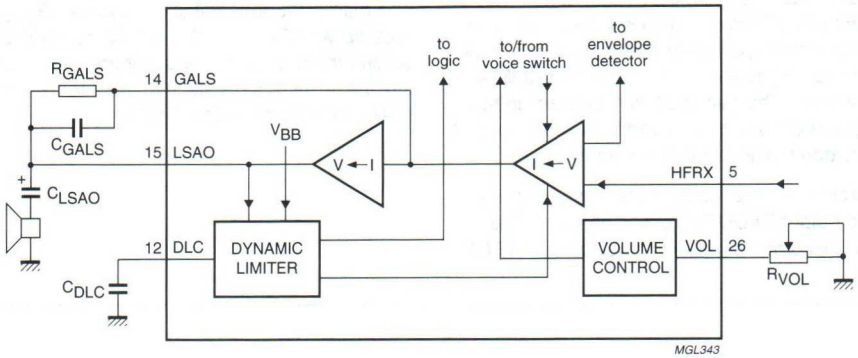


Fig.8 Loudspeaker channel.

Loudspeaker amplifier: pins HFRX, GALS and LSAO

The TEA1098TV has an asymmetrical input for the loudspeaker amplifier with an input resistance of 20 kΩ between HFRX and GND. It is biased at two diodes voltage. Without limitation from the output, the input stage can accommodate signals up to 580 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

The gain of the input stage varies according to the mode of the TEA1098TV. In the receive mode, the gain is at its maximum; in the transmit mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The rail-to-rail output stage is designed to power a loudspeaker connected as a single-ended load (between LSAO and GND).

In the receive mode, the overall gain of the loudspeaker amplifier can be adjusted from 0 dB up to 35 dB to suit specific application requirements. The gain from HFRX to LSAO is proportional to the value of R_{GALS} and equals 27.8 dB with R_{GALS} = 255 kΩ. A capacitor connected in parallel with R_{GALS} is recommended and provides a first-order low-pass filter.

Volume control: pin VOL

The loudspeaker amplifier gain can be adjusted with the potentiometer R_{VOL}. A linear potentiometer can be used to obtain logarithmic control of the gain at the loudspeaker amplifier. Each 1.9 kΩ increase of R_{VOL} results in a gain loss of 3 dB. The maximum gain reduction with the volume control is internally limited to the switching range.

Dynamic limiter: pin DLC

The dynamic limiter of the TEA1098TV prevents clipping of the loudspeaker output stage and protects the operation of the circuit when the supply voltage at V_{BB} falls below 2.7 V.

Hard clipping of the loudspeaker output stage is prevented by rapidly reducing the gain when the output stage starts to saturate. The time in which gain reduction is effected (clipping attack time) is approximately a few milliseconds. The circuit stays in the reduced gain mode until the peaks of the loudspeaker signals no longer cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time (typically 250 ms). Both attack and release times are proportional to the value of the capacitor C_{DLC}. The total harmonic distortion of the loudspeaker output stage, in reduced gain mode, stays below 2% up to 10 dB (minimum) of input voltage overdrive [providing V_{HFRX} is below 580 mV (RMS)].

When the supply voltage drops below an internal threshold voltage of 2.7 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). When the supply voltage exceeds 2.7 V, the gain of the loudspeaker amplifier is increased again.

By forcing a level lower than 0.2 V on pin DLC, the loudspeaker amplifier is muted and the TEA1098TV is automatically forced into the transmit mode.

DUPLEX CONTROLLER

Signal and noise envelope detectors: pins TSEN, TENV, TNOI, RSEN, RENV and RNOI

The signal envelopes are used to monitor the signal level strength in both channels. The noise envelopes are used to monitor background noise in both channels. The signal and noise envelopes provide inputs for the decision logic. The signal and noise envelope detectors are shown in Fig.9.

For the transmit channel, the input signal at TXIN is 40 dB amplified to TSEN. For the receive channel, the input signal at HFRX is 0 dB amplified to RSEN. The signals from TSEN and RSEN are logarithmically compressed and buffered to TENV and RENV respectively.

The sensitivity of the envelope detectors is set with R_{TSEN} and R_{RSEN}. The capacitors connected in series with the two resistors block any DC component and form a first-order high-pass filter. In the basic application, see Fig.15, it is assumed that V_{TXIN} = 1 mV (RMS) and V_{HFRX} = 100 mV (RMS) nominal and both R_{TSEN} and R_{RSEN} have a value of 10 kΩ. With the value of C_{TSEN} and C_{RSEN} at 100 nF, the cut-off frequency is at 160 Hz.

The buffer amplifiers leading the compressed signals to TENV and RENV have a maximum source current of 120 μA and a maximum sink current of 1 μA. Together with the capacitor C_{TENV} and C_{RENV}, the timing of the signal envelope monitors can be set. In the basic application, the value of both capacitors is 470 nF. Because of the logarithmic compression, each 6 dB signal increase means 18 mV increase of the voltage on the envelopes TENV or RENV at room temperature. Thus, timings can be expressed in dB/ms. At room temperature, the 120 μA sourced current corresponds to a maximum rise-slope of the signal envelope of 85 dB/ms. This is sufficient to track normal speech signals. The 1 μA current sunk by TENV or RENV corresponds to a maximum fall-slope of 0.7 dB/ms. This is sufficient for a smooth envelope and also eliminates the effect of echoes on switching behaviour.

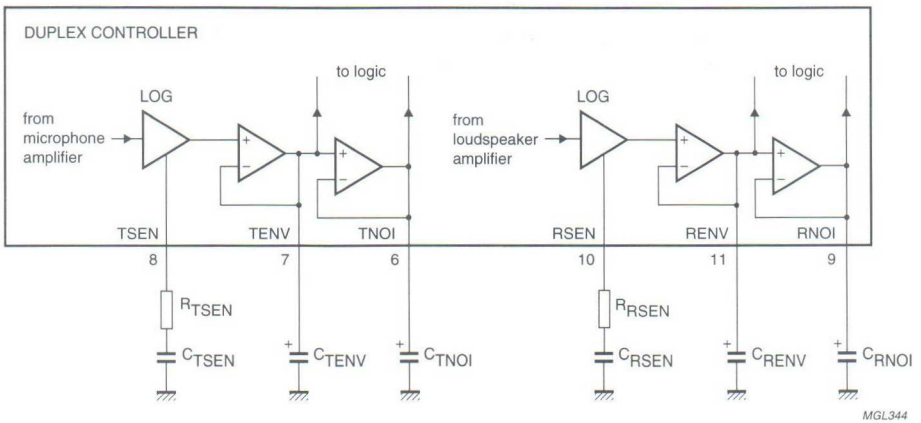


Fig.9 Signal and noise envelope detectors

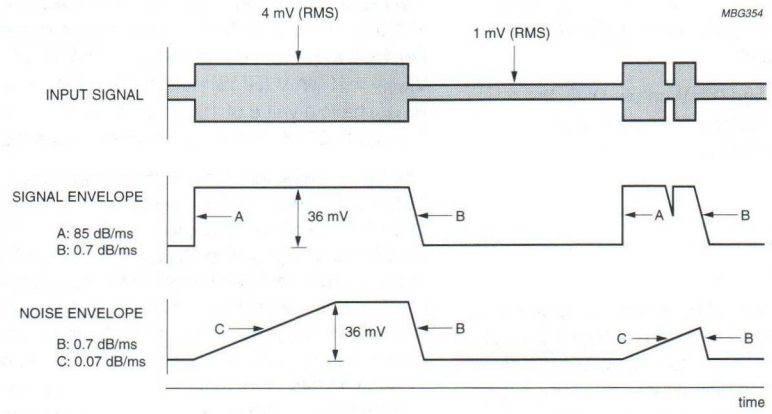
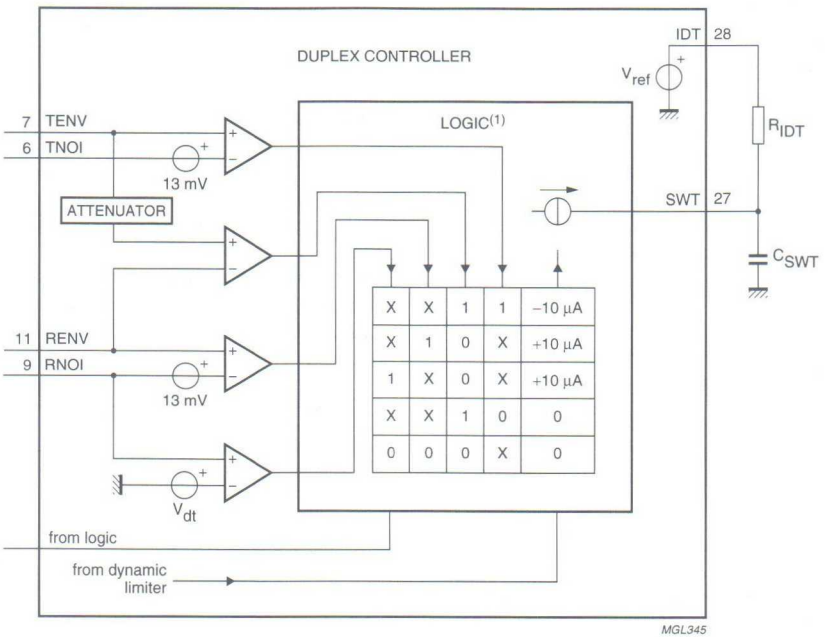


Fig.10 Signal and noise envelope waveforms.

To determine the noise level, the signals on TENV and RENV are buffered to TNOI and RNOI. These buffers have a maximum source current of 1 μA and a maximum sink current of 120 μA. Together with the capacitors C_{TNOI} and C_{RNOI}, the timing can be set. In the basic application, see Fig.15, the value of both capacitors is 4.7 μF. At room temperature, the 1 μA sourced current corresponds to a maximum rise-slope of the noise envelope of approximately 0.07 dB/ms.

This is small enough to track background noise and not to be influenced by speech bursts. The 120 μA current that is sunk corresponds to a maximum fall-slope of approximately 8.5 dB/ms. However, during the decrease of the signal envelope, the noise envelope tracks the signal envelope so it will never fall faster than approximately 0.7 dB/ms. The behaviour of the signal envelope and noise envelope monitors is illustrated in Fig.10.

Decision logic: pins IDT and SWT



X	X	1	1	−10 µA
X	1	0	X	+10 µA
1	X	0	X	+10 µA
X	X	1	0	0
0	0	0	X	0

(1) When DLC < 0.2 V, −10 µA is forced.

Fig.11 Decision logic.

The TEA1098TV selects its mode of operation (transmit, receive or idle mode) by comparing the signal and the noise envelopes of both channels. This is executed by the decision logic. The resulting voltage on pin SWT is the input for the voice-switch.

To facilitate the distinction between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference $V_{ENV} - V_{NOI} = 13$ mV. This so called speech/noise threshold is implemented in both channels.

The signal on pin TXIN contains both speech and the signal coming from the loudspeaker (acoustic coupling). When receiving, the contribution from the loudspeaker overrules the speech.

As a result, the signal envelope on TENV is formed mainly by the loudspeaker signal. To correct this, an attenuator is connected between TENV and the TENV/RENV comparator. Its attenuation equals that applied to the microphone amplifier.

When a dial tone is present on the line, without monitoring, the tone would be recognized as noise because it is a signal with a constant amplitude. This would cause the TEA1098TV to go into the idle mode and the user of the set would hear the dial tone fade away. To prevent this, a dial tone detector is incorporated which, in standard applications, does not consider input signals between HFRX and GND as noise when they have a level greater than 25 mV (RMS). This level is proportional to R_{RSEN}.

In the same way, a transmit detector is integrated which, in standard applications, does not consider input signals between TXIN and GNDTX as noise when they have a level greater than 0.75 mV (RMS). This level is proportional to R_{TSEN}.

As can be seen from Fig.11, the output of the decision logic is a current source. The logic table gives the relationship between the inputs and the value of the current source. It can charge or discharge the capacitor C_{SWT} with a current of 10 μA (switch-over). If the current is zero, the voltage on SWT becomes equal to the voltage on IDT via the high-ohmic resistor R_{IDT} (idling). The resulting voltage difference between SWT and IDT determines the mode of the TEA1098TV and can vary between −400 and +400 mV (see Table 1).

Table 1 Modes of TEA1098TV

$V_{SWT} - V_{IDT}$ (mV)	MODE
<−180	transmit mode
0	idle mode
>180	receive mode

The switch-over timing can be set with C_{SWT}, the idle mode timing with C_{SWT} and R_{IDT}. In the basic application given in Fig.15, C_{SWT} is 220 nF and R_{IDT} is 2.2 MΩ. This enables a switch-over time from transmit to receive mode or vice-versa of approximately 13 ms (580 mV swing on SWT). The switch-over time from idle mode to transmit mode or receive mode is approximately 4 ms (180 mV swing on SWT).

The switch-over time, from receive mode or transmit mode to idle mode is equal to $4 \times R_{IDT}C_{SWT}$ and is approximately 2 seconds (idle mode time).

The input DLC overrules the decision logic. When the voltage on pin DLC goes lower than 0.2 V, the capacitor C_{SWT} is discharged with 10 μA thus resulting in the transmit mode.

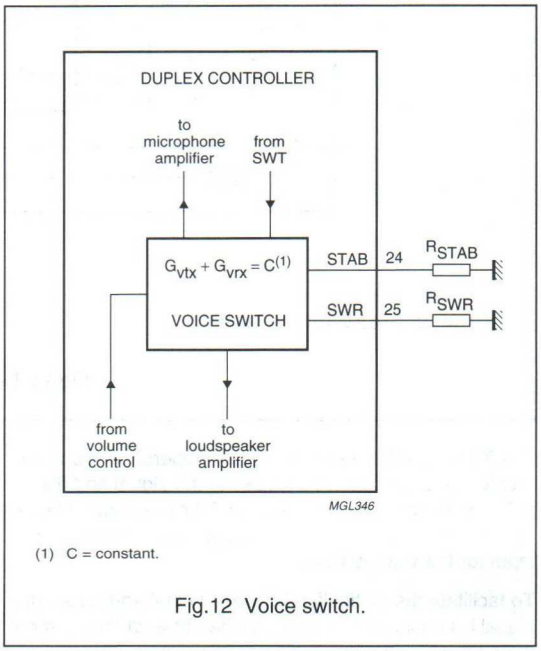
Voice-switch: pins STAB and SWR

A diagram of the voice-switch is illustrated in Fig.12. With the voltage on SWT, the TEA1098TV voice-switch regulates the gains of the transmit and the receive channels so that the sum of both is kept constant.

In the transmit mode, the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum. In the receive mode, the opposite applies. In the idle mode, both microphone and loudspeaker amplifier gains are halfway.

The difference between maximum and minimum is the so called switching range. This range is determined by the ratio of R_{SWR} and R_{STAB} and is adjustable between 0 and 52 dB. R_{STAB} should be 3.65 kΩ and sets an internally used reference current. In the basic application diagram given in Fig.15, R_{SWR} is 365 kΩ which results in a switching range of 40 dB. The switch-over behaviour is illustrated in Fig.13.

In the receive mode, the gain of the loudspeaker amplifier can be reduced using the volume control. Since the voice-switch keeps the sum of the gains constant, the gain of the microphone amplifier is increased at the same time (see dashed curves in Fig.13). In the transmit mode, however, the volume control has no influence on the gain of the microphone amplifier or the gain of the loudspeaker amplifier. Consequently, the switching range is reduced when the volume is reduced. At maximum reduction of volume, the switching range becomes 0 dB.



(1) C = constant.

Fig.12 Voice switch.

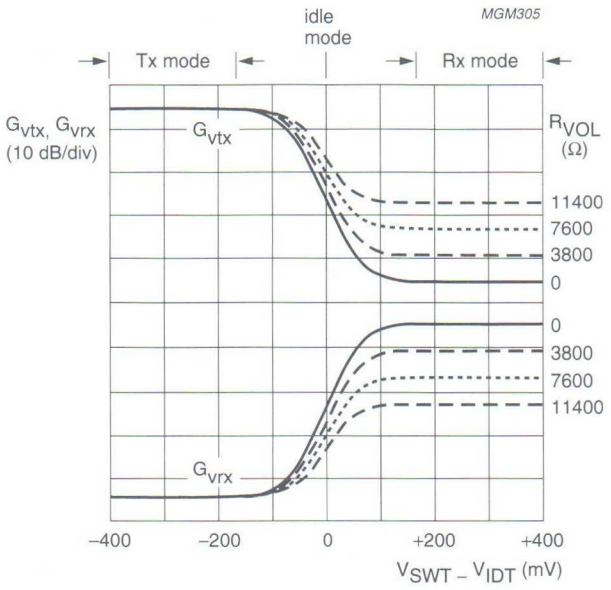


Fig.13 Switch-over behaviour.

Logic inputs

Table 2 Selection of transmit and receive channels for 4 different application modes

LOGIC INPUTS			FEATURES	APPLICATION EXAMPLES
$\overline{PD}$	HFC	$\overline{MUTE}$		
0	X	X		flash, DC dialling
1	0	0	DTMF to LN; DTMF to RECO; QR and MICS are active	DTMF dialling (telephone set)
1	0	1	MICS to LN; IR to RECO; QR and MICS are active	handset conversation (telephone set)
1	1	0	DTMF to LN; DTMF to RECO; HFRX to LSAO; QR and MICS are active	DTMF dialling in handsfree / group listening-in modes
1	1	1	TXIN to TXOUT; HFTX to LN; IR to RECO; HFRX to LSAO; MICS is active	handsfree conversation mode

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		GND – 0.4	12	V
	repetitive line voltage during switch-on or line interruption		GND – 0.4	13.2	V
$V_{n(max)}$	maximum voltage on pins REG, SLPE, IR, AGC		GND – 0.4	V_{LN} + 0.4	V
	maximum voltage on all other pins except V_{DD}		GND – 0.4	V_{BB} + 0.4	V
I_{line}	maximum line current		–	130	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C	–	800	mW
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	115	K/W

CHARACTERISTICS

I_{line} = 15 mA; R_{slpe} = 20 Ω; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; AGC pin connected to LN; $\overline{PD}$ = HIGH; HFC = LOW; $\overline{MUTE}$ = HIGH; measured according to test circuits; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
LINE INTERFACE AND INTERNAL SUPPLY (PINS LN, SLPE, REG AND V_{BB})						
V_{SLPE}	stabilized voltage between SLPE and GND	I_{line} = 15 mA	tbf	3.7	tbf	V
		I_{line} = 70 mA	tbf	6.15	tbf	V
V_{BB}	regulated supply voltage for internal circuitry	I_{line} = 15 mA	tbf	3.0	tbf	V
		I_{line} = 70 mA	tbf	5.35	tbf	V
I_{line}	line current for voltage increase					
	start current		–	18	–	mA
	stop current		–	46	–	mA
$\Delta V_{SLPE(T)}$	stabilized voltage variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C	–	±60	–	mV
$\Delta V_{BB(T)}$	regulated voltage variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C	–	±30	–	mV
I_{BB}	current available on pin V_{BB}					
	in speech mode		–	11	–	mA
	in handsfree mode		–	9	–	mA
V_{LN}	line voltage	I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	2.4	–	V
		I_{line} = 15 mA	tbf	4.0	tbf	V
		I_{line} = 130 mA	–	8.5	9.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SUPPLY FOR PERIPHERALS (PIN V_{DD})						
V_{DD}	regulated supply voltage on V_{DD}	V_{BB} > 3.35 V + 0.25 V (typ.)	–	3.35	3.6	V
		otherwise	–	V_{BB} – 0.25	–	V
$\Delta V_{DD(T)}$	regulated voltage variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C; V_{BB} > 3.35 V + 0.25 V (typ.)	–	±30	–	mV
I_{DD}	current consumption on V_{DD}	in trickle mode; I_{line} = 0 mA; V_{DD} = 1.5 V; V_{BB} discharging	–	–	0.15	µA
		V_{DD} > 3.35 V	60	120	–	µA
$I_{DD(o)}$	current available for peripherals	V_{DD} = 3.35 V	–	–3	–	mA
SUPPLY FOR MICROPHONE (PIN MICS)						
V_{MICS}	supply voltage for a microphone		–	2	–	V
I_{MICS}	current available on MICS		–	–	–1	mA
POWER DOWN INPUT (PIN $\overline{PD}$)						
V_{IL}	LOW-level input voltage		GND – 0.4	–	GND + 0.3	V
V_{IH}	HIGH-level input voltage		GND + 1.8	–	V_{BB} + 0.4	V
$I_{\overline{PD}}$	input current		–	–3	–6	µA
$I_{BB(PD)}$	current consumption on V_{BB} during power down phase	$\overline{PD}$ = LOW	–	500	–	µA
Preamplifier inputs (pins MIC+, MIC–, IR, DTMF, TXIN, HFTX, HFRX)						
$\lvert Z_{i(MIC)} \rvert$	input impedance					
	differential between pins MIC+ and MIC–		–	70	–	kΩ
	single-ended between pins MIC+/MIC– and GNDTX		–	35	–	kΩ
$\lvert Z_{i(IR)} \rvert$	input impedance between pins IR and LN		–	20	–	kΩ
$\lvert Z_{i(DTMF)} \rvert$	input impedance between pins DTMF and GND		–	20	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Z_{i(TXIN)} \rvert$	input impedance between pins TXIN and GNDTX		–	20	–	kΩ
$\lvert Z_{i(HFTX)} \rvert$	input impedance between pins HFTX and GND		–	20	–	kΩ
$\lvert Z_{i(HFRX)} \rvert$	input impedance between pins HFRX and GND		–	20	–	kΩ
TX amplifiers						
TX HANDSET MICROPHONE AMPLIFIER (PINS MIC+, MIC– AND LN)						
$G_{v(MIC-LN)}$	voltage gain from pin MIC+/MIC– to LN	V_{MIC} = 5 mV (RMS)	tbf	44.6	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±0.25	–	dB
CMRR	common mode rejection ratio		–	80	–	dB
THD	total harmonic distortion at LN	V_{LN} = 1.4 V (RMS)	–	–	2	%
		I_{line} = 4 mA; V_{LN} = 0.12 V (RMS)	–	–	10	%
$V_{no(LN)}$	noise output voltage at pin LN; pins MIC+/MIC– shorted through 200 Ω	psophometrically weighted (p53 curve)	–	–77.5	–	dBmp
$\Delta G_{v(m)}$	gain reduction if not activated	see Table 2	60	80	–	dB
DTMF AMPLIFIER (PINS DTMF, LN AND RECO)						
$G_{v(DTMF-LN)}$	voltage gain from pin DTMF to LN	V_{DTMF} = 50 mV (RMS)	tbf	25.7	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±0.25	–	dB
$\Delta G_{v(m)}$	gain reduction if not activated	see Table 2	60	80	–	dB
$G_{v(DTMF-RECO)}$	voltage gain from pin DTMF to RECO	V_{DTMF} = 50 mV (RMS)	–	–16.5	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TX AMPLIFIER USING HFTX (PINS HFTX AND LN)						
$G_{v(HFTX-LN)}$	voltage gain from pin HFTX to LN	V_{HFTX} = 15 mV (RMS)	tbf	35	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25 °C	T_{amb} = –25 to +75°C	–	±0.25	–	dB
THD	total harmonic distortion at LN	V_{LN} = 1.4 V (RMS)	–	–	2	%
$V_{HFTX(rms)}$	maximum input voltage at HFTX (RMS value)	I_{line} = 70 mA; THD = 2%	75	95	–	mV
$V_{no(LN)}$	noise output voltage at pin LN; pin HFTX shorted to GND through 200 Ω in series with 10 µF	psophometrically weighted (p53 curve)	–	–77.5	–	dBmp
$\Delta G_{v(m)}$	gain reduction if not activated	see Table 2	60	80	–	dB
RX amplifiers						
RX AMPLIFIERS USING IR (PINS IR AND RECO)						
$G_{v(IR-RECO)}$	voltage gain from pin IR (referred to LN) to RECO	V_{IR} = 8 mV (RMS)	tbf	29.7	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
$V_{IR/LN(rms)}$	maximum input voltage on IR (referred to LN) (RMS value)	I_{line} = 70 mA; THD = 2%	40	50	–	mV
$V_{RECO(rms)}$	maximum output voltage on RECO (RMS value)	THD = 2%	0.75	0.9	–	V
$V_{no(RECO)(rms)}$	noise output voltage at pin RECO; pin IR is an open-circuit (RMS value)	psophometrically weighted (p53 curve)	–	–88	–	dBVp

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta G_{v(m)}$	gain reduction if not activated	see Table 2	60	80	–	dB
RX EARPIECE AMPLIFIER (PINS GARX AND QR)						
$\Delta G_{v(QR)}$	gain voltage range between pins RECO and QR		–3	–	+15	dB
$V_{QR(rms)}$	maximum output voltage on QR (RMS value)	sine wave drive; R_L = 150 Ω; THD < 2%	0.75	0.9	–	V
$V_{no(QR)(rms)}$	noise output voltage at pin QR; pin IR is an open-circuit (RMS value)	$G_{v(QR)}$ = 0 dB; psophometrically weighted (p53 curve)	–	–88	–	dBVp
Automatic Gain Control (pin AGC)						
$\Delta G_{v(trx)}$	gain control range for transmit and receive amplifiers affected by the AGC; with respect to I_{line} = 15 mA	I_{line} = 70 mA; $G_{v(MIC-LN)}$; $G_{v(IR-RECO)}$ and $G_{v(IR-AUXO)}$	tbf	6.2	tbf	dB
		I_{line} = 70 mA for other transmit and receive gains affected	tbf	6.65	tbf	
I_{start}	highest line current for maximum gain		–	23	–	mA
I_{stop}	lowest line current for maximum gain		–	57	–	mA
Logic inputs (pins HFC, $\overline{\text{MUTE}}$)						
V_{IL}	LOW-level input voltage		GND – 0.4	–	GND + 0.3	V
V_{IH}	HIGH-level input voltage		GND + 1.8	–	V_{BB} + 0.4	V
I	input current					
	for pin HFC		–	3	6	µA
	for pin $\overline{\text{MUTE}}$		–	–3	–12	µA
Handsfree mode (HFC = HIGH)						
HF MICROPHONE AMPLIFIER (PINS TXIN, TXOUT AND GATX)						
$G_{v(TXIN-TXOUT)}$	voltage gain from pin TXIN to TXOUT	V_{TXIN} = 8 mV (RMS); R_{GATX} = 30.1 kΩ	–	15.2	–	dB
ΔG_v	voltage gain adjustment with R_{GATX}		–15	–	+16	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.1	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta G_{v(T)}$	gain variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±0.15	–	dB
$V_{no(TXOUT)(rms)}$	noise output voltage at pin TXOUT; pin TXIN is shorted through 200 Ω in series with 10 µF to GNDTX (RMS value)	psophometrically weighted (p53 curve)	–	–101	–	dBmp
$\Delta G_{v(m)}$	gain reduction if not activated	see Table 2	60	80	–	dB
HF LOUDSPEAKER AMPLIFIER (PINS HFRX, LSAO, GALS AND VOL)						
$G_{v(HFRX-LSAO)}$	voltage gain from pin HFRX to LSAO	V_{HFRX} = 30 mV (RMS); R_{GALS} = 255 kΩ; I_{line} = 70 mA	tbf	27.8	tbf	dB
ΔG_v	voltage gain adjustment with R_{GALS}		–28	–	+7	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.3	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
$\Delta G_{v(vol)}$	voltage gain variation related to ΔR_{VOL} = 1.9 kΩ	when total attenuation does not exceed the switching range	–	–3	–	dB
$V_{HFRX(rms)}$	maximum input voltage at pin HFRX (RMS value)	I_{line} = 70 mA; R_{GALS} = 33 kΩ; for 2% THD in the input stage	450	580	–	mV
$V_{no(LSAO)(rms)}$	noise output voltage at pin LSAO; pin HFRX is open-circuit (RMS value)	psophometrically weighted (p53 curve)	–	–79	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	see Table 2	60	80	–	dB
$V_{LSAO(rms)}$	output voltage (RMS value)	I_{BB} = 0 mA; I_{DD} = 1 mA				
		I_{line} = 18 mA	–	0.9	–	V
		I_{line} = 30 mA	–	1.2	–	V
		I_{line} > 50 mA	–	1.6	–	V
$I_{LSAO(max)}$	maximum output current at pin LSAO (peak value)		150	300	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DYNAMIC LIMITER (PINS LSAO AND DLC)						
t_{att}	attack time	when V_{HFRX} jumps from 20 mV to 20 mV + 10 dB	–	–	5	ms
		when V_{BB} jumps below $V_{BB(th)}$	–	1	–	ms
t_{rel}	release time	when V_{HFRX} jumps from 20 mV + 10 dB to 20 mV	–	100	–	ms
THD	total harmonic distortion	V_{HFRX} = 20 mV + 10 dB; $t > t_{att}$	–	1	2	%
$V_{BB(th)}$	V_{BB} limiter threshold		–	2.7	–	V
MUTE RECEIVE (PIN DLC)						
$V_{DLC(th)}$	threshold voltage required on pin DLC to obtain mute receive condition		GND – 0.4	–	GND + 0.2	V
$I_{DLC(th)}$	threshold current sourced by pin DLC in mute receive condition	V_{DLC} = 0.2 V	–	100	–	µA
$\Delta G_{vrx(m)}$	voltage gain reduction in mute receive condition	V_{DLC} = 0.2 V	60	80	–	dB
TX AND RX ENVELOPE AND NOISE DETECTORS (PINS TSEN, TENV, TNOI, RSEN, RENV AND RNOI)						
Preamplifiers						
$G_{v(TSEN)}$	voltage gain from pin TXIN to TSEN		–	40	–	dB
$G_{v(RSEN)}$	voltage gain from pin HFRX to RSEN		–	0	–	dB
Logarithmic compressor and sensitivity adjustment						
$\Delta V_{det(TSEN)}$	sensitivity detection on pin TSEN; voltage change on pin TENV when doubling the current from TSEN	I_{TSEN} = 0.8 to 160 µA	–	18	–	mV
$\Delta V_{det(RSEN)}$	sensitivity detection on pin RSEN; voltage change on pin RENV when doubling the current from RSEN	I_{RSEN} = 0.8 to 160 µA	–	18	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Signal envelope detectors						
$I_{source(ENV)}$	maximum current sourced from pin TENV or RENV		–	120	–	µA
$I_{sink(ENV)}$	maximum current sunk by pin TENV or RENV		−1.25	−1	−0.75	µA
ΔV_{ENV}	voltage difference between pins RENV and TENV	note 1; when 10 µA is sourced from both RSEN and TSEN; signal detectors tracking	–	±3	–	mV
Noise envelope detectors						
$I_{source(NOI)}$	maximum current sourced from pin TNOI or RNOI		0.75	1	1.25	µA
$I_{sink(NOI)}$	maximum current sunk by pin TNOI or RNOI		–	−120	–	µA
ΔV_{NOI}	voltage difference between pins RNOI and TNOI	note 1; when 5 µA is sourced from both RSEN and TSEN; noise detectors tracking	–	±3	–	mV
DIAL TONE DETECTOR						
$V_{HFRX(th)(rms)}$	threshold level at pin HFRX (RMS value)	R_{RSEN} = 10 kΩ	–	25	–	mV
TX LEVEL LIMITER						
$V_{TXIN(th)(rms)}$	threshold level at pin TXIN (RMS value)	R_{TSEN} = 10 kΩ	–	0.75	–	mV
DECISION LOGIC (PINS IDT AND SWT)						
Signal recognition						
$\Delta V_{Srx(th)}$	threshold voltage between pins RENV and RNOI to switch-over from receive to idle mode	note 2; $V_{HFRX} < V_{HFRX(th)}$	–	13	–	mV
$\Delta V_{Stx(th)}$	threshold voltage between pins TENV and TNOI to switch-over from transmit to idle mode	note 2; $V_{TXIN} < V_{TXIN(th)}$	–	13	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switch-over						
$I_{source(SWT)}$	current sourced from pin SWT when switching to receive mode		7.5	10	12.5	µA
$I_{sink(SWT)}$	current sunk by pin SWT when switching to transmit mode		−12.5	−10	−7.5	µA
$I_{idle(SWT)}$	current sourced from pin SWT in idle mode		–	0	–	µA
VOICE SWITCH (PINS STAB AND SWR)						
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referred to 365 kΩ	−40	–	+12	dB
$\lvert\Delta G_v\rvert$	voltage gain variation from transmit or receive mode to idle mode		–	20	–	dB
G_{tr}	gain tracking ($G_{vtx} + G_{vrx}$) during switching, referred to idle mode		–	0.5	–	dB

Notes

1. Corresponds to ±1 dB tracking.
2. Corresponds to 4.3 dB noise/speech recognition level.

TEST AND APPLICATION INFORMATION

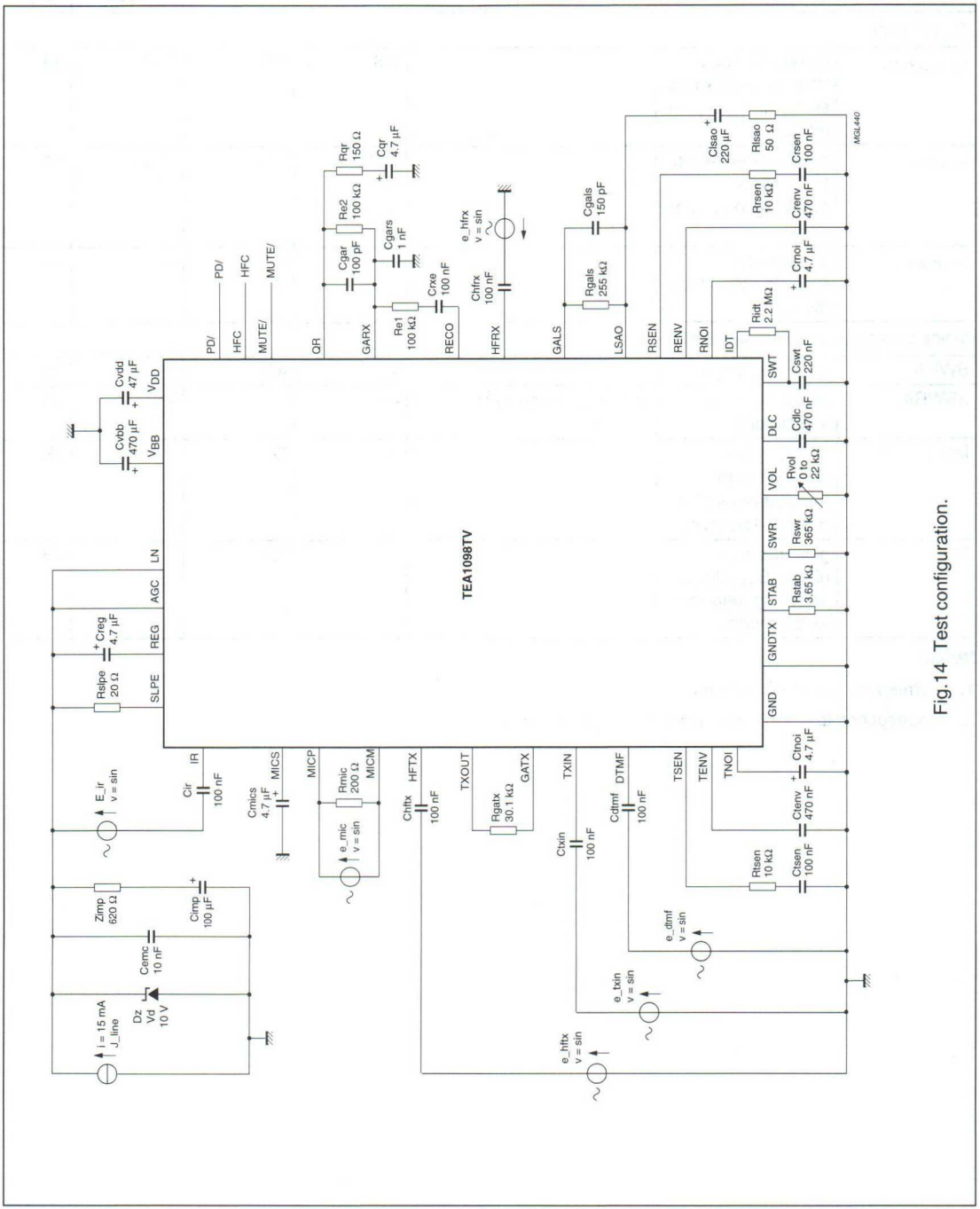


Fig.14 Test configuration.

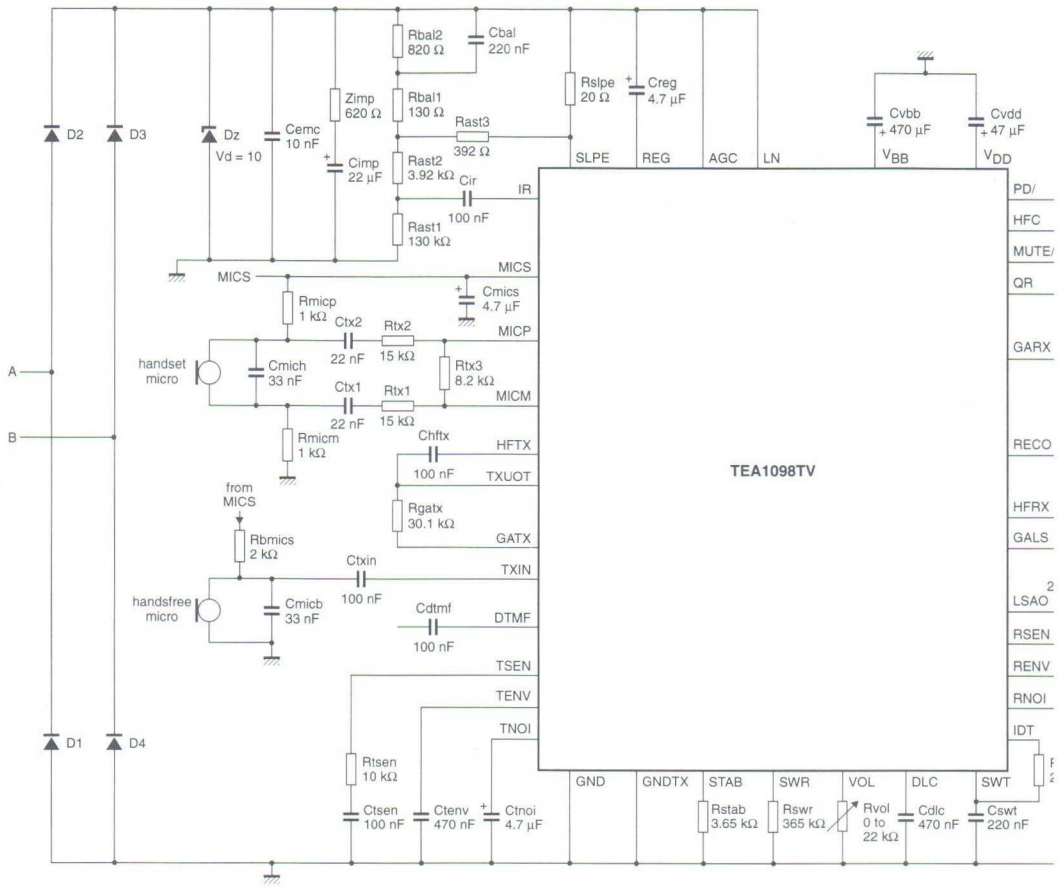


Fig.15 Basic application diagram.

Speech and Handsfree IC with auxiliary inputs/outputs and analog multiplexer

TEA1099H

FEATURES

Line interface

- Low DC line voltage
- Voltage regulator with adjustable DC voltage
- Symmetrical high impedance inputs (70 kΩ) for dynamic, magnetic or electret microphones
- DTMF input with confidence tone on earphone and/or loudspeaker
- Receive amplifier for dynamic, magnetic or piezo-electric earpieces (with externally adjustable gain)
- AGC: automatic gain control for true line loss compensation.

Supplies

- Provides a strong 3.35 V regulated supply for micro-controller or dialler
- Provides filtered power supply, optimized according to line current and compatible with external voltage or current sources
- Filtered 2 V power supply output for electret microphone
- Compatible with a ringer mode
- $\overline{PD}$ logic input for power down.

Handsfree

- Asymmetrical high input impedance for electret microphone
- Loudspeaker amplifier with single-ended rail-to-rail output and externally adjustable gain
- Dynamic limiter on loudspeaker amplifier to prevent distortion
- Logarithmic volume control on loudspeaker amplifier via linear potentiometer
- Duplex controller consisting of:
  - signal and noise envelope monitors for both channels (with adjustable sensitivities and timing)
  - decision logic (with adjustable switch-over and idle-mode timing)
  - voice switch control (with adjustable switching range and constant sum of gain during switching).

Auxiliary interfaces

- General auxiliary output for transmit and receive purposes
- Auxiliary transmit input with high signal level capability dedicated to line transmission
- Auxiliary receive input with high signal level capability
- Integrated multiplexer for channels selection.

APPLICATIONS

- Line powered telephone sets
- Cordless telephones
- Fax machines
- Answering machines.

GENERAL DESCRIPTION

The TEA1099H is an analog bipolar circuit dedicated for telephony applications. It includes a line interface, handset (HS) microphone and earpiece amplifiers, hands-free (HF) microphone and loudspeaker amplifiers, some specific auxiliary inputs/outputs (I/O's) and an analog multiplexer to enable the right transmit and/or receive channels. The multiplexer is controlled by a logic circuitry decoding four logic inputs provided by a micro-controller. Thirteen different application modes have been defined and can be accessed by selecting the right logic inputs. An application mode is a special combination of transmit and receive channels required by telephony applications.

This IC can be supplied by the line and/or by the mains if available (in a cordless telephone or an answering machine for example). It provides a 3.35 V supply for a micro-controller and a 2 V filtered voltage supply for an electret microphone. The IC is designed to facilitate the use of the loudspeaker amplifier during ringing phase.

QUICK REFERENCE DATA

I_{line} = 15 mA; R_{slpe} = 20 Ω; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; AGC pin connected to LN; $\overline{PD}$ = HIGH; HFC = LOW; AUXC = LOW; $\overline{MUTT}$ = HIGH; $\overline{MUTR}$ = HIGH; measured according to test circuits; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range	normal operation	11	–	140	mA
		with reduced performance	1	–	11	mA
V_{SLPE}	stabilized voltage between SLPE and GND	I_{line} = 15 mA	tbf	3.7	tbf	V
		I_{line} = 70 mA	tbf	6.15	tbf	V
V_{BB}	regulated supply voltage for internal circuitry	I_{line} = 15 mA	tbf	3.0	tbf	V
		I_{line} = 70 mA	tbf	5.35	tbf	V
V_{DD}	regulated supply voltage on pin V_{DD}	V_{BB} > 3.35 V + 0.25 V (typ)	–	3.35	3.6	V
		otherwise	–	V_{BB} – 0.25	–	V
V_{ESI}	external voltage supply allowed on pin ESI		–	–	6	V
I_{ESI}	external current supply allowed on pin ESI		–	–	140	mA
I_{BB}	current available on pin V_{BB}					
	in speech mode		–	11	–	mA
	in handsfree mode		–	9	–	mA
$I_{BB(PD)}$	current consumption on V_{BB} during power down phase	$\overline{PD}$ = LOW; AUXC = LOW	–	500	–	µA
$G_{v(MIC-LN)}$	voltage gain from pin MIC+/MIC– to LN	V_{MIC} = 5 mV (RMS)	tbf	44.6	tbf	dB
$G_{v(IR-RECO)}$	voltage gain from pin IR (referred to LN) to RECO	V_{IR} = 15 mV (RMS)	tbf	29.7	tbf	dB
$\Delta G_{v(QR)}$	gain voltage range between pins RECO and QR		–3	–	+15	dB
$G_{v(TXIN-TXOUT)}$	voltage gain from pin TXIN to TXOUT	V_{TXIN} = 8 mV (RMS); R_{GATX} = 30.1 kΩ	–	15.2	–	dB
$G_{v(HFTX-LN)}$	voltage gain from pin HFTX to LN	V_{HFTX} = 15 mV (RMS)	–	35	–	dB
$G_{v(HFRX-LSAO)}$	voltage gain from pin HFRX to LSAO	V_{HFRX} = 30 mV(RMS); R_{GALS} = 255 kΩ; I_{line} = 70 mA	–	27.8	–	dB
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referred to 365 kΩ	–40	–	+12	dB
$\Delta G_{v(trx)}$	gain control range for transmit and receive amplifiers affected by the AGC; with respect to I_{line} = 15 mA	I_{line} = 70 mA $G_{v(MIC-LN)}$, $G_{v(IR-RECO)}$ and $G_{v(IR-AUXO)}$	tbf	6.2	tbf	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1099H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body $10 \times 10 \times 1.75$ mm	SOT307-2

BLOCK DIAGRAM

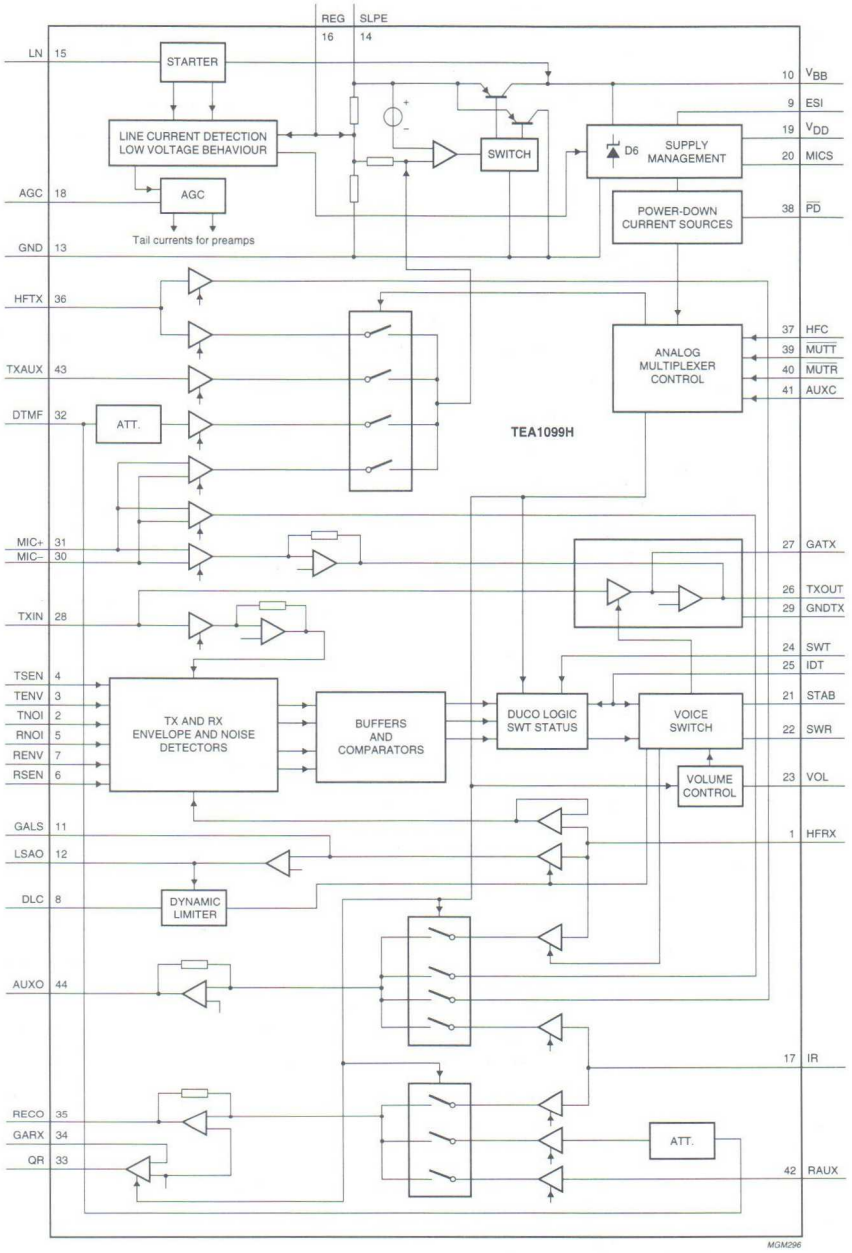


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
HFRX	1	receive input for loudspeaker amplifier or auxiliary receive amplifier
TNOI	2	transmit noise envelope timing adjustment
TENV	3	transmit signal envelope timing adjustment
TSEN	4	transmit signal envelope sensitivity adjustment
RNOI	5	receive noise envelope timing adjustment
RSEN	6	receive signal envelope sensitivity adjustment
RENV	7	receive signal envelope timing adjustment
DLC	8	dynamic limiter capacitor for the loudspeaker amplifier
ESI	9	external supply input
V_{BB}	10	stabilized supply for internal circuitry
GALS	11	loudspeaker amplifier gain adjustment
LSAO	12	loudspeaker amplifier output
GND	13	ground reference
SLPE	14	line current sense
LN	15	positive line terminal
REG	16	line voltage regulator decoupling
IR	17	receive amplifier input
AGC	18	automatic gain control / line loss compensation
V_{DD}	19	3.35 V regulated voltage supply for microcontrollers
MICS	20	microphone supply
STAB	21	reference current adjustment
SWR	22	switching range adjustment
VOL	23	loudspeaker volume adjustment
SWT	24	switch-over timing adjustment
IDT	25	idle mode timing adjustment
TXOUT	26	HF microphone amplifier output
GATX	27	HF microphone amplifier gain adjustment
TXIN	28	HF microphone amplifier input
GNDTX	29	ground reference for microphone amplifiers
MIC–	30	negative HS microphone amplifier input
MIC+	31	positive HS microphone amplifier input
DTMF	32	dual tone multi-frequency input
QR	33	earpiece amplifier output
GARX	34	earpiece amplifier gain adjustment
RECO	35	receive amplifier output
HFTX	36	transmit input for line amplifier or auxiliary receive amplifier
HFC	37	logic input
$\overline{PD}$	38	power-down input
$\overline{MUTT}$	39	logic input
$\overline{MUTR}$	40	logic input

SYMBOL	PIN	DESCRIPTION
AUXC	41	logic input
RAUX	42	auxiliary receive amplifier input
TXAUX	43	auxiliary transmit amplifier input
AUXO	44	auxiliary amplifier output

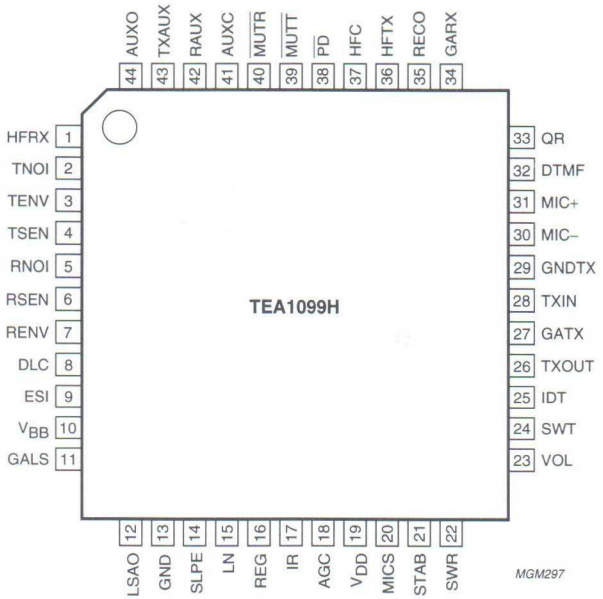


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supplies

LINE INTERFACE AND INTERNAL SUPPLY (PINS LN, SLPE, REG AND V_{BB})

The supply for the TEA1099H and its peripherals is obtained from the line. The IC generates a stabilized reference voltage (V_{ref}) between pins SLPE and GND. This reference voltage is equal to 3.7 V for line currents lower than 18 mA. It than increases linearly with the line current and reaches the value of 6.15 V for line currents higher than 46 mA. For line currents below 9 mA, the internal reference voltage generating V_{ref} is automatically adjusted to a lower value. This

is the so-called low voltage area and the TEA1099H has limited performances in this area (see "Low voltage behaviour" section). This reference voltage is temperature compensated.

The voltage between pins SLPE and REG is used by the internal regulator to generate the stabilized reference voltage and is decoupled by means of a capacitor between pins LN and REG. This capacitor converted into an equivalent inductance realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (done by an external impedance).

The IC regulates the line voltage at pin LN and it can be calculated as follows:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I^{x}$$

where:

I_{line} = line current

I^{x} = current consumed on pin LN (approximately a few μA)

I_{SLPE} = current flowing through the R_{SLPE} resistor

The preferred value for R_{SLPE} is 20 Ω. Changing this value will affect more than the DC characteristics; it also influences the transmit gains to the line, the gain control characteristic, the sidetone level and the maximum output swing on the line.

As can be seen from Fig.3, the internal circuitry is supplied by pin V_{BB}, which is a strong supply point combined with the line interface. The line current is flowing through the R_{SLPE} resistor and is sunk by the V_{BB} voltage stabilizer, becoming available for a loudspeaker amplifier or any peripheral IC. Its voltage is equal to 3.0 V for line currents lower than18 mA. It than increases linearly with the line current and reaches the value of 5.35 V for line currents greater than 46 mA. It is temperature compensated. See Fig.4 for the main DC voltages.

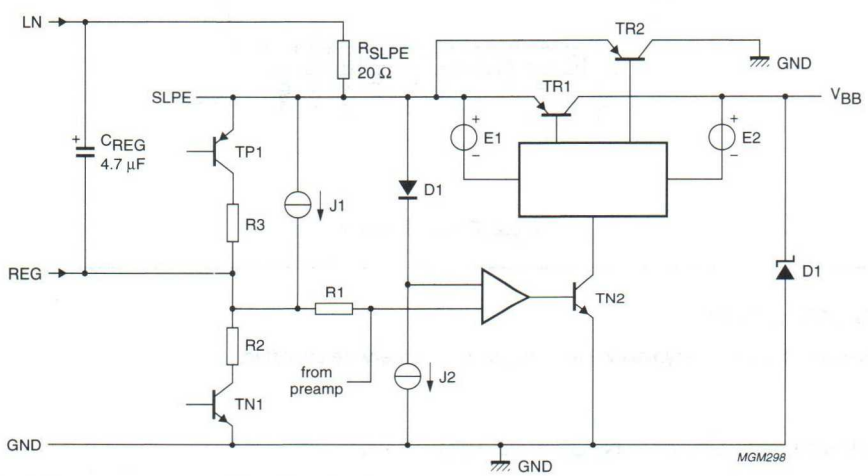


Fig.3 Line interface principle.

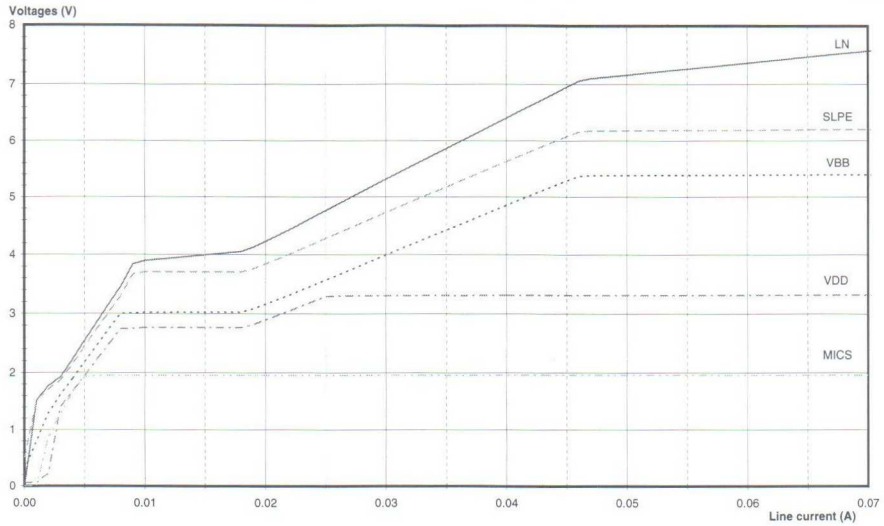


Fig.4 Main DC voltages

The aim of the current switch TR1-TR2 is to reduce distortion of large AC line signals. Current I_{SLPE} is supplied to V_{BB} via TR1 when the voltage on SLPE is greater than V_{BB} + 0.25 V. When the voltage on SLPE is lower than this value, the current I_{SLPE} is shunted to GND via TR2.

The reference voltage V_{ref} can be increased by connecting an external resistor between pins REG and SLPE. For large line currents, this increase can slightly affect some dynamic performances such as maximum signal level on the line for 2% THD. The voltage on pin V_{BB} is not affected by this external resistor.

External supply (pins ESI and V_{BB})

The TEA1099H can be supplied by the line as well as by external power sources (voltage or current sources) that must be connected at pin ESI.

The IC will choose which supply to use according to the voltage it can provide. A voltage supply on ESI is efficient only if its value is greater than the working voltage of the internal V_{BB} voltage stabilizer. Otherwise the IC continues to be line powered. The current consumed on this source is at least equal to the internal consumption. It increases with the voltage difference between the value forced on ESI and the working voltage of the internal stabilizer. The excess current compared to the internal consumption becomes then available for other purposes such as supplying a loudspeaker amplifier. The voltage source should not exceed 6 V. If the value of the external voltage source can be lower than the working voltage of the internal stabilizer, an external diode is required to avoid reverse current flowing into the external power supply.

In case of current source, the voltage on V_{BB} and ESI depends on the current available. It is internally limited to 6.6 V. The current source should not exceed 140 mA.

V_{DD} supply for micro-controller (pin V_{DD})

The voltage on V_{DD} supply point follows the voltage on V_{BB} with a difference typically equal to 250 mV and is internally limited to 3.35 V. This voltage is temperature compensated. This supply point can provide a current up to 3 mA typically. Its internal consumption stays low (a few 10 nA) as long as V_{DD} does not exceed 1.5 V (see Fig.5).

An external voltage can be connected on V_{DD} with limited extra consumption on V_{DD} (typically 120 μA). This voltage source should not be lower than 3.5 V and higher than 6 V.

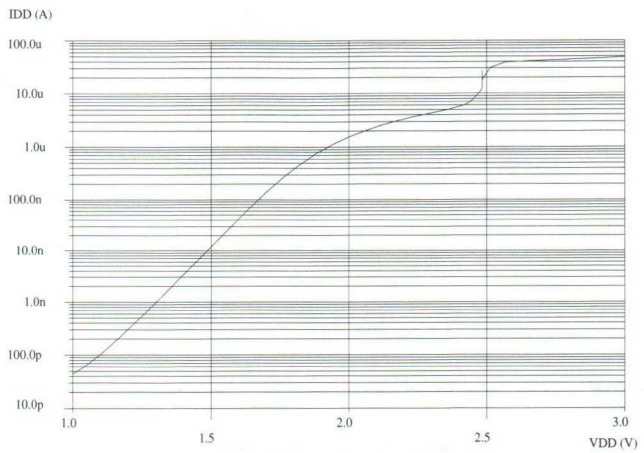


Fig.5 Current consumption on VDD

V_{BB} and V_{DD} can supply external circuits in the limit of currents provided either from the line or from ESI, taking into account the internal current consumption.

Supply for microphone (pins MICS and GNDTX)

The MICS output can be used as a supply for an electret microphone. Its voltage is equal to 2 V; it can source current up to 1 mA and has an output impedance equal to 200 Ω.

Low voltage behaviour

For line currents below 9 mA, the reference voltage is automatically adjusted to a lower value; the V_{BB} voltage follows the SLPE voltage with 250 mV difference. The excess current available for other purposes than DC biasing of the IC becomes small. In this low voltage area, the IC has limited performances.

When the V_{BB} voltage reaches 2.7 V, the V_{BB} detector of the receive dynamic limiter on LSAO acts and discharges the DLC capacitor.The loudspeaker is then automatically disabled below this DC voltage.

When V_{BB} becomes lower than 2.5 V, the TEA1099H is forced in a low voltage mode whatever the levels on the logic inputs are. It is a speech mode with reduced performances only enabling the microphone channel (between the MIC inputs and LN) and the earpiece amplifier. These two channels are able to deliver signals for line currents as small as 3 mA. The HFC input is tied to GND sinking a current typically equal to 300 μA.

Power-down mode (pins $\overline{PD}$ and AUXC)

To reduce consumption during dialling or register recall (flash), the TEA1099H is provided with a power-down input ($\overline{PD}$). When the voltage on both pins $\overline{PD}$ and AUXC is LOW, the current consumption from V_{BB} and V_{DD} is reduced to 500 μA. Therefore a capacitor of 470 μF on V_{BB} is sufficient to power the TEA1099H during pulse dialling or flash. The $\overline{PD}$ input has a pull-up structure, while AUXC has a pull-down structure. In this mode, the capacitor C_{REG} is internally disconnected.

RINGER MODE (PINS ESI, V_{BB}, AUXC AND $\overline{PD}$)

The TEA1099H is designed to be activated during the ringing phase. The loudspeaker amplifier can be used for the ringing signal. The IC must be powered by an external supply on ESI, while applying a 'high' level on the logic input AUXC and a 'low' level on $\overline{PD}$ input. Only the HFRX input and the LSAO output are activated, in order to limit the current consumption. Some dynamic limitation is provided to prevent the LSAO output from saturation and V_{BB} from being discharged below 2.7 V.

Transmit channels (pins MIC+, MIC−, DTMF, TXAUX, HFTX and LN)

HANDSET MICROPHONE AMPLIFIER (PINS MIC+, MIC− AND LN)

The TEA1099H has symmetrical microphone inputs. The input impedance between MIC+ and MIC− is typically equal to 70 kΩ. The voltage gain between pins MIC+/MIC− and LN is set to 44.6 dB. Without limitation from the output, the microphone input stage can accommodate signals up to 18 mV (RMS) at room temperature for 2% of total harmonic distortion (THD). The microphone inputs are biased at one diode voltage.

Automatic gain control is provided for line loss compensation.

DTMF AMPLIFIER (PINS DTMF, LN AND RECO)

The TEA1099H has an asymmetrical DTMF input. The input impedance between DTMF and GND is typically equal to 20 kΩ. The voltage gain between pins DTMF and LN is set to 25.7 dB. Without limitation from the output, the input stage can accommodate signals up to 180 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

When the DTMF amplifier is enabled, dialling tones may be sent on the line. These tones can be heard in the earpiece or in the loudspeaker at a low level. This is called the confidence tone. The voltage attenuation between pins DTMF and RECO is typically equal to −16.5 dB.

The DC biasing of this input is 0 V.

The automatic gain control has no effect on these channels.

AUXILIARY TRANSMIT AMPLIFIER (PINS TXAUX AND LN)

The TEA1099H has an asymmetrical auxiliary input TXAUX. The input impedance between TXAUX and GND is typically equal to 20 kΩ. The voltage gain between pins TXAUX and LN is set to 12.6 dB. Without limitation from the output, the input stage can accommodate signals up to 1.2 V (RMS) at room temperature for 2% of total harmonic distortion (THD). The TXAUX input is biased at two diodes voltage.

Automatic gain control is provided for line loss compensation.

HANDS-FREE TRANSMIT OUTPUT STAGE (PINS HFTX AND LN)

The TEA1099H has an asymmetrical HFTX input, which is mainly intended for use in combination with the TXOUT output. The input impedance between HFTX and GND is typically equal to 20 kΩ. The voltage gain between pins HFTX and LN is set to 35 dB. Without limitation from the output, the input stage can accommodate signals up to 95 mV (RMS) at room temperature for 2% of total harmonic distortion (THD). The HFTX input is biased at two diodes voltage.

Automatic gain control is provided for line loss compensation.

MICROPHONE MONITORING ON TXOUT (PINS MIC+, MIC− AND TXOUT)

The voltage gain between the microphone inputs MIC+/MIC− and the output TXOUT is set to 49.8 dB. This channel gives an image of the signal sent on the line while speaking in the handset microphone. Using an external circuitry, this signal can be used for several purposes such as sending dynamic limitation or anti-howling in a listening-in application. The TXOUT output is biased at two diodes voltage.

The automatic gain control has no effect on these channels.

Receive channels (pins IR, RAUX, RECO, GARX and QR)

RX AMPLIFIER (PINS IR AND RECO)

The receive amplifier has one input IR which is referred to the line. The input impedance between pins IR and LN is typically equal to 20 kΩ and the DC biasing between these pins is equal to one diode voltage. The gain between pins IR (referred to LN) and RECO is typically equal to 29.7 dB. Without limitation from the output, the input stage can accommodate signals up to 50 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

This receive amplifier has a rail-to-rail output RECO, which is designed for use with high ohmic (real) loads (larger than 5 kΩ). This output is biased at two diodes voltage.

Automatic gain control is provided for line loss compensation.

EARPIECE AMPLIFIER (PINS GARX AND QR)

The earpiece amplifier is an operational amplifier having its output (QR) and its inverting input (GARX) available. Its input signal comes, via a decoupling capacitor, from the receive RECO output. It is used in combination with two resistors to get the required gain or attenuation compared to the receive gain. It can be chosen between −3 dB and 15 dB.

Two external capacitors C_{GAR} (connected between GAR and QR) and C_{GARS} (connected between GAR and GND) ensure stability. The C_{GAR} capacitor provides a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAR} \times R_{E2}$. The relationship $C_{GARS} >= 10 \times C_{GAR}$ must be fulfilled.

The earpiece amplifier has a rail-to-rail output QR, biased at two diodes voltage. It is designed for use with low ohmic (real) loads (150 Ω) or capacitive loads (100 nF in series with 100 Ω).

AUXILIARY RECEIVE AMPLIFIER (PINS RAUX AND RECO)

The auxiliary receive amplifier has an asymmetrical input RAUX; it uses the RECO output. Its input impedance between pins RAUX and GND is typically equal to 20 kΩ. The voltage gain between pins RAUX and RECO is equal to − 2.3 dB. Without any limitation from the output, the input stage can accommodate signals up to 0.9 V (RMS) at room temperature for 2% of total harmonic distortion (THD).

This auxiliary amplifier has a rail-to-rail output RECO, which is designed for use with high ohmic (real) loads (larger than 5 kΩ). This output is biased at two diodes voltage.

The automatic gain control has no effect on this channel.

Auxiliary amplifiers using AUXO (pins MIC+, MIC−, HFTX, IR and AUXO)

The TEA1099H has an auxiliary output AUXO, biased at two diodes voltage. This output stage is a rail-to-rail one, designed for use with high ohmic (real) loads (larger than 5 kΩ). The AUXO output amplifier is used in three different channels, two transmit channels and one receive channel.

AUXILIARY AMPLIFIERS USING THE MICROPHONE INPUTS (PINS MIC+, MIC− AND AUXO)

The auxiliary transmit amplifier using the microphone MIC+/MIC− inputs has a gain of 25.2 dB referred to AUXO. Without limitation from the output, the input stage can accommodate signals up to 18 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

The automatic gain control has no effect on this channel.

AUXILIARY AMPLIFIERS USING HFTX (PINS HFTX AND AUXO)

The auxiliary transmit amplifier using the HFTX input has a gain of 15.2 dB referred to AUXO.

The automatic gain control has no effect on this channel.

RX AMPLIFIER USING IR (PINS IR AND AUXO)

The auxiliary receive amplifier uses pin IR as input. The input is referred to LN and the DC biasing between these two pins is one diode voltage. The voltage gain between the input IR (referred to LN) and the output AUXO is typically equal to 32.8 dB, which compensates typically the attenuation provided by the anti-sidetone network.

Automatic gain control is provided for line loss compensation.

AGC (pin AGC)

The TEA1099H performs automatic line loss compensation, which fits well with the true line attenuation. The automatic gain control varies the gain of some transmit and receive amplifiers in accordance with the DC line current. The control range is 6.2 dB for $G_{v(MIC-LN)}$, $G_{v(IR-RECO)}$ and $G_{v(IR-RECO)}$ and 6.65dB for the other affected channels, which corresponds approximately to a line length of 5.5 km for a 0.5 mm twisted-pair copper cable.

To enable this gain control, the pin AGC must be shorted to pin LN. The start current for compensation corresponds to a line current equal to typically 23 mA and the stop current to 57 mA. The start current can be increased by connecting an external resistor between pins AGC and LN. It can be increased up to 40 mA (using a resistor typically equal to 80 kΩ). The start and stop current will be maintained in a ratio equal to 2.5. By leaving the AGC pin opened, the gain control is disabled and no line loss compensation is performed.

Handsfree application

As can be seen from Fig.3, a loop is formed via the sidetone network in the line interface part and the acoustic coupling between loudspeaker and microphone of the hands-free part. When this loop gain is greater than 1, howling occurs. In a full duplex application, this would be the case. The loop-gain has to be much lower than 1 and therefore has to be decreased to avoid howling. This is achieved by the duplex controller. The duplex controller of the TEA1099H detects which channel has the 'largest' signal and then controls the gain of the microphone amplifier and the loudspeaker amplifier so that the sum of the gains remains constant.

As a result, the circuit in this hands-free application can be in three stable modes:

1. Transmit mode (Tx mode).

   The gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum.
2. Receive mode (RX mode).

   The gain of the loudspeaker amplifier is at its maximum and the gain of the microphone amplifier is at its minimum.
3. Idle mode.

   The gain of the amplifiers is halfway between their maximum and minimum value.

The difference between the maximum gain and minimum gain is called the switching range.

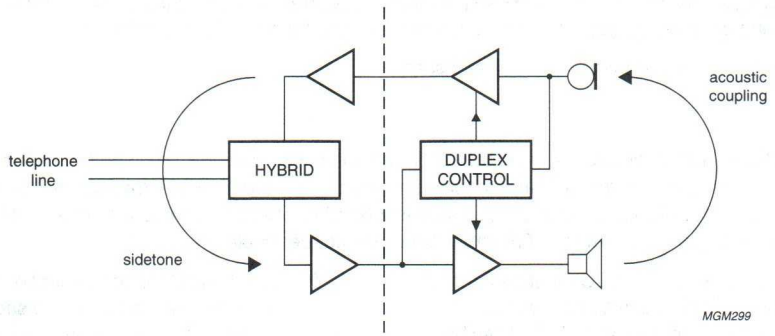


Fig.6 Hands-free telephone set principles.

HANDS-FREE MICROPHONE CHANNEL: PINS TXIN, GATX, TXOUT AND GNDTX (see Fig.7)

The TEA1099H has an asymmetrical hands-free microphone input TXIN with an input resistance of 20 kΩ. The DC biasing of the input is 0 V. The gain of the input stage varies according to the mode of the TEA1099H. In the transmit mode, the gain is at its maximum; in the receive mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum.

Switch-over from one mode to the other is smooth and click-free. The output TXOUT is biased at two diodes voltage and has a current capability equal to 20 μA (RMS). In the transmit mode, the overall gain of the microphone amplifier (from pins TXIN to TXOUT) can be adjusted from 0 dB up to 31 dB to suit specific application requirements. The gain is proportional to the value of R and equals 15.2 dB with R_{GATX} = 30.1 kΩ. Without limitation from the output, the microphone input stage can accommodate signals up to 18 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

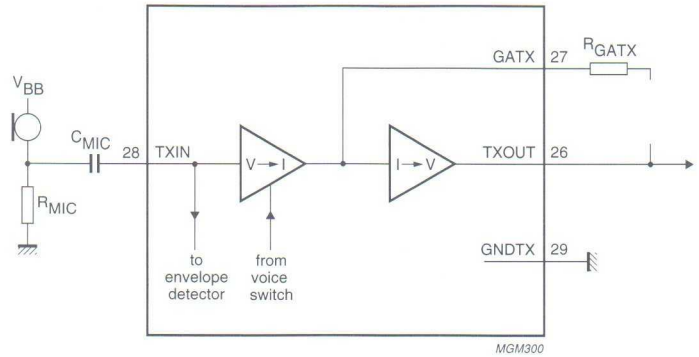


Fig.7 Hands-free microphone channel.

LOUDSPEAKER CHANNEL (SEE Fig.8)

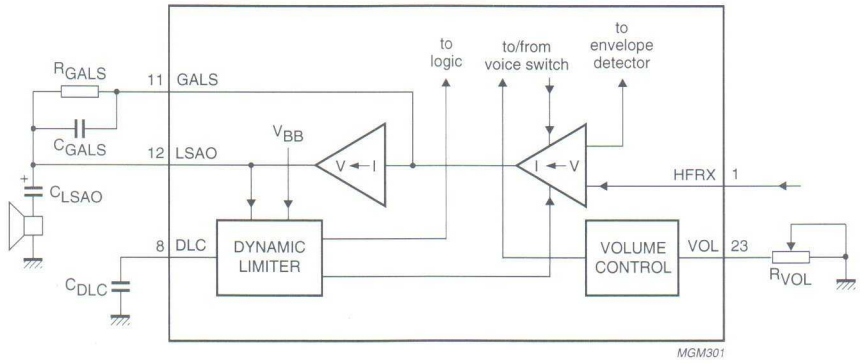


Fig.8 Loudspeaker channel.

Loudspeaker amplifier: pins HFRX, GALS and LSAO

The TEA1099H has an asymmetrical input for the loudspeaker amplifier with an input resistance of 20 kΩ between HFRX and GND. It is biased at two diodes voltage. Without limitation from the output, the input stage can accommodate signals up to 580 mV (RMS) at room temperature for 2% of total harmonic distortion (THD).

The gain of the input stage varies according to the mode of the TEA1099H. In the receive mode, the gain is at its maximum; in the transmit mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The rail-to-rail output stage is designed to power a loudspeaker connected as a single-ended load (between LSAO and GND).

In the receive mode, the overall gain of the loudspeaker amplifier can be adjusted from 0 dB up to 35 dB to suit specific application requirements. The gain from HFRX to LSAO is proportional to the value of R and equals 27.8 dB with R_{GALS} = 255 kΩ. A capacitor connected in parallel with R_{GALS} is recommended and provides a first-order low-pass filter.

Volume control: pin VOL

The loudspeaker amplifier gain can be adjusted with the potentiometer R_{VOL}. A linear potentiometer can be used to obtain logarithmic control of the gain at the loudspeaker amplifier. Each 1.9 kΩ increase of R_{VOL} results in a gain loss of 3 dB. The maximum gain reduction with the volume control is internally limited to the switching range.

Dynamic limiter: pin DLC

The dynamic limiter of the TEA1099H prevents clipping of the loudspeaker output stage and protects the operation of the circuit when the supply voltage at V_{BB} falls below 2.7 V.

Hard clipping of the loudspeaker output stage is prevented by rapidly reducing the gain when the output stage starts to saturate. The time in which gain reduction is effected (clipping attack time) is approximately a few milliseconds. The circuit stays in the reduced gain mode until the peaks of the loudspeaker signal no longer cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time (typically 250 ms). Both attack and release times are proportional to the value of the capacitor C_{DLC}. The total harmonic distortion of the loudspeaker output stage, in reduced gain mode, stays below 2% up to 10 dB (minimum) of input voltage overdrive [providing V is below

When the supply voltage drops below an internal threshold voltage of 2.7 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). When the supply voltage exceeds 2.7 V, the gain of the loudspeaker amplifier is increased again.

By forcing a level lower than 0.2 V on pin DLC, the loudspeaker amplifier is muted and the TEA1099H is automatically forced into the transmit mode.

RX amplifier using AUXO

In some cordless applications, the handset may be used to perform hands-free function (instead of the base). As the TEA1099H is in the base and the active loudspeaker in the handset, a second receive output is required. The amplifier using HFRX as an input and AUXO as an output will be used for communication with the RF IC, sending information to the handset. It will be controlled by the duplex controller in the same way as the loudspeaker amplifier.

The voltage gain between pins HFRX and AUXO is equal to 3.5 dB. The amplifier can manage the same input signal as the loudspeaker amplifier. It has a rail-to-rail output, biased at two diodes, designed for use with high ohmic (real) loads (larger than 5 kΩ). The volume control and the dynamic limiter don't have any action on this channel.

DUPLEX CONTROLLER

Signal and noise envelope detectors: pins TSEN, TENV, TNOI, RSEN, RENV and RNOI

The signal envelopes are used to monitor the signal level strength in both channels. The noise envelopes are used to monitor background noise in both channels. The signal and noise envelopes provide inputs for the decision logic. The signal and noise envelope detectors are shown in Fig.9.

For the transmit channel, the input signal at TXIN is 40 dB amplified to TSEN. For the receive channel, the input signal at HFRX is 0 dB amplified to RSEN. The signals from TSEN and RSEN are logarithmically compressed and buffered to TENV and RENV respectively. The sensitivity of the envelope detectors is set with R_{TSEN} and R_{RSEN}. The capacitors connected in series with the two resistors block any DC component and form a first-order high-pass filter. In the basic

application, see Fig.16, it is assumed that V_{TXIN} = 1 mV (RMS) and V_{HFRX} = 100 mV (RMS) nominal and both R_{TSEN} and R_{RSEN} have a value of 10 kΩ. With the value of C_{TSEN} and C_{RSEN} at 100 nF, the cut-off frequency is at 160 Hz.

The buffer amplifiers leading the compressed signals to TENV and RENV have a maximum source current of 120 µA and a maximum sink current of 1 µA. Together with the capacitor C_{TENV} and C_{RENV}, the timing of the signal envelope monitors can be set. In the basic application, the value of both capacitors is 470 nF. Because of the logarithmic compression, each 6 dB signal increase means 18 mV increase of the voltage on the envelopes TENV or RENV at room temperature. Thus, timings can be expressed in dB/ms. At room temperature, the 120 µA sourced current corresponds to a maximum rise-slope of the signal envelope of 85 dB/ms. This is sufficient to track normal speech signals. The 1 µA current sunk by TENV or RENV corresponds to a maximum fall-slope of 0.7 dB/ms. This is sufficient for a smooth envelope and also eliminates the effect of echoes on switching behaviour.

To determine the noise level, the signals on TENV and RENV are buffered to TNOI and RNOI. These buffers have a maximum source current of 1 µA and a maximum sink current of 120 µA. Together with the capacitors C_{TNOI} and C_{RNOI}, the timing can be set. In the basic application, see Fig.16, the value of both capacitors is 4.7 µF. At room temperature, the 1 µA sourced current corresponds to a maximum rise-slope of the noise envelope of approximately 0.07 dB/ms.

This is small enough to track background noise and not to be influenced by speech bursts. The 120 µA current that is sunk corresponds to a maximum fall-slope of approximately 8.5 dB/ms. However, during the decrease of the signal envelope, the noise envelope tracks the signal envelope so it will never fall faster than approximately 0.7 dB/ms. The behaviour of the signal envelope and noise envelope monitors is illustrated in Fig.10.

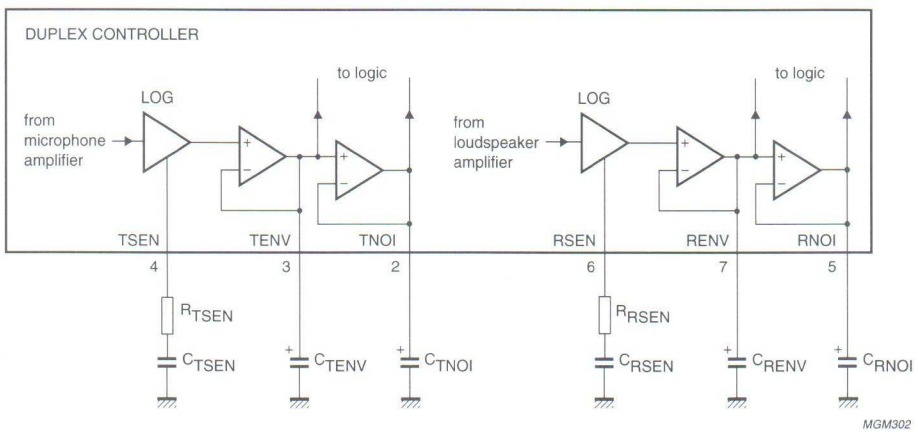


Fig.9 Signal and noise envelope detectors.

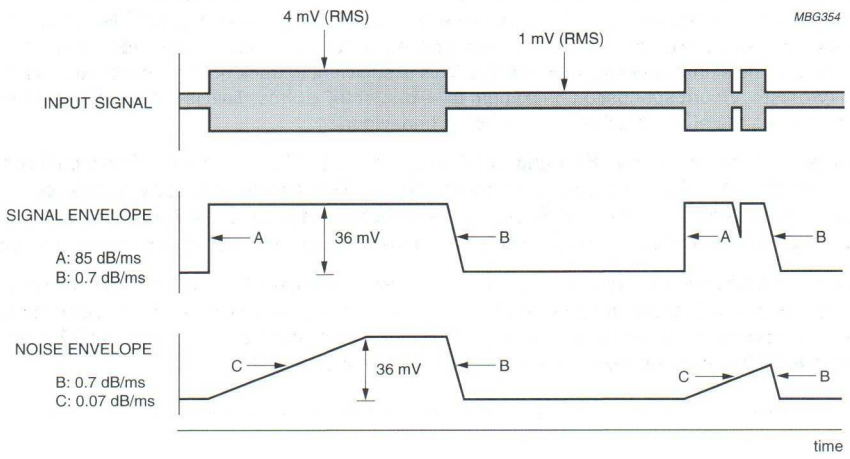
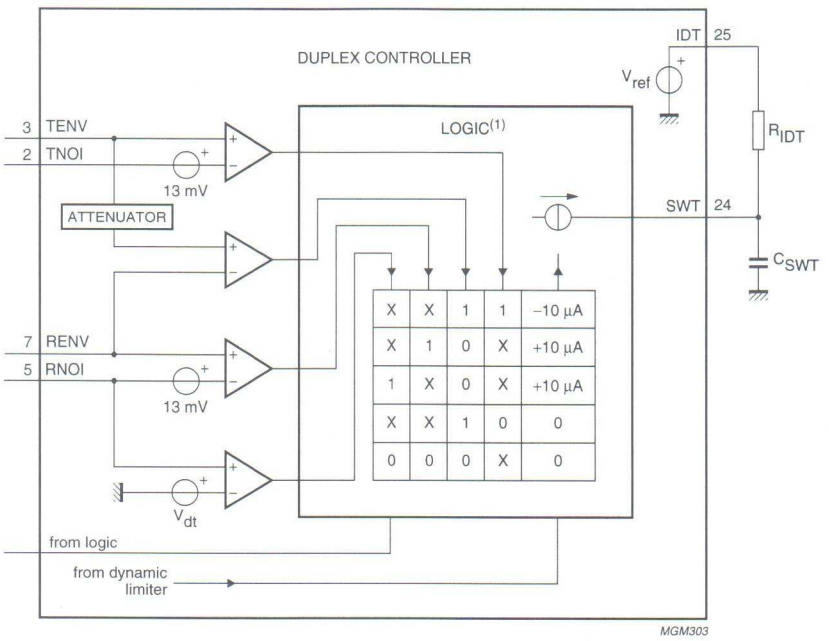


Fig.10 Signal and noise envelope waveforms.

Decision logic: pins IDT and SWT



X	X	1	1	−10 µA
X	1	0	X	+10 µA
1	X	0	X	+10 µA
X	X	1	0	0
0	0	0	X	0

(1) When DLC < 0.2 V, −10 µA is forced.

Fig.11 Decision logic.

The TEA1099H selects its mode of operation (transmit, receive or idle mode) by comparing the signal and the noise envelopes of both channels. This is executed by the decision logic. The resulting voltage on pin SWT is the input for the voice-switch.

To facilitate the distinction between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference $V_{ENV} - V_{NOI} = 13$ mV. This so called speech/noise threshold is implemented in both channels.

The signal on pin TXIN contains both speech and the signal coming from the loudspeaker (acoustic coupling). When receiving, the contribution from the loudspeaker overrules the speech. As a result, the signal envelope on TENV is formed mainly by the loudspeaker signal. To correct this, an attenuator is connected between TENV and the TENV/RENV comparator. Its attenuation equals that applied to the microphone amplifier.

When a dial tone is present on the line, without monitoring, the tone would be recognized as noise because it is a signal with a constant amplitude. This would cause the TEA1099H to go into the idle mode and the user of the set would hear the dial tone fade away. To prevent this, a dial tone detector is incorporated which, in standard applications, does not

consider input signals between HFRX and GND as noise when they have a level greater than 25 mV (RMS). This level is proportional to R_{RSEN}.

In the same way, a transmit detector is integrated which, in standard applications, does not consider input signals between TXIN and GNDTX as noise when they have a level greater than 0.75 mV (RMS). This level is proportional to R_{TSEN}.

As can be seen from Fig.11, the output of the decision logic is a current source. The logic table gives the relationship between the inputs and the value of the current source. It can charge or discharge the capacitor C_{SWT} with a current of 10 μA (switch-over). If the current is zero, the voltage on SWT becomes equal to the voltage on IDT via the high-ohmic resistor R_{IDT} (idling). The resulting voltage difference between SWT and IDT determines the mode of the TEA1099H and can vary between −400 and +400 mV (see Table 1).

Table 1 Modes of TEA1099H

$V_{SWT} - V_{IDT}$ (mV)	MODE
<−180	transmit mode
0	idle mode
>180	receive mode

The switch-over timing can be set with C_{SWT}, the idle mode timing with C_{SWT} and R_{IDT}. In the basic application given in Fig.16, C_{SWT} is 220 nF and R_{IDT} is 2.2 MΩ. This enables a switch-over time from transmit to receive mode or vice-versa of approximately 13 ms (580 mV swing on SWT). The switch-over time from idle mode to transmit mode or receive mode is approximately 4 ms (180 mV swing on SWT).

The switch-over time, from receive mode or transmit mode to idle mode is equal to $4 \times R_{IDT}C_{SWT}$ and is approximately 2 seconds (idle mode time).

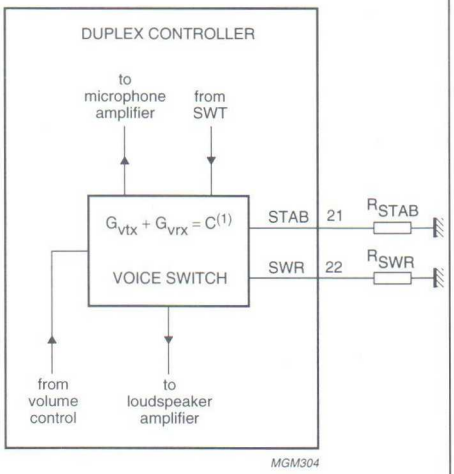
The input DLC overrules the decision logic. When the voltage on pin DLC goes lower than 0.2 V, the capacitor C_{SWT} is discharged with 10 μA thus resulting in the transmit mode.

Voice-switch: pins STAB and SWR

A diagram of the voice-switch is illustrated in Fig.12. With the voltage on SWT, the TEA1099H voice-switch regulates the gains of the transmit and the receive channels so that the sum of both is kept constant.

In the transmit mode, the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum. In the receive mode, the opposite applies. In the idle mode, both microphone and loudspeaker amplifier gains are halfway. The difference between maximum and minimum is the so called switching range. This range is determined by the ratio of R_{SWR} and R_{STAB} and is adjustable between 0 and 52 dB. R_{STAB} should be 3.65 kΩ and sets an internally used reference current. In the basic application diagram given in Fig.16, R_{SWR} is 365 kΩ which results in a switching range of 40 dB. The switch-over behaviour is illustrated in Fig.13.

In the receive mode, the gain of the loudspeaker amplifier can be reduced using the volume control. Since the voice-switch keeps the sum of the gains constant, the gain of the microphone amplifier is increased at the same time (see dashed curves in Fig.13). In the transmit mode, however, the volume control has no influence on the gain of the microphone amplifier or the gain of the loudspeaker amplifier. Consequently, the switching range is reduced when the volume is reduced. At maximum reduction of volume, the switching range becomes 0 dB.



(1) C = constant.

Fig.12 Voice switch.

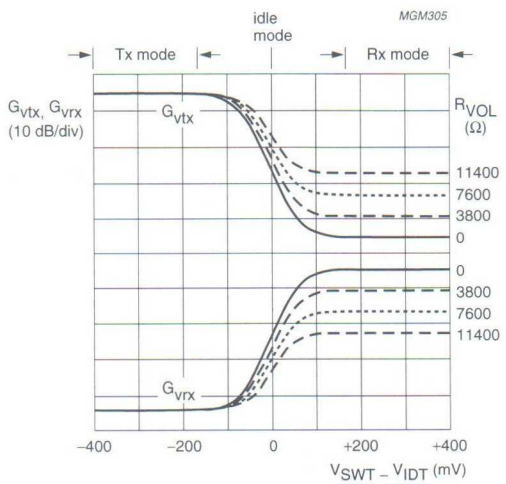


Fig.13 Switch-over behaviour.

Logic inputs

Table 2 Selection of transmit and receive channels for 13 different application modes.

LOGIC INPUTS					FEATURES	APPLICATION EXAMPLES
$\overline{PD}$	HFC	$\overline{MUTT}$	$\overline{MUTR}$	AUXC		
0	X	X	X	1	HFRX to LSAO	ringer mode
0	X	X	X	0		flash, DC dialling
1	0	0	0	0	DTMF to LN; DTMF to RECO; QR and MICS are active	DTMF dialling (tel. set)
1	0	0	1	0	MIC to AUXO; RAUX to RECO; QR and MICS are active	cordless intercom with handset
1	0	1	1	0	MICS to LN; IR to RECO; IR to AUXO MIC to TXOUT; QR and MICS are active	handset conversation (tel. set)
1	0	1	0	1	TXAUX to LN; IR to AUXO	conversation using auxiliary I/O such as cordless conversation
1	1	1	1	1	TXIN to TXOUT; HFTX to LN; IR to RECO; HFRX to AUXO	cordless: HF mode in handset
1	1	0	1	1	RAUX to RECO; HFRX to LSAO	listening on the loudspeaker
1	1	0	0	1	TXAUX to LN; IR to AUXO; RAUX to RECO; HFRX to LSAO	answering machine: play and record messages; listen the recorded message on the loudspeaker
1	1	0	0	0	DTMF to LN; DTMF to RECO; HFRX to LSAO; QR and MICS are active	DTMF dialling in HF/GL modes
1	1	1	0	1	TXAUX to LN; IR to AUXO; IR to RECO; HFRX to LSAO	answering machine: play and record messages while listening in the loudspeaker
1	1	0	1	0	TXIN to TXOUT; HFTX to AUXO; RAUX to RECO; HFRX to LSAO; MICS is active	cordless intercom with base
1	1	1	1	0	TXIN to TXOUT; HFTX to LN; IR to RECO; IR to AUXO; HFRX to LSAO; MICS is active	HF conversation mode
1	1	1	0	0	MIC to LN; IR to RECO; IR to AUXO; HFRX to LSAO; MIC to TXOUT; QR; MICS is active	handset conversation with listening-in

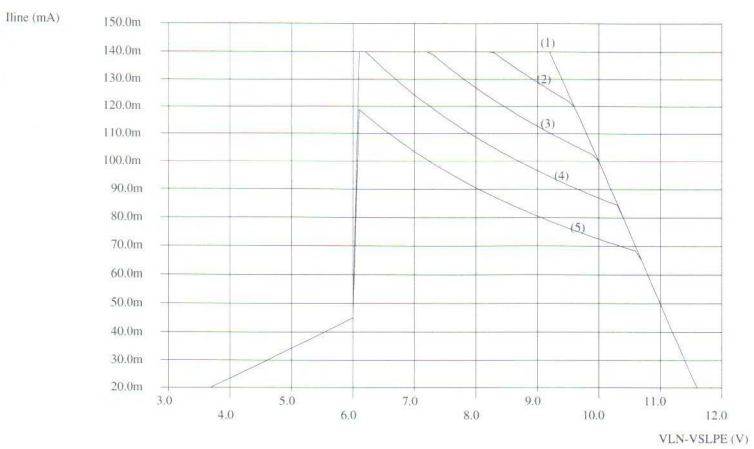
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		GND–0.4	12	V
	repetitive line voltage during switch-on or line interruption		GND–0.4	13.2	V
V_{ESI}	positive continuous voltage on pin ESI		GND–0.4	6	V
I_{ESI}	input current at pin ESI		–	140	mA
$V_{n(max)}$	maximum voltage on pins REG, SLPE, IR, AGC		GND–0.4	V_{LN}+0.4	V
	maximum voltage on all other pins except V_{DD}		GND–0.4	V_{BB}+0.4	V
I_{line}	maximum line current		–	140	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C	–	720	mW
T_{stg}	IC storage temperature		–40	125	°C
T_{amb}	operating ambient temperature		–25	75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	63	K/W



LINE	T_{amb} (°C)	P_{tot} (mW)
(1)	35	1304
(2)	45	1158
(3)	55	1012
(4)	65	866
(5)	75	720

Fig.14 Safe operating area (TEA1099H).

CHARACTERISTICS

I_{line} = 15 mA; R_{slpe} = 20 Ω; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25°C; AGC pin connected to LN; $\overline{PD}$ = HIGH; HFC = LOW; AUXC = LOW; $\overline{MUTT}$ = HIGH; $\overline{MUTR}$ = HIGH; measured according to test circuits; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
LINE INTERFACE AND INTERNAL SUPPLY (PINS LN, SLPE, REG AND V_{BB})						
V_{SLPE}	stabilized voltage between SLPE and GND	I_{line} = 15 mA	tbf	3.7	tbf	V
		I_{line} = 70 mA	tbf	6.15	tbf	V
V_{BB}	regulated supply voltage for internal circuitry	I_{line} = 15 mA	tbf	3.0	tbf	V
		I_{line} = 70 mA	tbf	5.35	tbf	V
I_{line}	line current for voltage increase					
	start current		–	18	–	mA
	stop current		–	46	–	mA
$\Delta V_{SLPE(T)}$	stabilized voltage variation with temperature referred to 25°C	T_{amb} = −25 to +75°C	–	±60	–	mV
$\Delta V_{BB(T)}$	regulated voltage variation with temperature referred to 25°C	T_{amb} = −25 to +75°C	–	±30	–	mV
I_{BB}	current available on V_{BB}					
	speech mode		–	11	–	mA
	handsfree mode		–	9	–	mA
V_{LN}	line voltage	I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	2.4	–	V
		I_{line} = 15 mA	tbf	4.0	tbf	V
		I_{line} = 140 mA	–	8.7	9.5	V
EXTERNAL SUPPLY (PIN ESI)						
V_{ESI}	external voltage supply allowed on pin ESI		–	–	6	V
I_{ESI}	input current on pin ESI	V_{ESI} = 3.5 V	–	3.1	–	mA
I_{ESI}	external current supply allowed on pin ESI		–	–	140	mA
V_{ESI}	voltage on pin ESI when supplied by a current source	I_{ESI} = 140 mA	–	6.6	–	V
SUPPLY FOR PERIPHERALS (PIN V_{DD})						
V_{DD}	regulated supply voltage on V_{DD}	V_{BB} > 3.35 V + 0.25 V (typ.)	–	3.35	3.6	V
		otherwise	–	V_{BB} − 0.25	–	V
$\Delta V_{DD(T)}$	regulated voltage variation with temperature referred to 25°C	T_{amb} = −25 to +75°C; V_{BB} > 3.35 V + 0.25 V (typ.)	–	±30	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DD}	current consumption on V_{DD} (capacitor disconnected)	in trickle mode; I_{line} = 0 mA; V_{DD} = 1.5 V; V_{BB} discharging	–	15	150	nA
		V_{DD} > 3.35 V	60	120	–	µA
$I_{DD(o)}$	current available for peripherals	V_{DD} = 3.35 V	–	–	–3	mA
SUPPLY FOR MICROPHONE (PIN MICS)						
V_{MICS}	supply voltage for a microphone	I_{MICS} = 0 mA	–	2	–	V
I_{MICS}	current available on MICS		–	–	–1	mA
POWER DOWN INPUT (PIN $\overline{PD}$)						
V_{IL}	low level input voltage		GND–0.4	–	GND+0.3	V
V_{IH}	high level input voltage		GND+1.8	–	V_{BB} +0.4	V
$I_{\overline{PD}}$	input current		–	–3	–6	µA
$I_{BB(PD)}$	current consumption on V_{BB} during power down phase	$\overline{PD}$ = LOW; AUXC = LOW	–	500	–	µA
RINGER MODE (PINS $\overline{PD}$, AUXC, HFRX, LSAO)						
I_{ESI}	input current on pin ESI	$\overline{PD}$ = LOW; AUXC = HIGH; V_{ESI} = 3.5 V	–	3.2	–	mA
$G_{v(HFRX-LSAO)}$	voltage gain from pin HFRX to LSAO	$\overline{PD}$ = LOW; AUXC = HIGH; V_{ESI} = 3.5 V; V_{HFRX} = 20 mV (RMS); R_{GALS} = 255 kΩ	–	29	–	dB
Preamplifier inputs (pins MIC+, MIC–, IR, DTMF, TXIN, HFTX, HFRX, TXAUX, RAUX)						
$\lvert Z_{i(MIC)} \rvert$	input impedance					
	differential between pins MIC+ and MIC–		–	70	–	kΩ
	single-ended between pins MIC+/MIC– and GNDTX		–	35	–	kΩ
$\lvert Z_{i(IR)} \rvert$	input impedance between pins IR and LN		–	20	–	kΩ
$\lvert Z_{i(DTMF)} \rvert$	input impedance between pins DTMF and GND		–	20	–	kΩ
$\lvert Z_{i(TXIN)} \rvert$	input impedance between pins TXIN and GNDTX		–	20	–	kΩ
$\lvert Z_{i(HFTX)} \rvert$	input impedance between pins HFTX and GND		–	20	–	kΩ
$\lvert Z_{i(HFRX)} \rvert$	input impedance between pins HFRX and GND		–	20	–	kΩ
$\lvert Z_{i(TXAUX)} \rvert$	input impedance between pins TXAUX and GND		–	20	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Z_{i(RAUX)} \rvert$	input impedance between pins RAUX and GND		–	20	–	kΩ
TX amplifiers						
TX HANDSET MICROPHONE AMPLIFIER (PINS MIC+, MIC– AND LN) NOTE 1						
$G_{v(MIC-LN)}$	voltage gain from pin MIC+/MIC– to LN	V_{MIC} = 5 mV (RMS)	tbf	44.6	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.25	–	dB
CMRR	common mode rejection ratio		–	80	–	dB
THD	total harmonic distortion at LN	V_{LN} = 1.4 V (RMS)	–	–	2	%
		I_{line} = 4 mA; V_{LN} = 0.12 V (RMS)	–	–	10	%
$V_{no(LN)}$	noise output voltage at pin LN; pins MIC+/MIC– shorted through 200 Ω	psophometrically weighted (p53 curve)	–	–77.5	–	dBmp
$\Delta G_{v(m)}$	gain reduction if not activated	HFC = LOW; $\overline{MUTT}$ = LOW; $\overline{MUTR}$ = LOW; AUXC = LOW;	60	80	–	dB
DTMF AMPLIFIER (PINS DTMF, LN AND RECO) NOTE 1						
$G_{v(DTMF-LN)}$	voltage gain from pin DTMF to LN	V_{DTMF} = 50 mV (RMS)	tbf	25.7	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.25	–	dB
$\Delta G_{v(m)}$	gain reduction if not activated	HFC = LOW; $\overline{MUTT}$ = HIGH; $\overline{MUTR}$ = HIGH; AUXC = LOW;	60	80	–	dB
$G_{v(DTMF-RECO)}$	voltage gain from pin DTMF to RECO	V_{DTMF} = 50 mV (RMS)	–	–16.5	–	dB
TX AUXILIARY AMPLIFIER USING TXAUX (PINS TXAUX AND LN) NOTE 1						
$G_{v(TXAUX-LN)}$	voltage gain from pin TXAUX to LN	V_{TXAUX} = 0.1 V (RMS)	tbf	12.6	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.25	–	dB
THD	Total harmonic distortion at LN	V_{LN} = 1.4 V (RMS)	–	–	2	%
$V_{TXAUX(rms)}$	Maximum input voltage at TXAUX (RMS value)	I_{line} = 70 mA; THD = 2%	1	1.2	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{no(LN)}$	noise output voltage at pin LN; pin TXAUX shorted to GND through 200 Ω in series with 10 µF	psophometrically weighted (p53 curve)	–	–80.5	–	dBmp
$\Delta G_{v(m)}$	gain reduction if not activated	HFC = LOW; $\overline{MUTT}$ = HIGH; $\overline{MUTR}$ = HIGH; AUXC = LOW;	60	80	–	dB
TX AMPLIFIER USING HFTX (PINS HFTX AND LN) NOTE 1						
$G_{v(HFTX-LN)}$	voltage gain from pin HFTX to LN	V_{HFTX} = 15 mV (RMS)	tbf	35	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.25	–	dB
THD	total harmonic distortion at LN	V_{LN} = 1.4 V (RMS)	–	–	2	%
$V_{HFTX(rms)}$	Maximum input voltage at HFTX (RMS value)	I_{line} = 70 mA; THD = 2%	75	95	–	mV
$V_{no(LN)}$	noise output voltage at pin LN; pin HFTX shorted to GND through 200 Ω in series with 10 µF	psophometrically weighted (p53 curve)	–	–77.5	–	dBmp
$\Delta G_{v(m)}$	gain reduction if not activated	HFC = LOW; $\overline{MUTT}$ = HIGH; $\overline{MUTR}$ = LOW; AUXC = HIGH;	60	80	–	dB
MICROPHONE MONITORING ON TXOUT (PINS MIC+, MIC– AND TXOUT) NOTE 1						
$G_{v(MIC-TXOUT)}$	voltage gain from pin MIC+/MIC– to TXOUT	V_{MIC} = 2 mV (RMS)	tbf	49.8	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.1	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.35	–	dB
RX amplifiers						
RX AMPLIFIERS USING IR (PINS IR AND RECO) NOTE 1						
$G_{v(IR-RECO)}$	voltage gain from pin IR (referred to LN) to RECO	V_{IR} = 15 mV (RMS)	tbf	29.7	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.3	–	dB
$V_{IR/LN(rms)}$	Maximum input voltage on IR (referred to LN) (RMS value)	I_{line} = 70 mA; THD = 2%	40	50	–	mV
$V_{RECO(rms)}$	Maximum output voltage on RECO (RMS value)	THD = 2%	0.75	0.9	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{no(RECO)(rms)}$	noise output voltage at pin RECO; pin IR is an open circuit (RMS value)	psophometrically weighted (p53 curve)	–	–88	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	HFC = LOW; $\overline{MUTT}$ = LOW; $\overline{MUTR}$ = LOW; AUXC = LOW;	60	80	–	dB
RX EARPIECE AMPLIFIER (PINS GARX AND QR) NOTE 1						
$\Delta G_{v(QR)}$	gain voltage range between pins RECO and QR		–3	–	+15	dB
$V_{QR(rms)}$	maximum output voltage on QR (RMS value)	sine wave drive; R_L = 150 Ω; THD < 2%	0.75	0.9	–	V
$V_{no(QR)(rms)}$	noise output voltage at pin QR; pin IR is an open circuit (RMS value)	$G_{v(QR)}$ = 0 dB; psophometrically weighted (p53 curve)	–	–88	–	dBVp
RX AMPLIFIER USING RAUX (PINS RAUX AND RECO) NOTE 1						
$G_{v(RAUX-RECO)}$	voltage gain from pin RAUX to RECO	V_{RAUX} = 0.4 V (RMS)	tbf	–2.3	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.25	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.25	–	dB
$V_{RAUX(rms)}$	Maximum input voltage on RAUX (RMS value)	THD = 2%	0.8	0.95	–	V
$V_{no(RECO)(rms)}$	noise output voltage at pin RECO; pin RAUX shorted to GND through 200 Ω in series with 10 μF (RMS value)	psophometrically weighted (p53 curve)	–	–100	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	HFC = LOW; $\overline{MUTT}$ = LOW; $\overline{MUTR}$ = LOW; AUXC = LOW;	60	80	–	dB
Auxiliary amplifiers using AUXO						
TX AUXILIARY AMPLIFIER USING MIC+ AND MIC– (PINS MIC+, MIC– AND AUXO) NOTE 1						
$G_{v(MIC-AUXO)}$	voltage gain from pin MIC+/MIC– to AUXO	V_{MIC} = 10 mV (RMS)	tbf	25.2	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.1	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.3	–	dB
$V_{MIC(rms)}$	Maximum input voltage on MIC+/MIC- (RMS value)	THD = 2%	–	18	-	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{no(AUXO)}$	noise output voltage at pin AUXO; pins MIC+/MIC– shorted to GNDTX through 200 Ω in series with 10 µF (RMS value)	psophometrically weighted (p53 curve)	–	–91	–	dBVp
TX AUXILIARY AMPLIFIER USING HFTX (PINS HFTX AND AUXO) NOTE 1						
$G_{v(HFTX-AUXO)}$	voltage gain from pin HFTX to AUXO	V_{HFTX} = 100 mV (RMS)	tbf	15.2	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.1	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.1	–	dB
$V_{AUXO(rms)}$	Maximum output voltage on AUXO (RMS value)	THD = 2%	0.8	0.9	–	V
$V_{no(AUXO)}$	noise output voltage at pin AUXO; pin TXAUX shorted to GND through 200 Ω in series with 10 µF (RMS value)	psophometrically weighted (p53 curve)	–	–91.5	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	HFC =LOW; $\overline{MUTT}$ = LOW; $\overline{MUTR}$ = HIGH; AUXC = LOW;	60	80	–	dB
RX AMPLIFIER USING IR (PINS IR AND AUXO) NOTE 1						
$G_{v(IR-AUXO)}$	voltage gain from pin IR (referred to LN) to AUXO	V_{IR} = 8 mV (RMS)	tbf	32.8	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.1	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.3	–	dB
$V_{AUXO(rms)}$	Maximum output voltage on AUXO (RMS value)	THD = 2%	0.8	0.9	–	V
$V_{no(AUXO)(rms)}$	noise output voltage at pin AUXO; pin IR is an open circuit (RMS value)	psophometrically weighted (p53 curve)	–	–85	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	HFC = HIGH; $\overline{MUTT}$ = LOW; $\overline{MUTR}$ = HIGH; AUXC = HIGH;	60	80	–	dB
Automatic Gain Control (pin AGC)						
$\Delta G_{v(trx)}$	gain control range for transmit and receive amplifiers affected by the AGC; with respect to I_{line} = 15 mA	I_{line} = 70 mA $G_{v(MIC-LN)}$, $G_{v(IR-RECO)}$ and $G_{v(IR-AUXO)}$	tbf	6.2	tbf	dB
		I_{line} = 70 mA for other transmit and receive gains affected	tbf	6.65	tbf	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{start}	highest line current for maximum gain		–	23	–	mA
I_{stop}	lowest line current for maximum gain		–	57	–	mA
Logic inputs (pins HFC, AUXC, $\overline{MUTT}$, $\overline{MUTR}$)						
V_{IL}	low level input voltage		GND–0.4	–	GND+0.3	V
V_{IH}	high level input voltage		GND+1.8	–	V_{BB}+0.4	V
I	input current					
	for pins HFC and AUXC		–	3	6	µA
	for pins $\overline{MUTT}$ and $\overline{MUTR}$		–	–2.5	–6	µA
Handsfree						
HF MICROPHONE AMPLIFIER (PINS TXIN, TXOUT AND GATX) NOTE 1						
$G_{v(TXIN-TXOUT)}$	voltage gain from pin TXIN to TXOUT	V_{TXIN} = 8 mV (RMS); R_{GATX} = 30.1 kΩ	tbf	15.2	tbf	dB
ΔG_v	voltage gain adjustment with R_{GATX}		–15	–	+16	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.1	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.15	–	dB
$V_{no(TXOUT)(rms)}$	noise output voltage at pin TXOUT; pin TXIN is shorted through 200 Ω in series with 10 µF to GNDTX (RMS value)	psophometrically weighted (p53 curve)	–	–101	–	dBmp
$\Delta G_{v(m)}$	gain reduction if not activated	HFC =HIGH; $\overline{MUTT}$ = LOW; $\overline{MUTR}$ = LOW; AUXC = LOW;	60	80	–	dB
HF LOUDSPEAKER AMPLIFIER (PINS HFRX, LSAO, GALS AND VOL) NOTE 1						
$G_{v(HFRX-LSAO)}$	voltage gain from pin HFRX to LSAO	V_{HFRX} = 30 mV (RMS); R_{GALS} = 255 kΩ; I_{line} = 70 mA	tbf	27.8	tbf	dB
ΔG_v	voltage gain adjustment with R_{GALS}		–28	–	+7	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.3	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = –25 to +75°C	–	±0.3	–	dB
$\Delta G_{v(vol)}$	voltage gain variation related to ΔR_{VOL} = 1.9 kΩ	when total attenuation does not exceed the switching range	–	–3	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{HFRX(rms)}$	maximum input voltage at pin HFRX (RMS value)	I_{line} = 70 mA R_{GALS} = 33 kΩ; for 2% THD in the input stage	450	580	–	mV
$V_{no(LSAO)(rms)}$	noise output voltage at pin LSAO; pin HFRX is open circuit (RMS value)	psophometrically weighted (p53 curve)	–	–79	–	dBVp
$V_{LSAO(rms)}$	output voltage (RMS value)	I_{BB} = 0 mA; I_{DD} = 1 mA				
		I_{line} = 18 mA	–	0.9	–	V
		I_{line} = 30 mA	–	1.2	–	V
		I_{line} > 50 mA	–	1.6	–	V
$I_{LSAO(max)}$	maximum output current at pin LSAO (peak value)		150	300	–	mA
$\Delta G_{v(m)}$	gain reduction if not activated	HFC =HIGH; $\overline{MUTT}$ = HIGH; $\overline{MUTR}$ = HIGH; AUXC = HIGH;	60	80	–	dB
DYNAMIC LIMITER (PINS LSAO AND DLC)						
t_{att}	attack time	when V_{HFRX} jumps from 20 mV to 20 mV + 10 dB	–	–	5	ms
		when V_{BB} jumps below $V_{BB(th)}$	–	1	–	ms
t_{rel}	release time	when V_{HFRX} jumps from 20 mV + 10 dB to 20 mV	–	100	–	ms
THD	Total Harmonic Distortion at V_{HFRX} = 20 mV + 10 dB	$t > t_{att}$	–	0.1	2	%
$V_{BB(th)}$	V_{BB} limiter threshold		–	2.7	–	V
MUTE LOUDSPEAKER (PIN DLC)						
$V_{DLC(th)}$	threshold voltage required on pin DLC to obtain mute receive condition		GND–0.4	–	GND+0.2	V
$I_{DLC(th)}$	threshold current sourced by pin DLC in mute receive condition	V_{DLC} = 0.2 V	–	100	–	µA
$\Delta G_{vrx(m)}$	voltage gain reduction in mute receive condition	V_{DLC} = 0.2 V	60	80	–	dB
RX AMPLIFIER USING HFRX (PINS HFRX AND AUXO) NOTE 1						
$G_{v(HFRX-AUXO)}$	voltage gain from pin HFRX to AUXO	V_{HFRX} = 0.25 V (RMS)	tbf	3.7	tbf	dB
$\Delta G_{v(f)}$	gain variation with frequency referred to 1 kHz	f = 300 to 3400 Hz	–	±0.1	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta G_{v(T)}$	gain variation with temperature referred to 25°C	T_{amb} = −25 to +75°C	–	±0.4	–	dB
$V_{HFRX(rms)}$	maximum input voltage at pin HFRX (RMS value)	I_{line} = 70 mA; for 2% THD in the input stage	450	580	–	mV
$V_{no(AUXO)(rms)}$	noise output voltage at pin AUXO; pin HFRX is an open circuit (RMS value)	psophometrically weighted (p53 curve)	–	−100	–	dBVp
$\Delta G_{v(m)}$	gain reduction if not activated	HFC =LOW; $\overline{MUTT}$ = LOW; $\overline{MUTR}$ = HIGH; AUXC = LOW	60	80	–	dB
TX AND RX ENVELOPE AND NOISE DETECTORS (PINS TSEN, TENV, TNOI, RSEN, RENV AND RNOI)						
Preamplifiers						
$G_{v(TSEN)}$	voltage gain from pin TXIN to TSEN		–	40	–	dB
$G_{v(RSEN)}$	voltage gain from pin HFRX to RSEN		–	0	–	dB
Logarithmic compressor and sensitivity adjustment						
$\Delta V_{det(TSEN)}$	sensitivity detection on pin TSEN; voltage change on pin TENV when doubling the current from TSEN	I_{TSEN} = 0.8 to 160 µA	–	18	–	mV
$\Delta V_{det(RSEN)}$	sensitivity detection on pin RSEN; voltage change on pin RENV when doubling the current from RSEN	I_{RSEN} = 0.8 to 160 µA	–	18	–	mV
Signal envelope detectors						
$I_{source(ENV)}$	maximum current sourced from pin TENV or RENV		–	120	–	µA
$I_{sink(ENV)}$	maximum current sunk by pin TENV or RENV		−1.25	−1	−0.75	µA
ΔV_{ENV}	voltage difference between pins RENV and TENV	note 2; when 10 µA is sourced from both RSEN and TSEN; signal detectors tracking	–	±3	–	mV
Noise envelope detectors						
$I_{source(NOI)}$	maximum current sourced from pin TNOI or RNOI		0.75	1	1.25	µA
$I_{sink(NOI)}$	maximum current sinked by pin TNOI or RNOI	dial tone detector or tx level limiter not activated	–	−120	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔV_{NOI}	voltage difference between pins RNOI and TNOI	note 2note ; when 5 µA is sourced from both RSEN and TSEN; noise detectors tracking	–	±3	–	mV
DIAL TONE DETECTOR						
$V_{HFRX(th)(rms)}$	threshold level at pin HFRX (RMS value)	R_{RSEN} = 10 kΩ	–	25	–	mV
TX LEVEL LIMITER						
$V_{TXIN(th)(rms)}$	threshold level at pin TXIN(RMS value)	R_{TSEN} = 10 kΩ	–	0.75	–	mV
DECISION LOGIC (PINS IDT AND SWT)						
Signal recognition						
$\Delta V_{Srx(th)}$	threshold voltage between pins RENV and RNOI to switch-over from receive to idle mode	note 3; $V_{HFRX} < V_{HFRX(th)}$	–	13	–	mV
$\Delta V_{Stx(th)}$	threshold voltage between pins TENV and TNOI to switch-over from transmit to idle mode	note 3; $V_{TXIN} < V_{TXIN(th)}$	–	13	–	mV
Switch-over						
$I_{source(SWT)}$	current sourced from pin SWT when switching to receive mode		7.5	10	12.5	µA
$I_{sink(SWT)}$	current sunk by pin SWT when switching to transmit mode		–12.5	–10	–7.5	µA
$I_{idle(SWT)}$	current sourced from pin SWT in idle mode		–	0	–	µA
VOICE SWITCH (PINS STAB AND SWR)						
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referred to 365 kΩ	–40	–	+12	dB
$\lvert\Delta G_v\rvert$	voltage gain variation from transmit or receive mode to idle mode		–	20	–	dB
G_{tr}	gain tracking ($G_{vtx} + G_{vrx}$) during switching, referred to idle mode		–	0.5	–	dB

Notes

1. when the channel is enabled according to Table 2
2. corresponds to ±1 dB tracking
3. corresponds to 4.3 dB noise/speech recognition level

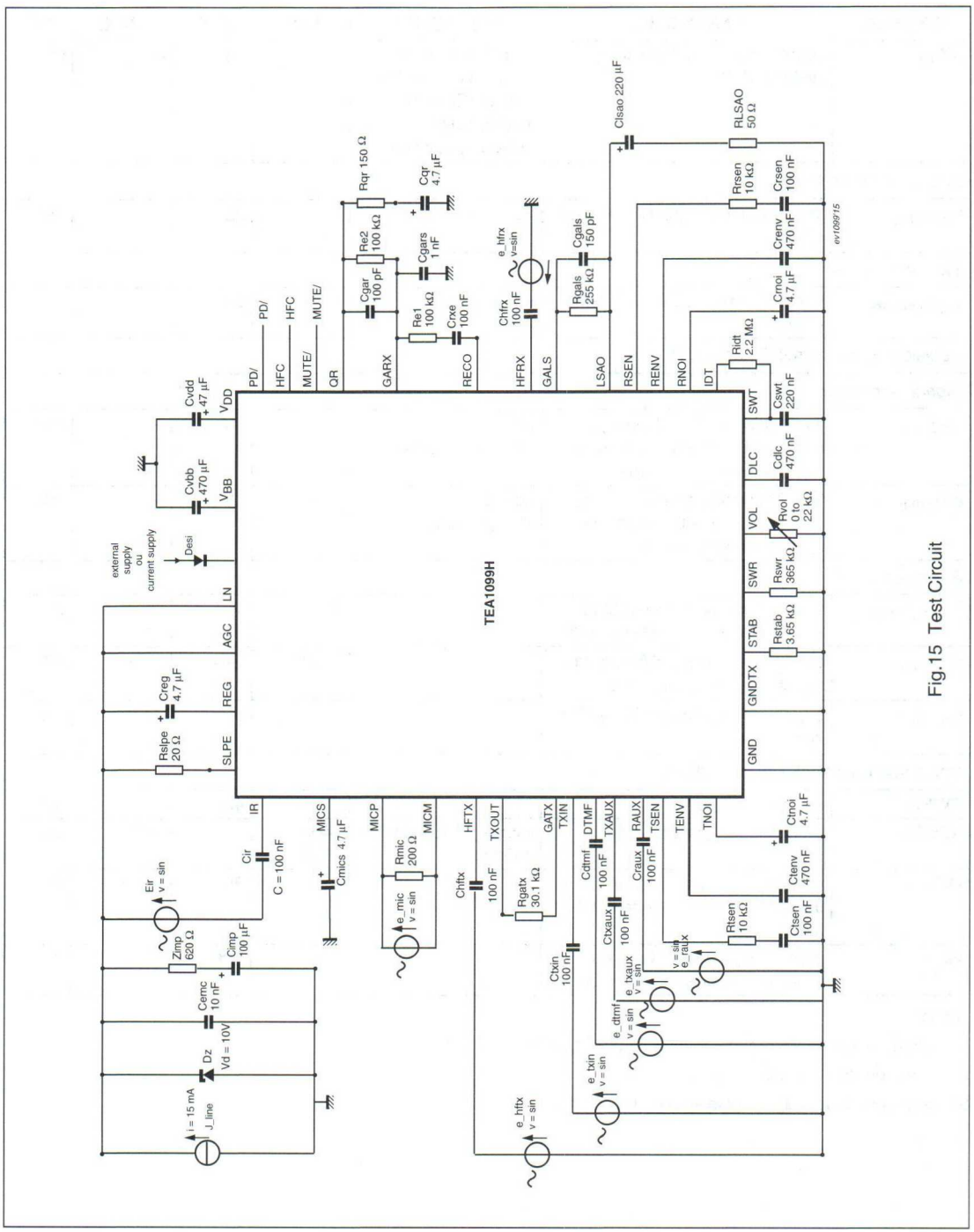


Fig.15 Test Circuit

APPLICATION INFORMATION

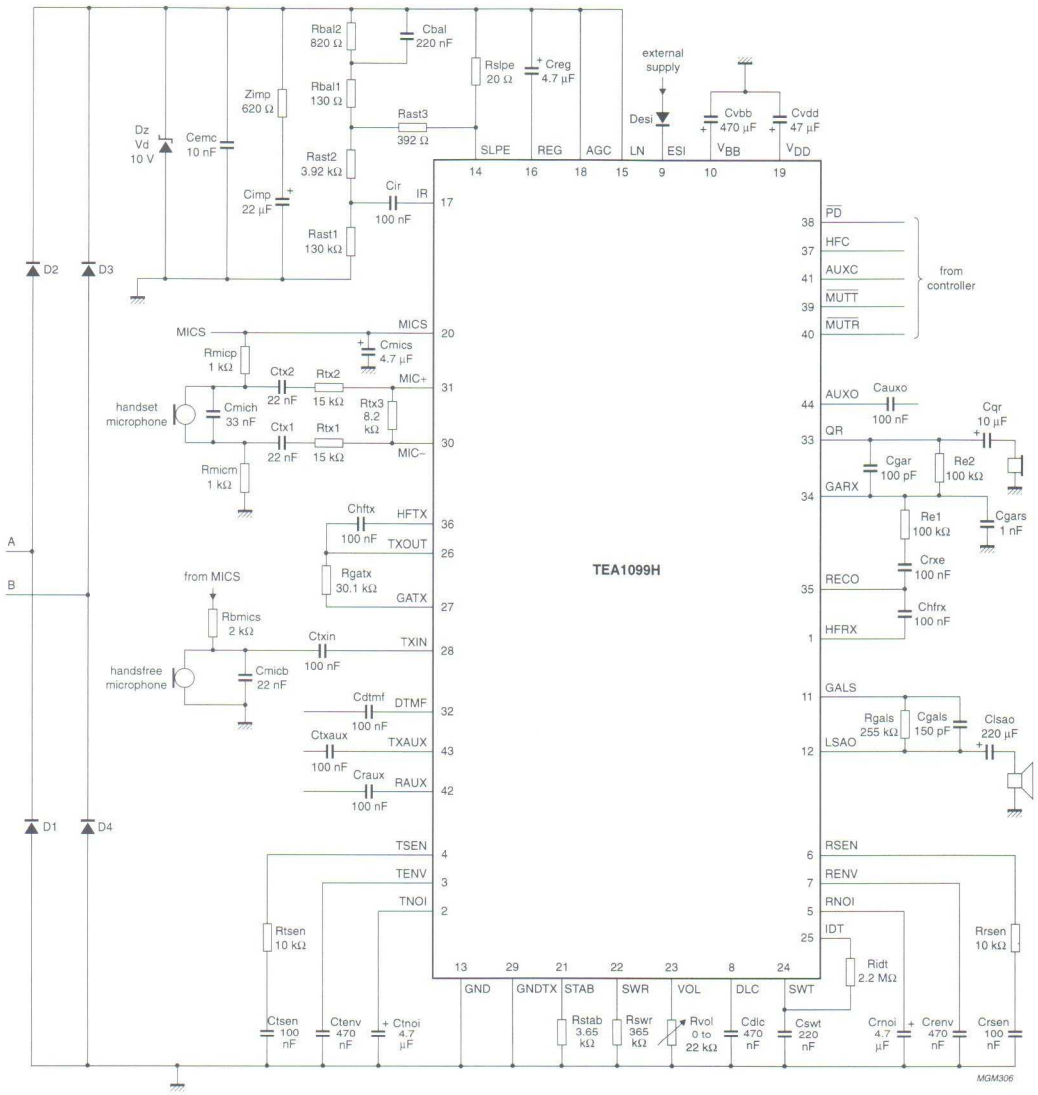


Fig.16 Basic application diagram

SINGLE-CHIP

Versatile speech/dialler/ringer with music-on-hold

TEA1069; TEA1069A

FEATURES

Speech part

- Voltage regulator with adjustable static resistance
- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Supply for dialler part and peripherals (not stabilized)
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic, or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- Asymmetrical earpiece output for dynamic, magnetic, or piezoelectric earpieces
- Internal mute to disable speech during dialling
- Confidence tone during DTMF dialling
- Line-loss compensation (line-current dependent) for microphone and earpiece amplifiers
- Gain-control curve adaptable to the exchange supply.

Dialler part

- Pulse/DTMF and mixed mode dialling
- Last Number Redial (LNR), up to 32 digits
- 13 repertory numbers (3 direct and 10 indirect) or 10 repertory numbers (10 direct), up to 32 digits, with a maximum of 224 digits in total
- Repertory and redial memory integrity check (memory contents check)
- Notepad memory function
- Flash and earth register recall
- Dial mode output
- Access pause generation and termination
- Function keys for: store, memory recall, register recall, LNR, pause, hold, mute, hook
- Keytone generation
- Hands-free control
- Volume control in hands-free mode (VOL+/VOL−)
- Hold function
- Mute function
- Music-on-hold
- Diode options:
  - DTMF tone burst/pause time
  - make/break ratio
  - access pause time
  - pulse or DTMF mode selection
  - register recall (earth and flash times)
  - keyboard layout selection
  - selection for german requirements
  - hold/mute mode selection.

Ringer part

- Ringer input frequency discrimination
- Ringer melody generation (3-tone)
- Ringer melody selection/volume control via keyboard
- Diode option: ringer frequency selection.

GENERAL DESCRIPTION

The TEA1069 and TEA1069A contain all the functions needed to build a highly featured, high-performance fully electronic telephone set.

The device incorporates a speech/transmission part, a dialler part and a ringer part. By offering a wide range of possible adaptations for each part, the TEA1069 and TEA1069A application can be easily adapted to meet different requirements.

The TEA1069A offers some different timings and diode options compared to the TEA1069.

Where pin numbers are mentioned in this data sheet we refer to the TEA1069N, unless otherwise indicated.

Speech part

The speech/transmission part performs all speech and line interface functions required in electronic sets. It operates at line voltages down to 1.6 V DC to facilitate the use of more telephones connected in parallel.

Dialler part

The dialler part offers a 32-digit Last Number Redial (LNR) and 13 memories. Hands-free control is included allowing the TEA1069 and TEA1069A to be used not only in basic telephones, but also in feature phones offering hands-free dialling via the TEA1083 call-progress monitor IC and/or full hands-free operation via the TEA1093 hands-free IC. The hold function allows the user to suspend the conversation and resume the call either on the same phone or on a parallel phone. Additionally through the music-on-hold function a melody is transmitted while the set is put on hold. The keytones provide in a buzzer an audible feedback of a valid key pressed.

Ringer part

The ringer part offers a discriminator input which enables the tone output as soon as a valid ring frequency is detected. It offers a melody based on 3 tones with programmable melody and volume via keyboard.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1069N	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1
TEA1069H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2
TEA1069AH	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

BLOCK DIAGRAM

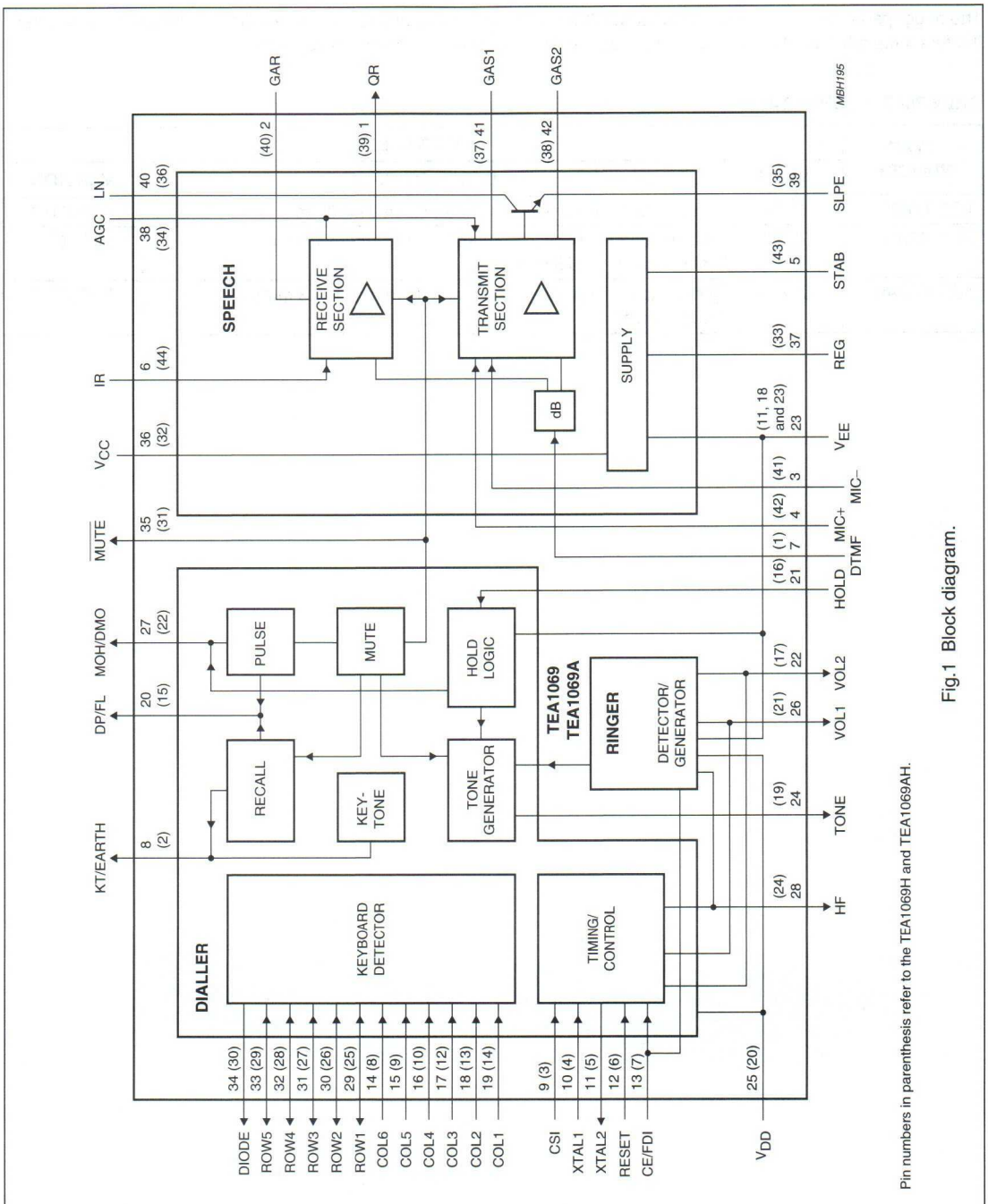


Fig.1 Block diagram.

Pin numbers in parenthesis refer to the TEA1069H and TEA1069AH.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT270-1	SOT307-2	
QR	1	39	receiving amplifier output
GAR	2	40	gain adjustment; receiving amplifier
MIC–	3	41	inverting microphone input
MIC+	4	42	non-inverting microphone input
STAB	5	43	current stabilizer
IR	6	44	receiving amplifier input
DTMF	7	1	dual-tone multi-frequency input
KT/EARTH	8	2	keytone/earth recall output
CSI	9	3	cradle switch input
XTAL1	10	4	oscillator input
XTAL2	11	5	oscillator output
RESET	12	6	reset input
CE/FDI	13	7	chip enable/frequency discrimination input
COL6	14	8	keyboard column input 6
COL5	15	9	keyboard column input 5
COL4	16	10	keyboard column input 4
COL3	17	12	keyboard column input 3
COL2	18	13	keyboard column input 2
COL1	19	14	keyboard column input 1
DP/FL	20	15	dial pulse/flash output
HOLD	21	16	hold control input
VOL2	22	17	volume 2 output
V_{EE}	23	11, 18, 23	negative line terminal
TONE	24	19	tone generator output
V_{DD}	25	20	dialler/ringer part supply voltage
VOL1	26	21	volume 1 output
MOH/DMO	27	22	music on hold/dial mode output
HF	28	24	hands-free control output
ROW1	29	25	keyboard row input/output 1
ROW2	30	26	keyboard row input/output 2
ROW3	31	27	keyboard row input/output 3
ROW4	32	28	keyboard row input/output 4
ROW5	33	29	keyboard row input/output 5
DIODE	34	30	diode option output
$\overline{MUTE}$	35	31	mute output, active LOW
V_{CC}	36	32	speech part supply voltage
REG	37	33	(DC) line voltage regulator decoupling
AGC	38	34	automatic gain control input

SYMBOL	PIN		DESCRIPTION
	SOT270-1	SOT307-2	
SLPE	39	35	slope (DC resistance) adjustment
LN	40	36	positive line terminal
GAS1	41	37	gain adjustment; transmitting amplifier
GAS2	42	38	gain adjustment; transmitting amplifier

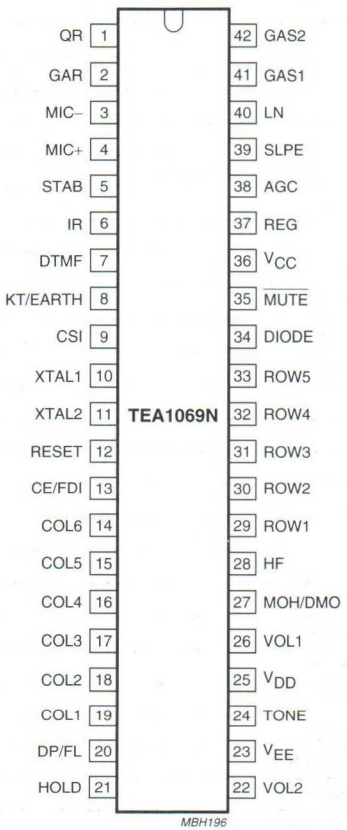


Fig.2 Pin configuration (SOT270-1).

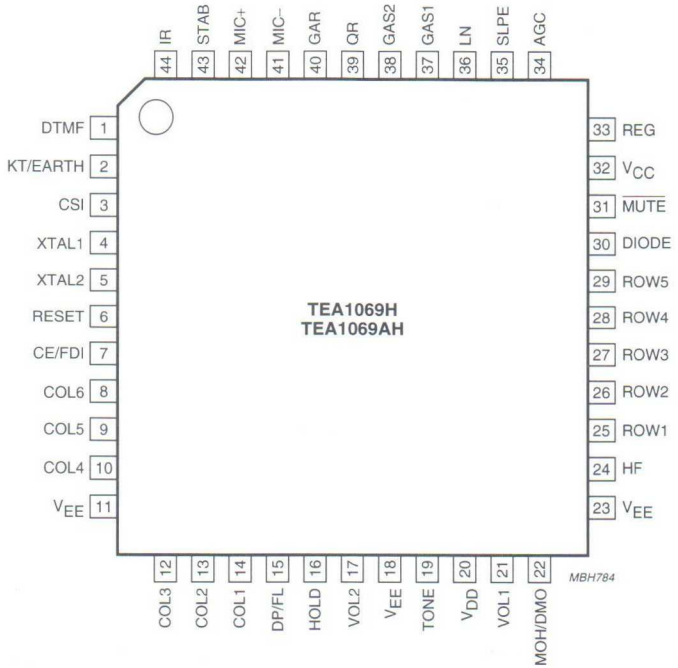


Fig.3 Pin configuration (SOT307-2).

FUNCTIONAL DESCRIPTION

Speech part

For numbering of components refer to Figs 28 and 29.

SUPPLIES V_{CC}, LN, SLPE, REG AND STAB

Power for the IC and its peripheral circuits is usually obtained from the telephone line (see Fig.4).

The circuit creates a stabilized voltage (V_{ref} = 3.7 V) between LN and SLPE. This reference voltage is temperature compensated and can be adjusted by means of an external resistor R_{VA}. It can be increased by connecting an R_{VA} resistor (R60) between REG and SLPE or decreased by connecting an R_{VA} resistor (R61) between REG and LN. This internal voltage reference is decoupled by capacitor C3 between REG and V_{EE}.

This decoupling capacitor realises the set impedance conversion from its DC value to its AC value in the audio frequency range.

The internal transmission part of the circuitry (including the earpiece amplifier) is supplied from V_{CC}. This voltage supply is derived from the LN voltage via a dropping resistor (R1) and must be decoupled by a capacitor (C1) between V_{CC} and V_{EE}. This supply point may also be used to supply the dialler/ringer (V_{DD}) part or external circuit e.g. electret microphone.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch} and the DC resistance of the telephone line R_{line}. When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p), the excess current is shunted to SLPE via LN.

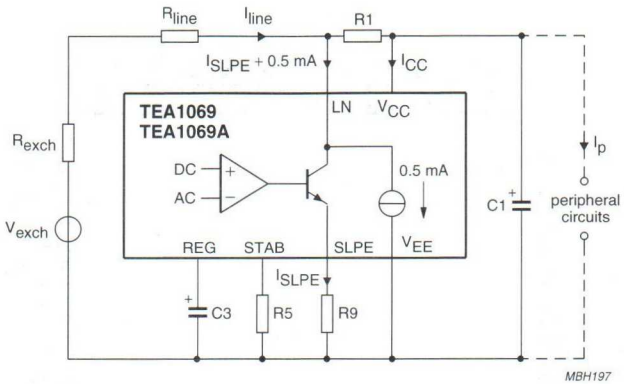


Fig.4 Supply arrangement.

Thus, the regulated voltage on the line terminal (V_{LN}) can be calculated as:

$V_{LN} = V_{ref} + I_{SLPE} \times R9$, where

$I_{SLPE} = I_{line} - \left(I_{CC} + I_p + 0.5 \times 10^{-3} A \right)$

V_{ref} is the internally generated temperature compensated reference voltage of 3.7 V and R9 is an external resistor connected between SLPE and V_{EE}.

The circuit has an internal current stabilizer operating at a level determined by resistor R5 connected between STAB and V_{EE}.

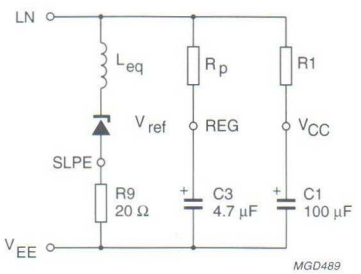
In normal use the value of R5 would be 3.6 kΩ and the value of R9 would be 20 Ω.

Changing the value of R5 or R9 will affect microphone gain, DTMF gain, gain control characteristics, sidetone level, maximum output swing on LN and the DC characteristics (especially at low line current).

At line currents below 9 mA the internal reference voltage is automatically adjusted to a lower value (typically 1.6 V at 1 mA). This means that more sets can be operated in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. At line currents below 9 mA the circuit has limited sending and receiving levels.

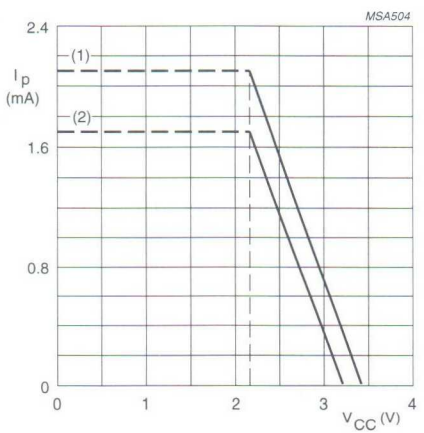
Under normal conditions, when $I_{SLPE} >> I_{CC} + 0.5$ mA + I_p, the static behaviour of the circuit is that of a 3.7 V regulator diode (V_{ref}) with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1. Figure 5 shows the equivalent impedance of the circuit.

Current (I_p) available from V_{CC} for the dialler part and peripheral circuits depends on the external components used. Figure 6 shows this current for $V_{CC} > 2.2$ V. When $\overline{\text{MUTE}}$ is HIGH i.e. when the receiving amplifier (supplied from V_{CC}) is driven, the available current is further reduced. Current availability can be increased by connecting the supply IC TEA1081 in parallel with R1, or by increasing the DC line voltage by means of an external resistor (R_{VA} = R60) connected between REG and SLPE.



$L_{eq} = C3 \times R9 \times R_p$.
$R_p = 16.2\ k\Omega$.

Fig.5 Equivalent impedance circuit.

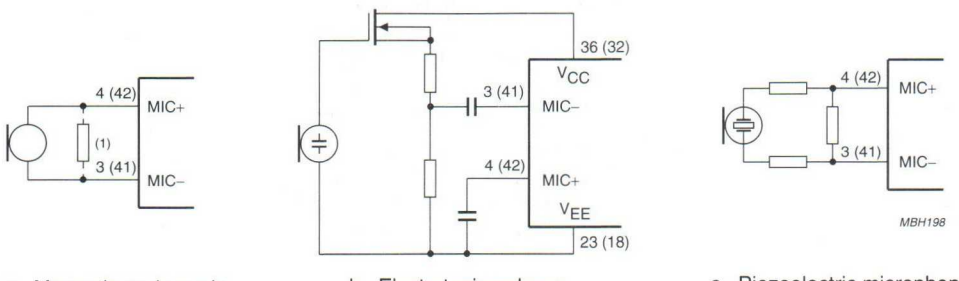


$V_{CC} > 2.2$ V; $I_{line} = 15$ mA at $V_{LN} = 4$ V; R1 = 620 Ω; R9 = 20 Ω.
(1) $I_p = 2.1$ mA. The curve is valid when the receiving amplifier is not driven or when $\overline{MUTE}$ = LOW.
(2) $I_p = 1.7$ mA. The curve is valid when $\overline{MUTE}$ = HIGH and the receiving amplifier is driven; $V_{o(rms)} = 150$ mV, $R_L = 150\ \Omega$.

Fig.6 Typical current I_P available from V_{CC} for peripheral circuitry.

MICROPHONE INPUTS MIC+ AND MIC– AND GAIN PINS GAS1 AND GAS2

The circuit has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 × 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) microphones can be used. Microphone arrangements are illustrated in Fig.7.



a. Magnetic or dynamic microphone.

b. Electret microphone.

c. Piezoelectric microphone.

Pin numbers in parenthesis refer to the TEA1069H and TEA1069AH.

(1) Resistor may be connected to reduce the terminating impedance.

Fig.7 Alternative microphone arrangements.

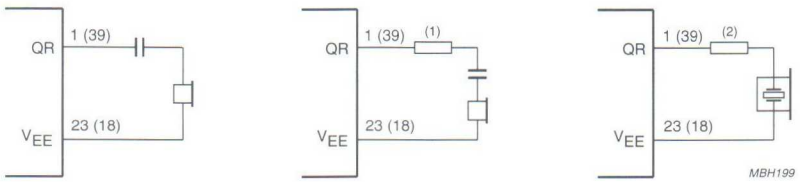
The gain of the microphone amplifier can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer in use. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2. Stability is ensured by two external capacitors, C6 connected between GAS1 and SLPE and C17 connected between GAS1 and V_{EE}. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The value of C17 is 10 times the value of C6. The cut-off frequency corresponds to the time constant R7 × C6.

RECEIVING AMPLIFIER IR, QR AND GAR

The receiving amplifier has one input (IR) and one output (QR). Earpiece arrangements are illustrated in Fig.8. The IR to QR gain is typically 31 dB (when R4 = 100 kΩ). It can be adjusted between 20 and 31 dB to match the sensitivity of the transducer in use.

The gain is set with the value of R4 which is connected between GAR and QR. The overall receive gain, between LN and QR, is calculated by subtracting the anti-sidetone network attenuation (32 dB) from the amplifier gain. Two external capacitors, C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 times the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 × C4.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.



a. Dynamic earpiece. b. Magnetic earpiece. c. Piezoelectric earpiece.

Pin numbers in parenthesis refer to the TEA1069H and TEA1069AH.
(1) Resistor may be connected to prevent distortion (inductive load).
(2) Resistor is required to increase the phase margin (capacitive load).

Fig.8 Alternative receiver arrangements.

Dual Tone Multi-Frequency input DTMF

When the DTMF input is enabled ($\overline{\text{MUTE}}$ is LOW) dialling tones may be sent on to the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The tones can be heard in the earpiece at a low level (confidence tone).

Automatic Gain Control input AGC

Automatic line loss compensation is achieved by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current.

The control range is 5.8 dB which corresponds to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and average attenuation of 1.2 dB/km. Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.9 and Table 1).
The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line-loss compensation is required the AGC pin may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

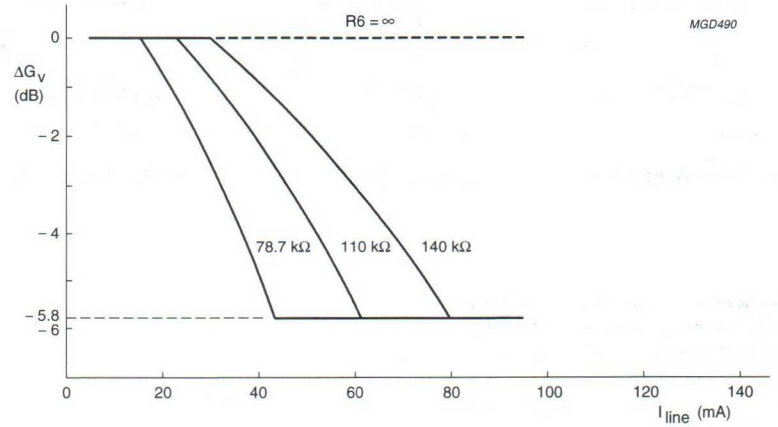


Fig.9 Variation of gain as function of line current with R6 as parameter.

Table 1 Values of resistor R6 for optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω

V_{exch} (V)	R6 (kΩ)			
	R_{exch} = 400 Ω	R_{exch} = 600 Ω	R_{exch} = 800 Ω	R_{exch} = 1000 Ω
36	100	78.7	–	–
48	140	110	93.1	82
60	–	–	120	102

SIDETONE SUPPRESSION

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising R1//Z_{line}, R2, R3, R8, R9 and Z_{bal} (see Fig.10). The maximum compensation is obtained when the following conditions are fulfilled:

$$R9 \times R2 = R1 \times (R3 + R8) \quad (1)$$

$$k = R3 \times \frac{(R8 + R9)}{(R2 \times R9)} \quad (2)$$

$$Z_{bal} = k \times Z_{line} \quad (3)$$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 series for Z_{line}. In practice, Z_{line} varies considerably with the line type and length. Therefore, the value chosen for Z_{bal} should be for an average line length thus giving optimum setting for short or long lines.

Example: the balance impedance Z_{bal} at which the optimum suppression is present can be calculated as follows:
suppose Z_{line} = 210 Ω + (1265 Ω//140 nF) representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).
When k = 0.64 then R8 = 390 Ω;
Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1069 and TEA1069A shown in Fig.10 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier.
The attenuation is almost constant over the whole audio-frequency range. Figure 11 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances. More information on the balancing of anti-sidetone bridges can be found in our publication *"Applications Handbook for Wired telecom systems, IC03b"*, order number 9397 750 00811.

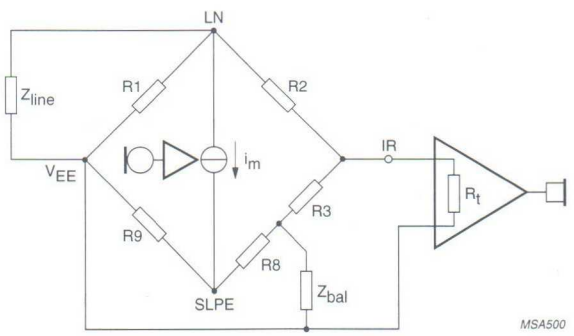


Fig.10 Equivalent circuit of TEA1069 and TEA1069A anti-sidetone bridge.

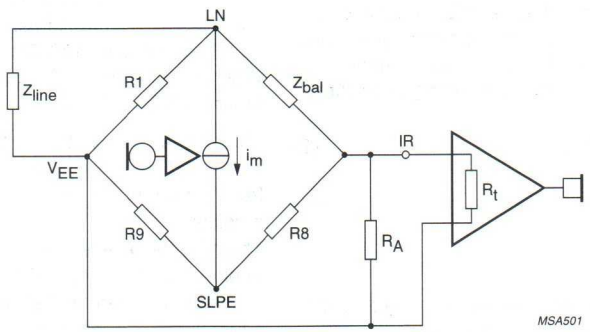


Fig.11 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

Dialler and ringer part

SUPPLY VOLTAGE: PINS V_{DD} AND V_{EE}

The power supply must be maintained for data storage. The RAM retention voltage (standby supply voltage) may drop down to 1.0 V. Applying a large capacitor across the supply terminals can retain the memory if power connections are broken. The minimum operation voltage is 2.5 V. The internal power-on reset is enabled for a voltage below this minimum operation voltage.

OSCILLATOR INPUT/OUTPUT: PINS XTAL1 AND XTAL2

Time base for the TEA1069 and TEA1069A is a crystal-controlled on-chip oscillator which is completed by connecting a 3.579545 MHz crystal or ceramic resonator between XTAL1 and XTAL2. The oscillator starts when V_{DD} reaches the operation voltage level and CE/FDI = HIGH. The following types of ceramic resonators are recommended:

- Kyocera PBRC3.58ARPC10 (wired)
- Kyocera KBR3.58MSATRPC10 (SMD)
- Murata CSA3.58MG310VA (wired).

RESET INPUT: PIN RESET

Pin RESET is an input to the internal reset circuit. When RESET = HIGH, it can be used to initialize the TEA1069 and TEA1069A which is normally done by the CE/FDI input. The on-chip power-on reset generates a reset pulse if V_{DD} drops below 2.5 V. In this event a proper start-up occurs after the supply voltage rises above the minimum operation voltage level again.
During and directly after reset pins 14 to 19, 21, 29 to 32, 34 and 35 are set HIGH; pins 8, 20, 22, 26 to 28 and 33 are set to LOW.

The RESET pin can be connected to V_{EE}, preferably via a resistor of 100 kΩ to 1 MΩ, which will save leakage current. A capacitor connected to V_{DD} can be used to extend the reset time, in case a longer reset is desirable.

To prevent the dialler from reacting on voltage disturbances on the telephone line a time-out is active. The dialler returns to standby state if the voltage on the line has disappeared for more than this reset-delay time (t_{rd}).

CHIP ENABLE/FREQUENCY DISCRIMINATOR INPUT: PIN CE/FDI

This active HIGH input is used to initialize part of the system, to select the on-line, standby, or ringer mode and to detect line power breaks. To keep the TEA1069 and TEA1069A in the on-line mode, CE/FDI has to be HIGH.

In the exchange, several AC signals can be superimposed on the DC signal, e.g. dialling tone, busy tone, disturbances (like line power breaks), and the ringer signal. The ringer signal is evaluated, and checked if its frequency is within the limits of the frequency interval as set by the diode option RFS. It is assumed that the ringer frequency at pin CE/FDI is the double of the frequency present on the telephone line.

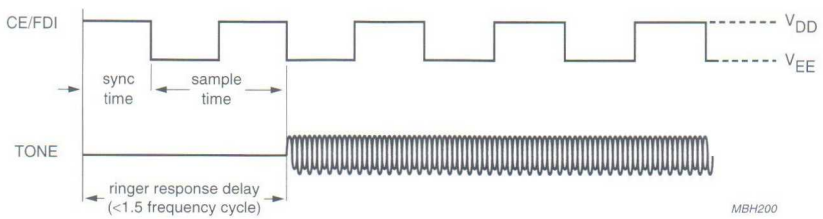


Fig.12 Ringer frequency detection.

In case of a valid ringer signal the user is alerted through a melody at the TONE output, generated by the ringer part of the TEA1069 and TEA1069A. This melody follows the cadence of the ringer signal. Both the melody and the volume can be selected. The melody frequency and duration are given in Table 2.

Table 2 Ringer melodies

NAME	FREQUENCY (Hz)	DURATION (ms)
Bell 1	800 + 1066 + 1333	28 + 28 + 28
Bell 2	826 + 925 + 1027	28 + 28 + 28
Bell 3	1037 + 1161 + 1297	28 + 28 + 28
Bell 4	1297 + 1455 + 1621	28 + 28 + 28

CRADLE SWITCH INPUT: PIN CSI

To distinguish among different operating states after CE/FDI is activated, input CSI is used. The basic states are shown in Table 3.

Table 3 TEA1069 and TEA1069A basic states

INPUT CSI	INPUT CE/FDI	STATE
LOW	LOW	standby
HIGH	LOW	not applicable
LOW	HIGH	ringer
HIGH	HIGH	on-line

For the hands-free state refer to Fig.23.

PULSE DIALLER: PINS DP/FL, MOH/DMO AND $\overline{\text{MUTE}}$

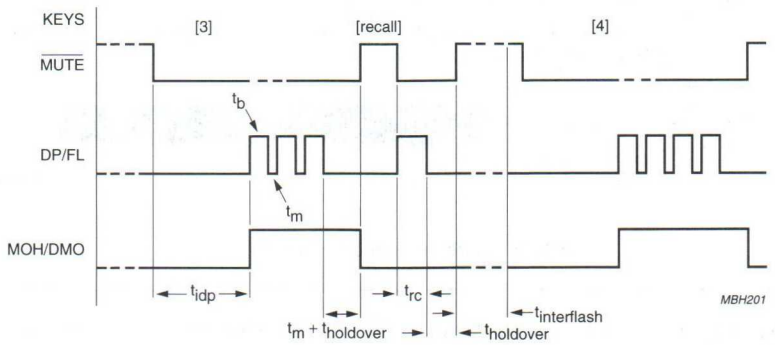
The pulse dialling system uses line current interruptions to signal the digits dialled to the exchange. The number of line current interruptions corresponds with the digit dialled except for the digit [0] which is characterized by 10 interruptions. Before each digit there is an inter-digit pause.

Valid keys are the digits [0] to [9] and [PAUSE].

The pulse dialling mode, the make/break ratio and the access pause time depend on the diode options: PTS, M/B, APT and APT2. DP/FL is LOW when V_{DD} is below power-on reset trip level and when RESET is HIGH.

The MOH/DMO pin (diode GOS = **on**) is used to reduce the voltage swing over the a/b terminals during pulse dialling. Several countries require this feature. The $\overline{\text{MUTE}}$ pin is an open drain output which requires a pull-up resistor. $\overline{\text{MUTE}}$ is HIGH when V_{DD} is below power-on reset trip level and when RESET is HIGH.

Figure 13 shows the timing diagram in pulse dialling mode when keys [3], [RECALL] and [4] are pressed.



t_b = break time.
t_m = make time.
t_{idp} = interdigit pause time.
t_{rc} = recall time.
$t_{holdover}$ = hold-over time.
$t_{interflash}$ = interflash hold-over time (only for TEA1069A).

Fig.13 Timing diagram in pulse dialling mode.

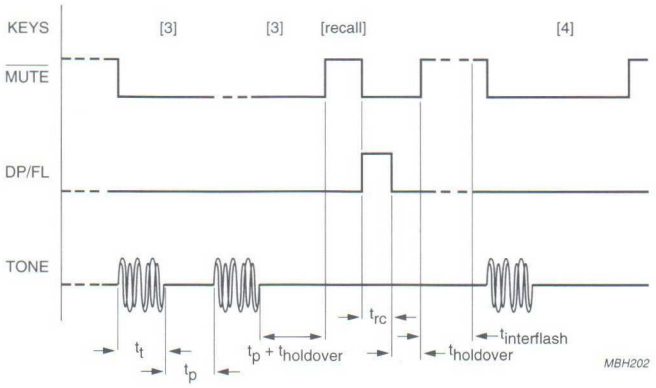
TONE DIALLER: PINS TONE AND $\overline{\text{MUTE}}$

In this system digits are transmitted as two tones simultaneously, the so called Dual-Tone Multi-Frequency (DTMF) system. Tone digits are separated by a pause time. Valid keys are the digits [0] to [9], [*], [#] and [PAUSE].

The DTMF dialling mode, the tone burst/pause times and the access pause time depend on the diode options: PTS, TBT, APT and APT2.

The $\overline{\text{MUTE}}$ pin is an open drain output which requires a pull-up resistor. $\overline{\text{MUTE}}$ is HIGH when V_{DD} is below power-on reset trip level and when RESET is HIGH.

Figure 14 shows the timing diagram in tone dialling mode when successively keys [3], [3], [RECALL] and [4] are dialled.



t_t = burst time.
t_p = pause time.
$t_{holdover}$ = hold-over time.
t_{rc} = recall time.
$t_{interflash}$ = interflash hold-over time (only for TEA1069A).

Note: in case of manual dialling only the minimum tone burst and pause time values depend on the chosen diode option, the maximum tone burst/pause times are equal to the real key press/release time.

Fig.14 Timing diagram in tone dialling mode.

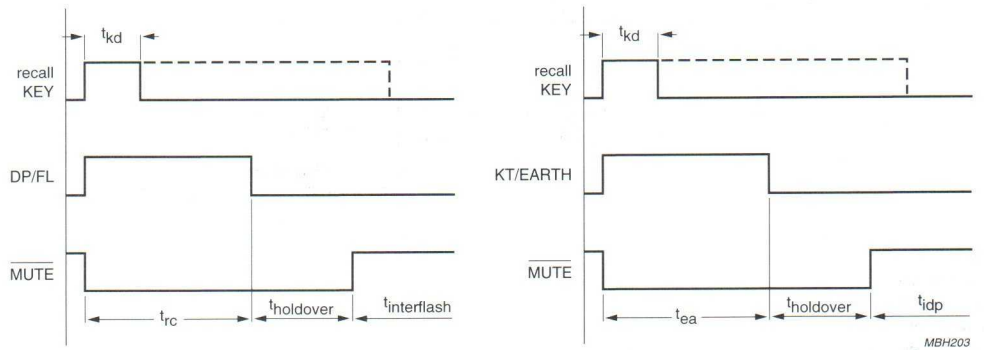
The DC-level at the TONE output measures $\frac{1}{2}V_{DD}$ and the impedance is typically 100 Ω. DTMF frequencies are composed by transmitting 2 tones simultaneously at pin TONE. The frequency tolerance for the tones at output TONE is shown in Table 4.

Table 4 DTMF frequency tolerances

DTMF FREQUENCY	FREQUENCY AT TONE	DEVIATION (%)	DEVIATION (Hz)
697	697.90	+0.13	+0.90
770	770.46	+0.06	+0.46
852	850.45	−0.18	−1.55
941	943.23	+0.24	+2.23
1209	1206.45	−0.21	−2.55
1336	1341.66	+0.42	+5.66
1477	1482.21	+0.35	+5.21

REGISTER RECALL: PINS DP/FL AND KT/EARTH

The RECALL function results in a calibrated pulse which drives the electronic line current interrupter via pin DP/FL or KT/EARTH. Flash or earth selection and various flash interruption times depend on the diode options: FES A and FES B (diode GOS = **on;** see Fig.15).



a. Recall using flash; t_{rc} = recall time using flash.

b. Recall using earth; t_{ea} = recall time using earth.

t_{kd} = key pressed time (depends on user).
$t_{holdover}$ = hold-over time.
t_{idp} = interdigit pause time.
$t_{interflash}$ = interflash hold-over time (only for TEA1069A).

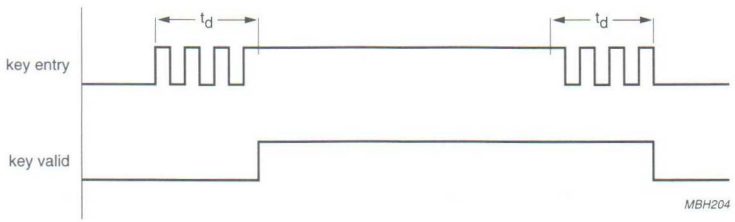
Fig.15 Recall mode timing diagram.

KEYBOARD: PINS ROW1 TO ROW5 AND COL1 TO COL6

The sense columns inputs and scanning rows outputs are directly connected to a single contact keyboard matrix. A second key entry will be valid after having released the first button and after having pressed the second button. Simultaneously pressing 2 buttons will disable the first entered key. A key entry becomes valid when the debounce time t_d has elapsed.

The column and row pins (except ROW5) are HIGH when V_{DD} is below power-on reset trip level and when RESET is HIGH.

ROW5 is an open-drain input/output; this configuration is used to avoid current flowing in the on-line or standby state. A pull-up resistor should be connected to ROW5. ROW5 is LOW when V_{DD} is below power-on reset trip level and when RESET is HIGH.



t_d = debounce time.

Fig.16 Timing diagram debouncing.

Keyboard layout

The TEA1069 and TEA1069A support three different keyboard layouts:

- With 10 direct accessible repertory numbers
- With 10 indirect accessible repertory numbers
- With 3 direct accessible repertory numbers and 10 indirect numbers.

For layouts see Figs 17 to 19; the keyboard layout can be selected by diode option KBS.

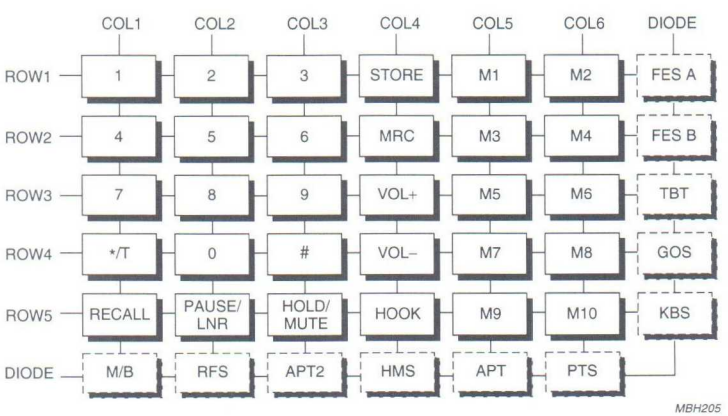


Fig.17 Keyboard and diodes with 10 direct accessible repertory numbers.

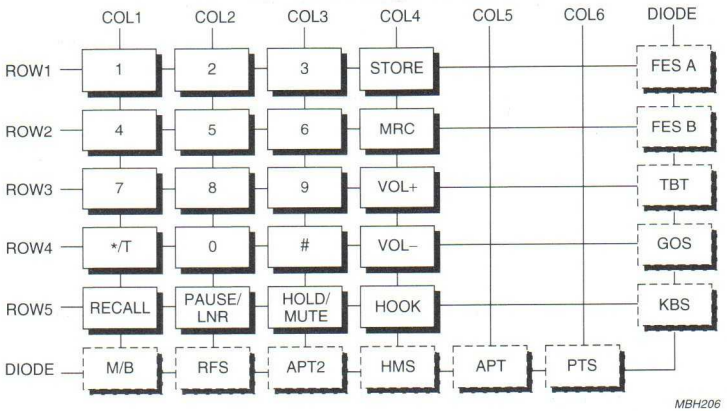


Fig.18 Keyboard and diodes with 10 indirect accessible repertory numbers.

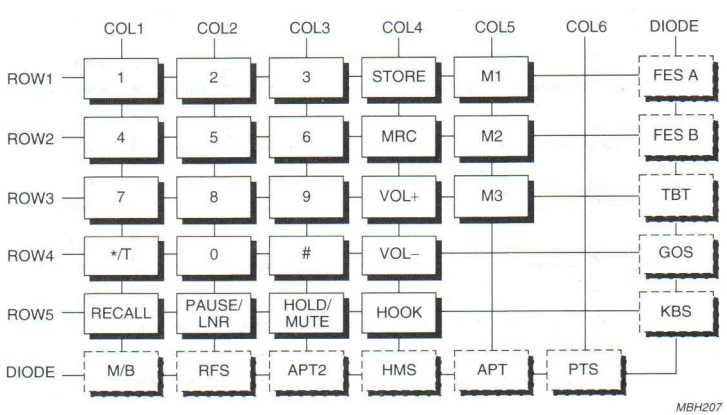


Fig.19 Keyboard and diodes with 3 direct and 10 indirect accessible repertory numbers.

DIODE OPTIONS: PIN DIODE

The DIODE pin is connected to the keyboard matrix as shown in Fig.20.

The diode options are read after each reset of the dialler.

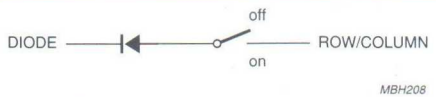


Fig.20 Diode connection.

Table 5 DIODE functions; TEA1069

DIODE	FUNCTION	CONDITION	ON[1]	OFF[1]
FES A	flash/earth time select	FES B = **off**	flash of 270 ms	flash of 100 ms
		FES B = **on**	earth of 400 ms	flash of 600 ms
TBT	tone burst/pause time		85/85 ms	100/100 ms
GOS	german output select		pin 8 = earth; pin 27 = DMO	pin 8 = keytone; pin 27 = MOH
KBS	keyboard select		keyboard layout; see Figs 17 and 18	keyboard layout; see Fig.19
PTS	pulse/tone selection		pulse mode	DTMF mode
APT	access pause time	APT2 = **off**	4 s	2 s
HMS	hold/mute select		hold mode	mute mode
RFS	ringer frequency select		29 to 146 Hz	40 to 120 Hz
M/B	make/break ratio		3 : 2	2 : 1

Note

1. **on** means option diode present; **off** means option diode not present.

Table 6 DIODE functions; TEA1069A

DIODE	FUNCTION	CONDITION	ON[1]	OFF[1]
FES A	flash/earth time select	FES B = **off**	flash of 270 ms	flash of 100 ms
		FES B = **on**	earth of 400 ms	flash of 600 ms
TBT	tone burst/pause time		85/85 ms	100/100 ms
GOS	german output select		pin 8 = earth; pin 27 = DMO	pin 8 = keytone; pin 27 = MOH
KBS	keyboard select		keyboard layout; see Fig.19	keyboard layout; see Figs 17 and 18
PTS	pulse/tone selection		pulse mode	DTMF mode
APT	access pause time	APT2 = **off**	4 s	1 s
		APT2 = **on**	3 s	2 s
HMS	hold/mute select		hold mode	mute mode
RFS	ringer frequency select		40 to 120 Hz	29 to 146 Hz
M/B	make/break ratio		3 : 2	2 : 1

Note

1. **on** means option diode present; **off** means option diode not present.

KEY TONE: PIN KT/EARTH

Every time a valid key is pressed a keytone is generated with a frequency of 606 Hz and a duration of 30 ms. This function is selected by the diode GOS = **off**. KT/EARTH is LOW when V_{DD} is below power-on reset trip level and when RESET is HIGH.

VOLUME CONTROL: PINS VOL1 AND VOL2

Both pins can control the volume of the ringer and/or the hands-free circuit. The state of VOL1/VOL2 is controlled by a state machine as depicted in Fig.24.

VOL1 and VOL2 are push-pull outputs. Both are set LOW when V_{DD} is below power-on reset trip level and when RESET is HIGH.

MUSIC-ON-HOLD: PIN MOH/DMO

When the dialler is in the hold state (see Fig.23) a melody is generated via pin TONE. In this state pin MOH/DMO can be used via diode GOS = **off** as an enable signal for the hardware to indicate that the tone should be switched to the telephone line.

MOH/DMO is a push-pull output. It is set LOW when V_{DD} is below power-on reset trip level and when RESET is HIGH.

HANDS-FREE: PIN HF

During the on-line state, the hands-free output pin HF is used for enabling the hands-free hardware. The pin will change state depending on specific key-sequences (see Fig.23).

HF is a push-pull output. It is set LOW when V_{DD} is below power-on reset trip level and when RESET is HIGH.

HOLD MODE: PIN HOLD

One way to terminate the hold state (see Fig.23) is a change in state of the signal at pin HOLD. This input should reflect the line current. If current is flowing the signal at pin HOLD should be HIGH, if not it should be LOW.

This pin is not debounced. The signal applied should be filtered by the hardware. HOLD is HIGH when V_{DD} is below power-on reset trip level and when RESET is HIGH.

Key sequences

The behaviour of the TEA1069 and TEA1069A can be modelled as a State Transition Diagram (STD) shown in Fig.21.

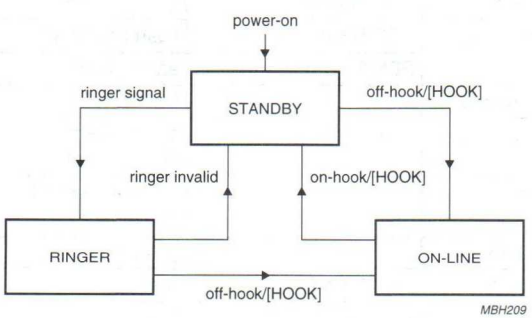


Fig.21 TEA1069 and TEA1069A dialler/ringer states.

The STD contains the states (rectangles in the figure) and state transitions (arrows) of the set. The upper arrow in the figure pointing to the standby state means that the set is initially in the standby state. When for instance an incoming call is detected, the set enters the ringer state, waiting for a reaction of the user. If the user answers the call on a handset, the set enters the on-line state.

The TEA1069 and TEA1069A have 3 basic states:

- Standby state
- Ringer state
- On-line state.

Each state with its own functional requirements is described in the following sections.

STANDBY STATE

In standby state the TEA1069 and TEA1069A are inactive. The current drawn is for memory retention and depends on the loads of the inputs/outputs of the dialler. In this state output DP/FL is HIGH so that the line is disconnected.

The ICs leave the standby state if:

- The set goes off-hook (lift handset or press [HOOK])
- A ringer-signal is available on the line.

The ICs go to the standby state if:

- The set goes on-hook (handset on the cradle or press [HOOK])
- A line-break occurs for at least the reset delay time (t_{rd})
- The ringer-signal becomes invalid.

RINGER STATE

If the set is in standby mode, a ringer signal can be received from the line. After evaluating the incoming ringer signal (and ringer signal is valid), the TEA1069 and TEA1069A start a melody via the TONE output ringer hardware, and stops this melody if the ringer signal is not valid any more. After going off-hook, the ringer signal stops and the set is in conversation (on-line) state.

During a ringer burst the ringer volume can be changed according to Fig.24 and melodies can be changed according to Table 7.

Table 7 Melody selection

MELODY	KEY
Bell 1	[1]
Bell 2	[2]
Bell 3	[3]
Bell 4	[4]

ON-LINE STATE

In this paragraph all the actions of the TEA1069 and TEA1069A during on-line state are described. The on-line mode starts with making output DP/FL LOW, which makes line current flow possible. The on-line state contains a number of sub-states (see Fig.22):

- Conversation state
- Dialling state
- Memory recall state
- Program state.

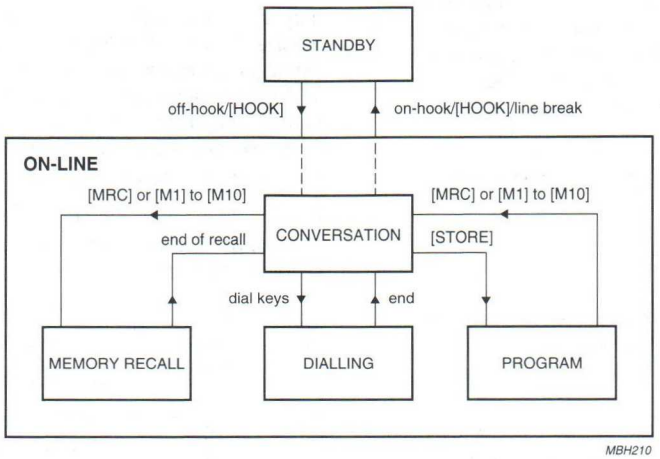


Fig.22 On-line states.

Conversation state

In this state conversation is possible. A number of sub-states (see Fig.23) exist:

- Handset state
- Hands-free state
- Hold state
- Mute state.

Depending on the diode option HMS the hold or the mute state is selected.

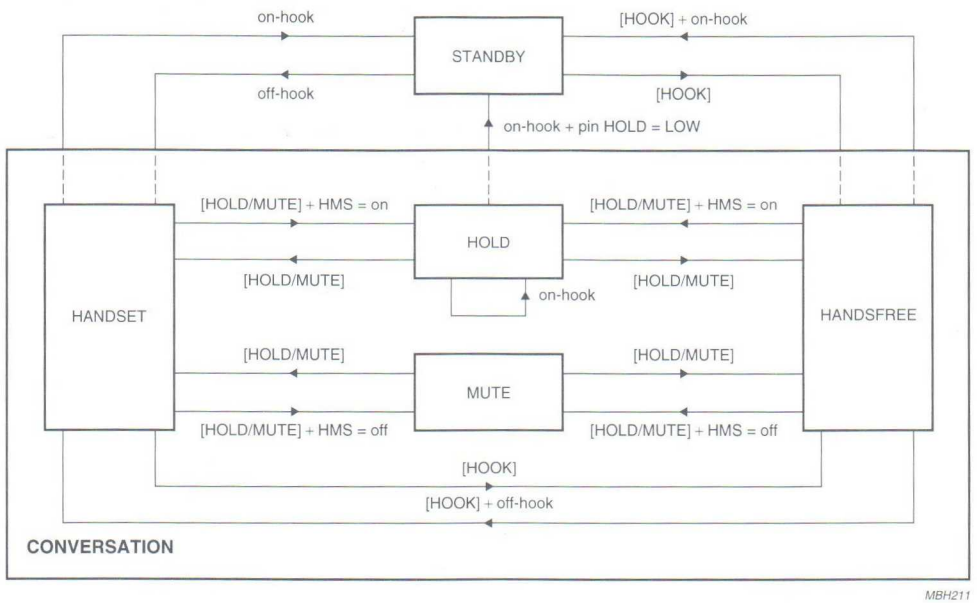


Fig.23 Conversation states.

- Handset state.

  The conversation states are shown in Fig.23.

- Hands-free state.

  In hands-free mode output HF becomes HIGH which activates a TEA1093/1094 hands-free IC. This state can be reached from standby state and from the handset state as follows:

  – the [HOOK] key is pressed during standby mode

  – the [HOOK] key is pressed during handset state is lifted, then when the handset is put on the cradle the set stays in the hands-free mode.

  The set leaves the hands-free mode and output HF becomes LOW when:

  – the [HOOK] key is pressed and the handset is on the cradle, the set goes to the standby mode

  – the [HOOK] key is pressed and the handset is lifted, the set goes to the handset state.

  The volume on the loudspeaker or buzzer, in hands-free and ringer mode, can be controlled in four levels using the [VOL+] and [VOL–] keys.

  The hands-free volume can be changed according to Fig.24.

- Hold state.

  The hold state is entered when the [HOLD/MUTE] key is pressed (diode HMS = **on**). This state can be entered either from handset state or from hands-free state. Upon entering this state outputs HF and $\overline{\text{MUTE}}$ become LOW.

  In hold state a music-on-hold melody is generated by output TONE. Pin MOH/DMO is HIGH (diode GOS = **off**) during this state. This signal can be used to adjust the volume of the TONE pin. Since $\overline{\text{MUTE}}$ is LOW the TONE output is transmitted to the telephone line. As long as the TEA1069 and TEA1069A are in this state the HOLD input pin is tested.

  The set leaves the hold state when:

  – [HOLD/MUTE] is pressed, the set returns to either the handset or hands-free state

  – the HOLD input becomes LOW, now the TEA1069 and TEA1069A return to the standby state.

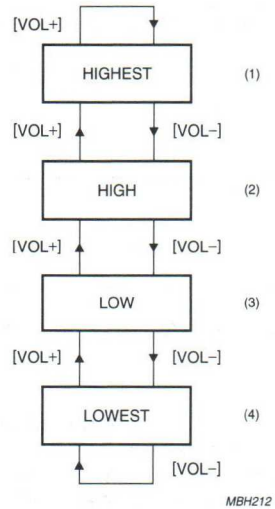
- Mute state.

  When the [HOLD/MUTE] key is pressed (HMS = **off**) the mute state is entered and $\overline{\text{MUTE}}$ becomes LOW.

  In mute state a music-on-hold melody is generated by output TONE. Pin MOH/DMO is HIGH (diode GOS = **off**) during this state.
  This signal can be used to adjust the volume of the TONE pin. Since $\overline{\text{MUTE}}$ is LOW the TONE output is transmitted to the telephone line. The mute state is left when:

  – [HOLD/MUTE] is pressed, set returns to either handset- or hands-free state

  – a dial action is started.



(1) VOL1 = HIGH, VOL2 = HIGH.
(2) VOL1 = LOW, VOL2 = HIGH.
(3) VOL1 = HIGH, VOL2 = LOW.
(4) VOL1 = LOW, VOL2 = LOW.

Fig.24 Volume control state machine.

Dialling state

During the dial-keys entries the TEA1069 and TEA1069A start immediately with transmission of the digit(s); the minimum transmission time is unaffected by the speed of the entry. Transmission continues as long as further dial-keys entries have to be processed.

However when keying-in is much faster then dialling-out, then the 32 digit dialling register will overflow. When this occurs the dialling is stopped and the error beep will be generated.

There are two dial modes: pulse dialling and tone dialling. The initial dialling mode is determined by option PTS. The state machine which controls the dial mode is shown in Fig.25.

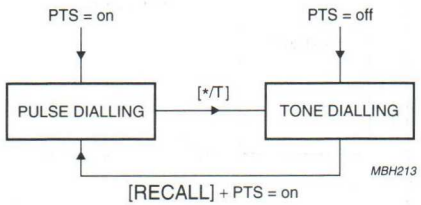


Fig.25 Dialling mode state machine.

- Pulse dialling.

  In this mode all valid keys are dialled by the pulse dialler. When during pulse dialling key [*/T] is pressed, the TEA1069 and TEA1069A switch over to tone dialling (mixed mode dialling). After the switch-over, valid keys are dialled by the tone dialler. The temporary tone mode is terminated by going on-hook or recall.

- Tone dialling.

  The ICs convert valid keys into data for the on-chip DTMF generator. Tones are transmitted via output TONE with minimum tone burst/pause duration.
  The maximum tone burst/pause duration is equal to the key pressing/release time.

- Register recall (flash/earth).

  The [RECALL] key will result in a flash or earth action.

- Access pause.

  When the [PAUSE/LNR] button is not the first key pressed, an access pause is entered for repertory or redialling procedures. When an access pause is executed $\overline{\text{MUTE}}$ is HIGH. During manual dialling no access pauses are dialled.

- Last Number Redial (LNR).

  If the first key pressed is the [PAUSE/LNR] button, the number stored in the redial register is recalled and transmitted. A maximum number of 32 digits can be

accepted for last number redial. If this maximum is reached the redial function is inhibited. During LNR programmed access pauses are also dialled.
The [RECALL] key and the (in pulse dialling mode allowed) tone switch key [*/T] are also stored in LNR memory.

- Notepad function.

  In conversation state it is possible to store a number into the LNR register, which may be dialled after an on-hook/off-hook action. The procedure is as follows:

  – press [STORE]
  – press to-be-stored sequence of the digits [0] to [9], [PAUSE/LNR], [*/T] or [RECALL]
  – press [STORE]
  – press [PAUSE/LNR].

Memory recall state

Repertory numbers can be dialled-out after or before entering manual dialling, last number redial and by entering the memory locations in successive order.

The stored numbers can be dialled by the following procedures:

- Press [MRC]
- Press one of the numeric keys [0] to [9], corresponding to the memory location

or

- Press one of the direct memory keys ([M1] to [M10]).

Program state

The program mode can be entered from the conversation (on-line) mode.

Pressing the [STORE] key in this state puts the TEA1069 and TEA1069A in the program mode. The program state can be left by going on-hook (by putting the handset on the cradle or pressing the [HOOK] key), the program mode is interrupted and nothing is stored, or by ending the store procedures resulting in a proper store of the programmed item.

- Programming repertory numbers.

  Storing of a new repertory number including access pauses, tone switch and register recall can be done by the following procedures:

  – press [STORE]
  – press to-be-stored sequence of the digits [0] to [9], [PAUSE/LNR], [*/T] or [RECALL]
  – press [MRC]
  – press one of the numeric keys [0] to [9], corresponding to the memory location

  or

  – press [STORE]
  – press to-be-stored sequence of the digits [0] to [9], [PAUSE/LNR], [*/T] or [RECALL]
  – press [M1] to [M10].

  For storing the redial number in repertory use:

  – press [STORE]
  – press [PAUSE/LNR]
  – press [MRC]
  – press one of the numeric keys [0] to [9], corresponding to the memory location

  or

  – press [STORE]
  – press [PAUSE/LNR]
  – press [M1] to [M10].

  If the keyboard described in Fig.17 is selected by the KBS diode option, repertory memory place [M1] = [MRC] + [1] to [M10] = [MRC] + [0], thus the set has 10 repertory numbers which can be selected via two different ways.

  If the keyboard described in Fig.19 is selected by the KBS diode option repertory memory place [MRC] + [0] to [MRC] + [9] and [M1], [M2] and [M3] are different repertory numbers, thus this set has in total 13 repertory numbers.

- Memory overflow.

  A maximum of 224 digits can be stored in the repertory memories. When the maximum is reached, no keytone is generated when trying to store more digits. The store procedure is cancelled automatically.

- Clear repertory number.

  Clearing a memory location is possible via the same procedure as for storing a number, except no telephone number is entered, thus one of the following sequences must be used:

  – press [STORE]
  – press [MRC]
  – press one of the numeric keys [0] to [9], corresponding to the memory location

  or

  – press [STORE]
  – press [M1] to [M10].

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{line}	line current	R9 = 20 Ω; note 1	–	140	mA
I_{EE}	ground supply current through V_{EE}		–	50	mA
P_{tot}	total power dissipation	R9 = 20 Ω; note 2			
	TEA1069N		–	770	mW
	TEA1069H and TEA1069AH		–	300	mW
T_{amb}	operating ambient temperature		–25	+70	°C
T_{stg}	IC storage temperature		–40	+125	°C
Speech part					
V_{LN}	positive continuous line voltage		–	12	V
$V_{LN(R)}$	repetitive line voltage during switch-on or line interruption		–	13.2	V
V_{CC}	input voltage on pin V_{CC}		–	12	V
V_i	input voltage on pins 1 to 7, 37, 38, 39, 41, 42		V_{EE} – 0.7	V_{CC} + 0.7	V
Dialler/ringer part					
V_{DD}	supply voltage		–0.7	+7	V
V_i	input voltages on pins 8 to 22, 24, 26 to 35		V_{EE} – 0.7	V_{DD} + 0.7	V
I_I	DC input current on pins 8 to 22, 24, 26 to 35		–10	+10	mA
I_O	DC output current on pins 8 to 22, 24, 26 to 35		–10	+10	mA
P_o	power dissipation per output on pins 8 to 22, 24, 26 to 35		–	30	mW

Notes

1. Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE (see Fig.26 for TEA1069N or Fig.27 for TEA1069H and TEA1069AH).
2. Calculated for the maximum specified ambient temperature (T_{amb} = 70 °C, see also Fig.26 for TEA1069N or Fig.27 for TEA1069H and TEA1069AH).

THERMAL CHARACTERISTICS

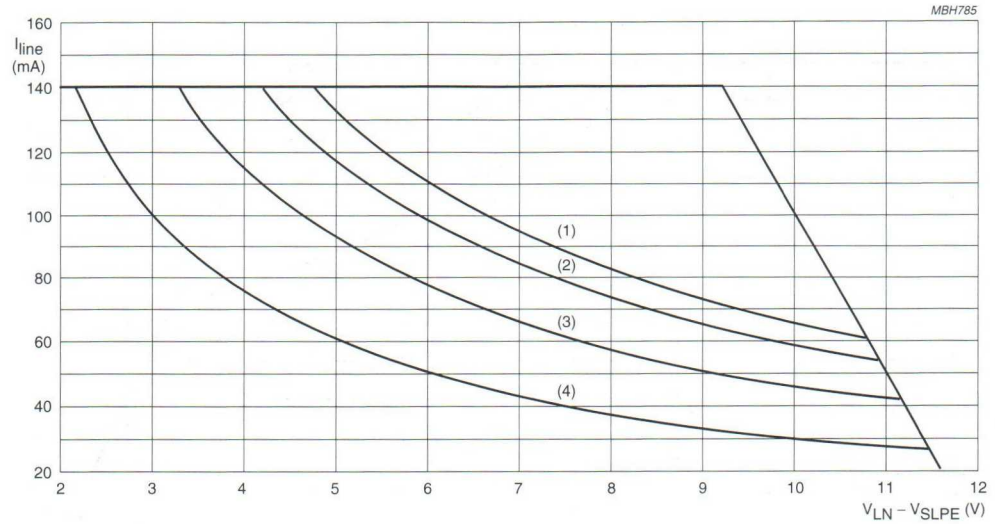
SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air mounted on glass epoxy board 28.5 × 19.1 × 1.5 mm		
	TEA1069N	63	K/W
	TEA1069H and TEA1069AH	116	K/W



(1) T_{amb} = 40 °C; P_{tot} = 1200 mW.
(2) T_{amb} = 50 °C; P_{tot} = 1050 mW.
(3) T_{amb} = 60 °C; P_{tot} = 910 mW.
(4) T_{amb} = 70 °C; P_{tot} = 770 mW.

Note: calculations based upon negligible dialler and ringer parts output power (null port sink current).

Fig.26 TEA1069N safe operating area.



(1) T_{amb} = 40 °C; P_{tot} = 665 mW.
(2) T_{amb} = 50 °C; P_{tot} = 590 mW.
(3) T_{amb} = 60 °C; P_{tot} = 460 mW.
(4) T_{amb} = 70 °C; P_{tot} = 300 mW.

Note: calculations based upon negligible dialler and ringer parts output power (null port sink current).

Fig.27 TEA1069H and TEA1069AH safe operating area.

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 1 kHz; V_{DD} = 3 V; f_{xtal} = 3.579545 MHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Speech part						
SUPPLIES LN AND V_{CC} (PINS 40 AND 36)						
V_{LN}	voltage drop over circuit between LN and V_{EE}	MIC inputs open-circuit				
		I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	1.9	–	V
		I_{line} = 15 mA	3.55	4.0	4.25	V
		I_{line} = 100 mA	4.9	5.7	6.5	V
		I_{line} = 140 mA	–	–	7.5	V
$\Delta V_{LN}/\Delta T$	variation with temperature	I_{line} = 15 mA	–	−0.3	–	mV/K
V_{LN}	voltage drop over circuit between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA				
		R_{VA} (LN to REG) = 68 kΩ	–	3.5	–	V
		R_{VA} (REG to SLPE) = 39 kΩ	–	4.5	–	V
I_{CC}	supply current	V_{CC} = 2.8 V	–	0.9	1.35	mA
V_{CC}	supply voltage available for peripheral circuitry	I_{line} = 15 mA; $\overline{MUTE}$ = LOW				
		I_p = 1.2 mA	2.2	2.7	–	V
		I_p = 0 mA	–	3.4	–	V
MICROPHONE INPUTS MIC– AND MIC+ (PINS 3 AND 4)						
$\|Z_i\|$	input impedance					
	differential	between MIC– and MIC+	–	64	–	kΩ
	single-ended	MIC– or MIC+ to V_{EE}	–	32	–	kΩ
CMRR	common mode rejection ratio		–	82	–	dB
G_v	voltage gain MIC+ or MIC– to LN	I_{line} = 15 mA; R7 = 68 kΩ	50.5	52.0	53.5	dB
$\Delta G_{v(f)}$	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referenced to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 to +70 °C	–	±0.2	–	dB
DTMF INPUT (PIN 7)						
$\|Z_i\|$	input impedance		–	20.7	–	kΩ
G_v	voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	24.0	25.5	27.0	dB
$\Delta G_{v(f)}$	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referenced to 25 °C	I_{line} = 50 mA; T_{amb} = −25 to +70 °C	–	±0.2	–	dB
GAIN ADJUSTMENT INPUTS GAS1 AND GAS2 (PINS 41 AND 42)						
ΔG_v	transmitting amplifier gain variation by adjustment of R7 between GAS1and GAS2		−8	–	0	dB

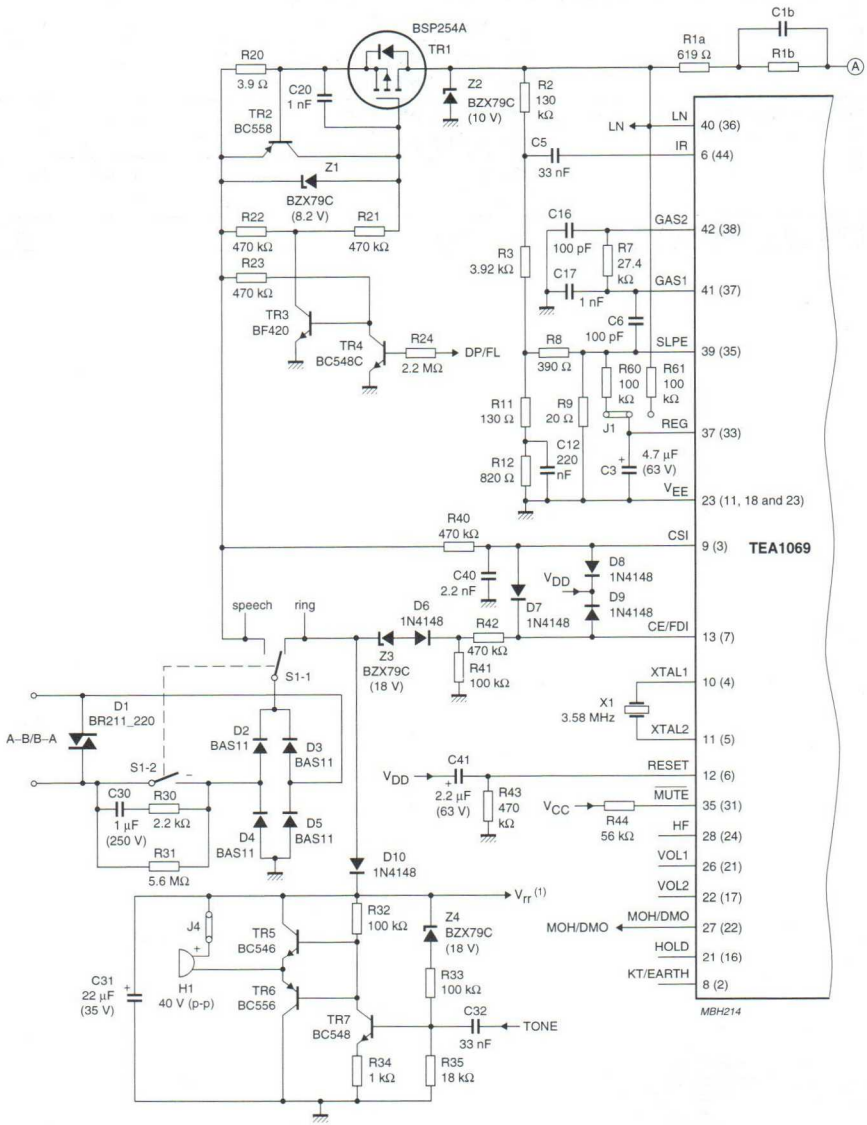
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SENDING AMPLIFIER OUTPUT LN (PIN 40)						
$V_{LN(rms)}$	output voltage (RMS value)	THD = 10%				
		I_{line} = 4 mA	–	0.8	–	V
		I_{line} = 15 mA	1.7	2.3	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	–	–69	–	dBmp
RECEIVING AMPLIFIER INPUT IR (PIN 6)						
$\|Z_i\|$	input impedance		–	21	–	kΩ
RECEIVING AMPLIFIER OUTPUT QR (PIN 1)						
$\|Z_o\|$	output impedance		–	4	–	Ω
G_v	voltage gain from IR to QR	I_{line} = 15 mA; R_L = 300 Ω (from pin 9 to pin 4)	29.5	31	32.5	dB
$\Delta G_{v(f)}$	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
$\Delta G_{v(T)}$	gain variation with temperature referenced to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 and +70 °C	–	±0.2	–	dB
$V_{o(rms)}$	output voltage (RMS value)	THD = 2%; sine wave drive; R4 = 100 kΩ; I_{line} = 15 mA; I_p = 0 mA				
		R_L = 150 Ω	0.22	0.33	–	V
		R_L = 450 Ω	0.3	0.48	–	V
		THD = 10%; R4 = 100 kΩ; R_L = 150 Ω; I_{line} = 4 mA	–	15	–	mV
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted (P53 curve); R_L = 300 Ω	–	50	–	μV
GAIN ADJUSTMENT INPUT GAR (PIN 2)						
ΔG_v	receiving amplifier gain variation by adjustment of R4 between GAR and QR		–11	–	0	dB
$\overline{\text{MUTE}}$ (PIN 35) GAIN REDUCTION						
ΔG_v	MIC+ or MIC– to LN	$\overline{\text{MUTE}}$ = LOW	–	70	–	dB
G_v	voltage gain from DTMF to QR	R4 = 100 kΩ; R_L = 300 Ω	–	–17	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AUTOMATIC GAIN CONTROL INPUT AGC (PIN 38)						
ΔG_v	gain control range (controlling the gain from IR to QR and the gain from MIC+, MIC– to LN)	R6 = 110 kΩ (between AGC and V_{EE}); I_{line} = 70 mA	–	–5.8	–	dB
I_{lineH}	highest line current for maximum gain	R6 = 110 kΩ	–	23	–	mA
I_{lineL}	lowest line current for minimum gain	R6 = 110 kΩ	–	61	–	mA
Dialler part						
V_{DD} (PIN 25)						
V_{DD}	supply voltage		2.5	–	6.0	V
$V_{DD(MR)}$	memory retention voltage		1.0	–	6.0	V
I_{DD}	supply current	DTMF generator **off**	–	0.3	0.6	mA
		DTMF generator **on**	–	0.9	1.8	mA
$I_{DD(MR)}$	memory retention current	standby state, V_{DD} = 1.8 V	–	1.2	–	µA
V_{POR}	power-on reset trip level		1.5	2.0	2.5	V
INPUTS/OUTPUTS (PINS 9, 12 TO 21, 29 TO 34)						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	input leakage	$V_{EE} < V_I < V_{DD}$	–1	–	+1	µA
I_{OL}	port sink current LOW	V_{DD} = 3 V; V_O = 0.4 V	0.7	8	–	mA
I_{OH}	port pull-up source current HIGH (not valid for pin 33)	V_{DD} = 3 V; V_O = 2.7 V	10	20	–	µA
		V_{DD} = 3 V; V_O = 0 V	–	100	300	µA
$\overline{MUTE}$ (PIN 35)						
I_{OL}	port sink current LOW	V_{DD} = 3 V; V_O = 0.4 V	0.7	8	–	mA
OUTPUTS (PINS 8, 22, 26 TO 28)						
I_{OL}	port sink current LOW	V_{DD} = 3 V; V_O = 0.4 V	0.7	8	–	mA
I_{OH}	port push-pull source current HIGH	V_{DD} = 3 V; V_O = 2.6 V	0.7	4	–	mA
OSCILLATOR (PINS 10 AND 11)						
g_m	transconductance		0.2	0.4	1.0	mA/V
R_f	feedback resistor		0.3	1.0	3.0	MΩ
CE/FDI (PIN 13)						
t_{rd}	reset delay time		–	280	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
KEYBOARD (PINS 14 TO 19 AND 29 TO 33)						
t_d	keyboard debounce time		–	20	–	ms
t_{ap}	access pause time					
	TEA1069	diodes APT **off**; APT2 **off**	–	2	–	s
		diodes APT **on**; APT2 **off**	–	4	–	s
	TEA1069A	diodes APT **off**; APT2 **off**	–	1	–	s
		diodes APT **on**; APT2 **off**	–	4	–	s
		diodes APT **off**; APT2 **on**	–	2	–	s
		diodes APT **on**; APT2 **on**	–	3	–	s
DP/FL OUTPUT (PIN 20)						
t_{idp}	interdigit pause time		–	840	–	ms
$t_{holdover}$	mute hold-over time		–	40	–	ms
$t_{interflash}$	interflash hold-over time	TEA1069	–	0	–	ms
		TEA1069A	–	960	–	ms
t_m	make time	diode M/B **off**	–	40	–	ms
		diode M/B **on**	–	33	–	ms
t_b	break time	diode M/B **off**	–	60	–	ms
		diode M/B **on**	–	66	–	ms
t_{rc}	recall time using flash	diode FES A **off**, FES B **off**	–	100	–	ms
		diode FES A **on**, FES B **off**	–	270	–	ms
		diode FES A **off**, FES B **on**	–	600	–	ms
t_{ea}	recall time using earth	diode FES A **on**, FES B **on**	–	400	–	ms
TONE OUTPUT (PIN 24)						
t_t	burst time	diode TBT **off**	–	100	–	ms
		diode TBT **on**	–	85	–	ms
t_p	pause time	diode TBT **off**	–	100	–	ms
		diode TBT **on**	–	85	–	ms
$\Delta f/f$	frequency deviation		−0.6		+0.6	%
$V_{HG(rms)}$	HGF voltage (RMS value)		158	181	205	mV
$V_{LG(rms)}$	LGF voltage (RMS value)		125	142	160	mV
V_{DC}	DC voltage level		–	$\frac{1}{2}V_{DD}$	–	V
$\lvert Z_o \rvert$	output impedance		–	100	500	Ω
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion		–	−25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ringer part						
f_{ringL}	ringer detection LOW frequency	diode RFS **off** (TEA1069); diode RFS **on** (TEA1069A)	–	40	–	Hz
		diode RFS **on** (TEA1069); diode RFS **off** (TEA1069A)	–	29	–	Hz
f_{ringH}	ringer detection HIGH frequency	diode RFS **off** (TEA1069); diode RFS **on** (TEA1069A)	–	120	–	Hz
		diode RFS **on** (TEA1069); diode RFS **off** (TEA1069A)	–	146	–	Hz
t_{rrd}	ringer response delay	<1.5 frequency cycle	–	–	150	ms

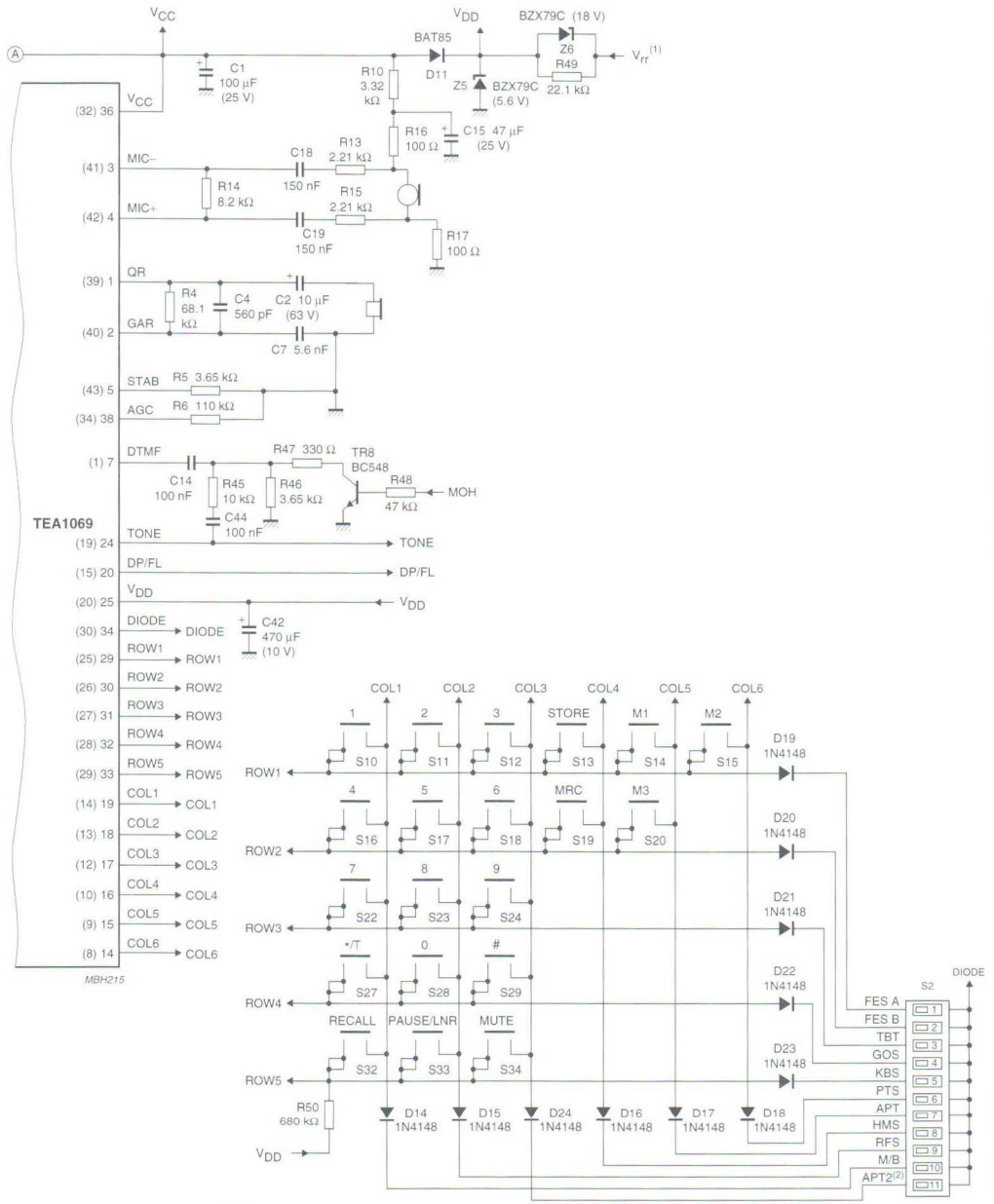
APPLICATION INFORMATION



Pin numbers in parenthesis refer to the TEA1069H and TEA1069AH.

(1) Ringer supply voltage.

Fig.28 Basic application diagram (continued in Fig.29).



Pin numbers in parenthesis refer to the TEA1069H and TEA1069AH.

(1) Ringer supply voltage.

(2) Only on TEA1069A.

Fig.29 Basic application diagram (continued from Fig.28).

DIALLERS AND DTMF GENERATORS

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1 FEATURES

- Pulse, DTMF and 'mixed mode' dialling
- Mixed mode dialling: start with pulse dial, end with DTMF dial (e.g. for control of DTMF user equipment via a pulse network)
- 23-digit memory stores last number dialled, or number noted during conversation (notepad)
- Redial of both PABX and external calls
- Supports 16 dial keys: 0 to 9, *, # A, B, C, and D
- Supports 4 function keys:
  - Program (P) used to input notepad numbers
  - Flash (FL) allows re-dialling without on-hook
  - Redial (R) recalls and redialls stored number
  - Change from pulse dial to DTMF dial in mixed mode (>)
- DTMF timing:
  - for manual dialling, maximum duration burst/pause intervals are user-determined, but at least minimum duration burst/pause intervals are ensured
  - for redial, minimum duration burst/pause intervals are used
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT compatible)
- On-chip oscillator uses low-cost 3.58 MHz (TV colour burst) crystal or piezo resonator
- Uses standard single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced
- Flash (register recall) output.

2 GENERAL DESCRIPTION

The PCD3310 and PCD3310A are single-chip silicon gate CMOS integrated circuits. They are dual-standard diallers for pulse or dual tone multi-frequency (DTMF) dialling, with on-chip oscillators suitable for use with 3.58 MHz crystals.

Input data is derived from any standard matrix keyboard for dialling in either the pulse or DTMF mode.

Numbers up to 23 digits can be retained in RAM for dialling/redialling.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage		2.5	–	6.0	V
V_{stb}	standby supply voltage		1.8	–	6.0	V
$I_{DD(stb)}$	standby current (on hook)	V_{stb} = 1.8 V	–	1.4	4	µA
$I_{DD(conv)}$	operating current in conversation mode	V_{DD} = 3 V	–	–	150	µA
$I_{DD(pulse)}$	operating current in pulse dialling mode	V_{DD} = 3 V	–	–	200	µA
$I_{DD(DTMF)}$	operating current in DTMF dialling mode	V_{DD} = 3 V	–	0.6	0.9	mA
$V_{HG(RMS)}$	DTMF output voltage level for HIGH group (RMS value)		–	192	–	mV
$V_{LG(RMS)}$	DTMF output voltage level for LOW group (RMS value)		–	150	–	mV
G_v	voltage gain (pre-emphasis) of group		–	2.1	–	dB
THD	total harmonic distortion		–	–25	–	dB
T_{amb}	operating ambient temperature		–25	–	+70	°C

4 ORDERING INFORMATION

Table 1 Package information

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3310P	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
PCD3310AP	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
PCD3310T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCD3310AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

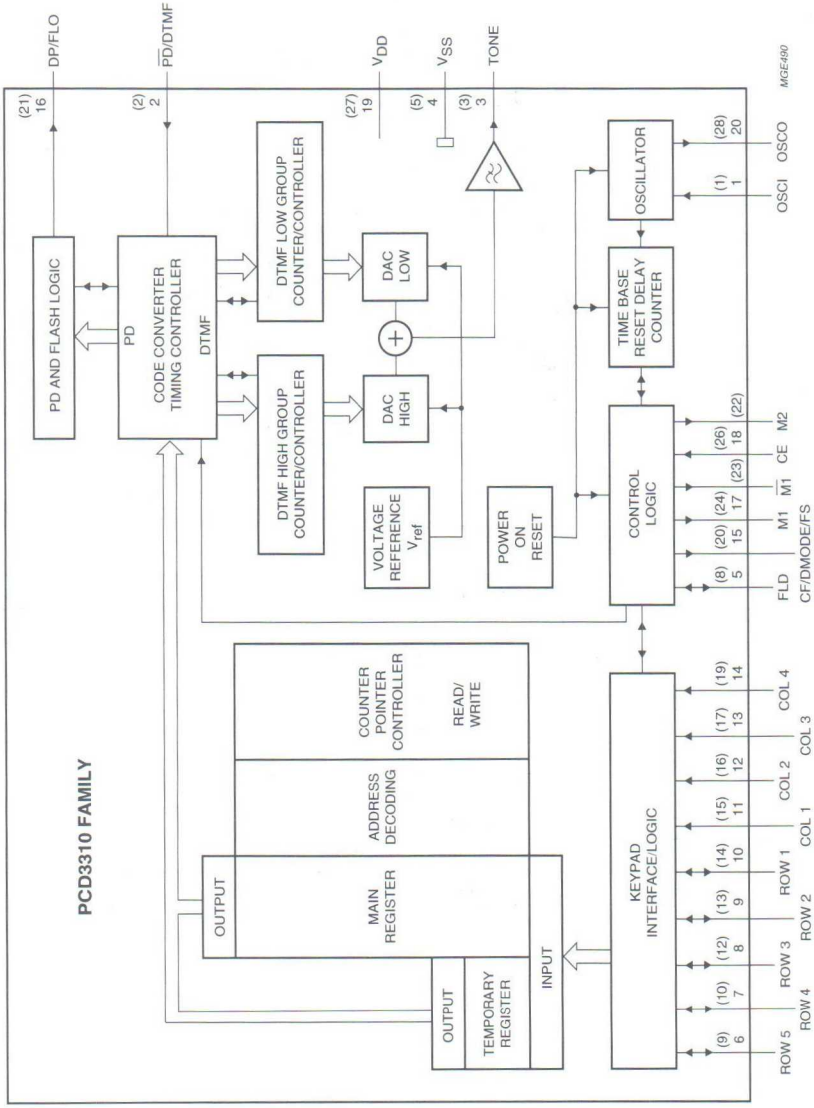
Table 2 Functional options

TYPE NUMBER	PULSE DIAL; BREAK/MAKE TIME (see notes 1 and 2)	MARK-TO-SPACE RATIO
PCD3310P	67, 33 ms	2 : 1
PCD3310T	67, 33 ms	2 : 1
PCD3310AP	60, 40 ms	3 : 2
PCD3310AT	60, 40 ms	3 : 2

Notes

1. Pulse frequency 10 Hz, inter-digit pause (t_{id}) = 840 ms.
2. Note that the PCD3310P; 10T and the PCD3310AP; 10AT differ only in the break/make ratio in pulse dialling. The break/make times equate to mark-to-space ratios of 2 : 1 and 3 : 2 respectively.

5 BLOCK DIAGRAM



The pin numbers given in parenthesis refer to the PCD3310T.

Fig.1 Block diagram.

6 PINNING

SYMBOL	PINS		TYPE	DESCRIPTION
	PCD3310P PCD3310AP	PCD3310T PCD3310AT		
OSCI	1	1	I	oscillator input
$\overline{PD}$/DTMF	2	2	I	select pin; pulse or DTMF dialling input
TONE	3	3	O	single or dual tone frequency output
n.c.	–	4	–	not connected
V_{SS}	4	5	P	negative supply
n.c.	–	6	–	not connected
n.c.	–	7	–	not connected
FLD	5	8	I/O	flash duration control input/output
ROW 5	6	9	I/O	scanning row 5 keyboard input/output
ROW 4	7	10	I/O	scanning row 4 keyboard input/output
n.c.	–	11	–	not connected
ROW 3	8	12	I/O	scanning row 3 keyboard input/output
ROW 2	9	13	I/O	scanning row 2 keyboard input/output
ROW 1	10	14	I/O	scanning row 1 keyboard input/output
COL 1	11	15	I	sense column 1 keyboard input (with internal pull-up resistor)
COL 2	12	16	I	sense column 2 keyboard input (with internal pull-up resistor)
COL 3	13	17	I	sense column 3 keyboard input (with internal pull-up resistor)
n.c.	–	18	–	not connected
COL 4	14	19	I	sense column 4 keyboard input (with internal pull-up resistor)
CF/DMODE/FS	15	20	O	confidence tone/dialling mode/frequency select outputs
DP/FLO	16	21	O	dialling pulse and flash output
M2	–	22	O	muting output 2
$\overline{M1}$	–	23	O	muting output 1 (active LOW)
M1	17	24	O	muting output 1
n.c.	–	25	–	not connected
CE	18	26	I	chip enable input
V_{DD}	19	27	P	positive supply voltage
OSCO	20	28	O	oscillator output

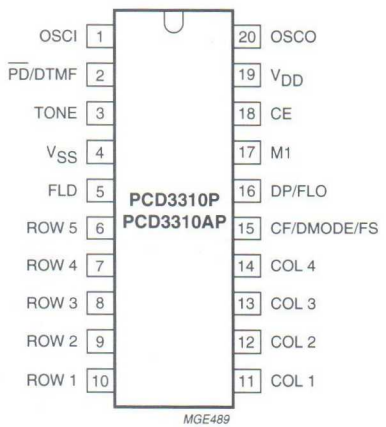


Fig.2 Pin configuration (DIP20 package).

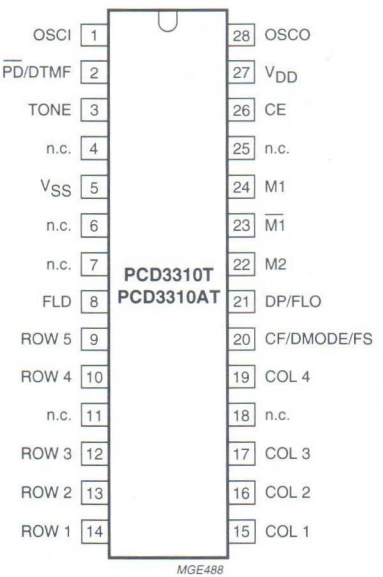


Fig.3 Pin configuration (SO28 package).

7 FUNCTIONAL DESCRIPTION

References to 'the device' apply to both the PCD3310 and the PCD3310A.

7.1 Power supply (V_{DD} and V_{SS})

The positive supply of the device (V_{DD}) must meet the voltage requirements as indicated in Chapter 11.
To avoid undefined states of the device at power-on, an internal reset circuit clears the control logic and counters. If V_{DD} drops below the minimum standby supply voltage of 1.8 V the power-on reset circuit inhibits redialling after hook-off. The power-on reset signal has the highest priority; it blocks and resets the device without delay regardless of the state of chip enable input (CE).

7.2 Clock oscillator (OSCI and OSCO)

The timebase for the device for both pulse and DTMF dialling is a crystal controlled on-chip oscillator which is completed by connecting a 3.58 MHz crystal or ceramic resonator between the OSCI and OSCO pins.
Recommended resonator type:

- 3.58 MHz PXE - Murata; CSA 3.58MG310VA.

7.3 Chip enable (CE)

The CE input enables the device and is used to initialize the device. When CE is LOW it provides the static standby condition. In this state the clock oscillator is disabled, all registers and logic are reset with the exception of the redial registers, Read Address Counter (RAC), Write Address Counter (WAC) and Temporary Write Address Counter (TWAC). The RAC points to the first digit of the last number dialled, the WAC and TWAC point to the last entered digits in the main and temporary registers (see Fig.6). The keyboard input is inhibited, but data previously entered is saved in the redial registers provided V_{DD} is higher than V_{stb}. The current drawn is I_{stb} (standby current) and serves to retain data in the redial registers during hook-on.

When CE is HIGH it activates the clock oscillator and the device changes from static standby condition to the conversation mode. The current consumption is $I_{DD(conv)}$ until the first digit is entered from the keyboard. Then a dialling or redialling operation starts. The operating current is $I_{DD(pulse)}$ if in the pulse dialling mode, or $I_{DD(DTMF)}$ if the DTMF dialling mode is selected.

If the CE input is taken to a LOW level for longer than time period t_{rd} (see Figs 11 and 12 and Chapter 12) an internal reset pulse will be generated at the end of the t_{rd} period. The system changes to the static standby state. Short CE pulses of $< t_{rd}$ will not affect the operation of the device and reset pulses are not produced.

7.4 Mode selection ($\overline{PD}$/DTMF)

7.4.1 PULSE MODE

If $\overline{PD}$/DTMF = V_{SS} the pulse mode is selected. Entries of non-numeric keys are neglected, they are neither stored in the redial register nor transmitted.

7.4.2 DTMF MODE

If $\overline{PD}$/DTMF = V_{DD} the dual tone multi-frequency dialling mode is selected. Each non-function key activated corresponds to a combination of two tones, one of four LOW and one of four HIGH frequencies, corresponding to the key's row and column in the keyboard matrix. See Fig.4 and Table 3. The frequencies are transmitted with a constant amplitude, regardless of power supply variations. Harmonic content is filtered out thus meeting the CEPT recommendations.

The transmission time is calibrated for redial. In manual operation the duration of bursts and pauses is the actual key depression time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

7.4.3 MIXED MODE

When the $\overline{PD}$/DTMF pin is open-circuit the mixed mode is selected. After activation of CE or FL (Flash) the device starts as a pulse dialler and remains in this state until a non-numeric dial key (A, B, C, D, *, #) or the function key > is activated. Pressing a non-numeric dial key causes the corresponding DTMF tones to be output, and any subsequent dialling to be in DTMF mode. Pressing > causes no output tones, but any subsequent dialling is in DTMF mode. The > key should be used if the first DTMF output required is numeric. The device remains in DTMF dial mode until FL is activated or after a static standby condition when CE is re-activated.

A connection between the $\overline{PD}$/DTMF pin and V_{DD} also initiates DTMF dialling. Chip enable, FL or a connection of $\overline{PD}$/DTMF pin to V_{SS} sets the device back to pulse dialling.

7.5 Keyboard inputs/outputs

The sense column inputs COL 1 to COL 4 and the scanning row outputs ROW 1 to ROW 5 of the device are connected to the keyboard as shown in Fig.4. All keyboard entries are debounced on both the leading and trailing edges for approximately time period t_e as shown in Figs 11, 12, 13 and 14. Each entry is tested for validity. When a key is depressed, keyboard scanning starts and only returns to the sense mode after release of that key.

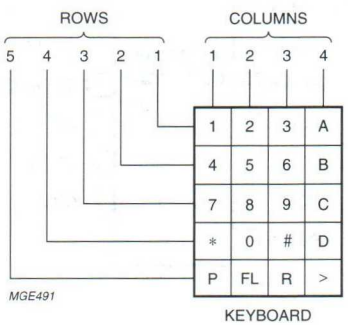


Fig.4 Keyboard organization.

ROW 5 of the keyboard contains the following function keys:

- P = memory clear and programming (notepad)
- FL = flash or register recall
- R = redial
- > = change of dial mode from pulse to DTMF in mixed dialling mode.

In the pulse dialling mode the valid keys are the 10 numeric dial keys (0 to 9). The non-numeric dial keys (A, B, C, D, *, #) have no effect on the dialling or the redial storage. Valid function keys are P, R and FL.

In the DTMF mode all dial keys are valid. They are transmitted as a dual tone combination and at the same time stored in the redial register. Valid function keys are P, FL and R.

In the mixed mode all key entries are valid and executed accordingly.

7.6 Flash duration control (FLD)

Flash (or register recall) is activated by the FL key and can be used in DTMF and pulse dialling modes.

The FL key has the same effect as placing the telephone 'on-hook' for a calibrated time. Pressing the FL key will produce a timed line-break of 100 ms (min.) at the DP/FLO output. During the conversation mode pressing FL also acts as a chip enable. The flash pulse duration (t_{FL}) is calibrated and can be prolonged with an external resistor and capacitor connected to the FLD input/output (see Fig.5). The flash pulse resets the Read Address Counter (RAC) to the address of the first entered digit of the last number dialled. Subsequent redial is possible (see Fig.9). The counter of the reset delay time is held for a period of t_{FL}.

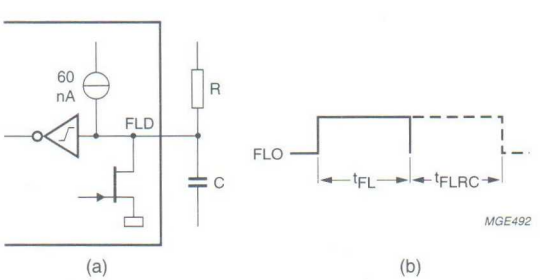
7.7 TONE output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched capacitor filter, followed by an on-chip active RC low-pass filter. Hence, the total harmonic distortion of the DTMF tones meets the CEPT recommendations. The tone output has the following states:

- tone OFF; 3-state
- tone ON; the associated frequencies are superimposed on a DC level of $\frac{1}{2}V_{DD}$.

When the DTMF mode is selected output tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS} and LOW group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

An on-chip reference voltage provides output tone levels independent of the supply voltage. Table 3 shows the frequency tolerance of the output tones for DTMF signalling.



(a) Flash duration control circuit.
(b) Flash pulse timing. $t_{FLRC} \approx R \times C$.

Fig.5 Flash pulse duration setting.

Table 3 Frequency tolerance of the output tones for DTMF signalling; f_{xtal} = 3.579545 MHz

ROW/COLUMN	STANDARD FREQUENCY (Hz)	TONE OUTPUT FREQUENCY (Hz)	FREQUENCY DEVIATION	
			%	Hz
ROW 1	697	697.90	+0.13	+0.90
ROW 2	770	770.46	+0.06	+0.46
ROW 3	852	850.45	−0.18	−1.55
ROW 4	941	943.23	+0.24	+2.23
COL 1	1209	1206.45	−0.21	−2.55
COL 2	1336	1341.66	+0.42	+5.66
COL 3	1477	1482.21	+0.35	+5.21
COL 4	1633	1638.24	+0.32	+5.25

7.8 Dial pulse and Flash output (DP/FLO)

This is a combined output which provides control signals for timing in pulse dialling or for a calibrated line break (flash or register recall) in both dialling modes.

7.9 Mute output (M1)

The MUTE output can be used to disable the microphone during dialling.

During pulse dialling the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialling the mute output becomes active HIGH for the period of tone transmission and remains at this level until the end of hold-over time. It is also active HIGH during flash and flash hold-over time.

7.10 Mute output ($\overline{M1}$)

Inverted output of M1. In the PCD3310P it is only available as a bonding option of M1.

7.11 Muting output (M2)

Active HIGH output during actual dialling; i.e. during break or make time in pulse dialling, or during tone ON/OFF in DTMF dialling. It is an open drain p-channel output.

8 DIALLING PROCEDURES (see Figs 7, 8 and 9)

8.1 Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address of both the main and temporary redial registers, ready to redial any stored number (see Fig.6). By dialling the first valid digit, the Temporary Write Address Counter (TWAC) will be set to the first address of the temporary register, and the decoded digit will be stored in the temporary register at that address. The TWAC is then incremented to the next address. The first 5 valid digits will be decoded and stored in the temporary register in this way, and have no effect on the main register and its associated Write Address Counter (WAC). After the sixth valid digit is entered, the TWAC indicates an overflow condition. The data from the temporary register will be copied into the 5 least significant places of the main register and the TWAC into the WAC. The sixth digit, and all subsequent digits will be stored in the main register (a total of not more than 23). If more than 23 digits are entered redial will be inhibited. If not more than 5 digits are entered only the temporary register and the associated TWAC are affected.

All entries are debounced on both the leading and trailing edges for at least time period t_e as shown in Figs 11, 12, 13 and 14.

Each entry is tested for validity before being stored in the redial registers.

- For DTMF dialling all dial keys are valid
- For pulse dialling only numeric dial keys are valid.

Simultaneous to their acceptance and corresponding to the selected mode (pulse, DTMF or mixed), the entries are transmitted as pulse-trains or as DTMF frequencies in accordance with PTT requirements. Non-numeric dial key entries are neglected during pulse dialling; they are neither stored nor transmitted.

8.2 Redialling

After CE has risen to V_{DD} the oscillator starts running. The address of the first digit in the redial register is stored in the RAC, and the device is in the conversation mode. If 'R' is the first keyboard entry the device starts redialling the contents of the temporary register. If the overflow flag of the TWAC was set in the previous dialling, the redialling continues in the main register.

Because access to an external line from a PABX usually involves dialling an access code and waiting for an access tone, a 'one-press' redial may fail due to insufficient delay between the access code and the external number. For this reason, the access code should be redialled. If the access code (up to 4 digits) matches the first part of the stored number, then pressing R after the access tone is obtained will cause the rest of the number to be redialled (see Fig.7, PABX).

Timing in the DTMF mode is calibrated for both tone bursts and pauses.

In mixed mode only the first part entered (the pulse dialled part of the stored number) can be redialled.

During redial keyboard entries (function or non-function) are not accepted until the device returns to the conversation mode after completion of redialling. No redial activity takes place if one of the following events occur:

- Power-on reset
- Memory clear ('P' without subsequent data entry)
- Memory overflow (more than 23 valid data entries).

8.3 Notepad

The redial register can also be used as a notepad. In the conversation mode a number with up to 23 digits can be entered and stored for redialling. By activating the program key (P) the WAC and TWAC pointers are reset. This acts like a memory clear (redial is inhibited). Afterwards, by entering and storing any digits, redialling will be possible after flash or hook-on and hook-off (see Fig.9).

During notepad programming the numbers entered will not be transmitted nor is the mute active, only the confidence tone is generated.

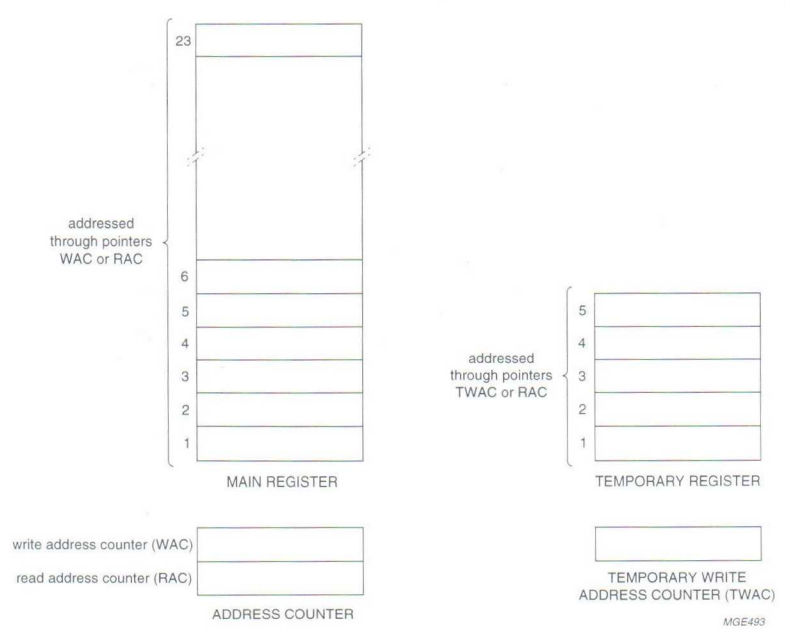
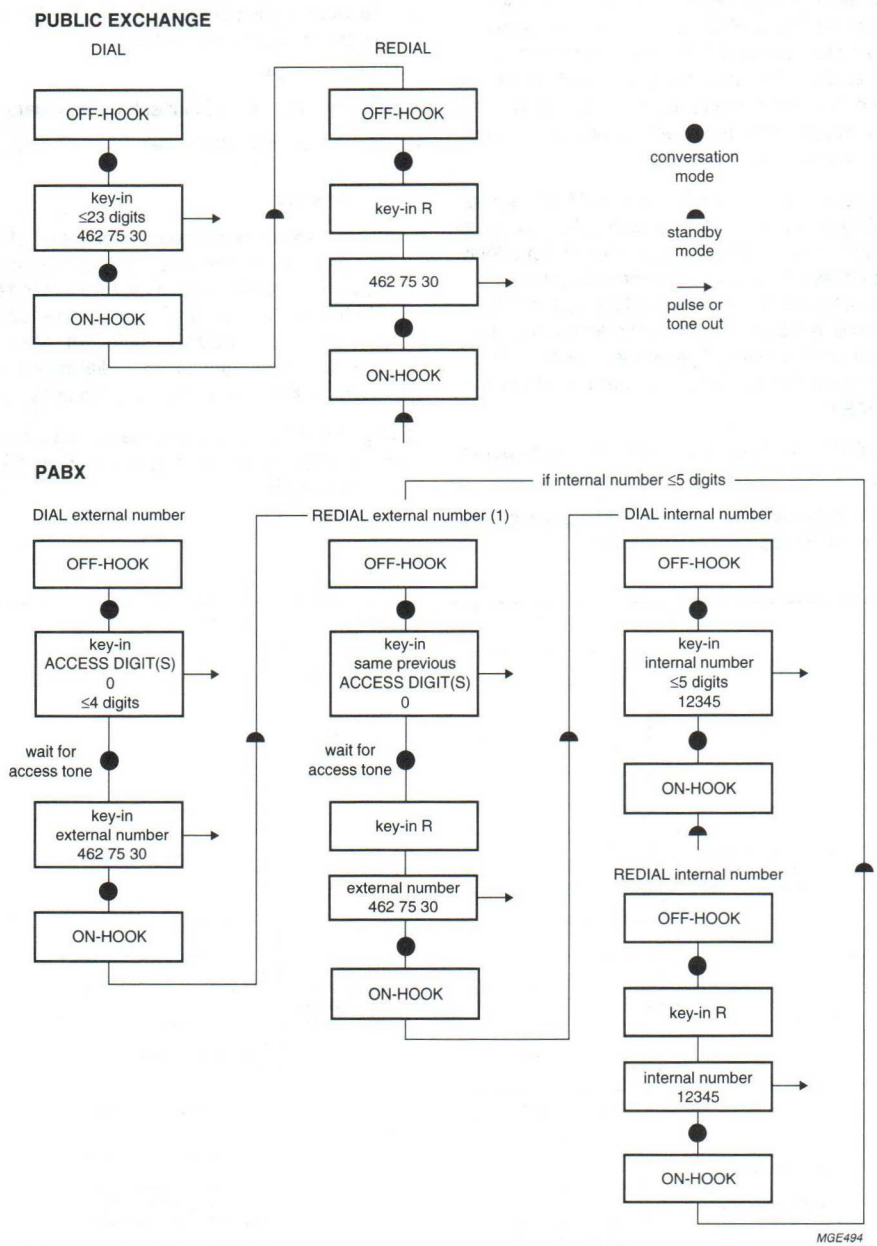


Fig.6 Program memory map.



(1) If [access digit(s) + external number] ≤23 digits.

Fig.7 $\overline{\text{Pulse}}$ or DTMF dialling mode.

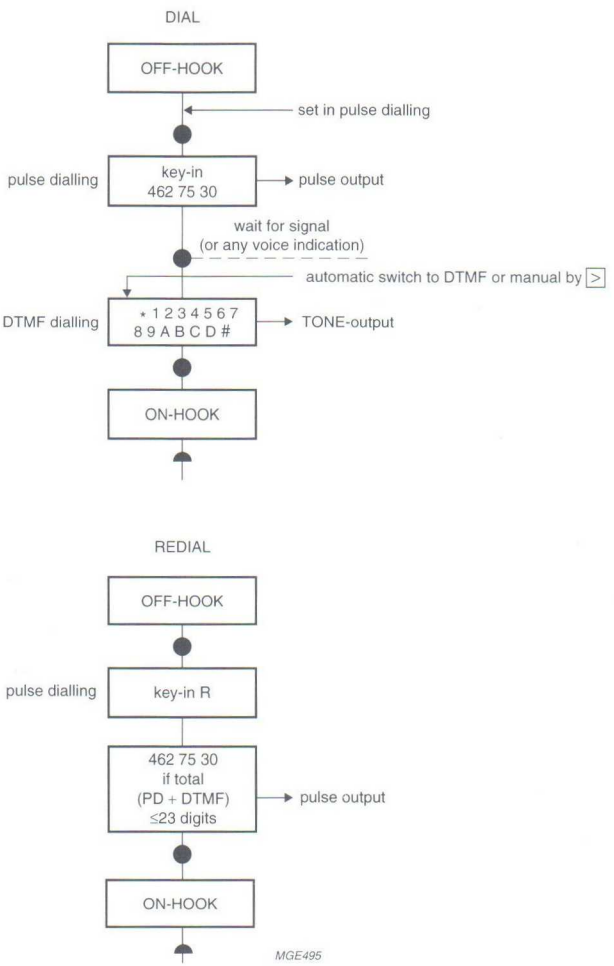


Fig.8 Pulse/DTMF and mixed mode dialling.

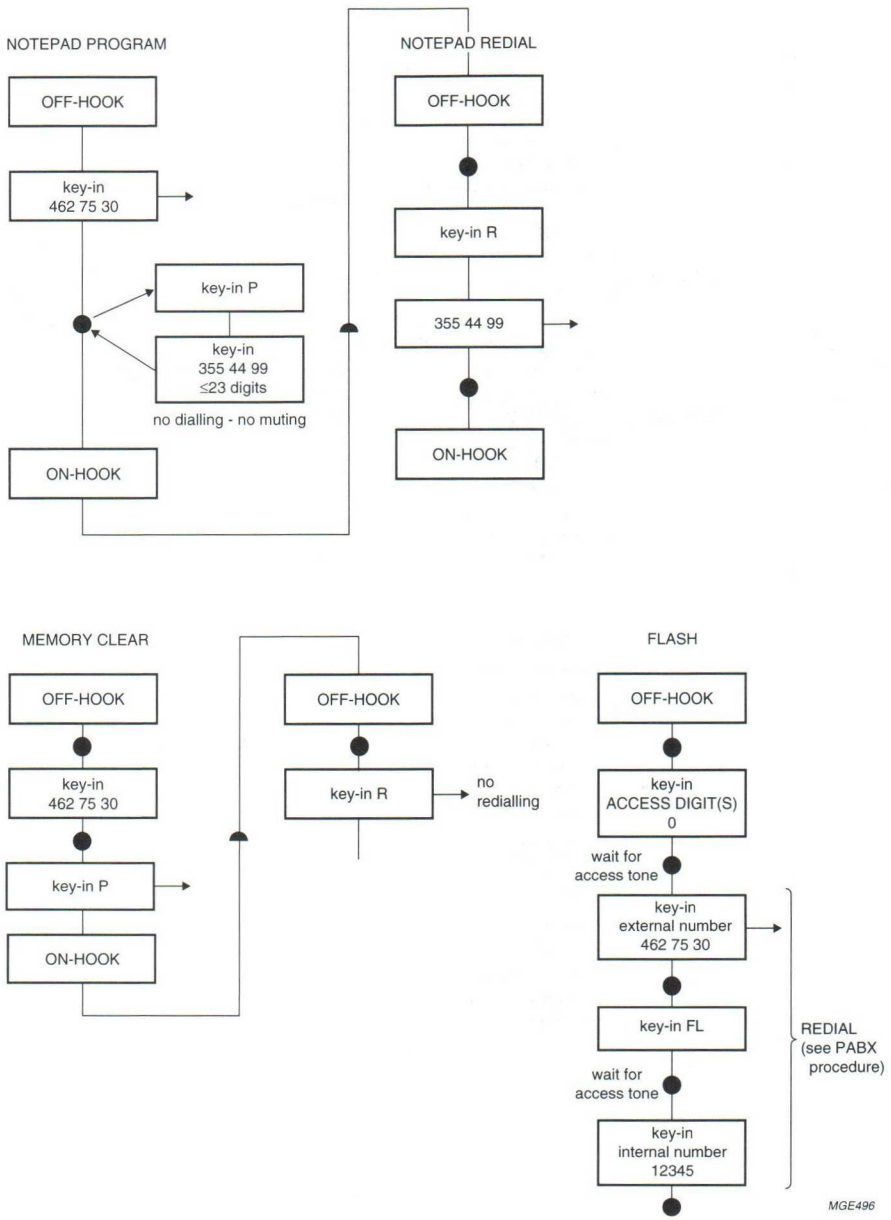


Fig.9 Notepad, memory clear, flash; independent of dialling mode.

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Data Handbook ICO3, Section: General, Handling MOS devices"*).

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+8.0	V
I_{DD}	supply current	−	50	mA
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
V_I	all input voltages	−0.8	V_{DD} + 0.8	V
P_{tot}	total power dissipation	−	300	mW
P_o	power dissipation per output	−	50	mW
T_{stg}	storage temperature range	−65	+150	°C
T_{amb}	operating ambient temperature	−25	+70	°C

11 CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; f_{osc} = 3.579545 MHz; T_{amb} = −25 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	operating supply voltage		2.5	−	6.0	V
V_{stb}	standby supply voltage		1.8	−	6.0	V
$I_{DD(conv)}$	operating supply current in conversation mode	oscillator ON	−	−	150	µA
$I_{DD(pulse)}$	operating supply current in pulse dialling or flash mode		−	−	200	µA
$I_{DD(DTMF)}$	operating supply current in DTMF dialling mode	tone ON	−	0.6	0.9	mA
		one OFF	−	−	200	µA
$I_{DD(stb)}$	standby supply current	V_{DD} = 1.8 V oscillator OFF; note 1	−	1.4	4.0	µA
Inputs						
V_{IL}	LOW level input voltage		0	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD}	V
I_{LI}	input leakage current pin CE		−1	−	+1	µA
Keyboard inputs						
R_{KON}	keyboard ON resistance		−	−	2	kΩ
R_{KOFF}	keyboard OFF resistance		1	−	−	MΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
I_{OL}	LOW level output sink current pins M1, $\overline{M1}$, DP/FLO, CF and FLD	$V_{OL} = V_{SS} + 0.5$ V	0.7	–	–	mA
	LOW level output sink current pin $\overline{PD}$/DTMF	$V_{OL} = V_{SS} + 0.5$ V; note 2	–	–	1	mA
I_{OH}	HIGH level output source current pins M1, $\overline{M1}$, DP/FLO, CF and M2	$V_{OH} = V_{DD} - 0.5$ V	–0.6	–	–	mA
	HIGH level output source current pin $\overline{PD}$/DTMF	$V_{OH} = V_{DD} - 0.5$ V; note 2	–	–	–1	mA
	HIGH level output source current pin FLD	$V_{OH} = V_{DD} - 0.5$ V; note 3	–	–60	–	nA
Tone output (see Fig.10)						
$V_{HG(RMS)}$	DTMF output voltage levels for HIGH group (RMS value)	$V_{DD} = 2.5$ to 6 V	158	192	205	mV
$V_{LG(RMS)}$	DTMF output voltage levels for LOW group (RMS value)	$V_{DD} = 2.5$ to 6 V	125	150	160	mV
Δf	frequency deviation		–0.6	–	+0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_O \rvert$	output impedance		–	0.1	0.5	kΩ
G_v	voltage gain (pre-emphasis) of group		1.85	2.1	2.35	dB
THD	total harmonic distortion	$T_{amb} = 25$ °C; note 4	–	–25	–	dB

Notes

1. Crystal connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
2. $< \lvert 10$ mA$\rvert$ dynamic current to set/reset $\overline{PD}$/DTMF pin (mixed mode).
3. Flash inactive; output voltage = V_{SS}.
4. Related to the level of the LOW group frequency component, according to CEPT recommendations.

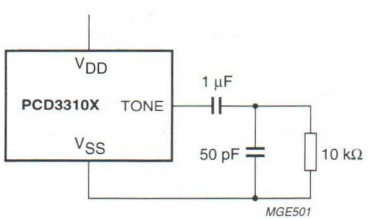
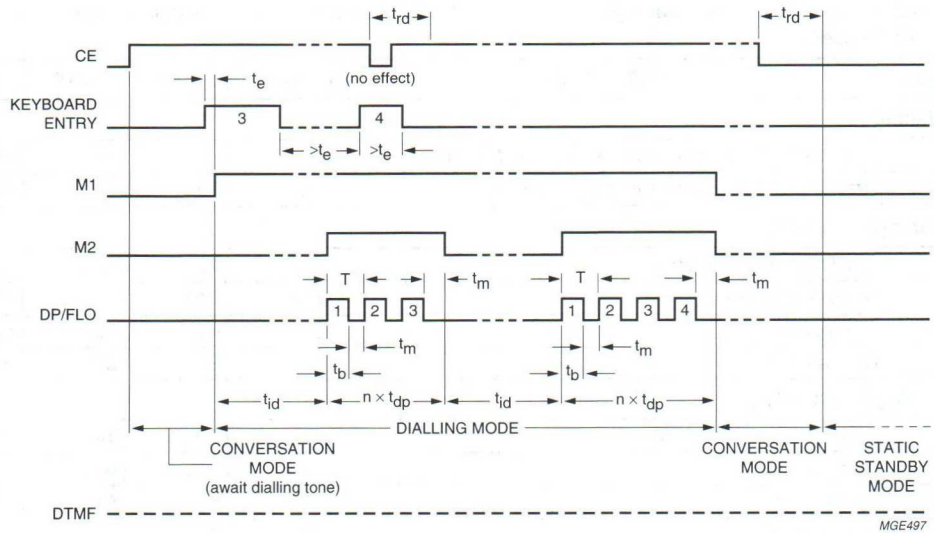


Fig.10 Tone output test circuit.

12 TIMING CHARACTERISTICS

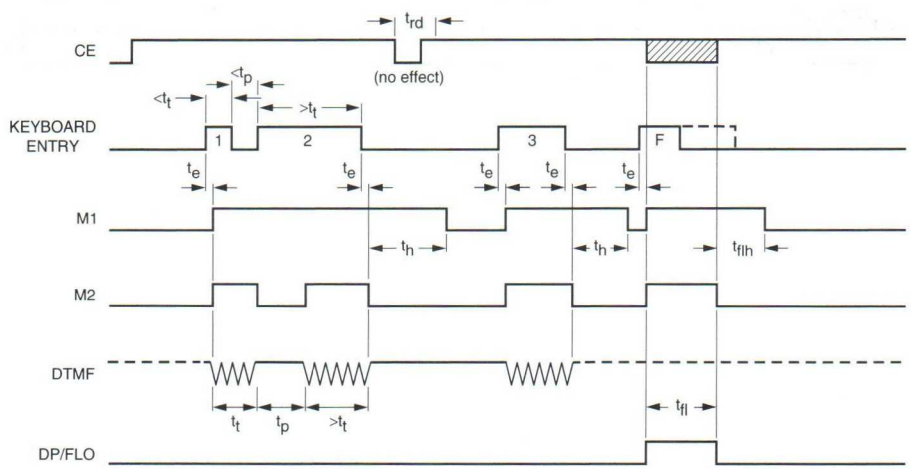
When any key is activated a square wave (330 Hz) is generated and appears at the CF output to serve as an acoustic feed-back for the user.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
DTMF dialling					
t_t, t_p	transmission and pause times (manual dialling)	68	–	–	ms
t_t, t_p	transmission and pause times (redialling)	68	70	72	ms
Pulse dialling (PCD3310)					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	66	67	68	ms
t_m	make time	32	33	34	ms
Pulse dialling (PCD3310A)					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	59	60	61	ms
t_m	make time	39	40	41	ms
General					
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	78	80	81	ms
t_{on}	clock start-up time	–	4	–	ms
t_e	debounce time	–	12	–	ms
t_{rd}	reset delay time	–	160	–	ms



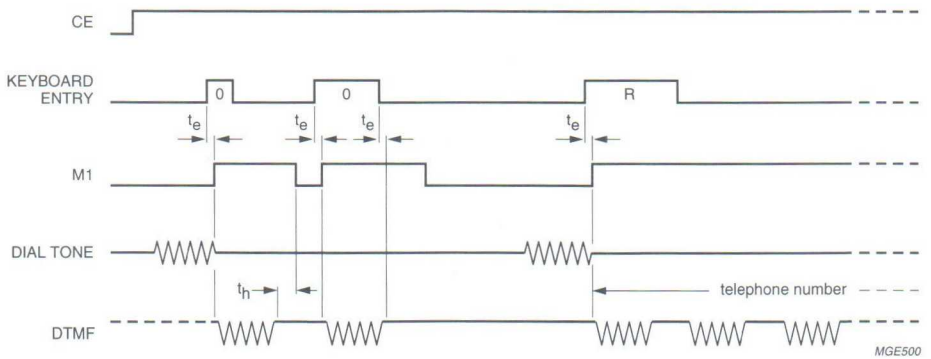
The dashed line signifies floating.

Fig.11 Timing diagram for pulse dialling ($\overline{PD}$/DTMF = V_{SS}).



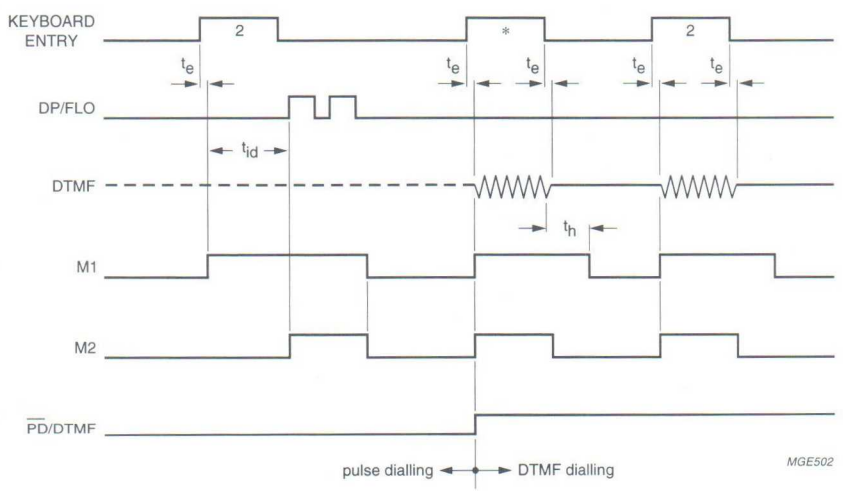
The dashed line signifies floating.

Fig.12 Timing diagram for DTMF dialling ($\overline{PD}$/DTMF = V_{DD}).



The dashed line signifies floating.

Fig.13 Timing diagram showing REDIAL where PABX access digits are the first keyboard entries in DTMF dialling mode.



The dashed line signifies floating.

Fig.14 .Timing diagram for mixed mode ($\overline{PD}$/DTMF open-circuit).

13 APPLICATION INFORMATION

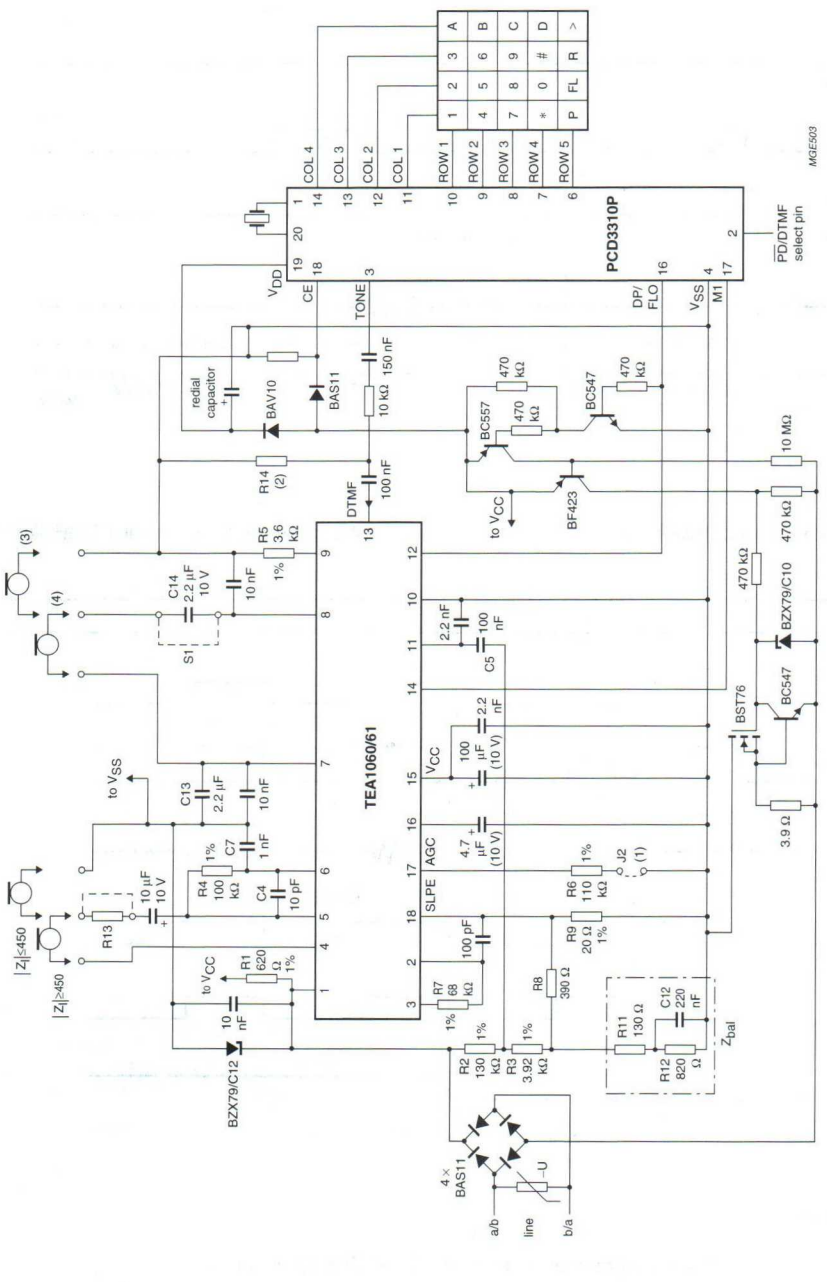


Fig.15 Application diagram of the full electronic basic telephone set.

(1) Automatic line compensation obtained by connecting R6 to V_{SS}.
(2) The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA1060 and TEA1061.
(3) Symmetrical low-impedance inputs for dynamic and magnetic microphones (TEA1060).
(4) Asymmetrical high-impedance inputs for electret microphones (TEA1061).

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1 FEATURES

- DTMF, modem and musical tone generation
- Stabilized output voltage level
- Low output distortion with on-chip filtering conforming to CEPT recommendations
- Latched inputs for data bus applications
- I^2C-bus compatible
- Selection of parallel or serial (I^2C-bus) data input (PCD3311C).

2 GENERAL DESCRIPTION

The PCD3311C and PCD3312C are single-chip silicon gate CMOS integrated circuits. They are intended principally for use in telephone sets to provide the dual-tone multi-frequency (DTMF) combinations required for tone dialling systems. The various audio output frequencies are generated from an on-chip 3.58 MHz quartz crystal-controlled oscillator. A separate crystal is used, and a separate microcontroller is required to control the devices.

Both the devices can interface to I^2C-bus compatible microcontrollers for serial input. The PCD3311C can also interface directly to all standard microcontrollers, accepting a binary coded parallel input.

With their on-chip voltage reference the PCD3311C and PCD3312C provide constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with CEPT recommendations.

In addition to the standard DTMF frequencies the devices can also provide:

- Twelve standard frequencies used in simplex modem applications for data rates from 300 to 1200 bits per second
- Two octaves of musical scales in steps of semitones.

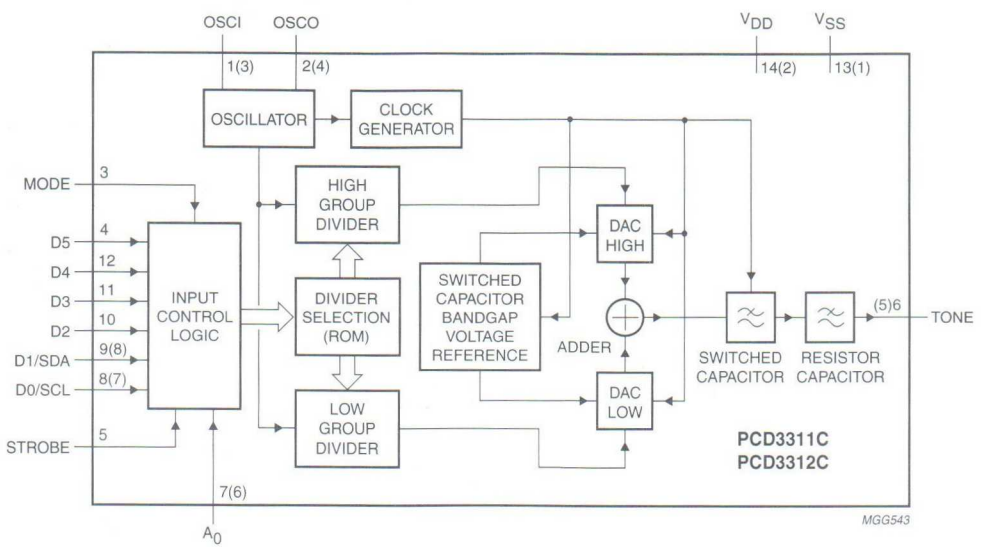
3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage	2.5	–	6.0	V
I_{DD}	operating supply current	–	–	0.9	mA
I_{stb}	standby current	–	–	3	µA
$V_{HG(RMS)}$	DTMF HIGH group output voltage level (RMS value)	158	192	205	mV
$V_{LG(RMS)}$	DTMF LOW group output voltage level (RMS value)	125	150	160	mV
G_v	pre-emphasis (voltage gain) of group	1.85	2.10	2.35	dB
THD	total harmonic distortion	–	–25	–	dB
T_{amb}	operating ambient temperature	–25	–	+70	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3311CP	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
PCD3311CT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCD3312CP	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCD3312CT	SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT176-1

5 BLOCK DIAGRAM



The un-parenthesised numbers are for the PCD3311CP, those in parenthesis for the PCD3312C.

Fig.1 Block diagram.

6 PINNING INFORMATION

6.1 Pinning PCD3311CP

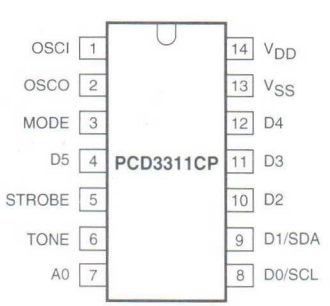


Fig.2 Pin configuration PCD3311CP.

6.2 Pin description PCD3311CP

SYMBOL	PIN	TYPE	DESCRIPTION
OSCI	1	I	oscillator input
OSCO	2	O	oscillator output
MODE	3	I	mode select input (selects I^2C or parallel data input)
D5	4	I	parallel data input
STROBE	5	I	strobe input (for loading data in parallel mode)
TONE	6	O	frequency output (DTMF, modem, musical tones)
A0	7	I	slave address input (to be connected to V_{DD} or V_{SS})
D0/SCL	8	I	parallel data input or I^2C-bus clock line
D1/SDA	9	I	parallel data input or I^2C-bus data line
D2 – D4	10 – 12	I	parallel data inputs
V_{SS}	13	P	negative supply
V_{DD}	14	P	positive supply

6.3 Pinning PCD3311CT

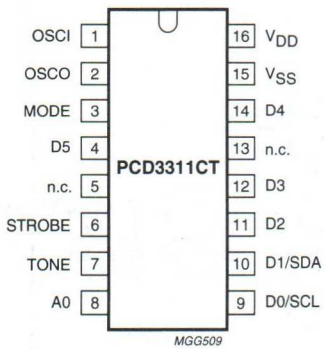


Fig.3 Pin configuration PCD3311CT.

6.4 Pin description PCD3311CT

SYMBOL	PIN	TYPE	DESCRIPTION
OSCI	1	I	oscillator input
OSCO	2	O	oscillator output
MODE	3	I	mode select input (selects I^2C or parallel data input)
D5	4	I	parallel data input
n.c.	5	–	not connected
STROBE	6	I	strobe input (for loading data in parallel mode)
TONE	7	O	frequency output (DTMF, modem, musical tones)
A0	8	I	slave address input (to be connected to V_{DD} or V_{SS})
D0/SCL	9	I	parallel data input or I^2C-bus clock line
D1/SDA	10	I	parallel data input or I^2C-bus data line
D2, D3	11, 12	I	parallel data inputs
n.c.	13	–	not connected
D4	14	I	parallel data input
V_{SS}	15	P	negative supply
V_{DD}	16	P	positive supply

6.5 Pinning PCD3312C

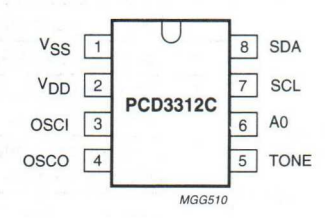


Fig.4 Pin configuration PCD3312C.

6.6 Pin description PCD3312C

SYMBOL	PIN	TYPE	DESCRIPTION
V_{SS}	1	P	negative supply
V_{DD}	2	P	positive supply
OSCI	3	I	oscillator input
OSCO	4	O	oscillator output
TONE	5	O	frequency output (DTMF, modem, musical tones)
A0	6	I	slave address input (to be connected to V_{DD} or V_{SS})
SCL	7	I	I^2C-bus clock line
SDA	8	I	I^2C-bus data line

7 FUNCTIONAL DESCRIPTION

7.1 General (see Fig.1)

The Input Control Logic decodes the input data to determine whether DTMF, modem or musical tones are selected; and which particular tone or combination of tones is required.

A code representing the required tones is sent to the Divider Selection ROM which selects the correct division ratio in both of the Frequency Dividers (or in one divider, if only a single tone is required).

The Oscillator circuit provides a square wave of frequency 3.58 MHz. Each Frequency Divider divides the frequency of the Oscillator to give a serial digital square wave with a frequency simply related to that of the required tone.

The output from each Frequency Divider goes to a DAC, which is also fed by a clock derived from the oscillator. Using these two signals, the DAC produces an approximate sine wave of the required frequency, with an amplitude derived from the Voltage Reference.

The output from the DAC goes to an Adder where, for DTMF, it is combined with the output from the other DAC.

The output from the Adder goes through two stages of Low Pass Filters to give a smoothed tone (single or dual), and finally to the TONE output.

7.2 Clock/oscillator connection

The timebase for the PCD3311C and PCD3312C is a crystal-controlled oscillator, requiring a 3.58 MHz quartz crystal to be connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock of 3.58 MHz.

7.3 Mode selection (PCD3311C)

The MODE input selects the data input mode for the PCD3311C. When MODE is connected to V_{DD} (HIGH), data can be received in the parallel mode. When connected to V_{SS} (LOW) or left open, data can be received via the serial I^2C-bus.

PCD 3312C has no MODE input as data input is via the I^2C-bus only.

7.4 Data inputs (PCD3311C)

Inputs D0, D1, D2, D3, D4 and D5 are used in the parallel data input mode of the PCD3311C. Inputs D0 and D1 are also used in serial input mode when they act as the SCL and SDA inputs respectively. Inputs D0 and D1 have no internal pull-down or pull-up resistors and must not be left open in any application. Inputs D2, D3, D4 and D5 have internal pull-down.

D4 and D5 are used to select between DTMF dual, DTMF single, modem and musical tones (see Table 1). D0, D1, D2 and D3 select the tone combination or single tone within the selected application. They also, in combination with D4, select the standby mode. See Tables 2, 3, 4 and 5.

PCD 3312C has no parallel data pins as data input is via the I^2C-bus.

Table 1 Use of D5 and D4 to select application

D5	D4	APPLICATION
LOW	LOW	DTMF single tones; musical tones; standby
LOW	HIGH	DTMF dual tones (all 16 combinations)
HIGH	LOW	modem tones
HIGH	HIGH	musical tones

7.5 Strobe input (PCD3311C)

The STROBE input (with internal pull-down) allows the loading of parallel data into D0 to D5 when MODE is HIGH.

The data inputs must be stable preceding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received. Figure 5 is an example of the timing relationship between STROBE and the data inputs.

When MODE is LOW, data is received serially via the I^2C-bus.

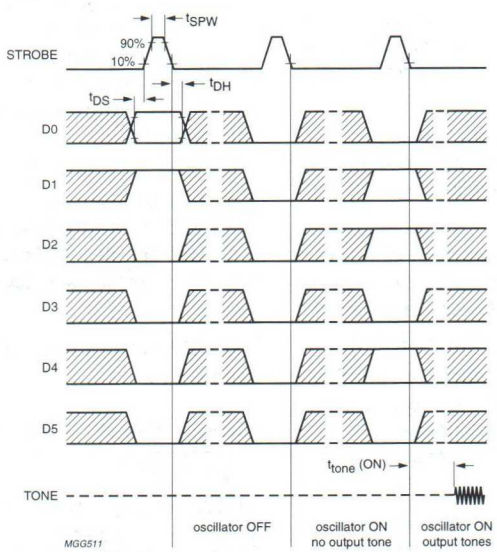


Fig.5 Timing of STROBE, parallel data inputs and TONE output (770 Hz + 1477 Hz in example) in the parallel mode (MODE = HIGH).

7.6 I²C-bus clock and data inputs

SCL and SDA are the serial clock and serial data inputs according to the I²C-bus specification, see Chapter 8. SCL and SDA must be pulled up externally to V_{DD}.

For the PCD3311C, SCL and SDA are combined with parallel inputs D0 and D1 respectively - D0/SCL and D1/SDA operate serially only when MODE is LOW.

7.7 Address input

Address input A0 defines the least significant bit of the I²C-bus address of the device (see Fig.6). The first 6 bits of the address are fixed internally. By tying the A0 of each device to V_{DD} (HIGH) and V_{SS} (LOW) respectively, two different PCD3311C or PCD3312C devices can be individually addressed on the bus.

Whether one or two devices are used, A0 must be connected to V_{DD} or V_{SS}.

7.8 I²C-bus data configuration (see Fig.6)

The PCD3311C and PCD3312C are always slave receivers in the I²C-bus configuration. The R/$\overline{W}$ bit in is thus always LOW, indicating that the master (microcontroller) is writing.

The slave address in the serial mode consists of 7 bits: 6 bits internally fixed, 1 externally set via A0. in the serial mode, the same input data codes are used as in the parallel mode. See Tables 2, 3, 4 and 5.

7.9 Tone output

The single and dual tones provided at the TONE output are first filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. The filtered tones fulfil the CEPT recommendations for total harmonic distortion of DTMF tones. An on-chip reference voltage provides output tone levels independent of the supply voltage. Tables 3, 4 and 5 give the frequency deviation of the output tones with respect to the standard DTMF, modem and music frequencies.

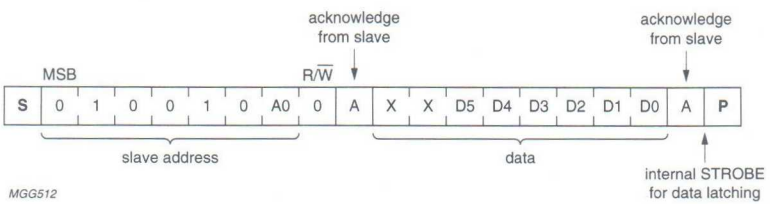


Fig.6 I²C-bus data format.

7.10 Power-on reset

In order to avoid an undefined state when the power is switched ON, the devices have an internal reset circuit which sets the standby mode (oscillator OFF).

7.11 TABLES OF INPUT AND OUTPUT

The specified output tones are obtained when a 3.579545 MHz crystal is used.

In each table, the logical states for the input data lines are related to voltage levels as follows:

1 = HIGH = V_{DD}

0 = LOW = V_{SS}

X = don't care

Table 2 Input data for no output tone, TONE in 3-state

D5	D4	D3	D2	D1	D0	HEX(1)	OSCILLATOR
X	0	0	0	0	0	00 or 20	ON
X	0	0	0	0	1	01 or 21	OFF
X	0	0	0	1	0	02 or 22	OFF
X	0	0	0	1	1	03 or 23	OFF

Note

1. The alternative HEX values depend on the value of D5.

Table 3 Input data and output for DTMF tones

D5	D4	D3	D2	D1	D0	HEX	SYMBOL	STANDARD FREQUENCY	TONE OUTPUT FREQ.	FREQUENCY DEVIATION	
								Hz	Hz	%	Hz
0	0	1	0	0	0	08	–	697	697.90	+0.13	+0.90
0	0	1	0	0	1	09	–	770	770.46	+0.06	+0.46
0	0	1	0	1	0	0A	–	852	850.45	–0.18	–1.55
0	0	1	0	1	1	0B	–	941	943.23	+0.24	+2.23
0	0	1	1	0	0	0C	–	1209	1206.45	–0.21	–2.55
0	0	1	1	0	1	0D	–	1336	1341.66	+0.42	+5.66
0	0	1	1	1	0	0E	–	1477	1482.21	+0.35	+5.21
0	0	1	1	1	1	0F	–	1633	1638.24	+0.32	+5.24
0	1	0	0	0	0	10	0	941+1336	–	–	–
0	1	0	0	0	1	11	1	697+1209	–	–	–
0	1	0	0	1	0	12	2	697+1336	–	–	–
0	1	0	0	1	1	13	3	697+1477	–	–	–
0	1	0	1	0	0	14	4	770+1209	–	–	–
0	1	0	1	0	1	15	5	770+1336	–	–	–
0	1	0	1	1	0	16	6	770+1477	–	–	–
0	1	0	1	1	1	17	7	852+1209	–	–	–
0	1	1	0	0	0	18	8	852+1336	–	–	–
0	1	1	0	0	1	19	9	852+1477	–	–	–
0	1	1	0	1	0	1A	A	697+1633	–	–	–
0	1	1	0	1	1	1B	B	770+1633	–	–	–
0	1	1	1	0	0	1C	C	852+1633	–	–	–
0	1	1	1	0	1	1D	D	941+1633	–	–	–
0	1	1	1	1	0	1E	*	941+1209	–	–	–
0	1	1	1	1	1	1F	#	941+1477	–	–	–

Table 4 Input data and output for modem tones

D5	D4	D3	D2	D1	D0	HEX	STANDARD FREQUENCY	TONE OUTPUT FREQ.	FREQUENCY DEVIATION		TELECOM. STANDARD
							Hz	Hz	%	Hz	
1	0	0	1	0	0	24	1300	1296.94	–0.24	–3.06	V.23
1	0	0	1	0	1	25	2100	2103.14	+0.15	+3.14	
1	0	0	1	1	0	26	1200	1197.17	–0.24	–2.83	Bell 202
1	0	0	1	1	1	27	2200	2192.01	–0.36	–7.99	
1	0	1	0	0	0	28	980	978.82	–0.12	–1.18	V.21
1	0	1	0	0	1	29	1180	1179.03	–0.08	–0.97	

D5	D4	D3	D2	D1	D0	HEX	STANDARD FREQUENCY	TONE OUTPUT FREQ.	FREQUENCY DEVIATION		TELECOM. STANDARD
							Hz	Hz	%	Hz	
1	0	1	0	1	0	2A	1070	1073.33	+0.31	+3.33	Bell 103
1	0	1	0	1	1	2B	1270	1265.30	−0.37	−4.70	
1	0	1	1	0	0	2C	1650	1655.66	+0.34	+5.66	V.21
1	0	1	1	0	1	2D	1850	1852.77	+0.15	+2.77	
1	0	1	1	1	0	2E	2025	2021.20	−0.19	−3.80	Bell 103
1	0	1	1	1	1	2F	2225	2223.32	−0.08	−1.68	

Table 5 Input/output for musical tones

D5	D4	D3	D2	D1	D0	HEX	NOTE	STD. FREQ. BASED ON A4 = 440 Hz	TONE OUTPUT FREQUENCY
								Hz	Hz
1	1	0	0	0	0	30	D#5	622.3	622.5
1	1	0	0	0	1	31	E5	659.3	659.5
1	1	0	0	1	0	32	F5	698.5	697.9
1	1	0	0	1	1	33	F#5	740.0	741.1
1	1	0	1	0	0	34	G5	784.0	782.1
1	1	0	1	0	1	35	G#5	830.6	832.3
1	1	0	1	1	0	36	A5	880.0	879.3
1	1	0	1	1	1	37	A#5	932.3	931.9
1	1	1	0	0	0	38	B5	987.8	985.0
1	1	1	0	0	1	39	C6	1046.5	1044.5
1	1	1	0	1	0	3A	C#6	1108.7	1111.7
1	0	1	0	0	1	29	D6	1174.7	1179.0
1	1	1	0	1	1	3B	D#6	1244.5	1245.1
1	1	1	1	0	0	3C	E6	1318.5	1318.9
1	1	1	1	0	1	3D	F6	1396.9	1402.1
0	0	1	1	1	0	0E	F#6	1480.0	1482.2
1	1	1	1	1	0	3E	G6	1568.0	1572.0
1	0	1	1	0	0	2C	G#6	1661.2	1655.7
1	1	1	1	1	1	3F	A6	1760.0	1768.5
0	0	0	1	0	0	04	A#6	1864.7	1875.1
0	0	0	1	0	1	05	B6	1975.5	1970.0
1	0	0	1	0	1	25	C7	2093.0	2103.1
1	0	1	1	1	1	2F	C#7	2217.5	2223.3
0	0	1	1	1	0	06	D7	2349.3	2358.1
0	0	0	1	1	1	07	D#7	2489.0	2470.4

8 I²C-BUS INTERFACE

The I²C-bus is for two-way communication between different ICs or modules. It uses only two lines, a serial data line (SDA) and a serial clock line (SCL), both of which are bi-directional. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer (see Fig.7)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

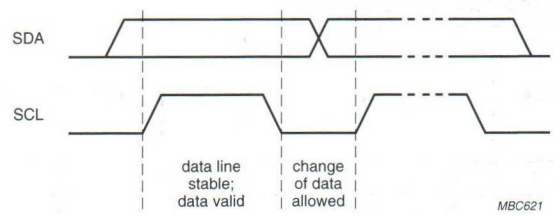


Fig.7 Bit transfer.

8.2 Start and stop conditions (see Fig.8)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

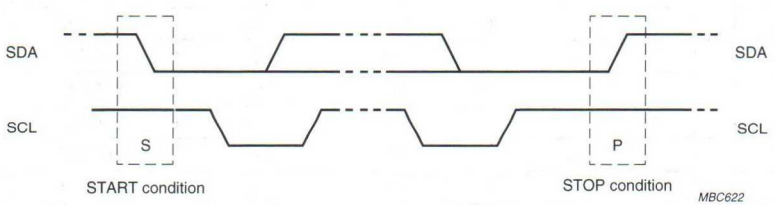


Fig.8 Start and stop conditions.

8.3 System configuration (see Fig.9)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls message transfer is the 'master' and the devices that are controlled by the master are the 'slaves'.

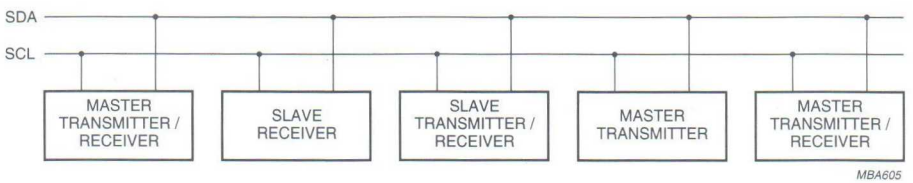


Fig.9 System configuration.

8.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge after the reception of each byte. Also a master must generate an acknowledge after reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge-related clock pulse. Set-up and hold times must be taken into account to ensure that the SDA line is stable LOW during the whole HIGH period of the acknowledge-related clock pulse. A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate the stop condition.

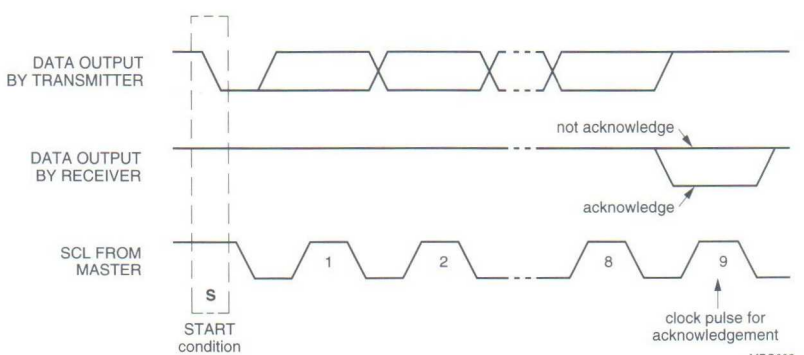


Fig.10 Acknowledgment on the I^2C-bus.

8.5 Timing specifications

The PCD3311C and PCD3312C accept data input from a microcontroller and are 'slave receivers' when operating via the I²C-bus. They support the 'standard' and 'low-speed' modes of the I²C-bus, but not the 'fast' mode detailed in *"The I²C-bus and how to use it"* document order no. 9398 393 40011. The timing requirements for the devices are described in Sections 8.5.1 and 8.5.2.

8.5.1 STANDARD MODE

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig.11, where the two signal levels are LOW = V_{IL} and HIGH = V_{IH}, see Chapter 11. Figure 12 shows a complete data transfer in standard mode. The time symbols are explained in Table 6.

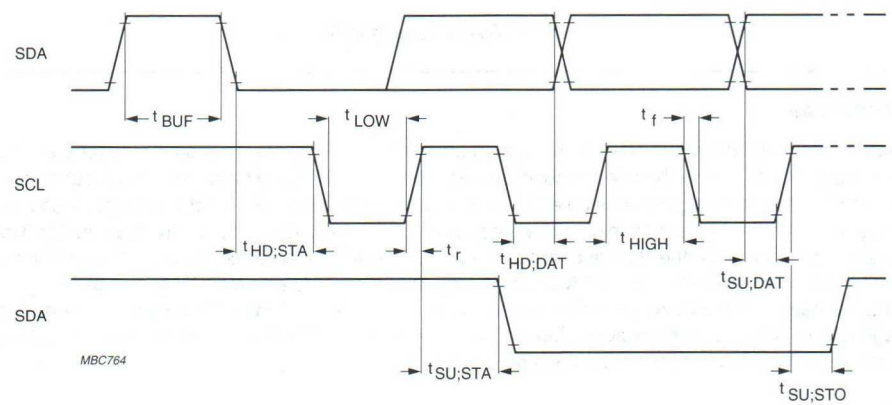
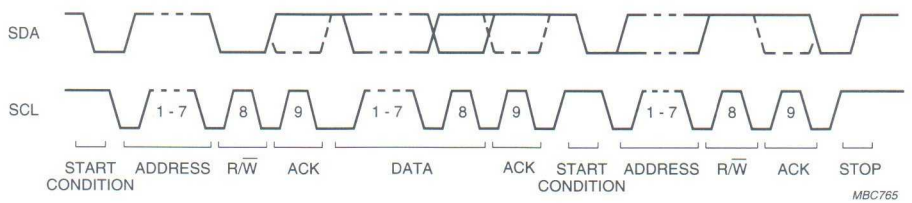


Fig.11 Standard mode timing.



Clock LOW minimum = 4.7 μs; clock HIGH minimum = 4 μs.
The dashed line is the acknowledgment of the receiver.
Mark-to-space ratio = 1 : 1 (LOW-to-HIGH).
Maximum number of bytes is unrestricted.
Premature termination of transfer is allowed by generation of STOP condition.
Acknowledge clock bit must be provided by master.

Fig.12 Complete data transfer in standard mode.

Table 6 Explanation of time symbols used in Fig.11

SYMBOL	PARAMETER	REMARKS	MIN.	MAX.	UNIT
f_{SCL}	SCL clock frequency		0	100	kHz
t_{SW}	tolerable pulse spike width		–	100	ns
t_{BUF}	bus free time	The time that the bus is free (SDA is HIGH) before a new transmission is initiated by SDA going LOW.	4.7	–	μs
$t_{SU;STA}$	set-up time repeated START	Only valid for repeated start code.	4.7	–	μs
$t_{HD;STA}$	hold time START condition	The time between SDA going LOW and the first valid negative-going transition of SCL.	4.0	–	μs
t_{LOW}	SCL LOW time	The LOW period of the SCL clock.	4.7	–	μs
t_{HIGH}	SCL HIGH time	The HIGH period of the SCL clock.	4.0	–	μs
t_r	rise time SDA and SCL		–	1.0	μs
t_f	fall time SDA and SCL		–	0.3	μs
$t_{SU;DAT}$	data set-up time		250	–	ns
$t_{HD;DAT}$	data hold time		0	–	ns
$t_{SU;STO}$	set-up time STOP condition		4.0	–	μs

8.5.2 LOW-SPEED MODE

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig.13, where the two signal levels are LOW = V_{IL} and HIGH = V_{IH}, see Chapter 11. Figure 14 shows a complete data transfer in low-speed mode.The time symbols are explained in Table 7.

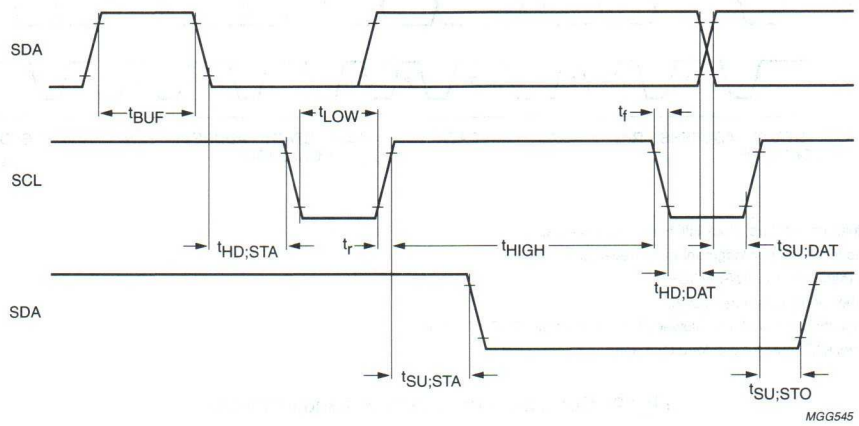
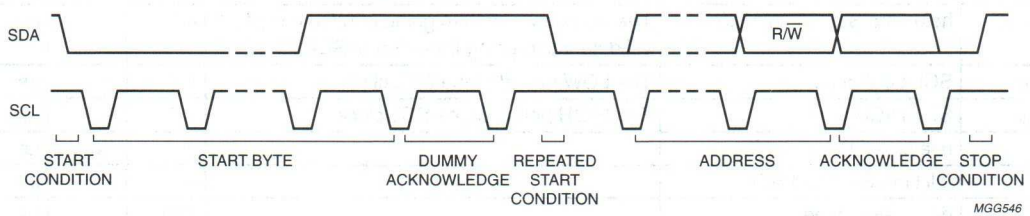


Fig.13 Low-speed mode timing.



Clock LOW minimum = 130 µs ±25 µs; clock HIGH minimum 390 µs ±25 µs.
Mark-to-space ratio = 1 : 3 (LOW-to-HIGH).
Start byte 0000 0001.
Maximum number of bytes = 6.
Premature termination of transfer not allowed.
Acknowledge clock bit must be provided by master.

Fig.14 Complete data transfer in low speed mode.

Table 7 Explanation of time symbols used in Fig.13

SYMBOL	PARAMETER	REMARKS	MIN.	MAX.	UNIT
f_{SCL}	SCL clock frequency		0	2	kHz
t_{SW}	tolerable pulse spike width		–	100	ns
t_{BUF}	bus free time	The time that the bus is free (SDA is HIGH) before a new transmission is initiated by SDA going LOW.	105	–	µs
$t_{SU;STA}$	set-up time repeated START	Only valid for repeated start code.	105	155	µs
$t_{HD;STA}$	hold time START condition	The time between SDA going LOW and the first valid negative-going transition of SCL.	365	415	µs
t_{LOW}	SCL LOW time	The LOW period of the SCL clock.	105	155	µs
t_{HIGH}	SCL HIGH time	The HIGH period of the SCL clock.	365	–	µs
t_r	rise time SDA and SCL		–	1.0	µs
t_f	fall time SDA and SCL		–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	ns
$t_{HD;DAT}$	data hold time		0	–	ns
$t_{SU;STO}$	set-up time STOP condition		105	155	µs

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handbook IC03, Section: General, Handling MOS devices"*).

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+8.0	V
V_I	all input voltages	−0.8	V_{DD} + 0.8	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	−	300	mW
P_O	power dissipation per output	−	50	mW
I_{DD}	supply current through pin V_{DD}	−50	+50	mA
I_{SS}	supply current through pin V_{SS}	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−25	+70	°C

11 CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz (g_{mL}); maximum series resistance = 50 Ω; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{DD}	operating supply voltage	2.5	−	6.0	V
I_{DD}	operating supply current (note 1)				
	no output tone	−	50	100	µA
	single output tone	−	0.5	0.8	mA
	dual output tone	−	0.6	0.9	mA
I_{stb}	static standby current (note 2)	−	−	3	µA
Inputs/outputs (SDA)					
D0 TO D5; MODE; STROBE					
V_{IL}	LOW level input voltage	0	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	$0.7V_{DD}$	−	V_{DD}	V
D2 TO D5 MODE; STROBE; A0					
I_{IL}	pull-down input current; $V_I = V_{DD}$	−30	−150	−300	nA
SCL (D0); SDA (D1)					
I_{OL}	LOW level output current (SDA); V_{OL} = 0.4 V	3	−	−	mA
f_{SCL}	SCL clock frequency	−	−	100	kHz
C_i	input capacitance; $V_I = V_{SS}$	−	−	7	pF
t_i	allowable input spike pulse width	−	−	100	ns

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
TONE output (see test circuit, Fig.15)					
$V_{HG(RMS)}$	DTMF output voltage (RMS), HIGH group	158	192	205	mV
$V_{LG(RMS)}$	DTMF output voltage (RMS), LOW group	125	150	160	mV
V_{DC}	DC voltage level	–	$\frac{1}{2} V_{DD}$	–	V
G_v	voltage gain (pre-emphasis) of group	1.85	2.10	2.35	dB
THD	Total Harmonic Distortion; T_{amb} = 25 °C				
	dual tone (note 3)	–	–25	–	dB
	modem tone (note 4)	–	–29	–	dB
$\|Z_o\|$	output impedance	–	0.1	0.5	kΩ
OSCI input					
$V_{OSC(p-p)}$	maximum allowable amplitude at OSCI	–	–	$V_{DD} - V_{SS}$	V
Timing (V_{DD} = 3 V)					
$t_{OSC(ON)}$	oscillator start-up time	–	3	–	ms
$t_{TONE(ON)}$	TONE start-up time (note 5)	–	0.5	–	ms
t_{SPW}	STROBE pulse width (note 6)	400	–	–	ns
t_{DS}	data set-up time (note 6)	150	–	–	ns
t_{DH}	data hold time (note 6)	100	–	–	ns

Notes

1. Oscillator ON; V_{DD} = 3 V; crystal connected between OSCI and OSCO; D0/SCL and D1/SDA connected via resistance of 5.6 kΩ to V_{DD}; all other pins left open.
2. As note 1, but with oscillator OFF.
3. Related to the level of the LOW group frequency component, according to CEPT recommendations.
4. Related to the level of the fundamental frequency.
5. Oscillator must be running.
6. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

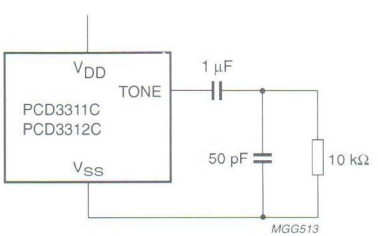


Fig.15 TONE output test circuit.

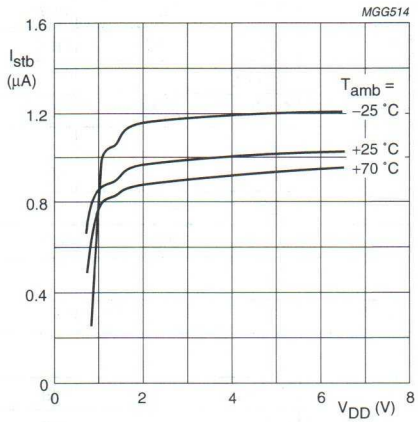


Fig.16 Standby supply current as a function of supply voltage; oscillator OFF.

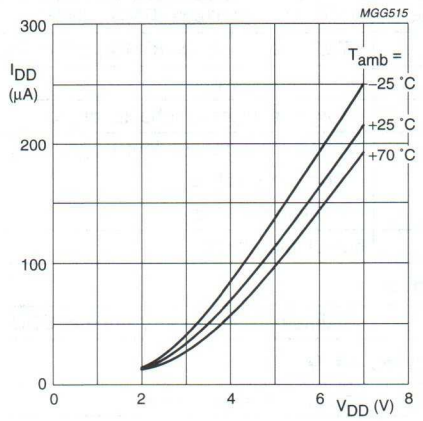


Fig.17 Operating supply current as a function of supply voltage; oscillator ON, no output at TONE.

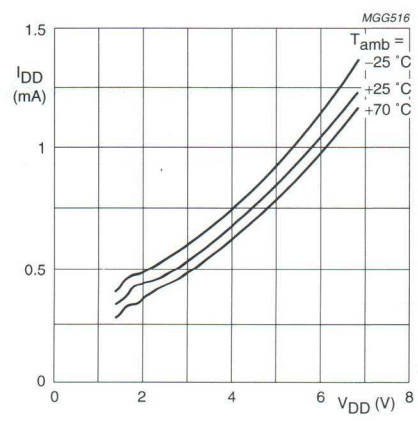


Fig.18 Operating supply current as a function of supply voltage; oscillator ON, dual tone at TONE.

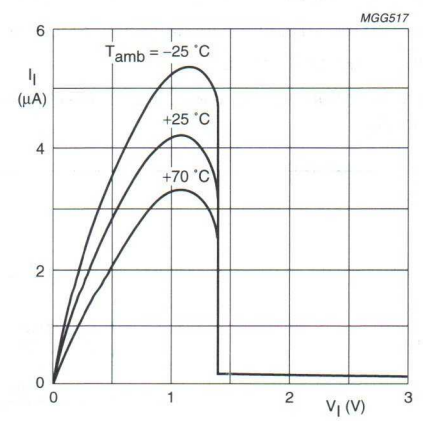


Fig.19 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

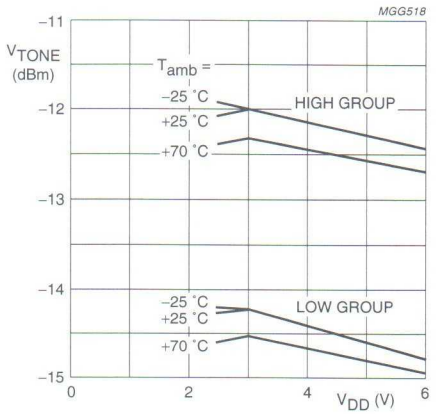


Fig.20 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

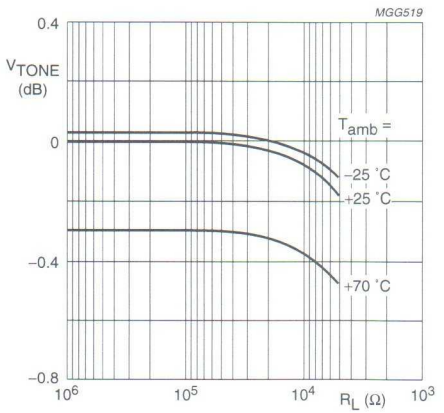


Fig.21 Dual tone output voltage level as a function of output load resistance.

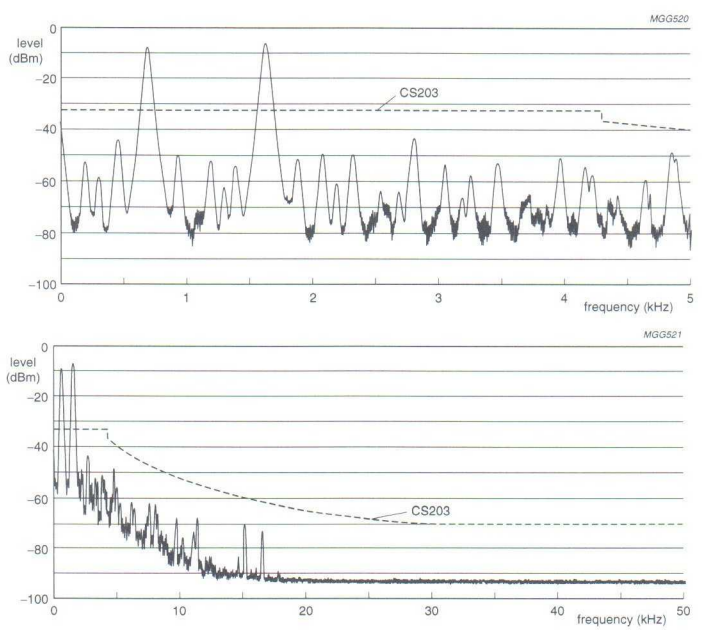


Fig.22 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

12 APPLICATION INFORMATION

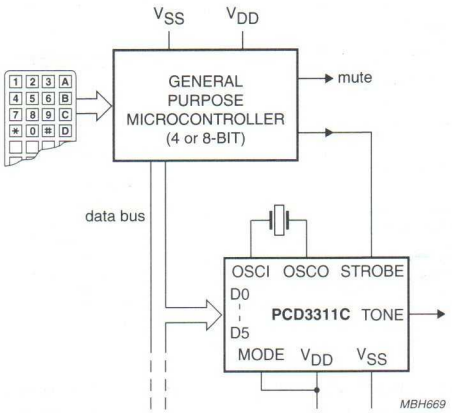


Fig.23 PCD3311C driven by microcontroller with parallel data bus.

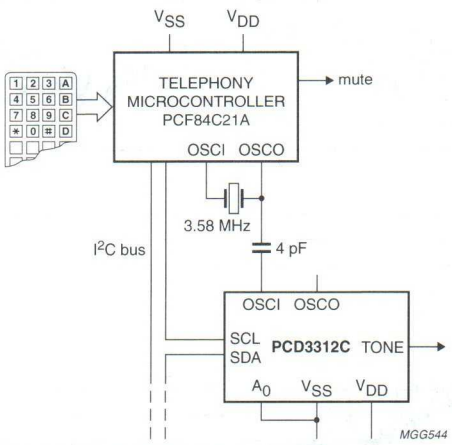


Fig.24 PCD3312C driven by microcontroller PCF84C21A. The PCF84C21A is a single-chip 8-bit microcontroller with 2 kbytes ROM and I²C-bus. The same application is possible with the PCD3311C with MODE = V_{SS}.

DSP-BASED SOLUTIONS

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Digital telephone answering machine chip PCD6002

1 FEATURES



- Excellent speech quality at average 2.6 kbit/s or 3.2 kbits/s or 5.2 kbit/s compression rate
- Excellent background noise suppression for speech quality improvement
- Speech compression rate selection: 2.6 kbit/s or 3.2 kbits/s or 5.2 kbit/s
- Speech decompression rate selection: 2.6 kbit/s, 3.2 kbit/s or 5.2 kbit/s
- Variable playback speed: 50%, 100% and 200% of real time
- Voice prompt playback
- Philips International Language Library (PILL) support tools available. Coding at 2.6 kbit/s, 3.2 kbit/s or 5.2 kbit/s
- Voice operated start message recording (VOX)
- Call progress detection by busy tone detection and programmable silence detection
- Recording time of minimum 20 minutes in 4-Mbit Flash memory (at 3.2 kbit/s)
- Excellent true full-duplex handsfree performance provided by Philips 'Phlux' algorithm
- On-hook caller ID detection according to Bell 202 and V.23 standards, as well as DTMF caller ID support
- Caller Alerting Signal (CAS) - caller ID level 2
- Dual tone generation for DTMF, melody tones and information tones
- Optional dial tone detection, and optional ringing detection using hardware Caller Identification (CID) interface
- DTMF detection (for remote control function) with local echo canceller for high reliability
- Digital volume control
- Mixed digital/analog adaptive limit and/or level control of audio input signals
- Programmable analog CODEC gain for easy interfacing
- Built-in 32-kbyte OTP (with in system programming capabilities)
- Internal 80C51 microcontroller can operate as system controller, with selectable operating frequencies between 1 and 21 MHz
- Internal 80C51 microcontroller emergency operation down to 2.0 V eliminates the need for external diallers in telephone answering machine applications
- Standard 80C51 development tools allow fast design of MMI features
- On-board Minimum Shift Keying (MSK) modem for CT0/CT1 applications
- Two integrated differential bit stream A/D converters for high quality audio input
- Two Integrated differential bit stream D/A converters for high quality audio output
- Software selectable auxiliary CODEC input channel

- 34 general purpose digital I/O lines including I²C-bus, available for connection to keyboard, display, line interface etc.
- On-chip 2-channel time multiplexed 8-bit general purpose A/D converter for e.g. parallel set detection and battery voltage measurement
- On-chip 8-bit general purpose D/A converter for e.g. speaker amplifier volume control
- Day and time stamp possibility using built-in Real Time Clock
- Flexible speech memory interface for connection of several types of speech Flash memory (serial, CAD or parallel)
- I²C master/slave bus for peripheral control or I²C-bus speech memory access
- Extensive Power Management support for battery and emergency operation, also allowing portable (voice memo) applications
- Digital IOM A/u-law interface for slave or master mode operation at various bitrates.
- Emergency operation from telephone line power only - microprocessor and DTMF generator continue to operate in this mode (< 3 mA)
- On-chip Power-on reset Circuitry
- On-chip software switchable supply voltage for electret microphone
- Single low supply voltage (2.0 V and 2.7 to 3.6 V)
- Built-in single low-frequency, low-power, crystal or ceramic resonator oscillator and on-chip PLL to reduce EMI
- Stand-alone operation with low cost PAL, NTSC and DTMF crystals
- API providing Flash memory management functions such as speech, telephone or CID data storage.

2 APPLICATION SUMMARY

The PCD6002 can be used in various applications, some of which are listed below. Refer to Chapter 18 for the corresponding outline application diagrams.

- Stand-alone digital answering machine, with handsfree
- Feature phone with integrated digital answering machine and full-duplex handsfree
- Dual-line digital answering machines
- Analog cordless applications such as CT0/1 base stations, with handsfree, and MSK modem function for RF digital data transmission
- Portable voice memo recorders
- Automotive applications - car status announcements, for example
- Low-cost desktop video conferencing
- IOM master/slave interface to connect directly to digital systems like ISDN and DECT.

2.1 Metalink emulation

Metalink emulation is possible with an OTP-less PCD6002. References to Metalink emulation in this data sheet assume this condition.

2.2 OTP Programming

Ceibo tools provide parallel programming by setmakers of application specific parameters into the OTP programming.

Additionally in system programming of the OTP memory is possible during production.

3 GENERAL DESCRIPTION

The PCD6002 integrates all the digital and analog speech management and processing functions required for a feature-phone with integrated digital answering machine, or a stand-alone digital answering machine into a single low-cost chip.

Key hardware features which give the chip distinct advantages in performance and application over competitive solutions include:

- The flexibility to change the man-machine-interface (MMI)
- An easy-to-program standard 80C51 microcontroller with 32-kbyte internal OTP memory
- High 80C51 microprocessor power for system controller functions of CT0/CT1 system control functions
- 34 general purpose I/O lines for peripheral control
- I^2C-bus interface
- Flexible Flash memory control to interface to several types of serial and parallel Flash memory
- Two integrated 16-bit bitstream audio CODECs for true full duplex handsfree operation or dual-line stand-alone answering machine operation
- Internal Digital Speech Processor (DSP) for excellent 'HARMONY' sinusoidal speech compression, decompression and variable playback speed
- Embedded DTMF detection, Call Progress Detection, Voice Operated Recording (VOX)
- High quality caller ID FSK demodulation and Caller Alerting Signal (CAS) Detection for CID Level 2
- 2-channel telephone line input for Caller ID FSK and audio interfacing

Philips provides a sophisticated API running on the internal 80C51, allowing product developers to design their MMIs quickly to suit particular applications. The API takes care of all Flash memory and DSP management tasks and can be enhanced on request.

For the pre-recorded voice prompts, the Philips International Language Library (PILL) tools are available for a standard multimedia PC platform under Windows 95. These tools provide a way to compile a range of multi-lingual voice prompts for efficient storage in the speech (Flash-) memory. The PILL tools support various languages and their grammar adaptations.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE (°C)
	NAME	DESCRIPTION	VERSION	
PCD6002H/F1	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT318-2	−25 to +70

5 BLOCK DIAGRAM

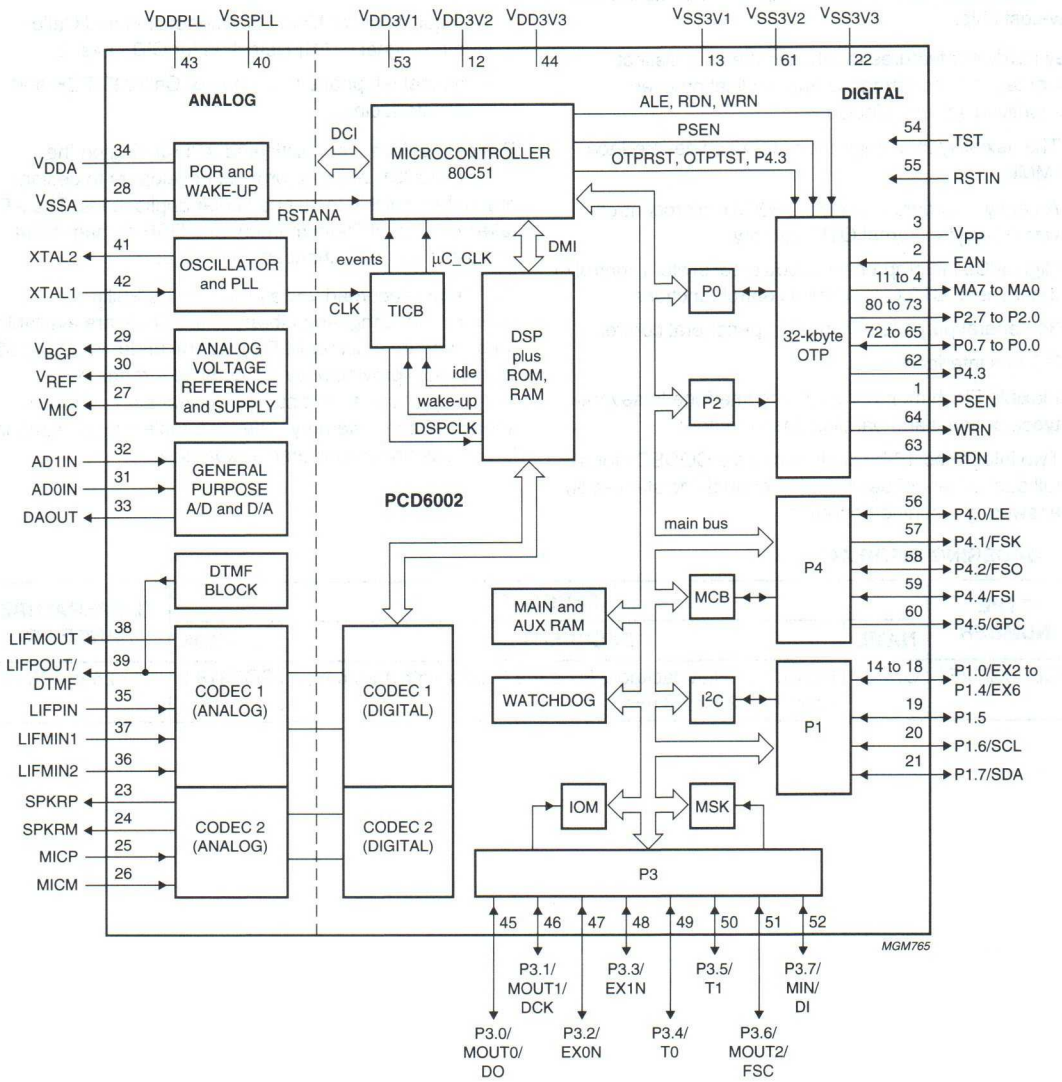


Fig.1 Block diagram.

6 PINNING INFORMATION

6.1 Pinning

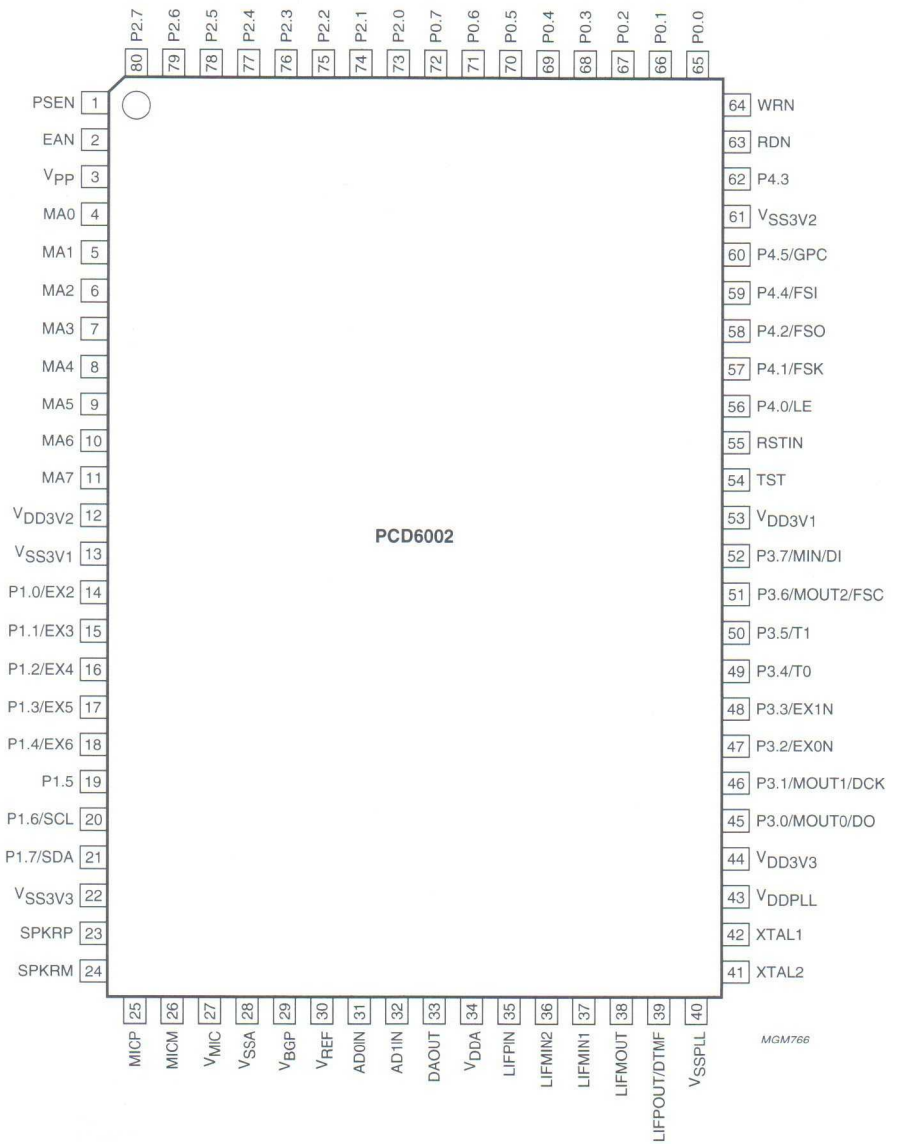


Fig.2 Pin configuration.

6.2 Pin description

SYMBOL	PIN	I/O TYPE	RESET STATE	PIN TYPE[1]	DESCRIPTION
PSEN	1	O	H	B4	Program store enable (80C51)
EAN	2	I		IBUF	80C51 External Access NOT
V_{PP}	3	Power supply			Program voltage for OTP
MA0	4	O	L	B4	General purpose output, EAN = 1; add_low, EAN = 0
MA1	5	O	L	B4	General purpose output, EAN = 1; add_low, EAN = 0
MA2	6	O	L	B4	General purpose output, EAN = 1; add_low, EAN = 0
MA3	7	O	L	B4	General purpose output, EAN = 1; add_low, EAN = 0
MA4	8	O	L	B4	General purpose output, EAN = 1; add_low, EAN = 0
MA5	9	O	L	B4	General purpose output, EAN = 1; add_low, EAN = 0
MA6	10	O	L	B4	General purpose output, EAN = 1; add_low, EAN = 0
MA7	11	O	L	B4	General purpose output, EAN = 1; add_low, EAN = 0
V_{DD3V2}	12	Power supply			Positive supply 2 (3 V) for digital circuitry
V_{SS3V1}	13	Power supply			Negative supply 1 (ground) for digital circuitry
P1.0 / EX2	14	I/O	H	BUP4SW	80C51 port pin/EX2 input
P1.1 / EX3	15	I/O	H	BUP4SW	80C51 port pin/EX3 input
P1.2/ EX4	16	I/O	H	BUP4SW	80C51 port pin/EX4 input
P1.3 / EX5	17	I/O	H	BUP4SW	80C51 port pin/EX5 input
P1.4 / EX6	18	I/O	H	BUP4SW	80C51 port pin/EX6 input
P1.5	19	I/O	H	BUP4SW	80C51 port pin
P1.6 / SCL	20	I/O	Z	BD4SCI4	80C51 port pin/I^2C-bus clock
P1.7 / SDA	21	I/O	Z	BD4SCI4	80C51 port pin/I^2C-bus data
V_{SS3V3}	22	Power supply			Negative supply 3 (ground) for digital circuitry
SPKRP	23	O	1.4 V	ANA	Positive output to speaker
SPKRM	24	O	0.7 V	ANA	Negative output to speaker
MICP	25	I	0.7V	ANA	Positive input from microphone
MICM	26	I	0.7V	ANA	Negative input from microphone
V_{MIC}	27	O	Off	ANA	Positive microphone supply voltage (+2 V)
V_{SSA}	28	Power supply			Negative supply voltage for analog circuits
V_{BGP}	29	O	1.2V	ANA	Band gap output voltage (+1.2 V)
V_{REF}	30	O	2.0V	ANA	Reference voltage (+2 V)
AD0IN	31	I	–	ANA	Analog input channel 1 for general purpose A/D converter
AD1IN	32	I	–	ANA	Analog input channel 2 for general purpose A/D converter
DAOUT	33	O	–	ANA	Analog output channel for general purpose D/A converter
V_{DDA}	34	Power supply			Positive supply (3 V) for analog circuits
LIFPIN	35	I	–	ANA	Positive analog input of LI CODEC
LIFMIN2	36	I	–	ANA	Negative analog input 2 of LI CODEC
LIFMIN1	37	I	–	ANA	Negative analog input 1 of LI CODEC
LIFMOUT	38	O	–	ANA	Negative analog output of LI CODEC

SYMBOL	PIN	I/O TYPE	RESET STATE	PIN TYPE[1]	DESCRIPTION
LIFPOUT/ DTMF	39	O	–	ANA	Positive analog output of LI CODEC or DTMF output
V_{SSPLL}	40	Power supply			Negative supply (ground) for XTAL clock and PLL circuitry
XTAL2	41	O	running	ANA	Crystal oscillator output
XTAL1	42	I	–	ANA	Crystal oscillator input
V_{DDPLL}	43	Power supply			Positive supply (3 V) for XTAL clock and PLL circuitry
V_{DD3V3}	44	Power supply			Positive supply 3 (3 V) for digital circuitry
P3.0/MOUT0 / DO	45	I/O	H	BUP4SW	80C51 port pin / MSK output 0 / IOM data output
P3.1/MOUT1 / DCK	46	I/O	H	BUP4SW	80C51 port pin / MSK output 1 / IOM DCK signal
P3.2 /EX0N	47	I/O	H	BUP4SW	80C51 port pin / EX0N input
P3.3 /EX1N	48	I/O	H	BUP4SW	80C51 port pin / EX1N input
P3.4 / T0	49	I/O	H	BUP4SW	80C51 port pin / Timer 0 input
P3.5 / T1	50	I/O	H	BUP4SW	80C51 port pin / Timer 1 input
P3.6/MOUT2 / FSC	51	I/O	H	BUP4SW	80C51 port pin / MSK output 2 IOM FSC signal
P3.7 / MIN / DI	52	I/O	H	BUP4SW	80C51 port pin / MSK input / IOM data input
V_{DD3V1}	53	Power supply			Positive supply 1 (3 V) for digital circuitry
TST	54	I	–	IBUFD	Test input
RSTIN	55	I	–	SCHMITC	Reset in
P4.0/LE	56	I/O	L	BUP4SW(OD)	General purpose I/O / LCD Enable
P4.1/FSK	57	O	Z	B8ROD	General purpose output / Flash Serial clock
P4.2/FSO	58	I/O	Z	BUP4SW(OD)	General purpose I/O / Flash Serial Out
P4.4/FSI	59	I/O	Z	BUP4SW(OD)	General purpose I/O / Flash Serial In
P4.5/GPC	60	I/O	L	BUP4SW	General purpose output / GP Clock output (crystal clock or micro clock)
V_{SS3V2}	61	Power supply			Negative supply 2 (ground) for digital circuitry
P4.3	62	O	Z	BD4SCI	5 V tolerant open-drain general purpose output port
RDN	63	O	Z	B4OD	80C51 Read NOT
WRN	64	O	Z	B4OD	80C51 Write NOT
P0.0	65	I/O	Z	BUP4A	80C51 Port 0 input/output
P0.1	66	I/O	Z	BUP4A	80C51 Port 0 input/output
P0.2	67	I/O	Z	BUP4A	80C51 Port 0 input/output
P0.3	68	I/O	Z	BUP4A	80C51 Port 0 input/output
P0.4	69	I/O	Z	BUP4A	80C51 Port 0 input/output
P0.5	70	I/O	Z	BUP4A	80C51 Port 0 input/output
P0.6	71	I/O	Z	BUP4A	80C51 Port 0 input/output
P0.7	72	I/O	Z	BUP4A	80C51 Port 0 input/output

SYMBOL	PIN	I/O TYPE	RESET STATE	PIN TYPE(1)	DESCRIPTION
P2.0	73	O	L	B4	General purpose output, EAN = 1; add_high, EAN = 0
P2.1	74	O	L	B4	General purpose output, EAN = 1; add_high, EAN = 0
P2.2	75	O	L	B4	General purpose output, EAN = 1; add_high, EAN = 0
P2.3	76	O	L	B4	General purpose output, EAN = 1; add_high, EAN = 0
P2.4	77	O	L	B4	General purpose output, EAN = 1; add_high, EAN = 0
P2.5	78	O	L	B4	General purpose output, EAN = 1; add_high, EAN = 0
P2.6	79	I/O	L	BUP4A	General purpose output, EAN = 1; add_high, EAN = 0; or input for testing purposes
P2.7	80	I/O	L	BUP4A	General purpose output, EAN = 1; add_high, EAN = 0; or input for testing purposes

Note

1. The pin type codes are explained in Section 6.3.

6.3 Pin types

6.3.1 Power supply pins

There are 6 different power supply domains (see Fig.3):

- Digital core circuits: V_{DD3V1}/V_{SS3V1}, V_{DD3V2}/V_{SS3V2} and V_{DD3V3}/V_{SS3V3}
- Program supply voltage for OTP programming: V_{PP}
- PLL circuits and crystal oscillator: V_{DDPLL} and V_{SSPLL}
- Analog circuits: V_{DDA} and V_{SSA}.

All V_{SS} pins must be connected to the same ground plane on the PCB. All V_{DD} pins must be connected to the same power supply. All V_{DD} pins have to be separately decoupled, according to Fig.36 (the application diagram).

6.3.2 Analog pins

- **ANA:** Full ESD protected analog I/O pad (double protection diode)

6.3.3 Digital pins

- **BUP4SW**: 4 mA 3 V 80C51 I/O pins, OD = configured as open-drain
- **IBUFD**: Input pad buffer, pull down
- **IBUF**: Input pad buffer
- **SCHMITC**: Input pad buffer with Schmitt trigger
- **BD4SCI**: 4 mA 5 V tolerant bidirectional open-drain output only
- **B4**: 4 mA plain output cell
- **B4OD**: 4 mA open-drain output cell
- **BUP4A**: 4 mA microport pad, analog input
- **BD4SCI4**: 4 mA bidirectional open-drain I^2C pad
- **B8ROD**: 8 mA open-drain output.

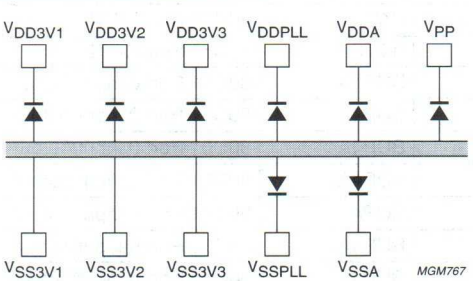


Fig.3 PCD6002 chip supply rails with protection diodes.

7 FUNCTIONAL OVERVIEW

7.1 Architecture

The PCD6002 architecture is based on an embedded 8-bit 80C51 microcontroller, a Philips 'REAL' DSP core, two high quality AD/DA CODECs and a 32-kbyte OTP microcontroller memory. Refer to the block diagram in Chapter 5.

The most important DSP peripherals are the:

- CODECs
- DSP Program ROM
- DSP RAM.
- IOM interface

The most important microcontroller peripherals are the:

- Memory Control Block (MCB)
- Watchdog
- General purpose ports
- I^2C-bus interface
- DTMF block
- MSK block (used for digital data transfer and analogue cordless applications).

The MCB, through ports P0, P2, P4 and MA (Memory Address) can interface to various types of Flash memory including serial, parallel or multiplexed command/address/data. Most of the peripherals are controlled via microcontroller Special Function Registers.

The microcontroller initializes and controls the:

- DSP via the DSP to Microcontroller Interface (DMI)
- Speech Flash memory via the Memory Control Block (MCB), and P0/P4 port pins
- Clock and power settings via the Timing and Control Block (TICB)
- Analog section via a 4-wire Digital Control Interface (DCI)

7.2 I/O summary

All digital I/O for peripherals such as keyboard, display, line interface and others is handled by the microcontroller via ports P0, P1, P3, P4, P2 and MA.

Port 2 and port MA provide 16 general purpose output-only lines (not bit-addressable, push-pull, 4 mA) to drive peripherals. These ports can be used for peripheral control if EAN is HIGH. The 4 mA driving level should be adequate to drive a low power LED directly if required.

In addition to these16 output-only lines, 16 general purpose I/O lines are provided by port 1 and port 3. Port 1 can handle 5 external interrupts (P1.0 to P1.4) that are also high/low interrupt level programmable. Port 1 also contains the I^2C-bus. Port 3 can handle an additional 2 external interrupts (P3.2, P3.3) which are active low only. The Timer 0/1 inputs are available on port 3 as for the standard 80C51. Port 1 and Port 3 are 80C51 weak pull-up I/O lines with a 4 mA sink capability, with the exception of the I^2C-bus lines P1.6, P1.7 which are open-drain. If the P3 alternate port function for the MSK modem is chosen then the standard I/O is not available on pins P3.0, P3.1, P3.6 and P3.7.

Port 4 lines are open-drain with the exception of P4.5 which will be push-pull. These open-drains can be connected via pull-up resistors to the telephone system supply or to the mains AC supply. If a Flash memory with a different supply voltage (VDD_FLASH up to 5 V) is connected, P4.3 can be pulled up to this voltage. This is required such that the CEN (Chip Enable Not) input of a Flash device is equal to VDD_FLASH to reduce the standby power consumption. All other Port 4 pins should not be pulled up to a voltage higher than VDD_DTAM.

In case a CAD Flash is used, P4.4 and P4.5 are free bit-addressable ports; P4.4 general purpose open-drain I/O, and P4.5 push-pull or open-drain output. This brings the total of I/O lines to 34.

In case an I²C LCD driver is used, P4.0, at which a latch enable (LE) function is provided for 68xx family microcontroller peripherals, is an additional free bit-addressable open-drain I/O port.

The analog interfacing for the PCD6002 consists of the analog audio I/O of the 2 CODECs and 2 additional general purpose A/D inputs and a general purpose D/A output for voltage measurement and control respectively. Furthermore a stabilized microphone supply output V_{MIC} is provided which can be switched on/off for power control.

One audio CODEC is dedicated for the PSTN line communication. This Line CODEC has a differential low ohmic analog output which consists of LIFPOUT and LIFMOUT. In case only one of the differential outputs is used, LIFPOUT should be chosen, since at this output also the emergency mode DTMF signal is available. The line CODEC has 3 inputs which are configurable as 2 single ended inputs LIFMIN1 and LIFMIN 2 that can be selected by software control, while LIFPIN is AC coupled to ground. It is also possible to use one of the LIFMIN inputs (leaving the other unconnected) in conjunction with the LIFPIN input as a differential input, in case a high CMRR is required.

The second CODEC is dedicated for a local microphone and loudspeaker connection. This Handsfree CODEC has a differential low ohmic analog output which consists of SPKRP and SPKRM. This output can be used either differential or single ended. The speaker output impedance and driving level is not suitable to directly connect a speaker. The Handsfree CODEC has a differential microphone input which consists of MICP and MICM. This differential input features a fixed microphone preamplifier of 16 dB.

Both the Line and Handsfree CODEC outputs have on-chip filtering for out of band signals such that no external filters are required.

There are 2 8-bit A/D inputs AD0IN and AD1IN for voltage measurements which can be used for parallel set detection algorithms or battery control. An 8-bit D/A converter output DAOUT can provide an analog peripheral control signal.

7.3 Overview of functional description

The detailed functional description is divided into separate chapters covering the major functional blocks, as follows:

Chapter 8, "Power supply, reset and start-up"

Chapter 9, "TICB - Generation and selection of system clocks"

Chapter 10, "The Microcontroller"

Chapter 11, "DSP I/O registers"

Chapter 12, "External memory interface"

Chapter 13, "The CODECs"

Chapter 16, "External I/O interfaces"

8 POWER SUPPLY, RESET AND START-UP

8.1 Power supply

The PCD6002 core circuitry is supplied by three 3 V supply pairs. The crystal oscillator and PLL are supplied with a separate pair of supply pins to provide a 'clean' supply voltage required for low jitter. The OTP can be programmed via the supply V_{PP} and V_{SS3V2}. The following supplies exist:

V_{DD3V1} and V_{SS3V1}: Digital Supply 1 (3 V)

V_{DD3V2} and V_{SS3V2}: Digital Supply 2 (3 V)

V_{DD3V3} and V_{SS3V3}: Digital Supply 3 (3 V)

V_{DDA} and V_{SSA}: Analog Supply (3 V)

V_{DDPLL} and V_{SSPLL}: Crystal Clock and PLL Supply (3 V)

V_{PP} and V_{SS3V2}: OTP Program supply (variable).

8.2 Reset and start-up

After applying the power supply voltage, the chip will perform a Power-on reset, responding to $V_{DDA} - V_{SSA}$. This is one of 4 possible ways to perform a reset. The following reset conditions exist:

- RSTIN, reset in from pin RSTIN
- PORST, signal from the Power-on reset circuit
- Watchdog Timer expiration
- Wake up from system off (crystal is off, but power is on) by an external interrupt.

To reduce power consumption during reset, the following reset strategy is used. The POR signal is active until V_{DDA} rises above V_{TRH} and will not become active again until V_{DDA} drops V_{HYS} below V_{TRH}. If the DSP function is not required, it can be switched off by the micro. The DSP reset will then be delayed (until it is switched on again), in order to avoid a large (reset) power consumption. Figure 4 shows the POR signal generation.

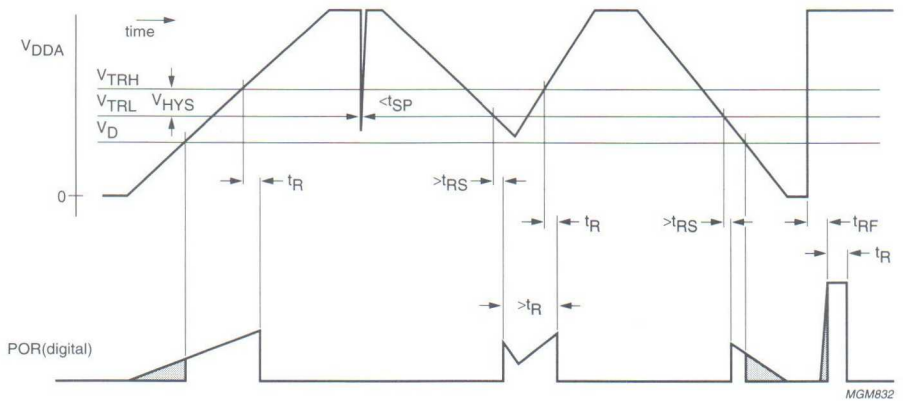


Fig.4 Power-on-reset (POR) signal generation.

9 TICB - GENERATION AND SELECTION OF SYSTEM CLOCKS

The TICB generates the clocks for all digital chip blocks, and controls the on/off switching of these blocks by using clock gating. The TICB is controlled via the microcontroller SFR registers SYMOD, CKCON and SPCON. The TICB contains:

- An input section to adapt to different input clock rates.
- A clock generation section.
- A clock selection section.
- The Real Time Clock for a 1 minute interrupt generation
- The microcontroller interrupt timers (FS_event and TIME_event) and the DSP interrupt timer (FS1) to respectively synchronize the microcontroller and DSP processes.

9.1 Microprocessor, DSP, CODEC and IOM clock generation

Figure 5 shows the TICB input section and the clock generation section.

The clock generation section contains a PLL to generate the clockrates which are higher then the input clockrate.

With the input section a wider variety of input clock frequencies can be adapted to the input frequency values needed by the PLL (3.456 MHz or 3.58 MHz). In order to save power the PLL can be switched off. This should however only be done when the chip is in the emergency mode. When switching on the PLL, it takes 50 µs (173 emergency clock periods) plus the latency of writing SYMOD (see Section 10.7) until the clock frequencies are derived from the PLL output.

Table 1 gives a description of the signals and their values for a crystal frequency of 3.456 MHz and 3.580 MHz.

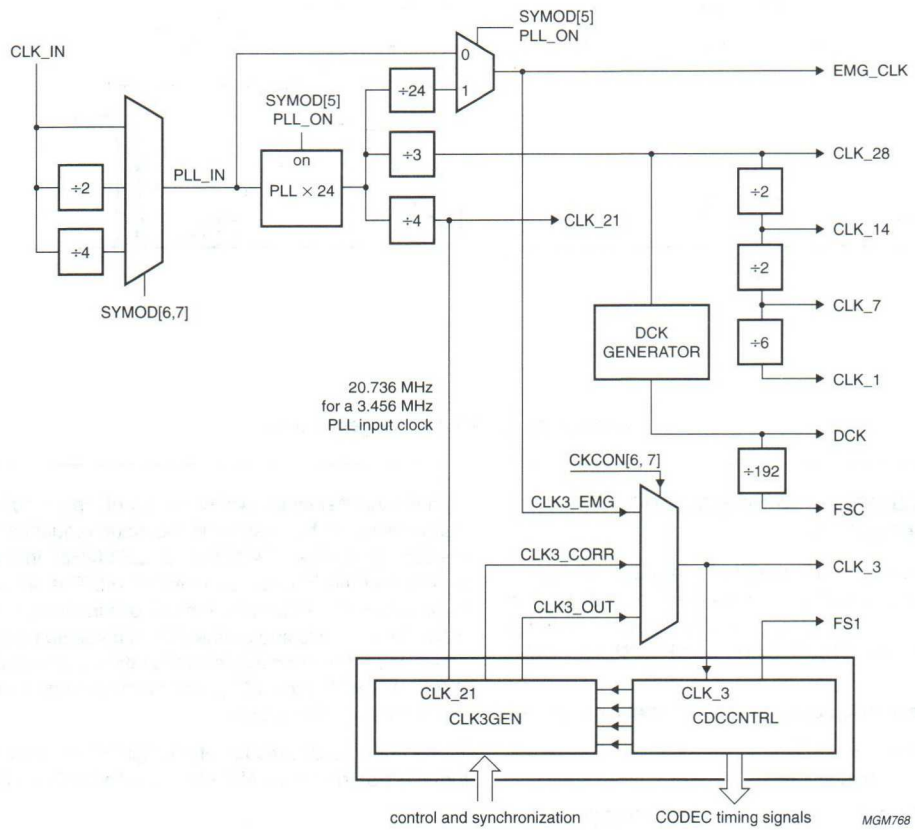


Fig.5 TICB input section and clock generation.

Table 1 Descriptions and frequency values for signals shown in Fig.5

SIGNAL	FUNCTION	VALUE (MHz)	
		PLL_IN 3.456	PLL_IN 3.580
Microprocessor and DSP clock signals			
EMG_CLK	Emergency clock	3.456	3.580
CLK_28	DSP selectable clock frequency	27.648	28.640
CLK_21	DSP and microcontroller selectable clock frequency	20.736	21.480
CLK_14	Microcontroller selectable clock frequency	13.824	14.320
CLK_7	DSP and microcontroller selectable clock frequency	6.912	7.160
CLK_1	DSP and microcontroller selectable clock frequency	1.152	1.193
CODEC clock signals			
CLK_21	Input clock for phase corrected CLK3_OUT	20.736	21.480
CLK3_EMG	EMG_CLK input to CLK_3 multiplexer	3.456	3.580
CLK3_CORR	Frequency corrected CODEC clock (24/25 × 3.58 MHz)	–	3.437[1][2]
CLK3_OUT	Phase corrected 3.456 MHz CODEC clock	3.456[1][2]	-
IOM clock/timing signals			
DCKmaster	The IOM master clock signal DCK generated by the TICB	1.536[1][3]	1.527[1][3]
FSCmaster	The IOM master frame sync FSC generated by the TICB	8 kHz[1][3]	7.955 kHz[1][3]

Notes

1. These values are only valid if the RTC mode bit CKCON.6 has been set according to the PLL_IN frequency used (see also Table 5).
2. If the IOM slave mode is activated, these clock signals are synchronized to the externally applied FSC.
3. If the IOM slave mode is activated, the externally applied DCK and FSC signals are used.

The clock generation section also contains logic to synchronize the CODEC timing signals and the DSP and micro interrupt timers to an external Frame Sync. (FSC). This synchronization is only activated when using the IOM in slave mode. If the IOM is activated in master mode, the TICB generates the DCK and FSC signals from CLK28.

Some of the clock signals can be made available as General Purpose Clock, for various peripherals needing a clock source such as an PCA1070 line interface. This GPC (General Purpose Clock) signal is an alternative output of P4.5 and can be turned on with ALTP bit 3. With ALTP bit 2, the source for GPC can be defined. The GPC source is EMG_CLK (normally 3.58 MHz) when bit 2 is logic 0 and the GPC source is µC_CLK when bit 2 is set to logic 1. The ALTP register is described in more detail in Section 16.2.

9.2 Selection of system clocks

Selection of system clocks involves:

- Selection of the crystal input clock in conjunction with PLL on/off selection (SYMOD register)
- Selection of clocks for the DSP, microcontroller and CODEC, together with microcontroller timing interrupt rates (CKCON register).
- Activation, deactivation of individual clocks or deactivation of the whole TICB in order to get an optimum power consumption (SPCON register).

Tables 2, 3 and 4 summarize the control registers and settings used for system clock selection. SYMOD is a control register in the analog section which the microcontroller accesses via the DCI. SPCON and CKCON are SFR registers in the digital section which can be directly accessed by the microcontroller.

The activation of the DSP, and the digital part of both CODECs is controlled via the SPCON Special Function Register. The clock rates of the DSP and microcontroller, and the microcontroller timing interrupt rates are set via the CKCON Special Function Register.

Figure 6 shows the multiplexers with their input and control signals for the DSP processor clock, the microcontroller clock, the CODEC clock (CLK_3) and the chip input clock frequency. Figure 6 also shows the signals affecting DIS_XTAL. The functional position of the CODEC clock multiplexer is shown in Fig.5.

Table 2 SYMOD register (C5H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Input clock 1	Input clock 0	PLL On/Off	V_{MIC} On/Off	Handsfree CODEC, Analog		Line CODEC, Analog	
				D/A (Loudspeaker) On/Off	A/D (Microphone) On/Off	D/A (To_line) On/Off[1]	A/D (From_line) On/Off

Note

1. The D/A of the Line CODEC should not be enabled at the same time as the DTMF TONE output, since there would be a conflict between the two output drivers. This would lead to a high current consumption. The DTMF TONE output is enabled with the TONE bit (DTCON.0).

Table 3 SPCON register (99H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
System off	Spare	Spare	DSP on	Handsfree CODEC, Digital		Line CODEC, Digital	
				D/A (Loudspeaker) On/Off	A/D (Microphone) On/Off	D/A (To_line) On/Off	A/D (From_line) On/Off

Table 4 CKCON register (9AH) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EMG mode	RTC mode	DSP clock 1	DSP clock 0	Micro clock 1	Micro clock 0	FS_event 1	FS_event 0

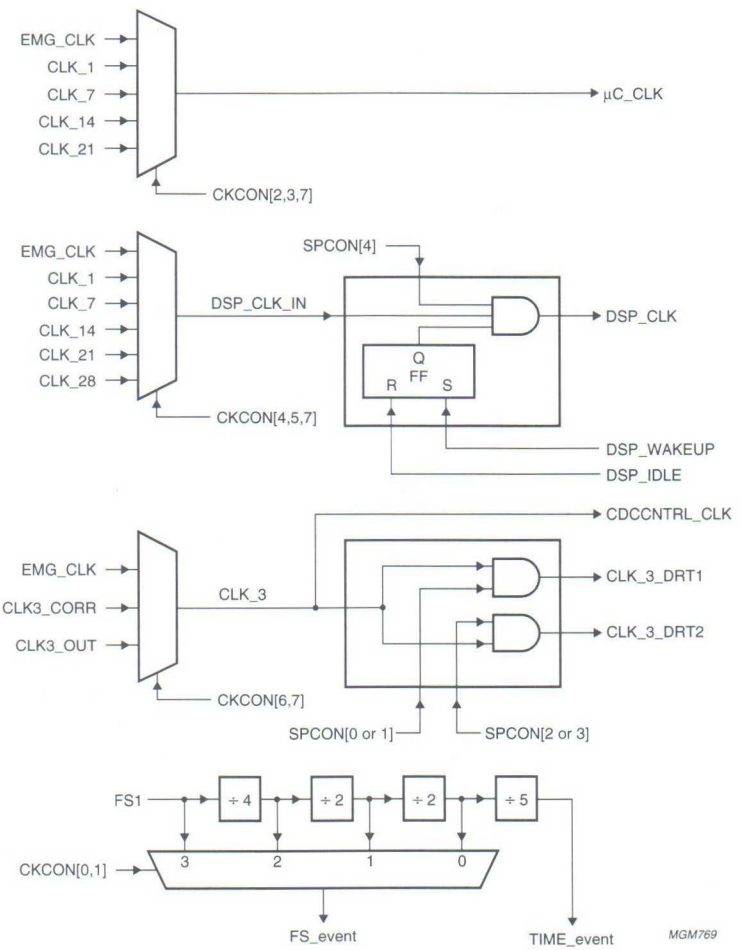


Fig.6 Clock and event rate selection.

Table 5 shows the input clock selection in the analog section of the chip. Note that for 3.456 MHz and the 3.58 MHz crystal input clock, no clock division is done prior to inputting it to the PLL. After reset the input clock division rate is per default 1. This means that application using an other input clock frequency than 3.456 or 3.580 MHz, will have to set the proper division rate, after system start-up. Otherwise proper functionality of the analog blocks is not guaranteed.

Table 5 Input clock selection.

CKCON BIT 6 RTC MODE	SYMOD BIT 7	SYMOD BIT 6	INPUT CLOCK DIVISION RATIO	CHIP INPUT CLOCK FREQUENCY (MHz)
0	0	0	1	3.456
1	0	0	1	3.580[1]
0	0	1	2	6.912
0	1	0	4	13.824

Note

1. The PCD6002 timing system is based on the 3.456 MHz (or multiples) input clock frequency. In order to be able to use the low cost 3.58 MHz crystal or ceramic resonator, a clock frequency correction is needed for some blocks (RTC, CODEC, IOM)

Table 6 shows the microcontroller clock frequencies. In emergency mode (BIT 7 of CKCON reset), the EMG_CLK is input directly to the microcontroller. The values of CKCON bits 2 and 3 are then irrelevant.

Table 6 Microcontroller clock selection

CKCON BIT 7 (EMG MODE)	CKCON BIT 3	CKCON BIT 2	SYMOD BIT 5 PLL ON	MICROCONTROLLER CLOCK FREQUENCY[1]
0	X	X	X	EMG_CLK
1	X	X	0	**DO NOT USE**[2]
1	0	0	1	CLK_1
1	0	1	1	CLK_7
1	1	0	1	CLK_14
1	1	1	1	CLK_21

Notes

1. 6 clocks/cycle.
2. **If the PLL is switched off when not in emergency mode, the selected clock would not be available. The micro would hang up. Before CKCON.7 is set to logic 1, SYMOD.5 must be set to logic 1 to activate the PLL.**

Table 7 shows the DSP clock frequency settings. Setting the DSP frequency to the correct value according to the operation mode of the DSP is done by the Application Programming Interface (API). Please refer to the API specification for more details.

Table 7 DSP clock selection

CKCON BIT 7 (EMG MODE)	CKCON BIT 5	CKCON BIT 4	SYMOD BIT 5 PLL ON	DSP CLOCK FREQUENCY
0	X	X	X	EMG_CLK
1	X	X	0	no clock active
1	0	0	1	CLK_1
1	0	1	1	CLK_7
1	1	0	1	CLK_21
1	1	1	1	CLK_28

Table 8 shows CLK_3 selection (CLK3_SEL according to Fig.5). The selection depends on the type of crystal which is connected (determined by RTC Mode setting according to Table 5). The setting of CKCON [6,7], thus determine the selection of the CLK_3 source (see Table 1 and Fig.5). If CKCON[7] = 0 - to denote emergency mode - CLK_3 will be derived from the EMG_CLK, as shown in the following tables.

Table 8 CODEC clock selection

CKCON BIT 7 (EMG MODE)	CKCON BIT 6 (RTC MODE)	CLK_3 SOURCE
0	X	EMG_CLK
1	1	CLK3_CORR
1	0	CLK3_OUT(1)

Note

1. CLK3GEN is only active if in this mode and phase correction is required **and** CLK_21 is available.

The TICB provides two periodic outputs to the microcontroller: FS_event and TIME_event. FS_event is programmable to 4 different rates. Both outputs are derived from and therefore synchronized to FS1. The outputs are connected to an interrupt input of the microcontroller and called 'Time_event Interrupt' and 'FS_event Interrupt' respectively. The selection of the FS_event interrupt rate is done via the CKCON SFR register see Section 9.2. Figure 9 shows the generation of these interrupts. Table 9 shows the selection of the FS_event rate. The FS1 clock is provided by the CDCCNTRL block shown in Fig.5.

Table 9 FS_event rate selection

CKCON BIT 1	CKCON BIT 0	FS_event INTERRUPT RATE		
0	0	FS1/16	500 Hz	2 ms
0	1	FS1/8	1 kHz	1 ms
1	0	FS1/4	2 kHz	500 µs
1	1	FS1	8 kHz	125 µs

9.3 Real Time Clock generation

The Real Time Clock (RTC) divider provides a 1 minute timing signal which is available as an interrupt to the microcontroller. The RTC_CLK input clock is always active, whether the PLL is active or not. Thus the complete chip can be set into power-down mode (but not system-off mode), where the microcontroller can be woken up by the RTC to maintain the values for date and time. The RTC_CLK is directly derived from the EMG_CLK input clock signal.

Figure 7 shows the RTC clock generation. To divide a 3.456 MHz or a 3.580 MHz clock into a 1 minute RTC signal a 28 bit counter is required to count $60 \times 3.456 \times 10^6$ clock periods. To determine the number of most significant bits of this counter required for an accurate RTC, the maximum allowed time deviation per month and the crystal accuracy need to be taken into account. The LSB of the 28 counter has an accuracy of $1/(60 \times 3.456 \times 10^6) = 0.005$ parts-per-million (ppm). Since a normal crystal accuracy is about 10 ppm it is tolerable to have only the 17 MSB of the counter available (10/0.005 = 2000, which implies that the 11LSB can be disregarded), as shown in Fig.7.

If one month is set to $30 \times 24 \times 60 \times 60 = 2.6 \times 106$ seconds, 10 ppm deviation equals 26 seconds per month or about 5 minutes per year, which is tolerable.

Since there are 2 possible RTC_CLK values, 3.580 MHz and 3.456 MHz, there are 2 comparators selectable for the RTC; COMP_3.580 and COMP_3.456. The nominal value of these comparators are (11 LSB are set to logic 0):

COMP_3.580: CCD2800H (RTCON = A5H)
COMP_3.456: C5C1000H (RTCON = 82H)

In Section 9.2 the conditions for the RTC_MODE signal are described.To allow connection of various crystals or ceramic resonators, as well as to provide adjustment of the RTC clock according to the crystal tolerance, 8 of the 17 most significant bits of the comparators are programmable via the SFR register RTCON. The binary values of the comparators are then as shown in Table 10.

Since the accuracy of Q11 is 10 ppm, with the adjustment of the RTC via RTCON an accuracy of ±5 ppm can be achieved. For an RTC pulse every 1 minute the outer limits of the crystal frequency inputs which can be connected are:

COMP_3.580

Maximum: CCFF800H → 3.582600 MHz;

Minimum: CC80000H → 3.573897 MHz.

COMP_3.456

Maximum: C5FF800H → 3.460267 MHz;

Minimum: CC80000H → 3.451563 MHz.

The default value of RTCON for an input frequency 3.58 MHz is A5H and for an input frequency of 3.456 MHz is 82H.

Table 10 Comparator contents

	Q27									Q18							Q11
COMP_3.580:	1	1	0	0	1	1	0	0	1	x	x	x	x	x	x	x	x
COMP_3.456:	1	1	0	0	0	1	0	1	1	x	x	x	x	x	x	x	x
										Bit7			**<-- RTCON -->**				**Bit0**

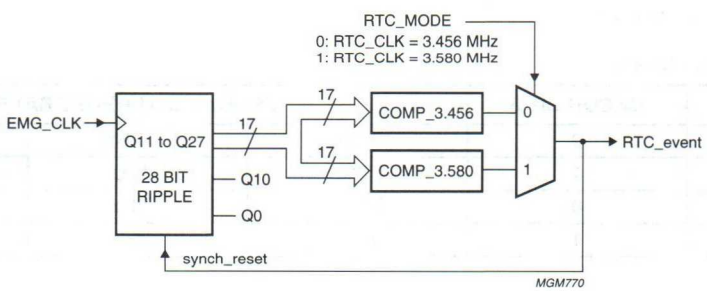


Fig.7 Real Time Clock (RTC) generation.

10 THE MICROCONTROLLER

The embedded μCMS 80C51 microcontroller controls the DTAM chip by means of Special Function Registers (SFRs). SFRs are defined for the blocks MCB, TICB, DCI, PCON, DSP, I²C, P1/3/4, MA and MSK. All of these (except PCON - Power Control) are shown in the block diagram, Fig.1. The architecture of the microcontroller itself and the interface to these blocks will be described in this chapter.

10.1 Microcontroller architecture

The microcontroller architecture and its environment is shown in Fig.8.

The microcontroller has some application-specific peripherals such as I²C-bus, Watchdog (WD), P1, P3, P4, MCB and the SFRs of the DSP block, the TICB and the DCI block.

All these functions and SFRs are located in the application specific function block (ASF), see Fig.8.

The 80C51 core contains the 80C51 standard functions such as Timer 0, Timer 1 and Power Down/IDLE states and a 15-vector dual-level interrupt controller INT15L2. Moreover the microcontroller contains the Metalink Enhanced Hooks protocol which enables Metalink emulation via ALE, PSEN, EAN, P0 and P2. The external program memory access is done via the standard ports P0 and P2. Connection of external Flash memory is done via the P4, P0 and P2 I/O pads. The microcontroller clock driver (CD) has no clock divider, which means that. the microcontroller operates on 6 μC_CLK clocks per machine cycle.

The 80C51 has a few basic modes of operation: RESET, NORMAL, METALINK, TEST (various), IDLE and PD. Entering the METALINK mode can be done via inputs ALE, PSEN_N, EA_N and P2.0 to P2.2 during a reset.

The IDLE mode can be entered by setting the IDLE bit in PCON. Leaving the IDLE mode can be done via the master reset (MRST), any external interrupt, a DSP_event, TIME_event or RTC_event, Timer 0, Timer 1 or I²C-bus interrupt; if these interrupts are enabled.

The PD mode can be entered by setting the PD bit in PCON. The power down logic of the microcontroller will turn all micro clocks off. The TIME_event, DSP_event, RTC_event and EX2 to EX6 are mixed with EX0 (see Fig.11) and therefore make use of the standard wake-up circuitry of the 80C51. These interrupts should be active for more than 6 clocks (read, modify, write of IRQ1 takes 1 instruction) to guarantee the interrupt for the micro.

Setting the PD bit of PCON after setting the system-off bit of SPCON, will trigger the analog section to turn off the oscillator and therefore the whole chip. Wake-up from system-off can be done via a RST_IN, POR or an external interrupt EX0 to EX6, if the EX0 or EX1 interrupt is enabled. A wake-up from system-off will always reset the PCD6002. The EX interrupt condition should last more than 4096 + 64 + 4 clocks to be sure that the interrupt is handled when entering the NORMAL mode. If the interrupt is shorter the microcontroller will only enter the NORMAL mode after the reset is gone.

10.2 Memory mapping

The memory map of the 80C51 is shown in Fig.9. In addition to all the SFRs, the microcontroller has 128 bytes of directly addressable (DATA) memory, 128 bytes of indirectly addressable (IDATA) memory and 512 bytes of AUX RAM – the on-chip 'MOVX' addressable (XDATA) memory. On-chip XDATA memory access can be disabled by setting the ARD bit in PCON to logic 1. Via ports P0, P2 and P4 it is possible to access up to 512 kbytes of external speech data memory stored in a parallel Flash memory. A CAD Flash memory can also be mapped in this area. A serial (SPI or Microwire compatible) Flash memory can be connected to P4 which is controlled by the MCB. Up to 64 kbytes of program (CODE) memory can be connected to the P0, P2 and PSEN pads. This can be the INTERNAL 32-kbyte OTP if EAN is set to logic 1 or any external program memory (like the MON51 target debug ROM) if EAN is logic 0. The OTP control registers can only be accessed if P4.3 is logic 1.

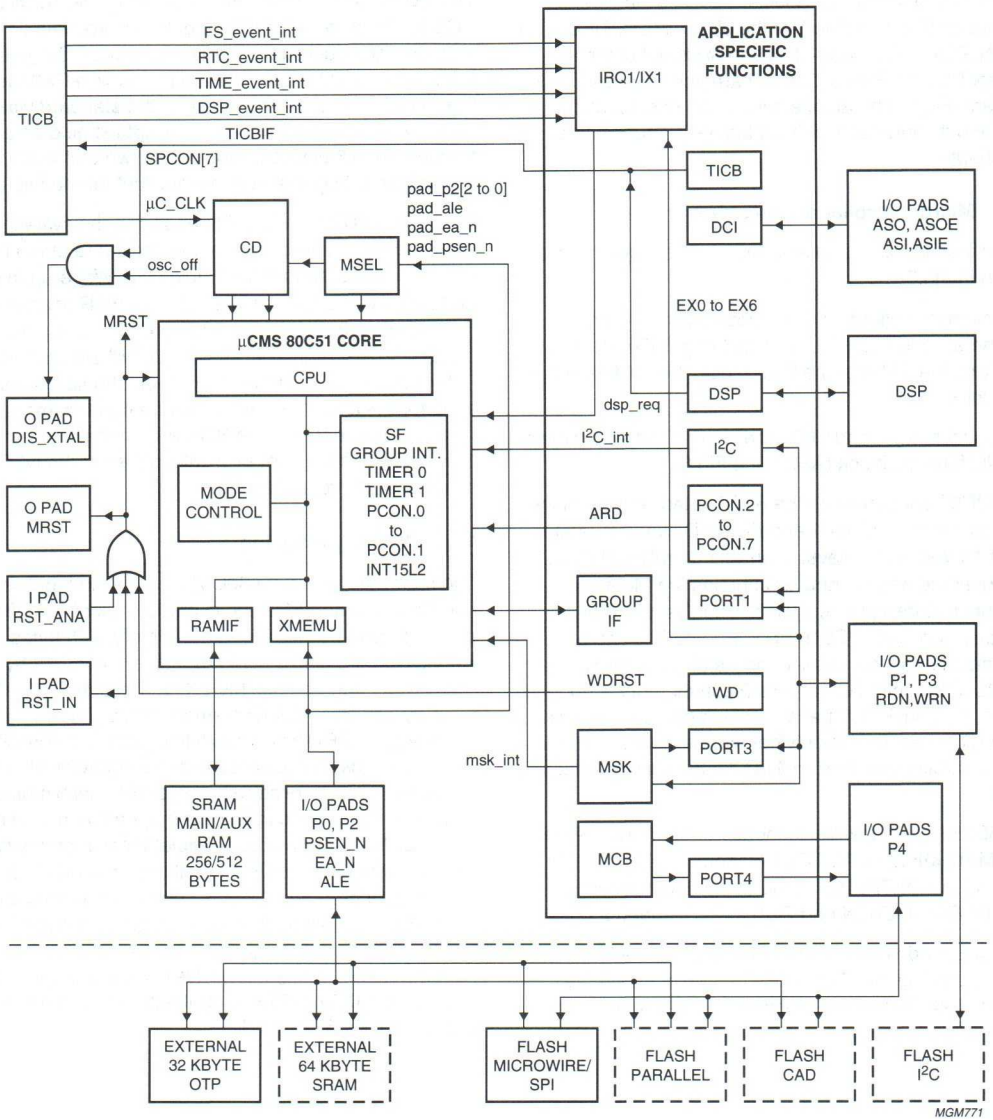


Fig.8 Microcontroller (µCMS 80C51) architecture and environment.

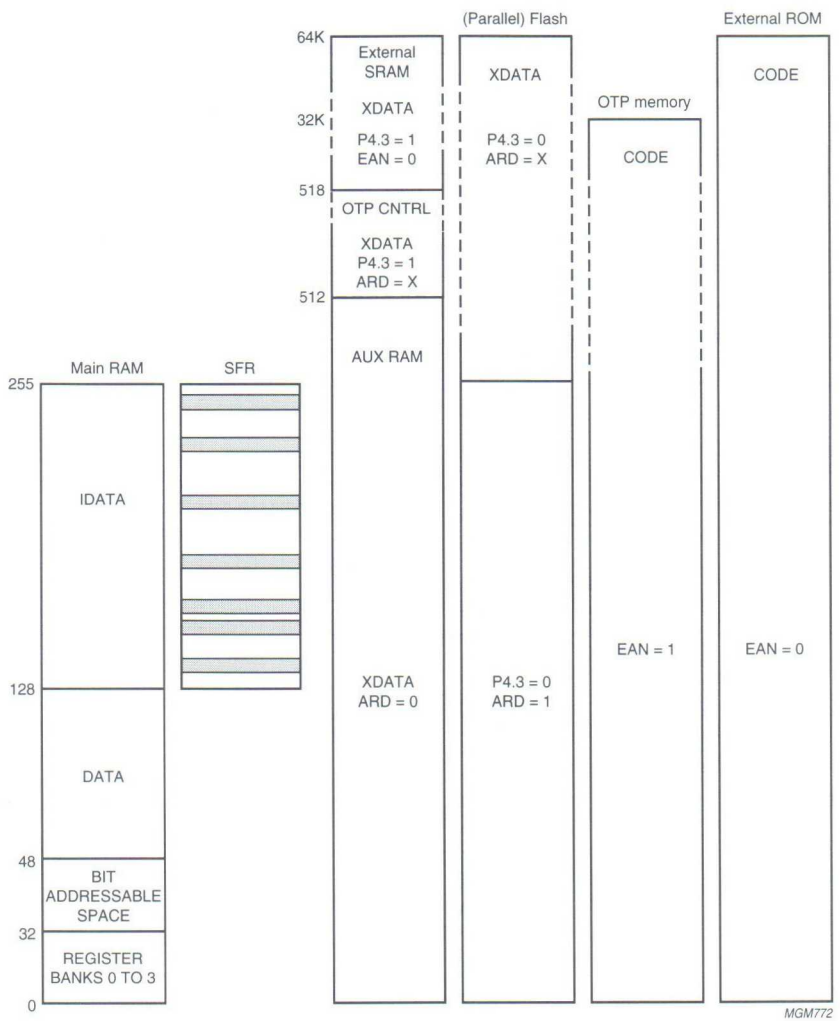


Fig.9 Microcontroller memory map.

10.3 SFR mapping

The SFR mapping for the microcontroller is shown in Table 11. All SFRs together with their reset states are described in Table 12.

Table 11 SFR mapping

SFR ADDRESS (HEX)	SPECIAL FUNCTION REGISTERS - 8 BYTES EACH							
	SEE NOTE 1	ONLY BYTE ADDRESSABLE						
F8 to FF	IP1[2]	–	–	–	–	–	–	WDT[2]
F0 to F7	B[2]	–	–	–	–	–	–	WDTKEY
E8 to EF	IEN1[2]	IX1	–	–	–	–	–	–
E0 to E7	ACC[2]	–	–	–	–	–	–	–
D8 to DF	S1CON[2]	S1STA[2][3]	S1DAT[2]	S1ADR[2]	–	–	–	–
D0 to D7	PSW[2]	–	–	–	–	–	–	–
C8 to CF	MCON	MBUF	MSTAT		–	–	–	–
C0 to C7	IRQ1	INTC	GPADR	GPADC[4]	GPDAR[4]	SYMOD[4]	DHGF[4]	DTCON[4]
B8 to BF	IP0[2]	XWUD	VREFR[4]	CDVC1[4]	CDVC2[4]	CODTR[4]	DLGF[4]	–
B0 to B7	P3[2]	–	–	–	–	–	–	–
A8 to AF	IEN0[2]	MCSC	MCSD	ALTP	–	–	–	–
A0 to A7	–		DTM0[3]	DTM1[3]	DTM2[3]	MTD0	MTD1	MTD2
98 to 9F	P4	SPCON	CKCON	RTCON	–	–	–	–
90 to 97	P1[2]	–	–	–	–	–	–	–
88 to 8F	TCON[2]	TMOD[2]	TL0[2]	TL1[2]	TH0[2]	TH1[2]	–	–
80 to 87	–	SP[2]	DPL[2]	DPH[2]	–	–	–	PCON

Notes

1. SFRs in this column are both bit and byte-addressable.
2. Complies to 80C51 family architecture specification.
3. Read only. (All other SFRs are read/write.)
4. Control register of the analog section. Rewriting these SFRs during the latency period described in Section 10.7 is forbidden.

Table 12 Microcontroller register list

NAME	ADDRESS (HEX)	DESCRIPTION	RESET STATE[1]
ACC	E0	Accumulator	0000 0000
ALTP	AB	LE and GPC control	X000 0000
A		Accumulator	0000 0000
B	F0	B register for multiply, divide or scratch	0000 0000
CKCON	9A	Clock Control register	0000 0000
CDVC1	BB	CODEC Digital Volume Control for CODEC1	0000 0000
CDVC2	BC	CODEC Digital Volume Control for CODEC2	0000 0000
CODTR	BD	CODEC test register	0000 0000
DLGF	BE	DTMF Low Group Frequency	0000 0000
DHGF	C6	DTMF Low Group Frequency	0000 0000
DTCON	C7	DTMF Control register	0000 0000
DPL	82	Data Pointer Low	0000 0111
DPH	83	Data Pointer High	0000 0000
DTM0	A2	DSP To microcontroller communication register 0	0000 0000
DTM1	A3	DSP To microcontroller communication register 1	0000 0000
DTM2	A4	DSP To microcontroller communication register 2	0000 0000
GPADC	C3	Channel Select bit, Request/Confirm bit, V offset	XXXX X000
GPADR	C2	Digital value of analog input	0000 0000
GPDAR	C4	Digital value of analog output	1000 0000
IEN0	A8	Interrupt Enable register 0	000X 0000
IEN1	E8	Interrupt Enable register 1	0000 0000
INTC	C1	INTerrupt Control register	XXXX XX00
IP0	B8	Interrupt Priority register 0	X000 0000
IP1	F8	Interrupt Priority register 1	0000 0000
IRQ1	C0	Interrupt Request flag register	0000 0000
IX1	E9	Interrupt Polarity register	XXX0 0000
MCSD	AA	Memory Control Serial Data register	0000 0000
MCSC	A9	Memory Control Serial Command register	0000 0000
MTD0	A5	microcontroller to DSP communication register 0	0000 0000
MTD1	A6	microcontroller to DSP communication register 1	0000 0000
MTD2	A7	microcontroller to DSP communication register 2	0000 0000
MCON	C8	MSK Control register	0000 0000
MBUF	C9	MSK data Buffer register	XXXX XXXX
MSTAT	CA	MSK status register	XX00 0000
P1	90	General Purpose Digital I/O	1111 1111
P3	B0	General Purpose Digital I/O	1111 1111
P4	98	P4 can be used to control Flash memory	XX01 1110
PCON	87	Power and interrupt control register	X000 0000
PSW	D0	Program Status Word	0000 0000

NAME	ADDRESS (HEX)	DESCRIPTION	RESET STATE[1]
RTCON	9B	Real Time Clock control	0000 0000
S1CON	D8	I^2C Serial Control register	0000 0000
S1ADR	DB	I^2C Own Slave Address register	0000 0000
S1DAT	DA	I^2C Data Shift register	0000 0000
S1STA	D9	I^2C Status register	1111 1000
SYMOD	C5	analog SYstem MODe control	0000 0000
SPCON	99	System Power and Clock Configuration	0000 0000
SP	81	Stack Pointer	0000 0000
TCON	88	Timer/Counter Control register	0000 0000
TMOD	89	Timer/Counter Mode Control register	0000 0000
TL0	90	Timer Low register 0	0000 0000
TL1	91	Timer Low register 1	0000 0000
TH0	92	Timer High register 0	0000 0000
TH1	93	Timer High register 1	0000 0000
VREFR	BA	Voltage Reference register	1001 1010
WDT	FF	Watchdog timer	0000 0000
WDTKEY	F7	Watchdog key register	0000 0000
XWUD	B9	eXternal WakeUp Disable	0000 0000

Note

1. All SFR bits with a reset state with an 'X' are spare but have a flip-flop in this position with reset state '0'.

10.4 Microcontroller interrupts

The microcontroller has 15 interrupt sources which can be programmed to have a low or high priority:

- EX2 to EX6 asynchronous external interrupts via P1.0 to P1.4
- EX0, EX1 asynchronous external interrupts via P3.2 (INT0N) and P3.3 (INT1N)
- DSP_event
- FS_event
- TIME_event
- I^2C interrupt
- RTC_event
- Timer 0 and Timer 1 interrupt
- MSK interrupt.

If enabled these interrupts sources result in jump to the addresses shown in Table 13.

Table 13 Allocation of interrupt sources

VECTOR	SOURCE	NUMBER(1)	PRIORITY(2)	DESCRIPTION	IENx/IPx
0003	EX0	0	1	External interrupt 0	IEN0.0/IP0.0
000B	T0	1	4	Timer 0 interrupt	IEN0.1/IP0.1
0013	EX1	2	7	External interrupt 1	IEN0.2/IP0.2
001B	T1	3	10	Timer 1 interrupt	IEN0.3/IP0.3
0023	MSK_event	4	13	MSK RI or TI interrupt	IEN0.4/IP0.4
002B	TIME_event	5	2	TIME interrupt	IEN0.5/IP0.5
0033	FS_event	6	5	FS interrupt	IEN0.6/IP0.6
003B	EX2	7	8	External interrupt 2	IEN1.0/IP1.0
0043	EX3	8	11	External interrupt 3	IEN1.1/IP1.1
004B	EX4	9	14	External interrupt 4	IEN1.2/IP1.2
0053	EX5	10	3	External interrupt 5	IEN1.3/IP1.3
005B	EX6	11	6	External interrupt 6	IEN1.4/IP1.4
0063	I^2C	12	9	I^2C interrupt	IEN1.5/IP1.5
006B	DSP_event	13	12	DSP interrupt	IEN1.6/IP1.6
0073	RTC_event	14	15	RTC interrupt	IEN1.7/IP1.7

Notes

1. For some C-compilers '1' has to be added to this number.
2. The interrupt controller supports up to 15 interrupt sources, each with a 2-level (high or low) priority. A high priority interrupt is always serviced before a low priority interrupt, but within the high and low levels, interrupts are serviced in the order shown in this column.

The external interrupt configuration of P1 is shown in Fig.10. Pins P1.5, P1.6 and P1.7 cannot be used as external interrupts. The IX1 SFR determines the polarity of the external interrupt sources of P1. Clearing the EA bit in IEN0 disables all interrupt sources. Using IEN0 (and IEN1) each individual external interrupt can be enabled or disabled.

The IRQ1 SFR stores all external interrupts. So if an external interrupt with a low priority is detected during execution of another (high or low priority) interrupt it will be handled just after the return of this interrupt. The interrupt service routine for an external interrupt must clear the right IRQ1 flag to indicate that it has serviced the interrupt request. Notice that during the interrupt routine this flag can be set again immediately after clearing the IRQ1 flag if the interrupt source is (still) HIGH.

The complete interrupt system is shown in Fig.11. All 15 interrupts are allocated and can be given a low or high priority according to the setting of IP0 and IP1.

Each interrupt source can be individually enabled by means of IEN0 and IEN1.

The IRQ1 and IX.7 registers are clocked (a clock which is active during IDLE) and can be set by P1.0 to P1.4, the TIME_event, the DSP_event, the FS_event and the RTC_event. These flags can only be cleared by software. Only TCON.1, TCON.3, TCON.5 and TCON.7 flags are cleared by the interrupt controller hardware. All other flags must be cleared by software.

The polling of a potential interrupt goes from a high priority to a low priority interrupt. Within a high (or low) priority interrupt level the EX0 (if set to high priority) will be polled first followed by the next high priority interrupt.

The interrupt SFRs IP0, IP1, IEN0, IEN1, IRQ1 and IX1 (described previously) are defined in Tables 14 to 19. A flag set to logic 1 in IP0 or IP1 (Tables 14 and 15) causes the corresponding interrupt to have high priority.

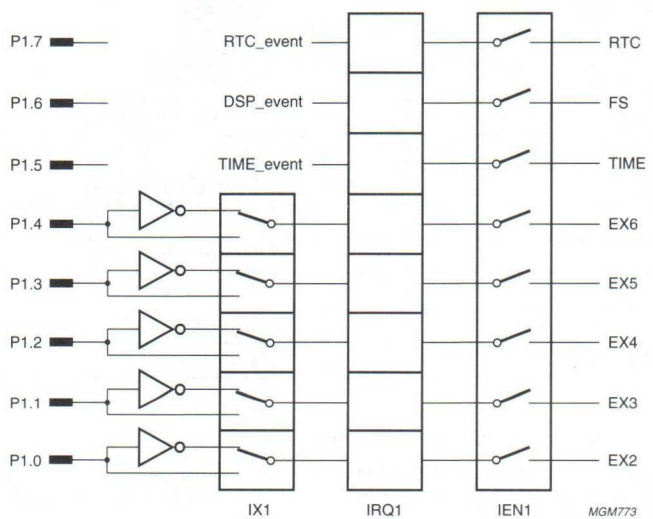


Fig.10 PCD6002 Port 1 external interrupt configuration.

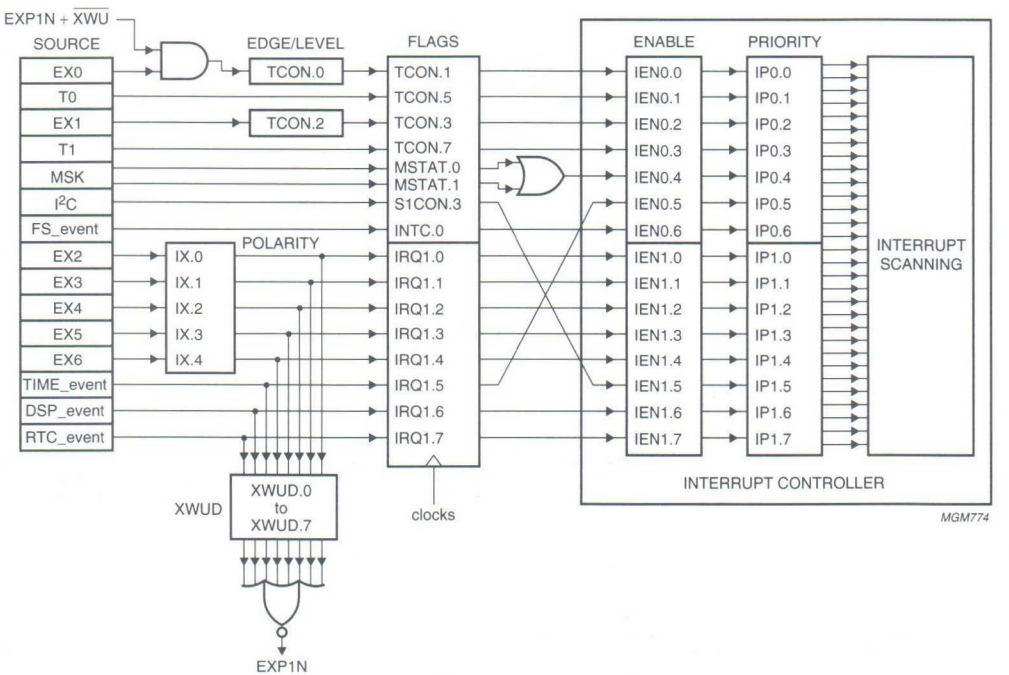


Fig.11 PCD6002/80C51 interrupt system.

Table 14 IP0 (B8H) bit assignment, reset state X0000000B

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Spare	Priority FS_event	Priority TIME	Priority MSK	Priority T1	Priority EX1	Priority T0	Priority EX0

Table 15 IP1 (F8H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Priority RTC	Priority DSP	Priority I²C	Priority EX6	Priority EX5	Priority EX4	Priority EX3	Priority EX2

Table 16 IEN0 (A8H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Global Enable	Enable FS_event	Enable TIME	Enable MSK_event	Enable T1	Enable EX1	Enable T0	Enable EX0

Table 17 IEN1 (E8H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Enable RTC	Enable DSP	Enable I^2C	Enable EX6	Enable EX5	Enable EX4	Enable EX3	Enable EX2

Table 18 IRQ1 (C0H) bit assignment, reset state 00H; note 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RTC Flag	DSP Flag	TIME Flag	EX6 Flag	EX5 Flag	EX4 Flag	EX3 Flag	EX2 Flag

Note

1. The flags of IRQ1 will be set to logic 1 by hardware if the interrupt occurs. They must be cleared by software in the interrupt service routine.

Table 19 IX1 (E9H) bit assignment, reset state 00H; note 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Spare	Spare	Spare	Polarity EX6	Polarity EX5	Polarity EX4	Polarity EX3	Polarity EX2

Note

1. A polarity bit set to logic 1 in IX1 will cause the external interrupt to be active 'HIGH'.

Table 20 INTC (C1H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Spare	Spare	Spare	Spare	Spare	Spare	eXtended Wake-Up	FS Flag

Table 21 XWUD (B9H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RTC XWU Disable	DSP XWU Disable	TIME XWU Disable	EX6 XWU Disable	EX5 XWU Disable	EX4 XWU Disable	EX3 XWU Disable	EX2 XWU Disable

10.5 Interface to DSP

The DSP to microcontroller interface (DMI) can be used for the following purposes:

- Transferring compressed speech data from microcontroller to DSP
- Transferring compressed speech data from DSP to microcontroller
- Transferring DSP parameters (DSP mode, tone frequency etc.) from microcontroller (API) to the DSP
- Transferring DSP events (Caller ID, Ring Detect, VOX, Call Progress etc.) to the microcontroller

The microcontroller and the DSP can communicate by means of 6 SFRs (MTD0/1/2 and DTM0/1/2) and 4 DSP IO registers (DTMC, DTMD, MTDC and MTDD), see Fig.12. The DTMC and MTDC registers are used for communication and control and the DTMD and MTDD registers for transferring data.

The MT (Micro Transmit), DR (DSP receive) and DT (DSP Transmit), MR (Micro Receive) ensure that either the old data is read or new data is read although the DSP and microcontroller operate on different clocks. This can be achieved by means of simple handshake circuitry in either direction. The DR state machine ensures that the DSP will never read new MTDC control data and old MTDD speech data. In order to guarantee proper transitions of the DR state machine the DSP always has to read the DTMC first and afterwards the DTMD IO register.

The TICB generates the DSP_event interrupt when it receives a dsp_uc_req signal. The dsp_uc_req cannot be generated by the microcontroller because the dsp_event interrupt must be able to wake up the microcontroller from PD.

MTD0/1/2 are written by the microcontroller. After each write to MTD0 the contents of MTD0/1/2 are transferred to the 16 bit register MTDD and the 8-bit register MTDC (the MSB is set to 00H), which can be read by the DSP via the DSP I/O bus. In this way the DSP always receives a valid control byte and a valid 16-bit data word. **If MTD0 is written while the DSP is turned off the MTD0 value will be transferred to the MTDC IO-register as soon as the DSP is turned on.**

The MTDC and MTDD registers are continuously and immediately read by the DSP after every FS1 interrupt. The microcontroller can write a new word to MTD0/1/2 but has to wait for at least 125 µs to be sure that the DSP has read the previous value.

DTM0/1/2 are read by the microcontroller as SFRs. The contents of the DTMD and DTMC registers are transferred to the DTM0/1/2 SFRs when the DSP writes the DTMC register. At this time an interrupt signal called DSP_event is generated to the microcontroller, which triggers the microcontroller to read the DTM0/1/2 SFRs. In this way DSP events and speech data can be transferred easily to the microcontroller. The DSP will transfer a maximum of 3 bytes - one command byte and two data bytes, for example - every 125 µs to the microcontroller. Thus one write to DTMC takes place every 125 µs.

Similarly, the microcontroller can transfer a maximum of 3 bytes every 125 µs to the DSP. Thus one write to MTD0 takes place every 125 µs. The default rate for the FS_event interrupt will be FS1/8 resulting in a data transfer rate of 10 words every 10 ms which equals 16 kbit/s. In case a higher rate is needed the FS_event interrupt rate can be switched to FS1/4.

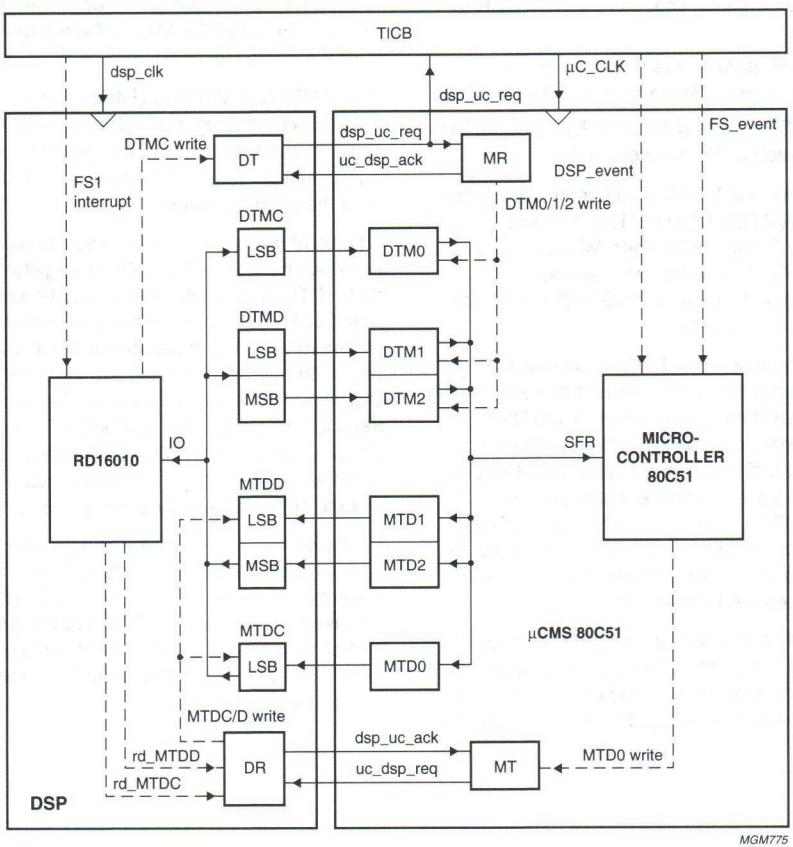


Fig.12 DSP to microcontroller interface (DMI).

10.6 Interface to Real Time Clock (RTC)

When the RTC_event interrupt is enabled in IEN1 and the EA bit in IEN0 is set the microcontroller will get an RTC_event interrupt every 1 minute. The RTC interrupt service routine must clear the RTC flag. The RTC_event interrupt will also wake up the microcontroller when it is in the PD or in the IDLE state. Under power saving conditions this will allow the user to switch off the microcontroller and still maintain an accurate real time clock.

10.7 Interface to the analog section

The analog section is controlled by the microcontroller by means of the 10 SFRs, listed below. The value of the GPADR register is defined by the analog section and can be read by the microcontroller as an SFR. The SFRs which are copied from digital section to analog section are:

- SYMOD
- GPADC
- GPDAR
- RVREF
- CDVC1
- CDVC2
- CODTR
- DLGF
- DHGF
- DTCON

Due to the implementation of the analog section, it takes 15 emergency clock periods until a change of the SFR value is seen by the analog section. If the SFR is written a second time during this period, the value seen by the analog section will be corrupted.

When multiple analog control SFRs are written shortly after each other the latency of the individual bytes adds up. This can lead to a 120 emergency clock periods long latency, during which rewriting of the SFRs is forbidden.

10.8 Interface to the Memory Control Block (MCB)

The MCB is a 3-wire serial interface designed to interface with a versatile range of serial Flash memories (both Microwire and SPI mode 0/3 compatible slave devices) in parallel with program OTP/external ROM and even external data SRAM.

The 3-wire serial interface is consisting of a serial data output (FSO) serial data input (FSI) and a serial clock signal (FSK). FSK, FSO and FSI are alternative functions of the general purpose I/O pins P4.1, P4.2 and P4.4. The serial interface is controlled via the MCSC and MCSD Special Function Registers. The FSK and FSO outputs are both open-drain and must be pulled to 3 V with external resistors R_{FSK} and R_{FSO}. The recommended value for both resistors at high FSK speeds (> 1 MHz) is 1 kΩ.
The MCSC SFR is defined in Table 22.

Turning the MCB on by setting bit MCSC.3, will switch the FSK and FSO pins to logic 0. A write to MCSD will generate the appropriate FSK/FSO signal. A read from MCSD will only generate 8 FSK pulses and will shift-in the next byte. The shifting and the FSK/FSO signal can be suppressed by setting bit 2 of MCSC. This can be used for reading the last byte out of the serial Flash memory during a read sequence. The FSK shift off operation however is not necessary if the MCB is already turned off when reading the MCSD SFR for the last time.

If a serial Flash memory is chosen the FSK master clock rate can be selected with bits 0 and 1, as shown in Table 23. The MCB is always master, which means that the FSK clock is always generated by the PCD6002.

Data coming from or going to the serial Flash memory can be accessed by means of the MCSD SFR. This is simply an 8-bit serial shift register. The first FSO and FSI bits are always the most significant bit of MCSD. The first read of the MCSD SFR will only serially load the MCSD SFR with valid data. Therefore the first read operation must always be followed with another read operation which reads the actual received data out of the MCSD SFR.

The serial shifting of bits into and out of MCSD is done at the same moment: 1 microcontroller clock before the falling edge of FSK (= t_{SF}). When the FSK speed is programmed at the highest speed (μC_CLK/4) this shifting will be done in the middle of the FSK high level time. The most time-critical situation is when FSK is only 2 clocks wide and has a frequency of 3.5 MHz (14 MHz/4). In this case make sure that $t_{r(FSK)}$, which can be controlled by the value of R_{FSK}, is greater than the hold time requirement of the slave device.

Fig.13 describes how a Microwire compatible device can be accessed with an FSK speed of µC_CLK/4. A SPI mode 0/3 device requires an additional FSK clock falling edge to trigger the slave device to generate valid data on the FSI line. The SPI mode 3 can be achieved by starting with FSK HIGH when the device is turned on (turn MCB on after asserting the chip enable of the slave device) and by ending with FSK. The SPI mode 0 can be achieved by generating an additional FSK pulse (by turning the MCB off and on again, see figure) between the last write to MCSD and the first read of MCSD.

A variety of serial Flash memory driver software packages is included in the API software for the microcontroller that is provided with the chip.

Table 22 MCSC (A9H) bit assignment

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Spare	Spare	Spare	Spare	MCB On	Shift off	FSK Rate 1	FSK Rate 0

Table 23 FSK clock rate

MCSC BIT 1	MCSC BIT 0	FSK CLOCK RATE
0	0	µC_CLK/4
0	1	µC_CLK/8
1	0	µC_CLK/16
1	1	µC_CLK/32

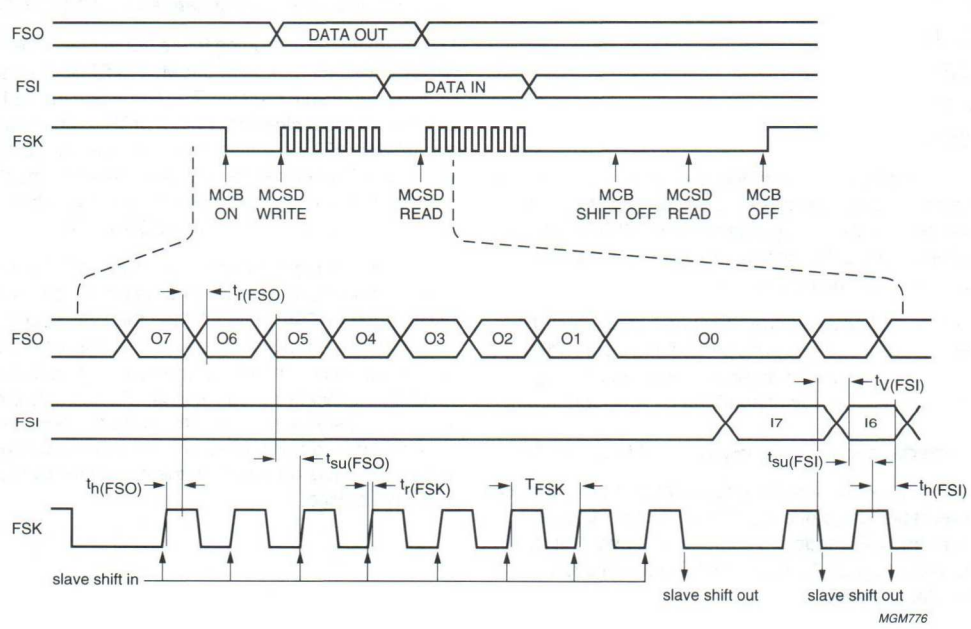


Fig.13 MCB timing for a Microwire compatible device

Table 24 MCB timing

SYMBOL	PARAMETER	VALUE
T_{FSK}	FSK period	$N \times t_{micro_clock}$[1]
$t_{su(FSO)}$	FSO setup time with respect to the rising edge of FSK	$(N/2 + 1) \times t_{micro_clock} - t_{r(FSO)}$
$t_{h(FSO)}$	FSO hold time with respect to the rising edge of FSK	$(N/2 - 1) \times t_{micro_clock} - t_{r(FSK)}$
$t_{r(FSK)}$	FSK rise time	note 2
$t_{r(FSO)}$	FSO rise time	note 2
$t_{su(FSI)}$	FSI setup time with respect to the internal shift clock	$(N/2 - 1) \times t_{micro_clock} - t_{V(FSI)}$
$t_{h(FSI)}$	FSI hold time with respect to the internal shift clock	$> t_{micro_clock}$
$t_{V(FSI)}$	FSI valid time with respect to the falling edge of FSK	depending on the used Flash memory

Notes

1. N depends on the chosen FSK clock rate and can be 4, 8, 16, 32.
2. The rise time of FSK and FSO depends on the externally connected pull-up resistor and the capacitive load.

10.8.1 Parallel Flash interface

If a parallel (4-Mbit) Flash memory is chosen Table 25 is valid.

Table 25 Using P4 with 4-Mbit parallel Flash memory

P4.2	P4.1	P4.0	ADDRESS
0	0	0	Bank 0, 00000H to 0FFFFH
0	0	1	Bank 1, 10000H to 1FFFFH
0	1	0	Bank 2, 20000H to 2FFFFH
0	1	1	Bank 3, 30000H to 3FFFFH
1	0	0	Bank 4, 40000H to 4FFFFH
1	0	1	Bank 5, 50000H to 5FFFFH
1	1	0	Bank 6, 60000H to 6FFFFH
1	1	1	Bank 7, 70000H to 7FFFFH

Since parallel Flash memory has a much larger addressing range than the 64 kbytes addressing capability of the 80CL51, additional addressing is done by means of the P4 SFR and the P4 I/O pad. The P4 SFR is connected to port P4 as shown in Table 26.

One pin is necessary to enable and disable the Flash memory to reduce power consumption. Four pins of P4 are necessary to connect various types of Flash memories:

- A parallel Flash: P4.0 to P4.2, P4.3, RDN and WRN are connected to MA[16:18], CEN, OEN and WN
- A serial Flash: FSO, FSI, FSC and P4.3 are connected to DI, DO, SK and CEN pins
- A CAD Flash: P4.1 to P4.3, RDN, WRN are connected to CLE, ALE, CEN, REN and WEN pins.

RDN and WRN are available as separate pins. If an access is done to the AUX RAM (ARD bit of PCON equals logic 1) the RDN and WRN will be logic 1 on these pins.

Bits 1, 2 and 4 of port 4 are set to FSI, FSK and FSO when a serial Flash is selected in the MCSC SFR.

The P4 SFR is defined in Table 27. Bits P4.6 and P4.7 are not available as chip port pins. These bits can however be used as bit-addressable general purpose bits.

Table 26 P4 port pin behaviour

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Spare	Spare	P4.5/GPC	P4.4/FSI	P4.3	P4.2/FSO	P4.1/FSK	P4.0/LE

Table 27 P4 (98H) bit assignment

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0

10.9 The test register CODTR

The Special Function Register CODTR can put the DSP or the digital parts of the CODECs into various test modes. In these test modes normal operation is not guaranteed any more. The output behaviour of P3.0, P3.1, P3.2, P3.3 and P3.4 can be changed and the DSP test modes can lead to a higher current consumption and to malfunction of the DSP. Therefore changing the value of this register should be avoided.

10.10 Interface to Timing and Control Block (TICB)

The interface to the TICB consists of the Special Function Registers SPCON, CKCON and RTCON and the signals µC_CLK_EN, µC_CLK, FS_event, Time_event and RTC_event. The signals are described in Section 10.1.

10.11 The PCON Special Function Register

Table 28 PCON (87H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Spare	ARD	spare	WLE/EW	GF1	GF0	PD	IDL

Bits 0 and 1 of PCON can be set to logic 1 to put the microcontroller into the IDLE or PD state. In the IDLE state the functions Timer 0/1 and the I^2C controller are still clocked. The CPU status along with all SFRs, Main RAM and AUX RAM registers are preserved. Leaving the IDLE state can be done by any enabled interrupt or reset. The microcontroller hardware will clear the IDLE flag and start executing the interrupt. When the interrupt is serviced (RETI instruction) the microcontroller will execute the next instruction following the instruction that put the microcontroller in the IDLE state.

In the PD state the clock of the entire microcontroller with its peripherals is off. The CPU status along with all SFRs, Main RAM and AUX RAM registers are preserved. Leaving the PD state can be done by any active enabled interrupt source or reset.

The microcontroller hardware will clear the PD flag and start executing the interrupt. When the interrupt is serviced (RETI instruction) the microcontroller will execute the instruction following the instruction that put the microcontroller in the PD state.

Bits 2 and 3 of PCON are general purpose flags. Bit 4 is used to enable the (load of) the Watchdog timer. The Watchdog function is explained in the next paragraph.

The ARD bit is used to disable the access of a MOVX instruction to the 512 bytes of the AUX RAM. If ARD is set to logic 1 a MOVX operation can access the lower 512 bytes of the external memory. The upper part of the external memory can always be accessed independently of the setting of the ARD bit.

10.12 The Watchdog circuitry

The purpose of the Watchdog is to reset the microcontroller if it enters erroneous states caused by EMI or bugs in the software that cannot be detected or eliminated.

When enabled the Watchdog circuitry will generate a reset if the user program fails to reload the Watchdog timer within a specified length of time known as the Watchdog interval.

The Watchdog interval is determined by the following equation: $T_{WD} = (256 - WDT) \times \frac{12287}{\mu C_CLK}$

The programmer should implement the following protocol:

1. Write the key value 55H to the WDTKEY SFR to disable the Watchdog.
2. Set the WLE/EW bit to logic 1 to initially enable the Watchdog. WLE/EW now functions as a WLE bit. Only a reset can clear the EW bit.
3. Enable the Watchdog timer by writing a value not equal to 55H to the WDTKEY SFR. This is only necessary if the previous value of the WDTKEY register was 55H. The value after reset is 00H
4. Enable the load of the WDT SFR by setting the WLE bit to logic 1.
5. Load the Watchdog interval by writing the required value into the WDT SFR. After the load the WLE bit is set to logic 0 again by the Watchdog hardware. The value of WDT is 00H after reset
6. Write a value not equal to 55H to the WDTKEY SFR to enable the Watchdog
7. Repeat steps 4 and 5 in the user software before the Watchdog timer expires

Note that in metalink emulation mode the Watchdog cannot be used and that the Watchdog reset will reset the entire chip.

10.13 I²C-bus

The serial port I²C-bus is a simple bidirectional 2-wire bus for efficient inter-IC data exchange. The I²C-bus consists of a data line (SDA) and a clock line (SCL). These lines also function as I/O port P1.7 and P1.6 respectively. The system is unique because data transport, clock generation, address recognition and bus arbitration are all controlled by hardware. The I²C-bus serial I/O has complete autonomy in byte handling and supports all four I²C operating modes:

- Master transmitter
- Master receiver
- Slave transmitter
- Slave receiver.

The I²C block contains 4 SFR registers. The mode of operation is controlled by the S1CON register. S1STA is the status register whose contents may also be used as a vector to various service routines. S1DAT is the data shift register and S1ADR is the slave address register. Slave address recognition is performed by hardware.

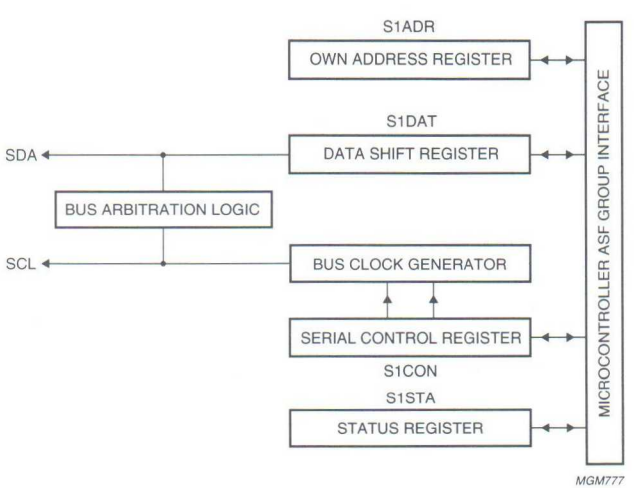


Fig.14 I²C-bus serial I/O.

10.13.1 Special Function Register S1CON (D8H)

Refer to Tables 29 and 30. Two bits are affected by the SIO1 hardware, the SI bit is set to logic 1 when a serial interrupt is requested, and the STO bit is set to logic 0 (cleared) when a STOP condition is present on the I^2C-bus. The STO bit is also cleared when ENS1 = 0. When the SIO1 is in the master mode the serial clock frequency is determined by the clock rate bits CR2, CR1 and CR0.

Table 29 Serial control register S1CON

BITS	SYMBOL	DESCRIPTION
7	CR2	Determines together with CR1 and CR0 the SCL bit rate, see Table 30.
6	ENS1	When this bit is set to logic 0 the SIO1 is disabled, outputs SDA and SCL are in high impedance state, and P1.6 and P1.7 function as open-drain ports. With this bit set to logic 1 the SIO1 is enabled. The P1.6 and P1.7 port latched must be set to logic 1.
5	STA	Start flag. When the STA bit is set to logic 1 in slave mode, the SIO1 hardware checks the status of the I^2C-bus and generates a start condition if the bus is free. If STA is set to logic 1 while the SIO1 is in master mode, SIO1 transmits a repeat START condition.
4	STO	Stop flag. With this bit set to logic 1 while in master mode a STOP condition is generated. When a STOP condition is detected on the bus, the SIO1 hardware clears the STO flag. In the slave mode, the STO flag may also be set to logic 1 to recover from an error condition. In this case no STOP condition is transmitted to the I^2C-bus. However, the SIO1 hardware behaves as if a STOP condition has been received and releases SDA and SCL. The SIO1 then switches to the "not addressed" receiver mode. The STO flag is automatically cleared by hardware.
3	SI	SIO1 interrupt flag. When this flag is set to logic 1, an acknowledge is returned after any one of the following conditions: • a start condition is generated in master mode • own slave address received during AA = 1 • general call address received while S1ADR[0] = 1and AA = 1 • data byte received or transmitted in master mode (even if arbitration is lost • data byte received or transmitted as selected slave • stop or start condition received as selected slave receiver or transmitter.
2	AA	Assert Acknowledge. When set to logic 1 an acknowledge will be returned during the acknowledge clock pulse on SCL when: • own slave address is received • general call address is received while S1ADR[0] = 1 • data byte is received while device is a selected slave. With AA = 0 no acknowledge will be returned. Consequently, no interrupt is requested when the "own slave address" or general call address is received.
1, 0	CR1, CR0	Together with CR2 these bits determine the serial clock frequency when SIO1 is in master mode. See also Table 30.

Table 30 I²C-bus bit frequencies in master mode

CR2	CR1	CR0	$f_{\mu C_CLK}$ DIVIDED BY	I²C-BUS BIT FREQUENCY (kHz) AT $f_{\mu C_CLK}$				
				0.9 MHz	3.58 MHz	7.16 MHz	14.32 MHz	21 MHz
0	0	0	10	90	358	–	–	–
0	0	1	20	45	179	358	–	–
0	1	0	30	30	119	239	–	–
0	1	1	40	22	90	179	358	–
1	0	0	80	11	45	89.5	179	269
1	0	1	120	7.5	30	59.7	119	179
1	1	0	160	5.6	22	44.8	89.5	134
1	1	1	–	–	–	–	–	–

Note that any I²C device tolerates a maximum and sometimes a minimum SCL frequency. The right setting of bits CR2, CR1 and CR0 using a specific microcontroller clock frequency is therefore important.

10.13.2 Special Function Register S1STA (D9H)

Refer to Table 31. The Status register S1STA is an 8-bit read-only register. Its contents may be used as a vector to a service routine. This optimizes the response time of the software and consequently the I²C-bus.

Table 31 Status register S1STA (reset state 0xF8)

BITS	SYMBOL	DESCRIPTION
7, 6, 5, 4, 3	SC4, SC3, SC2, SC1, SC0	Contains the status code defined by the I²C protocol
2, 1, 0	–	Not used, all bits are 0

10.13.3 Special Function Register S1DAT(DAH)

Refer to Table 32. The Data shift register S1DAT contains the serial data to be transmitted or data that has just been received. Bit 7 is transmitted or received first.

Table 32 Status register S1DAT (reset state 0x00)

BITS	SYMBOL	DESCRIPTION
7 to 0	Bit 7 to 0	I²C-bus serial data

10.13.4 Special Function Register S1ADR (DBH)

Refer to Table 33. This 8-bit "own address register" may be loaded with the 7-bit address to which the controller will respond when programmed as a slave receiver/transmitter. The LSB bit GC is used to determine whether the general CALL address is recognized.

Table 33 Status register S1ADR (reset state 0x00)

BITS	SYMBOL	DESCRIPTION
7 to 1	Address	Own I²C-bus address
0	GC	0: General CALL address is not recognized 1: General CALL address is recognized

10.14 MSK modem.

The MSK modem is used for in-band signalling between handset and base in analog cordless telephone systems CT0, CT1 and CT1+. The MSK modem's receiver and transmitter can be enabled separately. Receive and transmit interrupts can wake-up the microcontroller during its power saving idle mode. The baud rates are programmable between 1200 and 4800 baud. Fig.15 shows the functional diagram of the MSK modem.

The min input is the alternative input of P3.7 and MOUT[2:0] is the alternative output of P3.0, P3.1 and P3.6. The Rx and Tx mute can be done in software by any pin of MA, P1, P3 and P2. The mti and mri interrupts are OR-ed together to a single interrupt called msk_int. So the msk_in interrupt handler should investigate the status of the MRI and MTI bit in the MCON SFR.

The MOUT[2:0] outputs and the min input are alternative functions of P3.0, P3.1, P3.6 and P3.7. The MOUT[2:0] outputs are "111" when the MSK transmitter is disabled (default after reset). So P3.0, P3.1, P3.6 and P3.7 can still be used as general purpose I/O ports. Setting bit 7 of MSTAT will invert the min polarity.

The modem has the following features:

- Full duplex operation via 8-bit parallel interface
- The message is fully manchester.
- Automatic detection of 16 bit manchester preamble pattern
- The last received 4 bits of the preamble pattern are programmable
- Receiver full, transmitter empty indication bits.
- Manchester coding and decoding for clock recovery and early error detection
- Programmable input polarity
- Baud rate selection from 1200, 2400, 3600, 4800 baud with internal modem timer
- Receiver and transmitter off-states with no power consumption.

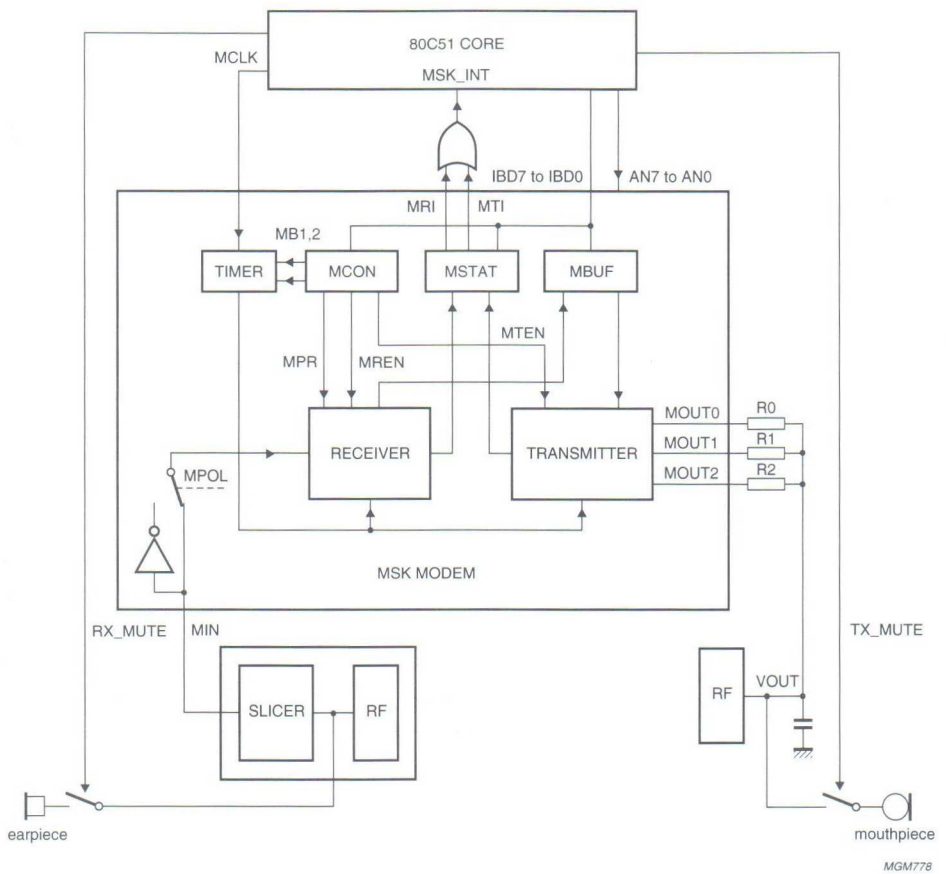


Fig.15 MSK Modem functional diagram.

10.14.1 80C51 MICRO INTERFACE.

The modem block interfaces to the microcontroller via the interrupt signal MSK_INT and via the control and data SFRs MCON, MSTAT and MBUF. The MSK modem receive and transmit registers are both accessed via the Special Function Register MBUF. Writing to MBUF loads the transmit register and reading MBUF accesses a physically separate receive register.

10.14.1.1 MSK modem control Register (MCON)

Table 34 MSK modem Control Register (SFR address D3H).

7	6	5	4	3	2	1	0
MPR3	MPR2	MPR1	MPR0	MB1	MB0	MTEN	MREN

Table 35 Description of MCON bits.

BIT	SYMBOL	DESCRIPTION
MCON.7 to MCON.4	MPR3 to MPR0	These bits define the modems preamble pattern.
MCON.3 to MCON.2	MB1 to MB0	These bits define the modem transmit/receive frequency. See Table 36.
MCON.1	MTEN	Modem Transmitter ENable. If set the transmitter is active and MOUT<3:1> will get the value <100> if no data is transmitted. If reset, MOUT<3:1> will get the value <111> to zero the currents in the resistive DA convertor.
MCON.0	MREN	Modem Receiver ENable. If set the modem receiver is active and scans for manchester data.

Table 36 Baud rates.

MB1	MB0	MODEM BAUD RATE
0	0	1200 baud
0	1	2400 baud
1	0	3600 baud
1	1	4800 baud

If both the transmitter and the receiver are disabled (MTEN = 0 and MREN = 0), the clock of the MSK modem is switched off. It is advised to use this state for power saving.

10.14.1.2 MSK modem Status Register (MSTAT)

Table 37 MSK modem Status Register (SFR address CAH).

7	6	5	4	3	2	1	0
MPOL	–	MRF	MRE	MRP	MRL	MTI	MRI

Table 38 Description of MSTAT bits.

BIT	SYMBOL	DESCRIPTION
MSTAT.6	MPOL	MIN polarity switch. If MPOL = 1 the value of the MIN pin is inverted before being applied to the MSK block.
MSTAT.5	MRF	Modem Receiver Full flag. This bit is set when MBUF holds a newly received byte. MRF is reset if the receiver is disabled (MREN = 0) or by reading MBUF. This bit is read-only. Writing to it will have no effect.
MSTAT.4	MRE	Modem Receiver Error flag. Indicates the reception of a non-manchester bit. This bit is set by hardware and is reset by reading MBUF, by disabling the receiver (MREN = 0) or by resetting MRI. This bit is read-only. Writing to it will have no effect.
MSTAT.3	MRP	Modem Receiver Preamble flag. This bit is set by hardware when the modem recognized the programmed preamble pattern (AAAH, MPR3 to MPR0) after locking the receiver clock (MRL = 1). MRP is reset by hardware if the receiver is disabled (MREN = 0) or if non-manchester data is received (MRE = 1). This bit is read-only. Writing to it will have no effect.
MSTAT.2	MRL	Modem Receiver Clock Locked flag. This bit is set when the clock of the receiver is locked, i.e. when the receiver has detected manchester data but has not found the preamble pattern yet. MRL is reset when the receiver detects a non-manchester bit or when the receiver is disabled. This bit is read-only. Writing to it will have no effect.
MSTAT.1	MTI	Modem Transmit Interrupt flag. Indicates MBUF is empty to accept a new byte for transmission. This bit is reset by writing to MBUF or by writing a 0 to it. Writing a 1 to MTI will set the bit. This allows to generate a hardware interrupt by software.
MSTAT.0	MRI	Modem Receive Interrupt flag. Indicates: Modem Receiver Full (MRF = 1) or Modem Receiver Error (MRE = 1) or Modem Receiver Preamble (MRP = 1) or Modem Receiver Clock Locked (MRL = 1) This bit is reset by reading MBUF or by writing a 0 to MRI. A reset of MRI will also reset MRE. Writing a 1 to MRI will have no effect.

10.14.1.3 MSK modem Data Buffer (MBUF)

Table 39 MSK modem Data Buffer (SFR address C9H).

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 40 Description of MBUF bits.

BIT	SYMBOL	DESCRIPTION
MBUF.7 to MBUF.0	D7 to D0	Writing to MBUF will load the data in the transmit buffer, and automatically start a transmission at MOUT if the transmitter is enabled (MTEN = 1). A new byte can be loaded after MTI is set. If a new byte is loaded before the setting of MTI then the previous byte will be lost. After data has been received at MIN, indicated by MRI, the received byte can be read from MBUF.

10.14.2 DATA TRANSMISSION

Data transmission is enabled if bit MTEN in register MCON is set to logic 1. If MTEN is logic 0 data transmission is disabled and MOUT<2:0> is set to <111> to zero the currents in the resistive DA converter. Setting MTEN to logic 1 sets MOUT<2:0> to the idle value <100>. This results in a value close to $\frac{1}{2}V_{DD}$ on the output signal of the external DAC. Transmission is started by loading the first byte into register MBUF. All bytes are transmitted starting with the MSB.

A message is transferred in a block of 3 or more bytes, the first two bytes being the programmed manchester preamble pattern. In order to insert the preamble pattern, the first two bytes AAH and AXH (with X being the MPR3 to MPR0 values programmed in the receiver MSK modem) have to be written to MBUF by software. After this, the first byte of the message is written to MBUF. As soon as MBUF is ready to accept new input, signal MTI is set. A new byte written to MBUF automatically clears MTI. The time between two MTI interrupts is $T = 8 \times 1/\text{baud rate}$. (e.g. for 1200 baud, T = 6,7 ms). If no new byte is written to MBUF at the end of a byte transmission, the modem transmitter stops transmission and MOUT<2:0> is set to the idle state <100>. In this case MTI must be cleared explicitly. If MTEN is reset during transmission, the transmitter will finish the transmission of the current byte and then will set MOUT<2:0> to the off state <111>. No interrupt on mti will be generated at the end of the transmission.

During reception, a digital PLL re-synchronises on the active transition of every bit. This allows a continuous transmission of long messages. Fig.16 shows a possible timing diagram of data transmission.

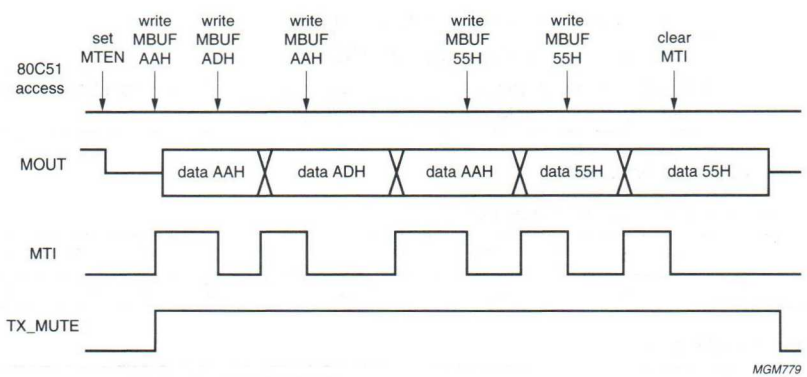


Fig.16 Data transmission timing diagram

10.14.3 Data reception

A message is received as a block of one or more data bytes. When enabled, the receiver starts sampling MIN and tries to detect a manchester pattern. As soon as 3 consecutive manchester bits are detected the receiver clock is locked (MRL = 1) and the receiver starts scanning the incoming data for the programmed manchester preamble pattern. When the modem recognizes the preamble pattern, bit MRP is set to logic 1. If a non manchester bit is detected before finding the preamble pattern then MRL is reset and MRE is set to logic 1. The synchronisation process has to restart. If the preamble pattern has been detected the receiver starts to manchester decode the incoming data bits and shifts them into an internal register. After eight bits the contents of the internal register are copied to MBUF and MRF bit is set to logic 1. The received byte can be read from MBUF while receiving continues in the internal register. If a non-manchester bit is received during data reception then MRE is set to logic 1 and MRL and MRP are reset. The receiver has to resynchronize before receiving new data.

Whenever one of the bits MRF, MRE, MRP and MRL is set the MRI bit is also set and an MRI interrupt is generated. This means that when an MRI interrupt occurs the 4 status bits have to be polled by software. The bit MRL allows the software to decide very quickly whether an occupied channel contains manchester coded data or not. The MRP bit is used to find the start of data transmission in a message that is repeated over and over again. MRE is used to detect a manchester error, which is a violation of the manchester coding rule that the received level should change in the middle of a bitcell. The MRF bit indicates that the data in MBUF is ready to be read by the software. During data reception the time between two settings of MRF (each one generating an MRI interrupt) is $T = 8 \times 1/\text{baud rate}$. Fig.17 shows an example of the timing diagram of data reception.

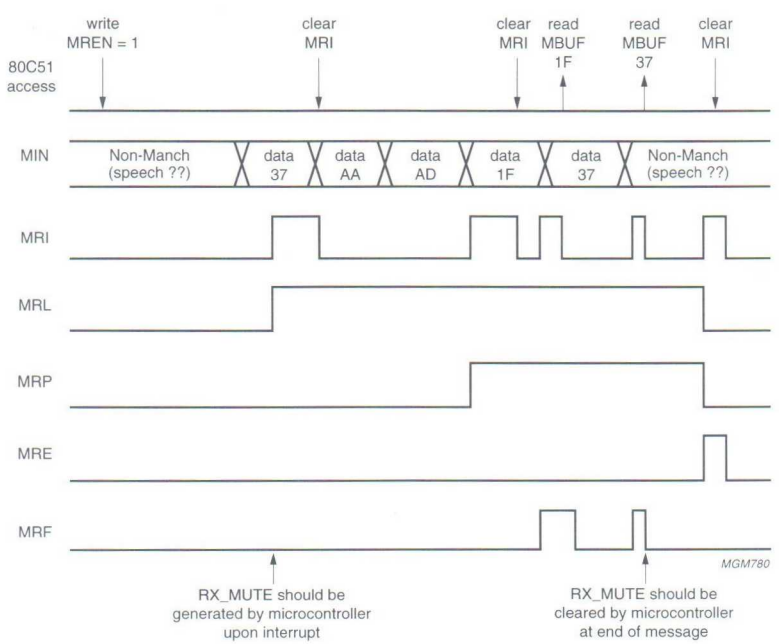


Fig.17 Data reception timing diagram.

10.14.4 MANCHESTER CODING OF DATA

The bits of the data byte written in MBUF are manchester encoded as shown in Fig.18: A logic 1 is coded as a LOW-to-HIGH transition in the middle of a bitcell, a logic 0 is coded as a HIGH-to-LOW transition.The manchester encoded signal contains redundancy for early error detection in received bits. A non matching 1-0 or 0-1 pair indicates an error condition.The manchester encoded signal has a polarity change in each bitcell.

10.14.5 WAVEFORM GENERATION WITH MOUT<2:0>

The 3 digital output pins MOUT<2:0> should be used as an input to a three bit external DA convertor. The signals can be connected via external resistors R2,R1 and R0 to a summation point and then be filtered with an external capacitor C1.This 3-bit DAC is shown in Fig.18.

Table 41 gives a relation between MOUT<2:0> and the resistor values and voltage VOUT.

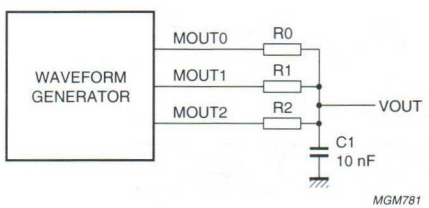


Fig.18 3-bit DAC with MOUT<2:0>.

Table 41 VOUT as a function of MOUT and the resistor values.

MOUT2,1,0	VOUT	RESISTOR VALUES
000	0	R0 = R R1 = 0.48 × R R2 = 0.25 × R
001	$0.14V_{DD}$	
010	$0.29V_{DD}$	
011	$0.43V_{DD}$	
100	$0.57V_{DD}$	
101	$0.71V_{DD}$	
110	$0.86V_{DD}$	
111	V_{DD}	

Figure 19 shows the possible waveforms that are produced by the waveform generator. The horizontal axis shows the sample counter on which the waveform changes its value. Each bit is built-up out of 2 × 40 samples (n × 3.456 MHz crystal, CKCON.6 = 0) or 2 × 42 samples (3.58 MHz, CKCON.6 = 1). The vertical axis shows the values of MOUT<2:0>, forming the inputs of the resistive DA converter. The first half of the waveform is determined by the previous and the current bit, whereas the second half of the waveform is determined by the current and the next bit to be transmitted. The count frequency of the sample counter depends on the programmed baud rate.

If the transmitter is disabled with MTEN set to logic 0, MOUT<2:0> is <111> to save power in the resistive DA converter. If the transmitter is enabled and no data is transmitted, MOUT<2:0> has an idle value of <100>, which corresponds to $0.57V_{DD}$.

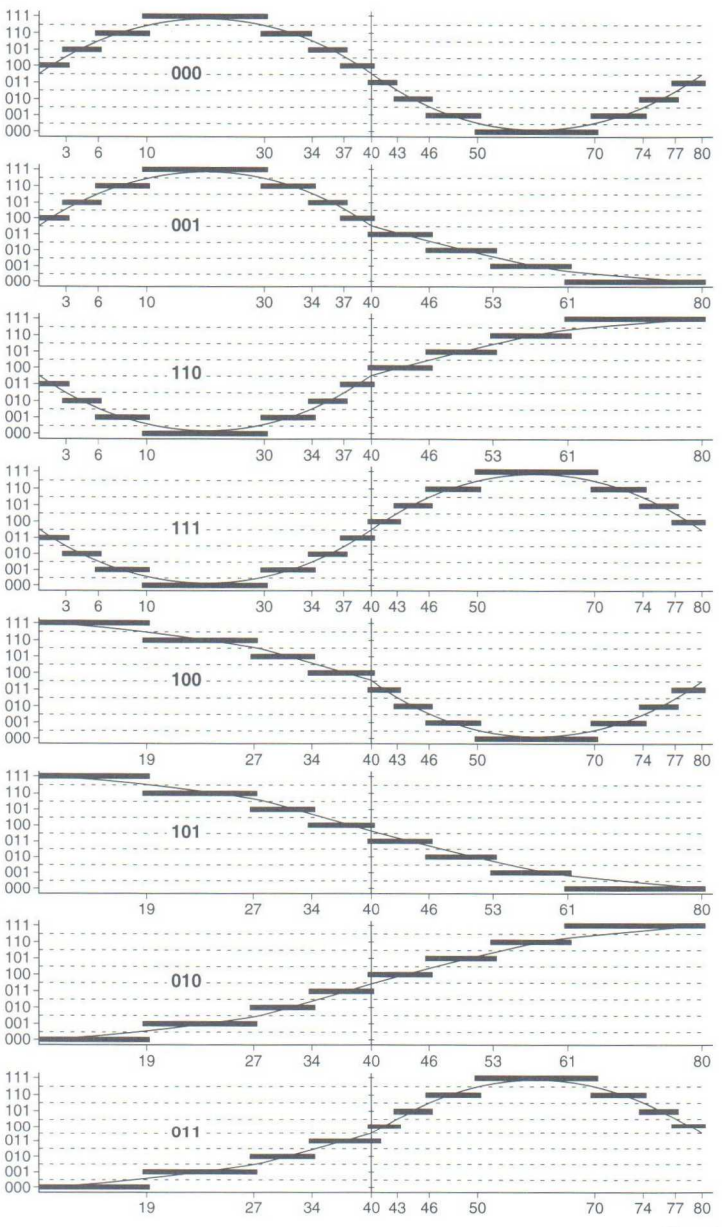


Fig.19 Waveforms with MOUT<2:0> for previous, current and next bits to be transmitted

10.14.6 SYNCHRONISATION

When enabled the receiver samples MIN with a frequency f = 8 × baud rate. The sampled values are shifted into an 8-bit shift register. This register is regularly checked whether it contains samples that fulfil the manchester coding rule i.e. whether there is a LOW-to-HIGH or a HIGH-to-LOW transition in the middle of the bitcell. The receiver searches for 3 consecutive sets of 8 samples that fulfil the manchester coding rule. If these sets have been found the clock is locked (MRL = 1) and the receiver starts looking for the manchester preamble pattern. From this point on the receiver uses a PLL (Phase Locked Loop) to adjust the synchronisation after each received manchester bit.

10.15 DTMF generator

A versatile frequency generator section is provided (see Fig.20). The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets. One bit of the DTMF control register (DTCON) is used to select which line input is used for the CODEC.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available.

10.15.1 FREQUENCY GENERATOR DERIVATIVE REGISTERS

Table 42 gives the derivative addresses, mnemonics and access types of the three frequency generator derivative registers. When bit ETONE in register DTCON is set to logic 1 the TONE output is enabled. Bit LINESEL is used to select the alternative inputs for the line CODEC (see Chapter 13). To reach lowest possible power consumption, it is strongly recommended to write 00H in both the frequency registers HGF and LGF. Reserved bits should not be changed.

Table 42 Addresses of the frequency generator derivative registers

ADDR	TYPE	MNEMONICS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
C7H	W	DTCON: DTMF Control Register	reserved	reserved	–	LINESEL 0: LIFMIN1 1: LIFMIN2	–	–	reserved	ETONE
C6H	W	HGF: High Group Frequency Register	H7	H6	H5	H4	H3	H2	H1	H0
BEH	W	LGF: Low Group Frequency Register	L7	L6	L5	L4	L3	L2	L1	L0

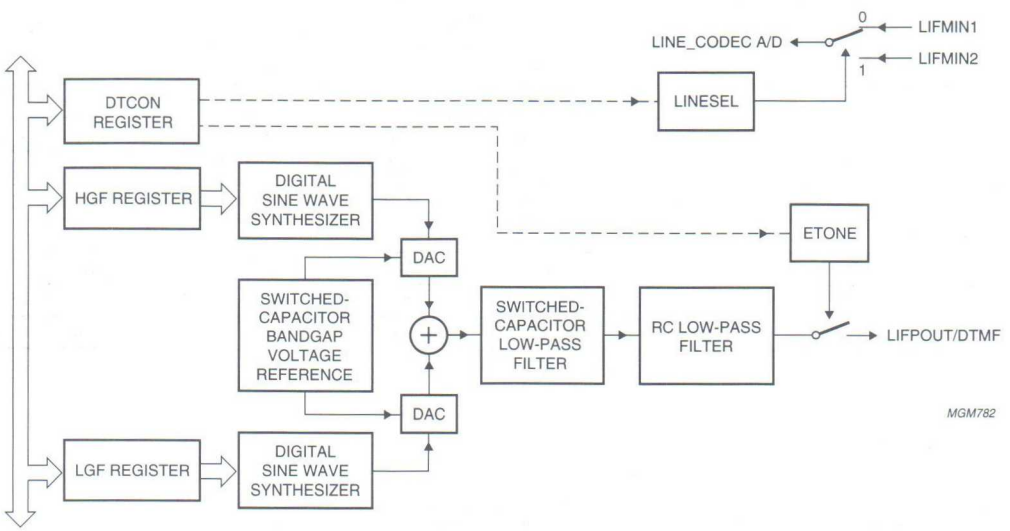


Fig.20 Frequency generator section, and CODEC input selection.

10.15.2 Frequency registers

The two frequency registers define two frequencies. From these, the digital sine synthesizers together with the digital-to-analog converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures tone output levels independent of supply voltage and temperature. The amplitude of the Low group frequency sine is attenuated by 2 dB compared to the amplitude of the High group frequency sine wave.

The two sine waves are summed and then filtered by on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT CS203 recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components. '00H' in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain '00H', the whole frequency generator is shut off, resulting in lower power consumption.

A decimal value of 'x' in a frequency register yields a digital sine signal with frequency:

$$f = \frac{f_{xtal}}{[23\,(x+2)\,]}\ ;\ \text{where } 60 \leq x \leq 255.$$

The frequency limitation given by $x \geq 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

10.15.3 DTMF frequencies

The input frequency to the frequency generator is f_{PSC}. Assuming an oscillator frequency of a multiple of $f_{DTMF} = 3.579545$ MHz, the division factor of the prescaler should be chosen such that $f_{PSC} = f_{DTMF}$. The DTMF standard frequencies can then be implemented as shown in Table 43. The relationship between telephone keyboard symbols and the frequency register contents are given in Table 44.

Table 43 DTMF standard frequencies and their implementation

STANDARD FREQUENCY (Hz)	REGISTER VALUE		GENERATE FREQUENCY (Hz)		DEVIATION			
					(%)		(Hz)	
	f_{xtal1}[1]	f_{xtal2}[2]	f_{xtal1}	f_{xtal2}	f_{xtal1}	f_{xtal2}	f_{xtal1}	f_{xtal2}
697	DDH	D6H	697.90	695.65	0.13	−0.19	0.90	−1.35
770	C8H	C1H	770.46	770.57	0.06	0.07	0.46	0.57
852	B5H	AEH	850.45	853.75	−0.18	0.21	−1.55	1.75
941	A3H	9EH	943.23	939.13	0.24	−0.20	2.23	−1.87
1209	7FH	7AH	1206.45	1211.78	−0.21	0.23	−2.55	2.78
1336	72H	6EH	1341.66	1341.61	0.42	0.42	5.66	5.61
1477	67H	64H	1482.21	1473.15	0.35	−0.26	5.21	−3.85
1633	5DH	5AH	1638.24	1633.27	0.32	0.02	5.24	0.27

Notes

1. f_{xtal1} = 3.58 MHz.
2. f_{xtal2} = 3.456 MHz.

Table 44 Dialling symbols, corresponding DTMF frequency pairs and frequency registers content

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	3.58 MHz CRYSTAL	
		LGF VALUE	HGF VALUE
0	(941, 1336)	A3H	72H
1	(697, 1209)	DDH	7FH
2	(697, 1336)	DDH	72H
3	(697, 1477)	DDH	67H
4	(770, 1209)	C8H	7FH
5	(770, 1336)	C8H	72H
6	(770, 1477)	C8H	67H
7	(852, 1209)	B5H	7FH
8	(852, 1336)	B5H	72H
9	(852, 1477)	B5H	67H
A	(697, 1633)	DDH	5DH
B	(770, 1633)	C8H	5DH
C	(852, 1633)	B5H	5DH
D	(941, 1633)	A3H	5DH
•	(941, 1209)	A3H	7FH
#	(941, 1477)	A3H	67H

10.15.4 MODEM FREQUENCIES

Again assuming an oscillator frequency $f_{PSC} = f_{DTMF} = 3.579545$ MHz, the standard modem frequency pairs summarized in Table 45 can be implemented. It is suggested to define the frequency by the HGF register while the LGF register contains '00H', disabling Low group frequency generation.

Table 45 Standard modem frequency pairs and their implementation

HGF VALUE	FREQUENCY (Hz) IF 3.58 MHz CRYSTAL		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9DH	980[1]	978.82	−0.12	−1.18
82H	1180[1]	1179.03	−0.08	−0.97
8FH	1070[2]	1073.33	0.31	3.33
79H	1270[2]	1265.30	−0.37	−4.70
80H	1200[3]	1197.17	−0.24	−2.83
45H	2200[3]	2192.01	−0.36	−7.99
76H	1300[4]	1296.94	−0.24	−3.06
48H	2100[4]	2103.14	0.15	3.14
5CH	1650[1]	1655.66	0.34	5.66
52H	1850[1]	1852.77	0.15	2.77
4BH	2025[2]	2021.20	−0.19	−3.80
44H	2225[2]	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

10.15.5 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency $f_{PSC} = f_{DTMF} = 3.579545$ MHz (Table 46). It is suggested to define the frequency by the HGF register while the LGF contains '00H', disabling Low group frequency generation

Table 46 Musical scale frequencies and their implementation when using a 3.58 MHz crystal

NOTE	HGF VALUE	FREQUENCY (Hz) IF 3.58 MHz CRYSTAL	
		STANDARD[1]	GENERATED
D#5	F8H	622.3	622.5
E5	EAH	659.3	659.5
F5	DDH	698.5	697.9
F#5	D0H	740.0	741.1
G5	C5H	784.0	782.1
G#5	B9H	830.6	832.3
A5	AFH	880.0	879.3
A#5	A5H	923.3	931.9
B5	9CH	987.8	985.0
C6	93H	1046.5	1044.5
C#6	8AH	1108.7	1111.7
D6	82H	1174.7	1179.0
D#6	7BH	1244.5	1245.1
E6	74H	1318.5	1318.9
F6	6DH	1396.9	1402.1
F#6	67H	1480.0	1482.2
G6	61H	1568.0	1572.0
G#6	5CH	1661.2	1655.7
A6	56H	1760.0	1768.5
A#6	51H	1864.7	1875.1
B6	4DH	1975.5	1970.0
C7	48H	2093.0	2103.3
C#7	44H	2217.5	2223.3
D7	40H	2349.3	2358.1
D#7	3DH	2489.0	2470.4

Note

1. Standard scale based on A4 @ 440 Hz.

10.16 LE control

The LE signal is an alternative output of P4.0 and can be turned on with ALTP bit 1. The LE signal can be used to connect to the E input of 68 microcontroller compatible peripherals such as an LCD controller. If these peripherals have a slow access time the LE signal can be made HIGH earlier by setting bit 0 of ALTP. Bit 0 of ALTP will be cleared by hardware after the execution of a MOVX instruction. The ALTP register is described in more detail in Section 16.2.

Figure 21 shows the LE signal shapes for early read and/or write when the P4.0 alternate port function for LE is selected. In Fig.21, the DTAM WRN signal is only shown for timing reference. Neither WRN nor RDN are physically connected to the display.The display RS and R/W pin can be connected to Port 2 or Port MA pins (logic 0 after reset) and controlled by software. the early LE timing hardware makes it possible to access LCD drivers (or other peripheral devices with the same interface) which require a large access time (> $3 \times \mu$C_CLK)

The display LE pin (P4.0) rising edge is determined by software, by setting Bit 0 and Bit 1 of the ALTP SFR. In order to latch the Port 0 data at the correct moment, the falling edge is determined by internal DTAM hardware. This generates for the LCD write operation an LE falling edge at 0.5 of a microcontroller clock before the falling edge of WRN, such that the LCD data hold time (T_{HOLD}) requirement is always fulfilled.

Figure 22 shows the LE signal shape for normal read and/or write when the P4.0 alternate port function for LE is selected.Again, the DTAM WRN signal is only shown for timing reference. Both the rising and falling edges of the display LE pin (P4.0) are determined by hardware if only Bit 1 of the ALTP SFR is set. This generates for the LCD write operation an LE falling edge at 0.5 of a microcontroller clock before the falling edge of WRN, such that the LCD data hold time (T_{HOLD}) requirement is always fulfilled.

The normal LE timing is actually the inverted value of either the RDN or WRN signal. This timing can be used for peripheral devices that have an access time of less than $3 \times \mu$C_CLK.

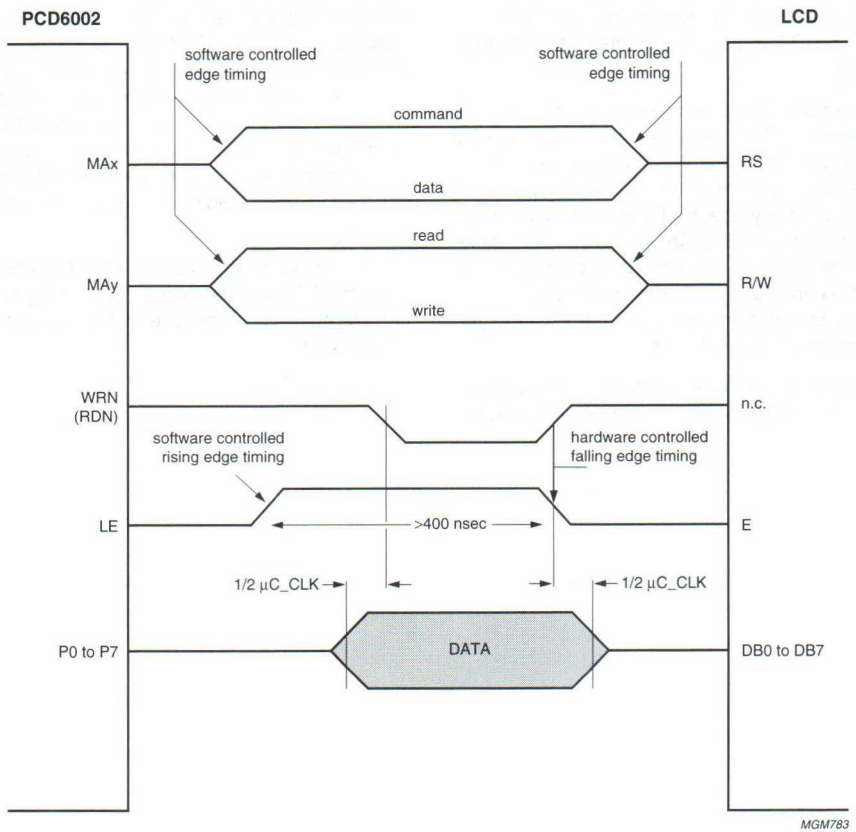


Fig.21 Early LE timing.

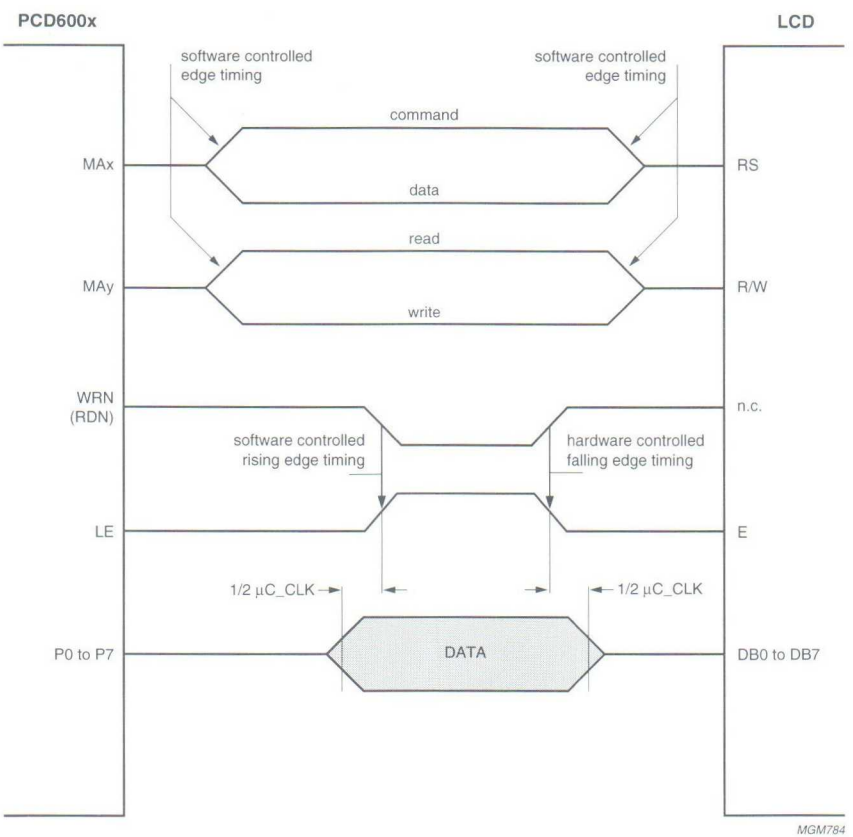


Fig.22 Normal LE timing.

11 DSP I/O REGISTERS

For the DTAM application, the DSP is connected with several peripherals as shown in Fig.23. Basically, the DSP is connected to the analog interfaces CODEC1 and CODEC2.

The DSP communicates with the peripherals via the DSP I/O registers. The data transfer is performed by the 16 bit XD data bus. The I/O registers of the different I/O units are 16 bits wide.

The microcontroller controls the DSP and is the link between an external speech memory and the DSP. The TICB provides the FS1 clock, which interrupts the DSP every 125 μs.

11.1 Interface to CODEC

The CODEC data buffers are used to exchange speech data between the DSP and the CODECs (see Fig.23). The digital decimation filter DDF writes equidistant in time 16-bit linear PCM samples to the DSP I/O registers CDC_DI0 to CDC_DI3 (address 01H to 04H for CODEC1 and address 09H to 0CH for CODEC2) at a rate of 32 kHz. The digital noise shaper DNS reads equidistant in time 16 bit linear PCM samples from the DSP I/O registers CDC_DO0 to CDC_DO3 (address 05H to 08H for CODEC1 and address 0DH to 10H for CODEC2) at a rate of 32 kHz. The input registers CDC_DI0 to CDC_DI3 and the output registers CDC_DO0 to CDC_DO3 are also called data input/output DIO registers.

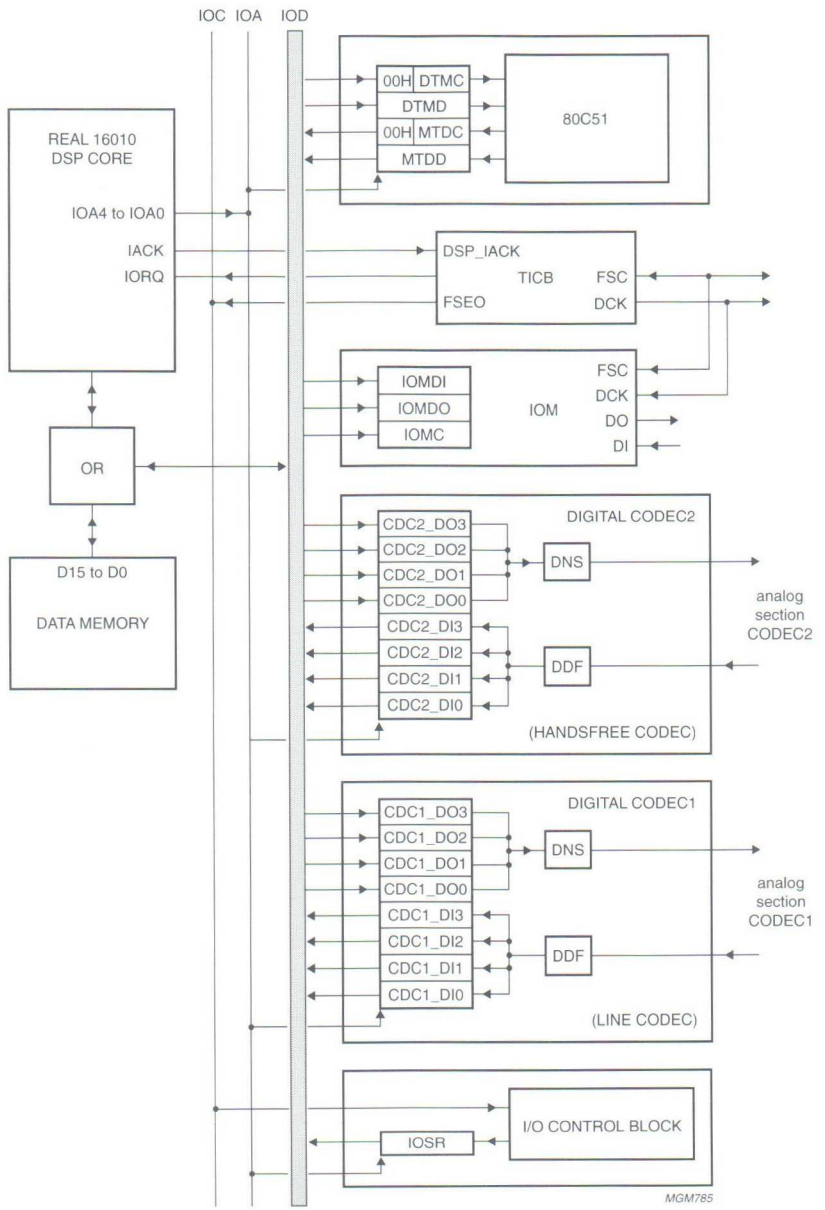


Fig.23 DSP I/O architecture.

12 EXTERNAL MEMORY INTERFACE

The external memory interface consists of the interface from the OTP to external Flash memory and software debugging circuitry such as a Metalink Emulator or Target Debugger. The interface from the OTP to the remainder of the digital section is nearly the same as the OTP to external memory interface which facilitates the connection of external memory. The external memory interface also allows in system programming of the OTP via the microcontroller. The external memory interface is shown in Fig.24.

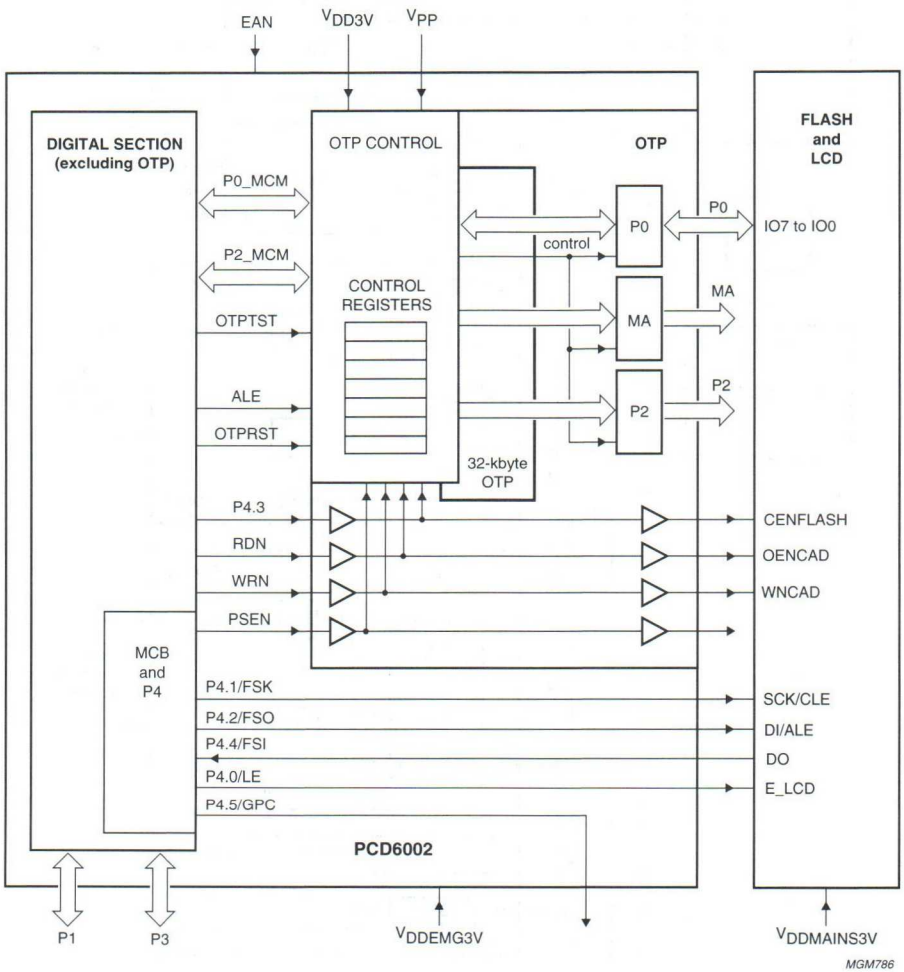


Fig.24 External memory interface.

The OTP will be activated by making EAN logic 1. If EAN is logic 0 external program memory can be connected and the OTP will be disabled. The OTP CNTRL block contains the MA and P2 generation and, in system programming, logic and registers.

The P2 and MA latches have special enable signals and the P2 latch has a special output to make P2 and MA available as general purpose output ports or as the 80C51 address bus. The last option is necessary for target debugging (EAN = 0), external ROM (EAN = 0) or parallel Flash memory (MAGP = 1 and P2GP = 1). In these cases external latches must be provided if the application needs the P2/MA output ports.

The MAGP and P2GP signals are bit 3 and bit 4 of the Configuration Register latch. MA will be a general purpose output port when MAGP is set to logic 0 by software (default after reset). If MAGP is set to logic 1 the MAGP port operates as the lower 8 bits of the program/data address bus. P2 will be a general purpose output port when P2GP is set to logic 0 by software (default after reset). If P2GP is set to logic 1 the MAGP port operates as the higher 8 bits of the program/data address bus. The P2GP and MAGP bits of the GP register in the OTP CNTRL block can only be read and written if P4.3 is logic 1. The select signals are retrieved from the signals P0_AL, P2 and P4.3.

Besides the Configuration Register, MA and P2 latches there are 5 other latches in the OTP CNTRL block used for system OTP programming. The OTP latches are mapped at address 200H to 206H of the external data memory and can only be accessed if P4.3 SFR bit is logic 1. Refer to Table 47.

- Register **ADDL (8-bit):** latches the low address byte for parallel/in system programming.
- Register **ADDH (8-bit):** latches the high address byte for parallel/in system programming.
- Register **DATA (8-bit):** latches the data or the security bits which should be programmed in 'in system programming mode'
- Register **TestControl (8-bit):** In this register the test mode can be selected. If the value of this register is changed, proper operation of the OTP block and proper code fetching can not be guaranteed.
- Register **ConfReg (6-bit)**: This is the configuration register. In this registers single bits are set to control the functionality of the OTP chip. The content of this register is given in Table 48. With the bits **P2GP** (P2 General Purpose) and **MAGP** (MA General Purpose) the output function of MA and P2 is determined.

  With bit P2GP = 0 (reset value) the output P2 is latched and can be used as a general purpose output for example to drive LEDs. Data can be written to the register P2 with a MOVX command. With P2GP = 1 the input bus P2_IF[7:0] is directly transferred to the output P2[7:0]. This mode is for example applied when using parallel Flash. Output P2[7:0] delivers then the low address byte for the parallel Flash. The output pins P2[7:6] are different from the ones P2[5:0]. The reason for this is that P2[7:6] can be changed to inputs when in 'in system programming mode'.

  The bit **VPon** of the configuration register indicates high voltage for programming. VPon = 1 whenever there is a high voltage on input V_{PP} (V_{PP} = 12.5 to 13 V) indicating an insytem programming condition. VPon is the only bit of the configuration which is read only.

  The bit **CO = 1** (reset value CO = 0) (Change Output) of the configuration register changes the outputs P2[7:6] to inputs which are used for in system programming. The in system programming algorithm is explained in detail in a following section. The block InsysProg Direction Switch changes P2[7:6] from inputs to outputs.

  With **MAGP** = 1 (reset value MAGP = 0) the output MA[7:0] can be used as general purpose output. Otherwise output MA[7:0] serves as latch (with ALE_IF as enable signal) for the low address byte provided by the bus P0_IF[7:0].

  With **SIG** = 1 (SIG = Signature byte) the 1-kbyte test memory array can be accessed during in system programming mode. The test memory can be addressed either with SIG = 1 or with an address above the ordinary memory range of 32 kbytes (addresses >7FFFH). The signature bytes (which are read only) are located in the test memory space.

  With **SEC** = 1 the security bits can be programmed in 'in system programming mode'.
- Register **MA (8-bit):** If EAN = 1 (internal OTP used) and MAGP = 0 (default after reset) the MA pins will output the contents of the MA register (0201H) which contains 00H after reset. The state of the MA pins can be changed by writing a new value to the MA register. This must be done with a MOVX instruction while the P4.3 bit is a logic 1.
- Register **P2 (8-bit):** If EAN = 1 (internal OTP used) and P2GP = 0 (default after reset) the P2 pins will output the contents of the P2 register (0202H) which contains 00H after reset. The state of the P2 pins can be changed by writing a new value to the P2 register. This must be done with a MOVX instruction while the P4.3 bit is a logic 1.

Table 47 OTP control registers

OTP CONTROL REGISTER	ADDRESS P2/P0 (P4.3 = 1)	RESET VALUE	ACCESS
Configuration Register	0200H	00H	R&W
MA	0201H	00H	R&W
P2	0202H	00H	R&W
Test Control	0203H	00H	R&W
ADDL	0204H	00H	R&W
ADDH	0205H	00H	R&W
DATA	0206H	00H	R&W

Table 48 Configuration Register (ConfReg), reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
–	–	VPon (read only)	P2GP	MAGP	SEC	SIG	CO

12.1 Supported Flash memories

Table 49 shows the ports that are available in an application using various Flash memories.

For all types of Flash memory shown in Table 49 (except for the parallel Flash memory) - at least 34 general purpose I/O pins can be used for the application (display, line interface, keypad, LEDs; for example). P0 can also be used for the application to connect memory mapped peripherals such as an LCD controller or keypad.

P0 pins have no output latch, so data written to this port will not remain here.

Table 49 Ports available for the application

FLASH MEMORY	PORTS USED BY FLASH			PORTS AVAILABLE FOR APPLICATION		
	I/O	I	O	I/O	I/O	O
CAD	P0	–	P4.1, P4.2, P4.3	P1, P3, P4.0, P4.4, P4.5	P0[1]	MA, P2
SPI/Microwire	–	P4.4	P4.1, P4.2, P4.3	P1, P3, P4.0, P4.5	P0	MA, P2
I^2C	P1.6, P1.7	–	–	P1, P3, P4	P0[1]	MA, P2, P4.3
Parallel	P0	–	MA, P2, P4.0, P4.1, P4.2, P4.3	P1, P3, P4.4, P4.5	P0[1]	–

Note

1. P0 can be used as a data bus for other peripherals if not conflicting with the Flash memory.

There are many different types of Flash memories manufactured, and the PCD6002 will work with many of them. Table 50 below explains the most important characteristics of a few of the commercially available Flash memories which can be connected to the PCD6002 directly.

Table 50 Ports available for the application

FLASH MEMORY TYPE NUMBER	MADE BY	INTERFACE TYPE	SIZE (MBIT)	MIN. WRITE SIZE (bytes)	MIN. READ SIZE (bytes)	MIN. ERASE SIZE (bytes)	t_{ACC} (ns)	SUPPLY (V)	TYPICAL STAND-BY CURRENT (μA)
AM29LV004	AMD	Parallel 8	4	1	1	64 K	100	3	1
AM29LV400	AMD	Parallel 8/16	4	1	1	64 K	100	3	1
MBM29LV004	Fujitsu	Parallel 8	4	1	1	64 K	100	3	5
KM29V040[1]	Samsung	Mux CAD	4	32	1	4 K	100	3	10
AT45DB041[1]	ATMEL	SPI	4	1[2]	1	264	–	3	10
NM29A040[1]	National Semiconductors	Microwire	4	32	32	4 K	–	5	5
TMS29F040	Texas Instruments	Parallel 8	4	1	1	64 K	60	5	25
TC58A040F[1]	Toshiba	Microwire	4	32	32	4 K	–	5	50
M29V040	SGS Thomson	Parallel 8	4	1	1	64 K	120	3	25

Notes

1. Supported by Philips PCD6002 API software.
2. With the aid of the internal Flash data memory buffers.

The access time requirement of any external memory like the OTP, parallel Flash (PF), CAD Flash or external ROM is explained in Table 51.

Table 51 Memory access time requirements

CASE	MEMORY TYPE	CEN CONNECTION	OEN OPERATION	t_{ACC} REQUIREMENT
1	ROM/OTP	VSS	PSEN	$t_{ACC} < (5/2 \times T_{\mu C_CLK})$ – delay
2	CAD/PF	VSS	RDN	$t_{ACC} < (5 \times T_{\mu C_CLK})$ – delay
3	ROM/OTP	ALE	PSEN	$t_{ACC} < (2 \times T_{\mu C_CLK})$ – delay
4	CAD/PF	ALE	RDN	$t_{ACC} < (9/2 \times T_{\mu C_CLK})$ – delay
5	ROM/OTP	PSEN	VSS	$t_{ACC} < (3/2 \times T_{\mu C_CLK})$ – delay
6	CAD/PF	RDN AND WRN	RDN	$t_{ACC} < (3 \times T_{\mu C_CLK})$ – delay

The delay parameters are defined by the delay (capacitive load) of the address bus, data bus, RDN and PSEN pins, the power supply voltage and the internal delay in the OTP and digital section. As shown in Table 51 there is a trade-off between power consumption and memory speed requirement.

12.1.1 DTAM EXTERNAL MEMORY USING A PARALLEL FLASH

A parallel Flash memory can be connected to the PCD6002 chip as shown in Fig.25. The GPMA and GPP2 bits in the OTP configuration register must be set. Clearing P4.3 will enable the Flash memory.

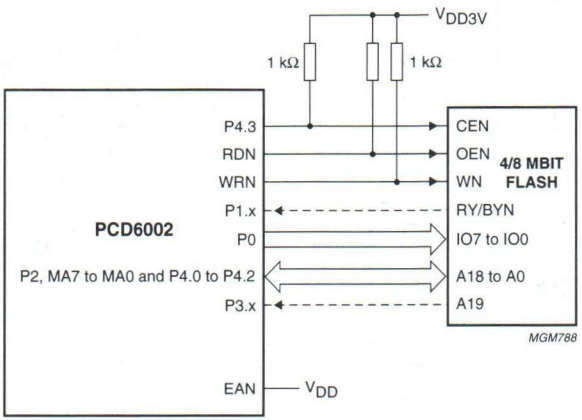


Fig.25 Parallel Flash memory connection.

12.1.2 DTAM EXTERNAL MEMORY INTERFACE USING A 4-WIRE SERIAL FLASH

A 4-wire serial Flash memory (like SPI or Microwire Flash memory) can be connected to the PCD6002 chip as shown in Fig.26. P4.3 must be pulled up to 5 V with a resistor when using a 5 V serial Flash memory. P4.1 and P4.2 must be pulled to 3 V with a resistor. When using a 5 V Flash memory the DO output of the Flash must be level-shifted to 3 V with 2 resistors (1 kΩ and 1.5 kΩ).

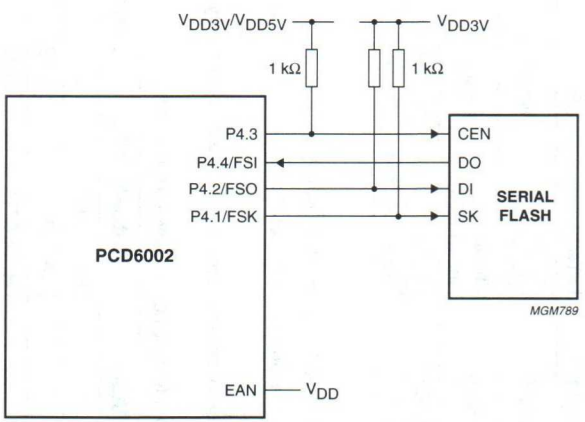


Fig.26 Serial Flash memory connection.

12.1.3 DTAM EXTERNAL MEMORY INTERFACE USING AN I²C SERIAL FLASH

An I²C Flash memory can be connected to the PCD6002 chip as shown in Fig.27.

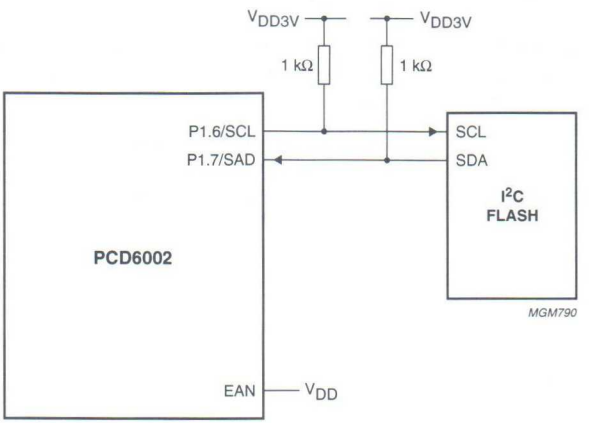


Fig.27 I²C serial Flash memory connection.

12.1.4 DTAM EXTERNAL MEMORY USING A CAD FLASH

A CAD Flash memory can be connected to the PCD6002 chip as shown in Fig.28. P4.3 must be pulled up to 3 V with a resistor when using a 3 V serial Flash memory. P4.1, P4.2, RDN and WRN must also be pulled to 3 V with a resistor.

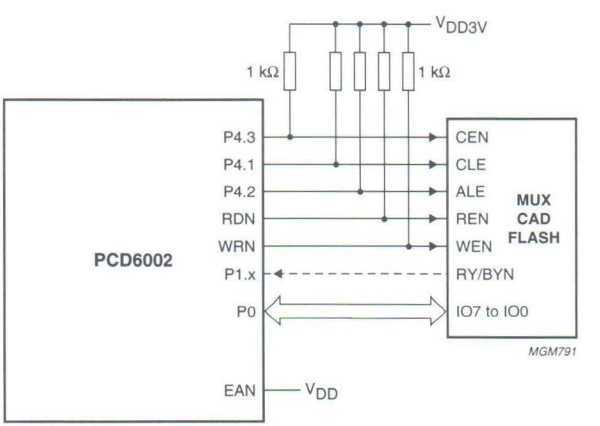


Fig.28 Muxed CAD Flash memory connection.

12.2 DTAM external interface during target debugging

If the DTAM chip is used with the tScope-51 target debug tool the DTAM chip needs executable SRAM where the monitor program MON51 can store the program code. This SRAM is accessible by means of the RDN, WRN and PSEN signals. Since connection to parallel Flash memory with XSRAM and ROM is the worst case situation this case is shown in Fig.29. Since it is not a commercial system additional logic can be connected to the DTAM chip to create executable SRAM.

The target debug logic only consists of combinational logic:

- CENROM <= P2.7 or P2.6 or P2.5
- CENFLASH <= P4.3
- CENXSRAM <= (PSEN or not CENROM) and (RDN or not CENFLASH)
- OENXSRAM <= PSEN and RDN
- WRNXSRAM <= WRN

The port restore logic is necessary to make the MA/P2/P0 ports available for the application.

The MON51 program is assumed to be in the lowest 8 kbytes of the ROM. If the Flash memory should be accessed clear P4.3 to logic 0. Now the MON51 program has no access to the XSRAM with RDN so no breakpoints are allowed in the code area where P4.3 is logic 0. Set P4.3 to logic 1 again after the Flash memory access to enable MON51 again to access the XSRAM.

Target debugging requires I^2C and one general purpose input port. This means that at least 33 I/O ports are available for the application (not using parallel Flash) during target debugging.

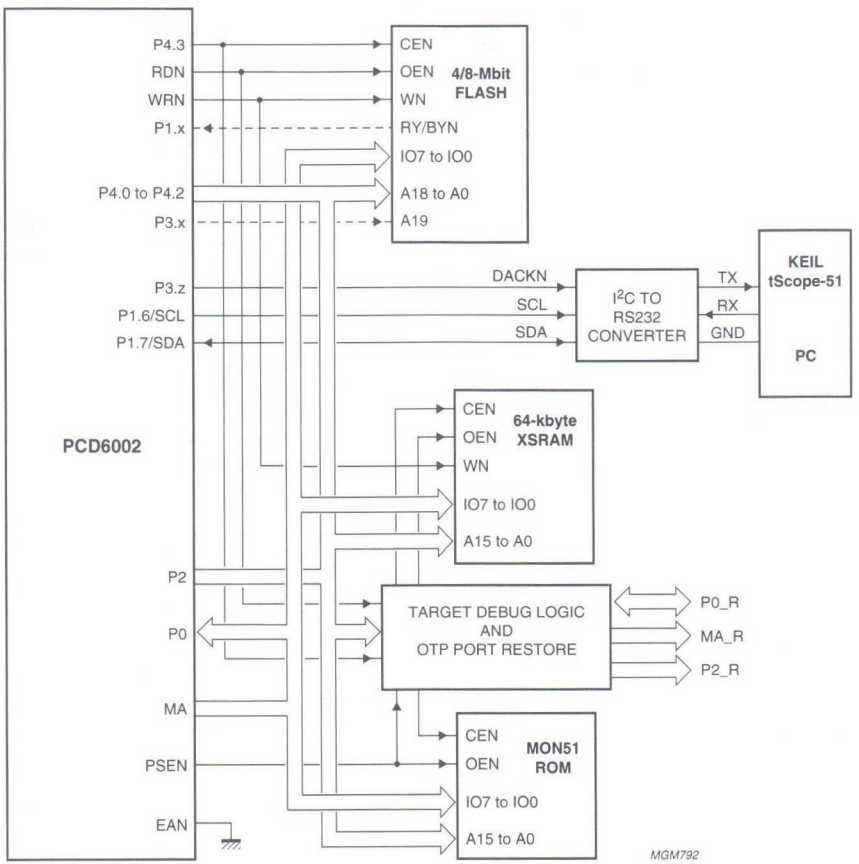


Fig.29 Flash, XSRAM and MON51 ROM memory connection.

13 THE CODECS

13.1 Definitions.

In the description of the codec amplitude units in dB are used. The following definitions apply:

- **dBm** used for absolute analog signal power levels. 0 dBm equals 1 mW in 600 Ω. A single sinewave signal with a power level of 0 dBm corresponds to an RMS voltage value of 774.6 mV_{rms}.
- **dBm0** used for relative digital signal power levels. 0 dBm0 is defined in *"CCITT Recommendation G.711 (Section 4, Table 5)"*. It follows that the maximum signal power level is +3.14 dBm0 (A-law). Thus +3.14 dBm0 is the RMS value of a sinewave signal whose peaks just reach the full scale of the digital code. For the (internal) bitstream signal (output of ARS and DNS) the positive full scale value is a continuous stream of 'ones', whereas the negative full scale value is a continuous stream of 'zeroes'. For the (internal) digital 14 or 16-bit words, represented in 2's complement (MSB first) the positive full scale value is a 'zero' followed by 13 or 15 'ones', whereas the negative full scale value is a 'one' followed by 13 or 15 'zeroes'.
- **dBmp** used for absolute analog signal power levels with psophometric weighting according to *"CCITT Recommendation G.223"*. This unit is used to express analog noise power levels.
- **dBm0p** used for relative digital signal power levels with psophometric weighting.
- The **uniform PCM reference point** is the (virtual) signal node in the DSP at the input of the ADPCM encoder for the A/D speech path. The uniform PCM reference point is the (virtual) signal node in the DSP at the output of the ADPCM decoder for the D/A speech path. These definitions apply for both the handset and base station version.
- **dB** is used for the signal level gain between any two nodes within the speech path. As different signal representations are used within the speech path, the gain value depends on the used signal definitions.

13.2 CODEC architecture.

The PCD6002 is provided with two CODECs that perform the AD/DA conversion of speech signals. As shown in Fig.30, the CODECs are the interface between the external analog peripherals and the DSP. CODEC1 is used for the line interface and CODEC2 is used for the loudspeaker and the microphone. For convenience the DTMF block and associated registers are also shown in Fig.30. The DTCON register bit DTCON.4 selects either DTMF or CODEC output, and also the input to CODEC 1. Refer to Table 42 in Section 10.15.

The main CODEC functions are:

- AMP - Pre-amplifier.
- ARS - Analog Receive Sigma delta A/D converter
- DDF - Digital Decimation Filter
- DNS - Digital Noise Shaper
- ATD - Analog Transmit D/A converter

For CODEC1 the balanced line interface input is fed to the ARS block that performs A/D conversion and has an analog amplifier. This amplifier has a fixed gain of 6 dB and an additional +0 to +15 dB programmable amplification range. This programmable range is used by the microcontroller on command of the DSP to perform limit or automatic gain control. The total gain then results in +6 to +21 dB. The analog data is converted by ARS to a bit stream. The basic sampling frequency F_s is 8 kHz. The DDF decimates the bit stream down to 16 bit linear PCM data. The DDF has a gain of 3.14 dB to achieve a uniform reference point at the DSP input for linear PCM data. Finally, the DSP will decimate this data to 16-bit linear PCM data at a rate of 8 kHz.

The reverse operation is performed in the transmit path. The DSP produces 16 bit linear PCM to the digital noise shaper DNS. The ATD which is a DAC converts the bit stream into an analog signal. The converter has a programmable amplification range of 15 dB.

CODEC2 is built up in a similar manner as CODEC1, the only difference being the microphone amplifier before the A/D converter. This will amplify the balanced analog (microphone) signal in the receive path with a fixed +16 dB. For direct connectivity of an external microphone, a software on/off switchable supply voltage is available.

For control of the 2 CODECS several registers are available:

- DTCON: for selecting the input to CODEC1
- CDVC1: the volume control register for CODEC1
- CODTR: the test mode control register for both CODECS
- CDVC2: the volume control register for CODEC2

Table 52 gives the bit assignment for CDVC1 and CDVC2.

Table 53 shows the D/A and A/D gain values in the corresponding CODEC 1/2 paths.

Table 52 CDVC1 (BBH) and CDVC2 (BCH) Bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
D/A3	D/A2	D/A1	D/A0	A/D3	A/D2	A/D1	A/D0

Table 53 D/A and A/D gain values

BIT 7 TO BIT 4	D/A GAIN	BIT 3 TO BIT0	A/D GAIN[1]	
			CODEC1[2]	CODEC2[3]
0000	−13 dB	0000	+6 dB	+22 dB
0001	−12 dB	0001	+7 dB	+23 dB
0010	−11 dB	0010	+8 dB	+24 dB
0011	−10 dB	0011	+9 dB	+25 dB
0100	−9 dB	0100	+10 dB	+26 dB
0101	−8 dB	0101	+11 dB	+27 dB
0110	−7 dB	0110	+12 dB	+28 dB
0111	−6 dB	0111	+13 dB	+29 dB
1000	−5 dB	1000	+14 dB	+30 dB
1001	−4 dB	1001	+15 dB	+31 dB
1010	−3 dB	1010	+16 dB	+32 dB
1011	−2 dB	1011	+17 dB	+33 dB
1100	−1 dB	1100	+18 dB	+34 dB
1101	+0 dB	1101	+19 dB	+35 dB
1110	+1 dB	1110	+20 dB	+36 dB
1111	+2 dB	1111	+21 dB	+37 dB

Notes

1. +3 dB digital gain of DDF hardware block not included here.
2. System application should be such that the maximum line input signal level does not exceed −6 dBm to avoid distortion. At a minimum line input level of −21 dBm full scale control the internal A/D converter can be achieved by a maximum gain setting of 21 dB.
3. System application should be such that the maximum differential microphone input signal level does not exceed −22 dBm to avoid distortion. At a minimum microphone input level of −37 dBm full scale control the internal A/D converter can still be achieved by a maximum gain setting of 37 dB. The high dynamic range of the AD converter allows for additional digital gain up to 18 dB by the DSP.

The analog and A/D D/A parts of both CODECs can be independently activated by the SYMOD register; see Table 2. Bit 4 of SYMOD is used to activate the microphone supply voltage, if the bit is logic 0 the supply is off.

The balanced microphone input has an input resistance of about 200 kΩ, and the balanced line interface input has an input resistance of about 20 kΩ. The output resistance of the balanced CODEC outputs is about 10 Ω with a typical output level of 1350 mV (RMS).

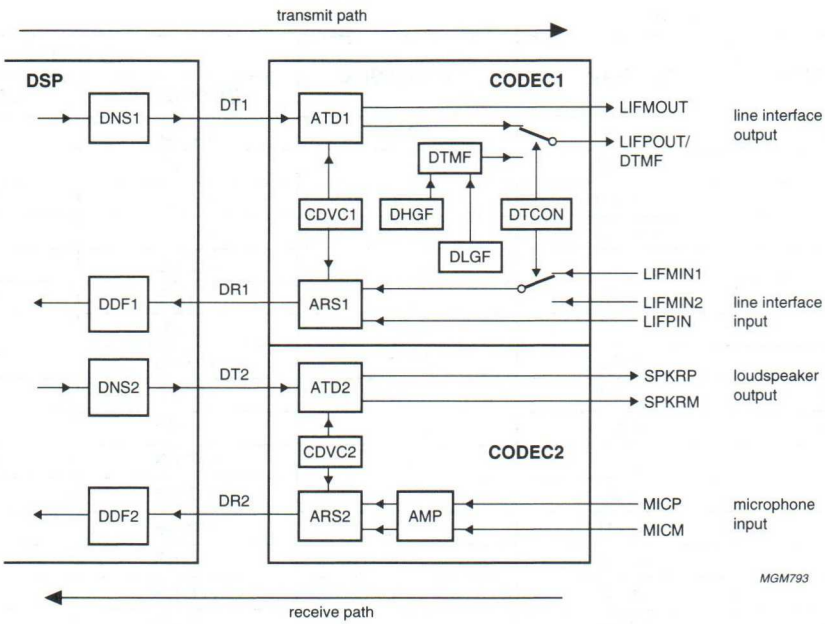


Fig.30 Block diagram of CODECs.

14 ANALOG VOLTAGE REFERENCE

14.1 Bandgap reference

The analog voltage reference circuitry includes a bandgap circuit with a nominal output voltage of about 1.25 V. This voltage is used by the power on reset block and by the analog voltage source to generate the reference voltage V_{REF}. Block AVR is always on, even in system-off mode, and will consume only a few μA of current. The output AVR is directly connected to the power on reset block and it determines the power on reset threshold levels accuracy in first order. The connection from AVR to AVS is via an internal series resistor of about 200 kΩ. The voltage after this resistor is connected to pin V_{BGP}, which allows an external capacitor (100 nF) to be connected to filter out any noise from AVR otherwise entering AVS. With this configuration the noise at pin V_{BGP} will be about −115 dBmp. The pin also allows a direct measurement of the bandgap voltage, but no current must be drawn.

14.2 Analog voltage source

The analog voltage source generates the following voltages:

- A precise reference voltage V_{REF}. The value in register VREFR determines the V_{REF}. In the application this voltage should be tuned to 2000 mV, since it will determine the absolute accuracy of the auxiliary A/D and D/A conversion, as well as the gains in the CODEC A/D and D/A paths. V_{REF} is the direct output of an opamp which can source an output current, and not sink. An external capacitor in the order of 10 to 30 μF should be connected between V_{REF} and V_{SSA} for stability and noise performance. The reference voltage can also directly supply an external electret microphone via pin V_{MIC}. The switch between V_{REF} and V_{MIC} is controlled via bit 4 in the SYMOD Special Function Register.
- An analog output voltage DAOUT. This voltage can be set between approximately 8 mV (1 LSB = $V_{REF}/256$) and V_{REF} (= 2000 mV) by changing the register GPDAR. This large range is possible while no opamp is used. This causes a relatively high output resistance with a settling time of about 10 ms. The dynamic switching of DAOUT causes the output resistance to be dependent of the actual load on DAOUT. This effect can be cancelled if an external capacitor larger than 500 pF between DAOUT and V_{SSA} is applied. This will however result in a slower settling time of the output voltage, to about 30 μs.
- The internal analog common mode voltage V_{acm}, used in the CODEC. The voltage is fixed to $V_{REF} \times 161/256$ and cannot be changed by any register.
- The internal voltage V_{adc} is used only when an A/D conversion is executed.

As mentioned above, the reference voltage V_{REF} has to be adjusted in the application to 2000 mV. For this purpose the VREFR Special Function Register has been defined. It is reset to 9AH. The reset state should ensure that the reference voltage is about 2000 mV. Exact adjustment has to be done under software control using the VREFR register, where increasing the VREFR value will decrease the reference voltage.

Table 54 VREFR (BAH) Bit assignment, reset state 9AH

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Spare	V_{REF} bit 6	V_{REF} bit 5	V_{REF} bit 4	V_{REF} bit 3	V_{REF} bit 2	V_{REF} bit 1	V_{REF} bit 0

15 IOM

15.1 Features

The IOM block in the PCD6002 is a 4-wire serial interface performing following functions:

- Digital interface with up to two 64 kbit/s channels at a bit rate of n × 256 kbit/s (n = 1, 2, 3, 4 or 8), complying with the *"IOM-2 specifications"* (IOM-2 is a registered trademark of Siemens AG).
- Digital interface with 32 slots/frame and non-doubled data clock, compatible with the digital interface of some speech CODEC ICs.
- Autonomous storing/fetching of data into/from the DSP I/O registers.
- Byte or word (16 bits) transfer

15.2 Pin description

The following pins are used by the IOM interface:

- **DI**: serial data input with a bit rate of n × 256 kbit/s (n = 1, 2, 3, 4 or 8)
- **DO**: serial data output with a bit rate of n × 256 kbit/s (n = 1, 2, 3, 4 or 8)
- **FSC**: 8 kHz frame synchronization input/output.
- **DCK**: data clock input/output. Twice the data transmission frequency on DI and DO, except in the non-doubled data clock mode (see Section 15.3).

These pins are alternative functions of P3. When activated, DO is an open-drain pin, as many devices must be able to write on the same data line in a time-multiplexed mode. Therefore DO must be externally pulled up. FSC and DCK are inputs or push-pull outputs, depending on the IOM being in slave or master mode. Activation of the IOM alternative functions of P3 and switching between slave or master mode is controlled by the SFR ALTP, bit6 and bit5 respectively (see Section 16.2 for more details).

15.3 Functional description

The digital interface of the PCD6002 can work at several bit rates, summarized in Table 55. A particular bit rate is selected by writing the 3-bit code given in the first column of the table into the IOM control register bits IOMC.15, IOMC.14, IOMC.13. Choosing the code '000' or '001' deactivates the IOM interface and stops all the transactions on the IOM bus. This is the default state after reset.

The PCD6002 IOM can be master or slave. After reset the IOM is in slave mode. Switching between slave or master mode is controlled by the SFR ALTP, bit 6 and bit 5 respectively (see Section 16.2 for more details). In slave mode both FSC and DCK are inputs. In master mode both FSC and DCK are outputs. In master mode FSC and DCK are generated by the TICB (see Section 9.1). Master mode should only be used in combination with the bit rate 768 kbit/s.

FSC is an 8 kHz framing signal for synchronizing data transmission on DI and DO. The rising edge of FSC gives the time reference for the first bit transmitted in the first slot of a speech frame. The number of slots per speech frame depends on the selected data rate. Each slot contains 8 data bits.

DCK is a data clock. Its frequency is twice the selected data rate in IOM mode. In Speech mode, the DCK frequency is equal to the data rate (2048 kHz for 2048 kbit/s).

DI is the serial data input. Data coming on DI in packets of 8 bits (A-law PCM encoded data) or 16 bits (linear PCM data) is stored temporarily in an IOM data buffer, from where it is processed by the on-chip DSP. On the other hand, data written into the IOM data buffers by the DSP is shifted out on pin DO.

There are two IOM data buffers, allowing the use of two 8-bit channel. One channel is 64 kbit/s in case of A-law PCM encoded data and 128 kbit/s if linear PCM data is transferred, in which case two consecutive slots are used.

The Speech mode was implemented to support the Codec interface of some speech compression ICs. This mode is very similar to the IOM 32 slots mode, the main difference being the non-doubled data clock. See Section 15.6 for timing information.

Table 55 IOM modes

CODE (IOMC[15:13])	MODE
000 or 001	Inactive (default after reset)
010	IOM slave mode, 256 kbit/s in 4 slots/speech-frame
011	IOM slave mode, 512 kbit/s in 8 slots/speech-frame
100	IOM master/slave mode, 768 kbit/s in 12 slots/speech-frame
101	IOM slave mode, 1024 kbit/s in 16 slots/speech-frame
110	Speech slave mode, 2048 kbit/s in 32 slots/speech-frame(1)
111	IOM slave mode, 2048 kbit/s in 32 slots/speech-frame

Note

1. The Speech mode is similar to the IOM slave 32 slots mode, but with a non-doubled data clock DCK.

15.4 IOM data buffers

Table 56 and 57 show the two 16-bit DSP registers used as data buffers: IOMDI for storing inbound data and IOMDO for the outbound data. The high bytes store the data of buffer 1, the low bytes the data of buffer 0.

Table 56 IOMDI bit assignment, reset state 00H

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	IOM inbound data buffer 1								IOM inbound data buffer 0							

Table 57 IOMDO bit assignment, reset state 00H

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	IOM outbound data buffer 1								IOM outbound data buffer 0							

15.5 IOM control register

The bit rates, the selection of active slots on the IOM interface and the logic connection between an IOM slot and an IOM data buffer is defined in the IOM control register IOMC. The IOM modes which can be selected are listed in Table 55.

Writing of the IOMC register is done via the API software (Application Programming Interface). Please refer to the API specification for more details.

Table 58 IOMC bit assignment, reset state 00H

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	IOM Mode select			IOM buffer 0: slot position					spare	buffer 0 active	buffer 1 active	IOM buffer 1: slot position				

15.6 Timing

The timing on the 4-wire interface is given in Fig.31 and Table 59 for the IOM mode, and in Fig.32 and Table 60 for the Speech mode.

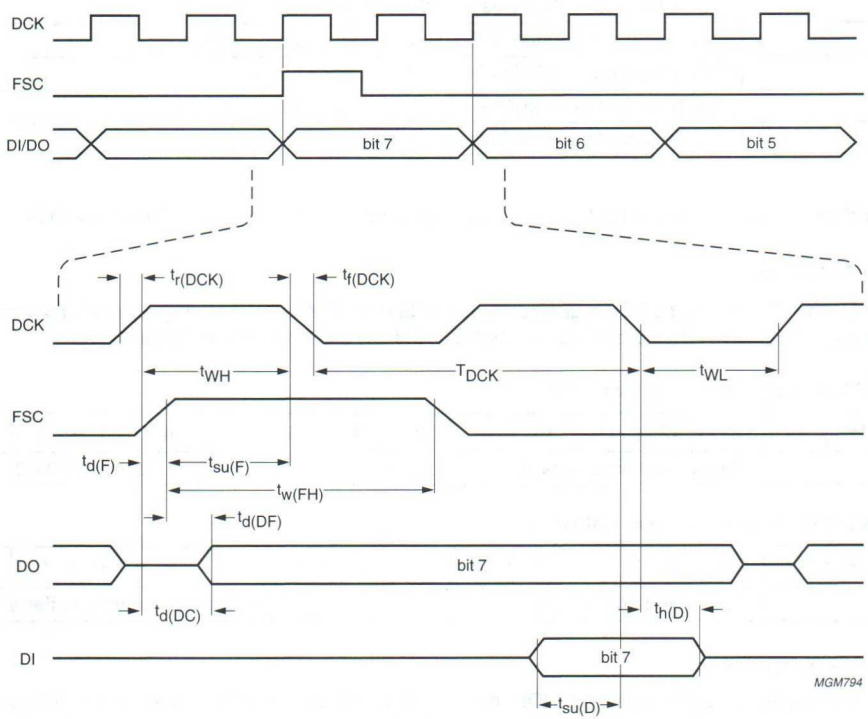


Fig.31 4-wire interface timing in IOM mode

Table 59 Timing parameters in IOM mode

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
$t_{r(DCK)}$	data clock (DCK) rise time	–	60	ns
$t_{f(DCK)}$	data clock (DCK) fall time	–	60	ns
T_{DCK}	data clock (DCK) period	220[1]	–	ns
t_{WH}	data clock (DCK) high time pulse width	80	–	ns
t_{WL}	data clock (DCK) low time pulse width	80	–	ns
$t_{r(FSC)}$	frame sync (FSC) rise time	–	60	ns
$t_{f(FSC)}$	frame sync (FSC) fall time	–	60	ns
$t_{d(FSC)}$	frame sync (FSC) delay time	$-t_{WL}$	60	ns
$t_{su(FSC)}$	frame sync (FSC) set-up time	60	–	ns
t_{WFH}	frame sync (FSC) high time pulse width	130	–	ns
$t_{d(DC)}$	output data (DO) to data clock delay time	–	100[2]	ns
$t_{d(DF)}$	output data (DO) to frame sync delay time	–	150[2]	ns
$t_{su(D)}$	input data (DI) set-up time	t_{WH}	–	ns
$t_{h(D)}$	input data (DI) hold time	50	–	ns

Notes

1. Corresponds to the highest DCK frequency allowed (4.096 MHz) with a 10% margin.
2. Condition C_L = 150 pF.

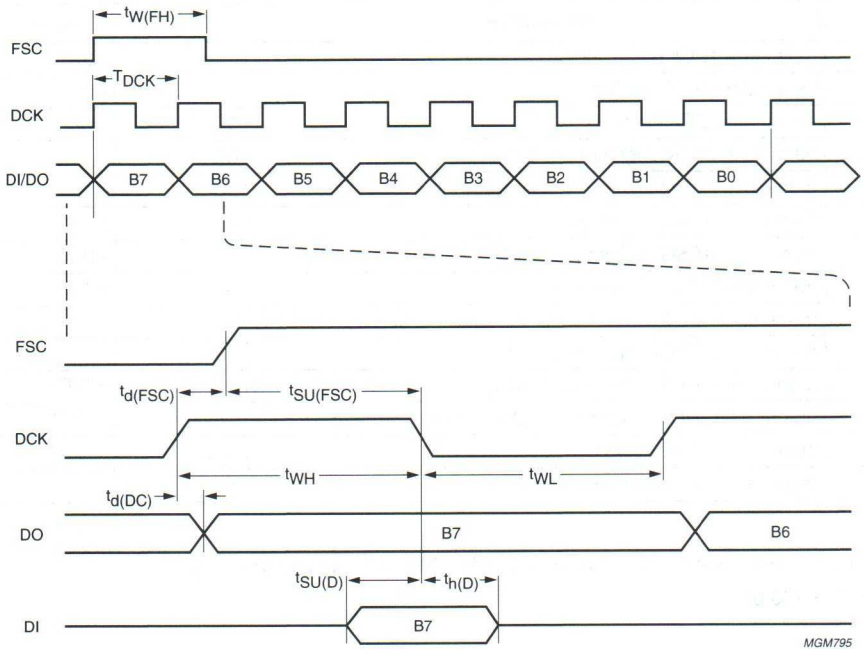


Fig.32 4-wire interface timing in Speech mode

Table 60 Timing parameters in Speech mode

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
$t_{d(FSC)}$	frame sync (FSC) delay time	$-t_{WL}$	100	ns
$t_{su(FSC)}$	frame sync (FSC) set-up time	60	–	ns
t_{WFH}	frame sync (FSC) high time pulse width	130	–	ns
T_{DCK}	data clock (DCK) period	440(1)	–	ns
t_{WH}	data clock (DCK) high time pulse width	150	–	ns
t_{WL}	data clock (DCK) low time pulse width	150	–	ns
$t_{d(DC)}$	output data (DO) to data clock delay time	–	100(2)	ns
$t_{su(D)}$	input data (DI) set-up time	60	–	ns
$t_{h(D)}$	input data (DI) hold time	60	–	ns

Notes

1. Corresponds to the DCK frequency (2.048 MHz) with a 10% margin.
2. Condition CL = 150 pF.

16 EXTERNAL I/O INTERFACES

16.1 External analog interfaces

16.1.1 General purpose A/D and D/A

For general use like for instance battery management, parallel set detection or speaker amplifier volume control a 2 line multiplexed 8-bit A/D converter and a 8-bit D/A converter are on board the chip. The A/D and D/A converters consist of several analog sub blocks called AVS and AAD, which are controlled by the digital block DCA (see Fig.33). Block AVS generates voltages in a time multiplexed way, and as such is a D/A converter with the bandgap voltage V_{BGP} as input voltage. Block AAD contains a comparator that is part of the successive approximation A/D converter formed by a combination of AVS, AAD and DCA. The A/D conversion can be performed on two external input signals AD0IN and AD1IN.

The whole circuit is active as long as the chip is in system-on mode. Both the A/D and D/A converters can be controlled by the microcontroller, the Special Function Register mapped DCA block, allowing the user a flexible interface to analog peripherals.

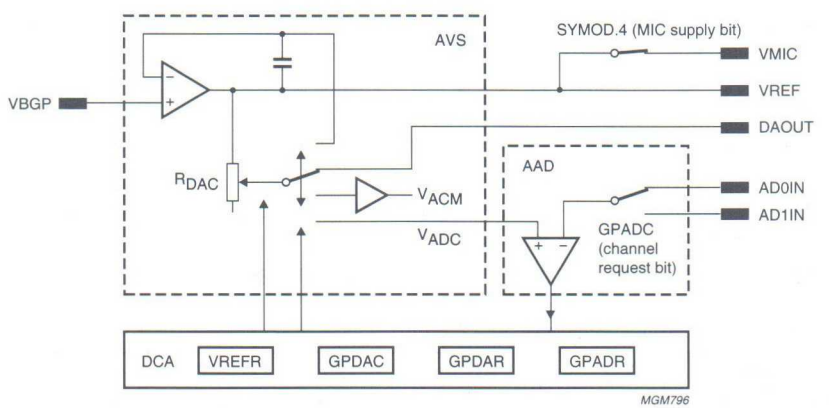


Fig.33 The architecture of the auxiliary D/A and A/D converter.

16.1.2 General purpose A/D

The A/D converter on the chip is a two channel multiplexed 8-bit converter. The control of this converter is done via two bits in the microcontroller GPADC SFR. One bit selects the channel and the other bit is the converter request bit. The request bit is reset by hardware when the converter has finished it's conversion cycle. The A/D converter (AAD in Fig.33), is of the successive approximation type.

An internal register contains the value of the slider position and is changed after each comparison of V_{adc} with one of the two possible A/D inputs (AD0IN and AD1IN). After 8 comparisons the conversion is finished and the contents of the internal register is copied in to the register GPADR. The conversion time will be less than 30 µs. This register can in turn be read by the internal microcontroller.

Table 61 GPADC (C3H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Spare	Spare	Spare	Spare	Spare	Automatic A/D conversion[1]	Channel select[2]	Request confirm

Notes

1. Automatic A/D conversion is performed every 30 ms if this bit is logic 1 – regardless of state of Request confirm bit.
2. Channel select = 0, A/D conversion input is on pin AD0IN.
   Channel select = 1, A/D conversion input is on pin AD1IN.

Table 62 GPADR (C2H) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Result A/D7	Result A/D6	Result A/D5	Result A/D4	Result A/D3	Result A/D2	Result A/D1	Result A/D0

In the GPADR register the 8-bit result value from the conversion is presented. The conversion range is 0 to 2000 mV (V_{REF}) with 8 mV resolution.

16.1.3 General purpose D/A

The D/A converter on the chip is a single channel 8-bit converter. The control of this converter is done via the GPDAR register.

The value written in this register triggers the conversion which will be present at the output pin after the DA conversion cycle (<10 µs). The range from the DA output is 0 to 2000 mV (V_{REF}).

The conversion principle for both A/D and D/A conversion is shown in Fig.34.

Table 63 GPDAR (C4H) bit assignment, reset state 80H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Output D/A7	Output D/A6	Output D/A5	Output D/A4	Output D/A3	Output D/A2	Output D/A1	Output D/A0

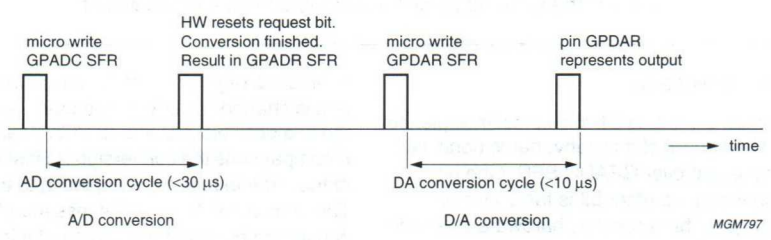


Fig.34 A/D and D/A conversion principle.

16.2 External digital Interfaces

For control of peripherals like a display, ringer, key pad and line interface a large number of general purpose digital I/O pins are available in addition to the Flash memory, LCD control pins and MSK or IOM modem pins. The exact number of free I/O pins depends on the choice of peripherals that make up the system configuration. In case all alternate port functions of P1 and P3 are used, 10 input lines remain available on P1 and P3 of which 7 are programmable for interrupts. I/O ports P1 and P3 are 'weak pull up' types which can therefore be used either as inputs or outputs. The reset value of P1 and P3 is FFH (input mode). In output mode for driving with a logic 1 (weak pull up) the external load of P1 and P3 should be equivalent to >100 kΩ, for 'driving' with a logic 0 the sink current should not exceed 4 mA. In addition to P1 and P3 there are 16 output ports available at P2 and MA. Output ports P2 and MA are push pull ports and their reset value is 00H (output 00H). The driving level of P2 and MA is 4 mA for either logic 0 or logic 1. Port P4 provides the Flash memory and display control signals. The P1, P3, and P4 I/O lines are available as SFR bit-addressable I/O registers in the configuration shown in Fig.35, while P2 and MA are (not bit addressable) XDATA mapped ports when EAN = 1.

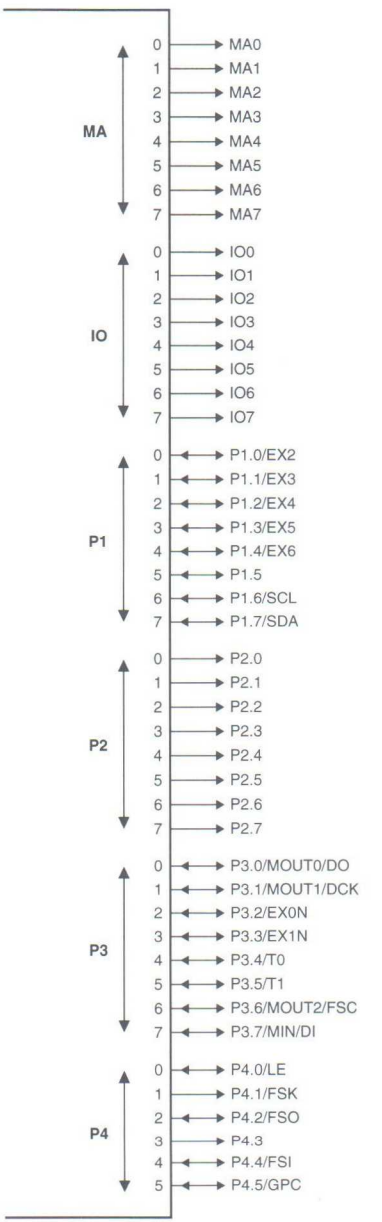


Fig.35 DTAM general purpose digital I/O configuration.

The MA and P2 ports are described in Chapter 12. The configuration of ports P1 and P3 are described in the tables below.

Table 64 P1 (90H) Bit assignment, bit addressable, reset state FFH

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P1.7/SDA	P1.6/SCL	P1.5	P1.4/EX6	P1.3/EX5	P1.2/EX4	P1.1/EX3	P1.0/EX2

Note

1. The alternative outputs (SDA, SCL) are connected with the general purpose outputs via an AND. Therefore when using the alternative functions the corresponding port bits should be set to a logic 1.

Table 65 P1 pin configuration

PORT PINS	CONFIGURATION
P1.7, P1.6	open-drain
P1.5 to P1.0	quasi-bidirectional

For control of I^2C peripherals like for instance EEPROMs and LCD displays, P1.6 and P1.7 can also be used as SDA and SCL to support I^2C. See Section 10.13 on how to activate this alternative function of P1.6 and P1.7. The rest of port 1 is defined as general purpose I/O pins like the standard 80C51 microcontroller.

Table 66 P3 (B0H) Bit assignment, bit addressable, reset state FFH

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P3.7/ MIN/ DI	P3.6/ MOUT2/ FSC	P3.5/T1	P3.4/T0	P3.3/EX1N	P3.2/EX0N	P3.1/ MOUT1/ DCK	P3.0/ MOUT0/ DO

Note

1. The alternative outputs (MOUT2, MOUT1, MOUT0, FSC, DCK, DO) are connected with the general purpose outputs via a AND. Therefore when using the alternative functions the corresponding port bits should be set to a logic 1.

Table 67 P3 pin configuration

PORT PINS	CONFIGURATION
P3.7, P3.6, P3.1, P3.0	see Table 68
P3.5 to P3.2	quasi-bidirectional

Port 3 is defined as a set of 8 general purpose I/O pins like the standard 80C51 microcontroller except for P3.6 and P3.7 which do not have the RDN and WRN functionality (the RDN and WRN are separate pins). Table 68 gives the different functions and the corresponding port configurations available on P3.7, P3.6, P3.1 and P3.0. The last column gives the function and configuration after reset.

Table 68 Port 3.7,3.6,3.1,3.0 modes and configuration

MSK		IOM			GENERAL PURPOSE I/O PORT (RESET STATE)	
			MASTER	SLAVE		
MOUT0	push-pull	DO	open-drain 4 mA	open-drain 4 mA	P3.0	quasi-bidirectional weak pull-up
MOUT1	push-pull	DCK	push-pull	input	P3.1	
MOUT2	push-pull	FSC	push-pull	input	P3.6	
MIN	input	DI	input	input	P3.7	

Table 69 shows how the pin configuration required for the MSK, IOM master/slave and general purpose function can be selected with the Alternative Port function register bits ALTP.6 and ALTP.5

Table 69 P3.7, P3.6, P3.1, P3.0 selection of pin configurations for alternative function.

ALTP.6	ALTP.5	MODE
0	0	General Purpose I/O port
0	1	MSK
1	0	IOM slave
1	1	IOM master

Table 70 P4 (98H) Bit assignment, bit addressable, reset state 1EH

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
–	–	P4.5/GPC	P4.4/FSI	P4.3	P4.2/FSO	P4.1/FSK	P4.0/LE

Note

1. The alternative outputs (GPC, FSO, FSK, LE) are connected with the general purpose outputs via a AND. Therefore when using the alternative functions the corresponding port bits should be set to a logic 1.

Table 71 P4 pin configuration

PORT PINS	CONFIGURATION
P4.5	open-drain (if ALTP.4 = 0) or push-pull (if ALTP.4 = 1)
P4.4, P4.2, P4.0	open-drain
P4.3	open-drain, write only, 5 V tolerant
P4.1	open-drain, write only, double drive (8 mA)

The ALTP Special Function Register is defined in Table 72.

Table 72 ALTP (ABH) bit assignment, reset state 00H

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Spare	IOM on P3	IOM master/ MSK	P4.5 OD/PP	GPC On/Off	GPC source	LE On/Off	Early LE

Notes

1. The General Purpose Clock function is described in more detail at the end of Section 9.1.
2. The LE functionality is described in more detail in Section 10.16.

17 ELECTRICAL SPECIFICATION

17.1 Limiting values

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	3.6	V
V_I	input voltage on any pin with respect to ground (V_{SS})	−0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation	–	800	mW
T_{stg}	storage temperature	−65	+150	°C

17.2 Supply characteristics

SYMBOL	PARAMETER	CONDITIONS / REMARKS	MIN.	TYP.	MAX.	UNIT
V_{DD3V}	digital supply voltage to pins V_{DD3V1}, V_{DD3V2}, V_{DD3V3}	–	2.7	3.0	3.3	V
V_{DDA}	analog supply voltage to pin V_{DDA}	–	2.7	3.0	3.3	V
V_{DDPLL}	analog supply voltage to pin V_{DDPLL}	–	2.7	3.0	3.3	V
V_{PP}	programming voltage	–	12.5		13.0	V
$I_{DD(max)}$	total input current when recording a message from PSTN, CAS, Line Echo Cancellation, Listen in on CODEC2 to all supply pins	PLL on, CODEC1 and CODEC2 active, DSP at 28 MHz, microcontroller at 21 MHz, no load		35	tbf	mA
	V_{DD3V1} only			26		mA
	V_{DD3V2} only			2		mA
	V_{DD3V3} only			2		mA
	V_{DDA} only			4		mA
	V_{DDPLL} only			2		mA
$I_{DD(POTS)}$	POTS mode supply current to all supply pins	PLL off, DSP off, CODECs off, XTAL and microcontroller run at 3.58 MHz, DTMF on, no load		3		mA
$I_{DD(sys.\ off)}$	total input current when in system off mode			0.4	tbf	mA
POR (Power-on-reset)						
V_{TRH}	POR threshold value high	note 1	tbf	2.0	tbf	V
V_{TRL}	POR threshold value low	note 1	tbf	1.8	tbf	V
V_{HYS}	POR hysteresis	note 1	tbf	0.2		V
OSC						
$C_{LX1,2}$	Crystal Load capacitances at XTAL1 and XTAL2 to VSS	3.58 MHz		39		pF
		13.824 MHz		18		pF

Note

1. The POR responds to $V_{DDA} - V_{SSA}$.

17.3 Digital I/O

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IL}	LOW-level input voltage					
	SDA, SCL		0	–	$0.3V_{DD}$	V
	other pins		0	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage					
	SDA, SCL		$0.7V_{DD}$	–	V_{DD}	V
	other pins		$0.8V_{DD}$	–	V_{DD}	V
V_{OL}	LOW-level input voltage					
	SDA, SCL		0	–	$0.3V_{DD}$	V
	other pins		0	–	$0.2V_{DD}$	V
V_{OH}	HIGH-level input voltage					
	SDA, SCL		$0.7V_{DD}$	–	V_{DD}	V
	other pins		$0.8V_{DD}$	–	V_{DD}	V
$\lvert I_{OL} \rvert$	LOW-level output current	note 1				
	CEN, RDN, WRN, PSEN, P0, P1, P2, P3, P4.0, P4.2, P4.4, P4.5, MA		4	–	–	mA
	P4.1		8	–	–	mA
I_{OH}	HIGH level output current	note 1				
	PSEN, P0, P2, MA		4	–		mA
	P1.0, P1.1, P1.2, P1.3, P1.4, P1.5, P3		tbf[2][3]	–	tbf	µA

Notes

1. V_{DD} – VOUT = 400 mV (for $\lvert I_{OL} \rvert$), VOUT – V_{SS} = 400 mV (for I_{OH}).
2. On a LOW-to-HIGH transition, the output current value will be 4 mA for one micro controller clock period, before changing to the specified lower value.
3. If the MSK mode is activated, the output current value for P3.0, P3.1 and P3.6 will continuously be 4 mA. If the IOM master mode is activated, the output current value for P3.1 and P3.6 will continuously be 4 mA.

17.4 Analog supplies and general purpose AD/DA converter

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BGP}	AVR bandgap voltage	note 1	tbf	1.20	tbf	V
V_{REF}	Reference voltage	notes 2 and 3	tbf	2000	tbf	mV
R_{DAOUT}	DAOUT output resistance				tbf	kΩ
V_{DAOUT}	DAOUT output voltage		8		V_{REF}	mV
$V_{ADIN1,2}$	ADIN1, ADIN2 input voltage range		0		V_{REF}	mV
$V_{ADIN,OFS}$	ADIN1, ADIN2 input offset voltage		tbf	-50 to +50	tbf	mV
$R_{ADIN1,2}$	ADIN1, ADIN2 input resistance		tbf	200 to 500	tbf	kΩ

Notes

1. V_{BGP} output current is zero. Decoupling capacitance between V_{BGP} and V_{SSA} is 100 nF. Value at 25 °C. The bandgap has a temperature coefficient between −0.2 and +0.2 mV/°C.
2. V_{REF} output current is zero. Decoupling capacitance between V_{REF} and V_{SSA} is between 1 µF and 100 µF, with a 100 nF capacitance in parallel. The voltage is programmed by setting in register RVREF. The output can only source current (i.e. not sink).
3. Pin V_{MIC} is internally connected to V_{REF} via a switch. The V_{MIC} switch is closed by setting SYMOD.4 = 1. The V_{MIC} DC output current is max. 400 µA, and V_{REF} must be programmed to its typical value. For the connections of V_{MIC} to a microphone see Fig.36. V_{MIC} adjustment can only be done by adjusting V_{REF}.

17.5 DTMF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DTMF(LG)}$	DTMF level, low group, at LIFPOUT	RMS values	125	142	160	mV
$V_{DTMF(HG)}$	DTMF level, high group, at LIFPOUT	RMS values	158	181	205	mV

17.6 CODECs

V_{REF} is tuned to 2.0 V. Unless mentioned differently, typical values for the A/D and D/A filter characteristics conform to the G.712 specification.

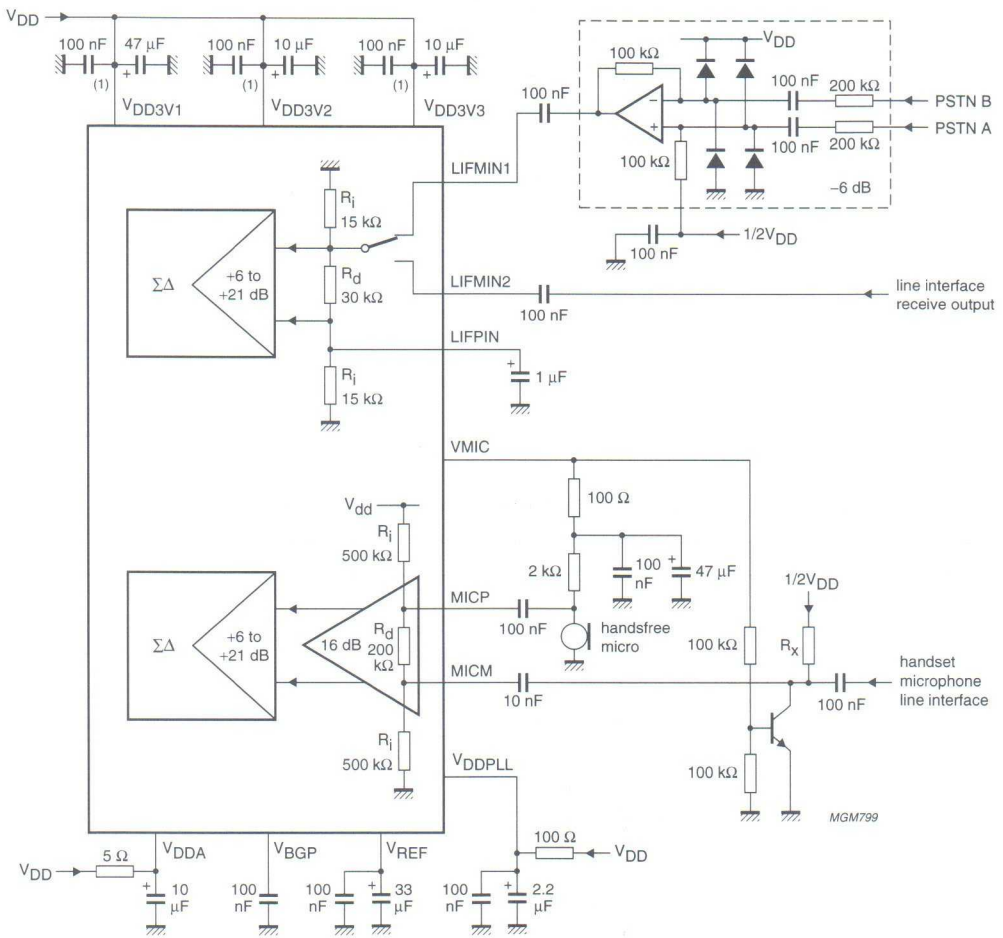
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{MICIN}	Microphone input level	notes 1 and 2			–22	dBm
R_{MICDM}	Microphone input resistance, differential mode	note 3		200		kΩ
R_{MICCM}	Microphone input resistance, common mode	note 3		500		kΩ
V_{LIFIND}	Differential input level between LIFPIN and LIFMIN1 or LIFMIN2	notes 1 and 4			–6	dBm
V_{LIFINS}	Single ended input level at LIFMIN1 or LIFMIN2 with LIFPIN AC ground	notes 1 and 5			–12	dBm
$R_{LIFINDM}$	LIFPIN to LIFMIN1 or LIFMIN2 input resistance, differential mode	note 6		30		kΩ
$R_{LIFINCM}$	LIFPIN, LIFMIN1, LIFMIN2 input resistance, common mode	note 6		15		kΩ
$\delta G_{MIC(A/D)}$	delta A/D path gain of CODEC2 from MIC to PCM	notes 1 and 7	tbf	0	tbf	dB
$\delta G_{LIF(A/D)}$	delta A/D path gain of CODEC1 from LIF to PCM	notes 1 and 8	tbf	0	tbf	dB
$\delta G_{(D/A)}$	delta D/A path gain from PCM to SPKR or LIFOUT	notes 1 and 9	tbf	0	tbf	dB
G_{step}	gain difference between adjacent steps	notes 1 and 10	tbf	1	tbf	dB
$F_{(A/D)(idle)}$	A/D idle channel noise	notes 1 and 11		–85	-tbf	dBm0p
$S/(N+THD)_{(A/D)(-25)}$	A/D Signal-to-(Noise + Total Harmonic Distortion) Ratio for CODEC2	notes 1 and 12	tbf	60		dBp
$S/(N+THD)_{(A/D)(-65)}$		notes 1 and 13		40		dBp
$S/(N+THD)_{(A/D)(-9)}$	A/D Signal-to-(Noise + Total Harmonic Distortion) Ratio for CODEC1	notes 1 and 14	tbf	60		dBp
$S/(N+THD)_{(A/D)(-49)}$		notes 1 and 15		40		dBp
$t_{d(g)(A/D)}$	A/D-path group delay			500		µs
$V_{LIFOUTD}$	Line interface differential output level	note 16		1350		mV
R_{LIFOUT}	Line interface output resistance			15		Ω
V_{SPKRD}	Speaker output, Differential level	note 17		1350		mV
R_{SPKR}	Speaker output resistance			15		Ω
$F_{(D/A)(idle)}$	D/A idle channel noise	notes 1 and 18		–85	-tbf	dBmp
$S/(N+THD)_{(D/A)(0)}$	D/A Signal-to-(Noise + Total Harmonic Distortion) Ratio	notes 1 and 19	tbf	70		dBp
$S/(N+THD)_{(D/A)(-40)}$		notes 1 and 20		40		dBp
$t_{d(g)(D/A)}$	D/A-path group delay			500		µs

Notes

1. For the definition of the amplitude units (dB, dBm, dBm0, dBmp, dBm0p) see Section 13.1.
2. Sinewave RMS level applied differentially between pins MICP and MICM. V_{REF} is tuned to 2.0 V and the A/D path gain in control register CDVC2 = 00H is set to +22 dB (minimal gain for CODEC2). For larger input levels the output signal will saturate.

3. The differential resistance is seen between pins MICP and MICM, and the common mode resistance is seen between MICP and V_{SSA} or MICM and V_{SSA}.
4. Sinewave rms level applied differentially between pins LIFP and LIFM. V_{REF} is tuned to 2.0 V and the A/D path gain in control register CDVC1 = 00H is set to +9 dB (minimal gain for CODEC1). For larger input levels the output signal will saturate.
5. Sinewave rms level applied between V_{SSA} and LIFMIN1 or LIFMIN2. LIFPIN is connected to V_{SSA} via a capacitor (see Fig.36). V_{REF} is tuned to 2.0 V and the A/D path gain in control register CDVC1 is set to +9 dB. For larger input levels the output signal will saturate.
6. The differential resistance is seen between pins LIFP and LIFMIN1 or LIFM, and the common mode resistance is seen between LIFP and V_{SSA} or LIFM and V_{SSA}.
7. The deviation of the absolute gain as specified in CDVC2, measured at 1020 Hz.
8. The deviation of the absolute gain as specified in CDVC1, measured at 1020 Hz.
9. The deviation of the absolute gain as specified in CDVC1/CDVC2, measured at 1020 Hz.
10. The difference between two adjacent gain settings as specified in CDVC1/CDVC2. Valid for both A/D and D/A path.
11. The A/D path gain for CODEC1 is set to +9 dB and for CODEC2 is set to +24 dB (CDCV1/2 = 00H). LIFPIN and LIFMIN1 or LIFMIN2 are shorted together, for CODEC1 and MICP and MICM are shorted together for CODEC2. The measured value is psophometrically weighted.
12. The A/D path gain in control register CDVC2 = 00H is set to +24 dB for CODEC2, when a sinewave of 1020 Hz with a level of –24d Bm is applied between MICP and MICM. The value includes harmonic distortion and is psophometrically weighted.
13. The A/D path gain in control register CDVC2 = 00H is set to +24 dB for CODEC2, when a sinewave of 1020 Hz with a level of –65 dBm is applied between MICP and MICM. The value includes harmonic distortion and is psophometrically weighted.
14. The A/D path gain in control register CDVC1 = 00H is set to +9 dB for CODEC1, when a sinewave of 1020 Hz with a level of –9 dBm is applied between LIFPIN and LIFMIN1 or LIFMIN2. The value includes harmonic distortion and is psophometrically weighted.
15. The A/D path gain in control register CDVC1 = 00H is set to +9 dB for CODEC1, when a sinewave of 1020 Hz with a level of –49 dBm is applied between LIFPIN and LIFMIN1 or LIFMIN2. The value includes harmonic distortion and is psophometrically weighted.
16. Sinewave rms level applied differentially between pins LIFPIN and LIFMIN1 or LIFMIN2. V_{REF} is tuned to 2.0 V and the A/D path gain is set to +9 dB and the D/A path gain is set to +2 dB (CDVC1 = F0H). The input signal is 970 Hz with a level of +3.14 dBm0 at the PCM interface. Load resistance is larger than 120 Ω.
17. Sinewave rms level applied differentially between pins SPKRP and SPKRM. V_{REF} is tuned to 2.0 V and the A/D path gain is set to +24 dB and the D/A path gain is set to +2 dB (CDVC2 = F0H). The input signal is 970 Hz with a level of +3.14 dBm0 at the PCM interface. Load resistance is larger than 120 Ω.
18. The D/A path gain for CODEC1 and CODEC2 is set to 0 dB (CDVC1/2 = D0H). The DSP is in idle mode. The value is differentially measured and psophometrically weighted.
19. The D/A path gain in control register CDVC1/2 = D0H is set to 0 dB for CODEC1 and CODEC2, when a bit stream representing a sinewave of 970 Hz with a level of 0 dBm0 is applied at the PCM interface (DSP output). The value includes harmonic distortion and is psophometrically weighted. The load between SPKRM and SPKRP or LIFMOUT and LIFPOUT is 200 pF in parallel to 150 Ω and 800 μH
20. The D/A path gain in control register CDVC1/2 = D0H is set to 0 dB for CODEC1 and CODEC2, when a bit stream representing a sinewave of 970 Hz with a level of –40 dBm0 is applied at the PCM interface (DSP output). The value includes harmonic distortion and is psophometrically weighted. The load between SPKRM and SPKRP or LIFMOUT and LIFPOUT is 200 pF in parallel to 150 Ω and 800 μH.

18 APPLICATION DIAGRAMS



(1) The decoupling capacitors for V_{DD3V1}, V_{DD3V2} and V_{DD3V3} must be mounted as close as possible to the respective pins.

Fig.36 Supply connections and analog input connections for Line Interface, Caller ID and Handsfree.

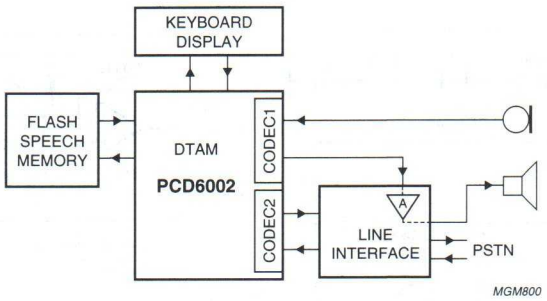


Fig.37 Stand alone digital answering machine with handsfree application example.

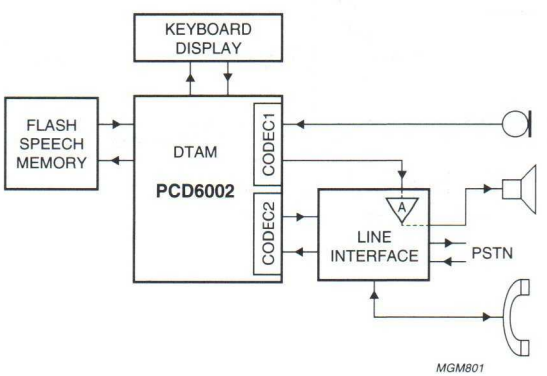


Fig.38 Digital telephone answering machine with handsfree application example.

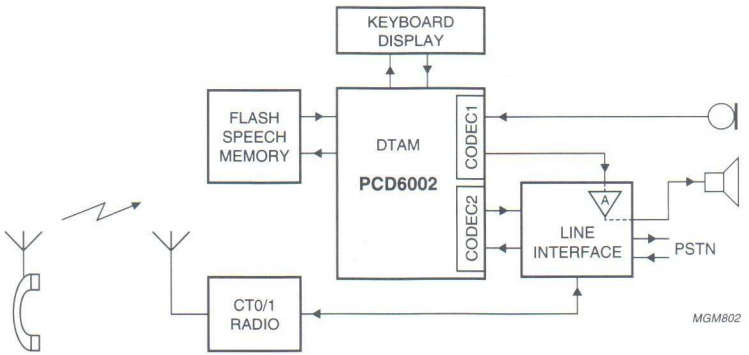


Fig.39 Analog cordless base station with digital handsfree answering machine application example.

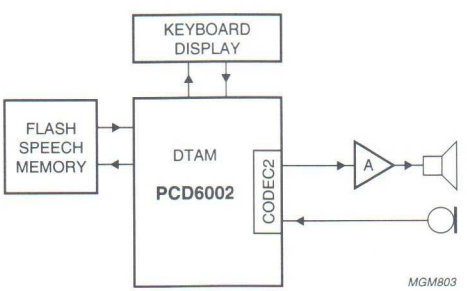


Fig.40 Portable voice memo recorder application example.

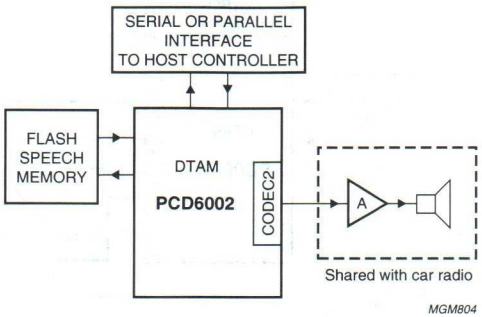


Fig.41 Automotive application example (audible car status information is presented to the driver).

ADVANCED TELEPHONY SERVICES ICs

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19 FEATURES

- Bellcore's 'CPE Alerting Signal (CAS)' and BT's 'Loop State Tone Alert Signal' detection
- BT's 'Idle State Tone Alert Signal' by means of monitoring the input signal level.
- 1200 baud FSK (Frequency Shift Keying) demodulator conform Bell 202 and CCITT V23 standards
- Ring or polarity change detector
- Ring period measurement
- Low battery comparator
- Signal level detector
- On-hook and off-hook application according to *"Bellcore TR-NWT-000030"* and *"SR-TSV-002476"* specifications
- Receive sensitivity of –37.8 dBm (in 600 Ω) for CAS
- 2.5 to 3.6 V supply; low power standby mode
- Selectable 1 second or 1 minute timebase interrupt
- 3.58 MHz and 32.768 kHz crystal oscillators
- SO16 package.

20 APPLICATIONS

- Analog Display Services Interface (ADSI) phones
- Feature phones and adjunct boxes with Bellcore CID (Caller-ID), CIDCW (Caller-ID on Call Waiting) and CNAM (Caller-Name) systems
- Computer Telephony Integrated (CTI) systems.

21 GENERAL DESCRIPTION

The PCD3316 is a low power mixed signal CMOS integrated circuit for receiving physical layer signals like Bellcore's CAS and the signals used in similar services. The device is capable of a very high precision detection of the dual tone (2130 and 2750 Hz) by using a patented digital algorithm. The PCD3316 can be used for on-hook and off-hook CID, CIDCW and CNAM applications.

For timing purposes the PCD3316 can be programmed to generate an interrupt signal to the microcontroller every second or every minute. These timings are derived from an on chip 32.768 kHz oscillator.

Also incorporated in the device are an FSK receiver/demodulator and a Ring or Polarity Change detector.

The status of the PCD3316, the received FSK data bytes and the ringer period can be read and many options can be selected via the I²C-bus serial interface.

Two on-chip oscillators are available.
One 3.58 MHz oscillator for all internal functions and a low frequency 32.768 kHz oscillator for the 1 second or 1 minute timing.

In Power-down mode only the polarity comparators and the 32.768 kHz oscillator are active. The CAS detection, the FSK receiver and the 3.58 MHz oscillator can be enabled separately. Detection of a polarity change on the inputs POL0 or POL1, the reception of an FSK data byte, the detection of a CAS tone or a timebase interrupt is signalled to the microcontroller by an interrupt request signal (IRQ). The microcontroller can communicate with the PCD3316 device via the serial interface.

The PCD3316 is designed for use in a microcontroller controlled system.

The device is available in a SO16 package.

A demonstration board OM5843 is available.

22 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3316T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

5 BLOCK DIAGRAM

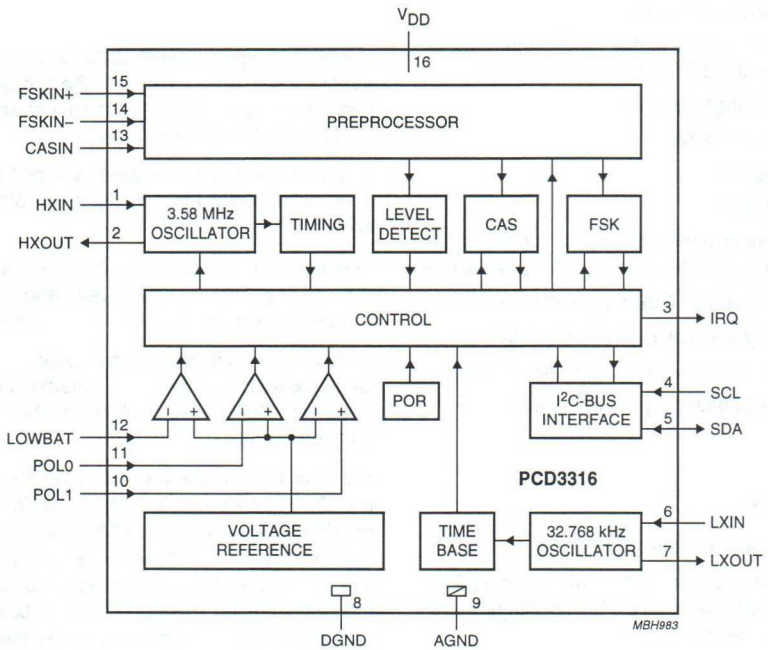


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
HXIN	1	I	3.58 MHz crystal oscillator input
HXOUT	2	O	3.58 MHz crystal oscillator output
IRQ	3	O	interrupt output; programmable active HIGH or active LOW
SCL	4	I	serial clock line of I^2C-bus
SDA	5	I/O	serial data line of I^2C-bus
LXIN	6	I	32.768 kHz crystal oscillator input
LXOUT	7	O	32.768 kHz crystal oscillator output
DGND	8	–	digital ground
AGND	9	–	analog ground
POL1	10	I	polarity detector input 1
POL0	11	I	polarity detector input 0
LOWBAT	12	I	low battery detector input
CASIN	13	I	input pin for CAS signal
FSKIN–	14	I	negative input for FSK signal
FSKIN+	15	I	positive input for FSK signal
V_{DD}	16	–	supply

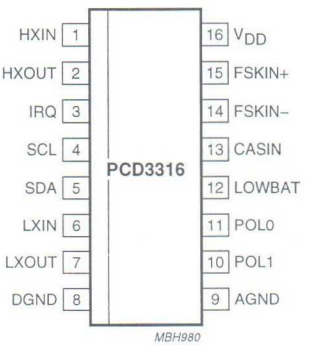


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Preprocessor and analog inputs

The preprocessor for the CAS detection and the FSK receiver incorporates an A/D converter and a digital bandpass filter.

The LOWBAT input of the PCD3316 can be used for low battery detection. The voltage on the LOWBAT pin is compared with an internal voltage reference circuit. When the LOWBAT voltage drops below the reference voltage, Status register, bit 5 is set to logic 1.

The PCD3316 can be forced in a Power-down state by switching off the 3.58 MHz system clock and the A/D converter. This is done by setting Mode register 2, bit 7 to logic 0. To guarantee correct operation the following order of actions must be performed: (see also Section 7.8 about interrupts)

1. Switch off CAS and FSK detection (if turned on)
2. Read the interrupt register (thus clearing pending interrupts generated by the CAS and FSK detector)
3. Switch off the 3.58 MHz oscillator by clearing bit 7 of Mode register 2.

Two low power comparators (inputs POL0 and POL1) and the 32.768 kHz clock are always active. They can be used for ring or line polarity reversal detection. The POL on/off bit (Mode register 1, bit 4) must be set to enable generation of an interrupt when a polarity change occurs. The result of the two comparators can be read in bits 7 and 6 (POL0 and POL1) of the Status register (see Section 7.4).

No 3.58 MHz clock is needed for the generation of a polarity interrupt.

7.2 CAS detection

After a Power-on reset or after enabling the CAS detector the internal registers of the CAS detection function are initialized. The initialization takes a maximum of 100 periods of the 3.58 MHz clock.

If the CAS detection is enabled the PCD3316 will generate an interrupt (Interrupt register, bit 1 is set) when a correct dual tone (2130 and 2750 Hz) is detected. Interrupts will be blocked when the signal level on the CAS input is below the threshold in the level detector.

7.3 FSK reception

The FSK receiver function can be enabled by setting the FSK on/off bit (Mode register 1, bit 7).

In the FSK transmission specification of BT and Bellcore a channel seizure is transmitted first (sequence of 1010..). After the channel seizure a block of marks and finally the data pattern is sent (see Fig.3). These mark bits are detected by the PCD3316 which sets the FSK-BOM Indication bit (Status register, bit 4). The FSK-BOM Indication bit is reset when the FSK receiver is disabled.

If the FSK-BOM Indication bit is set, the FSK receiver will generate an interrupt after it has received a complete data word. An FSK data word consists of one start bit (space), followed by eight data bits and one stop bit (mark). Interrupts will therefore not be generated during the channel seizure and during the block of marks. When a valid data word has been received, FSK data is available in the FSK data register.

By clearing the FSK BOM-mask on/off bit (Mode register 1, bit 6), the FSK receiver will not wait with the generation of interrupts until a Begin Of Mark (BOM) has been detected but will handle the channel seizure as normal data. The block of marks which is a string of logic 1 will still not generate interrupts because there are no start bits

After the generation of an interrupt the IRQ pin will become active (see Fig.4), and the FSK Interrupt bit is set (Interrupt register, bit 5). The received data is available in the FSK data register.

The FSK-OVR Error bit (Status register, bit 3) indicates that a previous byte is lost due to an overrun.
The FSK-FRM Error bit (Status register, bit 2) indicates an incorrect start- or stop-bit. These frame errors indicate that there are synchronization problems.

The on-chip level detector can be used to detect a carrier loss during FSK transmission. FSK data can be rejected when the signal level is below the reference level, this to avoid that noise is interpreted as data. (Interrupt register, bit 4 is logic 1)

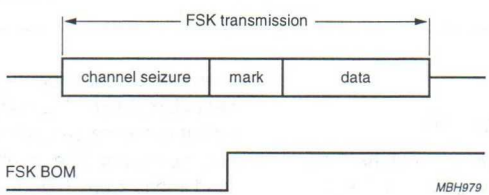


Fig.3 FSK transmission specification.

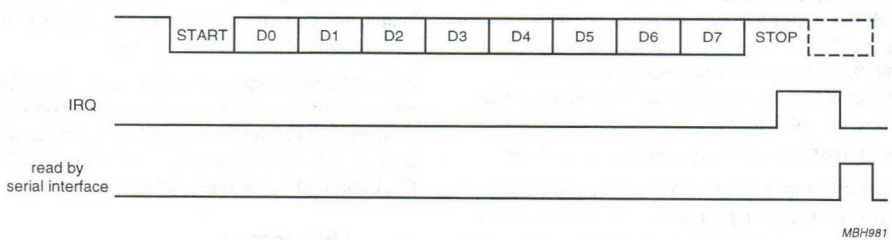


Fig.4 IRQ generation after reading a valid data byte.

25.4 Ring or polarity change detector

For ring and polarity change detection two comparators are available in the PCD3316. The reference level of the comparators is set internally by the reference voltage generator. The voltage levels on the two polarity comparator inputs, POL0 and POL1, are compared with the reference voltage V_{ref}. If POL0 < V_{ref} or POL1 > V_{ref}, POL0 and POL1 of the Status register (Status register, bit 7 and 6) are set respectively and reset if POL0 > V_{ref} and POL1 < V_{ref}. Every time the POL0 status bit changes from logic 1 to logic 0, a POL0 interrupt is generated. Every time the POL1 status bit changes from logic 0 to logic 1, a POL1 interrupt is generated.

The period time of a POL1-POL0-POL1 sequence is available in the Ringer period register. It is preset to 255 on Power-on and updated every time a POL1 interrupt is generated. The sequence is:

- Power-on:
  - Ringer period register = 255
- First POL1 interrupt:
  - Ringer period register = 255
- First POL1 interrupt after a POL0 interrupt:
  - Ringer period register = new time
- First POL1 interrupt after more than $^{255}/_{2048}$ s:
  - Ringer period register = 255.

The period is given in multiples of $^{1}/_{2048}$ s. The maximum value is 255.

The POL1-POL0-POL1 sequence is recognized when one or more POL1 interrupts are generated followed by one or more POL0 interrupts, followed by a POL1 interrupt.

The 32.768 kHz clock is needed for the generation of a polarity interrupt.

25.5 Low battery detection

The low battery voltage detection input (pin LOWBAT) is connected to the positive input of a comparator. The negative input is connected to the internal reference voltage. If the voltage on the LOWBAT input pin is less than the reference voltage V_{ref}, the LOW-BAT Indication (Status register, bit 5) is set. If the LOWBAT input rises above V_{ref} again, the LOW-BAT Indication is cleared.

The 32.768 kHz clock signal must be available.

The LOW-BAT Indication bit does not generate interrupts, thus the bit should be polled.

Table 73 Selection of interrupt modes

MODE REGISTER 2		INTERRUPT REGISTER	INTERRUPT
TB on/off (BIT 6)	SEC/MIN (BIT 5)		
0	X (don't care)	bit 7 = 0; bit 6 = 0	no time base interrupt (time base is reset)
1	0	bit 7 = 1; bit 6 = 0	every minute an interrupt is generated; no second interrupt;
1	1	bit 7 = 1; bit 6 = 1	every second an interrupt is generated; every minute an interrupt is generated

25.6 Level detect

When the input signal level on the FSK or the CAS input (the one that is selected) is below a threshold of typically −40 dBm, the Low Level bit will be set (Interrupt register, bit 4). The level detector can be used to observe a carrier loss during FSK transmission and to detect the 'Idle State Tone Alert Signal' for British Telecom.

The signal power on the input can be monitored by polling the register bit since it will not generate an interrupt. The Low Level bit will be updated every 8 ms. When FSK and CAS are both disabled the signal level on the FSK input is measured

The 32.768 kHz clock signal must be available.

25.7 Time base

The 32.768 kHz oscillator is used to generate either a 1 second or a 1 minute interrupt signal. If the TB on/off bit is set (Mode register 2, bit 6) every second or minute an interrupt is generated and MIN Interrupt and/or SEC Interrupt bits (Interrupt register, bit 7 and 6) are set. After reading the Interrupt register the interrupt is cleared. The SEC/MIN (Mode register 2, bit 5) selects whether every second (SEC/MIN is set) or every minute (SEC/MIN is cleared) an interrupt is generated. All possible selections are shown in Table 73. Resetting bit TB on/off in Mode register 2 will only disable time base interrupts, and the 32 kHz oscillator will continue to run.

7.8 Interrupt

The interrupt request output (IRQ) is active HIGH by default. The polarity of the IRQ output can be made active LOW by the INT Polarity HIGH/LOW bit (Mode register 1, bit 3). The IRQ pin is in 3-state when not active, so an external pull-up or pull-down resistor is required.
The interrupt cause is indicated by the flags in the Interrupt register. Interrupt flags are set by hardware but must be reset by software. All flags of the Interrupt register are reset when the register is read via I^2C-bus interface.

The IRQ pin is deactivated at the positive edge of SCL which reads the first data bit of the Interrupt register. The IRQ pin will stay inactive for one SCL cycle. IRQ can handle a next interrupt after the next positive edge of SCL.

7.9 The internal Power-on reset (POR)

The device contains an on-chip Power-on reset circuitry which activates a reset as long as V_{DD} is below a predefined level $V_{POR(H)}$. If V_{DD} exceeds $V_{POR(H)}$, the 3.58 MHz oscillator will start. The PCD3316 is initialized and the internal registers are set to the default value (see Section 7.13). It takes a maximum of 100 cycles of the 3.58 MHz clock to initialize all internal functions. The POR circuitry also ensures, that the chip will be switched off as soon as a falling V_{DD} reaches a predefined level ($V_{POR(L)}$).

7.10 3.58 MHz oscillator circuitry

The 3.58 MHz oscillator is needed for the FSK receiver and the CAS detection. This on-chip amplitude controlled oscillator circuitry is a single-stage inverting amplifier biased by an internal feedback resistor R_{fb}. The oscillator circuit is shown in Fig.5. When using a quartz resonator to drive the oscillator, normally no external components are needed. When using ceramic resonators to drive the oscillator, in some cases external components are needed depending on the ceramic resonator specifications (refer to product specification). Two different configurations are shown in Fig.7a and b.

To drive the device with an external clock source, apply the external clock signal to HXIN, and leave HXOUT to float, as shown in Fig.7c. If the amplitude of the input signal is less than V_{DD} to GND or a sine wave is applied, capacitive decoupling is needed as shown in Fig.7d.

In the Power-down mode (Mode register 2, bit 7 = 0), the oscillator is stopped and HXIN and HXOUT are internally pulled LOW. The current of the whole oscillator is switched off.

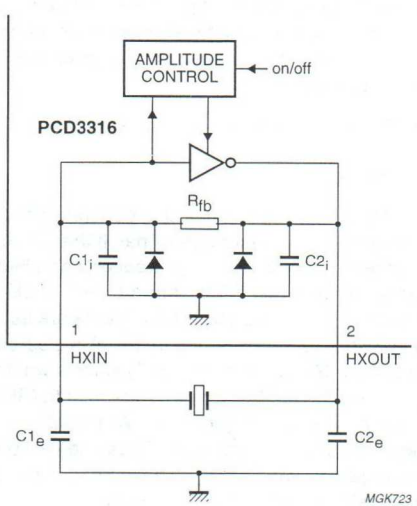
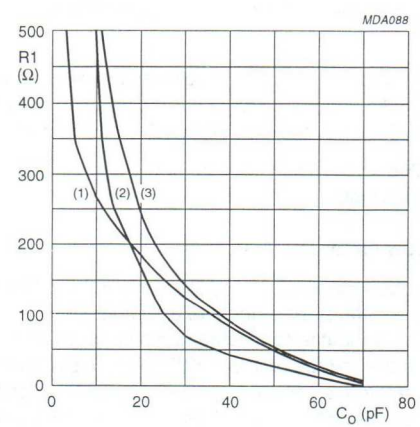


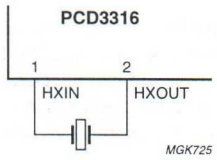
Fig.5 Oscillator.



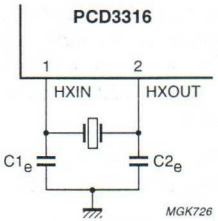
C_{1e} and C_{2e} are the external load capacitances (see Fig.7b). Normally, they are not needed (curve 2) due to integrated load capacitances of 10 pF.

(1) $C_{1e} = C_{2e} = 22$ pF.
(2) $C_{1e} = C_{2e} = 0$ pF.
(3) $C_{1e} = C_{2e} = 12$ pF.

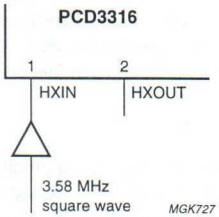
Fig.6 Resonator requirements for the ACO (see Fig.8 for equivalent circuit).



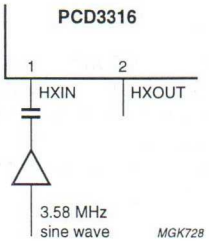
a. Standard oscillator (quartz or PXE).



b. Oscillator (quartz or PXE) with external capacitors.



c. External clock (square wave).



d. External clock (sine wave).

Fig.7 3.58 MHz oscillator configurations.

For correct function of the oscillator, the values of R_1 and C_0 of the chosen resonator in Fig.8 (quartz or PXE) must be below the line shown in Fig.6. The value of the parallel resistor R_0 must be less than 47 kΩ.

Recommended resonator types are:

- CSA 3.58MG (supplier Murata)
- FCR 3.58M5 (supplier TDK).

The wiring between chip and resonator should be kept as short as possible.

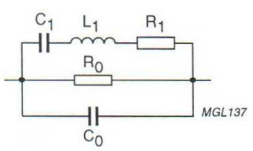


Fig.8 Resonator equivalent circuit.

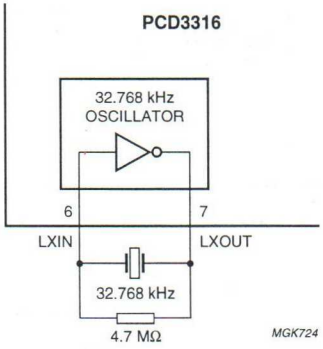


Fig.9 Connections of the 32 kHz oscillator.

7.11 32 kHz oscillator

The 32.768 kHz oscillator is enabled permanently and is used to generate either a 1 second or 1 minute interrupt. The 32.768 kHz clock is also used for the 'Ring or polarity change detector', the 'Low battery detection' and the 'Level detect' function.

An external 32.768 kHz signal may be applied to pin LXIN while leaving pin LXOUT not connected.

The 32 kHz oscillator requires an external 32.768 kHz quartz crystal and an external feedback resistor (4.7 MΩ) between the LXIN and LXOUT pins. See Fig.9.

7.12 Serial interface

The serial interface of the PCD3316 is the I²C-bus. A detailed description of the I²C-bus specification, including applications, is given in the brochure: *"The I²C-bus and how to use it"*, order no. 9398 393 40011 or *"I²C Peripherals Data Handbook IC12"*, order no. 9397 750 01647.

7.12.1 Characteristics of the I²C-bus (see Fig.10)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are called the 'slaves'. The PCD3316 operates in the slave transmitter/receiver mode only.

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

7.12.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as a STOP condition (P) (see Fig.11).

7.12.3 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Fig.12).

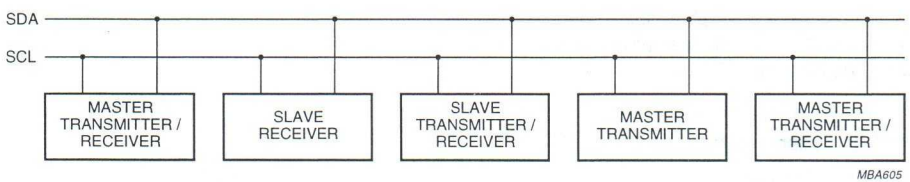


Fig.10 I²C-bus configuration.

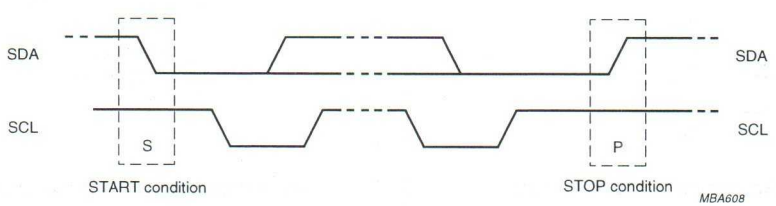


Fig.11 START and STOP conditions for the I²C-bus.

7.12.4 ACKNOWLEDGE

The number of data bytes transferred between the START and the STOP conditions from the transmitter to the receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge-related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock period (SCL LOW + HIGH) immediately after the 8th SCL pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

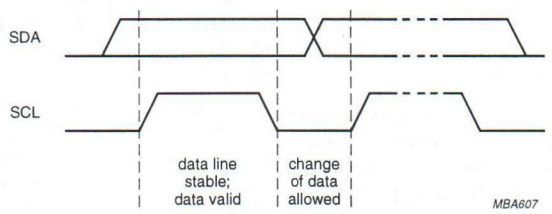


Fig.12 I²C-bus bit transfer.

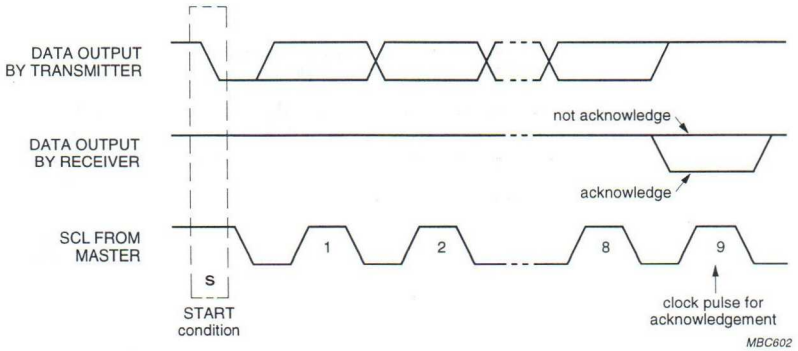


Fig.13 I²C-bus acknowledge.

7.12.5 I²C-BUS PROTOCOL

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with first byte transmitted after the START procedure. One I²C slave address is reserved for the PCD3316, E0H (1110 0000 for write and 1110 0001 for read).

The I²C protocol is shown in Figs 14 and 15. Two different sequences are considered, the WRITE sequence and the READ sequence. Both sequences are initiated with a START condition (S) from the I²C-bus master which is followed by the PCD3316 slave address with the read bit cleared. The first byte after the I²C address is interpreted as the address of a PCD3316 register.

During the write sequence the register address of the PCD3316 is auto-incremented on each acknowledge. The write sequence is ended with a STOP condition from the master. If the addressed register is read-only or non-existent, nothing will be changed.

For the read sequence the bus master issues a repeated START condition followed by the PCD3316 slave address with the read bit set. Then data is read from previously set address and sent out. When the master responds with an acknowledge the address of the register is auto incremented and the slave will put the data from the next register on the bus. The read sequence is stopped when the master stops giving an acknowledge and generates a STOP condition.

When a non-existing register is addressed the PCD3316 will return FFH. Existing register addresses are shown in Section 7.13. An additional register address (73H) is reserved for test purposes. This address cannot be reached with the auto-increment function of the I²C-interface.

7.12.6 I²C-BUS BIT RATE

When a microcontroller is used that implements an I²C-bus in software, the bit rate of the I²C-bus can be critical during reception of FSK. The collection of the interrupt data and FSK-data from the PCD3316 takes 48 bits on the I²C-bus. With an FSK baud rate of 1200 (corresponds to 1200 bits per second) the minimal speed of the I²C-bus should be 5.76 kbits/s. Additional interrupts generated by the time base of the PCD3316 will cause the processor to collect extra information from the PCD3316. As a consequence, the FSK-data can be overrun in the PCD3316 and one data byte will be lost. In this case, the time base interrupt should be suppressed while FSK is active. This can be done by setting the INT-SUP on/off bit (bit 4 in Mode register 2). The TB on/off bit (bit 6 in Mode register 2) will still be set but the IRQ output will not be activated by the time base interrupt. Any time base interrupt can be detected by the microcontroller when an FSK interrupt is processed by reading the Interrupt register.

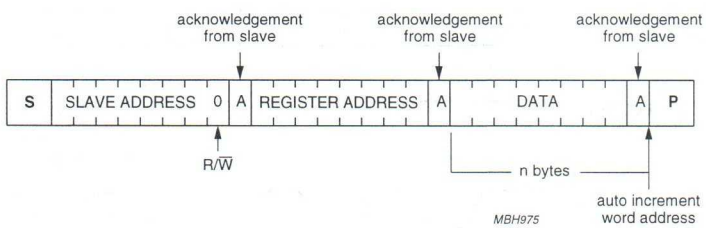


Fig.14 I²C-bus write sequence.

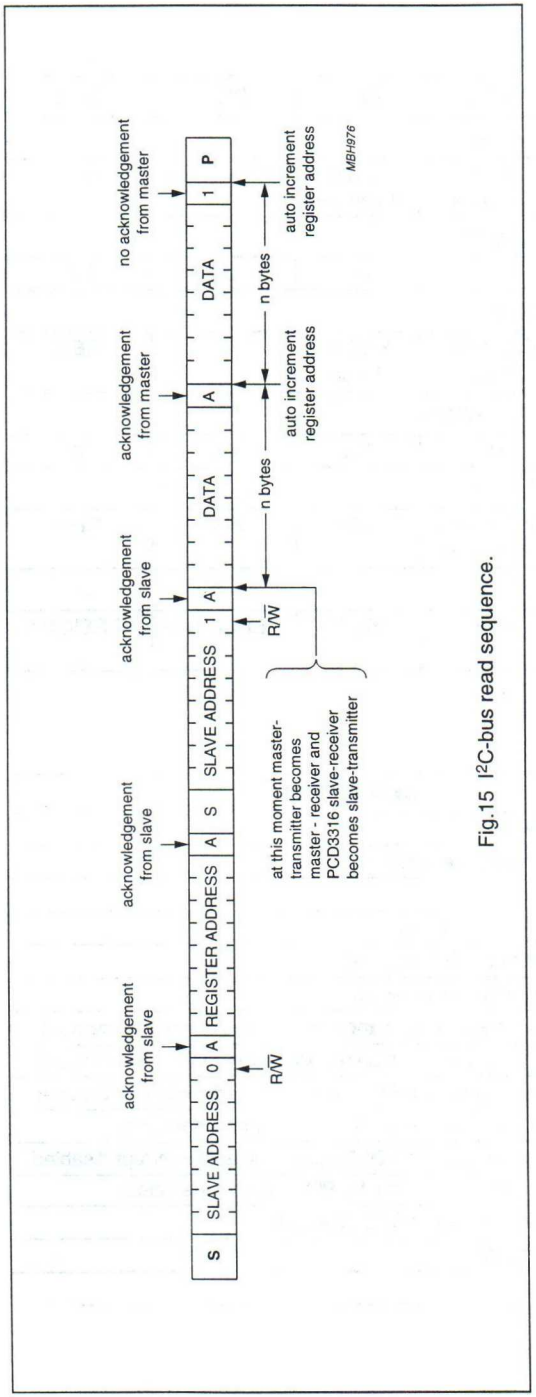


Fig.15 I²C-bus read sequence.

25.13 Register overview

Table 74 Register contents

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Interrupt register CIDINT; address 00H; read only; see Table 75							
MIN Interrupt	SEC Interrupt	FSK Interrupt	Low Level Status	POL1 Interrupt	POL0 Interrupt	CAS Interrupt	RES
FSK data register CIDFSK; address 01H; read only; see Table 76							
D7	D6	D5	D4	D3	D2	D1	D0
Status register CIDSTA; address 02H; read only; see Table 77							
POL1	POL0	LOW-BAT Indication	FSK-BOM Indication	FSK-OVR Error	FSK-FRM Error	RES	RES
Ringer period register CIDRNG; address 03H; read only; see Table 78							
D7	D6	D5	D4	D3	D2	D1	D0
Mode register 1 CIDMD1; address 04H; read/write; see Table 79							
FSK on/off	FSK BOM-mask on/off	CAS on/off	POL on/off	INT Polarity HIGH/LOW	RES	RES	RES
Mode register 2 CIDMD2; address 05H; read/write; see Table 80							
XTAL on/off	TB on/off	SEC/MIN	INT-SUP on/off	RES	RES	VERSION 1	VERSION 0

25.14 Detailed register descriptions

Table 75 Description of the Interrupt register bits

BIT	SYMBOL	DEFAULT	DESCRIPTION
CIDINT.7	MIN Interrupt	0	0: no interrupt request
			1: one minute interrupt request
CIDINT.6	SEC Interrupt	0	0: no interrupt request
			1: one second interrupt request
CIDINT.5	FSK Interrupt	0	0: no FSK interrupt or FSK disabled
			1: FSK interrupt, one byte received
CIDINT.4	Low Level Status	0	0: signal level on selected input above power reference (no interrupt)
			1: signal level on selected input below power reference (no Interrupt)
CIDINT.3	POL1 Interrupt	0	0: no zero to one changes on POL1 input or polarity interrupt disabled
			1: a one to zero input change on the POL1 input is detected
CIDINT.2	POL0 Interrupt	0	0: no one to zero changes on POL0 input or polarity interrupt disabled
			1: a zero to one input change on the POL0 input is detected
CIDINT.1	CAS Interrupt	0	0: no CAS signal detected or CAS disabled
			1: CAS signal detected
CIDINT.0	RES	0	reserved bit

Table 76 Description of FSK data bits

BIT	SYMBOL	DESCRIPTION
CIDFSK.7 to CIDFSK.0	D7 to D0	If an FSK interrupt has occurred and no FSK error is detected, the FSK data register contains valid data.

Table 77 Description of the status register bits.

BIT	SYMBOL	DESCRIPTION
CIDSTA.7	POL1	0: POL1 input < V_{ref}
		1: POL1 input > V_{ref}
CIDSTA.6	POL0	0: POL0 input > V_{ref}
		1: POL0 input < V_{ref}
CIDSTA.5	LOW-BAT Indication	0: LOWBAT input > V_{ref}
		1: LOWBAT input < V_{ref}
CIDSTA.4	FSK-BOM Indication	0: begin of mark period not yet detected
		1: begin of mark period detected
CIDSTA.3	FSK-OVR Error	0: no FSK overrun error
		1: FSK overrun error, data byte(s) lost
CIDSTA.2	FSK-FRM Error	0: no FSK frame error
		1: FSK frame error, stop bit was wrong
CIDSTA.1	RES	reserved bit
CIDSTA.0	RES	reserved bit

Table 78 Description of CIDRNG bits

BIT	SYMBOL	DESCRIPTION
CIDRNG7 to CIDRNG0	D7 to D0	time between two positive edges of the POL1 comparator output (between two positive edges of POL1 one positive edge of POL0 must have been detected)

Table 79 Description of the Mode register 1 bits.

BIT	SYMBOL	DEFAULT	DESCRIPTION
CIDMD1.7	FSK on/off	0	0: FSK receiver disabled
			1: FSK receiver enabled
CIDMD1.6	FSK BOM-mask on/off	1	0: enable FSK interrupts before mark period
			1: disable FSK interrupts before mark period
CIDMD1.5	CAS on/off	0	0: CAS detector disabled
			1: CAS detector disabled
CIDMD1.4	POL on/off	1	0: disable interrupts due to polarity change
			1: enable interrupts due to polarity change
CIDMD1.3	INT polarity HIGH/LOW	1	0: interrupt pin active LOW
			1: interrupt pin active HIGH
CIDMD1.2	RES	0	reserved bit
CIDMD1.1	RES	0	reserved bit
CIDMD1.0	RES	0	reserved bit

Table 80 Description of the Mode register 2 bits

BIT	SYMBOL	DEFAULT	DESCRIPTION
CIDMD2.7	XTAL on/off	1	0: disable 3.58 MHz oscillator
			1: enable 3.58 MHz oscillator
CIDMD2.6	TB on/off	1	0: disable 32.768 kHz timebase
			1: enable 32.768 kHz timebase
CIDMD2.5	SEC/MIN	0	0: every minute a timebase interrupt
			1: every second a timebase interrupt
CIDMD2.4	INT-SUP on/off	1	0: enable SEC/MIN interrupts during FSK reception
			1: disable SEC/MIN interrupts during FSK reception
CIDMD2.3	RES	0	reserved bit
CIDMD2.2	RES	0	reserved bit
CIDMD2.1	RES	0	reserved bit
CIDMD2.0	RES	0	reserved bit

26 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+5.0	V
I_{DD}	supply current		–	50	mA
I_I	DC input current at any input		−10	+10	mA
I_O	DC output current at any output		−10	+10	mA
V_I	input voltage on all inputs	note 1	−0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation		–	300	mW
P_O	power dissipation per output		–	10	mW
T_{amb}	operating ambient temperature		−25	+70	°C
T_{stg}	storage temperature		−65	+150	°C

Note

1. $V_{I(max)}$ = 5.0 V.

27 ELECTRICAL CHARACTERISTICS

V_{DD} = 2.5 to 3.6 V; T_{amb} = −25 to +70 °C; HXIN = 3.579545 MHz ±0.05%; LXIN = 32.768 kHz ±0.1%; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	note 1	2.5	3.3	3.6	V
$V_{POR(H)}$	power-on reset high voltage		1.85	2.05	2.25	V
$V_{hys(POR)}$	power-on reset hysteresis voltage	note 2	50	100	150	mV
I_{DD}	supply currents	V_{DD} = 2.5 V				
	power down	note 3	–	30	70	µA
	operating	notes 3 and 4	–	2.0	2.3	mA
Low voltage and polarity comparators (pins LOWBAT, POL0 and POL1)						
V_{hys}	hysteresis voltage of POL0, POL1 and LOWBAT inputs		–	20	–	mV
I_i	input current	note 5	–	–	1	µA
Internal reference						
V_{ref}	reference voltage level		1.125	1.25	1.375	V
$P_{i(ref)}$	input signal reference power	in 600 Ω load, note 6	−43.8	–	−37.8	dBm
$t_{r(level)}$	input signal to Low Level bit rise time	input signal power < $P_{i(ref)}$	–	–	8	ms
$t_{f(level)}$	input signal to Low Level bit fall time	input signal power > $P_{i(ref)}$	–	–	8	ms
Logical output (pin IRQ) (see note 7)						
I_{OL}	LOW-level output current	V_{IRQ} = 0.4 V	2	–	–	mA
I_{OH}	HIGH-level output current	V_{IRQ} = V_{DD} − 0.4 V	2	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FSK receiver (pins FSKIN+ and FSKIN–)						
Z_i	input impedance FSKIN+ to FSKIN–		–	1.4	–	MΩ
$Z_{source(max)}$	maximum source impedance		–	–	200	kΩ
$P_{i(FSKIN)}$	input signal power	in 600 Ω load; note 8	–50	–	0	dBm
$TH_{ns(FSK)}$	no signal threshold	in 600 Ω load	–43.8	–	–37.8	dBm
S/N_{FSK}	signal-to-noise ratio	200 to 3400 Hz	20	–	–	dB
$\lvert V_{dif} \rvert$	differential voltage between mark and space (twist)		–	–	10	dB
f_D	data transmission rate		1180	1200	1212	bits/s
f_s	space frequency		2068	–	2222	Hz
f_m	mark frequency		1188	–	1320	Hz
CAS detector (pin CASIN)						
Z_i	input impedance CASIN to V_{ref}		–	1.4	–	MΩ
$Z_{source(max)}$	maximum source impedance		–	–	200	kΩ
P_i	input signal power	in 600 Ω load	–37.8	–	0	dBm
$TH_{ns(CAS)}$	no signal threshold (CAS)	in 600 Ω load	–43.8	–	–37.8	dBm
f_l	low tone frequency		–	2130	–	Hz
f_h	high tone frequency		–	2750	–	Hz
Δf_{max}	maximum frequency deviation	note 9	–0.5	–	+0.5	%
V_{dif}	differential voltage level (twist)	note 9	–	–	6	dB
t_{dt}	dual tone detection time		60	–	–	ms
I^2C interface (pins SCL and SDA); see Figs 57 and 58						
V_{IL}	LOW-level input voltage	note 10	0	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	note 10	$0.7V_{DD}$	–	V_{DD}	V
I_{OL1}	LOW-level output current for pin SDA (open drain)	$V_{O(SDA)}$ = 0.4V	2	–	–	mA
C_i	capacitance for each I/O pin		–	–	10	pF
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	maximum SCL and SDA rise time	note 11	–	–	1000	ns
t_f	maximum SCL and SDA fall time	note 11	–	–	300	ns
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid time		–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time		4.0	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
3.58 MHz oscillator (pins HXIN and HXOUT)						
$V_{HXIN(p-p)}$	external clock signal amplitude (peak-to-peak value)		0.5	–	V_{DD}	V
$Z_{i(HXIN)}$	input impedance on pin HXIN		300	1000	–	kΩ
C_{1i}; C_{2i}	input capacitance on pins HXIN and HXOUT	note 12	–	10	–	pF
32 kHz oscillator (pins LXIN and LXOUT)						
g_m	transconductance	$V_{i(p-p)} < 50$ mV	2	4	10	μS
$C_{i(LXIN)}$	LXIN input capacitance		–	13	–	pF
$C_{o(LXOUT)}$	LXOUT output capacitance		–	10	–	pF

Notes

1. Except for FSK and CAS detection, all circuitry works already when $V_{DD} > V_{POR(H)}$. Since the I^2C-bus interface will work (starts to acknowledge), the application can start reading the LOWBAT bit (Status register, bit 5) to check whether the supply voltage has reached the operating voltage level. A voltage divider network can be connected to pins V_{DD}, LOWBAT and GND such that $V_{LOWBAT} = V_{ref}$ if $V_{DD} = V_{DD(min)}$.
2. The Power-on reset low level is defined as $V_{POR(L)} = V_{POR(H)} - V_{hys(POR)}$. By design $V_{POR(L)}$ is always lower than $V_{POR(H)}$.
3. 32 kHz oscillator on (Min, Sec interrupt, Polarity change, Low battery and Level detection available).
4. 3.58 MHz oscillator on (device fully operational).
5. $GND < V_I < V_{DD}$. The leakage currents are generally very small, <1 nA. The value given here, 1 μA, is a maximum that can occur after an Electrostatic Stress on the pin.
6. When FSK is selected the signal power is measured between 1000 Hz and 2200 Hz. When CAS is selected signal levels are measured between 2000 and 2800Hz.
7. The IRQ pin is implemented as a 3-state pin which is only active (either HIGH or LOW) when an interrupt comes. A pull-up or pull-down has to be connected to define the line when no interrupt is generated.
8. Verified on sampling basis.
9. According to Bellcore specification: near end speech level ≤ –7 dBm ASL (ASL = Active Speech Level, referenced to 600 Ω, according to method B of recommendation P.56.
10. The input threshold voltage of SCL and SDA meet the I^2C-bus specification. Therefore, an input voltage below $0.3V_{DD}$ will be recognized as a logic 0 and an input voltage above $0.7V_{DD}$ will be recognized as a logic 1.
11. Maximum capacitive load for each bus line is 400 pF.
12. C_{1i} and C_{2i} are the total internal capacitances (including gate capacitance and leadframe capacitance).

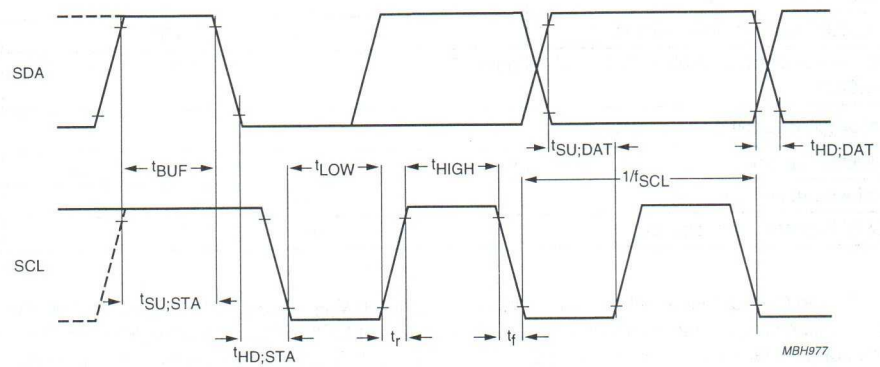


Fig.16 I²C-bus timing.

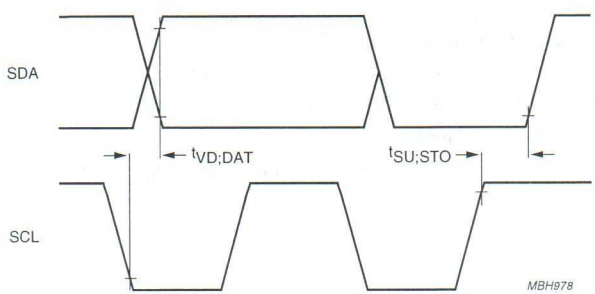
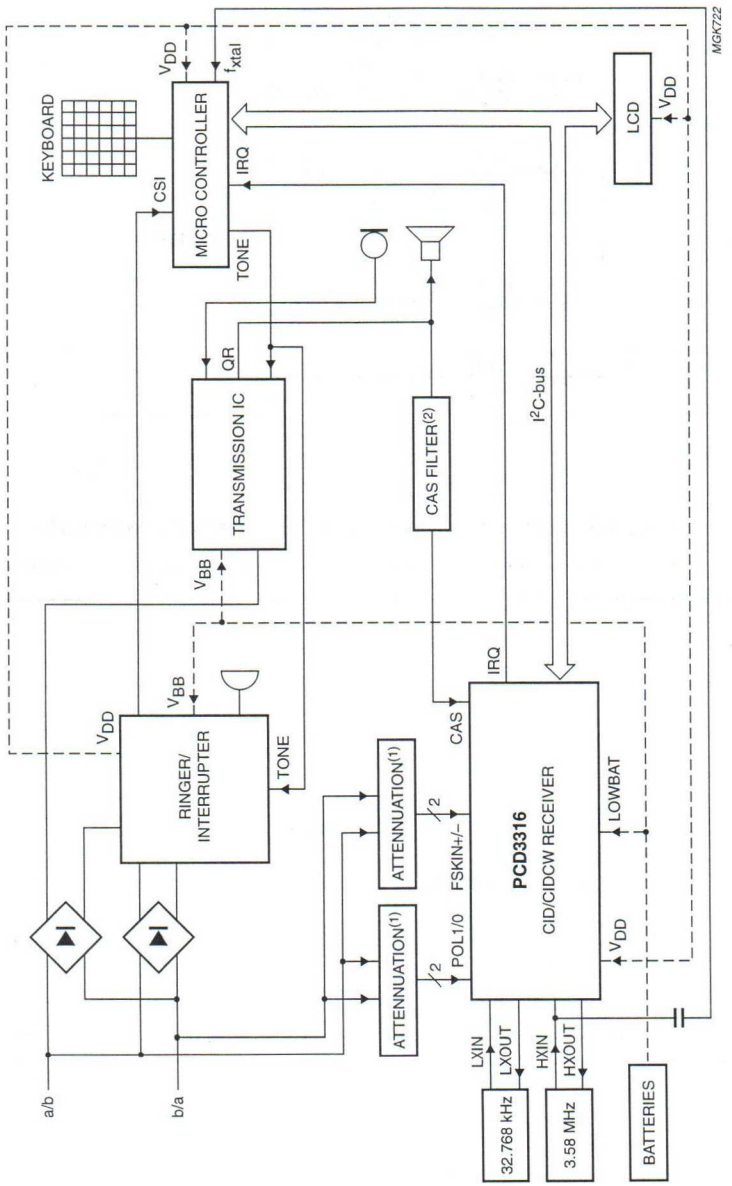


Fig.17 I²C-bus timing.

10 APPLICATION INFORMATION



A demo-board (OM5843) of this configuration is available. Please contact your Philips sales office.

(1) See Fig.19.

(2) See Fig.20.

Fig.18 Application diagram for a telephone with CID/CW functionality.

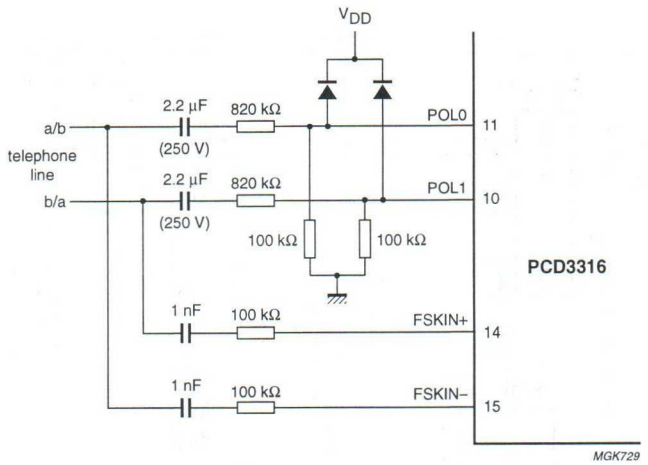


Fig.19 Attenuation networks to connect the polarity and FSK inputs to the telephone line.

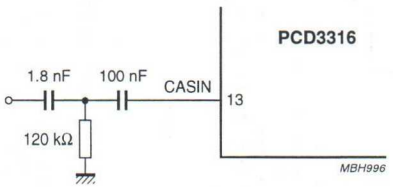


Fig.20 High-pass filter (cut-off frequency ≈ 1 kHz) to improve performance of CAS detection.

COMPLEMENTARY PRODUCTS

Tone decoder/phase-locked loop

NE/SE567

DESCRIPTION

The NE/SE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency and output delay are independently determined by means of four external components.

FEATURES

- Wide frequency range (.01Hz to 500kHz)
- High stability of center frequency
- Independently controllable bandwidth (up to 14%)
- High out-band signal and noise rejection
- Logic-compatible output with 100mA current sinking capability
- Inherent immunity to false signals
- Frequency adjustment over a 20-to-1 range with an external resistor
- Military processing available

APPLICATIONS

- Touch-Tone® decoding
- Carrier current remote controls
- Ultrasonic controls (remote TV, etc.)
- Communications paging
- Frequency monitoring and control
- Wireless intercom
- Precision oscillator

PIN CONFIGURATIONS

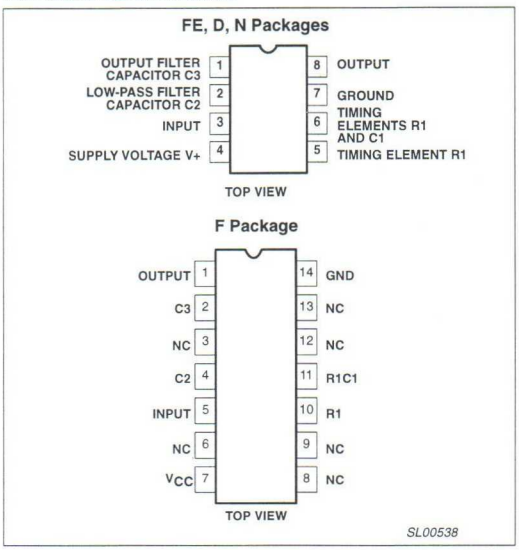
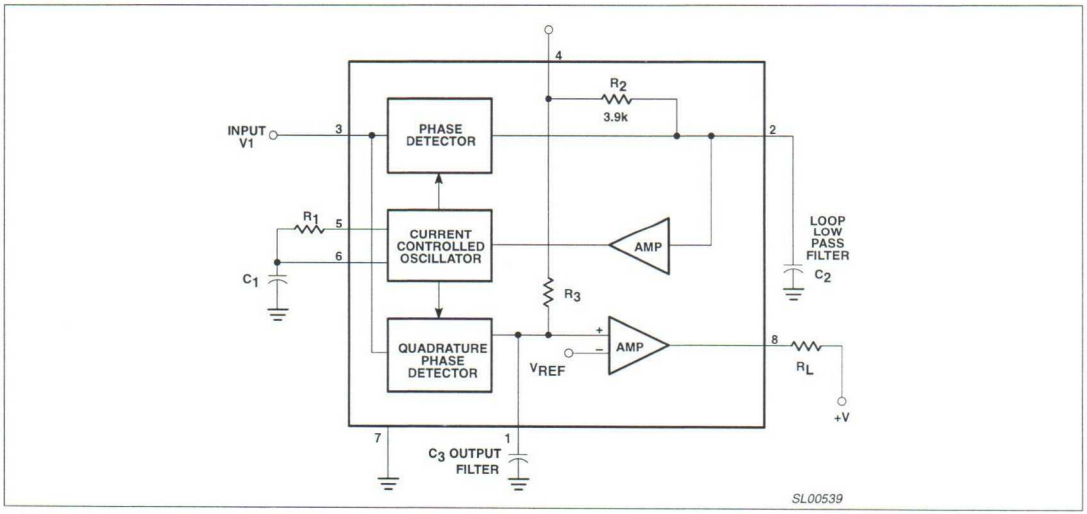


Figure 1. Pin Configurations

BLOCK DIAGRAM



®Touch-Tone is a registered trademark of AT&T.

Figure 2. Block Diagram

EQUIVALENT SCHEMATIC

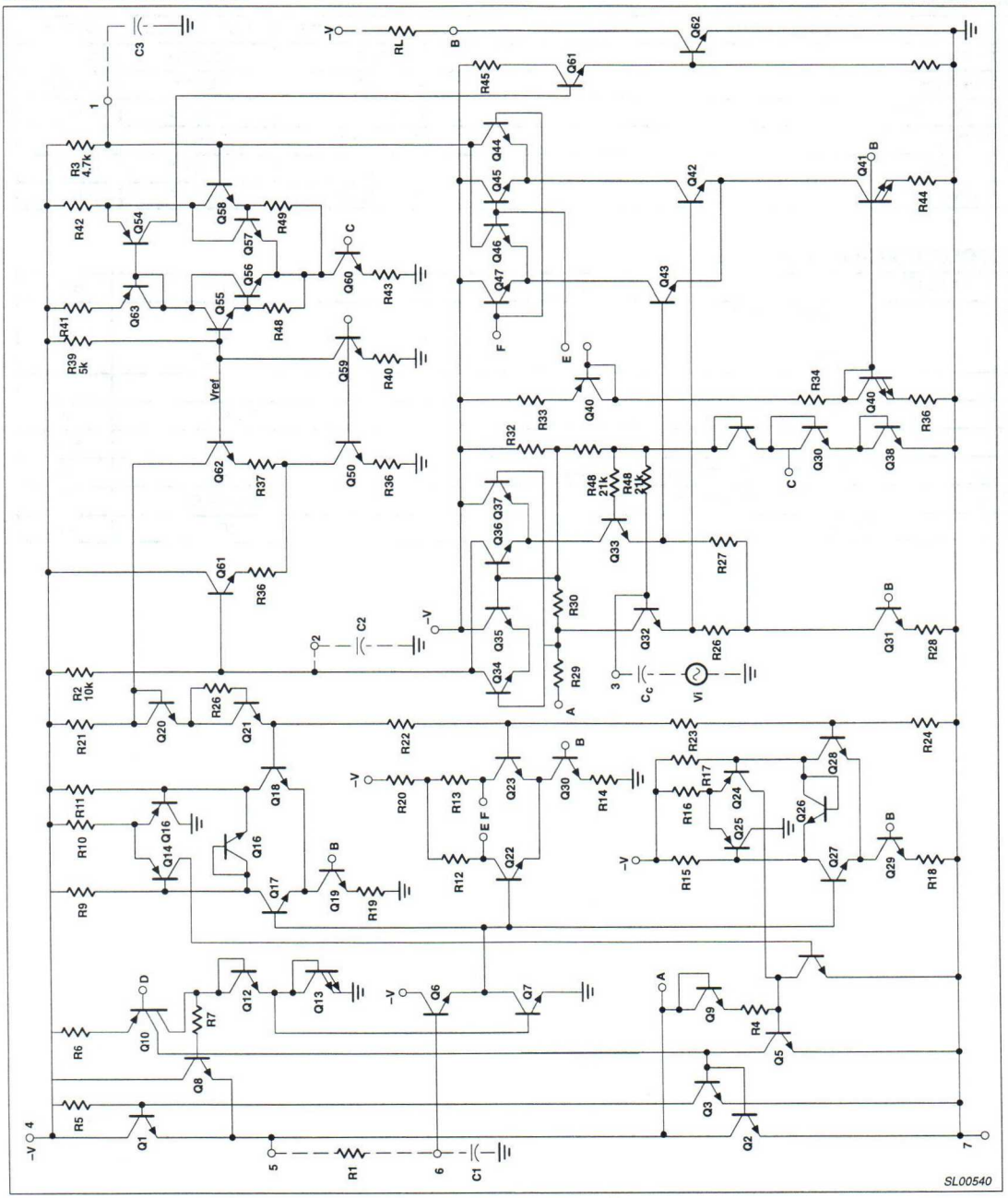


Figure 3. Equivalent Schematic

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic SO	0 to +70°C	NE567D	SOT96-1
14-Pin Cerdip	0 to +70°C	NE567F	0581B
8-Pin Plastic DIP	0 to +70°C	NE567N	SOT97-1
8-Pin Plastic SO	-55°C to +125°C	SE567D	SOT96-1
8-Pin Cerdip	-55°C to +125°C	SE567FE	0581B
8-Pin Plastic DIP	-55°C to +125°C	SE567N	SOT97-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating temperature NE567 SE567	 0 to +70 -55 to +125	 °C °C
V_{CC}	Operating voltage	10	V
V+	Positive voltage at input	0.5 +V_S	V
V-	Negative voltage at input	-10	V_{DC}
V_{OUT}	Output voltage (collector of output transistor)	15	V_{DC}
T_{STG}	Storage temperature range	-65 to +150	°C
P_D	Power dissipation	300	mW

DC ELECTRICAL CHARACTERISTICS

V +=5.0V; T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE567			NE567			UNIT
			Min	Typ	Max	Min	Typ	Max	
Center frequency[1]									
f_O	Highest center frequency			500			500		kHz
f_O	Center frequency stability[2]	-55 to +125°C		35 ±140			35 ±140		ppm/°C
		0 to +70°C		35 ±60			35 ±60		ppm/°C
f_O	Center frequency distribution	$f_O = 100kHz = \frac{1}{1.1R_1C_1}$	-10	0	+10	-10	0	+10	%
f_O	Center frequency shift with supply voltage	$f_O = 100kHz = \frac{1}{1.1R_1C_1}$		0.5	1		0.7	2	%/V
Detection bandwidth									
BW	Largest detection bandwidth	$f_O = 100kHz = \frac{1}{1.1R_1C_1}$	12	14	16	10	14	18	% of f_O
BW	Largest detection bandwidth skew			2	4		3	6	% of f_O
BW	Largest detection bandwidth—variation with temperature	V_I=300mV$_{RMS}$		±0.1			±0.1		%/°C
BW	Largest detection bandwidth—variation with supply voltage	V_I=300mV$_{RMS}$		±2			±2		%/V
Input									
R_{IN}	Input resistance		15	20	25	15	20	25	kΩ
V_I	Smallest detectable input voltage[4]	I_L=100mA, f_I=f_O		20	25		20	25	mV$_{RMS}$
	Largest no-output input voltage[4]	I_L=100mA, f_I=f_O	10	15		10	15		mV$_{RMS}$
	Greatest simultaneous out-band signal-to-in-band signal ratio			+6			+6		dB
	Minimum input signal to wide-band noise ratio	B_n=140kHz		-6			-6		dB
Output									
	Fastest on-off cycling rate			f_O/20			f_O/20		
	"1" output leakage current	V_8=15V		0.01	25		0.01	25	µA
	"0" output voltage	I_L=30mA		0.2	0.4		0.2	0.4	V
		I_L=100mA		0.6	1.0		0.6	1.0	V
t_F	Output fall time[3]	R_L=50Ω		30			30		ns
t_R	Output rise time[3]	R_L=50Ω		150			150		ns
General									
V_{CC}	Operating voltage range		4.75		9.0	4.75		9.0	V
	Supply current quiescent			6	8		7	10	mA
	Supply current—activated	R_L=20kΩ		11	13		12	15	mA
t_{PD}	Quiescent power dissipation			30			35		mW

NOTES:

1. Frequency determining resistor R_1 should be between 2 and 20kΩ
2. Applicable over 4.75V to 5.75V. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.
4. With R_2=130kΩ from Pin 1 to V+. See Figure 17.

TYPICAL PERFORMANCE CHARACTERISTICS

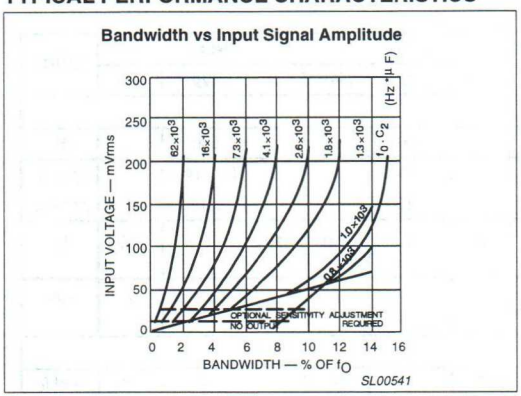


Figure 4.

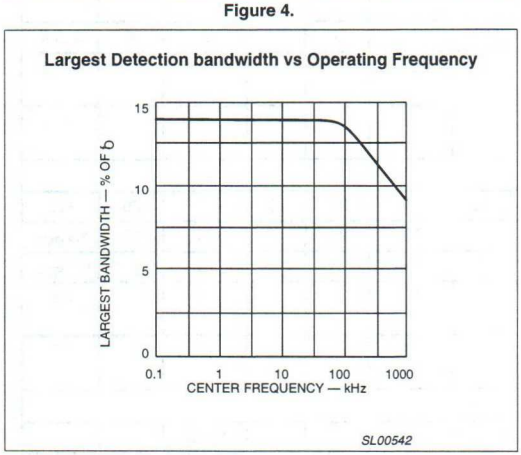


Figure 5.

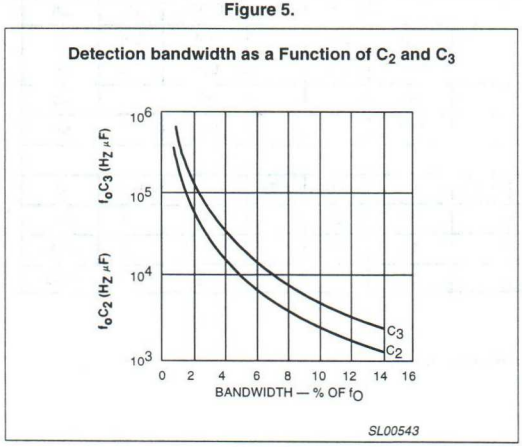


Figure 6.

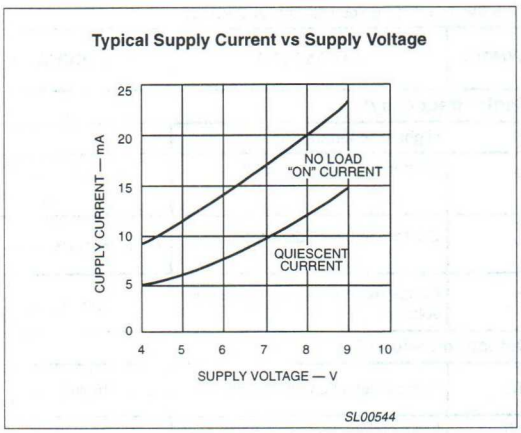


Figure 7.

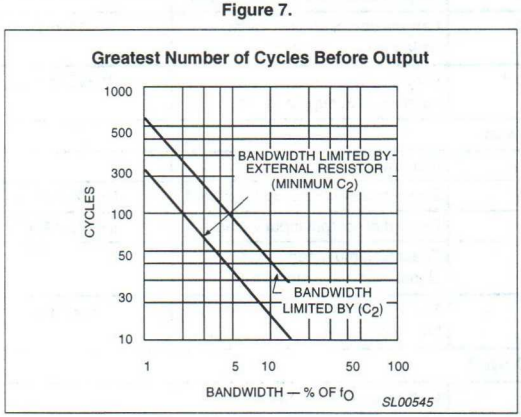


Figure 8.

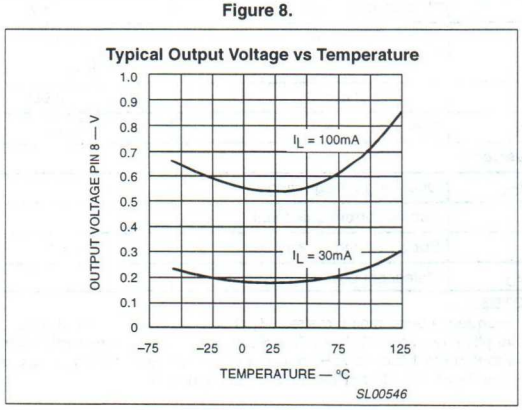


Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

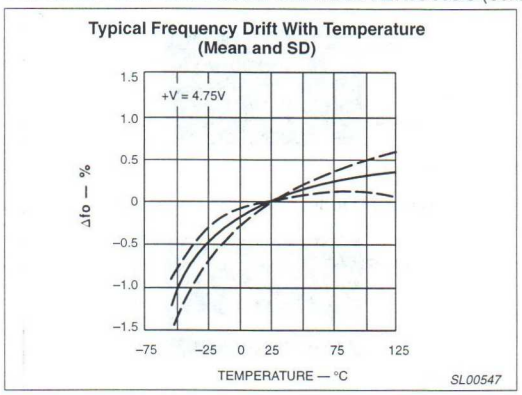


Figure 10.

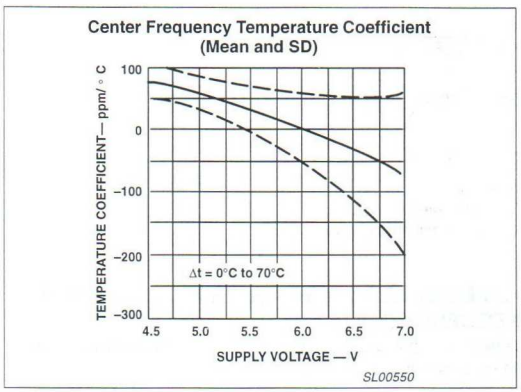


Figure 13.

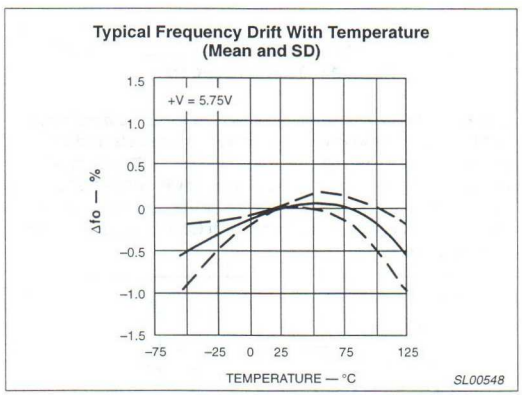


Figure 11.

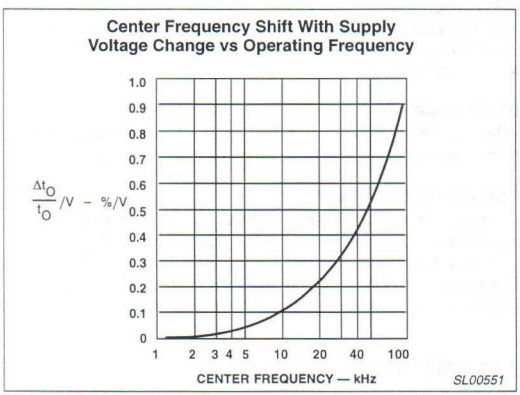


Figure 14.

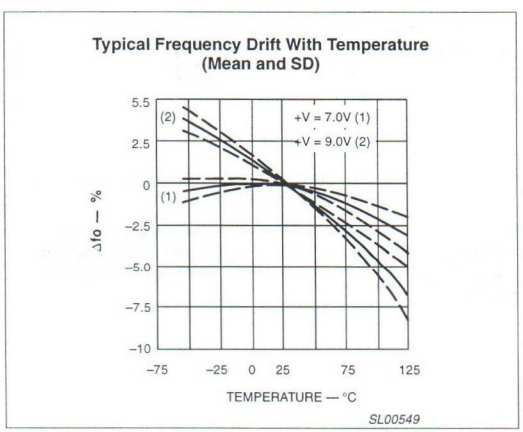


Figure 12.

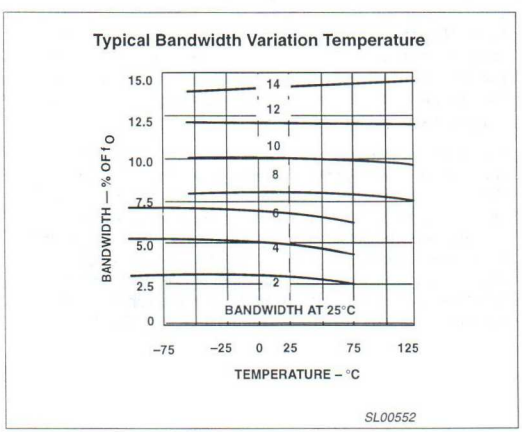


Figure 15.

DESIGN FORMULAS

$$f_O \approx \frac{1}{1.1R_1 C_1}$$

$$BW \approx 1070 \sqrt{\frac{V_I}{f_O C_2}} \text{ in \% of } f_O$$

$$V_I \leq 200mV_{RMS}$$

Where
V_I=Input voltage (V_{RMS})
C_2=Low-pass filter capacitor (μF)

PHASE-LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (f_O)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection Bandwidth (BW)

The frequency range, centered about f_O, within which an input signal above the threshold voltage (typically $20mV_{RMS}$) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection Band Skew

A measure of how well the detection band is centered about the center frequency, f_O. The skew is defined as $(f_{MAX}+f_{MIN}-2f_O)/2f_O$ where fmax and fmin are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

OPERATING INSTRUCTIONS

Figure 17 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

1. Select R1 and C1 for the desired center frequency. For best temperature stability, R1 should be between 2K and 20K ohm, and the combined temperature coefficient of the R1C1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.

2. Select the low-pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude Variation is known, the appropriate value of $f_O \cdot C_2$ necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above $200mV_{RMS}$. The bandwidth, as noted on the graph, is then controlled solely by the $f_O \cdot C_2$ product (f_O (Hz), C2(μF)).

TYPICAL RESPONSE

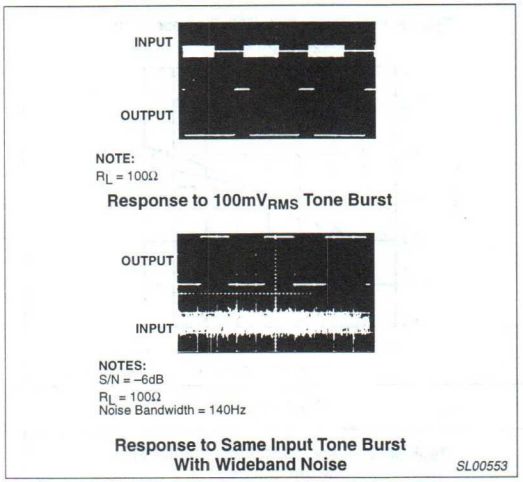


Figure 16. Typical Response

3. The value of C3 is generally non-critical. C3 sets the band edge of a low-pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C3 is too large, turn-on and turn-off of the

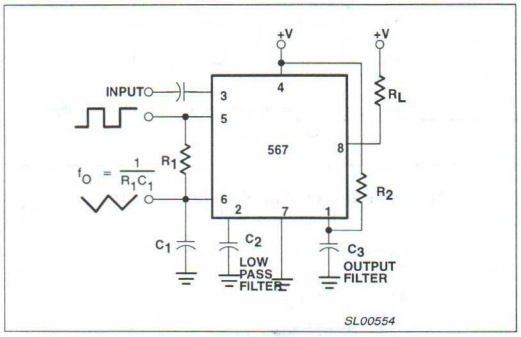


Figure 17.

output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

4. Optional resistor R2 sets the threshold for the largest "no output" input voltage. A value of 130kΩ is used to assure the tested limit of $10mV_{RMS}$ min. This resistor can be referenced to ground for increased sensitivity. The explanation can be found in the "optional controls" section which follows.

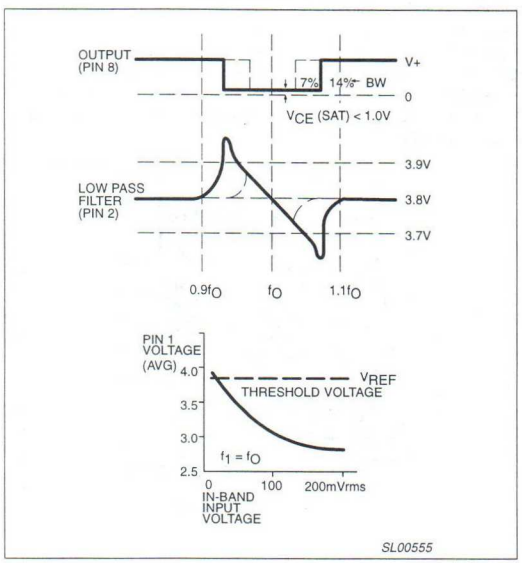


Figure 18. Typical Output Response

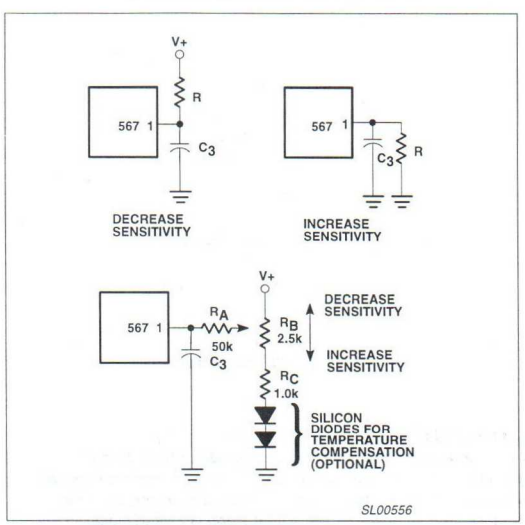


Figure 19. Sensitivity Adjust

AVAILABLE OUTPUTS (Figure 17)

The primary output is the uncommitted output transistor collector, Pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at Pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_O with a slope of about 20mV per percent of frequency deviation. The average voltage at Pin 1 is, during lock, a function of the in-band input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(+V - 2V_{BE}) \cong (+V - 1.4V)$ having a DC average of +V/2. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of $1V_{P-P}$ with an average DC level of +V/2. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input
   stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the inband signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_O/3$, $f_O/5$, etc.
2. The 567 will lock onto signals near $(2n+1)\ f_O$, and will give an output for signals near $(4n+1)\ f_O$ where n=0, 1, 2, etc. Thus, signals at $5f_O$ and $9f_O$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.
3. Maximum immunity from noise and out-band signals is afforded in the low input level (below $200mV_{RMS}$) and reduced bandwidth operating mode. However, decreased loop damping causes the worst-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.
4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency

rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_O/10$ baud.

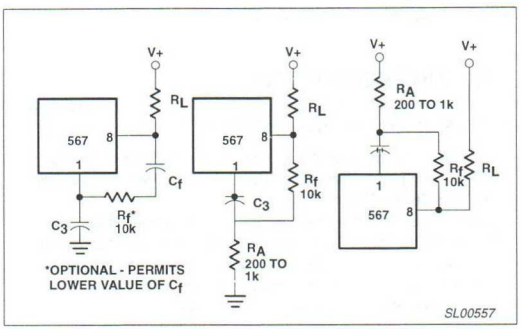


Figure 20. Chatter Prevention

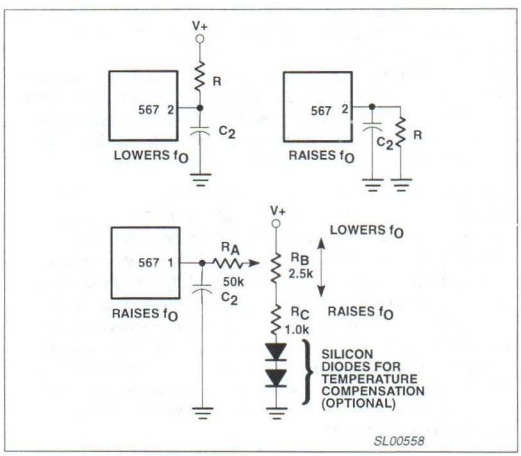


Figure 21. Skew Adjust

$$C_2 = \frac{130}{f_O}\ \mu F$$

$$C_3 = \frac{260}{f_O}\ \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

OPTIONAL CONTROLS (Figure 19)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

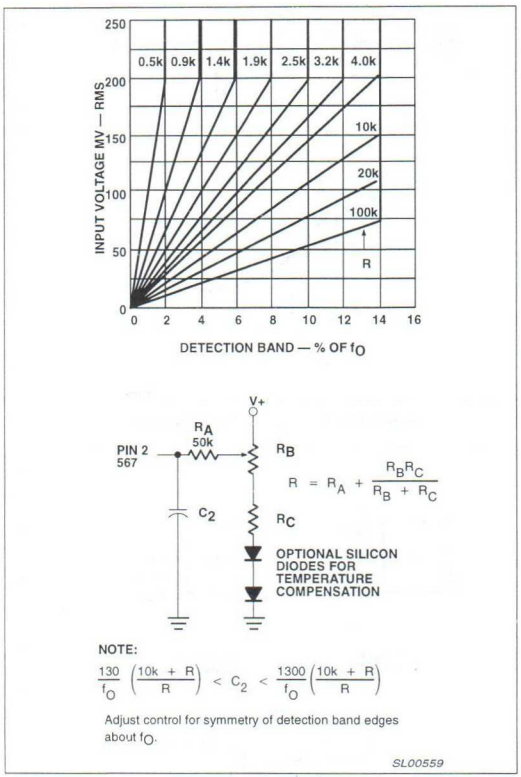


Figure 22. BW Reduction

SENSITIVITY ADJUSTMENT (Figure 19)

When operated as a very narrow-band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and out-band signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the out-band beat notes do not feed through to the output stage. Since the input level must

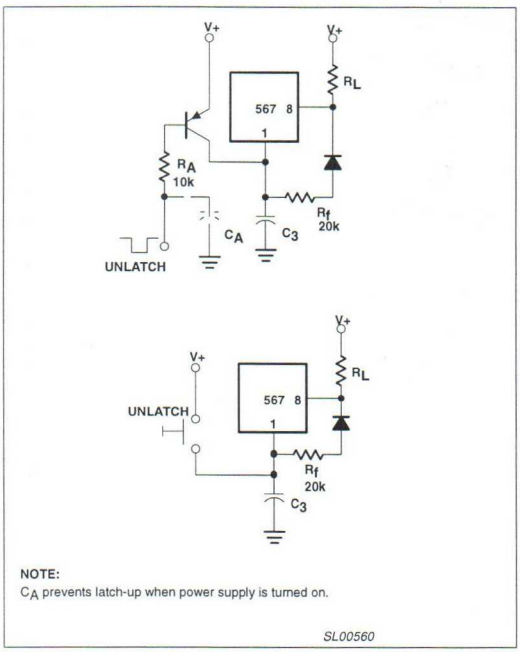


Figure 23. Output Latching

CHATTER PREVENTION (Figure 20)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (Pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 20. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT (Figure 21)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

ALTERNATE METHOD OF BANDWIDTH REDUCTION (Figure 22)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff
frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

OUTPUT LATCHING (Figure 23)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between Pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

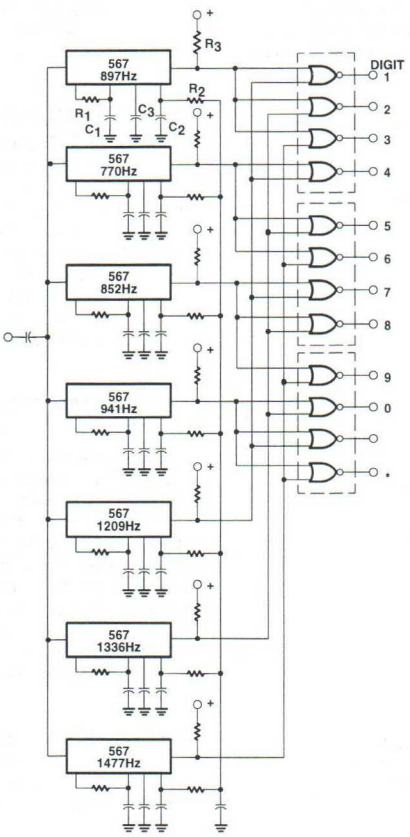
REDUCTION OF C1 VALUE

For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage-follower between the R_1 C_1 junction and Pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

PROGRAMMING

To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating NPN transistors.

TYPICAL APPLICATIONS



NOTES:

Component values (Typical)

R_1 = 26.8 to 15kΩ
R_2 = 24.7kΩ
R_3 = 20kΩ
C_1 = 0.10mF
C_2 = 1.0mF 5V
C_3 = 2.2mF 6V
C_4 = 250μF 6V

Touch-Tone® Decoder

SL00561

Figure 24. Typical Applications

TYPICAL APPLICATIONS (Continued)

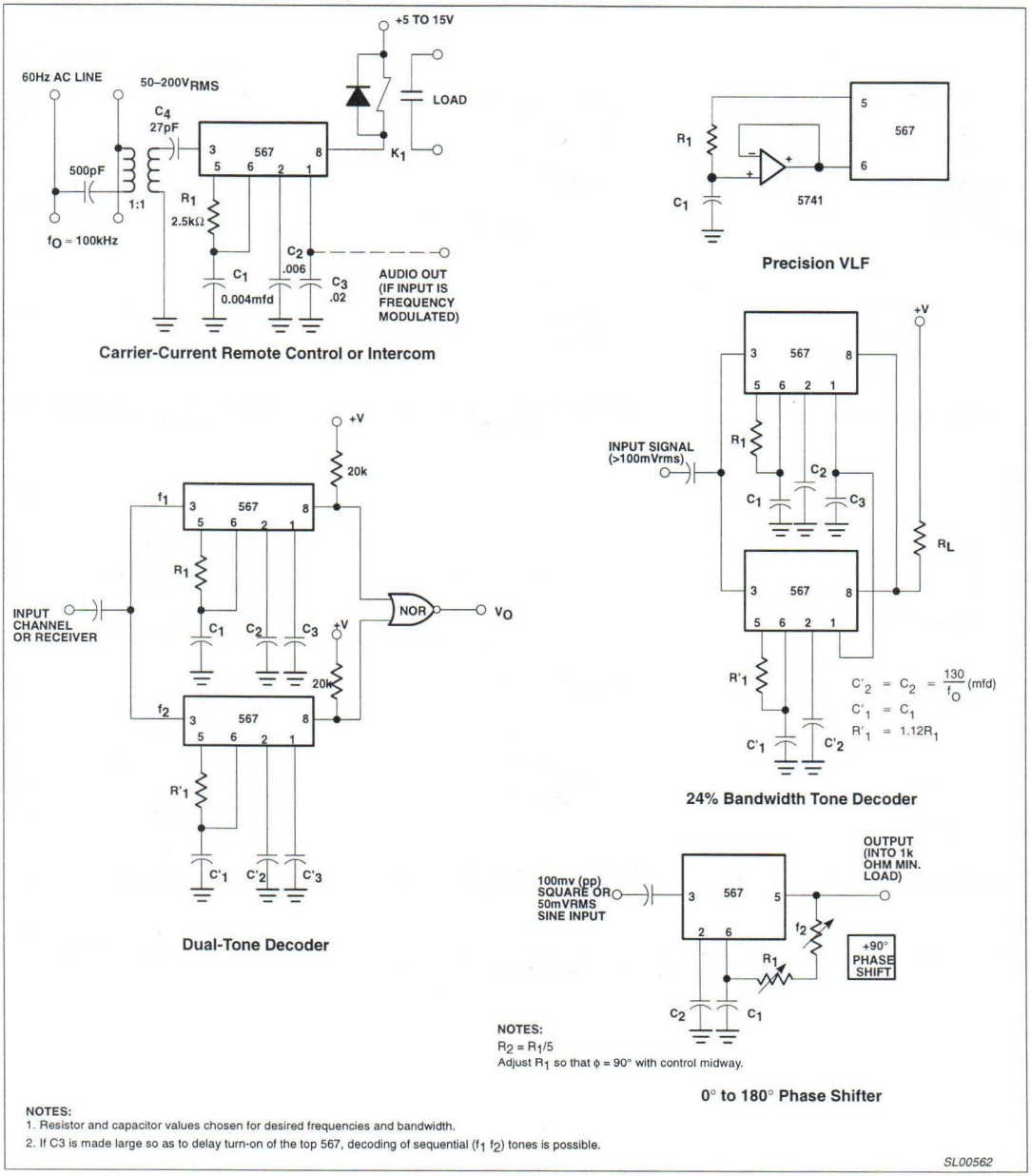


Figure 25. Typical Applications (cont.)

TYPICAL APPLICATIONS (Continued)

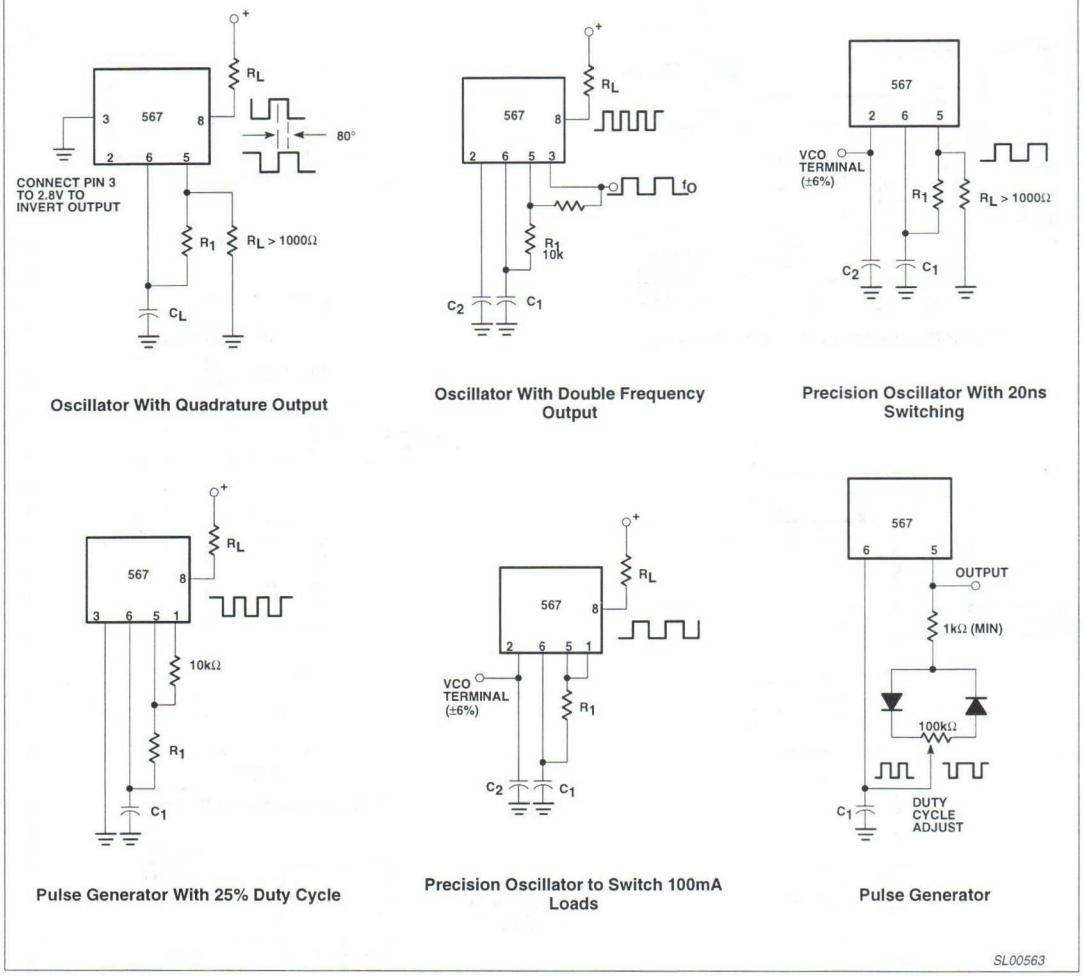


Figure 26. Typical Applications (cont.)

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Call progress decoder NE5900

DESCRIPTION

The NE5900 call progress decoder (CPD) is a low cost, low power CMOS integrated circuit designed to interface with a microprocessor-controlled smart telephone capable of making preprogrammed telephone calls. The call progress decoder information to permit microprocessor decisions whether to initiate, continue, or terminate calls. A tri-state, 3-bit output code indicates the presence of dial tone, audible ring-back, busy signal, or re-order tones.

A front-end bandpass filter is accomplished with switched capacitors. The bandshaped signal is detected and the cadence is measured prior to output decoding. In addition to the three data bits, a buffered bandpass output and envelope output are available. All logic inputs and outputs can interface with LSTTL, CMOS and NMOS.

Circuit features include low power consumption and easy application. Few and inexpensive external components are required. A typical application requires a 3.58MHz crystal or clock, 470kΩ resistor, and two bypass capacitors. The NE5900 is effective where traditional call progress tones, PBX tones, and precision call progress tones must be correctly interpreted with a single circuit.

FEATURES

- Fully decoded tri-state call progress status output
- Works with traditional, precision, or PBX call progress tones
- Low power consumption
- Low cost 3.58MHz crystal or clock
- No calibration or adjustment
- Interfaces with LSTLL, CMOS, NMOS
- Easy application

PIN CONFIGURATION

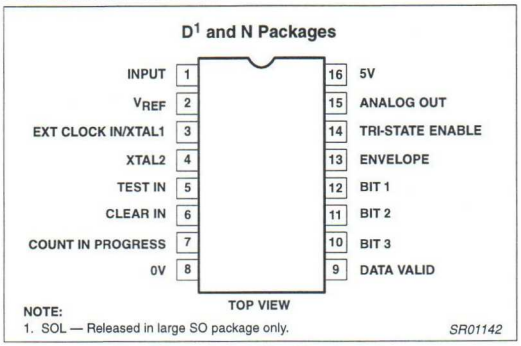


Figure 1. Pin Configuration

APPLICATIONS

- Modems
- PBXs
- Security equipment
- Auto dialers
- Answering machines
- Remote diagnostics
- Pay telephones

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SOL) Package	0 to +70°C	NE5900DK	SOT162-1
16-Pin Plastic Dual In-Line (DIP) Package	0 to +70°C	NE5900N	SOT38-4

BLOCK DIAGRAM

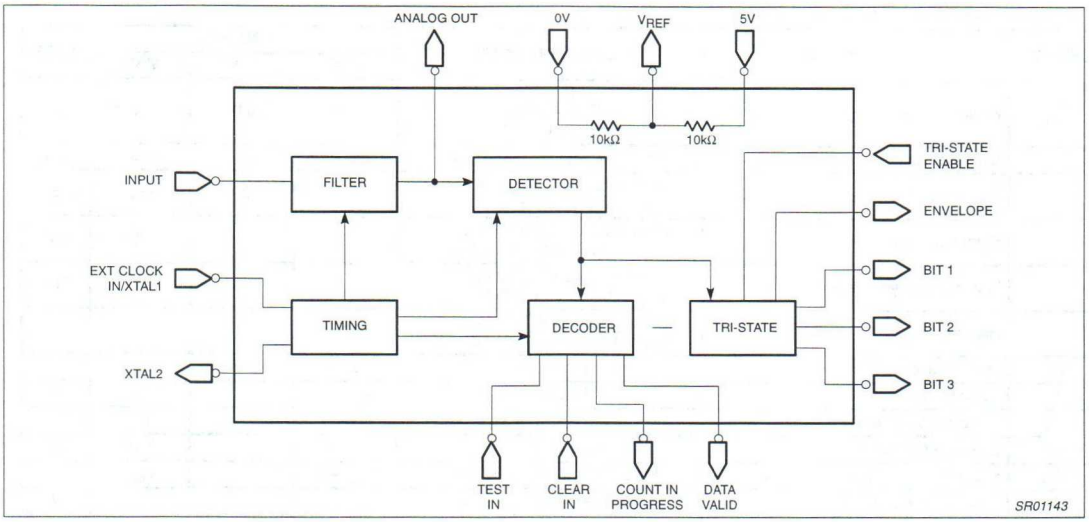


Figure 2. NE5900 Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	9	V
V_{IN}	Logic control input voltages	-0.3 to +16	V
V_{IN}	All other input voltages[1]	-0.3 to V_{CC} + 0.3	V
V_{OUT}	Output voltages	-0.3 to V_{CC} + 0.3	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating temperature range	0 to +70	°C
T_{SOLD}	Lead soldering temperature (10s)	+300	°C
T_{JMAX}	Junction temperature	+150	°C

NOTE:
1. Includes Pin 3 — Ext Clock In

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{DD}	Power supply voltage	Pin 16 Pin 14 = V_{DD} Pin 5, 6 = 0V	4.5	5.0	5.5	V
	Quiescent current	As above with no output loads		2.0	4.0	mA
	Input threshold	Pin 1 level, frequency = 460Hz, V_{DD} = V_{REF} Output Pin 13 = V_{DD}		-39	-35	dB[1]
	Signal rejection	Pin 1 level, frequency = 300Hz, V_{DD} = V_{REF} Output Pin 13 = 0V			-50	dB[1]
	Low frequency[2] rejection	Pin 1 frequency, 0dB max., V_{DC} = V_{REF} Output Pin 13 = 0V			180	Hz
	High frequency[2] rejection	Pin 1 frequency, 0dB max., V_{DC} = V_{REF} Output Pin 13 = 0V	800			Hz
V_{IH}	Logic 1 level	Pins 6, 14	2.0		15	V
V_{IL}	Logic 0 level	Pins 6, 14	0		0.8	V
I_{IH}	Logic 1 input current	Pins 3, 6, 14 = V_{DD}	-1.0		1.0	µA
I_{IL}	Logic 0 input current	Pins 3, 6, 14 = 0V	-1.0		1.0	µA
V_{IH}	Logic 1 input voltage	Pin 3 External Clock In/XTAL	V_{DD} – 1		V_{DD}	V
V_{IL}	Logic 0 input voltage	Pin 3 External Clock In/XTAL	0		1.0	V
V_{OL}	Logic 0 output voltage	I_{SINK} = 1.6mA Pins 7, 9, 10, 11, 12, 13	0		0.4	V
V_{OH}	Logic 1 output voltage	I_{SOURCE} = 0.5mA Pins 7, 9, 10, 11, 12, 13	V_{DD} – 0.4		V_{DD}	V
I_{OZ}	Tri-state leakage	V_{OUT} = V_{DD} or 0V Pins 10, 11, 12, 13, Pin 14 = 0V	-3.0		3.0	µA
	Filter output gain	Input Pin 1, 460Hz – 20dB, V_{DC} = V_{REF} Output Pin 15, R_{LOAD} = 1MΩ	6.5	8.5	10.5	dB
	Filter frequency response	As above from 300Hz to 630Hz, referenced to 460Hz	-1.0		1.0	dBmo
	Input impedance	Pin 1, frequency = 460MHz	1			MΩ
V_{REF}	Reference voltage	Pin 2, V_{DD} = 5V	2.4	2.5	2.6	V
R_{REF}	Reference resistance	Pin 2		5		Ω
	Envelope response time	Time from removal or application of 460Hz – 20dB (V_{DC} = V_{REF} on Pin 1) to response of Pin 13		38		ms

NOTE:
1. 0dB = 0.775V_{RMS}
2. By design; not tested.

The NE5900 uses the signal in the call progress tone passband and the cadence of interrupt rate of the signal to determine which call progress tone is present.

Figure 3 shows a detailed block diagram of the NE5900.

The signal input from the phone line is coupled through a 470kΩ resistor which, together with two internal capacitors and an internal resistor, form an anti-aliasing filter. This passive low pass filter strongly rejects AM radio interference. Insertion loss is typically 1.5dB at 460Hz. The 470kΩ resistor also provides protection from the transients. The input (Pin 1) DC voltage can be derived from V_{REF} (Pin 2) or allowed to self-bias through a series coupling capacitor (10nF minimum).

Following this is a switched capacitor bandpass filter which accepts call progress tones and inhibits tones not in the call progress band of 300Hz to 630Hz. The bandpass limits are determined by the input clock frequency of 3.58MHz. An on-board inverter between Pins 3 and 4 can be used either as a crystal oscillator or as a buffer for an external 3.58MHz clock signal. The switched capacitor filters provide typical rejection of greater than 40dB for frequencies below 120Hz and above 1.6kHz.

The decoder responds to signals between 300Hz and 630Hz with a threshold of -39dB typical (0dB = 0.775V_{RMS}). The decoder will not respond to any signal below -50dB or to tones up to 0dB which are below 180Hz or above 800Hz. Dropouts of 20ms or bursts of only 20ms duration are ignored. A gap of 40ms or a valid tone of 40ms is detected.

The buffered output of the switched capacitor filter is available at the analog output, Pin 15. A logic output representing the detected envelope of this signal is available at the envelope output, Pin 13.

At the start of an in-band tone (envelope output goes high), a 2.3 second interval is timed out. Transitions of the envelope during this interval are counted to determine the signal present. At 2.3 seconds, the three bits of data representing this decision are stored in the latch and appear at the outputs. A data valid signal goes high at this time, signaling that the data bits, Pins 10 – 12, can be read.

The output code is as follows:

	Pin 12	Pin 11	Pin 10
Dial Tone	0	0	0
Ringing Signal	1	0	0
Busy Signal	0	1	0
Re-order Tone	0	0	1
Overflow	1	1	1

The overflow condition occurs in the event that too many transitions occur during the 2.3 second interval. This can result from noise, voice, or other line disturbances not normally present during the post-dialing interval. Note that the end of dial tone in interpreted as a valid ringing signal.

The clear input resets all internal registers and the output latch, and is to be set low after the completion of dialing. The clear input should be pulsed high for proper operation. Recommended pulse width is between 0.2µs and 20ms. If clear is held high when envelope is high, a false output pulse (Pin 13) can result when clear is returned low.

For applications where dialing is done by a person rather than by a microprocessor, an uncertainty exists about the number of digits to be dialed (local vs long distance). In such situations it is possible to clear the NE5900 by application of the DTMF signal or dial pulses to the clear pin (Pin 6). When dialing is complete, the device is cleared and ready to respond to the next call progress unit.

Enable is held at 5V to enable Pins 10, 11, 12 and 13. When enable is brought low, data valid is also set low. Enable must remain high while the data is also set low. Enable must remain high while the data is being read. The test pin is for production test only and must be kept low in all user applications.

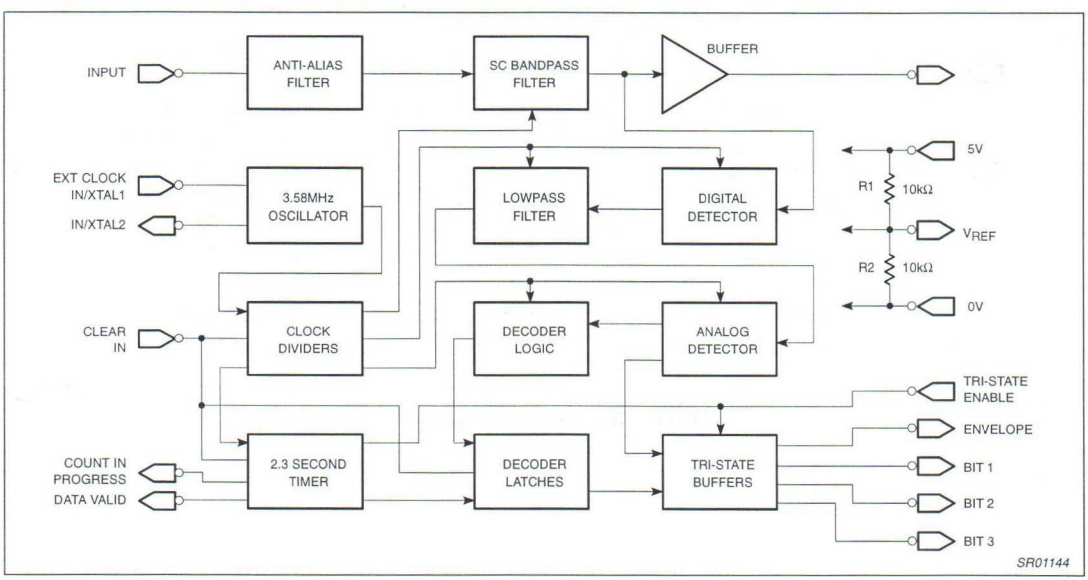


Figure 3. Detailed Block Diagram CPD

Figure 4 shows a typical application of the call progress decoder.

In this application only one external component is needed an no microprocessor activity other than clear is required.

Figure 5 shows the recommended direct interface to the telephone line. Bus connection is possible by utilizing tri-state, and internal timing is accomplished with a 3.58MHz crystal.

The designer can utilize the input signal, clock, bus, or microprocessor interface which best serves the application. Figure 6 gives a typical timing diagram for the application of Figures 4 and 5.

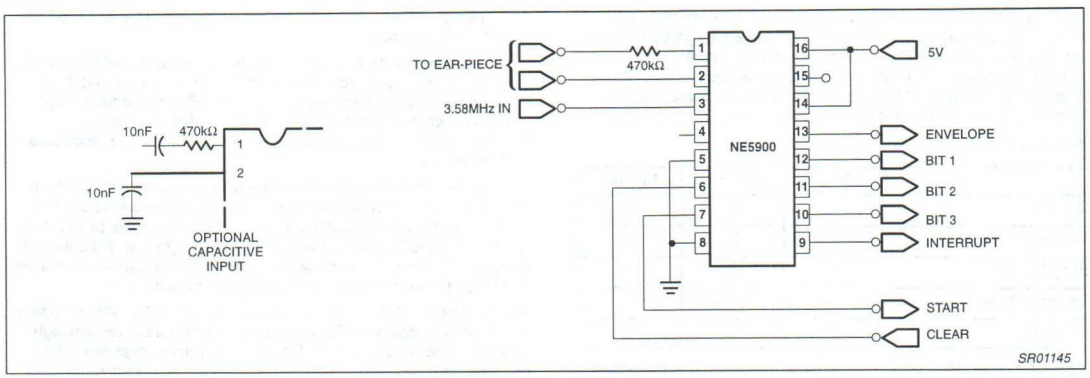


Figure 4. Typical Application

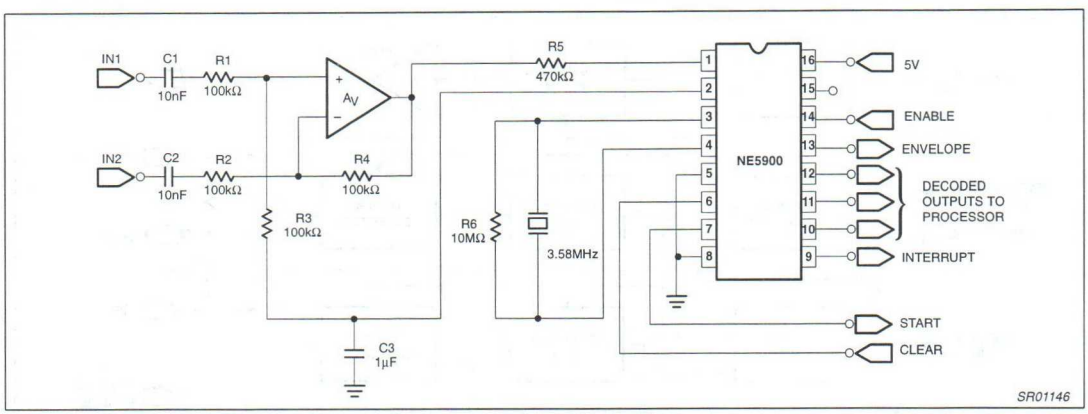


Figure 5. Typical Two-Wire Application

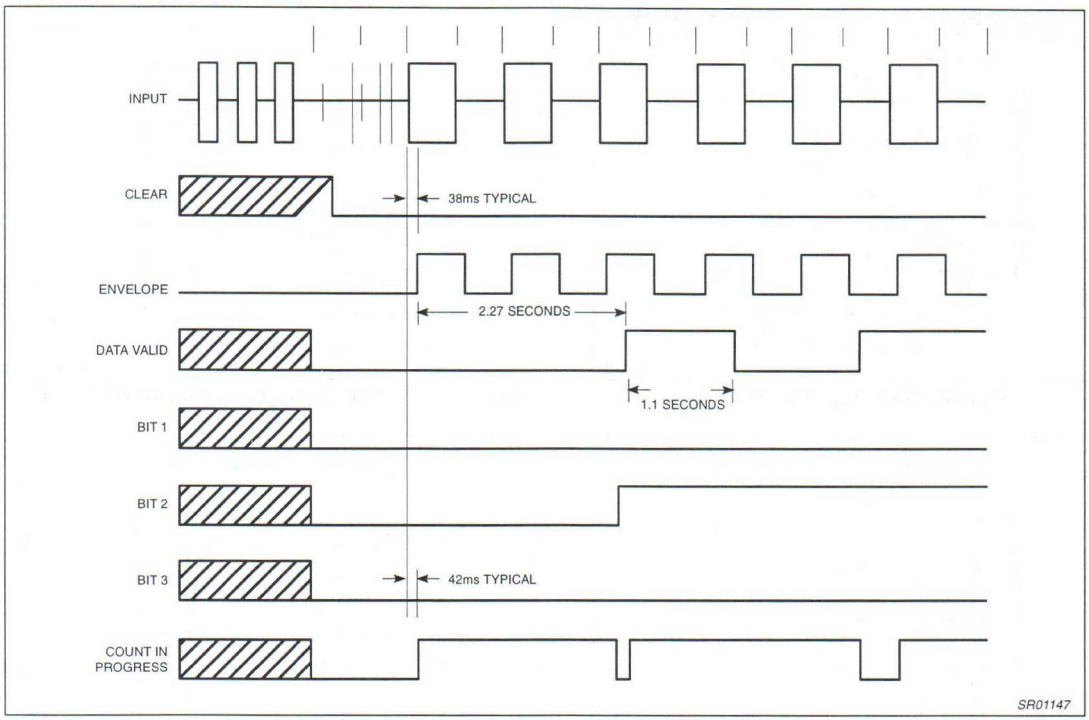

INPUT
CLEAR
38ms TYPICAL
ENVELOPE
2.27 SECONDS
DATA VALID
1.1 SECONDS
BIT 1
BIT 2
BIT 3
42ms TYPICAL
COUNT IN PROGRESS
SR01147

Figure 6.

TYPICAL PERFORMANCE CHARACTERISTICS

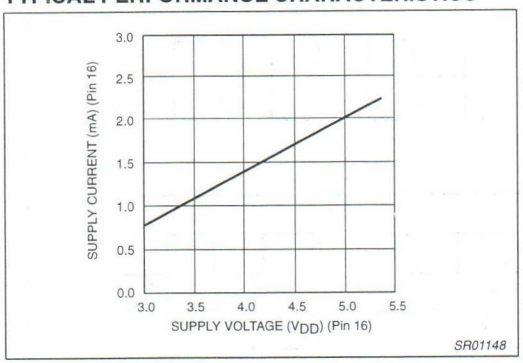


Figure 7. Power Supply Current vs V_{DD}

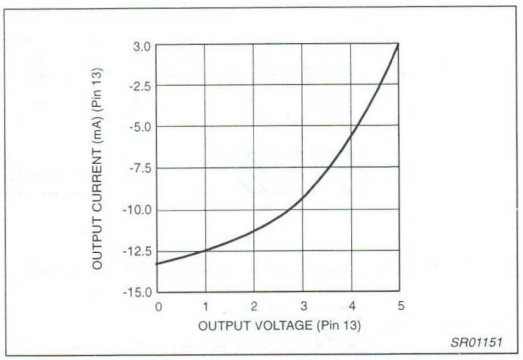


Figure 10. Output Voltage Current Curve Digital Output High

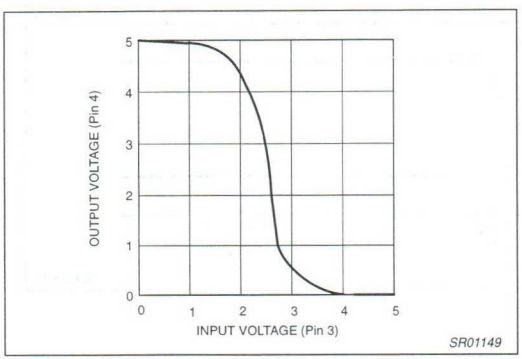


Figure 8. Voltage Transfer Curve

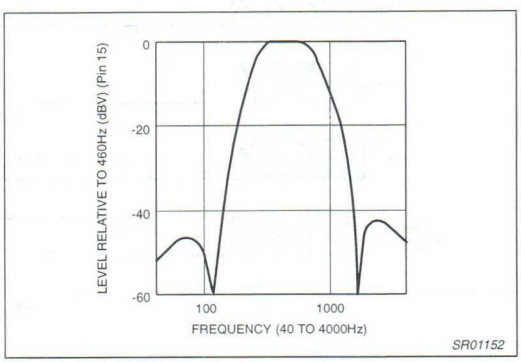


Figure 11. Filter Frequency Response

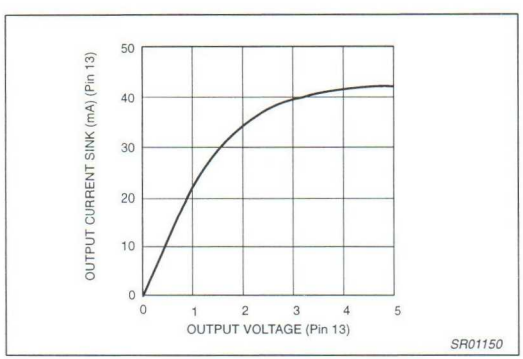


Figure 9. Digital Output Low

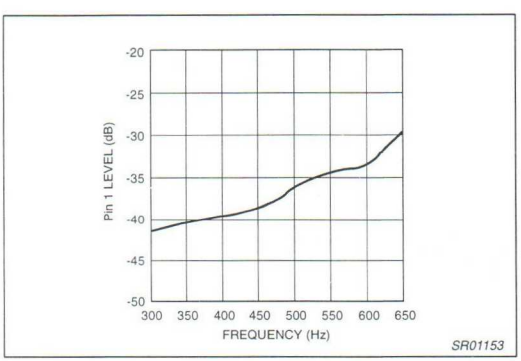


Figure 12. Typical Threshold

Supply circuit with power-down for telephone set peripherals

TEA1081

FEATURES

- High input impedance for audio signals
- Low DC series resistance
- High output current
- Large audio signal handling capability
- Low distortion
- Two modes of operation:
  - output voltage that follows the DC line voltage
  - regulated output voltage
- Power-down input
- Low number of external components.

GENERAL DESCRIPTION

The TEA1081 is an integrated circuit for use in line-powered telephone sets to supply peripheral circuits for extended dialling and/or loudspeaker facilities.

The IC uses a part of the surplus line current normally drawn by the voltage regulator of the speech/transmission circuit. A power-down function isolates the IC from its load and reduces the input current.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	operating DC line voltage		2.5	–	12.0	V
V_O	DC output voltage		2.0	–	10.0	V
ΔV_{LN-O}	voltage drop from line to output	I_O = 0 mA	–	0.5	–	V
R_S	internal series resistance		–	20	–	Ω
I_O	output current (pin 7)	V_{LN} = 4 V				
	TEA1081		–	–	30	mA
	TEA1081T		–	–	20	mA
$V_{LN(rms)}$	AC line voltage (RMS value)	V_{LN} = 4 V; I_O = 15 mA; THD = 2%	–	1.5	–	V
I_{INT}	internal supply current	V_{LN} = 4 V; I_O = 0 mA; PD = LOW; $V_{SP} = V_O$	–	0.8	1.4	mA
T_{amb}	operating ambient temperature		–25	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1081	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TEA1081T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

BLOCK DIAGRAM

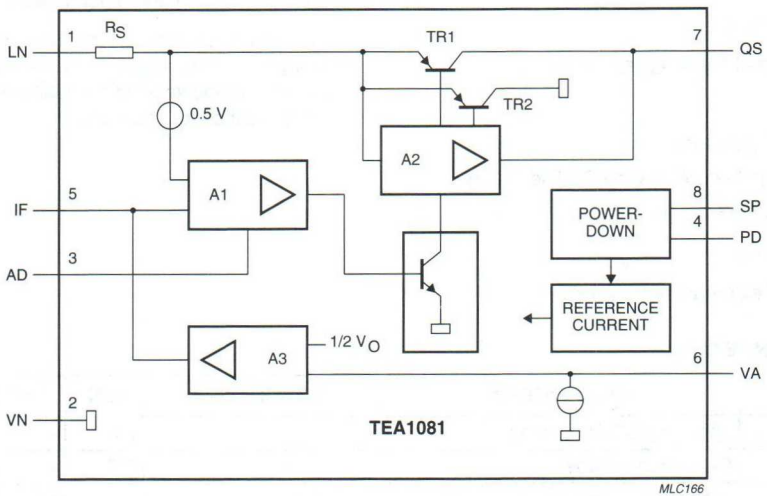


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
VN	2	negative line terminal
AD	3	amplifier decoupling
PD	4	power-down input
IF	5	low-pass filter input
VA	6	output voltage adjustment
QS	7	power supply output
SP	8	supply input; power-down circuit

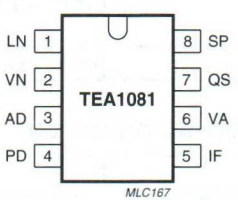


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TEA1081 is a supply interface between telephone line and peripheral devices in the telephone set. The high input impedance of the circuit allows direct connection to the telephone line (via a diode bridge). An inductor function is obtained by amplifier A1, resistor R_S (see Fig.1) and an external low-pass RC filter.

Under the control of amplifier A2, transistor TR1 supplies peripheral devices and transistor TR2 minimizes line signal distortion by momentarily diverting input current to ground whenever the instantaneous value of the line voltage drops below the output voltage.

Internal circuits are biased by a temperature and line voltage compensated reference current source.

The power-down circuit isolates the supply circuit from external circuitry.

Line terminals: LN and VN (pins 1 and 2)

The input terminals LN and VN can be connected directly to the line. The minimum DC line voltage required at the input is expressed by formula (1); see also Table 1.

$$V_{LN} = I_1 \times R_S + V_{LNmin} + V_{LN(P)} \ (V) \qquad (1)$$

Table 1 Explanation of formula (1).

SYMBOL	DESCRIPTION
I_1	input current
R_S	internal series resistance
V_{LNmin}	minimum instantaneous line voltage (1.4 V at I_O = 5 mA)
$V_{LN(P)}$	required peak level of AC line voltage

The internal current (I_{INT}) at I_O = 0 mA is typically 0.8 mA at V_{LN} = 4 V and reaches a maximum of 1.4 mA at V_{LN} = 12 V.

Supply terminals: QS and VA (pins 7 and 6)

Peripheral devices are supplied from QS (pin 7). Two modes of output voltage regulation are available.

OUTPUT VOLTAGE FOLLOWS LINE VOLTAGE (SEE FIG.3)

The TEA1081 operates in this mode when there is no external resistor (R_V) between QS and VA (see Fig.6).

The output voltage follows the line voltage and is expressed by formula (2); see also Table 2.

$$V_O = V_{LN} - (I_1 \times R_S + 0.5) \ (V) \qquad (2)$$

Table 2 Explanation of formula (2).

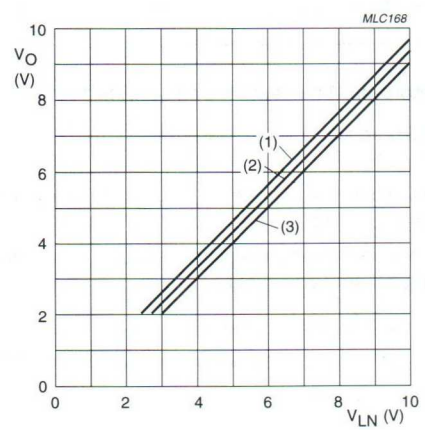
SYMBOL	DESCRIPTION
V_{LN}	line voltage
I_1	input current
R_S	internal series resistance

REGULATED OUTPUT VOLTAGE (SEE FIG.4)

The circuit operates in this mode when an external resistor (R_V) is connected between QS and VA (see Fig.6).

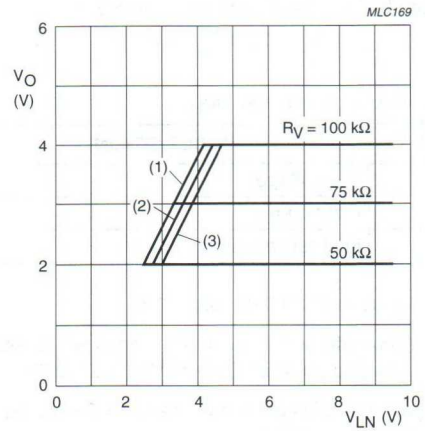
The output voltage is held constant at $V_O = 2 \times I_6 \times R_V$ (V) as soon as the line voltage $V_{LN} > (2 \times I_6 \times R_V + I_1 \times R_S + 0.5)$ (V)

The control current I6 is typically 20 μA.



Application without R_V.
(1) I_1 = 5 mA.
(2) I_1 = 20 mA.
(3) I_1 = 30 mA; not valid for TEA1081T.

Fig.3 Output voltage as a function of line voltage.



R_V connected between QS and VA.
(1) I_1 = 5 mA.
(2) I_1 = 20 mA.
(3) I_1 = 30 mA; not valid for TEA1081T.

Fig.4 Output voltage as a function of line voltage.

Input and output currents I_1 and I_O (pins 1 and 7)

The maximum available current into pin 1 (I_1) is determined by:

- The minimum line current ($I_{LINEmin}$) that is available for the telephone set
- The specified minimum input current (I_{LNmin}) for the speech/transmission circuit.

That is $I_{1max} = I_{LINEmin} - I_{LNmin}$.

At $V_{LN(rms)} < 150$ mV, the input current I_1 is approximately:

$I_1 = I_{INT} + k \times I_O$ (mA)

Where:

I_{INT} = internal supply current (0.8 mA at V_{LN} = 4 V);

k = correction factor (k < 1.1 for the specified output current range).

With large line signals the instantaneous line voltage may drop below V_O + 0.4 V. Normally (when $V_{LN} > V_O + 0.4$ V), instantaneous current flows from LN to QS (pin 1 to pin 7) to the output load.

When $V_{LN} < V_O + 0.4$ V, the instantaneous current is diverted to pin 2 to prevent distortion of the line signal.

Input current at $V_{LN(rms)}$ = 1 V and without R_V approximates to:

$I_1 = I_{INT} + 2 \times I_O$ (mA)

The maximum supply current (within the specified output current limits) available for peripheral devices is shown by:

$$I_{Omax} = \frac{I_{LINEmin} - I_{LNmin} - I_{INT}}{2}$$

Where:

$I_{LINEmin}$ is the minimum line current of the telephone set;

I_{LNmin} is the specified minimum input current of the speech/transmission circuit.

Input low-pass filter: IF (pin 5)

The input impedance between LN and VN at audio frequencies is determined by the filter elements C_L (between pins 1 and 5), R_L (between pins 5 and 7) and the internal resistor R_S (typical value 20 Ω).

At audio frequencies the TEA1081 behaves as an inductor of the value $L_I = C_L \times R_L \times R_S$ (H). The typical value of L_I at C_L = 2.2 μF and R_L = 100 kΩ is 4.4 H.

Amplifier decoupling: AD (pin 3)

To ensure stability, a 68 pF decoupling capacitor is required between AD (pin 3) and LN (pin 1).
If $I_{Omin} < 1.5$ mA, a 47 pF capacitor has to be added between AD (pin 3) and VA (pin 6).

Power-down inputs: PD and SP (pins 4 and 8)

During pulse dialling or register recall, or if the input current to pin 1 is insufficient to maintain the output current, the supply to peripheral devices can be switched off by activating the PD input at pin 4. With PD = HIGH, the input current is reduced to 40 μA (typ.) at V_{LN} = 4 V and the internal circuits are isolated from the load at QS (pin 7).

The power-down circuit is supplied via the SP input (pin 8). SP can be wired to QS in conditions where $V_O > V_{SPmin}$ during line interruptions. When $V_O < V_{SPmin}$, SP should be wired to an external supply point (e.g. to V_{CC} of the TEA1060 family circuit).

When power-down is not required, the PD and SP inputs can be left open-circuit.

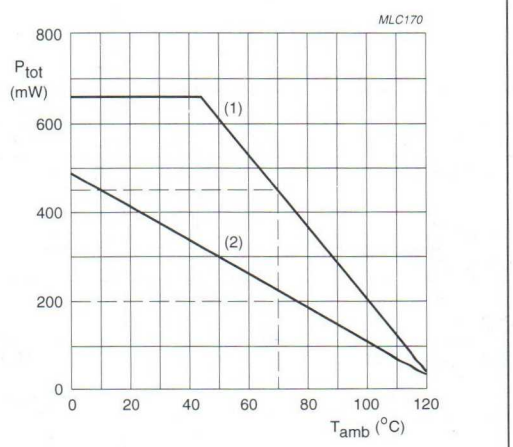
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive line voltage	continuous	–	12	V
		during switch-on or line interruptions	–	12.5	V
$V_{LN(RM)}$	repetitive peak line voltage for a 1 ms pulse per 5 s	12 Ω resistor in series with pin 1	–	28	V
V_I	input voltage (all other terminals)		V_{VN} – 0.5	V_{LN} + 0.5	V
I_1	DC input current				
	TEA1081		–	120	mA
	TEA1081T		–	80	mA
I_I	input current (all other terminals)		–1	+1	mA
P_{tot}	total power dissipation		see Fig.5		
T_{amb}	operating ambient temperature		–25	+70	°C
T_{stg}	storage temperature		–40	+125	°C
T_j	junction temperature		–	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1081	120	K/W
	TEA1081T (mounted on a printed-circuit board of 50 × 50 × 1.5 mm)	260	K/W



(1) TEA1081.
(2) TEA1081T.

Fig.5 Power derating curves.

CHARACTERISTICS

V_{LN} = 4 V; $V_{LN(rms)}$ = 100 mV; I_O = 5 mA; f = 300 to 3400 Hz; R_L = 100 kΩ; C_L = 2.2 μF; R_V = 75 kΩ; T_{amb} = 25 °C; unless otherwise specified; see Fig.6.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	operating DC line voltage		2.5	–	12.0	V
V_{LNmin}	minimum instantaneous line voltage		–	–	1.4	V
V_{LNmax}	maximum instantaneous line voltage		12.0	–	–	V
Characteristics with R_V = 75 kΩ connected between pins 6 and 7 and C_L = 10 μF						
I_1	input current (pin 1)	$V_{LN(rms)}$ = 0 V	–	5.8	–	mA
		$V_{LN(rms)}$ = 1.5 V; I_O = 15 mA	–	30	–	mA
V_O	output voltage (pin 7)		–	3.0	–	V
ΔV_O	variation of output voltage over the ranges of:					
	line voltage	V_{LN} = 4 to 6 V	–	100	–	mV
	temperature	T_{amb} = +25 to −25 °C	–	−100	–	mV
	temperature	T_{amb} = +25 to +75 °C	–	−100	–	mV
	output current	I_O = 5 to 20 mA	–	−100	–	mV
I_6	control current (pin 6)		–	20	–	μA
Characteristics without R_V						
I_1	input current (pin 1)	$V_{LN(rms)}$ = 0 V	–	6.0	–	mA
		$V_{LN(rms)}$ = 1.5 V; I_O = 15 mA	–	31	–	mA
ΔV_{LN-O}	voltage drop from line to output	I_O = 0 mA	–	0.5	–	V
		I_O = 15 mA; $V_{LN(rms)}$ = 1.5 V	–	1.1	–	V
I_O	output current (pin 7)					
	TEA1081		–	–	30	mA
	TEA1081T		–	–	20	mA
R_S	internal series resistance		–	20	–	Ω
I_{INT}	internal supply current	I_O = 0 mA; PD = LOW; V_{SP} = V_O	–	0.8	1.4	mA
		I_O = 0 mA; PD = HIGH (note 1); V_{SP} > 2 V	–	40	60	μA
THD	total harmonic distortion	$V_{LN(rms)}$ = 1.5 V	–	–	2	%
BRL	balance return loss	600 Ω reference	25	–	–	dB
$V_{LN(2H)}$	second harmonic level of line voltage	f = 500 Hz; V_{LN} = 0 dBm; Z_{line} = 600 Ω	–	−58	–	dBm
$V_{LN(3H)}$	third harmonic level of line voltage	f = 500 Hz; V_{LN} = 0 dBm; Z_{line} = 600 Ω	–	−60	–	dBm
$V_{ni(rms)}$	noise voltage on input terminal (RMS value)	$V_{LN(rms)}$ = 0 V; R_L = 600 Ω; P53 curve	–	−83	–	dBmp
Power-down input (pin 4)						
V_{IL}	LOW level input voltage		–	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{SP}	V
I_4	input current		–	–	10	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power-down input (pin 8)						
V_8	supply voltage for power-down		2	–	V_{LN}	V
I_8	supply current to power-down circuit	V_8 = 3 V	–	–	70	μA

Note

1. Power-down circuit supplied via external source.

APPLICATION INFORMATION

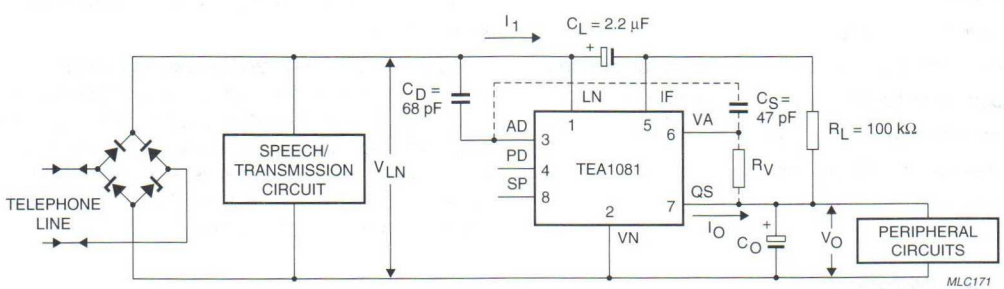


Fig.6 Application diagram.

Line interrupter driver and ringer UBA1702; UBA1702A

FEATURES

Speech part

- Driver for the line interrupter that can be either a PMOST when UBA1702 is used or a PNP when UBA1702A is used
- Adjustable over-current protection
- Adjustable over-voltage protection for transmission circuit
- Adjustable mute (dialling mode voltage; DMO or NSA)
- Adjustable current loop detection (hook switch status)
- Microcontroller supply
- Provision for electronic hook switch.

Ringer part

- Over-voltage protection
- Ringer frequency output for frequency discrimination
- Adjustable ringer threshold for piezo-driver enable
- Three bits ringer volume control
- Bridge-tied-load (BTL) output stage for piezo transducer
- Fast start-up microcontroller supply.

Miscellaneous

- Separated ground pins for transmission circuit interface and control signals (e.g. for TEA1064A)
- Possibility to supply the microcontroller with an external voltage source.

APPLICATIONS

- Telephone sets with software controlled ringer function
- Telephone sets with electronic hook switch.

GENERAL DESCRIPTION

The UBA1702; UBA1702A performs the high voltage interface and ringer functions of the corded analog telephone set in close cooperation with a microcontroller and transmission circuit.

The UBA1702; UBA1702A incorporates several protections, a driver for the line interrupter and a ringer. Because of the practical division of functions between the microcontroller, the transmission circuit and the UBA1702; UBA1702A, it is possible to have a higher integration level thereby reducing significantly the number of discrete components in a telephone set.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UBA1702	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
UBA1702A	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
UBA1702T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
UBA1702AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

QUICK REFERENCE DATA

Speech part: I_{line} = 20 mA; DPI = LOW; T_{amb} = 25 °C; V_{EE} = 0 V; unless otherwise specified.
Ringer part: $V_{line(rms)}$ = 45 V; f = 25 Hz; using an RC combination of 2.2 kΩ and 820 nF and a diode bridge between the line and the RPI input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Speech part						
SWITCH DRIVER AND REFERENCES (PINS SDI, SDO, EHI AND DPI); UBA1702A ONLY						
R_{SDO}	resistance between pins SDO and V_{EE}		–	2.2	–	kΩ
SWITCH DRIVER AND REFERENCES (PINS SDI, SDO, EHI AND DPI); UBA1702 AND UBA1702A						
$R_{SDI-SDO}$	resistance between pins SDI and SDO	$V_{SDI} - V_{SDO} < 12$ V	–	1.1	–	MΩ
R_{SDI}	resistance between pins SDI and V_{EE}	V_{SDI} = 240 V; DPI = HIGH	5	–	–	MΩ
MUTE SWITCH AND ADJUSTABLE PROTECTION ZENER VOLTAGE (PINS MSI, MSA AND ZPA)						
$V_{SPO(M)}$	adjustable mute voltage referenced to V_{EE}	MSI = HIGH; MSA open-circuit	–	2.7	3	V
$V_{SPO(Z)}$	adjustable zener voltage referenced to V_{EE}	MSI = LOW; ZPA open-circuit	11	12	13	V
CURRENT MANAGEMENT (PINS SPI, SPO, CDA, CLA AND CDO)						
$I_{SPI(lim)}$	current limitation (pin SPI)	CLA shorted to V_{EE}	–	120	–	mA
$I_{SPI(det)}$	current detection (pin SPI)	CDA open-circuit	2	3	4	mA
MICROCONTROLLER SUPPLY (V_{DD} AND V_{BB})						
V_{DD}	supply output voltage referenced to V_{SS}	V_{BB} > 3.7 V; I_{DD} = −1 mA	3.0	3.3	3.6	V
Ringer part						
PROTECTION (PIN RPI)						
$I_{RPI(max)}$	maximum input current		70	–	–	mA
RINGER THRESHOLD AND FREQUENCY DETECTION (PINS V_{RR}, RTA AND RFO)						
$V_{RR(th)}$	ringer supply threshold voltage referenced to V_{SS}	RTA open-circuit	–	11	–	V
VOLUME CONTROL (PINS RV0, RV1 AND RV2)						
ΔG_s	step resolution	(RV2, RV1, RV0) from (0, 0, 0) to (1, 1, 0); note 1	–	6	–	dB
ΔG_{ls}	last step resolution	(RV2, RV1, RV0) from (1, 1, 0) to (1, 1, 1); note 2	–	9.5	12	dB
RINGER MELODY INPUT AND PIEZO DRIVER (PINS RMI, ROA AND ROB)						
$V_{o(max\ p-p)}$	maximum output voltage between pins ROA and ROB (peak-to-peak value)	RV2 = 1; RV1 = 1; RV0 = 1	–	28.7	32	V

Notes

1. Independent of V_{RR} if greater than 10 V.
2. Without piezo transducer, dependent on V_{RR}.

BLOCK DIAGRAM

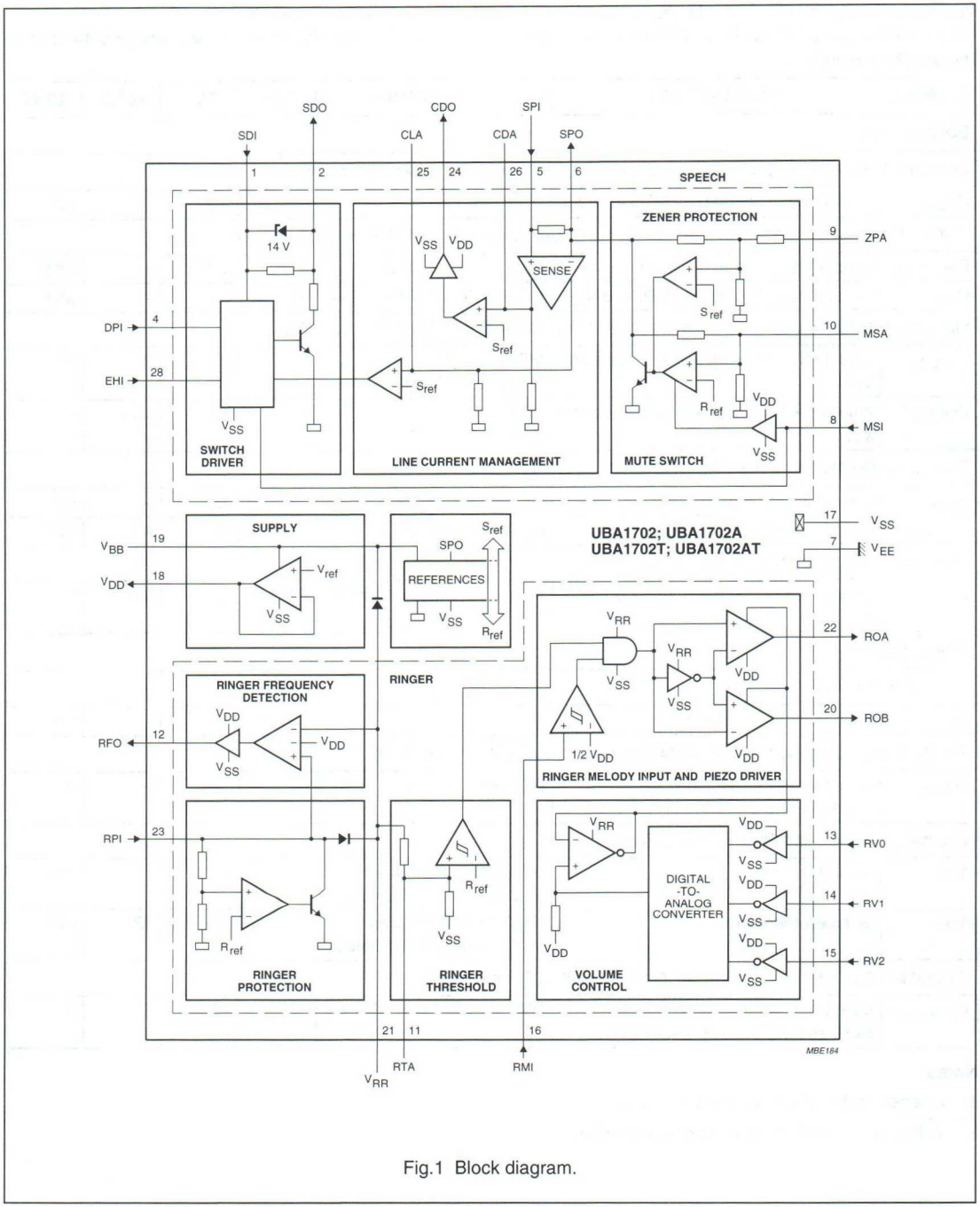


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDI	1	switch driver input
SDO	2	switch driver output
n.c.	3	not connected
DPI	4	dialling pulse input
SPI	5	speech part input
SPO	6	speech part output
V_{EE}	7	ground for transmission circuit
MSI	8	mute switch input
ZPA	9	Zener protection adjustment input
MSA	10	mute switch adjustment input
RTA	11	ringer threshold adjustment input
RFO	12	ringer frequency output
RV0	13	ringer volume input; bit 0
RV1	14	ringer volume input; bit 1
RV2	15	ringer volume input; bit 2
RMI	16	ringer melody input
V_{SS}	17	ground for microcontroller and ringer
V_{DD}	18	microcontroller supply voltage
V_{BB}	19	supply voltage from transmission circuit
ROB	20	ringer output B
V_{RR}	21	ringer supply voltage
ROA	22	ringer output A
RPI	23	ringer part input
CDO	24	current detection output
CLA	25	current limitation adjustment input
CDA	26	current detection adjustment input
n.c.	27	not connected
EHI	28	electronic hook switch input

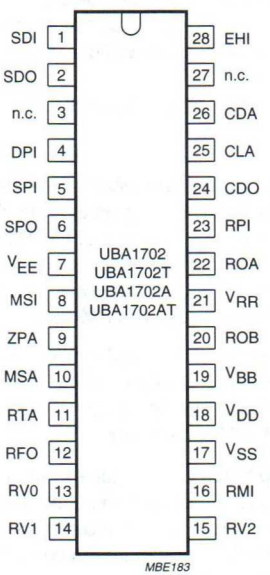


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The values given in this functional description are typical values except when otherwise specified.

Speech part

The speech part consists of three blocks, the switch driver, the line current management and the mute switch (DMO or NSA) combined with an adjustable over-voltage (zener) protection circuit. The reference block, which generates reference voltages and currents, is also used in the speech part (see Fig.1) by the mute switch block.

SWITCH DRIVER (PINS SDI, SDO, EHI AND DPI)

UBA1702

The UBA1702 switch driver block is intended to generate the appropriate signal to drive an external PMOST interrupter. The source and gate of this PMOST are respectively connected to SDI and SDO. The electronic hook switch input (EHI) and the dialling pulse input (DPI) signals control the state of this PMOST.

The EHI pin is provided with high voltage capability. When the voltage applied at pin EHI is HIGH, the switch driver block will start and generate the proper signals to switch on the external PMOST interrupter.

When the telephone set is equipped with a mechanical hook switch, pin EHI can be connected directly to the switch driver input (pin SDI). For electronic hook switch applications, the EHI pin can be driven by the microcontroller output.

In some special applications, the EHI pin can be current driven. In such a case, the current available at SDO to turn on the PMOST interrupter is approximately 10 times the EHI input current (providing $I_{EHI} < 2\ \mu A$).

The EHI pin presents an impedance of 250 kΩ at low input voltage. When the applied voltage at EHI goes above approximately 30 V, the EHI input current remains constant (see Fig.3) so that the EHI impedance increases.

The DPI is designed to switch on or off the external PMOST interrupter (providing EHI is HIGH). When the voltage applied at pin DPI is HIGH, the switch driver block turns off the external PMOST interrupter. When the voltage applied at pin DPI is LOW, the switch driver block turns on the external PMOST interrupter.

The external PMOST interrupter is controlled by the voltage between the switch driver input and output (pins SDI and SDO).

When the voltage applied at pin EHI is HIGH and the voltage applied at pin DPI is LOW, the voltage at SDO is pulled down to a value less than 0.2 V in order to create a high source-gate voltage (V_{SG}) for the external PMOST. However, in order to avoid break-down of the external PMOST, the voltage difference between SDI and SDO is internally limited to 14 V.

When the voltage applied at pin EHI and the one applied at pin DPI are both HIGH, pin SDO can be considered as being connected to pin SDI via a 1.1 MΩ pull-up resistor while the impedance between SDI and V_{EE} becomes very high (a few MΩ).

When the voltage applied at pin EHI is LOW, whatever the one applied at DPI is, pin SDO can be considered as being connected to pin SDI via a 1.1 MΩ pull-up resistor while the impedance between SDI and V_{EE} becomes almost infinite.

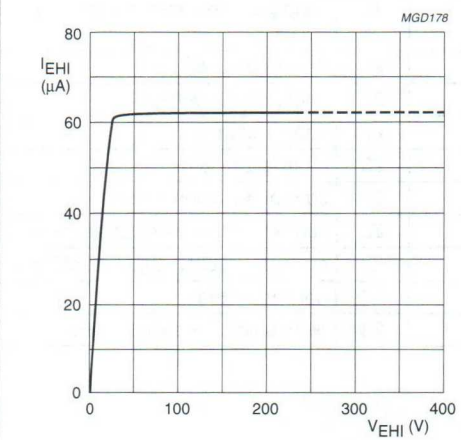


Fig.3 EHI input characteristics.

UBA1702A

The UBA1702A switch driver block is intended to generate the appropriate signal to drive an external PNP interrupter. The emitter and base of this PNP are respectively connected to SDI and SDO. The EHI and DPI signals control the state of this PNP.

The EHI pin is provided with high voltage capability. When the voltage applied at pin EHI is HIGH, the switch driver block will start and generate the appropriate signals to switch on the external PNP interrupter.

When the telephone set is equipped with a mechanical hook switch, pin EHI can be connected directly to pin SDI. For electronic hook switch applications, the EHI pin can be driven by the microcontroller output.

The EHI pin presents an impedance of 250 kΩ at low input voltage. When the applied voltage at EHI goes above approximately 30 V, the EHI input current remains constant (see Fig.3) so that the EHI impedance increases.

The DPI is designed to switch on or off the external PNP interrupter (providing EHI is HIGH). When the voltage applied at pin DPI is HIGH, the switch driver block turns off the external PNP interrupter. When the voltage applied at pin DPI is LOW, the switch driver block turns on the external PNP interrupter.

The external PNP interrupter is controlled by the current flowing into pin SDO.

When the voltage applied at pin EHI is HIGH and the voltage applied at pin DPI is LOW, pin SDO can be considered as being connected to pin V_{EE} via a 2.2 kΩ resistor in order to create a base current for the external PNP.

When the voltage applied at pin EHI and the one applied at pin DPI are both HIGH, pin SDO can be considered as being connected to pin SDI via a 1.1 MΩ pull-up resistor while the impedance between SDI and V_{EE} becomes very high (a few MΩ).

When the voltage applied at pin EHI is LOW, whatever the one applied at DPI is, pin SDO can be considered as being connected to pin SDI via a 1.1 MΩ pull-up resistor while the impedance between SDI and V_{EE} becomes almost infinite.

LINE CURRENT MANAGEMENT
(PINS SPI, SPO, CDA, CLA AND CDO)

The line current is measured by an internal 2 Ω resistor and a sense circuit connected between the speech part input and output (pins SPI and SPO). The circuit delivers information about the hook switch status at the current detection output (pin CDO) and controls the line current limitation.

When the SPI current exceeds a certain level (3 mA), the sense circuit injects some image of the SPI current into an internal resistor (see Fig.1). The created voltage becomes higher than an internal reference (approximately 0.3 V) and CDO goes HIGH. This current detection level can be increased by connecting a resistor between pins CDA (current detection adjustment) and V_{EE}. It is also possible to connect a capacitor between pins CDA and V_{EE} to filter unwanted AC components of the line current signal. Line current interruption during pulse dialling influences the CDO output.

When the SPI current exceeds another current level (45 mA), the sense circuit injects some image of the SPI current into an internal resistor (see Fig.1). The created voltage becomes higher than an internal reference (approximately 0.4 V) and an internal signal is generated in order to limit the current in the external interrupter thus resulting in a line current limitation. This line current limitation level can be increased up to a maximum value of 120 mA by connecting a resistor between pins CLA (current limitation adjustment) and V_{EE}.

When a PMOST (UBA1702) is used as an interrupter, the SPI current equals the drain or source current of the PMOST and thus also equals the line current.

When a PNP (UBA1702A) is used as an interrupter, the SPI current equals the collector current of the PNP and thus differs from the line current (the PNP base current does not flow into the SPI pin).

MUTE SWITCH AND ZENER PROTECTION (PINS MSI, MSA AND ZPA)

The mute switch is, in fact, a switchable and electronic zener diode connected between the speech part output (pin SPO) and V_{EE}.

When the voltage applied at the mute switch input (pin MSI) is LOW, the switch is in over-voltage protection mode and the maximum SPO voltage is limited to 12 V. This level can be increased or decreased by connecting a resistor between pins ZPA (zener protection adjustment) and V_{EE} or ZPA and SPO respectively.

When the voltage applied at pin MSI is HIGH, the switch is in mute mode (DMO or NSA) resulting in a SPO voltage below 3 V. This level can be decreased by connecting a resistor between pins MSA (mute switch adjustment) and SPO. It should be noted that the mute switch stage is supplied from V_{DD} thus a minimum voltage of approximately 2.1 V is required on V_{DD}.

REFERENCE

The bias currents and voltages for the various speech blocks are generated by the reference block which is, in most cases, supplied from pin SPO. This block guarantees a high AC impedance at the SPO pin operating down to a low SPO voltage. Therefore, most speech part blocks operate independently from V_{DD}.

Ringer part

The ringer part consists of five blocks, the ringer protection, the ringer threshold, the ringer frequency detection, the volume control and the piezo driver. The reference block which generates reference voltages and currents is also used in the ringer part (see Fig.1).

RINGER PROTECTION (PINS RPI AND V_{RR})

The ringer protection block converts the ringing current into a limited voltage between the ringer part input (pin RPI) and V_{EE}. This voltage is used (via an internal diode) to generate the ringer supply voltage V_{RR} which is mainly used for all ringer parts. The voltage at pin V_{RR} must be filtered with a 22 µF capacitor connected between pins V_{RR} and V_{SS}.

In electronic hook switch applications and also in speech mode (see Fig.8), pin RPI is always connected to the telephone line (through a series RC network and a diode bridge). In order not to disturb normal speech operation, a high AC impedance is present at pin RPI (providing the speech level is less than 1.5 V (RMS) i.e. 5.7 dBm).

In the DMO or NSA mode (i.e. MSI is HIGH), the voltage across RPI and V_{EE} is limited to 2.1 V. With this feature and in electronic hook switch applications, several additional ringers can be placed in parallel without tinkling during pulse dialling phase.

RINGER THRESHOLD (PIN RTA)

The piezo driver is internally enabled when the voltage at pin V_{RR} exceeds a threshold level of 11 V. This threshold level can be increased or decreased by connecting a resistor between pins RTA (ringer threshold adjustment) and V_{SS} or RTA and V_{RR} respectively.

Because of the built-in 6.5 V hysteresis, a voltage change at pin V_{RR} (coming from current consumption increase when the piezo output is driven with a melody) will have no influence on this internal enabling signal.

RINGER FREQUENCY DETECTION (PIN RFO)

The ringer frequency detection block generates a square wave signal at the ringer frequency output (pin RFO) with twice the ringer signal frequency. This RFO signal can be used by the microcontroller for frequency discrimination.

When the voltage at pin RPI drops below the voltage at pin V_{DD}, RFO goes LOW. Pin RFO goes HIGH when the voltage at pin RPI exceeds the voltage at pin V_{RR}. This $V_{RR} - V_{DD}$ hysteresis allows the frequency detection circuit to ignore parasitic signals superimposed on the ringing signal.

The voltage at pin EHI must be LOW to get a square wave at pin RFO. When the voltage at pin EHI is LOW, the voltage at pin RFO is always HIGH whatever the one at pin RPI is.

VOLUME CONTROL (PINS RV0, RV1 AND RV2)

The volume control input has three bits RV2, RV1 and RV0 to realize eight volume levels. The volume is controlled by regulating the supply voltage of the piezo output stage. The first six steps have a fixed value of 6 dB, the value of the last step (maximum volume) is dependent on the available voltage at pin V_{RR}.

Default setting during start-up is (RV2 = 0, RV1 = 0, RV0 = 0) which corresponds to minimum volume. In order not to damage the piezo transducer, the differential output ROA – ROB is internally limited to a value less than 32 V (p-p).

RINGER MELODY INPUT AND PIEZO DRIVER (PINS RMI, ROA AND ROB)

The input signal at the ringer melody input (pin RMI) may be a square wave or a sine wave which is generated by the microcontroller. The input stage incorporates a small hysteresis (between $0.48V_{DD}$ and $0.52V_{DD}$) and is referenced to $\frac{1}{2}V_{DD}$ which is also the DC level of the signal coming from the microcontroller. Nevertheless, when a sine wave is used, a coupling capacitor of 10 nF (connected between pin RMI and the output of the microcontroller) is required. This 10 nF capacitor value is enough since the RMI input impedance is approximately 250 kΩ.

The piezo driver is an output stage for a piezo transducer which has to be connected between ringer output A and ringer output B (pins ROA and ROB) as a Bridged Tied Load (BTL) or between ROA and V_{SS} as a Single-Ended Load (SEL). The ROA and ROB output signals are square wave and in opposite phase driven by the ringer melody input stage. The minimum output current capability of the ROA and ROB outputs is greater than 80 mA at maximum volume setting (RV2 = 1, RV1 = 1, RV0 = 1) and becomes even greater during output switching. This gives fast rise and fall times resulting in a lot of harmonics.

To obtain maximum efficiency, the piezo driver stage is supplied in series with the V_{DD} supply.

REFERENCE

The bias current for the various ringer blocks is generated by the reference block while this block is supplied from pin V_{RR} or V_{DD}.

Supply part (pins V_{BB} and V_{DD})

The supply block regulates the voltage at pin V_{DD}, referenced to V_{SS}, to a typical value of 3.3 V and can deliver a minimum of 2 mA. This is sufficient to supply most normal microcontrollers. The voltage at pin V_{DD} must be filtered with a 22 μF capacitor connected between pins V_{DD} and V_{SS}.

In speech mode, this block is supplied from the transmission circuit using pin V_{BB}. The voltage drop between V_{BB} and V_{DD} has been minimized (100 mV at 1 mA, providing $2.5\ V < V_{BB} < 3.0\ V$) in order to allow low voltage operation of the transmission circuit.

In ringer mode, this block is supplied from the ringer part using pin V_{RR} and pin V_{BB} which are tied together through an internal diode (see Fig.1).

When an external (mains or battery) supply is connected to V_{BB} and no speech or ringer signal is applied, V_{DD} (3.3 V) is still present.

During on-hook phase, and when a small current is derived from the line to the microcontroller supply, the circuit stays in a kind of stand-by mode to provide sufficient voltage at pin V_{DD}. This is done to ensure memory retention in the microcontroller.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{SDI}, V_{SDO}	maximum input/output switch driver voltage (pins SDI or SDO)	DC; note 1	–	240	V
		pulsed; note 2	–	400	V
V_{EHI}	maximum hook switch input voltage (pin EHI)	DC; note 1	–	240	V
		pulsed; note 2	–	400	V
$V_{i(max)}$	maximum voltage at all logic inputs (pins DPI, MSI, RV0, RV1, RV2 and RMI)		V_{SS} – 0.4	V_{DD} + 0.4	V
$V_{n(max)}$	maximum voltage at all other pins		–	24	V
$I_{SPI(max)}$	maximum speech part input current (pin SPI)		–	150	mA
$I_{RPI(max)}$	maximum ringer part input current (pin RPI)		–	70	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C			
	UBA1702		–	1	W
	UBA1702T		–	0.625	W
T_{stg}	IC storage temperature		–40	+150	°C
T_{amb}	operating ambient temperature		–25	+75	°C

Notes

1. Continuous.
2. 2 kV surge:
   a) according to IEC 805-1 part 5. Test generator 10 µs/700 µs according to CCITT (Rm1 = 15 Ω and Rm2 = 25 Ω).
   b) pulse sequence > 60 s.
   c) number of surges: 10.
   d) polarity change after 5 surges.
   e) test circuit in combination with 150 V Voltage Dependent Resistor (VDR) and a 3.9 Ω resistor connected in series with the source of the PMOST interrupter (UBA1702).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air		
	UBA1702, UBA1702A	45	K/W
	UBA1702T, UBA1702AT	70	K/W

CHARACTERISTICS

Speech part: I_{line} = 20 mA; DPI = LOW; T_{amb} = 25 °C; V_{EE} = 0 V; unless otherwise specified.
Ringer part: $V_{line(rms)}$ = 45 V; f = 25 Hz; using an RC combination of 2.2 kΩ and 820 nF and a diode bridge between the line and the RPI input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Speech Part						
SWITCH DRIVER AND REFERENCES (PINS SDI, SDO, EHI AND DPI); UBA1702 ONLY						
I_{EE}	V_{EE} current consumption	V_{SPO} = 4.2 V	–	−330	–	μA
V_{SDO}	switch driver output voltage	V_{SDI} < 12 V	–	–	0.2	V
SWITCH DRIVER AND REFERENCES (PINS SDI, SDO, EHI AND DPI); UBA1702A ONLY						
I_{EE}	V_{EE} current consumption; excluding PNP interrupter base current	V_{SDO} = 4.2 V	–	−510	–	μA
R_{SDO}	resistance between pins SDO and V_{EE}		–	2.2	–	kΩ
$I_{SDO(max)}$	maximum input current (pin SDO)		7.0	–	–	mA
SWITCH DRIVER AND REFERENCES (PINS SDI, SDO, EHI AND DPI); UBA1702 AND UBA1702A						
I_{SS}	V_{SS} current consumption	V_{SPO} = 4.2 V; note 1	–	−280	–	μA
$V_{SDI-SDO}$	internal voltage limitation between pins SDI and SDO		–	14	–	V
$R_{SDI-SDO}$	resistance between pins SDI and SDO	$V_{SDI} - V_{SDO}$ < 12 V	–	1.1	–	MΩ
R_{SDI}	resistance between pins SDI and V_{EE}	$V_{SDI} = V_{EHI}$ = 48 V; DPI = HIGH	–	4	–	MΩ
		$V_{SDI} = V_{EHI}$ = 240 V; DPI = HIGH	5	20	–	MΩ
R_{EHI}	resistance between pins EHI and V_{EE}	V_{EHI} = 4.2 V	170	420	–	kΩ
		V_{EHI} = 48 V	–	740	–	kΩ
		V_{EHI} = 240 V	–	3.5	–	MΩ
$\lvert Z_{SPO} \rvert$	impedance between pins SPO and V_{EE}	f = 0.3 to 3.4 kHz	20	–	–	kΩ
$\lvert Z_{VSS} \rvert$	impedance between pins V_{SS} and V_{EE}	f = 0.3 to 3.4 kHz	10	–	–	kΩ
V_{IH}	HIGH-level input voltage (pin EHI)		V_{SS} + 1.5	–	240	V
V_{IL}	LOW-level input voltage (pin EHI)		V_{SS}	–	V_{SS} + 0.3	V
I_{IH}	HIGH-level input current (pin EHI)	V_{EHI} = 4.2 V	0	10	20	μA
I_{IL}	LOW-level input current (pin EHI)	V_{EHI} = LOW	–	0	–	μA
V_{IH}	HIGH-level input voltage (pin DPI)		V_{SS} + 1.5	–	V_{DD}	V
V_{IL}	LOW-level input voltage (pin DPI)		V_{SS}	–	V_{SS} + 0.3	V
I_{IH}	HIGH-level input current (pin DPI)	V_{DPI} = HIGH	0	–	10	μA
I_{IL}	LOW-level input current (pin DPI)	V_{DPI} = LOW	–	0	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MUTE SWITCH AND ZENER PROTECTION (PINS MSI, MSA AND ZPA)						
$V_{SPO(M)}$	adjustable mute voltage referenced to V_{EE}	MSI = HIGH; MSA open-circuit	–	2.7	3	V
		MSI = HIGH; MSA shorted to SPO	–	1.7	–	V
$V_{SPO(Z)}$	adjustable zener voltage referenced to V_{EE}	MSI = LOW; ZPA open-circuit	11.0	12.0	13.0	V
		MSI = LOW; ZPA shorted to SPO	8.3	9.0	9.7	V
		MSI = LOW; ZPA shorted to V_{EE}	16.4	18.0	19.6	V
I_{SPI}	current capability (pin SPI)		150	–	–	mA
V_{IH}	HIGH-level input voltage (pin MSI)		$0.7V_{DD}$	–	V_{DD}	V
V_{IL}	LOW-level input voltage (pin MSI)		V_{SS}	–	V_{SS} + 0.3	V
I_{IH}	HIGH-level input current (pin MSI)	V_{MSI} = HIGH	0	–	10	µA
I_{IL}	LOW-level input current (pin MSI)	V_{MSI} = LOW	–	0	–	µA
CURRENT MANAGEMENT (PINS SPI, SPO, CDA, CLA AND CDO)						
$I_{SPI(lim)}$	current limitation (pin SPI)	CLA open-circuit	–	45	–	mA
		CLA shorted to V_{EE}	–	120	–	mA
$I_{SPI(det)}$	current detection (pin SPI)	CDA open-circuit	2	3	4	mA
$R_{SPI-SPO}$	series resistance between pins SPI and SPO		–	2	–	Ω
I_{OH}	HIGH level output current (pin CDO)	$V_{CDO} = V_{DD} - 0.5$ V	–	–	–100	µA
I_{OL}	LOW level output current (pin CDO)	$V_{CDO} = V_{SS} + 0.5$ V	100	–	–	µA
MICROCONTROLLER SUPPLY (PINS V_{DD} AND V_{BB})						
V_{DD}	supply output voltage referenced to V_{SS}	V_{BB} > 3.7 V; I_{DD} = –1 mA	3.0	3.3	3.6	V
$\Delta V_{DD}/\Delta T$	supply output voltage temperature gradient		–	–0.2	–	mV/K
I_{DD}	supply output current capability	V_{BB} > 3.7 V	–	–	–2	mA
$V_{BB}–V_{DD}$	voltage drop between V_{BB} and V_{DD}	I_{DD} = –1 mA; 2.5 V < V_{BB} < 3.0 V	–	100	–	mV
V_{DDM}	voltage at pin V_{DD} when neither speech nor ringer signal is applied	I_{DD} = 9 µA	–	1.4	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ringer part						
PROTECTION (PIN RPI)						
I_{SS}	current consumption	RV2 = 0; RV1 = 0; RV0 = 0	–	–850	–	μA
$I_{RPI(max)}$	maximum input current		70	–	–	mA
V_{RPI}	voltage limit referenced to V_{EE}		–	21	–	V
V_{RPId}	voltage limit in DMO or NSA mode referenced to V_{EE}	I_{RPI} = 30 mA; MSI = HIGH	–	2.1	–	V
$\lvert Z_{RPI} \rvert$	AC input impedance referenced to V_{EE}	f = 0.3 to 3.4 kHz; V_{RPI} < 1.5 V (RMS)	100	220	–	kΩ
RINGER THRESHOLD AND FREQUENCY DETECTION (PINS V_{RR}, RTA AND RFO)						
V_{RRth}	ringer supply threshold voltage referenced to V_{SS}	RTA open-circuit;	–	11	–	V
V_{RRhys}	ringer threshold hysteresis voltage		–	6.5	–	V
V_{RPIhys}	ringer frequency detection hysteresis voltage referenced to V_{EE}	RFO = HIGH	–	V_{RR}	–	V
		RFO = LOW	–	V_{DD}	–	V
I_{OH}	HIGH-level output current (pin RFO)	$V_{RFO} = V_{DD} - 0.5$ V	–	–	–100	μA
I_{OL}	LOW-level output current (pin RFO)	$V_{RFO} = V_{SS} + 0.5$ V	100	–	–	μA
VOLUME CONTROL (PINS RV0, RV1 AND RV2)						
ΔG	gain adjustment range	(RV2, RV1, RV0) from (0, 0, 0) to (1 ,1, 0); note 2	–	36	–	dB
ΔG_s	step resolution	(RV2, RV1, RV0) from (0, 0, 0) to (1, 1, 0); note 2	–	6	–	dB
ΔG_{ls}	last step resolution	(RV2, RV1, RV0) from (1, 1, 0) to (1, 1, 1); note 3	–	9.5	12	dB
V_{IH}	HIGH-level input voltage (pins RVx)		$0.7V_{DD}$	–	V_{DD}	V
V_{IL}	LOW-level input voltage (pins RVx)		V_{SS}	–	$0.3V_{DD}$	V
I_{IH}	HIGH-level input current (pins RVx)	V_{RVx} = HIGH	0	–	5	μA
I_{IL}	LOW-level input current (pins RVx)	V_{RVx} = LOW	0	–	5	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RINGER MELODY INPUT AND PIEZO DRIVER (PINS RMI, ROA AND ROB)						
V_{IH}	HIGH-level input voltage (pin RMI)		$0.52V_{DD}$	–	V_{DD}	V
V_{IL}	LOW-level input voltage (pin RMI)		V_{SS}	–	$0.48V_{DD}$	V
I_{IH}	HIGH-level input current (pin RMI)	V_{RMI} = HIGH	0	–	10	μA
I_{IL}	LOW-level input current (pin RMI)	V_{RMI} = LOW	−10	–	0	μA
$V_{o(min\ p-p)}$	minimum output voltage between pins ROA and ROB (peak-to-peak value)	RV2 = 0; RV1 = 0; RV0 = 0	–	0.15	–	V
$V_{o(p-p)}$	output voltage between pins ROA and ROB (peak-to-peak value)	RV2 = 1; RV1 = 1; RV0 = 0	–	9.6	–	V
$V_{o(max\ p-p)}$	maximum output voltage between pins ROA and ROB (peak-to-peak value)	RV2 = 1; RV1 = 1; RV0 = 1	–	28.7	32	V
$\|I_{RO}\|$	ROA or ROB output current capability	sink and source; RV2 = 1; RV1 = 1; RV0 = 1	80	–	–	mA
REGULATED MICROCONTROLLER SUPPLY (PIN V_{DD})						
V_{DD}	supply output voltage referenced to V_{SS}	I_{DD} = −1 mA	3.0	3.35	3.6	V
$\Delta V_{DD}/\Delta T$	supply output voltage temperature gradient		–	0	–	mV/K
I_{DD}	supply output current capability		–	–	−2	mA

Notes

1. I_{SS} has no influence on AGC characteristics of the TEA106x transmission circuit when V_{SS} is connected to the SLPE pin of TEA106x.
2. Independent of V_{RR} if greater than 10 V.
3. Without piezo transducer, dependent on V_{RR}.

TEST AND APPLICATION INFORMATION

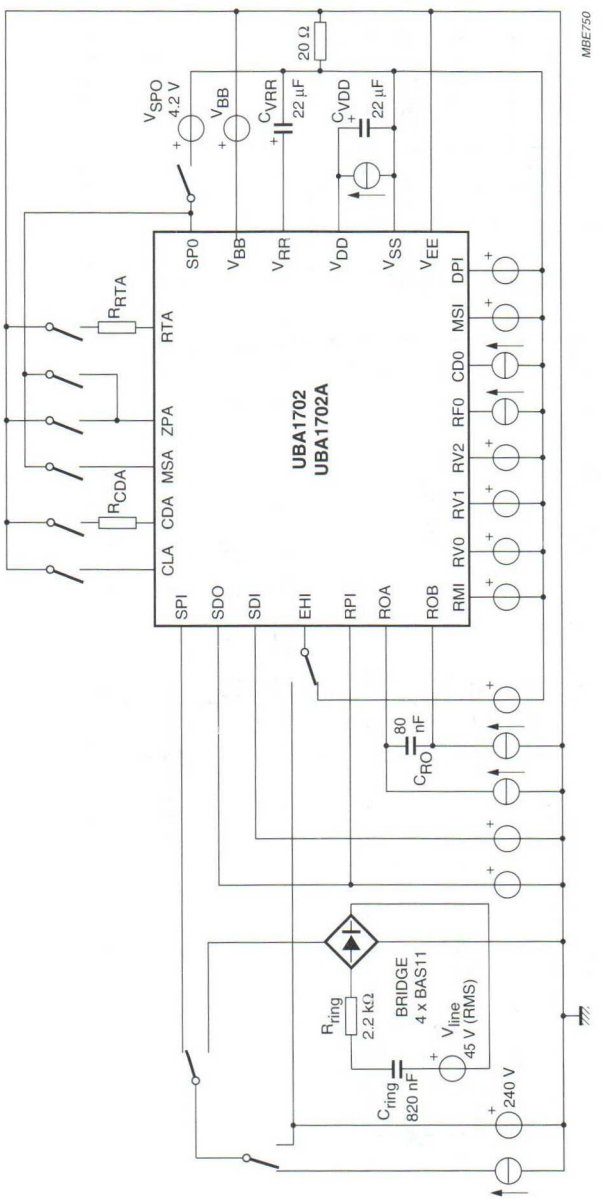


Fig.4 Test circuit.

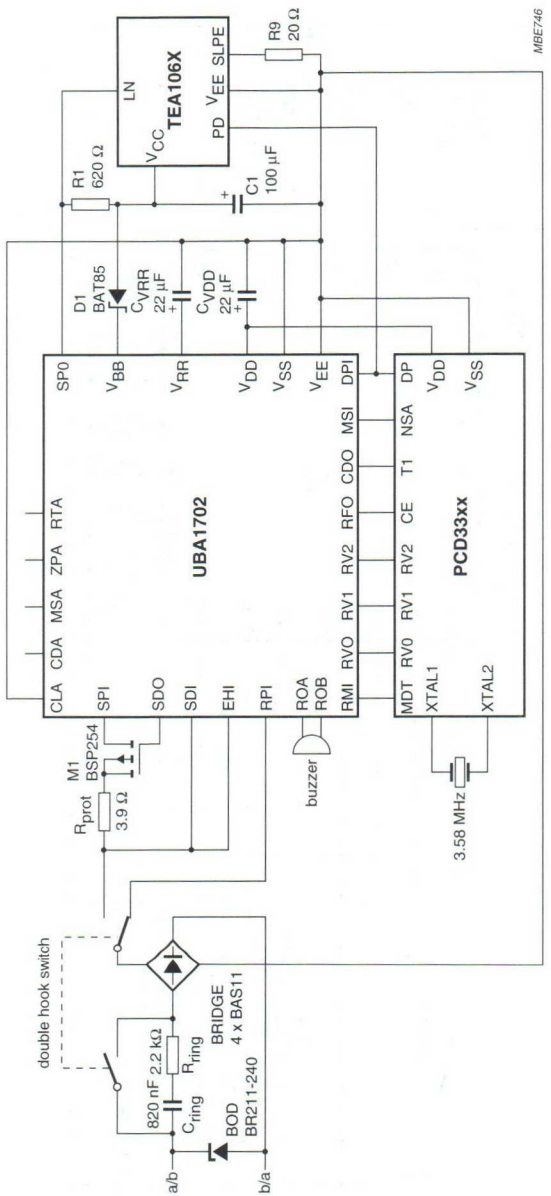


Fig.5 Simplified basic application of the UBA1702 with the TEA106x.

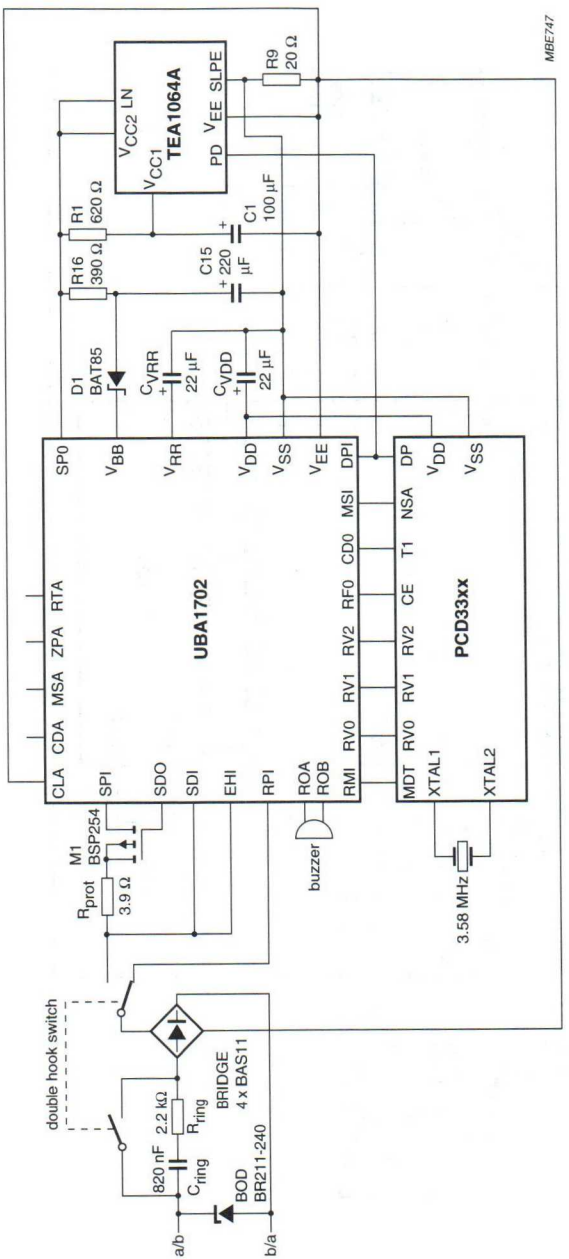


Fig.6 Simplified basic application of the UBA1702 with the TEA1064A.

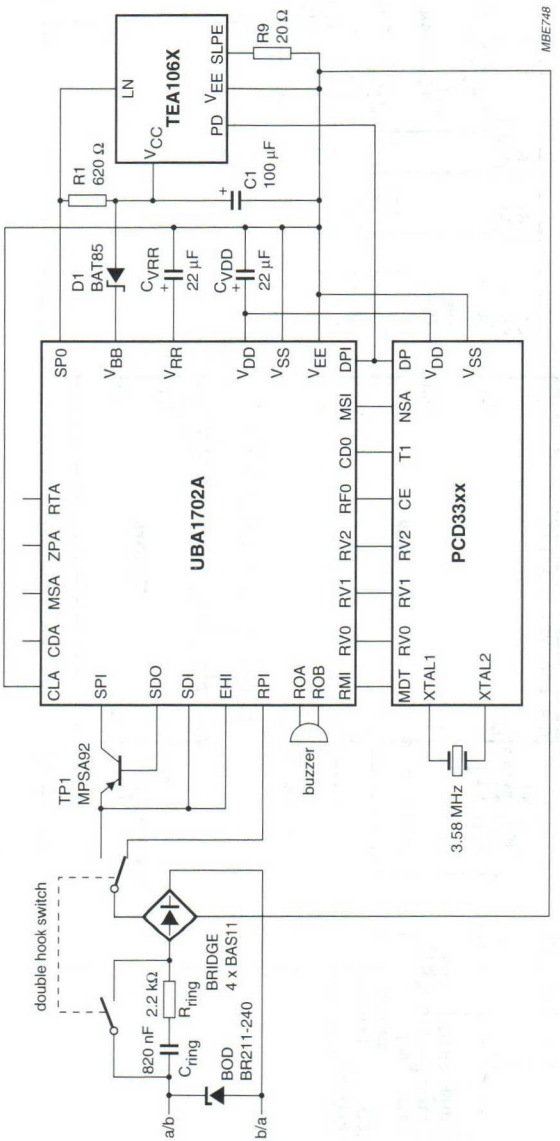


Fig.7 Simplified basic application of the UBA1702A with the TEA106x.

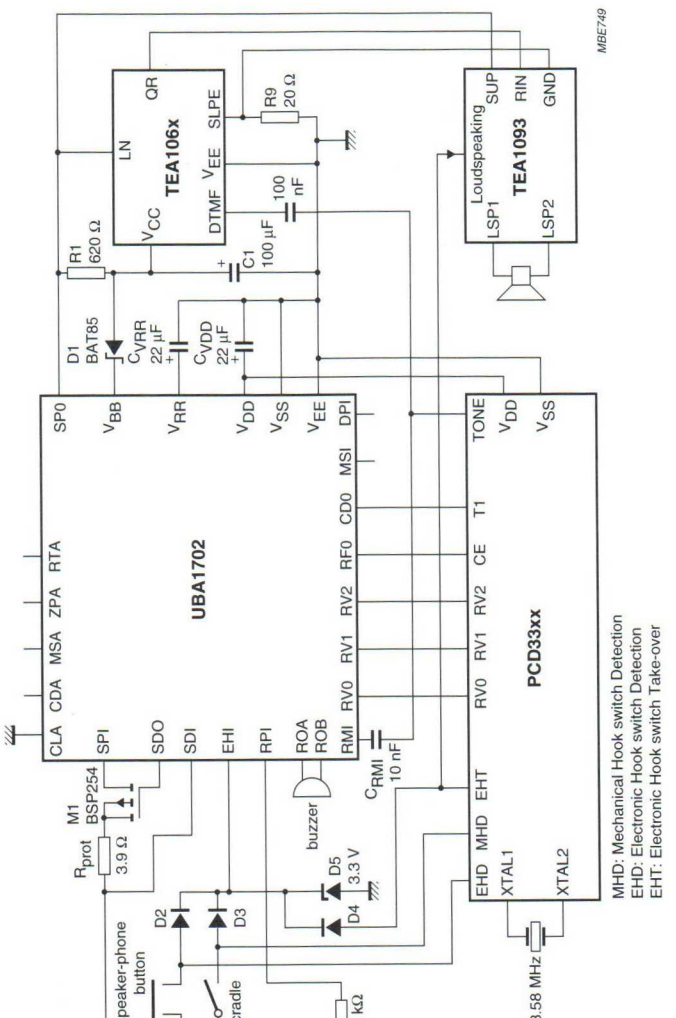


Fig.8 Simplified proposal for electronic hook switch application of the UBA1702 in combination with a transmission and a hands-free circuit.

MICROCONTROLLERS

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1 FEATURES

- Full static 80C51 CPU (8-bit CPU) with a minimum 6 clocks per instruction
- OTP/ROM program memory
- RAM, expandable externally to 64 kbytes (only on certain devices)
- DTMF generator
- MSK modem including Manchester encoder/decoder for analog cordless telephones (standards CT0/CT1/CT1+)
- Pulse Width Modulated output (8-bit resolution)
- EEPROM data memory, accessed internally via I²C-bus interface
- 8-bit ports, I/O lines
- Three 16-bit timer/event counters, including one with capture, compare and PWM function
- Watchdog Timer
- External memory expandable up to 128 kbytes external ROM up to 64 kbytes and/or RAM up to 64 kbytes (only possible on certain devices)
- On-chip amplitude controlled oscillator (ACO) suitable for quartz crystal or ceramic resonator
- 32 kHz Real-Time Clock (RTC) with programmable interrupt periods
- Twenty source, twenty vector interrupt structure with two priority levels
- Full duplex enhanced UART with double buffering
- I²C-bus interface for 2-wire serial transfer, 400 kHz maximum
- Enhanced architecture with:
  - Non-page oriented instructions
  - Direct addressing
  - Four 8 byte RAM register banks
  - Stack depth limited only by available internal RAM (maximum 256 bytes)
  - Multiply, divide, subtract and compare instructions
- Eight additional interrupts on Port 1
  - Edge or level sensitive triggering selectable via software
  - Power-saving use for keyboard control.
- Improved Power-on/Power-off reset circuitry (POR) with 9 hardware programmable levels
- Low Voltage Detection (LVD) with 11 software programmable levels
- Wake-up from Power-down mode via external interrupts at Port 1, via RTC or via LVD
- Very low current consumption.

2 GENERAL DESCRIPTION

The TELX microcontroller family is manufactured in an advanced CMOS technology and is based on MCM (Multi-Chip-Module) technology as the non-volatile memory parts OTP and EEPROM are integrated on a separate chip.

The TELX family are 8-bit microcontrollers especially suited for analog cordless telephones (CT0, CT1, CT1+ standards), mid/high-end corded telephones and pagers. For this purpose, features like DTMF, EEPROM, MSK modem, PWM, POR/LVD, ACO and RTC are integrated on-chip. The device is optimized for low power consumption. The TELX family has two software selectable features for power reduction: Idle and Power-down modes.

The instruction set of the TELX family is based on that of the 8051. The TELX family also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

This data sheet details the shared properties of the TELX family. For a particular microcontroller, read this data sheet in conjunction with the individual data sheet of the specific device. For details on the I²C-bus functions see *"Data Handbook IC12"*.

3 BLOCK DIAGRAM

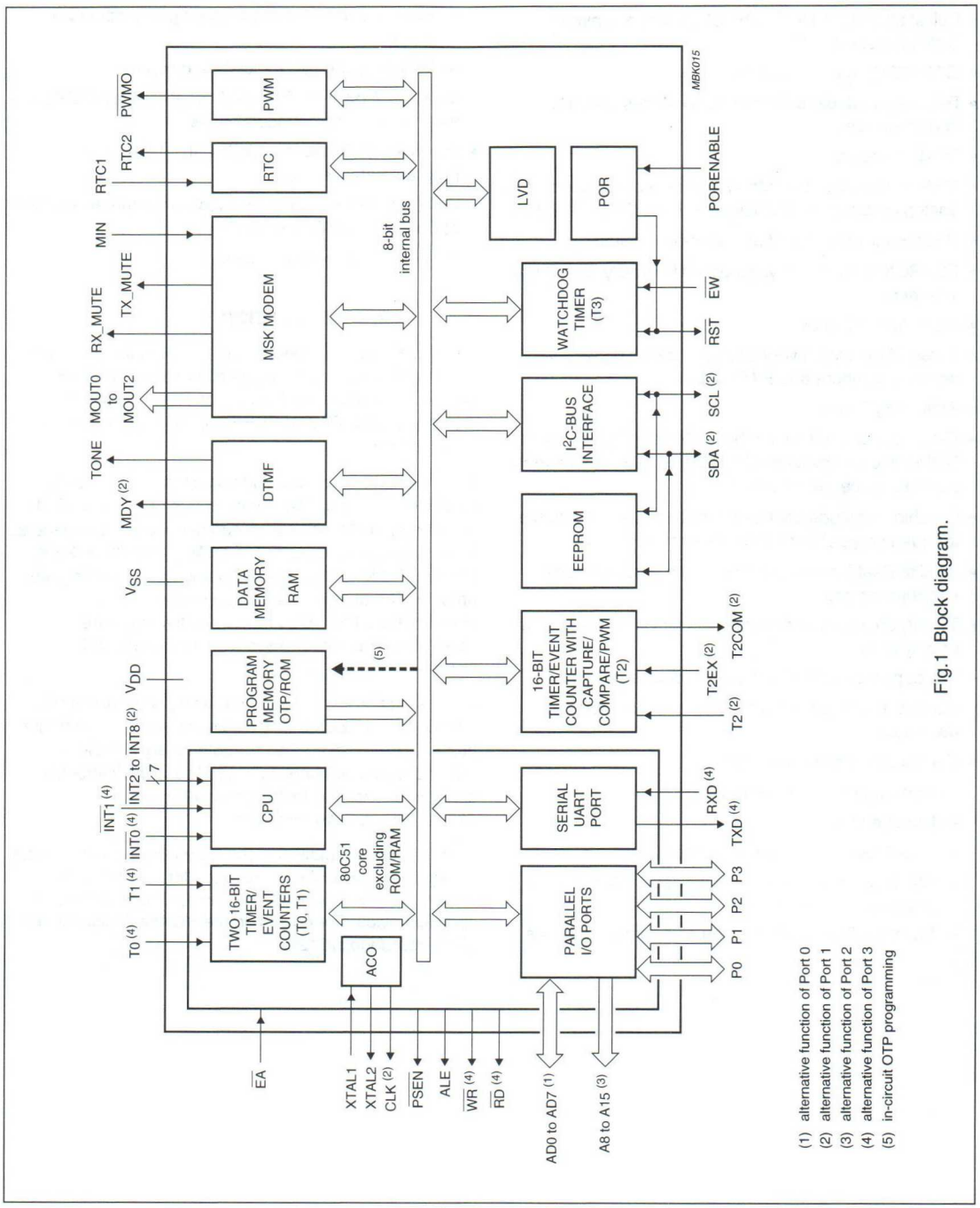


Fig.1 Block diagram.

(1) alternative function of Port 0
(2) alternative function of Port 1
(3) alternative function of Port 2
(4) alternative function of Port 3
(5) in-circuit OTP programming

4 FUNCTIONAL DESCRIPTION

4.1 General

The TELX family provides stand-alone high-performance CMOS microcontrollers designed for use in mid/high-end corded telephones, analog cordless telephones (CT0, CT1, CT1+ standards) and pagers. For this purpose, features such as DTMF, MSK modem, EEPROM, Real-Time-Clock and PWM have been integrated on-chip. The devices provide hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 kbytes of program memory and/or up to 64 kbytes of data storage.

The TELX family contains ROM or OTP program memory; a static read/write data memory; I/O lines; three 16-bit timer/event counters; a twenty-source two priority-level, nested interrupt structure and on-chip oscillator and timing circuit.

The TELX devices have two software selectable modes of reduced activity for power reduction: Idle and Power-down. The Idle mode freezes the CPU while allowing the RAM, timers, serial I/O and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

Two serial interfaces are provided on-chip; a standard UART serial interface and an I²C-bus serial interface. The I²C-bus serial interface has byte orientated master and slave functions allowing communication with the whole family of I²C-bus compatible devices.

4.2 CPU timing

A machine cycle consists of a sequence of 6 states. Each state lasts for one oscillator period, thus a machine cycle takes 6 oscillator periods or e.g. 1.68 µs if the oscillator frequency is 3.58 MHz. This means that the TELX family is twice as fast as a standard 80C51 based on the same oscillator frequency.

4.3 Clocking concept with prescaler PSC

The clocking concept of the TELX family is shown in Fig.2. The on-chip oscillator directly clocks the CPU (including timers T0 and T1), timer T2, PWM, the Watchdog Timer and the Analog-to-Digital Converter (ADC).

The DTMF block requires an input frequency of 3.58 MHz for correct operation. For this purpose a prescaler (PSC) has been included to enable multiples of 3.58 MHz to be used as the oscillator frequency. The blocks I²C-bus, UART special purpose baud rate generator, MSK modem, Watchdog Timer and EEPROM are also clocked via the PSC prescaler to minimize the number of prescalers on-chip and thereby reducing the power consumption. The division factors 1:1 through to 1:8 of the PSC prescaler are software programmable via the PRESC register, see Tables 2 and 3. The PSC division factor should only be set in the initialization routine directly after start-up. The prescaler and the special baud rate timer for the UART are described in Section 4.13.

In order to minimize power consumption, the individual blocks automatically switch-off their clock (gated clock) when they are not enabled.

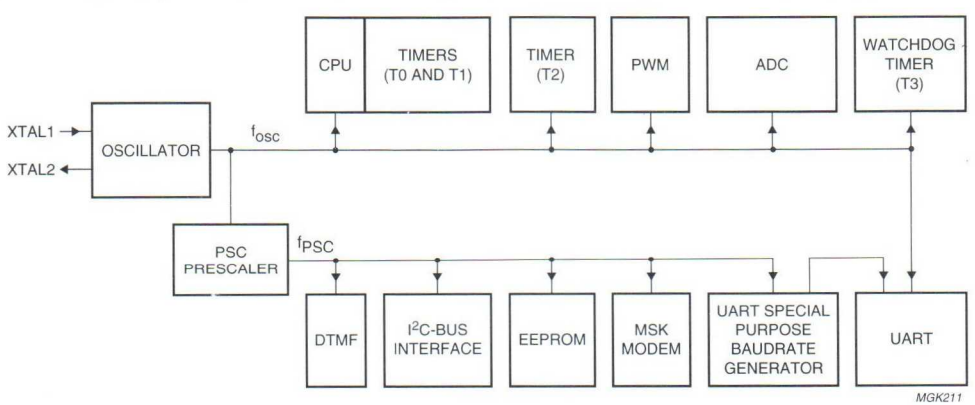


Fig.2 Clocking concept.

4.3.1 PRESCALER REGISTER (PRESC)

Table 1 Prescaler Register (SFR address F3H)

7	6	5	4	3	2	1	0
–	PTWO2	PTWO1	PTWO0	P3	PS2	PS1	PS0

Table 2 Description of PRESC bits

BIT	SYMBOL	DESCRIPTION
PRESC.7	–	This bit will always read a logic 0.
PRESC.6	PTWO2	These 3-bits specify the power of two in the division factor of the UART baud rate timer; see Section 4.13.3.1.
PRESC.5	PTWO1	
PRESC.4	PTWO0	
PRESC.3	P3	This bit specifies the power of three in the division factor of the UART baud rate timer; see Section 4.13.3.1.
PRESC.2	PS2	These 3-bits select the PSC division factor; see Table 3.
PRESC.1	PS1	
PRESC.0	PS0	

Table 3 Selection of PSC division factors

PS2	PS1	PS0	DIVISION RATIO (f_{PSC} : f_{osc})
0	0	0	1:1
0	0	1	1:2
0	1	0	1:3
0	1	1	1:4
1	0	0	1:5
1	0	1	1:6
1	1	0	1:7
1	1	1	1:8

4.4 32 kHz Real-Time Clock

The Real-Time Clock (RTC) consists of a 32 kHz crystal oscillator, a 32 kHz to 1 second or 1 minute divider chain, an 8-bit Frequency Adjustment Register (FAR) and the Clock Control Register (CLCR). The complete RTC section works independent of the microcontroller status, even in Idle and Power-down mode.

The RTC can generate an interrupt periodically every 1 minute or every 1, 2 or 4 seconds. This interrupt can be used to wake-up the microcontroller from the Power-down mode without resetting it. This feature is especially useful in CT0/CT1 cordless phone applications to wake-up the microcontroller periodically to perform channel scanning.

The internal 32 kHz oscillator requires an external quartz crystal with a frequency of 32.768 kHz (a positive deviation up to +200 ppm is allowed) and an external feedback resistor connected between pins RTC1 and RTC2; 4.7 MΩ is recommended.

The oscillator is controlled by the RUN bit in the Clock Control Register.

The divider chain operates with the 32 kHz oscillator output and divides this signal down to two clocks with a period of 1, 2 or 4 seconds or 1 minute respectively. Depending on the state of the ITS1 and ITS0 bits in the Clock Control Register, the falling edge of the seconds or minutes clock is used to set the Clock Interrupt Flag (CIF) in the Clock Control Register.

Additionally, the divider chain generates a 16 kHz clock (RTCLK) that can be routed through the port line P1.3/RTCLK, controlled by the ERCO bit in the Clock Control Register.

Frequency adjustment is used to extend the interrupt time by defining the number of 16 kHz clocks in the Frequency Adjustment Register (FAR) that will be counted twice within the first second period after a minute interrupt.

4.4.1 Clock Control Register (CLCR)

Table 4 Clock Control Register (address ACH; access type R/W)

7	6	5	4	3	2	1	0
TST2	TST1	ERC0	RUN	CIF	–	ITS1	ITS0

Table 5 Description of CLCR bits

BIT	SYMBOL	DESCRIPTION
7	TST2	**Test 2 input.** This is a testing bit and must be fixed at a logic 0 by user software.
6	TST1	**Test 1 input.** This is a testing bit and must be fixed at a logic 0 by user software.
5	ERCO	**Enable 16 kHz Clock Output.** If ERCO = 0, then P1.3/RTCLK is a port line. If ERCO = 1, then P1.3/RTCLK is a 16 kHz clock output. ERCO = 1 does not inhibit the port instructions for P1.3/RTCLK. Therefore, the state of both port line and flip-flop may be read in and the port flip-flop may be written by derivative port instructions. However, the port flip-flop of P1.3/RTCLK must remain set to avoid conflicts between the 16 kHz clock and port outputs.
4	RUN	**Clock Run/Stop.** If RUN = 0, then the oscillator is stopped and the clock is reset. If RUN = 1, then the oscillator and the clock are both running.
3	CIF	**Clock Interrupt Flag.** Set by hardware, if RTC divider chain overflows (period depending on the state the ITS1 and ITS0 bits) or by software. Reset by software.
2	–	Not used.
1	ITS1	**Interrupt Time Select bits.** The state of ITS1 and ITS0 determine the interrupt period, see Table 6.
0	ITS0	

Table 6 Selection of the RTC Interrupt period

ITS1	ITS0	INTERRUPT PERIOD
0	0	1 second; note 1
0	1	2 seconds
1	0	4 seconds
1	1	1 minute

Note

1. If the 1 second interrupt is used, every 60th interval may be up to 15.3 ms longer than the others as a result of the frequency adjustment. The adjusted Minute Interrupt Time (MIT) shows now a maximum deviation of 0.5 ppm.

4.4.2 FREQUENCY ADJUSTMENT REGISTER (FAR)

The frequency adjustment value of the RTC section is defined by the 8-bit Frequency Adjustment Register. The register access type is R/W. The significance of the individual bits of the FAR register can be illustrated by the following equation:

$$\text{Minute interrupt time (MIT)} = 60 \times 2^{\frac{14}{f_{RTCLK}}} + \frac{FAR}{2^{14}}$$

where f_{RTCLK} = RTC frequency and FAR represents the decimal value of the contents of the Frequency Adjustment Register.

Table 7 Frequency Adjustment Register (address ADH)

7	6	5	4	3	2	1	0
FAR7	FAR6	FAR5	FAR4	FAR3	FAR2	FAR1	FAR0

Table 8 Description of FAR bits

BIT	SYMBOL	DESCRIPTION
7	FAR7	The state of these 8-bits determine the frequency adjustment value for the Real-Time Clock; see Table 9.
6	FAR6	
5	FAR5	
4	FAR4	
3	FAR3	
2	FAR2	
1	FAR1	
0	FAR0	

Table 9 Selection of FAR value based on f_{RTCLK}

FAR (HEX)	f_{RTCLK}
00	16384.000
01	16384.018
02	16384.033
03	16384.051
04	16384.066
05	16384.084
06	16384.100
07	16384.117
08	16384.135
09	16384.150
0A	16384.168
0B	16384.184
0C	16384.201
0D	16384.217
0E	16384.234
0F	16384.250
10	16384.268
11	16384.283
12	16384.301
13	16384.316
14	16384.334
15	16384.350
16	16384.367
17	16384.385
18	16384.400
19	16384.418
1A	16384.434
1B	16384.451
1C	16384.467
1D	16384.484
1E	16384.500
1F	16384.518
20	16384.533

FAR (HEX)	f_{RTCLK}
21	16384.551
22	16384.566
23	16384.584
24	16384.600
25	16384.617
26	16384.635
27	16384.650
28	16384.668
29	16384.684
2A	16384.701
2B	16384.717
2C	16384.734
2D	16384.750
2E	16384.768
2F	16384.783
30	16384.801
31	16384.816
32	16384.834
33	16384.850
34	16384.867
35	16384.885
36	16384.900
37	16384.918
38	16384.934
39	16384.951
3A	16384.967
3B	16384.984
3C	16385.000
3D	16385.018
3E	16385.033
3F	16385.051
40	16385.066
41	16385.084

FAR (HEX)	f_{RTCLK}
42	16385.100
43	16385.117
44	16385.135
45	16385.150
46	16385.168
47	16385.184
48	16385.201
49	16385.217
4A	16385.234
4B	16385.250
4C	16385.268
4D	16385.283
4E	16385.301
4F	16385.316
50	16385.334
51	16385.350
52	16385.367
53	16385.385
54	16385.400
55	16385.418
56	16385.434
57	16385.451
58	16385.467
59	16385.484
5A	16385.500
5B	16385.518
5C	16385.533
5D	16385.551
5E	16385.566
5F	16385.584
60	16385.600
61	16385.617
62	16385.635
63	16385.650

FAR (HEX)	f_{RTCLK}
64	16385.668
65	16385.684
66	16385.701
67	16385.717
68	16385.734
69	16385.750
6A	16385.768
6B	16385.783
6C	16385.801
6D	16385.816
6E	16385.834
6F	16385.850
70	16385.867
71	16385.885
72	16385.900
73	16385.918
74	16385.934
75	16385.951
76	16385.967
77	16385.984
78	16386.000
79	16386.018
7A	16386.033
7B	16386.051
7C	16386.066
7D	16386.084
7E	16386.100
7F	16386.117
80	16386.135
81	16386.150
82	16386.168
83	16386.184
84	16386.201
85	16386.217

FAR (HEX)	f_{RTCLK}
86	16386.234
87	16386.250
88	16386.268
89	16386.283
8A	16386.301
8B	16386.316
8C	16386.334
8D	16386.350
8E	16386.367
8F	16386.385
90	16386.400
91	16386.418
92	16386.434
93	16386.451
94	16386.467
95	16386.484
96	16386.500
97	16386.518
98	16386.533
99	16386.551
9A	16386.566
9B	16386.584
9C	16386.600
9D	16386.617
9E	16386.635
9F	16386.650
A0	16386.668
A1	16386.684
A2	16386.701
A3	16386.717
A4	16386.734
A5	16386.750
A6	16386.768
A7	16386.783

FAR (HEX)	f_{RTCLK}
A8	16386.801
A9	16386.816
AA	16386.834
AB	16386.850
AC	16386.867
AD	16386.885
AE	16386.900
AF	16386.918
B0	16386.934
B1	16386.951
B2	16386.967
B3	16386.984
B4	16387.000
B5	16387.018
B6	16387.033
B7	16387.051
B8	16387.066
B9	16387.084
BA	16387.100
BB	16387.117
BC	16387.135
BD	16387.150
BE	16387.168
BF	16387.184
C0	16387.201
C1	16387.217
C2	16387.234
C3	16387.250
C4	16387.268
C5	16387.283
C6	16387.301
C7	16387.316
C8	16387.334
C9	16387.350

FAR (HEX)	f_{RTCLK}
CA	16387.367
CB	16387.385
CC	16387.400
CD	16387.418
CE	16387.434
CF	16387.451
D0	16387.467
D1	16387.484
D2	16387.500
D3	16387.518
D4	16387.533
D5	16387.551
D6	16387.566
D7	16387.584
D8	16387.600
D9	16387.617
DA	16387.635
DB	16387.650
DC	16387.668
DD	16387.684
DE	16387.701
DF	16387.717
E0	16387.734
E1	16387.750
E2	16387.768
E3	16387.783
E4	16387.801

FAR (HEX)	f_{RTCLK}
E5	16387.816
E6	16387.834
E7	16387.850
E8	16387.867
E9	16387.885
EA	16387.900
EB	16387.918
EC	16387.934
ED	16387.951
EE	16387.967
EF	16387.984
F0	16388.002
F1	16388.018
F2	16388.035
F3	16388.051
F4	16388.068
F5	16388.084
F6	16388.102
F7	16388.117
F8	16388.135
F9	16388.152
FA	16388.168
FB	16388.186
FC	16388.201
FD	16388.219
FE	16388.234
FF	16384.000

4.5 Memory organization

The TELX family has Program Memory (OTP or ROM) plus Data Memory (RAM) on-chip. The device has separate address spaces for Program and Data Memory as shown in Fig.3. On devices with ports P0 and P2 available, up to 64 kbytes of external memory can be addressed. In this case, the CPU generates both read ($\overline{RD}$) and write ($\overline{WR}$) signals for external Data Memory accesses, and the read strobe ($\overline{PSEN}$) for external Program Memory.

4.5.1 Program memory

After reset the CPU begins execution at location 0000H of the Program Memory. The Program Memory can be implemented in either internal OTP/ROM or external memory. If the $\overline{EA}$ pin is tied to V_{DD}, then program memory fetches are directed to the internal program memory. If the $\overline{EA}$ pin is tied to V_{SS} and if the security bits are not set, then program memory fetches are directed to external memory.

4.5.2 Data memory

The data memory organisation of the TELX family is exactly the same as for the P8xCE558. The TELX family contains a maximum of 512 bytes internal RAM (consisting of 256 bytes standard RAM and 256 bytes AUX-RAM) and Special Function Registers (SFRs). Figure 3 shows the internal Data Memory space divided into the lower 128 bytes, the upper 128 bytes, the SFR space and 256 bytes Auxiliary RAM. Internal RAM locations 0 to 127 are directly and indirectly addressable. Internal RAM locations 128 to 255 are only indirectly addressable. The SFRs locations 128 to 255 bytes are only directly addressable and the Auxiliary RAM is indirectly addressable as external RAM (MOVX) unless it is disabled by setting ARD = 1.

4.5.3 Special Function Registers

The second 128 bytes are the address locations of the SFRs. Figure 4 and Table 10 define the SFRs memory space. The SFRs include the port latches, timers, peripheral control, serial I/O registers, etc. These registers can only be accessed by direct addressing. There are 128 addressable locations in the SFR address space (those SFRs whose addresses are divisible by eight). Refer to the product specifications for the precise list of the SFRs implemented and their value directly after reset.

4.6 Addressing

The TELX family has five methods for addressing source operands:

- Register
- Direct
- Register-Indirect
- Immediate
- Base-Register plus Index-Register-Indirect.

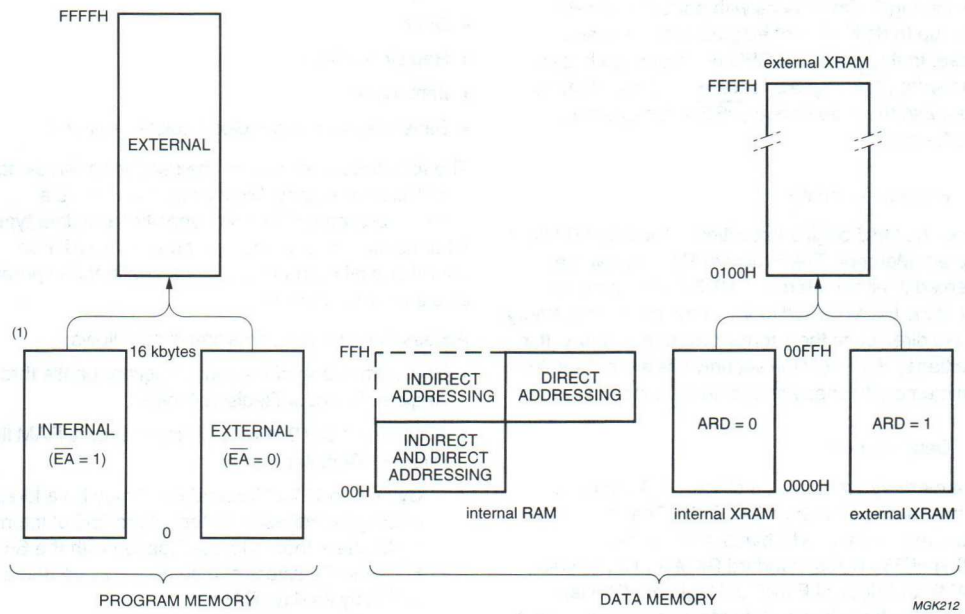
The first three methods can be used for addressing destination operands. Most instructions have a 'destination/source' field that specifies the data type, addressing methods and operands involved. For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four 8-register banks through Register Direct or Register-Indirect
- A maximum of 1 024 bytes of internal data RAM through Direct or Register-Indirect
  - Bytes 0 to 127 of internal RAM may be addressed directly or indirectly. Bytes 128 to 255 of internal RAM share their address location with the Special Function Registers and so may only be addressed indirectly as data RAM
  - Bytes 0 to 256 of AUX-RAM can only be addressed indirectly via MOVX instructions.
- Special Function Registers through Direct
- External data memory through Register-Indirect
- Program memory look-up tables through Base-Register plus Index-Register-Indirect.

The members of the TELX family are classified as 8-bit devices since their internal ROM, RAM, Special Function Registers, Arithmetic Logic Unit and external data bus are all 8-bits wide. All perform operations on bit, nibble, byte and double-byte data types.

Facilities are available for byte transfer, logic and integer arithmetic operations. Data transfer, logic and conditional branch operations can be performed directly on Boolean variables to provide excellent bit handling.



(1) The upper limit is device dependent.

Fig.3 Memory map.

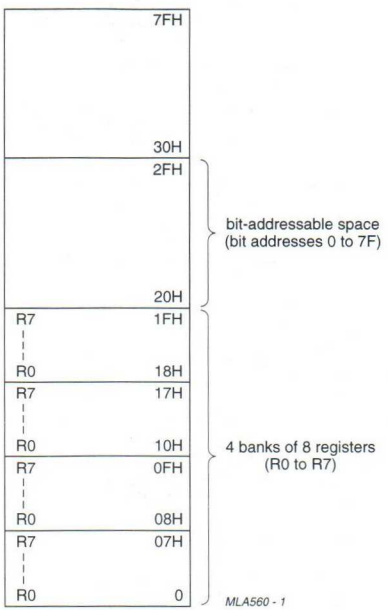


Fig.4 The lower 128 bytes of internal RAM.

Table 10 Special Function Register memory map (bit addressing)

REGISTER MNEMONIC	START ADDRESS	REGISTER BIT								END ADDRESS
		0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
IP1	F8H	PX2	PX3	PX4	PX5	PX6	PX7	PX8	PX9	FFH
B	F0H	B0	B1	B2	B3	B4	B5	B6	B7	F7H
IEN1	E8H	EX2	EX3	EX4	EX5	EX6	EX7	EX8	EX9	EFH
ACC	E0H	ACC0	ACC1	ACC2	ACC3	ACC4	ACC5	ACC6	ACC7	E7H
S1CON	D8H	CR0	CR1	AA	SI	STO	STA	ENS1	CR2	DFH
PSW	D0H	P	–	0V	RS0	RS1	F0	AC	CY	D7H
T2CON	C8H	CP/$\overline{RL2}$	C/$\overline{T2}$	TR2	EXEN2	ECOMP	COMP	EXF2	TF2	CFH
IRQ1	C0H	IQ2	IQ3	IQ4	IQ5	IQ6	IQ7	IQ8	IQ9	C7H
IP0	B8H	PX0	PT0	PX1	PT1	PS0	PS1	PT2	–	BFH
P3	B0H	P30	P31	P32	P33	P34	P35	P36	P37	B7H
IEN0	A8H	EX0	ET0	EX1	ET1	ES0R	ES1	ET2	EA	AFH
P2	A0H	P20	P21	P22	P23	P24	P25	P26	P27	A7H
S0CON	98H	RI	TI	RB8	TB8	REN	SM2	SM1	SM0	9FH
P1	90H	P10	P11	P12	P13	P14	P15	P16	P17	97H
TCON	88H	IT0	IE0	IT1	IE1	TR0	TF0	TR0	TF1	8FH
P0	80H	P00	P01	P02	P03	P04	P05	P06	P07	87H

4.7 I/O facilities

4.7.1 PORTS

The TELX family has 32 I/O lines treated as 32 individually addressable bits or as four parallel 8-bit addressable ports. Ports 0 to 3 perform the following alternative functions.

Port 0 Provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals.

Port 1 Used for a number of special functions:

- Provides the inputs for the external interrupts INT2 to INT9
- External inputs of Timer 2
- External activation and compare output of Timer 2
- Real-Time Clock output (16 kHz)
- DTMF melody output
- CLK/P1.4 for the clock output
- SCL/P1.6 and SDA/P1.7 for the I^2C-bus interface are open-drain outputs.

Port 2 Provides the high-order address bus when expanding the device with external program memory and/or external data memory.

Port 3 Pins can be configured individually to provide:

- Serial port receiver input and transmitter output (UART)
- External interrupt request inputs
- Counter inputs
- Control signals to read and write to external memories.

To enable a port pin alternative function, the port bit latch in its SFR must contain a logic 1.

Each port consists of a latch (SFRs P0 to P3), an output driver and input buffer. All ports have internal pull-ups. Figure 5(a) shows that the strong transistor p1 is turned on for only 1 oscillator period after a LOW-to-HIGH transition in the port latch. When on, it turns on p3 (a weak pull-up) through the inverter IN1. This inverter and p3 form a latch which holds the logic 1.

The Alternative Port Function Register (ALTP) is described in Section 4.10.4.

4.7.2 PORT I/O CONFIGURATION

I/O port output configurations are determined by the settings in the port configuration SFRs. Each port has two associated SFRs: PnCFGA and PnCFGB, where 'n' indicates the specific port number (0 to 3). One bit in each of the 2 SFRs relates to the output setting for the corresponding port pin, allowing any combination of the 2 output types to be mixed on those port pins. For example, the output type of Port 1 pin 3 is controlled by setting bit 3 in the SFRs P1CFGA and P1CFGB.

The port pins may be individually configured with one of the following modes (P1.6 and P1.7 can be open-drain or high-impedance but never have any diodes against V_{DD}).

Mode 0 Open-drain; quasi-bidirectional I/O with n-channel open-drain output. Use as an output (e.g. Port 0 for external memory accesses ($\overline{EA}$ = 0) or access above the built-in memory boundary) requires the connection of an external pull-up resistor. The ESD protection diodes against V_{DD} and V_{SS} are still present. Except for the I^2C-bus port (P1.6 and P1.7), ports which are configured as open-drain still have a protection diode to V_{DD}. See Fig.5(a).

Mode 1 Standard Port; quasi-bidirectional I/O with pull-up. The strong pull-up p1 is turned on for only two oscillator periods after a LOW-to-HIGH transition in the port latch. After these two oscillator periods the port is only weakly driven through p2 and 'very weakly' driven through p3. See Fig.5(b).

Mode 2 High-impedance; this mode turns all port output drivers off. Thus, the pin will not source or sink current and may be used as an input-only pin with no internal drivers for an external device to overcome. See Fig.5(c).

Mode 3 Push-pull; output with drive capability in both polarities. In this mode, pins can only be used as outputs. See Fig.5(d).

Tables 11 and 12 show the configuration register settings for the four output configurations.

The electrical characteristics of each output type may be found in the DC characteristics in the specific product data sheet.

The default port configuration after reset is also given in the specific product data sheet.

Table 11 Selection of the port output configuration

MODE	PnCFGA	PnCFGB	PORT OUTPUT CONFIGURATION	
			NORMAL PORTS	I²C-BUS PORTS (P1.6 AND P1.7)
0	0	0	open-drain	open-drain (port data and I²C-bus output)
1	1	0	quasi-bidirectional	open-drain (port data only)
2	0	1	high-impedance	high-impedance
3	1	1	push-pull	open-drain (port data only)

Note

1. If P1CFGA.7 is set the I²C-bus interfaces of the microcontroller and other on-chip blocks with an I²C-bus interface (e.g. EEPROM) are connected internally. This means that the microcontroller can access these blocks via the I²C-bus without using P1.6 and P1.7.

Table 12 Special Function Registers for port configurations; note 1

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS (HEX)	STATE AFTER RESET
Port P0 Configuration A Register	P0CFGA	8E	depending on product, refer to product specification
Port P0 Configuration B Register	P0CFGB	8F	
Port P0 output data Register	P0	80	
Port P1 Configuration A Register	P1CFGA	9E	
Port P1 Configuration B Register	P1CFGB	9F	
Port P1 output data Register	P1	90	
Port P2 Configuration A Register	P2CFGA	AE	
Port P2 Configuration B Register	P2CFGB	AF	
Port P2 output data Register	P2	A0	
Port P3 Configuration A Register	P3CFGA	BE	
Port P3 Configuration B Register	P3CFGB	BF	
Port P3 output data Register	P3	B0	

Note

1. Mode changes may cause glitches to occur during transitions. When modifying both registers, WRITE instructions should be carried out consecutively.

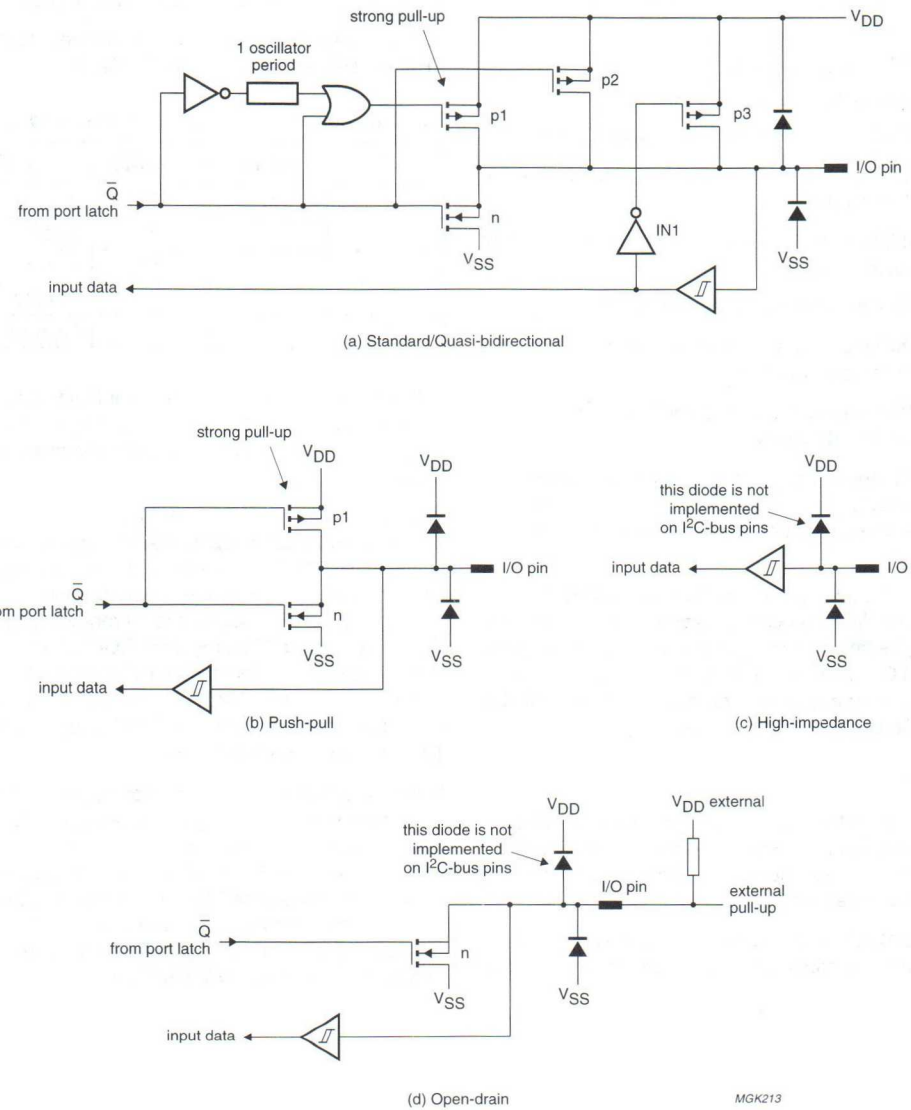


Fig.5 Port configuration options.

4.8 Timer/event counters

The TELX family contains three 16-bit timer/event counters: Timer 0, Timer 1 and Timer 2 which perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests
- Generate output on comparator match
- Generate a pulse width modulated output signal.

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler

Mode 1 16-bit time-interval or event counter

Mode 2 8-bit time-interval or event counter with automatic reload upon overflow

Mode 3 Timer 0 establishes TL0 and TH0 as two separate counters.

In the timer mode the register is incremented every machine cycle. Since a machine cycle consists of a minimum of 6 oscillator periods, the maximum count rate is $1/6 \times f_{osc}$.

In the counter mode, the register is incremented in response to a HIGH-to-LOW transition. Since it takes one machine cycle (minimum 6 oscillator periods) to recognize a HIGH-to-LOW transition, the maximum count rate is $1/6 \times f_{osc}$. To ensure a given level is sampled, it should be held for at least one complete machine cycle.

4.8.1 Timer T2

Note that the function of Timer 2 may deviate from the following description for certain products in the TELX family. In such a case, the deviation is described in the specific product data sheet.

Timer 2 is a 16-bit timer/counter that can operate as a timer, as an event counter or as a pulse width modulator.

The following operating modes are available: External interrupt, T2-only, Auto-Reload and Capture mode.
If Timer 2 is in the OFF state, its clock is switched off and the timer has an extremely low power consumption.
Parallel to these operating modes, a Compare function and/or a pulse generator function is provided.

The operating modes are selected via the T2CON bits TR2, CP/$\overline{RL2}$ and EXEN2 (see Table 13).

Table 13 Selection of Timer 2 operating modes

TR2	EXEN2	CP/$\overline{RL2}$	MODE
0	0	X	OFF
0	1	X	External interrupt
1	X	0	Auto-reload
1	0	1	T2-only
1	1	1	Capture

In the T2-only mode, TH2 and TL2 function as a 16-bit timer or counter which upon overflowing sets the Timer 2 overflow bit TF2. This may then be used to generate an interrupt.

In the Capture mode, TH2 and TL2 function as a 16-bit timer or counter which upon overflowing sets the Timer 2 overflow bit TF2. This may then be used to generate an interrupt. Additionally a HIGH-to-LOW transition at external input T2EX causes the current value in TL2 and TH2 to be captured into registers RCAP2L and RCAP2H respectively. In addition, the transition at T2EX causes the EXF2 interrupt flag in T2CON to be set, this may also be used to generate an interrupt. The Capture mode and the T2-only mode are shown in Fig.6.

In the Auto-Reload mode the 16-bit counter (TH2, TL2) does not continue counting at the value 0000H, after an overflow occurred, but will be reloaded with the 16-bit value stored in the SFRs RCAP2H and RCAP2L. If in Auto-Reload mode, the EXEN2 bit is set, a HIGH-to-LOW transition at external input T2EX will set the EXF2 bit and will also trigger the reloading of TH2,TL2. The Auto-Reload mode is shown in Fig.7.

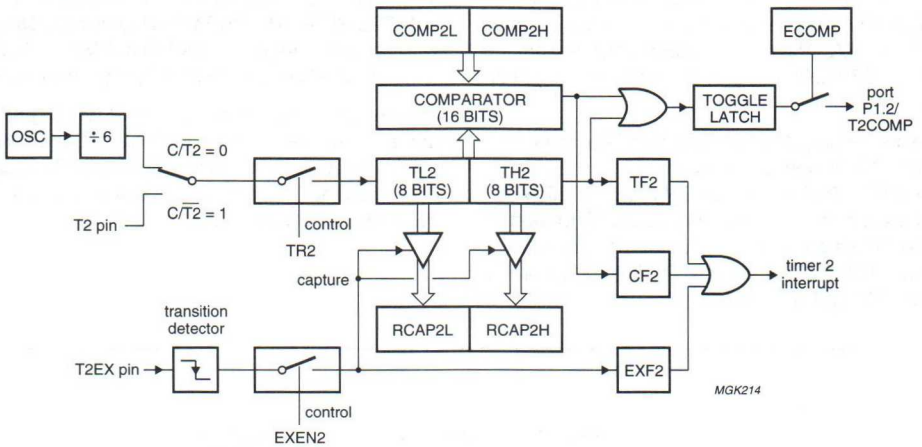


Fig.6 Timer 2 in T2-only and/or Capture mode.

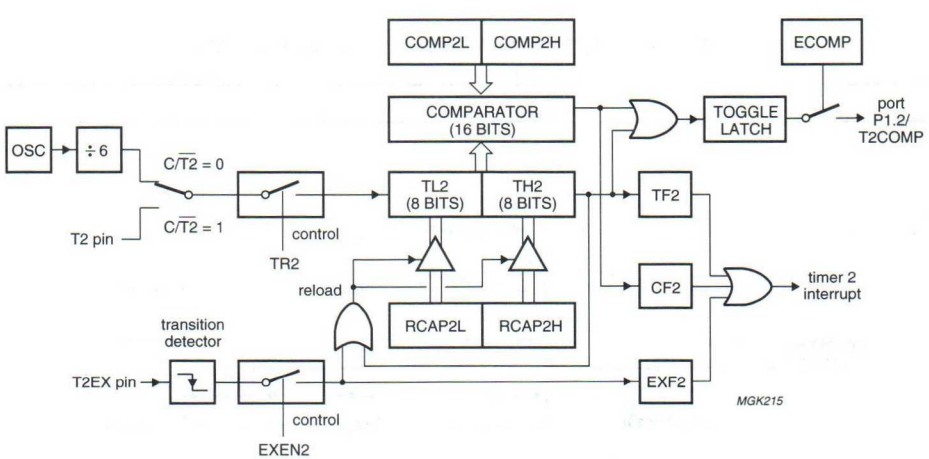


Fig.7 Timer 2 in Auto-Reload mode.

Parallel to the T2-only, Capture and Auto-Reload mode, a compare function can be activated by writing a value other than 0000H to the compare SFRs COMP2H and COMP2L. A compare match is generated when the timer register TL2/TH2 increments to the value of the compare register COMP2L/COM2H. A compare match will set the compare flag CF2, this may also be used to generate an interrupt.

Parallel to the T2-only, Capture and Auto-Reload mode, a Pulse Width Modulation function can be activated by setting the ECOMP bit in the T2CON register. This will activate the alternative port function T2COMP for port bit P1.2. Every time a compare match or a timer overflow occurs, P1.2 (T2COMP) is toggled. The initial state of P1.2 after setting ECOMP is LOW.

If this pulse function is used in conjunction with the Auto-Reload mode and the compare function, a Pulse Width Modulation (PWM) function is realized. The PWM frequency is given by the reload value stored in register RCAP2L/RCAP2H. The PWM duty cycle is given by the value stored in register COMP2L/COMP2H. In Fig.8 an example of this is given with a 25/75% duty cycle.

As a special case, if both registers COMP2H and COMP2L are reset, the frequency on pin P1.2/T2COMP will be given only by the value of the reload register RCAP2L/RCAP2H and is half the frequency for an active compare. The duty cycle will be 50% as shown in Fig.9.

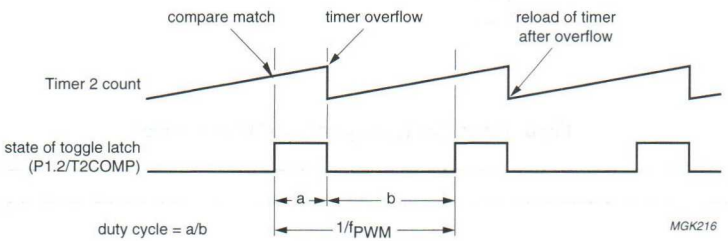


Fig.8 Timer 2: PWM output function with duty cycle 25/75%.

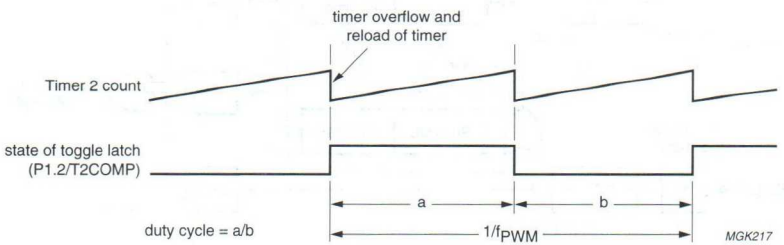


Fig.9 Timer 2: PWM output function with duty cycle 50/50%.

4.8.2 Timer/Counter 2 Control Register (T2CON)

Table 14 Timer/Counter 2 Control Register (SFR address C8H)

7	6	5	4	3	2	1	0
TF2	EXF2	CF2	ECOMP	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 15 Description of T2CON bits

BIT	SYMBOL	DESCRIPTION
T2CON.7	TF2	**Timer 2 overflow flag.** TF2 is set by a Timer 2 overflow and must be cleared by software. When Timer T2 interrupt is enabled, TF2 = 1 will cause the CPU to vector to Timer 2 interrupt routine. TF2 must be cleared by software. TF2 can also be set by software.
T2CON.6	EXF2	**Timer 2 external flag.** EXF2 is set when either a capture or reload is caused by a negative transition on T2EX and when EXEN2 = 1. When Timer T2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 can also be set by software.
T2CON.5	CF2	**Compare flag.** CF2 is set by hardware if the timer register TL2/TH2 increments to the value of the compare register COMP2L/COMP2H. CF2 must be cleared by software. When Timer T2 interrupt is enabled, CF2 = 1 will cause the CPU to vector to Timer 2 interrupt routine. CF2 must be cleared by software. CF2 can also be set by software.
T2CON.4	ECOMP	**Enable compare.** When set by software, the controller toggles port bit P1.2 (T2COMP) every time a compare match or a timer overflow occurs. The toggle latch connected to port P1.2/T2COMP is reset when bit ECOMP is cleared.
T2CON.3	EXEN2	**Timer 2 external enable flag.** When set, allows a capture or reload to occur as a result of a negative transition on T2EX. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
T2CON.2	TR2	**Timer 2 start/stop control.** If TR2 is set, the 16-bit counter (TH2,TL2) will start counting.
T2CON.1	C/$\overline{T2}$	**Timer 2 timer or counter select.** C/$\overline{T2}$ = 0 selects the internal timer with a clock frequency of $\frac{1}{6} \times f_{osc}$. C/$\overline{T2}$ = 1 selects the external event counter; negative edge-triggered.
T2CON.0	CP/$\overline{RL2}$	**Capture/reload flag.** When set captures will occur on negative transitions at T2EX, if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1.

4.8.3 WATCHDOG TIMER

In addition to the standard timers and Timer 2, a Watchdog Timer consisting of an 13-bit prescaler and an 8-bit timer WDTIM is also incorporated. The prescaler is incremented by the external clock. The 8-bit timer is incremented every 8192 clock cycles.

If the clock frequency is 3.58 MHz, the Watchdog Timer can operate in the range of 2.3 ms up to 0.56 s. The Watchdog Timer is disabled after reset. It can be enabled by writing any value to the WDCON register. A running Watchdog Timer will only be disabled if the microcontroller enters Power-down mode or if the microcontroller is reset.

When a timer overflow occurs and the Watchdog Enable pin ($\overline{EW}$) is LOW, the reset pin ($\overline{RST}$) will be activated (pulled-down) and the microcontroller will be reset. To prevent an overflow of the Watchdog Timer, the user program must reload the Watchdog register within a period shorter than the programmed timer interval.

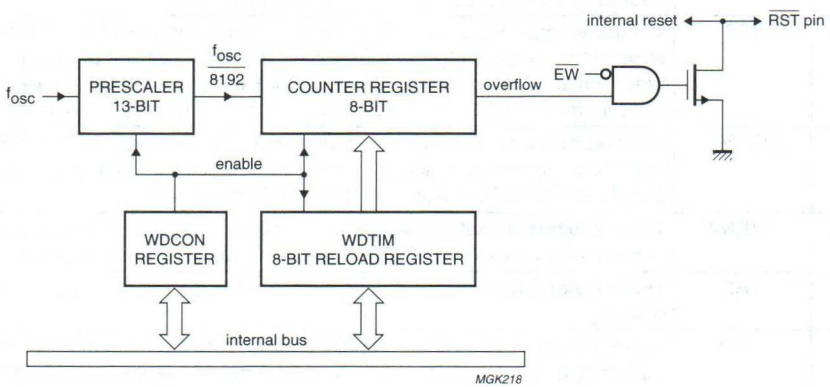


Fig.10 Functional diagram of the Watchdog Timer (T3).

4.8.4 Watchdog timer interval Register (WDTIM)

The reset value of WDTIM is 00H. The WDTIM register can only be written to if the WDCON register contains the value 5AH. The Watchdog Timer period can be calculated as follows:

$$\text{Watchdog period} = \frac{(256 - \text{WDTIM}) \times 8192}{f_{osc}}$$

Table 16 Watchdog Timer Interval Register (SFR address FFH)

7	6	5	4	3	2	1	0
WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0

Table 17 Description of WDTIM bits

BIT	SYMBOL	DESCRIPTION
WDTIM.7 to WDTIM.0	WD7 to WD0	The state of these 8-bits determine the Watchdog Timer period.

4.8.5 Watchdog Timer control Register (WDCON)

The Watchdog Timer is controlled by the WDCON register. A value of A5H in WDCON clears both the prescaler and the timer WDTIM. After reset WDCON contains the value A5H. Every value other than A5H in WDCON enables the Watchdog Timer. Since the WD0 bit of the WDCON input is tied to a logic 0 by hardware during write operations to WDCON, the reset value A5H can not be programmed again and can only be restored by a reset.

Timer WDTIM can be written only if WDCON has previously been loaded with 5AH, otherwise WDTIM and the prescaler are not affected. A successful write operation to WDTIM also clears the prescaler and clears WDCON.

Only the values A5H and 5AH are stored, all other values are stored with a dummy value 00H.

Table 18 Watchdog Control Register (SFR address A5H)

7	6	5	4	3	2	1	0
WC7	WC6	WC5	WC4	WC3	WC2	WC1	WC0

Table 19 Description of WDCON bits

BIT	SYMBOL	DESCRIPTION
WDCON.7 to WDCON.0	WC7 to WC0	Watchdog Timer control bits

4.8.6 Pulse Width Modulated output

One pulse width modulated output channel is provided which outputs pulses of programmable length and interval. The repetition frequency is defined by an 8-bit prescaler (PWMP) that generates the clock for the counter. The 8-bit counter counts modulo 255 i.e. from 0 to 254 inclusive. The value held in the 8-bit counter is compared to the contents of the register PWM0. Provided the contents of this register are greater than the counter value, the $\overline{\text{PWM0}}$ output is set LOW. If the contents of register PWM0 are equal to, or less than the counter value, the $\overline{\text{PWM0}}$ output is set HIGH. The pulse-width-ratio is therefore defined by the contents of register PWM0. The pulse-width-ratio will be in the range 0 to 255/255 and may be programmed in increments of $1/255$.

The repetition frequency at the $\overline{\text{PWM0}}$ output is given by:

$$f_{PWM} = \frac{f_{osc}}{[(1 + PWMP) \times 255]}$$

When using an oscillator frequency of 3.58 MHz for example, the above formula gives a repetition frequency range of 55 Hz to 14 kHz.

By loading the PWMO register with either 00H or FFH, the $\overline{\text{PWM0}}$ output can be maintained at a constant HIGH or LOW level respectively. When loading FFH into the PWM0 register, the 8-bit counter will never actually reach this value.

The $\overline{\text{PWM0}}$ output pin is driven by push-pull drivers and is not shared with any other function.

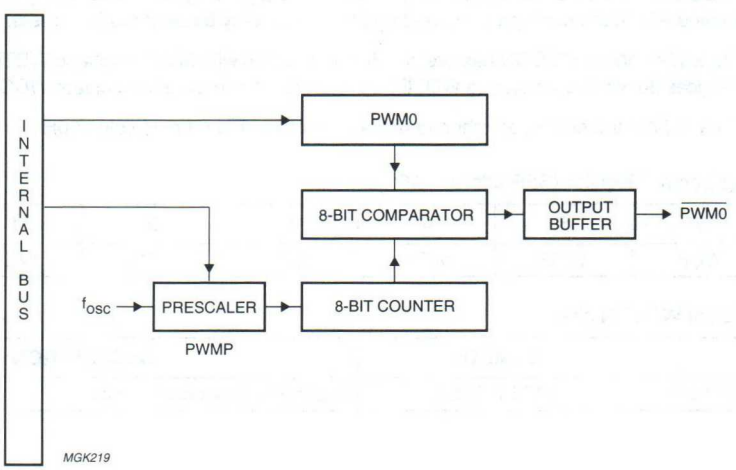


Fig.11 Functional diagram of pulse width modulated output.

4.8.7 Prescaler Frequency Control Register (PWMP)

Table 20 Prescaler Frequency Control Register (SFR address FEH)

7	6	5	4	3	2	1	0
PWMP.7	PWMP.6	PWMP.5	PWMP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.0

Table 21 Description of PWMP bits

BIT	SYMBOL	DESCRIPTION
7 to 0	PWMP7 to PWMP.0	prescaler division factor = (PWMP) + 1

4.8.8 Pulse Width Modulated Register (PWM0)

Table 22 Pulse Width Modulated Register (SFR address FCH)

7	6	5	4	3	2	1	0
PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0

Table 23 Description of PWM0 bits

BIT	SYMBOL	DESCRIPTION
7 to 0	PWM07 to PWM0.0	These 8-bits define the pulse-width-ratio.

4.9 EEPROM

4.9.1 General description

Most microcontrollers in the TELX family contain an on-chip low-power Electrically Erasable Programmable ROM (EEPROM) memory for non-volatile data storage. The memory offers the following features:

- Low power consumption
- No current consumption if the EEPROM is disabled (see Section 4.9.6)
- Single supply programming; the programming voltage is generated internally via an on-chip voltage multiplier
- Automatic ERASE before WRITE when programming
- User defined programming time (see Section 4.9.6)
- Page programming; 1 to 8 bytes can be programmed simultaneously, reducing programming time
- Accessible via I²C-bus:
  - Fixed slave address
  - Operates in Slave Transmitter or Slave Receiver modes
  - Can be accessed from a master connected to the external I²C-bus (EEPROM access in external mode)
  - Can be accessed from the host master even if ports P1.6 and P1.7 are not used as I²C-bus pins (EEPROM access in internal mode)
  - Supports continuous read and page-write, (word address automatically incremented).

4.9.2 I²C-bus operation

The operation of the EEPROM memory depends on the state of the I²C-bus interface (see Section 4.12) and of the port pins P1.6 and P1.7 (see Section 4.7.2). Three situations are possible:

1. **EEPROM access in internal mode.** The I²C-bus serial I/O interface and the EEPROM memory are active, but the port pins P1.6 and P1.7 are not used as I²C-bus pins.

   The CPU of the TELX microcontroller can program and read the EEPROM. Port pins P1.6 and P1.7 can be used as open-drain ports for other purposes.
2. **EEPROM access in external mode.** The I²C-bus serial I/O master is not active, port pins P1.6 and P1.7 are configured as I²C-bus pins, and the EEPROM is active.

   The EEPROM can be accessed from a master connected to the I²C-bus (see Fig.13), but not from the TELX CPU.
3. **EEPROM access in mixed mode**. Both the serial I/O interface and EEPROM are active, P1.6 and P1.7 are configured as I²C-bus pins.

   Both the CPU of the TELX and external master(s) can read/programme the EEPROM.

After reset, the I²C-bus is in internal mode. In external mode, I²C-bus pull-up resistors must be connected to P1.6 and P1.7.

Table 24 EEPROM modes of operation

MODE	CONTROL REGISTER					
	PnCFGA[1]		PnCFGB[1]		S1CON[2]	EECON[3]
	P1CFGA.6	P1CFGA.7	P1CFGB.6	P1CFGB.7	ENS1	EEPE
EEPROM disabled[4]	X	X	X	X	X	0
Internal mode	X	1	X	X	1	1
External mode	0	0	0	0	0	1
Mixed mode	0	0	0	0	1	1

Notes

1. See Section 4.7.2, Table 11.
2. See Section 4.12.
3. See Section 4.9.6.
4. When disabled, the EEPROM will not acknowledge any I²C-bus request, and consumes no power.

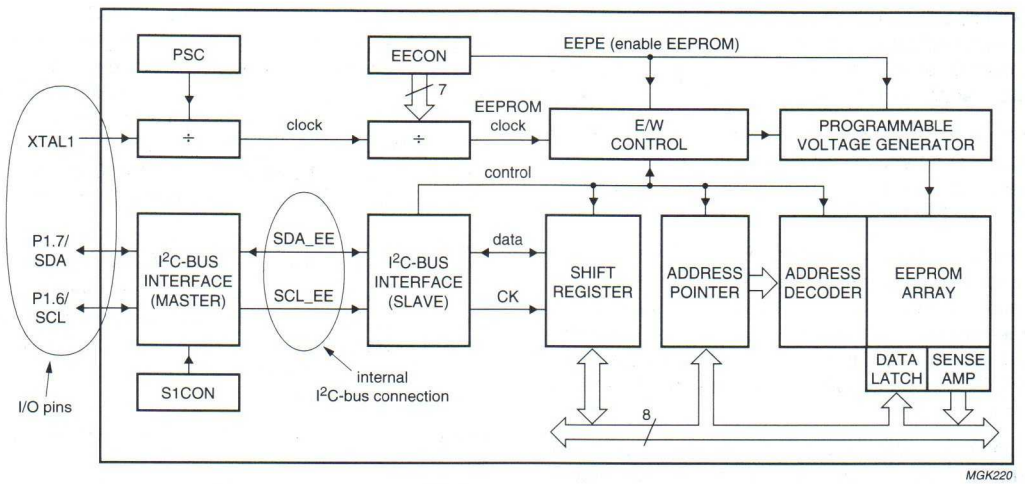


Fig.12 Block diagram of the EEPROM with I²C-bus interface.

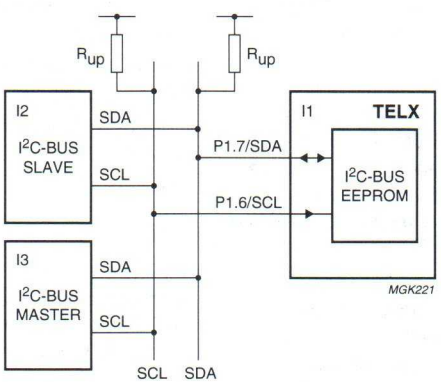


Fig.13 EEPROM access in external mode. The device I3 can access the EEPROM of the TELX.

4.9.3 EEPROM Addressing And Operation

The EEPROM is accessed with an I²C Start (S) condition, followed by a 7-bit slave address and a control bit (R/$\overline{W}$). Upon successful decoding of the address, the EEPROM answers with an I²C Acknowledge (A). Figure 14 shows the slave addresses for the different EEPROM sizes.

In microcontrollers with a 512-byte EEPROM, the 7th bit (A8) sent after the 6-bit slave address is part of the word address (A8 is the most significant address bit of the 512-byte EEPROM array).

The last bit of the slave address (R/$\overline{W}$) defines the operation to be performed. When set to logic 1 a read operation is selected (the EEPROM will output the addressed data onto SDA at every SCL pulse), and when set to logic 0 the EEPROM will be ready to accept 7 bits of EEPROM address, possibly followed by data bytes to be stored in the EEPROM.

The master can abort any Read or Write operation at any time during I²C-bus data transfer by generating a new Start (S) without generating a Stop (P) condition.

4.9.4 Write Operations

4.9.4.1 Byte Write

After addressing the EEPROM with the R/$\overline{W}$ bit set to a logic 0, the EEPROM responds with an acknowledge and expects to receive a word address, followed by a byte of data to be written. In the case of a 512-byte EEPROM, the bit before R/$\overline{W}$ is the MSB of the word address of the byte to be written (A8). The master then sends the word address (A0 to A7), to which the EEPROM sends an acknowledge (A). Finally the master sends the data to be written, acknowledged by the EEPROM. The master sends a Stop condition (P) to start an Erase/Write cycle. The cycle takes typically 10 ms and is controlled by the E/W control circuitry (see Fig.12). The byte write sequence is shown in Fig.15, for the case n = 1.

Note that a Write to the EEPROM is implemented as a logical OR with the previously stored data; a Write operation must therefore be preceded with an Erase to clear the byte first. The E/W control logic will automatically generate the necessary Erase followed by the Write when a Stop condition is generated. The write time is specified for the complete Erase/Write cycle.

During the Erase/Write cycle the I²C-bus interface of the EEPROM is idle, i.e., it does not acknowledge when addressed (see also Section 4.9.4.3).

4.9.4.2 Page Write

In order to reduce total programming time when several bytes of data are to be written to the EEPROM, a page-write operation is available. Up to 8 bytes of data can be programmed with a single Erase/Write cycle, as long as all bytes are on the same page, i.e., their addresses only differ on the 3 lowest bits (A0 to A2). The sequence is similar to the byte-write: the master sends a Start (S) and slave address with the R/$\overline{W}$ bit set to logic 0, followed by the word address of the first data byte to be programmed.

Then the first data byte is sent, and instead of immediately generating a Stop condition, the master sends up to 7 additional bytes; the 3 lowest bits of the address are automatically incremented, the highest bits remain fixed. The EEPROM acknowledges each data byte. Finally a Stop (P) is generated to start an Erase/Write cycle. This sequence is shown Fig.15.

Any number of bytes from 1 to 8 can be written, but their low addresses (A0 to A2) must be sequential. When the page addresses reaches end-of-page (A0 to A2 = 111), the address will wrap around to '000' (binary). Fig.16 shows two examples of possible page set-up; the first example shows eight bytes written starting from the beginning of the page (address 00H), and the second example shows six bytes written starting in the middle of the page, at address 15H.

If more then 8 bytes are sent by the master, the EEPROM will ignore and will **not** acknowledge the 9th, 10th etc., bytes. The master can proceed in one of two ways:

- Abort the write procedure, by sending a Start (S) and repeating the complete page-write procedure of Fig.15
- Start and Erase/Write cycle by generating a Stop (P). The first 8 bytes transmitted will be written into the EEPROM cells.

4.9.4.3 Acknowledge Polling

During programming, the EEPROM does not acknowledge when addressed by an I²C-bus master. To find out when the EEPROM is again accessible, the microcontroller must perform ACK polling, i.e. repeatedly send a Start and slave address and check if an acknowledge is generated.

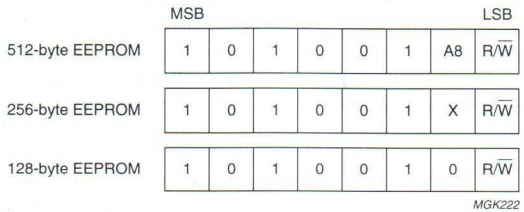


Fig.14 Slave address format for the EEPROM.

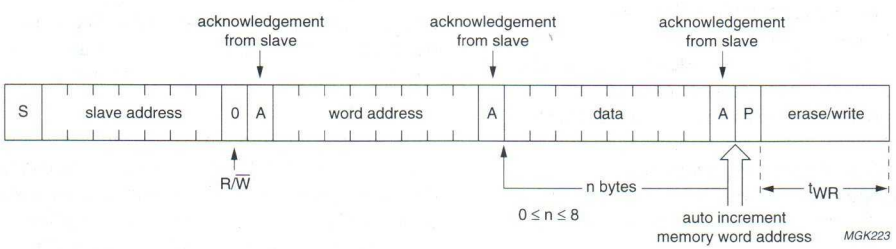


Fig.15 Master transmits to slave receiver (Write mode).

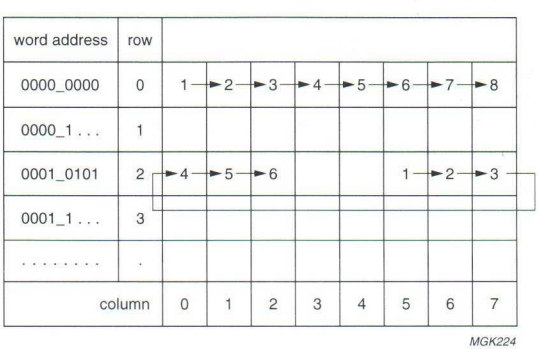


Fig.16 Two examples of writing eight or six bytes with different word addresses.

4.9.5 Read Operations

An unlimited number of data bytes can be read, the address being automatically incremented after each byte is transmitted. A Read can be done in two ways: by first setting the word address (Random Read), or without setting the word address (Current Address Read). Both ways allow to sequentially read any number of bytes (Sequential Read).

4.9.5.1 Current Address Read

The master addresses the EEPROM slave with the R/$\overline{W}$ bit set to a logic 1. The EEPROM acknowledges, transmits the data byte addressed by the current contents of the address pointer, and increments it by 1. The master ends the read operation by generating a No-acknowledge (A = 1) and Stop (P).

If the master wishes to read more than one byte (Sequential Read), it generates an Acknowledge (A = 0) after receiving the data byte, and does not generate a Stop. Any number of bytes can be read with this procedure; the address pointer will wrap-around to address 00H when the highest address is read. To end Sequential Read, the master generates a No-acknowledge (A = 1) and a Stop (P). Figure 17 illustrates the Current Address Read and Sequential Read procedure.

When using the Current Address Read, the contents of the address pointer are equal to the address of the byte previously accessed (either by a previous read or write) incremented by 1; e.g., if the previous action was writing or reading byte addressed by 'n', using Current Address Read will retrieve the byte addressed by 'n + 1'.

Note there is an exception to the above rule: when using Current Address Read with 512-byte EEPROMs, the MSB of the current read address (A8) is overwritten each time the Slave address is sent. For example, if the byte previously accessed was addressed by 000H, and the EEPROM is selected using A8 = 1, the data retrieved will be in address 101H (A8 = 1, A0 to A7 incremented by 1) and not 001H.

4.9.5.2 Random Read

In Random Read mode, the address of the byte to be read is sent prior to the read. The master selects the EEPROM with the R/$\overline{W}$ bit set to logic 0 (write), and upon Acknowledge from the EEPROM sends the 8-bit word address, which is loaded into the Address pointer and acknowledged by the EEPROM. The master then sends a Repetitive Start (Sr, a Start without previously having generated a Stop) selecting again the slave with the R/$\overline{W}$ bit to logic 1 (read). The EEPROM transmits the byte addressed by the address pointer and increments it at the end. The master ends Random Read by generating a No-acknowledge (A = 1) and a Stop (S).

If the master wishes to read more bytes, it generates an Acknowledge (A = 0) after receiving each byte (Sequential Read). Any number of bytes can be read; the address pointer will wrap-around to address 00H when the highest address is read. To end Sequential Read, the master generates a No-acknowledge (A = 1) and a Stop (P). Figure 18 shows the Random Read and Sequential Read procedure.

Note when using Random Read with EEPROM memories with 512-bytes, the MSB of the word address (A8) sent during the Write frame is overwritten when the slave is addressed a second time, after the Repetitive Start (Sr). For example, if the word-address sent is 000H (A8 = 0), and the slave address after the Repetitive Start contains A8 = 1, then the data retrieved is addressed by 100H and not 000H.

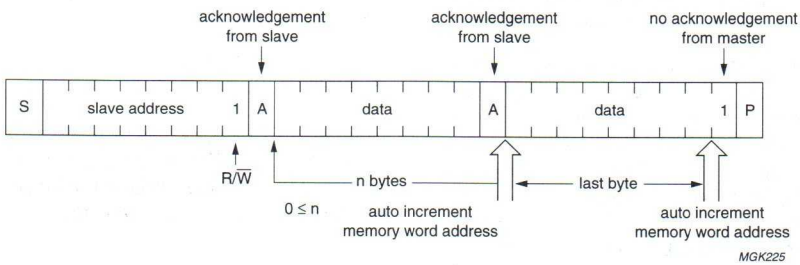


Fig.17 Current Address Read.

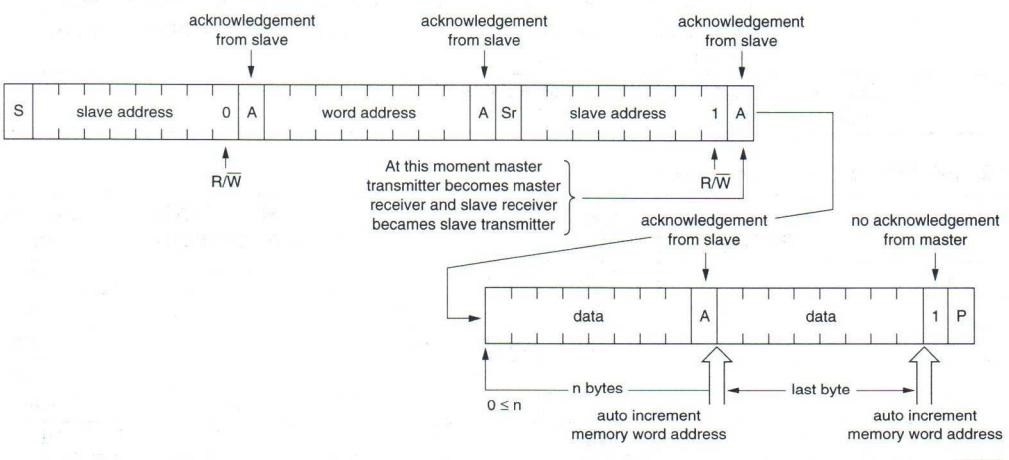


Fig.18 Random Read.

4.9.6 EEPROM Control Register (EECON)

This Special Function Register controls the operation of the EEPROM. The programming time (Erase/Write cycle) is defined by the crystal frequency, the pre-scaler division factor and the EECON bits (EEC0 to EEC6). Erase and Write operations take the same time. Typically 4 to 5 ms are necessary to erase or write the EEPROM cells giving a total Erase/Write cycle time of 8 (minimum) to 10 ms.

To achieve these programming times, the E/W control circuit requires a clock (EEPROM clock, see Fig.12) with a frequency between 51 and 63.75 kHz (max.). Frequencies lower than 51 kHz are acceptable, but result in a programming time greater than 10 ms. The frequency of XTAL is divided by the contents of the PSC register to define the internal clock frequency. This clock is then divided by the contents of the EEC0 to EEC6 bits to generate the 51 kHz EEPROM clock. The Erase and Write times are obtained by further dividing this clock by 255.

The total Erase/Write time is given by the relationship shown below:

$$t_{WR} = 2 \times 255 \times \frac{XTAL1}{PSC \times EECON}$$

To determine the EECON value given the XTAL frequency and the PSC factor the relationship shown below should be used:

$$EECON = \frac{XTAL1 \times t_{WR}}{PSC \times 510}$$

Note that EECON can only take integer values between 2 and 127. Table 27 shows some examples of XTAL frequencies, Prescaler Division Factor and EECON values and the resulting Erase/Write times.

Table 25 EEPROM Control Register (see Section 4.6 for the SFR addressing)

7	6	5	4	3	2	1	0
EEPE	EEC6	EEC5	EEC4	EEC3	EEC2	EEC1	EEC0

Table 26 Description of EECON bits

BIT	SYMBOL	DESCRIPTION
7	EEPE	**EEPROM Enable.** When EEPE = 1, the EEPROM is enabled and can be read and written to. When EEPE = 0, the EEPROM is disabled and in this state consumes no power; reading and writing operations are not possible and the I^2C-bus interface will not acknowledge any request.
6 to 0	EEC6 to EEC0	The decimal value of these 7-bits determines the divider value for the EEPROM programming clock.

Table 27 EEPROM division factor examples

XTAL FREQUENCY (MHz)	PSC DIVISION FACTOR	f_{PSC} (kHz)	EECON VALUE(1)	EEPROM CLOCK FREQUENCY (kHz)	E/W TIME (ms)
30	8	3.75	65 (1100 0001)	57.7	8.84
20	6	3.33	57 (1011 1001)	58.4	8.73
8.0	2	4.00	69 (1100 0101)	57.8	8.80
3.58	1	3.58	62 (1011 1110)	57.7	8.84
1.0	1	1.00	17 (1001 0001)	58.8	8.67
0.102	1	0.102	2 (1000 0010)	51.0	10.0

Note

1. The EECON division value is in decimal notation and between brackets in binary. The EEPE bit is set to a logic 1 in all cases. The smallest EECON VALUE is 2 (1000 0010). EECON VALUE = 1 (1000 0001) or 0 (1000 0000) generates no EEPROM clock and should not be used.

4.10 DTMF generator section

A versatile frequency generator section is provided and is shown in Fig.19. For normal operation use a 3.579545 MHz (or a multiple of this frequency) quartz crystal or PXE resonator. The frequency generator includes precision circuitry for dual-tone multi-frequency (DTMF) signals, which is typically used for tone dialling telephone sets. The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s. In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available.

4.10.1 Frequency registers

The two frequency registers (LGF and HGF) define two frequencies and from these, the digital sine wave synthesizers together with the Digital-to-Analog Convertors construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures tone output levels independent of supply voltage and temperature.

The amplitude of the Low Group Frequency sine wave is attenuated by 2 dB compared to the amplitude of the High Group Frequency sine wave.

The two sine waves are summed and then filtered by on-chip switched capacitor and RC low-pass filters. These guarantee all DTMF tones generated fulfil the CEPT CS203 recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components. A value of 00H in a frequency register stops the corresponding digital sine wave synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption. A decimal value of 'x' in a frequency register yields a digital sine wave signal with frequency:

$$f = \frac{f_{xtal}}{[23\,(x+2)]}\ ;\ \text{where } 60 \leq x \leq 255$$

The frequency limitation given by $x \geq 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

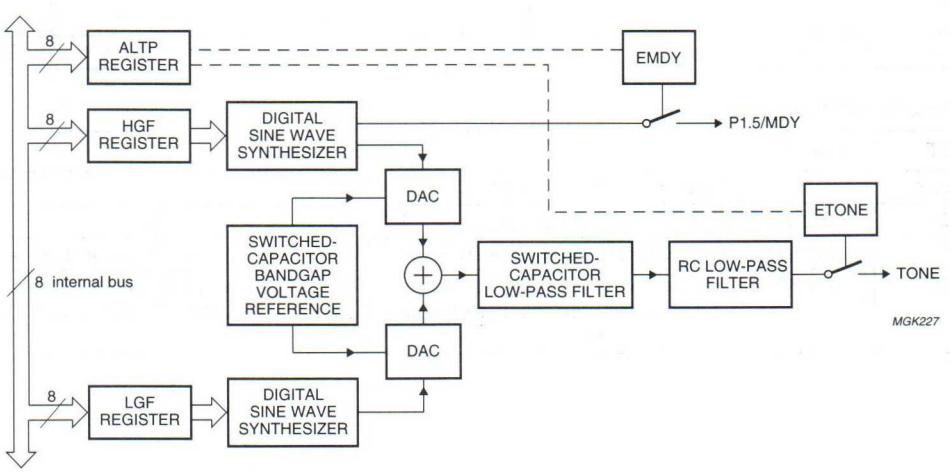


Fig.19 Block diagram of the Frequency Generator section.

4.10.2 Low Group Frequency Register (LGF)

Table 28 Low Group Frequency Register (address A1H; access type W)

7	6	5	4	3	2	1	0
L7	L6	L5	L4	L3	L2	L1	L0

Table 29 Description of LGF bits

BIT	SYMBOL	DESCRIPTION
7 to 0	L7 to L0	The decimal value of these 8-bits determines the Low Group Frequency.

4.10.3 High Group Frequency Register (HGF)

Table 30 High Group Frequency Register (address A2H; access type W)

7	6	5	4	3	2	1	0
H7	H6	H5	H4	H3	H2	H1	H0

Table 31 Description of HGF bits

BIT	SYMBOL	DESCRIPTION
7 to 0	H7 to H0	The decimal value of these 8-bits determines the High Group Frequency.

4.10.4 Alternative Port Function Control Register (ALTP)

Table 32 Alternative Port Control Register (address A3H; access type W)

7	6	5	4	3	2	1	0
–	–	–	–	–	ECLK	EMLDY	ETONE

Table 33 Description of ALTP bits

BIT	SYMBOL	DESCRIPTION
7 to 3	–	These 5-bits are not used.
2	ECLK	**Enable Clock.** When ECLK = 1, P1.4 will output the system clock.
1	EMLDY	**Enable MLDY.** When EMLDY = 1, the MLDY output is enabled (multiplexed with P1.5).
0	ETONE	**Enable Tone.** When ETONE = 1, the TONE output is enabled. When ETONE = 0, the TONE output is disabled (default after reset) however the MLDY output can still be active if required.

4.10.5 DTMF FREQUENCIES

The input frequency to the frequency generator is f_{PSC}. Assuming an oscillator frequency of a multiple of f_{DTMF} = 3.579545 MHz, the division factor of the prescaler should be chosen such that $f_{PSC} = f_{DTMF}$. The DTMF standard frequencies can then be implemented as shown in Table 34. The relationship between telephone keyboard symbols and the frequency register contents are given in Table 35.

Table 34 DTMF standard frequencies and their implementation

LGF/HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 35 Dialling symbols, corresponding DTMF frequency pairs and frequency registers content

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQUENCY PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
•	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

4.10.6 MODEM FREQUENCIES

Assuming an oscillator frequency of $f_{PSC} = f_{DTMF} = 3.579545$ MHz, the standard modem frequency pairs summarized in Table 36 can be implemented. It is suggested to define the frequency using the HGF register while the LGF register contains 00H, disabling Low Group Frequency generation.

Table 36 Standard modem frequency pairs and their implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980[1]	978.82	−0.12	−1.18
82	1180[1]	1179.03	−0.08	−0.97
8F	1070[2]	1073.33	0.31	3.33
79	1270[2]	1265.30	−0.37	−4.70
80	1200[3]	1197.17	−0.24	−2.83
45	2200[3]	2192.01	−0.36	−7.99
76	1300[4]	1296.94	−0.24	−3.06
48	2100[4]	2103.14	0.15	3.14
5C	1650[1]	1655.66	0.34	5.66
52	1850[1]	1852.77	0.15	2.77
4B	2025[2]	2021.20	−0.19	−3.80
44	2225[2]	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

4.10.7 MUSICAL SCALE FREQUENCIES

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency $f_{PSC} = f_{DTMF} = 3.579545$ MHz (Table 37). It is suggested to define the frequency using the HGF register while the LGF register contains 00H, disabling Low group frequency generation.

Table 37 Musical scale frequencies and their implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD[1]	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 at 440 Hz.

4.11 MSK modem

The MSK modem is used for in-band signalling between handset and base in analog cordless telephone systems CT0, CT1 and CT1+. The MSK modem's receiver and transmitter can be enabled separately. Receive and transmit interrupts can wake-up the microcontroller during its power saving Idle mode. Baud rates are programmable between 1200 and 4800 Baud. Fig.20 shows the functional diagram of the MSK modem.

The modem has the following features:

- Full duplex operation via 8-bit parallel interface
- The message is fully Manchester coded/decoded
- Automatic detection of 16-bit Manchester preamble pattern
- The last received 4 bits of the preamble pattern are software programmable
- Receiver full, transmitter empty indication bits
- Manchester coding and decoding for clock recovery and early error detection
- Programmable input polarity
- Baud rate selection from 1200, 2400, 3600 and 4800 baud with internal modem timer
- Receiver and transmitter off-states with no power consumption.

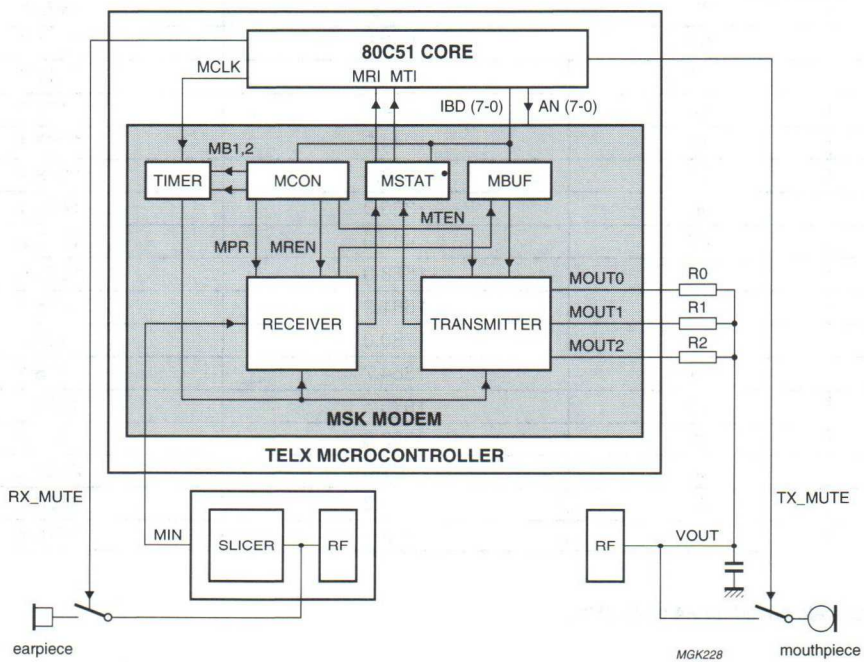


Fig.20 MSK modem functional diagram.

4.11.1 80C51 MICROCONTROLLER INTERFACE

The modem block interfaces to the microcontroller via the interrupt signals MRI and MTI and via the control and data SFRs MCON, MSTAT and MBUF. The MSK modem receive and transmit registers are both accessed via the Special Function Register MBUF. Writing to MBUF loads the transmit register and reading MBUF accesses a physically separate receive register.

4.11.1.1 MSK Modem Control Register (MCON)

Table 38 MSK Modem Control Register (SFR address D3H)

7	6	5	4	3	2	1	0
MPR3	MPR2	MPR1	MPR0	MB1	MB0	MTEN	MREN

Table 39 Description of MCON bits

BIT	SYMBOL	DESCRIPTION
MCON.7	MPR3	**Modem preamble pattern.** These 4 bits define the modem's preamble pattern.
MCON.6	MPR2	
MCON.5	MPR1	
MCON.4	MPR0	
MCON.3	MB1	**Modem transmit/receive frequency.** These 2-bits define the modem's transmit/receive frequency; see Table 40.
MCON.2	MB0	
MCON.1	MTEN	**Modem Transmitter Enable.** If this bit is set the transmitter is active and MOUT<3:1> will get the value <100> if no data is transmitted; if reset, MOUT<3:1> will get the value <111> to zero the currents in the resistive DAC. See note 1.
MCON.0	MREN	**Modem Receiver Enable.** If this bit is set the modem receiver is active and scans for Manchester data. See note 1.

Note

1. If both the transmitter and the receiver are disabled (MTEN = 0 and MREN = 0), the clock of the MSK modem is switched-off. It is advised to use this state for power saving.

Table 40 Selection of the modem's baud rates

MB1	MB0	MODEM BAUD RATE
0	0	1200 Baud
0	1	2400 Baud
1	0	3600 Baud
1	1	4800 Baud

4.11.1.2 MSK Modem Status Register (MSTAT)

Table 41 MSK modem Status Register (SFR address D2H)

7	6	5	4	3	2	1	0
–	–	MRF	MRE	MRP	MRL	MTI	MRI

Table 42 Description of MSTAT bits

BIT	SYMBOL	DESCRIPTION
MSTAT.5	MRF	**Modem Receiver Full flag.** MRF is set when MBUF holds a newly received byte. MRF is reset if the receiver is disabled (MREN = 0) or by reading MBUF. This bit is read-only. Writing to it will have no effect.
MSTAT.4	MRE	**Modem Receiver Error flag.** Indicates the reception of a non-Manchester bit. This bit is set by hardware and is reset by reading MBUF, by disabling the receiver (MREN = 0) or by resetting MRI. This bit is read-only. Writing to it will have no effect.
MSTAT.3	MRP	**Modem Receiver Preamble flag.** MRP is set by hardware when the modem recognizes the programmed preamble pattern (AAAH) after locking the receiver clock (MRL = 1). MRP is reset by hardware if the receiver is disabled (MREN = 0) or if non-Manchester data is received (MRE = 1). This bit is read-only. Writing to it will have no effect.
MSTAT.2	MRL	**Modem Receiver Clock Locked flag.** This bit is set when the clock of the receiver is locked, i.e. when the receiver has detected Manchester data but has not found the preamble pattern yet. MRL is reset when the receiver detects a non-Manchester bit or when the receiver is disabled. This bit is read-only. Writing to it will have no effect.
MSTAT.1	MTI	**Modem Transmit Interrupt flag.** Indicates MBUF is empty and ready to accept a new byte for transmission. MTI is reset by writing to MBUF or by writing a logic 0 to it. Writing a logic 1 to MTI sets the bit and allows a hardware interrupt to be generated by software.
MSTAT.0	MRI	**Modem Receive Interrupt flag.** Indicates Modem Receiver Full (MRF = 1) or Modem Receiver Error (MRE = 1) or Modem Receiver Preamble (MRP = 1) or Modem Receiver Clock Locked (MRL = 1) This bit is reset by reading MBUF or by writing a logic 0 to MRI. A reset of MRI will also reset MRE. Writing a logic 1 to MRI will have no effect.

4.11.1.3 MSK Modem Data Buffer (MBUF)

Table 43 MSK Modem Data Buffer (SFR address D1H)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 44 Description of MBUF bits

BIT	SYMBOL	DESCRIPTION
MBUF.7 to MBUF.0	D7 to D0	Writing to MBUF loads the data into the transmit buffer and starts a transmission at MOUT if the transmitter is enabled (MTEN = 1). A new byte can be loaded after MTI is set. If a new byte is loaded before MTI is set the previous byte will be lost. After data has been received at MIN, indicated by MRI, the received byte can be read from MBUF.

4.11.2 MODEM INTERFACE

The modem block has the following modem interface signals.

- **MIN:** digital MSK Manchester coded input signal from the Data slicer. MIN is the alternative input function of P4.0. If P4.0 is used for MIN, it has to be configured to be an input port. The data that is written to the ports data SFR can be used to switch the polarity of MIN. If P4.0 data is set, the value on the pin is passed to MIN with inverted polarity. If P4.0 data is reset, the value on the pin is passed directly to MIN.
- **MOUT0 to MOUT2:** 3-bit Manchester coded output signal of the modem.

The mute signals RX_MUTE and TX_MUTE must be generated by software. Any standard I/O port pin can be used for this purpose.

4.11.3 DATA TRANSMISSION

Data transmission is enabled if bit MTEN in register MCON is set to a logic 1. If MTEN is a logic 0, data transmission is disabled and MOUT<2:0> is set to <111> to zero the currents in the resistive DAC. Setting MTEN to a logic 1 sets MOUT<2:0> to the idle value <100>. This results in a value close to $\frac{1}{2} \times V_{DD}$ on the output signal of the external DAC. Transmission is started by loading the first byte into register MBUF. All bytes are transmitted starting with the MSB.

A message is transferred in a block of 3 or more bytes, the first two bytes being the programmed Manchester preamble pattern. In order to insert the preamble pattern, the first two bytes AAH and AXH (with X being the MPR3 to MPR0 value programmed in the receiver MSK modem) have to be written to MBUF by software. After this, the first byte of the message is written to MBUF. As soon as MBUF is ready to accept new input, signal MTI is set. A new byte written to MBUF automatically clears MTI. The time between two MTI interrupts is $T = 8 \times 1/$ baud rate (e.g. for baud rate 1200 baud, T = 6.7 ms). If no new byte is written to MBUF at the end of a byte transmission, the modem transmitter stops transmission and MOUT<2:0> is set to the idle state <100>.

In this case MTI must be cleared explicitly. If MTEN is reset during transmission, the transmitter will finish the transmission of the current byte and then will set MOUT<2:0> to the off state <111>. No interrupt on MTI will be generated at the end of the transmission.

4.11.4 DATA RECEPTION

A message is received as a block of one or more data bytes. When enabled, the receiver starts sampling MIN and tries to detect a Manchester pattern. As soon as 3 consecutive Manchester bits are detected the receiver clock is locked (MRL = 1) and the receiver starts scanning the incoming data for the programmed Manchester preamble pattern. When the modem recognizes the preamble pattern, bit MRP is set to a logic 1. If a non-Manchester bit is detected before finding the preamble pattern then MRL is reset and MRE is set to a logic 1. The synchronisation process has to restart. If the preamble pattern has been detected the receiver starts to Manchester decode the incoming data bits and shifts them into an internal register. After eight bits the contents of the internal register are copied to MBUF and MRF bit is set to a logic 1. The received byte can be read from MBUF while receiving continues in the internal register. If a non-Manchester bit is received during data reception then MRE is set to a logic 1 and MRL and MRP are reset. The receiver has to resynchronize before receiving new data.

Whenever one of the bits MRF, MRE, MRP and MRL is set the MRI bit is also set and an RTI interrupt is generated. This means that when an RTI interrupt occurs the 4 status bits have to be polled by software. The bit MRL allows the software to decide very quickly whether an occupied channel contains Manchester coded data or not. The MRP bit is used to find the start of data transmission in a message that is repeated over and over again. MRE is used to detect a Manchester error, which is a violation of the Manchester coding rule that the received level should change in the middle of a bitcell. The MRF bit indicates that the data in MBUF is ready to be read by the software. During data reception the time between two settings of MRF (each one generating an MRI interrupt) is $T = 8 \times 1/$baud rate. Figure 22 shows an example of the timing diagram of data reception.

4.11.5 MANCHESTER CODING OF DATA

The bits of the data byte written in MBUF are Manchester encoded as shown in Fig.22: A '1' is coded as a LOW-to-HIGH transition in the middle of a bitcell, a '0' is coded as a HIGH-to-LOW transition.The Manchester encoded signal contains redundancy for early error detection in received bits. A non-matching HIGH-to-LOW or LOW-to-HIGH pair indicates an error condition.The Manchester encoded signal has a po!arity change in each bitcell.

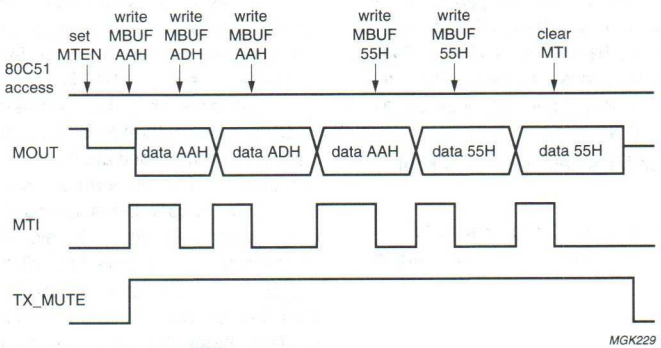


Fig.21 Data transmission timing diagram.

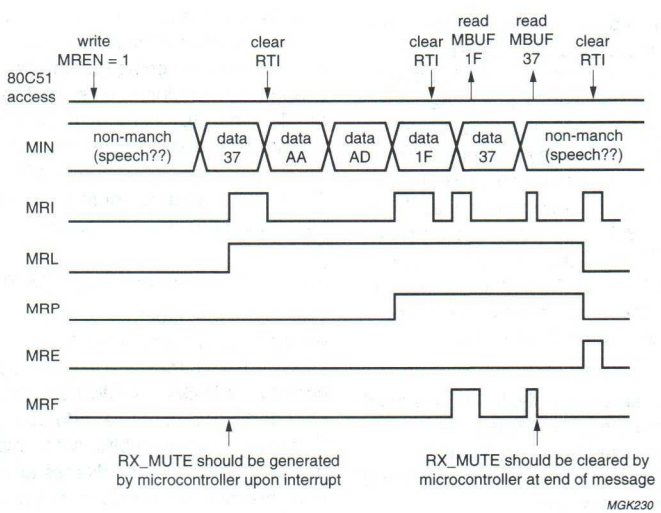


Fig.22 Data reception timing diagram.

4.11.6 WAVEFORM GENERATION WITH MOUT<2:0>

The 3 digital output pins MOUT0 to MOUT2, should be used as an input to a three bit external DAC. The signals can be connected via external resistors R0, R1 and R2 to a summation point and then be filtered with an external capacitor (C1). The 3-bit DAC is shown in Fig.23. Table 45 gives the relationship between the MOUT pins, the resistor values and VOUT.

Figure 24 shows the waveforms that are produced by the waveform generator. The horizontal axis shows the sample counter on which the waveform changes its value. Each bit is built-up out of 2 × 124 samples. The vertical axis shows the values of MOUT<2:0>, forming the inputs of the resistive DAC. The first half of the waveform is determined by the previous and the current bit, whereas the second half of the waveform is determined by the current and the next bit to be transmitted. The count frequency of the sample counter depends on the programmed baud rate.

If the transmitter is disabled with MTEN set to a logic 0, MOUT<2:0> is <111> to save power in the resistive DAC. If the transmitter is enabled and no data is transmitted, MOUT<2:0> has an idle value of <100>, which corresponds to $0.57 \times V_{DD}$.

4.11.7 SYNCHRONISATION

When enabled the receiver samples MIN with a frequency f = 8 × baud rate. The sampled values are shifted into an 8-bit shift register. This register is regularly checked to determine whether it contains samples that fulfil the Manchester coding rule i.e. whether there is a LOW-to-HIGH or a HIGH-to-LOW transition in the middle of the bitcell. The receiver searches for 3 consecutive sets of 8 samples that fulfil the Manchester coding rule. If these sets have been found the clock is locked (MRL = 1) and the receiver starts looking for the Manchester preamble pattern. From this point on the receiver uses a PLL (Phase Locked Loop) to adjust the synchronisation after each received Manchester bit.

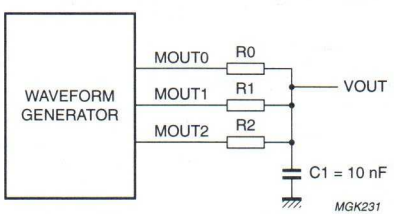


Fig.23 3 bit DAC with MOUT<2:0>.

Table 45 V_{out} as a function of MOUT<2:0> and the resistor values

MOUT2	MOUT1	MOUT0	VOUT	RESISTOR VALUES
0	0	0	0	R0 = R R1 = 0.48 × R R2 = 0.25 × R
0	0	1	$0.14 \times V_{DD}$	
0	1	0	$0.29 \times V_{DD}$	
0	1	1	$0.43 \times V_{DD}$	
1	0	0	$0.57 \times V_{DD}$	
1	0	1	$0.71 \times V_{DD}$	
1	1	0	$0.86 \times V_{DD}$	
1	1	1	V_{DD}	

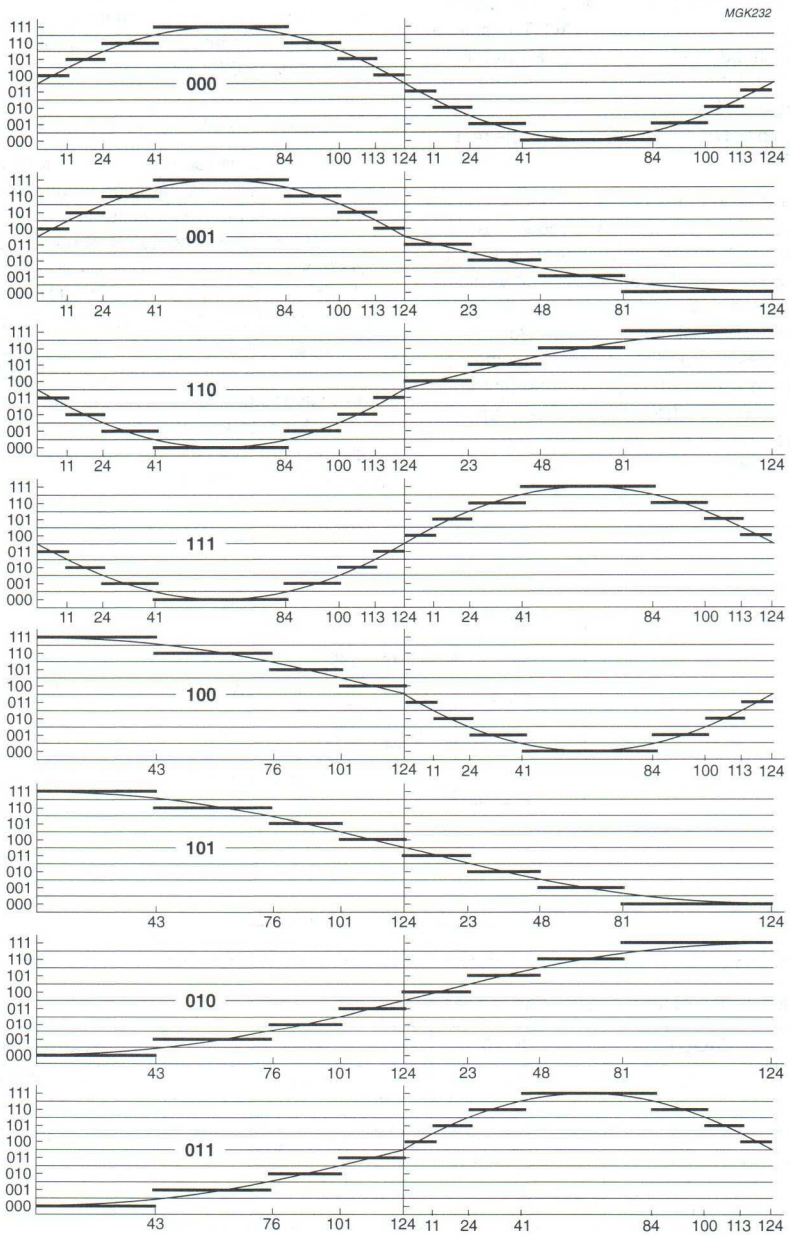


Fig.24 Waveforms with MOUT<2:0> for previous, current and next bits to be transmitted.

4.12 I²C-bus serial I/O

The serial port supports the twin line I²C-bus. The I²C-bus consists of two lines: a data line (SDA) and a clock line (SCL). These lines also function as the I/O port lines P1.7 and P1.6 respectively. The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware.

The I²C-bus serial I/O has complete autonomy in byte handling and operates in 4 modes:

- Master transmitter
- Master receiver
- Slave transmitter
- Slave receiver.

These functions are controlled by the S1CON register. S1STA is the Status Register whose contents may also be used as a vector to various service routines. S1DAT is the Data Shift Register and S1ADR the Slave Address Register. Slave address recognition is performed by on-chip hardware. The block diagram of the I²C-bus serial I/O is shown in Fig.25.

4.12.1 I²C-bus internal mode

A special internal mode is provided. In this mode other on-chip blocks with an I²C-bus interface can communicate without using the I/O port lines P1.7 and P1.6, thus freeing them for other purposes. The microcontroller can be configured to use this internal mode or the normal external mode, with the port configuration bits; see Section 4.7.2.

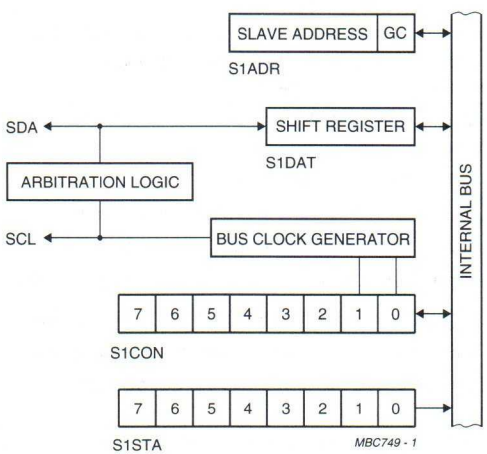


Fig.25 Block diagram of I²C-bus serial I/O.

4.12.2 Serial Control Register (S1CON)

Table 46 Serial Control Register (SFR address D8H)

7	6	5	4	3	2	1	0
CR2	ENS1	STA	STO	SI	AA	CR1	CR0

Table 47 Description of S1CON bits

BIT	SYMBOL	DESCRIPTION
S1CON.7	CR2	This bit along with bits CR1 and CR0 determines the serial clock frequency when SIO is in the Master mode. See Table 48. When CR2 = 0 the I^2C-bus is in fast mode.
S1CON.6	ENS1	**ENABLE serial I/O.** When ENS1 = 0, the serial I/O is disabled. SDA and SCL outputs are in the high-impedance state; P1.6 and P1.7 function as open-drain ports. When ENS1 = 1, the serial I/O is enabled. Output port latches P1.6 and P1.7 must be set to logic 1.
S1CON.5	STA	**START flag.** When this bit is set in Slave mode, the SIO hardware checks the status of the I^2C-bus and generates a START condition if the bus is free or after the bus becomes free. If STA is set while the SIO is in Master mode, SIO will generate a repeated START condition.
S1CON.4	STO	**STOP flag.** With this bit set while in Master mode a STOP condition is generated. When a STOP condition is detected on the I^2C-bus, the SIO hardware clears the STO flag. STO may also be set in Slave mode in order to recover from an error condition. In this case no STOP condition is transmitted to the I^2C-bus. However, the SIO hardware behaves as if a STOP condition has been received and releases the SDA and SCL. The SIO then switches to the not addressed slave receiver mode. The STOP flag is cleared by the hardware.
S1CON.3	SI	**SIO interrupt flag.** This flag is set, and an interrupt is generated, after any of the following events occur: • A start condition is generated in Master mode • Own slave address has been received during AA = 1 • The general call address has been received while S1ADR0 and AA = 1 • A data byte has been received or transmitted in Master mode (even if arbitration is lost) • A data byte has been received or transmitted as selected slave • A Stop or Start condition is received as selected slave receiver or transmitter. If this flag is set, the I^2C-bus is halted (by pulling down SCL). Received data is only valid until this flag is reset.
S1CON.2	AA	**Assert Acknowledge.** When this bit is set, an acknowledge (LOW level to SDA) is returned during the acknowledge clock pulse on the SCL line when: • Own slave address is received • General call address is received (S1ADR.0 = 1) • A data byte is received while the device is programmed to be a Master Receiver • A data byte is received while the device is a selected Slave Receiver. When this bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own slave address or general call address is received.
S1CON.1	CR1	These two bits along with the CR2 bit determine the serial clock frequency when SIO is in the Master mode. See Table 48.
S1CON.0	CR0	

Table 48 Selection of the serial clock frequency in the Master mode of operation; see notes 1 and 2

CR2	CR1	CR0	f_{osc} DIVISOR	BIT RATE (kHz) at f_{PSC}		
				3.58 MHz	4 MHz	6 MHz
0	0	0	10	358	400	(600)
0	0	1	20	179	200	300
0	1	0	30	119.33	133	199.5
0	1	1	40	89.5	100	150
1	0	0	80	44.75	50	75
1	0	1	120	29.83	33	49.5
1	1	0	160	22.38	25	37.5
1	1	1	(256 – T1 reload value) × 12 24 to 3072	1.17 to 149	1.3 to 167	100

Notes

1. Bit rates greater than 400 kHz are outside the specified frequency range.
2. When the CR (2:0) = 111, the maximum bit rate for the data transfer will be derived from the Timer 1 overflow rate divided by 2, i.e. every time the Timer 1 overflows the SCL signal will toggle.

4.12.3 Data Shift Register (S1DAT)

S1DAT contains the serial data to be transmitted or data which has just been received. Bit 7 is transmitted or received first; i.e. data shifted from left to right.

Table 49 Data Shift Register (SFR address DAH)

7	6	5	4	3	2	1	0
S1DAT.7	S1DAT.6	S1DAT.5	S1DAT.4	S1DAT.3	S1DAT.2	S1DAT.1	S1DAT.0

4.12.4 Address Register (S1ADR)

This 8-bit register may be loaded with the 7-bit slave address to which the controller will respond when programmed as a slave receiver/transmitter.

Table 50 Address Register (SFR address DBH)

7	6	5	4	3	2	1	0
SLA6	SLA5	SLA4	SLA3	SLA2	SLA1	SLA0	GC

Table 51 Description of S1ADR bits

BIT	SYMBOL	DESCRIPTION
S1ADR.7 to S1ADR.1	SLA6 to 0	own slave address
S1ADR.0	GC	this bit is used to determine whether the general CALL address is recognized; when a logic 0, the general CALL address is not recognized; when a logic 1, the general CALL address is recognized

4.12.5 Serial Status Register (S1STA)

The contents of this register may be used as a vector to a service routine. This optimizes the response time of the software and consequently that of the I²C-bus. S1STA is a read-only register. The status codes for all possible modes of the I²C-bus interface are given in Tables 54 to 58.

Table 52 Serial Status Register (SFR address D9H)

7	6	5	4	3	2	1	0
SC4	SC3	SC2	SC1	SC0	0	0	0

Table 53 Description of S1STA bits

BIT	SYMBOL	DESCRIPTION
S1STA.3 to S1STA.7	SC4 to SC0	5-bit status code
S1STA.0 to S1STA.2	–	these three bits are held LOW

Table 54 MST/TRX mode

S1STA VALUE	DESCRIPTION
08H	a START condition has been transmitted
10H	a repeated START condition has been transmitted
18H	SLA and W have been transmitted, ACK has been received
20H	SLA and W have been transmitted, $\overline{\text{ACK}}$ received
28H	DATA of S1DAT has been transmitted, ACK received
30H	DATA of S1DAT has been transmitted, $\overline{\text{ACK}}$ received
38H	arbitration lost in SLA, R/W or DATA

Table 55 MST/REC mode

S1STA VALUE	DESCRIPTION
38H	arbitration lost while returning $\overline{\text{ACK}}$
40H	SLA and R have been transmitted, ACK received
48H	SLA and R have been transmitted, $\overline{\text{ACK}}$ received
50H	DATA has been received, ACK returned
58H	DATA has been received, $\overline{\text{ACK}}$ returned

Table 56 SLV/REC mode

S1STA VALUE	DESCRIPTION
60H	own SLA and W have been received, ACK returned
68H	arbitration lost in SLA, R/W as MST; own SLA and W have been received, ACK returned
70H	general CALL has been received, ACK returned
78H	arbitration lost in SLA, R/W as MST; general CALL has been received
80H	previously addressed with own SLA; DATA byte received, ACK returned
88H	previously addressed with own SLA; DATA byte received, $\overline{\text{ACK}}$ returned
90H	previously addressed with general CALL; DATA byte has been received, ACK has been returned
98H	previously addressed with general CALL; DATA byte has been received, $\overline{\text{ACK}}$ has been returned
A0H	a STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX

Table 57 SLV/TRX mode

S1STA VALUE	DESCRIPTION
A8H	own SLA and R have been received, ACK returned
B0H	arbitration lost in SLA, R/W as MST. Own SLA and R have been received, ACK returned
B8H	DATA byte has been transmitted, ACK received
C0H	DATA byte has been transmitted, $\overline{\text{ACK}}$ received
C8H	last DATA byte has been transmitted (AA = logic 0), ACK received

Table 58 Miscellaneous

S1STA VALUE	DESCRIPTION
00H	bus error during MST mode or selected SLV mode, due to an erroneous START or STOP condition
F8H	no information available (reset value). The serial interrupt flag SI, is not yet set

Table 59 Symbols used in Tables 54 to 58

SYMBOL	DESCRIPTION
SLA	7-bit slave address
R	read bit
W	write bit
ACK	acknowledgement (acknowledge bit = logic 0)
$\overline{\text{ACK}}$	no acknowledgement (acknowledge bit = logic 1)
DATA	8-bit data byte to or from I^2C-bus
MST	master
SLV	slave
TRX	transmitter
REC	receiver

4.13 Standard serial interface SIO0: UART

This serial port is full duplex which means that it can transmit and receive simultaneously. It is also receive-buffered and can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte has not been read by the time the reception of the second byte is complete, the second bytes will be lost). The serial port receive and transmit registers are both accessed via the Special Function Register S0BUF. Writing to S0BUF loads the transmit register and reading S0BUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

Mode 0 Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted/received (LSB first). The baud rate is fixed at $1/6$ the oscillator frequency.

Mode 1 10 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first) and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register S0CON. The baud rate is variable.

Mode 2 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (1). On transmit, the 9th data bit (TB8 in S0CON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in S0CON, while the stop bit is ignored. The baud rate is programmable to either $1/32$ or $1/64$ of the oscillator frequency.

Mode 3 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that uses S0BUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

4.13.1 Multiprocessor communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th bit goes into RB8. The following bit is the stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated, but only if RB8 = 1. This feature is enabled by setting bit SM2 in S0CON. One use of this feature, in multiprocessor systems, is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is HIGH in an address byte and LOW in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be sent. The slaves that were not being addressed leave their SM2 bits set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

4.13.2 Serial Port Control Register (S0CON)

The Serial Port Control and Status Register is the Special Function Register S0CON; shown in Table 60. The register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Table 60 Serial Port Control Register (SFR address 98H)

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Table 61 Description of S0CON bits

BIT	SYMBOL	DESCRIPTION
S0CON.7	SM0	These 2 bits are used to select the serial port mode; see Table 62
S0CON.6	SM1	
S0CON.5	SM2	Enables the multiprocessor communication feature in Modes 2 and 3. In these modes, if SM2 = 1, then RI will not be activated if the received 9th data bit (RB8) is a logic 0. In Mode 1, if SM2 = 1, then RI will not be activated unless a valid Stop bit was received. In Mode 0, SM2 should be a logic 0.
S0CON.4	REN	enables serial reception and is set by software to enable reception, and cleared by software to disable reception
S0CON.3	TB8	is the 9th data bit that will be transmitted in Modes 2 and 3. Set or cleared by software as desired
S0CON.2	RB8	in Modes 2 and 3, is the 9th data bit received. In Mode 1, if SM2 = 0 then RB8 is the stop bit that was received; in Mode 0, RB8 is not used
S0CON.1	TI	The transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit time in the other modes, in any serial transmission. Must be cleared by software.
S0CON.0	RI	The receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial transmission (for exception see SM2). Must be cleared by software.

Table 62 Selection of the serial port modes

SM0	SM1	MODE	DESCRIPTION	BAUD RATE
0	0	0	shift register	$1/6 \times f_{osc}$
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	$1/64 \times f_{osc}$ or $1/32 \times f_{osc}$
1	1	3	9-bit UART	variable

4.13.3 BAUD RATES

In Mode 0 the baud rate is fixed as shown in Eqtn.(1):

$$\text{Baud rate} = \frac{f_{osc}}{6} \quad (1)$$

In Mode 2 the baud rate depends on the value of the SMOD bit in the PCON register and is calculated as shown in Eqtn.(2).

$$\text{Baud rate} = \frac{2^{SMOD}}{64} \times f_{osc} \quad (2)$$

For Modes 1 and 3 baud rates see Section 4.13.3.1.

4.13.3.1 Using the special purpose baud rate Timer to generate baud rates

In Modes 1 and 3 the baud rate is determined by the overflow rate of the special purpose baud rate timer and the value of the SMOD bit, as shown in Eqtn. (3):

$$\text{Baud rate} = \frac{2^{SMOD}}{32} \times \text{baud rate timer overflow rate} \quad (3)$$

The baud rate timer overflow rate is controlled by the value of the bits PRESC.7 to PRESC.3 in the PRESC register according to Eqtn.(4)

$$\text{Timer overflow rate} = f_{PSC} \times \frac{1}{2^{PTW0} \times 3^{P3}} \quad (4)$$

This gives the following formula for the baud rate:

$$\text{Baud rate} = \frac{2^{SMOD}}{32} \times f_{PSC} \times \frac{1}{2^{PTWO} \times 3^{P3}} \quad (5)$$

PTWO (PRESC.6 to PRESC.4) defines a power of two in the division factor of the baud rate timer. P3 (PRESC.3) defines a factor of 3 or 1 in the division factor of the baud rate timer. f_{PSC} is the frequency defined by the prescaler (see Section 4.3) and is the DTMF frequency of 3.579545 MHz in typical telecom applications.
The prescaler is controlled with the PS0 to PS2 bits in the PRESC register. Table 63 lists various commonly used baud rates and how they can be obtained with the special purpose baud rate timer and the PRESC register. For detailed description on PRESC see Section 4.3.1.

Table 63 Baud rate timer generated commonly used baud rates, based on f_{PSC} = 3.579545 MHz

BAUD RATE (kbits/s)		SMOD	PRESC.6 TO PRESC.3	DIVISION FACTOR
TARGET	ACTUAL[1]			
115.2[2]	111.8608	1	0010	2 × 16 = 32
57.6	55.9304	0	0010	2 × 32 = 64
38.4	37.2869	0	0001	3 × 32 = 96
28.8	27.9652	0	0100	4 × 32 = 128
19.2	18.6435	0	0011	6 × 32 = 192
14.4	13.9826	0	0110	8 × 32 = 256
9.6	9.3217	0	0101	12 × 32 = 384
7.2	6.9913	0	1000	16 × 32 = 512
4.8	4.6609	0	0111	24 × 32 = 768
3.6	3.4956	0	1010[3]	32 × 32 = 1024
2.4	2.3304	0	1001	48 × 32 = 1536
1.2[4]	1.1652	0	1011[5]	96 × 32 = 3072

Notes

1. Error compared to the target values is less then 3%.
2. Maximum baud rate.
3. And also 1100 and 1110.
4. Minimum baud rate.
5. And also 1101 and 1111.

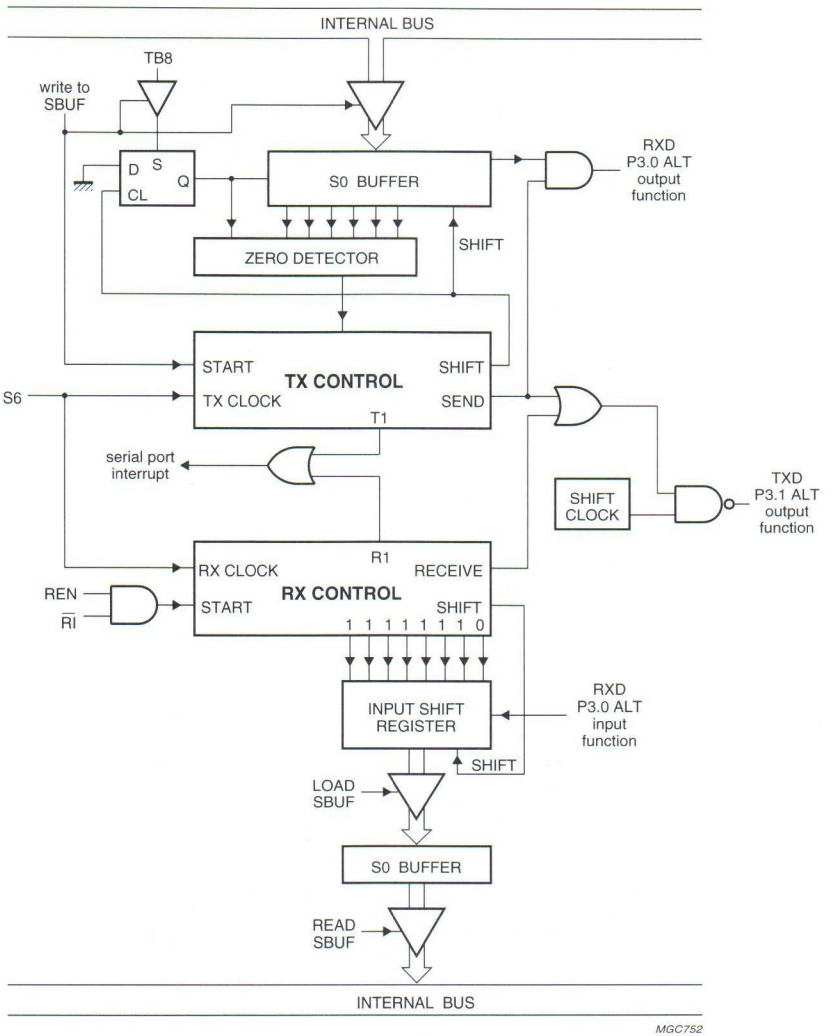


Fig.26 Serial port Mode 0.

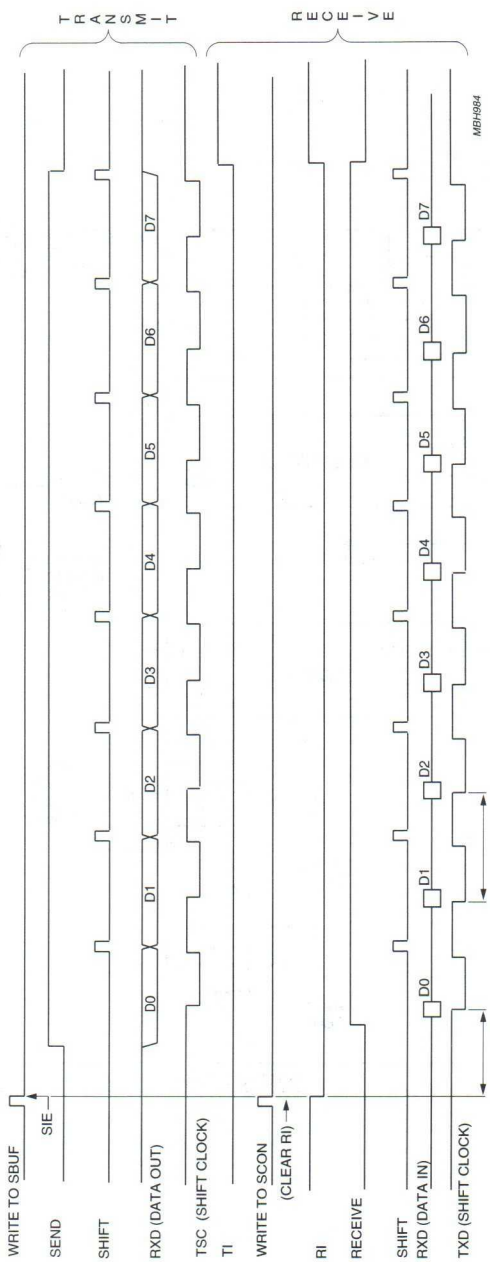


Fig.27 Serial port Mode 0 timing.

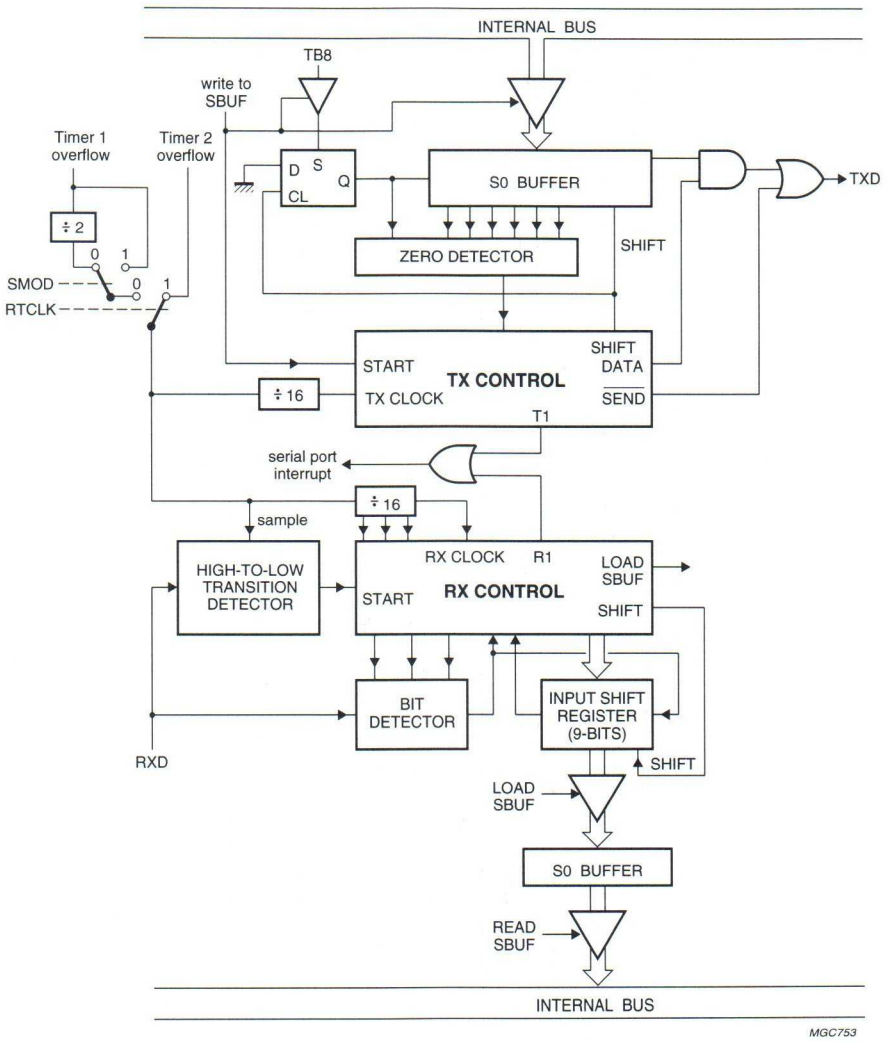


Fig.28 Serial port Mode 1.

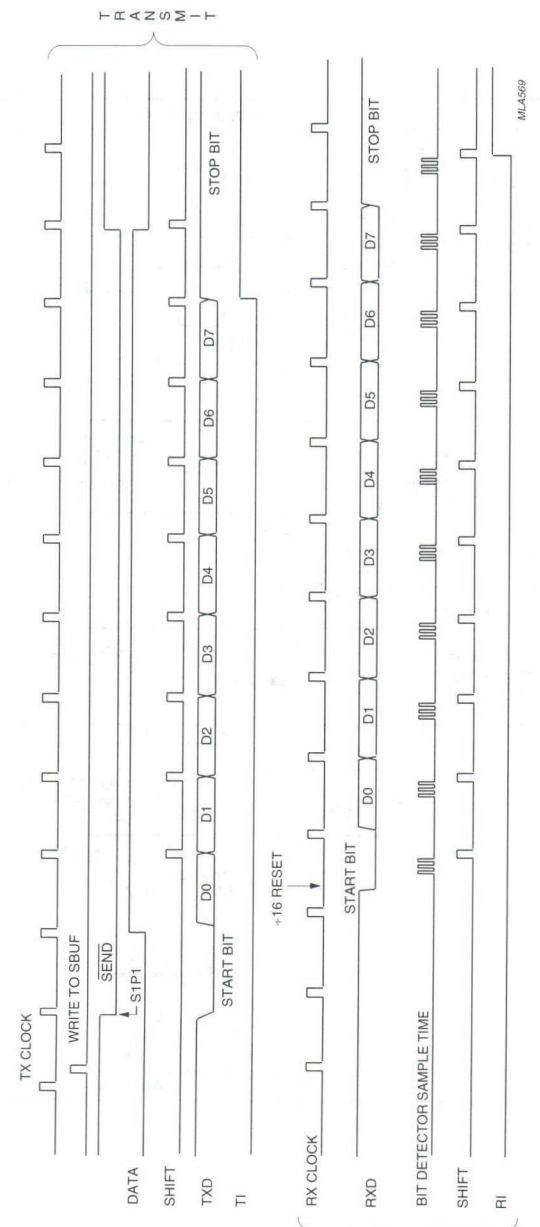


Fig.29 Serial port Mode 1 timing.

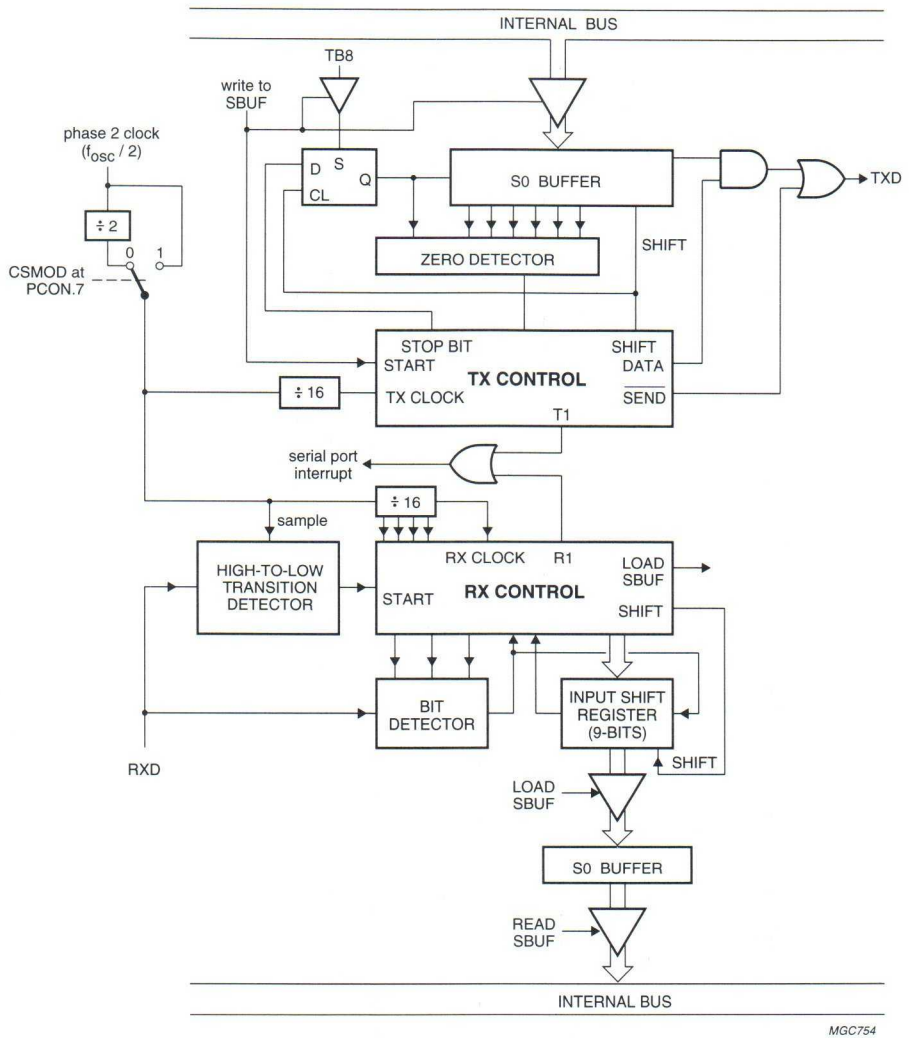


Fig.30 Serial port Mode 2.

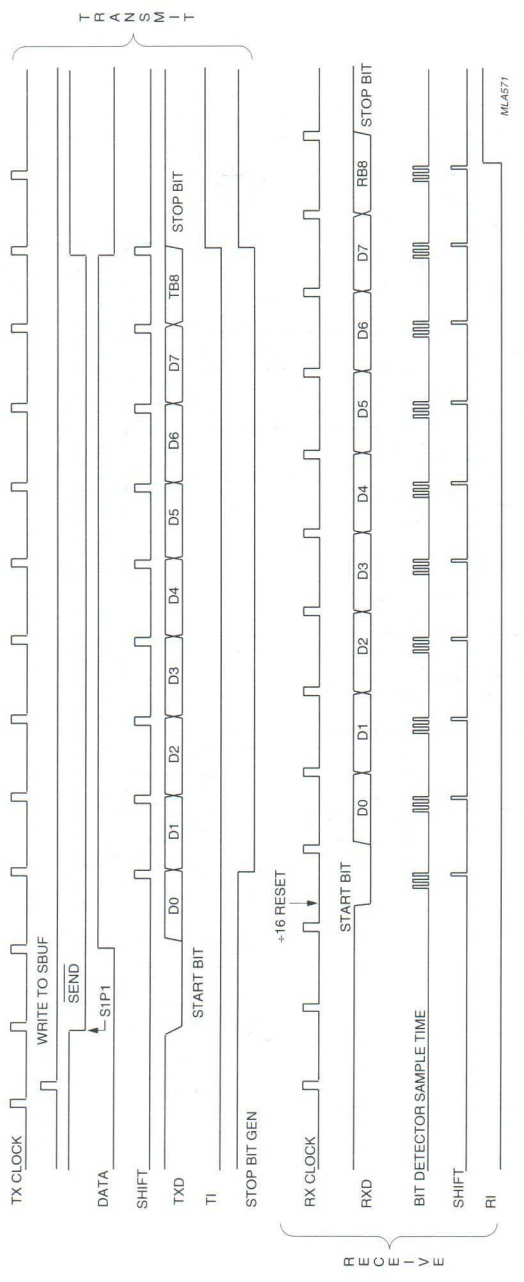


Fig.31 Serial port Mode 2 timing.

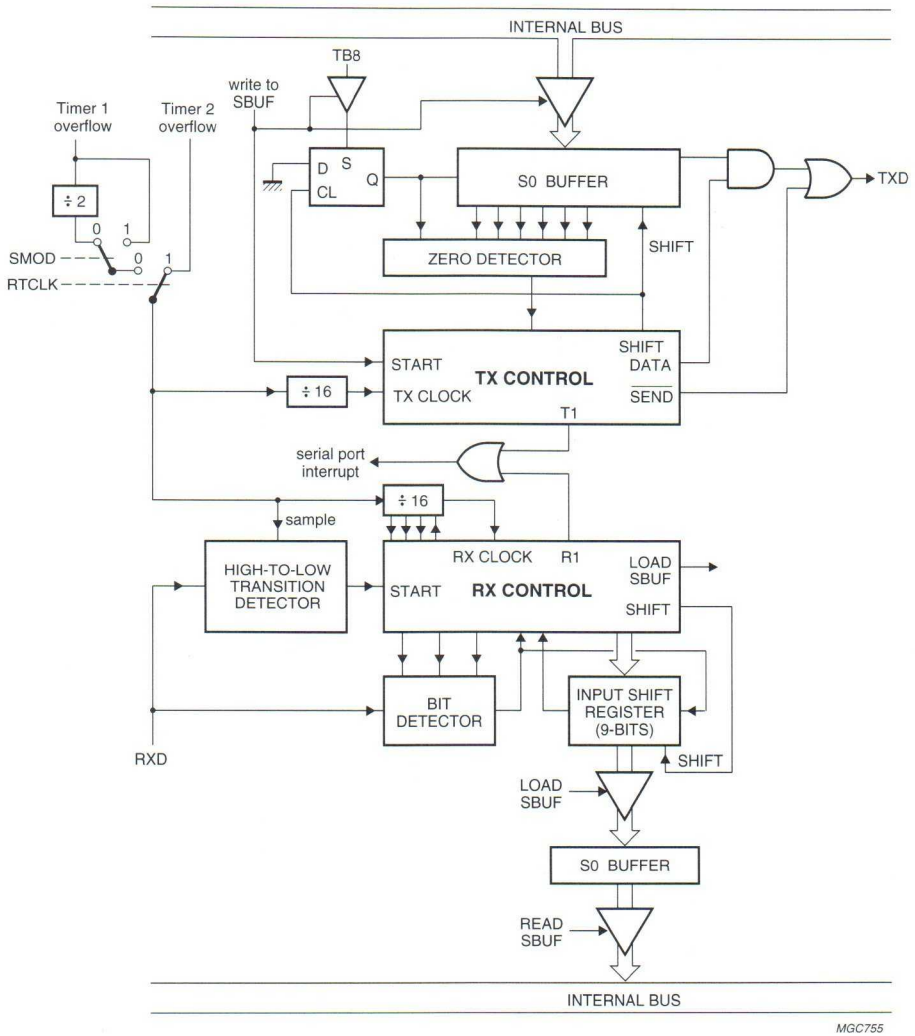


Fig.32 Serial port Mode 3.

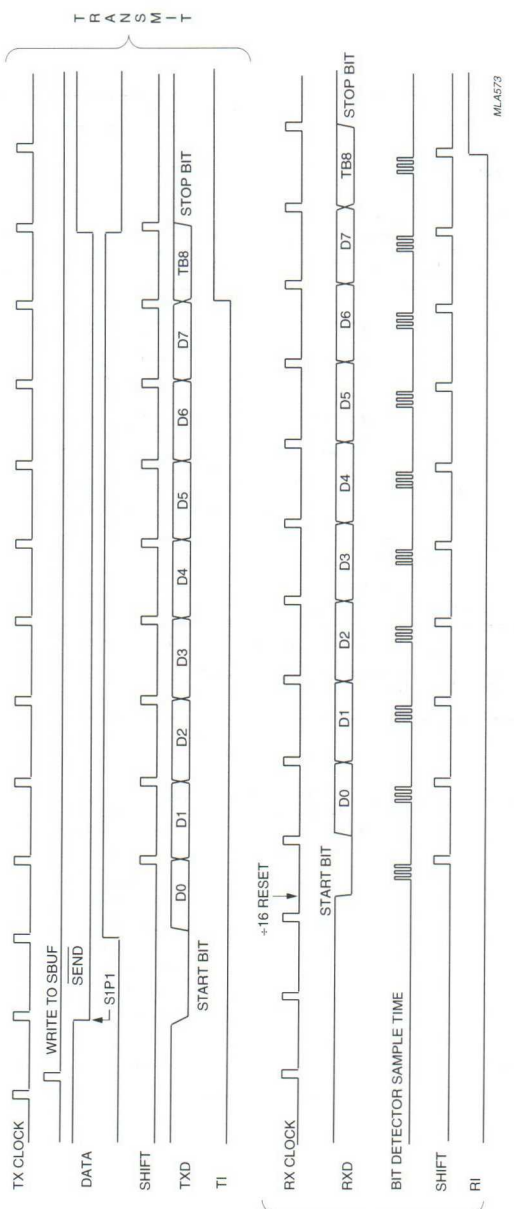


Fig.33 Serial port Mode 3 timing.

4.14 Interrupt system

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronously to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. The TELX family acknowledges interrupt requests from twenty sources:

- INT0 to INT9
- Timer 0, Timer 1 and Timer 2
- I²C-bus serial I/O
- UART transmitter and receiver
- MSK modem transmitter and receiver
- Low Voltage Detector
- 32 kHz Real-Time Clock.

Each interrupt vectors to a separate location in program memory for its service routine. Each source can be individually enabled or disabled by its corresponding bit in the Interrupt Enable Registers (IEN0 to IEN2). The priority level is selected via the Interrupt Priority Registers (IP0 to IP2). All enabled sources can be globally disabled or enabled. The interrupt system is shown in Fig.34.

4.14.1 External interrupts INT2 to INT9

Port 1 lines serve an alternative purpose as eight additional interrupts: INT2 to INT9. When enabled, each of these lines may wake-up the device from the Power-down mode.

Using the Interrupt Polarity Register (IX1) and the Interrupt Sensitivity Register (ISE1), each pin may be initialized to be either active HIGH, active LOW (i.e. level sensitive), or triggered on a rising or falling edge. A Port 1 level sensitive interrupt will be recognized when a level (HIGH or LOW depending on the Interrupt Polarity Register) on P1.n (n = 0 to 7) is held active for at least one machine cycle. The interrupt request is not serviced until the next machine cycle. The external interrupt configuration is shown in Fig.35.

IRQ1 is the Interrupt Request Flag Register. If the interrupt is enabled, each flag will be set on an interrupt request but must be cleared by software, i.e. via the interrupt software or when the interrupt is disabled by its corresponding bit in IE1. A global interrupt disable will disable the servicing of the interrupts however it does not reset an active interrupt request neither does it stop the detection of an interrupt condition.

4.14.2 Interrupt priority

Each interrupt source can be set to either a high priority or to a low priority. If both priorities are requested simultaneously, the processor will branch to the high priority vector. A low priority interrupt can only be interrupted by a high priority interrupt. A high priority interrupt routine can not be interrupted.

Table 64 shows the interrupt vectors in order of priority. X0 having the highest priority; RTC the lowest. The vector indicates the ROM location where the appropriate interrupt service routine starts.

Table 64 Interrupt vectors

SOURCE	SYMBOL	VECTOR (HEX)
External 0	X0	0003
I²C-bus port	S1	002B
External 5	X5	0053
MSK modem receiver	MRI	008B
Timer 0	T0	000B
Timer 2	T2	0033
External 6	X6	005B
MSK modem transmitter	MTI	0083
External 1	X1	0013
External 2	X2	003B
External 7	X7	0063
UART transmitter	SOT	007B
Timer 1	T1	001B
External 3	X3	0043
External 8	X8	006B
Low Voltage Detector	LVD	0093
UART receiver	SOR	0023
External 4	X4	004B
External 9	X9	0073
Real-Time Clock	RTC	009B

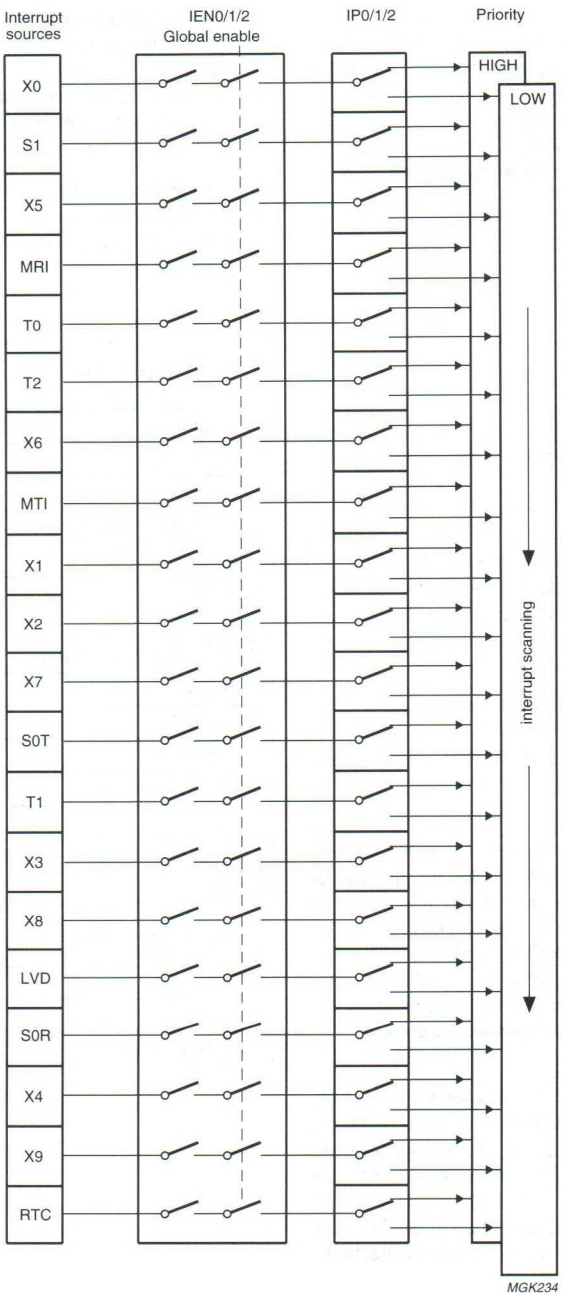


Fig.34 Interrupt system.

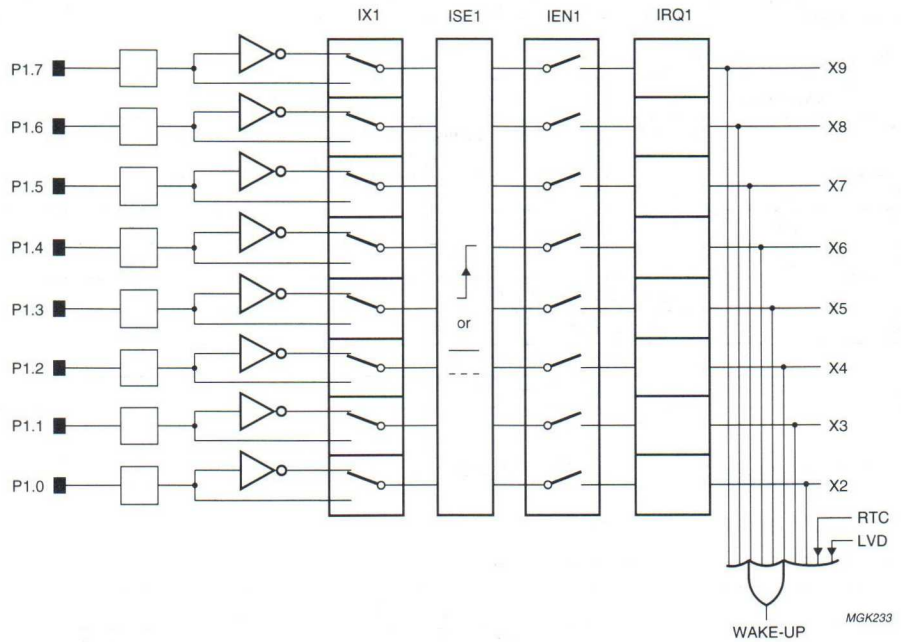


Fig.35 External interrupt configuration.

4.14.3 Interrupt Enable Register (IEN0)

Table 65 Interrupt Enable Register (SFR address A8H)

7	6	5	4	3	2	1	0
EA	ET2	ES1	ESOR	ET1	EX1	ET0	EX0

Table 66 Description of IEN0 bits

BIT[1]	SYMBOL	DESCRIPTION
IEN0.7	EA	General enable/disable control; if EA = 0, no interrupt is enabled; if EA = 1, any individually enabled interrupt will be accepted.
IEN0.6	ET2	enable T2 interrupt
IEN0.5	ES1	enable I^2C-bus interrupt
IEN0.4	ESOR	enable UART receiver interrupt
IEN0.3	ET1	enable Timer 1 interrupt (T1)
IEN0.2	EX1	enable external interrupt 1
IEN0.1	ET0	enable Timer 0 interrupt (T0)
IEN0.0	EX0	enable external interrupt 0

Note

1. Where: logic 0 = interrupt disabled; logic 1 = interrupt enabled.

4.14.4 Interrupt Enable Register (IEN1)

Table 67 Interrupt Enable Register (SFR address E8H)

7	6	5	4	3	2	1	0
EX9	EX8	EX7	EX6	EX5	EX4	EX3	EX2

Table 68 Description of IEN1 bits

BIT[1]	SYMBOL	DESCRIPTION
IEN1.7	EX9	enable external interrupt 9
IEN1.6	EX8	enable external interrupt 8
IEN1.5	EX7	enable external interrupt 7
IEN1.4	EX6	enable external interrupt 6
IEN1.3	EX5	enable external interrupt 5
IEN1.2	EX4	enable external interrupt 4
IEN1.1	EX3	enable external interrupt 3
IEN1.0	EX2	enable external interrupt 2

Note

1. Where: logic 0 = interrupt disabled; logic 1 = interrupt enabled.

4.14.5 Interrupt Enable Register (IEN2)

Table 69 Interrupt Enable Register (SFR address F1H)

7	6	5	4	3	2	1	0
–	–	–	ERTC	ELVD	ESOT	EMTI	EMRI

Table 70 Description of IEN2 bits

BIT[1]	SYMBOL	DESCRIPTION
IEN2.7	–	these 3 bits are reserved
IEN2.6	–	
IEN2.5	–	
IEN2.4	ERTC	enable RTC interrupt
IEN2.3	ELVD	enable Low Voltage Detector interrupt
IEN2.2	ESOT	enable UART transmitter interrupt
IEN2.1	EMTI	enable MSK modem transmitter interrupt
IEN2.0	EMRI	enable MSK modem receiver interrupt

Note

1. Where: logic 0 = interrupt disabled; logic 1 = interrupt enabled.

4.14.6 Interrupt Priority Register (IP0)

Table 71 Interrupt Priority Register (SFR address B8H)

7	6	5	4	3	2	1	0
–	PT2	PS1	PS0	PT1	PX1	PT0	PX0

Table 72 Description of IP0 bits

BIT[1]	SYMBOL	DESCRIPTION
IP0.7	–	Reserved
IP0.6	PT2	Timer 2 interrupt priority level
IP0.5	PS1	I^2C-bus interrupt priority level
IP0.4	PS0	UART SIO interrupt priority level
IP0.3	PT1	Timer 1 interrupt priority level
IP0.2	PX1	External interrupt 1 priority level
IP0.1	PT0	Timer 0 interrupt priority level
IP0.0	PX0	External interrupt 0 priority level

Note

1. Where: logic 0 = low priority; logic 1 = high priority.

4.14.7 Interrupt Priority Register (IP1)

Table 73 Interrupt Priority Register (SFR address F8H)

7	6	5	4	3	2	1	0
PX9	PX8	PX7	PX6	PX5	PX4	PX3	PX2

Table 74 Description of IP1 bits

BIT[1]	SYMBOL	DESCRIPTION
IP1.7	PX9	external interrupt 9 priority level
IP1.6	PX8	external interrupt 8 priority level
IP1.5	PX7	external interrupt 7 priority level
IP1.4	PX6	external interrupt 6 priority level
IP1.3	PX5	external interrupt 5 priority level
IP1.2	PX4	external interrupt 4 priority level
IP1.1	PX3	external interrupt 3 priority level
IP1.0	PX2	external interrupt 2 priority level

Note

1. Where: logic 0 = low priority; logic 1 = high priority.

4.14.8 Interrupt Priority Register (IP2)

Table 75 Interrupt Priority Register (SFR address F9H)

7	6	5	4	3	2	1	0
–	–	–	PRTC	PLVD	PS0T	PMTI	PMRI

Table 76 Description of IP2 bits

BIT[1]	SYMBOL	DESCRIPTION
IP2.7	–	These 3 bits are reserved
IP2.6	–	
IP2.5	–	
IP2.4	PRTC	RTC interrupt priority level
IP2.3	PLVD	Low Voltage Detector interrupt priority level
IP2.2	PS0T	UART transmitter interrupt priority level
IP2.1	PMTI	MSK modem transmitter interrupt priority level
IP2.0	PMRI	MSK modem receiver interrupt priority level

Note

1. Where: logic 0 = low priority; logic 1 = high priority.

4.14.9 Interrupt Polarity Register (IX1)

Writing either a logic 1 or logic 0 to any Interrupt Polarity Register bit sets the polarity level of the corresponding external interrupt to an active HIGH (rising edge) or active LOW (falling edge) respectively.

Table 77 Interrupt Polarity Register (SFR address E9H)

7	6	5	4	3	2	1	0
IX9	IX8	IX7	IX6	IX5	IX4	IX3	IX2

Table 78 Description of IX1 bits

BIT	SYMBOL	DESCRIPTION
IX1.7	IX9	external interrupt 9 polarity level
IX1.6	IX8	external interrupt 8 polarity level
IX1.5	IX7	external interrupt 7 polarity level
IX1.4	IX6	external interrupt 6 polarity level
IX1.3	IX5	external interrupt 5 polarity level
IX1.2	IX4	external interrupt 4 polarity level
IX1.1	IX3	external interrupt 3 polarity level
IX1.0	IX2	external interrupt 2 polarity level

4.14.10 Interrupt Sensitivity Register (ISE1)

Writing either a logic 1 or logic 0 to an Interrupt Sensitivity Register bit sets the type of the corresponding external interrupt to edge sensitive or level sensitive respectively.

Table 79 Interrupt Sensitivity Register (SFR address E1H)

7	6	5	4	3	2	1	0
ISE9	ISE8	ISE7	ISE6	ISE5	ISE4	ISE3	ISE2

Table 80 Description of ISE1 bits

BIT	SYMBOL	DESCRIPTION
ISE1.7	ISE9	external interrupt 9 sensitivity
ISE1.6	ISE8	external interrupt 8 sensitivity
ISE1.5	ISE7	external interrupt 7 sensitivity
ISE1.4	ISE6	external interrupt 6 sensitivity
ISE1.3	ISE5	external interrupt 5 sensitivity
ISE1.2	ISE4	external interrupt 4 sensitivity
ISE1.1	ISE3	external interrupt 3 sensitivity
ISE1.0	ISE2	external interrupt 2 sensitivity

4.14.11 Interrupt Request Flag Register (IRQ1)

Table 81 Interrupt Request Flag Register (SFR address C0H)

7	6	5	4	3	2	1	0
IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2

Table 82 Description of IRQ1 bits

BIT	SYMBOL	DESCRIPTION
IRQ1.7	IQ9	external interrupt 9 request flag
IRQ1.6	IQ8	external interrupt 8 request flag
IRQ1.5	IQ7	external interrupt 7 request flag
IRQ1.4	IQ6	external interrupt 6 request flag
IRQ1.3	IQ5	external interrupt 5 request flag
IRQ1.2	IQ4	external interrupt 4 request flag
IRQ1.1	IQ3	external interrupt 3 request flag
IRQ1.0	IQ2	external interrupt 2 request flag

4.14.12 Interrupt Related registers

The following registers are used in conjunction with the interrupt system.

Table 83 Interrupt Related registers

REGISTER	FUNCTION	SFR ADDRESS
IX1	Interrupt Polarity Register	E9H
ISE1	Interrupt Sensitivity Register	E1H
IRQ1	Interrupt Request Flag Register	C0H
IEN0	Interrupt Enable Register	A8H
IEN1	Interrupt Enable Register (INT2 to INT9)	E8H
IEN2	Interrupt Enable Register	E8H
IP0	Interrupt Priority Register	B8H
IP1	Interrupt Priority Register (INT2 to INT9)	F8H
IP2	Interrupt Priority Register	B8H

4.15 Idle and Power-down operation

Idle mode operation permits the interrupt, serial ports (UART and I²C-bus), serial interfaces, RTC and timer blocks to continue to function while the clock to the CPU is halted.

The following functions remain active during the Idle mode. These functions may generate an interrupt or reset; thus ending the Idle mode.

- Timer 0, Timer 1 and Timer 2
- UART and I²C-bus interface
- MSK modem
- External interrupts
- 32 kHz Real-Time Clock.

The Power-down operation stops the oscillator and reduces power consumption to a few micro-amps. This mode can only be activated by setting the PD bit in the PCON register or via the Low Voltage Detector. The Idle and Power-down clock configuration is shown in Fig.36.

4.15.1 IDLE MODE

The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before the Idle mode is activated. Once in the Idle mode, the CPU status is preserved along with the Stack Pointer, Program Counter, Program Status Word and Accumulator. The RAM and all other registers maintain their data during Idle mode.

There are two ways to terminate the Idle mode:

1. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware thus terminating the Idle mode. The interrupt is serviced, and following the RETI instruction, the next instruction to be executed will be the one following the instruction that put the device in the Idle mode. The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When the Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
2. The second way of terminating the Idle mode is with an external hardware reset, or an internal reset caused by an overflow of the Watchdog Timer. Since the oscillator is still running, the hardware reset is required to be active for two machine cycles (12 oscillator periods) to complete the reset operation. Reset redefines all SFRs but does not affect the on-chip RAM.

4.15.2 POWER-DOWN MODE

The instruction that sets PCON.1 is the last executed prior to going into the Power-down mode. Once in the Power-down mode, the oscillator is stopped. The contents of the on-chip RAM and the SFRs are preserved. The port pins output the value held in their respective SFRs. ALE is held LOW and $\overline{\text{PSEN}}$ is held HIGH.

The EEPROM should be switched off via register EECON before the Power-down mode is entered. Make sure not to enter the Power-down mode before a write or erase cycle is finished. For details on EEPROM operations, see Section 4.9.

The Power-down mode can also be entered and exited automatically by using the on-chip Low Voltage Detection circuit. This is described in Sections 4.18.2 and 4.18.3.

To reach lowest possible power consumption it is strongly recommended to write 00H in both the DTMF frequency registers HGF and LGF.

In the Power-down mode, V_{DD} may be reduced to minimize circuit power consumption. The supply voltage must not be reduced until the Power-down mode is entered, and must be restored before the hardware reset is applied which will free the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

4.15.3 WAKE-UP FROM POWER-DOWN MODE

Setting the PD flag in the PCON register forces the controller into the Power-down mode. Setting this flag enables the controller to be woken-up from the Power-down mode with either the external interrupts INT2 to INT9, a reset operation, the LVD or via the RTC.

4.15.3.1 *Wake-up using INT2 to INT9*

If any of the interrupts INT2 to INT9 are enabled, the device can be woken-up from the Power-down mode with the external interrupts. To ensure that the oscillator is stable before the controller restarts, the internal clock will remain inactive for either 32 or 1024 oscillator periods. The length of the delay is programmable via the DELS bit in the PCON register. The delay is generated by an on-chip delay counter. After reset, 1024 oscillator periods delay is the default setting.

4.15.3.2 *Wake-up using $\overline{RST}$*

If using the $\overline{RST}$ pin for Wake-up, refer to Section 4.17.1.

4.15.3.3 *Wake-up using LVD*

The Power-down mode can be entered and exited automatically by using the on-chip Low Voltage Detection circuit. This is described in detail in the Section 4.18.2.

4.15.3.4 *Wake-up using RTC*

The on-chip 32 kHz Real-Time Clock (RTC) can be used to wake-up the microcontroller periodically without reset. This is described in detail in Section 4.4.

4.15.4 STATUS OF EXTERNAL PINS

The status of the external pins during Idle and Power-down mode is shown in Table 84. If the Power-down mode is activated whilst accessing external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull-up transistor p1 (see Fig.5).

Table 84 Status of external pins during Idle and Power-down modes

MODE	MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	internal	1	1	port data	port data	port data	port data
Idle	external	1	1	weak pull-up	port data	address	port data
Power-down	internal	0	1	port data	port data	port data	port data
Power-down	external	0	1	weak pull-up	port data	port data	port data

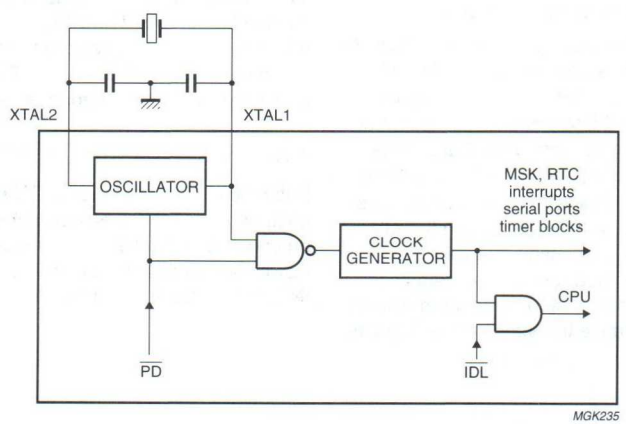


Fig.36 Internal Idle and Power-down clock configuration.

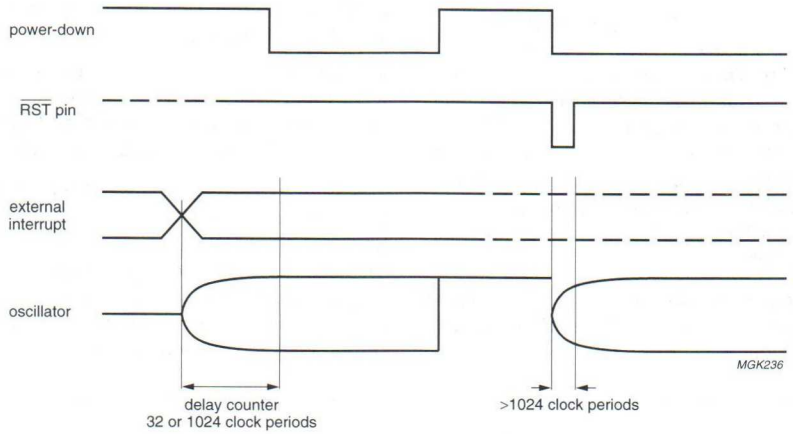


Fig.37 Wake-up operation.

4.15.5 Power Control Register (PCON)

The reduced power modes are activated by software using this Special Function Register. PCON is not bit addressable.

Table 85 Power Control Register (SFR address 87H)

7	6	5	4	3	2	1	0
SMOD	ARD	RFI	DELS	GF1	GF0	PD	IDL

Table 86 Description of PCON bits

BIT	SYMBOL	DESCRIPTION
PCON.7	SMOD	**Double Baud rate.** When set to a logic 1 the baud rate is doubled when the serial port SIO0 is being used in Modes 1, 2 or 3.
PCON.6	ARD	**AUX-RAM disable.** When ARD = 1, the internal AUX-RAM is disabled and all MOVX instructions access the external data memory - as it is with the standard PCB80C51.
PCON.5	RFI	**Reduced Radio Frequency Interference.** When set to a logic 1 the toggling of ALE pin is prohibited; this bit is cleared on reset.
PCON.4	DELS	**Delay Short.** To ensure that the oscillator is stable before the controller restarts after wake-up from power-down, the internal clock will remain inactive for either 32 or 1024 oscillator periods. DELS = 0 means a delay of 1024 clock periods (default at reset), DELS = 1 means a delay of 32 clock periods.
PCON.3	GF1	**General Purpose Flag bit.**
PCON.2	GF0	**General Purpose Flag bit.**
PCON.1	PD	**Power-down.** Setting this bit activates the Power-down mode; see note 1.
PCON.0	IDL	**Idle mode.** Setting this bit activates the Idle mode; see note 1.

Note

1. If logic 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (0XX00000).

4.16 Oscillator circuitry

The on-chip amplitude controlled oscillator circuitry is a single-stage inverting amplifier biased by an internal feedback resistor R_{fb}. The oscillator circuit is shown in Fig.38. When using a quartz crystal to drive the oscillator, no external components are needed. When using an external ceramic resonator to drive the oscillator, external components may be required depending upon the ceramic resonator specifications (refer to specific product specification). Two different configurations are shown in Fig.39(a) and Fig.39(b).

To drive the device with an external clock source, apply the external clock signal to XTAL1, and leave XTAL2 to float, as shown in Fig.39(c).

If the amplitude of the input signal is less than V_{DD} to V_{SS} or a sine wave is applied, capacitive decoupling is needed as shown in Fig.39(d).

In the Power-down mode the oscillator is stopped and XTAL1 and XTAL2 are internally pulled LOW. The current of the whole oscillator is switched off (signals ENABLECUR and ENABLECLK are inactive).

The system clock can be made available on a port pin by setting the ECLK bit in the ALTP register (see Section 4.10.4). This is useful in applications where the system clock of the microcontroller is used to clock other ICs. In this case the port latch of the port pin should be set to a logic 1 in order to avoid conflict between the system clock output and the port output.

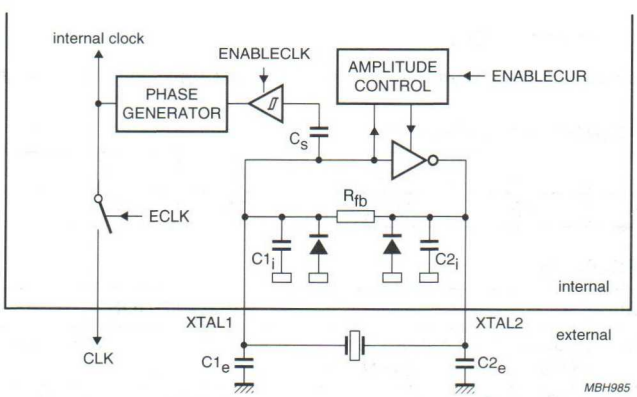


Fig.38 Oscillator.

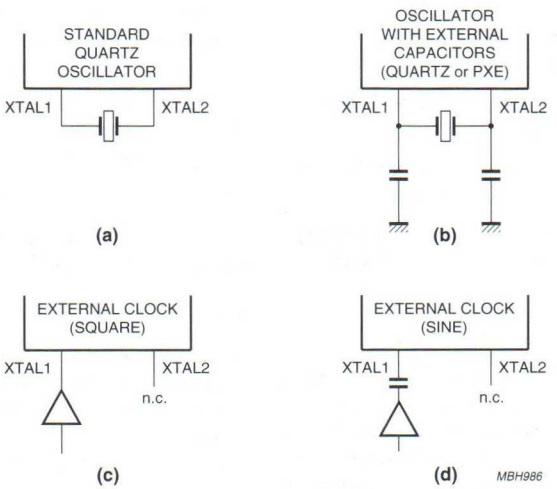


Fig.39 Alternative oscillator configurations.

4.17 Reset

To initialize the TELX microcontroller a reset is performed by one of three methods:

- Applying an external signal to the $\overline{RST}$ pin
- Via internal Power-on reset circuitry
- Via the on-chip Watchdog Timer.

The state of the port pins after a reset is given in the respective product specification.

The $\overline{RST}$ pin can function as an input or output pin. As an output pin it can be used to reset other IC's.

The internal RAM and the EEPROM are not affected by reset. When V_{DD} is turned on, the RAM contents are indeterminate.

4.17.1 External reset using the $\overline{RST}$ pin

The external reset input for the TELX microcontroller is the $\overline{RST}$ pin, it is asynchronous to the internal clock. A Schmitt trigger is used at the input for noise rejection. Immediately after the $\overline{RST}$ goes LOW the CPU responds by executing an internal reset, the SFRs and port pins adopt their reset state, ALE and $\overline{PSEN}$ are held HIGH. As long as $\overline{RST}$ pin remains LOW, the slot generator is halted at timeslot 1 and the reset state is maintained. When $\overline{RST}$ goes HIGH, the slot generator is started and program execution starts after 2 machine cycles.

4.17.2 External Power-on reset using the $\overline{RST}$ pin

An automatic reset can be obtained by connecting the $\overline{RST}$ pin to V_{SS} via a capacitor. At power-on, the voltage on the $\overline{RST}$ pin is equal to V_{SS} and increases from V_{SS} as the capacitor charges through the internal resistor (R_{RST}) to V_{DD}. V_{RST} must remain below the higher threshold of the Schmitt trigger long enough for the oscillator to become stable. The time required is approximately 1024 oscillator periods. The reset configuration is shown in Fig.40.

4.17.3 Internal Power-on/Power-off reset (POR)

The device contains an on-chip Power-on-reset circuit which activates a reset as long as V_{DD} is below a predefined level (V_{PORH}). If V_{DD} exceeds V_{PORH}, the oscillator will start-up. However, to ensure that the oscillator is stable before the controller starts, the clock signals are gated away from the CPU for 1024 oscillator periods.After this delay the slot generator is started and program execution starts after 2 machine cycles.

The Power-on-reset circuit also ensures, that the microcontroller will be switched-off as soon as a second predefined level (V_{PORL}) is reached as V_{DD} decreases.

The on-chip POR circuit can also be switched off by connecting the PORACTIVE pin to V_{SS}. This reduces the Power-down current even further and can be chosen if external reset circuitry is used.

If the POR signal is active, the $\overline{RST}$ pin will be pulled LOW.

The state of internal registers after a reset are given in the product specifications.

4.17.4 Trip points of POR (Power-On/Off-Reset)

At power-up or at varying supply voltage, the POR circuit will ensure that the microcontroller is reset correctly at predefined levels. The POR trip points are defined as follows:

- POR trip level HIGH (V_{PORH}). When this level is reached at rising V_{DD}, the internal reset signal is deactivated (oscillator released and CPU released after a delay of 1024 or 32 clock periods).
- POR trip level LOW (V_{PORL}). When this level is reached at falling V_{DD}, the internal reset signal is activated (oscillator stopped).

The minimum V_{DD} for the microcontroller depends on the clock frequency used.

Eight different voltages for trip level HIGH (V_{PORH}) can be chosen. The hysteresis $V_{PORH} - V_{PORL}$ can be chosen either to be fixed at a level relative to V_{PORH}, typically 100 mV (so V_{PORL} will be $V_{PORH} - 100$ mV), or at a very low value typically at 1.3 V. Any combination of a V_{PORH} option and a hysteresis option can be chosen. The chosen option for the trip levels and the type of hysteresis can be checked by reading the Reset Status Register (RSTAT); see Section 4.17.5.

The hysteresis option with $V_{PORL} = 1.3$ V is foreseen for the case when no reset is wanted when V_{DD} is decreasing below minimum V_{DD} (operating) but still being above minimum V_{DD} (RAM retention).

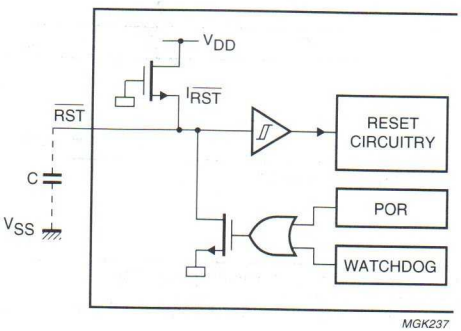


Fig.40 Reset configuration.

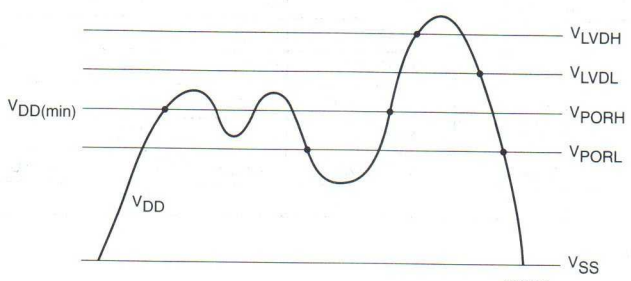


Fig.41 Power-on reset switching level.

4.17.5 Reset Status Register (RSTAT)

This 8-bit register gives the chosen reset option for the POR circuit and for the on-chip oscillator.

Table 87 Reset Status register RSTAT (SFR address E6H)

7	6	5	4	3	2	1	0
–	–	–	O3	O2	O1	O0	GMH

Table 88 Description of RSTAT bits

BIT	SYMBOL	DESCRIPTION
RSTAT.7	–	These 3-bits are not used.
RSTAT.6	–	
RSTAT.5	–	
RSTAT.4	O3	This bit defines the hysteresis of the POR.
RSTAT.3	O2	These 3-bits define the high trip point of the POR; see Table 89.
RSTAT.2	O1	
RSTAT.1	O0	
RSTAT.0	GMH	This bit reflects the chosen transconductance of the on-chip oscillator; its value should not be changed, since this could affect the behaviour of the oscillator

Table 89 POR trip points

PARAMETER	OPTION	RSTAT CONTENTS	MIN.	TYP.	MAX.	UNIT
Accuracy of V_{PORH}			–10		10	%
Trip level HIGH (V_{PORH})	Option 1	XXXX 000X	1.75	1.94	2.13	V
	Option 2	XXXX 001X	1.84	2.04	2.24	V
	Option 3	XXXX 010X	1.94	2.15	2.37	V
	Option 4	XXXX 011X	2.03	2.26	2.49	V
	Option 5	XXXX 100X	2.13	2.37	2.61	V
	Option 6	XXXX 101X	2.42	2.69	2.96	V
	Option 7	XXXX 110X	2.52	2.80	3.08	V
	Option 8	XXXX 111X	2.61	2.90	3.19	V
Trip level LOW (V_{PORL})	Option A	XXX0 XXXX	V_{PORH} – 0.15	V_{PORH} – 0.10	V_{PORH} – 0.05	V
	Option B	XXX1 XXXX	–	1.30	–	V

4.17.6 Internal Reset via the Watchdog

The Watchdog which is available on the $\overline{RST}$ pin is described in Section 4.8.3.

4.18 Low Voltage Detection

The Low Voltage Detection (LVD) is a feature which can be used to determine if a certain voltage level of V_{DD} has been reached, e.g. low voltage warning for EEPROM or DTMF operation, or for normal operation. The LVD is programmed by software via the LVD Control Register (LVDCON).

An active output from the Low Voltage Detection block will set the LVDI bit in the LVD Control Register, this can be detected by software, and an internal interrupt will be generated providing the ELVD bit in the IEN2 register is set. The LVDI bit must be reset by software. The LVD interrupt can be activated on a rising or falling edge of V_{DD}. The selection is made using the LVDX bit in the LVDCON register.

The state of the LVD signal is indicated by the LVDS bit in LVDCON. LVDS can only be read.

The LVD can also be used to enter and exit the Power-down mode automatically without first setting the PD bit in the PCON register. This feature is further described in Section 4.18.2.

Programming of the LVD trip points is done by software for both the OTP and ROM versions, via the LVDCON register. The trip levels can be changed any time during program execution. Ten different options for the high trip level (V_{LVDH}) plus an option 'Off' for power saving are offered. The hysteresis between the high and low trip points ($V_{LVDH} - V_{LVDL}$) is typically 100 mV. The various options are listed in Table 92.

The variation of the different trip points for POR and LVD are related as both blocks use the same on-chip bandgap reference. The levels of the POR and LVD trip points should be programmed to be in the following order: $V_{LVDH} > V_{LVDL} > V_{PORH} > V_{PORL}$ (refer to Fig.41).

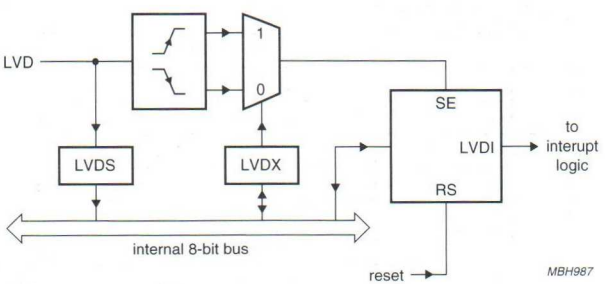


Fig.42 LVD interrupt logic.

4.18.1 LVD Control Register (LVDCON)

Table 90 LVD Control Register (SFR address F2H)

7	6	5	4	3	2	1	0
LVDPEN	LVDI	LVDX	LVDS	SEL3	SEL2	SEL1	SEL0

Table 91 Description of LVDCON bits

BIT	SYMBOL	DESCRIPTION
LVDCON.7	LVDPEN	**LVD Power-down enable.**
LVDCON.6	LVDI	**LVD Interrupt Flag.** Set by hardware, reset by software.
LVDCON.5	LVDX	**LVD Polarity Flag.** If LVDX = 0, then the LVD interrupt is activated on the falling edge of V_{DD}. If LVDX = 1, then the LVD interrupt is activated on the rising edge of V_{DD}. See Fig.42.
LVDCON.4	LVDS	**LVD Status.** read only; see Fig.42
LVDCON.3	SEL3	**Select option.** These 4-bits select the LVD trip level option; see Table 92.
LVDCON.2	SEL2	
LVDCON.1	SEL1	
LVDCON.0	SEL0	

Table 92 Selection and levels of the LVD trip points

PARAMETER	SEL3	SEL2	SEL1	SEL0	OPTION	MIN.	TYP.	MAX.	UNIT
Accuracy of V_{LVDH}	–	–	–	–	–	–10	–	+10	%
Trip level HIGH (V_{LVDH})	0	0	0	0	Option 0	Off	Off	Off	
	0	0	0	1	Option 1	1.75	1.94	2.13	V
	0	0	1	0	Option 2	1.84	2.04	2.24	V
	0	0	1	1	Option 3	1.94	2.15	2.37	V
	0	1	0	0	Option 4	2.03	2.26	2.49	V
	0	1	0	1	Option 5	2.13	2.37	2.61	V
	0	1	1	0	Option 6	2.22	2.47	2.72	V
	0	1	1	1	Option 7	2.32	2.58	2.84	V
	1	0	0	0	Option 8	2.42	2.69	2.96	V
	1	0	0	1	Option 9	2.52	2.80	3.08	V
	1	0	1	0	Option 10	2.61	2.90	3.19	V
Trip level LOW (V_{LVDL})	–	–	–	–	–	V_{LVDH} – 0.15	V_{LVDH} – 0.10	V_{LVDH} – 0.05	V

4.18.2 Entering and exiting Power-down mode automatically using LVD.

The TELX family offers the feature of entering the Power-down mode automatically, without any external voltage detector, see Fig.43. If the LVDPEN bit in the LVDCON register is set, the TELX microcontroller will enter the Power-down mode automatically as soon as the low LVD trip level (V_{LVDL}) is reached when the supply voltage decreases. This is useful when the Power-down mode must be entered quickly before the $V_{DD(min)}$ level is reached.

The trip point for V_{LVDL} is set by software as described in Section 4.18. Exit from Power-down mode is done either via a reset, or when the high LVD trip level (V_{LVDH}) is reached when the supply voltage rises.

4.18.3 Entering and exiting Power-down mode explicitly, using an LVD interrupt.

The Power-down mode can also be entered via an interrupt generated by the LVD and a corresponding interrupt software routine. In the interrupt routine, actions such as saving data in EEPROM or displaying a warning could be taken before entering the Power-down mode by setting LVDPEN. If V_{DD} rises above V_{LVDH}, the microcontroller exits the Power-down mode and resumes program execution inside the interrupt routine, see Fig.44.

Note that the next instruction after setting the LVDPEN bit will be executed before the microcontroller enters the Power-down mode. If this is not wanted, a NOP instruction should be inserted directly after the instruction setting the LVDPEN bit.

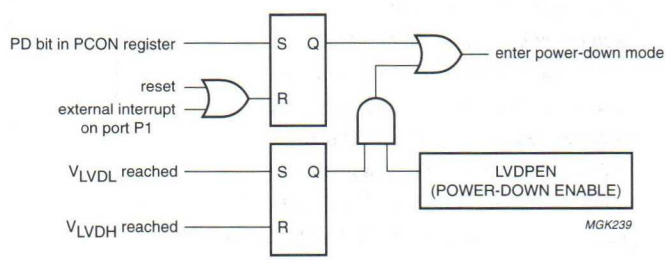


Fig.43 Power-down mode entry.

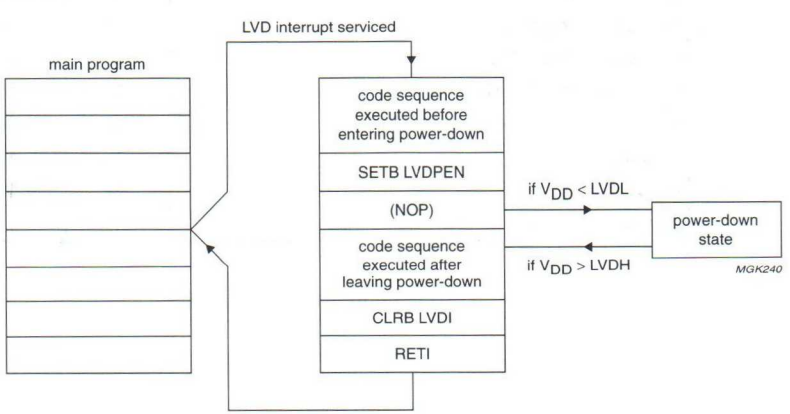


Fig.44 Power-down entry via interrupt.

5 INSTRUCTION SET

The TELX Family uses a powerful instruction set which permits the expansion of on-chip CPU peripherals and optimizes byte efficiency and execution speed. Assigned opcodes add new high-power operation and permit new addressing modes. The instruction set consists of 49 single-byte, 46 two-byte and 16 three-byte instructions. When using a 3.58 MHz oscillator, 64 instructions execute in 1.68 μs and 45 instructions execute in 3.35 μs. Multiply and divide instructions execute in 6.70 μs.

Table 93 Instruction Set

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Arithmetic operations					
ADD	A, Rr	add register to A	1	1	2*
ADD	A, direct	add direct byte to A	2	1	25
ADD	A, @Ri	add indirect RAM to A	1	1	26, 27
ADD	A, #data	add immediate data to A	2	1	24
ADDC	A, Rr	add register to A with carry flag	1	1	3*
ADDC	A, direct	add direct byte to A with carry flag	2	1	35
ADDC	A, @Ri	add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A, #data	add immediate data to A with carry flag	2	1	34
SUBB	A, Rr	subtract register from A with borrow	1	1	9*
SUBB	A, direct	subtract direct byte from A with borrow	2	1	95
SUBB	A, @Ri	subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A, #data	subtract immediate data from A with borrow	2	1	94
INC	A	increment A	1	1	04
INC	Rr	increment register	1	1	0*
INC	direct	increment direct byte	2	1	05
INC	@Ri	increment indirect RAM	1	1	06, 07
DEC	A	decrement A	1	1	14
DEC	Rr	decrement register	1	1	1*
DEC	direct	decrement direct byte	2	1	15
DEC	@Ri	decrement indirect RAM	1	1	16, 17
INC	DPTR	increment data pointer	1	2	A3
MUL	AB	multiply A and B	1	4	A4
DIV	AB	divide A by B	1	4	84
DA	A	decimal adjust A	1	1	D4

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Logic operations					
ANL	A, Rr	AND register to A	1	1	5*
ANL	A, direct	AND direct byte to A	2	1	55
ANL	A, @Ri	AND indirect RAM to A	1	1	56, 57
ANL	A, #data	AND immediate data to A	2	1	54
ANL	direct, A	AND A to direct byte	2	1	52
ANL	direct, #data	AND immediate data to direct byte	3	2	53
ORL	A, Rr	OR register to A	1	1	4*
ORL	A, direct	OR direct byte to A	2	1	45
ORL	A, @Ri	OR indirect RAM to A	1	1	46, 47
ORL	A, #data	OR immediate data to A	2	1	44
ORL	direct, A	OR A to direct byte	2	1	42
ORL	direct, #data	OR immediate data to direct byte	3	2	43
XRL	A, Rr	exclusive-OR register to A	1	1	6*
XRL	A, direct	exclusive-OR direct byte to A	2	1	65
XRL	A, @Ri	exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A, #data	exclusive-OR immediate data to A	2	1	64
XRL	direct, A	exclusive-OR A to direct byte	2	1	62
XRL	direct, #data	exclusive-OR immediate data to direct byte	3	2	63
CLR	A	clear A	1	1	E4
CPL	A	complement A	1	1	F4
RL	A	rotate A left	1	1	23
RLC	A	rotate A left through the carry flag	1	1	33
RR	A	rotate A right	1	1	03
RRC	A	rotate A right through the carry flag	1	1	13
SWAP	A	swap nibbles within A	1	1	C4

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Data transfer					
MOV	A, Rr	move register to A	1	1	E*
MOV	A, direct**	move direct byte to A	2	1	E5
MOV	A, @Ri	move indirect RAM to A	1	1	E6, E7
MOV	A, #data	move immediate data to A	2	1	74
MOV	Rr, A	move A to register	1	1	F*
MOV	Rr, direct	move direct byte to register	2	2	A*
MOV	Rr, #data	move immediate data to register	2	1	7*
MOV	direct, A	move A to direct byte	2	1	F5
MOV	direct, Rr	move register to direct byte	2	2	8*
MOV	direct, direct	move direct byte to direct byte	3	2	85
MOV	direct, @Ri	move indirect RAM to direct byte	2	2	86, 87
MOV	direct, #data	move immediate data to direct byte	3	2	75
MOV	@RI, A	move A to indirect RAM	1	1	F6, F7
MOV	@Ri, direct	move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri, #data	move immediate data to indirect RAM	3	1	76, 77
MOV	DPTR, #data 16	load data pointer with a 16-bit constant	3	2	90
MOVC	A, @A + DPTR	move code byte relative to DPTR to A	1	2	93
MOVC	A, @A + PC	move code byte relative to PC to A	1	2	83
MOVX	A, @Ri	move external RAM (8-bit address) to A	1	2	E2, E3
MOVX	A, @DPTR	move external RAM (16-bit address) to A	1	2	E0
MOVX	@Ri, A	move A to external RAM (8-bit address)	1	2	F2, F3
MOVX	@DPTR, A	move A to external RAM (16-bit address)	1	2	F0
PUSH	direct	push direct byte onto stack	2	2	C0
POP	direct	pop direct byte from stack	2	2	D0
XCH	A, Rr	exchange register with A	1	1	C*
XCH	A, direct	exchange direct byte with A	2	1	C5
XCH	A, @Ri	exchange indirect RAM with A	1	1	C6, C7
XCHD	A, @Ri	exchange LOW-order nibble indirect RAM with A	1	1	D6, D7

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Boolean variable manipulation					
CLR	C	clear carry flag	1	1	C3
CLR	bit	clear direct bit	2	1	C2
SETB	C	set carry flag	1	1	D3
SETB	bit	set direct bit	2	1	D2
CPL	C	complement carry flag	1	1	B3
CPL	bit	complement direct bit	2	1	B2
ANL	C, bit	AND direct bit to carry flag	2	2	82
ANL	C, /bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C, bit	OR direct bit to carry flag	2	2	72
ORL	C, /bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C, bit	move direct bit to carry flag	2	1	A2
MOV	bit, C	move carry flag to direct bit	2	2	92
Program and machine control					
ACALL	addr11	absolute subroutine call	2	2	•1 addr
LCALL	addr16	long subroutine call	3	2	12
RET		return from subroutine	1	2	22
RETI		return from interrupt	1	2	32
AJMP	addr11	absolute jump	2	2	♦1 addr
LJMP	addr16	long jump	3	2	02
SJMP	rel	short jump (relative address)	2	2	80
JMP	@A + DPTR	jump indirect relative to the DPTR	1	2	73
JZ	rel	jump if A is zero	2	2	60
JNZ	rel	jump if A is not zero	2	2	70
JC	rel	jump if carry flag is set	2	2	40
JNC	rel	jump if carry flag is not set	2	2	50
JB	bit, rel	jump if direct bit is set	3	2	20
JNB	bit, rel	jump if direct bit is not set	3	2	30
JBC	bit, rel	jump if direct bit is set and clear bit	3	2	10
CJNE	A, direct, rel	compare direct to A and jump if not equal	3	2	B5
CJNE	A, #data, rel	compare immediate to A and jump if not equal	3	2	B4
CJNE	Rr, #data, rel	compare immediate to register and jump if not equal	3	2	B*
CJNE	@Ri, #data, rel	compare immediate to indirect and jump if not equal	3	2	B6, B7
DJNZ	Rr, rel	decrement register and jump if not zero	2	2	D*
DJNZ	direct, rel	decrement direct and jump if not zero	3	2	D5
NOP		no operation	1	1	00

Table 94 Notation for data addressing modes

SYMBOL	DESCRIPTION
Rr	working registers R0 to R7
direct	128 internal RAM locations and any special function register (SFR)
@Ri	indirect internal RAM location addressed by register R0 or R1
#data	8-bit constant included in instruction
#data 16	16-bit constant included as bytes 2 and 3 of instruction
bit	direct addressed bit in internal RAM or SFR
addr16	16-bit destination address; used by LCALL and LJMP; the branch will be anywhere within the 64 kbyte program memory address space
addr11	11-bit destination address; used by ACALL and AJMP; the branch will be within the same 2 kbyte page of program memory as the first byte of the following instruction
rel	signed (two's complement) 8-bit offset byte; used by SJMP and all conditional jumps. Range is −128 to +127 bytes relative to first byte of the following instruction

Table 95 Hexadecimal opcode cross-reference

SYMBOL	DESCRIPTION
*	8, 9, A, B, C, D, E, F.
•	11, 31, 51, 71, 91, B1, D1, F1.
♦	01, 21, 41, 61, 81, A1, C1, E1.

5.1 Instruction Map

first hexadecimal character of opcode

second hexadecimal character of opcode

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr 11	LJMP addr 16	RR A	INC A	INC dir	INC @ Ri					INC Rr				
1	JBC bit, rel	ACALL addr 11	LCALL addr 16	RRC A	DEC A	DEC dir	DEC @ Ri					DEC Rr				
2	JB bit, rel	AJMP addr 11	RET	RL A	ADD A, # data	ADD A, dir	ADD A, @ Ri					ADD A, Rr				
3	JNB bit, rel	ACALL addr 11	RETI	RLC A	ADDC A, # data	ADDC A, dir	ADDC A, @ Ri					ADDC A, Rr				
4	JC rel	AJMP addr 11	ORL dir, A	ORL dir, # data	ORL A, # data	ORL A, dir	ORL A, @ Ri					ORL A, Rr				
5	JNC rel	ACALL addr 11	ANL dir, A	ANL dir, # data	ANL A, # data	ANL A, dir	ANL A, @ Ri					ANL A, Rr				
6	JZ rel	AJMP addr 11	XRL dir, A	XRL dir, # data	XRL A, # data	XRL A, dir	XRL A, @ Ri					XRL A, Rr				
7	JNZ rel	ACALL addr 11	ORL C, bit	JMP @ A+DPTR	MOV A, # data	MOV dir, # data	MOV @ Ri, # data					MOV Rr, # data				
8	SJMP rel	AJMP addr 11	ANL C, bit	MOVC A, @ A+PC	DIV AB	MOV dir, dir	MOV dir, @ Ri					MOV dir, Rr				
9	MOV DPTR, # data 16	ACALL addr 11	MOV bit, C	MOVC A, @ A+DPTR	SUBB A, # data	SUBB A, dir	SUBB A, @ Ri					SUBB A, Rr				
A	ORL C, / bit	AJMP addr 11	MOV bit, C	INC DPTR	MUL AB		MOV @ Ri, dir					MOV Rr, dir				
B	ANL C, / bit	ACALL addr 11	CPL bit	CPL C	CJNE A, # data, rel	CJNE A, dir, rel	CJNE @ Ri, # data, rel					CJNE Rr, # data, rel				
C	PUSH dir	AJMP addr 11	CLR bit	CLR C	SWAP A	XCH A, dir	XCH A, @ Ri					XCH A, Rr				
D	POP dir	ACALL addr 11	SETB bit	SETB C	DA A	DJNZ dir, rel	XCHD A, @ Ri					DJNZ Rr, rel				
E	MOVX A, @ DPTR	AJMP addr 11	MOVX A, @ Ri 0 1		CLR A	MOV * A, dir	MOV A, @ Ri					MOV A, Rr				
F	MOVX @ DPTR, A	ACALL addr 11	MOVX @ Ri, A 0 1		CPL A	MOV dir, A	MOV @ Ri, A					MOV Rr, A				

* MOV A, ACC is not a valid instruction.

MLA632 - 1

TELX microcontrollers for CT0 handsets/basestation applications

P83CL883; P87CL883; P83CL884; P87CL884

FEATURES

- Full static 80C51 CPU; enhanced 8-bit architecture with:
  - minimum 6 cycles per instruction (twice as fast as a standard 80C51 core)
  - non-page oriented instructions
  - direct addressing
  - four 8-byte RAM register banks
  - stack depth limited only by available internal RAM (maximum 256 bytes)
  - multiply, divide, subtract and compare instructions
- 8-bit ports:
  - P83CL883 and P87CL883: 3 (19 I/O lines)
  - P83CL884 and P87CL884: 3 (18 I/O lines)
- Program Memory:
  - P87CL883/P87CL884: 8 kbytes One Time Programmable (OTP)
  - P83CL883/P83CL884: 8 kbytes ROM
- 256 bytes RAM
- 128 bytes EEPROM Data Memory, accessed internally via I²C-bus interface (P83CL884 and P87CL884 only)
- Amplitude Controlled Oscillator (ACO) suitable for quartz crystal or ceramic resonator
- Improved Power-on/Power-off reset (POR) circuitry
- Low Voltage Detection (LVD) with 11 software programmable levels
- Eight interrupts on Port 1:
  - edge or level sensitive triggering selectable via software
  - power-saving use for keyboard control
- Twenty source, twenty vector interrupt structure with two priority levels
- Wake-up from Power-down mode via LVD or external interrupts at Port 1
- DTMF generator (P83CL884/P87CL884 only)
- MSK modem including Manchester encoder/decoder with 2 digital outputs for analog cordless telephones (standards CT0/CT1/CT1+)
- Two standard 16-bit timer/event counters
- Additional 16-bit timer/event counter with Capture, Compare and Auto-reload function
- Watchdog Timer
- Full duplex enhanced UART with double buffering
- I²C-bus interface for serial transfer on two lines, maximum 400 kHz
- Very low current consumption
- Single supply voltage: 2.7 to 3.6 V
- Frequency range: 3.58 MHz
- Operating temperature: –25 to +70 °C
- 28 pins SO package.

GENERAL DESCRIPTION

The P8xCL883/P8xCL884 - denoting the P83CL883; P87CL883; P83CL884 and P87CL884 - are manufactured in an advanced CMOS technology. The P83CL883 and P87CL883 are based on single chip technology and the P83CL884 and P87CL884 are based on MCM (Multi-Chip-Module) technology as the EEPROM is integrated on a separate chip.

The P8xCL883/P8xCL884 are 8-bit microcontrollers especially suited for low cost analog cordless telephone applications (CT0, CT1, CT1+ standards). For this purpose, features like DTMF, EEPROM, MSK modem and POR/LVD are integrated on-chip.

The device is optimized for low power consumption. The P8xCL883/P8xCL884 have two software selectable features for power reduction: Idle and Power-down modes. In addition, all derivative blocks can switch off their clock if they are inactive.

The instruction set of the P8xCL883/P8xCL884 is based on that of the 8051. The P8xCL883/P8xCL884 also function as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte. Due to the missing port P2, there is no external data or memory access and the MOVX operations cannot be used.

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

This data sheet details the specific properties of the P8xCL883/P8xCL884; for details of the P8xCL883/P8xCL884 core and the derivative functions see the *"TELX family"* data sheet and *"Data Handbook IC20; 80C51-based 8-bit Microcontrollers"*.

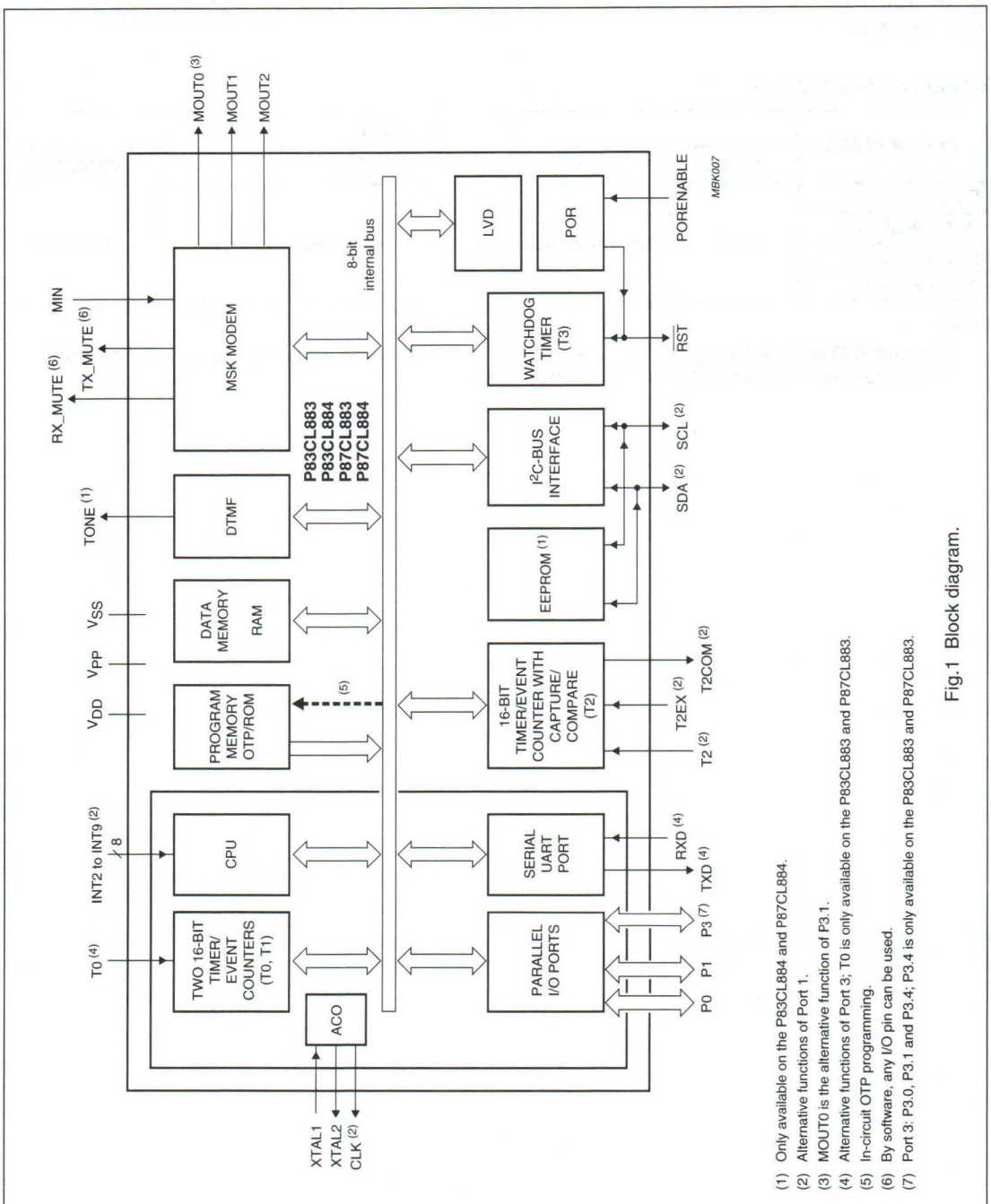
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
P83CL883DDT	SO28[1]	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
P87CL883DDT			
P83CL884DDT			
P87CL884DDT			

Note

1. When using IR reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* (order number 9398 510 34011) are followed.

BLOCK DIAGRAM

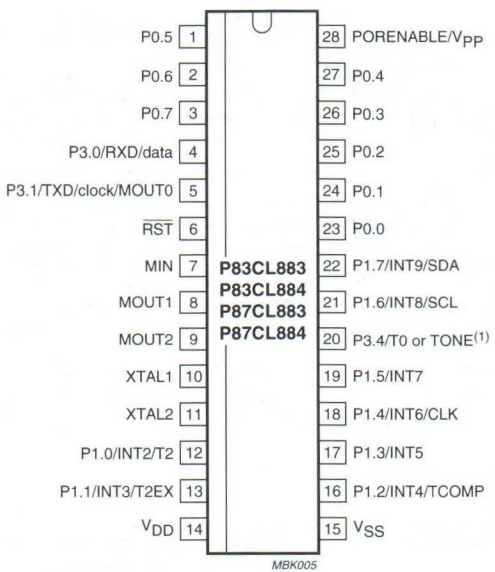


(1) Only available on the P83CL884 and P87CL884.
(2) Alternative functions of Port 1.
(3) MOUT0 is the alternative function of P3.1.
(4) Alternative functions of Port 3; T0 is only available on the P83CL883 and P87CL883.
(5) In-circuit OTP programming.
(6) By software, any I/O pin can be used.
(7) Port 3: P3.0, P3.1 and P3.4; P3.4 is only available on the P83CL883 and P87CL883.

Fig.1 Block diagram.

PINNING INFORMATION

Pinning



(1) **Pin 20**: P3.4/T0 on the P83CL883 and P87CL883; TONE on the P83CL884 and P87CL884.

Fig.2 Pin configuration.

Pin description

SYMBOL	PIN	DESCRIPTION
$\overline{RST}$	6	**Active low reset:** a LOW level on this pin for two machine cycles while the oscillator is running, resets the device. The $\overline{RST}$ pin is also an output which can be used to reset other ICs.
MIN	7	Digital **MSK** modem input.
MOUT1	8	Digital **MSK** modem outputs.
MOUT2	9	
XTAL1	10	**Crystal input:** Input to the Amplitude Controlled Oscillator. Also the input for an externally generated clock source.
XTAL2	11	**Crystal output:** Output of the Amplitude Controlled Oscillator. To be left non-connected when an external oscillator clock is used.
V_{DD}	14	Power supply.
V_{SS}	15	Ground.
P0.0 to P0.7	23 to 27, 1 to 3	**Port 0**: 8-bit bidirectional I/O port. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output.
P1.0/INT2/T2	12	**Port 1**: 8-bit bidirectional I/O port with alternative functions. Every port pin except P1.6 and P1.7 (I^2C-bus pins) can be used as open-drain, standard port, high-impedance input or push-pull output. Port P1.3 has LED drive capability. Port 1 also serves the alternative functions: **INT2 to INT9** interrupts; Timer T2 external inputs **T2** and **T2EX**; Timer T2 compare output **T2COMP**; external clock output **CLK**; I^2C-bus clock **SCL** and data in/outputs **SDA**.
P1.1/INT3/T2EX	13	
P1.2/INT4/T2COMP	16	
P1.3/INT5	17	
P1.4/INT6/CLK	18	
P1.5/INT7	19	
P1.6/INT8/SCL	21	
P1.7/INT9/SDA	22	
P3.0/RXD/data	4	**Port 3:** 3 or 2-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output. Port 3 also serves the alternative functions: **RXD/data** is the serial port receiver data input (asynchronous) or data I/O (synchronous); **TXD/clock** is the serial port transmitter data output (asynchronous) or clock output (synchronous) or digital MSK modem output **MOUT0**; **T0** is an external input for Timer 0. **P3.4/T0** is only available on the P83CL883 and P87CL883.
P3.1/TXD/clock/ MOUT0	5	
P3.4/T0	20	
TONE	20	**DTMF** output; **TONE** is only available on the P83CL884 and P87CL884.
PORENABLE/V_{PP}	28	**PORENABLE**: Power-on-reset circuit enable. If PORENABLE = 1, the internal Power-on-reset circuit is enabled. If external reset circuitry is used, it is recommended to keep PORENABLE = 0 to reach lowest power consumption. This pin is also used for the OTP programming voltage V_{PP}.

TELX microcontrollers for CT0 handset/basestation applications

P83CL886; P87CL886

FEATURES

- Full static 80C51 CPU; enhanced 8-bit architecture with:
  - Minimum 6 cycles per instruction (twice as fast as a standard 80C51 core)
  - Non-page oriented instructions
  - Direct addressing
  - Four 8-byte RAM register banks
  - Stack depth limited only by available internal RAM (maximum 256 bytes)
  - Multiply, divide, subtract and compare instructions
- Three 8-bit ports (18 I/O lines)
- Program Memory:
  - P87CL886: 16 kbytes One Time Programmable
  - P83CL886: 16 kbytes ROM
- 512 bytes RAM
- Amplitude Controlled Oscillator (ACO) suitable for quartz crystal or ceramic resonator
- Improved Power-on/Power-off reset (POR) circuitry
- Low Voltage Detection (LVD) with 11 software programmable levels
- Eight interrupts on Port 1:
  - Edge or level sensitive triggering selectable via software
  - Power-saving use for keyboard control
- Twenty source, twenty vector interrupt structure with two priority levels
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- MSK modem including Manchester encoder/decoder with 2 digital outputs for analog cordless telephones (standards CT0/CT1/CT1+)
- Watchdog Timer
- Two standard 16-bit timer/event counters
- Additional 16-bit timer/event counter with Capture, Compare and Auto-reload function
- Full duplex enhanced UART with double buffering
- I²C-bus interface for serial transfer on two lines, maximum 400 kHz
- Very low current consumption
- Single supply voltage: 2.7 to 3.6 V
- Frequency: 3.58 MHz
- Operating temperature: –25 to +70 °C
- 28 pin SO package.

GENERAL DESCRIPTION

The P8xCL886 (denoting the P83CL886 and P87CL886) are manufactured in an advanced CMOS technology and are 8-bit microcontrollers especially suited for low cost analog cordless telephone applications (CT0, CT1 and CT1+ standards). Consequently, features like DTMF, MSK modem and POR/LVD are integrated on-chip.

Both devices are optimized for low power consumption and in addition have two software selectable modes for further power reduction: Idle and Power-down modes. All derivative blocks can switch off their clock if they are inactive.

The instruction set of the P8xCL886 is based on that of the 80C51. The P8xCL886 also function as arithmetic processors having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte. As port P2 is not implemented there is no external data or memory access and MOVX operations cannot be used.

This data sheet details the specific properties of the P8xCL886; for details of the P8xCL886 core and the derivative functions see the *"TELX family"* data sheet and *"Data Handbook IC20"*.

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
P83CL886DFT	SO28[1]	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
P87CL886DFT			

Note

1. When using IR reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* (order number 9398 510 34011) are followed.

BLOCK DIAGRAM

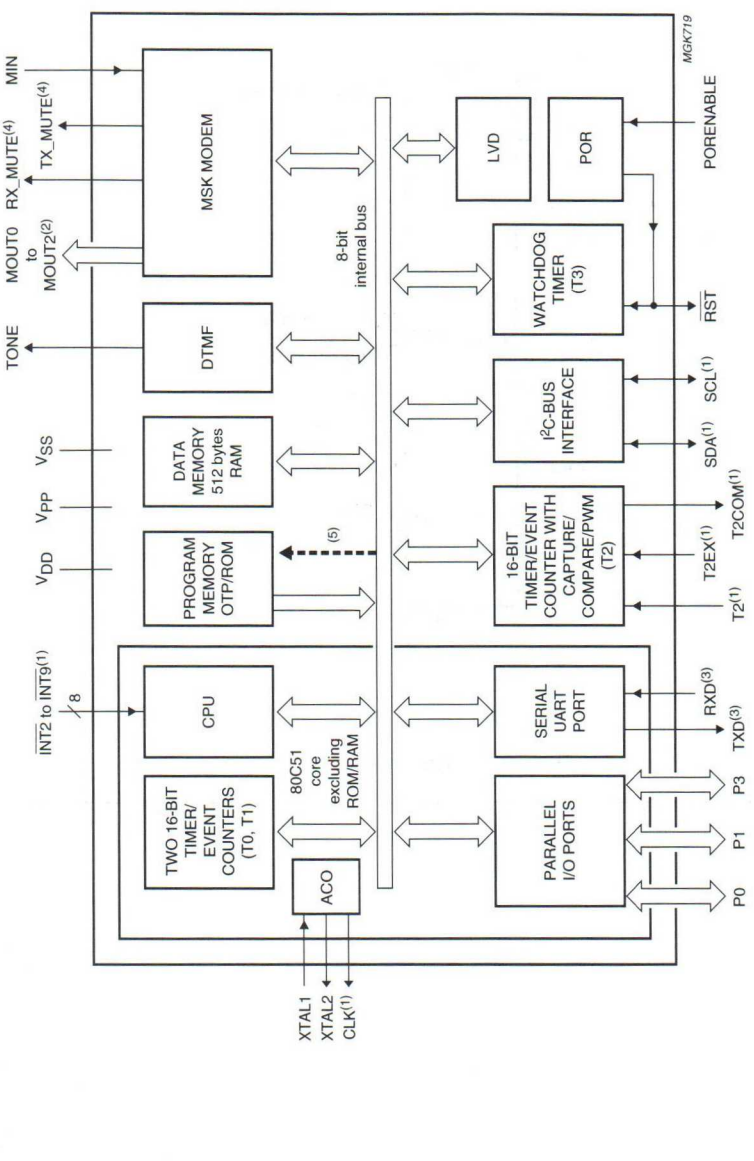


Fig.1 Block diagram.

(1) Alternative functions of Port 1.
(2) MOUT0 is the alternative function to P3.1.
(3) Alternative function of Port 3.
(4) By software any I/O port pin can be used.
(5) In-circuit OTP programming.

PINNING INFORMATION

Pinning

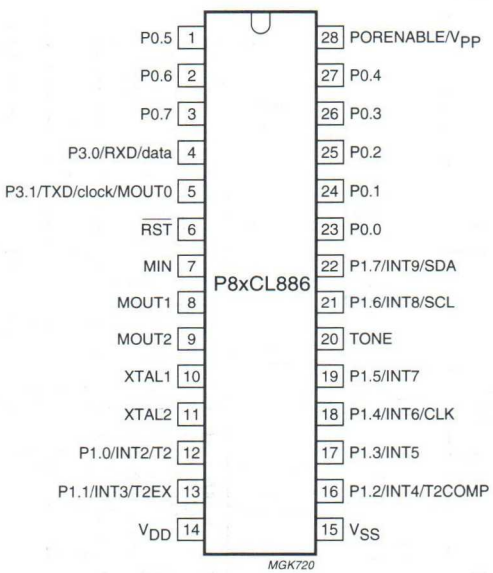


Fig.2 Pin configuration.

Pin description

Table 1 SO28 package

SYMBOL	PIN	DESCRIPTION
$\overline{RST}$	6	**Active low reset:** a LOW level on this pin for two machine cycles while the oscillator is running, resets the device. The $\overline{RST}$ pin is also an output which can be used to reset other ICs.
MIN	7	Digital **MSK** modem input.
MOUT1	8	Digital **MSK** modem outputs.
MOUT2	9	
XTAL1	10	**Crystal input:** Input to the Amplitude Controlled Oscillator. Also the input for an externally generated clock source.
XTAL2	11	**Crystal output:** Output of the Amplitude Controlled Oscillator; to be left non-connected when an external oscillator clock is used.
V_{DD}	14	Power supply.
V_{SS}	15	Ground.
P0.0 to P0.7	23 to 27, 1 to 3	**Port 0:** 8-bit bidirectional I/O port; every port pin can be used as open-drain, standard port, high-impedance input or push-pull output.
P1.0/INT2/T2	12	**Port 1:** 8-bit bidirectional I/O port with alternative functions. Every port pin except P1.6 and P1.7 (I^2C-bus pins) can be used as open-drain, standard port, high-impedance input or push-pull output. Port P1.3 has LED drive capability. Port 1 also serves the alternative functions: **INT2 to INT9** interrupts; Timer T2 external inputs **T2** and **T2EX**; Timer T2 compare output **T2COMP**; external clock output **CLK**; I^2C-bus clock **SCL** and data in/outputs **SDA**.
P1.1/INT3/T2EX	13	
P1.2/INT4/T2COMP	16	
P1.3/INT5	17	
P1.4/INT6/CLK	18	
P1.5/INT7	19	
P1.6/INT8/SCL	21	
P1.7/INT9/SDA	22	
P3.0/RXD/data	4	**Port 3:** 3 or 2-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output. Port 3 also serves the alternative functions: **RXD/data** is the serial port receiver data input (asynchronous) or data I/O (synchronous); **TXD/clock** is the serial port transmitter data output (asynchronous) or clock output (synchronous) or digital MSK modem output **MOUT0**.
P3.1/TXD/clock/ MOUT0	5	
TONE	20	**DTMF** output.
PORENABLE/V_{PP}	28	**PORENABLE**: Power-on-reset circuit enable. If PORENABLE = 1, the internal Power-on-reset circuit is enabled. If external reset circuitry is used, it is recommended to keep PORENABLE = 0 to reach lowest power consumption. This pin is also used for the OTP programming voltage V_{PP}.

TELX microcontrollers for CT0 handset/basestation applications

P83CL887; P87CL887

FEATURES

- Full static 80C51 CPU; enhanced 8-bit architecture with:
  - Minimum 6 cycles per instruction (twice as fast as a standard 80C51 core)
  - Non-page oriented instructions
  - Direct addressing
  - Four 8-byte RAM register banks
  - Stack depth limited only by available internal RAM (maximum 256 bytes)
  - Multiply, divide, subtract and compare instructions
- Three 8-bit ports (18 I/O lines)
- Program Memory:
  - P87CL887: 12 kbytes One Time Programmable
  - P83CL887: 12 kbytes ROM
- 512 bytes RAM
- Amplitude Controlled Oscillator (ACO) suitable for quartz crystal or ceramic resonator
- Improved Power-on/Power-off reset (POR) circuitry
- Low Voltage Detection (LVD) with 11 software programmable levels
- Eight interrupts on Port 1:
  - Edge or level sensitive triggering selectable via software
  - Power-saving use for keyboard control
- Twenty source, twenty vector interrupt structure with two priority levels
- Wake-up from Power-down mode via LVD or external interrupts at Port 1
- DTMF generator
- MSK modem including Manchester encoder/decoder with 2 digital outputs for analog cordless telephones (standards CT0/CT1/CT1+)
- Watchdog Timer
- Two standard 16-bit timer/event counters
- Additional 16-bit timer/event counter with Capture, Compare and Auto-reload function
- Full duplex enhanced UART with double buffering
- I²C-bus interface for serial transfer on two lines, maximum 400 kHz
- Very low current consumption
- Single supply voltage: 2.7 to 3.6 V
- Frequency: 3.58 MHz
- Operating temperature: –25 to +70 °C
- 28 pin SO package.

GENERAL DESCRIPTION

The P8xCL887 (denoting the P83CL887 and P87CL887) are manufactured in an advanced CMOS technology and are 8-bit microcontrollers especially suited for low cost analog cordless telephone applications (CT0, CT1 and CT1+ standards). Consequently, features like DTMF, MSK modem and POR/LVD are integrated on-chip.

Both devices are optimized for low power consumption and in addition have two software selectable modes for further power reduction: Idle and Power-down modes. All derivative blocks can switch off their clock if they are inactive.

The instruction set of the P8xCL887 is based on that of the 80C51. The P8xCL887 also function as arithmetic processors having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte. As port P2 is not implemented there is no external data or memory access and MOVX operations cannot be used.

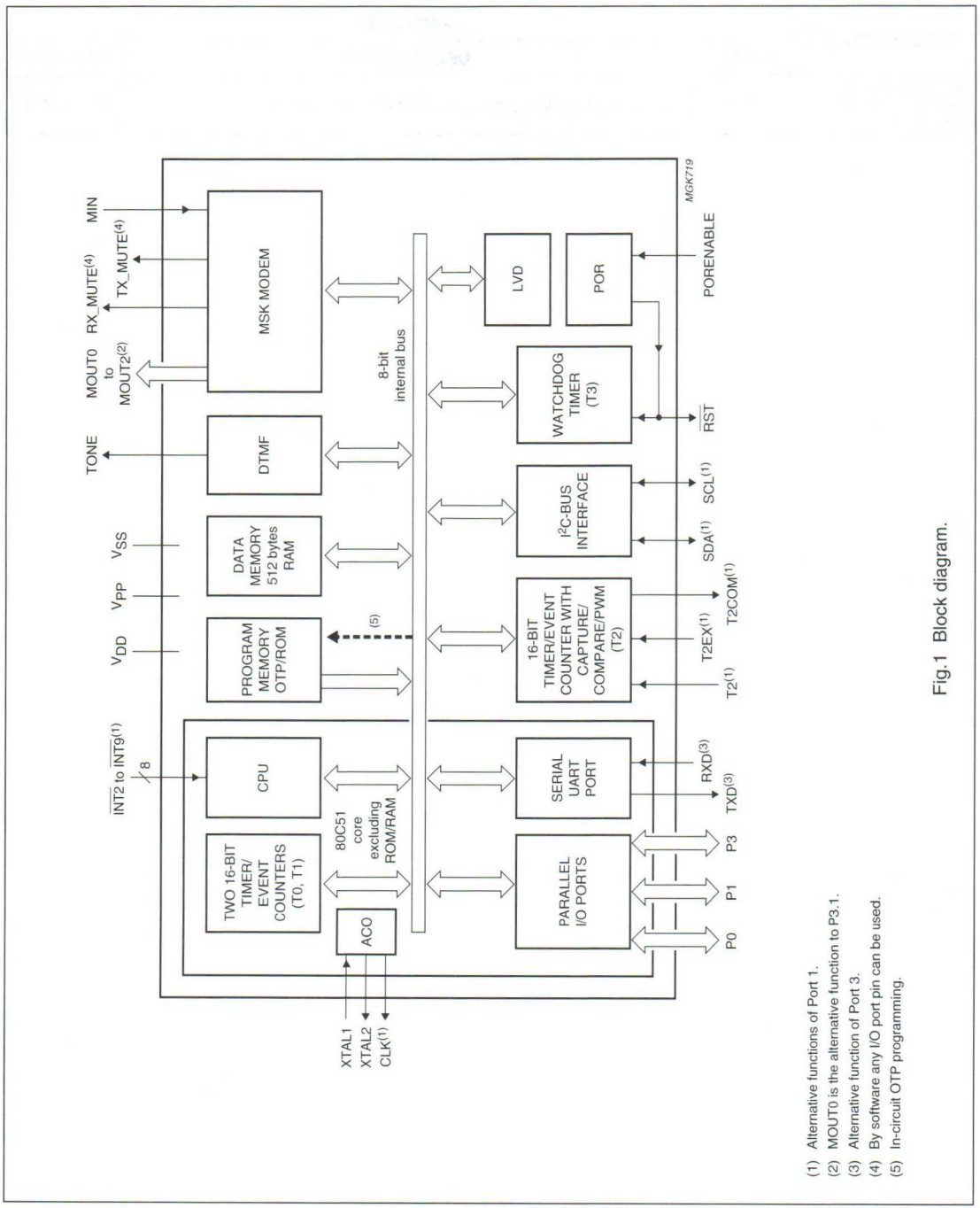
This data sheet details the specific properties of the P8xCL887; for details of the P8xCL887 core and the derivative functions see the *"TELX family"* data sheet and *"Data Handbook IC20"*.

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
P83CL887DFT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
P87CL887DFT			

BLOCK DIAGRAM



(1) Alternative functions of Port 1.
(2) MOUT0 is the alternative function to P3.1.
(3) Alternative function of Port 3.
(4) By software any I/O port pin can be used.
(5) In-circuit OTP programming.

Fig.1 Block diagram.

PINNING INFORMATION

Pinning

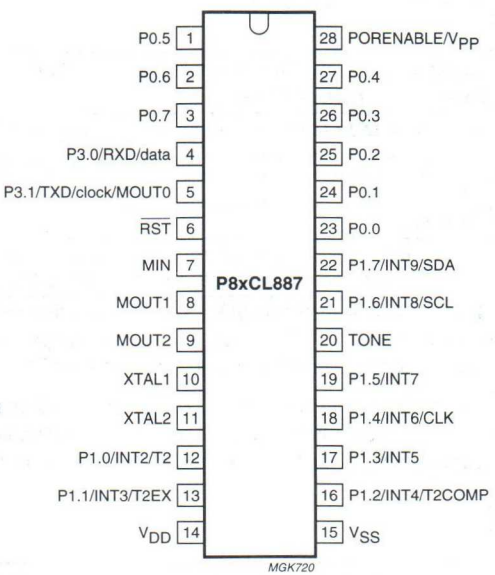


Fig.2 Pin configuration.

Pin description

Table 1 SO28 package

SYMBOL	PIN	DESCRIPTION
$\overline{RST}$	6	**Active low reset:** a LOW level on this pin for two machine cycles while the oscillator is running, resets the device. The $\overline{RST}$ pin is also an output which can be used to reset other ICs.
MIN	7	Digital **MSK** modem input.
MOUT1	8	Digital **MSK** modem outputs.
MOUT2	9	
XTAL1	10	**Crystal input:** Input to the Amplitude Controlled Oscillator. Also the input for an externally generated clock source.
XTAL2	11	**Crystal output:** Output of the Amplitude Controlled Oscillator; to be left non-connected when an external oscillator clock is used.
V_{DD}	14	Power supply.
V_{SS}	15	Ground.
P0.0 to P0.7	23 to 27, 1 to 3	**Port 0:** 8-bit bidirectional I/O port; every port pin can be used as open-drain, standard port, high-impedance input or push-pull output.
P1.0/INT2/T2	12	**Port 1:** 8-bit bidirectional I/O port with alternative functions. Every port pin except P1.6 and P1.7 (I^2C-bus pins) can be used as open-drain, standard port, high-impedance input or push-pull output. Port P1.3 has LED drive capability. Port 1 also serves the alternative functions: **INT2 to INT9** interrupts; Timer T2 external inputs **T2** and **T2EX**; Timer T2 compare output **T2COMP**; external clock output **CLK**; I^2C-bus clock **SCL** and data in/outputs **SDA**.
P1.1/INT3/T2EX	13	
P1.2/INT4/T2COMP	16	
P1.3/INT5	17	
P1.4/INT6/CLK	18	
P1.5/INT7	19	
P1.6/INT8/SCL	21	
P1.7/INT9/SDA	22	
P3.0/RXD/data	4	**Port 3:** 3 or 2-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output. Port 3 also serves the alternative functions: **RXD/data** is the serial port receiver data input (asynchronous) or data I/O (synchronous); **TXD/clock** is the serial port transmitter data output (asynchronous) or clock output (synchronous) or digital MSK modem output **MOUT0**.
P3.1/TXD/clock/ MOUT0	5	
TONE	20	**DTMF** output.
PORENABLE/V_{PP}	28	**PORENABLE**: Power-on-reset circuit enable. If PORENABLE = 1, the internal Power-on-reset circuit is enabled. If external reset circuitry is used, it is recommended to keep PORENABLE = 0 to reach lowest power consumption. This pin is also used for the OTP programming voltage V_{PP}.

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8-bit microcontrollers with DTMF generator and 128 bytes EEPROM

PCA3351C; 52C; 53C PCD3351A; 52A; 53A; 55A

1 FEATURES

- 8-bit CPU, ROM, RAM, EEPROM and I/O; all in one (28-lead or 32-lead) package
- ROM:
  - 2 kbytes (PCA3351C and PCD3351A)
  - 4 kbytes (PCA3352C and PCD3352A)
  - 6 kbytes (PCA3353C and PCD3353A)
  - 8 kbytes (PCD3355A)
- RAM:
  - 64 bytes (PCA3351C and PCD3351A)
  - 128 bytes (PCA3352C, PCD3352A, PCA3353C, PCD3353A and PCD3355A)
- 128 bytes Electrically Erasable Programmable Read-Only Memory (EEPROM)
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- 8-bit reloadable Timer 2
- Three single-level vectored interrupts:
  - external
  - 8-bit programmable Timer/event counter 1
  - derivative; triggered by reloadable Timer 2
- Two test inputs, one of which also serves as the external interrupt input
- DTMF, modem, musical tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT compatible)
- Melody output for ringer application
- Power-on-reset
- Stop and Idle modes
- Supply voltage: 1.8 to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- Clock frequency: 1 to 16 MHz (3.58 MHz for DTMF suggested)
- Operating ambient temperature: –25 to +70 °C or 0 to 50 °C
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

This data sheet details the specific properties of the devices referred to. The shared properties of the PCD33xxA family of microcontrollers are described in the *"PCD33xxA family"* data sheet, which should be read in conjunction with this publication.

- 'PCA3351C; 52C; 53C' denotes the types PCA3351C, PCA3352C and PCA3353C. Unless specified, these types will hereafter be referred to collectively as 'PCA335xC'.
- 'PCD3351A; 52A; 53A; 55A' denotes the types PCD3351A, PCD3352A, PCD3353A, PCD3355A. Unless specified, these types will hereafter be referred to collectively as 'PCD335xA'.

The PCA335xC and PCD335xA are microcontrollers designed primarily for telephony applications. They include an on-chip generator for dual tone multifrequency (DTMF), modem and musical tones. In addition to dialling, generated frequencies can be made available as square waves for melody generation, providing ringer operation.

The PCA335xC and PCD335xA also incorporate 128 bytes of EEPROM, permitting data storage without battery backup. The EEPROM can be used for storing telephone numbers, particularly for implementing redial functions.

The PCA335xC and PCD335xA can be emulated with the OTP microcontrollers PCD3755A and PCD3755E. See Chapter 14, Table 25.

The instruction set is similar to that of the MAB8048 and is a sub-set of that listed in the *"PCD33xxA family"* data sheet.

The differences between PCA335xC and PCD335xA are shown in Table 1.

Table 1 Differences: PCA335xC and PCD335xA

TYPE	V_{POR}	AMBIENT TEMP. RANGE
PCA335xC	fixed at 2.0 V ±0.3 V	0 to 50 °C
PCD335xA	(1.2 to 3.6 V) ±0.5 V[1]	–25 to +70 °C

Note

1. See Chapter 14, Table 26.

3 ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA335xCP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD335xAP			
PCA335xCT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCD335xAT			
PCA335xCH	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
PCD335xAH			

Note

1. The types:
   a) PCA335xC denotes: PCA3351C, PCA3352C or PCA3353C.
   b) PCD335xA denotes: PCD3351A, PCD3352A, PCD3353A or PCD3355A.

4 BLOCK DIAGRAM

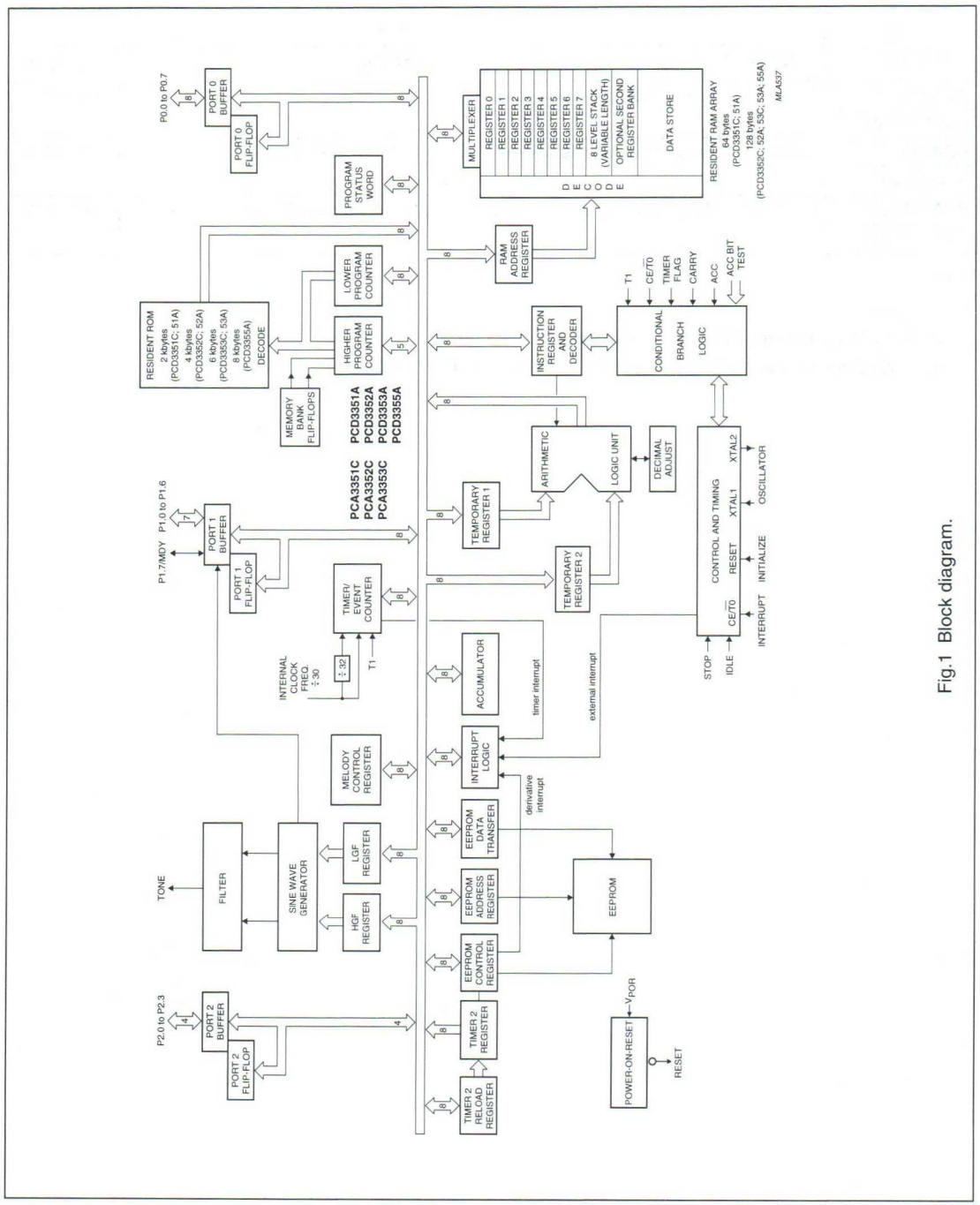
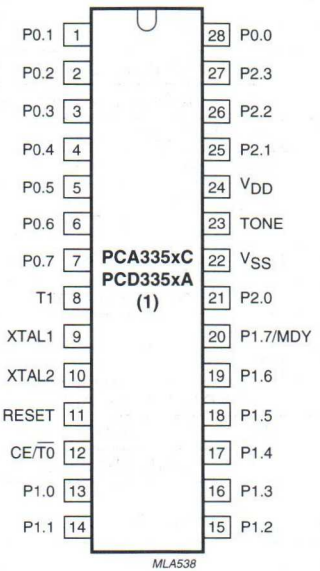


Fig.1 Block diagram.

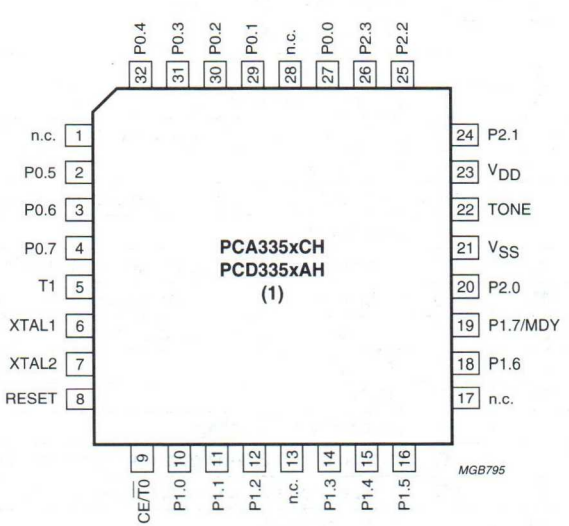
5 PINNING INFORMATION

5.1 Pinning



(1) **PCA335xC denotes**: PCA3351C, PCA3352C or PCA3353C.
PCD335xA denotes: PCD3351A, PCD3352A, PCD3353A or PCD3355A.

Fig.2 Pin configuration for DIP28 (SOT117-1) and SO28 (SOT136-1).



(1) **PCA335xCH denotes**: PCA3351CH, PCA3352CH or PCA3353CH.
PCD335xAH denotes: PCD3351AH, PCD3352AH, PCD3353AH or PCD3355AH.

Fig.3 Pin configuration for LQFP32 (SOT358-1).

5.2 Pin description

Table 2 SOT117-1 and SOT136-1 packages (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	TYPE	DESCRIPTION
P0.1 to P0.7	1 to 7	I/O	7 bits of Port 0: 8-bit quasi-bidirectional I/O port
T1	8	I	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	9	I	crystal oscillator or external clock input
XTAL2	10	O	crystal oscillator output
RESET	11	I	reset input
CE/$\overline{T0}$	12	I	Chip Enable or Test 0
P1.0 to P1.6	13 to 19	I/O	7 bits of Port 1: 8-bit quasi-bidirectional I/O port
P1.7/MDY	20	I/O	1 bit of Port 1: 8-bit quasi-bidirectional I/O port; or melody output
P2.0	21	I/O	1 bit of Port 2: 4-bit quasi-bidirectional I/O port
V_{SS}	22	P	ground
TONE	23	O	DTMF output
V_{DD}	24	P	positive supply voltage
P2.1 to P2.3	25 to 27	I/O	3 bits of Port 2: 4-bit quasi-bidirectional I/O port
P0.0	28	I/O	1 bit of Port 0: 8-bit quasi-bidirectional I/O port

Table 3 SOT358-1 package (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	TYPE	DESCRIPTION
n.c.	1	–	not connected
P0.5 to P0.7	2 to 4	I/O	3 bits of Port 0: 8-bit quasi-bidirectional I/O port
T1	5	I	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	6	I	crystal oscillator or external clock input
XTAL2	7	O	crystal oscillator output
RESET	8	I	reset input
CE/$\overline{T0}$	9	I	Chip Enable or Test 0
P1.0 to P1.2	10 to 12	I/O	3 bits of Port 1: 8-bit quasi-bidirectional I/O port
n.c.	13	–	not connected
P1.3 to P1.5	14 to 16	I/O	3 bits of Port 1: 8-bit quasi-bidirectional I/O port
n.c.	17	–	not connected
P1.6	18	I/O	1 bit of Port 1: 8-bit quasi-bidirectional I/O port
P1.7/MDY	19	I/O	1 bit of Port 1: 8-bit quasi-bidirectional I/O port; or melody output
P2.0	20	I/O	1 bit of Port 2: 4-bit quasi-bidirectional I/O port
V_{SS}	21	P	ground
TONE	22	O	DTMF output
V_{DD}	23	P	positive supply voltage
P2.1 to P2.3	24 to 26	I/O	3 bits of Port 2: 4-bit quasi-bidirectional I/O port
P0.0	27	I/O	1 bit of Port 0: 8-bit quasi-bidirectional I/O port
n.c.	28	–	not connected
P0.1 to P0.4	29 to 32	I/O	4 bits of Port 0: 8-bit quasi-bidirectional I/O port

6 FREQUENCY GENERATOR

A versatile frequency generator section is provided (see Fig.4). For normal operation, use a 3.58 MHz quartz crystal or PXE resonator. The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets.

Their frequencies are provided in purely sinusoidal form on the TONE output or as square waves on the port line P1.7/MDY.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available.

When no tones are generated the TONE output is in 3-state mode.

6.1 Frequency generator derivative registers

6.1.1 High and Low Group Frequency registers

Table 4 gives the addresses, symbols and access types of the High Group Frequency (HGF) and Low Group Frequency (LGF) registers.

Table 4 Hexadecimal addresses, symbols, access types and bit symbols of the frequency registers

REGISTER ADDRESS	REGISTER SYMBOL	ACCESS TYPE	BIT SYMBOLS							
			7	6	5	4	3	2	1	0
11H	HGF	W	H7	H6	H5	H4	H3	H2	H1	H0
12H	LGF	W	L7	L6	L5	L4	L3	L2	L1	L0

6.1.2 Melody Control Register (MDYCON)

Table 5 Melody Control Register, MDYCON (address 13H; access type R/W)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	EMO

Table 6 Description of MDYCON bits

BIT	SYMBOL	DESCRIPTION
7 to 1	–	These bits are set to a logic 0.
0	EMO	Enable Melody Output. If bit EMO = 0, then P1.7/MDY is a standard port line. If bit EMO = 1, then P1.7/MDY is the melody output. EMO = 1 does not inhibit the port instructions for P1.7/MDY. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by port instructions. However, the port flip-flop of P1.7/MDY must remain set to avoid conflicts between melody and port outputs. When the HGF contents are zero while EMO = 1, P1.7/MDY is in the HIGH state.

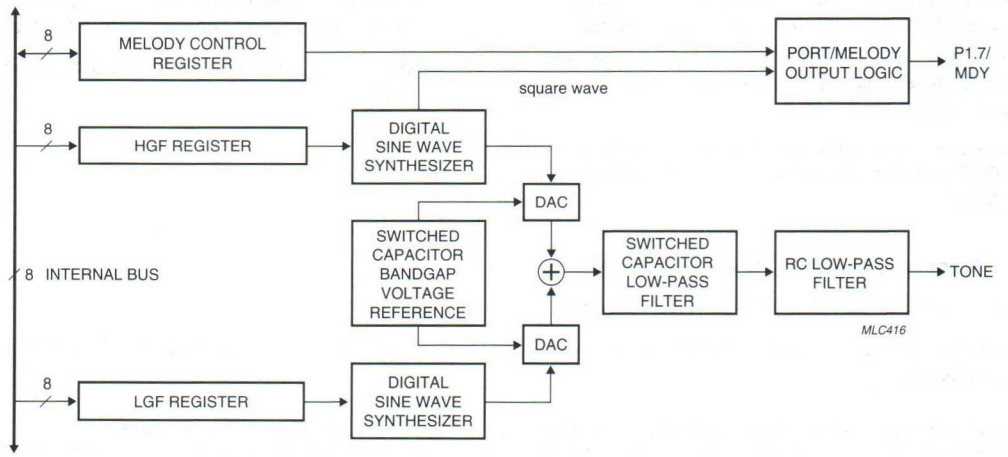


Fig.4 Block diagram of the frequency generator and melody output (P1.7/MDY) section.

6.2 Melody output (P1.7/MDY)

The melody output (P1.7/MDY) is very useful for generating musical notes when a purely sinusoidal signal is not required, such as for ringer applications.

The square wave (duty cycle = $^{12}/_{23}$ or 52%) will include the attenuated harmonics of the base frequency, which is defined by the contents of the HGF register (Table 4). However, even higher frequency notes may be produced since the low-pass filtering on the TONE output is not applied to the P1.7/MDY output. This results in the minimum decimal value x in the HGF register (see equation in Section 6.3) being 2 for the P1.7/MDY output, rather than 60 for the TONE output. A sinusoidal TONE output is produced at the same time as the melody square wave, but due to the filtering, the higher frequency sine waves with $x < 60$ will not appear at the TONE output.

Since the melody output is shared with P1.7, the port flip-flop of P1.7 has to be set HIGH before using the melody output. This to avoid conflicts between melody and port outputs. The melody output drive depends on the configuration of port P1.7/MDY, see Chapter 14, Table 26.

6.3 Frequency registers

The two frequency registers HGF and LGF define two frequencies. From these, the digital sine synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures tone output levels independent of supply voltage and temperature.

The amplitude of the Low Group Frequency sine wave is attenuated by 2 dB compared to the amplitude of the High Group Frequency sine wave.

The two sine waves are summed and then filtered by an on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

The value 00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption.

The frequency of the sine wave generated from either HGF or LGF is a function of the decimal value 'x' held in the register. The variables are related by the equation:

$$f = \frac{f_{xtal}}{[23\,(x+2)]}; \text{ where } 60 \leq x \leq 255 \text{ for TONE output.}$$

6.4 DTMF frequencies

Assuming an oscillator frequency f_{xtal} = 3.58 MHz, the DTMF standard frequencies can be implemented as shown in Table 7.

The relationships between telephone keyboard symbols, DTMF frequency pairs and the frequency register contents are given in Table 8.

Table 7 DTMF standard frequencies and their implementation; value = LGF, HGF contents

VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 8 Dialling symbols, corresponding DTMF frequency pairs and frequency register contents

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
•	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

6.5 Modem frequencies

Again assuming an oscillator frequency f_{xtal} = 3.58 MHz, the standard modem frequencies can be implemented as in Table 9. It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling Low Group Frequency generation.

Table 9 Standard modem frequencies and their implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980[1]	978.82	−0.12	−1.18
82	1180[1]	1179.03	−0.08	−0.97
8F	1070[2]	1073.33	0.31	3.33
79	1270[2]	1265.30	−0.37	−4.70
80	1200[3]	1197.17	−0.24	−2.83
45	2200[3]	2192.01	−0.36	−7.99
76	1300[4]	1296.94	−0.24	−3.06
48	2100[4]	2103.14	0.15	3.14
5C	1650[1]	1655.66	0.34	5.66
52	1850[1]	1852.77	0.15	2.77
4B	2025[2]	2021.20	−0.19	−3.80
44	2225[2]	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

6.6 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{xtal} = 3.58 MHz (Table 10). It is suggested to define the frequency by the HGF register while the LGF contains 00H, disabling Low Group Frequency generation

Table 10 Musical scale frequencies and their implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD[1]	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 @ 440 Hz.

7 EEPROM AND TIMER 2 ORGANIZATION

The PCD335xA and PCA335xC have 128 bytes of Electrically Erasable Programmable Read-Only Memory (EEPROM). Such non-volatile storage provides data retention without the need for battery backup. In telecom applications, the EEPROM is used for storing redial numbers and for short dialling of frequently used numbers. More generally, EEPROM may be used for customizing microcontrollers, such as to include a PIN code or a country code, to define trimming parameters, to select application features from the range stored in ROM.

The most significant difference between a RAM and an EEPROM is that a bit in EEPROM, once written to a logic 1, cannot be cleared by a subsequent write operation. Successive write accesses actually perform a logical OR with the previously stored information. Therefore, to clear a bit, the whole byte must be erased and re-written with the particular bit cleared. Thus, an erase-and-write operation is the EEPROM equivalent of a RAM write operation

Whereas read access times to an EEPROM are comparable to RAM access times, write and erase access times are much slower at 5 ms each. To make these operations more efficient, several provisions are available in the PCD335xA and PCA335xC.

First, the EEPROM array is structured into 32 four-byte pages (see Fig.5) permitting access to 4 bytes in parallel (write page, erase/write page and erase page). It is also possible to erase and write individual bytes. Finally, the EEPROM address register provides auto-incrementing, allowing very efficient read and write accesses to sequential bytes.

To simplify the erase and write timing, the derivative 8-bit down-counter (Timer 2) with reload register is provided. In addition to EEPROM timing, Timer 2 can be used for general real-time tasks, such as for measuring signal duration and for defining pulse widths.

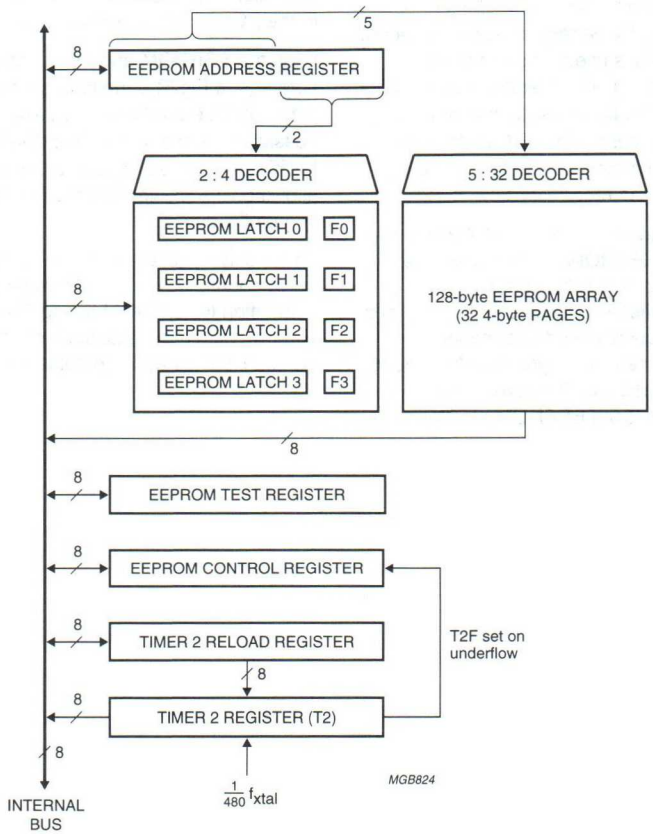


Fig.5 Block diagram of the EEPROM and Timer 2.

7.1 EEPROM registers

7.1.1 EEPROM CONTROL REGISTER (EPCR)

The behaviour of the EEPROM and Timer 2 section is defined by the EEPROM Control Register. See Tables 11, 12 and 13.

Table 11 EEPROM Control Register, EPCR (address 04H, access type R/W)

7	6	5	4	3	2	1	0
STT2	ET2I	T2F	EWP	MC3	MC2	MC1	0

Table 12 Description of the EPCR bits

BIT	SYMBOL	DESCRIPTION
7	STT2	Start T2. If STT2 = 0, then Timer 2 is stopped; T2 value held. If STT2 = 1, then T2 decrements from reload value.
6	ET2I	Enable T2 interrupt. If ET2I = 0, then T2F event cannot request interrupt. If ET2I = 1, then T2F event can request interrupt.
5	T2F	Timer 2 flag. Set when T2 underflows (or by program); reset by program.
4	EWP	Erase or write in progress (EWP). Set by program (EWP starts EEPROM erase and/or write and Timer 2). Reset at the end of EEPROM erase and/or write.
3	MC3	Mode control 3 to 1. These three bits in conjunction with bit EWP select the mode as shown in Table 13.
2	MC2	
1	MC1	
0	–	This bit is set to a logic 0.

Table 13 Mode selection; X = don't care

EWP	MC3	MC2	MC1	DESCRIPTION
0	0	0	0	read byte
0	0	1	0	increment mode
1	0	1	X	write page
1	1	0	0	erase/write page
1	1	1	1	erase page
X	0	0	1	not allowed
X	1	0	1	
X	1	1	0	

7.1.2 EEPROM ADDRESS REGISTER (ADDR)

The EEPROM Address Register determines the EEPROM location to which an EEPROM access is directed.

As a whole, ADDR auto-increments after read and write cycles to EEPROM, but remains fixed after erase cycles. This behaviour generates the correct ADDR contents for sequential read accesses and for sequential write or erase/write accesses with intermediate page setup. Overflow of the 8-bit counter wraps around to zero.

Table 14 EEPROM Address Register, ADDR (address 01H, access type R/W)

7	6	5	4	3	2	1	0
0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 15 Description of ADDR bits

BIT	SYMBOL	DESCRIPTION
7	–	This bit is set to a logic 0.
6 to 2	AD6 to AD2	AD2 to AD6 select one of 32 pages.
1 to 0	AD1 to AD0	AD1 and AD0 are irrelevant during erase and write cycles. For read accesses, AD0 and AD1 indicate the byte location within an EEPROM page. During page setup, finally, AD0 and AD1 select EEPROM Latch 0 to 3 whereas AD2 to AD6 are irrelevant. If increment mode (Table 13) is active during page setup, the subcounter consisting of AD0 and AD1 increments after every write to an EEPROM latch, thus enhancing access to sequential EEPROM latches. Incrementing stops when EEPROM Latch 3 is reached, i.e. when AD0 and AD1 are both a logic 1.

7.1.3 EEPROM DATA REGISTER (DATR)

Table 16 EEPROM Data Register, DATR (address 03H; access type R/W)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 17 Description of DATR bits

BIT	SYMBOL	DESCRIPTION
7 to 0	D7 to D0	The EEPROM Data Register (DATR) is only a conceptual entity. A read operation from DATR, reads out the EEPROM byte addressed by ADDR. On the other hand, a write operation to DATR, loads data into the EEPROM latch (see Fig.5) defined by bits AD0 and AD1 of ADDR.

7.1.4 EEPROM TEST REGISTER (TST)

The EEPROM Test register is used for testing purposes during device manufacture. It must not be accessed by the device user.

7.2 EEPROM latches

The four EEPROM latches (EEPROM Latch 0 to 3; Fig.5) cannot be read by user software. Due to their construction, the latches can only be preset, but not cleared. Successive write operations through DATR to the EEPROM latches actually perform a logical OR with the previously stored data in EEPROM. The EEPROM latches are reset at the conclusion of any EEPROM cycle.

7.3 EEPROM flags

The four EEPROM flags (F0 to F3; Fig.5) cannot be directly accessed by user software. An EEPROM flag is set as a side-effect when the corresponding EEPROM latch is written through DATR. The EEPROM flags are reset at the conclusion of any EEPROM cycle.

7.4 EEPROM macros

The instruction sequence used in an EEPROM access should be treated as an indivisible entity. Erroneous programs result if ADDR, DATR, RELR or EPCR are inadvertently changed during an EEPROM cycle or its setup. Special care should be taken if the program may asynchronously divert due to an interrupt. A new access to the EEPROM may only be initiated when no write, erase or erase/write cycles are in progress. This can be verified by reading bit EWP (register EPCR).

For write, erase and erase/write cycles, it is assumed that the Timer 2 Reload Register (RELR) has been loaded with the appropriate value for a 5 ms delay, which depends on f_{xtal} (see Table 24). The end of a write, erase or erase/write cycle will be signalled by a cleared EWP and by a Timer 2 interrupt provided that ET2I = 1 and that the derivative interrupt is enabled.

7.5 EEPROM access

One read, one write, one erase/write and one erase access are defined by bits EWP and MC1 to MC3 in the EPCR register; see Table 11.

Read byte retrieves the EEPROM byte addressed by ADDR when DATR is read. Read cycles are instantaneous.

Write and erase cycles take 5 ms, however. Erase/write is a combination of an erase and a subsequent write cycle, consequently taking 10 ms.

As their names imply, **write page, erase page and erase/write page** are applied to a whole EEPROM page. Therefore, bits AD0 and AD1 of register ADDR (see Table 14), defining the byte location within an EEPROM page, are irrelevant during write and erase cycles. However, write and erase cycles need not affect all bytes of the page. The EEPROM flags F0 to F3 (see Fig.5) determine which bytes within the EEPROM page are affected by the erase and/or write cycles. A byte whose corresponding EEPROM flag is zero remains unchanged.

With erase page, a byte is erased if its corresponding EEPROM flag is set. With write page, data in EEPROM Latch 0 to 3 (Fig.5) are ORed to the individual page bytes if and only if the corresponding EEPROM flags are set.

In an erase/write cycle, F0 to F3 select which page bytes are erased and ORed with the corresponding EEPROM latches.

ORing, in this event, means that the EEPROM latches are copied to the selected page bytes.

The described page-wise organization of erase and write cycles allows up to four bytes to be individually erased or written within 5 ms. This advantage necessitates a preparation step, called **page setup**, before the actual erase and/or write cycle can be executed.

Page setup controls EEPROM latches and EEPROM flags. This will be described in the Sections 7.5.1 to 7.5.5.

7.5.1 PAGE SETUP

Page setup is a preparation step required before write page, erase page and erase/write page cycles.
As previously described, these page operations include single-byte write, erase and erase/write as a special event. EEPROM flags F0 to F3 determine which page bytes will be affected by the mentioned page operations. EEPROM Latch 0 to 3 must be preset through DATR to specify the write cycle data to EEPROM and to set the EEPROM flags as a side-effect. Obviously, the actual preset value of the EEPROM latches is irrelevant for erase page. Preset of one, two, three or all four EEPROM latches and the corresponding EEPROM flags can be performed by repeatedly defining ADDR and writing to DATR (see Table 18).

If more than one EEPROM latch must be preset, the subcounter consisting of AD0 and AD1 can be induced to auto-increment after every write to DATR, thus stepping through all EEPROM latches. For this purpose, increment mode (Table 13) must be selected. Auto-incrementing stops at EEPROM Latch 3. It is not mandatory to start at EEPROM Latch 0 as in shown in Table 19.

Note that AD2 to AD6 are irrelevant during page setup. They will usually specify the intended EEPROM page, anticipating the subsequent page cycle.

From now on, it will be assumed that AD2 to AD6 will contain the intended EEPROM page address after page setup.

Table 18 Page setup; preset

INSTRUCTION	RESULT
MOV A, #addr	address of EEPROM latch
MOV ADDR, A	send address to ADDR
MOV A, #data	load write, erase/write or erase data
MOV DATR, A	send data to addressed EEPROM latch

Table 19 Page setup; auto-incrementing

INSTRUCTION	RESULT
MOV A, #MC2	increment mode control word
MOV EPCR, A	select increment mode
MOV A, #baddr	EEPROM Latch 0 address (AD0 = AD1 = 0)
MOV ADDR, A	send EEPROM Latch 0 address to ADDR
MOV A, R0	load 1st byte from Register 0
MOV DATR, A	send 1st byte to EEPROM Latch 0
MOV A, R1	load 2nd byte from Register 1
MOV DATR, A	send 2nd byte to EEPROM Latch 1
MOV A, R2	load 3rd byte from Register 2
MOV DATR, A	send 3rd byte to EEPROM Latch 2
MOV A, R3	load 4th byte from Register 3
MOV DATR, A	send 4th byte to EEPROM Latch 3

7.5.2 READ BYTE

Since ADDR auto-increments after a read cycle regardless of the page boundary, successive bytes can efficiently be read by repeating the last instruction.

Table 20 Read byte

INSTRUCTION	RESULT
MOV A, #RDADDR	load read address
MOV ADDR, A	send address to ADDR
MOV A, DATR	read EEPROM data

7.5.3 WRITE PAGE

The write cycle performs a logical OR between the data in the EEPROM latches and that in the addressed EEPROM page. To actually copy the data from the EEPROM latches, the corresponding bytes in the page should previously have been erased.

The EEPROM latches are preset as described in Section 7.5.1. The actual transfer to the EEPROM is then performed as shown in Table 21.

The last instruction also starts Timer 2. The data in the EEPROM latches are ORed with that in the corresponding page bytes within 5 ms. A single-byte write is simply a special case of 'write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by bits AD2 to AD6) and to EEPROM Latch 0 (by bits AD0 and AD1). This allows efficient coding of multi-page write operations.

Table 21 Write page

INSTRUCTION	RESULT
MOV A, #EWP + MC2	'write page' control word
MOV EPCR, A	start 'write page' cycle

7.5.4 ERASE/WRITE PAGE

The EEPROM latches are preset as described in Section 7.5.1. The page bytes corresponding to the asserted flags (among F0 to F3) are erased and re-written with the contents of the respective EEPROM latches.

The last instruction also starts Timer 2. Erasure takes 5 ms upon which Timer Register T2 reloads for another 5 ms cycle for writing. The top cycles together take 10 ms. A single-byte erase/write is simply a special case of 'erase/write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by AD2 to AD6) and to EEPROM Latch 0 (by AD0 and AD1). This allows efficient coding of multi-page erase/write operations.

Table 22 Erase/write page

INSTRUCTION	RESULT
MOV A, #EWP + MC3	'erase/write page' control word
MOV EPCR, A	start 'erase/write page' cycle

7.5.5 ERASE PAGE

The EEPROM flags are set as described in Section 7.5.1. The corresponding page bytes are erased.

The last instruction also starts Timer 2. Erasure takes 5 ms. A single-byte erase is simply a special case of 'erase page'.

Note that ADDR does not auto-increment after an erase cycle.

Table 23 Erase page

INSTRUCTION	RESULT
MOV A, #EWP + MC3 + MC2 + MC1	'erase page' control word
MOV EPCR, A	start 'erase page' cycle

7.6 Timer 2

Timer 2 is a 8-bit down-counter decremented at a rate of $1/480 \times f_{xtal}$. It may be used either for EEPROM timing or as a general purpose timer. Conflicts between the two applications should be carefully avoided.

7.6.1 TIMER 2 FOR EEPROM TIMING

When used for EEPROM timing, Timer 2 serves to generate the 5 ms intervals needed for erasing or writing the EEPROM. At the decrement rate of $1/480 \times f_{xtal}$, the reload value for a 5 ms interval is a function of f_{xtal}. Table 24 summarizes the required reload values for a number of oscillator frequencies.

Timer 2 is started by setting bit EWP in the EPCR. The Timer Register T2 is loaded with the reload value from RELR. T2 decrements to zero.

For an erase/write cycle, underflow of T2 indicates the end of the erase operation. Therefore, Timer Register T2 is reloaded from RELR for another 5 ms interval during which the flagged EEPROM latches are copied to the corresponding bytes in the page addressed by ADDR.

The second underflow of an erase/write cycle and the first underflow of write page and erase page conclude the corresponding EEPROM cycle. Timer 2 is stopped, T2F is set whereas EWP and MC1 to MC3 are cleared.

Table 24 Reload values as a function of f_{xtal}

f_{xtal} (MHz)	RELOAD VALUE[1] (HEX)
1	0A
2	14
3.58	25
6	3E
10	68
16	A6

Note

1. The reload value is $(5 \times 10^{-3} \times 1/480 \times f_{xtal}) - 1$; f_{xtal} in MHz.

7.6.2 TIMER 2 AS A GENERAL PURPOSE TIMER

When used for purposes other than EEPROM timing, Timer 2 is started by setting STT2. The Timer Register T2 (see Table 27) is loaded with the reload value from RELR. T2 decrements to zero. On underflow, T2 is reloaded from RELR, T2F is set and T2 continues to decrement.

Timer 2 can be stopped at any time by clearing STT2. The value of T2 is then held and can be read out. After setting STT2 again, Timer 2 decrements from the reload value. Alternatively, it is possible to read T2 'on the fly' i.e. while Timer 2 is operating.

8 DERIVATIVE INTERRUPTS

One derivative interrupt event is defined. It is controlled by bits T2F and ET2I in the EPCR (see Tables 11 and 12).

The derivative interrupt event occurs when T2F is set. This request is honoured under the following circumstances:

- No interrupt routine proceeds
- No external interrupt request is pending
- The derivative interrupt is enabled
- ET2I is set.

The derivative interrupt routine must include instructions that will remove the cause of the derivative interrupt by explicitly clearing T2F. If the derivative interrupt is not used, T2F may directly be tested by the program. Obviously, T2F can also be asserted under program control, e.g. to generate a software interrupt.

9 TIMING

Although the PCD335xA and PCA335xC operate over a clock frequency range from 1 to 16 MHz, f_{xtal} = 3.58 MHz will usually be chosen to take full advantage of the frequency generator section.

10 RESET

In addition to the conditions given in the *"PCD33XXA Family"* data sheet, all derivative registers are cleared in the reset state.

11 IDLE MODE

In Idle mode, the frequency generator, the EEPROM and the Timer 2 sections remain operative. Therefore, the IDLE instruction may be executed while an erase and/or write access to EEPROM is in progress.

12 STOP MODE

Since the oscillator is switched off, the frequency generator, the EEPROM and the Timer 2 sections receive no clock. It is suggested to clear both the HGF and the LGF registers before entering Stop mode. This will cut off the biasing of the internal amplifiers, considerably reducing current requirements.

The Stop mode **must not** be entered while an erase and/or write access to EEPROM is in progress. The STOP instruction may only be executed when EWP in EPCR is zero. The Timer 2 section is frozen during Stop mode.

After exit from Stop mode by a HIGH level on CE/$\overline{T0}$, Timer 2 proceeds from the held state.

13 INSTRUCTION SET RESTRICTIONS

- For PCD3351A and PCA3351C only:
  - ROM space being restricted to 2 kbytes, the 'SEL MB1/2/3' instructions would define non-existing program memory banks and should therefore be avoided.
  - RAM space being restricted to 64 bytes, care should be taken to avoid accesses to non-existing RAM locations.
- For PCD3352A and PCA3352C only:
  - ROM space being restricted to 4 kbytes, the 'SEL MB2/3' instructions would define non-existing program memory banks and should therefore be avoided.
- For PCD3353A and PCA3353Conly:
  - ROM space being restricted to 6 kbytes, the 'SEL MB3' instructions would define non-existing program memory banks and should therefore be avoided.
- For the PCD3352A, PCD3353A, PCD3355A, PCA3352C and PCA3353C, RAM space is restricted to 128 bytes, thus care should be taken to avoid accesses to non-existing RAM locations.

14 OVERVIEW OF PORT AND POWER-ON-RESET CONFIGURATIONS

- The PCA335xC microcontrollers support one port and Power-on-reset configuration which is compatible with the OTP PCD3755E.
- The PCD335xA microcontrollers support two port and Power-on-reset configurations which can be chosen: one is compatible with the OTP PCD3755A, the other is compatible with the OTP PCD3755E.

Table 25 Available mask configurations

TYPE	CONFIGURATION	
	PCD3755A	PCD3755E
PCA3351C	–	X
PCA3352C	–	X
PCA3353C	–	X
PCD3351A	X	X
PCD3352A	X	X
PCD3353A	X	X
PCD3355A	X	X

Table 26 Port and Power-on-Reset configurations

See note 1 and 2.

COVERED BY OTP	PORT 0								PORT 1								PORT 2				V_{POR}
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	
PCD3755A	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1R	1R[3]	2S	2S	2S	2S	1.3 V
PCD3755E	1S	1S	1S	1S	1S	1S	1S	1S	2S	2S	2S	2S	2S	2S	1S	1S[3]	2S	1R	1R	1R	2.0 V

Notes

1. Port output drive: 1 = standard I/O; 2 = open-drain I/O, see *"PCD33xxA Family"* data sheet.
2. Port state after reset: S = Set (HIGH) and R = Reset (LOW).
3. The melody output drive type is push-pull.

15 SUMMARY OF DERIVATIVE REGISTERS

Table 27 Register map

ADDR. (HEX)	REGISTER	7	6	5	4	3	2	1	0	R/W
00	not used									
01	EEPROM Address Register (ADDR)	0	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/W
02	not used									
03	EEPROM Data Register (DATR)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
04	EEPROM Control Register (EPCR)	STT2	ET21	TF2	EWP	MC3	MC2	MC1	0	R/W
05	Timer 2 Reload Register (RELR)	R7	R6	R5	R4	R3	R2	R1	R0	R/W
06	Timer 2 Register (T2)	T2.7	T2.6	T2.5	T2.4	T2.3	T2.2	T2.1	T2.0	R
07	Test Register (TST)	only for test purposes; not to be accessed by the device user								
08 to 10	not used									
11	High Group Frequency Register (HGF)	H7	H6	H5	H4	H3	H2	H1	H0	W
12	Low Group Frequency Register (LGF)	L7	L6	L5	L4	L3	L2	L1	L0	W
13	Melody Control Register (MDYCON)	0	0	0	0	0	0	0	EMO	R/W
14 to FF	not used									

16 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Data Handbook IC14, Section: Handling MOS devices"*).

17 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+7.0	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{SS}	ground supply current	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	–	90	°C

18 DC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = 0 to +50 °C (PCA335xC) or −25 to +70 °C (PCD335xA); all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	see Fig.6				
	operating	note 1	1.8	–	6	V
	RAM data retention in Stop mode		1.0	–	6	V
I_{DD}	operating supply current	see Figs 7 and 8; note 2				
		V_{DD} = 3 V; value HGF or LGF ≠ 0	–	0.8	1.6	mA
		V_{DD} = 3 V	–	0.35	0.7	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.5	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	2.4	6.0	mA
$I_{DD(idle)}$	supply current (Idle mode)	see Figs 9 and 10; note 2				
		V_{DD} = 3 V; value HGF or LGF ≠ 0	–	0.7	1.4	mA
		V_{DD} = 3 V	–	0.25	0.5	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.1	3.4	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	1.7	5.0	mA
$I_{DD(stp)}$	supply current (Stop mode)	see Fig.11; note 3				
		V_{DD} = 1.8 V; T_{amb} = 25 °C;	–	1.0	5.5	µA
		V_{DD} = 1.8 V; T_{amb} = 70 °C;	–	–	10	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	−1	–	1	µA
Port outputs						
I_{OL}	LOW level port sink current	V_{DD} = 3 V; V_O = 0.4 V; see Fig.12	0.7	3.5	–	mA
I_{OH}	HIGH level pull-up output source current	V_{DD} = 3 V; V_O = 2.7 V; see Fig.13	−10	−30	–	µA
		V_{DD} = 3 V; V_O = 0 V; see Fig.13	–	−140	−300	µA
I_{OH1}	HIGH level push-pull output source current	V_{DD} = 3 V; V_O = 2.6 V; see Fig.14	−0.7	−3.5	–	mA
Tone output (see Fig.15)						
$V_{HG(RMS)}$	HGF voltage (RMS value)		158	181	205	mV
$V_{LG(RMS)}$	LGF voltage (RMS value)		125	142	160	mV
$\Delta f/f$	frequency deviation		−0.6	–	0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_o \rvert$	output impedance		–	100	500	Ω
G_v	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	T_{amb} = 25 °C; note 5	–	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EEPROM (notes 1 and 6)						
$CY_{t/w}$	endurance (erase/write cycles)	note 7	10^5	–	–	
t_{ret}	data retention time		10	–	–	years
Power-on-reset (see Fig.16)						
V_{POR}	Power-on-reset level					
	PCD335xA	configuration as PCD3755A	0.8	1.3	1.8	V
	PCD335xA	configuration as PCD3755E	1.5	2.0	2.5	V
	PCA335xC	configuration as PCD3755E	1.7(8)	2.0	2.3	V
Oscillator (see Fig.17)						
g_m	transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

Notes

1. TONE output, EEPROM erase and write require $V_{DD} \geq 2.5$ V.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open; value HGF = LGF = 0, unless otherwise specified.
   a) Maximum values: external clock at XTAL1 and XTAL2 open-circuit.
   b) Typical values: T_{amb} = 25 °C; crystal connected between XTAL1 and XTAL2.
3. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; RESET, T1 and CE/T0 at V_{SS}; crystal connected between XTAL1 and XTAL2; pins T1 and $\overline{CE}/T0$ at V_{SS}.
4. Values are specified for DTMF frequencies only (CEPT).
5. Related to the Low Group Frequency (LGF) component (CEPT).
6. After final testing the value of each EEPROM bit is a logic 1, but this cannot be guaranteed after board assembly.
7. Verified on sampling basis.
8. Each device is tested on the condition: $V_{DD(min)} < V_{POR}$; to ensure a correct start-up, even for slow rising supply voltages.

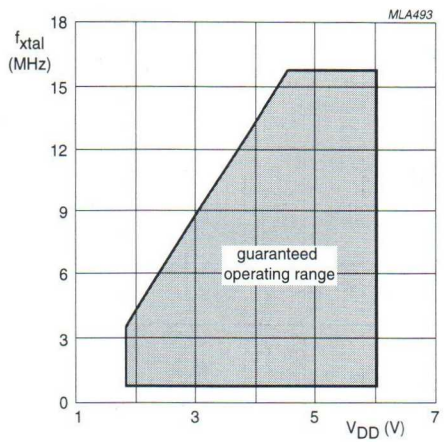
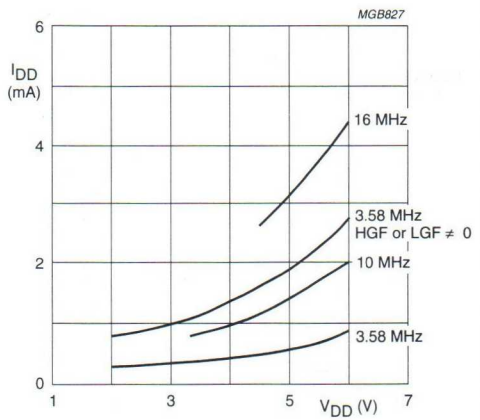
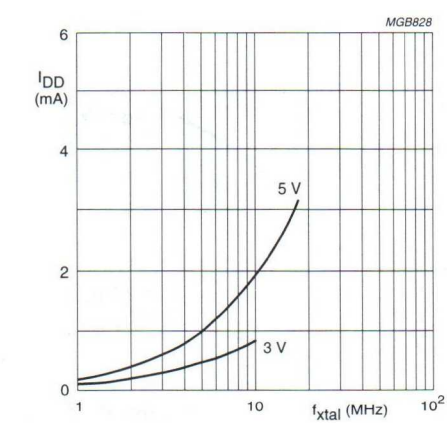


Fig.6 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).



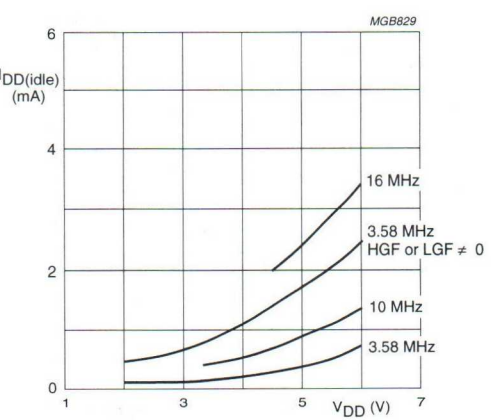
Measured with crystal between XTAL1 and XTAL2.

Fig.7 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).



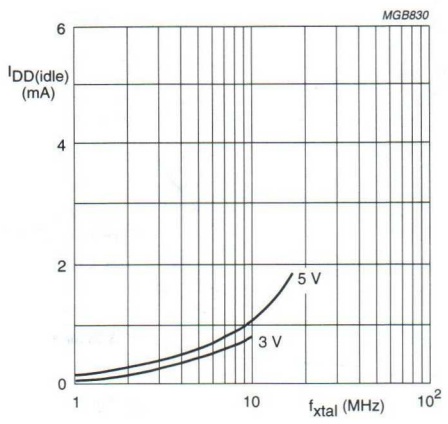
Measured with function generator on XTAL1.

Fig.8 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



Measured with crystal between XTAL1 and XTAL2.

Fig.9 Typical supply current in Idle mode ($I_{DD(idle)}$) as a function of supply voltage (V_{DD}).



Measured with function generator on XTAL1.

Fig.10 Typical supply current in Idle mode ($I_{DD(idle)}$)as a function of clock frequency (f_{xtal}).

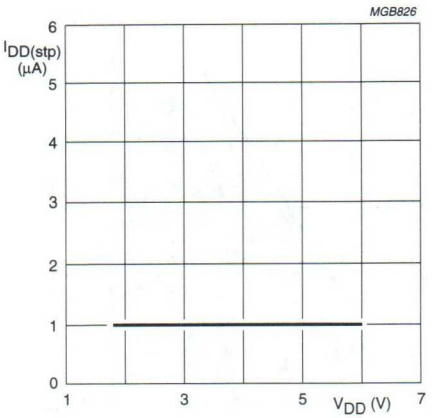
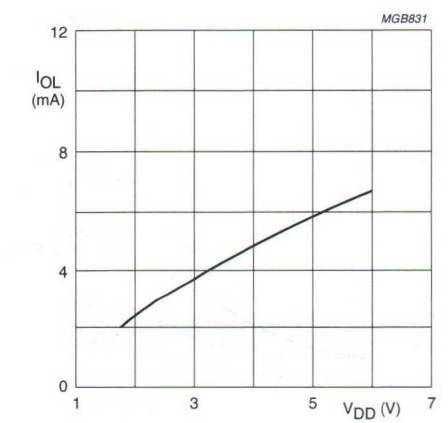


Fig.11 Typical supply current in Stop mode ($I_{DD(stp)}$) as a function of supply voltage (V_{DD}).



V_O = 0.4 V.

Fig.12 Typical LOW level output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

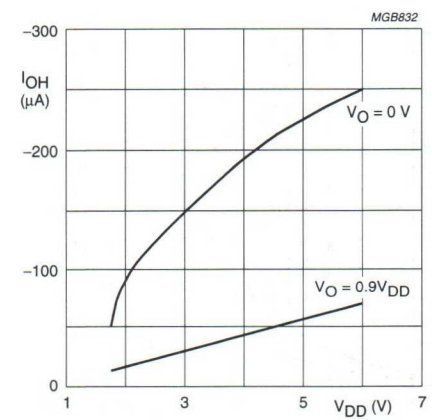
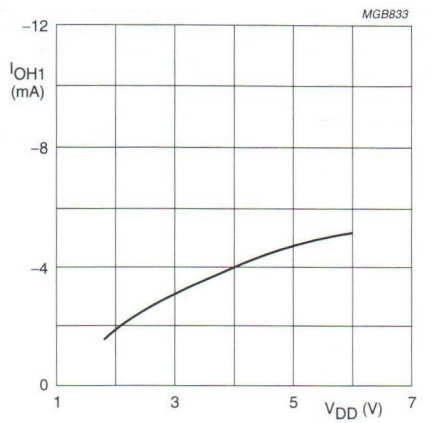
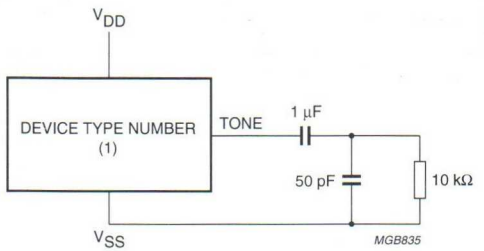


Fig.13 Typical HIGH level pull-up output source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.14 Typical HIGH level push-pull output source current (I_{OH1}) as a function of supply voltage (V_{DD}).



(1) Device type number: PCA3351C, PCA3352C, PCA3353C, PCD3351A, PCD3352A, PCD3353A or PCD3355A.

Fig.15 TONE output test circuit.

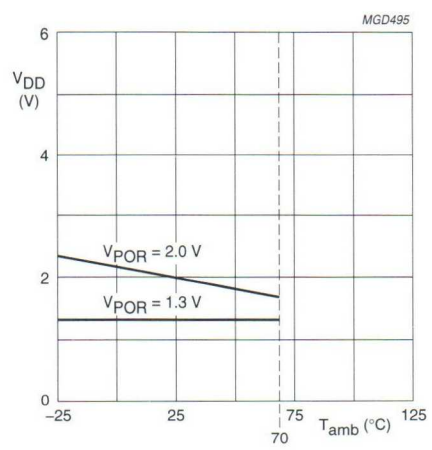


Fig.16 Typical Power-on-reset level (V_{POR}) as function of ambient temperature (T_{amb}).

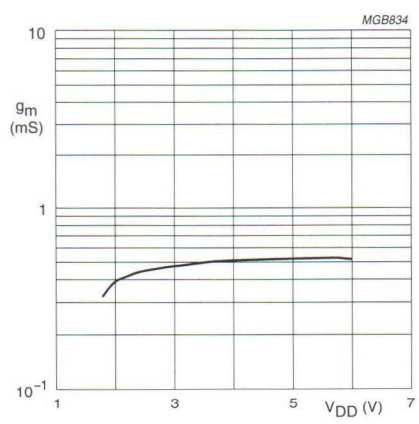


Fig.17 Typical transconductance (g_m) as a function of supply voltage (V_{DD}).

19 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = 0 to +50 °C (PCA335xC) or −25 to +70 °C (PCD335xA); all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.6	1	–	16	MHz

Multistandard repertory dialler/ringer with EEPROM

PCD3330-1

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1 FEATURES

1.1 Pulse/DTMF dialling

- Pulse, DTMF and 'mixed mode' dialling
- Mixed mode dialling: start with pulse dial, end with DTMF dial (e.g. for control of DTMF user equipment via a pulse network)
- Number of digits per call is infinite (FIFO register)
- Flash or register recall
- Connect a/b to earth function
- Mute functions
- Disconnect function
- Supports 16 dial key: 0 to 9 and *, #, A, B, C and D
- Supports up to 6 × 6 keyboard and various function keys including:
  - FLASH: calibrated line-break pulse
  - HOOK: toggle on-hook/off-hook or loudspeaker on/off
  - MUTE: activate/deactivate mute output
  - TONE: change to DTMF dialling (mixed mode)
  - DISconnect: return to on-hook state for calibrated time
- On-hook dialling control
- Country specifications which can be stored in EEPROM are:
  - * and # to be transmitted/not transmitted when switching over to DTMF dialling mode
  - mark-to-space ratio (3 : 2 or 2 : 1)
  - 6 tone time selections (60/90, 70/70, 80/80, 100/100, 100/140 or 140/140 ms)
  - 4 flash time selections (100, 115, 270 or 600 ms)
  - mute output type selection (M1, $\overline{M1}$, M2 or $\overline{M2}$)
  - microphone mute generated via the LSE output
  - DTMF keys or Function keys selection
- On-chip voltage reference for stabilized supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT compatible).

1.2 Number storage

- Redial by 'cursor' method (maximum 24 digits) stored in internal EEPROM
- Storage for 13 repertory dial numbers (16 digits each) or 10 repertory dial numbers (20 digits each) in internal EEPROM
- Access pause generation and termination: manually or by 'Atlanta' procedure
- Function keys for: LNR, Memory recall, Store, Access Pause and 1 key repertory
- Country specifications which can be stored in EEPROM are:
  - access pause time selection (1.5/1.0, 2.5/1.5, 3.0/3.5 or 6.0/6.0 s)
  - 10 number repertory dialler selection (1 or 2 key)
  - two repertory number programming procedures (General or Germany)
  - repertory length (16 or 20 digits)
  - generating a keytone during program actions.

1.3 Ringer

- Ringer input frequency detection
- Function key for: Program Ringer
- Three-tone ringer with 4 different ringer frequencies
- Ringer melody generation with four signal speeds and four output volume steps, keypad controlled
- Country specifications which can be stored in EEPROM are:
  - ringer input frequency detection selection
  - ringer output selection (via DTMF tone output or special ringer tone output)
  - 4 possible ringer melodies
  - 4 possible ringer repetition rates
  - 4 possible ringer volumes.

1.4 General

- On-chip oscillator uses low-cost 3.58 MHz (TV colour burst) crystal or PXE resonator
- On-chip power-on reset (typically 2.0 V)
- Supply voltage range 1.8 to 6.0 V (2.5 to 6.0 V in EEPROM erase/write and DTMF and ringer mode).

2 GENERAL DESCRIPTION

The PCD3330-1 is a mixed-mode multistandard repertory dialler/ringer IC fabricated in a low threshold voltage CMOS technology.

The (maximum 13) repertory numbers, redial and various country specifications are stored in EEPROM so that memory retention is guaranteed for 10 years without using a battery back-up.

National telecommunications specifications can be fulfilled by changing a few bytes in EEPROM which contain the different telephone timing and dialling procedures.

The two on-chip tone generators are used for Dual Tone Multi-Frequency (DTMF) dialling, and for generating a melody during ringing, which is activated when a correct incoming ringer frequency is detected.

As an output transducer for the ringer, a loudspeaker (ringer out via tone output) or a PXE (ringer out via the special ringer output which generates square wave ringer tones with a peak-to-peak voltage of V_{DD} to V_{SS}) can be used.

The operating supply voltage is 1.8 V (2.5 V in EEPROM erase/write and DTMF and ringer mode) to 6.0 V with a low current consumption in all operating modes: standby, conversation, dialling, programming and ringer.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3330-1P	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3330-1T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

4 PINNING

SYMBOL	PIN	DESCRIPTION
COL1	1	sense column keyboard input/programming EEPROM
COL2	2	sense column keyboard input/programming EEPROM
COL3	3	sense column keyboard input/programming EEPROM
COL4	4	sense column keyboard input/programming EEPROM
COL5	5	sense column keyboard input
COL6	6	sense column keyboard input
DMO	7	dial mode output
HOOK	8	cradle contact input
XTAL1	9	crystal/PXE oscillator input
XTAL2	10	crystal/PXE oscillator output
RESET	11	reset input
CE/RF	12	chip enable and zero crossing for ringer input
ROW1	13	scanning row keyboard output
ROW2	14	scanning row keyboard output
ROW3	15	scanning row keyboard output
ROW4	16	scanning row keyboard output
ROW5	17	scanning row keyboard output
ROW6	18	scanning row keyboard output
MUTE	19	mute output
RTO	20	ringer melody output
$\overline{DP}/\overline{FL}$	21	dial pulse/flash inverted output
V_{SS}	22	negative supply
TONE	23	DTMF tones or ringer melody output
V_{DD}	24	positive supply
PD/DTMF	25	pulse/DTMF dial selection
RVOL1	26	ringer volume output 1
RVOL2/LSE	27	ringer volume output 2 /loudspeaker enable output
EARTH	28	earth output

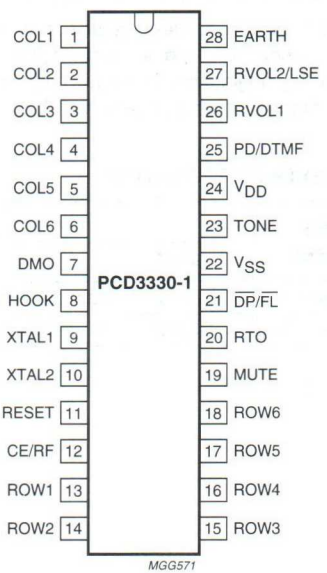


Fig.1 Pin configuration.

5 FUNCTIONAL DESCRIPTION

5.1 Inputs/Outputs

5.1.1 COL1 TO COL6, KEYBOARD INPUTS

The sense column inputs COL1 to COL6 and the scanning row outputs ROW1 to ROW6 can be directly connected to several keyboard layouts, up to a maximum 6 × 6 single contact keyboard matrix.

Four of the sense columns are used to store the contents of the EEPROM in the factory (see Section 5.3).

5.1.2 DMO, DIAL MODE OUTPUT

This output is HIGH during the make and break times in pulse dial mode. Its function is to lower the DC line voltage during these pulses.

This output is LOW during DTMF dialling, during the inter-digit-pause in pulse dial mode and during conversation mode.

5.1.3 HOOK, ON/OFF HOOK DETECTION INPUT

If inputs CE and HOOK are both HIGH then the conversation, programming or dialling mode is selected. Switching the HOOK input LOW longer than the reset-delay-time results in switching to the standby mode.

If CE = HIGH and HOOK = LOW the PCD3330-1 is in the ringer mode.

5.1.4 XTAL1 AND XTAL2, OSCILLATOR INPUT/OUTPUT

Time base for the PCD3330-1 is a crystal-controlled on-chip oscillator which is completed by connecting a 3.579545 MHz crystal or ceramic resonator (PXE) between XTAL1 and XTAL2. The XTAL2 is the oscillator output and can be used as driver for another oscillator input. A low-cost quartz crystal from Philips (code number. 4322 143 04401) is available, specially for telephony applications.
The oscillator starts when V_{DD} reaches the operating voltage level and CE = HIGH.

5.1.5 RESET, RESET INPUT

When the RESET pin is connected to V_{SS}, a reset is generated by an internal power-on-reset circuit, which produces an internal reset pulse every time that the supply voltage V_{DD} crosses the power-on-reset voltage level (typ. 2.0 V).

Depending on the application it can be necessary to generate a reset via an external circuit (e.g. an external RC network). When the RESET input becomes HIGH it initializes the IC.

The RESET-pin should not be left open (not-connected) in any circumstances.

5.1.6 CE/RF, CHIP ENABLE AND RINGER-FREQUENCY DETECT INPUT

As chip enable input (active HIGH) it is used to initialize part of the system, to switch from standby to the ringer or conversation, programming or dialling mode and to detect line breaks.

As ringer-frequency input it measures the time between two LOW-to-HIGH transitions, thus measuring the ringer frequency.

5.1.7 ROW1 TO ROW6, KEYBOARD OUTPUTS

The scanning row outputs ROW1 to ROW6 and the sense column inputs COL1 to COL6 can directly be connected to several keyboard layouts (max. a 6 × 6 single contact keyboard matrix).

5.1.8 MUTE, MUTE OUTPUT

The MUTE output is used during dialling. In the PCD3330-1 the MUTE output has four different selectable options:

- M1, normally LOW, but HIGH during inter-digit-pause and make/break in pulse dial mode, during tone-on and tone-off in DTMF mode, and during flash or earth
- $\overline{M1}$, the inverted signal of M1
- M2, normally LOW, HIGH during make/break in pulse dial mode, during tone-on in DTMF mode, and during flash or earth
- $\overline{M2}$, the inverted signal of M2.

Each time the M-key on the keyboard is pressed the MUTE output goes to its inverted state.

5.1.9 RTO, RINGER TONE OUTPUT

This is the special ringer output. When this output is selected the output of the internal tone generators is not connected to the TONE output but to this RTO output. The ringer output signal has a peak to peak square output voltage of $V_{DD} - V_{SS}$ (this is used with a PXE transducer).

5.1.10 $\overline{DP}/\overline{FL}$, PULSE DIALLING AND REGISTER RECALL OUTPUT

The $\overline{DP}/\overline{FL}$ output drives an external switching transistor in pulse dial mode.

It pulses a calibrated FLASH or register recall pulse (if selected) when the keyboard input FLASH is pressed.

5.1.11 V_{DD} AND V_{SS}

V_{DD} and V_{SS} are the supply terminals.

5.1.12 TONE, DTMF OR RINGER TONE OUTPUT

In DTMF dialling mode the dual tones which are provided at the output TONE are filtered by an on-chip switched capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT recommendations. An on-chip reference voltage provides output tone levels independent of supply voltages. The impedance is 100 Ω typically.

In ringer mode this TONE output can be used for generating the ringer output tones. Whether this TONE output or the special RTO (ringer tone) output is used is selected via EEPROM.

5.1.13 PD/DTMF, PULSE/TONE MODE SELECTION

To select the dialling mode, this input PD/DTMF must be connected to V_{DD} or V_{SS}.

PD/DTMF = HIGH (V_{DD}) = DTMF mode.
PD/DTMF = LOW (V_{SS}) = pulse mode.

The PCD3330-1 accept the information also during manual dialling. Switching the input to pin PD/DTMF changes the dialling mode after finishing the digit in progress.

5.1.14 RVOL1 AND RVOL2/LSE, RINGER VOLUME OUTPUTS

The RVOL1 and RVOL2 outputs can be used to control the ringer output volume in four steps. The volume can be changed via keyboard during ringing or conversation mode (off-hook). The selected output level is stored in EEPROM.

During on-hook dialling the RVOL2 output becomes the LSE output for switching the listening-in amplifier.

When the on-hook dialling option is not selected and the microphone mute option is active output LSE change to a microphone mute which is controlled by the M-key. After off-hook this output is HIGH and will toggle by every press off the M-key.

5.1.15 EARTH, a/b LINE TO EARTH CONNECTION

The EARTH output drives an external switching transistor. which connects the a- or b-line to earth.

It pulses a calibrated EARTH pulse (if selected) when the keyboard input FLASH is pressed.

5.2 Keyboard

The PCD3330-1 is programmed to work with various keyboards which can be connected to the sense column inputs COL1 to COL6 and the scanning row outputs ROW1 to ROW6. In this specification four examples are given:

- Figure 2. The simplest keyboard. All basic functions are available but only 2-key abbreviated dialling (MEM + digit) is possible.
- Figure 3. As Fig.2 but with 3 extra 1-key abbreviated dialling keys.
- Figure 4. As Fig.2 but the 10 repertory numbers can be reached via M0 to M9 with 1-key abbreviated dialling.
- Figure 5. The most complex keyboard. A second possibility for column 4 exists. This column can be selected via EEPROM.

Keyboard entries are valid 20 ms (debounce time) after the leading edge of a keyboard entry.

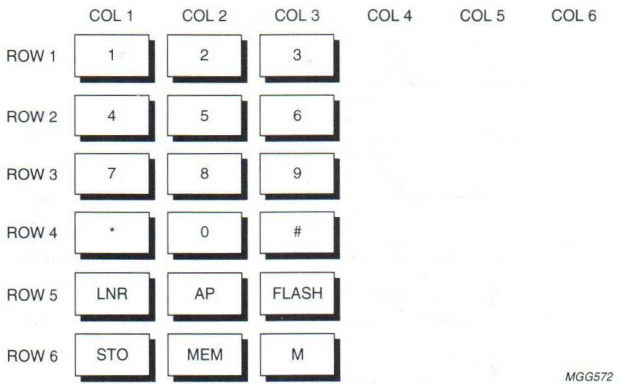


Fig.2 Basic keyboard.

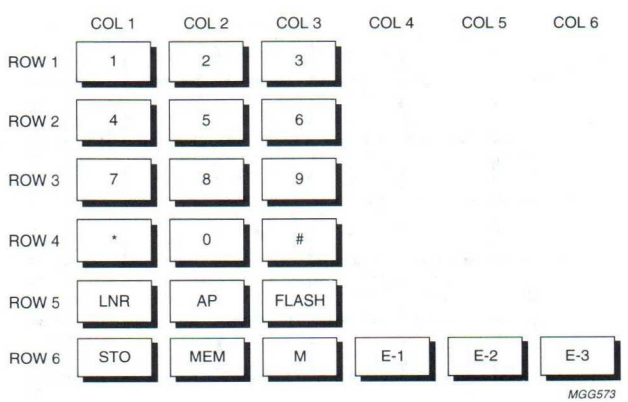


Fig.3 Basic keyboard with 3 extra 1-key abbreviated dialling keys.

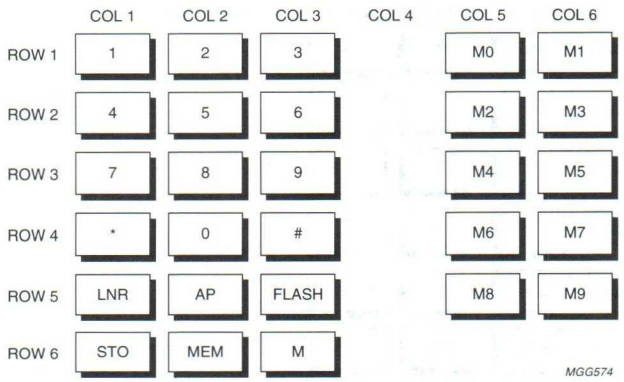


Fig.4 Basic keyboard with 10 extra 1-key abbreviated dialling keys.

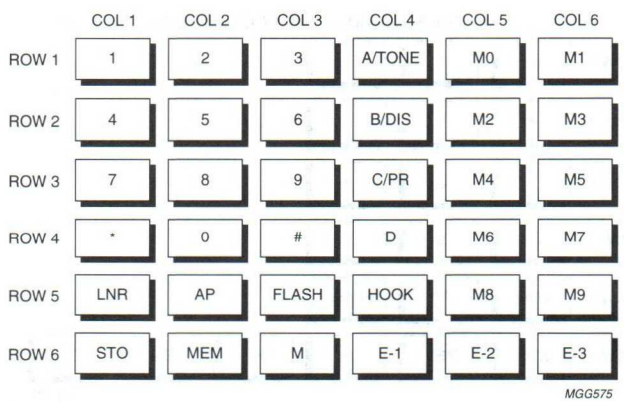


Fig.5 The most complex keyboard, option for column 4 is programmed into EEPROM.

Table 1 Function of the keys

SYMBOL	DESCRIPTION
0 to 9, * and #	Standard keyboard. In pulse dialling mode the valid keys are the 10 numeric keys (0 to 9) – the 2 non-numeric dial keys (* and #) have no effect on the dialling. In DTMF dialling mode the 10 numeric keys and the 2 non-numeric dial keys are valid.
A to D	If selected (EEPROM bit), these keys are only valid in DTMF dialling mode.
TONE	If selected, pulse to DTMF switching key (mixed mode dialling).
DIS	If selected (EEPROM bit), disconnect key will activate output $\overline{DP}/\overline{FL}$ for 800 ms. In this case the telephone set turns to the ON-HOOK state for this calibrated time.
PR	If selected (EEPROM bit), program ringer key. With this key the ringer output volume and ringer repetition rate can be changed.
M0 to M9	One key abbreviated dialling, the 10 repertory numbers are directly accessible via keys M0 to M9.
LNR	Last number redial.
AP	Access pause key, results in inserting an access pause in the telephone number.
FLASH	FLASH/EARTH key, depending on the status programmed this key starts a FLASH or an EARTH procedure.
HOOK	Hook key (for on-hook dialling/loudspeaker on/off); as long as the handset stays on the cradle activation of this key switches the set off-hook/on-hook. When the handset is not on the cradle activation of this key switches the loudspeaker on/off (listening-in feature).
STO	STORE key.
MEM	Two-key abbreviated dialling (MEM + digit), the repertory numbers M0 to M9 are also accessible via this two-key dialling procedure.
M	Mute key, each time this key is pressed and dialling is not active, the mute output goes to HIGH or LOW depending on the previous state.
E-1 to E-3	One key abbreviated dialling, three extra repertory numbers which are only directly accessible by keys E-1 to E-3; these numbers can only be used when the repertory length is 16 digits (programmable in EEPROM).

5.3 EEPROM organization and programming procedures

5.3.1 EEPROM ORGANIZATION

The dialling, memory, and ringer options and the telephone numbers are all stored in EEPROM. By using EEPROM no special backup requirement are necessary such as battery, current from the line, or very big capacitors.
Table 2 describes the meaning of each EEPROM byte at a repertory length of 16 and 20 digits.
Table 3 describes the meaning of each bit of all the bytes that do not contain telephone numbers.

Table 2 EEPROM organization

FUNCTION	REPERTORY LENGTH IS 16 DIGITS		REPERTORY LENGTH IS 20 DIGITS	
	LENGTH	BYTE PLACES	LENGTH	BYTE PLACES
Redial	13 bytes	0 to 12	13 bytes	0 to 12
M0 or MEM + 0	8 bytes	16 to 23	10 bytes	16 to 25
M1 or MEM + 1	8 bytes	24 to 31	10 bytes	26 to 35
M2 or MEM + 2	8 bytes	32 to 39	10 bytes	36 to 45
M3 or MEM + 3	8 bytes	40 to 47	10 bytes	46 to 55
M4 or MEM + 4	8 bytes	48 to 55	10 bytes	56 to 65
M5 or MEM + 5	8 bytes	56 to 63	10 bytes	66 to 75
M6 or MEM + 6	8 bytes	64 to 71	10 bytes	76 to 85
M7 or MEM + 7	8 bytes	72 to 79	10 bytes	86 to 95
M8 or MEM + 8	8 bytes	80 to 87	10 bytes	96 to 105
M9 or MEM + 9	8 bytes	88 to 95	10 bytes	106 to 115
E-1	8 bytes	96 to 103	not available	–
E-2	8 bytes	104 to 111	not available	–
E-3	8 bytes	112 to 119	not available	–
Options	4 bytes	120 to 123	4 bytes	120 to 123
Program Blocking	1 byte	127	1 byte	127

Table 3 Option bit status and location

FUNCTION	EEPROM BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not sending *	120	X	X	X	X	X	X	X	0
Sending *	120	X	X	X	X	X	X	X	1
Not sending #	120	X	X	X	X	X	X	0	X
Sending #	120	X	X	X	X	X	X	1	X
Mark to space ratio 3 : 2	120	X	X	X	X	X	0	X	X
Mark to space ratio 2 : 1	120	X	X	X	X	X	1	X	X
Tone/pause 60/90 ms	120	X	X	0	0	0	X	X	X
Tone/pause 70/70 ms	120	X	X	0	0	1	X	X	X
Tone/pause 80/80 ms	120	X	X	0	1	0	X	X	X
Tone/pause 100/100 ms	120	X	X	0	1	1	X	X	X
Tone/pause 100/140 ms	120	X	X	1	0	0	X	X	X
Tone/pause 140/140 ms	120	X	X	1	0	1	X	X	X
Flash duration 100 ms	120	0	0	X	X	X	X	X	X
Flash duration 115 ms	120	0	1	X	X	X	X	X	X
Flash duration 270 ms	120	1	0	X	X	X	X	X	X
Flash duration 600 ms	120	1	1	X	X	X	X	X	X
Mute is M1	121	X	X	X	X	X	X	0	0
Mute is $\overline{M1}$	121	X	X	X	X	X	X	0	1
Mute is M2	121	X	X	X	X	X	X	1	0
Mute is $\overline{M2}$	121	X	X	X	X	X	X	1	1
General program proc.	121	X	X	0	X	X	X	X	X
General program proc.	121	X	X	1	X	X	X	X	X
Repertory 16 digits	121	X	0	X	X	X	X	X	X
Repertory 20 digits	121	X	1	X	X	X	X	X	X
M1/M2 mute	121	0	X	X	X	X	X	X	X
Microphone mute	121	1	X	X	X	X	X	X	X
Access Pause time for pulse dialling (Inter-digit pause not included)									
A.P. time 1.5 s	121	X	X	X	0	0	X	X	X
A.P. time 2.5 s	121	X	X	X	0	1	X	X	X
A.P. time 3.0 s	121	X	X	X	1	0	X	X	X
A.P. time 6.0 s	121	X	X	X	1	1	X	X	X
Access Pause time for DTMF dialling (Tone-off time not included)									
A.P. time 1.0 s	121	X	X	X	0	0	X	X	X
A.P. time 1.5 s	121	X	X	X	0	1	X	X	X
A.P. time 3.5 s	121	X	X	X	1	0	X	X	X
A.P. time 6.0 s	121	X	X	X	1	1	X	X	X

FUNCTION	EEPROM BYTE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Ringer via pin RTO	122	X	X	X	X	X	X	X	0
Ringer via pin TONE	122	X	X	X	X	X	X	X	1
Ringer melody A	122	X	X	X	X	0	0	X	X
Ringer melody B	122	X	X	X	X	0	1	X	X
Ringer melody C	122	X	X	X	X	1	0	X	X
Ringer melody D	122	X	X	X	X	1	1	X	X
Ringer volume 1	122	X	X	0	0	X	X	X	X
Ringer volume 2	122	X	X	0	1	X	X	X	X
Ringer volume 3	122	X	X	1	0	X	X	X	X
Ringer volume 4	122	X	X	1	1	X	X	X	X
Ringer repetition 1	122	0	0	X	X	X	X	X	X
Ringer repetition 2	122	0	1	X	X	X	X	X	X
Ringer repetition 3	122	1	0	X	X	X	X	X	X
Ringer repetition 4	122	1	1	X	X	X	X	X	X
Ringer detection LOW 1	123	X	X	X	X	X	X	0	0
Ringer detection LOW 2	123	X	X	X	X	X	X	0	1
Ringer detection LOW 3	123	X	X	X	X	X	X	1	0
Ringer detection LOW 4	123	X	X	X	X	X	X	1	1
Ringer detection HIGH 1	123	X	X	X	X	0	0	X	X
Ringer detection HIGH 2	123	X	X	X	X	0	1	X	X
Ringer detection HIGH 3	123	X	X	X	X	1	0	X	X
Ringer detection HIGH 4	123	X	X	X	X	1	1	X	X
A to D keys	123	X	X	X	0	X	X	X	X
Function keys	123	X	X	X	1	X	X	X	X
Flash keytone	123	X	X	0	X	X	X	X	X
EARTH function	123	X	X	1	X	X	X	X	X
No keytone	123	X	0	X	X	X	X	X	X
Keytone active	123	X	1	X	X	X	X	X	X
No on-hook dialling	123	0	X	X	X	X	X	X	X
On-hook dialling control	123	1	X	X	X	X	X	X	X

5.3.2 EEPROM PROGRAMMING PROCEDURES

The PCD3330-1 supports four EEPROM programming procedures:

1. LNR is described in Section 5.6.2
2. Repertory numbers is described in Section 5.6.9
3. Via pins 1 to 4 (COL1 to COL4)
4. Via keyboard (can be locked with the **Program Blocking** byte).

Method 3 is normally used by the setmaker before the set leaves his factory.
Method 4 is most suited for usage in the field (e.g. the shop where the set is purchased).

5.3.2.1 Factory EEPROM programming procedure

The COL1 to COL4 of the PCD3330-1 can be used in the factory to read or write the contents of the internal EEPROM. COL1 (pin 1) is the SCL and COL2 (pin 2) is the SDA of the I^2C-bus interface, while COL3 (pin 3) and COL4 (pin 4) determine the mode selected. In Fig.6 the principle for this programming procedure is given.

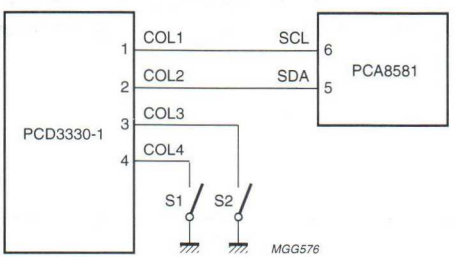


Fig.6 Circuit diagram for the EEPROM programming procedure.

The status of pins COL3 and COL4 is read directly after a power-on-reset and the status can be changed with switches S1 and S2 (open: pin is HIGH; closed: pin is LOW).

Table 4 Function of switches S1 and S2

S1	S2	MODE
open	open	normal mode
closed	open	test mode: PCD3330-1 EEPROM write
closed	closed	test mode: PCD3330-1 EEPROM read

If during the programming mode S1 is opened the programming stops and the PCD3330-1 goes to the telephone mode. If now S1 is closed again the set stays in telephone mode.

In the write mode the PCD3330-1 is able to read the contents of an external RAM (128 bytes) or the PCF8581 (EEPROM) via COL1 and COL2.

In the read mode the PCD3330-1 sends the contents of its internal EEPROM via COL1 and COL2 to the external device.

All 128 bytes of EEPROM are read or written in each read or write operation.

5.3.2.2 EEPROM programming procedures via keyboard

This procedure is only active if EEPROM **Program Blocking** byte (number 127 of the internal EEPROM) is set to 'FF' hex. If this byte is '00' hex it is not possible to do the program procedures described in this chapter.
Byte 127 of the EEPROM can only be set by the factory EEPROM programming procedure.

In the field all telephone options can be changed easily by a special program procedure:

- Depress the STO-key (this selects the program mode)
- Depress the LNR-key (switches the program module to storing EEPROM options
- Depress the first key of a three digit access code (the 1)
- Depress the second key of a three digit access code (the 6)
- Depress the third key of a three digit access code (the 0)
- Depress the LNR-key again (end the access code)
- Press the byte number (last digit of the EEPROM byte number given in Table 2)
- Press the number of the bit to change (see Table 2)
- Press 0 or 1 (this changes the EEPROM bit contents)
- Depress the LNR-key, which stores the correction into EEPROM, now select a new byte or go to end
- End the routine by pressing the STO-key again.

If during this procedure a mistake is made correction is possible after proper access code by pressing the LNR-key and during access code only by STO-key.
In all cases the routine can be ended by pressing the STO-key.

Example:

Change the mark-to-space ratio from 3 : 2 to 2 : 1. Then bit 2 of EEPROM byte-120 has to be changed from 0 to 1. The necessary action is as follows:

- Depress the STO-key
- Depress the LNR-key
- Depress the 1-key (first digit access code)
- Depress the 6-key (second digit access code
- Depress the 0-key (third digit access code)
- Depress the LNR-key again (end the access code)
- Press the 0-key (last digit of EEPROM byte-120 is the 0)
- Press the 2-key (bit 2 has to be changed)
- Press the 1 (changes the mark-to-space ratio to 2 : 1)
- Press the LNR or STO-key.

The STO-key will end the programming procedure, whereas after the LNR-key a new byte can be selected to have the required bit changed.

5.4 Operation mode overview

The PCD3330-1 has in total five operation modes: standby, conversation, ringer, dialling and programming. The state diagram is given in Fig.7.

When both CE/RF and the HOOK input are LOW the PCD3330-1 goes to the standby mode, in which the contents of the redial register is refreshed, the oscillator switched off and the device enters the low current state.

A HIGH state on the CE/RF and/or the HOOK input will cause a complete initialization of the PCD3330-1 which means setting of the I/O pins, clearing of the RAM and reloading the EEPROM contents into it.

5.5 Pulse/DTMF dialling function

5.5.1 PULSE/DTMF MODE SELECTION BY PIN

The PCD3330-1 has two dialling modes, pulse dialling and Dual Tone Multi Frequency (DTMF). These can be selected via the PD/DTMF input in the following way:

PD/DTMF = HIGH (V_{DD}) = DTMF mode.
PD/DTMF = LOW (V_{SS}) = pulse mode.

The controller accepts the information also during manual dialling. Switching the input to the pin PD/DTMF changes the dialling mode after transmitting the digit in progress.

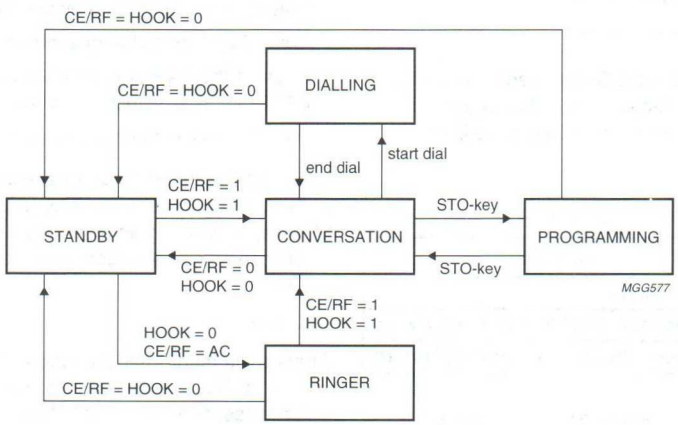


Fig.7 State diagram of the PCD3330-1 dialler/ringer.

5.5.2 Pulse dialling (PD/DTMF = LOW)

The keyboard entry initiates a recall of a previously stored number or is a simultaneous keying-in and pulsing-out activity, with storing for possible later recall. If in the recalled number or at keying-in the keys A,B,C or D (options A to D keys selected) are used these digits are not transmitted.
If at keying-in the keys * or # are used this results in a switch over to DTMF dialling. Normally, keying in is faster than pulsing-out (fed from the redial register). Pulse sequences start with an inter-digit pause of 840 ms duration, followed by a sequence of pulses corresponding to the present digit in store. Each pulse starts with a mark (line break) followed by space (line make).
The pulse period is 100 ms with a mark-to-space ratio of 3 : 2 or 2 : 1 (mark-to-space ratio selection). After transmission of a digit, the next digit is processed, again starting with an inter-digit pause. The pulses are available at the $\overline{DP}/\overline{FL}$ output and can be used to drive an external switching transistor in pulse dialling mode.
The transmission IC is put in the dialling mode by means of output MUTE.

Output MUTE has several programmable options, MUTE can be configured as M1, $\overline{M1}$, M2 and $\overline{M2}$. In Fig.8 the timing diagram of these output possibilities is given.
After completion of the number string the circuit changes from dialling mode to conversation mode.

5.5.3 Dual tone multi frequency (DTMF) dialling (PD/DTMF = HIGH)

The PCD3330-1 converts keyboard inputs into data for the on-chip DTMF generator. Tones are transmitted via output TONE with six programmable minimum tone burst/pause durations of 60/90, 70/70, 80/80, 100/100, 100/140 or 140/140 ms. The maximum tone burst duration is equal to the key depression time. With redial and repertory dialling tones are automatically fed at the programmed rate. Again the MUTE output has several programmable options namely, M1, $\overline{M1}$, M2 and $\overline{M2}$.
In Fig.9 the timing diagram of these output possibilities is given.

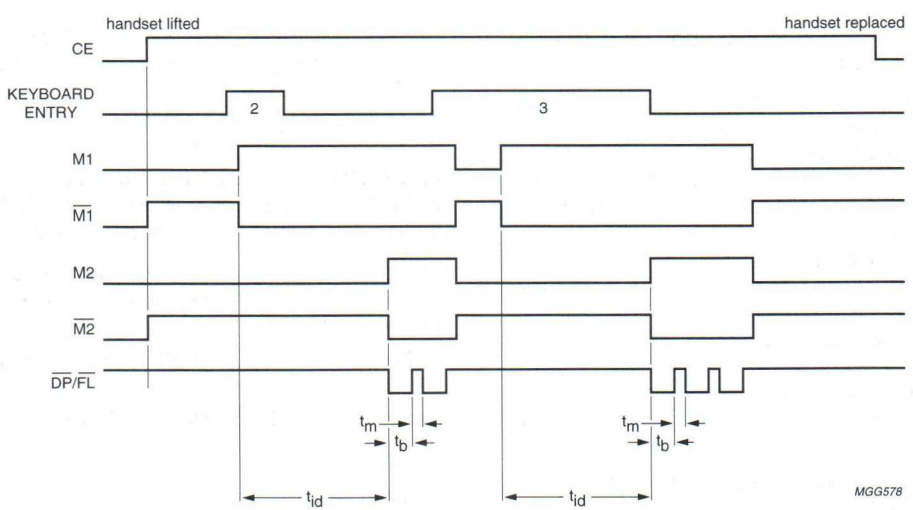


Fig.8 Timing diagram in pulse mode, showing $\overline{DP}/\overline{FL}$ and MUTE outputs.

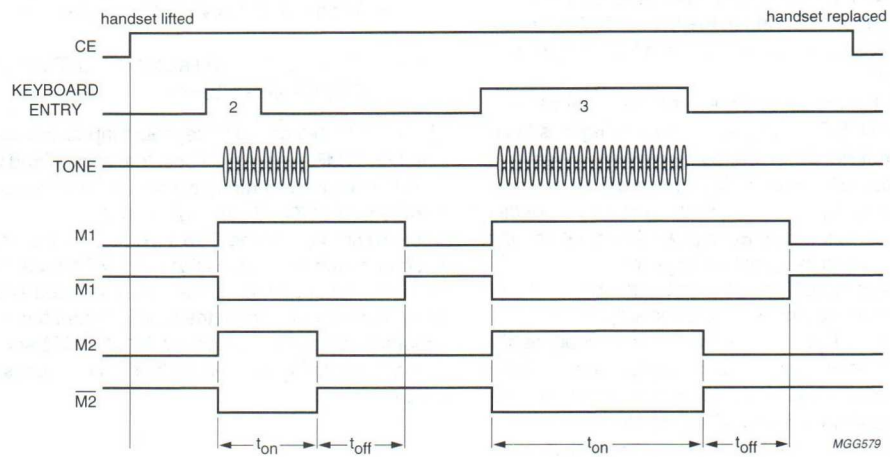


Fig.9 Timing diagram in DTMF mode, showing MUTE outputs.

5.5.4 DTMF DIALLING IN PULSE DIALLING MODE (MIXED MODE DIALLING)

If the controller is set to the pulse dial mode (pin PD/DTMF is LOW), activation of keys TONE, * or # changes the dialling mode to DTMF.
Its entry is stored in the redial register and it generates automatically an access pause, after which the following digits are transmitted in the DTMF mode.
The digits entered after keys TONE, * or # are not transmitted in the redial mode. The TONE key is never transmitted in the redial mode.
The TONE key is never transmitted, whether * or # are transmitted depends on the selected option.
A second touch of the TONE key is ignored. The * or # keys pressed after a switch over to DTMF dialling are all transmitted.

If the controller is initially set to the DTMF mode (pin PD/DTMF is HIGH), activation of TONE is ignored and the * or # are stored in the redial register and transmitted in DTMF mode.

5.5.5 FLASH OR EARTH FUNCTION

Whether the Flash or Earth function is activated by the FLASH key is programmed in the EEPROM.

If the FLASH function is selected a calibrated FLASH pulse (recall register) is generated on the $\overline{DP}/\overline{FL}$ output and the MUTE output is active.
The calibrated FLASH time is programmed for 100, 115, 270 or 600 ms in EEPROM.

If the EARTH ('Connect a/b to earth') function is selected, the EARTH output becomes HIGH and the MUTE output is active. The time of earth connection is 400 ms.

When the FLASH key is pressed the telephone number entered before the FLASH key is stored in the redial register (EEPROM).

- After dialling 1 - 2 - 3 - 'FLASH' - on-hook Redial is 1 - 2 - 3
- After dialling 1 - 2 - 3 - 'FLASH' - 4 - 5 - 6 - on-hook Redial is 4 - 5 - 6.

5.5.6 DISCONNECT FUNCTION

This DIS (disconnect) key is only available if the function key option is programmed. Touching the DIS key activates output $\overline{DP}/\overline{FL}$ for 800 ms. In this case the telephone set turns to the ON-HOOK state for this calibrated time, after which it comes back to the OFF-HOOK mode.

5.5.7 MUTE FUNCTION (M-KEY)

When no dialling or programming is active, every time this M-key is pressed the MUTE output goes to the active or inactive state depending on its previous status.
When the MUTE output is in the active state and another key is pressed then the MUTE output is switched back to the inactive state.

When there is the on-hook dialling is not selected and the Microphone mute flag in EEPROM is HIGH, every press off the M-key will result in the inverted value of the RVOL2/LSE output. At off-hook the status of this output is HIGH.

5.5.8 ON-HOOK DIALLING CONTROL

If required, the on-hook dialling control feature can be selected by programming the corresponding bit in EEPROM.
When this on-hook dialling feature is selected, the power supply to the PCD3330-1 must be maintained during on-hook.

In telephone sets developed for on-hook dialling (an electronic hook-switch must be present) activation of the HOOK-key during on-hook results in an off-hook via the $\overline{DP}/\overline{FL}$ output, and the LSE output becomes HIGH. As long as the handset stays on the cradle a new activation of the HOOK-key results in an on-hook, and the LSE output becomes LOW.

When during on-hook dialling the handset is lifted from the cradle the on-hook dialling mode is switched off and the LSE output is set to the active (LOW) state.

When the handset is off-hook (not on the cradle) activation of this HOOK-key switches the loudspeaker on (LSE = HIGH) or off (LSE = LOW) (listening-in feature).

5.6 Number storage, transmission and redial

5.6.1 NUMBER STORAGE AND TRANSMISSION

If the first key pressed at off-hook is 0 to 9 in pulse dialling or 0 to 9, * and # in DTMF dialling mode, digits are entered into the work register and compared with the previous entries stored in the redial register. As long as the newly dialled digits are equal to those stored, the contents of the redial register are unaffected.

When the newly pressed digit is different from the one stored in the redial register the contents of the work register are copied to the redial register when going on-hook (or every other action equal to on-hook).

Up to 24 digits can be stored in the redial register. After the work register overflows, a 10 digits First-In-First-Out register (FIFO) takes over as buffer and the contents of the work register is now copied to the redial register.
After transmitting the first digit of the FIFO register this position is automatically cleared to provide space for the storage of new data. In this way, the total number that can be transmitted is unlimited, provided the key-in rate is not excessive. However, if the FIFO register overflows (more than 10 digits in store) further input is ignored.

Input digits are transmitted immediately with minimum transmission time. Transmission continues for as long as digits are input.

5.6.2 LAST NUMBER REDIAL (1 TO 24 DIGITS)

If the first key pressed and released is LNR, the stored number in the redial register is recalled and transmitted immediately.

The LNR key can be used in two other ways, known as the 'cursor' method and the 'Atlanta' procedure, to allow external numbers to be redialled from a PABX with an appropriate access pause.

5.6.3 ACCESS PAUSE BY CURSOR METHOD

If the first key entered is not LNR but numerical digits, these digits are compared to those held in store. As long as the digits entered equal those stored, the redial register in not cleared and dialling can be continued by pressing the redial key. The already dialled part is not redialled. Redial is inhibited as soon an entry is unequal to the digit at the same position held in store.

This 'cursor' method allows an access code to be entered and access confirmation tone to be received before an external number is redialled.

5.6.4 ACCESS PAUSE BY ATLANTA PROCEDURE

If the first key entered is the redial key, but this key is kept down, then only the first digit held in the redial register is transmitted. After releasing the redial key the remaining digits held in the redial register are dialled.

The 'Atlanta' procedure allows a single stored access digit to be transmitted, but redial of the external number to be delayed until access has been confirmed.

5.6.5 10-NUMBER REPERTORY DIALLING

The PCD3330-1 includes a 10-number repertory dialler, 16 or 20 digits each, which is accessible with a one or two-key procedure.

The 10 repertory numbers can be recalled with the M0 to M9 keys or by pressing the MEM key followed by a numeric digit from 0 to 9.
If the keyboard matrix contains the keys M0 to M9, each of the 10 repertory numbers can be recalled using the corresponding single key.
If the keyboard matrix contains the MEM key each of the 10 repertory numbers can be recalled by depressing MEM followed by the numeric digit 0 to 9.

The maximum length of these repertory numbers is 16 or 20 digits (depending on the programmed repertory number length) including the manually stored access pauses.

5.6.5.1 Chain dialling

Repertory numbers can be dialled-out after or before entering manual dialling or last number redial and by entering the memory locations in successive order ('chain dialling').
During transmission of a number recalled from the memory location, the controller does not accept keyboard entries. Dialling can be continued as soon as the number under transmission is completed.
Note that the last memory location which is transmitted is stored in the redial register.

5.6.6 3-NUMBER REPERTORY DIALLING

When the repertory length programmed in EEPROM is set to 16 digits, the PCD3330-1 includes also an additional 3-number repertory dialler.
These repertory numbers are only accessible with the one-key procedure.

These 3 repertory numbers can only be recalled with the E-1 to E-3 keys.

The maximum length of these repertory numbers is 16 digits including the manually stored access pauses. The chain dialling procedure is equal to that explained in 10-number repertory dialling.

5.6.7 ACCESS PAUSE STORAGE

If during entering a telephone number via keyboard for normal dialling or during repertory number programming the AP-key (access pause key) is pressed, then an access pause is stored in the redial or repertory dial register.

5.6.8 MANUAL ACCESS PAUSES

The AP-key is used to insert an access pause during manual dialling. It is possible to select between four possible access pause times for each dialling mode:

For pulse dialling 1.5, 2.5, 3.0 or 6.0 s (inter-digit pause not included).
For DTMF dialling 1.0,1.5, 3.5 or 6.0 s (inter-digit pause not included).

5.6.9 STORING REPERTORY NUMBERS

When the Keytone active bit in EEPROM is HIGH, every key activation in programming mode will result in a keytone of 1046 Hz lasting 200 ms.

The store mode starts after going off-hook and depressing the STO-key. With the PCD3330-1 a selection can be made between two store modes, the 'General' and the 'German'.

Repertory numbers can be stored into EEPROM via the one-key access or the two-key access method and following the German or General storing procedures. This is detailed in Tables 5 and 6.

Table 5 One-key access repertory number mode (M0 to M9 and E-1 to E-3)

GENERAL PROCEDURE	GERMAN PROCEDURE
Set in operation mode	set in operation mode
Depress STO (store key)	depress STO (store key)
Telephone number	location (M0 to M9/E-1 to E-3)
Depress STO (store key)	telephone number
Location (M0 to M9/E-1 to E-3)	STO (store key)

Table 6 Two-key access repertory number mode (MEM + 0 to 9)

GENERAL PROCEDURE	GERMAN PROCEDURE
Set in operation mode	set in operation mode
Depress STO (store key)	depress STO (store key)
Telephone number	depress MEM (location key)
Depress STO (store key)	depress 0 to 9 (real location)
Depress MEM (location key)	telephone number
Depress 0 to 9 (real location)	depress STO (store key)

Memory locations can be cleared by following the same procedure as for storing a number, without actually entering a number.

5.7 Ringer function

The PCD3330-1 has a three-tone melody ringer with the following characteristics:

- Ringer output pin selection
- Ringer input frequency measurement
- Ringer melodies selection
- Ringer volume change during conversation and ringer mode
- Ringer repetition rate change during conversation and ringer mode.

In Fig.10 the timing diagram of the ringer function is given.

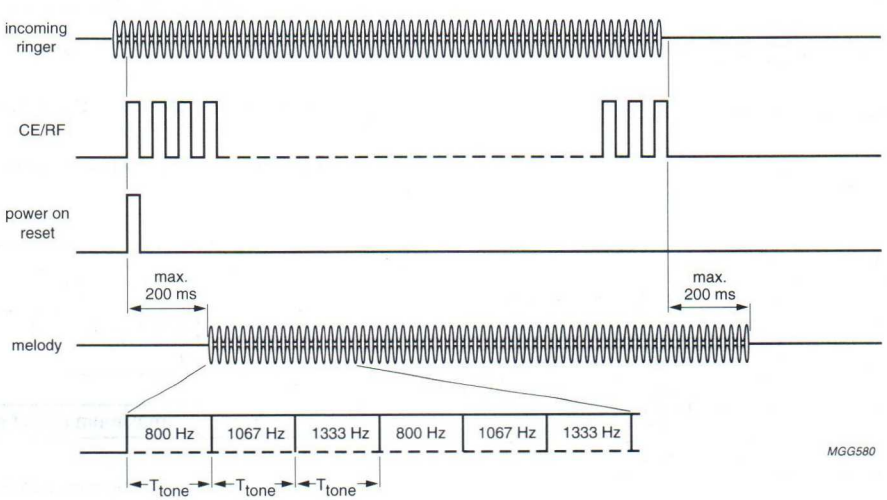


Fig.10 The timing diagram of the ringer function.

5.7.1 Ringer output pin selection

The ringer signal is sent via the special Ringer Tone Output (RTO) or via the TONE output depending on the option selected.
When a loudspeaker is used as a transducer, it is better to use the TONE output. One of the internal tone generators directly supplies this output with V_{RMS} = 181 mV.
The RTO output signal, used for PXE transducers, is a block with a peak-to-peak output voltage of $V_{DD} - V_{SS}$.

5.7.2 Ringer input frequency measurement

The melody ringer becomes active for all incoming ringer frequencies higher then the ringer detection LOW frequency and lower then the ringer detection HIGH frequency supplied to the CE/RT input of the PCD3330-1. The ringer detection LOW and ringer detection HIGH frequencies are selected such that it is possible to use this PCD3330-1 for both single and double phase rectifier applications. It is possible to select one out of four ringer detection LOW and four ringer detection HIGH frequencies options which are given below:

- Ringer detection LOW 1: 16 Hz
- Ringer detection LOW 2: 20 Hz
- Ringer detection LOW 3: 32 Hz
- Ringer detection LOW 4: 40 Hz
- Ringer detection HIGH 1: 35 Hz
- Ringer detection HIGH 2: 60 Hz
- Ringer detection HIGH 3: 70 Hz
- Ringer detection HIGH 4: 120 Hz.

5.7.3 Ringer melodies selection

The ringer melody generator can select out of four different ringer melody options (stored in EEPROM), given in Table 7.

Table 7 Ringer melody options

RINGER MELODY	FREQ. 1 (Hz)	FREQ. 2 (Hz)	FREQ. 3 (Hz)
Ringer melody A	738	826	925
Ringer melody B	800	1067	1333
Ringer melody C	1455	1621	1810
Ringer melody D	1995	2223	2510

5.7.4 Ringer volume change during conversation and ringer mode

The ringer volume can be controlled by the port pins RVOL1 and RVOL2 and its value is stored in EEPROM.

The output volume can be changed:

- Via the EEPROM programming procedure (see Section 5.3.2)
- During conversation mode, when the function keys option is chosen, with a special key sequence
- During active ringer by a simple key press.

In Conversation mode the procedure is as follows:

- Put the set in conversation mode (supply necessary)
- Depress PR (ringer program key)
- Press one of the four acceptable volume keys (1 to 4); see Table 8.

Table 8 Ringer volume control, conversation mode

KEY	RVOL1	RVOL2
1	0	0 (minimum output power)
2	1	0
3	0	1
4	1	1 (maximum output power)

The newly selected value is directly stored into EEPROM.

During active ringing the PR key is not used, the procedure is as follows:

- Activate the ringer (only then this volume correction is possible)
- Press one of the four acceptable volume keys (1 to 4); see Table 9.

Table 9 Ringer volume control, active ringer mode

KEY	RVOL1	RVOL2
1	0	0 (minimum output power)
2	1	0
3	0	1
4	1	1 (maximum output power)

The newly selected value is directly stored into EEPROM.

5.7.5 RINGER REPETITION RATE CHANGE DURING CONVERSATION AND RINGER MODE

The generated melody is built up out of three frequencies. These frequencies are generated successively in a selected repeat frequency.
There are four steps and they can be changed:

- Via the EEPROM programming procedure (See Section 5.3.2)
- During conversation mode, when the function keys option is chosen, with a special key sequence
- During active ringer by a simple key press.

In conversation mode the procedure is as follows:

- Put the set in conversation (supply necessary)
- Depress PR (ringer program key)
- Press one of the four acceptable repeat frequency keys (9, *, 0 or #) see Table 10.

Table 10 Ringer repetition rate selection, conversation mode

KEY	FREQUENCY (Hz)	TONE TIME (ms)
9	7	47.6
*	11	30.3
0	15	22.2
#	20	16.6

The newly selected value is directly stored into EEPROM.

During active ringing the PR key is not used, the procedure is as follows:

- Active the ringer (only then this repetition rate correction is possible)
- Press one of the four acceptable repeat frequency keys (9, *, 0 or #) see Table 11.

Table 11 Ringer repetition rate selection, active ringer mode

KEY	FREQUENCY (Hz)	TONE TIME (ms)
9	7	47.6
*	11	30.3
0	15	22.2
#	20	16.6

The newly selected value is directly stored into EEPROM.

6 LIMITING VALUES

In according with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+7	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	−	125	mW
P_O	power dissipation per output	−	30	mW
I_{SS}	ground supply current	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	−	90	°C

7 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *Data Handbook IC03, Section: General, Handling MOS devices*").

8 DC CHARACTERISTICS

V_{DD} = 1.8 to 6 V (note 1); V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; f_{osc} = 3.579545 MHz; $R_X \leq 100\ \Omega$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage						
V_{DD}	supply voltage	operating; note 1	1.8	−	6	V
		RAM data retention in Standby mode	1.0	−	6	V
Supply current						
I_{DD}	supply current	Dialling/Ringer mode; V_{DD} = 3 V; note 2	−	0.8	1.6	mA
		Conversation/Programming mode; V_{DD} = 3 V; note 2	−	0.35	0.7	mA
		Standby mode (notes 2 and 3); at V_{DD} = 1.8 V; T_{amb} = 25 °C	−	1.0	5.5	µA
		Standby mode (notes 2 and 3); at V_{DD} = 1.8 V; T_{amb} = 70 °C	−	−	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	–1	–	+1	µA
Port outputs						
I_{OL}	LOW level output sink current	at V_{DD} = 3 V; V_O = 0.4 V	0.7	3.5	–	mA
I_{OH}	HIGH level output pull-up source current	at V_{DD} = 3 V; V_O = 2.7 V	10	30	–	µA
		at V_{DD} = 3 V; V_O = 0 V	–	140	300	µA
I_{OH1}	HIGH level output push-pull source current	at V_{DD} = 3 V; V_O = 2.6 V	0.7	3.5	–	mA
Tone output (notes 1 and 4)						
$V_{HG(RMS)}$	output RMS voltage	HIGH group	158	181	205	mV
$V_{LG(RMS)}$		LOW group	125	142	160	mV
Δf	frequency deviation		–0.6	–	+0.6	%
V_{DC}	DC voltage level		–	$\frac{1}{2}V_{DD}$	–	V
$\lvert Z_O \rvert$	output impedance		–	100	500	Ω
G_v	voltage gain (pre-emphasis) of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	at T_{amb} = 25 °C; note 5	–	–25	–	dB
EEPROM (notes 1, 6 and 7)						
N_{cyc}	endurance (erase/write cycles)		100000	–	–	cycles
t_{ret}	data retention		10	–	–	years

Notes to characteristics

1. Tone output, EEPROM erase and EEPROM write require $V_{DD} \geq 2.5$ V.
2. $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$; open drain outputs connected to V_{SS}; all other outputs open; maximum values: external clock at XTAL1; XTAL2 open; typical values at T_{amb} = 25 °C; crystal connected between XTAL1 and XTAL2.
3. $V_{IL} = V_{SS}$, $V_{IL} = V_{DD}$; RESET, HOOK and CE/RT at V_{SS}; crystal connected between XTAL1 and XTAL2; open-drain outputs connected to V_{SS}; all other outputs open.
4. Values are specified for DTMF frequencies only (CEPT compatible).
5. Related to the low group frequency component (CEPT compatible).
6. Verified on sampling basis.
7. After final testing the value of each EEPROM bit is typically HIGH, but this state cannot be guaranteed.

9 APPLICATION INFORMATION

A block diagram of an electronic feature phone built around the PCD3330-1 is shown in Fig.11. It comprises the following dedicated telecom ICs:

- TEA1067 speech/transmission IC
- TEA1083A call progress monitor IC
- PCD3330-1 dialler/ringer IC.

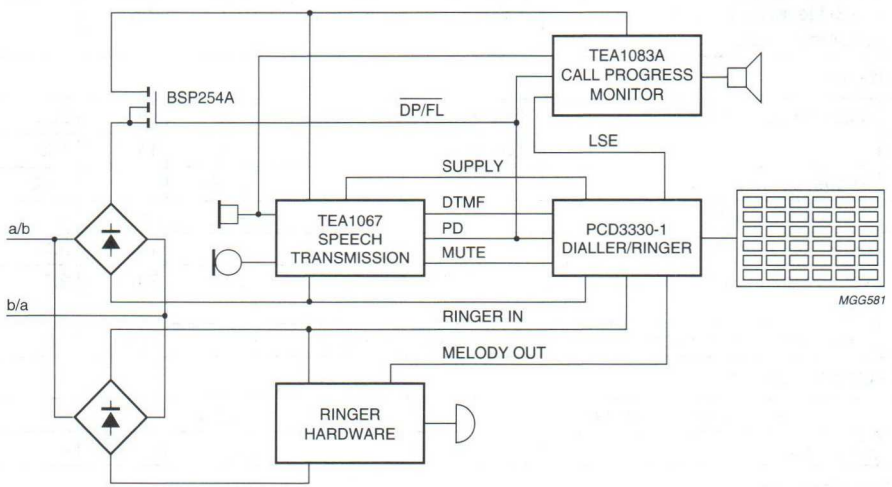


Fig.11 Block diagram of an electronic feature phone.

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1 FEATURES

- Pulse, DTMF and VT 'mixed mode' dialling
- 13 number repertory dial, up to 32 digits per number
  - 10 one-touch redial or 3 one-touch plus 10 two-touch
  - 250 digits maximum storage
- Last number redial up to 32 digits
- Repertory and redial memory integrity check (memory contents check)
- Notepad memory function
- Flash and Earth register recall
- Access pause generation and termination
- On-chip power-on reset
- Supports function keys as follows:
  - STORE: Program/Store
  - MRC: Memory Recall
  - FLASH: calibrated line-break pulse
  - LNR: Last Number Redial
  - PAUSE: insert access pause between stored digits
  - TONE: change from pulse to DTMF dialling (mixed mode)
  - VOL+/–: speaker/ringer volume control
  - 10 dedicated memory keys
- Strap functions (diode options):
  - MLA: Memory Location Access selection
  - RDS: Enable/Disable ringer validation delay (PCD3332-2)
  - DOO: enable/disable transmission * or # (PCD3332-3/S)
  - F/E: register recall Flash or Earth
  - M/S: Mark-to-Space ratio selection (3 : 2 or 2 : 1)
  - APT: Access Pause Timing selection
  - TBT: Tone Burst Time selection
  - FTS: Flash Time Selection
  - P/T: Pulse or Tone (DTMF) mode selection
  - RMS: Ringer Melody Selection (PCD3332-2 and PCD3332-S)
  - RFS: Ringer input frequency range selection (19.5 to 57 Hz or 14.4 to 68 Hz) (PCD3332-3)
- Ringer tone generator
- Ringer-input frequency discriminator
- Ringer melody selection via keypad
- Volume control for loudspeaker phones (PCD3332-3)
- On-hook dialling/hands-free mode control (PCD3332-3)
- Pacifier tones.

2 GENERAL DESCRIPTION

The PCD3332-2, PCD3332-3 and PCD3332-S are mixed-mode multistandard repertory dialler/ringer ICs, fabricated in a low threshold voltage CMOS technology. Dial parameters of these ICs can be set by diode options to meet the specific requirements for various countries. The on-chip tone generators are used for DTMF dialling and ringer melody generation. A discriminator input enables the tone output only if a correct ringer frequency is applied. Repertory numbers of up to 32 digits can be stored, with maximum storage of 250 digits.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3332-2P	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3332-2T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCD3332-3P	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3332-3T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCD3332-SP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3332-ST	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

4 PINNING

4.1 PCD3332-2

SYMBOL	PIN	TYPE	DESCRIPTION
ROW2	1	I/O[1]	row 2 keyboard output
ROW3	2	I/O[1]	row 3 keyboard output
ROW4	3	I/O[1]	row 4 keyboard output
ROW5	4	O[2]	row 5 keyboard output
DIODE	5	I/O[1]	diode option
MUTE	6	O[4]	mute output
EARTH	7	O[4]	earth recall
CSI	8	I	cradle switch input
XTAL1	9	I	oscillator input
XTAL2	10	O	oscillator output
RESET	11	I	reset input
CE/FDI	12	I	chip enable/frequency discriminator
COL6	13	I/O[1]	column 6 input
COL5	14	I/O[1]	column 5 input
COL4	15	I/O[1]	column 4 input
COL3	16	I/O[1]	column 3 input
COL2	17	I/O[1]	column 2 input
COL1	18	I/O[1]	column 1 input
$\overline{DP}/\overline{FL}$	19	O[2]	dial pulse/flash output
not used	20	O[4]	not used, leave pin unconnected
VOL2	21	O[3]	volume 2 output
V_{SS}	22	P	ground
TONE	23	O	tone generator output
V_{DD}	24	P	positive supply voltage
VOL1	25	O[3]	volume 1 output
DMO/KTE	26	O[4]	dial mode output
RTE	27	O[4]	key/ringer tone enable
ROW1	28	I/O[1]	row 1 keyboard output

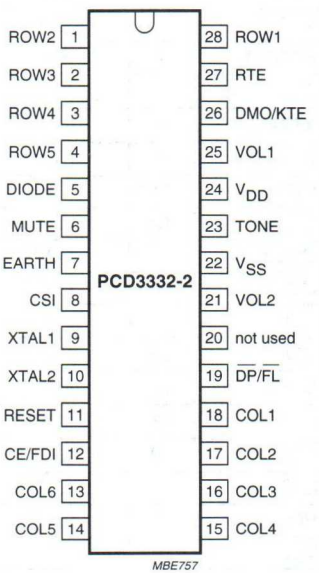


Fig.1 Pin configuration.

Notes on types and initial states of inputs and outputs

1. Standard input or output, set to HIGH state.
2. Open-drain output, set to HIGH state.
3. Open-drain output, reset to LOW state.
4. Push-pull output, reset to LOW state.

4.2 PCD3332-3

SYMBOL	PIN	TYPE	DESCRIPTION
ROW2	1	I/O[1]	row 2 keyboard output
ROW3	2	I/O[1]	row 3 keyboard output
ROW4	3	I/O[1]	row 4 keyboard output
ROW5	4	O[2]	row 5 keyboard output
DIODE	5	I/O[1]	diode option
MUTE	6	O[4]	mute output
EARTH	7	O[4]	earth recall
CSI	8	I	cradle switch input
XTAL1	9	I	oscillator input
XTAL2	10	O	oscillator output
RESET	11	I	reset input
CE/FDI	12	I	chip enable/frequency discriminator
COL6	13	I/O[1]	column 6 input
COL5	14	I/O[1]	column 5 input
COL4	15	I/O[1]	column 4 input
COL3	16	I/O[1]	column 3 input
COL2	17	I/O[1]	column 2 input
COL1	18	I/O[1]	column 1 input
$\overline{DP}/\overline{FL}$	19	O[2]	dial pulse/flash output
LFE	20	O[4]	low-frequency amplifier enable
VOL2	21	O[3]	volume 2 output
V_{SS}	22	P	ground
TONE	23	O	tone generator output
V_{DD}	24	P	positive supply voltage
VOL1	25	O[3]	volume 1 output
DMO/KTE	26	O[4]	dial mode output
HF/RTE	27	O[4]	hands-free/ringer tone enable
ROW1	28	I/O[1]	row 1 keyboard output

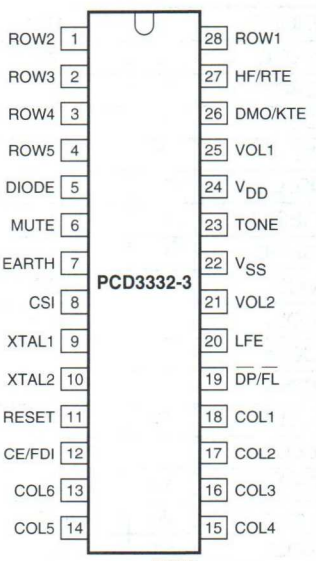


Fig.2 Pin configuration.

Notes on types and initial states of inputs and outputs

1. Standard input or output, set to HIGH state.
2. Open-drain output, set to HIGH state.
3. Open-drain output, reset to LOW state.
4. Push-pull output, reset to LOW state.

4.3 PCD3332-S

SYMBOL	PIN	TYPE	DESCRIPTION
ROW2	1	I/O[1]	row 2 keyboard output
ROW3	2	I/O[1]	row 3 keyboard output
ROW4	3	I/O[1]	row 4 keyboard output
ROW5	4	O[2]	row 5 keyboard output
DIODE	5	I/O[1]	diode option
MUTE	6	O[4]	mute output
EARTH	7	O[4]	earth recall
CSI	8	I	cradle switch input
XTAL1	9	I	oscillator input
XTAL2	10	O	oscillator output
RESET	11	I	reset input
CE/FDI	12	I	chip enable/frequency discriminator
COL6	13	I/O[1]	column 6 input
COL5	14	I/O[1]	column 5 input
COL4	15	I/O[1]	column 4 input
COL3	16	I/O[1]	column 3 input
COL2	17	I/O[1]	column 2 input
COL1	18	I/O[1]	column 1 input
$\overline{DP}/\overline{FL}$	19	O[2]	dial pulse/flash output
not used	20	O[4]	not used, leave pin unconnected
VOL2	21	O[3]	volume 2 output
V_{SS}	22	P	ground
TONE	23	O	tone generator output
V_{DD}	24	P	positive supply voltage
VOL1	25	O[3]	volume 1 output
DMO/KTE	26	O[4]	dial mode output
RTE	27	O[4]	key/ringer tone enable
ROW1	28	I/O[1]	row 1 keyboard output

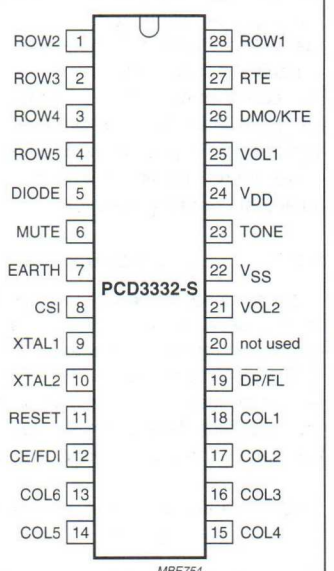


Fig.3 Pin configuration.

Notes on types and initial states of inputs and outputs

1. Standard input or output, set to HIGH state.
2. Open-drain output, set to HIGH state.
3. Open-drain output, reset to LOW state.
4. Push-pull output, reset to LOW state.

5 FUNCTIONAL DESCRIPTION

References to the 'PCD3332' or the 'device' apply to the PCD3332-2, the PCD3332-3 and the PCD3332-S.

5.1 Pin description

5.1.1 SUPPLY TERMINALS (V_{DD} AND V_{SS})

To retain data in the RAM, the standby supply voltage of 1 V, must be maintained. To ensure that the contents of the RAM are secure in the event of a power failure, a capacitor may be connected across the supply terminals. The capacitor must have a suitable value to maintain the standby voltage for a certain period of time. The minimum operating voltage of these devices is 2.5 V. The internal power-on reset is enabled for a voltage below this minimum operating voltage.

5.1.2 OSCILLATOR INPUT/OUTPUT (XTAL1 AND XTAL2)

The time base for the PCD3332 is a crystal-controlled on-chip oscillator, which incorporates a 3.58 MHz crystal or ceramic resonator connected between XTAL1 and XTAL2. It should be noted that when using a ceramic resonator, the minimum supply voltage increases. The oscillator starts when V_{DD} reaches its operating voltage level and CE = HIGH (min. 2.5 V).

5.1.3 CHIP ENABLE AND FREQUENCY DISCRIMINATOR INPUT (CE/FDI)

For DC inputs this pin acts as the chip enable (CE) input, and is active HIGH. CE in combination with the Cradle Switch Input (CSI) determines the mode of the device. See Table 1.

For AC inputs the pin acts as the (ringer) Frequency Discriminator Input (FDI).

To generate a correct ringer output tone, the input frequency must be between 19.5 Hz and 57 Hz; frequencies below 18 Hz and higher than 64 Hz are omitted.

The PCD3332-3 has a second (diode selectable) range of valid input frequencies of 14.5 Hz to 68 Hz; frequencies below 14 Hz and higher than 76 Hz are omitted.

Ringer response timing and detection is illustrated in Fig.15.

5.1.4 CRADLE SWITCH INPUT (CSI)

CSI is normally generated from the physical 'off-hooking' of the phone. CSI in combination with CE/FDI determines the operating mode of the PCD3332, as shown in Table 1.

Table 1 Different modes of the PCD3332

INPUT CSI	INPUT CE/FDI	PCD3332 STATUS
LOW	LOW	stop or power-down mode
HIGH	LOW	idle mode
LOW	HIGH	ringer mode
HIGH	HIGH	conversation or off-hook mode

5.1.5 RESET INPUT (RESET)

RESET activates the on-chip reset circuit and is active HIGH. The reset circuit initializes all inputs and outputs. Two other events will cause the chip to initialize:

- CE going HIGH
- V_{DD} falling below 2.5 V, then being restored (power-on reset).

For this reason, RESET may not be required, and can be connected to V_{SS}. This should preferably be via a 100 kΩ resistor, to save leakage current.

Note that a suitable capacitor connected between V_{DD} and V_{SS} will inhibit the decrease of voltage at V_{DD} after a power failure, and thus extend the time until the power-on reset is initiated.

5.1.6 PULSE DIAL AND FLASH OUTPUT ($\overline{DP}/\overline{FL}$)

This pin is the output for:

- The dial pulse sequence ($\overline{DP}$)
- The calibrated LOW pulse ($\overline{FL}$) after the FLASH key is pressed.

The dialling sequence for pulse dialling is shown in Figs 11 and 12. $\overline{DP}/\overline{FL}$ starts HIGH, pulses are LOW, and the inter-digit pauses are HIGH. Thus, $\overline{DP}/\overline{FL}$ is HIGH during a line-make and LOW during a line-break.

If the Flash/Earth diode option is set to FLASH, then when FLASH is pressed a LOW pulse is output, with a calibrated duration also determined by diode option.

5.1.7 MUTE OUTPUT (MUTE)

During the dialling sequence this push-pull output is activated. In the pulse dialling mode, MUTE goes HIGH prior to the dialling action and goes LOW after the last t_{idp} (interdigit pause), see Figs 11 and 12. In DTMF dialling, MUTE goes HIGH prior to the dialling action and goes LOW after an additional 'holdover' time, see Figs 13 and 14.

This output is also activated if the device enters the programming mode, to avoid transmitting the keys entered.

5.1.8 DTMF OUTPUT (TONE)

The timing sequence for DTMF dialling is illustrated in Figs 13 and 14. The tones generated by this TONE are filtered by an on-chip switched capacitor filter, and active RC low-pass filter. Therefore, the total harmonic distortion fulfils the CEPT CS203 recommendations. An on-chip reference voltage provides output tone levels independent of supply voltages and temperatures. Spread among the individual parts is extremely low.

The DC level of the TONE output measures $0.5V_{DD}$ and the impedance is 100 Ω (typ.). Table 2 shows the frequency tolerances.

The TONE output is also used to generate the ringer melody, key entry acceptance beep, error or warning beeps and confirmation beeps. These beeps are generated/set in programming mode as a response to the users action. The ringer is designed to generate 3-melodies that may be selected using the keyboard. Table 3 shows the implemented ringer melodies.

Table 2 DTMF frequency tolerances

ROW/COL	STANDARD FREQUENCY (Hz)	OUTPUT FREQUENCY (Hz)	DEVIATION (%)	DEVIATION (Hz)
ROW 1	697	697.90	+0.13	+0.90
ROW 2	770	770.46	+0.06	+0.46
ROW 3	852	852.45	−0.18	−1.55
ROW 4	941	943.23	+0.24	+2.23
COL 1	1209	1206.45	−0.21	−2.55
COL 2	1336	1341.66	+0.42	+5.66
COL 3	1477	1482.21	+0.35	+5.21

Table 3 Ringer melodies

KEY DEPRESSED	TONE 1 (Hz)	TONE 2 (Hz)	TONE 3 (Hz)	TONE ON TIME (ms)
1	826	925	1037	30
2	1037	1161	1297	30
3	1297	1455	1621	30

Table 4 Beep frequencies

BEEP FUNCTION	TONE 1 (Hz)	TONE 2 (Hz)	TONE 3 (Hz)	TONE ON TIME (ms)	TONE OFF TIME (ms)
Key accept	2358	–	–	40	–
Error	2358	2358	2358	134	35
Confirmation	806	899	1010	134	67

5.1.9 REGISTER RECALL (EARTH)

If the Flash/Earth diode option of the PCD3332 is set to the Earth, then dialling the EARTH either out of Repertory/LNR or by pressing the FLASH key will generate a HIGH pulse at the push-pull output EARTH for a calibrated time. Figures 12 and 14 illustrate the EARTH timing relationship with other signals. The calibrated EARTH time is followed by an interdigit time t_{idp}. A second dialling of EARTH can only be performed after the interdigit time has elapsed.

If the Flash key was the first key depressed directly after going off-hook, followed by a second depressing of the Flash key while the EARTH is still in progress, then the second depression will be ignored.

5.1.10 RINGER TONE ENABLE (RTE: PCD3332-2/S)

The PCD3332-2 and PCD3332-S generate tones for the ringer output stage and key tones when depressing a function key at the keypad. Output RTE will go HIGH and stay HIGH for the duration of the tone generated at output TONE.

5.1.11 HANDS-FREE/RINGER TONE ENABLE (HF/RTE: PCD3332-3)

The PCD3332-3 generates tones for the ringer output stage and key tones when depressing a function key at the keypad. Output HF/RTE will go HIGH and stay HIGH for the duration of the tone generated at output TONE.

During the conversation mode, HF/RTE is used for enabling the hands-free mode. Depressing the HOOK key will change the operation mode as follows:

- Change from on-hook (stop mode) to hands-free mode
- Toggles the listening-in mode
- Change from handset to hands-free.

5.1.12 VOLUME CONTROL OUTPUTS (VOL1 AND VOL2)

5.1.12.1 PCD3332-2

The PCD3332-2 has the facility to control the ringer output signal, as well as the loudspeaker volume, by depressing the keys */VOL– or #/ VOL+ during the ringer mode.

If the maximum volume level is reached, depressing #/VOL+ key will not change the volume setting. If the minimum volume level is reached, depressing */VOL– key will not change the volume setting. Selection between ringer volume or conversation mode volume, is performed in the hardware using the RTE output. In the ringer mode the output RTE is HIGH.

Table 5 shows the volume outputs setting, as well as the default setting in case of a power failure or if the power is supplied for the first time.

5.1.12.2 PCD3332-3

The PCD3332-3 has the facility to control the ringer output signal and the loudspeaker signal during listening-in or hands-free operation. Depressing the keys VOL– or VOL+ during the ringer mode will change the ringer volume setting. Depressing the keys VOL– or VOL+ during the conversation mode will change the loudspeaker volume setting.

If the maximum volume level is reached, depressing the VOL+ key will not change the volume setting. If the minimum volume level is reached, depressing the VOL– key will not change the volume setting. Selection between ringer volume or conversation mode volume, is performed in the hardware using the HF/RTE output. In the ringer mode the output HF/RTE is HIGH.

Table 5 shows the volume outputs setting, as well as the default setting in case of a power failure or if the power is supplied for the first time.

5.1.12.3 PCD3332-S

The PCD3332-S has the facility to control the ringer output signal by depressing the keys VOL– or VOL+ during the ringer mode.

If the maximum volume level is reached, depressing the VOL+ key will not change the volume setting. If the minimum volume level is reached, depressing the VOL– key will not change the volume setting. Selection between ringer volume or conversation mode volume, is performed in the hardware using the RTE output. In the ringer mode the output RTE is HIGH.

Table 5 shows the volume outputs setting, as well as the default setting in case of a power failure or if the power is supplied for the first time.

5.1.13 RINGER VOLUME SETTINGS

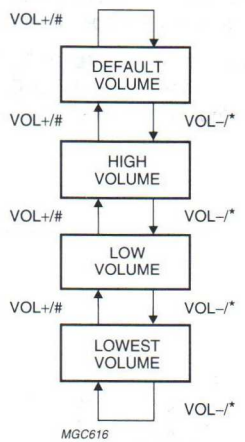


Fig.4 FSM for volume control (PCD3332-2).

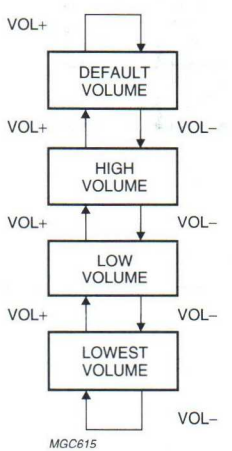


Fig.5 FSM for volume control (PCD3332-3/S).

Table 5 State assignment

STATE	VOL2	VOL1
Default volume setting	HIGH	HIGH
High volume setting	HIGH	LOW
Low volume setting	LOW	HIGH
Lowest volume setting	LOW	LOW

5.1.14 DIAL MODE OUTPUT /KEY-TONE ENABLE (DMO/KTE)

In the PULSE dialling mode the DMO/KTE output is activated (HIGH), at dialling the Make/Brake pulse dial sequences. Figures 11 and 12 illustrate the signal timing relationship.

In the programming mode, the DMO/KTE output is activated at the same time the key beeps are generated at output TONE and may be used to enable the key tone to the earpiece amplifier.

5.1.15 KEYBOARD INPUTS/OUTPUTS

A single contact keyboard with a maximum of 6 columns and 5 rows can be connected to the PCD3332-2. The keyboard scanning is started if a key depression is detected. The rows are scanned while the columns are used as sense inputs.

To overcome key bouncing, a debounce on/off time of approximately 14 to 20 ms is implemented.

Only one single key depression is validated and accepted at any one time. Once a key is accepted the keyboard scanning is continued until no further keys are depressed. This means that if a key is accepted but still depressed while a second key is entered, the second key depression is ignored. Also, if two or more keys are depressed within the debounce time while no key is yet accepted, all keys are ignored.

Keyboard detection is also performed in the ringer mode to enable the ringer volume setting and ringer melody selection.

In the on-hook mode or power-down mode of the PCD3332-2 and PCD3332-S, the keyboard I/Os are set to HIGH except ROW 5 which is set to LOW.

In the on-hook mode or power-down mode of the PCD3332-3, the keyboard I/Os are set to HIGH except ROW 5 which is set to LOW. In this instance, depression of the HOOK key can be detected by the external hardware circuitry and converted to an active HIGH signal which is passed to CE in order to 'wake-up' the PCD3332-3.
When the HOOK key has been accepted the PCD3332-3 enters the hands-free mode.

ROW 5 was used to detect the HOOK key, this function is deleted.

ROW 5 is an open-drain input, this configuration is used to avoid current flowing in the on-hook mode or power-down mode. A pull-up resistor should be connected to ROW 5.

The keyboards which the PCD3332-2, PCD3332-3 and PCD33332-S support are shown in Figs 6, 7 and 8 respectively. The figures also show the diode options as 'dotted' keys.

5.2 Keyboards

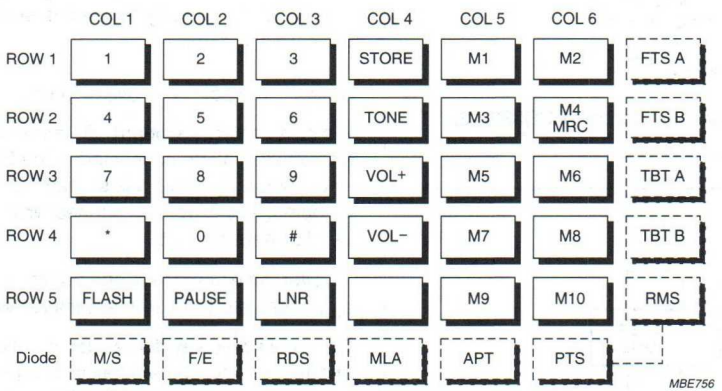


Fig.6 Keyboard layout (PCD3332-2).

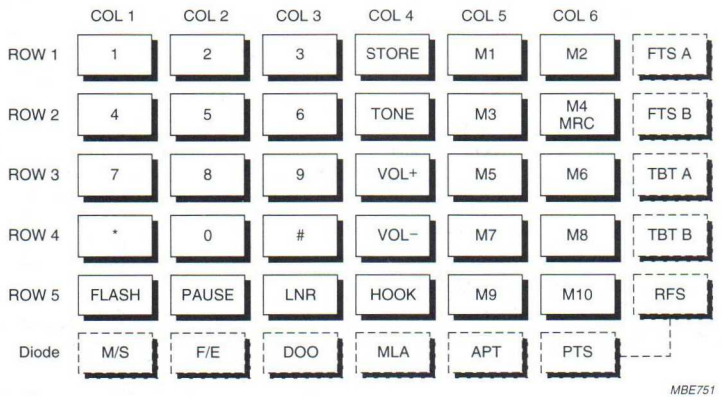


Fig.7 Keyboard layout (PCD3332-3).

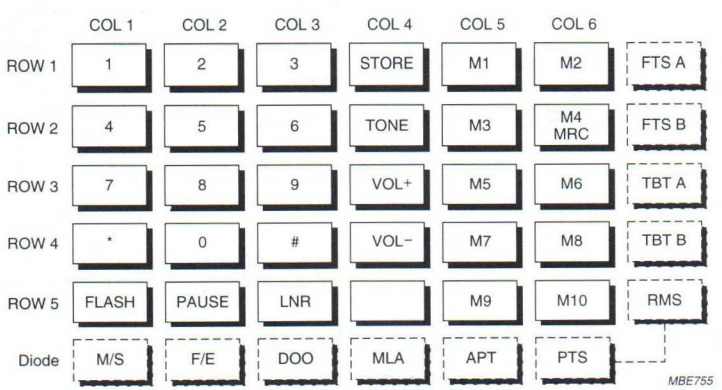


Fig.8 Keyboard layout (PCD3332-S).

5.2.1 KEYBOARD FUNCTION KEYS

5.2.1.1 LNR

If the first key operated after CE = HIGH (off-hook) is key LNR the PCD3332 will transmit the last number dialled before CE was LOW (on-hook).

5.2.1.2 PAUSE

Pressing the PAUSE key will insert an access pause during manual dialling and/or during programming. During manual dialling the pause time is not dialled, but is stored in the redial memory. This means that with manual dialling the user actually waits for the dial tone before dialling is continued. Repertory and LNR dialling however, will dial out the access pause. If the pause key is depressed while an access pause is being dialled, the access pause in progress is terminated and dialling will continue at the next non-access pause digit. The access pause duration is option selectable.

5.2.1.3 TONE (mixed mode dialling)

If the pulse dial mode is selected by the diode option, then pressing the 'TONE', '*' or '#' keys will change the dial mode to DTMF. Pressing the Flash key or going on-hook will restore the pulse dial mode.

5.2.1.4 RECALL (Flash or Earth)

Depressing the FLASH key will activate output $\overline{DP}/\overline{FL}$ or output EARTH for the calibrated time, depending on which function Flash or Earth is selected.

5.2.1.5 STORE

Pressing the STORE key will start/stop the programming mode. To inhibit transmitting the key entries while in programming mode, the output and MUTE is activated.

5.2.1.6 MRC

In order to access one of the memory locations, the MRC key must be depressed followed by one of the numerical keys 0 to 9. To enable the MRC key, diode option MLA must be disconnected.

5.2.1.7 VOL– and VOL+

For the PCD3332-3's 'hands-free' and 'listening-in' modes, where the loudspeaker is on, the VOL keys control the loudspeaker volume. In the ringer mode (all devices), the VOL keys control the ringer volume.

At power-on reset a default volume is preset for both the loudspeaker and the ringer volume.

5.2.2 DIODE OPTIONS

Table 6 Tone Burst Time diode configuration

TBT A DIODE	TBT B DIODE	SELECTED TIMING (ms)
Not connected	not connected	70/70
Not connected	connected	100/100
Connected	not connected	85/85
Connected	connected	70/140

Table 7 Flash time select diode configuration

FTS A DIODE	FTS B DIODE	SELECTED TIMING (ms)
Not connected	not connected	95
Not connected	connected	115
Connected	not connected	270
Connected	connected	600

Table 8 Flash/Earth diode configuration

F/E DIODE	SELECTED MODE
Not connected	Flash
Connected	Earth (400 ms)

Table 9 Mark/space diode configuration

M/S DIODE	SELECTED MAKE/BRAKE RATIO (ms)
Not connected	33/66 (1 : 2)
Connected	40/60 (2 : 3)

Table 10 Pulse/tone diode configuration

P/T DIODE	SELECTED DIAL MODE
Not connected	DTMF
Connected	Pulse

Table 11 Access Pause Time diode configuration

APT DIODE	SELECTED TIMING (s)
Not connected	2
Connected	4

Table 12 Ringer melody selection (PCD3331-2/S)

RMS DIODE	RINGER FREQUENCY SELECTION (Hz)
Not connected	ringer melody selection by keys 1, 2 and 3
Connected	default ringer melody

Table 13 Ringer input frequency selection (PCD3332-3)

RFS DIODE	RINGER FREQUENCY SELECTION (Hz)
Not connected	19.5 to 54
Connected	14.5 to 68

Table 14 Memory Location Access diode configuration

MLA DIODE	KEY FUNCTION
Not connected	M4/MRC key is MRC
Connected	M4/MRC key is M4

Table 15 Ringer Delay Selection diode configuration (PCD3332-2)

RDS DIODE	OUTPUT SELECTION
Not connected	no delay
Connected	ringer validation delay, 100 ms

Table 16 DTMF output option diode configuration (PCD3332-3/S)

DOO DIODE	OUTPUT SELECTION
Not connected	no transmission of */#
Connected	transmission of */#

5.2.2.1 Ringer Delay Selection (RDS: PCD3332-2)

If the diode is connected, then the actual ringer frequency validation is started after a delay of 100 ms. This is only performed at the start of each ringer burst signal.

5.2.2.2 DOO DTMF output selection (PCD3332-3/S)

If the diode is connected, then the * and # DTMF signals will be dialled out during pulse-to-tone switching. If the diode is not connected * and # will not be dialled out during pulse-to-tone switching.

5.2.2.3 Ringer Melody Selection (RMS: PCD3332-2/S)

The ringer melody for these devices can be changed by depressing keys 1, 2 and 3. To give default melody only, apply a diode at RMS location.

5.2.2.4 Ringer Input Frequency Range Selection (RFS: PCD3332-3)

For the PCD3332-3, this diode is used to select between two input frequency ranges, 19.5 to 54 Hz or 14.5 to 68 Hz.

5.2.2.5 Memory Location Access (MLA)

To be able to build various telephone models by using the PCD3332, a possibility has been created to define different keypad layouts. e.g. a 13 number repertory dial consist of 10 numbers recalled via MRC + 0 to 9, and 3 direct access numbers M1, M2 and M3. A 10 number direct accessible dialler can be created by applying the keys M1 to M10 while a diode is connected at the MLA location.

5.2.2.6 Mark-to-Space ratio (M/S)

Changes the make-break ratio from 60 : 40 ms (3 : 2) to 66 : 33 ms (2 : 1).

5.2.2.7 Access Pause Time (APT)

To adapt the access pause timing to local requirements, 2 different times for DTMF and the corresponding times for pulse dialling are built-in.

5.2.2.8 Tone Burst Time (TBT)

During automatic transmission of a number in the DTMF mode the tone-on time and the pause time between two digits can be selected by option TBT A and TBT B. During manual dialling this option selects the minimum tone-on and pause time while the maximum time is determined by the time a key is depressed.

5.2.2.9 Pulse/Tone mode Selection (PTS)

The telephone set can be initially set to the PULSE or DTMF mode by switching on and off the diode in the matrix.

The first entry of keys * and # in the pulse dial mode will change the dial mode as well.

5.2.2.10 Flash or Earth register recall (F/E)

Dependent on this option, the output $\overline{DP}/\overline{FL}$ or output EARTH will be activated after a flash key operation.

5.2.2.11 Flash Time Select

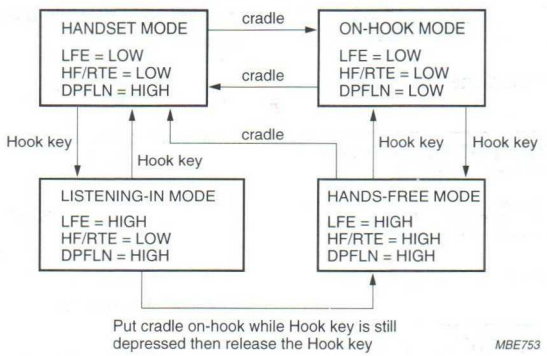
These two diodes set the calibrated flash pulse duration: 100, 115, 270 or 600 ms for the $\overline{DP}/\overline{FL}$ output, when this output is selected. When the EARTH output is selected the earth pulse is 400 ms.

5.2.2.12 Low Frequency amplifier Enable (LFE: PCD3332-3)

Output LFE can be used to enable the TEA108x or TEA109x listening-in or hands-free IC. The HOOK key functions as a toggle to control the hands-free mode (LFE = LOW) or listening-in mode (LFE = HIGH). while in the off-hook condition the key can be pressed and kept down to replace the handset while saving the LFE and $\overline{DP}/\overline{FL}$ selection.

5.2.3 HOOK MODES

Figure 9 illustrates the different HOOK modes and how those modes are entered (PCD3332-3). For the PCD3332-2/S only the 'handset' mode and 'on-hook' mode are valid.



For PCD3332-2 and PCD3332-S, only the 'handset mode' and 'on-hook mode' are valid.

Fig.9 Schematic diagram of the HOOK modes.

6 OPERATING PROCEDURES

6.1 Operating modes

The PCD3332-2/S has 4 operating modes:

1. On-hook mode or ringer mode
2. Off-hook mode or conversation mode
3. Programming mode or store mode
4. Dial mode.

The PCD3332-3 has 4 operating modes:

1. On-hook mode or ringer mode
2. Conversation mode which is divided into hands-free mode and listening-in mode
3. Programming mode or store mode
4. Dial mode.

6.1.1 ON-HOOK MODE OR RINGER MODE

When the chip enable input CE/FDI is LOW the PCD3332 is disabled. In the standby mode, the only current drawn is for memory retention of the redial digits. During the standby mode all keyboard pins are HIGH, except ROW 5 which is set to LOW.

6.1.2 DIAL MODE

Lifting the cradle (handset) or pressing the hook key will put the set in the conversation mode, an accepted key entry is processed and may initiate the following:

- Dialling the digits entered
- Redialling the previously entered digits
- Dialling out a repertory memory
- Enter programming mode.

6.1.3 RESET DELAY TIME

All modes, except for the ringer mode, are terminated by a line break (CE is deactivated), or by going on-hook. If this condition is detected, the reset delay time is initiated. The set will not enter the on-hook state unless the reset delay has expired. In the event of a line break, the set will remain in the actual operation mode if the line-break is ended while the reset delay is still in progress (see Fig.10).

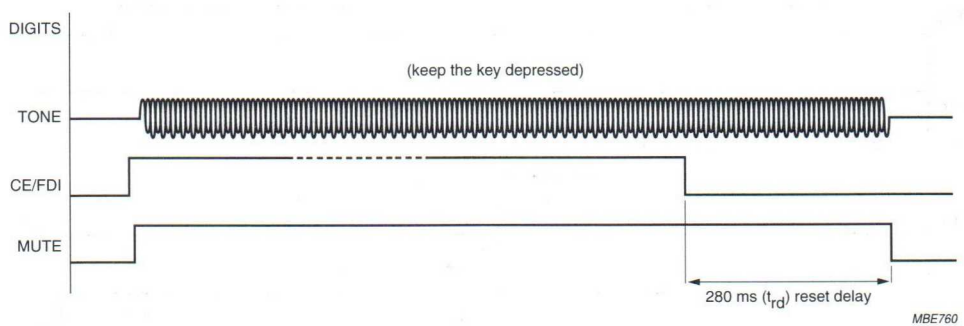
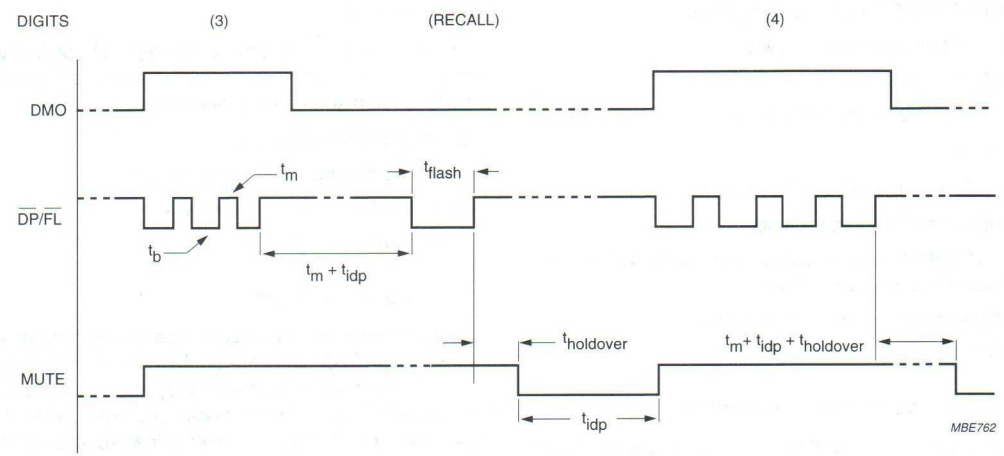


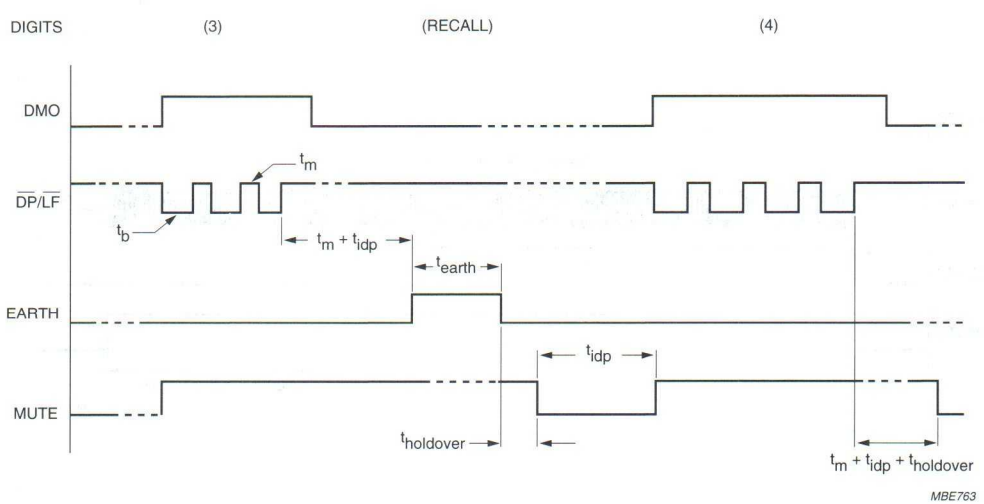
Fig.10 Reset delay timing relationship.

6.1.3.1 Pulse dialling (PTS = ON)



$t_{holdover}$ = 80 ms; t_{idp} = 840 ms.
t_b = break time; t_m = make time; t_{idp} = interdigit pause time.

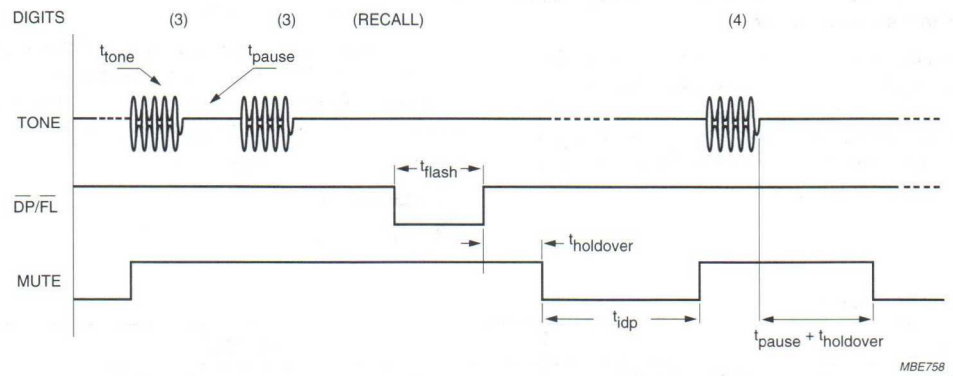
Fig.11 $\overline{DP}/\overline{FL}$, DMO and MUTE timing relationship.



$t_{holdover}$ = 80 ms; t_{idp} = 840 ms.
t_b = break time; t_m = make time; t_{idp} = interdigit pause time.

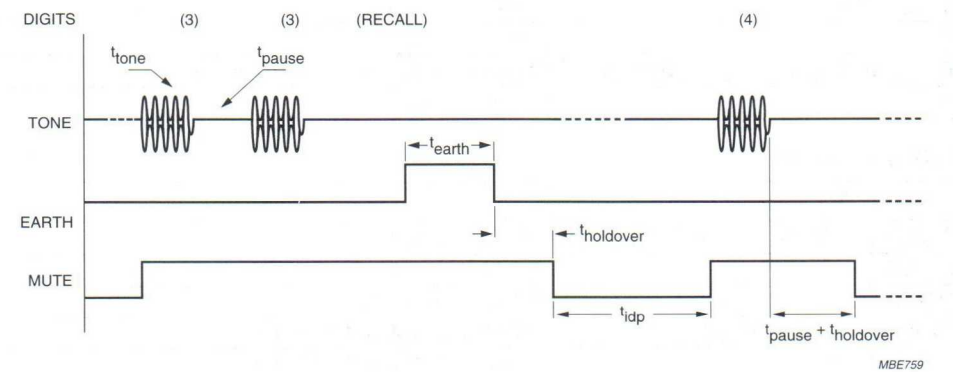
Fig.12 $\overline{DP}/\overline{FL}$, DMO, MUTE and EARTH timing relationship.

6.1.3.2 DTMF dialling (PTS = OFF)



$t_{holdover}$ = 80 ms; t_{idp} = 840 ms.
t_{idp} = interdigit pause time.

Fig.13 $\overline{DP}/\overline{FL}$, MUTE and TONE timing relationship.



$t_{holdover}$ = 80 ms; $t_{idp\ (flash - idp)}$ = 840 ms.
t_{idp} = interdigit pause time.

Fig.14 TONE, MUTE and EARTH timing relationship.

6.1.3.3 Manual dialling

During digit entry, the device immediately starts to transmit the digit(s). The minimum transmission time is unaffected by the speed of entry. Transmission continues as long as further data input has to be processed. Up to 32 digits can be stored in the redial register.

After the main register overflows, a 10 digits First-In First-Out register (FIFO) takes over as buffer. After transmitting the first digit of the FIFO register this position is automatically cleared to provide space for storing new data. In this way, the total number of digits which can be transmitted is unlimited, provided the key-in rate is not excessive.

If the key-in rate causes both the redial register and FIFO register to overflow, the PCD3332-2 will return to the conversation mode and no keyboard entries will be accepted.

6.1.3.4 Last number redial

If the first key entered is the LNR key, the stored LNR number is dialled out. LNR can hold a maximum of 32 digits. LNR is inhibited If more than 32 digits are entered, normal dialling however is continued.

LNR functional examples:

⇓ = Go on-hook

⇑ = Go off-hook

Table 17 LNR capacity

INPUT	OUTPUT
⇑, [1], [2], [3], [4], [5], [6], [7], [8], [9], [0], [1], [2], [3], [4], [5], [6], [7], [8], [9], [0], [1], [2], [3], [4], [5], [6], [7], [8], [9], [0], [1], [2], ⇓	DTMF: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2
⇑. [LNR], ⇓	DTMF: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2
⇑, [LNR], [0], ⇓	DTMF: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 0
⇑, [LNR], ⇓	nothing dialled

Table 18 LNR after programming

INPUT	OUTPUT
⇑, [1], [2], [3], [4], [5], ⇓	DTMF: 1, 2, 3, 4, 5
⇑, [LNR], ⇓	DTMF: 1, 2, 3, 4, 5
⇓, ⇑, [STORE] [5], [4], [3], [2], [1], [STORE], [M1], ⇓	beep for each entry (confirmation beep)
⇑, [LNR], ⇓	nothing dialled

Table 19 LNR sliding cursor

INPUT (M1 = 1, 2, 3, 4 or 5)	OUTPUT
⇑, [1], [2], [3], [4], [5], [6], [7], [8], [9], [0], ⇓	DTMF: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0
⇑, [1], [2], [3], [LNR], ⇓	DTMF: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0
⇑, [STORE] [5], [4], [3], [2], [1], [STORE], [M1] ⇓	DTMF: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0
⇑, [M1], Wait for end of dial, [M1], ⇓	DTMF: 1, 2, 3, 4, 5, 1, 2, 3, 4, 5
⇑[1], [2], [3], [LNR], ⇓	DTMF: 1, 2, 3, 4, 5, 1, 2, 3, 4, 5
⇑[2], [3], [LNR], ⇓	DTMF: 2, 3
⇑[2], [3], [LNR], ⇓	DTMF: 2, 3

Table 20 LNR if *, #, Tone, and recall is entered in DTMF mode

INPUT	OUTPUT
⇑ [1], [2], [*], [3], [4], [Recall], [6], [7], ⇓	DTMF: 1, 2, *, 3, 4, Flash, 6, 7
⇑, [LNR], ⇓	DTMF: Flash, 6, 7
⇑ [Recall], Wait 0.5 sec, [Recall], Wait 0.5 sec, [Recall], [1], [2], [3], ⇓	Flash, Flash, Flash, 1, 2, 3
⇑ [LNR], ⇓	Flash, 1, 2, 3
⇑ [1], [2], [3], [Recall], [3], [2], [1], ⇓	1, 2, 3, Flash, 3, 2, 1
⇑ [LNR], ⇓	Flash, 3, 2, 1
⇑ [1], [2], [3], [Recall], [*], [3], [2], [1], ⇓	1, 2, 3, Flash, *, 3, 2, 1
⇑ [LNR], ⇓	*, 3, 2, 1
⇑ [*], [1], [2], [3], [Recall], [3], [2], [1], ⇓	*, 1, 2, 3, Flash, 3, 2, 1
⇑ [LNR], ⇓	Flash, 3, 2, 1
⇑ [*], [1], [2], [3], [Recall], [*], [3], [2], [1], ⇓	*, 1, 2, 3, Flash, 3, 2, 1
⇑ [LNR], ⇓	Flash, 3, 2, 1

Table 21 LNR if *, #, Tone, and recall is entered in PULSE mode

INPUT	OUTPUT
⇑ [1], [2], [*], [3], [4], [Recall], [6], [7], ⇓	PULSE: 1, 2, DTMF: 3, 4, Earth, PULSE: 6, 7
⇑ [LNR], ⇓	PULSE: 1, 2
⇑ [Recall], Wait 0.5 sec, [Recall], Wait 0.5 sec, [Recall], [1], [2], [3], ⇓	PULSE: Earth, Earth, Earth, 1, 2, 3
⇑ [LNR], ⇓	PULSE: Earth, 1, 2, 3
⇑ [1], [2], [3], [Recall], [3], [2], [1], ⇓	PULSE: 1, 2, 3, Earth, 3, 2, 1
⇑ [LNR], ⇓	PULSE: Earth, 3, 2, 1
⇑ [1], [2], [3], [Recall], [*], [3], [2], [1], ⇓	PULSE: 1, 2, 3, Earth, DTMF: 3, 2, 1
⇑ [LNR], ⇓	PULSE: 1, 2, 3
⇑ [*], [1], [2], [3], [Recall], [3], [2], [1], ⇓	DTMF: 1, 2, 3, Earth, PULSE: 3, 2, 1
⇑ [LNR], ⇓	PULSE: Earth, 3, 2, 1
⇑ [*], [1], [2], [3], [Recall], [*], [3], [2], [1], ⇓	DTMF: 1, 2, 3, Earth, 3, 2, 1
⇑ [LNR], ⇓	DTMF: 1, 2, 3

6.1.3.5 *Access pause dialling and termination*

Access pauses entered during manual dialling or repertory number storage are not dialled out, but are stored. When LNR or a repertory number is selected for redial, the access pauses are dialled out. If at LNR or repertory dial, an access pause is being dialled out, then depressing the PAUSE key will terminate the access pause in progress and dialling will continue at the first non-access pause digit.

6.1.3.6 *Flash/Earth recall*

Depending on the option selected (see Table 8), depressing the Flash key will generate a calibrated Flash time at output $\overline{DP}/\overline{FL}$, or a calibrated earth time on the EARTH output. The calibrated earth time is 400 ms, the flash time is set by diodes as shown in Table 7.

The Flash/Earth will also refer the set to dial mode selected by the diode option.

6.1.3.7 *Data dialling in the pulse dialling mode*

If the PCD3332 is initially set to the pulse dial mode (PTS = ON), depressing the TONE, * or # key will continue dialling in the DTMF mode. Flash/Earth recall will restore the pulse dialling mode.

6.1.4 PROGRAMMING MODE

The PCD3332 has an on-chip CMOS RAM which can store up to 10 numbers of 32 digits with a total of 250 digits (floating memory). If the memory overflows, a warning beep is generated. If the controller is initially set to the pulse dial mode, digits can be stored in the pulse dial and/or in the DTMF mode by depressing key * or # or using the 'change mode' procedure during the store procedure. This function is best illustrated in Table 22.

6.1.4.1 *Memory overflow*

A total of 250 digits can be stored. If an attempt is made to store a number which will bring the total amount of digits stored to over 250, the TONE output will generate the memory overflow beeps and the store procedure is cancelled.

6.1.4.2 *Notepad function*

In the speech mode, a number can be entered on the keyboard. This number may be dialled out at the next off-hook situation by LNR or may be entered in memory. This function effectively mimics a notepad for a number passed during a telephone conversation.

6.1.4.3 *Repertory and chain dialling*

Repertory numbers can be dialled out before or after manual dialling or LNR, and can be entered one after another in a chain. However, during transmission of LNR or a repertory number, a subsequent repertory number is not accepted. This means that a repertory number can only be entered if the previous repertory dial or LNR is ended.

Depending on the MLA diode configuration (see Table 14) the procedure is as follows:

- Direct repertory access: M1 to M10
- Two-key repertory access: MRC_0 to MRC_9.

6.1.5 RINGER MODE (PCD3332-2/S)

The PCD3332-2/S has a built-in frequency discriminator circuit, with CE/FDI being used as the discriminator input. If the ringer frequency supplied is accepted, a ringer melody is generated. When the ringer melody sounds, the ringer volume is adjustable in 4 steps using the */VOL– and #/VOL+ keys.

Depending on the diode RMS, either a default ringer melody is selected, or 1 out of 3 ringer melodies may be selected from the keypad (see Table 12).

6.1.6 RINGER MODE (PCD3332-3)

The PCD3332-3 has a built-in frequency discriminator circuit, with CE/FDI being used as the discriminator input. If the ringer frequency supplied is accepted, a ringer melody is generated. When the ringer melody sounds, the ringer volume is adjustable in 4 steps using the */VOL– and #/VOL+ keys.

Depending on the diode RFS, 1 of 2 different input ringer frequency ranges is selected (see Table 13).

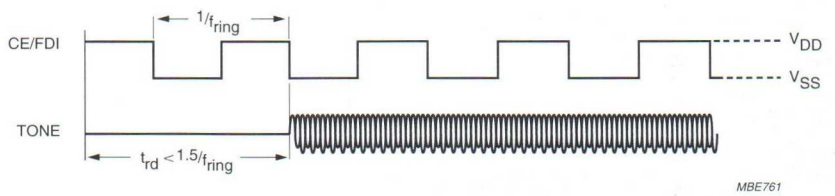


Fig.15 Ringer response timing and detection.

Table 22 Key sequences in programming mode

KEY SEQUENCE
Programming a repertory location
[STORE] data [STORE] [M1][1]
[STORE] data [M1][1]
[STORE] data [STORE] [0][2]
[STORE] data [STORE] [MRC] [0][2], and [STORE] data [STORE] [M1][3]
[STORE] data [MRC] [0][2], and [STORE] data [M1][3]
Copy LNR to a repertory location
[STORE] [LNR] [STORE] [M1][1]
[STORE] [LNR] [M1][1]
[STORE] [LNR] [STORE] [0][2]
[STORE] [LNR] [STORE] [MRC] [0][2], and [STORE] [LNR] [STORE] [M1][3]
[STORE] [LNR] [MRC] [0][2], and [STORE] [LNR] [M1][3]
Clearing a repertory location
[STORE] [M1][1]
[STORE] [STORE] [0][2]
[STORE] [STORE] [MRC] [0][2], and [STORE] [STORE] [M1][3]
[STORE] [MRC] [0][2], and [STORE] [M1][3]
[STORE] data [MRC] [0][2], and [STORE] data [M1][3]
Notepad programming
[STORE] data [STORE] [LNR]
[STORE] data [LNR]
Clear Notepad
[STORE] [STORE] [LNR]
[STORE] [LNR]

Notes

1. Select [M1] to [M10].
2. Select [0] to [9].
3. Select [M1] to [M3].

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7.0	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	−	125	mW
P_O	power dissipation per output	−	30	mW
I_{SS}	ground supply current	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	−	90	°C

8 DC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	operating		2.5	−	6	V
	standby	CE = 0	1.0	−	6	V
$I_{DD(dial)}$	supply current (dialling mode)	note 1, CE = 1				
		V_{DD} = 3 V; TONE active	−	0.9	1.8	mA
		V_{DD} = 3 V; TONE not active	−	0.3	0.6	mA
$I_{DD(conv)}$	supply current (conversation mode)	note 1; CE = 1; V_{DD} = 3 V	−	0.2	0.4	mA
$I_{DD(stb)}$	supply current (standby mode)	note 2; CE = 0				
		V_{DD} = 1.8 V; T_{amb} = 25 °C;	−	1.0	2.5	µA
		V_{DD} = 1.8 V; T_{amb} = 70 °C;	−	−	10	µA
Inputs						
V_{IL}	LOW level input voltage		0	−	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	−	V_{DD}	Vtz
I_{LI}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	−1	−	+1	µA
Port outputs						
I_{OL}	LOW level output sink current	V_{DD} = 3 V; V_O = 0.4 V	0.7	3.5	−	mA
I_{OH}	HIGH level pull-up output source current	V_O = 2.7 V; V_{DD} = 3 V	−10	−20	−	µA
		V_O = 0 V; V_{DD} = 3 V	−	−100	−300	µA
I_{OH1}	HIGH level push-pull output source current	V_{DD} = 3 V; V_O = 2.6 V	−0.7	−4	−	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TONE output (notes 3 and 4)						
$V_{HG(RMS)}$	High Group Frequency voltage. Voltage of higher frequency component for DTMF (RMS value)		158	181	205	mV
$V_{LG(RMS)}$	Low Group Frequency voltage. Voltage of lower frequency component for DTMF (RMS value)		125	142	160	mV
$\Delta f/f$	frequency deviation		–0.6	–	0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_o \rvert$	output impedance		–	100	500	Ω
G_v	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	T_{amb} = 25 °C; note 5	–	25	–	dB
Power-on-reset						
V_{POR}	Power-on-reset level		1.5	2.0	2.5	V
Oscillator						
g_m	transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

Notes

1. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open; TONE not active, unless otherwise specified.
2. Crystal connected between XTAL1 and XTAL2; pins T1 and CE/$\overline{T0}$ at V_{SS}; TONE not active.
3. TONE output requires $V_{DD} \geq 2.5$ V.
4. Values are specified for DTMF frequencies only (CEPT).
5. Related to the Low Group Frequency component (CEPT).

9 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = –25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns

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8-bit microcontroller with DTMF generator PCD3349A

1 FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead package
- 4-kbyte ROM
- 224-byte RAM
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- 2 single-level vectored interrupts:
  - external
  - Timer/event counter 1
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent TONE output
- Filtering for low output distortion (CEPT compatible)
- Power-on-reset
- Stop and Idle modes
- Supply voltage: 1.8 to 6 V (DTMF TONE output from 2.5 V)
- Low standby voltage of 1 V
- Low Stop mode current of 1 μA (typical)
- Clock frequency: 1 to 16 MHz (3.58 MHz for DTMF suggested)
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCD3349A provides 4 kbytes of Program Memory, 224 bytes of RAM and 20 I/O lines.

The PCD3349A is a microcontroller which has been designed primarily for telecom applications. It includes an on-chip dual tone multi-frequency (DTMF) generator.

The instruction set is based on that of the MAB8048 and is software compatible with the PCD33xxA family.

This data sheet details the specific properties of the PCD3349A. The shared characteristics of the PCD33xxA family of microcontrollers are described in the *"PCD33xxA Family"* data sheet and also in *"Data Handbook IC03; Section PCD33xxA Family"*, which should be read in conjunction with this publication.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3349AP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3349AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

4 BLOCK DIAGRAM

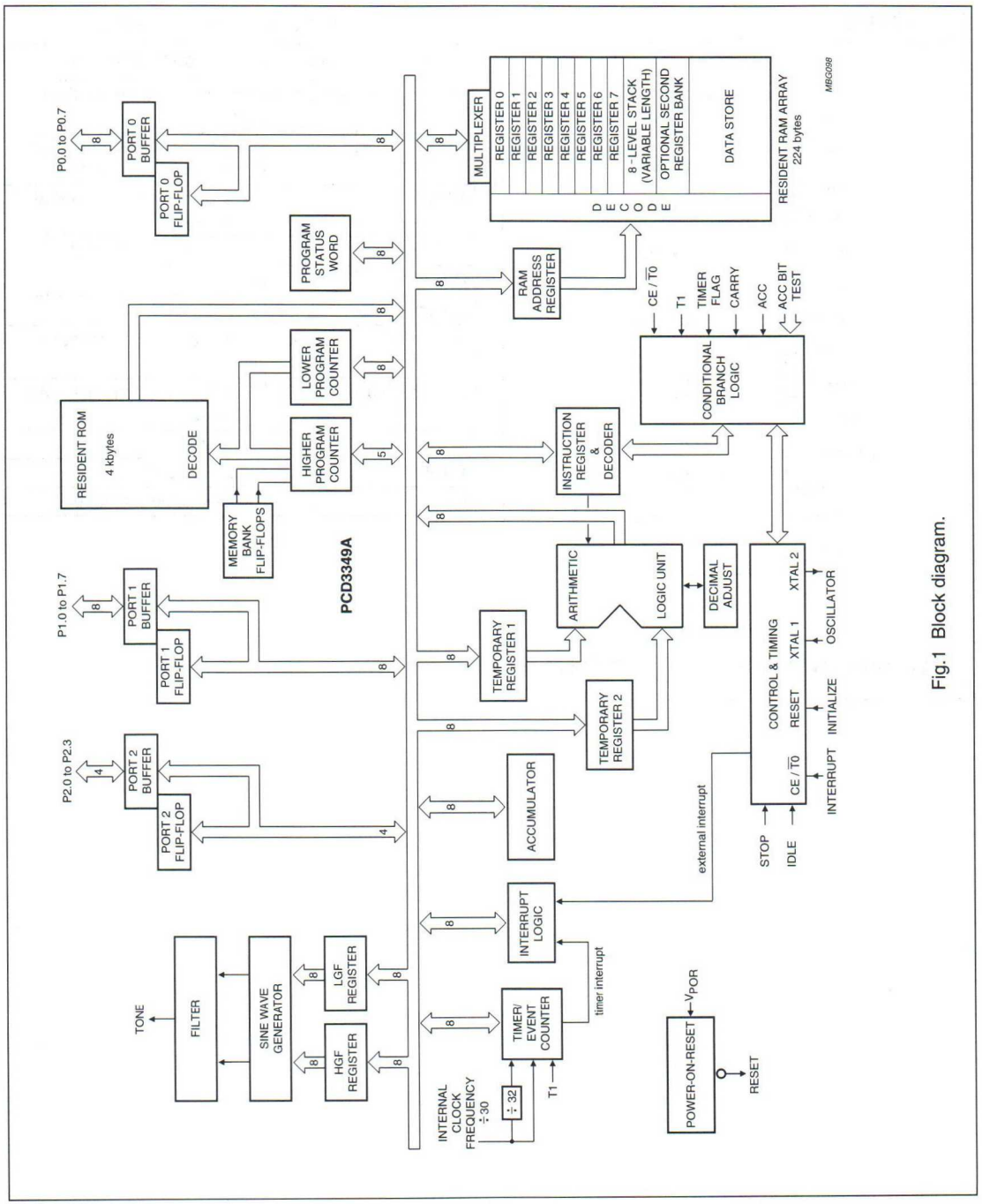


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

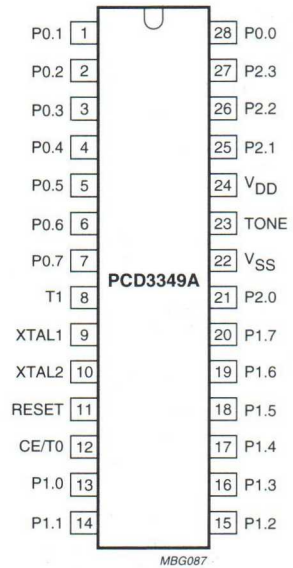


Fig.2 Pin configuration (SOT117-1 and SOT136-1).

5.2 Pin description

Table 1 SOT117-1 and SOT136-1 packages

SYMBOL	PIN	DESCRIPTION
P0.0 to P0.7	28, 1 to 7	Port 0: 8 quasi-bidirectional I/O lines
T1	8	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	9	crystal oscillator or external clock input
XTAL2	10	crystal oscillator output
RESET	11	reset input
CE/$\overline{T0}$	12	Chip Enable or Test 0
P1.0 to P1.7	13 to 20	Port 1: 8 quasi-bidirectional I/O lines
P2.0 to P2.3	21, 25, 26, 27	Port 2: 4 quasi-bidirectional I/O lines
V_{SS}	22	ground
TONE	23	DTMF output
V_{DD}	24	positive supply voltage

6 FREQUENCY GENERATOR

A versatile frequency generator section is provided (see Fig.3). For normal operation, use a 3.58 MHz quartz crystal or PXE resonator. The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available.

6.1 Frequency generator derivative registers

Table 2 gives the derivative addresses, mnemonics and access types of the frequency generator derivative registers. The addresses 03H to FFH are not used.

Table 2 Addresses of the frequency generator derivative registers

ADDRESS	REGISTER	7	6	5	4	3	2	1	0
01H	HGF[1]	H7	H6	H5	H4	H3	H2	H1	H0
02H	LGF[2]	L7	L6	L5	L4	L3	L2	L1	L0

Notes

1. HGF = High Group Frequency; access type W.
2. LGF = Low Group Frequency; access type W.

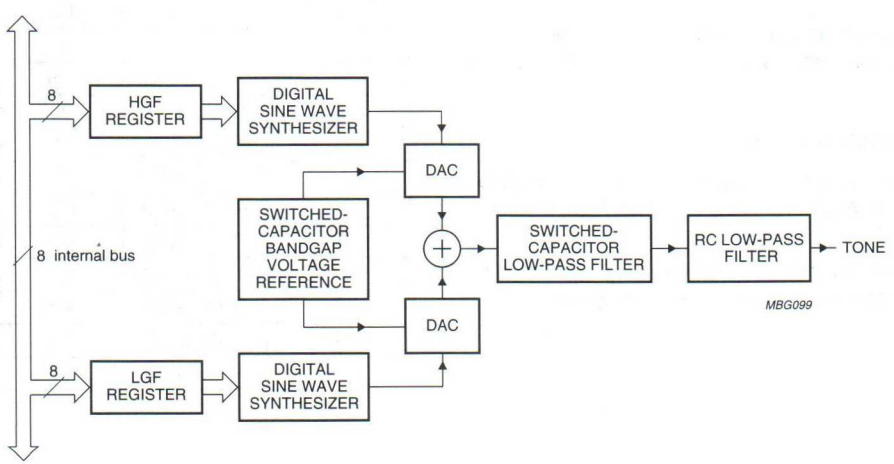


Fig.3 Block diagram of the frequency generator section.

6.2 Frequency registers

The two frequency registers HGF and LGF define two frequencies. From these, the digital sine synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures TONE output levels independent of supply voltage and temperature. The amplitude of the Low Group Frequency sine wave is attenuated by 2 dB compared to the amplitude of the High Group Frequency sine wave.

The two sine waves are summed and then filtered by an on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

The value 00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption.

The frequency of the sine wave generated is dependent upon the decimal value 'x' held in the frequency registers (HGF and LGF), and this may be calculated as follows:

$$f = \frac{f_{xtal}}{[23\,(x+2)\,]}; \text{ where } 60 \leq x \leq 255.$$

The frequency limitation given by $x \geq 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

6.3 DTMF frequencies

Assuming an oscillator frequency f_{xtal} = 3.58 MHz, the DTMF standard frequencies can be implemented as shown in Table 3.

The relationship between telephone keyboard symbols and the frequency register contents are given in Table 4.

Table 3 DTMF standard frequencies and their implementation; value = LGF, HGF contents

VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 4 Dialling symbols, corresponding DTMF frequency pairs and frequency registers content

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
*	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

6.4 Modem frequencies

Again assuming an oscillator frequency f_{xtal} = 3.58 MHz, the standard modem frequency pairs summarized in Table 5 can be implemented. It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling Low Group Frequency generation.

Table 5 Standard modem frequency pairs and their implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980[1]	978.82	−0.12	−1.18
82	1180[1]	1179.03	−0.08	−0.97
8F	1070[2]	1073.33	0.31	3.33
79	1270[2]	1265.30	−0.37	−4.70
80	1200[3]	1197.17	−0.24	−2.83
45	2200[3]	2192.01	−0.36	−7.99
76	1300[4]	1296.94	−0.24	−3.06
48	2100[4]	2103.14	0.15	3.14
5C	1650[1]	1655.66	0.34	5.66
52	1850[1]	1852.77	0.15	2.77
4B	2025[2]	2021.20	−0.19	−3.80
44	2225[2]	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

6.5 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{xtal} = 3.58 MHz (Table 6). It is suggested to define the frequency by the HGF register while the LGF contains 00H, disabling Low Group Frequency generation.

Table 6 Musical scale frequencies and their implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD[1]	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 at 440 Hz.

7 TIMING

Although the PCD3349A operates over a clock frequency range from 1 to 16 MHz, f_{xtal} = 3.58 MHz will usually be chosen to take full advantage of the frequency generator section.

8 RESET

In addition to the conditions given in the *"PCD33xxA Family"* data sheet, all derivative registers are cleared in the RESET state.

9 STOP MODE

Since the oscillator is switched off, the frequency generator receives no clock. It is suggested to clear both the HGF and LGF registers before entering Stop mode. This will cut-off the biasing of the internal amplifiers, considerably reducing current requirements.

10 IDLE MODE

In the Idle mode, the frequency generator remains operative.

11 INSTRUCTION SET RESTRICTIONS

Since no serial I/O interface is provided, the serial I/O (Input/Output) instructions are not available. 'MOV Dx, A' is the only applicable derivative instruction because the derivative registers are write-only.

ROM space being restricted to 4 kbytes, SEL MB2/3 would define non-existing Program Memory banks and should therefore be avoided.

RAM space being restricted to 224 bytes, care should be taken to avoid accesses to non-existing RAM locations.

12 SUMMARY OF MASK OPTIONS

Table 7 Port mask options

PORT NAME	PORT OUTPUT DRIVE(1)			PORT STATE AFTER RESET(2)	
	OPTION 1	OPTION 2	OPTION 3	SET	RESET
Port 0 (P0.0 to P0.7)	X	X	X	X	X
Port 1 (P1.0 to P1.7)	X	X	X	X	X
Port 2 (P2.0 to P2.7)	X	X	X	X	X

Notes

1. Port output drives:
   a) Option 1: standard I/O.
   b) Option 2: open-drain I/O.
   c) Option 3: push-pull output; see *"PCD33xxA Family"* data sheet.
2. Port state after reset: S = Set (HIGH) and R = Reset (LOW).

Table 8 Mask options

FEATURE	DESCRIPTION
ROM code: program/data	Any mix of instructions and data up to ROM size of 4 kbytes.
Power-on-reset voltage level: V_{POR}	1.2 to 3.6 V in increments of 100 mV; OFF
Oscillator transconductance: g_m	LOW transconductance: g_{mL}
	MEDIUM transconductance: g_{mM}
	HIGH transconductance: g_{mH}

13 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); see note 1 and 2.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7.0	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I, I_O	DC input or output current	−10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{SS}	ground supply current	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	–	90	°C

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

14 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

15 DC CHARACTERISTICS

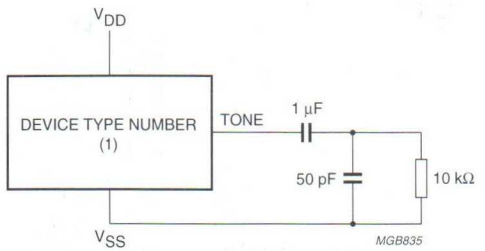
V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz (g_{mL}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (see Figs 5 to 9)						
V_{DD}	supply voltage					
	operating; note 1		1.8	–	6	V
	RAM data retention in Stop mode		1.0	–	6	V
I_{DD}	operating supply current; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0	–	0.9	1.8	mA
		V_{DD} = 3 V	–	0.3	0.6	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL})	–	1.1	3.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM})	–	1.7	5.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH})	–	2.5	6.0	mA
$I_{DD(idle)}$	supply current Idle mode; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0	–	0.7	1.4	mA
		V_{DD} = 3 V; value HGF = LGF = 0	–	0.2	0.4	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL})	–	0.8	1.6	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM})	–	1.2	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH})	–	1.7	5.0	mA
$I_{DD(stp)}$	supply current Stop mode	V_{DD} = 1.8 V; T_{amb} = 25 °C; note 3	–	1.0	2.5	µA
		V_{DD} = 1.8 V; T_{amb} = 70 °C; note 3	–	–	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	–1	–	+1	µA
Port outputs (see Figs 10 to 12)						
I_{OL}	LOW-level port sink current	V_{DD} = 3 V; V_O = 0.4 V	0.7	3.5	–	mA
I_{OH}	HIGH-level port pull-up source current	V_O = 2.7 V; V_{DD} = 3 V	–10	–20	–	µA
		V_O = 0 V; V_{DD} = 3 V	–	–100	–300	µA
I_{OH}	HIGH-level port push-pull source current	V_{DD} = 3 V; V_O = 2.6 V	–0.7	–4	–	mA
TONE output (see Fig.4; notes 1 and 4)						
V_{HGrms}	HGF voltage (RMS)		158	181	205	mV
V_{LGrms}	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		–0.6	–	0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_O \rvert$	output impedance		–	100	500	Ω
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	T_{amb} = 25 °C; note 5	–	25	–	dB
Power-on-reset						
ΔV_{POR}	Power-on-reset level variation around chosen V_{POR}	note 6	–0.5	0	+0.5	V

Notes

1. TONE output requires $V_{DD} \geq 2.5$ V.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open; value HGF = LGF = 0, unless otherwise specified.
3. Crystal connected between XTAL1 and XTAL2; pins T1 and CE/$\overline{T0}$ at V_{SS}; value HGF = LGF = 0.
4. Values are specified for DTMF frequencies only (CEPT).
5. Related to the Low Group Frequency (LGF) component (CEPT).
6. V_{POR} is an option chosen by the user. Depending on its value, it may restrict the supply voltage range.



(1) Device type number: PCD3349A

Fig.4 TONE output test circuit.

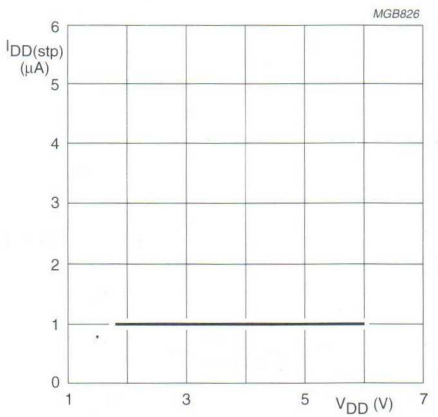
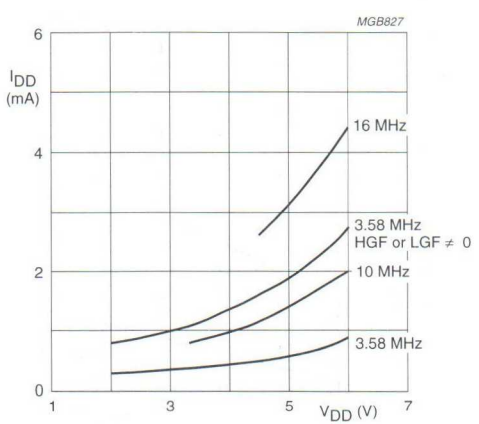
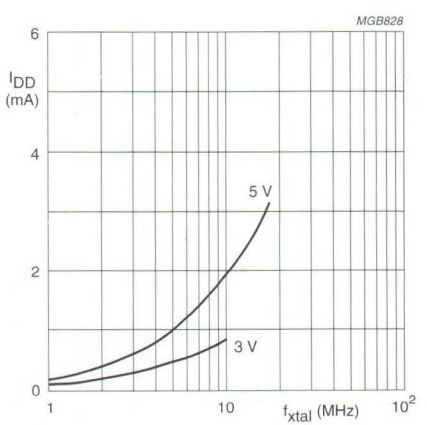


Fig.5 Typical supply current (I_{DD}) in Stop mode as a function of supply voltage (V_{DD}).



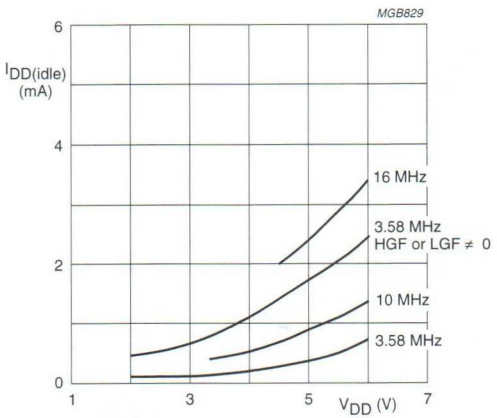
Measured with crystal between XTAL1 and XTAL2.

Fig.6 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).



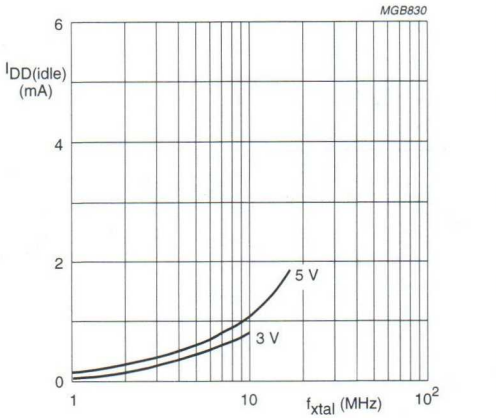
Measured with function generator on XTAL1.

Fig.7 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



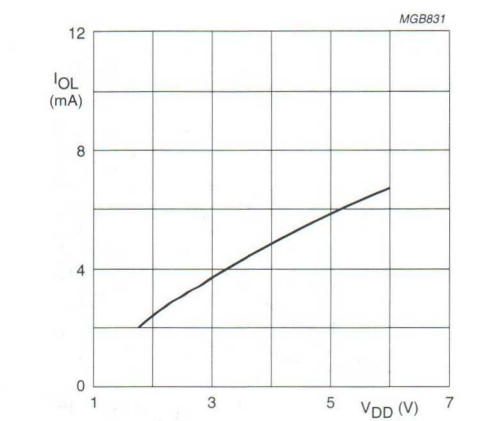
Measured with crystal between XTAL1 and XTAL2.

Fig.8 Typical supply current (I_{DD}) in Idle mode as a function of supply voltage (V_{DD}).



Measured with function generator on XTAL1.

Fig.9 Typical supply current (I_{DD}) in Idle mode as a function of clock frequency (f_{xtal}).



V_O = 0.4 V.

Fig.10 Typical LOW-level port output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

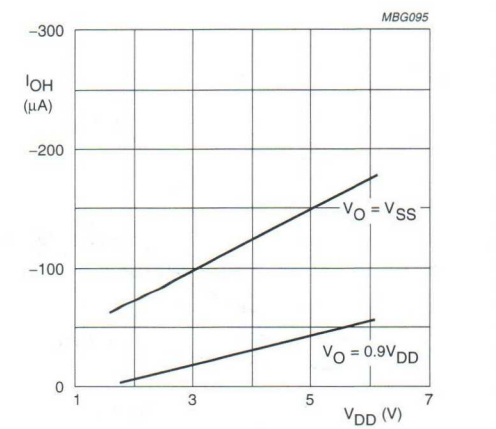
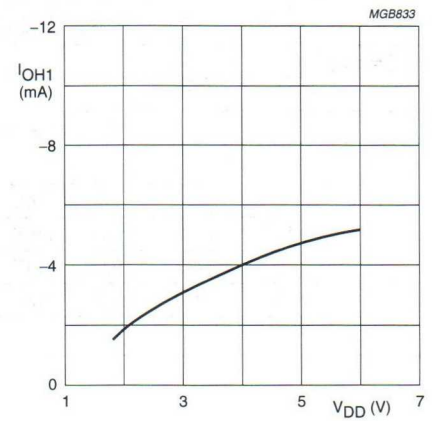


Fig.11 Typical HIGH-level output pull-up source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.12 Typical HIGH-level push-pull output source current (I_{OH}) as a function of supply voltage (V_{DD}).

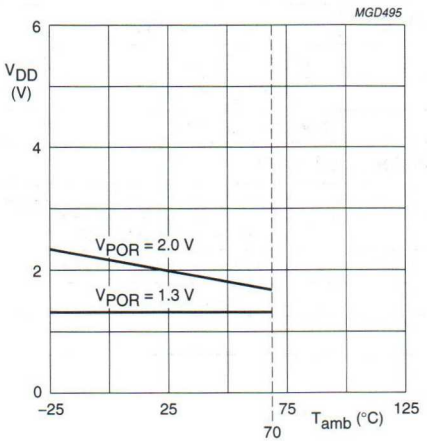


Fig.13 Typical Power-on-reset level (V_{POR}) as function of temperature.

16 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.14	1	–	16	MHz
Oscillator (see Fig.15)						
g_{mL}	LOW transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
g_{mM}	MEDIUM transconductance		0.9	1.6	3.2	mS
g_{mH}	HIGH transconductance		3.0	4.5	9.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

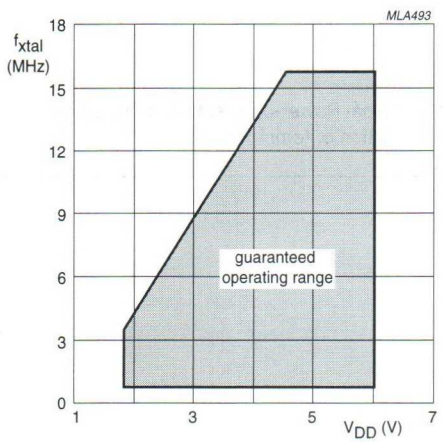


Fig.14 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).

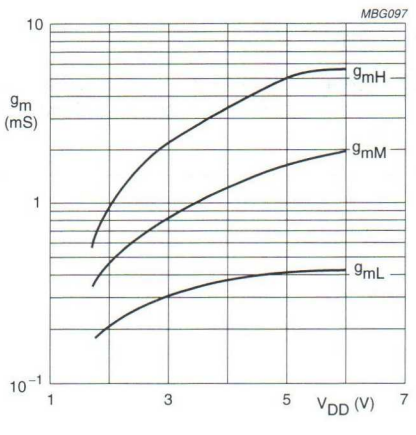


Fig.15 Typical transconductance as a function of supply voltage (V_{DD}).

8-bit microcontroller with DTMF generator, 256 bytes EEPROM and real-time clock

PCD3350A

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8-bit microcontroller with DTMF generator, 256 bytes EEPROM and real-time clock

PCD3350A

1 FEATURES

- 8-bit CPU, ROM, RAM, EEPROM, real-time clock and I/O; all in a 44-lead quad flat package
- 8 kbytes ROM
- 256 bytes RAM
- 256 bytes Electrically Erasable Programmable Read Only Memory (EEPROM)
- 32 kHz crystal oscillator for Real-Time Clock (RTC)
- EEPROM programmable RTC
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 34 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- 8-bit reloadable Timer 2
- Three single-level vectored interrupts:
  - external
  - 8-bit programmable Timer/event counter 1
  - derivative; triggered by reloadable Timer 2
- Two test inputs, one of which also serves as the external interrupt input
- DTMF, modem, musical tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT compatible)
- Melody output for ringer application
- Programmable DTMF clock divider
- Power-on-reset
- Stop and Idle modes
- Supply voltage: 1.8 to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- CPU clock frequency: 1 to 16 MHz (3.58 MHz or 10.74 MHz for DTMF)
- Operating ambient temperature: −25 to +70 °C
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

This data sheet details the specific properties of the PCD3350A. The shared properties of the PCD33xxA family of microcontrollers are described in the *"PCD33xxA family"* data sheet, which should be read in conjunction with this publication.

The PCD3350A is a microcontroller designed primarily for telephony applications. It includes 8 kbytes ROM, 256 bytes RAM, 34 I/O lines, and an on-chip generator for dual tone multifrequency (DTMF), modem and musical tones. In addition to dialling, the generated frequencies can be made available as square waves for melody generation, providing ringer operation.

The PCD3350A also incorporates 256 bytes of EEPROM, permitting data storage without battery backup. The EEPROM can be used for storing telephone numbers, particularly for implementing redial functions.

Finally, the PCD3350A includes a low power 32 kHz crystal oscillator with an EEPROM programmable Real-Time Clock (RTC) working in standby mode.

The instruction set is similar to that of the MAB8048 and is a sub-set of that listed in the *"PCD33xxA family"* data sheet.

3 ORDERING INFORMATION (see note 1)

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3350AH	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1

Note

1. Please refer to the Order Entry Form (OEF) for this device for the full type number to use when ordering. This type number will also specify the required program and the ROM mask options.

4 BLOCK DIAGRAM

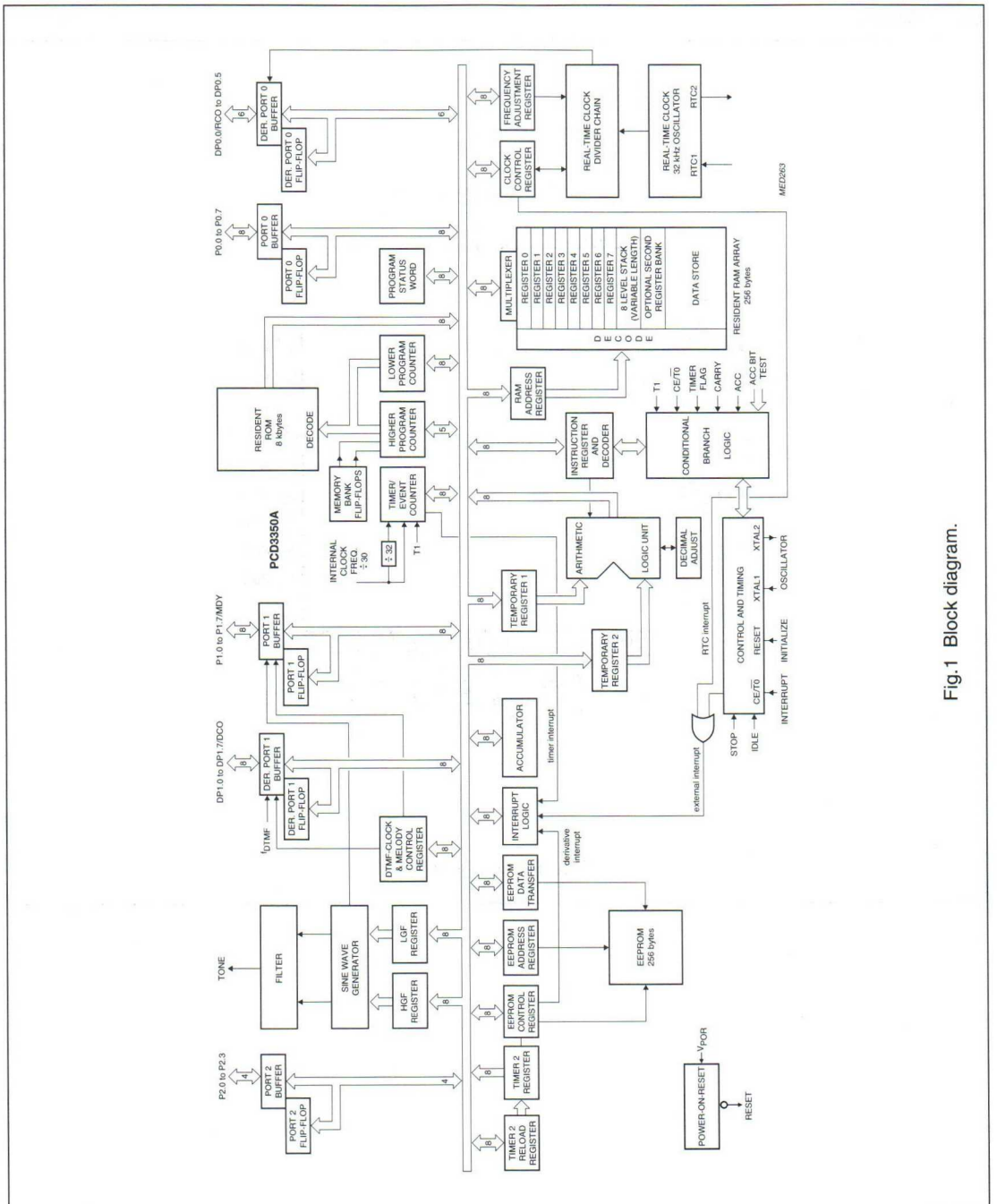


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

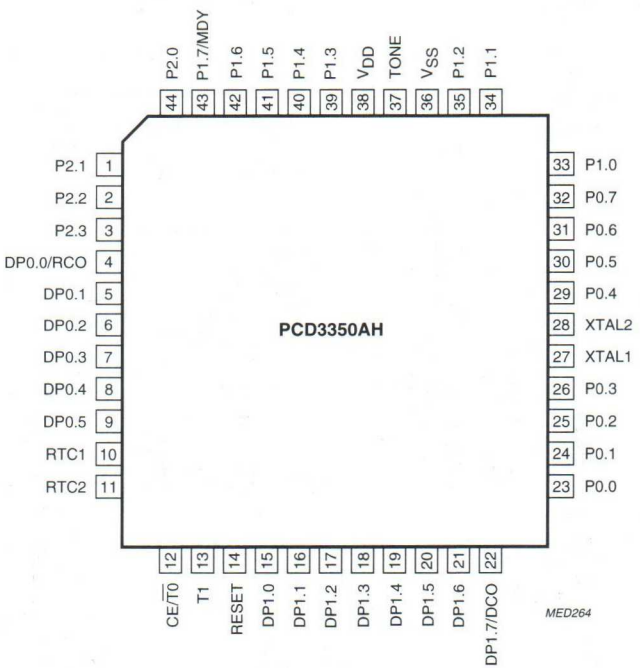


Fig.2 Pin configuration.

5.2 Pin description

Table 1 SOT205-1 package (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	TYPE	DESCRIPTION
P2.1 to P2.3	1 to 3	I/O	3 bits of Port 2: 4-bit quasi-bidirectional I/O port
DP0.0/RCO	4	I/O	1 bit of Derivative Port 0: 6-bit quasi-bidirectional I/O port; or RTC output
DP0.1 to DP0.5	5 to 9	I/O	5 bits of Derivative Port 0: 6-bit quasi-bidirectional I/O port
RTC1	10	I	Real Time Clock 32 kHz oscillator input
RTC2	11	O	Real Time Clock 32 kHz oscillator output
CE/$\overline{T0}$	12	I	Chip Enable or Test 0 input
T1	13	I	Test 1/count input of 8-bit Timer/event counter 1
RESET	14	I	reset input
DP1.0 to DP1.6	15 to 21	I/O	7 bits of Derivative Port 1: 8-bit quasi-bidirectional I/O port
DP1.7/DCO	22	I/O	1 bit of Derivative Port 1: 8-bit quasi-bidirectional I/O port; or DTMF clock output
P0.0 to P0.3	23 to 26	I/O	4 bits of Port 0: 8-bit quasi-bidirectional I/O port
XTAL1	27	I	crystal oscillator/external clock input
XTAL2	28	O	crystal oscillator output
P0.4 to P0.7	29 to 32	I/O	4 bits of Port 0: 8-bit quasi-bidirectional I/O port
P1.0 to P1.2	33 to 35	I/O	3 bits of Port 1: 8-bit quasi-bidirectional I/O port
V_{SS}	36	P	ground
TONE	37	O	DTMF output
V_{DD}	38	P	positive supply voltage
P1.3 to P1.6	39 to 42	I/O	4 bits of Port 1: 8-bit quasi-bidirectional I/O port
P1.7/MDY	43	I/O	1 bit of Port 1: 8-bit quasi-bidirectional I/O port; or melody output
P2.0	44	I/O	1 bit of Port 2: 4-bit quasi-bidirectional I/O port

6 FREQUENCY GENERATOR

A versatile frequency generator section with built-in programmable clock divider is provided (see Fig.3). The clock divider allows the DTMF section to run either with the main clock frequency ($f_{DTMF} = f_{xtal}$) or with a third of it ($f_{DTMF} = 1/3 \times f_{xtal}$) depending on the state of the divider control bit DIV3 (see Table 4). The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available. Their frequencies are provided either in purely sinusoidal form on the TONE output or as a square wave on the port line P1.7/MDY. The latter is typically for ringer applications in telephone sets. If no frequency output is selected the TONE output is in 3-state mode.

6.1 Frequency generator derivative registers

6.1.1 High and Low Group Frequency Registers

Table 2 gives the addresses, symbols and access types of the High Group Frequency (HGF) and Low Group Frequency (LGF) registers, used to set the frequency output.

Table 2 Hexadecimal addresses, symbols, access types and bit symbols of the frequency registers

REGISTER ADDRESS	REGISTER SYMBOL	ACCESS TYPE	BIT SYMBOLS							
			7	6	5	4	3	2	1	0
11H	HGF	W	H7	H6	H5	H4	H3	H2	H1	H0
12H	LGF	W	L7	L6	L5	L4	L3	L2	L1	L0

6.1.2 Clock and Melody Control Register (MDYCON)

Table 3 Clock and Melody Control Register, MDYCON (address 13H; access type R/W)

7	6	5	4	3	2	1	0
0	0	0	0	0	EDCO	DIV3	EMO

Table 4 Description of MDYCON bits

BIT	SYMBOL	DESCRIPTION
7 to 3	–	These bits are set to a logic 0.
2	EDCO	Enable DTMF clock output. If bit EDCO = 0, then DP1.7/DCO is a general purpose derivative port line. If bit EDCO = 1, then DP1.7/DCO is the DTMF clock output. EDCO = 1 does not inhibit the port instructions for DP1.7/DCO. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by derivative port instructions. However, the port flip-flop of DP1.7/DCO must remain set to avoid conflicts between DTMF clock and port outputs.
1	DIV3	Enable DTMF clock divider. If bit DIV3 = 0, then the DTMF clock $f_{DTMF} = f_{xtal}$. If bit DIV3 = 1, then $f_{DTMF} = 1/3 \times f_{xtal}$.
0	EMO	Enable Melody Output. If bit EMO = 0, then P1.7/MDY is a standard port line. If bit EMO = 1, then P1.7/MDY is the melody output. EMO = 1 does not inhibit the port instructions for P1.7/MDY. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by port instructions. However, the port flip-flop of P1.7/MDY must remain set to avoid conflicts between melody and port outputs. When the HGF contents are zero while EMO = 1, P1.7/MDY is in the HIGH state.

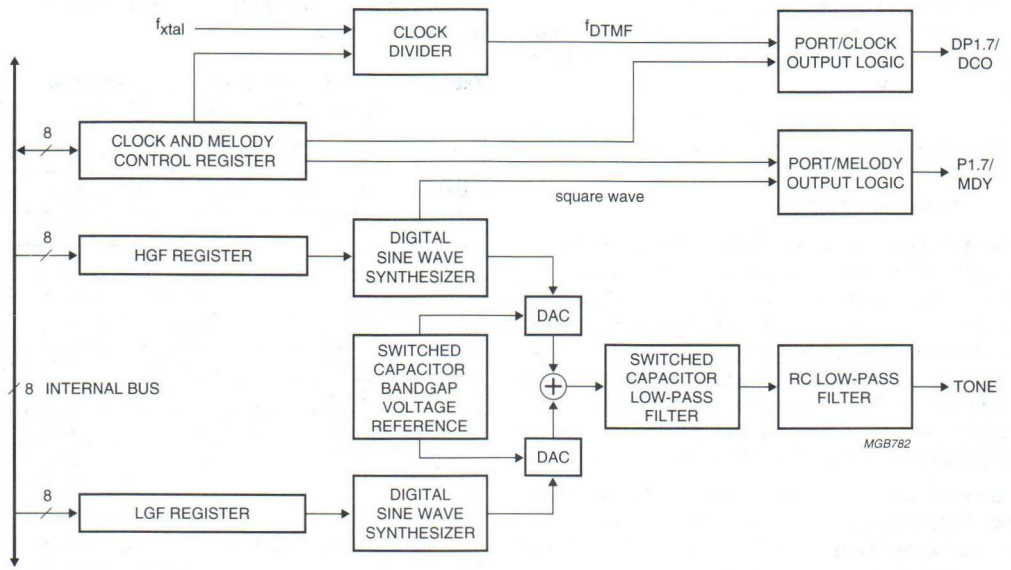


Fig.3 Block diagram of the frequency generator, melody output (P1.7/MDY) and DTMF clock output (DP1.7/DCO).

6.2 Melody output (P1.7/MDY)

The melody output (P1.7/MDY) is very useful for generating musical notes when a purely sinusoidal signal is not required, such as for ringer applications.

The square wave (duty cycle = $^{12}/_{23}$ or 52%) will include the attenuated harmonics of the base frequency, which is defined by the contents of the HGF register (Table 2). However, even higher frequency notes may be produced since the low-pass filtering on the TONE output is not applied to the P1.7/MDY output. This results in the minimum decimal value x in the HGF register (see equation in Section 6.4) being 2 for the P1.7/MDY output, rather than 60 for the TONE output. A sinusoidal TONE output is produced at the same time as the melody square wave, but due to the filtering, the higher frequency sine waves produced when $x < 60$ will not appear at the TONE output.

Since the melody output is shared with P1.7, the port flip-flop of P1.7 has to be set HIGH before using the melody output. This is to avoid conflicts between melody and port outputs. The melody output drive depends on the configuration of port P1.7/MDY, see Chapter 14, Table 27.

6.3 DTMF clock divider and output (DP1.7/DCO)

The DTMF clock divider allows the DTMF part to run either with the main clock frequency ($f_{DTMF} = f_{xtal}$) or with a third of it ($f_{DTMF} = {}^1/_3 \times f_{xtal}$) depending on the state of the divider control bit DIV3 in register MDYCON.

For low power applications, a 3.58 MHz quartz crystal or PXE resonator can be chosen together with the divide-by-one function of the clock divider.

For other applications a 10.74 MHz quartz crystal or PXE resonator may be chosen together with the divide-by-three function of the clock divider. This triples the program speed of the microcontroller, thereby keeping the assumed DTMF frequency of 3.58 MHz.

Since a 3.58 MHz clock is needed for peripheral telephony circuits such as the analog voice scrambler/descrambler PCD4440T, a switchable DTMF clock output is provided depending on the state of the enable clock output bit EDCO in register MDYCON.

If EDCO = 1 and DIV3 = 1 in the MDYCON register: a square wave with the frequency $f_{DTMF} = 1/3 \times f_{xtal}$ is output on the derivative port line DP1.7/DCO. If EDCO = 1 and DIV3 = 0: a square wave with the frequency $f_{DTMF} = f_{xtal}$ is output on the derivative port line DP1.7/DCO.

The melody output drive depends on the configuration of port P1.7/MDY, see Chapter 14, Table 27.

6.4 Frequency registers

The two frequency registers HGF and LGF define two frequencies. From these, the digital sine synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures tone output levels independent of supply voltage and temperature. The amplitude of the Low Group Frequency sine wave is attenuated by 2 dB compared to the amplitude of the High Group Frequency sine wave.

The two sine waves are summed and then filtered by an on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

The value 00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption.

The frequency 'f' of the sine wave generated from either of the frequency registers is a function of the clock frequency 'f_{xtal}' and the decimal value 'x' held in the register. The equation relating these variables is:

$$f = \frac{f_{xtal}}{[23\,(x+2)]}; \text{ where } 60 \leq x \leq 255.$$

The frequency limitation given by $x \geq 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

6.5 DTMF frequencies

Assuming an oscillator frequency f_{xtal} = 3.58 MHz, the DTMF standard frequencies can be implemented as shown in Table 5.

The relationships between telephone keyboard symbols, DTMF frequency pairs and the frequency register contents are given in Table 6.

Table 5 DTMF standard frequencies and their implementation; value = LGF, HGF contents

VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 6 Dialling symbols, corresponding DTMF frequency pairs and frequency register contents

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
•	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

6.6 Modem frequencies

Again assuming an oscillator frequency f_{xtal} = 3.58 MHz, the standard modem frequencies can be implemented as in Table 7. It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling Low Group Frequency generation.

Table 7 Standard modem frequencies and their implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980[1]	978.82	−0.12	−1.18
82	1180[1]	1179.03	−0.08	−0.97
8F	1070[2]	1073.33	0.31	3.33
79	1270[2]	1265.30	−0.37	−4.70
80	1200[3]	1197.17	−0.24	−2.83
45	2200[3]	2192.01	−0.36	−7.99
76	1300[4]	1296.94	−0.24	−3.06
48	2100[4]	2103.14	0.15	3.14
5C	1650[1]	1655.66	0.34	5.66
52	1850[1]	1852.77	0.15	2.77
4B	2025[2]	2021.20	−0.19	−3.80
44	2225[2]	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

6.7 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{xtal} = 3.58 MHz (Table 8). It is suggested to define the frequency by the HGF register while the LGF contains 00H, disabling Low Group Frequency generation.

Table 8 Musical scale frequencies and their implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD[1]	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 @ 440 Hz.

7 EEPROM AND TIMER 2 ORGANIZATION

The PCD3350A has 256 bytes of Electrically Erasable Programmable Read Only Memory (EEPROM). Such non-volatile storage provides data retention without the need for battery backup. In telecom applications, the EEPROM is used for storing redial numbers and for short dialling of frequently used numbers. More generally, EEPROM may be used for customizing microcontrollers, such as to include a PIN code or a country code, to define trimming parameters, to select application features from the range stored in ROM.

The most significant difference between a RAM and an EEPROM is that a bit in EEPROM, once written to a logic 1, cannot be cleared by a subsequent write operation. Successive write accesses actually perform a logical OR with the previously stored information. Therefore, to clear a bit, the whole byte must be erased and re-written with the particular bit cleared. Thus, an erase-and-write operation is the EEPROM equivalent of a RAM write operation.

Whereas read access times to an EEPROM are comparable to RAM access times, write and erase access times are much slower at 5 ms each. To make these operations more efficient, several provisions are available in the PCD3350A.

First, the EEPROM array is structured into 64 four-byte pages (see Fig.4) permitting access to 4 bytes in parallel (write page, erase/write page and erase page). It is also possible to erase and write individual bytes.

Finally, the EEPROM address register provides auto-incrementing, allowing very efficient read and write accesses to sequential bytes.

To simplify the erase and write timing, the derivative 8-bit down-counter (Timer 2) with reload register is provided. In addition to EEPROM timing, Timer 2 can be used for general real-time tasks, such as for measuring signal duration and for defining pulse widths.

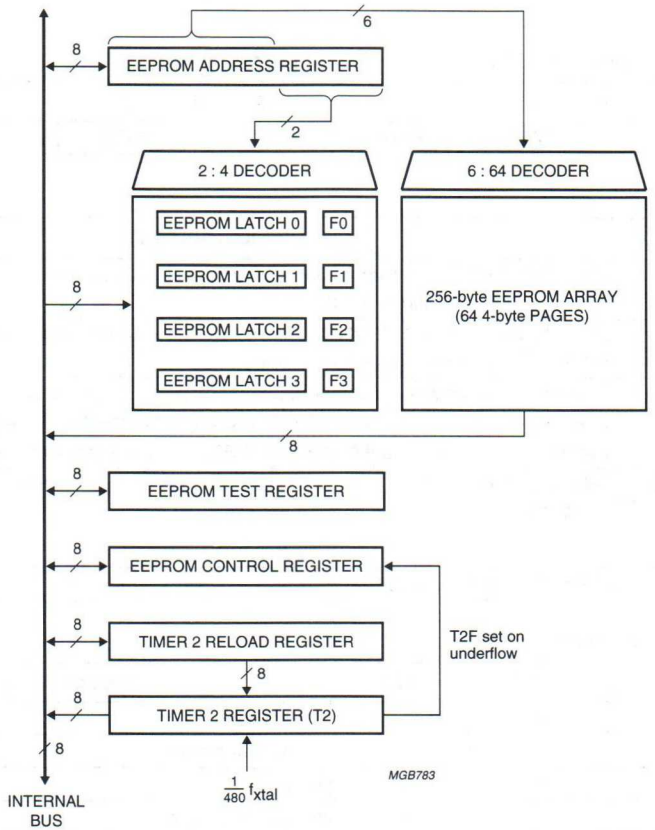


Fig.4 Block diagram of the EEPROM and Timer 2.

7.1 EEPROM registers

7.1.1 EEPROM Control Register (EPCR)

The behaviour of the EEPROM and Timer 2 section is defined by the EEPROM Control Register, as detailed in Tables 9, 10 and 11.

Table 9 EEPROM Control Register, EPCR (address 04H, access type R/W)

7	6	5	4	3	2	1	0
STT2	ET2I	T2F	EWP	MC3	MC2	MC1	0

Table 10 Description of EPCR bits

BIT	SYMBOL	DESCRIPTION
7	STT2	Start T2. If STT2 = 0, then Timer 2 is stopped; T2 value held. If STT2 = 1, then T2 decrements from reload value.
6	ET2I	Enable T2 interrupt. If ET2I = 0, then T2F event cannot request interrupt. If ET2I = 1, then T2F event can request interrupt.
5	T2F	Timer 2 flag. Set when T2 underflows (or by program); reset by program.
4	EWP	Erase or write in progress (EWP). Set by program (EWP starts EEPROM erase and/or write and Timer 2). Reset at the end of EEPROM erase and/or write.
3	MC3	Mode control 3 to 1. These three bits in conjunction with bit EWP select the mode as shown in Table 11.
2	MC2	
1	MC1	
0	–	This bit is set to a logic 0.

Table 11 Mode selection; X = don't care

EWP	MC3	MC2	MC1	DESCRIPTION
0	0	0	0	read byte
0	0	1	0	increment mode
1	0	1	X	write page
1	1	0	0	erase/write page
1	1	1	1	erase page
X	0	0	1	not allowed
X	1	0	1	
X	1	1	0	

7.1.2 EEPROM ADDRESS REGISTER (ADDR)

The EEPROM Address Register (ADDR) determines the EEPROM location to which an EEPROM access is directed.

As a whole, ADDR auto-increments after read and write cycles to EEPROM, but remains fixed after erase cycles. This behaviour generates the correct ADDR contents for sequential read accesses and for sequential write or erase/write accesses with intermediate page setup. Overflow of the 8-bit counter wraps around to zero. See Tables 12 and 13.

Table 12 EEPROM Address Register, ADDR (address 01H, access type R/W)

7	6	5	4	3	2	1	0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 13 Description of ADDR bits

BIT	SYMBOL	DESCRIPTION
7 to 2	AD7 to AD2	AD7 to AD2 select one of 64 pages.
1 to 0	AD1 to AD0	AD1 and AD0 are irrelevant during erase and write cycles. For read accesses, AD0 and AD1 indicate the byte location within an EEPROM page. During page setup, finally, AD0 and AD1 select EEPROM Latch 0 to 3 whereas AD2 to AD6 are irrelevant. If increment mode (see Table 11) is active during page setup, the subcounter consisting of AD0 and AD1 increments after every write to an EEPROM latch, thus enhancing access to sequential EEPROM latches. Incrementing stops when EEPROM Latch 3 is reached, i.e. when AD0 and AD1 are both a logic 1.

7.1.3 EEPROM DATA REGISTER (DATR)

Table 14 EEPROM Data Register, DATR (address 03H; access type R/W)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 15 Description of DATR bits

BIT	SYMBOL	DESCRIPTION
7 to 0	D7 to D0	The EEPROM Data Register (DATR) is only a conceptual entity. A read operation from DATR, reads out the EEPROM byte addressed by ADDR. On the other hand, a write operation to DATR, loads data into the EEPROM latch (see Fig.4) defined by bits AD0 and AD1 of ADDR.

7.1.4 EEPROM TEST REGISTER (TST)

The EEPROM Test Register is used for testing purposes during device manufacture. It must not be accessed by the device user.

7.2 EEPROM latches

The four EEPROM latches (EEPROM Latch 0 to 3; Fig.4) cannot be read by user software. Due to their construction, the latches can only be preset, but not cleared. Successive write operations through DATR to the EEPROM latches actually perform a logical OR with the previously stored data in EEPROM. The EEPROM latches are reset at the conclusion of any EEPROM cycle.

7.3 EEPROM flags

The four EEPROM flags (F0 to F3; Fig.4) cannot be directly accessed by user software. An EEPROM flag is set as a side-effect when the corresponding EEPROM latch is written through DATR. The EEPROM flags are reset at the conclusion of any EEPROM cycle.

7.4 EEPROM macros

The instruction sequence used in an EEPROM access should be treated as an indivisible entity. Erroneous programs result if ADDR, DATR, RELR or EPCR are inadvertently changed during an EEPROM cycle or its setup. Special care should be taken if the program may asynchronously divert due to an interrupt. A new access to the EEPROM may only be initiated when no write, erase or erase/write cycles are in progress. This can be verified by reading bit EWP (register EPCR).

For write, erase and erase/write cycles, it is assumed that the Timer 2 Reload Register (RELR) has been loaded with the appropriate value for a 5 ms delay, which depends on f_{xtal} (see Table 22). The end of a write, erase or erase/write cycle will be signalled by a cleared EWP and by a Timer 2 interrupt provided that ET2I = 1 and that the derivative interrupt is enabled.

7.5 EEPROM access

One read, one write, one erase/write and one erase access are defined by bits EWP and MC1 to MC3 in the EPCR register; see Table 9.

Read byte retrieves the EEPROM byte addressed by ADDR when DATR is read. Read cycles are instantaneous.

Write and erase cycles take 5 ms, however. Erase/write is a combination of an erase and a subsequent write cycle, consequently taking 10 ms.

As their names imply, **write page, erase page and erase/write page** are applied to a whole EEPROM page. Therefore, bits AD0 and AD1 of register ADDR (see Table 12), defining the byte location within an EEPROM page, are irrelevant during write and erase cycles. However, write and erase cycles need not affect all bytes of the page. The EEPROM flags F0 to F3 (see Fig.4) determine which bytes within the EEPROM page are affected by the erase and/or write cycles. A byte whose corresponding EEPROM flag is zero remains unchanged.

With erase page, a byte is erased if its corresponding EEPROM flag is set. With write page, data in EEPROM Latch 0 to 3 (Fig.4) are ORed to the individual page bytes if and only if the corresponding EEPROM flags are set.

In an erase/write cycle, F0 to F3 select which page bytes are erased and ORed with the corresponding EEPROM latches. ORing, in this case, means that the EEPROM latches are copied to the selected page bytes.

The described page-wise organization of erase and write cycles allows up to four bytes to be individually erased or written within 5 ms. This advantage necessitates a preparation step, called **page setup**, before the actual erase and/or write cycle can be executed.

Page setup controls EEPROM latches and EEPROM flags. This will be described in the Sections 7.5.1 to 7.5.5.

7.5.1 PAGE SETUP

Page setup is a preparation step required before write page, erase page and erase/write page cycles.
As previously described, these page operations include single-byte write, erase and erase/write as a special case. EEPROM flags F0 to F3 determine which page bytes will be affected by the mentioned page operations. EEPROM Latch 0 to 3 must be preset through DATR to specify the write cycle data to EEPROM and to set the EEPROM flags as a side-effect.

Obviously, the actual preset value of the EEPROM latches is irrelevant for erase page. Preset of one, two, three or all four EEPROM latches and the corresponding EEPROM flags can be performed by repeatedly defining ADDR and writing to DATR (see Table 16).

If more than one EEPROM latch must be preset, the subcounter consisting of AD0 and AD1 can be induced to auto-increment after every write to DATR, thus stepping through all EEPROM latches. For this purpose, increment mode (Table 11) must be selected. Auto-incrementing stops at EEPROM Latch 3. It is not mandatory to start at EEPROM Latch 0 as in shown in Table 17.

Note that AD2 to AD7 are irrelevant during page setup. They will usually specify the intended EEPROM page, anticipating the subsequent page cycle.

From now on, it will be assumed that AD2 to AD7 will contain the intended EEPROM page address after page setup.

Table 16 Page setup; preset

INSTRUCTION	RESULT
MOV A, #addr	address of EEPROM latch
MOV ADDR, A	send address to ADDR
MOV A, #data	load write, erase/write or erase data
MOV DATR, A	send data to addressed EEPROM latch

Table 17 Page setup; auto-incrementing

INSTRUCTION	RESULT
MOV A, #MC2	increment mode control word
MOV EPCR, A	select increment mode
MOV A, #baddr	EEPROM Latch 0 address (AD0 = AD1 = 0)
MOV ADDR, A	send EEPROM Latch 0 address to ADDR
MOV A, R0	load 1st byte from Register 0
MOV DATR, A	send 1st byte to EEPROM Latch 0
MOV A, R1	load 2nd byte from Register 1
MOV DATR, A	send 2nd byte to EEPROM Latch 1
MOV A, R2	load 3rd byte from Register 2
MOV DATR, A	send 3rd byte to EEPROM Latch 2
MOV A, R3	load 4th byte from Register 3
MOV DATR, A	send 4th byte to EEPROM Latch 3

7.5.2 READ BYTE

Since ADDR auto-increments after a read cycle regardless of the page boundary, successive bytes can efficiently be read by repeating the last instruction.

Table 18 Read byte

INSTRUCTION	RESULT
MOV A, #RDADDR	load read address
MOV ADDR, A	send address to ADDR
MOV A, DATR	read EEPROM data

7.5.3 WRITE PAGE

The write cycle performs a logical OR between the data in the EEPROM latches and that in the addressed EEPROM page. To actually copy the data from the EEPROM latches, the corresponding bytes in the page should previously have been erased.

The EEPROM latches are preset as described in Section 7.5.1. The actual transfer to the EEPROM is then performed as shown in Table 19.

The last instruction also starts Timer 2. The data in the EEPROM latches are ORed with that in the corresponding page bytes within 5 ms. A single-byte write is simply a special case of 'write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by bits AD2 to AD7) and to EEPROM Latch 0 (by bits AD0 and AD1). This allows efficient coding of multi-page write operations.

Table 19 Write page

INSTRUCTION	RESULT
MOV A, #EWP + MC2	'write page' control word
MOV EPCR, A	start 'write page' cycle

7.5.4 ERASE/WRITE PAGE

The EEPROM latches are preset as described in Section 7.5.1. The page bytes corresponding to the asserted flags (among F0 to F3) are erased and re-written with the contents of the respective EEPROM latches.

The last instruction also starts Timer 2. Erasure takes 5 ms upon which Timer Register T2 reloads for another 5 ms cycle for writing. The top cycles together take 10 ms. A single-byte erase/write is simply a special case of 'erase/write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by AD2 to AD7) and to EEPROM Latch 0 (by AD0 and AD1). This allows efficient coding of multi-page erase/write operations.

Table 20 Erase/write page

INSTRUCTION	RESULT
MOV A, #EWP + MC3	'erase/write page' control word
MOV EPCR, A	start 'erase/write page' cycle

7.5.5 ERASE PAGE

The EEPROM flags are set as described in Section 7.5.1. The corresponding page bytes are erased.

The last instruction also starts Timer 2. Erasure takes 5 ms. A single-byte erase is simply a special case of 'erase page'.

Note that ADDR does not auto-increment after an erase cycle.

Table 21 Erase page

INSTRUCTION	RESULT
MOV A, #EWP + MC3 + MC2 + MC1	'erase page' control word
MOV EPCR, A	start 'erase page' cycle

7.6 Timer 2

Timer 2 is a 8-bit down-counter decremented at a rate of $1/480 \times f_{xtal}$. It may be used either for EEPROM timing or as a general purpose timer. Conflicts between the two applications should be carefully avoided.

7.6.1 TIMER 2 FOR EEPROM TIMING

When used for EEPROM timing, Timer 2 serves to generate the 5 ms intervals needed for erasing or writing the EEPROM. At the decrement rate of $1/480 \times f_{xtal}$, the reload value for a 5 ms interval is a function of f_{xtal}. Table 22 summarizes the required reload values for a number of oscillator frequencies.

Timer 2 is started by setting bit EWP in the EPCR. The Timer Register T2 is loaded with the reload value from RELR. T2 decrements to zero.

For an erase/write cycle, underflow of T2 indicates the end of the erase operation. Therefore, Timer Register T2 is reloaded from RELR for another 5 ms interval during which the flagged EEPROM latches are copied to the corresponding bytes in the page addressed by ADDR.

The second underflow of an erase/write cycle and the first underflow of write page and erase page conclude the corresponding EEPROM cycle. Timer 2 is stopped, T2F is set whereas EWP and MC1 to MC3 are cleared.

Table 22 Reload values as a function of f_{xtal}

f_{xtal} (MHz)	RELOAD VALUE[1] (HEX)
1	0A
2	14
3.58	25
6	3E
10.74	6F
16	A6

Note

1. The reload value is $(5 \times 10^{-3} \times 1/480 \times f_{xtal}) - 1$; f_{xtal} in MHz.

7.6.2 TIMER 2 AS A GENERAL PURPOSE TIMER

When used for purposes other than EEPROM timing, Timer 2 is started by setting STT2. The Timer 2 Register T2 (see Table 28) is loaded with the reload value from RELR. T2 decrements to zero. On underflow, T2 is reloaded from RELR, T2F is set and T2 continues to decrement.

Timer 2 can be stopped at any time by clearing STT2. The value of T2 is then held and can be read out. After setting STT2 again, Timer 2 decrements from the reload value. Alternatively, it is possible to read T2 'on the fly' i.e. while Timer 2 is operating.

8 REAL-TIME CLOCK

The Real Time Clock (RTC) consists of a 32 kHz crystal oscillator, a 32 kHz to 1 second or 1 minute divider chain, an 8-bit Frequency Adjustment Register and the Clock Control Register. The complete RTC section works independently of the microcontroller status, even in Idle and Stop mode.

8.1 Oscillator

The internal 32 kHz oscillator needs an external quartz crystal with a frequency of 32768.00 Hz (a positive deviation up to $+259 \times 10^{-6}$ is allowed) and an external feedback resistor between pins RTC1 and RTC2; 4.7 MΩ is recommended. It is controlled by the RUN-bit in the Clock Control Register.

8.2 Divider chain

The divider chain operates with the 32 kHz oscillator output and divides this signal down to two clocks with a period of 1 second or 1 minute. Depending on bit ITS in the Clock Control Register, the falling edge of the seconds or minutes clock is used to set the Clock Interrupt Flag (CIF) in the Clock Control Register.

Since the clock interrupt is used to let the microcontroller leave the Stop mode, it is ORed to the external interrupt (CE/$\overline{T0}$) and has the same functionality, e.g. it must be enabled in the Clock Control Register (bit ECI) and by execution of the instruction 'EN I'. The clock interrupt will then be treated as an external interrupt.

Additionally, the divider chain generates a 16 kHz clock (RCO) that can be routed through derivative port line DP0.0/RCO, controlled by bit ERCO in the Clock Control Register.

8.3 Frequency adjustment

The frequency adjustment is used to extend the interrupt time by defining the number of 16 kHz clocks in the Frequency Adjustment Register that will be counted twice within the first second period after a minute interrupt.

If the second interrupt is used (ITS = 1), every 60^{th} interval may be up to 15.3 ms longer than the others as a result of the frequency adjustment. The adjusted Minute Interrupt Time (MIT) now shows a maximum deviation of 0.5×10^{-6}.

8.4 Real-time clock derivative registers

8.4.1 Clock Control Register (CLCR)

The register access type is R/W and the value at reset is 00H.

Table 23 Clock Control Register, CLCR (address 20H)

7	6	5	4	3	2	1	0
0	TST2	TST1	ERCO	RUN	ITS	CIF	ECI

Table 24 Description of CLCR bits

BIT	SYMBOL	DESCRIPTION
7	–	This bit is set to a logic 0.
6	TST2	Test 2 input. This is a testing bit; has to be fixed at a logic 0 by user software.
5	TST1	Test 1 input. This is a testing bit; has to be fixed at a logic 0 by user software.
4	ERCO	Enable 16 kHz clock output. If ERCO = 0, then the DP0.0/RCO is a derivative port line. If ERCO = 1, then DP0.0./RCO is a 16 kHz clock output. ERCO = 1 does not inhibit the port instructions for DP0.0/RCO. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by derivative port instructions. However, the port flip-flop of DP0.0/RCO must remain set to avoid conflicts between 16 kHz clock and port outputs.
3	RUN	Clock run or stop bit. If RUN = 0, then the oscillator is stopped and the clock is reset. If RUN = 1, then the oscillator and the clock are running.
2	ITS	Interrupt Time Select. If ITS = 1, then the interrupt time is one second. If ITS = 0, then the interrupt time is one minute.
1	CIF	Clock Interrupt Flag. Set by hardware, if RTC divider chain overflows (every second or minute depending on ITS) or by program. Reset by program.
0	ECI	Enable Clock Interrupt. If ECI = 0, then CIF event cannot request interrupt. If ECI = 1, then CIF event requests interrupt.

8.4.2 Frequency Adjustment Register (FAR)

The frequency adjustment value of the RTC is defined by the 8-bit Frequency Adjustment Register. The register access type is R/W. The value of FAR at reset is 00H.

The significance of the individual bits of FAR can be illustrated by the following equation:

$$\text{Minute Interrupt Time (MIT)} = \left(60 \times 2^{\frac{14}{f_{RCO}}} \right) + \frac{FAR}{2^{14}}$$

where f_{RCO} = RTC frequency and 'FAR' is the decimal contents of the Frequency Adjustment Register.

Table 26 shows the recommended correction factor FAR for all allowed RTC frequencies f_{RCO}.

Table 25 Frequency Adjustment Register, FAR (address 21H)

7	6	5	4	3	2	1	0
FAR7	FAR6	FAR5	FAR4	FAR3	FAR2	FAR1	FAR0

Table 26 FAR as a result of f_{RCO}

f_{RCO}	FAR (HEX)
16384.000	00
16384.018	01
16384.033	02
16384.051	03
16384.066	04
16384.084	05
16384.100	06
16384.117	07
16384.135	08
16384.150	09
16384.168	0A
16384.184	0B
16384.201	0C
16384.217	0D
16384.234	0E
16384.250	0F
16384.268	10
16384.283	11
16384.301	12
16384.316	13
16384.334	14
16384.350	15
16384.367	16
16384.385	17
16384.400	18
16384.418	19
16384.434	1A
16384.451	1B
16384.467	1C
16384.484	1D
16384.500	1E
16384.518	1F
16384.533	20
16384.551	21
16384.566	22
16384.584	23
16384.600	24
16384.617	25
16384.635	26
16384.650	27
16384.668	28
16384.684	29
16384.701	2A
16384.717	2B
16384.734	2C
16384.750	2D
16384.768	2E
16384.783	2F
16384.801	30
16384.816	31
16384.834	32
16384.850	33
16384.867	34
16384.885	35
16384.900	36
16384.918	37
16384.934	38
16384.951	39
16384.967	3A
16384.984	3B
16385.000	3C
16385.018	3D
16385.033	3E
16385.051	3F
16385.066	40
16385.084	41
16385.100	42
16385.117	43
16385.135	44
16385.150	45
16385.168	46
16385.184	47
16385.201	48
16385.217	49
16385.234	4A
16385.250	4B
16385.268	4C
16385.283	4D
16385.301	4E
16385.316	4F
16385.334	50
16385.350	51
16385.367	52
16385.385	53
16385.400	54
16385.418	55
16385.434	56
16385.451	57
16385.467	58
16385.484	59
16385.500	5A
16385.518	5B

f_{RCO}	FAR (HEX)
16385.533	5C
16385.551	5D
16385.566	5E
16385.584	5F
16385.600	60
16385.617	61
16385.635	62
16385.650	63
16385.668	64
16385.684	65
16385.701	66
16385.717	67
16385.734	68
16385.750	69
16385.768	6A
16385.783	6B
16385.801	6C
16385.816	6D
16385.834	6E
16385.850	6F
16385.867	70
16385.885	71
16385.900	72
16385.918	73
16385.934	74
16385.951	75
16385.967	76
16385.984	77

f_{RCO}	FAR (HEX)
16386.000	78
16386.018	79
16386.033	7A
16386.051	7B
16386.066	7C
16386.084	7D
16386.100	7E
16386.117	7F
16386.135	80
16386.150	81
16386.168	82
16386.184	83
16386.201	84
16386.217	85
16386.234	86
16386.250	87
16386.268	88
16386.283	89
16386.301	8A
16386.316	8B
16386.334	8C
16386.350	8D
16386.367	8E
16386.385	8F
16386.400	90
16386.418	91
16386.434	92
16386.451	93

f_{RCO}	FAR (HEX)
16386.467	94
16386.484	95
16386.500	96
16386.518	97
16386.533	98
16386.551	99
16386.566	9A
16386.584	9B
16386.600	9C
16386.617	9D
16386.635	9E
16386.650	9F
16386.668	A0
16386.684	A1
16386.701	A2
16386.717	A3
16386.734	A4
16386.750	A5
16386.768	A6
16386.783	A7
16386.801	A8
16386.816	A9
16386.834	AA
16386.850	AB
16386.867	AC
16386.885	AD
16386.900	AE
16386.918	AF

f_{RCO}	FAR (HEX)
16386.934	B0
16386.951	B1
16386.967	B2
16386.984	B3
16387.000	B4
16387.018	B5
16387.033	B6
16387.051	B7
16387.066	B8
16387.084	B9
16387.100	BA
16387.117	BB
16387.135	BC
16387.150	BD
16387.168	BE
16387.184	BF
16387.201	C0
16387.217	C1
16387.234	C2
16387.250	C3
16387.268	C4
16387.283	C5
16387.301	C6
16387.316	C7
16387.334	C8
16387.350	C9
16387.367	CA

f_{RCO}	FAR (HEX)
16387.385	CB
16387.400	CC
16387.418	CD
16387.434	CE
16387.451	CF
16387.467	D0
16387.484	D1
16387.500	D2
16387.518	D3
16387.533	D4
16387.551	D5
16387.566	D6
16387.584	D7
16387.600	D8
16387.617	D9
16387.635	DA
16387.650	DB
16387.668	DC
16387.684	DD
16387.701	DE
16387.717	DF
16387.734	E0
16387.750	E1
16387.768	E2
16387.783	E3
16387.801	E4
16387.816	E5

f_{RCO}	FAR (HEX)
16387.834	E6
16387.850	E7
16387.867	E8
16387.885	E9
16387.900	EA
16387.918	EB
16387.934	EC
16387.951	ED
16387.967	EE
16387.984	EF
16388.002	F0
16388.018	F1
16388.035	F2
16388.051	F3
16388.068	F4
16388.084	F5
16388.102	F6
16388.117	F7
16388.135	F8
16388.152	F9
16388.168	FA
16388.186	FB
16388.201	FC
16388.219	FD
16388.234	FE
16384.000	FF

9 DERIVATIVE INTERRUPTS

One derivative interrupt event is defined. It is controlled by bits T2F and ET2I in the EPCR (see Tables 9 and 10).

The derivative interrupt event occurs when T2F is set. This request is honoured under the following circumstances:

- No interrupt routine proceeds
- No external interrupt request is pending
- The derivative interrupt is enabled
- ET2I is set.

The derivative interrupt routine must include instructions that will remove the cause of the derivative interrupt by explicitly clearing T2F. If the derivative interrupt is not used, T2F may directly be tested by the program. Obviously, T2F can also be asserted under program control, e.g. to generate a software interrupt.

Although the clock interrupt is part of a derivative function it is linked to the external interrupt. A clock interrupt request is honoured under the following circumstances:

- No interrupt routine proceeds
- No external interrupt request is pending
- The enable clock interrupt bit in the derivative clock control register is set.

10 TIMING

Although the PCD3350A operates over a clock frequency range from 1 to 16 MHz, f_{xtal} = 3.58 MHz or 10.74 MHz will usually be chosen to take full advantage of the frequency generator (DTMF) section.

11 RESET

In addition to the conditions given in the *"PCD33xxA Family"* data sheet, all derivative registers are cleared in the reset state.

12 IDLE MODE

In Idle mode all derivative functions remain operative, i.e.:

- DTMF generator
- DTMF clock divider and output
- 32 kHz crystal oscillator and RTC
- EEPROM and Timer 2 sections.

13 STOP MODE

Since the oscillator is switched off, the frequency generator, the EEPROM and the Timer 2 sections receive no clock. It is suggested to clear both the HGF and the LGF registers before entering Stop mode. This will cut off the biasing of the internal amplifiers, considerably reducing current requirements.

The Stop mode **must not** be entered while an erase and/or write access to EEPROM is in progress. The STOP instruction may only be executed when EWP in EPCR is zero. The Timer 2 section is frozen during Stop mode. After exit from Stop mode by a HIGH level on CE/$\overline{T0}$, Timer 2 proceeds from the held state.

The 32 kHz crystal oscillator and the RTC section remain operative during Stop mode (depending only on bit RUN in the Clock Control Register). In addition to the description in the *"PCD33xxA Family"* data sheet, Stop mode may be left by a clock interrupt event (see Chapter 9).

14 SUMMARY OF I/O PORTS AND ROM MASK OPTIONS

All standard quasi-bidirectional I/O ports are available; see *"PCD33xxA Family"* data sheet.

- Port 0: 8 parallel port lines P0.0 to P0.7
- Port 1: 8 parallel port lines P1.0 to P1.7
- Port 2: 4 parallel port lines P2.0 to P2.3.

In addition to the standard ports, two derivative I/O ports are available:

- Derivative Port 0: 6 parallel port lines DP0.0 to DP0.5 (register DP0L)
- Derivative Port 1: 8 parallel port lines DP1.0 to DP1.7 (register DP1L).

The port options and the other ROM mask options are listed in Table 27. See Table 28 for the addresses of DP0L and DP1L.

Table 27 ROM mask options

FUNCTION IMPLEMENTED IN ROM	OPTION		
Program/data	Any mix of instructions and data up to ROM size of 8 kbytes.		
Port Output			
P0.0 to P0.7	standard	open-drain	push-pull
P1.0 to P1.6	standard	open-drain	push-pull
P1.7/MDY; note 1	standard	open-drain	push-pull
P2.0 to P2.3	standard	open-drain	push-pull
DP0.0 to DP0.5	standard	open-drain	push-pull
DP1.0 to DP1.6	standard	open-drain	push-pull
DP1.7/DCO; note 2	standard	open-drain	push-pull
Port State after reset			
P0.0 to P0.7	set	reset	–
P1.0 to P1.6	set	reset	–
P1.7/MDY	set	reset	–
P2.0 to P2.3	set	reset	–
DP0.0 to DP0.5	set	reset	–
DP1.0 to DP1.6	set	reset	–
DP1.7/DCO	set	reset	–
Oscillator			
Transconductance	LOW (g_{mL})	MEDIUM (g_{mM})	HIGH (g_{mH})
Power-on-reset			
Power-on-reset voltage level: V_{POR}	1.2 to 3.6 V in increments of 100 mV; OFF		

Notes

1. If standard (Option 1) or push-pull (Option 3) output is chosen, the P1.7/MDY output becomes a push-pull output. If open-drain (Option 2) is chosen, the P1.7/MDY output becomes an open-drain output.
2. If standard (Option 1) or push-pull (Option 3) output is chosen, the DP1.7/DCO output becomes a push-pull output. If open-drain (Option 2) is chosen, the DP1.7/DCO output becomes an open-drain output.

15 SUMMARY OF DERIVATIVE REGISTERS

Table 28 Register map

ADDR. (HEX)	REGISTER	7	6	5	4	3	2	1	0	R/W
00	not used									
01	EEPROM Address Register (ADDR)	0	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/W
02	not used									
03	EEPROM Data Register (DATR)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
04	EEPROM Control Register (EPCR)	STT2	ET21	TF2	EWP	MC3	MC2	MC1	0	R/W
05	Timer 2 Reload Register (RELR)	R7	R6	R5	R4	R3	R2	R1	R0	R/W
06	Timer 2 Register (T2)	T2.7	T2.6	T2.5	T2.4	T2.3	T2.2	T2.1	T2.0	R
07	Test Register (TST)	only for test purposes; not to be accessed by the device user								
08 to 10	not used									
11	High Group Frequency Register (HGF)	H7	H6	H5	H4	H3	H2	H1	H0	W
12	Low Group Frequency Register (LGF)	L7	L6	L5	L4	L3	L2	L1	L0	W
13	Clock and Melody Control Register (MDYCON)	0	0	0	0	0	DCO	DIV3	EMO	R/W
14 to 1F	not used									
20	Clock Control Register (CLCR)	0	TST2	TST1	ERCO	RUN	ITS	CIF	ECI	R/W
21	Frequency Adjustment Register (FAR)	FAR7	FAR6	FAR5	FAR4	FAR3	FAR2	FAR1	FAR0	R/W
22 to 2F	not used									
30	Derivative Port 0 lines (DP0L)	0	0	D0.5	D0.4	D0.3	D0.2	D0.1	D0.0	R
31	Derivative Port 1 lines (DP1L)	D1.7	D1.6	D1.5	D1.4	D1.3	D1.2	D1.1	D1.0	R
32	Derivative Port 0 flip-flop (DP0FF)	0	0	F0.5	F0.4	F0.3	F0.2	F0.1	F0.0	R/W
33	Derivative Port 1 flip-flop (DP1FF)	F1.7	F1.6	F1.5	F1.4	F1.3	F1.2	F1.1	F1.0	R/W
34 to FF	not used									

16 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Data Handbook IC14, Section: Handling MOS devices"*).

17 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7.0	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{SS}	ground supply current	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	–	90	°C

18 DC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz (g_{mL}); f_{RTC} = 32768 to 32768 + (32768 × 200 × 10^{-6}) Hz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	see Fig.5				
	operating	note 1	1.8	–	6	V
	RAM data retention in Stop mode		1.0	–	6	V
I_{DD}	operating supply current	see Figs 6 and 7; note 2				
		V_{DD} = 3 V; value HGF or LGF ≠ 0	–	0.8	1.6	mA
		V_{DD} = 3 V; value HGF = LGF = 0	–	0.35	0.7	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF or LGF ≠ 0; DIV3 = 1	–	2.7	6.2	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF = LGF = 0	–	1.7	4.2	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH}); value HGF = LGF = 0	–	3.5	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DD(idle)}$	supply current (Idle mode)	see Figs 8 and 9; note 2				
		V_{DD} = 3 V; value HGF or LGF ≠ 0	–	0.7	1.4	mA
		V_{DD} = 3 V; value HGF = LGF =0	–	0.25	0.5	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF or LGF ≠ 0; DIV3 = 1	–	2.3	5.5	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF = LGF = 0	–	1.3	3.5	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH}); value HGF = LGF = 0	–	2.4	–	mA
$I_{DD(stp)}$	supply current (Stop mode)	see Fig.10; notes 2 and 3				
		V_{DD} = 1.8 V; T_{amb} = 25 °C; RTC not running	–	1.0	5.5	µA
		V_{DD} = 1.8 V; T_{amb} = –25 to +70 °C; RTC not running	–	–	10	µA
		V_{DD} = 1.8 V; T_{amb} = 25 °C; RTC running	–	2.0	6.0	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	–1	–	+1	µA
Port outputs						
I_{OL}	LOW level output sink current	V_{DD} = 3 V; V_O = 0.4 V; see Fig.11	0.7	3.5	–	mA
I_{OH}	HIGH level pull-up output source current	V_{DD} = 3 V; V_O = 2.7 V; see Fig.12	–10	–30	–	µA
		V_{DD} = 3 V; V_O = 0 V; see Fig.12	–	–140	–300	µA
I_{OH1}	HIGH level push-pull output source current	V_{DD} = 3 V; V_O = 2.6 V; see Fig.13	–0.7	–3.5	–	mA
Real-time clock 32 kHz oscillator						
g_m	transconductance	$V_{i(p-p)}$ < 50 mV; see Fig.14	2	10	50	µS
$\delta f/f$	frequency adjustment		-0.6×10^{-6}	–	$+0.6 \times 10^{-6}$	
C_i	input capacitance (pin 10)		–	10	–	pF
C_o	output capacitance (pin 11)		–	10	–	pF
TONE output (see Fig.15; notes 1 and 4)						
$V_{HG(RMS)}$	HGF voltage (RMS value)		158	181	205	mV
$V_{LG(RMS)}$	LGF voltage (RMS value)		125	142	160	mV
$\Delta f/f$	frequency deviation		–0.6	–	0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_o \rvert$	output impedance		–	100	500	Ω
G_v	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	T_{amb} = 25 °C; note 5	–	–25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EEPROM (notes 1 and 6)						
n_{cyc}	endurance (erase/write cycles)	note 7	10^5	–	–	
$t_{D(ret)}$	data retention		10	–	–	years
Power-on-reset						
ΔV_{POR}	Power-on-reset level variation around chosen V_{POR}	note 8	−0.5	0	+0.5	V
Oscillator (see Fig. 17)						
g_{mL}	LOW transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
g_{mM}	MEDIUM transconductance	V_{DD} = 5 V	0.9	1.6	3.2	mS
g_{mH}	HIGH transconductance	V_{DD} = 5 V	3	4.5	9.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

Notes

1. TONE output; EEPROM erase and write require $V_{DD} \geq 2.5$ V:
   a) TONE output requires $f_{xtal} < 4$ MHz in case DIV3 = 0.
   b) TONE output requires $f_{xtal} < 12$ MHz in case DIV3 = 1.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open:
   a) Maximum values: external clock at XTAL1 and XTAL2 open-circuit.
   b) Typical values: T_{amb} = 25 °C; crystal connected between XTAL1 and XTAL2.
3. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; RESET, T1 and CE/$\overline{T0}$ at V_{SS}; crystal connected between XTAL1 and XTAL2; open-drain outputs connected to V_{SS}; all other outputs open.
4. Values are specified for DTMF frequencies only (CEPT).
5. Related to the Low Group Frequency (LGF) component (CEPT).
6. After final testing the value of each EEPROM bit is typically logic 1.
7. Verified on sampling basis.
8. V_{POR} is an option chosen by the user. Depending on its value, it may restrict the supply voltage range.

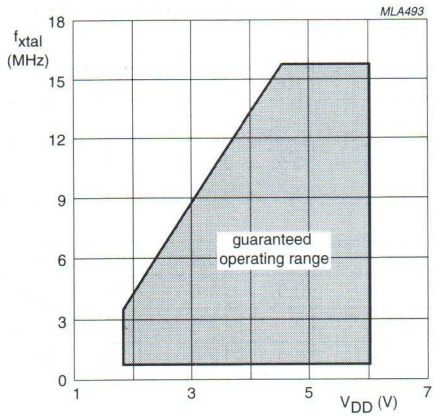
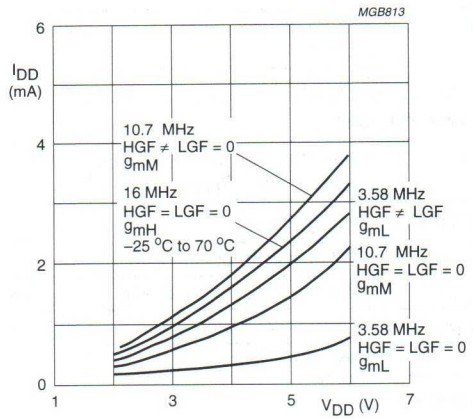
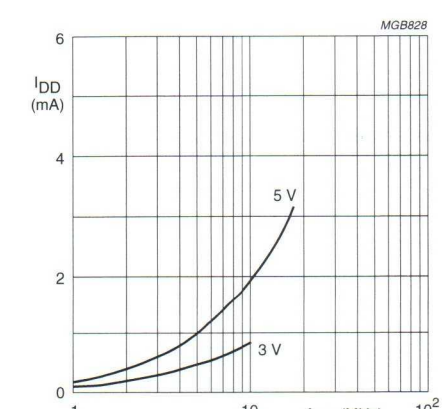


Fig.5 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).



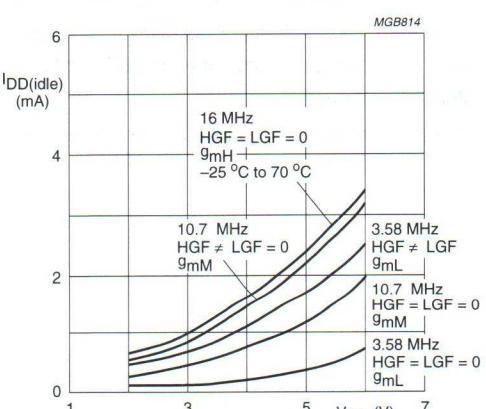
Measured with crystal between XTAL1 and XTAL2.

Fig.6 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).



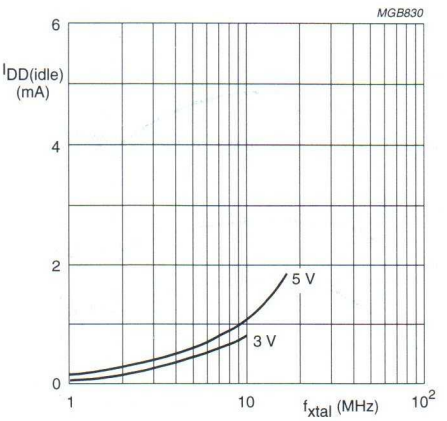
Measured with function generator on XTAL1.

Fig.7 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



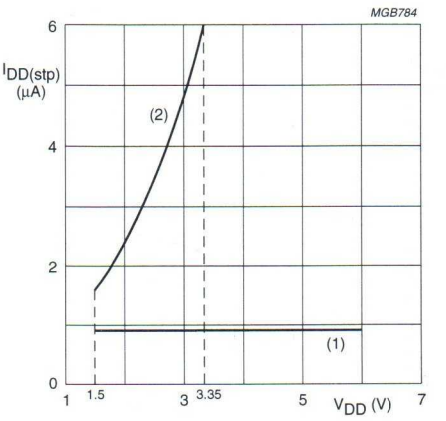
Measured with crystal between XTAL1 and XTAL2.

Fig.8 Typical supply current in Idle mode ($I_{DD(idle)}$) as a function of supply voltage (V_{DD}).



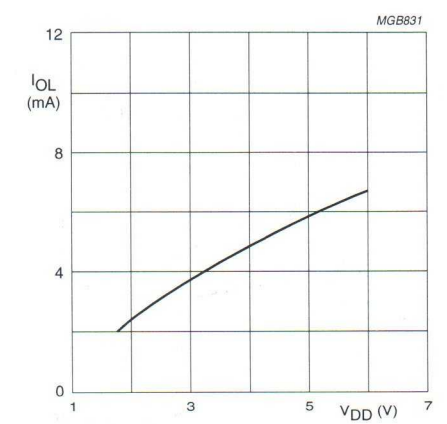
Measured with function generator on XTAL1.

Fig.9 Typical supply current in Idle mode ($I_{DD(idle)}$) as a function of clock frequency (f_{xtal}).



(1) RTC stopped; T_{amb} = −25 to +70 °C.
(2) RTC running; T_{amb} = −25 to +70 °C.

Fig.10 Typical supply current in Stop mode ($I_{DD(stp)}$) as a function of supply voltage (V_{DD}).



V_O = 0.4 V.

Fig.11 Typical LOW level output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

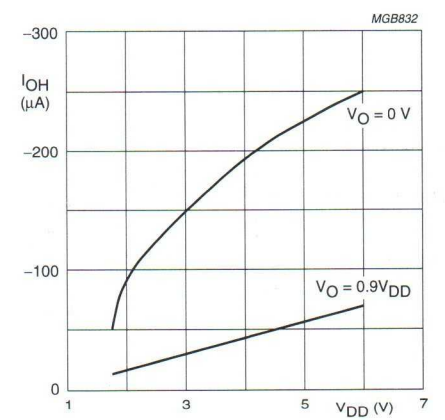
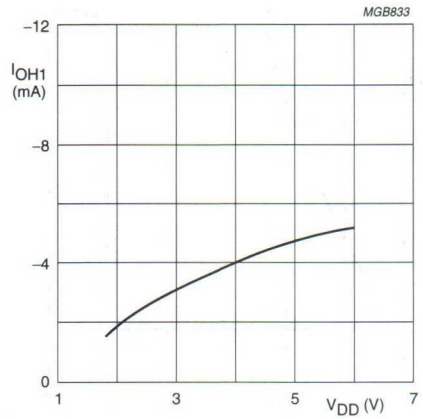


Fig.12 Typical HIGH level pull-up output source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.13 Typical HIGH level push-pull output source current (I_{OH1}) as a function of supply voltage (V_{DD}).

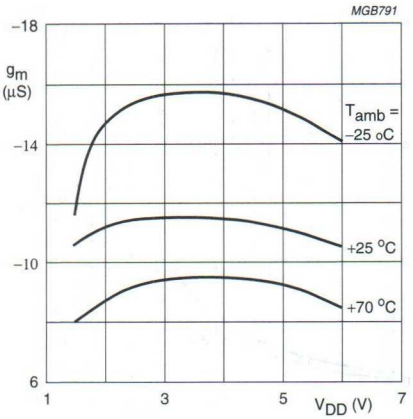
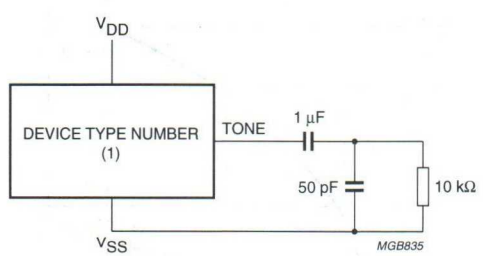


Fig.14 Typical RTC oscillator transconductance as a function of supply voltage (V_{DD}).



(1) Device type number: PCD3350A

Fig.15 Tone output test circuit.

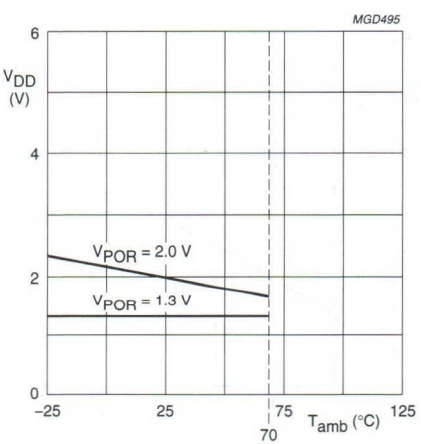


Fig.16 Typical Power-on-reset level (V_{POR}) as function of ambient temperature (T_{amb}).

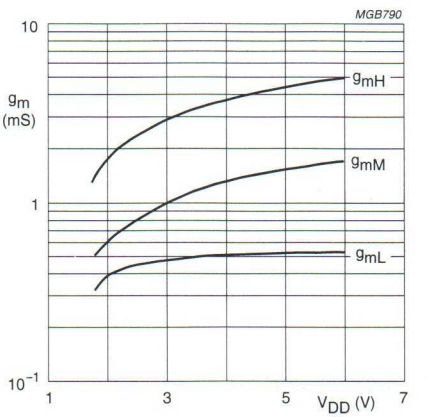


Fig.17 Typical oscillator transconductance (g_m) as a function of supply voltage (V_{DD}).

19 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = –25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.5	1	–	16	MHz

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8-bit microcontrollers with DTMF generator and 256 bytes EEPROM

PCA3354C; PCD3354A

1 FEATURES

- 8-bit CPU, ROM, RAM, EEPROM and I/O; all in a 44-lead quad flat package
- 8 kbytes ROM; 256 bytes RAM
- 256 bytes Electrically Erasable Programmable Read Only Memory (EEPROM)
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 36 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- 8-bit reloadable Timer 2
- Three single-level vectored interrupts:
  - external
  - 8-bit programmable Timer/event counter 1
  - derivative; triggered by reloadable Timer 2
- Two test inputs, one of which also serves as the external interrupt input
- DTMF, modem, musical tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT compatible)
- Melody output for ringer application
- Programmable DTMF clock divider
- Power-on-reset
- Stop and Idle modes
- Supply voltage: 1.8 to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- CPU clock frequency: 1 to 16 MHz (3.58 MHz or 10.74 MHz for DTMF)
- Operating ambient temperature:
  - –25 to +70 °C (PCD3354A)
  - 0 to 50 °C (PCA3354C)
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

This data sheet details the specific properties of the PCA3354C and PCD3354A. The shared properties of the PCD33xxA family of microcontrollers are described in the *"PCD33xxA family"* data sheet, which should be read in conjunction with this publication.

The PCA3354C and PCD3354A are microcontrollers oriented towards telephony applications. They include 8 kbytes ROM, 256 bytes RAM, 36 I/O lines, and an on-chip generator for dual tone multifrequency (DTMF), modem and musical tones. In addition to dialling, the generated frequencies can be made available as square waves for melody generation, providing ringer operation.

The PCA3354C and PCD3354A also incorporate 256 bytes of EEPROM, permitting data storage without battery backup. The EEPROM can be used for storing telephone numbers, particularly for implementing redial functions.

The differences between PCA3354C and PCD3354A are shown in Table 1.

The instruction set is similar to the MAB8048 and is a sub-set of that listed in the *"PCD33xxA family"* data sheet.

Table 1 Differences: PCA3354C and PCD3354A

TYPE	V_{POR}	AMBIENT TEMP. RANGE
PCA3354C	fixed at 2.0 V ±0.3 V	0 to 50 °C
PCD3354A	(1.2 to 3.6 V) ±0.5 V[1]	–25 to +70 °C

Note

1. See Chapter 13, Table 24.

3 ORDERING INFORMATION (see note 1)

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA3354CH	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1
PCD3354AH			

Note

1. Please refer to the Order Entry Form (OEF) for this device for the full type number to use when ordering. This type number will also specify the required program and the ROM mask options.

4 BLOCK DIAGRAM

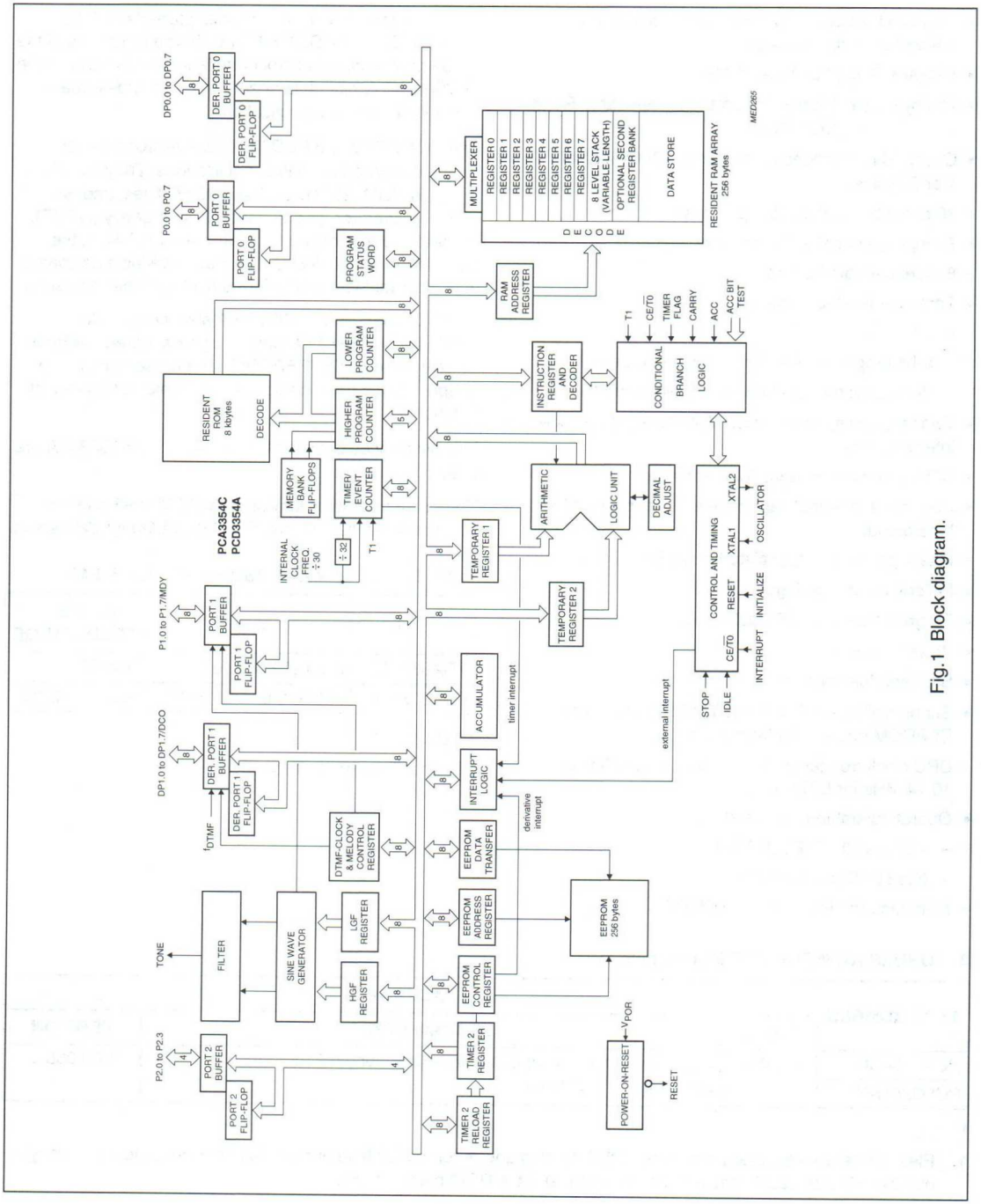


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

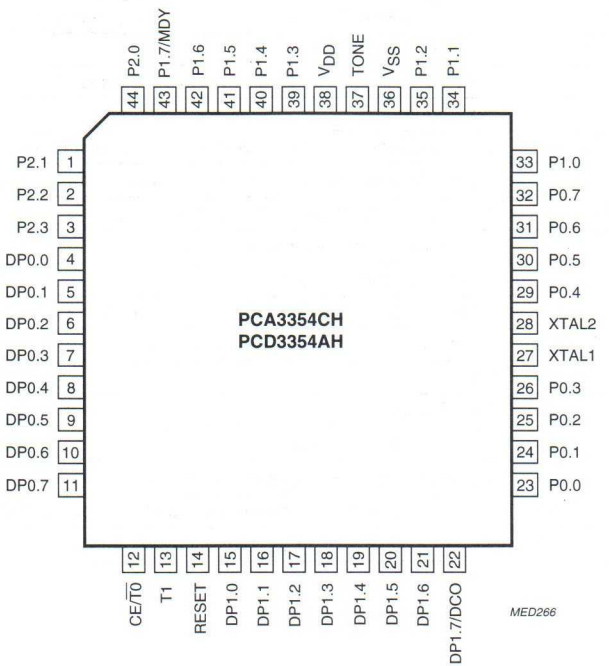


Fig.2 Pin configuration.

5.2 Pin description

Table 2 SOT205-1 package (for information on parallel I/O ports, see Chapter 13)

SYMBOL	PIN	TYPE	DESCRIPTION
P2.1 to P2.3	1 to 3	I/O	3 bits of Port 2: 4-bit quasi-bidirectional I/O port
DP0.0 to DP0.7	4 to 11	I/O	Derivative Port 0: 8-bit quasi-bidirectional I/O port
CE/$\overline{T0}$	12	I	Chip Enable or Test 0 input
T1	13	I	Test 1/count input of 8-bit Timer/event counter 1
RESET	14	I	reset input
DP1.0 to DP1.6	15 to 21	I/O	7 bits of Derivative Port 1: 8-bit quasi-bidirectional I/O port
DP1.7/DCO	22	I/O	1 bit of Derivative Port 1: 8-bit quasi-bidirectional I/O port; or DTMF clock output
P0.0 to P0.3	23 to 26	I/O	4 bits of Port 0: 8-bit quasi-bidirectional I/O port
XTAL1	27	I	crystal oscillator/external clock input
XTAL2	28	O	crystal oscillator output
P0.4 to P0.7	29 to 32	I/O	4 bits of Port 0: 8-bit quasi-bidirectional I/O port
P1.0 to P1.2	33 to 35	I/O	3 bits of Port 1: 8-bit quasi-bidirectional I/O port
V_{SS}	36	P	ground
TONE	37	O	DTMF output
V_{DD}	38	P	positive supply voltage
P1.3 to P1.6	39 to 42	I/O	4 bits of Port 1: 8-bit quasi-bidirectional I/O port
P1.7/MDY	43	I/O	1 bit of Port 1: 8-bit quasi-bidirectional I/O port; or melody output
P2.0	44	I/O	1 bit of Port 2: 4-bit quasi-bidirectional I/O port

6 FREQUENCY GENERATOR

A versatile frequency generator section with built-in programmable clock divider is provided (see Fig.3). The clock divider allows the DTMF section to run either with the main clock frequency ($f_{DTMF} = f_{xtal}$) or with a third of it ($f_{DTMF} = \frac{1}{3} \times f_{xtal}$) depending on the state of the divider control bit DIV3 (see Table 5). The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available. Their frequencies are provided either in purely sinusoidal form on the TONE output or as a square wave on the port line P1.7/MDY. The latter is typically for ringer applications in telephone sets. If no frequency output is selected the TONE output is in 3-state mode.

6.1 Frequency generator derivative registers

6.1.1 High and Low Group Frequency Registers

Table 3 gives the addresses, symbols and access types of the High Group Frequency (HGF) and Low Group Frequency (LGF) registers, used to set the frequency output.

Table 3 Hexadecimal addresses, symbols, access types and bit symbols of the frequency registers

REGISTER ADDRESS	REGISTER SYMBOL	ACCESS TYPE	BIT SYMBOLS							
			7	6	5	4	3	2	1	0
11H	HGF	W	H7	H6	H5	H4	H3	H2	H1	H0
12H	LGF	W	L7	L6	L5	L4	L3	L2	L1	L0

6.1.2 Clock and Melody Control Register (MDYCON)

Table 4 Clock and Melody Control Register, MDYCON (address 13H; access type R/W)

7	6	5	4	3	2	1	0
0	0	0	0	0	EDCO	DIV3	EMO

Table 5 Description of MDYCON bits

BIT	SYMBOL	DESCRIPTION
7 to 3	–	These bits are set to a logic 0.
2	EDCO	Enable DTMF clock output. If bit EDCO = 0, then DP1.7/DCO is a general purpose derivative port line. If bit EDCO = 1, then DP1.7/DCO is the DTMF clock output. EDCO = 1 does not inhibit the port instructions for DP1.7/DCO. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by derivative port instructions. However, the port flip-flop of DP1.7/DCO must remain set to avoid conflicts between DTMF clock and port outputs.
1	DIV3	Enable DTMF clock divider. If bit DIV3 = 0, then the DTMF clock $f_{DTMF} = f_{xtal}$. If bit DIV3 = 1, then $f_{DTMF} = \frac{1}{3} \times f_{xtal}$.
0	EMO	Enable Melody Output. If bit EMO = 0, then P1.7/MDY is a standard port line. If bit EMO = 1, then P1.7/MDY is the melody output. EMO = 1 does not inhibit the port instructions for P1.7/MDY. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by port instructions. However, the port flip-flop of P1.7/MDY must remain set to avoid conflicts between melody and port outputs. When the HGF contents are zero while EMO = 1, P1.7/MDY is in the HIGH state.

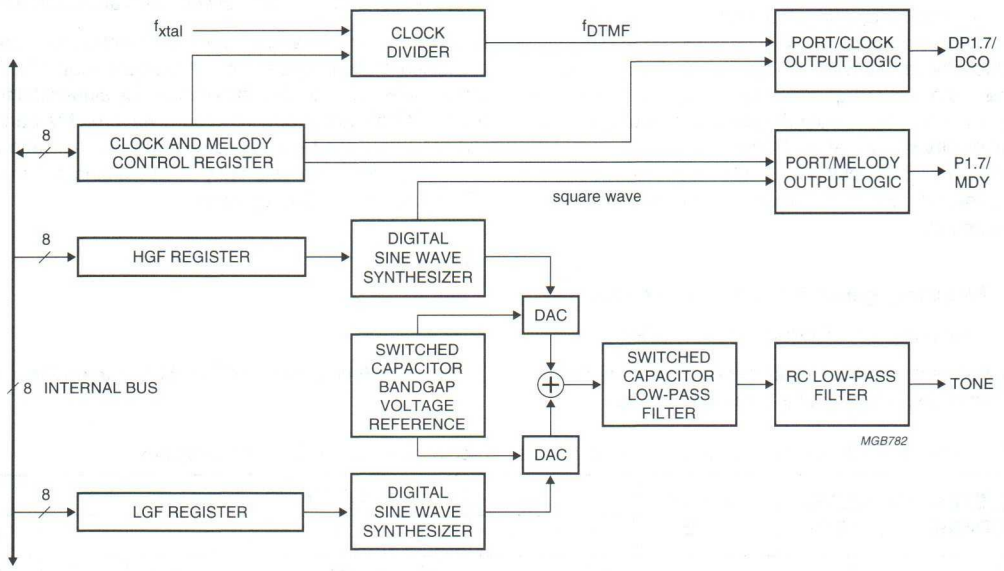


Fig.3 Block diagram of the frequency generator, melody output (P1.7/MDY) and DTMF clock output (DP1.7/DCO).

6.2 Melody output (P1.7/MDY)

The melody output (P1.7/MDY) is very useful for generating musical notes when a purely sinusoidal signal is not required, such as for ringer applications.

The square wave (duty cycle = $^{12}/_{23}$ or 52%) will include the attenuated harmonics of the base frequency, which is defined by the contents of the HGF register (Table 3). However, even higher frequency notes may be produced since the low-pass filtering on the TONE output is not applied to the P1.7/MDY output. This results in the minimum decimal value x in the HGF register (see equation in Section 6.4) being 2 for the P1.7/MDY output, rather than 60 for the TONE output. A sinusoidal TONE output is produced at the same time as the melody square wave, but due to the filtering, the higher frequency sine waves with x < 60 will not appear at the TONE output.

Since the melody output is shared with P1.7, the port flip-flop of P1.7 has to be set HIGH before using the melody output. This is to avoid conflicts between melody and port outputs. The melody output drive depends on the configuration of port P1.7/MDY, see Chapter 13, Table 24.

6.3 DTMF clock divider and output (DP1.7/DCO)

The DTMF clock divider allows the DTMF part to run either with the main clock frequency ($f_{DTMF} = f_{xtal}$) or with a third of it ($f_{DTMF} = {}^1/_3 \times f_{xtal}$) depending on the state of the divider control bit DIV3 in register MDYCON.

For low power applications, a 3.58 MHz quartz crystal or PXE resonator can be chosen together with the divide-by-one function of the clock divider.

For other applications a 10.74 MHz quartz crystal or PXE resonator may be chosen together with the divide-by-three function of the clock divider. This triples the program speed of the microcontroller, thereby keeping the assumed DTMF frequency of 3.58 MHz.

Since a 3.58 MHz clock is needed for peripheral telephony circuits such as the analog voice scrambler/descrambler PCD4440T, a switchable DTMF clock output is provided depending on the state of the enable clock output bit EDCO in register MDYCON.

If EDCO = 1 and DIV3 = 1 in the MDYCON register: a square wave with the frequency $f_{DTMF} = 1/3 \times f_{xtal}$ is output on the derivative port line DP1.7/DCO. If EDCO = 1 and DIV3 = 0: a square wave with the frequency $f_{DTMF} = f_{xtal}$ is output on the derivative port line DP1.7/DCO.

The melody output drive depends on the configuration of port P1.7/MDY, see Chapter 13, Table 24.

6.4 Frequency registers

The two frequency registers HGF and LGF define two frequencies. From these, the digital sine synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures tone output levels independent of supply voltage and temperature. The amplitude of the Low Group Frequency sine wave is attenuated by 2 dB compared to the amplitude of the High Group Frequency sine wave.

The two sine waves are summed and then filtered by an on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

The value 00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption.

The frequency 'f' of the sine wave generated from either of the frequency registers is a function of the clock frequency 'f_{xtal}' and the decimal value 'x' held in the register. The equation relating these variables is:

$$f = \frac{f_{xtal}}{[23\,(x+2)\,]}; \text{ where } 60 \leq x \leq 255.$$

The frequency limitation given by $x \geq 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

6.5 DTMF frequencies

Assuming an oscillator frequency f_{xtal} = 3.58 MHz, the DTMF standard frequencies can be implemented as shown in Table 6.

The relationship between telephone keyboard symbols, DTMF frequency pairs and the corresponding frequency register contents are given in Table 7.

Table 6 DTMF standard frequencies and their implementation; value = LGF, HGF contents

VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 7 Dialling symbols, corresponding DTMF frequency pairs and frequency register contents

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
•	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

6.6 Modem frequencies

Again assuming an oscillator frequency f_{xtal} = 3.58 MHz, the standard modem frequencies can be implemented as in Table 8. It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling Low Group Frequency generation.

Table 8 Standard modem frequencies and their implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980[1]	978.82	−0.12	−1.18
82	1180[1]	1179.03	−0.08	−0.97
8F	1070[2]	1073.33	0.31	3.33
79	1270[2]	1265.30	−0.37	−4.70
80	1200[3]	1197.17	−0.24	−2.83
45	2200[3]	2192.01	−0.36	−7.99
76	1300[4]	1296.94	−0.24	−3.06
48	2100[4]	2103.14	0.15	3.14
5C	1650[1]	1655.66	0.34	5.66
52	1850[1]	1852.77	0.15	2.77
4B	2025[2]	2021.20	−0.19	−3.80
44	2225[2]	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

6.7 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{xtal} = 3.58 MHz (Table 9). It is suggested to define the frequency by the HGF register while the LGF contains 00H, disabling Low Group Frequency generation.

Table 9 Musical scale frequencies and their implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD[1]	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 @ 440 Hz.

7 EEPROM AND TIMER 2 ORGANIZATION

The PCA3354C; PCD3354A have 256 bytes of Electrically Erasable Programmable Read Only Memory (EEPROM). Such non-volatile storage provides data retention without the need for battery backup. In telecom applications, the EEPROM is used for storing redial numbers and for short dialling of frequently used numbers. More generally, EEPROM may be used for customizing microcontrollers, such as to include a PIN code or a country code, to define trimming parameters, to select application features from the range stored in ROM.

The most significant difference between a RAM and an EEPROM is that a bit in EEPROM, once written to a logic 1, cannot be cleared by a subsequent write operation. Successive write accesses actually perform a logical OR with the previously stored information. Therefore, to clear a bit, the whole byte must be erased and re-written with the particular bit cleared. Thus, an erase-and-write operation is the EEPROM equivalent of a RAM write operation.

Whereas read access times to an EEPROM are comparable to RAM access times, write and erase accesses are much slower at 5 ms each. To make these operations more efficient, several provisions are available in the PCA3354C; PCD3354A.

First, the EEPROM array is structured into 64 four-byte pages (see Fig.4) permitting access to 4 bytes in parallel (write page, erase/write page and erase page). It is also possible to erase and write individual bytes.

Finally, the EEPROM address register provides auto-incrementing, allowing very efficient read and write accesses to sequential bytes.

To simplify the erase and write timing, the derivative 8-bit down-counter (Timer 2) with reload register is provided. In addition to EEPROM timing, Timer 2 can be used for general real-time tasks, such as for measuring signal duration and for defining pulse widths.

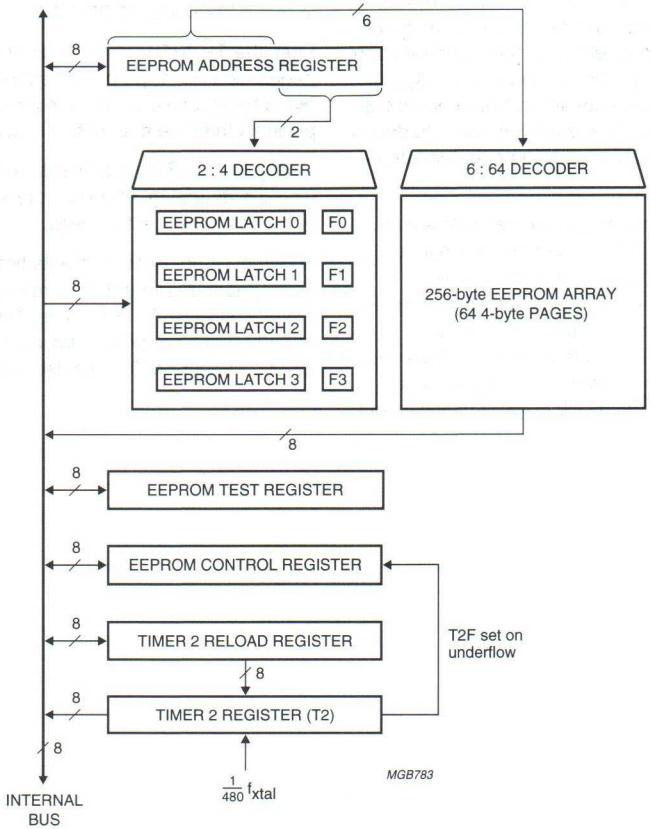


Fig.4 Block diagram of the EEPROM and Timer 2.

7.1 EEPROM registers

7.1.1 EEPROM Control Register (EPCR)

The behaviour of the EEPROM and Timer 2 section is defined by the EEPROM Control Register. See Tables 10, 11 and 12.

Table 10 EEPROM Control Register (address 04H, access type R/W)

7	6	5	4	3	2	1	0
STT2	ET2I	T2F	EWP	MC3	MC2	MC1	0

Table 11 Description of the EPCR bits

BIT	SYMBOL	DESCRIPTION
7	STT2	Start T2. If STT2 = 0, then Timer 2 is stopped; T2 value held. If STT2 = 1, then T2 decrements from reload value.
6	ET2I	Enable T2 interrupt. If ET2I = 0, then T2F event cannot request interrupt. If ET2I = 1, then T2F event can request interrupt.
5	T2F	Timer 2 flag. Set when T2 underflows (or by program); reset by program.
4	EWP	Erase or write in progress (EWP). Set by program (EWP starts EEPROM erase and/or write and Timer 2). Reset at the end of EEPROM erase and/or write.
3	MC3	Mode control 3 to 1. These three bits in conjunction with bit EWP select the mode as shown in Table 12.
2	MC2	
1	MC1	
0	–	This bit is set to a logic 0.

Table 12 Mode selection; X = don't care

EWP	MC3	MC2	MC1	DESCRIPTION
0	0	0	0	read byte
0	0	1	0	increment mode
1	0	1	X	write page
1	1	0	0	erase/write page
1	1	1	1	erase page
X	0	0	1	not allowed
X	1	0	1	
X	1	1	0	

7.1.2 EEPROM ADDRESS REGISTER (ADDR)

The EEPROM Address Register determines the EEPROM location to which an EEPROM access is directed.

As a whole, ADDR auto-increments after read and write cycles to EEPROM, but remains fixed after erase cycles. This behaviour generates the correct ADDR contents for sequential read accesses and for sequential write or erase/write accesses with intermediate page setup. Overflow of the 8-bit counter wraps around to zero.

Table 13 EEPROM Address Register (address 01H, access type R/W)

7	6	5	4	3	2	1	0
0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 14 Description of ADDR bits

BIT	SYMBOL	DESCRIPTION
7	–	This bit is set to a logic 0.
6 to 2	AD6 to AD2	AD2 to AD6 select one of 32 pages.
1 to 0	AD1 to AD0	AD1 and AD0 are irrelevant during erase and write cycles. For read accesses, AD0 and AD1 indicate the byte location within an EEPROM page. During page setup, finally, AD0 and AD1 select EEPROM Latch 0 to 3 whereas AD2 to AD6 are irrelevant. If increment mode (Table 12) is active during page setup, the subcounter consisting of AD0 and AD1 increments after every write to an EEPROM latch, thus enhancing access to sequential EEPROM latches. Incrementing stops when EEPROM Latch 3 is reached, i.e. when AD0 and AD1 are both a logic 1.

7.1.3 EEPROM DATA REGISTER (DATR)

Table 15 EEPROM Data Register (address 03H; access type R/W)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 16 Description of DATR bits

BIT	SYMBOL	DESCRIPTION
7 to 0	D7 to D0	The EEPROM Data Register (DATR) is only a conceptual entity. A read operation from DATR, reads out the EEPROM byte addressed by ADDR. On the other hand, a write operation to DATR, loads data into the EEPROM latch (see Fig.4) defined by bits AD0 and AD1 of ADDR.

7.1.4 EEPROM TEST REGISTER (TST)

The EEPROM Test register is used for testing purposes during device manufacture. It must not be accessed by the device user.

7.2 EEPROM latches

The four EEPROM latches (EEPROM Latch 0 to 3; Fig.4) cannot be read by user software. Due to their construction, the latches can only be preset, but not cleared. Successive write operations through DATR to the EEPROM latches actually perform a logical OR with the previously stored data in EEPROM. The EEPROM latches are reset at the conclusion of any EEPROM cycle.

7.3 EEPROM flags

The four EEPROM flags (F0 to F3; Fig.4) cannot be directly accessed by user software. An EEPROM flag is set as a side-effect when the corresponding EEPROM latch is written through DATR. The EEPROM flags are reset at the conclusion of any EEPROM cycle.

7.4 EEPROM macros

The instruction sequence used in an EEPROM access should be treated as an indivisible entity. Erroneous programs result if ADDR, DATR, RELR or EPCR are inadvertently changed during an EEPROM cycle or its setup. Special care should be taken if the program may asynchronously divert due to an interrupt. A new access to the EEPROM may only be initiated when no write, erase or erase/write cycles are in progress. This can be verified by reading bit EWP (register EPCR).

For write, erase and erase/write cycles, it is assumed that the Timer 2 Reload Register (RELR) has been loaded with the appropriate value for a 5 ms delay, which depends on f_{xtal} (see Table 23). The end of a write, erase or erase/write cycle will be signalled by a cleared EWP and by a Timer 2 interrupt provided that ET2I = 1 and that the derivative interrupt is enabled.

7.5 EEPROM access

One read, one write, one erase/write and one erase access are defined by bits EWP and MC1 to MC3 in the EPCR register; see Table 10.

Read byte retrieves the EEPROM byte addressed by ADDR when DATR is read. Read cycles are instantaneous.

Write and erase cycles take 5 ms, however. Erase/write is a combination of an erase and a subsequent write cycle, consequently taking 10 ms.

As their names imply, **write page, erase page and erase/write page** are applied to a whole EEPROM page. Therefore, bits AD0 and AD1 of register ADDR (see Table 13), defining the byte location within an EEPROM page, are irrelevant during write and erase cycles. However, write and erase cycles need not affect all bytes of the page. The EEPROM flags F0 to F3 (see Fig.4) determine which bytes within the EEPROM page are affected by the erase and/or write cycles. A byte whose corresponding EEPROM flag is zero remains unchanged.

With erase page, a byte is erased if its corresponding EEPROM flag is set. With write page, data in EEPROM latches 0 to 3 (Fig.4) are ORed to the individual page bytes if and only if the corresponding EEPROM flags are set.

In an erase/write cycle, F0 to F3 select which page bytes are erased and ORed with the corresponding EEPROM latches.

ORing, in this event, means that the EEPROM latches are copied to the selected page bytes.

The described page-wise organization of erase and write cycles allows up to four bytes to be individually erased or written within 5 ms. This advantage necessitates a preparation step, called **page setup**, before the actual erase and/or write cycle can be executed.

Page setup controls EEPROM latches and EEPROM flags. This will be described in the Sections 7.5.1 to 7.5.5.

7.5.1 PAGE SETUP

Page setup is a preparation step required before write page, erase page and erase/write page cycles.
As previously described, these page operations include single-byte write, erase and erase/write as a special event. EEPROM flags F0 to F3 determine which page bytes will be affected by the mentioned page operations. EEPROM Latch 0 to 3 must be preset through DATR to specify the write cycle data to EEPROM and to set the EEPROM flags as a side-effect.

Obviously, the actual preset value of the EEPROM latches is irrelevant for erase page. Preset of one, two, three or all four EEPROM latches and the corresponding EEPROM flags can be performed by repeatedly defining ADDR and writing to DATR (see Table 17).

If more than one EEPROM latch must be preset, the subcounter consisting of AD0 and AD1 can be induced to auto-increment after every write to DATR, thus stepping through all EEPROM latches. For this purpose, increment mode (Table 12) must be selected. Auto-incrementing stops at EEPROM Latch 3. It is not mandatory to start at EEPROM Latch 0 as in shown in Table 18.

Note that AD2 to AD6 are irrelevant during page setup. They will usually specify the intended EEPROM page, anticipating the subsequent page cycle.

From now on, it will be assumed that AD2 to AD6 will contain the intended EEPROM page address after page setup.

Table 17 Page setup; preset

INSTRUCTION	RESULT
MOV A, #addr	address of EEPROM latch
MOV ADDR, A	send address to ADDR
MOV A, #data	load write, erase/write or erase data
MOV DATR, A	send data to addressed EEPROM latch

Table 18 Page setup; auto-incrementing

INSTRUCTION	RESULT
MOV A, #MC2	increment mode control word
MOV EPCR, A	select increment mode
MOV A, #baddr	EEPROM Latch 0 address (AD0 = AD1 = 0)
MOV ADDR, A	send EEPROM Latch 0 address to ADDR
MOV A, R0	load 1st byte from Register 0
MOV DATR, A	send 1st byte to EEPROM Latch 0
MOV A, R1	load 2nd byte from Register 1
MOV DATR, A	send 2nd byte to EEPROM Latch 1
MOV A, R2	load 3rd byte from Register 2
MOV DATR, A	send 3rd byte to EEPROM Latch 2
MOV A, R3	load 4th byte from Register 3
MOV DATR, A	send 4th byte to EEPROM Latch 3

7.5.2 READ BYTE

Since ADDR auto-increments after a read cycle regardless of the page boundary, successive bytes can efficiently be read by repeating the last instruction.

Table 19 Read byte

INSTRUCTION	RESULT
MOV A, #RDADDR	load read address
MOV ADDR, A	send address to ADDR
MOV A, DATR	read EEPROM data

7.5.3 WRITE PAGE

The write cycle performs a logical OR between the data in the EEPROM latches and that in the addressed EEPROM page. To actually copy the data from the EEPROM latches, the corresponding bytes in the page should previously have been erased.

The EEPROM latches are preset as described in Section 7.5.1. The actual transfer to the EEPROM is then performed as shown in Table 20.

The last instruction also starts Timer 2. The data in the EEPROM latches are ORed with that in the corresponding page bytes within 5 ms. A single-byte write is simply a special case of 'write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by bits AD2 to AD6) and to EEPROM Latch 0 (by bits AD0 and AD1). This allows efficient coding of multi-page write operations.

Table 20 Write page

INSTRUCTION	RESULT
MOV A, #EWP + MC2	'write page' control word
MOV EPCR, A	start 'write page' cycle

7.5.4 ERASE/WRITE PAGE

The EEPROM latches are preset as described in Section 7.5.1. The page byte corresponding to the asserted flags (among F0 to F3) are erased and re-written with the contents of the respective EEPROM latches.

The last instruction also starts Timer 2. Erasure takes 5 ms upon which Timer Register T2 reloads for another 5 ms cycle for writing. The top cycles together take 10 ms. A single-byte erase/write is simply a special event of 'erase/write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by AD2 to AD6) and to EEPROM Latch 0 (by AD0 and AD1). This allows efficient coding of multi-page erase/write operations.

Table 21 Erase/write page

INSTRUCTION	RESULT
MOV A, #EWP + MC3	'erase/write page' control word
MOV EPCR, A	start 'erase/write page' cycle

7.5.5 ERASE PAGE

The EEPROM flags are set as described in Section 7.5.1. The corresponding page bytes are erased.

The last instruction also starts Timer 2. Erasure takes 5 ms. A single-byte erase is simply a special case of 'erase page'.

Note that ADDR does not auto-increment after an erase cycle.

Table 22 Erase page

INSTRUCTION	RESULT
MOV A, #EWP + MC3 + MC2 + MC1	'erase page' control word
MOV EPCR, A	start 'erase page' cycle

7.6 Timer 2

Timer 2 is a 8-bit down-counter decremented at a rate of $1/480 \times f_{xtal}$. It may be used either for EEPROM timing or as a general purpose timer. Conflicts between the two applications should be carefully avoided.

7.6.1 TIMER 2 FOR EEPROM TIMING

When used for EEPROM timing, Timer 2 serves to generate the 5 ms intervals needed for erasing or writing the EEPROM. At the decrement rate of $1/480 \times f_{xtal}$, the reload value for a 5 ms interval is a function of f_{xtal}. Table 23 summarizes the required reload values for a number of oscillator frequencies.

Timer 2 is started by setting bit EWP in the EPCR. The Timer Register T2 is loaded with the reload value from RELR. T2 decrements to zero.

For an erase/write cycle, underflow of T2 indicates the end of the erase operation. Therefore, Timer Register T2 is reloaded from RELR for another 5 ms interval during which the flagged EEPROM latches are copied to the corresponding bytes in the page addressed by ADDR.

The second underflow of an erase/write cycle and the first underflow of write page and erase page conclude the corresponding EEPROM cycle. Timer 2 is stopped, T2F is set whereas EWP and MC1 to MC3 are cleared.

Table 23 Reload values as a function of f_{xtal}

f_{xtal} (MHz)	RELOAD VALUE[1] (HEX)
1	0A
2	14
3.58	25
6	3E
10.74	6F
16	A6

Note

1. The reload value is $(5 \times 10^{-3} \times 1/480 \times f_{xtal}) - 1$; f_{xtal} in MHz.

7.6.2 TIMER 2 AS A GENERAL PURPOSE TIMER

When used for purposes other than EEPROM timing, Timer 2 is started by setting STT2. The Timer 2 Register T2 (see Table 25) is loaded with the reload value from RELR. T2 decrements to zero. On underflow, T2 is reloaded from RELR, T2F is set and T2 continues to decrement.

Timer 2 can be stopped at any time by clearing STT2. The value of T2 is then held and can be read out. After setting STT2 again, Timer 2 decrements from the reload value. Alternatively, it is possible to read T2 'on the fly' i.e. while Timer 2 is operating.

8 DERIVATIVE INTERRUPTS

One derivative interrupt event is defined. It is controlled by bits T2F and ET2I in the EPCR (see Tables 10 and 11).

The derivative interrupt event occurs when T2F is set. This request is honoured under the following circumstances:

- No interrupt routine proceeds
- No external interrupt request is pending
- The derivative interrupt is enabled
- ET2I is set.

The derivative interrupt routine must include instructions that will remove the cause of the derivative interrupt by explicitly clearing T2F. If the derivative interrupt is not used, T2F may directly be tested by the program. Obviously, T2F can also be asserted under program control, e.g. to generate a software interrupt.

9 TIMING

Although the PCA3354C; PCD3354A operate over a clock frequency range from 1 MHz to 16 MHz, f_{xtal} = 3.58 MHz or 10.74 MHz will usually be chosen to take full advantage of the frequency generator section.

10 RESET

In addition to the conditions given in the *"PCD33xxA Family"* data sheet, all derivative registers are cleared in the reset state.

11 IDLE MODE

In Idle mode, the frequency generator, the EEPROM and the Timer 2 sections remain operative. Therefore, the IDLE instruction may be executed while an erase and/or write access to EEPROM is in progress.

12 STOP MODE

Since the oscillator is switched off, the frequency generator, the EEPROM and the Timer 2 sections receive no clock. It is suggested to clear both the HGF and the LGF registers before entering stop mode. This will cut off the biasing of the internal amplifiers, considerably reducing current requirements.

The Stop mode **must not** be entered while an erase and/or write access to EEPROM is in progress. The STOP instruction may only be executed when EWP in EPCR is zero. The Timer 2 section is frozen during Stop mode. After exit from Stop mode by a HIGH level on CE/$\overline{T0}$, Timer 2 proceeds from the held state.

13 SUMMARY OF I/O PORTS AND MASK OPTIONS

All standard quasi-bidirectional I/O ports are available; see *"PCD33xxA Family"* data sheet.

- Port 0: 8 parallel port lines P0.0 to P0.7
- Port 1: 8 parallel port lines P1.0 to P1.7
- Port 2: 4 parallel port lines P2.0 to P2.3.

In addition to the standard ports, 2 derivative I/O ports are available:

- Derivative Port 0: 8 parallel port lines DP0.0 to DP0.7 (register DP0L)
- Derivative Port 1: 8 parallel port lines DP1.0 to DP1.7 (register DP1L).

The port options and the other ROM mask options are listed in Table 24. See Table 25 for the addresses of DP0L and DP1L.

Table 24 ROM mask options

FUNCTION IMPLEMENTED IN ROM	OPTION		
Program/data	Any mix of instructions and data up to ROM size of 8 kbytes.		
Port Output			
P0.0 to P0.7	standard	open-drain	push-pull
P1.0 to P1.6	standard	open-drain	push-pull
P1.7/MDY; note 1	standard	open-drain	push-pull
P2.0 to P2.3	standard	open-drain	push-pull
DP0.0 to DP0.7	standard	open-drain	push-pull
DP1.0 to DP1.6	standard	open-drain	push-pull
DP1.7/DCO; note 2	standard	open-drain	push-pull
Port State after reset			
P0.0 to P0.7	set	reset	–
P1.0 to P1.6	set	reset	–
P1.7/MDY	set	reset	–
P2.0 to P2.3	set	reset	–
DP0.0 to DP0.7	set	reset	–
DP1.0 to DP1.6	set	reset	–
DP1.7/DCO	set	reset	–
Oscillator			
Transconductance	LOW (g_{mL})	MEDIUM (g_{mM})	HIGH (g_{mH})
Power-on-reset			
Power-on-reset voltage level: V_{POR}	1.2 to 3.6 V in increments of 100 mV; OFF		

Notes

1. If standard (Option 1) or push-pull (Option 3) output is chosen, the P1.7/MDY output becomes a push-pull output. If open-drain (Option 2) is chosen the P1.7/MDY output becomes an open-drain output.
2. If standard (Option 1) or push-pull (Option 3) output is chosen, the DP1.7/DCO output becomes a push-pull output. If open-drain (Option 2) is chosen the DP1.7/DCO output becomes an open-drain output.

14 SUMMARY OF DERIVATIVE REGISTERS

Table 25 Register map

ADDR. (HEX)	REGISTER	7	6	5	4	3	2	1	0	R/W
00	not used									
01	EEPROM Address Register (ADDR)	0	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/W
02	not used									
03	EEPROM Data Register (DATR)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
04	EEPROM Control Register (EPCR)	STT2	ET21	TF2	EWP	MC3	MC2	MC1	0	R/W
05	Timer 2 Reload Register (RELR)	R7	R6	R5	R4	R3	R2	R1	R0	R/W
06	Timer 2 Register (T2)	T2.7	T2.6	T2.5	T2.4	T2.3	T2.2	T2.1	T2.0	R
07	Test Register (TST)	only for test purposes; not to be accessed by the device user								
08 to 10	not used									
11	High Group Frequency Register (HGF)	H7	H6	H5	H4	H3	H2	H1	H0	W
12	Low Group Frequency Register (LGF)	L7	L6	L5	L4	L3	L2	L1	L0	W
13	Clock and Melody Control Register (MDYCON)	0	0	0	0	0	DCO	DIV3	EMO	R/W
14 to 2F	not used									
30	Derivative Port 0 lines (DP0L)	D0.7	D0.6	D0.5	D0.4	D0.3	D0.2	D0.1	D0.0	R
31	Derivative Port 1 lines (DP1L)	D1.7	D1.6	D1.5	D1.4	D1.3	D1.2	D1.1	D1.0	R
32	Derivative Port 0 flip-flop (DP0FF)	F0.7	F0.6	F0.5	F0.4	F0.3	F0.2	F0.1	F0.0	R/W
33	Derivative Port 1 flip-flop (DP1FF)	F1.7	F1.6	F1.5	F1.4	F1.3	F1.2	F1.1	F1.0	R/W
34 to FF	not used									

15 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+7.0	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	−	125	mW
P_O	power dissipation per output	−	30	mW
I_{SS}	ground supply current	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	−	90	°C

16 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Data Handbook IC14, Section: Handling MOS devices"*).

17 DC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = 0 to +50 °C (PCA3354C) or −25 to +70 °C (PCD3354A); all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz (g_{mL}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	see Fig.5				
	operating	note 1	1.8	–	6	V
	RAM data retention in Stop mode		1.0	–	6	V
I_{DD}	operating supply current	see Figs 6 and 7; note 2				
		V_{DD} = 3 V; value HGF or LGF ≠ 0	–	0.8	1.6	mA
		V_{DD} = 3 V; value HGF = LGF = 0	–	0.35	0.7	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF or LGF ≠ 0; DIV3 = 1	–	2.7	6.2	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF = LGF = 0	–	1.7	4.2	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH}); value HGF = LGF = 0	–	3.5	–	mA
$I_{DD(idle)}$	supply current (Idle mode)	see Figs 8 and 9; note 2				
		V_{DD} = 3 V; value HGF or LGF ≠ 0	–	0.7	1.4	mA
		V_{DD} = 3 V; value HGF = LGF =0	–	0.25	0.5	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF or LGF ≠ 0; DIV3 = 1	–	2.3	5.5	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF = LGF = 0	–	1.3	3.5	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH}); value HGF = LGF = 0	–	2.4	–	mA
$I_{DD(stp)}$	supply current (Stop mode)	See Fig.10; notes 2 and 3				
		V_{DD} = 1.8 V; T_{amb} = 25 °C	–	1.0	5.5	µA
		V_{DD} = 1.8 V; T_{amb} = −25 to +70 °C	–	–	10	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	−1	–	+1	µA
Port outputs						
I_{OL}	LOW level output sink current	V_{DD} = 3 V; V_O = 0.4 V; see Fig.11	0.7	3.5	–	mA
I_{OH}	HIGH level pull-up output source current	V_{DD} = 3 V; V_O = 2.7 V; see Fig.12	−10	−30	–	µA
		V_{DD} = 3 V; V_O = 0 V; see Fig.12	–	−140	−300	µA
I_{OH1}	HIGH level push-pull output source current	V_{DD} = 3 V; V_O = 2.6 V; see Fig.13	−0.7	−3.5	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TONE output (see Fig.14; notes 1 and 4)						
$V_{HG(RMS)}$	HGF voltage (RMS values)		158	181	205	mV
$V_{LG(RMS)}$	LGF voltage (RMS values)		125	142	160	mV
$\Delta f/f$	frequency deviation		−0.6	–	0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_O \rvert$	output impedance		–	100	500	Ω
G_v	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	T_{amb} = 25 °C; note 5	–	−25	–	dB
EEPROM (notes 1 and 6)						
n_{cyc}	endurance (erase/write cycles)	note 7	10^5	–	–	
t_{ret}	data retention		10	–	–	years
Power-on-reset (see Fig.15)						
ΔV_{POR}	Power-on-reset level variation around chosen V_{POR}	note 8; for PCD3354A	−0.5	0	+0.5	V
V_{POR}	Power-on-reset level	note 9; for PCA3354C	1.7	2.0	2.3	V
Oscillator (see Fig.16)						
g_{mL}	LOW transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
g_{mM}	MEDIUM transconductance	V_{DD} = 5 V	0.9	1.6	3.2	mS
g_{mH}	HIGH transconductance	V_{DD} = 5 V	3	4.5	9.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

Notes to the DC characteristics

1. TONE output; EEPROM erase and write require $V_{DD} \geq 2.5$ V:
   a) TONE output requires $f_{xtal} < 4$ MHz in case DIV3 = 0.
   b) TONE output requires $f_{xtal} < 12$ MHz in case DIV3 = 1.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open:
   a) Maximum values: external clock at XTAL1 and XTAL2 open-circuit.
   b) Typical values: T_{amb} = 25 °C; crystal connected between XTAL1 and XTAL2.
3. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; RESET, T1 and CE/$\overline{T0}$ at V_{SS}; crystal connected between XTAL1 and XTAL2; open-drain outputs connected to V_{SS}; all other outputs open.
4. Values are specified for DTMF frequencies only (CEPT).
5. Related to the Low Group Frequency (LGF) component (CEPT).
6. After final testing the value of each EEPROM bit is typically logic 1.
7. Verified on sampling basis.
8. V_{POR} is an option chosen by the user. Depending on its value, it may restrict the supply voltage range.
9. Each device is tested on the condition: $V_{DD(min)} < V_{POR}$; to ensure a correct start-up, even for slow rising supply voltages.

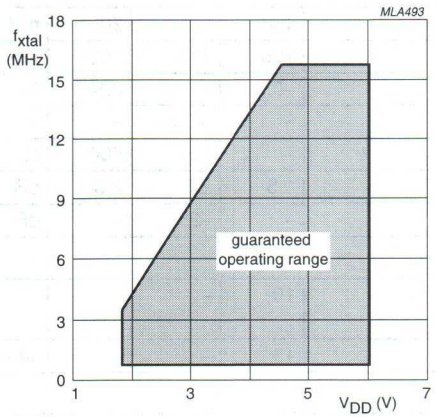
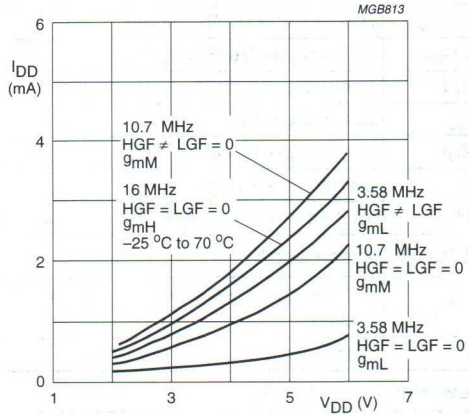
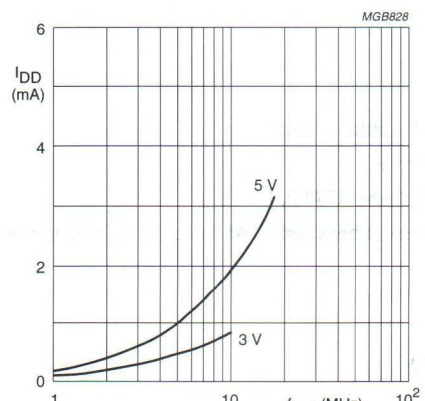


Fig.5 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).



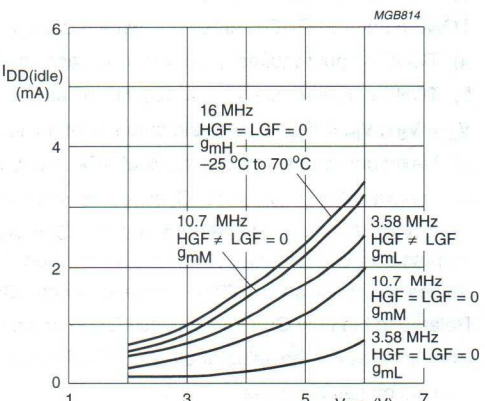
Measured with crystal between XTAL1 and XTAL2.

Fig.6 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).



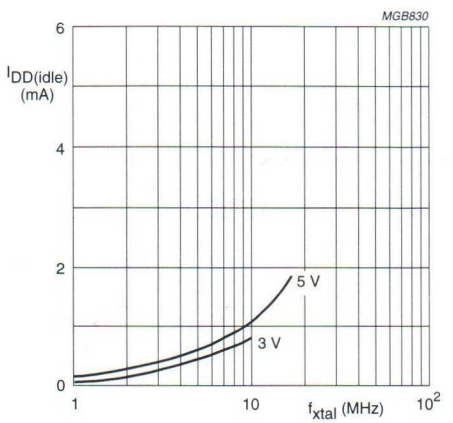
Measured with function generator on XTAL1.

Fig.7 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



Measured with crystal between XTAL1 and XTAL2.

Fig.8 Typical supply current in Idle mode ($I_{DD(idle)}$) as a function of supply voltage (V_{DD}).



Measured with function generator on XTAL1.

Fig.9 Typical supply current in Idle mode ($I_{DD(idle)}$) as a function of clock frequency (f_{xtal}).

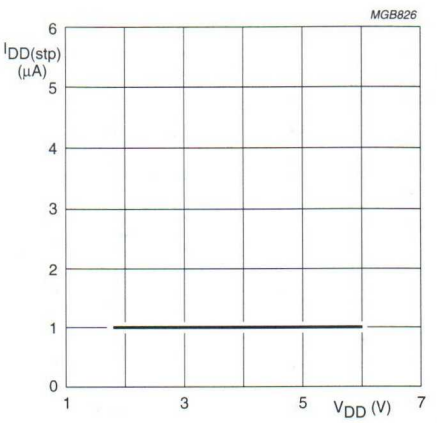
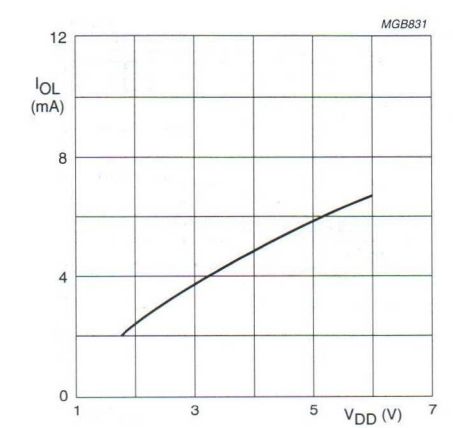


Fig.10 Typical supply current in Stop mode ($I_{DD(stp)}$) as a function of supply voltage (V_{DD}).



V_O = 0.4 V.

Fig.11 Typical LOW level output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

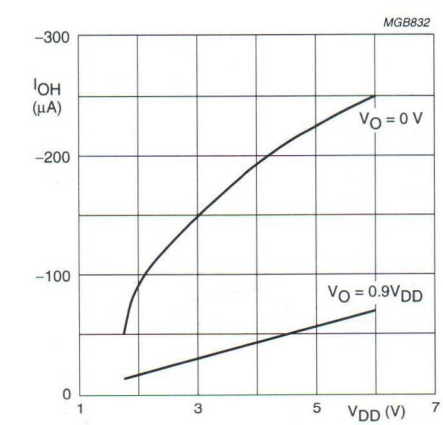
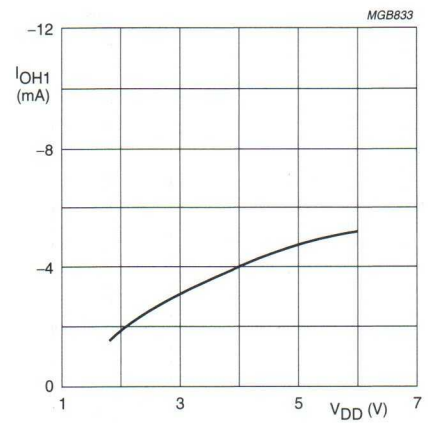
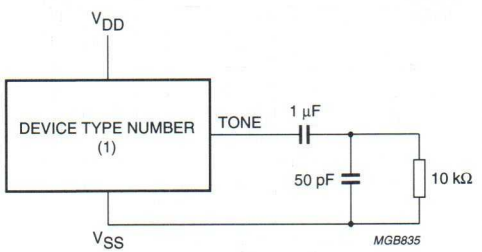


Fig.12 Typical HIGH level pull-up output source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.13 Typical HIGH level push-pull output source current (I_{OH1}) as a function of supply voltage (V_{DD}).



(1) Device type number: PCA3354C or PCD3354A.

Fig.14 TONE output test circuit.

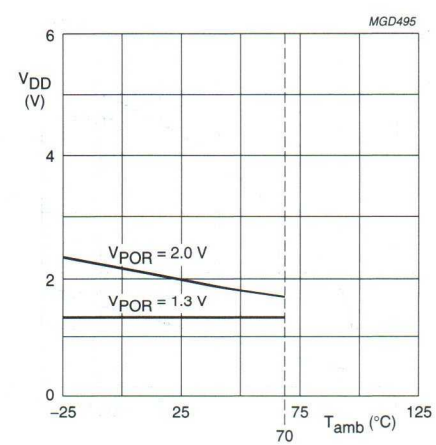


Fig.15 Typical Power-on-reset level (V_{POR}) as function of ambient temperature (T_{amb}).

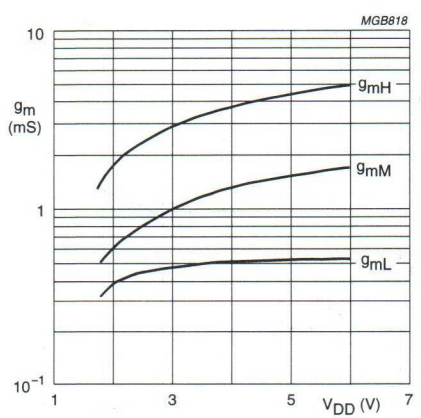


Fig.16 Typical transconductance (g_m) as a function of supply voltage (V_{DD}).

18 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = 0 to +50 °C (PCA3354C) or −25 to +70 °C (PCD3354A); all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.5	1	–	16	MHz

8-bit microcontroller with DTMF generator and 128 bytes EEPROM

PCD3359A

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8-bit microcontroller with DTMF generator and 128 bytes EEPROM

PCD3359A

1 FEATURES

- 8-bit CPU, ROM, RAM, EEPROM and I/O; in a single 28-lead or 32-lead package
- 2-kbyte ROM
- 64-byte RAM
- 128-byte EEPROM
- OTP version available
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- 8-bit reloadable Timer 2
- Three single-level vectored interrupts:
  - external
  - 8-bit programmable Timer/event counter 1
  - derivative; triggered by reloadable Timer 2
- Wake-up via external or Port 0 interrupt
- Two test inputs, one of which also serves as the external interrupt input
- DTMF, modem, musical tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT compatible)
- Melody output for ringer application
- Power-on-reset
- Stop and Idle modes
- Supply voltage: 1.8 to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- Clock frequency: 1 to 16 MHz (3.58 MHz for DTMF suggested)
- Operating temperature: –25 to +70 °C
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

This data sheet details the specific properties of the PCD3359A. The shared properties of the PCD33xxA family of microcontrollers are described in the *"PCD33xxA family"* data sheet, which should be read in conjunction with this publication.

The PCD3359A is a low voltage microcontroller oriented towards telephony applications. It includes an on-chip generator for dual tone multifrequency (DTMF) generator, modem and musical tones. In addition to dialling, generated frequencies can be made available as square waves (P1.7/MDY) for melody generation, providing ringer operation (in which case the TONE output is disabled). A wake-up function via Port 0 interrupt facilitates keyboard interfacing. The PCD3359A can be emulated with the OTP microcontroller PCD3756A.

The device also incorporates 128 bytes of Electrically Erasable Programmable Read-Only Memory (EEPROM). The EEPROM can be used for storing telephone numbers, particularly for implementing redial functions.

The instruction set is similar to that of the MAB8048 and is a sub-set of that listed in the *"PCD33xxA family"* data sheet.

3 ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3359AP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3359AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCD3359AH	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

Note

1. Please refer to the Order Entry Form (OEF) for this device for the full type number to use when ordering. This type number will also specify the required program and the ROM mask options.

4 BLOCK DIAGRAM

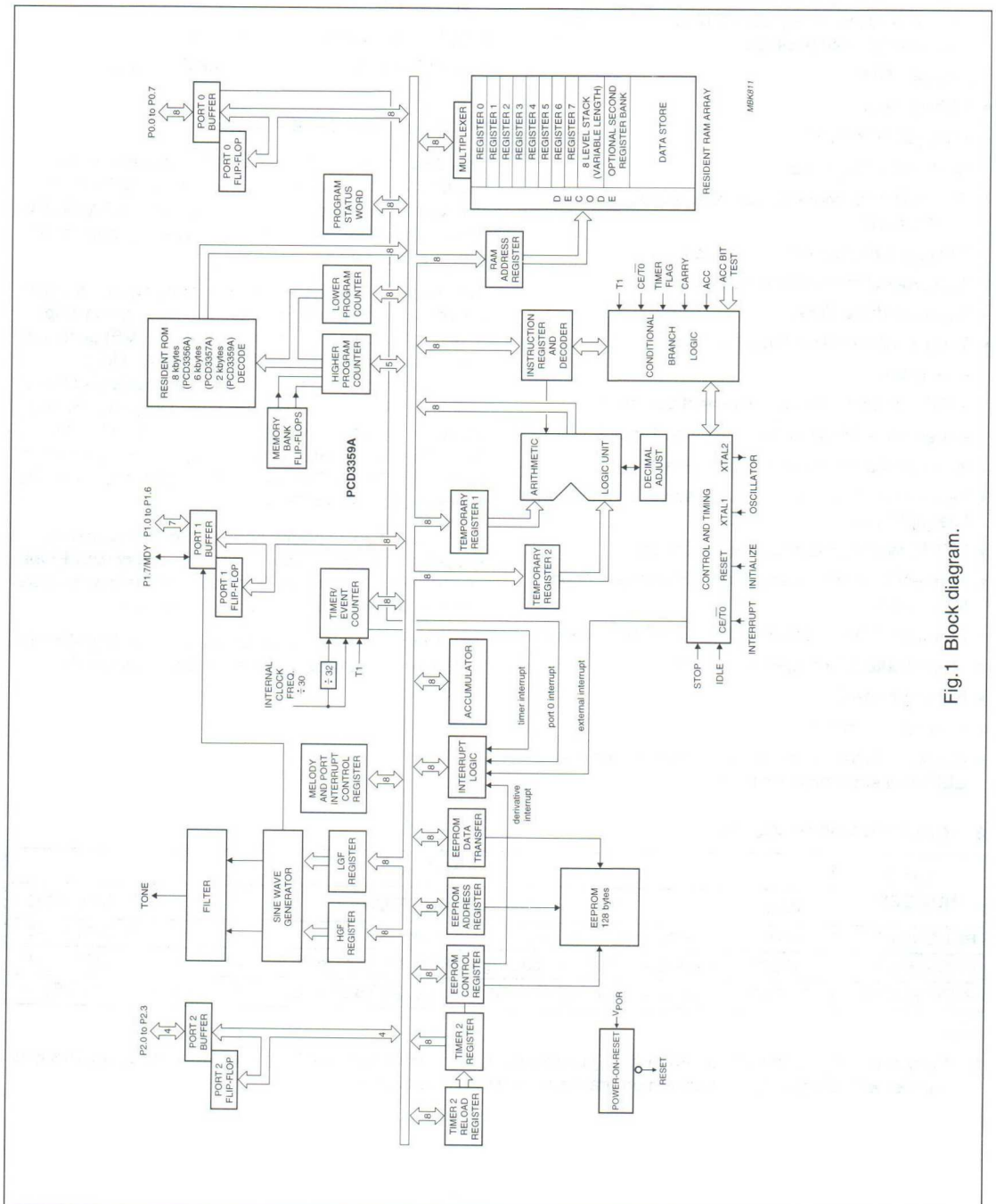


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

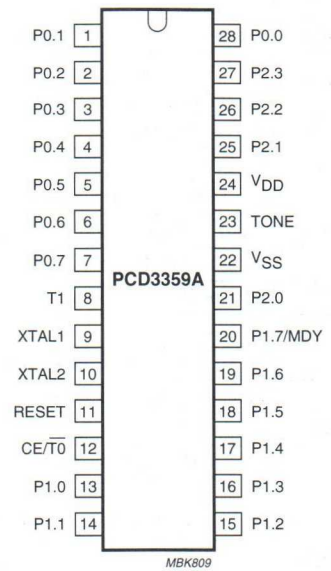


Fig.2 Pin configuration (SOT117-1 and SOT136-1).

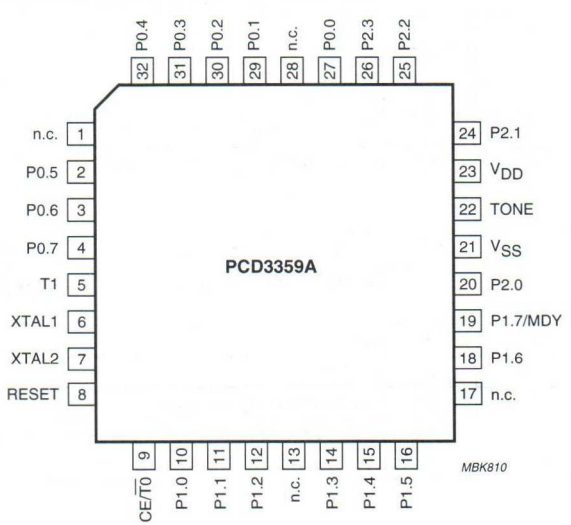


Fig.3 Pin configuration (SOT358-1).

5.2 Pin descriptions

Table 1 SOT117-1 and SOT136-1 packages (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	TYPE	DESCRIPTION
P0.1 to P0.7	1 to 7	I/O	7 bits of Port 0: 8-bit quasi-bidirectional I/O port; or wake-up interrupts
T1	8	I	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	9	I	crystal oscillator or external clock input
XTAL2	10	O	crystal oscillator output
RESET	11	I	reset input
CE/$\overline{T0}$	12	I	Chip Enable or Test 0
P1.0 to P1.6	13 to 19	I/O	7 bits of Port 1: 8-bit quasi-bidirectional I/O port
P1.7/MDY	20	I/O	1 bit of Port 1: 8-bit quasi-bidirectional I/O port; or melody output
P2.0	21	I/O	1 bit of Port 2: 4-bit quasi-bidirectional I/O port
V_{SS}	22	P	ground
TONE	23	O	DTMF, modem, musical tone output
V_{DD}	24	P	positive supply voltage
P2.1 to P2.3	25 to 27	I/O	3 bits of Port 2: 4-bit quasi-bidirectional I/O port
P0.0	28	I/O	1 bit of Port 0: 8-bit quasi-bidirectional I/O port; or wake-up interrupts

Table 2 SOT358-1 package (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	TYPE	DESCRIPTION
n.c.	1, 13, 17, 28	–	not connected
P0.5 to P0.7	2 to 4	I/O	3 bits of Port 0: 8-bit quasi-bidirectional I/O port; or wake-up interrupts
T1	5	I	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	6	I	crystal oscillator or external clock input
XTAL2	7	O	crystal oscillator output
RESET	8	I	reset input
CE/$\overline{T0}$	9	I	Chip Enable or Test 0
P1.0 to P1.6	10 to 12 14 to 16 18	I/O	7 bits of Port 1: 8-bit quasi-bidirectional I/O port
P1.7/MDY	19	I/O	1 bit of Port 1: 8-bit quasi-bidirectional I/O port; or melody output
P2.0 to P2.3	20, 24 to 26	I/O	4 bits of Port 2: 4-bit quasi-bidirectional I/O port
V_{SS}	21	P	ground
TONE	22	O	DTMF output
V_{DD}	23	P	positive supply voltage
P0.0 to P0.4	27, 29 to 32	I/O	5 bits of Port 0: 8-bit quasi-bidirectional I/O port; or wake-up interrupts

6 FREQUENCY GENERATOR

A versatile frequency generator section is provided (see Fig.4). For normal operation, use a 3.58 MHz quartz crystal or PXE resonator. The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets.Their frequencies are provided in purely sinusoidal form on the TONE output or as square waves on the P1.7/MDY output.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available.

In case no tones are generated, or the melody function is used, the TONE output is in 3-state mode.

6.1 Frequency generator derivative registers

6.1.1 High and Low Group Frequency Registers

Table 3 gives the addresses, symbols and access types of the High Group Frequency (HGF) and Low Group Frequency (LGF) Registers.

Table 3 Hexadecimal addresses, symbols, access types and bit symbols of the frequency registers

REGISTER ADDRESS	REGISTER SYMBOL	ACCESS TYPE	BIT SYMBOLS							
			7	6	5	4	3	2	1	0
11H	HGF	W	H7	H6	H5	H4	H3	H2	H1	H0
12H	LGF	W	L7	L6	L5	L4	L3	L2	L1	L0

6.1.2 Melody and Port Interrupt Control Register (MDYCON)

The Melody and Port Interrupt Control Register has two functions: bit 0 defines the behaviour of the melody output; bits 4 to 7 individually enable/disable specific pairs of Port 0 interrupts. MDYCON is a R/W register.

Table 4 Melody and Port Interrupt Control Register (address 13H)

7	6	5	4	3	2	1	0
EPI3	EPI2	EPI1	EPI0	0	0	0	EMO

Table 5 Description of MDYCON bits

BIT	SYMBOL	DESCRIPTION
7 to 4	EPI3 to EPI0	**Enable Port 0 interrupts.** Bits 7 to 4 individually enable/disable specific pairs of Port 0 interrupts; see Table 6 and Section 8.2 for details.
3 to 1	–	These bits are set to a logic 0.
0	EMO	**Enable Melody Output.** If bit EMO = 0, then P1.7/MDY is a standard port line and the TONE output is enabled. If bit EMO = 1, then P1.7/MDY is the melody output and the TONE output is disabled (3-state). EMO = 1 does not inhibit the port instructions for P1.7/MDY. Therefore, the state of both port line and flip-flop may be read in and the port flip-flop may be written by port instructions. However, the port flip-flop of P1.7/MDY must remain set to avoid conflicts between melody and port outputs. When the HGF contents are zero while EMO = 1, P1.7/MDY is in the logic HIGH state.

Table 6 Port 0 Interrupts control bits

BIT	STATE	INTERRUPTS			
		P0.0 AND P0.1	P0.2 AND P0.3	P0.4 AND P0.5	P0.6 AND P0.7
EPI0	1	enabled	–	–	–
	0	disabled	–	–	–
EPI0	1	–	enabled	–	–
	0	–	disabled	–	–
EPI0	1	–	–	enabled	–
	0	–	–	disabled	–
EPI0	1	–	–	–	enabled
	0	–	–	–	disabled

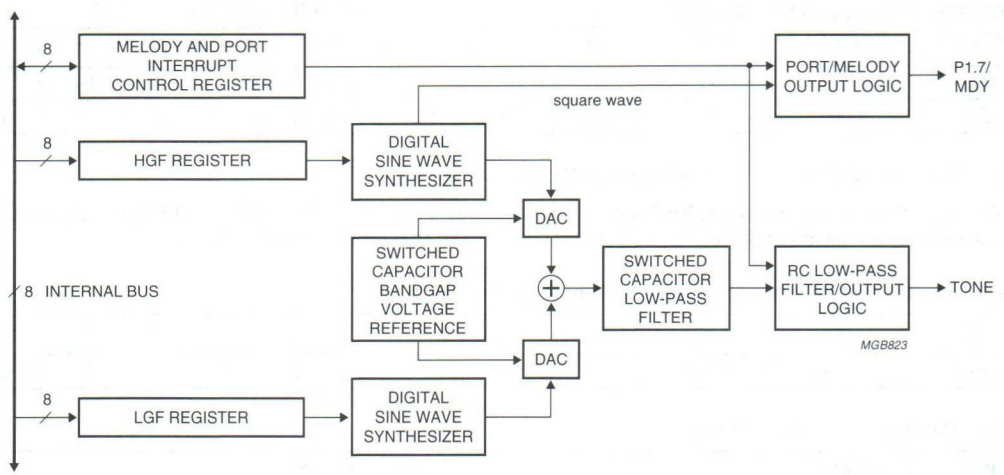


Fig.4 Block diagram of the frequency generator and melody output (P1.7/MDY) section.

6.2 Melody output (P1.7/MDY)

The melody output (P1.7/MDY) is very useful for generating musical notes when a purely sinusoidal signal is not required, such as for ringer applications.

If bit EMO = 1 in the Melody and Port Interrupt Control Register the TONE output is disabled (3-state) and a square wave with the frequency defined by the HGF contents is output on line P1.7/MDY. The square wave (duty cycle = $^{12}/_{23}$ or 52%) will include the attenuated harmonics of the base frequency, which is defined by the contents of the HGF register (Table 3). However, even higher frequency notes may be produced since the low-pass filtering on the TONE output is not applied to the P1.7/MDY output. This results in the minimum decimal value x in the HGF register (see equation in Section 6.3) being 2 for the P1.7/MDY output, rather than 60 for the TONE output. A sinusoidal TONE output is produced at the same time as the melody square wave, but due to the filtering, the higher frequency sine waves with $x < 60$ will not appear at the TONE output.

Since the melody output is shared with P1.7, the port flip-flop of P1.7 has to be set HIGH before using the melody output. This is to avoid conflicts between melody and port outputs. The melody output drive depends on the configuration of port P1.7/MDY; see Chapter 14, Table 25.

6.3 Frequency registers

The two frequency registers HGF and LGF define two frequencies. From these, the digital sine synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures tone output levels independent of supply voltage and temperature.

The amplitude of the Low Group Frequency sine wave is attenuated by 2 dB compared to the amplitude of the High Group Frequency sine wave. The two sine waves are summed and then filtered by an on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

The value 00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption.

The frequency of the sine wave generated 'f' is dependent on the crystal frequency 'f_{xtal}' and the decimal value 'x' held in the frequency registers (HGF and LGF). The variables are related by the equation:

$$f = \frac{f_{xtal}}{[23\,(x+2)\,]}; \text{ where } 60 \leq x \leq 255.$$

The frequency limitation given by $x \geq 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

6.4 DTMF frequencies

Assuming an oscillator frequency f_{xtal} = 3.58 MHz, the DTMF standard frequencies can be implemented as shown in Table 7.

The relationships between telephone keyboard symbols, DTMF frequency pairs and the frequency register contents are given in Table 8.

Table 7 DTMF standard frequencies and their implementation; value = LGF, HGF contents

VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 8 Dialling symbols, corresponding DTMF frequency pairs and frequency register contents

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
•	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

6.5 Modem frequencies

Again assuming an oscillator frequency f_{xtal} = 3.58 MHz, the standard modem frequencies can be implemented as in Table 9. It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling Low Group Frequency generation.

Table 9 Standard modem frequencies and their implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980[1]	978.82	−0.12	−1.18
82	1180[1]	1179.03	−0.08	−0.97
8F	1070[2]	1073.33	0.31	3.33
79	1270[2]	1265.30	−0.37	−4.70
80	1200[3]	1197.17	−0.24	−2.83
45	2200[3]	2192.01	−0.36	−7.99
76	1300[4]	1296.94	−0.24	−3.06
48	2100[4]	2103.14	0.15	3.14
5C	1650[1]	1655.66	0.34	5.66
52	1850[1]	1852.77	0.15	2.77
4B	2025[2]	2021.20	−0.19	−3.80
44	2225[2]	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

6.6 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{xtal} = 3.58 MHz (Table 10). It is suggested to define the frequency by the HGF register while the LGF contains 00H, disabling Low Group Frequency generation.

Table 10 Musical scale frequencies and their implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD[1]	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 at 440 Hz.

7 EEPROM AND TIMER 2 ORGANIZATION

The PCD3359A has 128 bytes of Electrically Erasable Programmable Read-Only Memory (EEPROM). Such non-volatile storage provides data retention without the need for battery backup. In telecom applications, the EEPROM is used for storing redial numbers and for short dialling of frequently used numbers. More generally, EEPROM may be used for customizing microcontrollers, such as to include a PIN code or a country code, to define trimming parameters, to select application features from the range stored in ROM.

The most significant difference between a RAM and an EEPROM is that a bit in EEPROM, once written to a logic 1, cannot be cleared by a subsequent write operation. Successive write accesses actually perform a logical OR with the previously stored information. Therefore, to clear a bit, the whole byte must be erased and re-written with the particular bit cleared. Thus, an erase-and-write operation is the EEPROM equivalent of a RAM write operation.

Whereas read access times to an EEPROM are comparable to RAM access times, write and erase accesses are much slower at 5 ms each. To make these operations more efficient, several provisions are available.

First, the EEPROM array is structured into 32 four-byte pages (see Fig.5) permitting access to 4 bytes in parallel (write page, erase/write page and erase page). It is also possible to erase and write individual bytes. Finally, the EEPROM address register provides auto-incrementing, allowing very efficient read and write accesses to sequential bytes.

To simplify the erase and write timing, the derivative 8-bit down-counter (Timer 2) with reload register is provided. In addition to EEPROM timing, Timer 2 can be used for general real-time tasks, such as for measuring signal duration and for defining pulse widths.

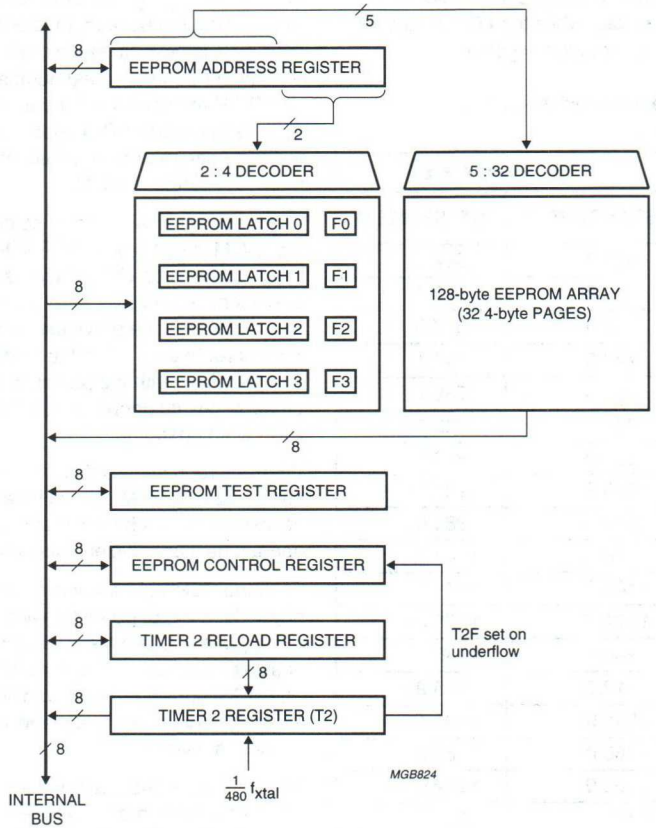


Fig.5 Block diagram of the EEPROM and Timer 2.

7.1 EEPROM registers

7.1.1 EEPROM Control Register (EPCR)

The behaviour of the EEPROM and Timer 2 section is defined by the EEPROM Control Register. See Tables 11, 12 and 13.

Table 11 EEPROM Control Register, EPCR (address 04H, access type R/W)

7	6	5	4	3	2	1	0
STT2	ET2I	T2F	EWP	MC3	MC2	MC1	0

Table 12 Description of EPCR bits

BIT	SYMBOL	DESCRIPTION
7	STT2	**Start T2.** If STT2 = 0, then Timer 2 is stopped; T2 value held. If STT2 = 1, then T2 decrements from reload value.
6	ET2I	**Enable T2 interrupt.** If ET2I = 0, then T2F event cannot request interrupt. If ET2I = 1, then T2F event can request interrupt.
5	T2F	**Timer 2 flag.** Set when T2 underflows (or by program); reset by program.
4	EWP	**Erase or write in progress.** Set by program (EWP starts EEPROM erase and/or write and Timer 2). Reset at the end of EEPROM erase and/or write.
3	MC3	**Mode control 3 to 1.** These three bits in conjunction with bit EWP select the mode as shown in Table 13.
2	MC2	
1	MC1	
0	–	This bit is set to a logic 0.

Table 13 Mode selection; X = don't care

EWP	MC3	MC2	MC1	DESCRIPTION
0	0	0	0	read byte
0	0	1	0	increment mode
1	0	1	X	write page
1	1	0	0	erase/write page
1	1	1	1	erase page
X	0	0	1	not allowed
X	1	0	1	
X	1	1	0	

7.1.2 EEPROM Address Register (ADDR)

The EEPROM Address Register determines the EEPROM location to which an EEPROM access is directed.

As a whole, ADDR auto-increments after read and write cycles to EEPROM, but remains fixed after erase cycles. This behaviour generates the correct ADDR contents for sequential read accesses and for sequential write or erase/write accesses with intermediate page setup. Overflow of the 8-bit counter wraps around to zero.

Table 14 EEPROM Address Register, ADDR (address 01H, access type R/W)

7	6	5	4	3	2	1	0
0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 15 Description of ADDR bits

BIT	SYMBOL	DESCRIPTION
7	–	This bit is set to a logic 0.
6 to 2	AD6 to AD2	AD2 to AD6 select one of 32 pages.
1 to 0	AD1 to AD0	AD1 and AD0 are irrelevant during erase and write cycles. For read accesses, AD0 and AD1 indicate the byte location within an EEPROM page. During page setup, finally, AD0 and AD1 select EEPROM Latch 0 to 3 whereas AD2 to AD6 are irrelevant. If increment mode (Table 13) is active during page setup, the subcounter consisting of AD0 and AD1 increments after every write to an EEPROM latch, thus enhancing access to sequential EEPROM latches. Incrementing stops when EEPROM Latch 3 is reached, i.e. when AD0 and AD1 are both a logic 1.

7.1.3 EEPROM Data Register (DATR)

Table 16 EEPROM Data Register (address 03H; access type R/W)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 17 Description of DATR bits

BIT	SYMBOL	DESCRIPTION
7 to 0	D7 to D0	The EEPROM Data Register (DATR) is only a conceptual entity. A read operation from DATR, reads out the EEPROM byte addressed by ADDR. On the other hand, a write operation to DATR, loads data into the EEPROM latch (see Fig.5) defined by bits AD0 and AD1 of ADDR.

7.1.4 EEPROM Test Register (TST)

The EEPROM Test Register is used for testing purposes during device manufacture. It must not be accessed by the device user.

7.2 EEPROM latches

The four EEPROM latches (EEPROM Latch 0 to 3; Fig.5) cannot be read by user software. Due to their construction, the latches can only be preset, but not cleared. Successive write operations through DATR to the EEPROM latches actually perform a logical OR with the previously stored data in EEPROM. The EEPROM latches are reset at the conclusion of any EEPROM cycle.

7.3 EEPROM flags

The four EEPROM flags (F0 to F3; Fig.5) cannot be directly accessed by user software. An EEPROM flag is set as a side-effect when the corresponding EEPROM latch is written through DATR. The EEPROM flags are reset at the conclusion of any EEPROM cycle.

7.4 EEPROM macros

The instruction sequence used in an EEPROM access should be treated as an indivisible entity. Erroneous programs result if ADDR, DATR, RELR or EPCR are inadvertently changed during an EEPROM cycle or its setup. Special care should be taken if the program may asynchronously divert due to an interrupt. Particularly, a new access to the EEPROM may only be initiated when no write, erase or erase/write cycles are in progress. This can be verified by reading bit EWP (register EPCR).

For write, erase and erase/write cycles, it is assumed that the Timer 2 Reload Register (RELR) has been loaded with the appropriate value for a 5 ms delay, which depends on f_{xtal} (see Table 24). The end of a write, erase or erase/write cycle will be signalled by a cleared EWP and by a Timer 2 interrupt provided that ET2I = 1 and that the SIO/derivative interrupt is enabled.

7.5 EEPROM access

One read, one write, one erase/write and one erase access are defined by bits EWP and MC1 to MC3 in the EPCR register; see Table 11.

Read byte retrieves the EEPROM byte addressed by ADDR when DATR is read. Read cycles are instantaneous.

Write and erase cycles take 5 ms, however. Erase/write is a combination of an erase and a subsequent write cycle, consequently taking 10 ms.

As their names imply, **write page, erase page and erase/write page** are applied to a whole EEPROM page. Therefore, bits AD0 and AD1 of register ADDR (see Table 14), defining the byte location within an EEPROM page, are irrelevant during write and erase cycles. However, write and erase cycles need not affect all bytes of the page. The EEPROM flags F0 to F3 (see Fig.5) determine which bytes within the EEPROM page are affected by the erase and/or write cycles. A byte whose corresponding EEPROM flag is zero remains unchanged.

With erase page, a byte is erased if its corresponding EEPROM flag is set. With write page, data in EEPROM Latch 0 to 3 (Fig.5) are ORed to the individual page bytes if and only if the corresponding EEPROM flags are set.

In an erase/write cycle, F0 to F3 select which page bytes are erased and ORed with the corresponding EEPROM latches.

ORing, in this event, means that the EEPROM latches are copied to the selected page bytes.

The described page-wise organization of erase and write cycles allows up to four bytes to be individually erased or written within 5 ms. This advantage necessitates a preparation step, called **page setup**, before the actual erase and/or write cycle can be executed.

Page setup controls EEPROM latches and EEPROM flags. This will be described in the Sections 7.5.1 to 7.5.5.

7.5.1 PAGE SETUP

Page setup is a preparation step required before write page, erase page and erase/write page cycles.
As previously described, these page operations include single-byte write, erase and erase/write as a special event. EEPROM flags F0 to F3 determine which page bytes will be affected by the mentioned page operations. EEPROM Latch 0 to 3 must be preset through DATR to specify the write cycle data to EEPROM and to set the EEPROM flags as a side-effect. Obviously, the actual preset value of the EEPROM latches is irrelevant for erase page. Preset of one, two, three or all four EEPROM latches and the corresponding EEPROM flags can be performed by repeatedly defining ADDR and writing to DATR (see Table 18).

If more than one EEPROM latch must be preset, the subcounter consisting of AD0 and AD1 can be induced to auto-increment after every write to DATR, thus stepping through all EEPROM latches. For this purpose, increment mode (Table 13) must be selected. Auto-incrementing stops at EEPROM Latch 3. It is not mandatory to start at EEPROM Latch 0 as in shown in Table 19.

Note that AD2 to AD6 are irrelevant during page setup. They will usually specify the intended EEPROM page, anticipating the subsequent page cycle.

From now on, it will be assumed that AD2 to AD6 will contain the intended EEPROM page address after page setup.

Table 18 Page setup; preset

INSTRUCTION	RESULT
MOV A, #addr	address of EEPROM latch
MOV ADDR, A	send address to ADDR
MOV A, #data	load write, erase/write or erase data
MOV DATR, A	send data to addressed EEPROM latch

Table 19 Page setup; auto-incrementing

INSTRUCTION	RESULT
MOV A, #MC2	increment mode control word
MOV EPCR, A	select increment mode
MOV A, #baddr	EEPROM Latch 0 address (AD0 = AD1 = 0)
MOV ADDR, A	send EEPROM Latch 0 address to ADDR
MOV A, R0	load 1st byte from Register 0
MOV DATR, A	send 1st byte to EEPROM Latch 0
MOV A, R1	load 2nd byte from Register 1
MOV DATR, A	send 2nd byte to EEPROM Latch 1
MOV A, R2	load 3rd byte from Register 2
MOV DATR, A	send 3rd byte to EEPROM Latch 2
MOV A, R3	load 4th byte from Register 3
MOV DATR, A	send 4th byte to EEPROM Latch 3

7.5.2 Read byte

Since ADDR auto-increments after a read cycle regardless of the page boundary, successive bytes can efficiently be read by repeating the last instruction.

Table 20 Read byte

INSTRUCTION	RESULT
MOV A, #RDADDR	load read address
MOV ADDR, A	send address to ADDR
MOV A, DATR	read EEPROM data

7.5.3 Write page

The write cycle performs a logical OR between the data in the EEPROM latches and that in the addressed EEPROM page. To actually copy the data from the EEPROM latches, the corresponding bytes in the page should previously have been erased.

The EEPROM latches are preset as described in Section 7.5.1. The actual transfer to the EEPROM is then performed as shown in Table 21.

The last instruction also starts Timer 2. The data in the EEPROM latches are ORed with that in the corresponding page bytes within 5 ms. A single-byte write is simply a special case of 'write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by bits AD2 to AD6) and to EEPROM Latch 0 (by bits AD0 and AD1). This allows efficient coding of multi-page write operations.

Table 21 Write page

INSTRUCTION	RESULT
MOV A, #EWP + MC2	'write page' control word
MOV EPCR, A	start 'write page' cycle

7.5.4 Erase/write page

The EEPROM latches are preset as described in Section 7.5.1. The page byte corresponding to the asserted flags (among F0 to F3) are erased and re-written with the contents of the respective EEPROM latches.

The last instruction also starts Timer 2. Erasure takes 5 ms upon which Timer Register T2 reloads for another 5 ms cycle for writing. The top cycles together take 10 ms. A single-byte erase/write is simply a special event of 'erase/write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by AD2 to AD6) and to EEPROM latch 0 (by AD0 and AD1). This allows efficient coding of multi-page erase/write operations.

Table 22 Erase/write page

INSTRUCTION	RESULT
MOV A, #EWP + MC3	'erase/write page' control word
MOV EPCR, A	start 'erase/write page' cycle

7.5.5 ERASE PAGE

The EEPROM flags are set as described in Section 7.5.1. The corresponding page bytes are erased.

The last instruction also starts Timer 2. Erasure takes 5 ms. A single-byte erase is simply a special case of 'erase page'.

Note that ADDR does not auto-increment after an erase cycle.

Table 23 Erase page

INSTRUCTION	RESULT
MOV A, #EWP + MC3 + MC2 + MC1	'erase page' control word
MOV EPCR, A	start 'erase page' cycle

7.6 Timer 2

Timer 2 is a 8-bit down-counter decremented at a rate of $^1/_{480} \times f_{xtal}$. It may be used either for EEPROM timing or as a general purpose timer. Conflicts between the two applications should be carefully avoided.

7.6.1 TIMER 2 FOR EEPROM TIMING

When used for EEPROM timing, Timer 2 serves to generate the 5 ms intervals needed for erasing or writing the EEPROM. At the decrement rate of $^1/_{480} \times f_{xtal}$, the reload value for a 5 ms interval is a function of f_{xtal}. Table 24 summarizes the required reload values for a number of oscillator frequencies.

Timer 2 is started by setting bit EWP in the EPCR. The Timer Register T2 is loaded with the reload value from RELR. T2 decrements to zero.

For an erase/write cycle, underflow of T2 indicates the end of the erase operation. Therefore, Timer Register T2 is reloaded from RELR for another 5 ms interval during which the flagged EEPROM latches are copied to the corresponding bytes in the page addressed by ADDR.

The second underflow of an erase/write cycle and the first underflow of write page and erase page conclude the corresponding EEPROM cycle. Timer 2 is stopped, T2F is set whereas EWP and MC1 to MC3 are cleared.

Table 24 Reload values as a function of f_{xtal}

f_{xtal} (MHz)	RELOAD VALUE[1] (HEX)
1	0A
2	14
3.58	25
6	3E
10	68
16	A6

Note

1. The reload value is $(5 \times 10^{-3} \times {}^1/_{480}\, f_{xtal}) - 1$; f_{xtal} in MHz.

7.6.2 TIMER 2 AS A GENERAL PURPOSE TIMER

When used for purposes other than EEPROM timing, Timer 2 is started by setting STT2. The Timer Register T2 (see Table 26) is loaded with the reload value from RELR. T2 decrements to zero. On underflow, T2 is reloaded from RELR, T2F is set and T2 continues to decrement.

Timer 2 can be stopped at any time by clearing STT2. The value of T2 is then held and can be read out. After setting STT2 again, Timer 2 decrements from the reload value. Alternatively, it is possible to read T2 'on the fly' i.e. while Timer 2 is operating.

8 INTERRUPTS

8.1 Derivative interrupt

One derivative interrupt event is defined. It is controlled by bits T2F and ET2I in the EPCR (see Tables 11 and 12).

The derivative interrupt event occurs when T2F is set. This request is honoured under the following circumstances:

- No interrupt routine proceeds
- No external interrupt request is pending
- The derivative interrupt is enabled
- ET2I is set.

The derivative interrupt routine must include instructions that will remove the cause of the derivative interrupt by explicitly clearing T2F. If the derivative interrupt is not used, T2F may directly be tested by the program. Obviously, T2F can also be asserted under program control, e.g. to generate a software interrupt.

8.2 Port 0 Wake-up interrupts

In addition to the external interrupt CE, the PCD3359A contain 8 level-sensitive external interrupt sources on Port 0. This function generates an interrupt request if any of the enabled lines of Port 0 (P0.0 to P0.7) is pulled LOW. Like the external interrupt (and contrary to the derivative interrupt) the Port 0 interrupt operates also in Stop mode and forces the CPU to exit the Stop mode.

The Port 0 Wake-up interrupts are controlled by the Enable Port 0 Interrupt bits EPI3 to EPI0 in the Melody and Port Interrupt Control Register MDYCON. Pairs of Port 0 interrupts are individually enabled/disabled via bits 4, 5, 6 and 7. For details see Section 6.1.2. As the Port 0 interrupt is directly linked to the external interrupt, it uses the same flag (EIF), enable instructions (EN I, DIS I) and interrupt vector.

A Port 0 Wake-up interrupt is serviced if:

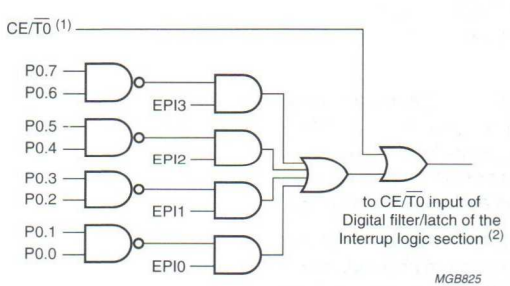
- No interrupt routine is in progress
- The external interrupt is enabled
- It's corresponding enable bit in register MDYCON is set to a logic 1.

If a Port 0 interrupt is to be used, the port flip-flop must first be set to a logic 1 (set to input mode) before it's corresponding EPIn
bit is set.

If only a portion of the Port 0 interrupts are used, the remaining port lines may still be used as normal I/O.

In order to configure an I/O as an input, a logic 1 must first be written to it. If a logic 0 is written to one of these port lines (e.g. ANL P0, 00H) while it's corresponding interrupt is enabled, a Port 0 interrupt will be generated.

For more details see data sheet *"PCD33xxA Family; Section External Interrupt"*.



(1) From pin CE/T0.
(2) See the *"PCD33XXA Family"* data sheet.

Fig.6 Simplified External/Port 0 interrupt structure.

9 TIMING

Although the PCD3359A operates over a clock frequency range from 1 to 16 MHz, f_{xtal} = 3.58 MHz will usually be chosen to take full advantage of the frequency generator section.

10 RESET

In addition to the conditions given in the *"PCD33XXA Family"* data sheet, all derivative registers are cleared in the reset state.

11 IDLE MODE

In Idle mode, the frequency generator, the EEPROM and the Timer 2 sections remain operative. Therefore, the IDLE instruction may be executed while an erase and/or write access to EEPROM is in progress.

12 STOP MODE

Since the oscillator is switched off, the frequency generator, the EEPROM and the Timer 2 sections receive no clock. It is suggested to clear both the HGF and the LGF registers before entering Stop mode. This will cut off the biasing of the internal amplifiers, considerably reducing current requirements.

The Stop mode **must not** be entered while an erase and/or write access to EEPROM is in progress. The STOP instruction may only be executed when EWP in EPCR is zero. The Timer 2 section is frozen during Stop mode. After exit from Stop mode by a HIGH level on CE/$\overline{T0}$, Timer 2 proceeds from the held state.

The Port 0 Wake-up interrupt function remains operative during Stop mode (depending only on the EPIn bits in register MDYCON). In addition to the description in the *"PCD33xxA family"* data sheet, Stop mode may be left by a Port 0 Wake-up interrupt event (see Section 8.2).

13 INSTRUCTION SET RESTRICTIONS

Please note the following:

- ROM space being restricted to 2 kbytes, the 'SEL MB1/2/3' instructions would define non-existing program memory banks and should therefore be avoided
- RAM space being restricted to 64 bytes, care should be taken to avoid accesses to non-existing RAM locations.

14 OVERVIEW OF PORT AND POWER-ON-RESET CONFIGURATION

All standard quasi-bidirectional I/O ports are available; see *"PCD33xxA family"* data sheet.

- Port 0: 8 parallel port lines P0.0 to P0.7 or wake-up interrupts
- Port 1: 8 parallel port lines P1.0 to P1.7
- Port 2: 4 parallel port lines P2.0 to P2.3.

Table 25 Port and Power-on-reset configuration

See notes 1 and 2.

COVERED BY OTP	PORT 0								PORT 1								PORT 2				V_{POR}
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	
PCD3756A	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1R	1R[3]	2S	2S	2S	2S	1.3 V

Notes

1. Port output drive: 1 = standard I/O; 2 = open-drain I/O, see *"PCD33xxA family"* data sheet.
2. Port state after reset: S = Set (HIGH) and R = Reset (LOW).
3. The melody output drive type is push-pull.

15 SUMMARY OF DERIVATIVE REGISTERS

Table 26 Register map

ADDR. (HEX)	REGISTER	7	6	5	4	3	2	1	0	R/W
00	not used									
01	EEPROM Address Register (ADDR)	0	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/W
02	not used									
03	EEPROM Data Register (DATR)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
04	EEPROM Control Register (EPCR)	STT2	ET21	TF2	EWP	MC3	MC2	MC1	0	R/W
05	Timer 2 Reload Register (RELR)	R7	R6	R5	R4	R3	R2	R1	R0	R/W
06	Timer 2 Register (T2)	T2.7	T2.6	T2.5	T2.4	T2.3	T2.2	T2.1	T2.0	R
07	Test Register (TST)	only for test purposes; not to be accessed by the device user								
08 to 10	not used									
11	High Group Frequency Register (HGF)	H7	H6	H5	H4	H3	H2	H1	H0	W
12	Low Group Frequency Register (LGF)	L7	L6	L5	L4	L3	L2	L1	L0	W
13	Melody and Port Interrupt Control Register (MDYCON)	EPI3	EPI2	EPI1	EPI0	0	0	0	EMO	R/W
14 to FF	not used									

16 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Data Handbook IC14, Section: Handling MOS devices"*).

17 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+7.0	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	−	125	mW
P_O	power dissipation per output	−	30	mW
I_{SS}	ground supply current	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	−	90	°C

18 DC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	see Fig.7				
	operating	note 1	1.8	–	6	V
	RAM data retention in Stop mode		1.0	–	6	V
I_{DD}	operating supply current	see Figs 8 and 9; note 2				
		V_{DD} = 3 V; value HGF or LGF ≠ 0	–	0.8	1.6	mA
		V_{DD} = 3 V	–	0.35	0.7	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.5	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	2.4	6.0	mA
$I_{DD(idle)}$	supply current (Idle mode)	see Figs 10 and 11; note 2				
		V_{DD} = 3 V; value HGF or LGF ≠ 0	–	0.7	1.4	mA
		V_{DD} = 3 V	–	0.25	0.5	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.1	3.4	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	1.7	5.0	mA
$I_{DD(stp)}$	supply current (Stop mode)	see Fig.12; note 3				
		V_{DD} = 1.8 V; T_{amb} = 25 °C	–	1.0	5.5	µA
		V_{DD} = 1.8 V; T_{amb} = 70 °C	–	–	10	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	−1	–	+1	µA
Port outputs						
I_{OL}	LOW level port sink current	V_{DD} = 3 V; V_O = 0.4 V; see Fig.13	0.7	3.5	–	mA
I_{OH}	HIGH level pull-up output source current	V_{DD} = 3 V; V_O = 2.7 V; see Fig.14	−10	−30	–	µA
		V_{DD} = 3 V; V_O = 0 V; see Fig.14	–	−140	−300	µA
I_{OH1}	HIGH level push-pull output source current	V_{DD} = 3 V; V_O = 2.6 V; see Fig.15	−0.7	−3.5	–	mA
Tone output (see Fig.16; note 4)						
$V_{HG(RMS)}$	HGF voltage (RMS value)		158	181	205	mV
$V_{LG(RMS)}$	LGF voltage (RMS value)		125	142	160	mV
$\Delta f/f$	frequency deviation		−0.6	–	+0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_o \rvert$	output impedance		–	100	500	Ω
G_v	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	T_{amb} = 25 °C; note 5	–	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EEPROM (notes 1 and 6)						
$CY_{t/w}$	endurance (erase/write cycles)	note 7	10^5	–	–	
t_{ret}	data retention time		10	–	–	years
Power-on reset (see Fig.17)						
V_{POR}	Power-on-reset level	configuration as PCD3756A; (see Table 25)	0.8	1.3	1.8	V
Oscillator (see Fig.18)						
g_m	transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

Notes

1. TONE output, EEPROM erase and write require $V_{DD} \geq 2.5$ V.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open; value HGF = LGF = 0, unless otherwise specified.
   a) Maximum values: external clock at XTAL1 and XTAL2 open-circuit.
   b) Typical values: T_{amb} = 25 °C; crystal connected between XTAL1 and XTAL2.
3. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; RESET, T1 and CE/T0 at V_{SS}; crystal connected between XTAL1 and XTAL2; pins T1 and CE/$\overline{T0}$ at V_{SS}.
4. Values are specified for DTMF frequencies only (CEPT).
5. Related to the Low Group Frequency (LGF) component (CEPT).
6. After final testing the value of each EEPROM bit is a logic 1, but this cannot be guaranteed after board assembly.
7. Verified on sampling basis.

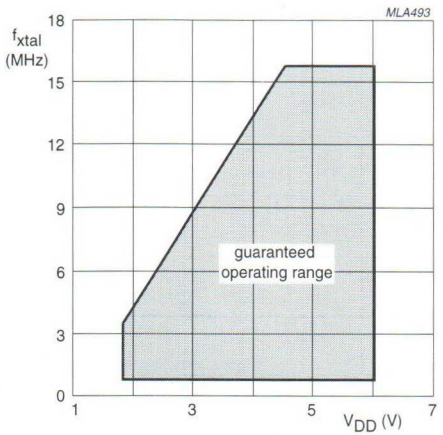
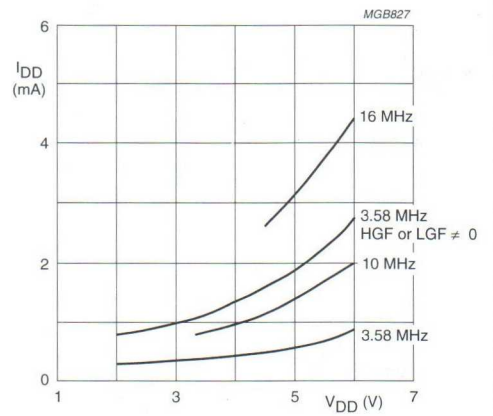
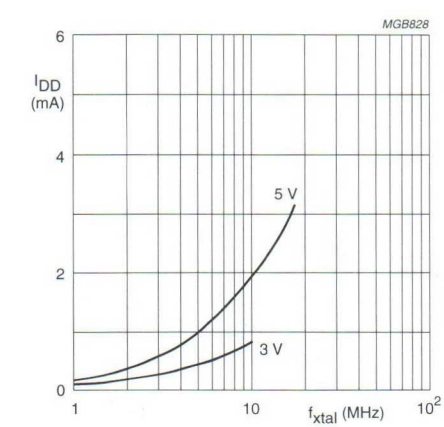


Fig.7 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).



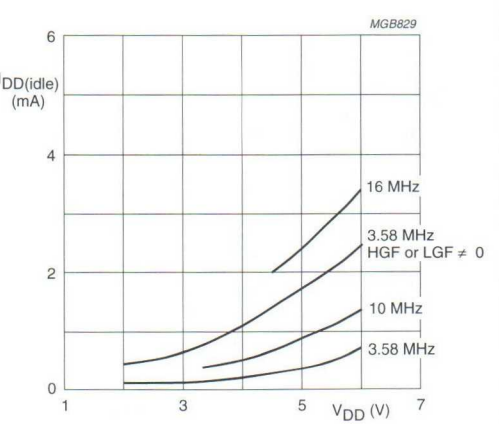
Measured with crystal between XTAL1 and XTAL2.

Fig.8 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).



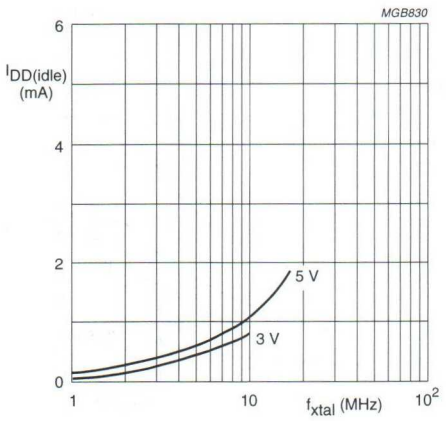
Measured with function generator on XTAL1.

Fig.9 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



Measured with crystal between XTAL1 and XTAL2.

Fig.10 Typical supply current in Idle mode ($I_{DD(idle)}$) as a function of supply voltage (V_{DD}).



Measured with function generator on XTAL1.

Fig.11 Typical supply current in Idle mode ($I_{DD(idle)}$)as a function of clock frequency (f_{xtal}).

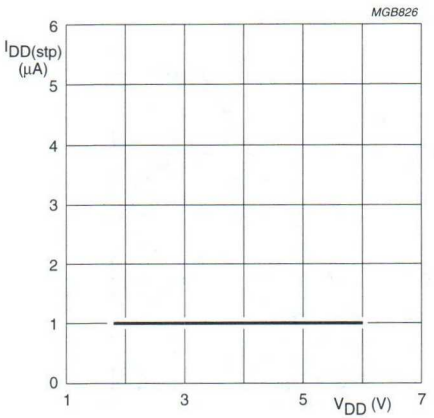
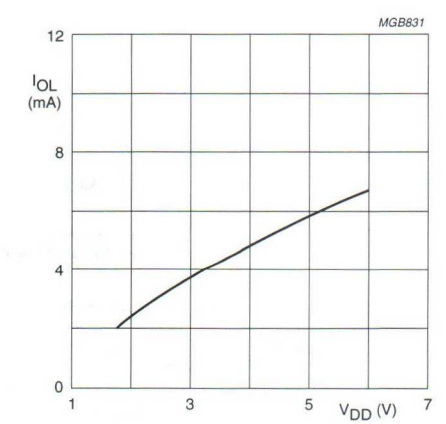


Fig.12 Typical supply current in Stop mode ($I_{DD(stp)}$) as a function of supply voltage (V_{DD}).



V_O = 0.4 V.

Fig.13 Typical LOW level output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

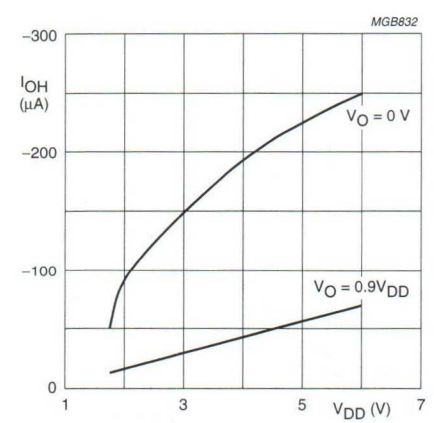
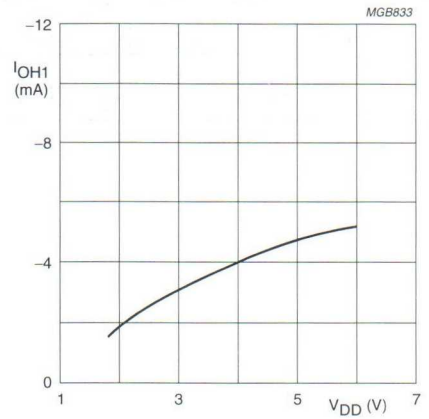
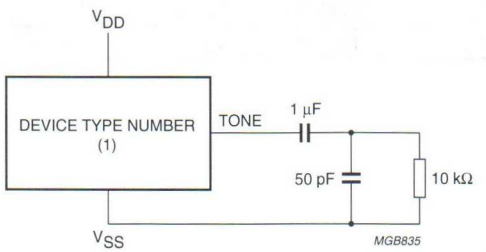


Fig.14 Typical HIGH level pull-up output source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.15 Typical HIGH level push-pull output source current (I_{OH1}) as a function of supply voltage (V_{DD}).



(1) Device type number: PCD3359A.

Fig.16 TONE output test circuit.

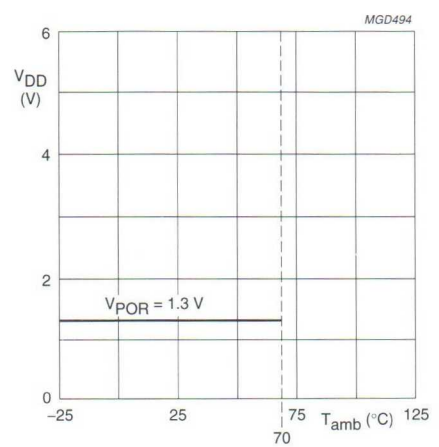


Fig.17 Typical Power-on-reset level (V_{POR}) as function of ambient temperature (T_{amb}).

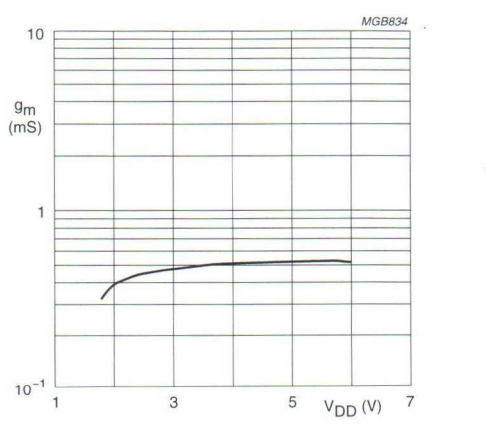


Fig.18 Typical transconductance as a function of supply voltage (V_{DD}).

19 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = –25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.7	1	–	16	MHz

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1 INTRODUCTION

This data sheet describes the shared properties of the PCD33xxA family of telecom microcontrollers. The family currently consists of:

- PCD3349A
- PCD3350A
- PCD3351A; 51C; 52A; 52 C; 53A; 53C; 55A
- PCD3354A; PCD3354C
- PCD 3356A; 57A; 59A
- PCD3755A; PCD3755E
- PCD3756A.

For a particular microcontroller, this data sheet should be read in conjunction with the individual data sheet of the specific device. The data can also be found in *"Data Handbook IC03, Semiconductors for Telecom Systems"* and in *"Data Handbook IC14, 8048-based 8-bit microcontrollers"*.

The PCF84xxxA family of microcontrollers offers similar characteristics to the PCD33xxA family, at lower cost, but without on-chip tone generation or EEPROM and with a higher minimum supply voltage of 2.5 V.

2 FEATURES

- 8-bit CPU, ROM, RAM, I/O and tone generator all in one package
- Up to 8 kbytes ROM
- Up to 256 bytes RAM
- DTMF, modem and musical tone generation
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 8 or more quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- 3 single-level vectored interrupts: external, timer/event counter, derivative
- Two test inputs, one of which also serves as the external interrupt input
- Power-on-reset, Stop and Idle modes
- Supply voltage range: 1.8 to 6 V
- Clock frequency: 1 to 16 MHz
- Operating temperature: –25 to +70 °C
- Manufactured in silicon gate CMOS process.
- Real-time clock (some devices)
- Up to 256 bytes of EEPROM (some devices).

3 GENERAL DESCRIPTION

The PCD33xxA Family of microcontrollers provide up to 8 kbytes of program memory and up to 256 bytes of RAM. All devices include flexible I/O ports, an 8-bit programmable timer/event counter and a choice of single-level vectored interrupts. The devices were designed primarily for telecom applications, and all feature on-chip DTMF, modem and musical tone generation.

The instruction set is based on that of the well-known MAB8048. Some of the devices have functional equivalents in the MAB84xx family of NMOS controllers. Where the lower power consumption and higher speed of CMOS provide advantages, the PCD33xxA devices can be used as direct replacements for their MAB84xx equivalents.

A range of One Time Programmable (OTP) devices with external program memory and 'Piggy-backs', as well as emulation probes and prototyping systems are also available.

4 BLOCK DIAGRAM

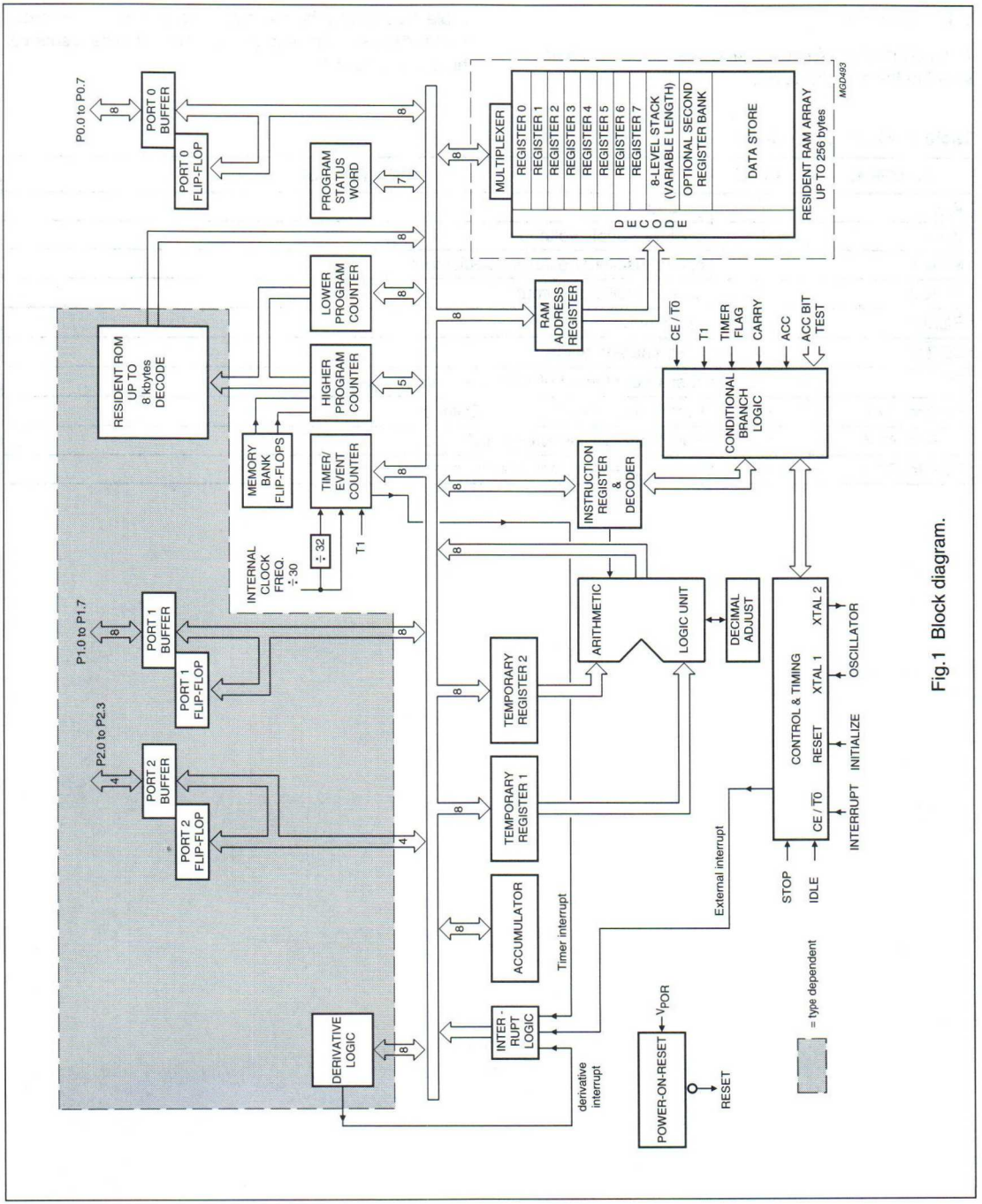


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

For individual pinning configurations consult the data sheet of the specific device.

5.2 Pin description

Table 1 describes the common functions of the devices. For full details of pin descriptions consult the data sheet of the specific device.

Table 1 Common functions

SYMBOL	TYPE	DESCRIPTION
V_{SS}	P	ground
V_{DD}	P	positive supply voltage
XTAL1	I	crystal oscillator/external clock input
XTAL2	O	crystal oscillator output
RESET	I	reset input
CE/$\overline{T0}$	I	Chip enable/Test 0
T1	I	Test 1/count input of 8-bit timer/event counter 1
P0.0 to P0.7	I/O	Port 0: quasi-bidirectional I/O lines
P1.0 to P1.7	I/O	Port 1: quasi-bidirectional I/O lines
P2.0 to P2.3	I/O	Port 2: quasi-bidirectional I/O lines

6 FUNCTIONAL DESCRIPTION

6.1 Central processing unit

The PCD33xxA Family provides an instruction set with arithmetic, logic, branching, input/output and control facilities. Special highlights are the instructions for BCD arithmetic, nibble handling, conditional branches, loop control (DJNZ) and table look-up (MOVP).

Code and execution efficiency is achieved by using a maximum of two bytes and two execution cycles per instruction (see Chapter 7).

6.2 Program memory

The program memory consists of up to 8 kbytes of read-only memory (ROM). Each location is directly addressable by the Program Counter. The program memory is mask-programmed at the factory. Figure 2 illustrates the program memory map.

Four program memory locations are of special importance:

- Location 0: first instruction to be executed after the processor is reset
- Location 3: first instruction of an external interrupt (CE/$\overline{T0}$) routine
- Location 5: first instruction of a derivative interrupt routine
- Location 7: first instruction of a timer/event counter interrupt routine.

Only 11 bits of the 13-bit Program Counter function as a counter. The two most significant bits can only be preset. The program memory is therefore, structured into banks of 2 kbytes. Transfer of control to other memory banks is performed by unconditional branches (JMP) or subroutine calls (CALL) when another memory bank has been pre-selected (by SEL MB instruction).

Each program memory bank is further divided into 8 pages of 256 bytes. Indirect (JMPP) and conditional branches cannot cross page boundaries.

6.3 Data memory

Data memory consists of up to 256 bytes of random access memory (RAM). All locations are indirectly addressable using RAM pointer registers. Up to 16 register locations are directly addressable.
Data memory also includes an 8-level Program Counter stack addressed by a 3-bit Stack Pointer. All RAM locations make efficient program loop counters if used with the decrement register and test instruction (DJNZ).
Figure 3 illustrates the data memory map.

6.3.1 Working registers

Locations 0 to 7 are working registers. They are accessible by efficient one byte/one cycle instructions, thus making these locations suitable for frequently accessed intermediate results.

As an alternative to locations 0 to 7, locations 24 to 31 may be used as working registers. Register Bank selection is made by SEL RB0/RB1 instructions. Register Bank 1 may be used as an extension of Register Bank 0, as an alternative register bank for interrupt service or as general purpose data memory.

The first two locations of each bank (R0, R1, R0' and R1') serve as RAM pointers that indirectly address all RAM locations.

6.3.2 Program Counter stack

Locations 8 to 23 may be used as an 8-level Program Counter stack reserving 2 locations per level, or as general purpose RAM. The stack (see Fig.5) saves return addresses and status during interrupt or subroutine servicing. Nesting of subroutines and/or interrupts is permitted up to 8-levels deep.

The 3-bit Stack Pointer always points to the next free stack level. Following device reset, the Stack Pointer points to level 0 (locations 8 and 9). On each subroutine call (CALL) or interrupt, the contents of the Program Counter and bits 4, 6 and 7 of the Program Status Word are transferred to the level indicated by the Stack Pointer. The Stack Pointer increments and points to the next free level. Overflow from level 7 to level 0 occurs after nesting eight levels deep. Further subroutine calls and/or interrupts must not occur at this stage since this would result in loss of program content; overriding level 0 content.

Return from interrupt must be performed by the RETR instruction, which decrements the Stack Pointer and restores the Program Counter and Program Status Word, valid before the interrupt occurred. Return from subroutine should be performed by the RET instruction. In contrast to RETR, RET does not restore the Program Status Word.

As a general rule, the use of RETR in conjunction with a subroutine call is not recommended. The use of RETR must also be avoided with subroutines called from interrupt routines because it prematurely terminates the interrupt state (see Section 6.6).

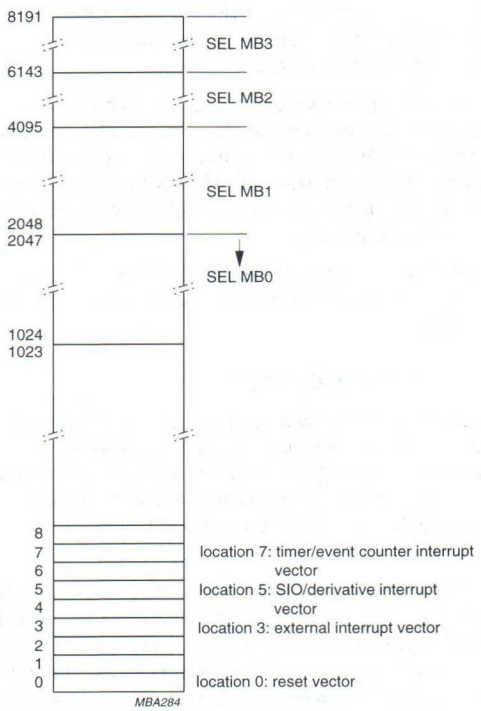


Fig.2 Program memory map.

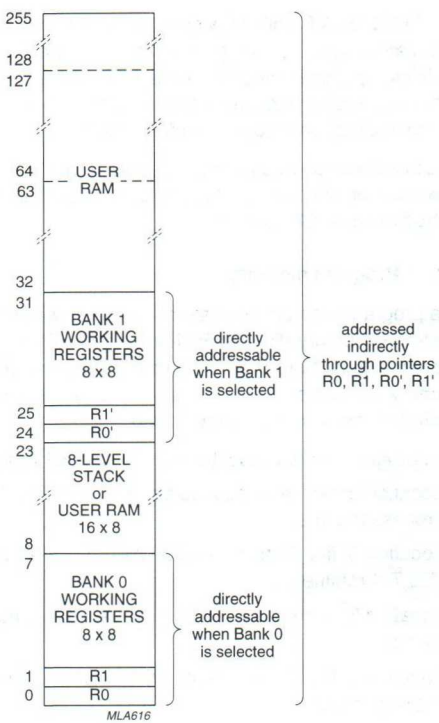


Fig.3 Data memory map.

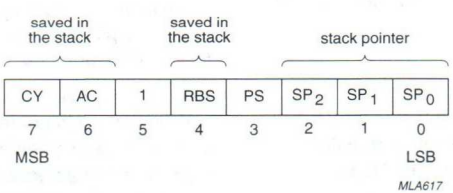


Fig.4 Program Status Word.

6.4 Program Counter

The 13-bit Program Counter is able to address up to 8 kbytes of ROM (see Fig.6). 11 bits (PC0 to PC10) are auto-incrementing. The two most significant bits (PC11 and PC12) must be changed under program control by SEL MB followed by a JMP or CALL instruction.

6.5 Program Status Word

The Program Status Word (PSW) is an 8-bit register in the CPU which stores information about the current status of the microcontroller (see Fig.4).

The PSW bits are:

- Bits 0 to 2: Stack Pointer bits (SP0, SP1, SP2)
- Bit 3: timer Prescaler Select (PS); 0 = modulo-32, 1 = modulo-1 (no prescaling)
- Bit 4: working Register Bank Select (RBS); 0 = register bank 0, 1 = register bank 1
- Bit 5: not used (fixed at 1)
- Bit 6: Auxiliary Carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7: Carry (CY); the carry flag indicates that the previous operation resulted in an overflow of the Accumulator.

All bits can be read using the MOV A, PSW instruction. Bits 0, 1 and 2 are affected by CALL, RET, RETR and interrupts. Bit 3 can be controlled by MOV PSW, A and bit 4 by SEL RB instructions. Bit 6 is set and cleared as a side-effect of ADD and ADDC instructions. Bit 7 is affected by ADD, ADDC, DA, RLC, RRC, CLR C and CPL C instructions.

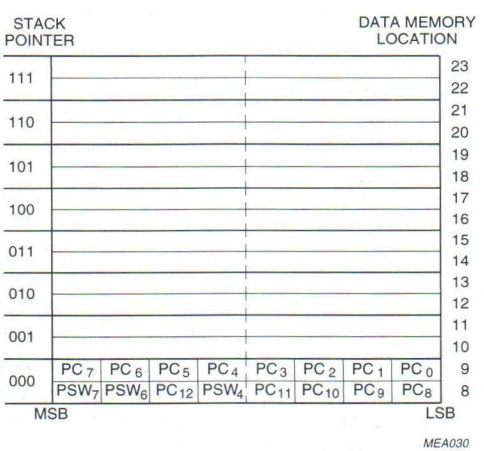


Fig.5 Program Counter Stack.

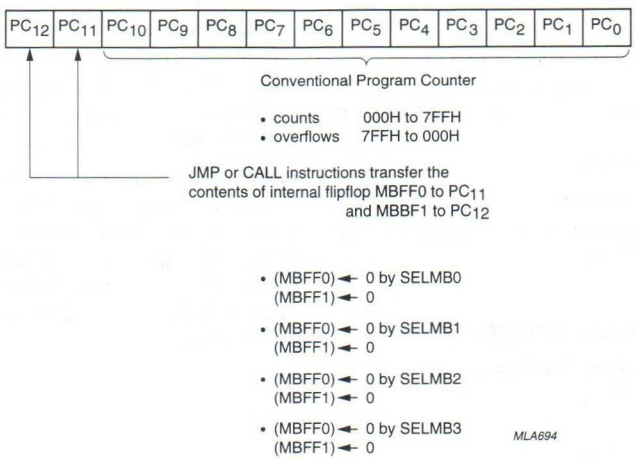


Fig.6 Program Counter.

6.6 Interrupts

External, derivative and timer/event counter interrupts are handled by the PCD33xxA Family. The interrupt mechanism is single level, i.e. an executing interrupt routine cannot be pre-empted unless by reset. Further interrupt requests are latched. If several interrupt requests are detected simultaneously, they are honoured according to their priority:

- External interrupt (highest priority)
- Derivative interrupt
- Timer/event counter interrupt (lowest priority).

An interrupt request is only sensed if the corresponding enable flag is set (see Fig.7). When the request is honoured, the contents of the Program Counter and bits 4, 6 and 7 of the Program Status Word are saved on the Program Counter stack. The Program Counter is loaded with the appropriate interrupt vector, thereby indicating the beginning of the interrupt routine. Since the Accumulator is not automatically saved, it must be saved and restored by user software. The interrupt routine must be terminated by the RETR (return and restore) instruction. At least one instruction of the main program will then be executed before another interrupt routine is entered.

To avoid erroneous real-time programs, a few words of caution:

- While the interrupt is in progress, the two most significant bits of the Program Counter are frozen at zero. Thus, interrupt routines and subroutines called from interrupt routines must reside entirely in Bank 0.
- The SEL MB instruction must not be used in interrupt routines and in subroutines called from interrupt routines. Otherwise, the changed contents of MBFF0 and MBFF1 (see Fig.6) may lead to erroneous JMP and CALL destinations after return from interrupt.
- Subroutines and nested subroutines called from the interrupt routine must all end with RET since RETR clears the Interrupt In Progress flag (IIP), as a side-effect (see Figs 7 and 8). Further pending interrupts would then interfere with the interrupt routine in progress.

6.6.1 External interrupt

A LOW-to-HIGH transition on the CE/$\overline{T0}$ pin is latched in the digital filter/latch if the HIGH state exceeds 7 clock periods after a LOW state of more than 4 clock periods. If the external interrupt is enabled the External Interrupt Flag (EIF) is also asserted, thus constituting a valid external interrupt request. As soon as the IIP is clear, indicating that no interrupt routine is in progress, the external interrupt is invoked by a forced CALL to location 3. The EIF is simultaneously cleared (see Figs 7 and 8). The interrupt routine may acknowledge the interrupt via port lines. Execution of a DIS I (disable external interrupt) instruction cancels a stored interrupt request by clearing both the digital filter/latch and the EIF.

For some devices the external interrupt is shared between the CE/$\overline{T0}$ pin and additional wake-up interrupts from the derivative logic. Software polling may be necessary to determine the origin of request. Since the interrupt flags of the derivative logic are not cleared by DIS I, the external interrupt routine must include instructions that will remove the cause of the external interrupt. For more details about shared external interrupts consult the data sheet of the specific device.

6.6.1.1 Chip Enable/Test 0 Input (CE/$\overline{T0}$)

The CE/$\overline{T0}$ input has two purposes:

- External interrupt input (see Section 6.6.1)
- Test 0 input.

When used as a Test 0 input (external interrupt disabled) the conditional branch instruction JT0 will cause a jump if CE/$\overline{T0}$ = 1. The conditional branch instruction JNT0 will also cause a jump if CE/$\overline{T0}$ = 0. If CE/$\overline{T0}$ is not used, it must be tied to V_{DD} or V_{SS}.

6.6.2 Derivative interrupt

The derivative interrupt is shared between all the interrupt sources in the derivative logic. Software polling may be necessary to determine the origin of a request.

An interrupt condition in the derivative logic will pull the PIN line LOW. If the derivative interrupt is enabled and no interrupt routine is in progress, the derivative interrupt routine will be invoked by a forced CALL to program memory location 5. The derivative interrupt routine must include instructions that will remove the cause of the derivative interrupt and thus reset PIN to its inactive HIGH state. For derivative interrupts, consult the data sheet of the specific device.

6.6.3 Timer/event counter interrupt

If the timer/event counter interrupt is enabled, a timer/event counter 1 overflow sets the Timer Interrupt Flag (TIF). As soon as IIP is clear, meaning that no interrupt routine is in progress, the timer/event counter interrupt routine is invoked by a forced CALL to program memory location 7. The TIF is simultaneously cleared (see Figs 7 and 8). Execution of a DIS TCNTI (disable timer/event counter interrupt) instruction cancels a stored interrupt request by clearing TIF.

The timer/event counter interrupt may also be used to simulate a second external interrupt. After an enable timer/event counter interrupt (EN TCNTI), the counter mode is enabled by a STRT CNT instruction which loads FFH (the state preceding overflow) into the counter. A positive edge on the T1 pin will overflow the counter and set TIF.

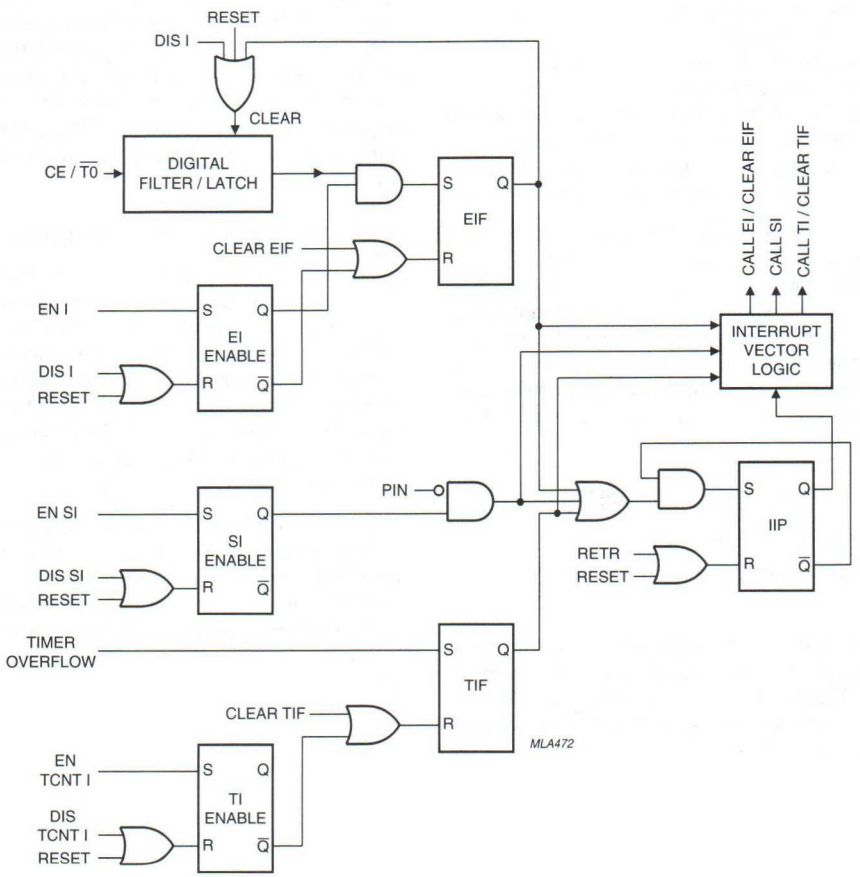


Fig.7 Simplified interrupt logic schematic (the R input overrules the S input for all flags).

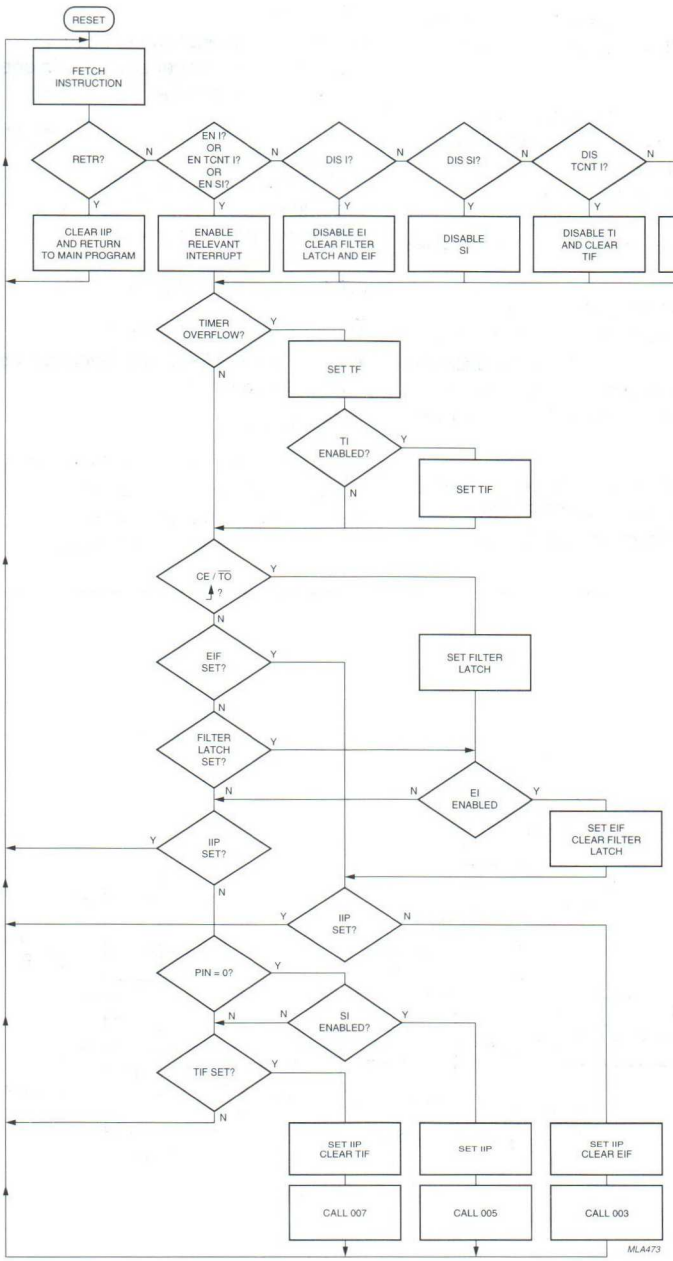


Fig.8 Flow chart illustrating CPU control in the presence of interrupts.

6.7 Timer/event counter 1

An internal 8-bit up counter is provided. The counter can be preset and read by the MOV T, A and MOV A, T instructions.

When the counter is to be used in the timer mode, a STRT T (start timer) instruction must be executed. Depending on the PS bit in the Program Status Word, the counter will increment every machine cycle (PS = 1, $1/30 \times f_{xtal}$) or every 32 machine cycles (PS = 0, $1/960 \times f_{xtal}$). STRT T clears the prescaler (see Fig.9) which is not otherwise accessible.

To count external events a STRT CNT (start event counter) instruction must be executed. A LOW-to-HIGH transition on pin T1 is counted if the HIGH state exceeds 4 clock periods after a LOW state of more than 4 clock periods. The maximum count rate is one increment per machine cycle ($1/30 \times f_{xtal}$).

The timer mode and the event counter mode are both inhibited after reset or by executing a STOP TCNT (stop timer/event counter) instruction (see Fig.9).

In both the timer and in event counter modes, overflow has two effects:

- If the timer/event counter interrupt is enabled TIF is asserted thereby generating a timer/event counter interrupt request (see Section 6.6).
- The Timer Flag (TF) is set. TF can be tested by conditional branch instructions JTF (jump if TF = 1) or JNTF (jump if TF = 0). The JTF and JNTF instruction, as a side-effect, reset TF. The only other way to clear TF is to reset the microcontroller.

6.7.1 TEST 1/COUNT INPUT (T1)

The T1 input has two purposes:

- Count input of 8-bit timer/event counter 1 (see Section 6.7)
- Test 1 input.

When used as a Test 1 input the conditional branch instruction JT1 will cause a jump if T1 = 1. The conditional branch instruction JNT1 will also cause a jump if T1 = 0. If T1 is not used, it must be tied to V_{DD} or V_{SS}.

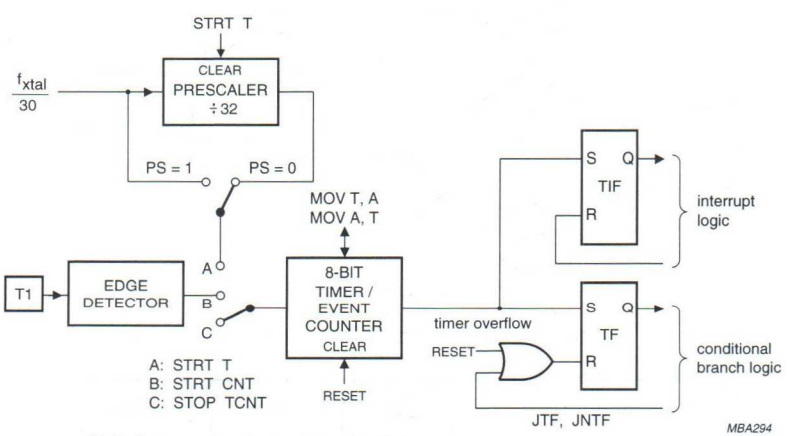


Fig.9 Timer/event counter 1.

6.8 Parallel ports

Three standard quasi-bidirectional I/O ports are defined:

- Port 0: parallel port of 8 lines (P0.0 to P0.7)
- Port 1: parallel port of 8 lines (P1.0 to P1.7)
- Port 2: parallel port of 4 lines (P2.0 to P2.3).

Several members of the PCD33xxA Family provide all 20 port lines. The eight Port 0 lines (P0.0 to P0.7) are available as a minimum. In addition to the standard ports, many PCD33xxA microcontrollers offer a variety of derivative ports. Please consult the data sheet of the specific device.

In general, all parallel ports can be used as either inputs or outputs. Output data written to a port is latched and remains unchanged until rewritten. If the port is used as an input, the external data is not latched and must remain stable until it is accessed by the CPU.

The standard port configuration is illustrated in Fig.11. When a logic 0 is written to the master/slave flip-flop, TR2 and TR3 are both in the OFF condition. TR1 turns ON and drives the output to V_{SS}.

When a logic 1 is written to the master/slave flip-flop, TR1 turns OFF. TR2 and TR3 both turn ON driving the output rapidly to V_{DD}. TR2 remains in the ON condition for the duration of the write pulse only. The constant current source is responsible for keeping the output line high. Sufficient source current is available for a TTL load HIGH level; the line can, however, be overridden by an external device. This is used when the port line serves as an input, but it may also be useful for wired-OR applications. In the latter case, unnecessary current through external devices is avoided since repeated logic 1 write operations will not activate TR2. The booster transistor TR2 is only asserted during a LOW-to-HIGH transition of the master/slave flip-flop. If the port line is to be used as an input, a logic 1 should first be stored in the master/slave flip-flop to turn TR1 OFF.

Access to Ports 0, 1 and 2 is provided by the parallel input/output instructions IN, OUTL, ANL and ORL. IN inputs port data to the Accumulator. OUTL outputs Accumulator data to the port. ANL and ORL are used for data manipulation in the port flip-flop. In contrast to Ports 0, 1 and 2, derivative ports are accessed by the derivative input/output instructions MOV, ANL and ORL. ANL and ORL are used for data manipulation in the port flip-flop. MOV is used for all data transfers between port and Accumulator. The source data for the Accumulator can be loaded from either the port line or the port flip-flop. Two derivative addresses are therefore provided per port (see Table 2).

All standard and derivative port accesses are performed by two-cycle instructions. Their instruction timing is shown in Fig.10. For input, data on port lines is sensed during timeslots 3 and 4 of machine cycle 2 (see Sections 6.9 and 6.11). For output, the data change occurs in timeslot 7. For OUTL, data changes during machine cycle 1. For ANL, ORL and MOV Dx, A, data changes during machine cycle 2.

Table 2 Derivative port address pair

ADDRESS	TYPE	ACCESS
8-bit line address	R	derivative port line
8-bit flip-flop address	R/W	derivative port flip-flop

Three port output configurations are available:

1. **Standard output**; quasi-bidirectional I/O with switched pull-up current source of 100 µA (typ.) and p-channel booster transistor TR2. TR2 is only active for 1 clock cycle during LOW-to-HIGH transitions (see Fig.11).
2. **Open-drain output**; quasi-bidirectional I/O with only an n-channel open-drain output. Application as an output requires connection of an external pull-up resistor (see Fig.12). If unused, an open-drain output should be tied to V_{SS}. This keeps the input path from floating, thereby avoiding undesirable current flow through input stages.
3. **Push-pull output**; drive capability of the output will be 5 mA (typ.) at V_{DD} = 3 V in both polarities. Since short circuit currents would flow during input, push-pull lines must only be used as outputs (see Fig.13).

Besides port output configurations, the port flip-flop state, after reset, is specified for each individual port line. Usually the 'set option' will be selected, which avoids short-circuits for ports intended as inputs. However, there may be cases in which the port should output a logic zero after reset. The user may then specify the 'reset option' for certain port lines.

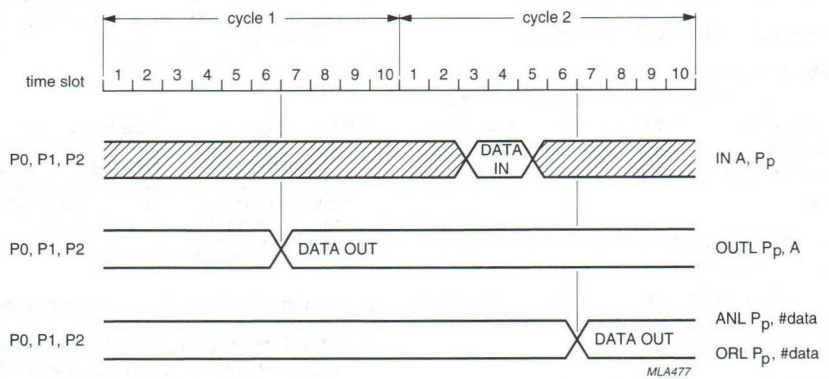


Fig.10 Input/output timing of standard and derivative ports.

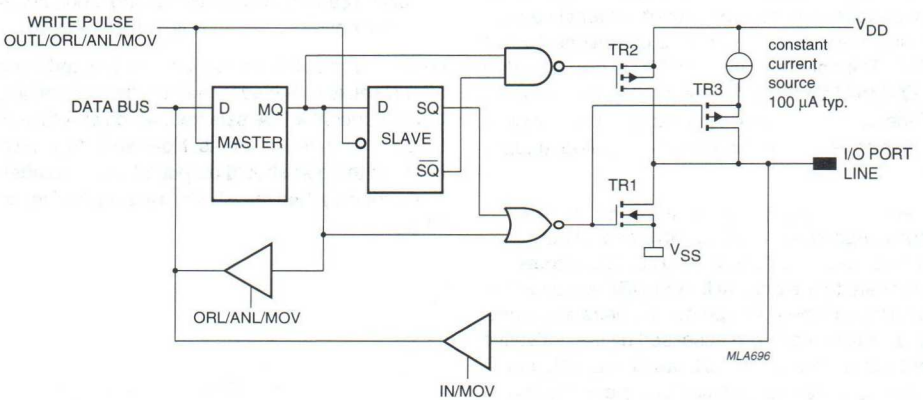


Fig.11 Standard output with switched current source.

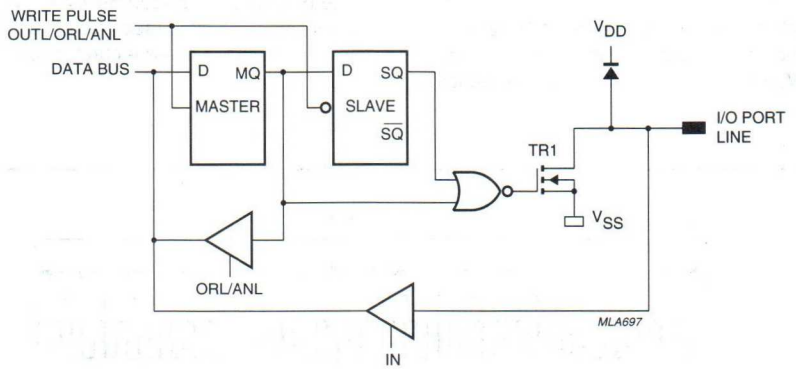


Fig.12 Open-drain output.

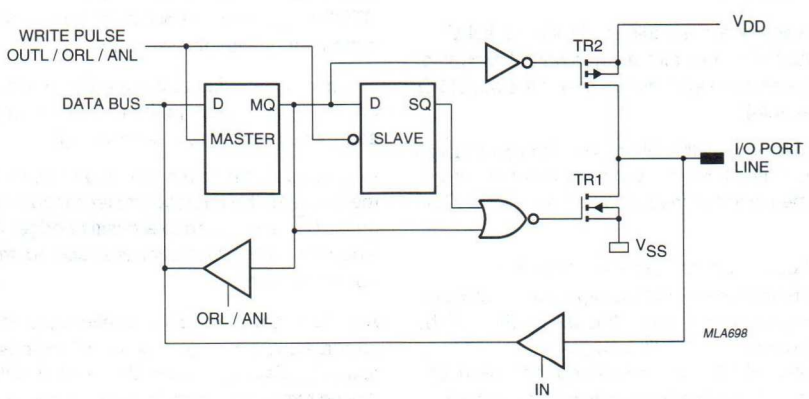


Fig.13 Push-pull output.

6.9 Timing

Every machine cycle consists of 10 time slots which are again subdivided into 3 clock periods each (see Fig.14).

Permitted clock frequencies range from 1 MHz to a maximum, which is a function of the supply voltage. At $V_{DD} \geq 4.5$ V, a 16 MHz maximum clock frequency is guaranteed.

The clock signal may be internally generated by an on-chip oscillator. Alternatively, an external clock may be applied to pin XTAL1. In this configuration, a short circuit with an internal pull-up transistor on XTAL1 may occur while the oscillator is inhibited (see Section 6.11). Care should be taken to avoid excessive current flow.

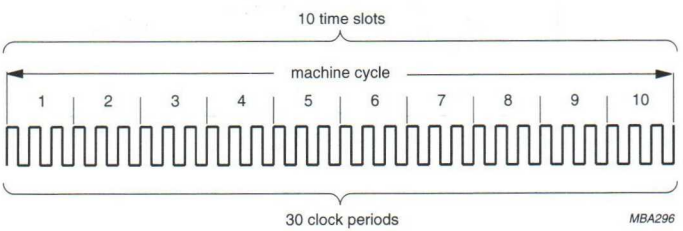


Fig.14 Timing of a machine cycle.

6.10 Reduced power modes

6.10.1 IDLE MODE

The Idle mode is very useful in low-power applications. When all computational tasks are completed, the device can be put into standby instead of into a busy waiting loop. Nevertheless, the device is on the alert and ready to respond rapidly to any interrupt.

The microcontroller enters the Idle mode via the IDLE instruction. In the Idle mode, all activity is halted except for the oscillator, the timer/event counter 1 and the serial I/O interface (if available).

The microcontroller leaves the Idle mode when an enabled interrupt occurs. The interrupt routine is executed before operation resumes with the instruction following the IDLE opcode.

For timer/event counter interrupts and derivative interrupts, termination of the Idle mode is straightforward. However, care must be taken when the Idle mode is left by the external interrupt since CE/$\overline{T0}$ is triggered on the rising edge. If CE/$\overline{T0}$ was HIGH prior to entering the Idle mode, it must be taken LOW before the positive edge can be generated. Figure 15 specifies the exact timing for leaving the Idle mode via the external interrupt CE/$\overline{T0}$.

If no interrupt is enabled, the Idle mode can only be terminated by an active signal on the RESET pin. A normal reset sequence is executed (see Fig.15).

6.10.2 STOP MODE

The Stop mode allows very low-power applications. When all computational tasks are completed, the device can be almost completely shut off by stopping its oscillator. In contrast to the Idle mode, the device is not ready to respond rapidly to any interrupt.

When the microcontroller enters the Stop mode via the STOP instruction; the oscillator is switched off. All internal states and I/O levels are maintained.

The microcontroller leaves the Stop mode by a HIGH level on CE/$\overline{T0}$ or a reset. In the latter case, a normal reset sequence is executed (see Fig.16).

In contrast to the Idle mode and the external interrupt mechanism, the microcontroller responds to a HIGH level on CE/$\overline{T0}$ rather than to a positive edge. If CE/$\overline{T0}$ is HIGH when the STOP instruction is executed, the Stop mode will not be entered.

A positive edge on CE/$\overline{T0}$ continues program execution after a 1866 clock cycle delay, which ensures proper oscillator start-up. If the external interrupt is enabled, the device executes the instruction following the STOP opcode before diverting to the interrupt routine. If the external interrupt is disabled, program execution continues with the instructions following the STOP opcode (see Fig.16).

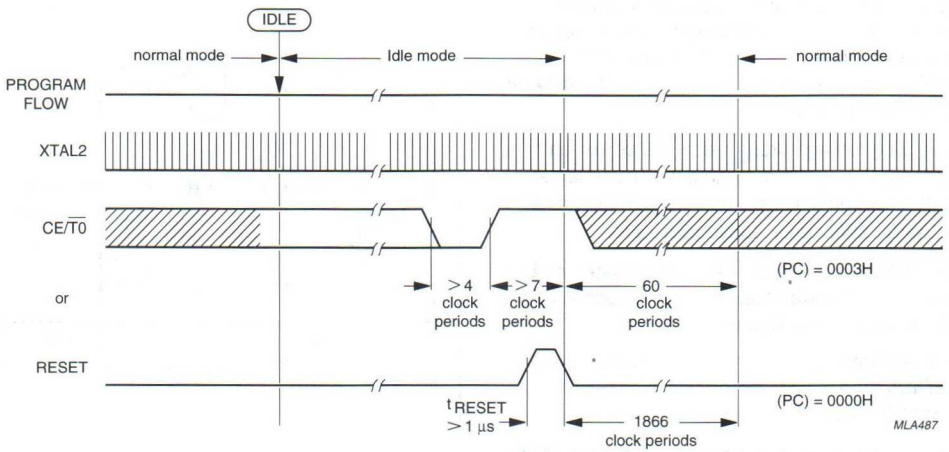


Fig.15 Entering and leaving the Idle mode.

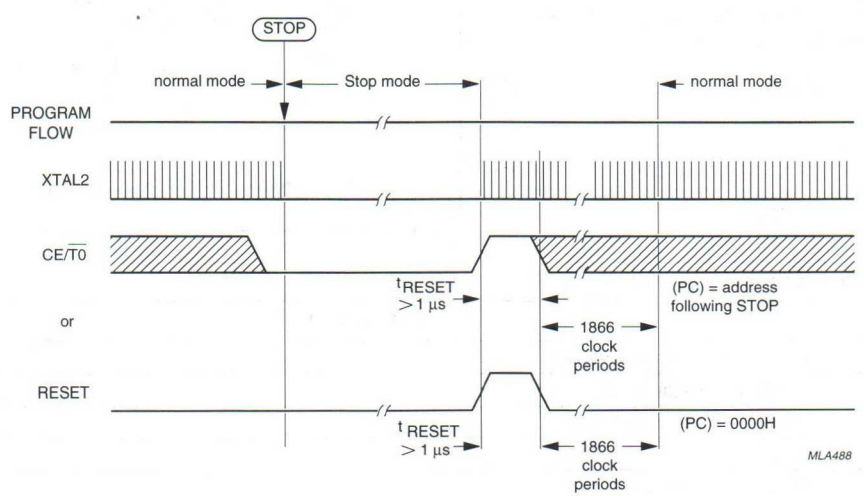


Fig.16 Entering and leaving the Stop mode.

6.11 Oscillator

The on-chip oscillator basically consists of an inverter stage which includes a feedback resistor and load capacitors (see Fig.17). In most applications, a quartz crystal will be connected between XTAL1 and XTAL2. Alternatively, a ceramic resonator or an inductor may be used as a timing element.

When the supply voltage drops below the power-on reference level, the oscillator is inhibited. The internal oscillator can also be inhibited by the STOP instruction under software control (see Section 6.10.2).

The transconductance (g_m) of the inverter stage can be mask-programmed, thereby optimizing the oscillator for a specific frequency and resonator.

Three standard transconductance options, referred to as LOW, MEDIUM and HIGH, can be specified by the user depending on the device chosen.

With $C_1 = C_2 = 10$ pF on-chip, external capacitors are not required for quartz oscillators. However, for adequate frequency stability, PXE resonators need external capacitors in the order of the static resonator capacitance C_0, such as external $C_1 = C_2 = 30$ to 100 pF.

Oscillator start-up time depends mainly on the external timing element. The start-up time of a quartz crystal is several milliseconds because of the narrow crystal bandwidth. For proper oscillator start-up, the transconductance (g_m) of the inverter stage must fulfil relationship (1) and (2); shown below.

$$g_m > 4.2\left[R_X\omega^2(C_L + C_0 + C_F)^2 + \frac{1}{R_P}\right] \quad (1)$$

$$g_m < \frac{C1 \times C2}{\left[R_X(C_0 + C_F)^2 + \frac{1}{\omega^2 R_P}\right]} \quad (2)$$

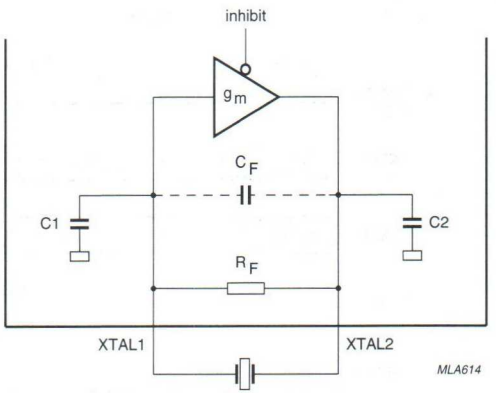


Fig.17 Oscillator with integrated elements.

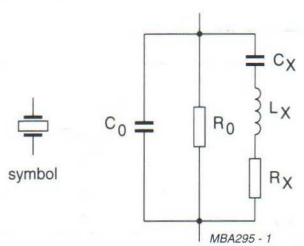


Fig.18 Crystal unit equivalent circuit.

Table 3 Notation to relationship (see Figs 17 and 18)

SYMBOL	DEFINITION
R_X	resonator series resistance
C_0	static resonator capacitance
R_0	resonator loss resistance
R_P	R_0 // R_F
R_F	feedback resistor
C_L	C1 × C2/(C1 + C2) (load capacitance)
C_F	parasitic feedback capacitance (typically 2 pF on-chip, external value depends on printed-circuit board wiring)
ω	$2\pi f_{osc}$

6.12 Reset

To ensure proper start-up, the microcontroller must be initialized to a defined starting condition. The device executes the first instruction 1866 clock cycles after the falling edge of the internal reset.

6.12.1 PASSIVE EXTERNAL RESET

A passive reset is generated by the RC circuit illustrated in Fig.19. While V_{DD} rises, the discharged C_{reset} keeps the RESET pin near the V_{DD} level. When V_{DD} crosses the power-on reference level (V_{POR}) the Power-on-reset circuit generates a reset pulse of approximately 50 µs. This pulse is without effect since it feeds into the reset signal forced by the pulse on the RESET pin.

The f_{xtal} dependent minimum V_{DD} must be reached before the voltage on RESET drops below $V_{IH} = 0.7V_{DD}$.

This translates into a lower bound for $C_{reset}R_{reset}$ equal to twice the rise time of V_{DD} (for linearly rising V_{DD}) or eight times the time constant of V_{DD} (for exponentially rising V_{DD}). The internal diode rapidly discharges C_{reset} when V_{DD} falls off, ensuring reliable reset even after short interruptions of supply voltage. To avoid overload of the internal diode, an external diode should be added in parallel if $C_{reset} > 2.2$ µF.

6.12.2 ACTIVE EXTERNAL RESET

An active reset can be generated by driving the RESET pin HIGH from an external logic device. Such an active reset pulse should not fall off before V_{DD} has reached its f_{xtal} dependent minimum operating value.

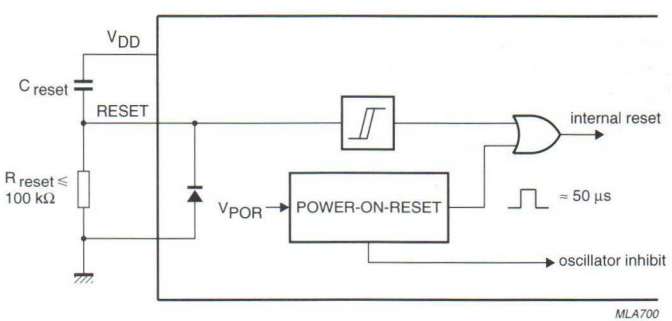


Fig.19 Passive external Power-on-reset.

6.12.3 INTERNAL RESET

In systems where V_{DD} reaches its f_{xtal} dependent minimum operating value before the clock f_{xtal} is applied, reset can be performed without external components. This condition is generally fulfilled with quartz and PXE resonators since oscillator start-up takes several milliseconds. Besides, rapid power-up is usually available in battery-powered systems.

If the internal Power-on-reset is used the RESET pin should be connected to V_{SS}. When V_{DD} increases above the power-on reference level V_{POR}, the Power-on-reset circuit generates a reset pulse of approximately 50 µs.

This pulse guarantees proper initialization under the conditions defined above.

The power-on reference level V_{POR} is a mask option. The user can select a reference voltage between 1.2 V and 3.6 V in discrete steps of 100 mV.

The chosen V_{POR} should have sufficient margin regarding the minimum intended V_{DD}.

A mask option without an internal Power-on-reset circuit is also available. It is recommended if the user does not intend to use the internal Power-on-reset circuit. In this case, the supply current requirements in Stop mode (see Section 6.10.2) will reduce to the level of leakage currents, i.e. virtually zero at ambient temperature.

6.12.4 RESET STATE

After a reset, the device state is characterized as follows:

- Program Counter 00H
- Memory bank 00H
- Register Bank 00H - Stack Pointer 00H (location pair 8 and 9)
- All interrupts disabled
- Timer/event counter 1 stopped and cleared
- Timer prescaler modulo-32 (PS = 0)
- Timer flag cleared
- All port flip-flops set to logic 1 or logic 0 depending on the port configuration
- Idle and Stop modes cancelled.

6.13 Derivative logic

Derivative logic is provided with many members of the PCD33xxA Family. The detailed description of the derivative circuitry is given in the data sheet of the specific device. In this section, the shared principles of derivative logic are briefly reviewed.

Derivative registers are accessed over the internal bus. The derivative registers are write-only, read-only or read/write (see Fig.20). They are addressed through the derivative Address Register when the derivative input/output instructions (MOV A, Dx; MOV Dx, A; ANL Dx, A and ORL Dx, A) are executed.

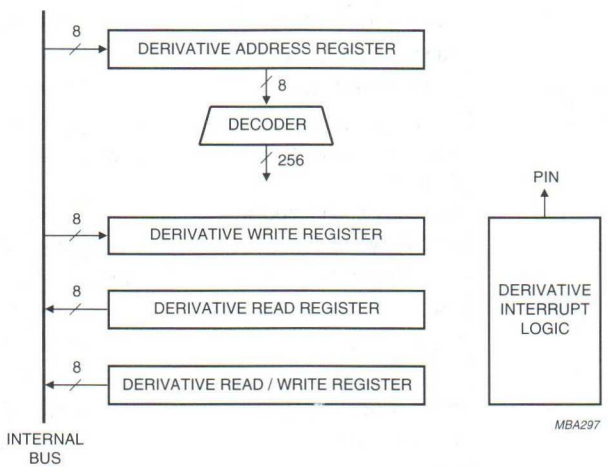


Fig.20 Block diagram of derivative logic.

Table 4 Summary of configurations

FEATURE	CONFIGURATION	DESCRIPTION
ROM	any mix of instructions	program; size restricted by ROM size (see Tables 5 and 6)
Ports	configuration 1	standard output (see Fig.11)
	configuration 2	open-drain output (see Fig.12)
	configuration 3	push-pull output (see Fig.13)
	set	flip-flop at logic 1 after reset
	reset	flip-flop at logic 0 after reset
Power-on reference	V_{POR}	1.2 to 3.6 V in increments of 100 mV; with ±500 mV accuracy
Oscillator	g_{mL}	LOW transconductance
	g_{mM}	MEDIUM transconductance
	g_{mH}	HIGH transconductance

7 INSTRUCTION SET

The PCD33xxA instruction set consists of over 100 one and two-byte instructions. Program code efficiency is high because all RAM locations and all ROM locations on a 256-byte page require only a single-byte address. Table 6 lists the symbols that are used in Table 5 and the Instruction map is shown in Section 7.1.

Table 5 PCD33xxA Family instruction set

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
Accumulator					
ADD A, Rr[1]	6<8 + r>	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0 to 7
ADD A, @Rr[1]	6r	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((Rr))	r = 0, 1
ADD A, #data[1]	03 data	2/2	Add immediate data to A	(A)←(A) + data	
ADDC A, Rr[1]	7<8 + r>	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0 to 7
ADDC A, @Rr[1]	7r	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((Rr)) + (C)	r = 0, 1
ADDC A, #data[1]	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)	
ANL A, Rr	5<8 + r>	1/1	AND Rr with A	(A)←(A) AND (Rr)	r = 0 to 7
ANL A, @Rr	5r	1/1	AND RAM data addressed by Rr, with A	(A)←(A) AND ((Rr))	r = 0, 1
ANL A, #data	53 data	2/2	AND immediate data with A	(A)←(A) AND data	
ORL A, Rr	4<8 + r>	1/1	OR Rr with A	(A)←(A) OR (Rr)	r = 0 to 7
ORL A, @Rr	4r	1/1	OR RAM data, addressed by Rr, with A	(A)←(A) OR ((Rr))	r = 0, 1
ORL A, #data	43 data	2/2	OR immediate data with A	(A)←(A) OR data)	
XRL A, Rr	D<8 + r>	1/1	XOR Rr with A	(A)←(A) XOR (Rr)	r = 0 to 7
XRL A, @Rr	Dr	1/1	XOR RAM data, addressed by Rr, with A	(A)←(A) XOR ((Rr))	r = 0, 1
XRL A, #data	D3 data	2/2	XOR immediate data with A	(A)←(A) XOR data)	
INC A	17	1/1	Increment A by 1	(A)←(A) + 1	
DEC A	07	1/1	Decrement A by 1	(A)←(A) – 1	
CLR A	27	1/1	Clear A to zero	(A)←0	
CPL A	37	1/1	One's complement A	(A)←NOT(A)	
RL A	E7	1/1	Rotate A left	$(A_{n+1})\leftarrow(A_n)$, $(A_0)\leftarrow(A_7)$	n = 0 to 6
RLC A[2]	F7	1/1	Rotate A left through carry	$(A_{n+1})\leftarrow(A_n)$, $(A_0)\leftarrow(C)$, $(C)\leftarrow(A_7)$	n = 0 to 6
RR A	77	1/1	Rotate A right	$(A_n)\leftarrow(A_{n+1})$, $(A_7)\leftarrow(A_0)$	n = 0 to 6
RRC A[2]	67	1/1	Rotate A right through carry	$(A_n)\leftarrow(A_{n+1})$, $(A_7)\leftarrow(C)$, $(C)\leftarrow(A_0)$	n = 0 to 6
DA A[2]	57	1/1	Decimal adjust A	(A)←(A) + 06H if AC = 1 or $(A_{0-3})>9$; (A)←(A) + 60H if $(A_{4-7})>9$	
SWAP A[2]	47	1/1	Swap nibbles of A	$(A_{4-7})\leftrightarrow(A_{0-3})$	

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
Data moves					
MOV A, Rr	F<8 + r>	1/1	Move register contents to A	(A)←(Rr)	r = 0 to 7
MOV A, @Rr	Fr	1/1	Move RAM data addressed by Rr, to A	(A)←((Rr))	r = 0, 1
MOV A, #data	23 data	2/2	Move immediate data to A	(A)←data	
MOV Rr, A	A<8 + r>	1/1	Move Accumulator contents to register	(Rr)←(A)	r = 0 to 7
MOV@Rr, A	Ar	1/1	Move Accumulator contents to RAM location addressed by Rr	((Rr))←(A)	r = 0, 1
MOV Rr, #data	B<8 + r> data	2/2	Move immediate data to Rr	(Rr)←data	r = 0 to 7
MOV @Rr, #data	Br data	2/2	Move immediate data to RAM location addressed by Rr	((R0))←data	r = 0, 1
XCH A, Rr	2<8 + r>	1/1	Exchange A contents with Rr	(A)↔(Rr)	r = 0 to 7
XCH A, @Rr	2r	1/1	Exchange Accumulator contents with RAM data addressed by Rr	(A)↔((Rr))	r = 0, 1
XCHD A, @Rr	3r	1/1	Exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3})\leftrightarrow((Rr_{0-3}))$	r = 0, 1
MOV A, PSW	C7	1/1	Move PSW contents to Accumulator	(A)←(PSW)	
MOV PSW, A[3]	D7	1/1	Move Accumulator bit 3 to PSW_3 (PS)	$(PS)\leftarrow(A_3)$	
MOV P A, @A	A3	1/2	Move indirectly addressed data in current page to A	$(PC_{0-7})\leftarrow(A)$, (A)←((PC))	
Carry flag					
CLR C[2]	97	1/1	Clear carry bit	(C)←0	
CPL C[2]	A7	1/1	Complement carry bit	(C)←NOT(C)	
Register					
INC Rr	1<8 + r>	1/1	Increment register by 1	(Rr)←(Rr) + 1	r = 0 to 7
INC @Rr	1r	1/1	Increment RAM data, addressed by Rr, by 1	((Rr))←((Rr)) + 1	r = 0,1
DEC Rr	C<8 + r>	1/1	Decrement register by 1	(Rr)←(Rr) – 1	r = 0 to 7
DEC @Rr	Cr	1/1	Decrement RAM data addressed by Rr, by 1	((Rr))←((Rr)) – 1	r = 0, 1

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
Branch					
JMP addr	<2n>4 addr	2/2	Unconditional jump within a 2 kbyte bank	$(PC_{8-10}) \leftarrow n$ $(PC_{0-7}) \leftarrow addr$ $(PC_{11-12}) \leftarrow$ (MBFF0-1)	n = 0 to 7
JMPP @A	B3	1/2	Indirect jump within a page	$(PC_{0-7}) \leftarrow ((A))$	
DJZN Rr, addr	E<8 + r> addr	2/2	Decrement Rr by 1 and jump if not zero to addr	$(Rr) \leftarrow (Rr) - 1$; if (Rr) not zero, then $(PC_{0-7}) \leftarrow addr$	r = 0 to 7
DJNZ @Rr, addr	Er	2/2	Decrement RAM data, addressed by Rr, by 1 and jump if not zero to addr	$((Rr)) \leftarrow ((Rr)) - 1$; if ((Rr)) not zero, then $(PC_{0-7}) \leftarrow addr$	r = 0 to 1
JBb addr	<2b + 1> 2 addr	2/2	Jump to addr if Accumulator bit b = 1	If $(A_b) = 1$, then $(PC_{0-7}) \leftarrow addr$	b = 0 to 7
JC addr	F6 addr	2/2	Jump to addr if C = 1	If (C) = 1, then $(PC_{0-7}) \leftarrow addr$	
JNC addr	E6 addr	2/2	Jump to addr if C = 0	If (C) = 0, then $(PC_{0-7}) \leftarrow addr$	
JZ addr	C6 addr	2/2	Jump to addr if A = 0	If (A) = 0, $(PC_{0-7}) \leftarrow addr$	
JNZ addr	96 addr	2/2	Jump to addr if A is NOT zero	If (A) $\neq$ 0, then $(PC_{0-7}) \leftarrow addr$	
JT0 addr	36 addr	2/2	Jump to addr if T0 = 0	If T0 = 0, then $(PC_{0-7}) \leftarrow addr$	
JNT0 addr	26 addr	2/2	Jump to addr if T0 = 1	If T0 = 1, then $(PC_{0-7}) \leftarrow addr$	
JT1 addr	56 addr	2/2	Jump to addr if T1 = 1	If T1 = 1, then $(PC_{0-7}) \leftarrow addr$	
JNT1 addr	46 addr	2/2	Jump to addr if T1 = 0	If T0 = 0, then $(PC_{0-7}) \leftarrow addr$	
JTF addr[4]	16 addr	2/2	Jump to addr if Timer Flag = 1	If TF = 1, then $(PC_{0-7}) \leftarrow addr$	
JNTF addr[4]	06 addr	2/2	Jump to addr if Timer Flag = 0	If T0 = 0, then $(PC_{0-7}) \leftarrow addr$	

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
Timer/event counter					
MOV A,T	42	1/1	Move timer/event counter contents to A	(A)←(T)	
MOV T, A	62	1/1	Move A contents to timer/event counter	(T)←(A)	
STRT CNT	45	1/1	Start event counter		
STRT T	55	1/1	Start timer		
STOP TCNT	65	1/1	Stop timer/event counter		
EN TCNTI	25	1/1	Enable timer/event counter interrupt		
DIS TCNTI	35	1/1	Disable timer/event counter interrupt		
Control					
EN I	05	1/1	Enable external (chip enable) interrupt		
DIS I	15	1/1	Disable external (chip enable) interrupt		
SEL RB0[5]	C5	1/1	Select Register Bank 0	(RBS)←0	
SEL RB1[5]	D5	1/1	Select Register Bank 1	(RBS)←1	
SEL MB0[9]	E5	1/1	Select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
SEL MB1[9]	F5	1/1	Select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
SEL MB2[9]	A5	1/1	Select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
SEL MB3[9]	B5	1/1	Select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
STOP	22	1/1	Enter Stop mode		
IDLE	01	1/1	Enter Idle mode		
NOP	00	1/1	No operation		
Subroutine					
CALL addr[6]	<2n + 1> 4addr	2/2	Jump to subroutine	((SP))←(PC) ($PSW_{4,6,7}$), (SP)←(SP) + 1, (PC_{8-10})←n, (PC_{0-7})←addr, (PC_{11-12}) ←(MBFF0-1)	n = 0 to 7
RET[6]	83	1/2	Return from subroutine	(SP)←(SP) – 1, (PC)←((SP))	
RETR[6]	93	1/2	Return from interrupt and restore bits 4, 6 and 7 of PSW	(SP)←(SP) – 1, ($PSW_{4,6,7}$) + (PC)←((SP))	

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
Parallel input/output					
IN A, P0	08	1/2	Input Port 0 data to Accumulator	(A)←(P0)	
IN A, P1	09	1/2	Input Port 1 data to Accumulator	(A)←(P1)	
IN A, P2[7]	0A	1/2	Input Port 2 data to Accumulator	(A)←(P2)	
OUTL P0, A	38	1/2	Output A data to Port 0	(P0)←(A)	
OUTL P1, A	39	1/2	Output A data to Port 1	(P1)←(A)	
OUTL P2, A	3A	1/2	Output A data to Port 2	(P2)←(A)	
ANL P0, #data	98 data	2/2	AND Port 0 data with immediate data	(P0)←(P0) AND data	
ANL P1, #data	99 data	2/2	AND Port 1 data with immediate data	(P1)←(P1) AND data	
ANL P2, #data	9A data	2/2	AND Port 2 data with immediate data	(P2)←(P2) AND data	
ORL P0, #data	88 data	2/2	OR Port 0 data with immediate data	(P0)←(P0) OR data	
ORL P1, #data	89 data	2/2	OR Port 1 data with immediate data	(P1)←(P1) OR data	
ORL P2, #data	8A data	2/2	OR Port 2 data with immediate data	(P2)←(P2) OR data	
Derivative input/output					
MOV A, Dx[8]	8C direct	2/2	Move derivative register contents to A	(A)←(Dx)	x = 0 to 255
MOV Dx, A[8]	8D direct	2/2	Move A contents to derivative register	(Dx)←(A)	x = 0 to 255
ANL Dx, A[8]	8E direct	2/2	AND derivative register with A	(Dx)←(Dx) AND (A)	x = 0 to 255
ORL Dx, A[8]	8F direct	2/2	OR derivative register with A	(Dx)←(Dx) OR (A)	x = 0 to 255
EN SI	85	1/1	Enable derivative interrupt		
DIS SI	95	1/1	Disable derivative interrupt		

Notes to Table 5

1. PSW CY, AC affected.
2. PSW CY affected.
3. PSW PS affected.
4. Execution of a JTF or JNTF instruction resets the Timer Flag (TF).
5. PSW RBS affected.
6. PSW SP_0, SP_1 and SP_2, affected.
7. (A) = 0000, P2.3, P2.2, P2.1 and P2.0.
8. For more information on the derivative I/O instructions of a particular microcontroller, consult the specific microcontroller data sheet.
9. SEL MB instructions may not be used within interrupt routines.

Table 6 Definitions of symbols used in Table 5

SYMBOL	DESCRIPTION
A	Accumulator
AC	auxiliary (half) carry
addr	program memory address
Bb	bit designation (b = 0 to 7)
CE/$\overline{T0}$	CE/$\overline{T0}$ input
CY	carry bit
Dx	mnemonic derivative register
data	8-bit number or expression
MB0	program memory bank 0
MB1	program memory bank 1
MB2	program memory bank 2
MB3	program memory bank 3
MBFF0	memory bank flip-flop 0
MBFF1	memory bank flip-flop 1
PC	Program Counter
PS	timer prescaler select
PSW	Program Status Word
RB0	Register Bank 0
RB1	Register Bank 1
RBS	Register Bank Select
Rr	register designation (r = 0 to 7)
SPn	Stack Pointer (n = 0, 1 or 2)
T	Timer 1
T1	T1 input
TF	Timer Flag
x	derivative register address (x = 0 to 255)
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with
#	immediate data prefix
@	indirect address prefix
*	hexadecimal; 8...F selects R0...R7
&	hexadecimal; 0, 2, 4, 6, 8, A, C, E selects page 0...7 in JMP, i.e. $(PC_{8-10}) \leftarrow \&_{1-3}$
%	hexadecimal; 1, 3, 5, 7, 9, B, D, F selects page 0...7 in CALL, i.e. $(PC_{8-10}) \leftarrow \&_{1-3}$ selects bit b = 0...7 in JBb, i.e. $b = \&_{1-3}$

7.1 Instruction map

first hexadecimal character of opcode — second hexadecimal character of opcode

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A, #data	JMP page 0	EN I	JNTF addr	DEC A	0	IN A,Pp 1	2					
1	INC @ Rr 0	1	JB0 addr	ADDC A,#data	CALL page 0	DIS I	JTF addr	INC A	0	1	2	3	INC Rr 4	5	6	7
2	XCH A, @Rr 0	1	STOP	MOV A, #data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	0	1	2	3	XCH A,Rr 4	5	6	7
3	XCHD A, @Rr 0	1	JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	0	OUTL Pp,A 1	2					
4	ORL A, @Rr 0	1	MOV A, T	ORL A, #data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	0	1	2	3	ORL A,Rr 4	5	6	7
5	ANL A, @Rr 0	1	JB2 addr	ANL A, #data	CALL page 2	STRT T	JT1 addr	DA A	0	1	2	3	ANL A,Rr 4	5	6	7
6	ADD A, @Rr 0	1	MOV T, A		JMP page 3	STOP TCNT		RRC A	0	1	2	3	ADD A,Rr 4	5	6	7
7	ADDC A, @Rr 0	1	JB3 addr		CALL page 3			RR A	0	1	2	3	ADDC A,Rr 4	5	6	7
8				RET	JMP page 4	EN SI			0	ORL Pp,#data 1	2		MOV A,Dx	MOV Dx,A	ANL Dx,A	ORL Dx,A
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	0	ANL Pp,#data 1	2					
A	MOV @ Rr,A 0	1		MOVP A,@A	JMP page 5	SEL MB2		CPL C	0	1	2	MOV Rr,A 3	4	5	6	7
B	MOV @Rr, #data 0	1	JB5 addr	JMPP @A	CALL page 5	SEL MB3			0	1	2	MOV Rr,#data 3	4	5	6	7
C	DEC @Rr 0	1			JMP page 6	SEL RB0	JZ addr	MOV A,PSW	0	1	2	DEC Rr 3	4	5	6	7
D	XRL A, @Rr 0	1	JB6 addr	XRL A,#data	CALL page 6	SEL RB1		MOV PSW,A	0	1	2	XRL A,Rr 3	4	5	6	7
E	DJNZ @ Rr,addr 0	1			JMP page 7	SEL MB0	JNC addr	RL A	0	1	2	DJNZ Rr,addr 3	4	5	6	7
F	MOV A, @Rr 0	1	JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	0	1	2	MOV A,Rr 3	4	5	6	7

MGD566

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8-bit microcontrollers with DTMF generator, 8 kbytes OTP and 128 bytes EEPROM

PCD3755A; PCD3755E; PCD3755F

1 FEATURES

- 8-bit CPU, ROM, RAM, EEPROM and I/O; in a single 28-lead or 32-lead package
- 8 kbytes user-programmable ROM (One-Time Programmable)
- 128 bytes RAM
- 128 bytes Electrically Erasable Programmable Read-Only Memory (EEPROM)
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- 8-bit reloadable Timer 2
- Three single-level vectored interrupts:
  - external
  - 8-bit programmable Timer/event counter 1
  - derivative; triggered by reloadable Timer 2
- Two test inputs, one of which also serves as the external interrupt input
- DTMF, modem, musical tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT compatible)
- Melody output for ringer application
- Power-on-reset
- Stop and Idle modes
- Supply voltage: 1.8 to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- Clock frequency: 1 to 16 MHz (3.58 MHz for DTMF suggested)
- Operating temperature: –25 to +70 °C
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

This data sheet details the specific properties of the PCD3755A, PCD3755E and PCD3755F. The devices differ in their Port and Power-on-reset configurations. References to 'PCD3755x' apply to all three types.
The devices are members of the PCD33xxA family of microcontrollers.
The shared properties of the family are described in the *"PCD33xxA family"* data sheet, which should be read in conjunction with this publication.

The PCD3755A, PCD3755E and PCD3755F are One-Time Programmable (OTP) microcontrollers designed primarily for telephony applications.They include an on-chip generator for dual tone multifrequency (DTMF), modem and musical tones. In addition to dialling, generated frequencies can be made available as square waves (P1.7/MDY) for melody generation, providing ringer operation.

The PCD3755A, PCD3755E and PCD3755F also incorporate 128 bytes of EEPROM. The EEPROM can be used for storing telephone numbers, particularly for implementing redial functions.

The Power-on-reset circuitry is extra accurate to accommodate parallel telephones and fax equipment.

The instruction set is similar to that of the MAB8048 and is a sub-set of that listed in the *"PCD33xxA family"* data sheet.

3 ORDERING INFORMATION (see note 1)

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3755xP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3755xT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCD3755xH	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

Note

1. Please refer to the Order Entry Form (OEF) for this device for the full type number to use when ordering. This type number will also specify the required program and the ROM mask options.

4 BLOCK DIAGRAM

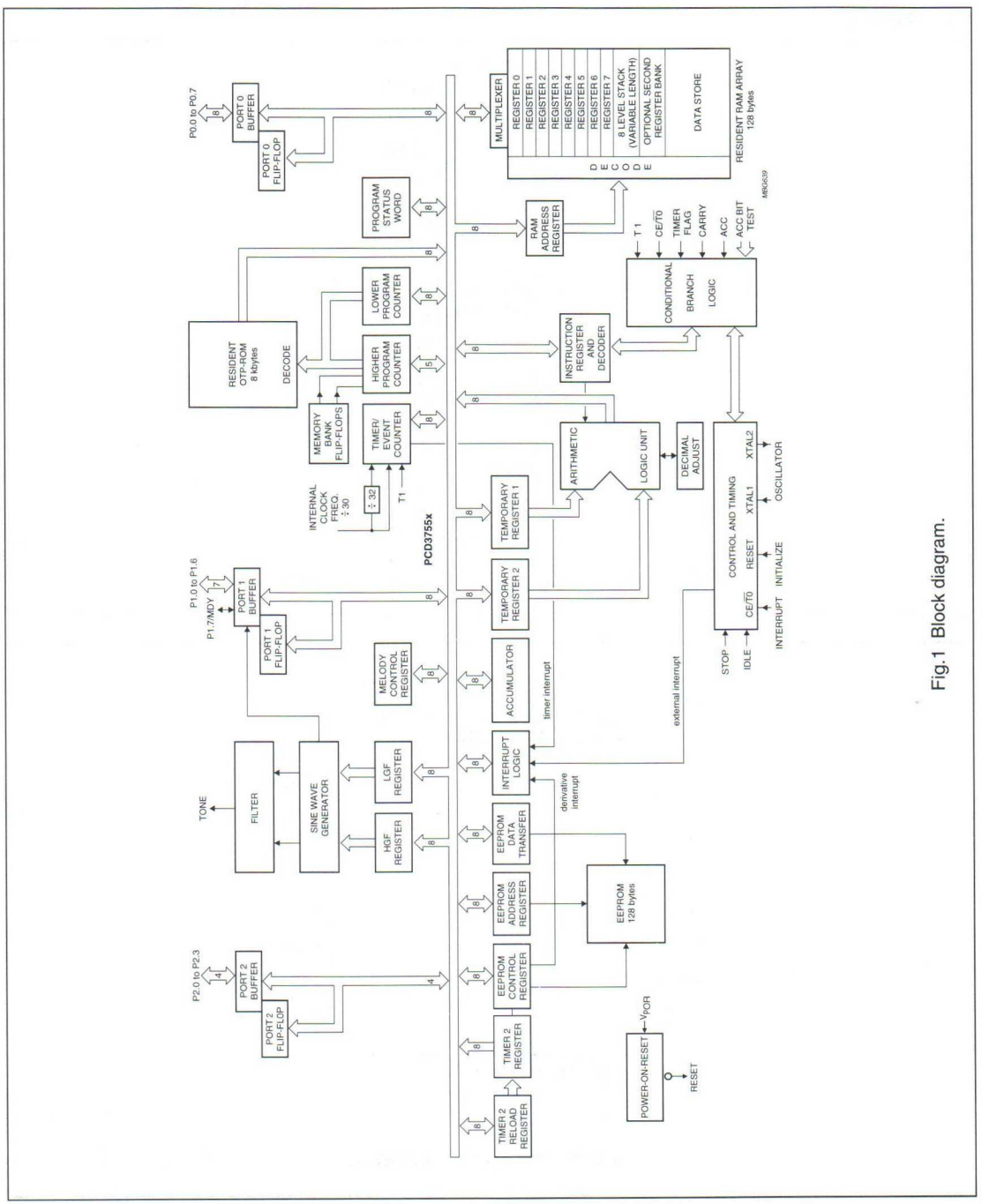


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

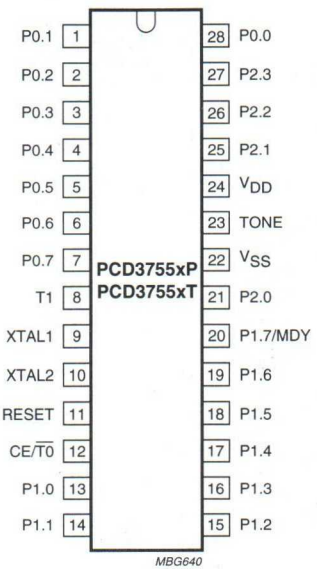


Fig.2 Pin configuration (SOT117-1 and SOT136-1).

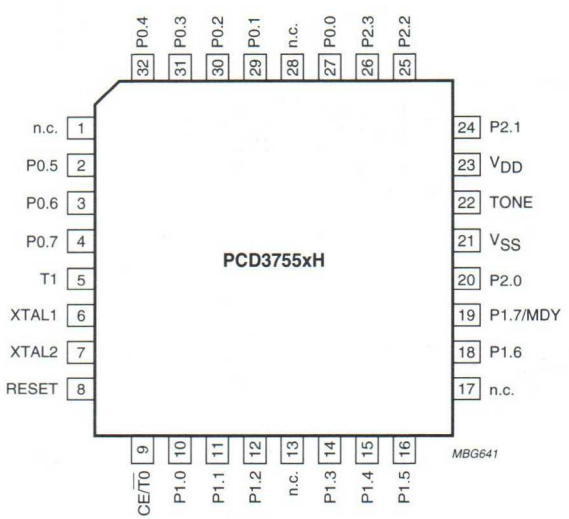


Fig.3 Pin configuration (SOT358-1).

5.2 Pin description

Table 1 SOT117-1 and SOT136-1 packages (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	TYPE	DESCRIPTION
P1.1 to P0.7	1 to 7	I/O	7 bits of Port 0: 8-bit quasi-bidirectional I/O port
T1	8	I	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	9	I	crystal oscillator or external clock input
XTAL2	10	O	crystal oscillator output
RESET	11	I	reset input
CE/$\overline{T0}$	12	I	Chip Enable or Test 0
P1.0 to P1.6	13 to 19	I/O	7 bits of Port 1: 8-bit quasi-bidirectional I/O port
P1.7/MDY	20	I/O	1 bit of Port 1: 8-bit quasi-bidirectional I/O port; or melody output
P2.0	21	I/O	1 bit of Port 2: 4-bit quasi-bidirectional I/O port
V_{SS}	22	P	ground
TONE	23	O	DTMF output
V_{DD}	24	P	positive supply voltage
P2.1 to P2.3	25 to 27	I/O	3 bits of Port 2: 4-bit quasi-bidirectional I/O port
P0.0	28	I/O	1 bit of Port 0: 8-bit quasi-bidirectional I/O port

Table 2 SOT358-1 package (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	TYPE	DESCRIPTION
n.c.	1, 13, 17, 28	–	not connected
P0.5 to P0.7	2 to 4	I/O	3 bits of Port 0: 8-bit quasi-bidirectional I/O port
T1	5	I	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	6	I	crystal oscillator or external clock input
XTAL2	7	O	crystal oscillator output
RESET	8	I	reset input
CE/$\overline{T0}$	9	I	Chip Enable or Test 0
P1.0 to P1.6	10 to 12, 14 to 16, 18	I/O	7 bits of Port 1: 8-bit quasi-bidirectional I/O port
P1.7/MDY	19	I/O	1 bit of Port 1: 8-bit quasi-bidirectional I/O port; or melody output
P2.0	20	I/O	1 bit of Port 2: 4-bit quasi-bidirectional I/O port
V_{SS}	21	P	ground
TONE	22	O	DTMF output
V_{DD}	23	P	positive supply voltage
P2.1 to P2.3	24 to 26	I/O	3 bits of Port 2: 4-bit quasi-bidirectional I/O port
P0.0 to P0.4	27, 29 to 32	I/O	5 bits of Port 0: 8-bit quasi-bidirectional I/O port

6 FREQUENCY GENERATOR

A versatile frequency generator section is provided (see Fig.4). For normal operation, use a 3.58 MHz quartz crystal or PXE resonator. The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets.

Their frequencies are provided in purely sinusoidal form on the TONE output or as square waves on the P1.7/MDY output.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available.

In case no tones are generated the TONE output is in 3-state mode.

6.1 Frequency generator derivative registers

6.1.1 High and Low Group Frequency registers

Table 3 gives the addresses, mnemonics and access types of the High Group Frequency (HGF) and Low Group Frequency (LGF) registers.

Table 3 Hexadecimal addresses, mnemonics, access types and bit mnemonics of the frequency registers

REGISTER ADDRESS	REGISTER MNEMONIC	ACCESS TYPE	BIT MNEMONICS							
			7	6	5	4	3	2	1	0
11H	HGF	W	H7	H6	H5	H4	H3	H2	H1	H0
12H	LGF	W	L7	L6	L5	L4	L3	L2	L1	L0

6.1.2 Melody Control Register (MDYCON)

MDYCON is a R/W register.

Table 4 Melody Control Register (address 13H)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	EMO

Table 5 Description of MDYCON bits

BIT	MNEMONIC	DESCRIPTION
7 to 1	–	These bits are set to a logic 0.
0	EMO	Enable Melody Output. If bit EMO = 0, then P1.7/MDY is a standard port line. If bit EMO = 1, then P1.7/MDY is the melody output. EMO = 1 does not inhibit the port instructions for P1.7/MDY. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by port instructions. However, the port flip-flop of P1.7/MDY must remain set to avoid conflicts between melody and port outputs. When the HGF contents are zero while EMO = 1, P1.7/MDY is in the logic HIGH state.

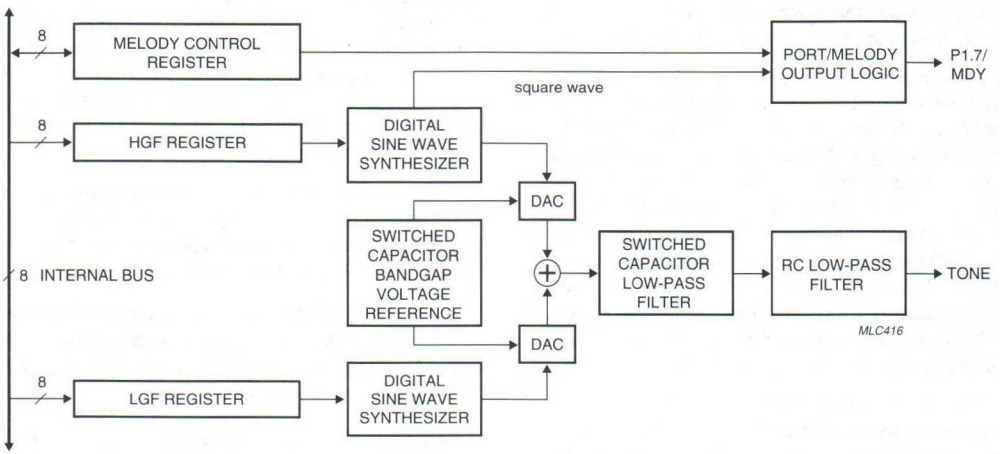


Fig.4 Block diagram of the frequency generator and melody output (P1.7/MDY) section.

6.2 Melody output (P1.7/MDY)

The melody output (P1.7/MDY) is very useful for generating musical tones when a purely sinusoidal signal is not required, such as for ringer applications.

The square wave (duty cycle = $^{12}/_{23}$ or 52%) will include the attenuated harmonics of the base frequency, which is defined by the contents of the HGF register (Table 3). However, even higher frequency tones may be produced since the low-pass filtering on the TONE output is not applied to the P1.7/MDY output. This results in the minimum decimal value x in the HGF register being 2 for the P1.7/MDY output, rather than 60 for the TONE output - the value shown in equation (1). A sinusoidal TONE output is produced at the same time as the melody square wave, but due to the filtering, the higher frequency sine waves with $x < 60$ will not appear at the TONE output.

Since the melody output is shared with P1.7, the port flip-flop of P1.7 has to be set HIGH before using the melody output. This is to avoid conflicts between melody and port outputs. The melody output drive depends on the configuration of port P1.7/MDY; see Chapter 14, Table 24.

6.3 Frequency registers

The two frequency registers HGF and LGF define two frequencies. From these, the digital sine synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures tone output levels independent of supply voltage and temperature.

The amplitude of the Low group frequency sine wave is attenuated by 2 dB compared to the amplitude of the High group frequency sine wave. The two sine waves are summed and then filtered by an on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

The value 00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption.

The frequency of the sine wave generated 'f' is dependent on the clock frequency 'f_{xtal}' and the decimal value 'x' held in the frequency registers (HGF and LGF). The variables are related by the equation:

$$f = \frac{f_{xtal}}{[23\,(x+2)\,]} \quad \text{where} \quad 60 \leq x \leq 255 \qquad (1)$$

The frequency limitation given by $x \geq 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

6.4 DTMF frequencies

Assuming an oscillator frequency f_{xtal} = 3.58 MHz, the DTMF standard frequencies can be implemented as shown in Table 6.

The relationships between telephone keyboard symbols, DTMF frequency pairs and the frequency register contents are given in Table 7.

Table 6 DTMF standard frequencies and their implementation; value = LGF, HGF contents

VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 7 Dialling symbols, corresponding DTMF frequency pairs and frequency register contents

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
•	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

6.5 Modem frequencies

Again assuming an oscillator frequency f_{xtal} = 3.58 MHz, the standard modem frequencies can be implemented as in Table 8. It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling Low Group Frequency generation.

Table 8 Standard modem frequencies and their implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980[1]	978.82	−0.12	−1.18
82	1180[1]	1179.03	−0.08	−0.97
8F	1070[2]	1073.33	0.31	3.33
79	1270[2]	1265.30	−0.37	−4.70
80	1200[3]	1197.17	−0.24	−2.83
45	2200[3]	2192.01	−0.36	−7.99
76	1300[4]	1296.94	−0.24	−3.06
48	2100[4]	2103.14	0.15	3.14
5C	1650[1]	1655.66	0.34	5.66
52	1850[1]	1852.77	0.15	2.77
4B	2025[2]	2021.20	−0.19	−3.80
44	2225[2]	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

6.6 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{xtal} = 3.58 MHz (Table 9). It is suggested to define the frequency by the HGF register while the LGF contains 00H, disabling Low Group Frequency generation.

Table 9 Musical scale frequencies and their implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD[1]	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 @ 440 Hz.

7 EEPROM AND TIMER 2 ORGANIZATION

The PCD3755A, PCD3755E and PCD3755F have 128 bytes of Electrically Erasable Programmable Read-Only Memory (EEPROM). Such non-volatile storage provides data retention without the need for battery backup. In telecom applications, the EEPROM is used for storing redial numbers and for short dialling of frequently used numbers. More generally, EEPROM may be used for customizing microcontrollers, such as to include a PIN code or a country code, to define trimming parameters, to select application features from the range stored in ROM.

The most significant difference between a RAM and an EEPROM is that a bit in EEPROM, once written to a logic 1, cannot be cleared by a subsequent write operation. Successive write accesses actually perform a logical OR with the previously stored information. Therefore, to clear a bit, the whole byte must be erased and re-written with the particular bit cleared. Thus, an erase-and-write operation is the EEPROM equivalent of a RAM write operation.

Whereas read access times to an EEPROM are comparable to RAM access times, write and erase accesses are much slower at 5 ms each. To make these operations more efficient, several provisions are available in the PCD3755A, PCD3755E and PCD3755F.

First, the EEPROM array is structured into 32 four-byte pages (see Fig.5) permitting access to 4 bytes in parallel (write page, erase/write page and erase page). It is also possible to erase and write individual bytes. Finally, the EEPROM address register provides auto-incrementing, allowing very efficient read and write accesses to sequential bytes.

To simplify the erase and write timing, the derivative 8-bit down-counter (Timer 2) with reload register is provided. In addition to EEPROM timing, Timer 2 can be used for general real-time tasks, such as for measuring signal duration and for defining pulse widths.

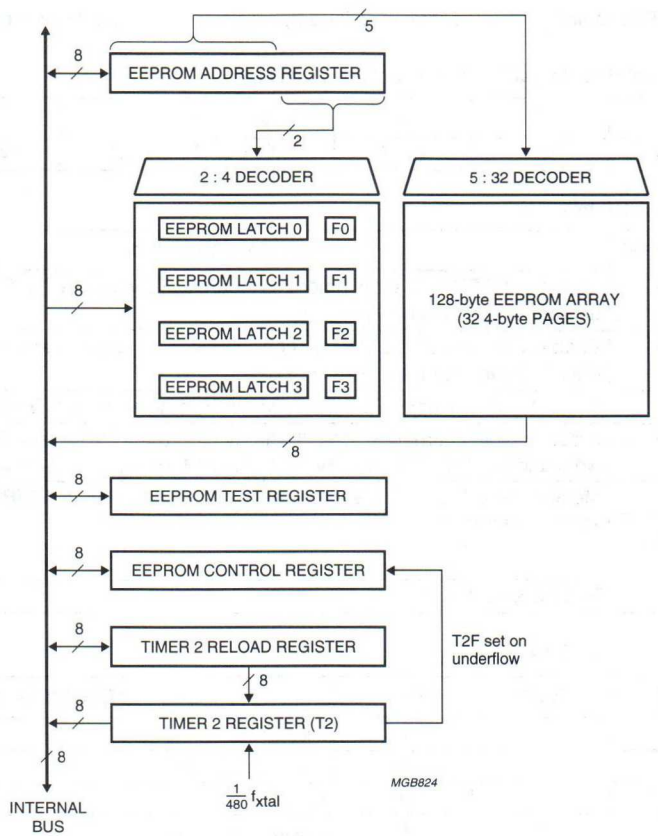


Fig.5 Block diagram of the EEPROM and Timer 2.

7.1 EEPROM registers

7.1.1 EEPROM Control Register (EPCR)

The behaviour of the EEPROM and Timer 2 section is defined by the EEPROM Control Register.

Table 10 EEPROM Control Register (address 04H, access type R/W)

7	6	5	4	3	2	1	0
STT2	ET2I	T2F	EWP	MC3	MC2	MC1	0

Table 11 Description of EPCR bits

BIT	MNEMONIC	DESCRIPTION
7	STT2	Start T2. If STT2 = 0, then Timer 2 is stopped; T2 value held. If STT2 = 1, then T2 decrements from reload value.
6	ET2I	Enable T2 interrupt. If ET2I = 0, then T2F event cannot request interrupt. If ET2I = 1, then T2F event can request interrupt.
5	T2F	Timer 2 flag. Set when T2 underflows (or by program); reset by program.
4	EWP	Erase or write in progress (EWP). Set by program (EWP starts EEPROM erase and/or write and Timer 2). Reset at the end of EEPROM erase and/or write.
3	MC3	Mode control 3 to 1. These three bits in conjunction with bit EWP select the mode as shown in Table 12.
2	MC2	
1	MC1	
0	–	This bit is set to a logic 0.

Table 12 Mode selection; X = don't care

EWP	MC3	MC2	MC1	DESCRIPTION
0	0	0	0	read byte
0	0	1	0	increment mode
1	0	1	X	write page
1	1	0	0	erase/write page
1	1	1	1	erase page
X	0	0	1	not allowed
X	1	0	1	
X	1	1	0	

7.1.2 EEPROM ADDRESS REGISTER (ADDR)

The EEPROM Address Register determines the EEPROM location to which an EEPROM access is directed.

As a whole, ADDR auto-increments after read and write cycles to EEPROM, but remains fixed after erase cycles. This behaviour generates the correct ADDR contents for sequential read accesses and for sequential write or erase/write accesses with intermediate page setup. Overflow of the 8-bit counter wraps around to zero.

Table 13 EEPROM Address Register (address 01H, access type R/W)

7	6	5	4	3	2	1	0
0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 14 Description of ADDR bits

BIT	MNEMONIC	DESCRIPTION
7	–	This bit is set to a logic 0.
6 to 2	AD6 to AD2	AD2 to AD6 select one of 32 pages.
1 to 0	AD1 to AD0	AD1 and AD0 are irrelevant during erase and write cycles. For read accesses, AD0 and AD1 indicate the byte location within an EEPROM page. During page setup, finally, AD0 and AD1 select EEPROM Latch 0 to 3 whereas AD2 to AD6 are irrelevant. If increment mode (Table 12) is active during page setup, the subcounter consisting of AD0 and AD1 increments after every write to an EEPROM latch, thus enhancing access to sequential EEPROM latches. Incrementing stops when EEPROM Latch 3 is reached, i.e. when AD0 and AD1 are both a logic 1.

7.1.3 EEPROM DATA REGISTER (DATR)

Table 15 EEPROM Data Register (address 03H; access type R/W)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 16 Description of DATR bits

BIT	MNEMONIC	DESCRIPTION
7 to 0	D7 to D0	The EEPROM Data Register (DATR) is only a conceptual entity. A read operation from DATR, reads out the EEPROM byte addressed by ADDR. On the other hand, a write operation to DATR, loads data into the EEPROM latch (see Fig.5) defined by bits AD0 and AD1 of ADDR.

7.1.4 EEPROM TEST REGISTER (TST)

The EEPROM Test register is used for testing purposes during device manufacture. It must not be accessed by the device user.

7.2 EEPROM latches

The four EEPROM latches (EEPROM Latch 0 to 3; Fig.5) cannot be read by user software. Due to their construction, the latches can only be preset, but not cleared. Successive write operations through DATR to the EEPROM latches actually perform a logical OR with the previously stored data in EEPROM. The EEPROM latches are reset at the conclusion of any EEPROM cycle.

7.3 EEPROM flags

The four EEPROM flags (F0 to F3; Fig.5) cannot be directly accessed by user software. An EEPROM flag is set as a side-effect when the corresponding EEPROM latch is written through DATR. The EEPROM flags are reset at the conclusion of any EEPROM cycle.

7.4 EEPROM macros

The instruction sequence used in an EEPROM access should be treated as an indivisible entity. Erroneous programs result if ADDR, DATR, RELR or EPCR are inadvertently changed during an EEPROM cycle or its setup. Special care should be taken if the program may asynchronously divert due to an interrupt. Particularly, a new access to the EEPROM may only be initiated when no write, erase or erase/write cycles are in progress. This can be verified by reading bit EWP (register EPCR).

For write, erase and erase/write cycles, it is assumed that the Timer 2 Reload Register (RELR) has been loaded with the appropriate value for a 5 ms delay, which depends on f_{xtal} (see Table 23). The end of a write, erase or erase/write cycle will be signalled by a cleared EWP and by a Timer 2 interrupt provided that ET2I = 1 and that the derivative interrupt is enabled.

7.5 EEPROM access

One read, one write, one erase/write and one erase access are defined by bits EWP and MC1 to MC3 in the EPCR register; see Table 10.

Read byte retrieves the EEPROM byte addressed by ADDR when DATR is read. Read cycles are instantaneous.

Write and erase cycles take 5 ms, however. Erase/write is a combination of an erase and a subsequent write cycle, consequently taking 10 ms.

As their names imply, **write page, erase page and erase/write page** are applied to a whole EEPROM page. Therefore, bits AD0 and AD1 of register ADDR (see Table 13), defining the byte location within an EEPROM page, are irrelevant during write and erase cycles. However, write and erase cycles need not affect all bytes of the page. The EEPROM flags F0 to F3 (see Fig.5) determine which bytes within the EEPROM page are affected by the erase and/or write cycles. A byte whose corresponding EEPROM flag is zero remains unchanged.

With erase page, a byte is erased if its corresponding EEPROM flag is set. With write page, data in EEPROM Latch 0 to 3 (Fig.5) are ORed to the individual page bytes if and only if the corresponding EEPROM flags are set.

In an erase/write cycle, F0 to F3 select which page bytes are erased and ORed with the corresponding EEPROM latches.

ORing, in this event, means that the EEPROM latches are copied to the selected page bytes.

The described page-wise organization of erase and write cycles allows up to four bytes to be individually erased or written within 5 ms. This advantage necessitates a preparation step, called **page setup**, before the actual erase and/or write cycle can be executed.

Page setup controls EEPROM latches and EEPROM flags. This will be described in the Sections 7.5.1 to 7.5.5.

7.5.1 PAGE SETUP

Page setup is a preparation step required before write page, erase page and erase/write page cycles.
As previously described, these page operations include single-byte write, erase and erase/write as a special event. EEPROM flags F0 to F3 determine which page bytes will be affected by the mentioned page operations. EEPROM Latch 0 to 3 must be preset through DATR to specify the write cycle data to EEPROM and to set the EEPROM flags as a side-effect. Obviously, the actual preset value of the EEPROM latches is irrelevant for erase page. Preset of one, two, three or all four EEPROM latches and the corresponding EEPROM flags can be performed by repeatedly defining ADDR and writing to DATR (see Table 17).

If more than one EEPROM latch must be preset, the subcounter consisting of AD0 and AD1 can be induced to auto-increment after every write to DATR, thus stepping through all EEPROM latches. For this purpose, increment mode (Table 12) must be selected. Auto-incrementing stops at EEPROM Latch 3. It is not mandatory to start at EEPROM Latch 0 as in shown in Table 18.

Note that AD2 to AD6 are irrelevant during page setup. They will usually specify the intended EEPROM page, anticipating the subsequent page cycle.

From now on, it will be assumed that AD2 to AD6 will contain the intended EEPROM page address after page setup.

Table 17 Page setup; preset

INSTRUCTION	RESULT
MOV A, #addr	address of EEPROM latch
MOV ADDR, A	send address to ADDR
MOV A, #data	load write, erase/write or erase data
MOV DATR, A	send data to addressed EEPROM latch

Table 18 Page setup; auto-incrementing

INSTRUCTION	RESULT
MOV A, #MC2	increment mode control word
MOV EPCR, A	select increment mode
MOV A, #baddr	EEPROM Latch 0 address (AD0 = AD1 = 0)
MOV ADDR, A	send EEPROM Latch 0 address to ADDR
MOV A, R0	load 1st byte from Register 0
MOV DATR, A	send 1st byte to EEPROM Latch 0
MOV A, R1	load 2nd byte from Register 1
MOV DATR, A	send 2nd byte to EEPROM Latch 1
MOV A, R2	load 3rd byte from Register 2
MOV DATR, A	send 3rd byte to EEPROM Latch 2
MOV A, R3	load 4th byte from Register 3
MOV DATR, A	send 4th byte to EEPROM Latch 3

7.5.2 Read byte

Since ADDR auto-increments after a read cycle regardless of the page boundary, successive bytes can efficiently be read by repeating the last instruction.

Table 19 Read byte

INSTRUCTION	RESULT
MOV A, #RDADDR	load read address
MOV ADDR, A	send address to ADDR
MOV A, DATR	read EEPROM data

7.5.3 Write page

The write cycle performs a logical OR between the data in the EEPROM latches and that in the addressed EEPROM page.

To actually copy the data from the EEPROM latches, the corresponding bytes in the page should previously have been erased.

The EEPROM latches are preset as described in Section 7.5.1. The actual transfer to the EEPROM is then performed as shown in Table 20.

The last instruction also starts Timer 2. The data in the EEPROM latches are ORed with that in the corresponding page bytes within 5 ms. A single-byte write is simply a special case of 'write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by bits AD2 to AD6) and to EEPROM Latch 0 (by bits AD0 and AD1). This allows efficient coding of multi-page write operations.

Table 20 Write page

INSTRUCTION	RESULT
MOV A, #EWP + MC2	'write page' control word
MOV EPCR, A	start 'write page' cycle

7.5.4 Erase/write page

The EEPROM latches are preset as described in Section 7.5.1. The page byte corresponding to the asserted flags (among F0 to F3) are erased and re-written with the contents of the respective EEPROM latches.

The last instruction also starts Timer 2. Erasure takes 5 ms upon which Timer Register T2 reloads for another 5 ms cycle for writing. The top cycles together take 10 ms. A single-byte erase/write is simply a special event of 'erase/write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by AD2 to AD6) and to EEPROM Latch 0 (by AD0 and AD1). This allows efficient coding of multi-page erase/write operations.

Table 21 Erase/write page

INSTRUCTION	RESULT
MOV A, #EWP + MC3	'erase/write page' control word
MOV EPCR, A	start 'erase/write page' cycle

7.5.5 ERASE PAGE

The EEPROM flags are set as described in Section 7.5.1. The corresponding page bytes are erased.

The last instruction also starts Timer 2. Erasure takes 5 ms. A single-byte erase is simply a special case of 'erase page'.

Note that ADDR does not auto-increment after an erase cycle.

Table 22 Erase page

INSTRUCTION	RESULT
MOV A, #EWP + MC3 + MC2 + MC1	'erase page' control word
MOV EPCR, A	start 'erase page' cycle

7.6 Timer 2

Timer 2 is a 8-bit down-counter decremented at a rate of $1/480 \times f_{xtal}$. It may be used either for EEPROM timing or as a general purpose timer. Conflicts between the two applications should be carefully avoided.

7.6.1 TIMER 2 FOR EEPROM TIMING

When used for EEPROM timing, Timer 2 serves to generate the 5 ms intervals needed for erasing or writing the EEPROM. At the decrement rate of $1/480 \times f_{xtal}$, the reload value for a 5 ms interval is a function of f_{xtal}. Table 23 summarizes the required reload values for a number of oscillator frequencies.

Timer 2 is started by setting bit EWP in the EPCR. The Timer Register T2 is loaded with the reload value from RELR. T2 decrements to zero.

For an erase/write cycle, underflow of T2 indicates the end of the erase operation. Therefore, Timer Register T2 is reloaded from RELR for another 5 ms interval during which the flagged EEPROM latches are copied to the corresponding bytes in the page addressed by ADDR.

The second underflow of an erase/write cycle and the first underflow of write page and erase page conclude the corresponding EEPROM cycle. Timer 2 is stopped, T2F is set whereas EWP and MC1 to MC3 are cleared.

Table 23 Reload values as a function of f_{xtal}

f_{xtal} (MHz)	RELOAD VALUE[1] (HEX)
1	0A
2	14
3.58	25
6	3E
10	68
16	A6

Note

1. The reload value is $(5 \times 10^{-3} \times 1/480 \times f_{xtal}) - 1$; f_{xtal} in MHz.

7.6.2 TIMER 2 AS A GENERAL PURPOSE TIMER

When used for purposes other than EEPROM timing, Timer 2 is started by setting STT2. The Timer Register T2 (see Table 26) is loaded with the reload value from RELR. T2 decrements to zero. On underflow, T2 is reloaded from RELR, T2F is set and T2 continues to decrement.

Timer 2 can be stopped at any time by clearing STT2. The value of T2 is then held and can be read out. After setting STT2 again, Timer 2 decrements from the reload value. Alternatively, it is possible to read T2 'on the fly' i.e. while Timer 2 is operating.

8 DERIVATIVE INTERRUPTS

One derivative interrupt event is defined. It is controlled by bits T2F and ET2I in the EPCR (see Tables 10 and 11).

The derivative interrupt event occurs when T2F is set. This request is honoured under the following circumstances:

- No interrupt routine proceeds
- No external interrupt request is pending
- The derivative interrupt is enabled
- ET2I is set.

The derivative interrupt routine must include instructions that will remove the cause of the derivative interrupt by explicitly clearing T2F. If the derivative interrupt is not used, T2F may directly be tested by the program. Obviously, T2F can also be asserted under program control, e.g. to generate a software interrupt.

9 TIMING

Although thePCD3755A, PCD3755E and PCD3755F operate over a clock frequency range from 1 to 16 MHz, f_{xtal} = 3.58 MHz will usually be chosen to take full advantage of the frequency generator section.

10 RESET

In addition to the conditions given in the *"PCD33xxA Family"* data sheet, all derivative registers are cleared in the reset state.

11 IDLE MODE

In Idle mode, the frequency generator, the EEPROM and the Timer 2 sections remain operative. Therefore, the IDLE instruction may be executed while an erase and/or write access to EEPROM is in progress.

12 STOP MODE

Since the oscillator is switched off, the frequency generator, the EEPROM and the Timer 2 sections receive no clock. It is suggested to clear both the HGF and the LGF registers before entering Stop mode. This will cut off the biasing of the internal amplifiers, considerably reducing current requirements.

The Stop mode **must not** be entered while an erase and/or write access to EEPROM is in progress. The STOP instruction may only be executed when EWP in EPCR is zero. The Timer 2 section is frozen during Stop mode. After exit from Stop mode by a HIGH level on $CE/\overline{T0}$, Timer 2 proceeds from the held state.

13 INSTRUCTION SET RESTRICTIONS

As RAM space is restricted to 128 bytes, care should be taken to avoid accesses to non-existing RAM locations.

14 OVERVIEW OF PORT AND POWER-ON-RESET CONFIGURATION

Table 24 Port and Power-on-reset configuration

See note 1 and 2.

TYPE	PORT 0								PORT 1								PORT 2				V_{POR}
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	
PCD3755A	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1R	1R[3]	2S	2S	2S	2S	1.3 V
PCD3755E	1S	1S	1S	1S	1S	1S	1S	1S	2S	2S	2S	2S	2S	2S	1S	1S[3]	2S	1R	1R	1R	2.0 V
PCD3755F	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1R	1R[3]	2S	2S	2S	2S	2.0 V

Notes

1. Port output drive: 1 = standard I/O; 2 = open-drain I/O, see *"PCD33xxA Family"* data sheet.
2. Port state after reset: S = Set (HIGH) and R = Reset (LOW).
3. The Melody Output drive type is push-pull.

15 OTP PROGRAMMING

The programming of the PCD3755x and PCD3756x OTPs is based on the OM4260 programmer (Ceibo MP-51), available from Philips. The OM4260 works in conjunction with various adapters supporting the different package types available as listed in Table 25.

The low-voltage OTP program memory used is of Anti-Fuse-PROM type and can not be erased after programming.

Thus, the complete OTP memory cannot be tested by the factory, but only partially via a special test array. The average expected yield is 97%.

Detailed information on the OTP programming is available in the *"PCD3755x Application Note"*, which is available via your Philips Sales office.

Table 25 OTP programming overview

DEVICE	PHILIPS TYPE NUMBER	CEIBO TYPE NUMBER	SUPPORTED PACKAGE
Ceibo MP-51	OM4260	MP-51 programmer base	–
PCD3755x/56x	OM5007	PCD3755A / 56A adapter DIP	DIP28
PCD3755x/56x	OM5030	PCD3755A / 56A adapter SO	SO28
PCD3755x/56x	OM5037(1)	PCD3755A / 56A adapter QFP32	LQFP32

Note

1. As the OM5037 is only a socket converter, the OM5007 is also needed to program the PCD3755x/56x in the LQFP32 package.

16 SUMMARY OF DERIVATIVE REGISTERS

Table 26 Register map

ADDR. (HEX)	REGISTER	7	6	5	4	3	2	1	0	R/W
00	not used									
01	EEPROM Address Register (ADDR)	0	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/W
02	not used									
03	EEPROM Data Register (DATR)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
04	EEPROM Control Register (EPCR)	STT2	ET21	TF2	EWP	MC3	MC2	MC1	0	R/W
05	Timer 2 Reload Register (RELR)	R7	R6	R5	R4	R3	R2	R1	R0	R/W
06	Timer 2 Register (T2)	T2.7	T2.6	T2.5	T2.4	T2.3	T2.2	T2.1	T2.0	R
07	Test Register (TST)	only for test purposes; not to be accessed by the device user								
08 to 10	not used									
11	High Group Frequency Register (HGF)	H7	H6	H5	H4	H3	H2	H1	H0	W
12	Low Group Frequency Register (LGF)	L7	L6	L5	L4	L3	L2	L1	L0	W
13	Melody Control Register (MDYCON)	0	0	0	0	0	0	0	EMO	R/W
14 to FF	not used									

17 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Data Handbook IC14, Section: Handling MOS devices"*).

18 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+7.0	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	−	125	mW
P_O	power dissipation per output	−	30	mW
I_{SS}	ground supply current	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	−	90	°C

19 DC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	see Fig.6				
	operating	note 1	1.8	–	6	V
	RAM data retention in Stop mode		1.0	–	6	V
I_{DD}	operating supply current	see Figs 7 and 8; note 2				
		V_{DD} = 3 V; value HGF or LGF ≠ 0	–	0.8	1.6	mA
		V_{DD} = 3 V	–	0.35	0.7	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.5	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	2.4	6.0	mA
$I_{DD(idle)}$	supply current (Idle mode)	see Figs 9 and 10; note 2				
		V_{DD} = 3 V; value HGF or LGF ≠ 0	–	0.7	1.4	mA
		V_{DD} = 3 V	–	0.25	0.5	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.1	3.4	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	1.7	5.0	mA
$I_{DD(stp)}$	supply current (Stop mode)	see Fig.11; note 3				
		V_{DD} = 1.8 V; T_{amb} = 25 °C	–	1.0	5.5	µA
		V_{DD} = 1.8 V; T_{amb} = 70 °C	–	–	10	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	−1	–	+1	µA
Port outputs						
I_{OL}	LOW level port sink current	V_{DD} = 3 V; V_O = 0.4 V; see Fig.12	0.7	3.5	–	mA
I_{OH}	HIGH level pull-up output source current	V_{DD} = 3 V; V_O = 2.7 V; see Fig.13	−10	−30	–	µA
		V_{DD} = 3 V; V_O = 0 V; see Fig.13	–	−140	−300	µA
I_{OH1}	HIGH level push-pull output source current	V_{DD} = 3 V; V_O = 2.6 V; see Fig.14	−0.7	−3.5	–	mA
Tone output (see Fig.15; note 4)						
$V_{HG(RMS)}$	HGF voltage (RMS)		158	181	205	mV
$V_{LG(RMS)}$	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		−0.6	–	+0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_o \rvert$	output impedance		–	100	500	Ω
G_v	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	T_{amb} = 25 °C; note 5	–	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EEPROM (notes 1 and 6)						
$CY_{t/w}$	endurance (erase/write cycles)	note 7	10^5	–	–	
t_{ret}	data retention time		10	–	–	years
Power-on-reset (see Fig.16)						
V_{POR}	Power-on-reset level					
	PCD3755A		0.8	1.3	1.8	V
	PCD3755E		1.5	2.0	2.5	V
	PCD3755F		1.5	2.0	2.5	V
Oscillator (see Fig.17)						
g_m	transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

Notes

1. TONE output, EEPROM erase and write require $V_{DD} \geq 2.5$ V.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open; value HGF = LGF = 0, unless otherwise specified.
   a) Maximum values: external clock at XTAL1 and XTAL2 open-circuit.
   b) Typical values: T_{amb} = 25 °C; crystal connected between XTAL1 and XTAL2.
3. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; RESET, T1 and CE/T0 at V_{SS}; crystal connected between XTAL1 and XTAL2; pins T1 and $\overline{CE}/T0$ at V_{SS}.
4. Values are specified for DTMF frequencies only (CEPT).
5. Related to the Low Group Frequency (LGF) component (CEPT).
6. After final testing the value of each EEPROM bit is a logic 1, but this cannot be guaranteed after board assembly.
7. Verified on sampling basis.

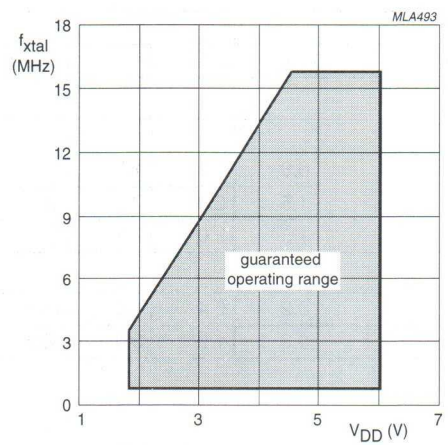
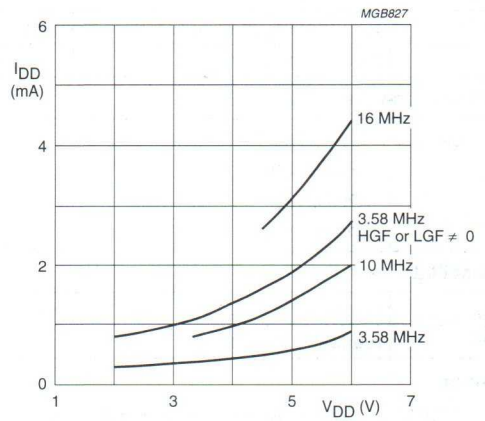
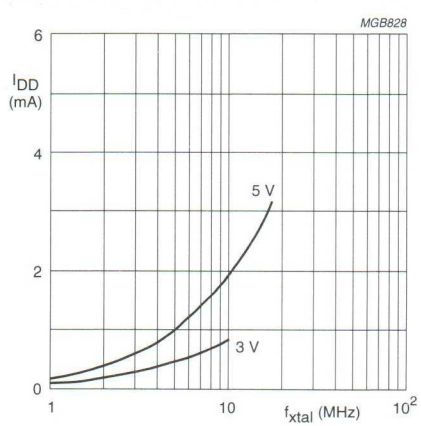


Fig.6 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).



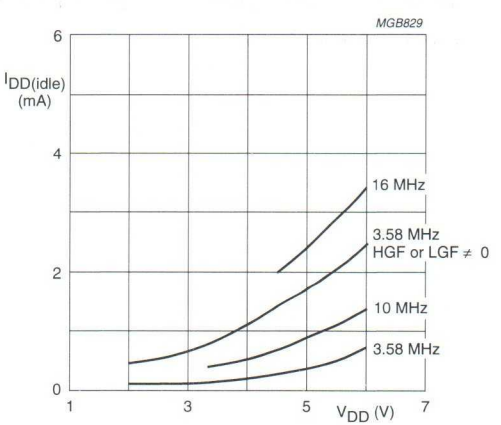
Measured with crystal between XTAL1 and XTAL2.

Fig.7 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).



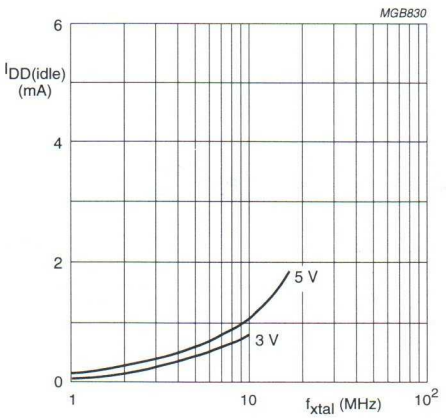
Measured with function generator on XTAL1.

Fig.8 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



Measured with crystal between XTAL1 and XTAL2.

Fig.9 Typical supply current in Idle mode ($I_{DD(idle)}$) as a function of supply voltage (V_{DD}).



Measured with function generator on XTAL1.

Fig.10 Typical supply current in Idle mode ($I_{DD(idle)}$) as a function of clock frequency (f_{xtal}).

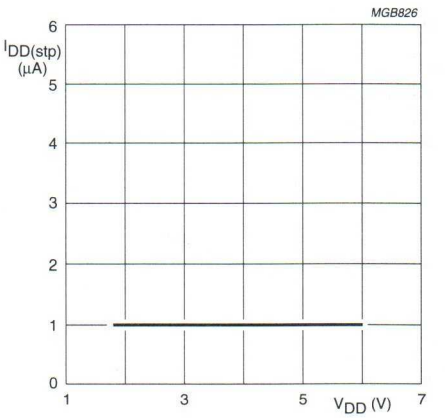
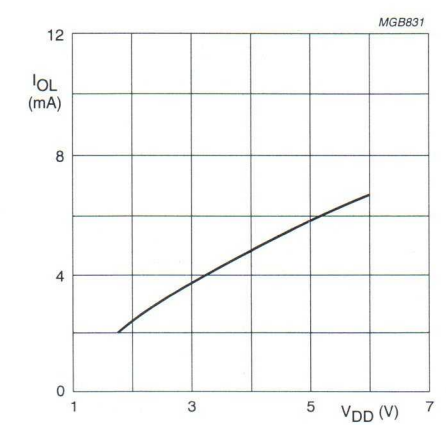


Fig.11 Typical supply current in Stop mode ($I_{DD(stp)}$) as a function of supply voltage (V_{DD}).



V_O = 0.4 V.

Fig.12 Typical LOW level output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

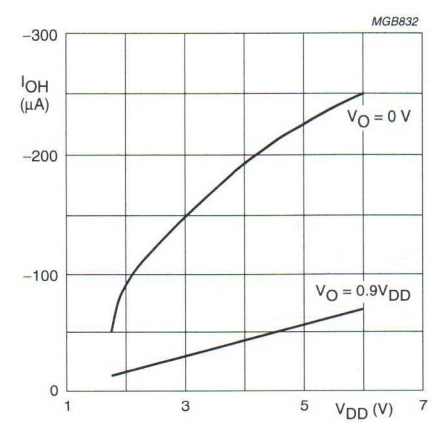
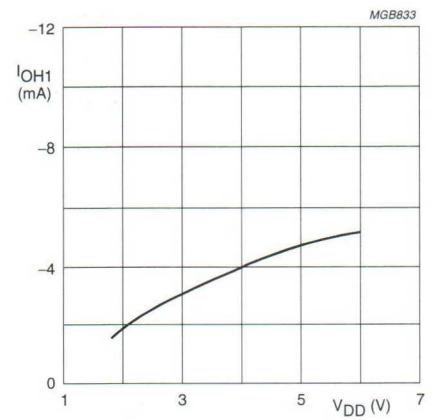
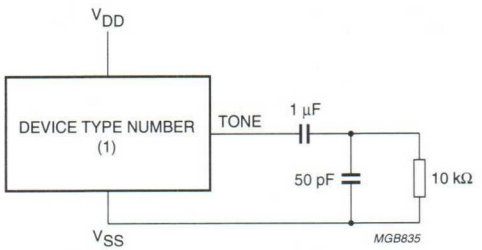


Fig.13 Typical HIGH level pull-up output source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.14 Typical HIGH level push-pull output source current (I_{OH1}) as a function of supply voltage (V_{DD}).



(1) Device type number: PCD3755A, PCD3755E or PCD3755F.

Fig.15 TONE output test circuit.

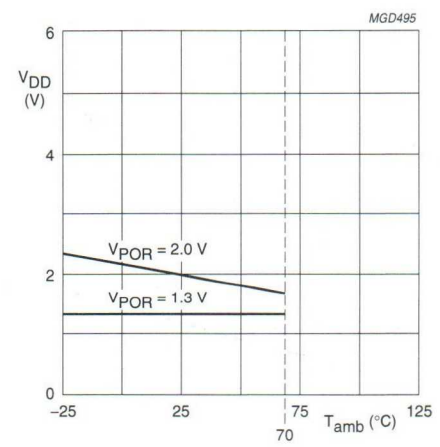


Fig.16 Typical Power-on-reset level (V_{POR}) as function of ambient temperature (T_{amb}).

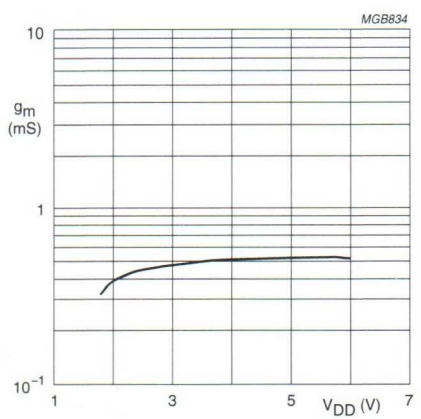


Fig.17 Typical transconductance (g_m) as a function of supply voltage (V_{DD}).

20 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.6	1	–	16	MHz

8-bit microcontroller with DTMF generator, 8 kbytes OTP and 128 bytes EEPROM

PCD3756A

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8-bit microcontroller with DTMF generator, 8 kbytes OTP and 128 bytes EEPROM

PCD3756A

1 FEATURES

- 8-bit CPU, ROM, RAM, EEPROM and I/O; in a single 28-lead or 32-lead package
- 8 kbytes user-programmable ROM (One-Time Programmable)
- 128 bytes RAM
- 128 bytes Electrically Erasable Programmable Read-Only Memory (EEPROM)
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- 8-bit reloadable Timer 2
- Three single-level vectored interrupts:
  - external
  - 8-bit programmable Timer/event counter 1
  - derivative; triggered by reloadable Timer 2
- Wake-up via external or Port 0 interrupt
- Two test inputs, one of which also serves as the external interrupt input
- DTMF, modem, musical tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT compatible)
- Melody output for ringer application
- Power-on-reset
- Stop and Idle modes
- Supply voltage: 1.8 to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- Clock frequency: 1 to 16 MHz (3.58 MHz for DTMF suggested)
- Operating ambient temperature: −25 to +70 °C
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

This data sheet details the specific properties of the PCD3756A. The device is sometimes referred to as the 'PCD3756x' to allow for common reference to possible future devices of the same basic type. The PCD3756A is a member of the PCD33xxA family of microcontrollers. The shared properties of the family are described in the *"PCD33xxA family"* data sheet, which should be read in conjunction with this publication.

The PCD3756A is a One-Time Programmable (OTP) microcontroller designed primarily for telephony applications. It includes an on-chip generator for dual tone multifrequency (DTMF), modem and musical tones. In addition to dialling, generated frequencies can be made available as square waves (P1.7/MDY) for melody generation, providing ringer operation (in which case the tone output is disabled). A wake-up function via Port 0 interrupt facilitates keyboard interfacing.

The PCD3756A also incorporate 128 bytes of EEPROM. The EEPROM can be used for storing telephone numbers, particularly for implementing redial functions.

The instruction set is similar to that of the MAB8048 and is a sub-set of that listed in the *"PCD33xxA family"* data sheet.

3 ORDERING INFORMATION (see note 1)

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3756AP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3756AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCD3756AH	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

Note

1. Please refer to the Order Entry Form (OEF) for this device for the full type number to use when ordering. This type number will also specify the required program and the ROM mask options.

4 BLOCK DIAGRAM

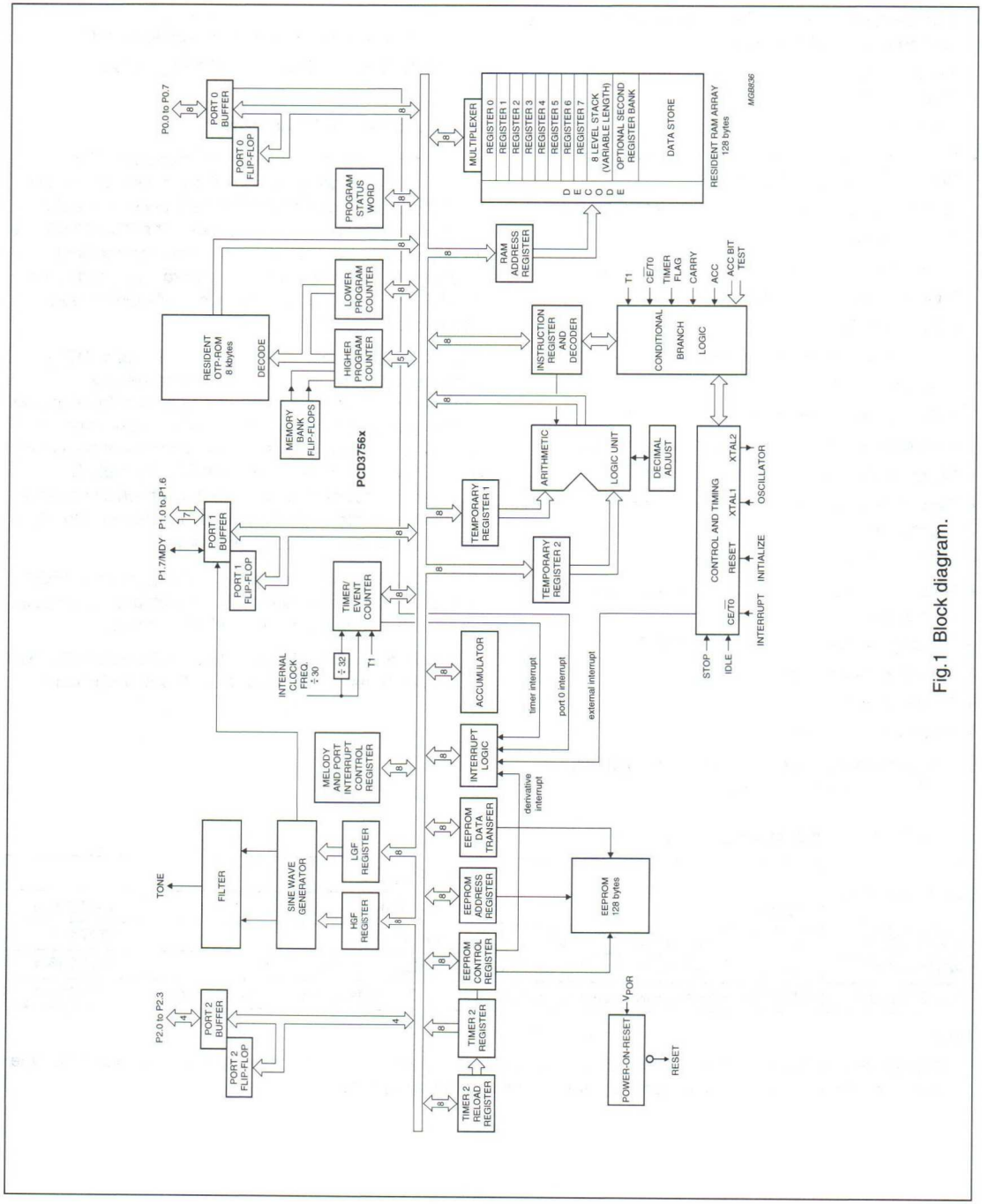


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

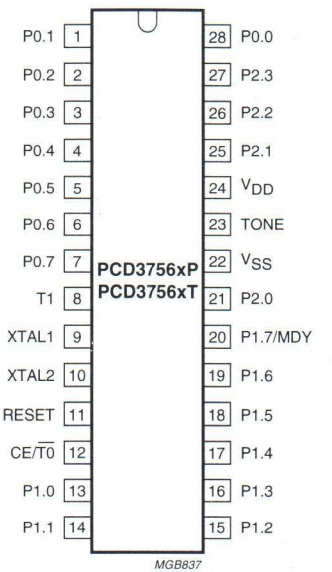


Fig.2 Pin configuration (SOT117-1 and SOT136-1).

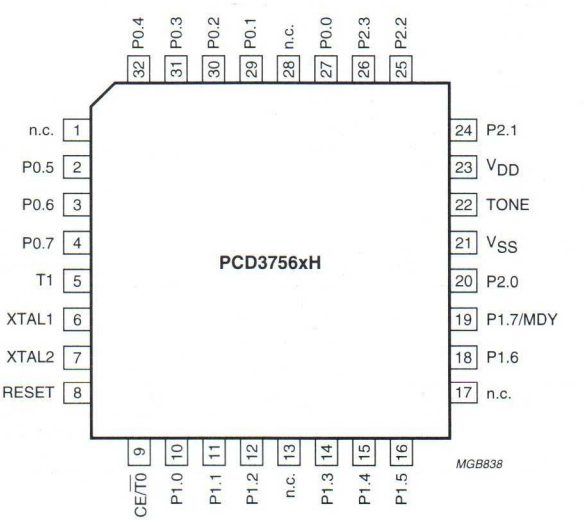


Fig.3 Pin configuration (SOT358-1).

5.2 Pin description

Table 1 SOT117-1 and SOT136-1 packages (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	TYPE	DESCRIPTION
P1.1 to P0.7	1 to 7	I/O	7 bits of Port 0: 8-bit quasi-bidirectional I/O port; or wake-up interrupts
T1	8	I	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	9	I	crystal oscillator or external clock input
XTAL2	10	O	crystal oscillator output
RESET	11	I	reset input
CE/$\overline{T0}$	12	I	Chip Enable or Test 0
P1.0 to P1.6	13 to 19	I/O	7 bits of Port 1: 8-bit quasi-bidirectional I/O port
P1.7/MDY	20	I/O	1 bit of Port 1: 8-bit quasi-bidirectional I/O port; or melody output
P2.0	21	I/O	1 bit of Port 2: 4-bit quasi-bidirectional I/O port
V_{SS}	22	P	ground
TONE	23	O	DTMF output
V_{DD}	24	P	positive supply voltage
P2.1 to P2.3	25 to 27	I/O	3 bits of Port 2: 4-bit quasi-bidirectional I/O port
P0.0	28	I/O	1 bit of Port 0: 8-bit quasi-bidirectional I/O port; or wake-up interrupts

Table 2 SOT358-1 package (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	TYPE	DESCRIPTION
n.c.	1, 13, 17, 28	–	not connected
P0.5 to P0.7	2 to 4	I/O	3 bits of Port 0: 8-bit quasi-bidirectional I/O port; or wake-up interrupts
T1	5	I	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	6	I	crystal oscillator or external clock input
XTAL2	7	O	crystal oscillator output
RESET	8	I	reset input
CE/$\overline{T0}$	9	I	Chip Enable or Test 0
P1.0 to P1.6	10 to 12, 14 to 16, 18	I/O	7 bits of Port 1: 8-bit quasi-bidirectional I/O port
P1.7/MDY	19	I/O	1 bit of Port 1: 8-bit quasi-bidirectional I/O port; or melody output
P2.0	20	I/O	1 bit of Port 2: 4-bit quasi-bidirectional I/O port
V_{SS}	21	P	ground
TONE	22	O	DTMF output
V_{DD}	23	P	positive supply voltage
P2.1 to P2.3	24 to 26	I/O	3 bits of Port 2: 4-bit quasi-bidirectional I/O port
P0.0 to P0.4	27, 29 to 32	I/O	5 bits of Port 0: 8-bit quasi-bidirectional I/O port; or wake-up interrupts

6 FREQUENCY GENERATOR

A versatile frequency generator section is provided (see Fig.4). For normal operation, use a 3.58 MHz quartz crystal or PXE resonator. The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets.

Their frequencies are provided in purely sinusoidal form on the TONE output or as square waves on the P1.7/MDY output.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available.

In case no tones are generated, or the melody function is used, the TONE output is in 3-state mode.

6.1 Frequency generator derivative registers

6.1.1 High and Low Group Frequency registers

Table 3 gives the addresses, mnemonics and access types of the High Group Frequency (HGF) and Low Group Frequency (LGF) registers.

Table 3 Hexadecimal addresses, mnemonics, access types and bit mnemonics of the frequency registers

REGISTER ADDRESS	REGISTER MNEMONIC	ACCESS TYPE	BIT MNEMONICS							
			7	6	5	4	3	2	1	0
11H	HGF	W	H7	H6	H5	H4	H3	H2	H1	H0
12H	LGF	W	L7	L6	L5	L4	L3	L2	L1	L0

6.1.2 Melody and Port Interrupt Control Register (MDYCON)

The Melody and Port Interrupt Control Register has two functions: bit 0 defines the behaviour of the melody output; bits 4 to 7 individually enable/disable specific pairs of Port 0 interrupts. MDYCON is a R/W register.

Table 4 Melody and Port Interrupt Control Register (address 13H)

7	6	5	4	3	2	1	0
EPI3	EPI2	EPI1	EPI0	0	0	0	EMO

Table 5 Description of MDYCON bits

BIT	MNEMONIC	DESCRIPTION
7 to 4	EPI3 to EPI0	Enable Port 0 interrupts. Bits 7 to 4 individually enable/disable specific pairs of Port 0 interrupts; see Table 6 and Section 8.2 for details.
3 to 1	–	These bits are set to a logic 0.
0	EMO	Enable Melody Output. If bit EMO = 0, then P1.7/MDY is a standard port line and the TONE output is enabled. If bit EMO = 1, then P1.7/MDY is the melody output and the TONE output is disabled (3-state). EMO = 1 does not inhibit the port instructions for P1.7/MDY. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by port instructions. However, the port flip-flop of P1.7/MDY must remain set to avoid conflicts between melody and port outputs. When the HGF contents are zero while EMO = 1, P1.7/MDY is in the logic HIGH state.

Table 6 Port 0 Interrupts control bits

BIT	STATE	INTERRUPTS			
		P0.0 AND P0.1	P0.2 AND P0.3	P0.4 AND P0.5	P0.6 AND P0.7
EPI0	1	enabled	–	–	–
	0	disabled	–	–	–
EPI1	1	–	enabled	–	–
	0	–	disabled	–	–
EPI2	1	–	–	enabled	–
	0	–	–	disabled	–
EPI3	1	–	–	–	enabled
	0	–	–	–	disabled

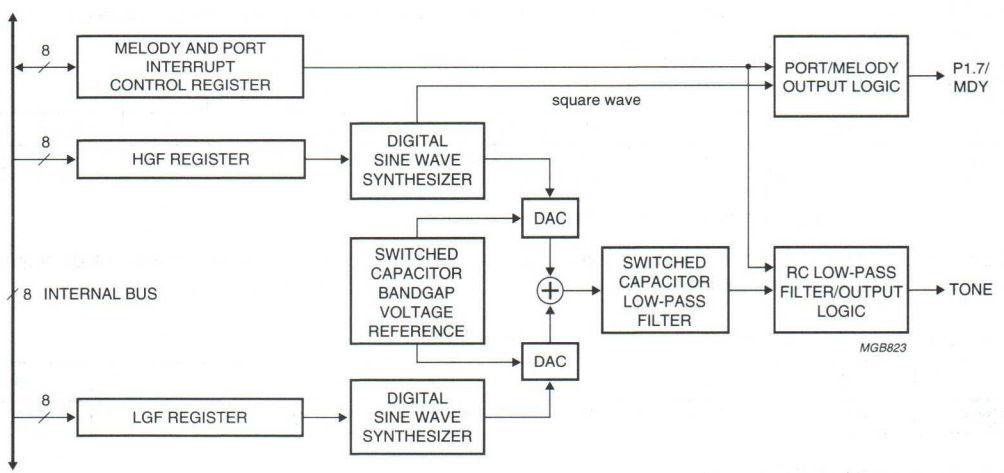


Fig.4 Block diagram of the frequency generator and melody output (P1.7/MDY) section.

6.2 Melody output (P1.7/MDY)

The melody output (P1.7/MDY) is very useful for generating musical notes when a purely sinusoidal signal is not required, such as for ringer applications.

If bit EMO = 1 in the Melody and Port Interrupt Control Register, the TONE output is disabled (3-state) and a square wave with the frequency defined by the HGF contents is output on line P1.7/MDY. The square wave (duty cycle = $^{12}/_{23}$ or 52%) will include the attenuated harmonics of the base frequency, which is defined by the contents of the HGF register (Table 3). However, even higher frequency notes may be produced since the low-pass filtering on the TONE output is not applied to the P1.7/MDY output. This results in the minimum decimal value x in the HGF register (see equation in Section 6.3) being 2 for the P1.7/MDY output, rather than 60 for the TONE output. A sinusoidal TONE output is produced at the same time as the melody square wave, but due to the filtering, the higher frequency sine waves with $x < 60$ will not appear at the TONE output.

Since the melody output is shared with P1.7, the port flip-flop of P1.7 has to be set HIGH before using the melody output. This to avoid conflicts between melody and port outputs. The melody output drive depends on the configuration of port P1.7/MDY; see Chapter 14, Table 25.

6.3 Frequency registers

The two frequency registers HGF and LGF define two frequencies. From these, the digital sine synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures tone output levels independent of supply voltage and temperature.

The amplitude of the Low Group Frequency sine wave is attenuated by 2 dB compared to the amplitude of the High Group Frequency sine wave. The two sine waves are summed and then filtered by an on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

The value 00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption.

The frequency of the sine wave generated 'f' is dependent on the crystal frequency 'f_{xtal}' and the decimal value 'x' held in the frequency registers (HGF and LGF). The variables are related by the equation:

$$f = \frac{f_{xtal}}{[23\,(x+2)\,]}; \text{ where } 60 \leq x \leq 255.$$

The frequency limitation given by $x \geq 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

6.4 DTMF frequencies

Assuming an oscillator frequency f_{xtal} = 3.58 MHz, the DTMF standard frequencies can be implemented as shown in Table 7.

The relationships between telephone keyboard symbols, DTMF frequency pairs and the frequency register contents are given in Table 8.

Table 7 DTMF standard frequencies and their implementation; value = LGF, HGF contents

VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 8 Dialling symbols, corresponding DTMF frequency pairs and frequency register contents

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
•	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

6.5 Modem frequencies

Again assuming an oscillator frequency f_{xtal} = 3.58 MHz, the standard modem frequencies can be implemented as in Table 9. It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling Low Group Frequency generation.

Table 9 Standard modem frequencies and their implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980[1]	978.82	−0.12	−1.18
82	1180[1]	1179.03	−0.08	−0.97
8F	1070[2]	1073.33	0.31	3.33
79	1270[2]	1265.30	−0.37	−4.70
80	1200[3]	1197.17	−0.24	−2.83
45	2200[3]	2192.01	−0.36	−7.99
76	1300[4]	1296.94	−0.24	−3.06
48	2100[4]	2103.14	0.15	3.14
5C	1650[1]	1655.66	0.34	5.66
52	1850[1]	1852.77	0.15	2.77
4B	2025[2]	2021.20	−0.19	−3.80
44	2225[2]	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

6.6 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{xtal} = 3.58 MHz (Table 10). It is suggested to define the frequency by the HGF register while the LGF contains 00H, disabling Low Group Frequency generation.

Table 10 Musical scale frequencies and their implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD[1]	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 @ 440 Hz.

7 EEPROM AND TIMER 2 ORGANIZATION

The PCD3756A has 128 bytes of Electrically Erasable Programmable Read-Only Memory (EEPROM). Such non-volatile storage provides data retention without the need for battery backup. In telecom applications, the EEPROM is used for storing redial numbers and for short dialling of frequently used numbers. More generally, EEPROM may be used for customizing microcontrollers, such as to include a PIN code or a country code, to define trimming parameters, to select application features from the range stored in ROM.

The most significant difference between a RAM and an EEPROM is that a bit in EEPROM, once written to a logic 1, cannot be cleared by a subsequent write operation. Successive write accesses actually perform a logical OR with the previously stored information. Therefore, to clear a bit, the whole byte must be erased and re-written with the particular bit cleared. Thus, an erase-and-write operation is the EEPROM equivalent of a RAM write operation.

Whereas read access times to an EEPROM are comparable to RAM access times, write and erase accesses are much slower at 5 ms each. To make these operations more efficient, several provisions are available in the PCD3756A.

First, the EEPROM array is structured into 32 four-byte pages (see Fig.5) permitting access to 4 bytes in parallel (write page, erase/write page and erase page). It is also possible to erase and write individual bytes. Finally, the EEPROM address register provides auto-incrementing, allowing very efficient read and write accesses to sequential bytes.

To simplify the erase and write timing, the derivative 8-bit down-counter (Timer 2) with reload register is provided. Besides for EEPROM timing, Timer 2 can be used for general real-time tasks, such as for measuring signal duration and for defining pulse widths.

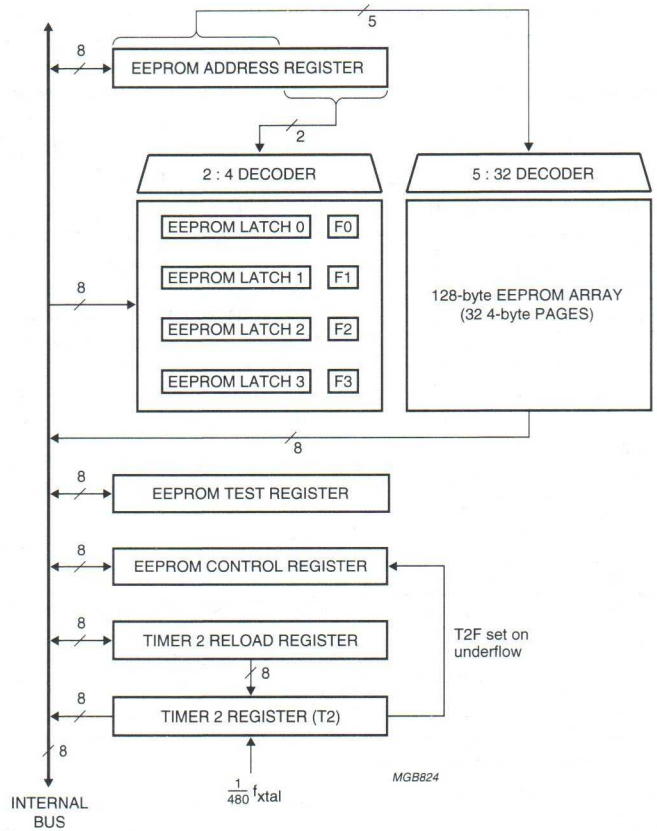


Fig.5 Block diagram of the EEPROM and Timer 2.

7.1 EEPROM registers

7.1.1 EEPROM Control Register (EPCR)

The behaviour of the EEPROM and Timer 2 section is defined by the EEPROM Control Register. See Tables 11, 12 and 13.

Table 11 EEPROM Control Register (address 04H, access type R/W)

7	6	5	4	3	2	1	0
STT2	ET2I	T2F	EWP	MC3	MC2	MC1	0

Table 12 Description of EPCR bits

BIT	MNEMONIC	DESCRIPTION
7	STT2	Start T2. If STT2 = 0, then Timer 2 is stopped; T2 value held. If STT2 = 1, then T2 decrements from reload value.
6	ET2I	Enable T2 interrupt. If ET2I = 0, then T2F event cannot request interrupt. If ET2I = 1, then T2F event can request interrupt.
5	T2F	Timer 2 flag. Set when T2 underflows (or by program); reset by program.
4	EWP	Erase or write in progress (EWP). Set by program (EWP starts EEPROM erase and/or write and Timer 2). Reset at the end of EEPROM erase and/or write.
3	MC3	Mode control 3 to 1. These three bits in conjunction with bit EWP select the mode as shown in Table 13.
2	MC2	
1	MC1	
0	–	This bit is set to a logic 0.

Table 13 Mode selection; X = don't care

EWP	MC3	MC2	MC1	DESCRIPTION
0	0	0	0	read byte
0	0	1	0	increment mode
1	0	1	X	write page
1	1	0	0	erase/write page
1	1	1	1	erase page
X	0	0	1	not allowed
X	1	0	1	
X	1	1	0	

7.1.2 EEPROM ADDRESS REGISTER (ADDR)

The EEPROM Address Register determines the EEPROM location to which an EEPROM access is directed.

As a whole, ADDR auto-increments after read and write cycles to EEPROM, but remains fixed after erase cycles. This behaviour generates the correct ADDR contents for sequential read accesses and for sequential write or erase/write accesses with intermediate page setup. Overflow of the 8-bit counter wraps around to zero.

Table 14 EEPROM Address Register (address 01H, access type R/W)

7	6	5	4	3	2	1	0
0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 15 Description of ADDR bits

BIT	MNEMONIC	DESCRIPTION
7	–	This bit is set to a logic 0.
6 to 2	AD6 to AD2	AD2 to AD6 select one of 32 pages.
1 to 0	AD1 to AD0	AD1 and AD0 are irrelevant during erase and write cycles. For read accesses, AD0 and AD1 indicate the byte location within an EEPROM page. During page setup, finally, AD0 and AD1 select EEPROM Latch 0 to 3 whereas AD2 to AD6 are irrelevant. If increment mode (Table 13) is active during page setup, the subcounter consisting of AD0 and AD1 increments after every write to an EEPROM latch, thus enhancing access to sequential EEPROM latches. Incrementing stops when EEPROM Latch 3 is reached, i.e. when AD0 and AD1 are both a logic 1.

7.1.3 EEPROM DATA REGISTER (DATR)

Table 16 EEPROM Data Register (address 03H; access type R/W)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 17 Description of DATR bits

BIT	MNEMONIC	DESCRIPTION
7 to 0	D7 to D0	The EEPROM Data Register (DATR) is only a conceptual entity. A read operation from DATR, reads out the EEPROM byte addressed by ADDR. On the other hand, a write operation to DATR, loads data into the EEPROM latch (see Fig.5) defined by bits AD0 and AD1 of ADDR.

7.1.4 EEPROM TEST REGISTER (TST)

The EEPROM Test register is used for testing purposes during device manufacture. It must not be accessed by the device user.

7.2 EEPROM latches

The four EEPROM latches (EEPROM Latch 0 to 3; Fig.5) cannot be read by user software. Due to their construction, the latches can only be preset, but not cleared. Successive write operations through DATR to the EEPROM latches actually perform a logical OR with the previously stored data in EEPROM. The EEPROM latches are reset at the conclusion of any EEPROM cycle.

7.3 EEPROM flags

The four EEPROM flags (F0 to F3; Fig.5) cannot be directly accessed by user software. An EEPROM flag is set as a side-effect when the corresponding EEPROM latch is written through DATR. The EEPROM flags are reset at the conclusion of any EEPROM cycle.

7.4 EEPROM macros

The instruction sequence used in an EEPROM access should be treated as an indivisible entity. Erroneous programs result if ADDR, DATR, RELR or EPCR are inadvertently changed during an EEPROM cycle or its setup. Special care should be taken if the program may asynchronously divert due to an interrupt. Particularly, a new access to the EEPROM may only be initiated when no write, erase or erase/write cycles are in progress. This can be verified by reading bit EWP (register EPCR).

For write, erase and erase/write cycles, it is assumed that the Timer 2 Reload Register (RELR) has been loaded with the appropriate value for a 5 ms delay, which depends on f_{xtal} (see Table 24). The end of a write, erase or erase/write cycle will be signalled by a cleared EWP and by a Timer 2 interrupt provided that ET2I = 1 and that the SIO/derivative interrupt is enabled.

7.5 EEPROM access

One read, one write, one erase/write and one erase access are defined by bits EWP and MC1 to MC3 in the EPCR register; see Table 11.

Read byte retrieves the EEPROM byte addressed by ADDR when DATR is read. Read cycles are instantaneous.

Write and erase cycles take 5 ms, however. Erase/write is a combination of an erase and a subsequent write cycle, consequently taking 10 ms.

As their names imply, **write page, erase page and erase/write page** are applied to a whole EEPROM page. Therefore, bits AD0 and AD1 of register ADDR (see Table 14), defining the byte location within an EEPROM page, are irrelevant during write and erase cycles. However, write and erase cycles need not affect all bytes of the page. The EEPROM flags F0 to F3 (see Fig.5) determine which bytes within the EEPROM page are affected by the erase and/or write cycles. A byte whose corresponding EEPROM flag is zero remains unchanged.

With erase page, a byte is erased if its corresponding EEPROM flag is set. With write page, data in EEPROM Latch 0 to 3 (Fig.5) are ORed to the individual page bytes if and only if the corresponding EEPROM flags are set.

In an erase/write cycle, F0 to F3 select which page bytes are erased and ORed with the corresponding EEPROM latches.

ORing, in this event, means that the EEPROM latches are copied to the selected page bytes.

The described page-wise organization of erase and write cycles allows up to four bytes to be individually erased or written within 5 ms. This advantage necessitates a preparation step, called **page setup**, before the actual erase and/or write cycle can be executed.

Page setup controls EEPROM latches and EEPROM flags. This will be described in the Sections 7.5.1 to 7.5.5.

7.5.1 PAGE SETUP

Page setup is a preparation step required before write page, erase page and erase/write page cycles.
As previously described, these page operations include single-byte write, erase and erase/write as a special event. EEPROM flags F0 to F3 determine which page bytes will be affected by the mentioned page operations. EEPROM Latch 0 to 3 must be preset through DATR to specify the write cycle data to EEPROM and to set the EEPROM flags as a side-effect. Obviously, the actual preset value of the EEPROM latches is irrelevant for erase page. Preset of one, two, three or all four EEPROM latches and the corresponding EEPROM flags can be performed by repeatedly defining ADDR and writing to DATR (see Table 18).

If more than one EEPROM latch must be preset, the subcounter consisting of AD0 and AD1 can be induced to auto-increment after every write to DATR, thus stepping through all EEPROM latches. For this purpose, increment mode (Table 13) must be selected. Auto-incrementing stops at EEPROM Latch 3. It is not mandatory to start at EEPROM Latch 0 as in shown in Table 19.

Note that AD2 to AD6 are irrelevant during page setup. They will usually specify the intended EEPROM page, anticipating the subsequent page cycle.

From now on, it will be assumed that AD2 to AD6 will contain the intended EEPROM page address after page setup.

Table 18 Page setup; preset

INSTRUCTION	RESULT
MOV A, #addr	address of EEPROM latch
MOV ADDR, A	send address to ADDR
MOV A, #data	load write, erase/write or erase data
MOV DATR, A	send data to addressed EEPROM latch

Table 19 Page setup; auto-incrementing

INSTRUCTION	RESULT
MOV A, #MC2	increment mode control word
MOV EPCR, A	select increment mode
MOV A, #baddr	EEPROM Latch 0 address (AD0 = AD1 = 0)
MOV ADDR, A	send EEPROM Latch 0 address to ADDR
MOV A, R0	load 1st byte from Register 0
MOV DATR, A	send 1st byte to EEPROM Latch 0
MOV A, R1	load 2nd byte from Register 1
MOV DATR, A	send 2nd byte to EEPROM Latch 1
MOV A, R2	load 3rd byte from Register 2
MOV DATR, A	send 3rd byte to EEPROM Latch 2
MOV A, R3	load 4th byte from Register 3
MOV DATR, A	send 4th byte to EEPROM Latch 3

7.5.2 READ BYTE

Since ADDR auto-increments after a read cycle regardless of the page boundary, successive bytes can efficiently be read by repeating the last instruction.

Table 20 Read byte

INSTRUCTION	RESULT
MOV A, #RDADDR	load read address
MOV ADDR, A	send address to ADDR
MOV A, DATR	read EEPROM data

7.5.3 WRITE PAGE

The write cycle performs a logical OR between the data in the EEPROM latches and that in the addressed EEPROM page. To actually copy the data from the EEPROM latches, the corresponding bytes in the page should previously have been erased.

The EEPROM latches are preset as described in Section 7.5.1. The actual transfer to the EEPROM is then performed as shown in Table 21.

The last instruction also starts Timer 2. The data in the EEPROM latches are ORed with that in the corresponding page bytes within 5 ms. A single-byte write is simply a special case of 'write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by bits AD2 to AD6) and to EEPROM Latch 0 (by bits AD0 and AD1). This allows efficient coding of multi-page write operations.

Table 21 Write page

INSTRUCTION	RESULT
MOV A, #EWP + MC2	'write page' control word
MOV EPCR, A	start 'write page' cycle

7.5.4 ERASE/WRITE PAGE

The EEPROM latches are preset as described in Section 7.5.1. The page byte corresponding to the asserted flags (among F0 to F3) are erased and re-written with the contents of the respective EEPROM latches.

The last instruction also starts Timer 2. Erasure takes 5 ms upon which Timer Register T2 reloads for another 5 ms cycle for writing. The top cycles together take 10 ms. A single-byte erase/write is simply a special event of 'erase/write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by AD2 to AD6) and to EEPROM latch 0 (by AD0 and AD1). This allows efficient coding of multi-page erase/write operations.

Table 22 Erase/write page

INSTRUCTION	RESULT
MOV A, #EWP + MC3	'erase/write page' control word
MOV EPCR, A	start 'erase/write page' cycle

7.5.5 ERASE PAGE

The EEPROM flags are set as described in Section 7.5.1. The corresponding page bytes are erased.

The last instruction also starts Timer 2. Erasure takes 5 ms. A single-byte erase is simply a special case of 'erase page'.

Note that ADDR does not auto-increment after an erase cycle.

Table 23 Erase page

INSTRUCTION	RESULT
MOV A, #EWP + MC3 + MC2 + MC1	'erase page' control word
MOV EPCR, A	start 'erase page' cycle

7.6 Timer 2

Timer 2 is a 8-bit down-counter decremented at a rate of $1/480 \times f_{xtal}$. It may be used either for EEPROM timing or as a general purpose timer. Conflicts between the two applications should be carefully avoided.

7.6.1 TIMER 2 FOR EEPROM TIMING

When used for EEPROM timing, Timer 2 serves to generate the 5 ms intervals needed for erasing or writing the EEPROM. At the decrement rate of $1/480 \times f_{xtal}$, the reload value for a 5 ms interval is a function of f_{xtal}. Table 24 summarizes the required reload values for a number of oscillator frequencies.

Timer 2 is started by setting bit EWP in the EPCR. The Timer Register T2 is loaded with the reload value from RELR. T2 decrements to zero.

For an erase/write cycle, underflow of T2 indicates the end of the erase operation. Therefore, Timer Register T2 is reloaded from RELR for another 5 ms interval during which the flagged EEPROM latches are copied to the corresponding bytes in the page addressed by ADDR.

The second underflow of an erase/write cycle and the first underflow of write page and erase page conclude the corresponding EEPROM cycle. Timer 2 is stopped, T2F is set whereas EWP and MC1 to MC3 are cleared.

Table 24 Reload values as a function of f_{xtal}

f_{xtal} (MHz)	RELOAD VALUE[1] (HEX)
1	0A
2	14
3.58	25
6	3E
10	68
16	A6

Note

1. The reload value is $(5 \times 10^{-3} \times 1/480 \times f_{xtal}) - 1$; f_{xtal} in MHz.

7.6.2 TIMER 2 AS A GENERAL PURPOSE TIMER

When used for purposes other than EEPROM timing, Timer 2 is started by setting STT2. The Timer Register T2 (see Table 27) is loaded with the reload value from RELR. T2 decrements to zero. On underflow, T2 is reloaded from RELR, T2F is set and T2 continues to decrement.

Timer 2 can be stopped at any time by clearing STT2. The value of T2 is then held and can be read out. After setting STT2 again, Timer 2 decrements from the reload value. Alternatively, it is possible to read T2 'on the fly' i.e. while Timer 2 is operating.

8 INTERRUPTS

8.1 Derivative interrupt

One derivative interrupt event is defined. It is controlled by bits T2F and ET2I in the EPCR (see Tables 11 and 12).

The derivative interrupt event occurs when T2F is set. This request is honoured under the following circumstances:

- No interrupt routine proceeds
- No external interrupt request is pending
- The derivative interrupt is enabled
- ET2I is set.

The derivative interrupt routine must include instructions that will remove the cause of the derivative interrupt by explicitly clearing T2F. If the derivative interrupt is not used, T2F may directly be tested by the program. Obviously, T2F can also be asserted under program control, e.g. to generate a software interrupt.

8.2 Port 0 Wake-up interrupts

In addition to the external interrupt CE, the PCD3756A contains 8 level-sensitive external interrupt sources on Port 0. This function generates an interrupt request if any of the enabled lines of Port 0 (P0.0 to P0.7) is pulled LOW. Like the external interrupt (and contrary to the derivative interrupt) the Port 0 interrupt operates also in Stop mode and forces the CPU to exit the Stop mode.

The Port 0 Wake-up interrupts are controlled by the Enable Port 0 Interrupt bits EPI3 to EPI0 in the Melody and Port Interrupt Control Register MDYCON. Pairs of Port 0 interrupts are individually enabled/disabled via bits 4, 5, 6 and 7. For details see Section 6.1.2. As the Port 0 interrupt is directly linked to the external interrupt, it uses the same flag (EIF), enable instructions (EN I, DIS I) and interrupt vector.

A Port 0 Wake-up interrupt is serviced if:

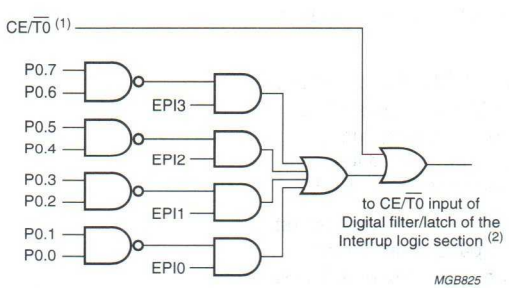
- No interrupt routine is in progress
- The external interrupt is enabled
- It's corresponding enable bit in register MDYCON is set to a logic 1.

If a Port 0 interrupt is to be used, the port flip-flop must first be set to a logic 1 (set to input mode) before it's corresponding EPIn bit is set.

If only a portion of the Port 0 interrupts are used, the remaining port lines may still be used as normal I/O.

In order to configure an I/O as an input, a logic 1 must first be written to it. If a logic 0 is written to one of these port lines (e.g. ANL P0, 00H) while it's corresponding interrupt is enabled, a Port 0 interrupt will be generated.

For more details see data sheet *"PCD33XXA Family; Section External Interrupt"*.



(1) From pin CE/T0.
(2) See the *"PCD33XXA Family"* data sheet.

Fig.6 Simplified External/Port 0 interrupt structure.

9 TIMING

Although the PCD3756A operates over a clock frequency range from 1 to 16 MHz, f_{xtal} = 3.58 MHz will usually be chosen to take full advantage of the frequency generator section.

10 RESET

In addition to the conditions given in the *"PCD33XXA Family"* data sheet, all derivative registers are cleared in the reset state.

11 IDLE MODE

In Idle mode, the frequency generator, the EEPROM and the Timer 2 sections remain operative. Therefore, the IDLE instruction may be executed while an erase and/or write access to EEPROM is in progress.

12 STOP MODE

Since the oscillator is switched off, the frequency generator, the EEPROM and the Timer 2 sections receive no clock. It is suggested to clear both the HGF and the LGF registers before entering Stop mode.

This will cut off the biasing of the internal amplifiers, considerably reducing current requirements.

The Stop mode **must not** be entered while an erase and/or write access to EEPROM is in progress. The STOP instruction may only be executed when EWP in EPCR is zero. The Timer 2 section is frozen during Stop mode. After exit from Stop mode by a HIGH level on CE/$\overline{T0}$, Timer 2 proceeds from the held state.

The Port 0 Wake-up interrupt function remains operative during Stop mode (depending only on the EPIn bits in register MDYCON). In addition to the description in the *"PCD33XXA Family"* data sheet, Stop mode may be left by a Port 0 Wake-up interrupt event (see Section 8.2).

13 INSTRUCTION SET RESTRICTIONS

RAM space is restricted to 128 bytes, care should be taken to avoid accesses to non-existing RAM locations.

14 OVERVIEW OF PORT AND POWER-ON-RESET CONFIGURATION

Table 25 Port and Power-on-reset configuration

See notes 1 and 2.

TYPE	PORT 0								PORT 1								PORT 2				V_{POR}
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	
PCD3756A	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1R	1R[3]	2S	2S	2S	2S	1.3 V

Notes

1. Port output drive:1 = standard I/O; 2 = open-drain I/O, see *"PCD33xxA Family"* data sheet.
2. Port state after reset: S = Set (HIGH) and R = Reset (LOW).
3. The melody output drive type is push-pull.

15 OTP PROGRAMMING

The programming of the PCD3755x and PCD3756x OTPs is based on the OM4260 programmer (Ceibo MP-51), available from Philips. The OM4260 works in conjunction with various adapters supporting the different package types available as listed in Table 26.

The low-voltage OTP program memory used is of Anti-Fuse-PROM type and can not be erased after programming.

Thus, the complete OTP memory cannot be tested by the factory, but only partially via a special test array. The average expected yield is 97%.

Detailed information on the OTP programming is available in the *"PCD3755x Application Note"*, being available via your Philips Sales office.

Table 26 OTP programming overview

DEVICE	PHILIPS TYPE NUMBER	CEIBO TYPE NUMBER	SUPPORTED PACKAGE
Ceibo MP-51	OM4260	MP-51 programmer base	–
PCD3755x/56x	OM5007	PCD3755A/56A adapter DIP	DIP28
PCD3755x/56x	OM5030	PCD3755A/56A adapter SO	SO28
PCD3755x/56x	OM5037(1)	PCD3755A/56A adapter QFP32	LQFP32

Note

1. As the OM5037 is only a socket converter, the OM5007 is also needed to program the PCD3755x/56x in the LQFP32 package.

16 SUMMARY OF DERIVATIVE REGISTERS

Table 27 Register map

ADDR. (HEX)	REGISTER	7	6	5	4	3	2	1	0	R/W
00	not used									
01	EEPROM Address Register (ADDR)	0	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/W
02	not used									
03	EEPROM Data Register (DATR)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
04	EEPROM Control Register (EPCR)	STT2	ET21	TF2	EWP	MC3	MC2	MC1	0	R/W
05	Timer 2 Reload Register (RELR)	R7	R6	R5	R4	R3	R2	R1	R0	R/W
06	Timer 2 Register (T2)	T2.7	T2.6	T2.5	T2.4	T2.3	T2.2	T2.1	T2.0	R
07	Test Register (TST)	only for test purposes; not to be accessed by the device user								
08 to 10	not used									
11	High Group Frequency Register (HGF)	H7	H6	H5	H4	H3	H2	H1	H0	W
12	Low Group Frequency Register (LGF)	L7	L6	L5	L4	L3	L2	L1	L0	W
13	Melody Control Register (MDYCON)	0	0	0	0	0	0	0	EMO	R/W
14 to FF	not used									

17 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+7.0	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	−	125	mW
P_O	power dissipation per output	−	30	mW
I_{SS}	ground supply current	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	−	90	°C

18 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Data Handbook IC14, Section: Handling MOS devices"*).

19 DC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	see Fig.7				
	operating	note 1	1.8	–	6	V
	RAM data retention in Stop mode		1.0	–	6	V
I_{DD}	operating supply current	see Figs 8 and 9; note 2				
		V_{DD} = 3 V; value HGF or LGF ≠ 0	–	0.8	1.6	mA
		V_{DD} = 3 V	–	0.35	0.7	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.5	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	2.4	6.0	mA
$I_{DD(idle)}$	supply current (Idle mode)	see Figs 10 and 11; note 2				
		V_{DD} = 3 V; value HGF or LGF ≠ 0	–	0.7	1.4	mA
		V_{DD} = 3 V	–	0.25	0.5	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.1	3.4	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	1.7	5.0	mA
$I_{DD(stp)}$	supply current (Stop mode)	see Fig.12; note 3				
		V_{DD} = 1.8 V; T_{amb} = 25 °C;	–	1.0	5.5	µA
		V_{DD} = 1.8 V; T_{amb} = 70 °C;	–	–	10	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	−1	–	1	µA
Port outputs						
I_{OL}	LOW level port sink current	V_{DD} = 3 V; V_O = 0.4 V; see Fig.13	0.7	3.5	–	mA
I_{OH}	HIGH level pull-up output source current	V_{DD} = 3 V; V_O = 2.7 V; see Fig.14	−10	−30	–	µA
		V_{DD} = 3 V; V_O = 0 V; see Fig.14	–	−140	−300	µA
I_{OH1}	HIGH level push-pull output source current	V_{DD} = 3 V; V_O = 2.6 V; see Fig.15	−0.7	−3.5	–	mA
Tone output (see Fig.16; note 4)						
$V_{HG(RMS)}$	HGF voltage (RMS value)		158	181	205	mV
$V_{LG(RMS)}$	LGF voltage (RMS value)		125	142	160	mV
$\Delta f/f$	frequency deviation		−0.6	–	0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_o \rvert$	output impedance		–	100	500	Ω
G_v	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	T_{amb} = 25 °C; note 5	–	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EEPROM (notes 1 and 6)						
$CY_{t/w}$	endurance (erase/write cycles)	note 7	10^5	–	–	
t_{ret}	data retention time		10	–	–	years
Power-on-reset (see Fig.17)						
V_{POR}	Power-on-reset level		0.8	1.3	1.8	V
Oscillator (see Fig.18)						
g_m	transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

Notes

1. TONE output, EEPROM erase and write require $V_{DD} \geq 2.5$ V.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open; value HGF = LGF = 0, unless otherwise specified.
   a) Maximum values: external clock at XTAL1 and XTAL2 open-circuit.
   b) Typical values: T_{amb} = 25 °C; crystal connected between XTAL1 and XTAL2.
3. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; RESET, T1 and CE/T0 at V_{SS}; crystal connected between XTAL1 and XTAL2; pins T1 and CE/T0 at V_{SS}.
4. Values are specified for DTMF frequencies only (CEPT).
5. Related to the Low Group Frequency (LGF) component (CEPT).
6. After final testing the value of each EEPROM bit is a logic 1, but this cannot be guaranteed after board assembly.
7. Verified on sampling basis.

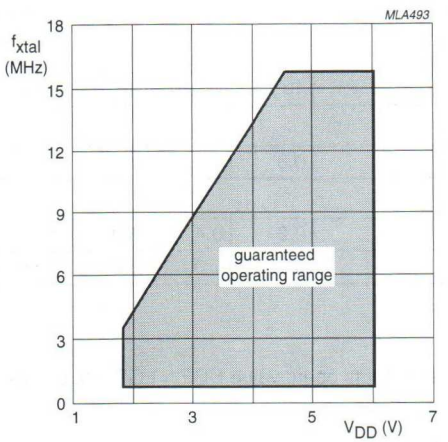
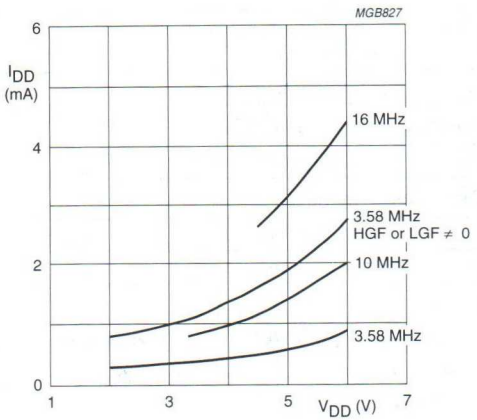
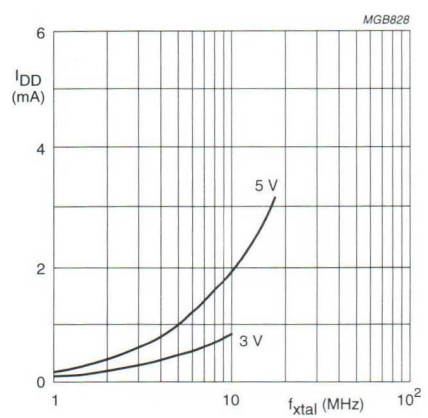


Fig.7 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).



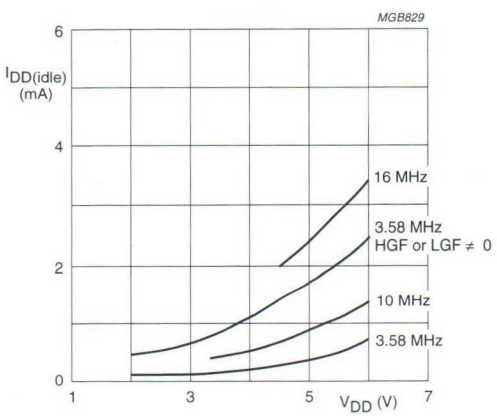
Measured with crystal between XTAL1 and XTAL2.

Fig.8 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).



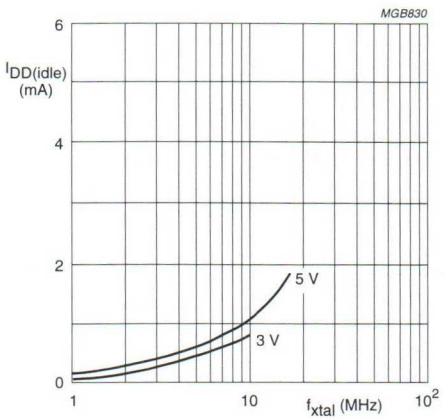
Measured with function generator on XTAL1.

Fig.9 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



Measured with crystal between XTAL1 and XTAL2.

Fig.10 Typical supply current in Idle mode ($I_{DD(idle)}$) as a function of supply voltage (V_{DD}).



Measured with function generator on XTAL1.

Fig.11 Typical supply current in Idle mode ($I_{DD(idle)}$)as a function of clock frequency (f_{xtal}).

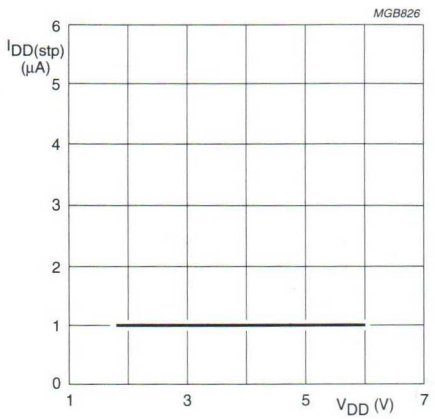
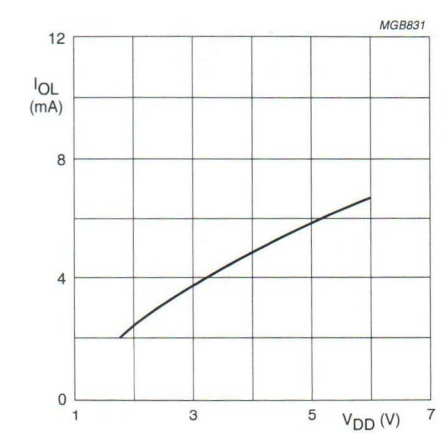


Fig.12 Typical supply current in Stop mode ($I_{DD(stp)}$) as a function of supply voltage (V_{DD}).



V_O = 0.4 V.

Fig.13 Typical LOW level output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

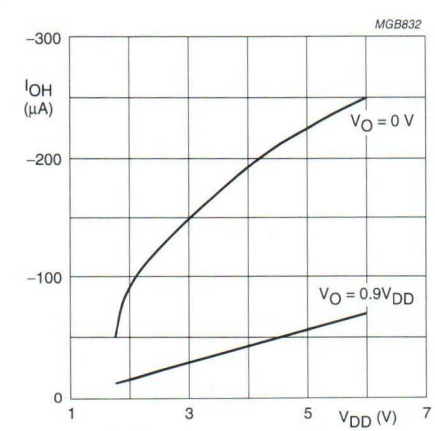
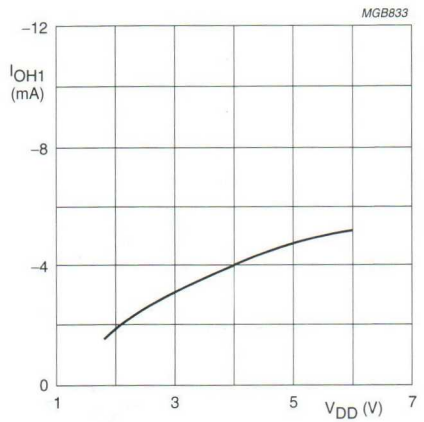
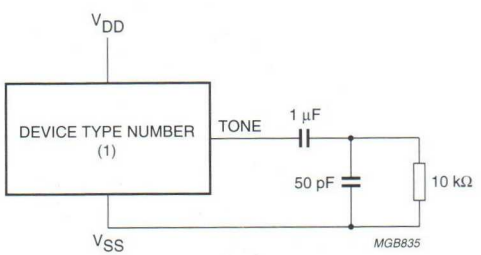


Fig.14 Typical HIGH level pull-up output source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.15 Typical HIGH level push-pull output source current (I_{OH1}) as a function of supply voltage (V_{DD}).



(1) Device type number: PCD3756A.

Fig.16 TONE output test circuit.

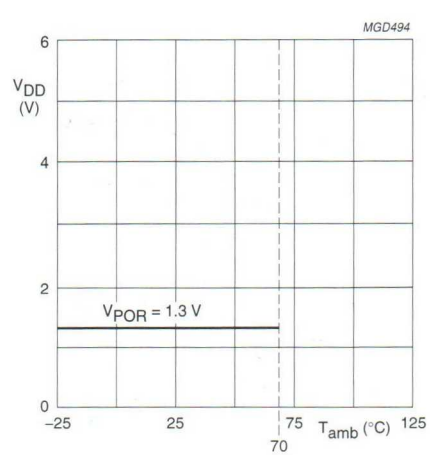


Fig.17 Typical Power-on-reset level (V_{POR}) as function of ambient temperature (T_{amb}).

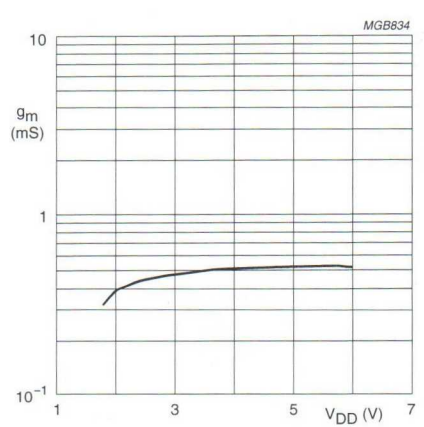


Fig.18 Typical transconductance as a function of supply voltage (V_{DD}).

20 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.7	1	–	16	MHz

8-bit microcontroller with I²C-bus interface

PCF84C00

FEATURES

- Manufactured in silicon gate CMOS process
- 8-bit CPU, RAM, I/O in a single 28-lead or 56-lead package
- 'Piggy-back' and ROM-less versions, external program memory
- 256 × 8 RAM
- 20 quasi-bidirectional I/O port lines
- Two test inputs, one of which is also the external interrupt input
- Three single-level vectored interrupts:
  - external
  - timer/event counter
  - I²C-bus
- I²C-bus interface for serial data transfer on two lines (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2.5 to 5.5 V)
- Stop and Idle modes
- Power-on reset circuit
- Operating temperature range: –40 to +85 °C.

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCF84C00. The shared properties of the PCF84CxxxA family of microcontrollers are described in the *"PCF84CxxxA family"* data sheet, which should be read in conjunction with this publication.

The PCF84C00 has 20 quasi-bidirectional I/O lines, an I²C-bus serial interface, a single-level vectored interrupt structure, an 8-bit timer/event counter and on-chip clock oscillator and clock circuits.

This efficient controller also performs well as an arithmetic processor. It has facilities for both binary and BCD arithmetic plus bit-handling capabilities.

The instruction set is similar to the MAB8048 and is a sub-set of that listed in the *"PCF84CxxxA family"* data sheet.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF84C00B	–	Non-standard 28-lead 'piggy-back' package with 28-pin EPROM socket on top. Bottom 'footprint' and pinning as DIP 28, version SOT117-1. The SOT117-1 information provided is correct in these respects, but **not** for the physical size of the PCF84C00B, which is larger than the SOT117-1 package.	–
PCF84C00T	VSO56	Plastic very small outline package; 56 leads.	SOT 190-1

BLOCK DIAGRAM

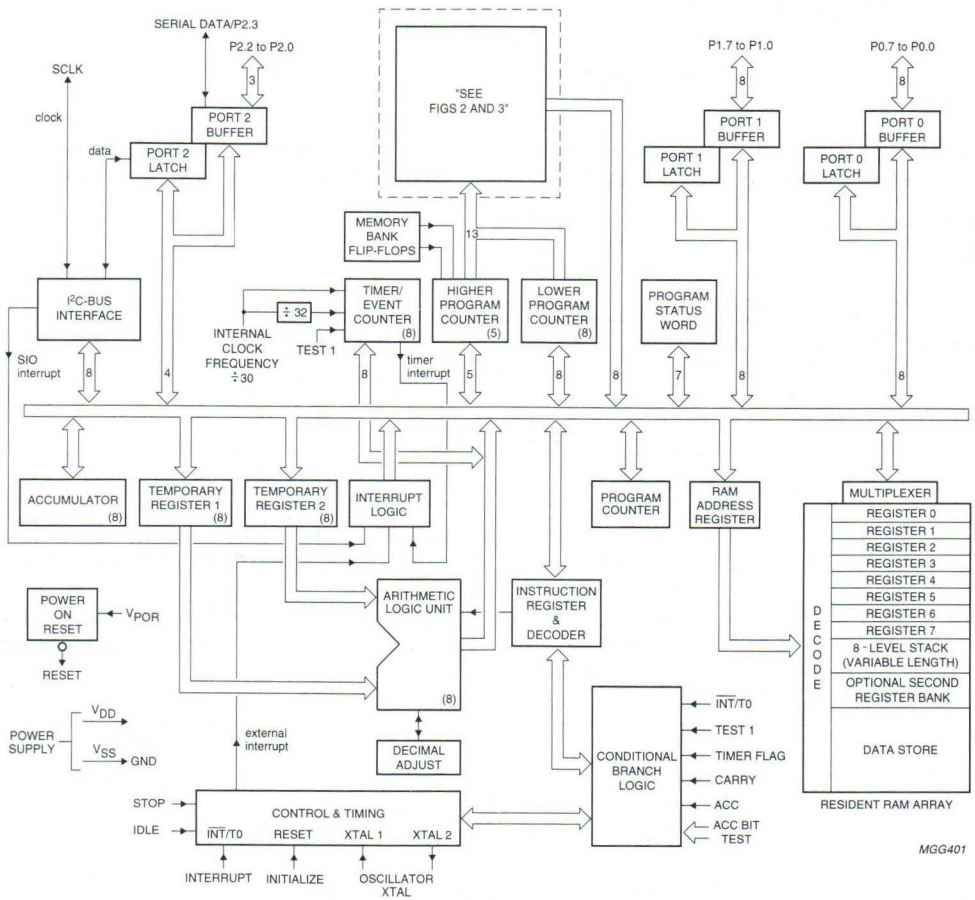


Fig.1 Block diagram.

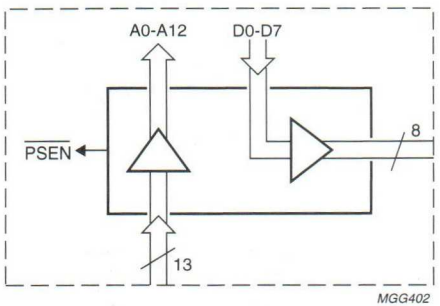


Fig.2 Replacement of dotted section in Fig.1, for the PCF84C00B 'piggy-back' version.

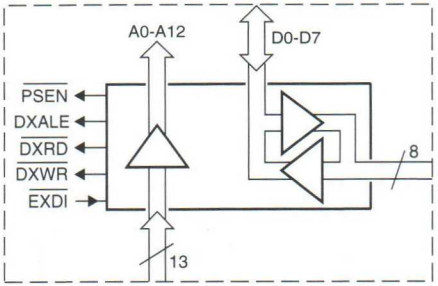


Fig.3 Replacement of dotted section in Fig.1, for the PCF84C00T ROM-less version.

PINNING

Table 1 PCF84C00B (see Fig.4)

SYMBOL	PIN	TYPE	DESCRIPTION
P2.2	1	I/O	1 bit of Port 2: 4-bit quasi-bidirectional I/O port
SDA/P2.3	2	I/O	bidirectional data line of the I²C-bus interface; or 1 bit of Port 2: 4-bit quasi-bidirectional I/O line
SCLK	3	I/O	bidirectional clock line of the I²C-bus interface
P0.0 to P0.7	4 to 11	I/O	8 bits of Port 0: 8-bit quasi-bidirectional I/O port
$\overline{INT}$/T0	12	I	Interrupt/Test 0: external interrupt input (negative edge triggered)/test input pin. When used as a test input, this pin is directly tested by conditional branch instructions JT0 and JNT0.
T1	13	I	Test 1: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 may also be selected as an input to the 8-bit timer/event counter via the STRT CNT instruction.
V_{SS}	14	P	ground: circuit earth potential
XTAL1	15	I	oscillator input: input from a crystal which determines the internal oscillator frequency or an external clock generator
XTAL2	16	I/O	oscillator output: output of the inverting amplifier
RESET	17	I/O	reset input: used to initialize the microcontroller (active HIGH); also output of power-on-reset circuit
P1.0 to P1.7	18 to 25	I/O	8 bits of Port 1: 8-bit quasi-bidirectional I/O port
P2.0 to P2.1	26, 27	I/O	2 bits of Port 2: 4-bit quasi-bidirectional I/O port
V_{DD}	28	P	power supply: 2.5 V to 5.5 V

Table 2 PCF84C00T (see Fig.5)

SYMBOL	PIN	TYPE	DESCRIPTION
P2.2	1	I/O	1 bit of Port 2: 4-bit quasi-bidirectional I/O port
SDA/P2.3	2	I/O	bidirectional data line of the I²C-bus interface; or 1 bit of Port 2: 4-bit quasi-bidirectional I/O port
SCLK	3	I/O	bidirectional clock line of the I²C-bus interface
P0.0 to P0.1	4, 5	I/O	2 bits of Port 0: 8-bit quasi-bidirectional I/O port
DXALE	6	O	Address latch enable: on the falling edge of DXALE, the Dx address can be latched in an external latch. This signal occurs only during execution of the MOV Dx, A, MOV A, Dx, ANL Dx, A and ORL Dx, A instructions, with x = 0 to 255. It is active during TS10 of cycle 1 and the first half of TS1 of cycle 2.
n.c.	7	–	not connected
P0.2 to P0.7	8 to 13	I/O	6 bits of Port 0: 8-bit quasi-bidirectional I/O port
$\overline{\text{INT}}$/T0	14	I	Interrupt/Test 0: external interrupt input (negative edge triggered)/test input pin. When used as a test input, this pin is directly tested by conditional branch instructions JT0 and JNT0; note 1.
T1	15	I	Test 1: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 may also be selected as an input to the 8-bit timer/event counter via the STRT CNT instruction.
D0 to D2	16 to 18	I/O	3 bits of 8-bit data bus: for external memory and peripherals. The specified Stop mode supply current is valid only if external pull-ups are connected to all data lines.
A12	19	O	1 bit of 13-bit address bus: for external memory and peripherals
$\overline{\text{DXWR}}$	20	O	Write strobe (active LOW): on the rising edge, data on D0-D7 may be written to external registers. This signal occurs only during MOV Dx, A, ANL Dx, A and ORL Dx, A instructions, with x = 0 to 255. It is active during TS7 of cycle 2.
n.c.	21	–	not connected
A11 to A6	22 to 27	O	6 bits of 13-bit address bus: for external memory and peripherals
V_{SS}	28	P	ground: circuit earth potential
A5 to A0	29 to 34	O	6 bits of 13-bit address bus: for external memory and peripherals
$\overline{\text{DXRD}}$	35	O	Read strobe (active LOW): when this signal is active, external registers emulating Dx registers can be read by the data bus. This signal occurs only during execution of MOV A, Dx, ANL Dx, A and ORL Dx, A instructions, with x = 0 to 255. It is active during TS3 and TS4 of cycle 2.
D3 to D7	36 to 40	I/O	5 bits of 8-bit data bus: for external memory and peripherals. The specified Stop mode supply current is valid only if external pull-ups are connected to all data lines.
$\overline{\text{PSEN}}$	41	O	Program store enable (active LOW): $\overline{\text{PSEN}}$ is used to enable external program memory and is active during TS9 and TS10 of each machine cycle and TS1 of each following cycle. $\overline{\text{PSEN}}$ is HIGH during the Stop mode.
XTAL1	42	I	oscillator input: input from a crystal which determines the internal oscillator frequency or an external clock generator
XTAL2	43	I/O	oscillator output: output of the inverting amplifier

SYMBOL	PIN	TYPE	DESCRIPTION
RESET	44	I/O	reset input: used to initialize the microcontroller (active HIGH); also output of power-on-reset circuit
P1.0 to P1.3	45 to 48	I/O	4 bits of Port 1: 8-bit quasi-bidirectional I/O port
$\overline{EXDI}$	49	I	External derivative interrupt (active LOW): $\overline{EXDI}$ is 'OR-ed' with the internal serial interrupt and can be used to initiate an interrupt from external hardware emulating derivative functions. $\overline{EXDI}$ is pulled HIGH internally. The derivative interrupt is polled during time slot TS6 (note 1), and is only accepted if an EN SI instruction has been executed and the device is not already executing an interrupt routine. Derivative interrupts are not latched in the PCF84C00.
P1.4 to P1.7	50 to 53	I/O	4 bits of Port 1: 8-bit quasi-bidirectional I/O port
P2.0 to P2.1	54, 55	I/O	2 bits of Port 2: 4-bit quasi-bidirectional I/O port
V_{DD}	56	P	power supply: 2.5 V to 5.5 V

Note

1. The interrupt signal must remain active until the vector address (05 H) is present on the address bus.

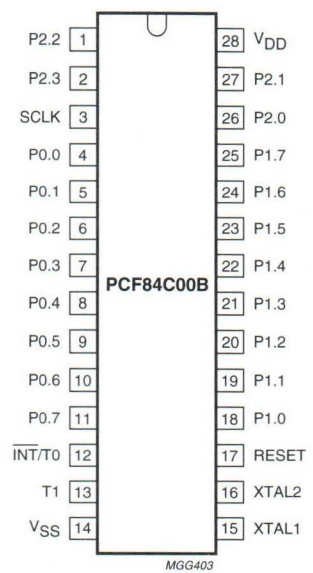


Fig.4 Bottom pinning diagram, 'piggy-back' version PCF84C00B.

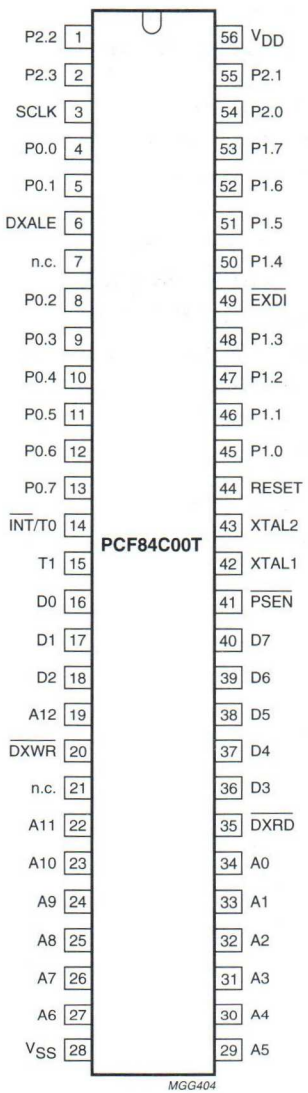


Fig.5 Pinning diagram; ROM-less version PCF84C00T.

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2 GENERAL DESCRIPTION
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4 BLOCK DIAGRAM
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8-bit microcontroller PCF84C12A

1 FEATURES

- Manufactured in silicon gate CMOS process
- 8-bit CPU, ROM, RAM, I/O in a 20-lead package
- 1 kbyte ROM
- 64 byte RAM
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 13 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- Two single-level vectored interrupts:
  - external
  - 8-bit programmable timer/event counter 1
- Two test inputs, one of which also serves as the external interrupt input
- Stop and Idle modes
- Supply voltage: 2.5 to 5.5 V
- Clock frequency: 1 to 16 MHz
- Operating temperature: –40 to +85 °C.

2 GENERAL DESCRIPTION

This data sheet details the specific properties of the PCF84C12A. The shared properties of the PCF84CxxxA family of microcontrollers are described in the *"PCF84CxxxA family"* data sheet, which should be read in conjunction with this publication. Note that the devices described in this data sheet do not feature I^2C-bus compatibility or derivative logic, so the information given in the family data sheet about these features can be ignored.

The PCF84C12A is a general purpose CMOS microcontroller with 1 kbyte of program memory. It includes 64 bytes of RAM and 13 I/O port lines. The instruction set is based on the MAB8048 and is a sub-set of that listed in the *"PCF84CxxxA family"* data sheet.

3 ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF84C12AP	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
PCF84C12AT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

Note

1. Please refer to the Order Entry Form (OEF) for these devices for the full type number to use when ordering. This type number will also specify the required program and ROM mask options.

4 BLOCK DIAGRAM

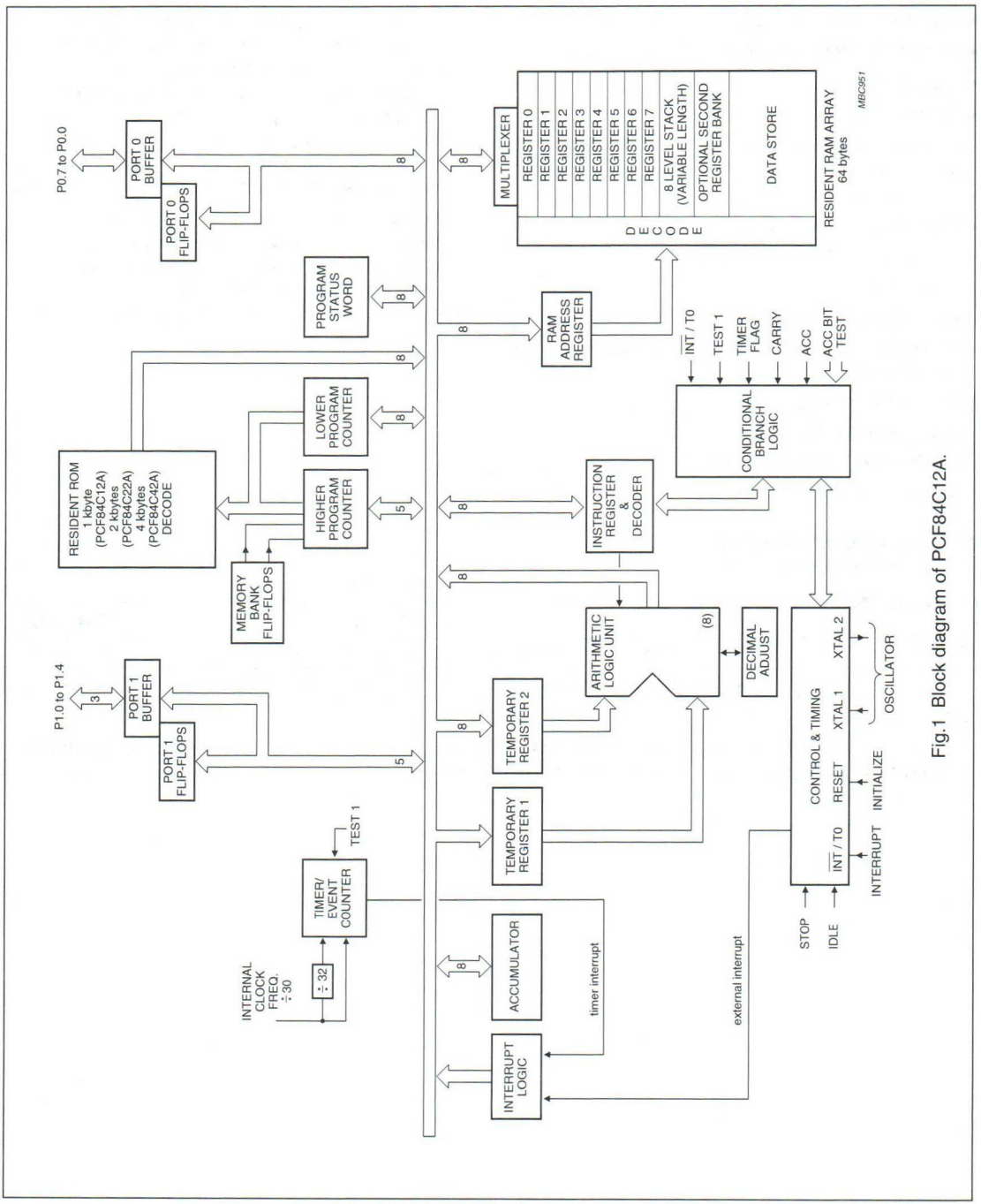


Fig.1 Block diagram of PCF84C12A.

5 PINNING INFORMATION

5.1 Pinning

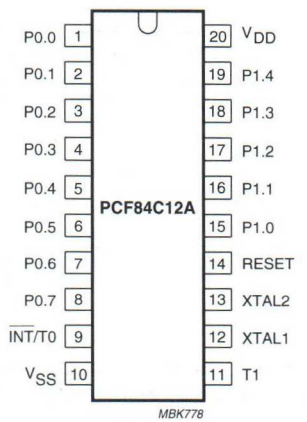


Fig.2 Pin configuration.

5.2 Pin description

Table 1 DIP20 and SO20 packages

SYMBOL	PIN	TYPE	DESCRIPTION
P0.0 to P0.7	1 to 8	I/O	Port 0: 8-bit quasi-bidirectional I/O port
$\overline{INT}$/T0	9	I	Interrupt/Test 0
V_{SS}	10	P	ground
T1	11	I	Test 1/count input of 8-bit timer/event counter 1
XTAL1	12	I	crystal oscillator input or external clock input
XTAL2	13	O	crystal oscillator output
RESET	14	I	reset input
P1.0 to P1.4	15 to 19	I/O	Port 1: 4-bit quasi-bidirectional I/O port
V_{DD}	20	P	positive supply

6 INSTRUCTION SET

Since the I^2C-bus interface, Port 2 and derivative logic are not provided, instructions associated with these functions are not available.

ROM space is restricted to 1 kbyte for the PCF84C12A. Therefore, the instructions SEL MB1/2/3 should be avoided as they would define non-existing program memory banks.

As RAM space is limited to 64 bytes, care should be taken to avoid accesses to non-existing RAM locations.

Refer to the *"PCF84CxxxA family"* data sheet, for a complete description of the instruction set.

7 ROM MASK OPTIONS

ROM CODE	OPTION		
Program/data	Any mix of instructions and data up to ROM size of 1 kbyte.		
Port Output			
P0.0 to P0.7	standard	open-drain	push-pull
P1.0 to P1.4	standard	open-drain	push-pull
Port State after reset			
P0.0 to P0.7	set	reset	–
P1.0 to P1.4	set	reset	–
Oscillator			
Transconductance	LOW (g_{mL})	MEDIUM (g_{mM})	HIGH (g_{mH})

8 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices. See *"Data Handbook IC14, Section: Handling MOS devices"*.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current (except Port 1); output LOW	−10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{DD}	supply current	−50	+50	mA
I_{SS}	ground supply current	−100	+50	mA
T_{stg}	storage temperature range	−55	+150	°C
T_j	operating junction temperature	–	90	°C

10 DC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage	see Fig.3	2.5	–	5.5	V
I_{DD}	operating supply current	note 1; see Figs 4 and 5				
		V_{DD} = 3 V; f_{xtal} = 3.58 MHz (g_{mL})	–	0.3	0.6	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL})	–	1.1	3.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM})	–	1.7	5.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH})	–	2.5	6.0	mA
$I_{DD(idle)}$	supply current (Idle mode)	note 1; see Figs 6 and 7				
		V_{DD} = 3 V; f_{xtal} = 3.58 MHz (g_{mL})	–	0.2	0.4	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL})	–	0.8	1.6	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM})	–	1.2	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH})	–	1.7	5.0	mA
$I_{DD(stp)}$	supply current (Stop mode)	V_{DD} = 2.5 V; notes 1 and 2; see Fig.8	–	1.2	10	µA
Inputs						
V_{IL}	LOW-level input voltage		0	–	$0.3V_{D}$ D	V
V_{IH}	HIGH-level input voltage		$0.7V_{D}$ D	–	V_{DD}	V
I_{LI}	input leakage	$V_{SS} \leq V_I \leq V_{DD}$	−1	–	+1	µA
Outputs						
I_{OL}	LOW-level output sink current	V_{DD} = 5 V; V_O = 0.4 V; see Fig.9	1.6	12	–	mA
I_{OH}	HIGH-level pull-up output source current	V_{DD} = 5 V; V_O = 3.5 V; see Fig.10	40	100	–	µA
		V_{DD} = 5 V; V_O = 0 V; see Fig.10	–	−140	−400	µA
I_{OH1}	HIGH-level push-pull output source current	V_{DD} = 5 V; V_O = 4.6 V; see Fig.11	−1.6	−7	–	mA
Oscillator (see Fig.12)						
g_{mL}	LOW transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
g_{mM}	MEDIUM transconductance	V_{DD} = 5 V	0.9	1.6	3.2	mS
g_{mH}	HIGH transconductance	V_{DD} = 5 V	3.0	4.5	9.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

Notes

1. V_{IL} = V_{SS}; V_{IH} = V_{DD}; open drain outputs connected to V_{SS}; all other outputs, including XTAL2, open (typical values at 25 °C with crystal connected between XTAL1 and XTAL2).
2. V_{IL} = V_{SS}; V_{IH} = V_{DD}; RESET and T1 at V_{SS}; $\overline{INT}$/T0 at V_{DD}; crystal connected between XTAL1 and XTAL2; open drain outputs connected to V_{SS}; all other outputs open.

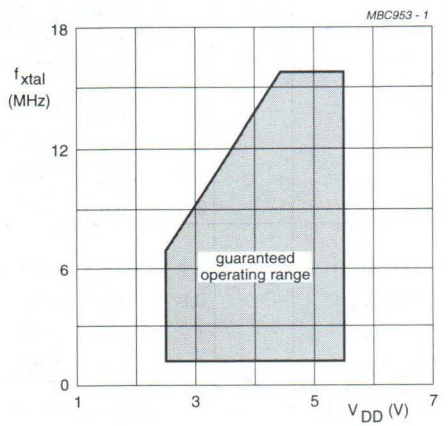
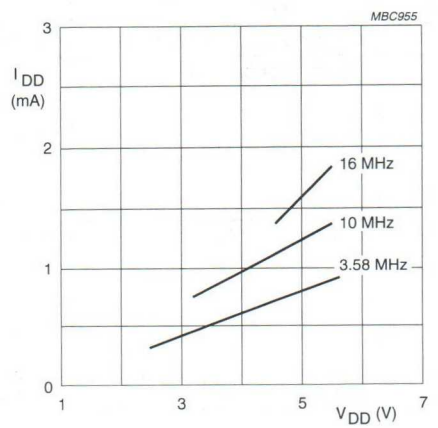
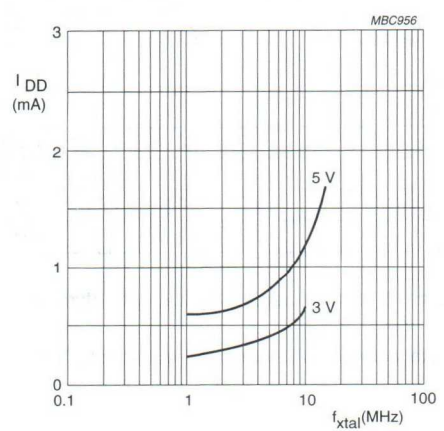


Fig.3 Maximum clock frequency as a function of operating supply voltage (V_{DD}).



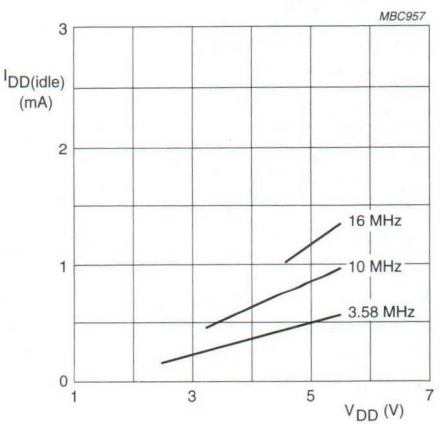
Supply current based on optimal oscillator selection.

Fig.4 Typical operating supply current (I_{DD}) as a function of operating supply voltage (V_{DD}).



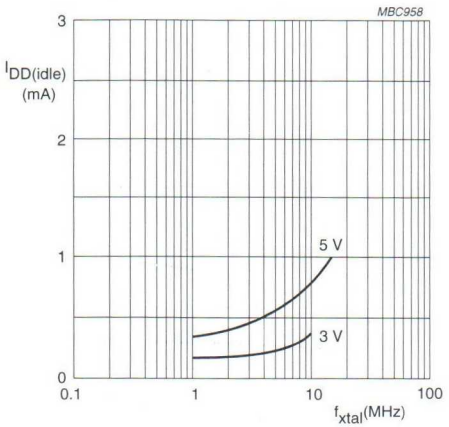
Supply current based on optimal oscillator selection.

Fig.5 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



Supply current based on optimal oscillator selection.

Fig.6 Typical supply current in Idle mode ($I_{DD(idle)}$) as a function of operating supply voltage (V_{DD}).



Supply current based on optimal oscillator selection.

Fig.7 Typical supply current in Idle mode ($I_{DD(idle)}$) as a function of clock frequency (f_{xtal}).

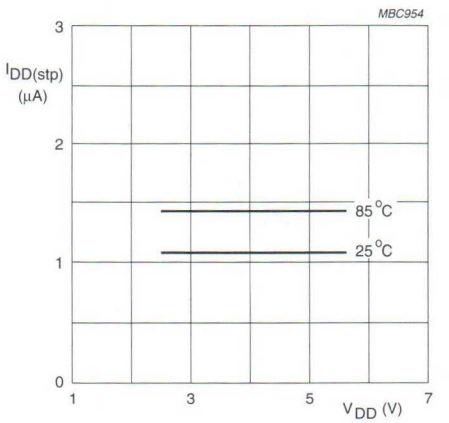
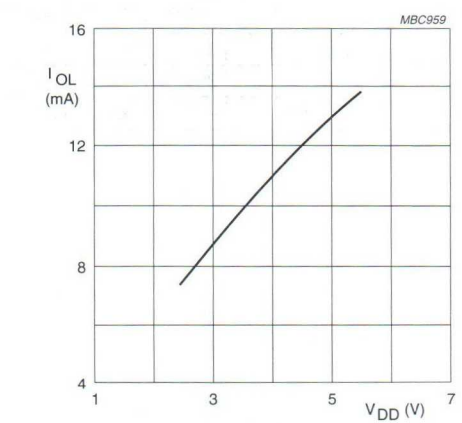


Fig.8 Typical supply current in Stop mode ($I_{DD(stp)}$) as a function of operating supply voltage (V_{DD}).



V_O = 0.4 V.

Fig.9 Typical LOW level output sink current (I_{OL}) as a function of operating supply voltage (V_{DD}).

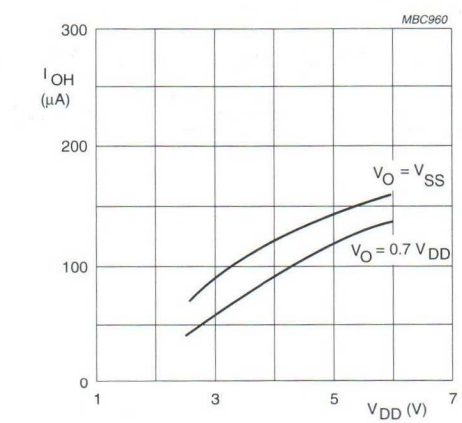
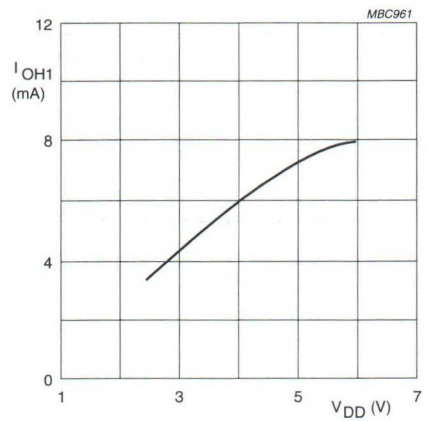


Fig.10 Typical HIGH level pull-up output source current (I_{OH}) as a function of operating supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.11 Typical HIGH-level push-pull output source current (I_{OH1}) as a function of operating supply voltage (V_{DD}).

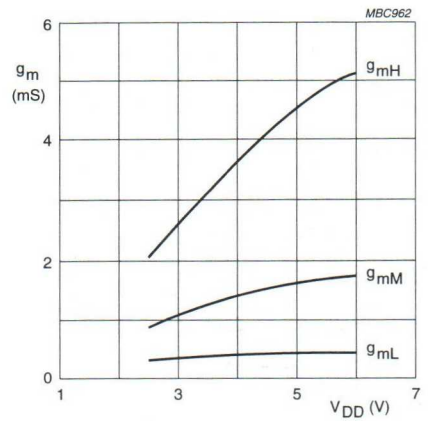


Fig.12 Typical transconductance values (g_m) as a function of operating supply voltage (V_{DD}) for the options g_{vmL}, g_{mM} and g_{mH}.

11 AC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
f_{xtal}	clock frequency	see Fig.3	1	–	16	MHz

Telecom microcontroller PCF84C81A

FEATURES

- Manufactured in silicon gate CMOS process
- 8-bit CPU, ROM, RAM, I/O in a 28-lead package
- 8 kbyte ROM, 256 byte RAM (PCF84C81A)
- I²C-bus interface with multi-master capability
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O Port lines
- High sink current capability on the 8 lines of Port 1
- 8-bit programmable timer/event counter 1
- 3 single-level vectored interrupts:
  - external
  - 8-bit programmable timer/event counter 1
  - I²C-bus
- Two test inputs, one of which also serves as the external interrupt input
- Stop and Idle modes
- Supply voltage: 2.5 to 5.5 V
- Clock frequency: 1 to 16 MHz
- Operating temperature: –40 to +85 °C.

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCF84C81A. The shared properties of the PCF84CxxxA family of microcontrollers are described in the *"PCF84CxxxA family"* data sheet which should be read in conjunction with this publication.

The PCF84C81A is a general purpose CMOS microcontroller with 8 kbytes of program memory and 256 bytes of RAM. In addition to 20 I/O port lines, the microcontrollers provide an on-chip I²C-bus interface. This two-line serial bus extends the microcontroller capabilities when implemented with the powerful I²C-bus peripherals. These include LCD drivers, I/O expanders, telecom circuits, ADC and DAC converters, clock/calendar circuits, EEPROM and RAM and are listed in *"Data Handbook IC12, I²C Peripherals"*.

The instruction set is based on that of the MAB8048 and is a sub-set of that listed in the *"PCF84CxxxA family"* data sheet.

ORDERING INFORMATION (see note 1)

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF84C81AP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCF84C81AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

Note

1. Please refer to the Order Entry Form (OEF) for the full type number to use when ordering. This type number will also specify the required program and the ROM mask options.

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM

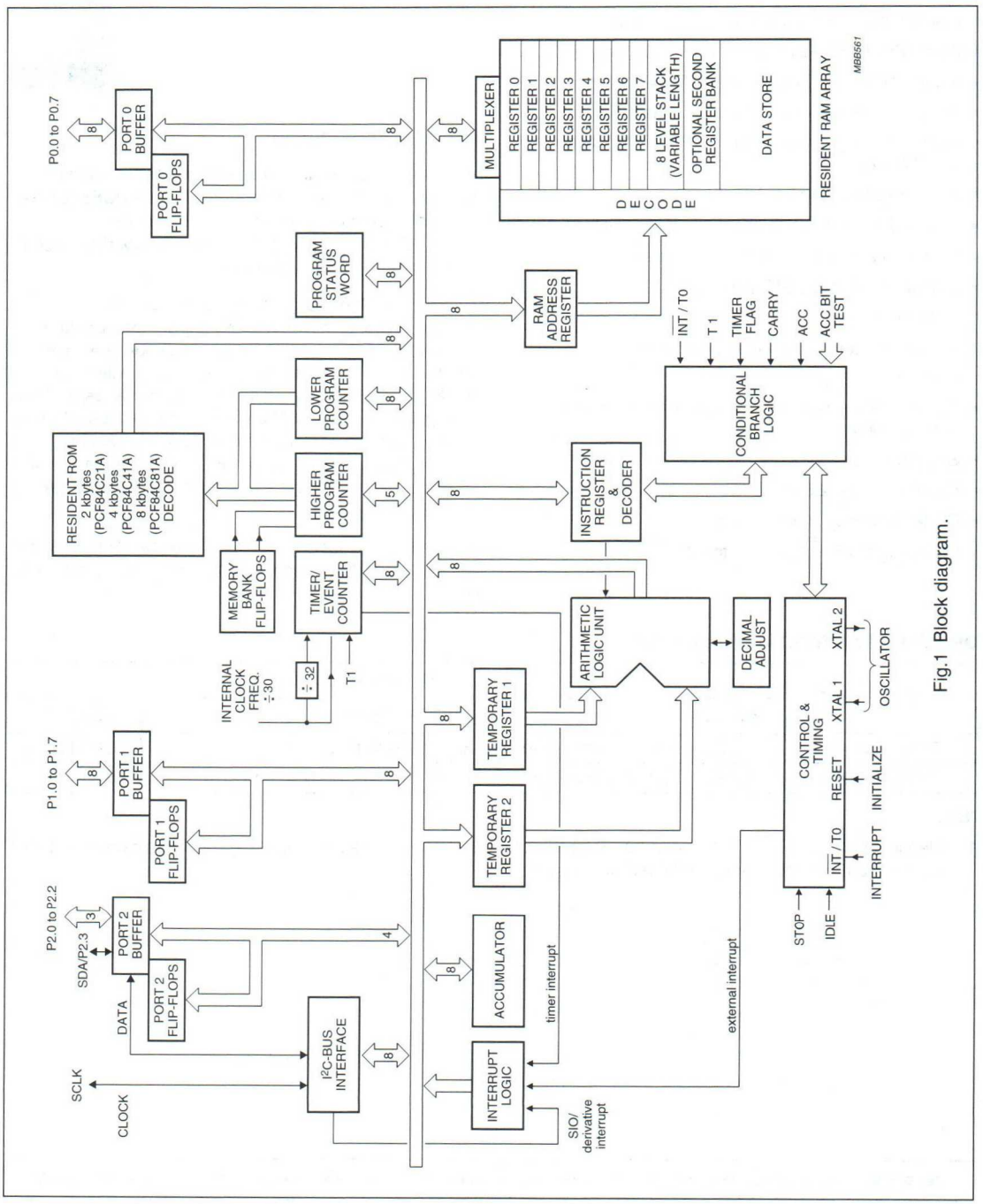


Fig.1 Block diagram.

PINNING INFORMATION

Pinning

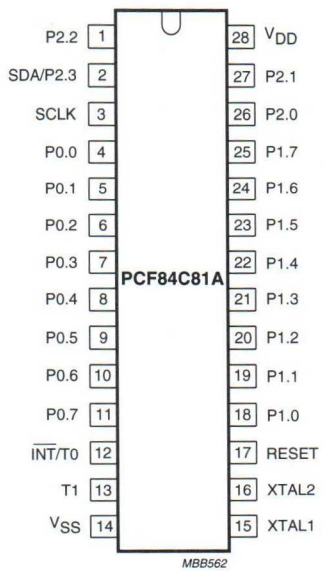


Fig.2 Pin configuration.

Pin description

Table 1 DIP28 and SO28 packages

SYMBOL	PIN	FUNCTION
P2.2	1	1 bit of Port 2: 4-bit quasi-bidirectional I/O port
SDA/P2.3	2	bidirectional data line of the I^2C-bus interface, or 1 bit of Port 2: 4-bit quasi-bidirectional I/O port
SCLK	3	bidirectional clock line of the I^2C-bus interface
P0.0 to P0.7	4 to 11	8 bits of Port 0: 8-bit quasi-bidirectional I/O port
$\overline{INT}$/T0	12	Interrupt/Test 0
T1	13	Test 1/count input of 8-bit timer/event counter 1
V_{SS}	14	ground
XTAL1	15	crystal oscillator input or external clock input
XTAL2	16	crystal oscillator output
RESET	17	Reset input
P1.0 to P1.7	18 to 25	8 bits of Port 1: 8-bit quasi-bidirectional I/O port
P2.0 to P2.1	26 to 27	2 bits of Port 2: 4-bit quasi-bidirectional I/O port
V_{DD}	28	positive supply

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1 INTRODUCTION

This data sheet describes the shared properties of the PCF84CxxxA family of microcontrollers. The family currently consists of:

- PCF84C00
- PCF84C12A; 22A; 42A
- PCF84C21A; 41A; 81A
- PCF84C85A
- PCF84C122; 222; 422; 622; 822
- PCF84C44x; 64x; 84x
- PCF84C846.

For a particular microcontroller, this data sheet should be read in conjunction with the individual data sheet of the specific device. Data sheets can be found in *"Data Handbook IC14, "8048-based 8-bit microcontrollers"*.

The PCD33xxA family of microcontrollers has similar characteristics to the PCF84CxxxA family, but with lower minimum operating voltage, DTMF/modem/musical tone generation and (for most devices) on-chip EEPROM. This family should be considered for telecom-specific applications. Please refer to the *"PCD33xxA family"* data sheet.

2 FEATURES

- 8-bit CPU, ROM, RAM, I/O all in one package
- Up to 8 kbytes ROM
- Up to 256 bytes RAM
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 8 or more quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- 2 or 3 single-level vectored interrupts: external, timer/event counter, (I^2C-bus/derivative)
- Two test inputs, one of which also serves as the external interrupt input
- I^2C-bus serial data interface (most devices)
- Derivative logic (most devices)
- Power-on-reset, Stop and Idle modes
- Supply voltage range: 2.5 to 6 V
- Clock frequency: 1 to 16 MHz
- Operating temperature: −40 to +85 °C
- Manufactured in silicon gate CMOS process.

3 GENERAL DESCRIPTION

The PCF84CxxxA family of microcontrollers provide up to 8 kbytes of program memory and up to 256 bytes of RAM. All devices include flexible I/O ports, an 8-bit programmable timer/event counter and a choice of single-level vectored interrupts. Most devices feature I^2C-bus compatibility. The instruction set is based on that of the well-known MAB8048. Some of the devices have functional equivalents in the MAB84xx family of NMOS controllers. Where the lower power consumption and higher speed of CMOS provide advantages, the PCF84CxxxA devices can be used as direct replacements for their MAB84xx equivalents.

A range of prototyping devices with external program memory and 'Piggy-backs', as well as emulation probes and prototyping systems are available.

4 BLOCK DIAGRAM

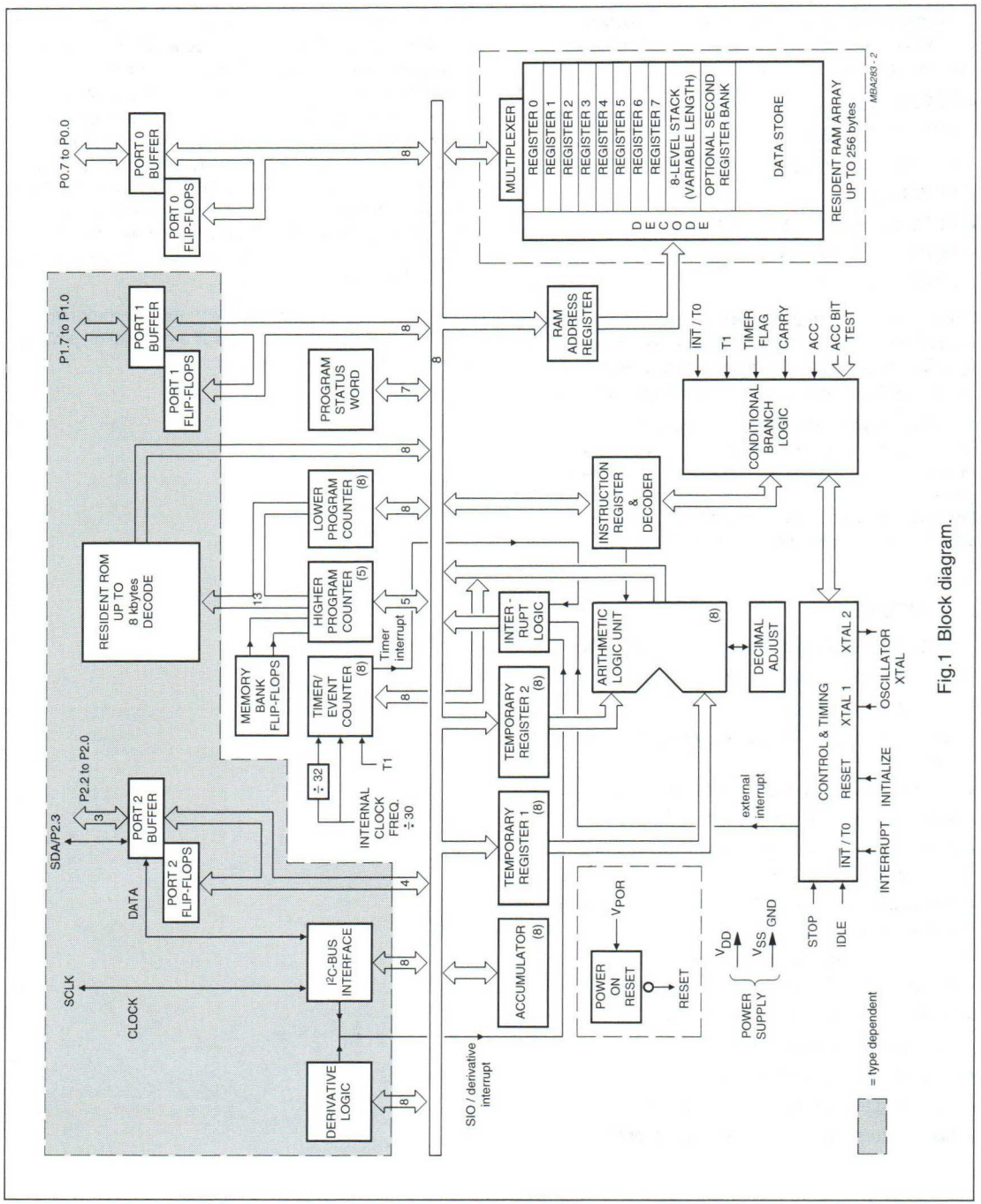


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

For individual pinning configurations consult the data sheet of the specific device.

5.2 Pin description

Table 1 describes the common functions of the devices. For full details of pin descriptions consult the data sheet of the specific device.

Table 1 Common functions

SYMBOL	TYPE	DESCRIPTION
V_{SS}	P	ground
V_{DD}	P	positive supply voltage
XTAL1	I	crystal oscillator/external clock input
XTAL2	O	crystal oscillator output
RESET	I	Reset input
$\overline{INT}$/T0	I	Interrupt/Test 0 input
T1	I	Test 1/count input of 8-bit timer/event counter 1
P0.0 to P0.7	I/O	Port 0: quasi-bidirectional I/O lines
P1.0 to P1.7	I/O	Port 1: quasi-bidirectional I/O lines
P2.0 to P2.2	I/O	Port 2: quasi-bidirectional I/O lines
SDA/P2.3	I/O	bidirectional data line of the I^2C-bus interface/Port 2: quasi-bidirectional I/O line
SCLK	I/O	bidirectional clock line of the I^2C-bus interface

6 FUNCTIONAL DESCRIPTION

6.1 Central processing unit

The PCF84CxxxA family provides an instruction set with arithmetic, logic, branching, input/output and control facilities. Special highlights are the instructions for BCD arithmetic, nibble handling, conditional branches, loop control (DJNZ) and table look-up (MOVP).

Code and execution efficiency is achieved by using a maximum of two bytes and two execution cycles per instruction (see Chapter 7).

6.2 Program memory

The program memory consists of up to 8 kbytes of read-only memory (ROM). Each location is directly addressable by the Program Counter. The program memory is mask-programmed at the factory. Figure 2 illustrates the program memory map.

Four program memory locations are of special importance:

- Location 0: first instruction to be executed after the processor is reset
- Location 3: first instruction of an external interrupt ($\overline{INT}$/T0) routine
- Location 5: first instruction of a I^2C-bus/derivative interrupt routine
- Location 7: first instruction of a timer/event counter interrupt routine.

Only 11 bits of the 13-bit Program Counter function as a counter. The two most significant bits can only be preset. The program memory is therefore, structured into banks of 2 kbytes. Transfer of control to other memory banks is performed by unconditional branches (JMP) or subroutine calls (CALL) when another memory bank has been pre-selected (by SEL MB instruction).

Each program memory bank is further divided into 8 pages of 256 bytes. Indirect (JMPP) and conditional branches cannot cross page boundaries.

6.3 Data memory

Data memory consists of up to 256 bytes of random access memory (RAM). All locations are indirectly addressable using RAM pointer registers. Up to 16 register locations are directly addressable. Data memory also includes an 8-level Program Counter stack addressed by a 3-bit Stack Pointer. All RAM locations make efficient program loop counters if used with the decrement register and test instruction (DJNZ). Figure 3 illustrates the data memory map.

6.3.1 Working registers

Locations 0 to 7 are working registers. They are accessible by efficient one byte/one cycle instructions, thus making these locations suitable for frequently accessed intermediate results.

As an alternative to locations 0 to 7, locations 24 to 31 may be used as working registers. Register bank selection is made by SEL RB0/RB1 instructions. Register bank 1 may be used as an extension of register bank 0, as an alternative register bank for interrupt service or as general purpose data memory.

The first two locations of each bank (R0, R1, R0' and R1') serve as RAM pointers that indirectly address all RAM locations.

6.3.2 Program Counter stack

Locations 8 to 23 may be used as an 8-level Program Counter stack reserving 2 locations per level, or as general purpose RAM. The stack (see Fig.5) saves return addresses and status during interrupt or subroutine servicing. Nesting of subroutines and/or interrupts is permitted up to 8-levels deep.

The 3-bit Stack Pointer always points to the next free stack level. Following device reset, the Stack Pointer points to level 0 (locations 8 and 9). On each subroutine call (CALL) or interrupt, the contents of the Program Counter and bits 4, 6 and 7 of the Program Status Word are transferred to the level indicated by the Stack Pointer. The Stack Pointer increments and points to the next free level. Overflow from level 7 to level 0 occurs after nesting eight levels deep. Further subroutine calls and/or interrupts must not occur at this stage since this would result in loss of program content; overriding level 0 content.

Return from interrupt must be performed by the RETR instruction, which decrements the Stack Pointer and restores the Program Counter and Program Status Word, valid before the interrupt occurred. Return from subroutine should be performed by the RET instruction. In contrast to RETR, RET does not restore the Program Status Word.

As a general rule, the use of RETR in conjunction with a subroutine call is not recommended. The use of RETR must also be avoided with subroutines called from interrupt routines because it prematurely terminates the interrupt state (see Section 6.6).

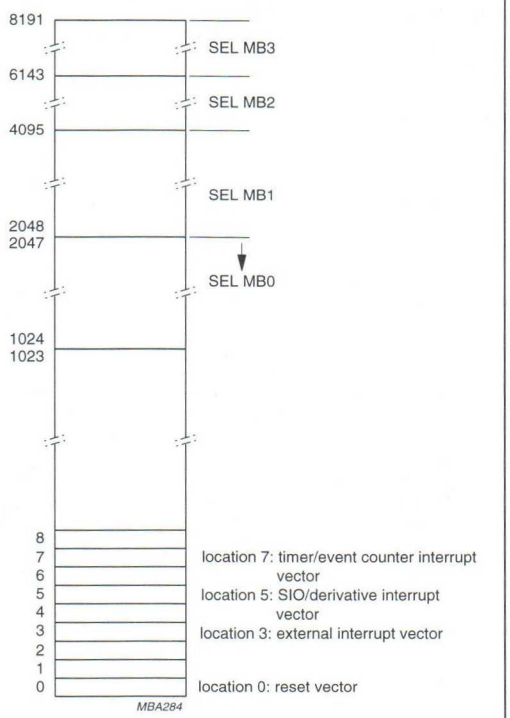


Fig.2 Program memory map.

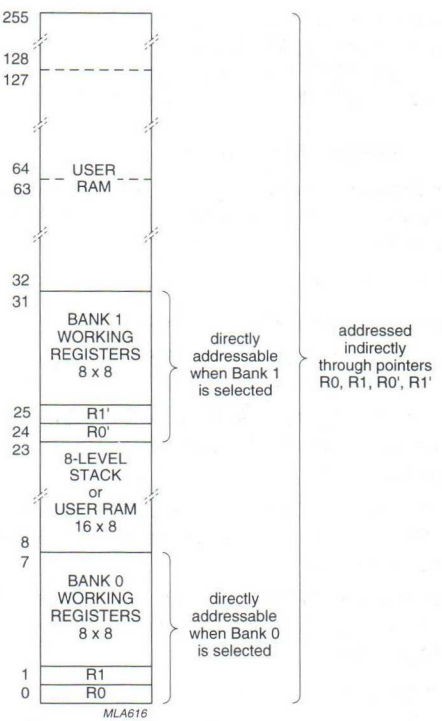


Fig.3 Data memory map.

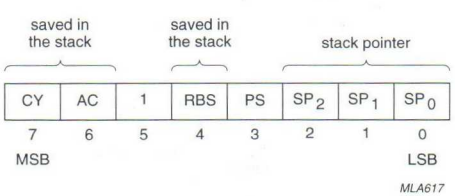


Fig.4 Program Status Word.

6.4 Program Counter

The 13-bit Program Counter is able to address up to 8 kbytes of ROM (see Fig.6). 11 bits (PC0 to PC10) are auto-incrementing. The two most significant bits (PC11 and PC12) must be changed under program control by SEL MB followed by a JMP or CALL instruction.

6.5 Program Status Word

The Program Status Word (PSW) is an 8-bit register in the CPU which stores information about the current status of the microcontroller (see Fig.4).

The PSW bits are:

- Bits 0 to 2: Stack Pointer bits (SP0, SP1, SP2)
- Bit 3: timer Prescaler Select (PS); 0 = modulo-32, 1 = modulo-1 (no prescaling)
- Bit 4: working Register Bank Select (RBS); 0 = register bank 0, 1 = register bank 1
- Bit 5: not used (fixed at 1)
- Bit 6: Auxiliary Carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7: Carry (CY); the carry flag indicates that the previous operation resulted in an overflow of the Accumulator.

All bits can be read using the MOV A, PSW instruction. Bits 0, 1 and 2 are affected by CALL, RET, RETR and interrupts. Bit 3 can be controlled by MOV PSW, A and bit 4 by SEL RB instructions. Bit 6 is set and cleared as a side-effect of ADD and ADDC instructions. Bit 7 is affected by ADD, ADDC, DA, RLC, RRC, CLR C and CPL C instructions.

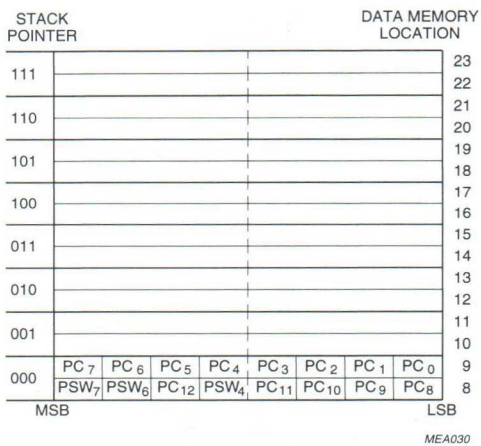


Fig.5 Program Counter Stack.

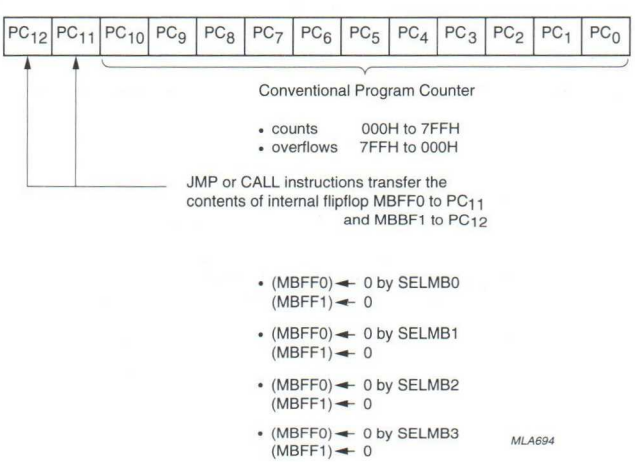


Fig.6 Program Counter.

6.6 Interrupts

External, I²C-bus/derivative and timer/event counter interrupts are handled by the PCF84CxxxA family. The interrupt mechanism is single level, i.e. an executing interrupt routine cannot be pre-empted unless by reset. Further interrupt requests are latched. If several interrupt requests are detected simultaneously, they are honoured according to their priority:

- External interrupt (highest priority)
- I²C-bus/derivative interrupt
- Timer/event counter interrupt (lowest priority).

An interrupt request is only sensed if the corresponding enable flag is set (see Fig.7). When the request is honoured, the contents of the Program Counter and bits 4, 6 and 7 of the Program Status Word are saved on the Program Counter stack. The Program Counter is loaded with the appropriate interrupt vector, thereby indicating the beginning of the interrupt routine. Since the Accumulator is not automatically saved, it must be saved and restored by user software. The interrupt routine must be terminated by the RETR (return and restore) instruction. At least one instruction of the main program will then be executed before another interrupt routine is entered. To avoid erroneous real-time programs, a few words of caution:

- While the interrupt is in progress, the two most significant bits of the Program Counter are frozen at zero. Thus, interrupt routines and subroutines called from interrupt routines must reside entirely in bank 0.
- The SEL MB instruction must not be used in interrupt routines and in subroutines called from interrupt routines. Otherwise, the changed contents of MBFF0 and MBFF1 (see Fig.6) may lead to erroneous JMP and CALL destinations after return from interrupt.
- Subroutines and nested subroutines called from the interrupt routine must all end with RET since RETR clears the Interrupt In Progress flag (IIP), as a side-effect (see Figs 7 and 8). Further pending interrupts would then interfere with the interrupt routine in progress.

6.6.1 External interrupt

A HIGH-to-LOW transition on the $\overline{INT}$/T0 pin is latched in the digital filter/latch if the LOW state exceeds 7 clock periods after a HIGH state of more than 4 clock periods. If the external interrupt is enabled the External Interrupt Flag (EIF) is also asserted, thus constituting a valid external interrupt request. As soon as the IIP is clear, indicating that no interrupt routine is in progress, the external interrupt is invoked by a forced CALL to location 3. The EIF is simultaneously cleared (see Figs 7 and 8). The interrupt routine may acknowledge the interrupt via port lines. Execution of a DIS I (disable external interrupt) instruction cancels a stored interrupt request by clearing both the digital filter/latch and the EIF.

6.6.1.1 Interrupt/Test 0 ($\overline{INT}$/T0)

The $\overline{INT}$/T0 input has two purposes:

- External interrupt input
- Test 0 input.

When used as a Test 0 input (external interrupt disabled) the conditional branch instruction JT0 will cause a jump if $\overline{INT}$/T0 = 1. The conditional branch instruction JNT0 will also cause a jump if $\overline{INT}$/T0 = 0. If $\overline{INT}$/T0 is not used, it must be tied to V_{DD} or V_{SS}.

6.6.2 I²C-bus/Derivative interrupt

The I²C-bus/derivative interrupt is shared between the I²C-bus interface (if available) and the derivative logic (if available). Software polling may be necessary to determine the origin of a request.

An interrupt condition in the I²C-bus interface and/or the derivative logic will pull the PIN line LOW. If the I²C-bus/derivative interrupt is enabled and no interrupt routine is in progress, the I²C-bus/derivative interrupt routine will be invoked by a forced CALL to program memory location 5. The I²C-bus/derivative interrupt routine must include instructions that will remove the cause of the I²C-bus/derivative interrupt and thus reset PIN to its inactive HIGH state (for further details see Section 6.9). For derivative interrupts, consult the data sheet of the specific device.

6.6.3 Timer/event counter interrupt

If the timer/event counter interrupt is enabled, a timer/event counter 1 overflow sets the Timer Interrupt Flag (TIF). As soon as IIP is clear, meaning that no interrupt routine is in progress, the timer/event counter interrupt routine is invoked by a forced CALL to program memory location 7. The TIF is simultaneously cleared (see Figs 7 and 8). Execution of a DIS TCNTI (disable timer/event counter interrupt) instruction cancels a stored interrupt request by clearing TIF.

The timer/event counter interrupt may also be used to simulate a second external interrupt. After an enable timer/event counter interrupt (EN TCNTI), the counter mode is enabled by a STRT CNT instruction which loads FFH (the state preceding overflow) into the counter. A positive edge on the T1 pin will overflow the counter and set TIF.

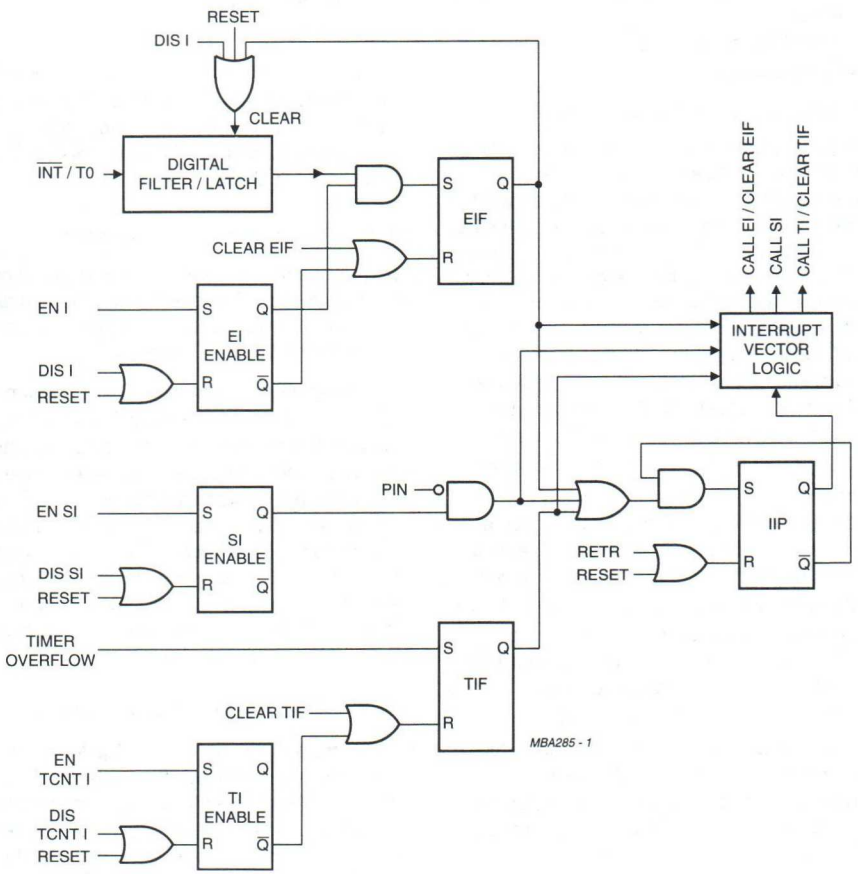


Fig.7 Simplified interrupt logic schematic (the R input overrules the S input for all flags).

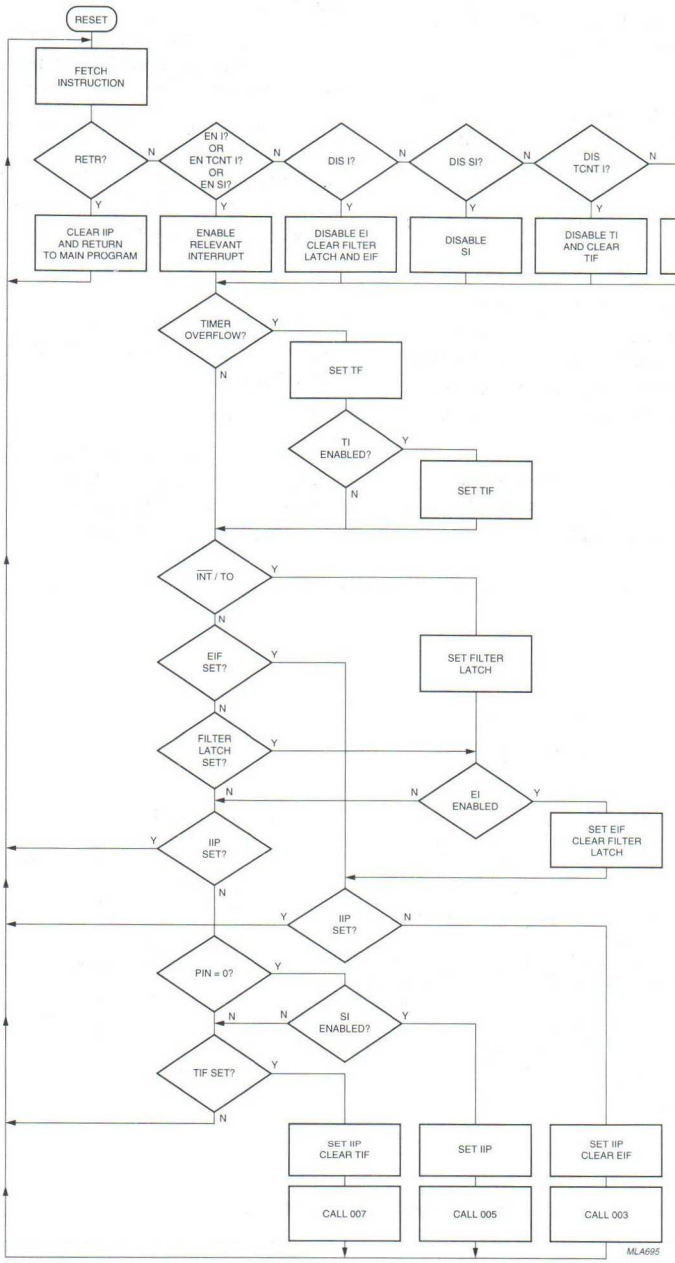


Fig.8 Flow chart illustrating CPU control in the presence of interrupts.

6.7 Timer/event counter 1

An internal 8-bit up counter is provided. The counter can be preset and read by the MOV T, A and MOV A, T instructions.

When the counter is to be used in the timer mode, a STRT T (start timer) instruction must be executed. Depending on the PS bit in the Program Status Word, the counter will increment every machine cycle (PS = 1, $1/30 \times f_{xtal}$) or every 32 machine cycles (PS = 0, $1/960 \times f_{xtal}$). STRT T clears the prescaler (see Fig.9) which is not otherwise accessible.

To count external events a STRT CNT (start event counter) instruction must be executed. A LOW-to-HIGH transition on pin T1 is counted if the HIGH state exceeds 4 clock periods after a LOW state of more than 4 clock periods. The maximum count rate is one increment per machine cycle ($1/30 \times f_{xtal}$).

The timer mode and the event counter mode are both inhibited after reset or by executing a STOP TCNT (stop timer/event counter) instruction (see Fig.9).

In both the timer and in event counter modes, overflow has two effects:

- If the timer/event counter interrupt is enabled TIF is asserted thereby generating a timer/event counter interrupt request (see Section 6.6).
- The Timer Flag (TF) is set. TF can be tested by conditional branch instructions JTF (jump if TF = 1) or JNTF (jump if TF = 0). The JTF and JNTF instruction, as a side-effect, reset TF. The only other way to clear TF is to reset the microcontroller.

6.7.1 Test 1/count input (T1)

The T1 input has two purposes:

- Count input of 8-bit timer/event counter 1 (see Section 6.7)
- Test 1 input.

When used as a Test 1 input the conditional branch instruction JT1 will cause a jump if T1 = 1. The conditional branch instruction JNT1 will also cause a jump if T1 = 0. If T1 is not used, it must be tied to V_{DD} or V_{SS}.

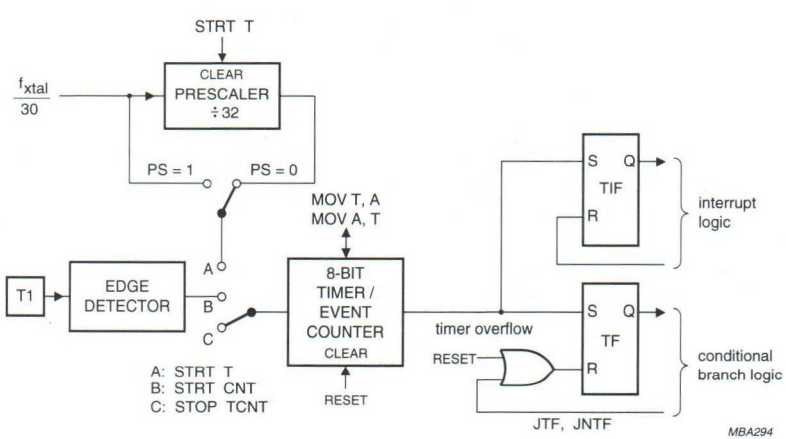


Fig.9 Timer/event counter 1.

6.8 Parallel ports

Three standard quasi-bidirectional I/O ports are defined:

- Port 0: parallel port of 8 lines (P0.0 to P0.7)
- Port 1: parallel port of 8 lines (P1.0 to P1.7)
- Port 2: parallel port of 4 lines (P2.0 to P2.2, SDA/P2.3).

Several members of the PCF84CxxxA family provide all 20 port lines. The eight Port 0 lines (P0.0 to P0.7) are available as a minimum. In addition to the standard ports, many PCF84CxxxA microcontrollers offer a variety of derivative ports. Please consult the data sheet of the specific device.

In general, all parallel ports can be used as either inputs or outputs. Output data written to a port is latched and remains unchanged until rewritten. If the port is used as an input, the external data is not latched and must remain stable until it is accessed by the CPU.

The standard port configuration is illustrated in Fig.11. When a logic 0 is written to the master/slave flip-flop, TR2 and TR3 are both in the OFF condition. TR1 turns ON and drives the output to V_{SS}.

When a logic 1 is written to the master/slave flip-flop, TR1 turns OFF. TR2 and TR3 both turn ON driving the output rapidly to V_{DD}. TR2 remains in the ON condition for the duration of the write pulse only. The constant current source is responsible for keeping the output line high. Sufficient source current is available for a TTL load HIGH level; the line can, however, be overridden by an external device. This is used when the port line serves as an input, but it may also be useful for wired-OR applications. In the latter case, unnecessary current through external devices is avoided since repeated logic 1 write operations will not activate TR2. The booster transistor TR2 is only asserted during a LOW-to-HIGH transition of the master/slave flip-flop. If the port line is to be used as an input, a logic 1 should first be stored in the master/slave flip-flop to turn TR1 OFF.

Access to Ports 0, 1 and 2 is provided by the parallel input/output instructions IN, OUTL, ANL and ORL. IN inputs port data to the Accumulator. OUTL outputs Accumulator data to the port. ANL and ORL are used for data manipulation in the port flip-flop. In contrast to Ports 0, 1 and 2, derivative ports are accessed by the derivative input/output instructions MOV, ANL and ORL. ANL and ORL are used for data manipulation in the port flip-flop. MOV is used for all data transfers between port and Accumulator. The source data for the Accumulator can be loaded from either the port line or the port flip-flop. Two derivative addresses are therefore provided per port (see Table 2).

All standard and derivative port accesses are performed by two-cycle instructions. Their instruction timing is shown in Fig.11. For input, data on port lines is sensed during timeslots 3 and 4 of machine cycle 2 (see Sections 6.10 and 6.11). For output, the data change occurs in timeslot 7. For OUTL, data changes during machine cycle 1. For ANL, ORL and MOV Dx, A, data changes during machine cycle 2.

Table 2 Derivative port address pair

ADDRESS	TYPE	ACCESS
8-bit line address	R	derivative port line
8-bit flip-flop address	R/W	derivative port flip-flop

Three mask-programmable options for port output configuration are available:

Option 1 **Standard Port**; quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and p-channel booster transistor TR2. TR2 is only active for 1 clock cycle during LOW-to-HIGH transitions (see Fig.11).

Option 2 **Open-drain**; quasi-bidirectional I/O with only an n-channel open drain output. Application as an output requires connection of an external pull-up resistor (see Fig.12). If unused, an option 2 output should be tied to V_{SS}. This keeps the input path from floating, thereby avoiding undesirable current flow through input stages.

Option 3 **Push-pull**; drive capability of the output will be 5 mA (typ.) at V_{DD} = 3 V in both polarities. Since short circuit currents would flow during input, push-pull lines must only be used as outputs (see Fig.13).

If available, SDA/P2.3 is shared between the I^2C-bus interface and the parallel Port 2. Therefore, only the open-drain configuration is permitted for SDA/P2.3. For the remaining standard port lines (P0.0 to P2.2), all three options are generally available.

Besides port output mask options, the port flip-flop state, after reset, may be specified for each individual port line (except SDA/P2.3). Usually the 'set option' will be selected, which avoids short-circuits for ports intended as inputs. However, there may be cases in which the port should output a logic zero after reset. The user may then specify the 'reset option' for certain port lines.

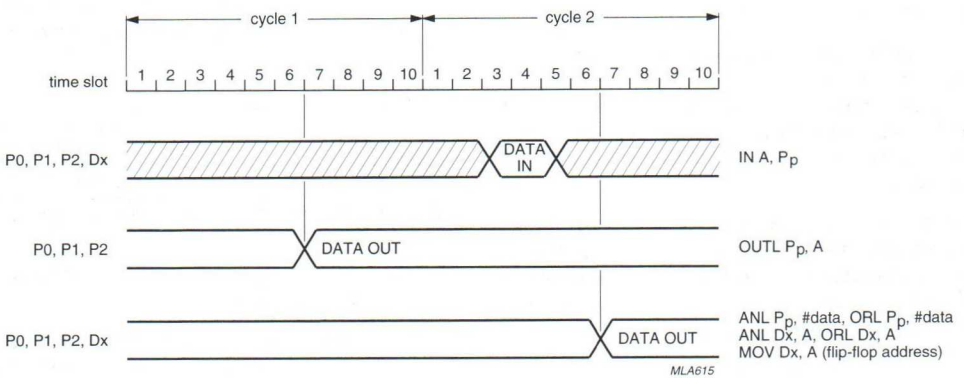


Fig.10 Input /output timing of standard and derivative ports.

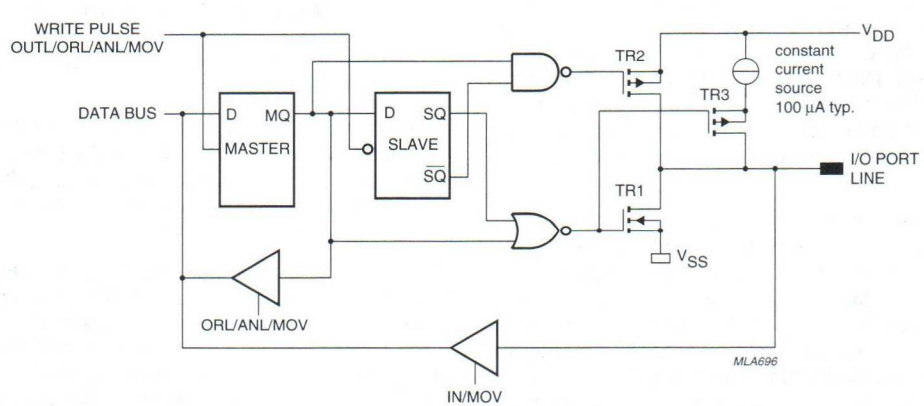


Fig.11 Standard output with switched current source.

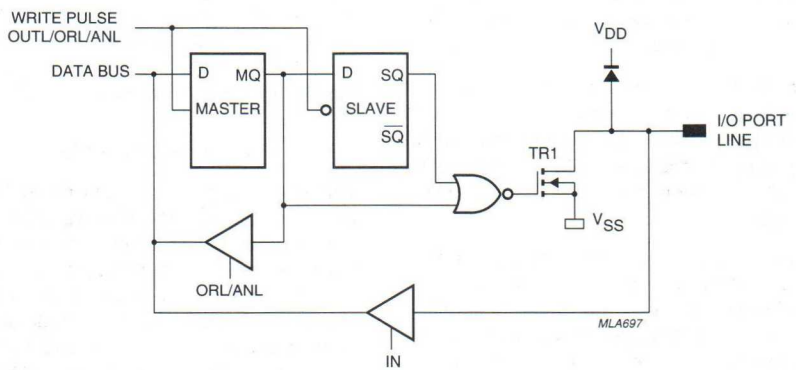


Fig.12 Open drain output.

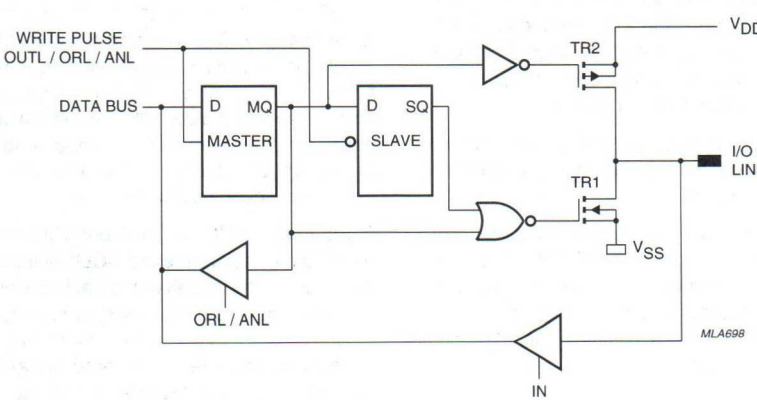


Fig.13 Push-pull output.

6.9 I²C-bus interface

Many members of the PCF84CxxxA family have a serial I/O interface - the I²C-bus or 'Inter-Integrated Circuit Bus'. This two-line serial bus extends the microcontroller capabilities when implemented with the powerful I²C-bus devices. Details of these devices can be found in *"Data Handbook IC12, I²C Peripherals"*.

Microcontrollers that do not have a I²C-bus interface can simulate it by software, by using port pins. However, such microcontrollers must continuously monitor the serial bus. As well as degrading the maximum data transfer rate, this approach may also consume significant processing and memory resources.

If available, however, the I²C-bus interface detects the valid 7-bit I²C-bus address of the device, transfers serial data and provides data conversion to and from parallel format, all without disrupting program execution. When a complete byte has been transferred, an interrupt is requested by which the next data byte can be written to or read out of the I²C-bus interface. The I²C-bus interface also facilitates the implementation of multimaster systems in which two or more microcontrollers communicate via the same I²C-bus. An automatic arbitration procedure resolves bus conflicts.

The I²C-bus consists of a bidirectional clock line (SCL) and a bidirectional data line (SDA). Whereas SCL uses the dedicated pin SCLK, SDA and Port line P2.3 share the pin, SDA/P2.3. When the I²C-bus interface is enabled, SDA/P2.3 is disabled as a port line. Input signals on SCLK and SDA are filtered for enhanced noise immunity. When used as outputs, SCLK and SDA/P2.3 require an external pull-up resistor because they are open drain. If unused, SCLK and SDA/P2.3 should be tied to V_{SS} (see Section 6.8, Option 2, Open-drain output).

Communication between CPU and I²C-bus interface is handled through the four I²C-bus interface registers S0, S0', S1 and S2 (see Fig.14).

A detailed description of the I²C-bus specification, with applications, is given in the brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011. Data handbook IC12, *"I²C Peripherals"* also contains this information, and data on all current I²C-bus slave devices.

6.9.1 Data shift register (S0)

The data shift register converts serial data to a parallel format and vice versa. The leading bit of a serial transfer corresponds to the most significant bit of the parallel word. An interrupt request is issued after transfer of a complete byte and after detection of the valid I²C-bus address. Register S0 is read by MOV A, S0. It is written by MOV S0, A or MOV S0, #data if the ESO (Enable Serial I/O) bit in the Status Register (S1) is set.

6.9.2 Address register (S0')

The address register contains the 7-bit I²C-bus address of the device and the ALS (Always Selected) bit. When ALS is zero, which is the recommended mode of operation, bus transfers are ignored unless the valid device address immediately follows the start condition. Besides the stored 7-bit address, the 'general call address' (pre-defined as zero) is also acceptable as a valid address. If ALS is set, however, any transfer on the bus will be stored in the data shift register.

The address register S0' is write-only. It can be written by MOV S0, A and MOV S0, #data if the ESO (Enable Serial I/O) bit in the Status Register (S1) is zero.

6.9.3 Clock control register (S2)

The Clock Control Register defines the frequency of f_{SCLK} as the microcontroller clock frequency divided by an integer (see Table 3). It also defines ASC (Asymmetrical Clock) and ACK (Acknowledge).

If ASC = 1, the generated SCLK has a duty cycle of approximately 75%. The asymmetrical clock limits the I²C-bus transmission rate to below 55 kHz. Divisors 39, 45 and 51 are not allowed if ASC = 1. However, an SCLK duty cycle of approximately 50% results if ASC = 0. This permits I²C-bus transmission rates of up to 100 kHz. All divisors of Table 3 are available. It is, therefore, recommended to select ASC = 0.

For the normal I²C-bus protocol ACK must be set. After each byte transfer an extra SCLK pulse is generated during which the receiver may acknowledge reception. If ACK is zero, no acknowledge phase is available. This mode is temporarily used when a master/receiver refuses the acknowledgement in order to signal an end of transmission to the slave transmitter (see Section 6.9.4.9).

The Clock Control Register (S2) is write-only. It can be written by MOV S2, A and MOV S2, #data.

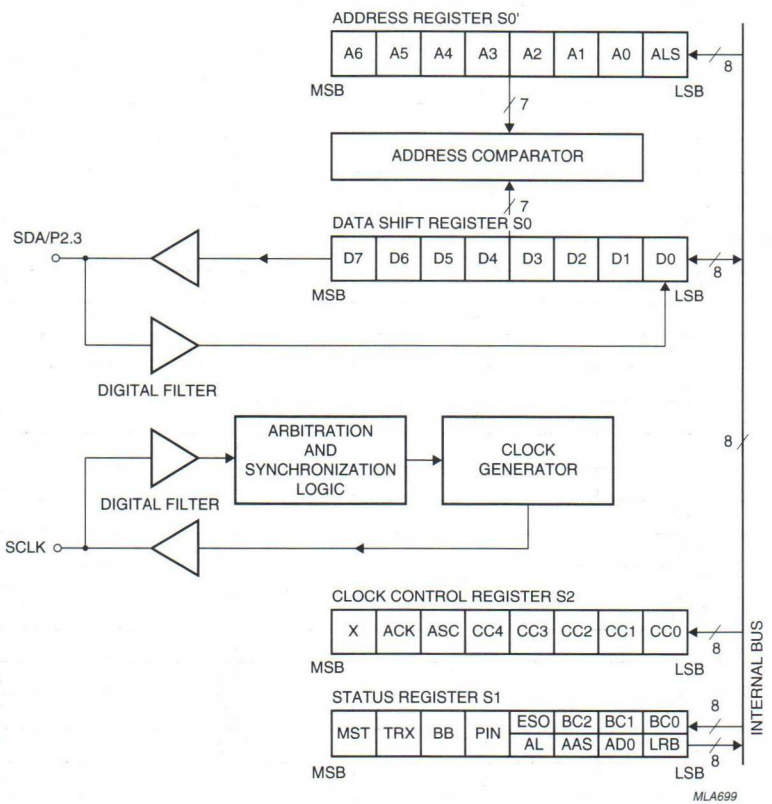


Fig.14 Block diagram of the I²C-bus interface.

Table 3 f_{SCLK} as defined by Clock Control Register (S2)

CC4 TO CC0 (HEX)	f_{xtal} DIVISOR (Division Factor)	f_{SCLK} (kHz) at		
		f_{xtal} = 3.58 MHz	f_{xtal} = 10 MHz	f_{xtal} = 16 MHz
00	forbidden	–	–	–
01	39	91.8	256.4(1)	410.3(1)
02	45	79.5	222.2(1)	355.6(1)
03	51	70.2	196.1(1)	313.7(1)
04	63	56.8	158.7(1)	254.0(1)
05	75	47.7	133.3(1)	213.3(1)
06	87	41.1	114.9(1)	183.9(1)
07	99	36.2	101.0(1)	161.6(1)
08	123	29.1	81.3	130.1(1)
09	147	4.4	68.0	108.8(1)
0A	171	20.9	58.5	93.6
0B	195	18.4	51.3	82.1
0C	243	14.7	41.2	65.8
0D	291	12.3	34.4	55.0
0E	339	10.6	29.5	47.2
0F	387	9.2	25.8	41.3
10	483	7.4	20.7	33.1
11	579	6.2	17.3	27.6
12	675	5.3	14.8	23.7
13	771	4.6	13.0	20.8
14	963	3.7	10.4	16.6
15	1155	3.1	8.7	13.9
16	1347	2.7	7.4	11.9
17	1539	2.3	6.5	10.4
18	1923	1.9	5.2	8.3
19	2307	1.6	4.3	6.9
1A	2691	1.3	3.7	5.9
1B	3075	1.2	3.3	5.2
1C	3843	0.9	2.6	4.2
1D	4611	0.8	2.2	3.5
1E	5379	0.7	1.9	3.0
1F	6147	0.6	1.6	2.6

Note

1. Not permitted; maximum f_{SCLK} = 100 kHz in I^2C-bus systems.

6.9.4 STATUS REGISTER (S1)

The Status Register controls the I²C-bus interface and provides feedback concerning on-going bus transfers. Register S1 can be accessed by MOV A, S1; MOV S1, A and MOV S1, #data. The lower nibble of the Status Register is twofold: control bits BC0, BC1, BC2 and ESO can only be written, whereas feedback bits LRB, AD0, AAS and AL can only be read. Table 4 describes the status bits.

The status bits interact in intricate ways with each other. This must be kept in mind when an I²C-bus application is programmed.

6.9.4.1 Master bit (MST) and Transmitter bit (TRX)

MST and TRX together define the state of the I²C-bus interface. When not engaged in a bus transfer MST and TRX should always be at zero, the slave/receiver state (see Fig.15). Return to this state is always performed by software. If the previous state was the master state, the transition (to slave/receiver by MOV1, #D8H) involves a stop condition which, as a consequence, clears both MST and TRX.

The transition to the master/transmitter state is also a programmed event. However, transitions to the master/receiver and the slave/transmitter states occur automatically if ALS = 0 (standard I²C-bus protocol). A slave/receiver becomes a slave/transmitter if R/$\overline{W}$ = 1 in its valid address (following the start condition). A master/transmitter becomes a master/receiver if R/$\overline{W}$ = 1 in the transmitted address.

6.9.4.2 Pending Interrupt Not bit (PIN)

If MST = 1 or, if ALS = 1, PIN is set to zero after every byte transfer. Conversely, PIN becomes zero when a valid address is detected and after each byte of the following transfer. In addition, the serial interrupt request, PIN = 0 initiates 'clock synchronization', i.e. the SCLK line is pulled to V_{SS} as long as PIN = 0. With this feature a slave may slow down a master, thus providing time to read the Data Register (in the case of a slave/receiver) or to write to the data register (in the case of a slave/transmitter). PIN is cancelled by an access to register S0 or by explicitly setting PIN to one.

If the I²C-bus/derivative interrupt is disabled, the I²C-bus interface may be serviced by testing PIN directly in user software.

6.9.4.3 Bus Busy bit (BB)

The Bus Busy bit (BB) is controlled by the I²C-bus interface or by software in the bus master to generate the start and stop conditions. When a master clears BB (by MOV S1, #D8H), the I²C-bus interface automatically clears MST and TRX, thereby returning to the slave/receiver state (see Fig.15). If BB = 1, write access to S1 is inhibited, except for the master or an addressed slave. Should BB be inadvertently set by excessive noise on the bus, the deadlock can be resolved by two consecutive MOV S1, #18H, the first of which just clears BB.

When a slave/transmitter detects an end of transmission (signalled by the lack of an acknowledgment from the master receiver), it has to access S1 in order to cancel PIN and to become slave/receiver. However, BB should remain set. This is reflected by MOV S1, #38H as illustrated in Fig.15. With PIN = 1, 'clock synchronization' terminates, enabling the master to generate the stop condition.

A start condition must only be generated when BB = 0; otherwise the I²C-bus interface will respond as if bus arbitration has been lost (see Section 6.9.4.4).

6.9.4.4 Arbitration Lost bit (AL)

The AL bit is set by the I²C-bus interface when it loses a bus arbitration in the master/transmitter mode. MST and TRX are cleared simultaneously to enable the interface, now in slave/receiver mode, to determine if it is validly addressed by the device that won the arbitration. PIN is activated when the byte transfer is complete. AL will be cleared when the serial interrupt is cancelled.

6.9.4.5 Addressed As Slave bit (AAS)

AAS is set by the I²C-bus interface following a start condition when the valid address is detected (ALS = 0 in register S0') or when the first byte is received (ALS = 1 in register S0'). AAS is cleared when the serial interrupt is cancelled.

6.9.4.6 Address Zero bit (AD0)

AD0 is set, independently of ALS, by the I²C-bus interface when byte 00H, the 'general call' address, is detected following a start condition. AD0 is cleared after a repeated start or a stop condition.

6.9.4.7 *Last Received Bit (LRB)*

LRB corresponds to the last bit transferred. If ACK = 1, LRB contains the acknowledgement bit. It remains valid as long as PIN = 0.

6.9.4.8 *Enable Serial I/O bit (ESO)*

When ESO = 0 access to register S0' is enabled. SCLK is in the high-impedance state and SDA/P2.3 is available as a normal port line.

When ESO = 1 the I^2C-bus interface and access to register S0 is enabled. Only when ESO = 1 may the other bits of register S1 be changed. SCLK and SDA/P2.3 are enabled as serial clock and data lines, respectively.

To avoid bus deadlock, ESO must be set to zero prior to the execution of the STOP instruction.

6.9.4.9 *Bit Counter bits (BC0, BC1 and BC2)*

The bit counter bits BC0, BC1 and BC2 should all be at zero for normal I^2C-bus operation. The bit counter is always cleared by a start condition. Therefore, all eight bits of the first byte are transferred.

If a non-zero bit counter value is chosen, it is only valid for one register S0 transfer since the counter decrements to zero. An important use of the bit counter arises when a master/receiver signals an end of transmission by sending a negative acknowledge after the last byte received. To do this, the last byte is received with bit ACK = 0 in register S2. The negative acknowledge is then issued by setting the bit counter to one and 'receiving' one bit from the HIGH level available on the SDA line.
The slave/transmitter interprets the same signals as a negative acknowledgement.

Table 4 Overview of Status Register bits

BIT	NAME	TYPE	DESCRIPTION
MST	Master	R/W	MST = 0: slave (SCLK input). MST = 1: master (SCLK output).
TRX	Transmitter		TRX = 0: receiver (SDA/P2.3 input. TRX = 1: transmitter (SDA/P2.3 output).
BB	Bus Busy	R/W	BB = 0: bus inactive (R)/generates stop condition (W). BB = 1: bus busy (R)/generates start condition (W).
PIN	Pending Interrupt Not	R/W	PIN = 0: serial interrupt pending (after byte transfer, valid address or lost arbitration). SCLK line forced to V_{SS}. PIN = 1: no serial interrupt pending.
ESO	Enable Serial Output	W	ESO = 0: I^2C-bus interface disabled/write access to S0' possible. ESO = 1: I^2C-bus interface enabled write access to S0 possible.
BC0 to BC2	Bit Counter 0 to 2	W	3-bit binary value of 0 to 7, counting down the number of bits transferred (0 used for complete byte).
AL	Arbitration Lost	R	Set: when a bus conflict is lost. Reset: when corresponding serial interrupt (PIN) is cancelled.
AAS	Addressed As Slave	R	Set: following a start condition if valid address is detected (ALS = 0) or if first byte is received (ALS = 1). Reset: when corresponding serial interrupt (PIN) is cancelled.
AD0	Address zero	R	Set: following a start condition if byte 00H ('general call' address) is detected. Reset: after a repeated start or a stop condition.
LRB	Last Received Bit	R	Set or Reset depending on the value of the last bit transferred, acknowledgement bit if ACK = 1.

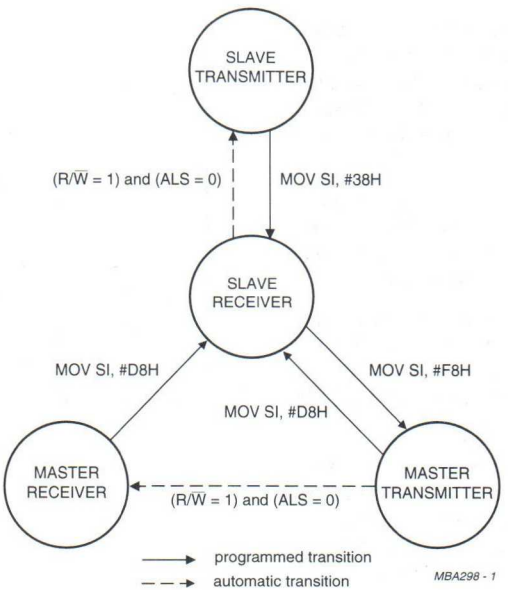


Fig.15 State diagram of the I²C-bus interface.

6.10 Timing

Every machine cycle consists of 10 time slots which are again subdivided into 3 clock periods each (see Fig.16).

Permitted clock frequencies range from 1 MHz to a maximum, which is a function of the supply voltage. At $V_{DD} \geq 4.5$ V, a 16 MHz maximum clock frequency is guaranteed.

The clock signal may be internally generated by an on-chip oscillator. Alternatively, an external clock may be applied to pin XTAL1. In this configuration, a short circuit with an internal pull-up transistor on XTAL1 may occur while the oscillator is inhibited (see Section 6.11). Care should be taken to avoid excessive current flow.

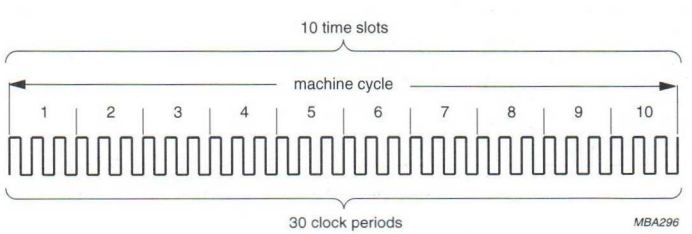


Fig.16 Timing of a machine cycle.

6.11 Oscillator

The on-chip oscillator basically consists of an inverter stage which includes a feedback resistor and load capacitors (see Fig.17). In most applications, a quartz crystal will be connected between XTAL1 and XTAL2. Alternatively, a ceramic resonator or an inductor may be used as a timing element.

When the supply voltage drops below the power-on reference level, the oscillator is inhibited. The internal oscillator can also be inhibited by the STOP instruction under software control (see Section 6.13.2).

The transconductance (g_m) of the inverter stage can be mask-programmed, thereby optimizing the oscillator for a specific frequency and resonator. Three standard transconductance options, referred to as LOW, MEDIUM and HIGH, can be specified by the user.

With $C_1 = C_2 = 10$ pF on-chip, external capacitors are not required for quartz oscillators. However, for adequate frequency stability, PXE resonators need external capacitors in the order of the static resonator capacitance C_0, such as external $C_1 = C_2 = 30$ to 100 pF.

Oscillator start-up time depends mainly on the external timing element. The start-up time of a quartz crystal is several milliseconds because of the narrow crystal bandwidth. For proper oscillator start-up, the transconductance (g_m) of the inverter stage must fulfil relationship (1); shown below.

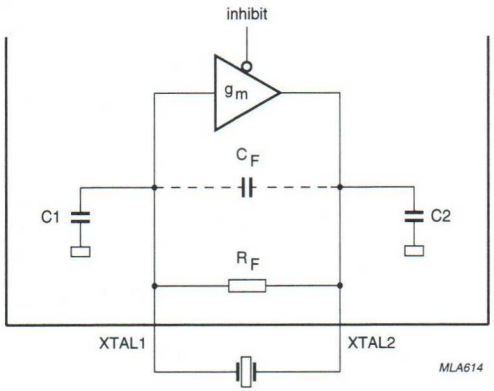


Fig.17 Oscillator with integrated elements.

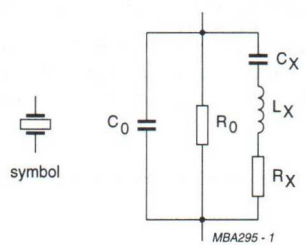


Fig.18 Crystal unit equivalent circuit.

Table 5 Notation to relationship (see Figs 17 and 18)

SYMBOL	DEFINITION
R_X	resonator series resistance
C_0	static resonator capacitance
R_0	resonator loss resistance
R_P	$R_0 // R_F$
R_F	feedback resistor
C_L	$C1 \times C2/(C1 + C2)$ (load capacitance)
C_F	parasitic feedback capacitance (typically 2 pF on-chip, external value depends on printed-circuit board wiring)
ω	$2\pi f_{osc}$

$$4.2\left[R_X\omega^2(C_L + C_0 + C_F)^2 + \frac{1}{R_P}\right] < g_m < \frac{C1 \times C2}{\left[R_X(C_0 + C_F)^2 + \frac{1}{\omega^2 R_P}\right]} \quad (1)$$

6.12 Reset

To ensure proper start-up, the microcontroller must be initialized to a defined starting condition. The device executes the first instruction 1866 clock cycles after the falling edge of the internal reset.

6.12.1 Passive external reset

A passive reset is generated by the RC circuit illustrated in Fig.19. While V_{DD} rises, the discharged C_{reset} keeps the RESET pin near the V_{DD} level. When V_{DD} crosses the power-on reference level (V_{ref}) the power-on reset circuit generates a reset pulse of approximately 50 µs. This pulse is without effect since it feeds into the reset signal forced by the one on the RESET pin. The f_{xtal} dependent minimum V_{DD} must be reached before the voltage on RESET drops below $V_{IH} = 0.7V_{DD}$. This translates into a lower bound for $C_{reset}R_{reset}$ equal to twice the rise time of V_{DD} (for linearly rising V_{DD}) or eight times the time constant of V_{DD} (for exponentially rising V_{DD}). The internal diode rapidly discharges C_{reset} when V_{DD} falls off, ensuring reliable reset even after short interruptions of supply voltage. To avoid overload of the internal diode, an external diode should be added in parallel if $C_{reset} > 2.2$ µF.

6.12.2 Active external reset

An active reset can be generated by driving the RESET pin HIGH from an external logic device. Such an active reset pulse should not fall off before V_{DD} has reached its f_{xtal} dependent minimum operating value.

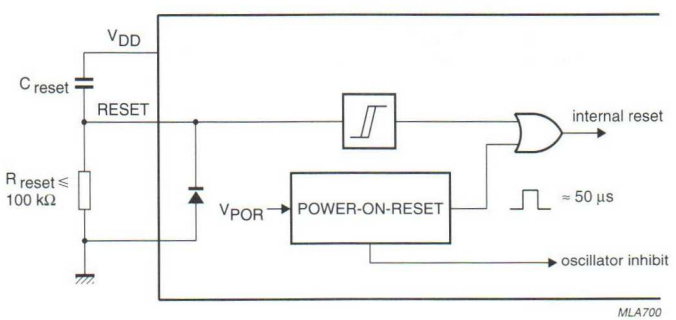


Fig.19 Passive external reset

6.12.3 INTERNAL RESET

In systems where V_{DD} reaches its f_{xtal} dependent minimum operating value before the clock f_{xtal} is applied, reset can be performed without external components. This condition is generally fulfilled with quartz and PXE resonators since oscillator start-up takes several milliseconds. Besides, rapid power-up is usually available in battery-powered systems.

If the internal power-on reset is used the RESET pin should be connected to V_{SS}. When V_{DD} increases above the power-on reference level V_{ref}, the power-on-reset circuit generates a reset pulse of approximately 50 µs. This pulse guarantees proper initialization under the conditions defined above.

The power-on reference level V_{ref} is a mask option. The user can select a reference voltage between 1.2 V and 3.6 V in discrete steps of 100 mV. The accuracy of the reference voltage is ±500 mV for the V_{ref} range 1.2 V to 3.0 V and ±800 mV for the V_{ref} range 3.1 V to 3.6 V. The chosen V_{ref} should have sufficient margin regarding the minimum intended V_{DD}.

A mask option without an internal power-on reset circuit is also available. It is recommended if the user does not intend to use the internal power-on-reset circuit. In this case, the supply current requirements in Stop mode (see Section 6.13.2) will reduce to the level of leakage currents, i.e. virtually zero at ambient temperature.

6.12.4 RESET STATE

After a reset, the device state is characterized as follows:

- Program Counter 0
- Memory bank 0
- Register bank 0 - Stack Pointer 0 (location pair 8 and 9)
- All interrupts disabled
- Timer/event counter 1 stopped and cleared
- Timer prescaler modulo-32 (PS = 0)
- Timer flag cleared
- All port flip-flops (except SDA/P2.3) set to 1 (set option) or 0 (reset option) as selected by the user
- SDA/P2.3 is high-impedance with the port flip-flop set to 1
- SCLK is high-impedance
- I^2C-bus interface disabled (ESO = 0) and in slave/receiver mode (S0, S0', S1 and S2 cleared except for PIN = 1)
- Idle and Stop modes cancelled.

6.13 Reduced power modes

6.13.1 IDLE MODE

The Idle mode is very useful in low-power applications. When all computational tasks are completed, the device can be put into standby instead of into a busy waiting loop. Nevertheless, the device is on the alert and ready to respond rapidly to any interrupt.

The microcontroller enters the Idle mode via the IDLE instruction. In the Idle mode, all activity is halted except for the oscillator, the timer/event counter 1 and the I²C-bus interface (if available).

The microcontroller leaves the Idle mode when an enabled interrupt occurs. The interrupt routine is executed before operation resumes with the instruction following the IDLE opcode.

For timer/event counter interrupts and I²C-bus/derivative interrupts, termination of the Idle mode is straightforward. However, care must be taken when the Idle mode is left by the external interrupt since $\overline{\text{INT}}$/T0 is negative-edge responding. If $\overline{\text{INT}}$/T0 was LOW prior to entering the Idle mode, it must be taken HIGH before the negative edge can be generated. Figure 20 specifies the exact timing for leaving the Idle mode via the external interrupt $\overline{\text{INT}}$/T0.

If no interrupt is enabled, the Idle mode can only be terminated by an active signal on the RESET pin. A normal reset sequence is executed (see Fig.20).

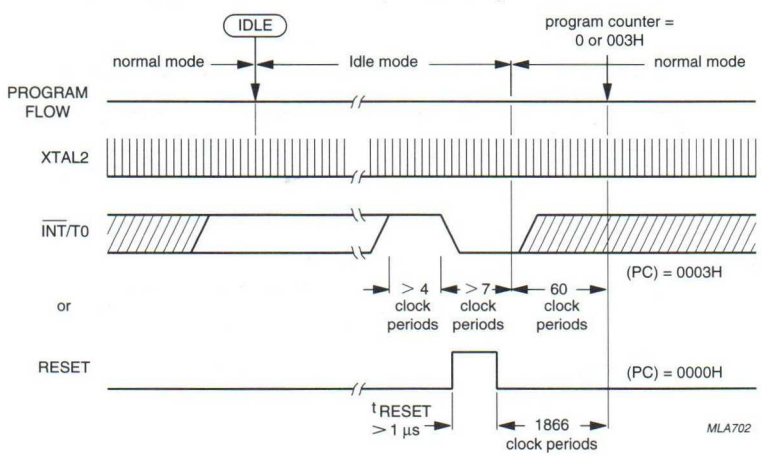


Fig.20 Entering and leaving the Idle mode.

6.13.2 STOP MODE

The Stop mode allows very low-power applications. When all computational tasks are completed, the device can be almost completely shut off by stopping its oscillator. In contrast to the Idle mode, the device is not ready to respond rapidly to any interrupt.

The microcontroller enters the Stop mode via the STOP instruction. The oscillator is switched off. All internal states and I/O levels are maintained.

The microcontroller leaves the Stop mode by a LOW level on $\overline{INT}$/T0 or a reset. In the latter case, a normal reset sequence is executed (see Fig.21).

In contrast to the Idle mode and the external interrupt mechanism, the microcontroller responds to a LOW level on $\overline{INT}$/T0 rather than to a negative edge. If $\overline{INT}$/T0 is LOW when the STOP instruction is executed, the Stop mode will not be entered.

A negative edge on $\overline{INT}$/T0 continues program execution after a 1866 clock cycle delay, which ensures proper oscillator start-up. If the external interrupt is enabled, the device executes the instruction following the STOP opcode before diverting to the interrupt routine. If the external interrupt is disabled, program execution continues with the instructions following the STOP opcode (see Fig.21).

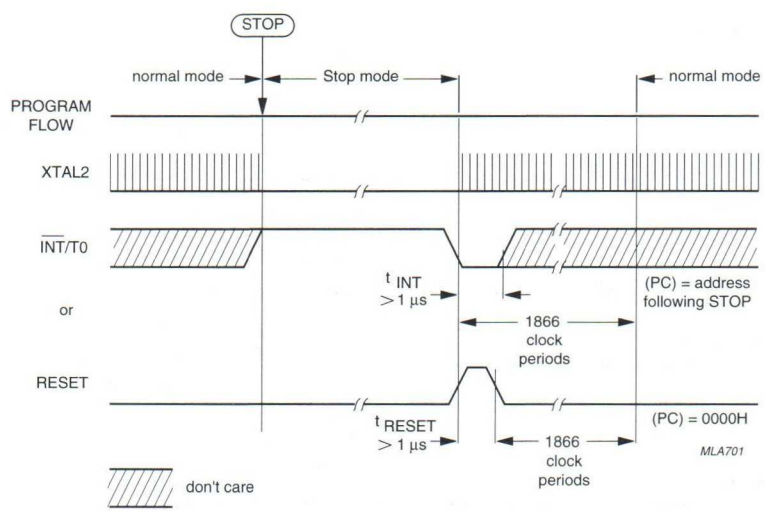


Fig.21 Entering and leaving the Stop mode.

6.14 Derivative logic

Derivative logic is provided with many members of the PCF84CxxxA family. The detailed description of the derivative circuitry is given in the data sheet of the specific device. In this section, the shared principles of derivative logic are briefly reviewed.

Derivative registers are accessed over the internal bus. The derivative registers are write-only, read-only or read/write (see Fig.22). They are addressed through the derivative address register when the derivative input/output instructions (MOV A, Dx; MOV Dx, A; ANL Dx, A and ORL Dx, A) are executed.

Derivative interrupts share the line PIN with the I^2C-bus interrupt (if available). When the derivative interrupt routine is executed, the PIN line must be de-activated by software.

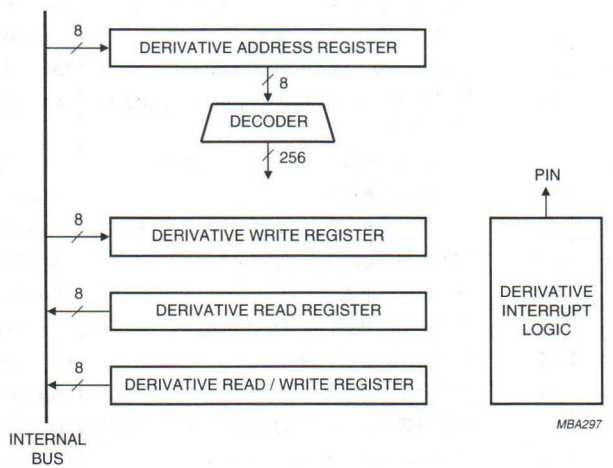


Fig.22 Block diagram of derivative logic.

Table 6 Summary of mask options

FEATURE	OPTION	DESCRIPTION
ROM	any mix of instructions	program; size restricted by ROM size (see Tables 7 and 8)
Ports	option 1	standard output (see Fig.11)
	option 2	open drain output (see Fig.12)
	option 3	push-pull output (see Fig.13)
	set	flip-flop at logic 1 after reset
	reset	flip-flop at logic 0 after reset
Oscillator	g_{mL}	LOW transconductance
	g_{mM}	MEDIUM transconductance
	g_{mH}	HIGH transconductance

7 INSTRUCTION SET

The PCF84CxxxA instruction set consists of over 100 one and two-byte instructions. Program code efficiency is high because all RAM locations and all ROM locations on a 256-byte page require only a single-byte address. Table 8 lists the symbols that are used in Table 7 and the Instruction map is shown in Section 7.1.

Table 7 PCF84CxxxA family instruction set

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
ACCUMULATOR					
ADD A, Rr[1]	6<8 + r>	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0 to 7
ADD A, @Rr[1]	6r	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((Rr))	r = 0, 1
ADD A, #data[1]	03 data	2/2	Add immediate data to A	(A)←(A) + data	
ADDC A, Rr[1]	7<8 + r>	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0 to 7
ADDC A, @Rr[1]	7r	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((Rr)) + (C)	r = 0, 1
ADDC A, #data[1]	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)	
ANL A, Rr	5<8 + r>	1/1	AND Rr with A	(A)←(A) AND (Rr)	r = 0 to 7
ANL A, @Rr	5r	1/1	AND RAM data addressed by Rr, with A	(A)←(A) AND ((Rr))	r = 0, 1
ANL A, #data	53 data	2/2	AND immediate data with A	(A)←(A) AND data	
ORL A, Rr	4<8 + r>	1/1	OR Rr with A	(A)←(A) OR (Rr)	r = 0 to 7
ORL A, @Rr	4r	1/1	OR RAM data, addressed by Rr, with A	(A)←(A) OR ((Rr))	r = 0, 1
ORL A, #data	43 data	2/2	OR immediate data with A	(A)←(A) OR data)	
XRL A, Rr	D<8 +r>	1/1	XOR Rr with A	(A)←(A) XOR (Rr)	r = 0 to 7
XRL A, @Rr	Dr	1/1	XOR RAM data, addressed by Rr, with A	(A)←(A) XOR ((Rr))	r = 0, 1
XRL A, #data	D3 data	2/2	XOR immediate data with A	(A)←(A) XOR data)	
INC A	17	1/1	Increment A by 1	(A)←(A) + 1	
DEC A	07	1/1	Decrement A by 1	(A)←(A) – 1	
CLR A	27	1/1	Clear A to zero	(A)←0	
CPL A	37	1/1	One's complement A	(A)←NOT(A)	
RL A	E7	1/1	Rotate A left	$(A_{n+1})\leftarrow(A_n)$, $(A_0)\leftarrow(A_7)$	n = 0 to 6
RLC A[2]	F7	1/1	Rotate A left through carry	$(A_{n+1})\leftarrow(A_n)$, $(A_0)\leftarrow(C)$, $(C)\leftarrow(A_7)$	n = 0 to 6
RR A	77	1/1	Rotate A right	$(A_n)\leftarrow(A_{n+1})$, $(A_7)\leftarrow(A_0)$	n = 0 to 6
RRC A[2]	67	1/1	Rotate A right through carry	$(A_n)\leftarrow(A_{n+1})$, $(A_7)\leftarrow(C)$, $(C)\leftarrow(A_0)$	n = 0 to 6
DA A[2]	57	1/1	Decimal adjust A	(A)←(A) + 06H if AC = 1 or $(A_{0-3})>9$; (A)←(A) + 60H if $(A_{4-7})>9$	
SWAP A[2]	47	1/1	Swap nibbles of A	$(A_{4-7})\leftrightarrow(A_{0-3})$	

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
DATA MOVES					
MOV A, Rr	F<8 + r>	1/1	Move register contents to A	(A)←(Rr)	r = 0 to 7
MOV A, @Rr	Fr	1/1	Move RAM data addressed by Rr, to A	(A)←((Rr))	r = 0, 1
MOV A, #data	23 data	2/2	Move immediate data to A	(A)←data	
MOV Rr, A	A<8 + r>	1/1	Move Accumulator contents to register	(Rr)←(A)	r = 0 to 7
MOV@Rr, A	Ar	1/1	Move Accumulator contents to RAM location addressed by Rr	((Rr))←(A)	r = 0, 1
MOV Rr, #data	B<8 + r> data	2/2	Move immediate data to Rr	(Rr)←data	r = 0 to 7
MOV @Rr, #data	Br data	2/2	Move immediate data to RAM location addressed by Rr	((R0))←data	r = 0, 1
XCH A, Rr	2<8 + r>	1/1	Exchange A contents with Rr	(A)↔(Rr)	r = 0 to 7
XCH A, @Rr	2r	1/1	Exchange Accumulator contents with RAM data addressed by Rr	(A)↔((Rr))	r = 0, 1
XCHD A, @Rr	3r	1/1	Exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3})\leftrightarrow((Rr_{0-3}))$	r = 0, 1
MOV A, PSW	C7	1/1	Move PSW contents to Accumulator	(A)←(PSW)	
MOV PSW, A[3]	D7	1/1	Move Accumulator bit 3 to PSW_3 (PS)	$(PS)\leftarrow(A_3)$	
MOV P A, @A	A3	1/2	Move indirectly addressed data in current page to A	$(PC_{0-7})\leftarrow(A)$, (A)←((PC))	
CARRY FLAG					
CLR C[2]	97	1/1	Clear carry bit	(C)←0	
CPL C[2]	A7	1/1	Complement carry bit	(C)←NOT(C)	
REGISTER					
INC Rr	1<8 + r>	1/1	Increment register by 1	(Rr)←(Rr) + 1	r = 0 to 7
INC @Rr	1r	1/1	Increment RAM data, addressed by Rr, by 1	((Rr))←((Rr)) + 1	r = 0, 1
DEC Rr	C<8 + r>	1/1	Decrement register by 1	(Rr)←(Rr) – 1	r = 0 to 7
DEC @Rr	Cr	1/1	Decrement RAM data addressed by Rr, by 1	((Rr))←((Rr)) – 1	r = 0, 1

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
BRANCH					
JMP addr	<2n>4 addr	2/2	Unconditional jump within a 2 kbyte bank	$(PC_{8-10})\leftarrow n$ $(PC_{0-7})\leftarrow$addr $(PC_{11-12})\leftarrow$ (MBFF0-1)	n = 0 to 7
JMPP @A	B3	1/2	Indirect jump within a page	$(PC_{0-7})\leftarrow((A))$	
DJZN Rr, addr	E<8 + r> addr	2/2	Decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1; if (Rr) not zero, then $(PC_{0-7})\leftarrow$addr	r = 0 to 7
DJNZ @Rr, addr	Er	2/2	Decrement RAM data, addressed by Rr, by 1 and jump if not zero to addr	((Rr))←((Rr)) – 1; if ((Rr)) not zero, then $(PC_{0-7})\leftarrow$addr	r = 0 to 1
JBb addr	<2b + 1> 2 addr	2/2	Jump to addr if Accumulator bit b = 1	If $(A_b) = 1$, then $(PC_{0-7})\leftarrow$addr	b = 0 to 7
JC addr	F6 addr	2/2	Jump to addr if C = 1	If (C) = 1, then $(PC_{0-7})\leftarrow$addr	
JNC addr	E6 addr	2/2	Jump to addr if C = 0	If (C) = 0, then $(PC_{0-7})\leftarrow$addr	
JZ addr	C6 addr	2/2	Jump to addr if A = 0	If (A) = 0, $(PC_{0-7})\leftarrow$addr	
JNZ addr	96 addr	2/2	Jump to addr if A is NOT zero	If (A) ≠ 0, then $(PC_{0-7})\leftarrow$addr	
JT0 addr	36 addr	2/2	Jump to addr if T0 = 1	If T0 = 1, then $(PC_{0-7})\leftarrow$addr	
JNT0 addr	26 addr	2/2	Jump to addr if T0 = 0	If T0 = 0, then $(PC_{0-7})\leftarrow$addr	
JT1 addr	56 addr	2/2	Jump to addr if T1 = 1	If T1 = 1, then $(PC_{0-7})\leftarrow$addr	
JNT1 addr	46 addr	2/2	Jump to addr if T1 = 0	If T0 = 0, then $(PC_{0-7})\leftarrow$addr	
JTF addr[4]	16 addr	2/2	Jump to addr if Timer Flag = 1	If TF = 1, then $(PC_{0-7})\leftarrow$addr	
JNTF addr[4]	06 addr	2/2	Jump to addr if Timer Flag = 0	If T0 = 0, then $(PC_{0-7})\leftarrow$addr	

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
TIMER/EVENT COUNTER					
MOV A,T	42	1/1	Move timer/event counter contents to A	(A)←(T)	
MOV T, A	62	1/1	Move A contents to timer/event counter	(T)←(A)	
STRT CNT	45	1/1	Start event counter		
STRT T	55	1/1	Start timer		
STOP TCNT	65	1/1	Stop timer/event counter		
EN TCNTI	25	1/1	Enable timer/event counter interrupt		
DIS TCNTI	35	1/1	Disable timer/event counter interrupt		
CONTROL					
EN I	05	1/1	Enable external (chip enable) interrupt		
DIS I	15	1/1	Disable external (chip enable) interrupt		
SEL RB0[5]	C5	1/1	Select register bank 0	(RBS)←0	
SEL RB1[5]	D5	1/1	Select register bank 1	(RBS)←1	
SEL MB0[10]	E5	1/1	Select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
SEL MB1[10]	F5	1/1	Select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
SEL MB2[10]	A5	1/1	Select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
SEL MB3[10]	B5	1/1	Select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
STOP	22	1/1	Enter Stop mode		
IDLE	01	1/1	Enter Idle mode		
SUBROUTINE					
CALL addr[6]	<2n + 1> 4addr	2/2	Jump to subroutine	((SP))←(PC) ($PSW_{4,6,7}$), (SP)←(SP) + 1, (PC_{8-10})←n, (PC_{0-7})←addr, (PC_{11-12}) ←(MBFF0-1)	n = 0 to 7
RET[6]	83	1/2	Return from subroutine	(SP)←(SP) – 1, (PC)←((SP))	
RETR[6]	93	1/2	Return from interrupt and restore bits 4, 6 and 7 of PSW	(SP)←(SP) – 1, ($PSW_{4,6,7}$) + (PC)←((SP))	

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
PARALLEL INPUT/OUTPUT					
IN A, P0	08	1/2	Input Port 0 data to Accumulator	(A)←(P0)	
IN A, P1	09	1/2	Input Port 1 data to Accumulator	(A)←(P1)	
IN A, P2[7]	0A	1/2	Input Port 2 data to Accumulator	(A)←(P2)	
OUTL P0, A	38	1/2	Output A data to Port 0	(P0)←(A)	
OUTL P1, A	39	1/2	Output A data to Port 1	(P1)←(A)	
OUTL P2, A	3A	1/2	Output A data to Port 2	(P2)←(A)	
ANL P0, #data	98 data	2/2	AND Port 0 data with immediate data	(P0)←(P0) AND data	
ANL P1, #data	99 data	2/2	AND Port 1 data with immediate data	(P1)←(P1) AND data	
ANL P2, #data	9A data	2/2	AND Port 2 data with immediate data	(P2)←(P2) AND data	
ORL P0, #data	88 data	2/2	OR Port 0 data with immediate data	(P0)←(P0) OR data	
ORL P1, #data	89 data	2/2	OR Port 1 data with immediate data	(P1)←(P1) OR data	
ORL P2, #data	8A data	2/2	OR Port 2 data with immediate data	(P2)←(P2) OR data	
DERIVATIVE INPUT/OUTPUT					
MOV A, Dx[8]	8C direct	2/2	Move derivative register contents to A	(A)←(Dx)	x = 0 to 255
MOV Dx, A[8]	8D direct	2/2	Move A contents to derivative register	(Dx)←(A)	x = 0 to 255
ANL Dx, A[8]	8E direct	2/2	AND derivative register with A	(Dx)←(Dx) AND (A)	x = 0 to 255
ORL Dx, A[8]	8F direct	2/2	OR derivative register with A	(Dx)←(Dx) OR (A)	x = 0 to 255
SERIAL INPUT/OUTPUT (I^2C-bus operations)					
MOV A, S0	0C	1/2	Move I^2C-bus register 0 contents to A	(A)←(S0)	
MOV A, S1[9]	0D	1/2	Move I^2C-bus register 1 contents to A	(A)←(S1)	
MOV S0, A	3C	1/2	Move A contents to I^2C-bus register 0	(S0)←(A)	
MOV S1, A[9]	3D	1/2	Move A contents to I^2C-bus register 1	(S1)←(A)	
MOV S2, A	3E	1/2	Move A contents to I^2C-bus register 2	(S2)←(A)	
MOV S0, #data	9C data	2/2	Move immediate data to I^2C-bus register 0	(S0)←data	
MOV S1, #data[9]	9D data	2/2	Move immediate data to I^2C-bus register 1	(S1)←data	
MOV S2, #data	9E data	2/2	Move immediate data to I^2C-bus register 2	(S2)←data	
EN SI	85	1/1	Enable serial I/O interrupt		
DIS SI	95	1/1	Disable serial I/O interrupt		
NOP	00	1/1	No operation	(PC_{0-10})←$(PC_{0-10}) + 1$	

Notes to Table 7

1. PSW CY, AC affected.
2. PSW CY affected.
3. PSW PS affected.
4. Execution of a JTF or JNTF instruction resets the Timer Flag (TF).
5. PSW RBS affected.
6. PSW SP_0, SP_1 and SP_2, affected.
7. (A) = 0000, P2.3, P2.2, P2.1 and P2.0.
8. For more information on the derivative I/O instructions of a particular microcontroller, consult the specific microcontroller data sheet.
9. (S1) has a different meaning for read and write operations. See Section 6.9.4.
10. SEL MB instructions may not be used within interrupt routines.

Table 8 Definitions of symbols used in Table 7

SYMBOL	DESCRIPTION
A	Accumulator
AC	auxiliary (half) carry
addr	program memory address
Bb	bit designation (b = 0 to 7)
CE/T0	CE/T0 input
CY	carry bit
Dx	mnemonic derivative register
data	8-bit number or expression
MB0	program memory bank 0
MB1	program memory bank 1
MB2	program memory bank 2
MB3	program memory bank 3
MBFF0	memory bank flip-flop 0
MBFF1	memory bank flip-flop 1
PC	Program Counter
PS	timer prescaler select
PSW	Program Status Word
RB0	register bank 0
RB1	register bank 1
RBS	register bank select
Rr	register designation (r = 0 to 7)
SPn	Stack Pointer (n = 0, 1 or 2)
T	Timer 1
T1	T1 input
TF	Timer Flag
x	derivative register address (x = 0 to 255)
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with
#	immediate data prefix
@	indirect address prefix
*	hexadecimal; 8...F selects R0...R7
&	hexadecimal; 0, 2, 4, 6, 8, A, C, E selects page 0...7 in JMP, i.e. $(PC_{8\text{-}10}) \leftarrow \&_{1\text{-}3}$
%	hexadecimal; 1, 3, 5, 7, 9, B, D, F selects page 0...7 in CALL, i.e. $(PC_{8\text{-}10}) \leftarrow \&_{1\text{-}3}$ selects bit b = 0...7 in JBb, i.e. $b = \&_{1\text{-}3}$

7.1 Instruction map

first hexadecimal character of opcode — second hexadecimal character of opcode

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A, #data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0	IN A,Pp 1	IN A,Pp 2		MOV A,Sn 0	MOV A,Sn 1		
1	INC @ Rr 0	INC @ Rr 1	JB0 addr	ADDC A,#data	CALL page 0	DIS I	JTF addr	INC A	INC Rr 0	INC Rr 1	INC Rr 2	INC Rr 3	INC Rr 4	INC Rr 5	INC Rr 6	INC Rr 7
2	XCH A, @Rr 0	XCH A, @Rr 1	STOP	MOV A, #data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	XCH A,Rr 0	XCH A,Rr 1	XCH A,Rr 2	XCH A,Rr 3	XCH A,Rr 4	XCH A,Rr 5	XCH A,Rr 6	XCH A,Rr 7
3	XCHD A, @Rr 0	XCHD A, @Rr 1	JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	OUTL Pp,A 0	OUTL Pp,A 1	OUTL Pp,A 2		MOV Sn,A 0	MOV Sn,A 1	MOV Sn,A 2	
4	ORL A, @Rr 0	ORL A, @Rr 1	MOV A, T	ORL A, #data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr 0	ORL A,Rr 1	ORL A,Rr 2	ORL A,Rr 3	ORL A,Rr 4	ORL A,Rr 5	ORL A,Rr 6	ORL A,Rr 7
5	ANL A, @Rr 0	ANL A, @Rr 1	JB2 addr	ANL A, #data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr 0	ANL A,Rr 1	ANL A,Rr 2	ANL A,Rr 3	ANL A,Rr 4	ANL A,Rr 5	ANL A,Rr 6	ANL A,Rr 7
6	ADD A, @Rr 0	ADD A, @Rr 1	MOV T, A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr 0	ADD A,Rr 1	ADD A,Rr 2	ADD A,Rr 3	ADD A,Rr 4	ADD A,Rr 5	ADD A,Rr 6	ADD A,Rr 7
7	ADDC A, @Rr 0	ADDC A, @Rr 1	JB3 addr		CALL page 3			RR A	ADDC A,Rr 0	ADDC A,Rr 1	ADDC A,Rr 2	ADDC A,Rr 3	ADDC A,Rr 4	ADDC A,Rr 5	ADDC A,Rr 6	ADDC A,Rr 7
8				RET	JMP page 4	EN SI			ORL Pp,#data 0	ORL Pp,#data 1	ORL Pp,#data 2		MOV A,Dx	MOV Dx,A	ANL Dx,A	ORL Dx,A
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,#data 0	ANL Pp,#data 1	ANL Pp,#data 2		MOV Sn,#data 0	MOV Sn,#data 1	MOV Sn,#data 2	
A	MOV @ Rr,A 0	MOV @ Rr,A 1		MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A 0	MOV Rr,A 1	MOV Rr,A 2	MOV Rr,A 3	MOV Rr,A 4	MOV Rr,A 5	MOV Rr,A 6	MOV Rr,A 7
B	MOV @Rr, #data 0	MOV @Rr, #data 1	JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr,#data 0	MOV Rr,#data 1	MOV Rr,#data 2	MOV Rr,#data 3	MOV Rr,#data 4	MOV Rr,#data 5	MOV Rr,#data 6	MOV Rr,#data 7
C	DEC @Rr 0	DEC @Rr 1			JMP page 6	SEL RB0	JZ addr	MOV A,PSW	DEC Rr 0	DEC Rr 1	DEC Rr 2	DEC Rr 3	DEC Rr 4	DEC Rr 5	DEC Rr 6	DEC Rr 7
D	XRL A, @Rr 0	XRL A, @Rr 1	JB6 addr	XRL A,#data	CALL page 6	SEL RB1		MOV PSW,A	XRL A,Rr 0	XRL A,Rr 1	XRL A,Rr 2	XRL A,Rr 3	XRL A,Rr 4	XRL A,Rr 5	XRL A,Rr 6	XRL A,Rr 7
E	DJNZ @ Rr,addr 0	DJNZ @ Rr,addr 1			JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr,addr 0	DJNZ Rr,addr 1	DJNZ Rr,addr 2	DJNZ Rr,addr 3	DJNZ Rr,addr 4	DJNZ Rr,addr 5	DJNZ Rr,addr 6	DJNZ Rr,addr 7
F	MOV A, @Rr 0	MOV A, @Rr 1	JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr 0	MOV A,Rr 1	MOV A,Rr 2	MOV A,Rr 3	MOV A,Rr 4	MOV A,Rr 5	MOV A,Rr 6	MOV A,Rr 7

MBA281

LCD DRIVERS AND MICROCONTROLLER PERIPHERALS

128 × 8-bit EEPROM with I²C-bus interface

PCA8581; PCA8581C

1 FEATURES

- Operating supply voltage:
  - 4.5 to 5.5 V (PCA8581)
  - 2.5 to 6.0 V (PCA8581C)
- Integrated voltage multiplier and timer for writing (no external components required)
- Automatic erase before write
- Low standby current; maximum 10 µA
- 8-byte page write mode
- Serial input/output bus (I²C-bus)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Designed for minimum 10000 write cycles per byte
- 10 years minimum non-volatile data retention
- Infinite number of read cycles
- Pin and address compatibility to PCF8570C and PCF8582
- Operating ambient temperature: –25 to +85 °C.

2 GENERAL DESCRIPTION

The PCA8581 and PCA8581C are low power CMOS EEPROMs with standard and wide operating voltages:

4.5 to 5.5 V (PCA8581)

2.5 to 6.0 V (PCA8581C).

In the following text, the generic term 'PCA8581' is used to refer to both types in all packages except when otherwise specified.

The PCA8581 is organized as 128 words of 8-bytes.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. All bytes can be read in a single operation. Up to 8 bytes can be written in one operation, reducing the total write time per byte. Three address pins, A0, A1 and A2 are used to define the hardware address, allowing the use of up to 8 devices connected to the bus without additional hardware.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage				
	PCA8581		4.5	5.5	V
	PCA8581C		2.5	6.0	V
I_{DD}	supply current (standby)	f_{SCL} = 0 Hz	–	10	µA
T_{amb}	operating ambient temperature		–25	+85	°C
T_{stg}	storage temperature	without EEPROM retention	–65	+150	°C
		with EEPROM retention	–65	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA8581P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCA8581CP	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCA8581T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA8581CT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

BLOCK DIAGRAM

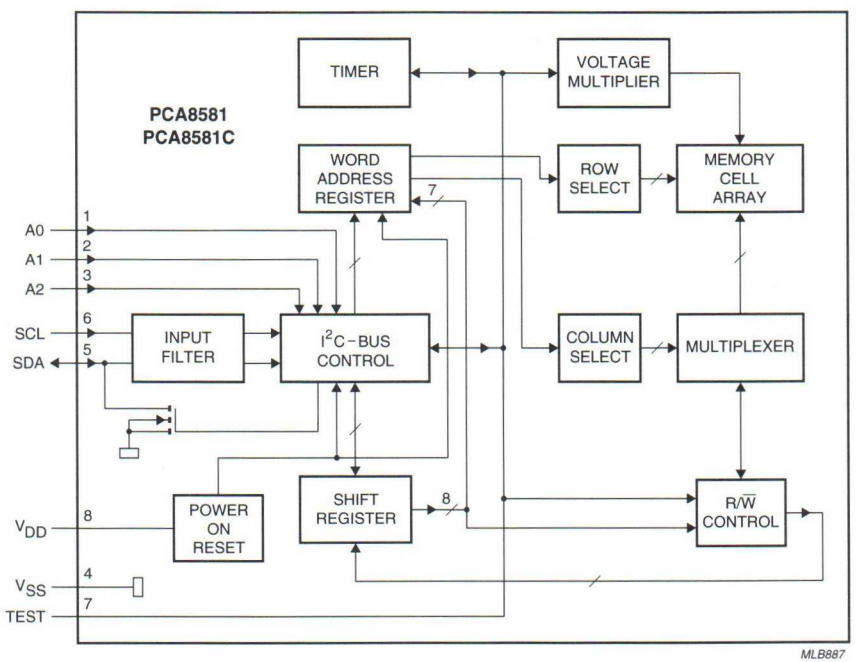


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	hardware address input 0
A1	2	hardware address input 1
A2	3	hardware address input 2
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
TEST	7	test output can be connected to V_{SS}, V_{DD} or left open-circuit
V_{DD}	8	positive supply

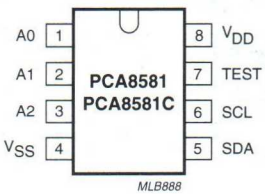


Fig.2 Pin configuration.

LCD driver for low multiplex rates OM4068

FEATURES

- Single-chip LCD controller/driver
- Static/duplex/triplex drive modes with up to 32/64/96 LCD segments drive capability per device
- Selectable backplane drive configuration: static or 2 or 3 backplane multiplexing
- Selectable display bias configuration drive: static, $\frac{1}{2}$ or $\frac{1}{3}$
- 32 segment drivers
- Serial data input (word length 32 to 96 bits)
- On-chip generation of intermediate LCD bias voltages
- 2 MHz fast serial bus interface
- CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications
- Logic supply voltage range ($V_{DD} - V_{SS}$) of 2.5 to 5.5 V
- Display supply voltage range ($V_{LCD} - V_{SS}$) of 3.5 to 6.5 V
- Low power consumption, suitable for battery operated systems
- No external components needed by the oscillator
- Manufactured in silicon gate CMOS process.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Alarm systems
- Automotive equipment.

GENERAL DESCRIPTION

The OM4068 is a low-power CMOS LCD driver, designed to drive Liquid Crystal Displays (LCDs) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to three backplanes and up to 32 segment lines and can be easily cascaded for larger LCD applications. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower power consumption. A 3-line bus structure enables serial data transfer with most microprocessors/microcontrollers. All inputs are CMOS compatible.

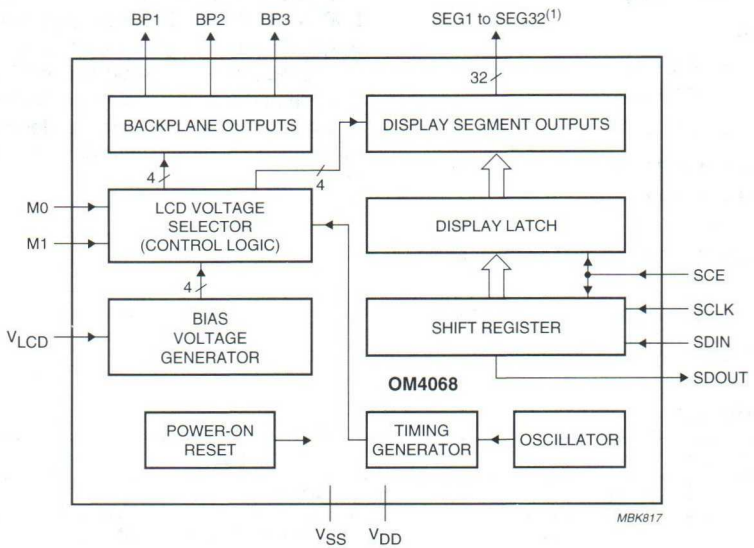
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OM4068H[1]	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2
OM4068P	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
OM4068U/5[2]	die	unsawn wafer	–
OM4068U	tray	chip in tray	–

Notes

1. Gull Wing package.
2. For details see Chapter "Bonding pad locations".

BLOCK DIAGRAM



(1) SEG1, SEG6, SEG15 and SEG25 are not available in DIP40 package.

Fig.1 Block diagram.

PINNING

See notes 1 to 8.

SYMBOL	PIN		DESCRIPTION
	QFP44	DIP40	
V_{LCD}	4	19	LCD supply voltage
V_{DD}	5	20	positive supply voltage
V_{SS}	6	21	ground
M0	7	22	drive mode select input 0
M1	8	23	drive mode select input 1
SDIN	9	24	serial bus data input
SCLK	10	25	serial bus clock input
SCE	11	26	serial bus clock enable
SDOUT	12	27	serial bus data output
BP1	13	28	LCD backplane driver output 1
BP2	14	29	LCD backplane driver output 2
BP3	15	30	LCD backplane driver output 3
SEG1	16	–	LCD segment driver output 1
SEG2	17	31	LCD segment driver output 2
SEG3	18	32	LCD segment driver output 3
SEG4	19	33	LCD segment driver output 4
SEG5	20	34	LCD segment driver output 5
SEG6	21	–	LCD segment driver output 6
SEG7	22	35	LCD segment driver output 7
SEG8	23	36	LCD segment driver output 8
SEG9	24	37	LCD segment driver output 9
SEG10	25	38	LCD segment driver output 10
SEG11	26	39	LCD segment driver output 11
SEG12	27	40	LCD segment driver output 12
SEG13	28	1	LCD segment driver output 13
SEG14	29	2	LCD segment driver output 14
SEG15	30	–	LCD segment driver output 15
SEG16	31	3	LCD segment driver output 16
SEG17	32	4	LCD segment driver output 17
SEG18	33	5	LCD segment driver output 18
SEG19	34	6	LCD segment driver output 19
SEG20	35	7	LCD segment driver output 20
SEG21	36	8	LCD segment driver output 21
SEG22	37	9	LCD segment driver output 22
SEG23	38	10	LCD segment driver output 23
SEG24	39	11	LCD segment driver output 24
SEG25	40	–	LCD segment driver output 25
SEG26	41	12	LCD segment driver output 26

SYMBOL	PIN		DESCRIPTION
	QFP44	DIP40	
SEG27	42	13	LCD segment driver output 27
SEG28	43	14	LCD segment driver output 28
SEG29	44	15	LCD segment driver output 29
SEG30	1	16	LCD segment driver output 30
SEG31	2	17	LCD segment driver output 31
SEG32	3	18	LCD segment driver output 32

Notes

1. SEG1 to SEG32 (LCD segment driver outputs) output the multi-level signals for the LCD segments.
2. BP0, BP1 and BP2 (LCD backplane driver outputs) output the multi-level signals for the LCD backplanes.
3. V_{LCD} (LCD power supply): power supply for the LCD.
4. SDIN (serial data line): input for the bus data line.
5. SCL (serial clock line): input for the bus clock line.
6. SDOUT (serial data output): output of the shift register to allow serial cascading of the OM4068 with other devices.
7. SCE (serial clock enable): input for enable/disable acquisition on the data input line. If disabled, data on the serial bus are not accepted by the device.
8. M0 and M1 (display mode select inputs): inputs to select the LCD drive configurations; static, duplex or triplex.

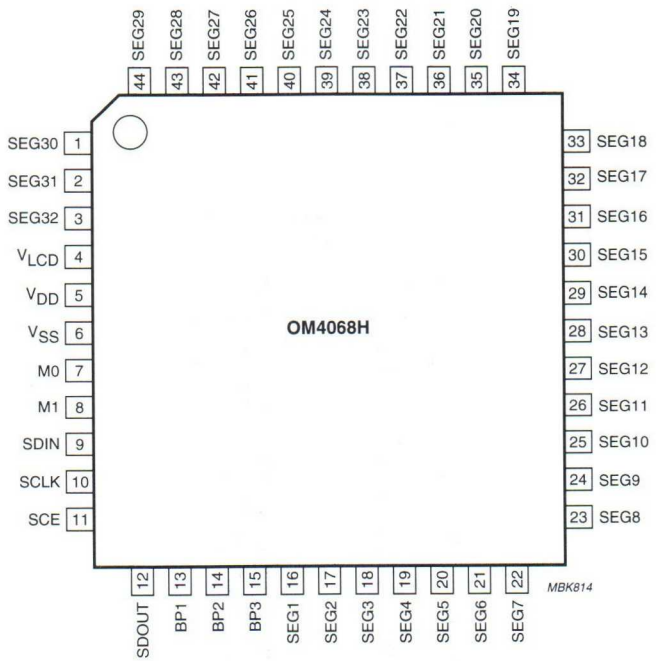


Fig.2 Pin configuration (QFP44).

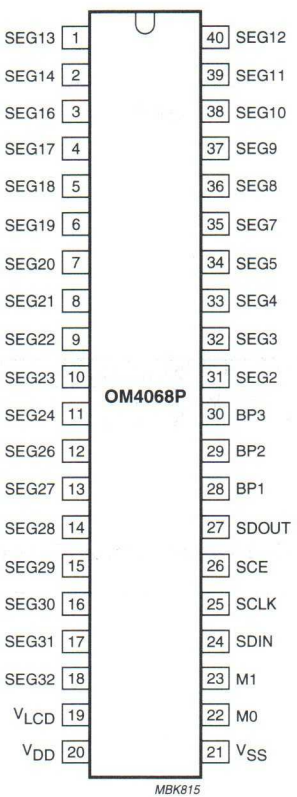


Fig.3 Pin configuration (DIP40).

FUNCTIONAL DESCRIPTION

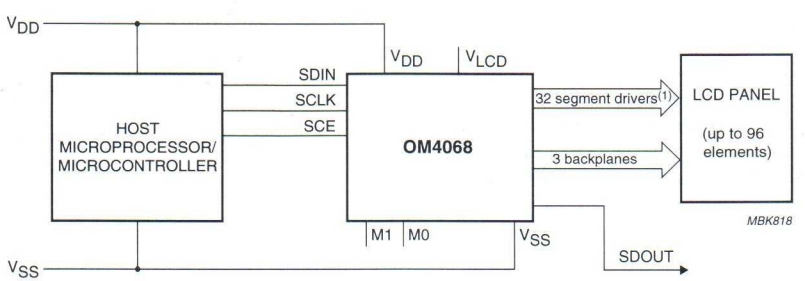
The OM4068 is a low-power LCD driver designed to interface with any microprocessor/microcontroller and a wide variety of LCDs. It can drive any static or multiplexed LCD containing up to three backplanes and up to 96 segments.

The display configurations possible with the OM4068 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

A typical system (MUX 1 : 3) is shown in Fig.4.

Table 1 Selection of display configurations

NUMBER OF		7-SEGMENTS NUMERIC		DOT MATRIX
BACKPLANES	DISPLAY SEGMENTS	DIGITS	INDICATOR SYMBOLS	
3	96	12	12	96 dots (3 × 32)
2	64	8	8	64 dots (2 × 32)
1	32	4	4	32 dots (1 × 32)



(1) 28 segment drivers for DIP40 package.

Fig.4 Typical system configuration.

The host microprocessor/microcontroller maintains the 3-line bus communication channel with OM4068. The internal oscillator requires no external components. The appropriate intermediate biasing voltage for the multiplexed LCD waveforms are generated on-chip.

The only other connections required to complete the system are to the power supplies (V_{SS}, V_{DD} and V_{LCD}) and suitable capacitors to decouple the V_{LCD} and V_{DD} pins to V_{SS}.

Power-on reset

The on-chip power-on reset block initializes the chip after power-on or power failures. The OM4068 resets to a starting condition as follows:

- All backplane and segment outputs are set to V_{SS} (display off)
- All shift registers and latches are set in 3-state
- SDOUT (allowing serial cascading) is set to logic 0 (with SCE LOW)
- Power-down mode.

Data transfers on the serial bus should be avoided for 0.5 ms following power-on to allow completion of the reset action.

Power-down

After power-on the chip is in power-down mode as long as the serial clock is not active. During power-down all static currents are switched off (no internal oscillator, no timing and no bias level generation) and all LCD-outputs are 3-stated. The power-on reset functions remain enabled.

The power-down mode is disabled at the first rising edge of the serial clock SCLK.

LCD bias voltage generator

The intermediate bias voltages for the LCD display are generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system power consumption. The full-scale LCD voltage V_{OP} equals $V_{LCD} - V_{SS}$. The optimum value of V_{OP} depends on the LCD threshold voltage (V_{th}) and the number of bias levels.

Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors ($\frac{1}{3}$bias) connected between V_{LCD} and V_{SS}. The centre resistor can be switched out of the circuit to provide a $\frac{1}{2}$bias voltage level for the 1 : 2 multiplex configuration.

The bias levels depend on the multiplex rate and are selected automatically when the display configuration is selected using M1 and M0.

LCD voltage selector

The LCD voltage selector (control logic) coordinates the multiplexing of the LCD in accordance with the selected drive or display configuration. The operation of the voltage selector is controlled by the input pins M0 and M1 (see Table 2).

Table 2 Drive mode selection

M1	M0	DRIVE MODE
0	0	test mode (not user accessible)
0	1	static drive (1 : 1)
1	0	duplex drive (1 : 2)
1	1	triplex drive (1 : 3)

For multiplex rates of 1 : 2 three bias levels are used including V_{LCD} and V_{SS}. Four bias level are used for the 1 : 3 multiplex rate. The various biasing configurations together with the biasing characteristics as functions of $V_{OP} = V_{LCD} - V_{SS}$ and the resulting discrimination ratios (D), are given in Table 3.

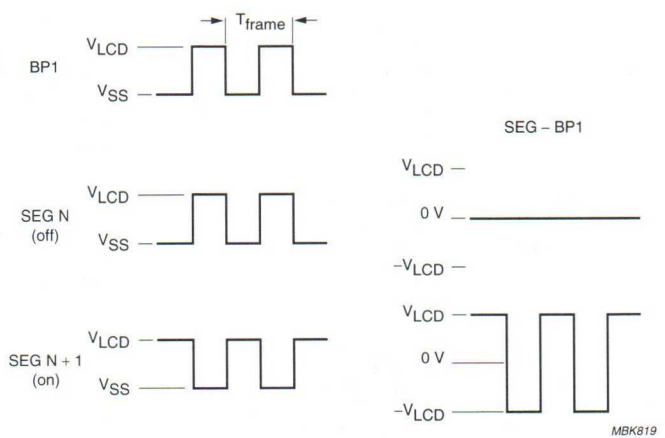
A practical value for V_{OP} is determinated by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In static mode a suitable choice is $V_{OP} > 3V_{th}$.

Table 3 LCD drive modes: summary of characteristics

LCD DRIVE MODE	NUMBER OF		LCD BIAS CONFIGURATION	$\frac{V_{off(rms)}}{V_{OP}}$	$\frac{V_{on(rms)}}{V_{OP}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
	BACKPLANES	LEVELS				
Static	1	2	static	0	1	–
1 : 2	2	3	½	0.354	0.791	2.2236
1 : 3	3	4	⅓	0.333	0.638	1.915

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.5.

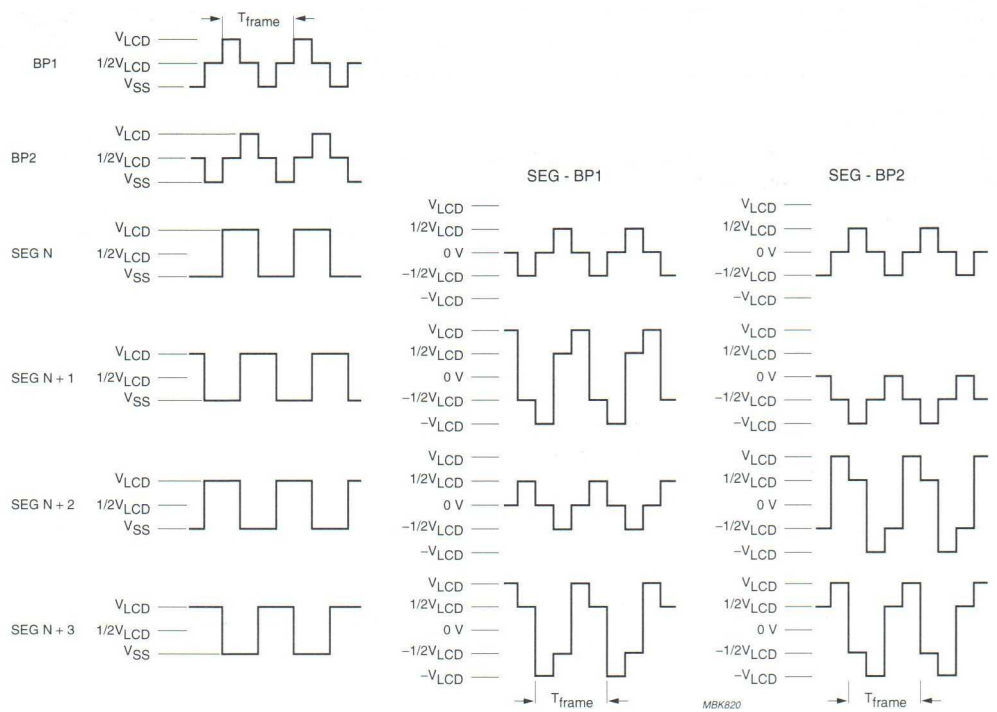


BACKPLANE DRIVER OUTPUT	SEGMENTS	
	SEG N	SEG N + 1
BP1	off	on

Fig.5 Static drive mode waveforms ($V_{OP} = V_{LCD} - V_{SS}$).

1 : 2 MULTIPLEX DRIVE MODE

When two backplanes are provided in the LCD, the 1 : 2 multiplex mode applies, as shown in Fig.6.

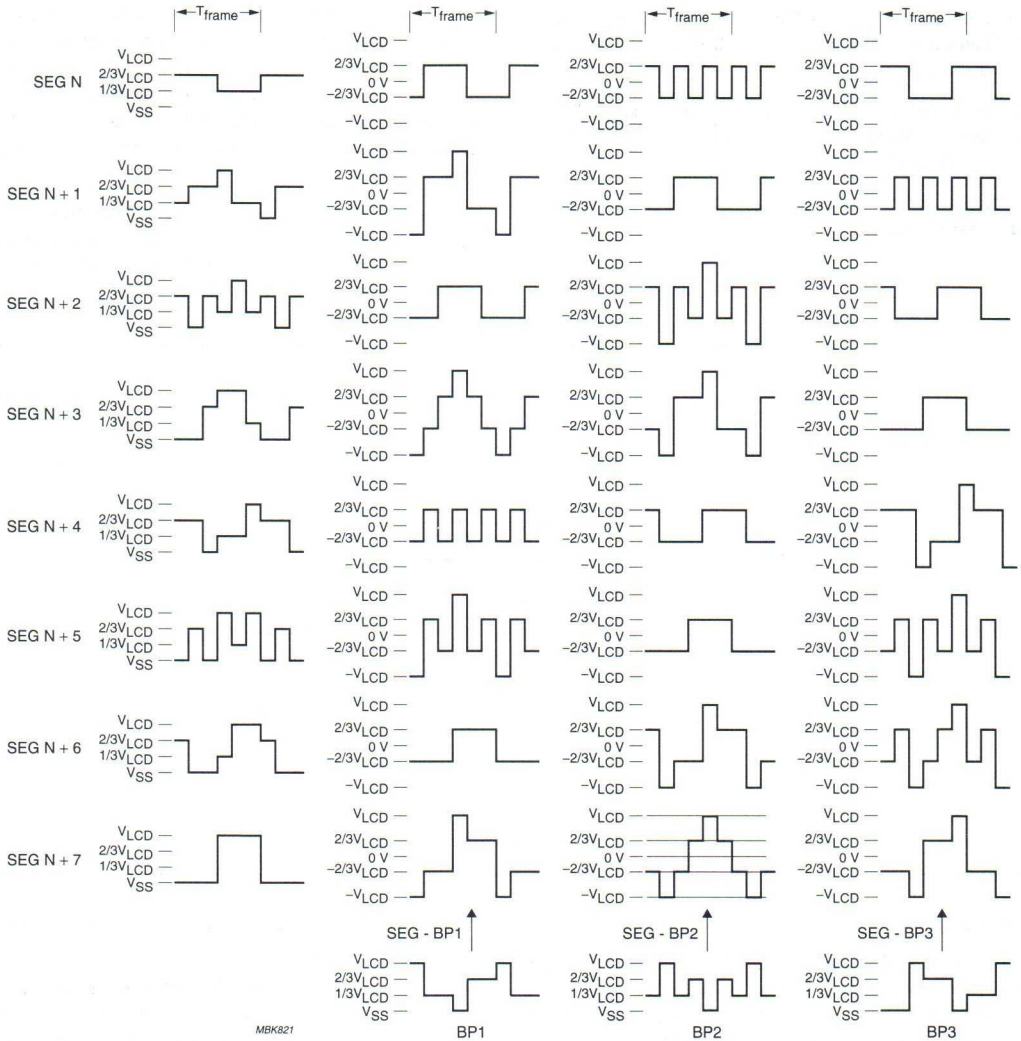


BACKPLANE DRIVER OUTPUTS	SEGMENTS			
	SEG N	SEG N + 1	SEG N + 2	SEG N + 3
BP1	off	on	off	on
BP2	off	off	on	on

Fig.6 Waveforms for 1 : 2 multiplex drive mode ($V_{OP} = V_{LCD} - V_{SS}$).

1 : 3 MULTIPLEX DRIVE MODE

When three backplanes are provided in the LCD, the 1 : 3 multiplex mode applies, as shown in Fig.7.



BACKPLANE DRIVER OUTPUTS	SEGMENTS							
	N	N + 1	N + 2	N + 3	N + 4	N + 5	N + 6	N + 7
BP1	off	on	off	on	off	on	off	on
BP2	off	off	on	on	off	off	on	on
BP3	off	off	off	off	on	on	on	on

Fig.7 Waveforms for 1 : 3 multiplex drive motive ($V_{OP} = V_{LCD} - V_{SS}$).

Oscillator

The internal logic and the multi-level LCD drive signals of the OM4068 are generated by the built-in RC oscillator. No external components are required.

In order to minimize radio frequency interference, the oscillator operates with symmetrical and slew-rate limited capacitor charge/discharge.

The oscillator runs continuously once the power down state after power-on has been left.

Interface to microprocessor unit: serial interface

A three-line bus structure enables serial unidirectional data transfer with microprocessors/microcontrollers. The three lines are a serial data input line (SDIN), a serial clock line (SCLK) and a data line enable (SCE). All inputs are CMOS compatible. These lines must always be in a defined state V_{SS} or V_{DD}. Floating inputs could damage the chip.

On the bus, one data bit is transferred during each clock pulse. The data on the SDIN line remains stable during the whole clock period. Data changes arrive with the falling edge of the serial clock SCLK (see Fig.8).

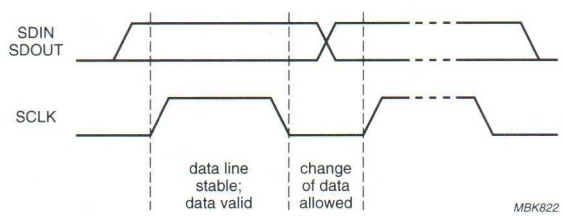


Fig.8 Bit transfer on bus.

Shift register

Data present on the SDIN pin is shifted into a shift register with the rising edge of the serial clock SCLK in a synchronous manner. The shift register serves to transfer display information from the serial bus to the (display) latch while previous data is displayed.

The shift register is organized as three 32-bit shift registers. Depending on the display driving mode selected (see Table 3), one, two or three registers are used and cascaded resulting in a shift register length of 32, 64 or 96 bits. Figure 9 shows the shift register organization with the display data bits after a shift operation is completed. The shift sequence begins with data bit D32 and finishes with data bit D1. The correspondence between the data bit numbers and the LCD display segments is shown in Table 4.

Data from the last stage of the register is supplied to the SDOUT pin to allow serial cascading of the OM4068 with other peripheral devices. Depending on the display driving mode selected, SDOUT corresponds to bit 32, 64 or 96 of the register (see Fig.10). Data on the SDOUT pin is shifted out with the falling edge of the SCLK clock. SDOUT is therefore delayed by ½SCLK cycle before it is applied to the SDIN pin of the next IC in the serial chain (see Fig.8).

The clock enable SCE signal must be HIGH in order to enable the shift operation. SDOUT output is latched with the last data after SCE returned to HIGH (shift operation terminated).

SDOUT is in 3-state mode when SCE is LOW.

Display latch

The 96-bit display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch and the LCD segment outputs. An LCD segment is activated when the corresponding data bit in the display latch is HIGH.

Display latches are in HOLD mode (SCE HIGH) during the shift operation to maintain the display data constant.

Data are latched into the display latch with the internal frame clock. Thus there is a delay of up to one half frame before new data are latched after signal SCE returns to zero.

Timing

The timing of the OM4068 organizes the internal data flow of the device. This includes the transfer of display data from the shift register to the display segments outputs. The timing also generates the LCD frame frequency which is derived from the clock frequency generated in the internal clock generator:

$$f_{fr(LCD)} = \frac{f_{osc}}{2400}$$

Shift register configuration

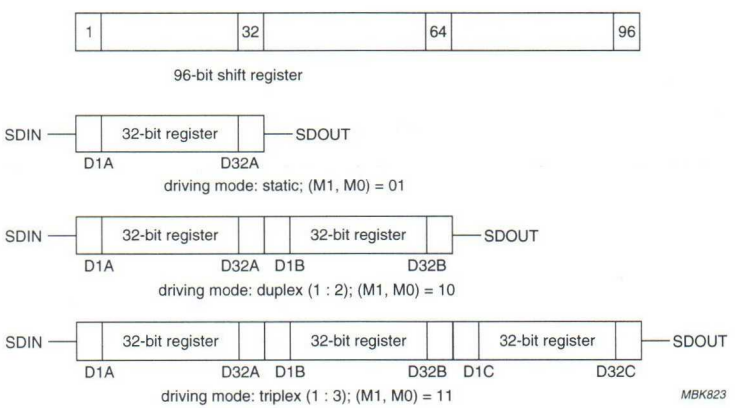


Fig.9 Display data bit position in shift register.

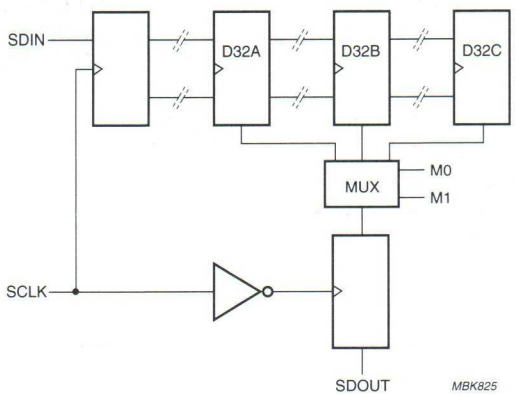


Fig.10 Shift register structure.

Table 4 Relationships between data bit numbers and the LCD segment outputs

SEGMENT NUMBER	DRIVING MODE					
	STATIC	DUPLEX		TRIPLEX		
SEG1	D1A	D1A	D1B	D1A	D1B	D1C
SEG2	D2A	D2A	D2B	D2A	D2B	D2C
SEG3	D3A	D3A	D3B	D3A	D3B	D3C
SEG4	D4A	D4A	D4B	D4A	D4B	D4C
SEG5	D5A	D5A	D5B	D5A	D5B	D5C
SEG6	D6A	D6A	D6B	D6A	D6B	D6C
SEG7	D7A	D7A	D7B	D7A	D7B	D7C
SEG8	D8A	D8A	D8B	D8A	D8B	D8C
SEG9	D9A	D9A	D9B	D9A	D9B	D9C
SEG10	D10A	D10A	D10B	D10A	D10B	D10C
SEG11	D11A	D11A	D11B	D11A	D11B	D11C
SEG12	D12A	D12A	D12B	D12A	D12B	D12C
SEG13	D13A	D13A	D13B	D13A	D13B	D13C
SEG14	D14A	D14A	D14B	D14A	D14B	D14C
SEG15	D15A	D15A	D15B	D15A	D15B	D15C
SEG16	D16A	D16A	D16B	D16A	D16B	D16C
SEG17	D17A	D17A	D17B	D17A	D17B	D17C
SEG18	D18A	D18A	D18B	D18A	D18B	D18C
SEG19	D19A	D19A	D19B	D19A	D19B	D19C
SEG20	D20A	D20A	D20B	D20A	D20B	D20C
SEG21	D21A	D21A	D21B	D21A	D21B	D21C
SEG22	D22A	D22A	D22B	D22A	D22B	D22C
SEG23	D23A	D23A	D23B	D23A	D23B	D23C
SEG24	D24A	D24A	D24B	D24A	D24B	D24C
SEG25	D25A	D25A	D25B	D25A	D25B	D25C
SEG26	D26A	D26A	D26B	D26A	D26B	D26C
SEG27	D27A	D27A	D27B	D27A	D27B	D27C
SEG28	D28A	D28A	D28B	D28A	D28B	D28C
SEG29	D29A	D29A	D29B	D29A	D29B	D29C
SEG30	D30A	D30A	D30B	D30A	D30B	D30C
SEG31	D31A	D31A	D31B	D31A	D31B	D31C
SEG32	D32A	D32A	D32B	D32A	D32B	D32C

Segment outputs

The LCD drive section includes 32 segment outputs SEG1 to SEG32 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplex backplane signals and with data in the display latch. When less than 32 segments are required the unused segment outputs should be left open-circuit.

Backplane outputs

The LCD drive section includes three backplane outputs (BP1 to BP3) which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than three backplane outputs are required the unused outputs should be left open-circuit. In 1 : 2 multiplex drive mode, BP3 is set to $\frac{1}{2}V_{LCD}$. In static drive mode BP3 and BP2 are set to V_{SS}.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+6.5	V
V_{LCD}	LCD supply voltage		−0.5	+7.5	V
V_I	input voltage (any input)		−0.5	V_{DD} + 0.5	V
V_O	output voltage (BP1, BP2, BP3, S1 to S32 and V_{LCD})		−0.5	V_{LCD} + 0.5	V
I_I	DC input current		−10	+10	mA
I_O	DC output current		−10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current		−50	+50	mA
$P_{tot(pack)}$	total power dissipation per package		−	500	mW
P/out	power dissipation per output		−	10	mW
T_{amb}	operating ambient temperature		−40	+105	°C
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		−	150	°C
V_{es}	electrostatic handling	note 1	−2000	+2000	V
		note 2	−150	+150	V

Notes

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor (human body model).
2. Equivalent to discharging a 200 pF capacitor via a 0.75 μH series inductor (machine model).

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

DC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 3.5 to 6.5 V; T_{amb} = −40 to +105 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		V_{SS} + 2.5	–	5.5	V
V_{LCD}	LCD supply voltage		V_{SS} + 3.5	–	6.5	V
I_{DD}	supply current	power-down state; note 1	–	4	10	μA
		normal mode; f_{osc} = intern; notes 2 and 3	–	12	25	μA
I_{LCD}	V_{LCD} current	power-down state; note 1	–	–	1.5	μA
		normal mode; f_{osc} = intern; notes 3 and 4	–	–	40	μA
V_{POR}	power-on reset voltage level	note 5	0.8	1.25	1.6	V
Logic						
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{OL}	LOW-level output current (SDOUT)	V_{OL} = 0.5 V; V_{DD} = 5 V	1.0	–	–	mA
I_{OH}	HIGH-level output current (SDOUT)	$V_{OH} = V_{DD} - 0.5$ V; V_{DD} = 5 V	–	–	−1	mA
I_{pu}	pull-up current M1 and M0	$V_I = V_{SS}$	0.04	0.15	1	μA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	μA
Segment and backplane outputs						
$R_{(o)seg}$	segment output resistance SEG1 to SEG32	note 6	–	15	40	kΩ
$R_{(o)back}$	backplane output resistance BP1 to BP3	note 6	–	15	40	kΩ
$V_{seg(bias)(tol)}$	bias tolerance SEG1 to SEG32	note 7	−100	0	+100	mV
$V_{back(bias)(tol)}$	bias tolerance BP1, BP2 and BP3	note 7	−100	0	+100	mV

Notes

1. Power-down state. After power-on the chip is in power-down state as long as the serial clock is not activated. During power-down all static currents are switched off except the power-on reset block.
2. Output SDOUT is open-circuit; inputs at V_{DD} or V_{SS}; bus inactive.
3. Drive mode: static, duplex and triplex.
4. LCD outputs are open-circuit, C_L = 50 pF typical, inputs at V_{DD} or V_{SS}; bus inactive.
5. Resets all logic when $V_{DD} < V_{POR}$.
6. Resistance of output terminal (S1 to S32 and BP1, BP2 and BP3) with a load current of 20 μA; outputs measured one at a time.
7. LCD outputs open-circuits.

AC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 5.0 V; T_{amb} = −40 to +105 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$f_{fr(LCD)}$	LCD frame frequency (internal clock)	50	84	175	Hz
f_{osc}	oscillator frequency (not available at any pin)	116	224	405	kHz
Bus timing characteristics: serial bus interface; note 1					
f_{SCLK}	SCLK clock frequency	0	–	2.1	MHz
t_{SCLKL}	SCLK clock LOW period	190	–	–	ns
t_{SCLKH}	SCLK clock HIGH period	190	–	–	ns
$t_{su(D)}$	data set-up time	100	–	–	ns
$t_{h(D)}$	data hold time	100	–	–	ns
t_r	SCLK, SDIN rise time	–	10	–	ns
t_f	SCLK, SDIN fall time	–	10	–	ns
$t_{su(en)(SDEH-SCLKH)}$	enable set-up time (SDE HIGH to SCLK HIGH)	250	–	–	ns
$t_{su(dis)(SCLKL-SDEL)}$	disable set-up time (SCLK LOW to SDE LOW)	250	–	–	ns
$t_{PHL(SDOUT)}$	SDOUT HIGH-to-LOW propagation delay	100	–	–	ns

Note

1. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

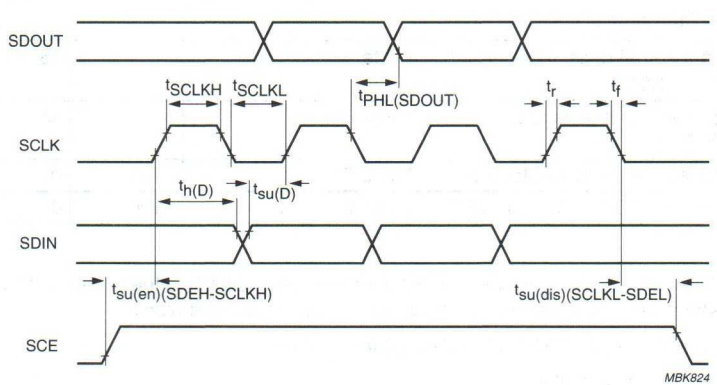
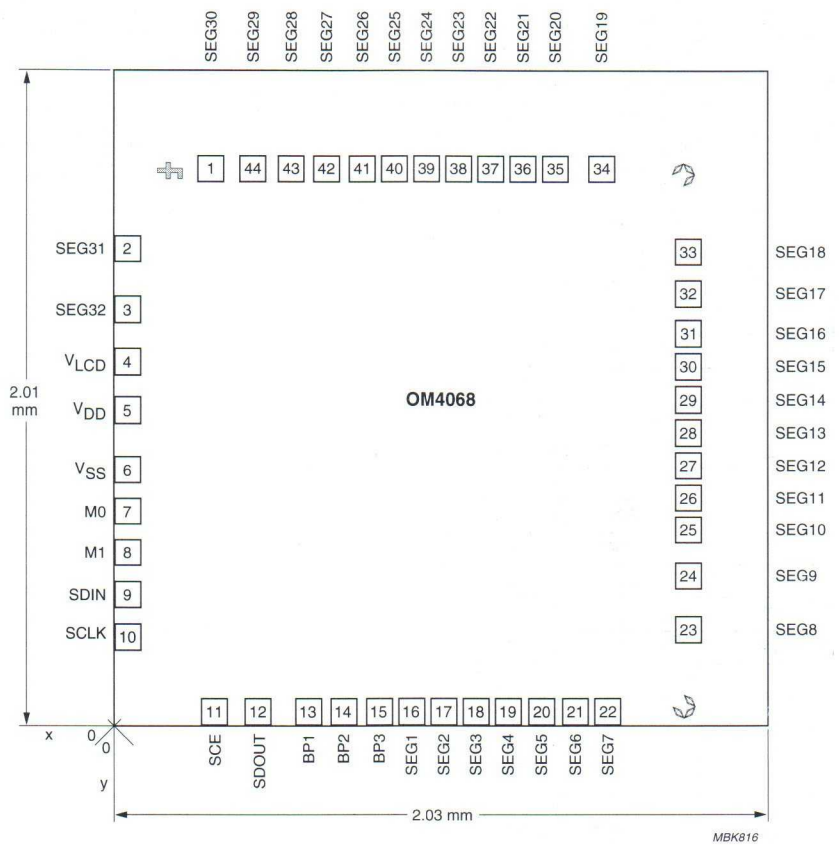


Fig.11 Serial data timing.

BONDING PAD LOCATIONS



Dimensions in mm.
Bonding pad dimensions: 80 × 80 μm.

Fig.12 Bonding pad locations.

Table 5 Bonding pad locations (dimensions in μm). All x/y coordinates are referenced to bottom left corner of chip (see Fig.12).

SYMBOL	PAD	x	y
V_{DD}	5	43.100	970.500
V_{SS}	6	42.900	791.850
M0	7	43.100	661.750
M1	8	43.100	531.750
SDIN	9	43.100	401.750
SCLK	10	43.100	271.750
SCE	11	310.450	43.100
SDOUT	12	447.350	43.100
BP1	13	604.800	43.100
BP2	14	714.850	43.100
BP3	15	824.850	43.100
SEG1	16	924.850	43.100
SEG2	17	1024.850	43.100
SEG3	18	1124.850	43.100
SEG4	19	1224.850	43.100
SEG5	20	1327.250	43.100
SEG6	21	1432.450	43.100
SEG7	22	1532.650	43.100
SEG8	23	1783.600	293.850
SEG9	24	1783.600	458.850
SEG10	25	1783.600	603.850
SEG11	26	1783.600	703.850
SEG12	27	1783.600	803.850
SEG13	28	1783.600	903.850
SEG14	29	1783.600	1003.850
SEG15	30	1783.600	1103.850
SEG16	31	1783.600	1203.850
SEG17	32	1783.600	1323.850
SEG18	33	1783.600	1453.850
SEG19	34	1514.600	1711.100
SEG20	35	1370.550	1711.100
SEG21	36	1270.500	1711.100
SEG22	37	1170.500	1711.100
SEG23	38	1070.500	1711.100
SEG24	39	970.550	1711.100
SEG25	40	870.550	1711.100
SEG26	41	770.550	1711.100
SEG27	42	660.550	1711.100
SEG28	43	550.550	1711.100
SEG29	44	430.550	1711.100
SEG30	1	300.550	1711.100
SEG31	2	43.100	1460.050
SEG32	3	43.100	1274.950
V_{LCD}	4	43.100	1158.700
Alignment marks			
C1	–	1769.6	1696.9
C2	–	1770.1	58.4
F	–	172.0	1705.2

Universal LCD driver for low multiplex rates

OM4085

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2, 3 or 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$ or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2.0 to 6 V power supply range
- Low power consumption
- Power saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576C
- Optimized pinning for single plane wiring in both single and multiple OM4085 applications
- Space-saving 40 lead plastic very small outline package (VSO40; SOT158-1)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The OM4085 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The OM4085 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OM4085T	VSO40	plastic very small outline package; 40 leads	SOT158-1

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM

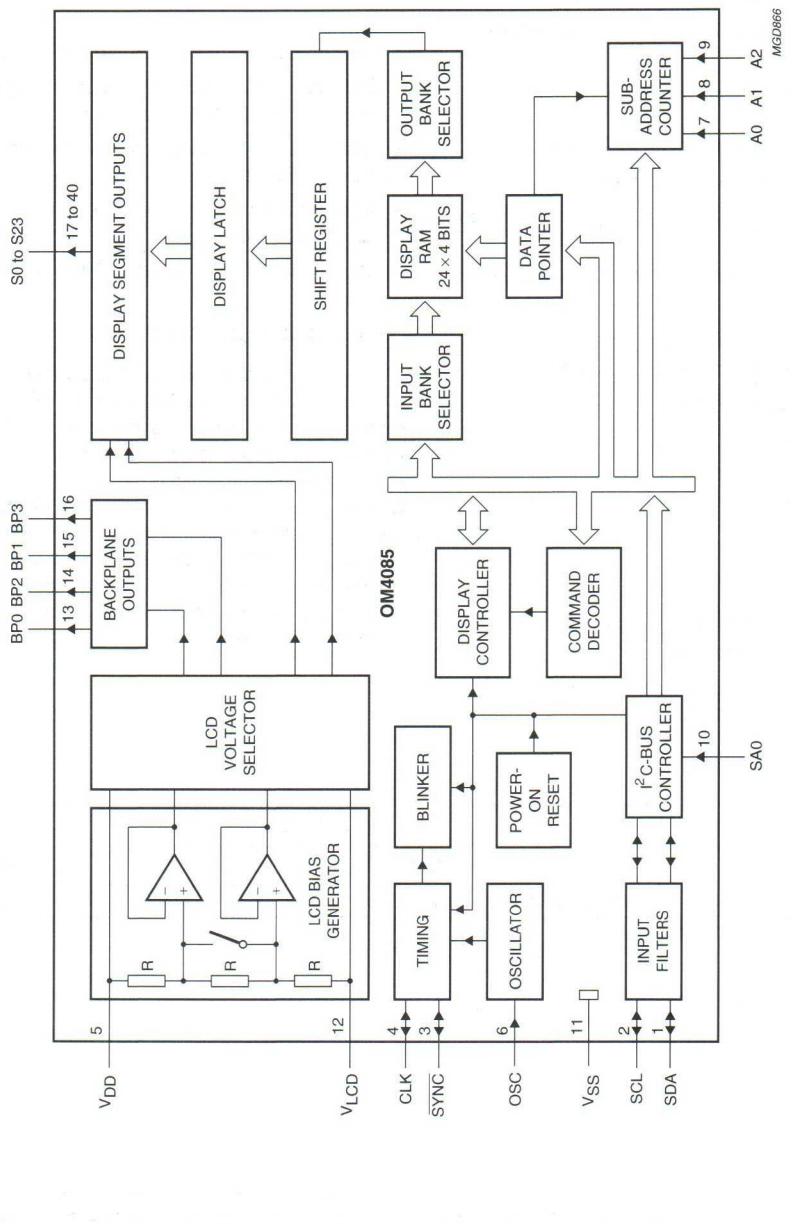


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus data input/output
SCL	2	I²C-bus clock input/output
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	external clock input/output
V_{DD}	5	positive supply voltage
OSC	6	oscillator input
A0	7	I²C-bus subaddress inputs
A1	8	
A2	9	
SA0	10	I²C-bus slave address bit 0 input
V_{SS}	11	logic ground
V_{LCD}	12	LCD supply voltage
BP0	13	LCD backplane outputs
BP2	14	
BP1	15	
BP3	16	
S0 to S23	17 to 40	LCD segment outputs

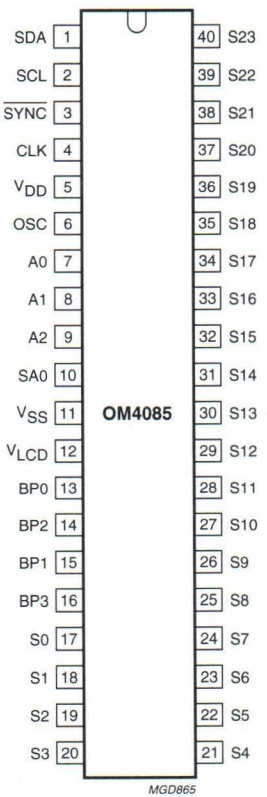


Fig.2 Pin configuration.

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1 FEATURES

- Single-chip LCD controller/driver
- 2-line display of up to 12 characters + 120 icons, or 1-line display of up to 24 characters + 120 icons
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- Icon mode: reduced current consumption while displaying icons only(1)
- Icon blink function
- On-chip:
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240, 5 × 8 characters
- Character generator RAM: 16, 5 × 8 characters; 3 characters used to drive 120 icons, 6 characters used if icon blink feature is used in application
- 4 or 8-bit parallel bus and 2-wire I²C-bus interface
- CMOS compatible
- 18 row, 60 column outputs
- Mux rates 1 : 18 (for normal operation) and 1 : 2 (for icon-only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage range, $V_{DD} - V_{SS}$ = 1.8 to 5.5 V; chip may be driven with two battery cells
- Display supply voltage range, $V_{LCD} - V_{SS}$ = 2.2 to 6.5 V
- Very low current consumption (20 to 120 μA):
  - Icon mode: <25 μA
  - Power-down mode: <2.5 μA.

(1) Icon mode is used to save current. When only icons are displayed, a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

3 GENERAL DESCRIPTION

The PCF2103 family is a low power CMOS LCD controller and driver, designed to drive a dot matrix LCD display of 2 line by 12 or 1 line by 24 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2103 interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters. The letter 'X' in PCF2103X characterizes the built-in character set. Various character sets can be manufactured on request.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2103EU/2/F2	–	chip with bumps in tray	–

5 BLOCK DIAGRAM

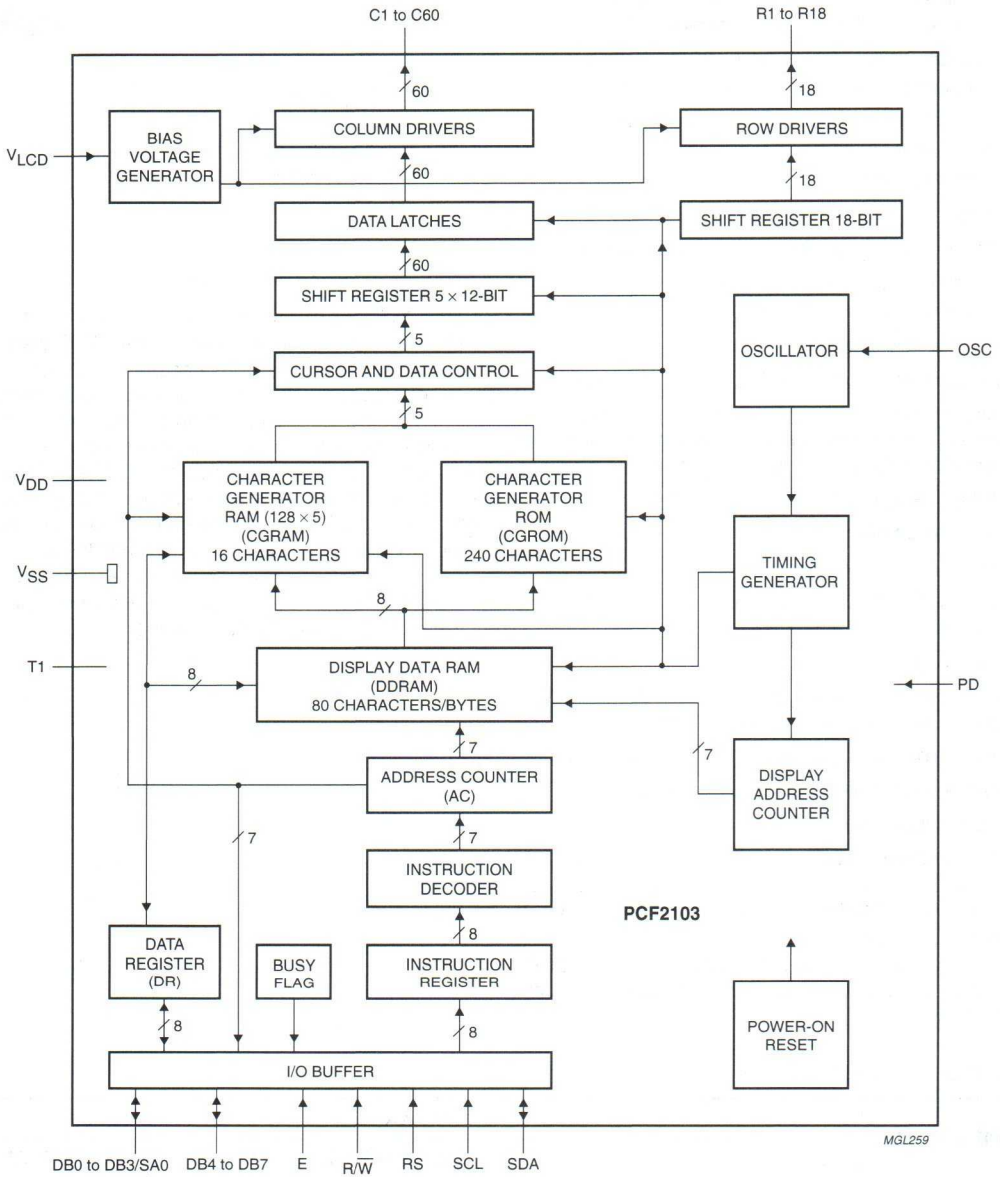


Fig.1 Block diagram.

6 PINNING

SYMBOL	DIE PAD	DESCRIPTION
V_{DD}	1	supply voltage
OSC	2	oscillator/external clock input
PD	3	power-down pad input
T1	4	test pad (connected to V_{SS})
V_{SS}	5	ground
V_{LCD}	6	V_{LCD} input; note 1
R9 to R16	7 to 14	LCD row driver outputs 9 to 16
R18	15	LCD row driver output 18
C60 to C1	16 to 23, 26 to 50, 53 to 77, 80, 81	LCD column driver outputs 60 to 1
R8 to R1	82 to 89	LCD row driver outputs 8 to 1
R17	90	LCD row driver output 17
SCL	91	I^2C-bus serial clock input
SDA	92	I^2C-bus serial data input/output
E	93	data bus clock input
RS	94	register select input
R/$\overline{W}$	95	read/write input
DB7	96	bit of bi-directional data bus
DB6	97	bit of bi-directional data bus
DB5	98	bit of bi-directional data bus
DB4	99	bit of bi-directional data bus
DB3/SA0	100	bit of bi-directional data bus/I^2C-bus address pin
DB2	101	bit of bi-directional data bus
DB1	102	bit of bi-directional data bus
DB0	103	bit of bi-directional data bus

Note

1. This is the voltage used for the generation of LCD bias levels.

Table 1 Pin functions; note 1

NAME	FUNCTION	DESCRIPTION
RS	register select	RS selects the register to be accessed for read and write; there is an internal pull-up on this pin RS = 0 selects the instruction register for write and the busy flag and address counter for read RS = 1 selects the data register for both read and write
R/$\overline{W}$	read/write	R/$\overline{W}$ selects either the read (R/$\overline{W}$ = 1) or write (R/$\overline{W}$ = 0) operation; there is an internal pull-up on this pin
E	data bus clock	pin E is set HIGH to signal the start of a read or write operation; data is clocked in or out of the chip on the negative edge of the clock
DB7 to DB0	data bus	the bi-directional, 3-state data bus transfers data between the system controller and the PCF2103; DB7 may be used as the busy flag, signalling that internal operations are not yet completed; in 4-bit operations the 4 higher order lines DB7 to DB4 are used; DB3 to DB0 must be left open-circuit; there is an internal pull-up on each of the data lines
C1 to C60	column driver outputs	these pins output the data for columns
R1 to R18	row driver outputs	these pins output the row select waveforms to the display; R17 and R18 drive the icons
V_{LCD}	LCD power supply	positive power supply for the liquid crystal display
OSC	oscillator	when the on-chip oscillator is used this pin must be connected to V_{DD}; an external clock signal, if used, is input at this pin
SCL	serial clock line	input for the I²C-bus clock signal
SDA	serial data line	I/O for the I²C-bus data line
SA0	address pin	the hardware sub-address line is used to program the device sub-address for two different PCF2103s on the same I²C-bus
T1	test pad	must be connected to V_{SS}; not user accessible
PD	power-down pad	PD selects chip power-down mode; for normal operation PD = 0

Note

1. When the I²C-bus is used, the parallel interface pin E must be defined as E = 0. In I²C-bus read mode DB7 to DB0 should be connected to V_{DD} or left open-circuit.
   a) When the parallel bus is used, pins SCL and SDA must be connected to V_{SS} or V_{DD}; they may not be left unconnected.
   b) If the 4-bit interface is used without reading out from the PCF2103 (i.e. R/$\overline{W}$ is set permanently to logic 0), the unused ports DB0 to DB3 can either be set to V_{SS} or V_{DD} instead of leaving them open.

7 FUNCTIONAL DESCRIPTION

7.1 LCD bias voltage generator

The intermediate bias voltages for the LCD display are generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system current consumption. The optimum value of V_{LCD} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels and is given by the relationships given in Tables 2 and 3. Using a 5-level bias scheme for 1 : 18 maximum rate allows V_{LCD} <5 V for most LCD liquids.

Table 2 Optimum/maximum values for V_{OP} (off pixels start darkening; $V_{off} = V_{th}$)

MUX RATE	NUMBER OF LEVELS	V_{on}/V_{th}	V_{OP}/V_{th}	V_{OP} (typical; for V_{th} = 1.4 V)
1 : 18	5	1.272	3.7	5.2 V
1 : 2	3	2.236	2.283	3.9 V

Table 3 Minimum values for V_{OP} (on pixels clearly visible; $V_{on} > V_{th}$)

MUX RATE	NUMBER OF LEVELS	V_{on}/V_{th}	V_{OP}/V_{th}	V_{OP} (typical; for V_{th} = 1.4 V)
1 : 18	5	1.12	3.2	4.6 V
1 : 2	3	1.2	1.5	2.1 V

7.2 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and pin OSC must be connected to V_{DD}.

7.3 External clock

If an external clock is to be used, it is input at the OSC pin. The resulting display frame frequency is given by

$$f_{frame} = \frac{f_{osc}}{3072}$$

Only in the power-down state is the clock allowed to be stopped (OSC connected to V_{SS}), otherwise the LCD is frozen in a DC state.

7.4 Power-on reset

The on-chip power-on reset block initializes the chip after power-on or power failure. This is a synchronous reset and requires 3 oscillator cycles to be executed. Afterwards, a clear display is initiated.

7.5 Power-down mode

The chip can be put into power-down mode where all static currents are switched off (no internal oscillator, no bias level generation, all LCD outputs are internally connected to V_{SS}) when PD = 1.

During power-down, the whole chip is being reset and will restart with a clear display after power-down. Therefore, the whole chip has to be initialized after a power-down as after an initial power-up.

7.6 Registers

The PCF2103 has two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register Select signal (RS) determines which register will be accessed. The instruction register stores instruction codes such as 'display clear' and 'cursor shift', and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM). The instruction register can be written from but not read by the system controller. The data register temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM corresponding to the address in the instruction register is written to the data register prior to being read by the 'read data' instruction.

7.7 Busy flag

The busy flag indicates the internal status of the PCF2103. Logic 1 indicates that the chip is busy and further instructions will not be accepted. The busy flag is output at pin DB7 when RS = 0 and R/$\overline{W}$ = 1. Instructions should only be written after checking that the busy flag is logic 0 or waiting for the required number of cycles.

7.8 Address Counter (AC)

The address counter assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the commands 'set CGRAM address' and 'set DDRAM address'. After a read/write operation the address counter is automatically incremented or decremented by 1.
The address counter contents are output to the bus (DB6 to DB0) when RS = 0 and R/$\overline{W}$ = 1.

7.9 Display Data RAM (DDRAM)

The DDRAM stores up to 80 characters of display data represented by 8-bit character codes. RAM locations which are not used for storing display data can be used as general purpose RAM. The basic RAM-to-display addressing scheme is shown in Fig.2. With no display shift the characters represented by the codes in the first 24 RAM locations starting at address 00 in line 1 are displayed. Figures 3 and 4 show the display mapping for right and left shift respectively.

When data is written to or read from the DDRAM wrap-around occurs from the end of one line to the start of the next line. When the display is shifted each line wraps around within itself, independently of the others. Thus all lines are shifted and wrapped around together.
The address ranges and wrap-around operations for the various modes are shown in Table 4.

7.10 Character Generator ROM (CGROM)

The Character Generator ROM (CGROM) generates 240 character patterns in 5 × 8 dot format from 8-bit character codes. Figure 6 shows the character set that is currently implemented.

7.11 Character Generator RAM (CGRAM)

Up to 16 user defined characters may be stored in the CGRAM. Some CGRAM characters (see Fig.14) are also used to drive icons (6 if icons blink and both icon rows are used in application; 3 if no blink but both icon rows are used in application; 0 if no icons are driven by the icon rows). The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Fig.6). Figure 7 shows the addressing principle for the CGRAM.

7.12 Cursor control circuit

The cursor control circuit generates the cursor (underline and/or cursor blink as shown in Fig.5) at the DDRAM address contained in the address counter. When the address counter contains the CGRAM address the cursor will be inhibited.

7.13 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

7.14 LCD row and column drivers

The PCF2103 contains 18 row and 60 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. R17 and R18 drive the icon rows.

The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figures 8, 9 and 10 show typical waveforms. Unused outputs should be left unconnected.

Table 4 Address space and wrap-around operation

MODE	ADDRESS SPACE	READ/WRITE WRAP-AROUND[1]	DISPLAY SHIFT WRAP-AROUND[2]
1 × 24	00H to 4FH	4FH to 00H	4FH to 00H
2 × 12	00H to 27H; 40H to 67H	27H to 40H; 67H to 00H	27H to 00H; 67H to 40H

Notes

1. Moves to next line.
2. Stays within line.

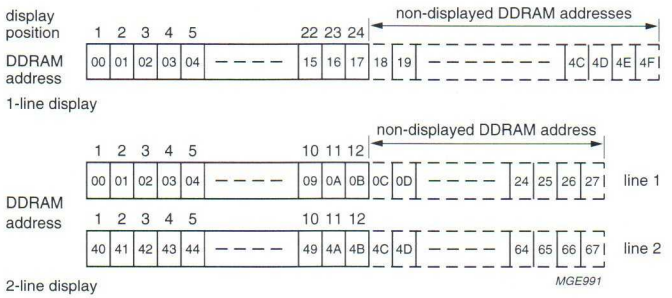


Fig.2 DDRAM-to-display mapping: no shift.

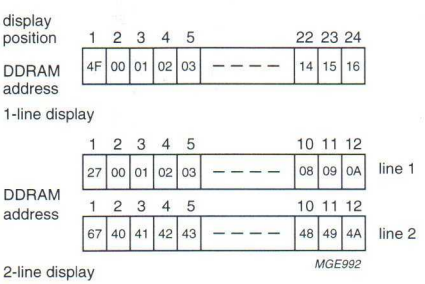


Fig.3 DDRAM-to-display mapping: right shift.

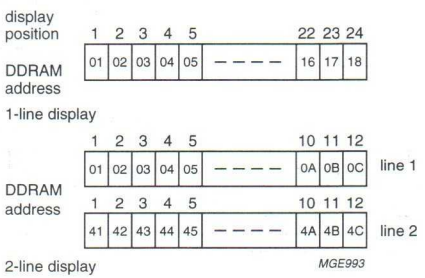
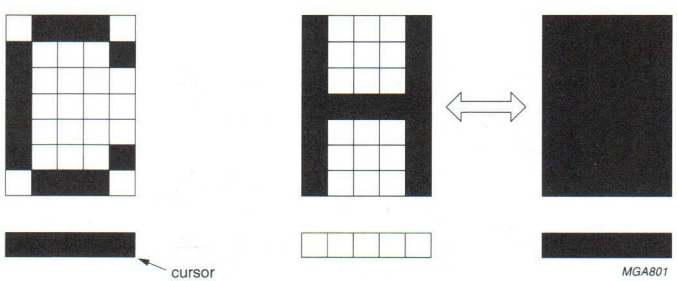


Fig.4 DDRAM-to-display mapping: left shift.



cursor display example

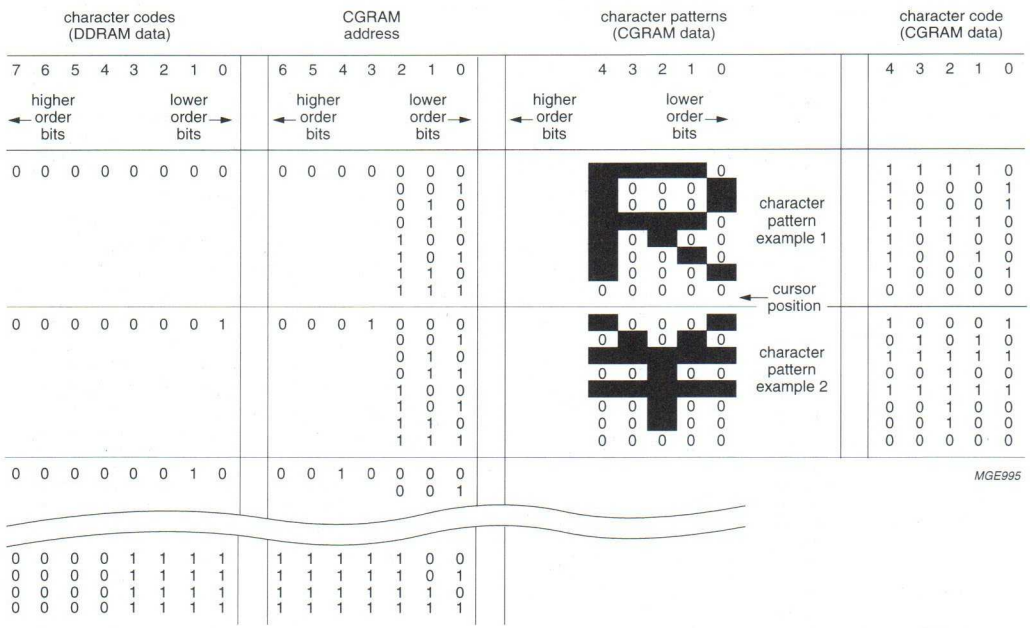
blink display example

Fig.5 Cursor and blink display examples.

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

MGD689

Fig.6 Character set 'E' in CGROM.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th position will appear in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4, as shown in Fig.6.

As shown in Figs 6 and 7, CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the 'set CGRAM address' command. Bit 6 can be set using the 'set DDRAM address' command in the valid address range or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'read busy flag and address counter' command; see Table 7.

Fig.7 Relationship between CGRAM addresses and data and display patterns.

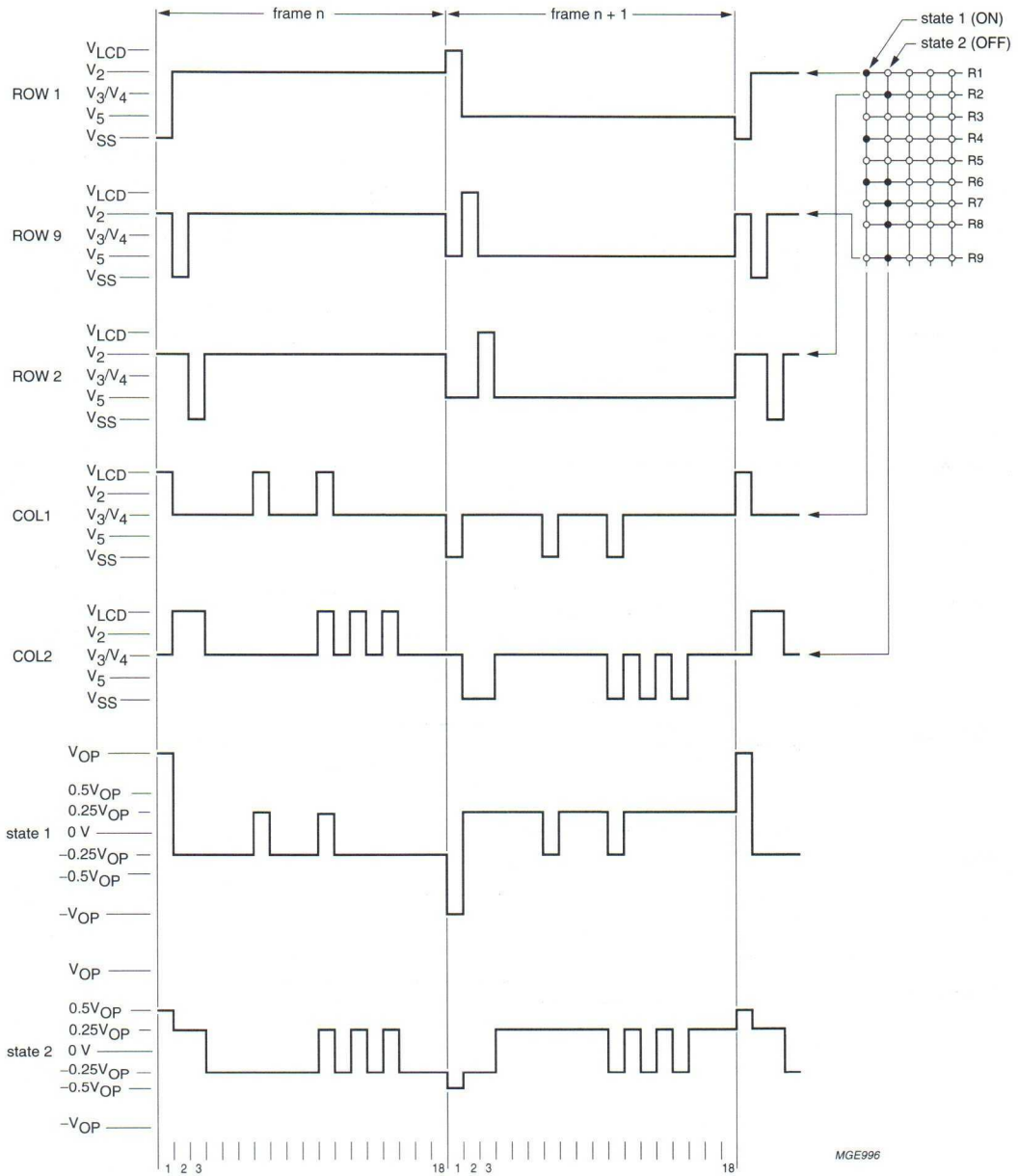


Fig.8 Typical LCD waveforms; character mode.

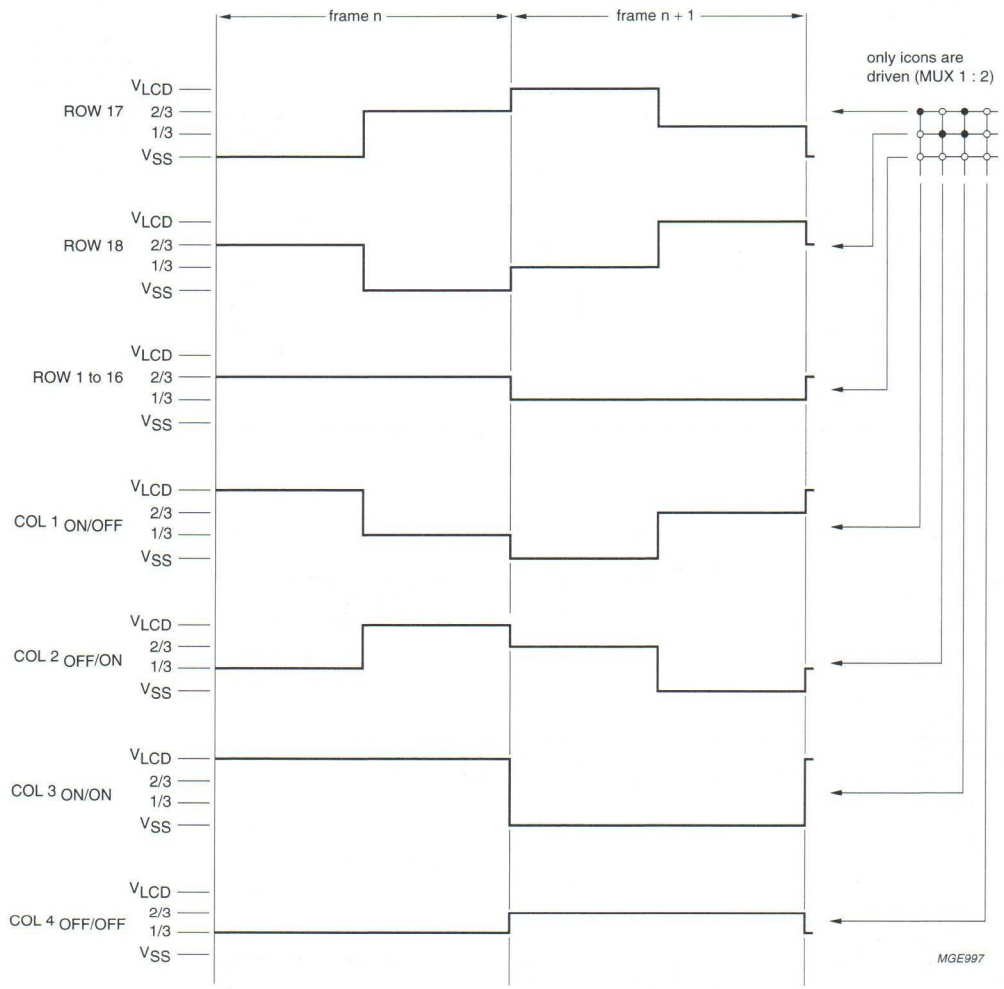
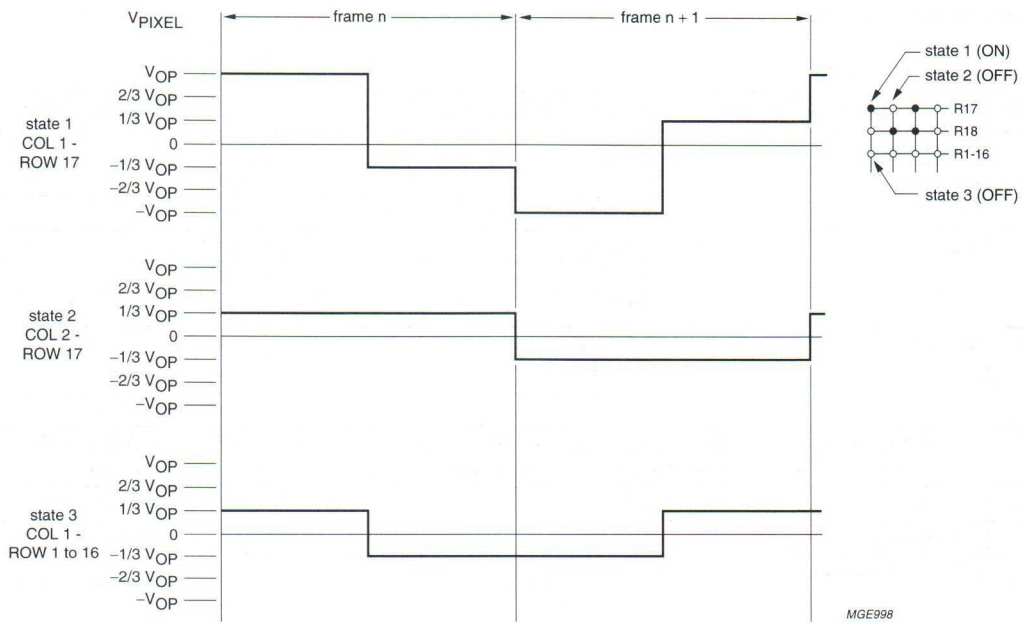


Fig.9 Mux 1 : 2 LCD waveforms; icon mode.



$V_{ON(rms)} = 0.745\ V_{OP}$.

$V_{OFF(rms)} = 0.333\ V_{OP}$.

$$D = \frac{V_{ON}}{V_{OFF}} = 2.23$$

Fig.10 Mux 1 : 2 LCD waveforms; icon mode.

7.15 Reset function

The PCF2103 automatically initializes (resets) when power is turned on. The reset executes a 'clear display' instruction, requiring 165 oscillator cycles. After the reset the chip has the state shown in Table 5.

Table 5 State after reset

STEP	INSTRUCTION	RESET STATE (BIT/REGISTER)	RESET STATE (DESCRIPTION)
1	clear display		
2	entry mode set	I/D = 1	+1 (increment)
		S = 0	no shift
3	display control	D = 0	display off
		C = 0	cursor off
		B = 0	cursor character blink off
4	function set	DL = 1	8-bit interface
		M = 0	1-line display
		H = 0	normal instruction set
5	default address pointer to DDRAM; the Busy Flag (BF) indicates the busy state (BF = 1) until initialization ends; the busy state lasts 2 ms; the chip may also be initialized by software; see Tables 16 and 17		
6	icon control	IM, IB = 00	icons/icon blink disabled
7	display/screen configuration	L, P, Q = 000	default configurations
8	I^2C-bus interface reset		

8 INSTRUCTIONS

Only two PCF2103 registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the microcontroller. Before internal operation, control information is stored temporarily in these registers to allow interface to various types of microcontrollers which operate at different speeds or to allow interface to peripheral control ICs. The format for instructions when I²C-bus control is used is shown in Table 6. The PCF2103 operation is controlled by the instructions given in Table 7 together with their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that:

1. Designate PCF2103 functions such as display format, data length, etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, instructions that perform data transfer with internal RAM are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the microcontroller program load. The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instruction other than the 'read busy flag and address counter' instruction will be executed. Because the busy flag is set to logic 1 while an instruction is being executed, the user should verify that the busy flag is at logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 7. An instruction sent while the busy flag is logic 1 will not be executed.

Table 6 Instruction set for I²C-bus commands

CONTROL BYTE								COMMAND BYTE								I²C-BUS COMMANDS
Co	RS	0	0	0	0	0	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	note 1

Note

1. R/$\overline{W}$ is set together with the slave address.

Table 7 Instruction set with parallel bus commands; note 1

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES
H = 0 or 1												
NOP	0	0	0	0	0	0	0	0	0	0	no operation	3
Function set	0	0	0	0	1	DL	0	M	0	H	sets interface Data Length (DL) and number of display lines (M); extended instruction set control (H)	3
Read busy flag and address counter	0	1	BF	AC							reads the Busy Flag (BF) indicating internal operating is being performed and reads address counter contents	0
Read data	1	1	read data								reads data from CGRAM or DDRAM	3
Write data	1	0	write data								writes data from CGRAM or DDRAM	3
H = 0												
Clear display	0	0	0	0	0	0	0	0	0	1	clears entire display and sets DDRAM address 0 in address counter	165
Return home	0	0	0	0	0	0	0	0	1	0	sets DDRAM address 0 in address counter; also returns shifted display to original position; DDRAM contents remain unchanged	3
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	sets cursor move direction and specifies shift of display; these operations are performed during data write and read	3
Display control	0	0	0	0	0	0	1	D	C	B	sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B); D = 0 (display off) puts chip into power-down mode	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	moves cursor and shifts display without changing DDRAM contents	3
Set CGRAM address	0	0	0	1	A_{CG}						sets CGRAM address; bit 6 is to be set by the command 'set DDRAM address'; look at the description of the commands	3
Set DDRAM address	0	0	1	A_{DD}							sets DDRAM address	3

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES
H = 1												
Reserved	0	0	0	0	0	0	0	0	0	1	do not use	–
Screen configuration	0	0	0	0	0	0	0	0	1	L	set screen configuration	3
Display configuration	0	0	0	0	0	0	0	1	P	Q	set display configuration	3
Icon control	0	0	0	0	0	0	1	IM	IB	0	set icon mode (IM), icon blink (IB)	3
Reserved	0	0	0	0	0	1	X	X	X	X	do not use	–
Reserved	0	0	0	1	X	X	X	X	X	X	do not use	–
Reserved	0	0	1	X	X	X	X	X	X	X	do not use	–

Note

1. X = don't care.

Table 8 Specification of mnemonics used in Table 7

BIT	LOGIC 0	LOGIC 1
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	cursor character blink off: character at cursor position does not blink	cursor character blink on: character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
DL	4 bits	8 bits
H	use basic instruction set	use extended instruction set
L (ignored, if M = 1)	left/right screen: standard connection (as in PCF2114); 1st 12 characters of 24: columns are from 1 to 60; 2nd 12 characters of 24: columns are from 1 to 60	left/right screen: mirrored connection (as in PCF2116); 1st 12 characters of 24: columns are from 1 to 60; 2nd 12 characters of 24: columns are from 60 to 1
P	column data: left to right (as in PCF2116); column data is displayed from 1 to 60	column data: right to left; column data is displayed from 60 to 1
Q	row data: top to bottom (as in PCF2116); row data is displayed from 1 to 16 and icon row data is in 17 and 18	row data: bottom to top; row data is displayed from 16 to 1 and icon row data is in 18 and 17
IM	character mode; full display	icon mode; only icons displayed
IB	icon blink disabled	icon blink enabled
M	1-line by 24 display	2-line by 12 display
C_0	last control byte; see Table 6	another control byte follows after data/command

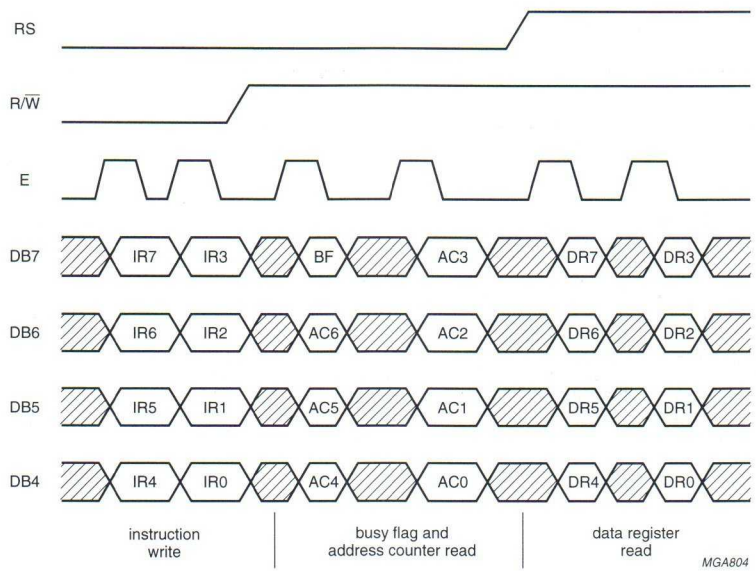
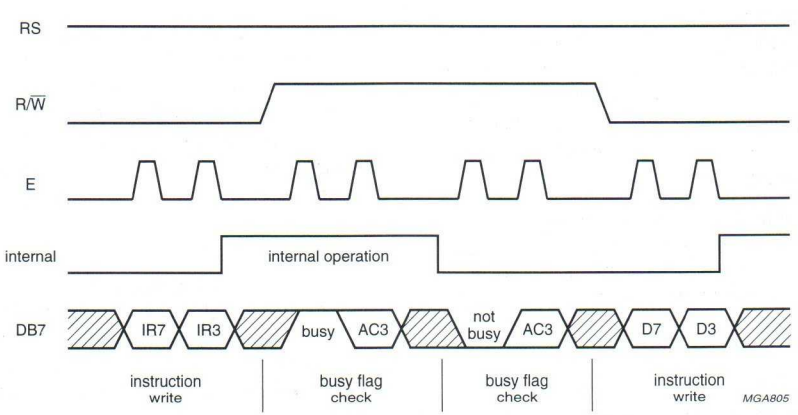


Fig.11 4-bit transfer example.



IR7 and IR3: instruction 7th and 3rd bit.
AC3: address counter 3rd bit.
D7 and D3: data 7th and 3rd bit.

Fig.12 An example of 4-bit data transfer timing sequence.

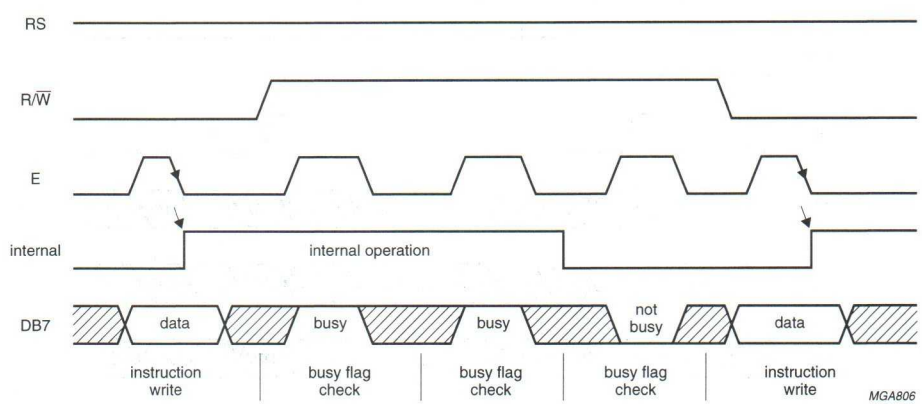


Fig.13 Example of busy flag checking timing sequence.

8.1 Clear display

'Clear display' writes character code 20H into all DDRAM addresses (the character pattern for character code 20H must be a blank pattern), sets the DDRAM address counter to logic 0 and returns display to its original position if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the display. Sets entry mode I/D = 1 (increment mode). S of entry mode does not change.

The instruction 'clear display' requires extra execution time. This may be allowed by checking the Busy Flag (BF) or by waiting until the 165 clock cycles have elapsed. The latter must be applied where no read-back options are foreseen, as in some Chip-On-Glass (COG) applications.

8.2 Return home

'Return home' sets the DDRAM address counter to logic 0 and returns display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the first display line. I/D and S of entry mode do not change.

8.3 Entry mode set

8.3.1 I/D

When I/D = 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor underline and cursor character blink are inhibited when the CGRAM is accessed.

8.3.2 S

When S = 1, the entire display shifts either to the right (I/D = 0) or to the left (I/D = 1) during a DDRAM write. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing into or reading out of the CGRAM. When S = 0 the display does not shift.

8.4 Display control (and partial power-down mode)

8.4.1 D

The display is on when D = 1 and off when D = 0. Display data in the DDRAM are not affected and can be displayed immediately by setting D to logic 1.

When the display is off (D = 0) the chip is in partial power-down mode:

- The LCD outputs are connected to V_{SS}
- Bias generator is turned off.

3 oscillator cycles are required after sending the 'display off' instruction to ensure all outputs are at V_{SS}, afterwards OSC can be stopped. If the oscillator is running during partial power-down mode ('display off') the chip can still execute instructions. Even lower current consumption is obtained by inhibiting the oscillator (OSC = V_{SS}).

To ensure $I_{DD} < 2\ \mu A$ the parallel bus pins DB7 to DB0 should be connected to V_{DD}; RS and R/$\overline{W}$ to V_{DD} or left open-circuit and PD to V_{DD}. Recovery from power-down mode: put PD back to logic 0, if necessary put OSC back to V_{DD} and send a 'display control' instruction with D = 1 to enable the display again.

8.4.2 C

The cursor is displayed when C = 1 and inhibited when C = 0. Even if the cursor disappears, the display functions I/D, etc. remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Fig.5).

8.4.3 B

The character indicated by the cursor blinks when B = 1. The cursor character blink is displayed by switching between display characters and all dots on with a period of approximately 1 s, with $f_{BLINK} = \frac{f_{osc}}{52224}$

The cursor underline and the cursor character blink can be set to display simultaneously.

8.5 Cursor or display shift

'Cursor/display shift' moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2-line displays, the cursor moves to the next line when it passes the last position (40) of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line.

The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the 'cursor shift'.

8.6 Function set

8.6.1 DL (PARALLEL MODE ONLY)

Sets interface data width. Data is sent or received in bytes (DB7 to DB0) when DL = 1 or in two nibbles (DB7 to DB4) when DL = 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus. In a 4-bit application DB3 to DB0 should be left open-circuit (internal pull-ups). Hence in the first 'function set' instruction after power-on N and H are set to logic 1. A second 'function set' must then be sent (2 nibbles) to set N and H to their required values.

'Function set' from the I²C-bus interface sets the DL bit to logic 1.

8.6.2 M

Chooses either 1-line by 24 display (M = 0) or 2-line by 12 display (M = 1).

8.6.3 H

When H = 0 the chip can be programmed via the standard 11 instruction codes used in the PCF2116 and other LCD controllers.

When H = 1 the extended range of instructions will be used. These are mainly for controlling the display configuration and the icons.

8.7 Set CGRAM address

'Set CGRAM address' sets bits 5 to 0 of the CGRAM address A_{CG} into the address counter (binary A[5] to A[0]). Data can then be written to or read from the CGRAM.

Attention: the CGRAM address uses the same address register as the DDRAM address and consists of 7 bits (binary A[6] to A[0]). With the 'set CGRAM address' command, only bits 5 down to 0 are set. Bit 6 can be set using the 'set DDRAM address' command first, or by using the auto-increment feature during CGRAM write.
All bits 6 to 0 can be read using the 'read busy flag and address counter' command.

When writing to the lower part of the CGRAM, ensure that bit 6 of the address is not set (e.g. by an earlier DDRAM write or read action).

8.8 Set DDRAM address

'Set DDRAM address' sets the DDRAM address A_{DD} into the address counter (binary A[6] to A[0]). Data can then be written to or read from the DDRAM.

8.9 Read busy flag and address counter

'Read busy flag and address counter' reads the Busy Flag (BF) and Address Counter (AC). BF = 1 indicates that an internal operation is in progress. The next instruction will not be executed until BF = 0, so BF should be checked before sending another instruction.

At the same time, the value of the address counter expressed in binary A[6] to A[0] is read out. The address counter is used by both CGRAM and DDRAM, and its value is determined by the previous instruction.

8.10 Write data to CGRAM or DDRAM

'Write data' writes binary 8-bit data D[7] to D[0] to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written into is determined by the previous 'set CGRAM address' or 'set DDRAM address' command. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits D[4] to D[0] of CGRAM data are valid, bits D[7] to D[5] are 'don't care'.

8.11 Read data from CGRAM or DDRAM

'Read data' reads binary 8-bit data D[7] to D[0] from the CGRAM or DDRAM.

The most recent 'set address' command determines whether the CGRAM or DDRAM is to be read.

The 'read data' instruction gates the content of the Data Register (DR) to the bus while pin E is HIGH. After pin E goes LOW again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

It should be noted that there are only three instructions that update the Data Register (DR). These are:

- 'set CGRAM address'
- 'set DDRAM address'
- 'read data' from CGRAM or DDRAM.

Other instructions (e.g. 'write data', 'cursor/display shift', 'clear display', 'return home') do not modify the data register content.

8.12 Extended function set instructions and features

8.12.1 NEW INSTRUCTIONS

H = 1 sets the chip into alternate instruction set mode.

8.12.2 ICON CONTROL

The PCF2103 can drive up to 120 icons. See Fig.14 for CGRAM to icon mapping.

8.12.3 IM

When IM = 0 the chip is in character mode. In character mode characters and icons are driven (mux 1 : 18).

When IM = 1 the chip is in icon mode. In icon mode only the icons are driven (mux 1 : 2).

8.12.4 IB

Icon blink control is independent of the cursor/character blink function.

When IB = 0 icon blink is disabled. Icon data is stored in CGRAM character 0 to 2 ($3 \times 8 \times 5 = 120$ bits for 120 icons).

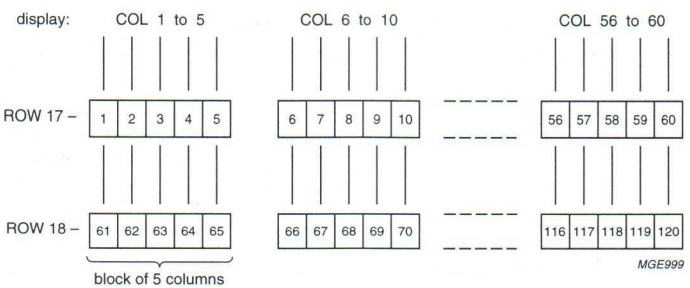
When IB = 1 icon blink is enabled. In this case each icon is controlled by two bits. Blink consists of two half phases (corresponding to the cursor on and off phases called even and odd phases hereafter).

Icon states for the even phase are stored in CGRAM characters 0 to 2 ($3 \times 8 \times 5 = 120$ bits for 120 icons). These bits also define the icon state when the icon blink is not used.

Icon states for the odd phase are stored in CGRAM character 4 to 6 (another 120 bits for the 120 icons). When icon blink is disabled CGRAM characters 4 to 6 may be used as normal CGRAM characters.

Table 9 Blink effect for icons and cursor character blink

PARAMETER	EVEN PHASE	ODD PHASE
Cursor underline	on	off
Cursor character blink	block (all on)	normal (display character)
Icons	state 1: CGRAM characters 0 to 2	state 2: CGRAM characters 4 to 6



icon no.	phase	ROW/COL	character codes	CGRAM address	CGRAM data	icon view
			7 6 5 4 3 2 1 0 MSB LSB	6 5 4 3 2 1 0 MSB LSB	4 3 2 1 0 MSB LSB	
1-5	even	17/1-5	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	1 0 1 0 1	
6-10	even	17/6-10	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1	0 1 0 1 0	
11-15	even	17/11-15	0 0 0 0 0 0 0 0	0 0 0 0 0 1 0	0 1 1 1 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
56-60	even	17/56-60	0 0 0 0 0 0 0 1	0 0 0 1 0 1 1	1 1 1 1 1	
61-65	even	18/1-5	0 0 0 0 0 0 0 1	0 0 0 1 1 0 0	1 1 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
116-120	even	18/56-60	0 0 0 0 0 0 1 0	0 0 1 0 1 1 1	1 1 1 0 1	
1-5	odd (blink)	17/1-5	0 0 0 0 0 1 0 0	0 1 0 0 0 0 0	0 0 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
116-120	odd (blink)	18/56-60	0 0 0 0 0 1 1 0	0 1 1 0 0 1 1	0 0 1 1 0	

MGG001

CGRAM data bit = logic 1 turns the icon on, data bit = logic 0 turns the icon off.
Data in character codes 0 to 2 define the icon states when icon blink is disabled or during the even phase when icon blink is enabled.
Data in character codes 4 to 6 define the icon state during the odd phase when icon blink is enabled (not used for icons when icon blink is disabled).

Fig.14 CGRAM-to-icon mapping.

8.12.5 SCREEN CONFIGURATION

The default value for L is logic 0. In the event of L = 0 the two halves of a split screen are connected in a standard way i.e. column 1/61, 2/62 to 60/120. In the event of L = 1 the two halves of a split screen are connected in a mirrored way i.e. column 1/120, 2/119 to 60/61. This allows single layer PCB or glass layout.

8.12.6 DISPLAY CONFIGURATION

The default value for P and Q is logic 0. P = 1 mirrors the column data whereas Q = 1 mirrors the row data.

8.12.7 REDUCING CURRENT CONSUMPTION

Reducing current consumption can be achieved by one of the options mentioned in Table 10.

Table 10 Reducing current consumption

ORIGINAL MODE	ALTERNATIVE MODE
Character mode	icon mode (control bit IM)
Display on	display off (control bit D)

9 INTERFACE TO MICROCONTROLLER

9.1 Parallel interface

The PCF2103 can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB7 to DB0. Three further control lines E, RS and R/$\overline{W}$ are required; see Table 1.

In 4-bit mode data is transferred in two cycles of 4 bits each using pins DB7 to DB4 for transaction. The higher order bits (corresponding to DB7 to DB4 in 8-bit mode) are sent in the first cycle and the lower order bits (DB3 to DB0 in 8-bit mode) in the second. Data transfer is complete after two 4-bit data transfers. Note that two cycles are also required for the busy flag check. 4-bit operation is selected by instruction. See Figs 11 to 14 for examples of bus protocol.

In 4-bit mode pins DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

9.2 I²C-bus interface

9.2.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH-level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

9.2.2 I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF2103 read and write cycles is shown in Figs 20 to 21. The slow down feature of the I²C-bus protocol (receiver holds SCL low during internal operations) is not used in the PCF2103.

9.2.3 Definitions

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

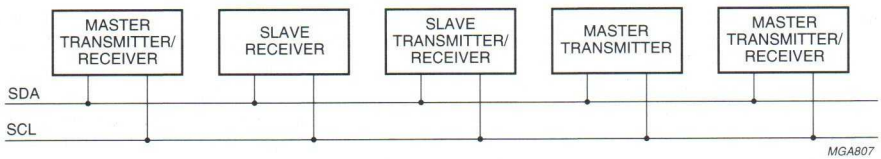


Fig.15 System configuration.

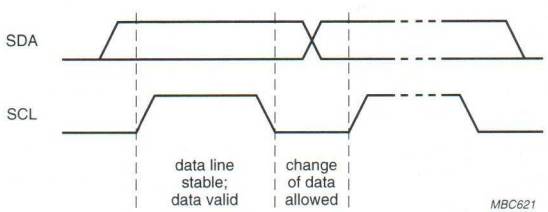


Fig.16 Bit transfer.

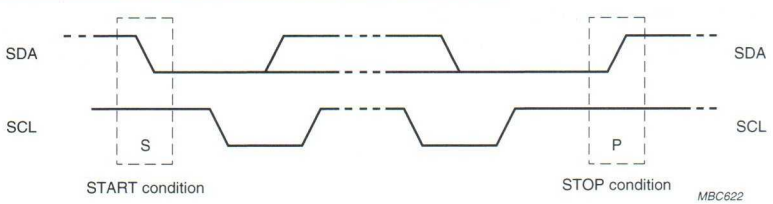


Fig.17 Definition of START and STOP conditions.

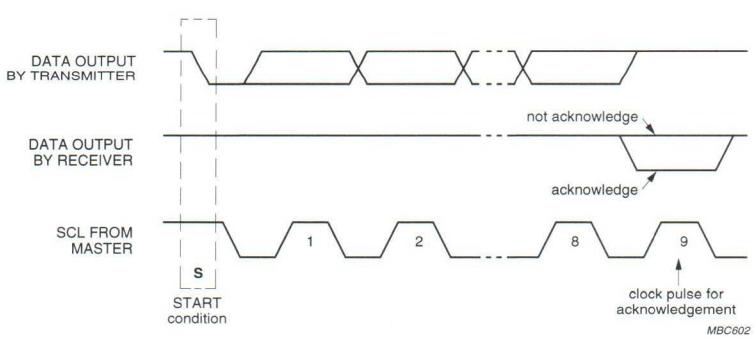


Fig.18 Acknowledgement on the I²C-bus.

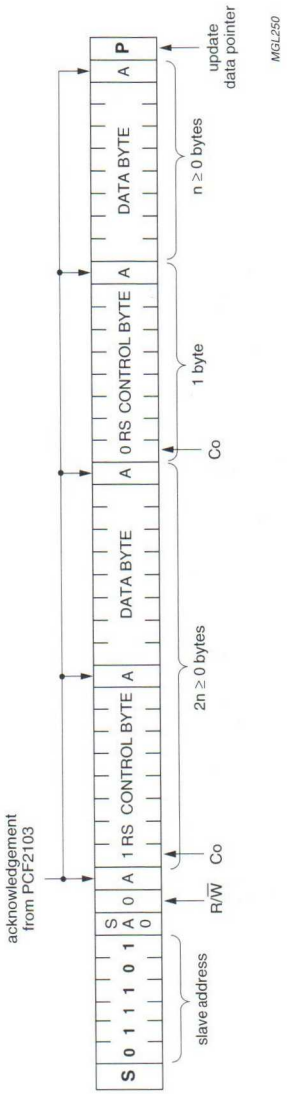
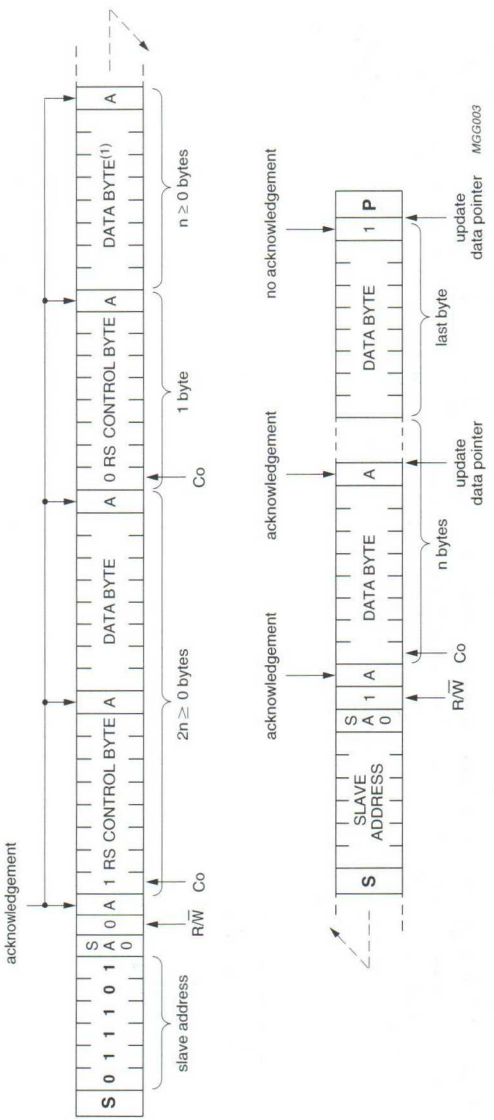


Fig.19 Master transmits to slave receiver; write mode.



(1) Last data byte is a dummy byte (may be omitted).

Fig.20 Master reads after setting word address; write word address, set RS; 'read data'.

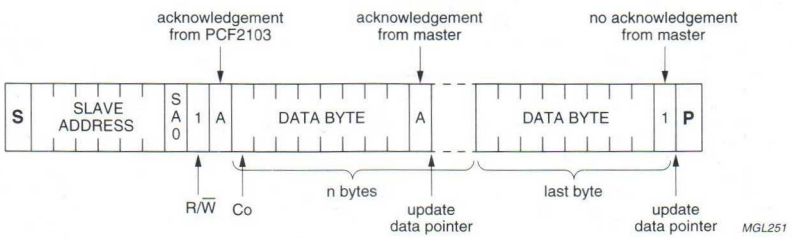


Fig.21 Master reads slave immediately after first byte; read mode (RS previously defined).

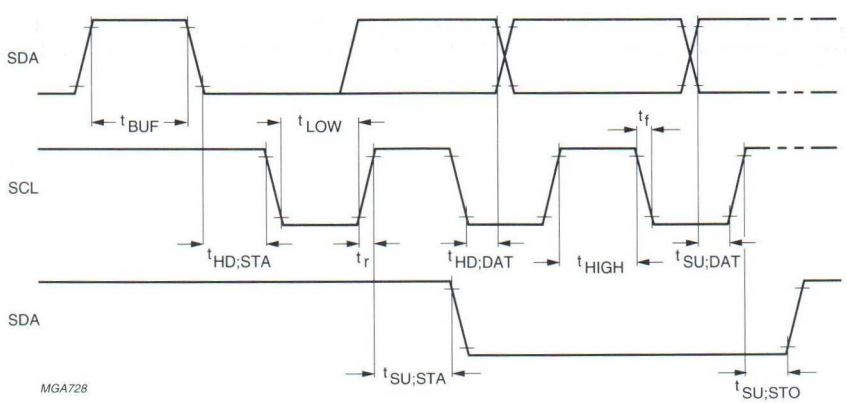


Fig.22 I²C-bus timing diagram.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_{LCD}	LCD supply voltage	−0.5	+7.5	V
$V_{I(1)}$	input voltage on pins OSC, RS, R/$\overline{W}$, E and DB7 to DB0	−0.5	V_{DD} + 0.5	V
$V_{I(2)}$	input voltage on pins SCL and SDA	−0.5	+6.5	V
V_O	output voltage on pins R1 to R18, C1 to C60 and V_{LCD}	−0.5	V_{LCD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
I_{DD}, I_{SS} and I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	−50	+50	mA
P_{tot}	total power dissipation	−	400	mW
P/out	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

12 DC CHARACTERISTICS

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.2 to 6.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		1.8	–	5.5	V
V_{LCD}	LCD supply voltage		2.2	–	6.5	V
I_{SS}	supply current	note 1	–	60	120	µA
		V_{DD} = 3 V; V_{LCD} = 5 V; notes 1 and 2	–	45	80	µA
		icon mode; V_{DD} = 3 V; V_{LCD} = 2.5 V; notes 1 and 2	–	25	45	µA
		power-down mode; V_{DD} = 3 V; V_{LCD} = 2.5 V; DB7 to DB0, RS and R/$\overline{W}$ = 1; OSC = 0; PD = 1; note 1	–	2	6	µA
V_{POR}	power-on reset voltage	note 3	–	1.3	1.6	V
Logic						
V_{IL}	LOW-level input voltage on pins T1, E, RS, R/$\overline{W}$, DB7 to DB0 and SA0		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage on pins T1, E, RS, R/$\overline{W}$, DB7 to DB0 and SA0		$0.7V_{DD}$	–	V_{DD}	V
$V_{IL(PD)}$	LOW-level input voltage on pin PD		0	–	$0.2V_{DD}$	V
$V_{IH(PD)}$	HIGH-level input voltage on pin PD		$0.8V_{DD}$	–	V_{DD}	V
$V_{IL(OSC)}$	LOW-level input voltage on pin OSC		0	–	V_{DD} − 1.5	V
$V_{IH(OSC)}$	HIGH-input voltage on pin OSC		V_{DD} − 0.1	–	V_{DD}	V
$I_{OL(DB)}$	LOW-level output current on pins DB7 to DB0	V_{OL} = 0.4 V; V_{DD} = 5 V	1.6	4	–	mA
$I_{OH(DB)}$	HIGH-level output current on pins DB7 to DB0	V_{OH} = 4 V; V_{DD} = 5 V	−1	−8	–	mA
I_{pu}	pull-up current on pins DB7 to DB0	V_I = V_{SS}	0.04	0.12	1	µA
I_L	leakage current on pins OSC, E, RS, R/$\overline{W}$, DB7 to DB0 and SA0	V_I = V_{DD} or V_{SS}	−1	–	+1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus						
SDA AND SCL						
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	5.5	V
I_L	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	μA
C_i	input capacitance	note 4	–	–	10	pF
I_{OL}	LOW-level output current pin SDA	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
LCD outputs						
$R_{o(ROW)}$	row output resistance on pins R1 to R18	note 5	–	10	30	kΩ
$R_{o(COL)}$	column output resistance on pins C1 to C60	note 5	–	15	40	kΩ
$V_{bias(tol)}$	bias tolerance on pins R1 to R18 and C1 to C60	note 6	–	20	130	mV

Notes

1. LCD outputs are open-circuit; inputs at V_{DD} or V_{SS}; bus inactive.
2. T_{amb} = 25 °C; f_{osc} = 200 kHz.
3. Resets all logic when $V_{DD} < V_{POR}$; 3 oscillator clock cycles required.
4. Tested on sample basis.
5. Resistance of output terminals (R1 to R18 and C1 to C60) with a load current of 20 μA; outputs measured one at a time.
6. LCD outputs open-circuit.

13 AC CHARACTERISTICS

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.2 – 6.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{fr(LCD)}$	LCD frame frequency (internal clock)	V_{DD} = 5.0 V	45	81	147	Hz
f_{osc}	oscillator frequency (not available at any pin)		140	250	450	kHz
$f_{osc(ext)}$	external clock frequency		140	–	450	kHz
t_{OSCST}	oscillator start-up time after PD going from logic 1 to logic 0		–	200	300	µs
Bus timing characteristics: parallel interface; note 1						
WRITE OPERATION (WRITING DATA FROM MICROCONTROLLER TO PCF2103); see Fig.23						
$T_{en(cy)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{su(D)}$	data set-up time		60	–	–	ns
$t_{h(D)}$	data hold time		25	–	–	ns
READ OPERATION (READING DATA FROM PCF2103 TO MICROCONTROLLER); see Fig.24						
$T_{en(cy)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{d(D)}$	data delay time		–	–	150	ns
$t_{h(D)}$	data hold time		20	–	100	ns
Timing characteristics: I^2C-bus interface; note 1						
f_{SCL}	SCL clock frequency		–	–	400	kHz
t_{LOW}	SCL clock LOW period		1.3	–	–	µs
t_{HIGH}	SCL clock HIGH period		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
t_r	SCL and SDA rise time		–	–	300	ns
t_f	SCL and SDA fall time		–	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns

Note

1. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

14 TIMING CHARACTERISTICS

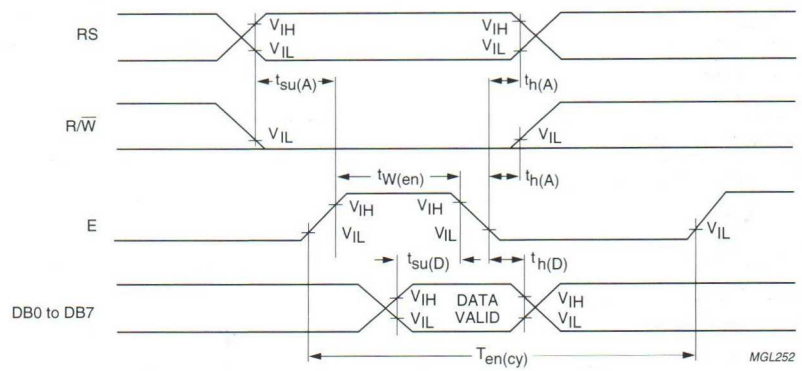


Fig.23 Parallel bus write operation sequence; writing data from microcontroller to PCF2103.

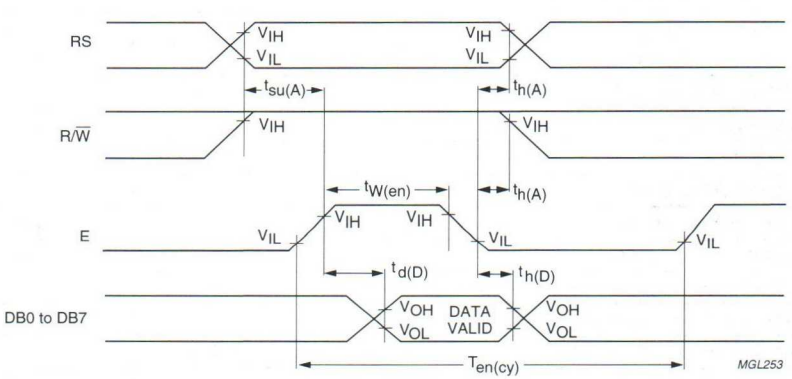


Fig.24 Parallel bus read operation sequence; reading data from PCF2103 to microcontroller.

15 APPLICATION INFORMATION

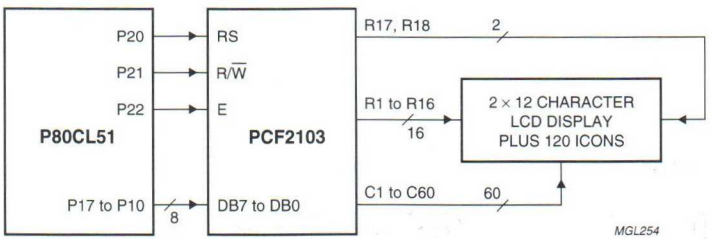


Fig.25 Direct connection to 8-bit microcontroller; 8-bit bus.

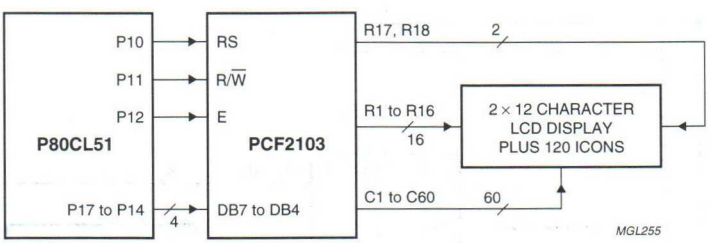


Fig.26 Direct connection to 8-bit microcontroller; 4-bit bus.

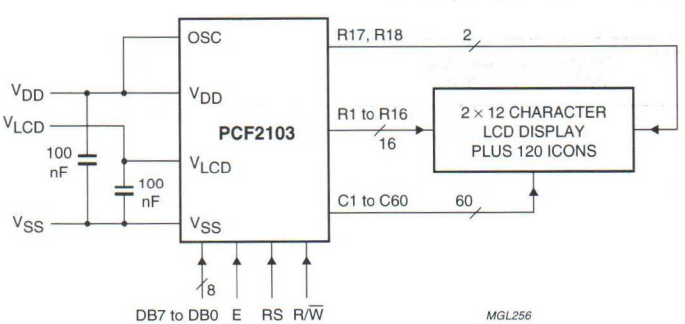


Fig.27 Application example using parallel interface.

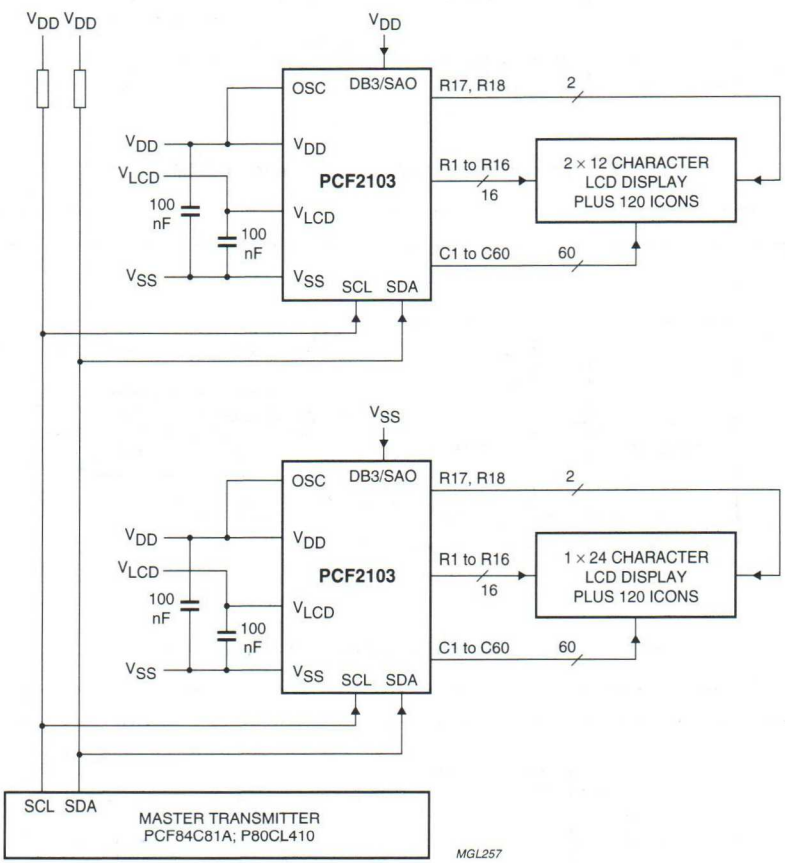


Fig.28 Application using I²C-bus interface.

15.1 4-bit operation, 1-line display using internal reset

The program must set functions prior to 4-bit operation; Table 11 shows an example. When power is turned on, 8-bit operation is automatically selected and the PCF2103 attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB0 to DB3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 11 step 3). Thus, DB4 to DB7 of the 'function set' are written twice.

15.2 8-bit operation, 1-line display using internal reset

Table 12 shows an example of a 1-line display in 8-bit operation. The PCF2103 functions must be set by the 'function set' instruction prior to display. Since the DDRAM can store data for 80 characters, the RAM can be used for advertising displays when combined with display shift operation.

Since the display shift operation changes display position only and DDRAM contents remain unchanged, display data entered first can be displayed when the 'return home' operation is performed.

15.3 8-bit operation, 2-line display

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the eighth character is completed (see Table 6). It should be noted that both lines of the display are always shifted together; data does not shift from one line to the other.

15.4 I²C-bus operation, 1-line display

A control byte is required with most commands (see Table 15).

Table 11 4-bit operation, 1-line display example; using internal reset

STEP	INSTRUCTION						DISPLAY	OPERATION
1	power supply on (PCF2103 is initialized by the internal reset circuit)							initialized; no display appears
2	function set							
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4		
	0	0	0	0	1	0		sets to 4-bit operation; in this instance operation is handled as 8-bit by initialization and only this instruction completes with one write
3	function set							
	0	0	0	0	1	0		
	0	0	0	0	0	0		sets to 4-bit operation, selects 1-line display and $V_{LCD} = V_0$; 4-bit operation starts from this point and resetting is needed
4	display on/off control							
	0	0	0	0	0	0	_	
	0	0	1	1	1	0		turns on display and cursor; entire display is blank after initialization
5	entry mode set							
	0	0	0	0	0	0	_	
	0	0	0	1	1	0		sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DD/CGRAM; display is not shifted
6	'write data' to CGRAM/DDRAM							
	1	0	0	1	0	1	**P**_	
	1	0	0	0	0	0		writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right

Table 12 8-bit operation, 1-line display example; using internal reset (character set 'A')

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2103 is initialized by the internal reset function)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P_**	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH_**	writes 'H'
7 to 11			
12	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS_**	writes 'S'
13	entry mode set 0 0 0 0 0 0 0 1 1 1	**PHILIPS_**	sets mode for display shift at the time of write
14	'write data' to CGRAM/DDRAM 1 0 0 0 1 0 0 0 0 0	**HILIPS _**	writes space
15	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ILIPS M_**	writes 'M'
16			

STEP	INSTRUCTION	DISPLAY	OPERATION
17	'write data' to CGRAM/DDRAM 1 0 0 0 1 0 0 1 1 1 1	**MICROKO_**	writes 'O'
18	cursor/display shift 0 0 0 0 0 0 1 0 0 0 0	**MICROK<u>O</u>**	shifts only the cursor position to the left
19	cursor/display shift 0 0 0 0 0 0 1 0 0 0 0	**MICRO<u>K</u>O**	shifts only the cursor position to the left
20	'write data' to CGRAM/DDRAM 1 0 0 0 1 0 0 0 0 1 1	**ICRO<u>K</u>O**	writes 'C' correction; the display moves to the left
21	cursor/display shift 0 0 0 0 0 0 1 1 1 0 0	**MICROK<u>O</u>**	shifts the display and cursor to the right
22	cursor/display shift 0 0 0 0 0 0 1 0 1 0 0	**MICROCO_**	shifts only the cursor to the right
23	'write data' to CGRAM/DDRAM 1 0 0 0 1 0 0 1 1 0 1	**ICROCOM_**	writes 'M'
24			
25	return home 0 0 0 0 0 0 0 0 0 1 0	**<u>P</u>HILIPS M**	returns both display and cursor to the original position (address 0)

Table 13 8-bit operation, 1-line display and icon example; using internal reset (character set 'A')

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2103 is initialized by the internal reset function)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	set CGRAM address 0 0 0 1 0 0 0 0 0 0	_	sets the CGRAM address to position of character 0; the CGRAM is selected
6	'write data' to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon even phase; icons appear
7			
8	set CGRAM address 0 0 0 1 1 1 0 0 0 0	_	sets the CGRAM address to position of character 4; the CGRAM is selected
9	'write data' to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon odd phase
10			
11	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 1
12	icon control 0 0 0 0 0 0 1 0 1 0	_	icons blink
13	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 0

STEP	INSTRUCTION	DISPLAY	OPERATION
14	set DDRAM address 0 0 1 0 0 0 0 0 0 0		sets the DDRAM address to the first position; DDRAM is selected
15	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes 'P'; the cursor is incremented by 1 and shifted to the right
16	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH**_	writes 'H'
17 to 20			
21	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS**	returns both display and cursor to the original position (address 0)

Table 14 8-bit operation, 2-line display example; using internal reset

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2103 is initialized by the internal reset function)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 0 0		sets to 8-bit operation; selects 2-line display and voltage generator off
3	display on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the CG/DDRAM; display is not shifted
5	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	P_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6 to 10			
11	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS_**	writes 'S'
12	set DDRAM address 0 0 1 1 0 0 0 0 0 0	**PHILIPS** _	sets DDRAM address to position the cursor at the head of the 2nd line
13	'write data' to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 0 1	**PHILIPS** **M_**	writes 'M'
14 to 19			

STEP	INSTRUCTION	DISPLAY	OPERATION
20	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	PHILIPS MICROCO_	writes 'O'
21	'write data' to CGRAM/DDRAM 0 0 0 0 0 0 0 1 1 1	PHILIPS MICROCO_	sets mode for display shift at the time of write
22	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	HILIPS ICROCOM_	writes 'M'; display is shifted to the left; the first and second lines shift together
23 . .			
24	return home 0 0 0 0 0 0 0 0 1 0	PHILIPS MICROCOM	returns both display and cursor to the original position (address 0)

Table 15 Example of I²C-bus operation; 1-line display (using internal reset, assuming SA0 = V_{SS}; note 1)

STEP	INSTRUCTION	DISPLAY	OPERATION
1	I²C-bus start		initialized; no display appears
2	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1		during the acknowledge cycle SDA will be pulled-down by the PCF2103
3	send a control byte for 'function set' Co RS 0 0 0 0 0 0 Ack 0 0 0 0 0 0 0 0 1		control byte sets RS for following data bytes
4	function set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 1 X 0 0 0 0 1		selects 1-line display; SCL pulse during acknowledge cycle starts execution of instruction
5	display on/off control DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 1 1 1 0 1	_	turns on display and cursor; entire display shows character 20H (blank in ASCII-like character sets)
6	entry mode set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 1 1 0 1	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM; display is not shifted
7	I²C-bus start	_	for writing data to DDRAM, RS must be set to 1; therefore a control byte is needed
8	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1	_	
9	send a control byte for 'write data' Co RS 0 0 0 0 0 0 Ack 0 1 0 0 0 0 0 0 1	_	
10	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 0 0 1	 **P**_	writes 'P'; the DDRAM has been selected at power-up; the cursor is incremented by 1 and shifted to the right

STEP	INSTRUCTION	DISPLAY	OPERATION
11	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 1	**PH_**	writes 'H'
12 to 15			
16	'write data' to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 1 1 1	**PHILIPS_**	writes 'S'
17	(optional I^2C-bus stop) I^2C-bus start + slave address for write (as step 8)	**PHILIPS_**	
18	control byte Co RS 0 0 0 0 0 0 Ack 1 0 0 0 0 0 0 0 1	**PHILIPS_**	
19	return home DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 0 1 0 1	**PHILIPS**	sets DDRAM address 0 in address counter (also returns shifted display to original position; DDRAM contents unchanged); this instruction does not update the Data Register (DR)
20	I^2C-bus start	**PHILIPS**	
21	slave address for read SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 1 1	**PHILIPS**	during the acknowledge cycle the content of the DR is loaded into the internal I^2C-bus interface to be shifted out; in the previous instruction neither a 'set address' nor a 'read data' has been performed; therefore the content of the DR was unknown; R/$\overline{W}$ has to be set to logic 1 while still in I^2C-bus write mode
22	control byte for read Co RS 0 0 0 0 0 0 Ack 0 1 1 0 0 0 0 0 1	**PHILIPS**	DDRAM content will be read from following instructions

STEP	INSTRUCTION	DISPLAY	OPERATION
23	'read data': 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack X X X X X X X X 0	PHILIPS	8 × SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA; MSB is DB7; during master acknowledge content of DDRAM address 01 is loaded into the I²C-bus interface
24	'read data': 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 0	PHILIPS	8 × SCL; code of letter 'H' is read first; during master acknowledge code of 'I' is loaded into the I²C-bus interface
25	'read data': 8 × SCL + no master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 1 1	PHILIPS	no master acknowledge; after the content of the I²C-bus interface register is shifted out no internal action is performed; no new data is loaded to the interface register, Data Register (DR) is not updated, Address Counter (AC) is not incremented and cursor is not shifted
26	I²C-bus stop	PHILIPS	

Notes

1. X = don't care.
2. SDA is left at high-impedance by the microcontroller during the read acknowledge.

Table 16 Initialization by instruction, 8-bit interface (note 1)

STEP										DESCRIPTION
power-on or unknown state										
wait 2 ms after V_{DD} rises above V_{POR}										
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
wait 2 ms										
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
wait more than 40 µs										
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
										BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 4)
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	function set (interface is 8 bits long); specify the number of display lines
0	0	0	0	1	1	0	M	0	H	
0	0	0	0	0	0	1	0	0	0	display off
0	0	0	0	0	0	0	0	0	1	clear display
0	0	0	0	0	0	0	1	I/D	S	entry mode set
Initialization ends										

Note

1. X = don't care.

Table 17 Initialization by instruction, 4-bit interface; not applicable for I²C-bus operation

STEP						DESCRIPTION
Power-on or unknown state						
			↓			
Wait 2 ms after V_{DD} rises above V_{POR}						
			↓			
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
			↓			
Wait 2 ms						
			↓			
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
			↓			
Wait 40 μs						
			↓			
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
			↓			BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 4)
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	function set (set interface to 4 bits long)
0	0	0	0	1	0	interface is 8 bits long
0	0	0	0	1	0	function set (interface is 4 bits long)
0	0	0	M	0	H	specify number of display lines
0	0	0	0	0	0	
0	0	1	0	0	0	display off
0	0	0	0	0	0	clear display
0	0	0	0	0	1	
0	0	0	0	0	0	entry mode set
0	0	0	1	I/D	S	
			↓			
Initialization ends						

16 BONDING PAD LOCATIONS

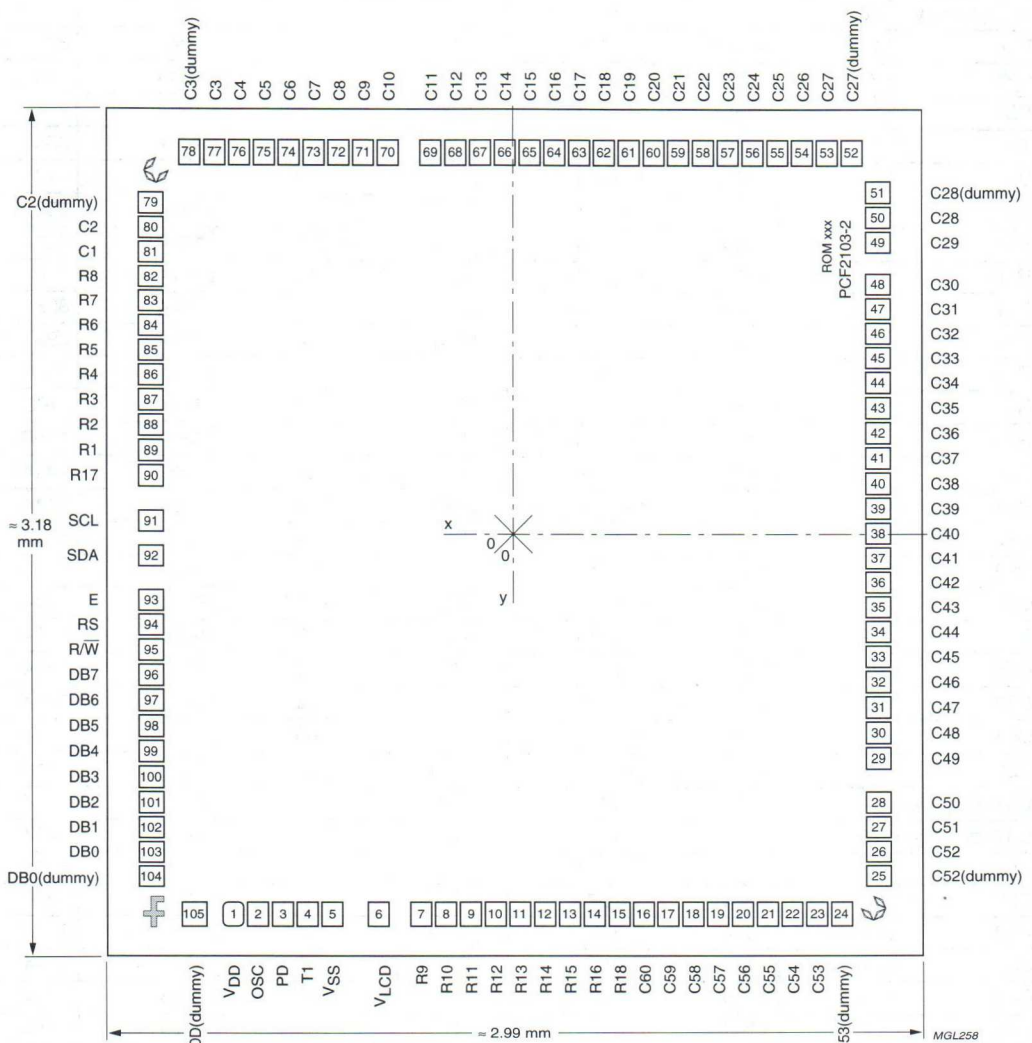


Fig.29 Bonding pad locations.

Table 18 Bonding pad locations (dimensions in μm). All x/y coordinates are referenced to centre of chip (see Fig.29)

SYMBOL	PAD	X	Y
V_{DD} (dummy)	105	−1228	−1414
V_{DD}	1	−1048	−1414
OSC	2	−958	−1414
PD	3	−868	−1414
T1	4	−778	−1414
V_{SS}	5	−688	−1414
V_{LCD}	6	−516	−1414
R9	7	−349	−1414
R10	8	−259	−1414
R11	9	−169	−1414
R12	10	−79	−1414
R13	11	11	−1414
R14	12	101	−1414
R15	13	191	−1414
R16	14	281	−1414
R18	15	371	−1414
C60	16	461	−1414
C59	17	551	−1414
C58	18	641	−1414
C57	19	731	−1414
C56	20	821	−1414
C55	21	911	−1414
C54	22	1001	−1414
C53	23	1091	−1414
C53 (dummy)	24	1181	−1414
C52 (dummy)	25	1344	−1254
C52	26	1344	−1164
C51	27	1344	−1074
C50	28	1344	−948
C49	29	1344	−812
C48	30	1344	−722
C47	31	1344	−632
C46	32	1344	−542
C45	33	1344	−452
C44	34	1344	−362
C43	35	1344	−272
C42	36	1344	−182
C41	37	1344	−92

SYMBOL	PAD	X	Y
C40	38	1344	−2
C39	39	1344	88
C38	40	1344	178
C37	41	1344	268
C36	42	1344	358
C35	43	1344	448
C34	44	1344	538
C33	45	1344	628
C32	46	1344	718
C31	47	1344	808
C30	48	1344	898
C29	49	1344	1070
C28	50	1344	1160
C28 (dummy)	51	1344	1250
C27 (dummy)	52	1262	1414
C27	53	1172	1414
C26	54	1082	1414
C25	55	992	1414
C24	56	902	1414
C23	57	805	1414
C22	58	715	1414
C21	59	625	1414
C20	60	535	1414
C19	61	445	1414
C18	62	355	1414
C17	63	265	1414
C16	64	175	1414
C15	65	85	1414
C14	66	−5	1414
C13	67	−95	1414
C12	68	−185	1414
C11	69	−275	1414
C10	70	−446	1414
C9	71	−536	1414
C8	72	−626	1414
C7	73	−716	1414
C6	74	−806	1414
C5	75	−896	1414

SYMBOL	PAD	X	Y
C4	76	−986	1414
C3	77	−1076	1414
C3 (dummy)	78	−1166	1414
C2 (dummy)	79	−1344	1303
C2	80	−1344	1213
C1	81	−1344	1123
R8	82	−1344	1033
R7	83	−1344	943
R6	84	−1344	853
R5	85	−1344	763
R4	86	−1344	673
R3	87	−1344	583
R2	88	−1344	493
R1	89	−1344	403
R17	90	−1344	313
SCL	91	−1344	131
SDA	92	−1344	−9
E	93	−1344	−195
RS	94	−1344	−289
RW	95	−1344	−382
DB7	96	−1344	−476
DB6	97	−1344	−572
DB5	98	−1344	−668
DB4	99	−1344	−765
DB3	100	−1344	−861
DB2	101	−1344	−957
DB1	102	−1344	−1054
DB0	103	−1344	−1150
DB0 (dummy)	104	−1344	−1240
Rec. Pat. C1		1335	−1405
Rec. Pat. C2		−1335	1405
Rec. Pat. F		−1340	−1397

Table 19 Bump specifications

PARAMETER	SPECIFICATION	UNIT
Bump variant	N	–
Type	galvanic; pure aurum	–
Bump width	60 ±6	µm
Bump length	90 ±6	µm
Bump height	17.5 ±5	µm
Height difference in one die	<2	µm
Convex deformation	<5	µm
Pad size; aluminium	80 × 100	µm
Passivation opening CBB	46 × 76	µm
Wafer thickness	380 ±25	µm
Minimum pitch	90	µm

LCD controllers/drivers PCF2104x

FEATURES

- Single chip LCD controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user-defined symbols
- On-chip:
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption.
- I²C-bus address: 011101 SA0.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

GENERAL DESCRIPTION

The PCF2104x integrated circuit is similar to the PCF2114x (described in the *"PCF2116 family"* data sheet) but does not contain the high voltage generator of that device.

The PCF2104x is optimized for chip-on-glass applications. The 'x' in 'PCF2104x' represents a specific letter code for a character set in the character generator ROM (CGROM).

Two standard character sets are currently available, specified by the letters 'C' and 'L'. Other character sets are available on request.

The PCF2104x is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with a 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages which results in a minimum of external components and lower system power consumption. To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}.

The chip contains a character generator and displays alphanumeric and kana characters. The PCF2104x interfaces to most microcontrollers via a 4 or 8-bit bus, or via the 2-wire I²C-bus.

Packages

- PCF2104xU/2; chip with bumps in tray
- PCF2104xU/7; chip with bumps on tape.

Available types

- PCF2104CU/x: character set 'C' in CGROM
- PCF2104LU/x: character set 'L' in CGROM
- PCF2104NU/x: character set 'N' in CGROM.

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2104CU/2	–	chip with bumps in tray	–
PCF2104CU/7	–	chip with bumps on tape	–
PCF2104LU/2	–	chip with bumps in tray	–
PCF2104LU/7	–	chip with bumps on tape	–
PCF2104NU/2	–	chip with bumps in tray	–
PCF2104NU/7	–	chip with bumps on tape	–

BLOCK DIAGRAM

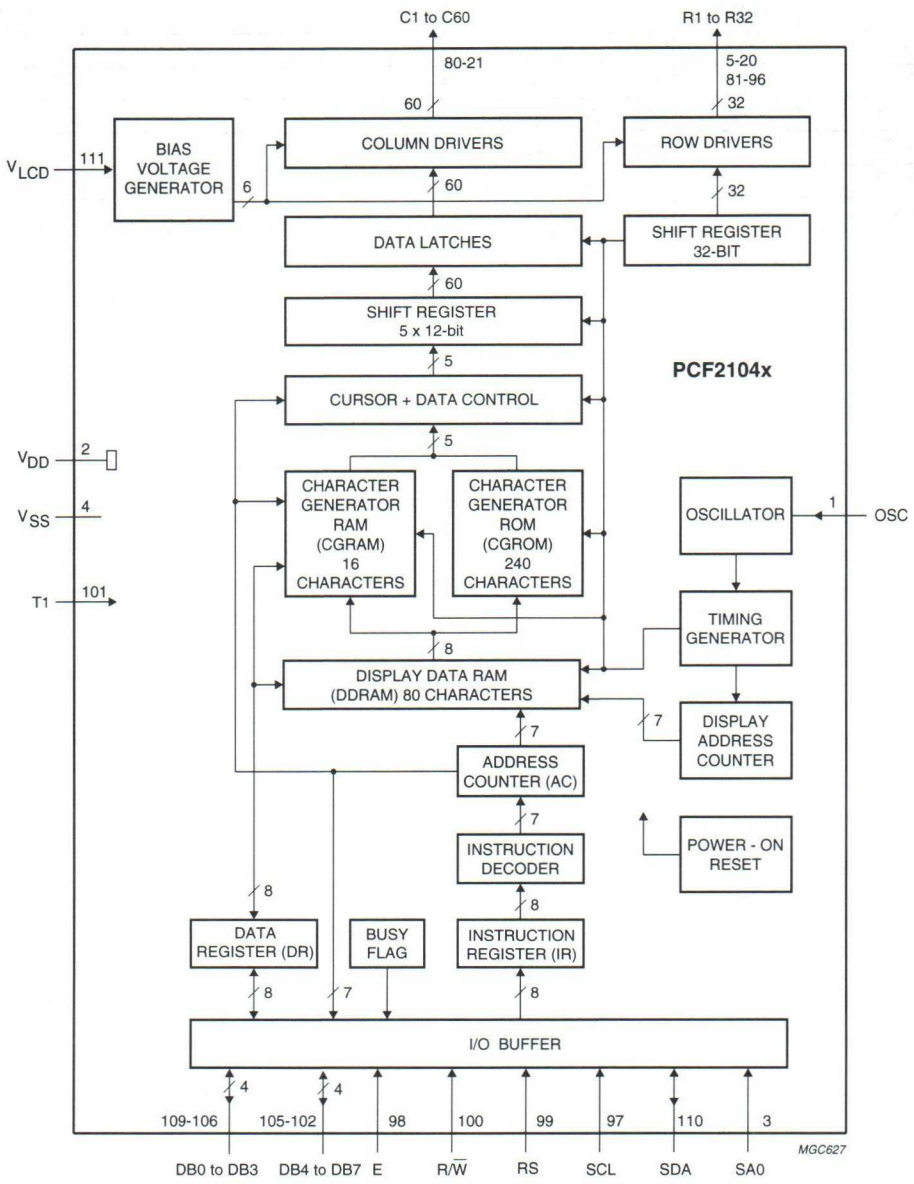


Fig.1 Block diagram.

PINNING

SYMBOL	FFC PAD	TYPE	DESCRIPTION
OSC	1	I	oscillator/external clock input
V_{DD}	2	P	logic supply voltage
SA0	3	I	I^2C-bus address pin input
V_{SS}	4	P	ground
R8 to R5	5 to 8	O	LCD row driver outputs
R32 to R29	9 to12	O	LCD row driver outputs
R24 to R17	13 to 20	O	LCD row driver outputs
C60 to C1	21 to 80	O	LCD column driver outputs
R9 to R16	81 to 88	O	LCD row driver outputs
R25 to R28	89 to 92	O	LCD row driver outputs
R1 to R4	93 to 96	O	LCD row driver outputs
SCL	97	I	I^2C-bus serial clock input
E	98	I	data bus clock input
RS	99	I	register select input
R/$\overline{W}$	100	I	read/write input
T1	101	I	test pad input
DB7 to DB0	102 to 109	I/O	8-bit bidirectional data bus input/output
SDA	110	I/O	I^2C-bus serial data input/output
V_{LCD}	111	I	LCD supply voltage input

LCD controller/driver PCF2105

FEATURES

- Single chip Liquid Crystal Display (LCD) controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4-line display of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user-defined symbols
- On-chip generation of intermediate LCD bias voltages
- On-chip oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface (400 kHz)
- CMOS and TTL compatible
- 32 row, 60 column outputs
- Multiplex (MUX) rates 1 : 32 and 1 : 16
- Uses common 11-code instruction set
- Logic supply voltage range: $V_{DD} - V_{SS}$ = 2.5 to 6 V
- Display supply voltage range: $V_{DD} - V_{LCD}$ = 3.5 to 9 V
- Low power consumption
- I²C-bus address selection (SA0): 011101.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

GENERAL DESCRIPTION

The PCF2105 integrated circuit is similar to the PCF2114x (described in the *"PCF2116 family"* data sheet) but does not contain the high voltage generator of that device. Furthermore, a fast I²C-bus interface (400 kHz) is provided.

The PCF2105 is optimized for chip-on-glass applications.

A specific letter code 'M' for a character set is programmed in the Character Generator ROM (CGROM).

The PCF2105 is a low power CMOS LCD controller/driver, designed to drive a split screen dot matrix LCD of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with a 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages which results in a minimum of external components and lower system power consumption. To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pads does not use a diode connected to V_{DD}.

The chip contains a character generator and displays alphanumeric and kana characters. The PCF2105 interfaces to most microcontrollers via a 4 or 8-bit parallel bus, or via the 2-wire I²C-bus.

Packages

- PCF2105MU/7: chip with bumps on-tape.

Available types

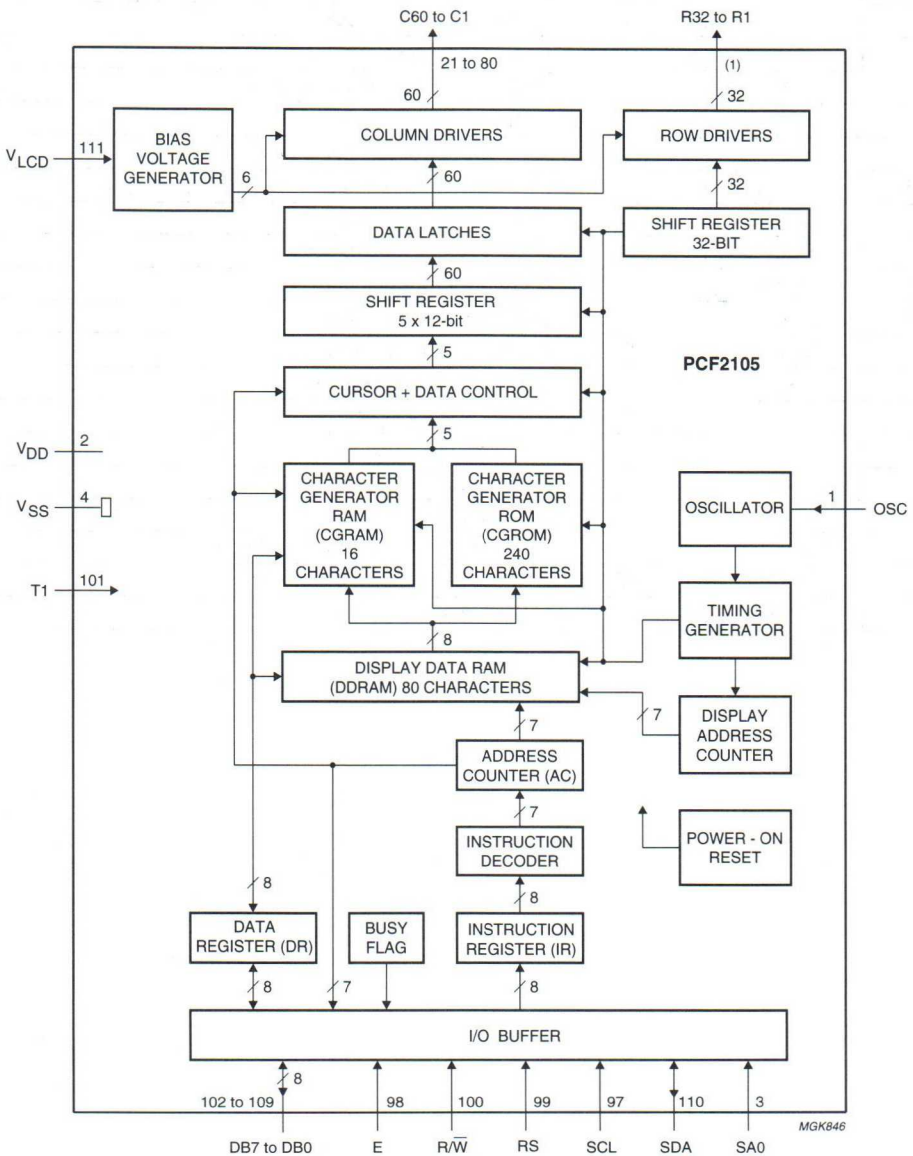
- PCF2105MU/7: character set 'M' in CGROM.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2105MU/7	–	chip with bumps on-tape	–

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM



(1) Pads 5 to 8 and 9 to 12 correspond with symbols R8 to R5 and R32 to R29.
Pads 13 to 20 and 81 to 88 correspond with symbols R24 to R17 and R9 to R16.
Pads 89 to 92 and 93 to 96 correspond with symbols R25 to R28 and R1 to R4.

Fig.1 Block diagram.

PINNING

SYMBOL	PAD	I/O	DESCRIPTION
OSC	1	I	oscillator/external clock input
V_{DD}	2	–	logic supply voltage
SA0	3	I	I²C-bus address selection input
V_{SS}	4	–	logic ground
R8 to R5	5 to 8	O	LCD row driver outputs
R32 to R29	9 to 12	O	LCD row driver outputs
R24 to R17	13 to 20	O	LCD row driver outputs
C60 to C1	21 to 80	O	LCD column driver outputs
R9 to R16	81 to 88	O	LCD row driver outputs
R25 to R28	89 to 92	O	LCD row driver outputs
R1 to R4	93 to 96	O	LCD row driver outputs
SCL	97	I	I²C-bus serial clock input
E	98	I	data bus clock input
RS	99	I	register select input
R/$\overline{W}$	100	I	read/write input
T1	101	I	test input
DB7 to DB0	102 to 109	I/O	8-bit bidirectional data bus input/output
SDA	110	I/O	I²C-bus serial data input/output
V_{LCD}	111	I	LCD supply voltage input

LCD controller/driver PCF2113x

FEATURES

- Single-chip LCD controller/driver
- 2-line display of up to 12 characters + 120 icons, or 1-line display of up to 24 characters + 120 icons
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- Icon mode: reduced current consumption while displaying icons only(1)
- Icon blink function
- On-chip:
  - generation of LCD supply voltage, programmable by instruction (external supply also possible)
  - temperature compensation of on-chip generated V_{LCD}: −8 to −12 mV/K at 5.0 V (programmable by instruction)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240, 5 × 8 characters
- Character generator RAM: 16, 5 × 8 characters; 3 characters used to drive 120 icons, 6 characters used if icon-blink feature is used in application
- 4 or 8-bit parallel bus and 2-wire I²C-bus interface
- CMOS compatible
- 18 row, 60 column outputs
- MUX rates 1 : 18 (for normal operation) and 1 : 2 (for icon-only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage range, $V_{DD} - V_{SS}$ = 1.8 to 4.0 V (up to 5.5 V if external V_{LCD} is used); chip may be driven with two battery cells
- Display supply voltage range, $V_{LCD} - V_{SS}$ = 2.2 to 6.5 V
- Very low current consumption (20 to 200 μA):
  - icon mode: <25 μA
  - power-down mode: <2.5 μA.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

GENERAL DESCRIPTION

The PCF2113x is a low power CMOS LCD controller and driver, designed to drive a dot matrix LCD display of 2 line by 12 and 1 line by 24 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2113x interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus. The chip co cter sets (A, D and E) are currently available. Various other character sets can be manufactured on request.

(1) Icon mode is used to save current. When only icons are displayed, a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}. Never use the voltage generator in icon mode.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2113AU/10/F2	–	chip on flexible film carrier	–
PCF2113DU/10/F2	–	chip on flexible film carrier	–
PCF2113DU/F2	–	chip in tray	–
PCF2113DH/F2	LQFP100	plastic low profile quad flat package; 100 leads; body $14 \times 14 \times 1.4$ mm	SOT407-1
PCF2113EU/2/F2	–	chip with bumps in tray	–

BLOCK DIAGRAM

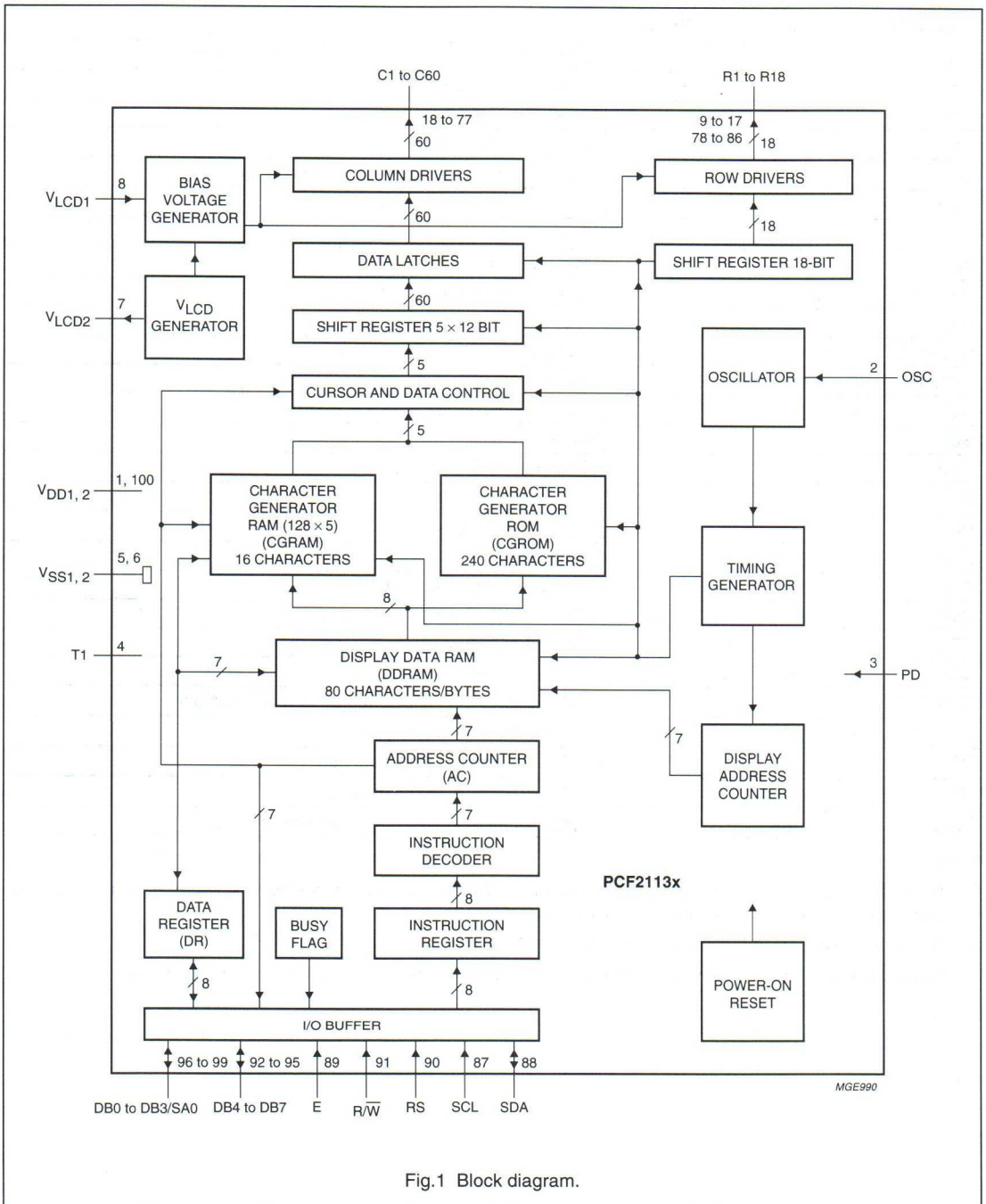


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
V_{DD1}	1	P	supply voltage for all except high voltage generator
OSC	2	I	oscillator/external clock input
PD	3	I	power-down pad input
T1	4	I	test pad (connected to V_{SS})
V_{SS1}	5	P	ground for all except high voltage generator
V_{SS2}	6	P	ground for high voltage generator
V_{LCD2}	7	O	V_{LCD} output; note 1
V_{LCD1}	8	I	V_{LCD} input; note 2
R9 to R16	9 to 16	O	LCD row driver outputs 9 to 16
R18	17	O	LCD row driver output 18
C60 to C1	18 to 77	O	LCD column driver outputs 60 to 1
R8 to R1	78 to 85	O	LCD row driver outputs 8 to 1
R17	86	O	LCD row driver output 17
SCL	87	I	I^2C serial clock input
SDA	88	I/O	I^2C serial data input/output
E	89	I	data bus clock input
RS	90	I	register select input
R/$\overline{W}$	91	I	read/write input
DB7	92	I/O	1 bit of 8-bit bidirectional data bus
DB6	93	I/O	1 bit of 8-bit bidirectional data bus
DB5	94	I/O	1 bit of 8-bit bidirectional data bus
DB4	95	I/O	1 bit of 8-bit bidirectional data bus
DB3/SA0	96	I/O	1 bit of 8-bit bi-directional data bus/I^2C address pin
DB2	97	I/O	1 bit of 8-bit bidirectional data bus
DB1	98	I/O	1 bit of 8-bit bidirectional data bus
DB0	99	I/O	1 bit of 8-bit bidirectional data bus
V_{DD2}	100	P	supply voltage for high voltage generator; note 3

Notes

1. This is the V_{LCD} output pin, if V_{LCD} is generated internally and has to be connected to V_{LCD1}. If V_{LCD1} is generated externally, V_{LCD2} has to be left open or connected to ground.
2. This is the voltage used for the generation of LCD bias levels.
3. This is the supply for the high voltage generator. If V_{LCD} is generated externally, connect V_{DD2} to V_{SS}.

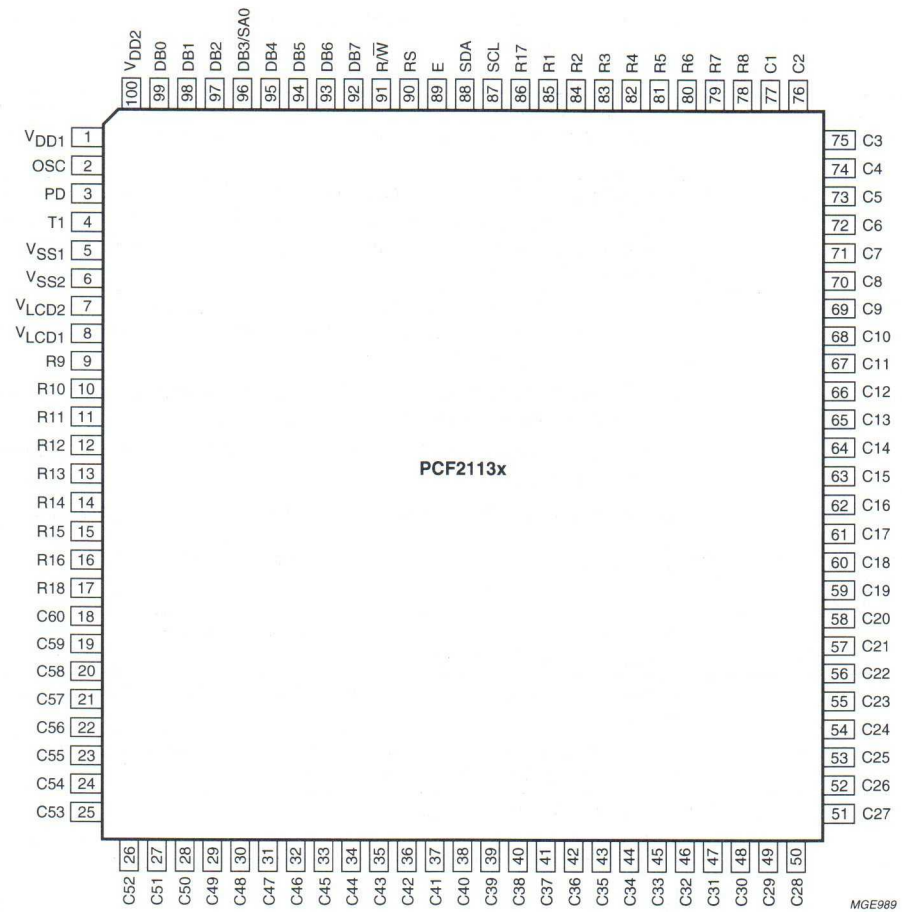


Fig.2 Pin configuration (LQFP100).

PIN FUNCTIONS

NAME	FUNCTION	DESCRIPTION
RS	register select	RS selects the register to be accessed for read and write when the device is controlled by the parallel interface. There is an internal pull-up on this pin. RS = logic 0 selects the instruction register for write and the Busy Flag and Address Counter for read. RS = logic 1 selects the data register for both read and write.
R/$\overline{W}$	read/write	R/$\overline{W}$ selects either the read (R/$\overline{W}$ = logic 1) or write (R/$\overline{W}$ = logic 0) operation when the device is controlled by the parallel interface. There is an internal pull-up on this pin.
E	data bus clock	The E pin is set HIGH to signal the start of a read or write operation when the device is controlled by the parallel interface. Data is clocked in or out of the chip on the negative edge of the clock. Note that this pin must be tied to logic 0 (V_{SS}) when I^2C-bus control is used.
DB7 to DB0	data bus	The parallel interface of the device. This bi-directional, 3-state data bus transfers data between the system controller and the PCF2113x. There is an internal pull-up on each of the data lines. DB7 to DB0 must be connected to V_{DD} or left open circuit when I^2C-bus control is used. Note that DB3 shares the same pin as SA0. In 4-bit operations only DB7 to DB4 are used, and DB3 to DB0 must be left open circuit. See note 1. DB7 may be used as the Busy Flag, signalling that internal operations are not yet completed.
C1 to C60	column driver outputs	These pins output the data for columns.
R1 to R18	row driver outputs	These pins output the row select waveforms to the display. R17 and R18 drive the icons.
V_{LCD}	LCD power supply	Positive power supply for the liquid crystal display. This may be generated on-chip or supplied externally.
OSC	oscillator	When the on-chip oscillator is used this pin must be connected to V_{DD}. An external clock signal, if used, is input at this pin.
SCL	serial clock line	Input for the I^2C-bus clock signal. SCL must be connected to V_{SS} or V_{DD} when the parallel interface is used.
SDA	serial data line	I/O for the I^2C-bus data line. SDA must be connected to V_{SS} or V_{DD} when the parallel interface is used.
SA0	address pin	The hardware sub-address line is used to program the device sub-address for two different PCF2113xs on the same I^2C bus. Note that SA0 shares the same pin as DB3.
T1	test pad	T1 must be connected to V_{SS} and is not user accessible.
PD	power-down pad	PD selects chip power-down mode. For normal operation PD = logic 0.

Note

1. If the 4-bit interface is used without reading out from the PCF2113x (i.e. R/$\overline{W}$ is set permanently to logic 0), the unused ports DB0 to DB3 can either be set to V_{SS} or V_{DD} instead of leaving them open.

LCD controller/drivers PCF2116 family

FEATURES

- Single chip LCD controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- On-chip:
  - generation of LCD supply voltage (external supply also possible)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I²C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption
- I²C-bus address: 011101 SA0.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

GENERAL DESCRIPTION

The PCF2116 family of LCD controller/drivers consists of the PCF2116x, the PCF2114x and the PCF2116K. The term 'PCF2116' is used to refer to all devices for common information. Specific information is given in separate paragraphs.

The 'x' in 'PCF2116x' and 'PCF2114x' represents a specific letter code for a character set in the character generator ROM (CGROM). The different character sets currently available are specified by the letters A, C, and G. Other character sets are available on request.

The PCF2116 is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system power consumption. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters. The PCF2116 interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus. To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}.

The PCF2116K differs from the other members of the family in that:

- V_{LCD}/V_{OP} generation is different
- It is available with character set C only.

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2116xU/10	–	chip on flexible film carrier	–
PCF2114xU/10	–	chip on flexible film carrier	–
PCF2116xU/12	–	chip with bumps on flexible film carrier	–
PCF2114xU/12	–	chip with bumps on flexible film carrier	–
PCF2116xHZ	LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm	SOT425-1

Note

1. The letter 'x' in the type number represents the letter of the required built-in character set: A, C or G.

BLOCK DIAGRAM

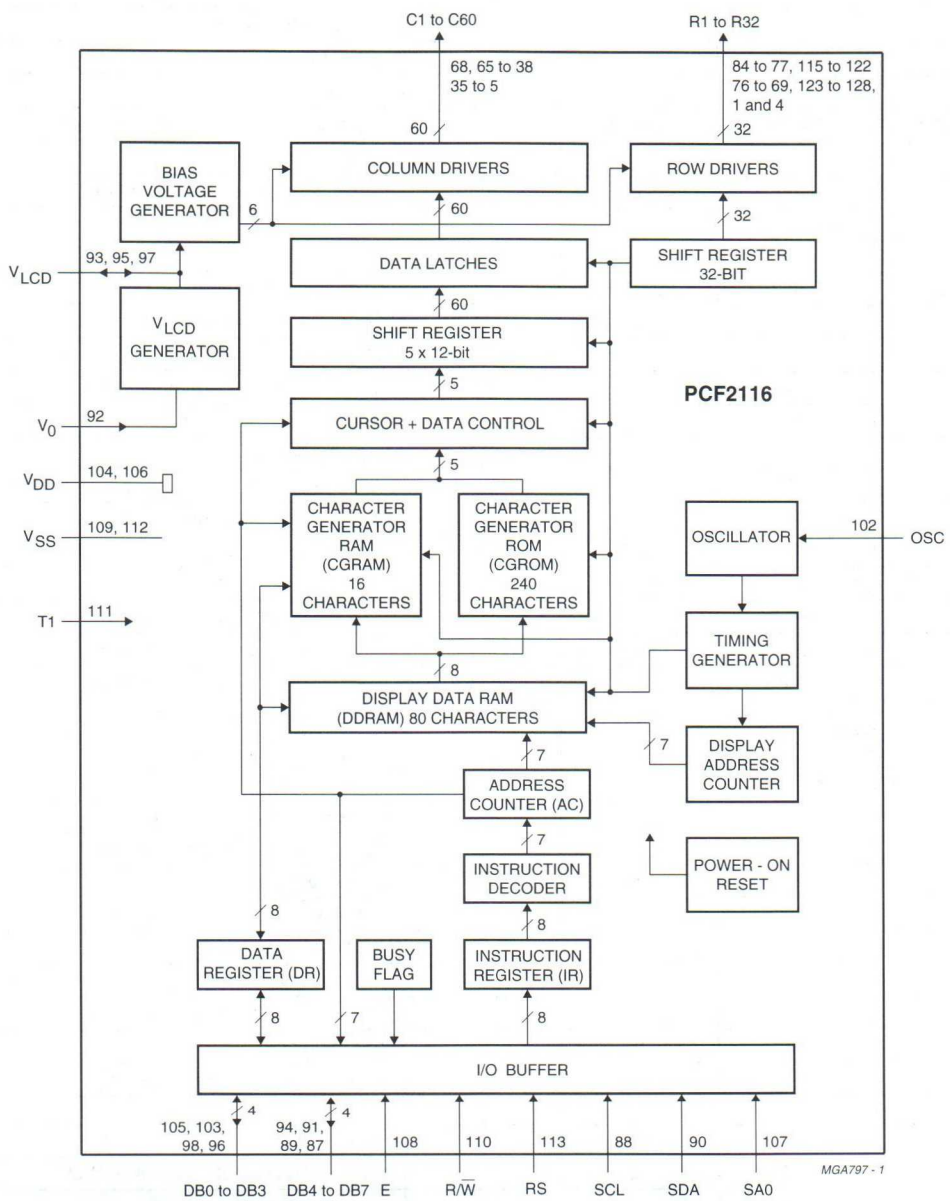


Fig.1 Block diagram (pin numbers for LQFP128 package).

PINNING

SYMBOL	LQFP128	FFC PAD	TYPE	DESCRIPTION
R31	1	27	O	LCD row driver output
n.c.	2 and 3	–	–	not connected
R32	4	28	O	LCD row driver output
C60 to C30	5 to 35	29 to 59	O	LCD column driver outputs 60 to 30
n.c.	36 and 37	–	–	not connected
C29 to C2	38 to 65	60 to 87	O	LCD column driver outputs 29 to 2
n.c.	66 and 67	–	–	not connected
C1	68	88	O	LCD column driver output 1
R24 to R17	69 to 76	89 to 96	O	LCD row driver outputs
R8 to R1	77 to 84	97 to 104	O	LCD row driver outputs
n.c.	85 and 86	–	–	not connected
DB7	87	105	I/O	1 bit of 8-bit bidirectional data bus
SCL	88	106	I	I²C-bus serial clock input
DB6	89	107	I/O	1 bit of 8-bit bidirectional data bus
SDA	90	108	I/O	I²C-bus serial data input/output
DB5	91	109	I/O	1 bit of 8-bit bidirectional data bus
V_0	92	110	I	control input for V_{LCD}
V_{LCD1}	93	111	I/O	LCD supply voltage input/output 1
DB4	94	112	I/O	1 bit of 8-bit bidirectional data bus
V_{LCD2}	95	113	I/O	LCD supply voltage input/output 2
DB3	96	114	I/O	1 bit of 8-bit bidirectional data bus
V_{LCD3}	97	115	I/O	LCD supply voltage input/output 3
DB2	98	116	I/O	1 bit of 8-bit bidirectional data bus
n.c.	99 to 101	–	–	not connected
OSC	102	1	I	oscillator/external clock input
DB1	103	2	I/O	1 bit of 8-bit bidirectional data bus
V_{DD2}	104	3	P	supply voltage 2
DB0	105	4	I/O	1 bit of 8-bit bidirectional data bus
V_{DD1}	106	5	P	supply voltage 1
SA0	107	6	I	I²C-bus address pin
E	108	7	I	data bus clock input (parallel control)
V_{SS1}	109	8	P	ground (logic) 1
R/$\overline{W}$	110	9	I	read/write input (parallel control)
T1	111	10	I	test pad (connect to V_{SS})
V_{SS2}	112	11	P	ground (logic) 2
RS	113	12	I	register select input (parallel control)
n.c.	114	–	–	not connected
R9 to R16	115 to 122	13 to 20	O	LCD row driver outputs
R25 to R30	123 to 128	21 to 26	O	LCD row driver outputs

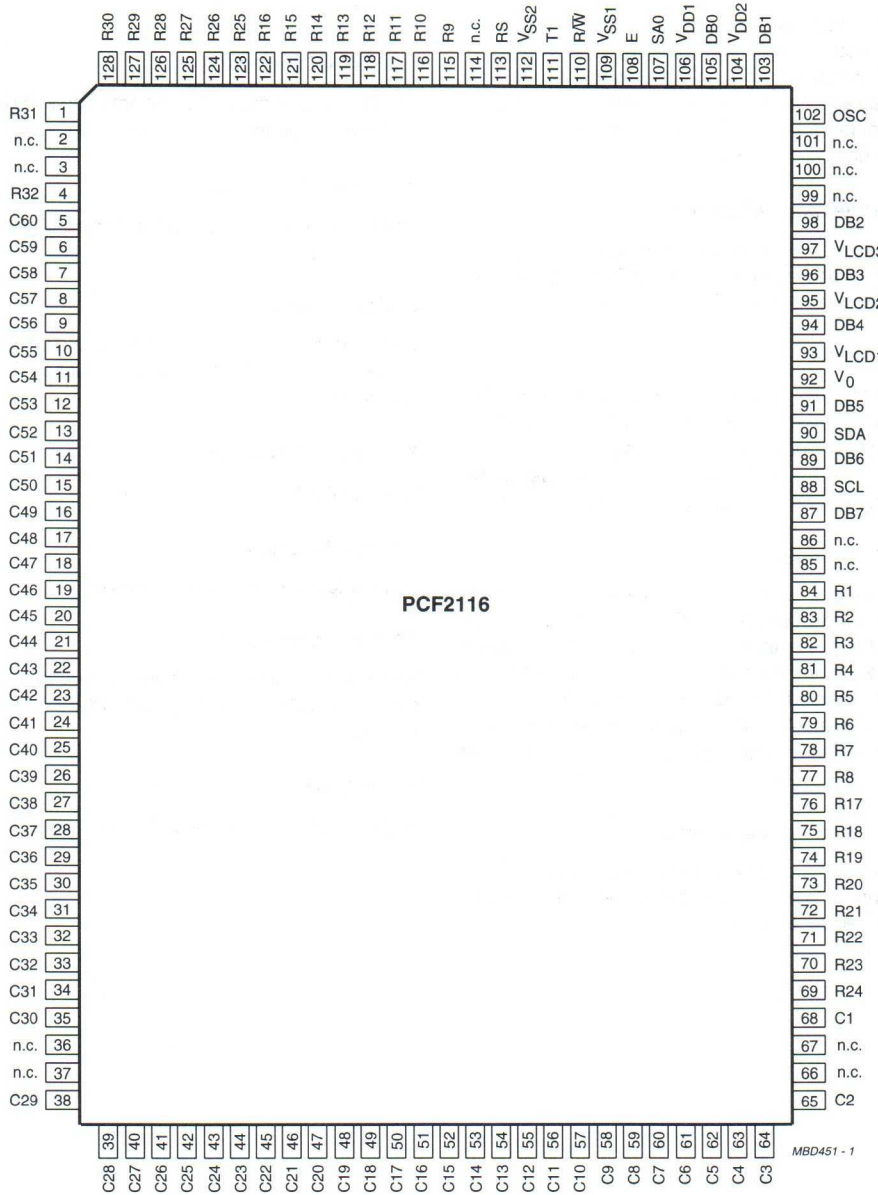


Fig.2 Pin configuration (LQFP128).

PIN FUNCTIONS

RS: register select (parallel control)

RS selects the register to be accessed for read and write when the device is controlled by the parallel interface. RS = logic 0 selects the instruction register for write and the Busy Flag and Address Counter for read. RS = logic 1 selects the data register for both read and write. There is an internal pull-up on pin RS.

R/$\overline{W}$: read/write (parallel control)

R/$\overline{W}$ selects either the read (R/$\overline{W}$ = logic 1) or write (R/$\overline{W}$ = logic 0) operation when control is by the parallel interface. There is an internal pull-up on this pin.

E: data bus clock

The E pin is set HIGH to signal the start of a read or write operation when the device is controlled by the parallel interface. Data is clocked in or out of the chip on the negative edge of the clock. Note that this pin must be tied to logic 0 (V_{SS}) when I^2C-bus control is used.

DB0 to DB7: data bus

The bidirectional, 3-state data bus transfers data between the system controller and the PCF2116. DB7 may be used as the Busy Flag, signalling that internal operations are not yet completed. In 4-bit operations the 4 higher order lines DB4 to DB7 are used; DB0 to DB3 must be left open circuit. There is an internal pull-up on each of the data lines. Note that these pins must be left open circuit when I^2C-bus control is used.

C1 to C60: column driver outputs

These pins output the data for pairs of columns. This arrangement permits optimized chip-on-glass (COG) layout for 4-line by 12 characters.

R1 to R32: row driver outputs

These pins output the row select waveforms to the left and right halves of the display.

V_{LCD}: LCD power supply

Negative power supply for the liquid crystal display. This may be generated on-chip or supplied externally.

V_0: V_{LCD} control input

The input level at this pin determines the generated V_{LCD} output voltage.

OSC: oscillator

When the on-chip oscillator is used this pin must be connected to V_{DD}. An external clock signal, if used, is input at this pin.

SCL: serial clock line

Input for the I^2C-bus clock signal.

SDA: serial data line

Input/output for the I^2C-bus data line.

SA0: address pin

The hardware sub-address line is used to program the device sub-address for 2 different PCF2116s on the same I^2C-bus.

T1: test pad

Must be connected to V_{SS}. Not user accessible.

LCD controllers/drivers PCF2119X

FEATURES

- Single-chip LCD controller/driver
- 2-line display of up to 16 characters + 160 icons, or 1-line display of up to 32 characters + 160 icons
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese) and user defined symbols
- Icon mode: reduced current consumption while displaying icons only
- Icon blink function
- On-chip:
  - generation of LCD supply voltage, independent of V_{DD}, programmable by instruction (external supply also possible)
  - temperature compensation of on-chip generated V_{LCD}: −8 to −12 mV/K at 5.0 V (programmable by instruction)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display Data RAM: 80 characters
- Character Generator ROM: 240, 5 × 8 characters
- Character Generator RAM: 16, 5 × 8 characters; 4 characters used to drive 160 icons, 8 characters used if icon-blink feature is used in application
- 4 or 8-bit parallel bus and 2-wire I²C-bus interface
- CMOS compatible
- 18 row, 80 column outputs
- Multiplex rates 1 : 18 (for normal operation), 1 : 9 (for single line operation) and 1 : 2 (for icon-only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage range, $V_{DD} - V_{SS}$ = 1.5 to 4.0 V (up to 5.5 V if external V_{LCD} is used); chip may be driven with two battery cells
- Display supply voltage range, $V_{LCD} - V_{SS}$ = 2.2 to 6.5 V
- Very low current consumption (20 to 200 μA):
  - icon mode: <25 μA
  - power-down mode: <2 μA
- Power control mode automatically reduces power when $V_{LCD} \approx V_{DD}$.

Note

Icon mode is used to save current. When only icons are displayed, a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

GENERAL DESCRIPTION

The PCF2119x is a low power CMOS LCD controller and driver, designed to drive a dot matrix LCD display of 2-line by 16 and 1-line by 32 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2119x interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I²C-bus. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters. The letter 'x' in PCF2119x characterizes the built-in character set. Various character sets can be manufactured on request.

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PC2119RU/2	–	chip with bumps in tray	–

BLOCK DIAGRAM

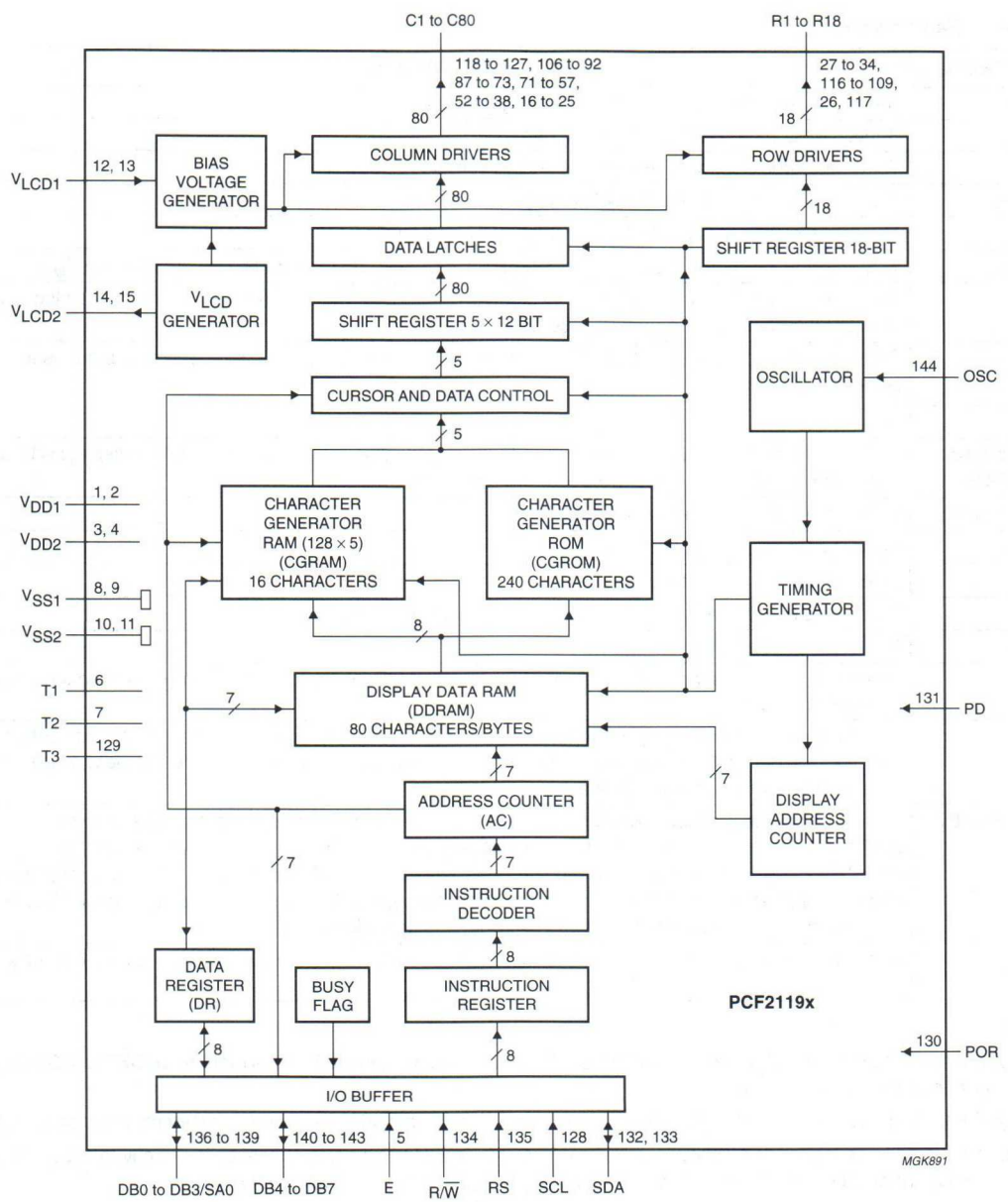


Fig.1 Block diagram.

PAD INFORMATION

Pad functions

Table 1 Pad function description

SYMBOL	DESCRIPTION
V_{DD1}	Supply voltage for all except the high voltage generator.
V_{DD2}	Supply voltage for the high voltage generator.
V_{SS1}	This is the ground pad for all except the high voltage generator.
V_{SS2}	This is the ground pad for the high voltage generator.
V_{LCD1}	This input is used for the generation of the LCD bias levels.
V_{LCD2}	This is the V_{LCD} output pad if V_{LCD} is generated internally. This pad must be connected to V_{LCD1}.
E	The data bus clock input is set HIGH to signal the start of a read or write operation; data is clocked in or out of the chip on the negative edge of the clock; note 1.
T1	These are three test pads. T1 and T2 must be connected to V_{SS1}; T3 is left open and is not user accessible.
T2	
T3	
R1 to R18; R17DUP	LCD row driver outputs R1 to R18; these pins output the row select waveforms to the display; R17 and R18 drive the icons. R17 has two pads R17 and R17DUP.
C1 to C80	LCD column driver outputs C1 to C80.
SCL	I^2C-bus serial clock input; note 1.
POR	External power-on reset input.
PD	PD selects the chip power-down mode; for normal operation PD = 0.
SDA	I^2C-bus serial data input/output; note 1.
R/$\overline{W}$	This is the read/write input. R/$\overline{W}$ selects either the read (R/$\overline{W}$ = 1) or write (R/$\overline{W}$ = 0) operation. This pad has internal pull-up.
RS	The RS input selects the register to be accessed for read and write. RS = 0, selects the instruction register for write and the busy flag and address counter for read. RS = 1, selects the data register for both read and write. This pad has an internal pull-up.
DB0 to DB7	The 8-bit bidirectional data bus (3-state) transfers data between the system controller and the PCF2119x. DB7 may be used as the busy flag, signalling that internal operations are not yet completed. In 4-bit operations the 4 higher order lines DB7 to DB4 are used; DB3 to DB0 must be left open-circuit. Data bus line DB3 has an alternative function (SA0), when selected this is the I^2C-bus address pad. Each data line has its own internal pull-up resistor; note 1.
OSC	Oscillator or external clock input. When the on-chip oscillator is used this pin must be connected to V_{DD1}.

Note

1. When the I^2C-bus is used, the parallel interface pin E must be a logic 0. In the I^2C-bus read mode DB7 to DB0 should be connected to V_{DD1} or left open.
   a) When the parallel bus is used, pins SCL and SDA must be connected to V_{SS1} or V_{DD1}; they must not be left open.
   b) If the 4-bit interface is used without reading out from the PCF2119x (i.e. R/$\overline{W}$ is set permanently to a logic 0), the unused ports DB0 to DB4 can either be set to V_{SS1} or V_{DD1} instead of leaving them open.

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1 FEATURES

- Supply voltage 2.25 to 6.0 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Stand-alone or expanded system
- Power-on reset clear
- LCD segments
  - 40 (PCF2100C)
  - 64 (PCF2111C)
  - 32 (PCF2112C)
- Multiplex rate
  - 1 : 2 (PCF2100C)
  - 1 : 2 (PCF2111C)
  - 1 : 1 (PCF2112C)
- Word length
  - 22 bits (PCF2100C)
  - 34 bits (PCF2111C)
  - 34 bits (PCF2112C).

2 GENERAL DESCRIPTION

The PCF21xxC family are single-chip, silicon gate CMOS LCD driver circuits. A 3-line bus (CBUS) structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

The devices have the same function and performance as those of the PCF21xx family, which they supersede. The maximum operating voltage required is reduced from 6.5 to 6.0 V.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.25	–	6.0	V
I_{DD1}	supply current 1	outputs open; CBUS inactive	–	20	50	µA
I_{DD2}	supply current 2	outputs open; CBUS inactive; T_{amb} = 25 °C	–	20	30	µA
P_O	power dissipation per output		–	–	100	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C
T_{stg}	storage temperature		–65	–	+150	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2100CP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCF2100CT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCF2111CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF2111CT	VSO40	plastic very small outline package; 40 leads	SOT158-1
PCF2112CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF2112CT	VSO40	plastic very small outline package; 40 leads	SOT158-1

5 BLOCK DIAGRAMS

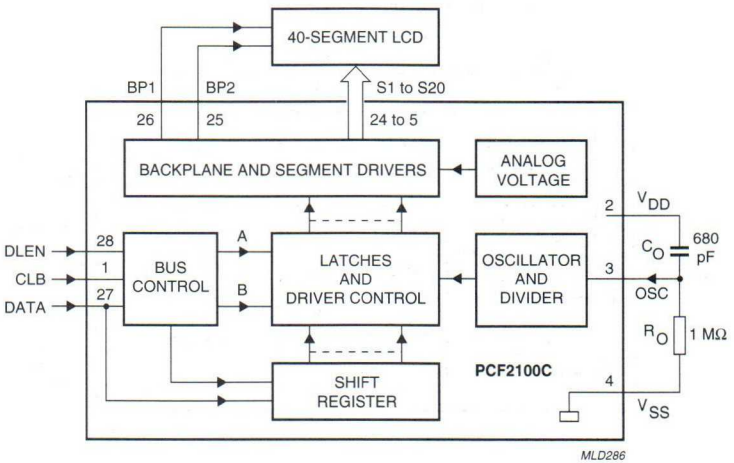


Fig.1 Block diagram; PCF2100C.

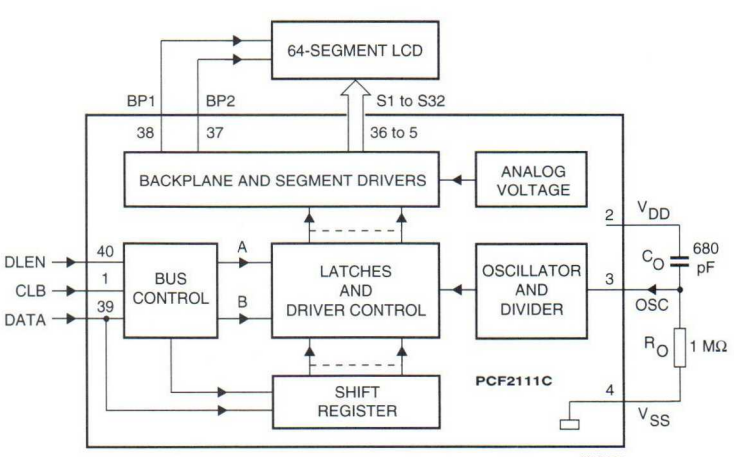


Fig.2 Block diagram; PCF2111C.

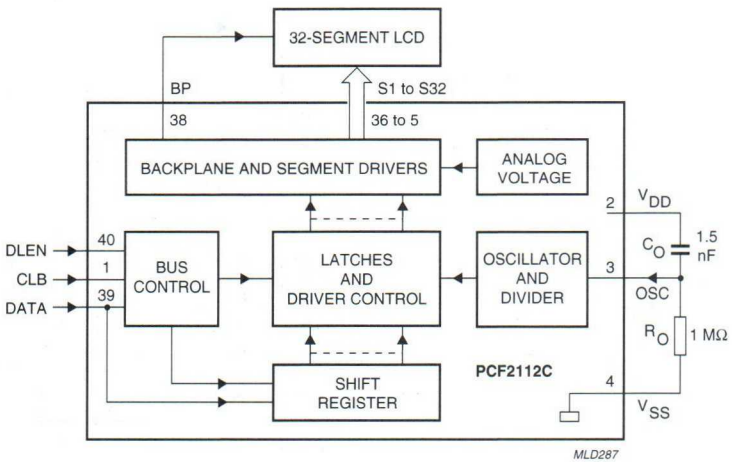


Fig.3 Block diagram; PCF2112C.

6 PINNING

6.1 PCF2100C

SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S20	5	LCD driver output 20
S19	6	LCD driver output 19
S18	7	LCD driver output 18
S17	8	LCD driver output 17
S16	9	LCD driver output 16
S15	10	LCD driver output 15
S14	11	LCD driver output 14
S13	12	LCD driver output 13
S12	13	LCD driver output 12
S11	14	LCD driver output 11
S10	15	LCD driver output 10
S9	16	LCD driver output 9
S8	17	LCD driver output 8
S7	18	LCD driver output 7
S6	19	LCD driver output 6
S5	20	LCD driver output 5
S4	21	LCD driver output 4
S3	22	LCD driver output 3
S2	23	LCD driver output 2
S1	24	LCD driver output 1
BP2	25	backplane driver output 2
BP1	26	backplane driver output 1
DATA	27	data input line (CBUS)
DLEN	28	data input line enable (CBUS)

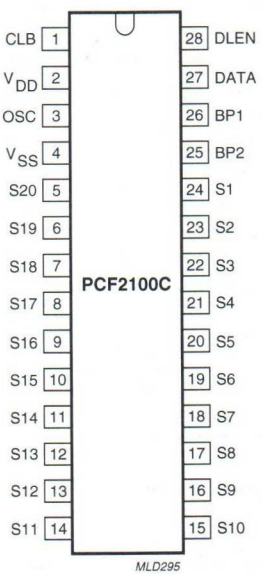


Fig.4 Pin configuration; SOT117-1 and SOT136-1.

6.2 PCF2111C

SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S32	5	LCD driver output 32
S31	6	LCD driver output 31
S30	7	LCD driver output 30
S29	8	LCD driver output 29
S28	9	LCD driver output 28
S27	10	LCD driver output 27
S26	11	LCD driver output 26
S25	12	LCD driver output 25
S24	13	LCD driver output 24
S23	14	LCD driver output 23
S22	15	LCD driver output 22
S21	16	LCD driver output 21
S20	17	LCD driver output 20
S19	18	LCD driver output 19
S18	19	LCD driver output 18
S17	20	LCD driver output 17
S16	21	LCD driver output 16
S15	22	LCD driver output 15
S14	23	LCD driver output 14
S13	24	LCD driver output 13
S12	25	LCD driver output 12
S11	26	LCD driver output 11
S10	27	LCD driver output 10
S9	28	LCD driver output 9
S8	29	LCD driver output 8
S7	30	LCD driver output 7
S6	31	LCD driver output 6
S5	32	LCD driver output 5
S4	33	LCD driver output 4
S3	34	LCD driver output 3
S2	35	LCD driver output 2
S1	36	LCD driver output 1
BP2	37	backplane driver output 2
BP1	38	backplane driver output 1
DATA	39	data input line (CBUS)
DLEN	40	data input line enable (CBUS)

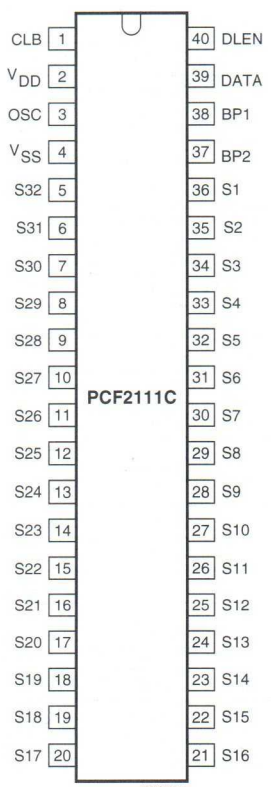


Fig.5 Pin configuration; SOT129-1 and SOT158-1.

6.3 PCF2112C

SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S32	5	LCD driver output 32
S31	6	LCD driver output 31
S30	7	LCD driver output 30
S29	8	LCD driver output 29
S28	9	LCD driver output 28
S27	10	LCD driver output 27
S26	11	LCD driver output 26
S25	12	LCD driver output 25
S24	13	LCD driver output 24
S23	14	LCD driver output 23
S22	15	LCD driver output 22
S21	16	LCD driver output 21
S20	17	LCD driver output 20
S19	18	LCD driver output 19
S18	19	LCD driver output 18
S17	20	LCD driver output 17
S16	21	LCD driver output 16
S15	22	LCD driver output 15
S14	23	LCD driver output 14
S13	24	LCD driver output 13
S12	25	LCD driver output 12
S11	26	LCD driver output 11
S10	27	LCD driver output 10
S9	28	LCD driver output 9
S8	29	LCD driver output 8
S7	30	LCD driver output 7
S6	31	LCD driver output 6
S5	32	LCD driver output 5
S4	33	LCD driver output 4
S3	34	LCD driver output 3
S2	35	LCD driver output 2
S1	36	LCD driver output 1
n.c.	37	not connected
BP	38	backplane driver output
DATA	39	data input line (CBUS)
DLEN	40	data input line enable (CBUS)

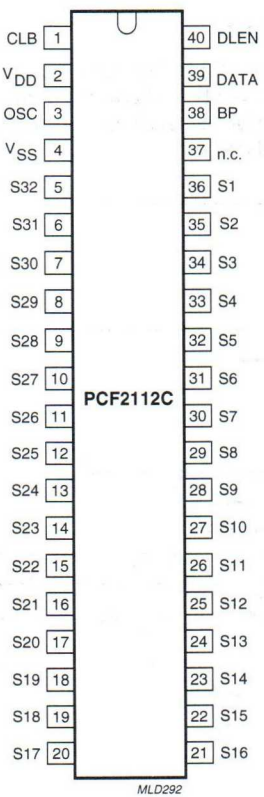


Fig.6 Pin configuration; SOT129-1 and SOT158-1.

7 FUNCTIONAL DESCRIPTION

An LCD segment or LED output is activated when the corresponding DATA bit is HIGH.

7.1 PCF2100C

When DATA bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA bit 21 LOW, the B-latches (BP2) are loaded. CLB pulse 23 transfers data from the shift register to the selected latches.

7.2 PCF2111C

When DATA bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA bit 33 LOW, the B-latches (BP2) are loaded. CLB pulse 35 transfers data from the shift register to the selected latches.

7.3 PCF2112C

When DATA bit 33 is HIGH, the latches are loaded. CLB pulse 35 transfers data from the shift register to the selected latches.

7.4 Bus control logic

The following tests are carried out by the bus control logic:

1. Test on leading zero
2. Test on number of DATA bits
3. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN LOW) and the driver is ready to receive new data.

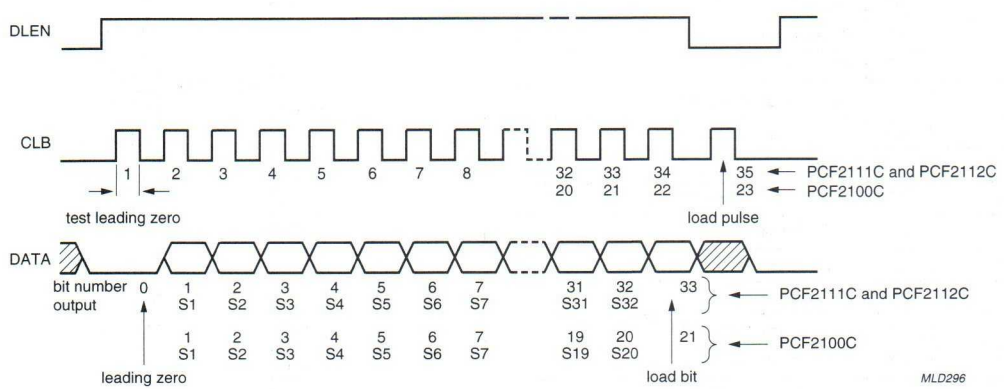


Fig.7 CBUS data format.

7.5 Timing

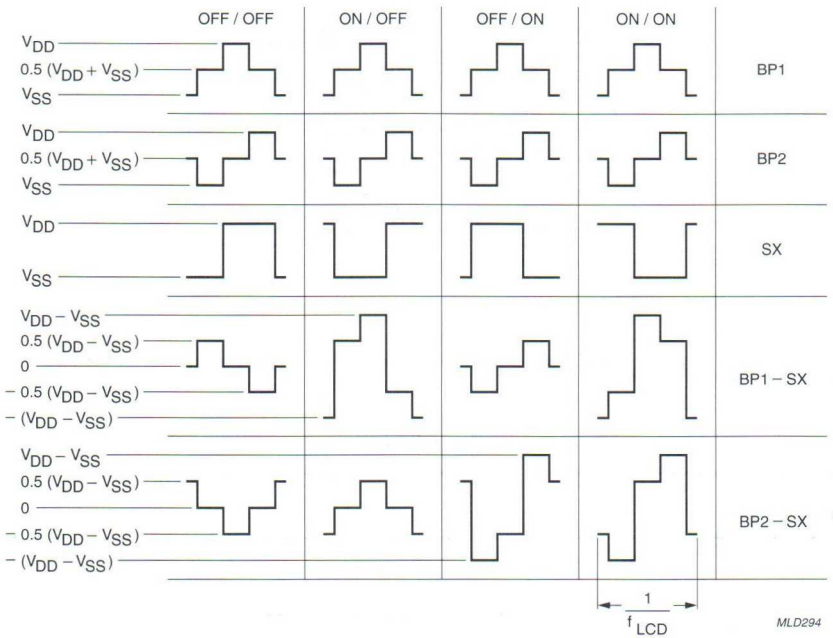


Fig.8 Timing diagram for PCF2100C and PCF2111C.

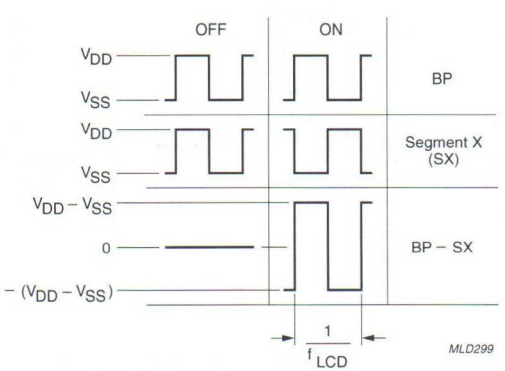
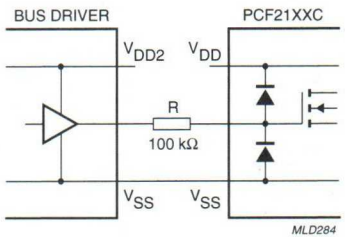


Fig.9 Timing diagram for PCF2112C.

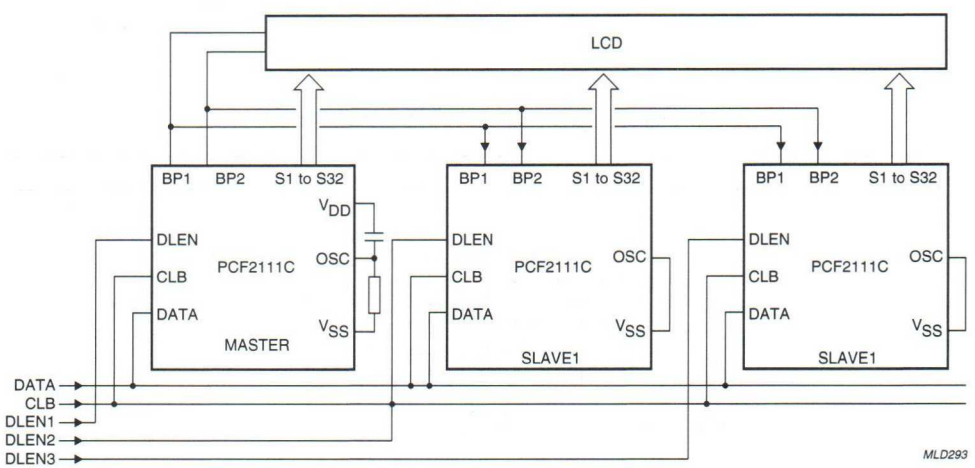
7.6 Input circuitry



V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0.5$ V, a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current ≤40 μA.

Fig.10 Input circuitry.

7.7 Expansion



By connecting OSC to V_{SS} the BP pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several members of the PCF21xxC family up to the BP drive capability of the master. The PCF2112C can only function as a master for other PCF2112Cs.

Fig.11 Expansion possibility (using PCF2111C).

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+8.0	V
V_I	input voltage DLEN, CLB, DATA and OSC		V_{SS} − 0.5	V_{DD} + 0.5	V
V_O	output voltage BP1, BP2 and S1 to S32		V_{SS} − 0.5	V_{DD} + 0.5	V
I_{DD}, I_{SS}	supply current		−50	+50	mA
I_I	DC input current		−20	+20	mA
I_O	DC output current		−25	+25	mA
P_{tot}	total power dissipation per package	note 1	−	500	mW
P_O	power dissipation per output		−	100	mW
T_{stg}	storage temperature		−65	+150	°C

Note

1. Derate by 7.7 mW/K when T_{amb} > 60 °C.

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. See *"Handling MOS devices"*.

ESD in accordance with *"MIL STD 883C, Method 3015"*.

10 DC CHARACTERISTICS

V_{DD} = 2.25 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +80 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.25	–	6.0	V
I_{DD}	supply current	note 1; see Fig.13	–	20	50	µA
		note 1; T_{amb} = 25 °C; see Fig.13	–	20	30	µA
V_{POR}	power-on reset voltage level	note 2	–	1.0	1.6	V
Inputs CLB, DATA and DLEN						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_{LI}	input leakage current	$V_I = V_{SS}$ or V_{DD}	–	–	±1	µA
C_i	input capacitance	note 3	–	–	10	pF
Input OSC						
I_{osc}	oscillator start-up current	$V_I = V_{SS}$	0.5	1.2	5.0	µA
LCD outputs						
V_{BP}	DC voltage of backplane drivers		–	±20	–	mV
$Z_{O(BP)}$	backplane driver output impedance	note 4; V_{DD} = 5 V	–	0.5	5.0	kΩ
$Z_{O(S)}$	segment driver output impedance	note 4; V_{DD} = 5 V	–	1	7	kΩ

Notes

1. Outputs open; CBUS inactive.
2. Resets all logic, when $V_{DD} < V_{POR}$.
3. Periodically sampled (not 100% tested).
4. Outputs measured one at a time.

11 AC CHARACTERISTICS

V_{DD} = 2.25 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +80 °C; R_O = 1 MΩ; C_O = 680 pF; all timing values are referenced to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs CLB, DATA and DLEN (see Fig.12)						
t_{SUDA}	data set-up time		3	–	–	µs
t_{HDDA}	data hold time		3	–	–	µs
t_{SUEN}	enable set-up time		1	–	–	µs
t_{SUDI}	disable set-up time		2	–	–	µs
t_{SULD}	load pulse set-up time		2.5	–	–	µs
t_{BUSY}	busy time		3	–	–	µs
t_{WH}	CLB HIGH time		1	–	–	µs
t_{WL}	CLB LOW time		5	–	–	µs
t_{CLB}	CLB cycle time		10	–	–	µs
t_r	rise time		–	–	10	µs
t_f	fall time		–	–	10	µs
LCD timing (see Figs. 12, 14, 15, 16 and 17)						
f_{LCD}	LCD frame frequency					
	PCF2100C, PCF2111C		60	75	100	Hz
	PCF2112C	C_O = 1.5 nF	30	35	50	Hz
t_{BS}	transfer time with test loads	V_{DD} = 5 V	–	20	100	µs
t_{PLCD}	driver delay time with test loads	V_{DD} = 5 V	–	20	100	µs

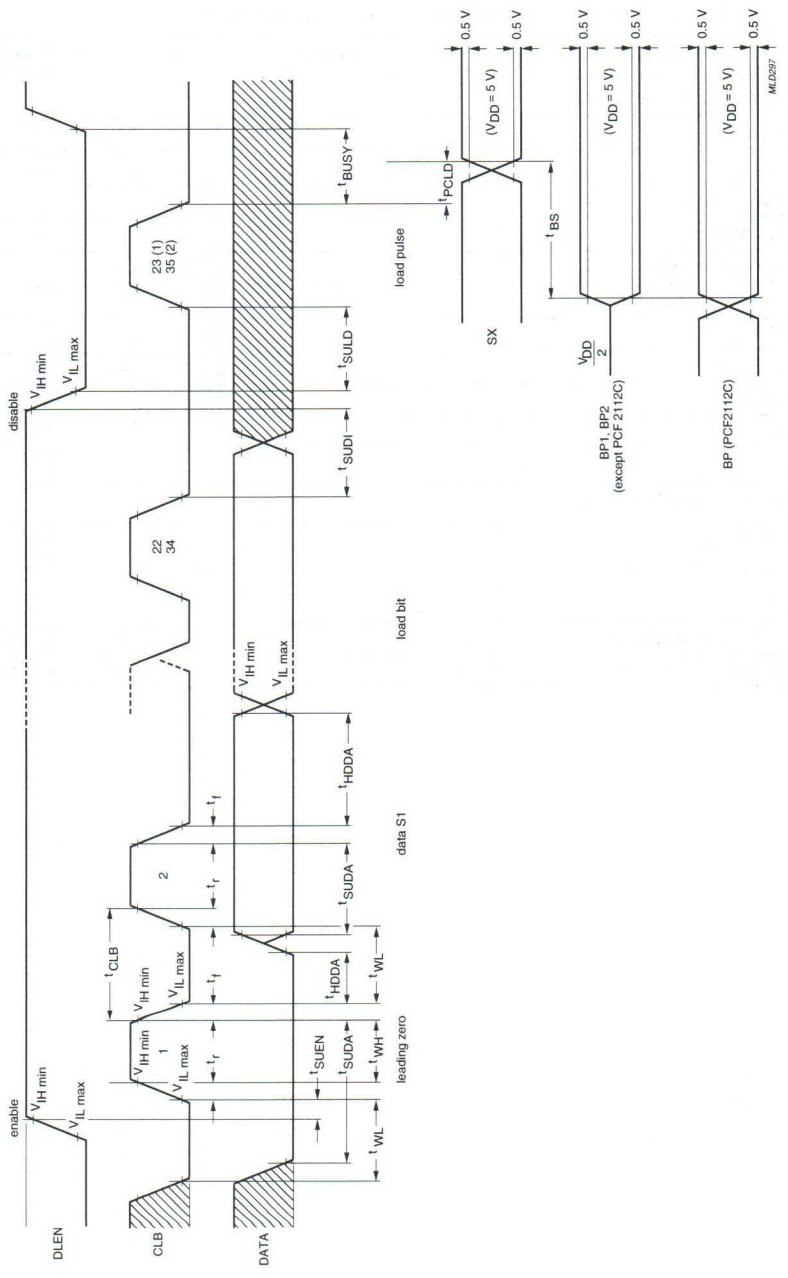
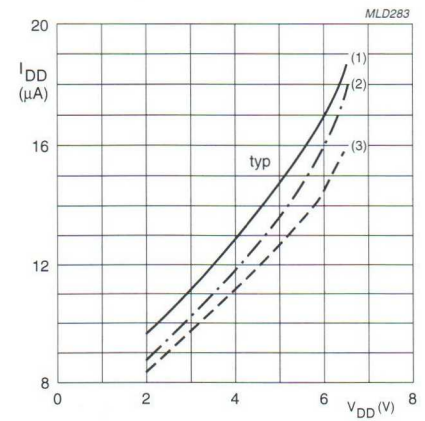


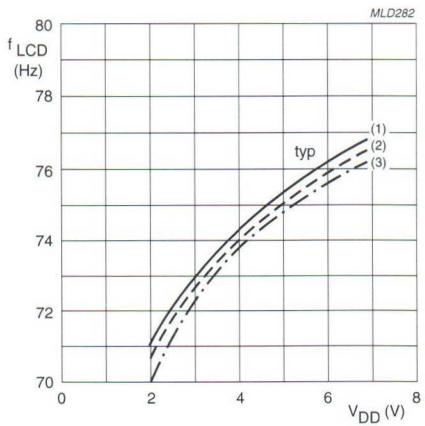
Fig.12 CBUS timing.

(1) Load pulse 23 for PCF2100C (see Fig.7).
(2) Load pulse 35 for PCF2111C and PCF2112C (see Fig.7).



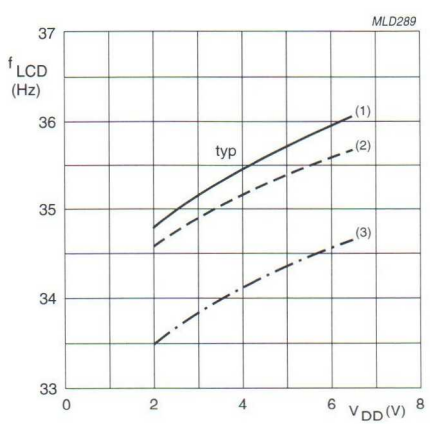
(1) T_{amb} = −40 °C.
(2) T_{amb} = +85 °C.
(3) T_{amb} = +25 °C.

Fig.13 Supply current as a function of supply voltage.



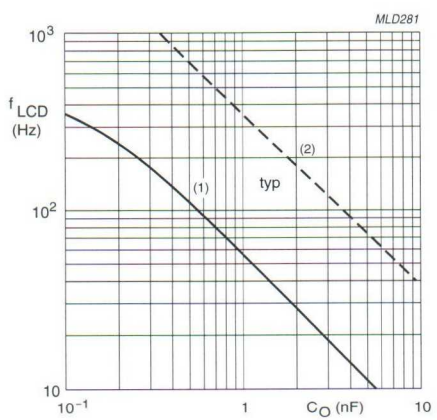
(1) T_{amb} = −40 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.14 Display frequency as a function of supply voltage; C_O = 680 pF (except PCF2112C).



(1) T_{amb} = −40 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.15 Display frequency as a function of supply voltage; C_O = 1.5 nF (only PCF2112C).



(1) R_O = 1 MΩ.
(2) R_O = 100 kΩ.

Fig.16 Display frequency as a function of R_O and C_O; T_{amb} = 25 °C; V_{DD} = 5 V.

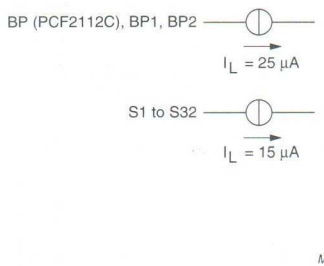
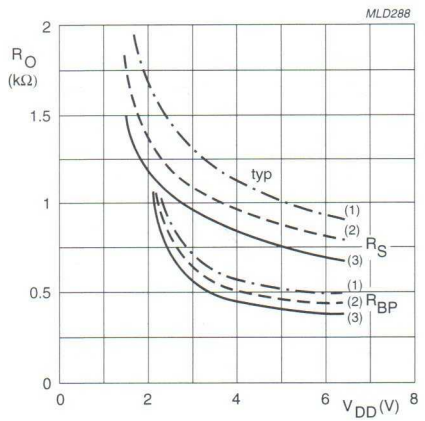
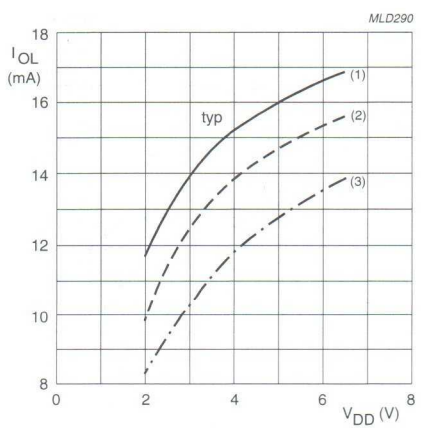


Fig.17 Test loads.



(1) T_{amb} = +85 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = −40 °C.

Fig.18 Output resistance of backplane and segments.



(1) T_{amb} = −40 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.19 LOW level output current as a function of supply voltage (only PCF2112C).

65 × 102 pixels matrix LCD driver PCF8549

FEATURES

- Single chip LCD controller/driver
- 65 row and 102 column outputs
- Display data RAM 65 × 102 bits
- On-chip:
  - Generation of LCD supply voltage
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- 400 kHz Fast I²C Interface
- CMOS compatible inputs
- Mux rate: 65
- Logic supply voltage range $V_{DD1} - V_{SS}$: 1.5 to 6 V
- Voltage generator voltage range $V_{DD2/2_HV} - V_{SS}$: 2.4 to 5 V
- Display supply voltage range $V_{LCD} - V_{SS}$: 7.0 to 16 V
- Low power consumption, suitable for battery operated systems
- Temperature compensation of V_{LCD}
- Interlacing for better display quality
- Slim chip layout, suited for chip-on-glass applications.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

GENERAL DESCRIPTION

The PCF8549 is a low power CMOS LCD controller driver, designed to drive a graphic display of 65 rows and 102 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption. The PCF8549 interfaces to most microcontrollers via an I²C interface.

Packages

The PCF8549U/2 is available as bumped die. Sawn wafer as chip sorted in chip tray.

Customized TCP upon request.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8549U/2/F1	TRAY	chip with bumps in tray	

BLOCK DIAGRAM

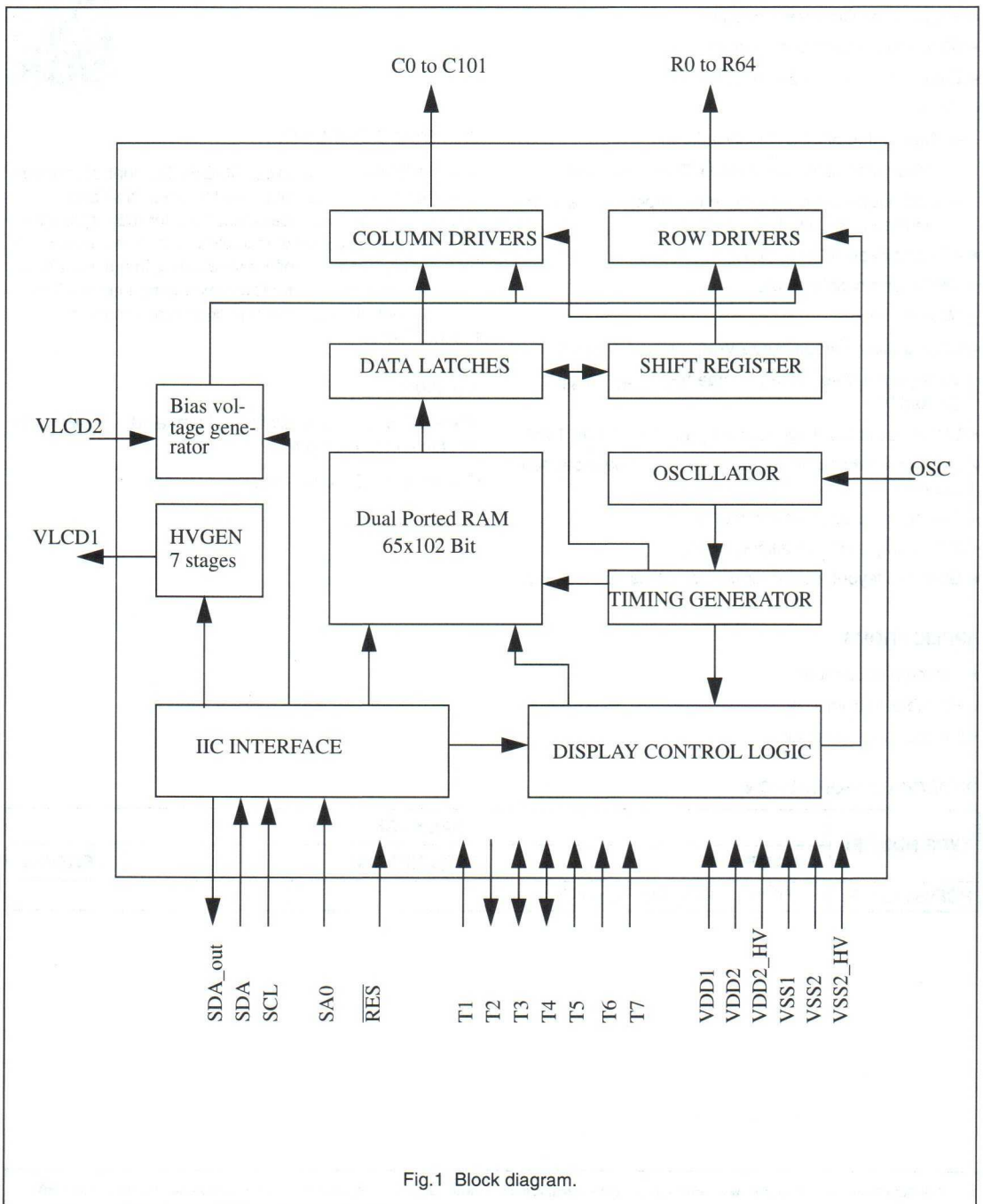


Fig.1 Block diagram.

PINNING

SYMBOL	DESCRIPTION
R0 to R64	LCD row driver outputs
C0 to C101	LCD column driver outputs
$V_{SS1,2,2_HV}$	negative power supply
$V_{DD1,2,2_HV}$	supply voltage
$V_{LCD1,2}$	LCD supply voltage
T1	test 1 input
T2	test 2 output
T3	test 3 I/O
T4	test 4 I/O
T5	test 5 input
T6	test 6 input
T7	test 7 input
SDA	I^2C data input
SCL	I^2C clock line
SDA_OUT	I^2C output
SA0	least significant bit of slave address
OSC	oscillator
$\overline{RES}$	external reset input, low active

Pin functions

R0 TO R64: ROW DRIVER OUTPUTS

These pads output the row signals.

C0 TO C101: COLUMN DRIVER OUTPUTS

These pads output the column signals.

$V_{SS1,2,2_HV}$: NEGATIVE POWER SUPPLY RAILS

Negative power supplies.

$V_{DD1,2,2_HV}$: POSITIVE POWER SUPPLY RAILS

V_{DD2} and V_{DD2_HV} are the supply voltages for the internal voltage generator. Both have to be on the same voltage and may be connected together outside of the chip. If the internal voltage generator is not used, they should be both connected to ground. V_{DD1} is used as power supply for the rest of the chip. This voltage can be a different voltage than V_{DD2} and V_{DD2_HV}.

$V_{LCD1,2}$: LCD POWER SUPPLY

Positive power supply for the liquid crystal display. If the internal voltage generator is used, the two supply rails V_{LCD1} and V_{LCD2} must be connected together. An external LCD supply voltage can be supplied using the V pad. In this case, V_{LCD1} has to be connected to ground, and the internal voltage generator has to be programmed to zero. If the PCF8549 is in power-down mode, the external LCD supply voltage has to be switched off.

T1, T2, T3, T4, T5, T6 AND T7: TEST PADS

T1, T3, T4, T5, T6 and T7 must be connected to V_{SS1}, T2 is to be left open. Not accessible to user.

SDA/SDA_OUT: I^2C DATA LINES

Output and input are separated. If both pads are connected together they behave like a standard I^2C pad.

SCL: I^2C CLOCK SIGNAL

Input for the I^2C-bus clock signal.

SA0: SLAVE ADDRESS

With the SA0 pin two different slave addresses can be selected. That allows to connect two PCF8549 LCD drivers to the same I^2C-bus.

OSC: OSCILLATOR

When the on-chip oscillator is used this input must be connected to V_{DD1}. An external clock signal, if used, is connected to this input.

$\overline{RES}$: RESET

This signal will reset the device. Signal is active low.

Universal LCD driver for small graphic panels

PCF8558

FEATURES

- Single-chip LCD controller/driver
- 40 row and 101 column outputs
- Display data RAM
  40 × 101 bits = 505 bytes = 4040 bits
- On-chip:
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- 400 kHz fast I²C-bus interface
- CMOS compatible
- MUX rate 1 : 40
- Logic supply voltage range $V_{DD} - V_{SS}$ = 2.5 to 6 V
- Display supply voltage range $V_{DD} - V_{LCD}$ = 3.5 to 9 V
- Low power consumption, suitable for battery operated systems.

GENERAL DESCRIPTION

The PCF8558 is a low power CMOS LCD controller driver, designed to drive a graphic display of 40 rows and 101 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower power consumption.

The PCF8558 interfaces to most microcontrollers via a I²C-bus interface.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals
- Alarm systems.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8558U/10	–	chip on FFC	–
PCF8558U/12	–	chip with bumps on FFC	–

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM

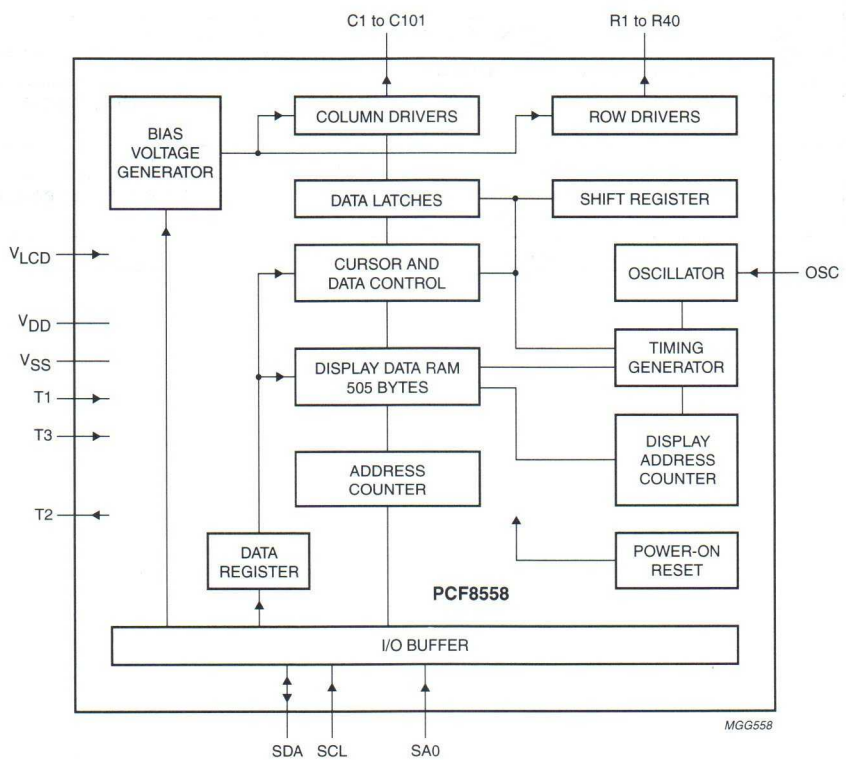


Fig.1 Block diagram.

PINNING

SYMBOL	PAD	DESCRIPTION
SCL	1	I^2C-bus serial clock input
R20 to R1	2 to 21	LCD row driver data outputs
C101 to C1	22 to 122	LCD column driver data outputs
R21 to R40	123 to 142	LCD row driver data outputs
T2	143	test pad output, must be left unconnected (not user accessible)
SDA	144	I^2C-bus serial data input/output
V_{SS}	145	ground
T1	146	test pad input, must be connected to V_{SS} (not user accessible)
V_{LCD}	147	negative supply voltage input
SA0	148	the LSB bit of the I^2C-bus slave address input is set by connecting this pin to either 0 (V_{SS}) or 1 (V_{DD})
T3	149	test pad input, must be connected to V_{DD} (not user accessible)
OSC	150	when the on-chip oscillator is used this pin must be connected to V_{DD}; an external clock signal, if used, is input at this pin
V_{DD}	151	positive supply voltage

Real-time clock/calendar PCF8563

FEATURES

- Provides year, month, day, weekday, hours, minutes, seconds based on 32.768 kHz quartz crystal
- Century flag
- Wide clock operating voltage: 1.0 - 5.5 V
- Low back-up current typical 0.25 µA @ 3.0 V, 25 °C
- 400 kHz two-wire I²C interface (1.8 - 5.5 V)
- Programmable clock output for peripheral devices (32.768 kHz, 1024 Hz, 32 Hz, 1 Hz)
- Alarm and timer functions
- Low-voltage detector
- Integrated oscillator capacitor
- Internal power-on reset
- I²C slave address: read A3h, write A2h
- Open drain interrupt pin.

GENERAL DESCRIPTION

The PCF8563 is a CMOS real-time clock/calendar optimized for low power consumption. A programmable clock output, interrupt output and voltage low detector are also provided. All address and data are transferred serially via a two-line bidirectional I²C bus. Maximum bus speed is 400 kbit/sec. The built-in word address register is incremented automatically after each written or read data byte.

APPLICATIONS

- Mobile telephones
- Portable instruments
- Fax machines
- Battery powered products.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	Supply voltage operating mode	I²C bus active –40 to +85 °C	1.8	5.5	V
		Clock operating, 25 °C	1.0	5.5	V
I_{DD}	Supply current (Timer and CLKOUT disabled)	f_{SCL} = 100 kHz	–	200	µA
		f_{SCL} = 400 kHz	–	800	µA
		f_{SCL} = 0 Hz: V_{DD} = 5 V, 25 °C	–	1.0	µA
		f_{SCL} = 0 Hz: V_{DD} = 2 V, 25 °C	–	0.75	µA
T_{AMB}	Operating ambient temperature		–40	+85	°C
T_{STG}	Storage temperature		–55	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8563P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8563T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

BLOCK DIAGRAM

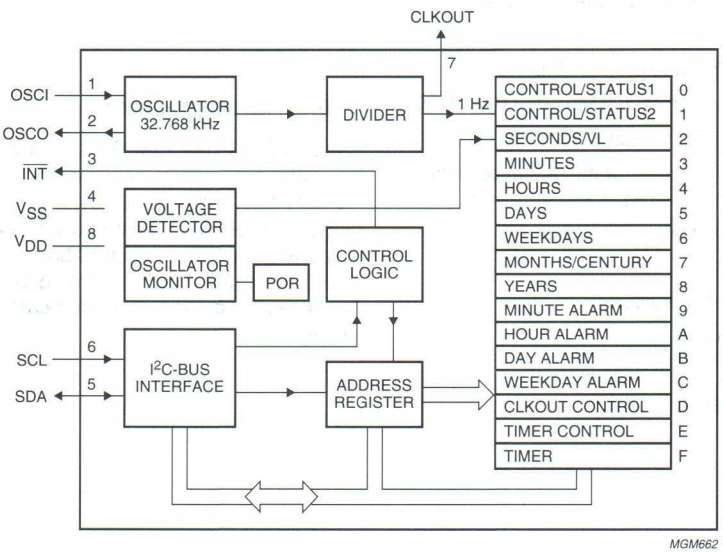


Fig.1 Block diagram PCF8563 real-time clock/calendar.

PINNING INFORMATION

Pin description

SYMBOL	PIN	DESCRIPTION
OSCI	1	Oscillator input
OSCO	2	Oscillator output
$\overline{INT}$	3	Open drain interrupt output (active LOW)
V_{SS}	4	Ground
SDA	5	Serial data I/O
SCL	6	Serial clock input
CLKOUT	7	Clock output
V_{DD}	8	Positive supply

Pinning

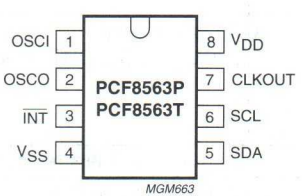


Fig.2 Pinning.

FUNCTIONAL DESCRIPTION

The PCF8563 contains sixteen 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with one integrated capacitor, a frequency divider which provides the source clock for the real time clock (RTC), a programmable clock output, a timer, an alarm, a voltage-low detector and a 400 kHz I^2C bus interface.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00, 01) are used as control and/or status registers. The memory addresses 02 through 08 are used as counters for the clock function (seconds up to year counters). Address locations 09 through 0C contain alarm registers which define the conditions for an alarm. Address 0D controls the CLKOUT output frequency. 0E and 0F are the timer control and timer registers, respectively.

The seconds, minutes, hours, days, weekdays, months, years as well as the minute alarm, hour alarm, day alarm and weekday alarm registers are all coded in BCD format.

When one of the RTC registers is read the contents of all counters are frozen. Therefore, faulty reading of the clock/calendar during a carry condition is prevented.

Alarm function modes

By clearing the MSB of one or more of the alarm registers (AE = 'Alarm Enable'), the corresponding alarm condition(s) will be active. In this way an alarm can be generated from once per minute up to once per week. The alarm condition sets the alarm flag, AF. The asserted AF can be used to generate an interrupt ($\overline{INT}$). The AF may only be cleared by software.

Timer

The 8-bit countdown timer at address 0F is controlled by the timer control register at address 0E. The timer control register determines one of 4 source clock frequencies for the timer (4096 Hz, 64 Hz, 1 Hz, or $1/_{60}$ Hz), and enables/disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the timer flag TF. The TF may only be cleared by software. The asserted TF can be used to generate an interrupt ($\overline{INT}$). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of TF. TI/TP is used to control this mode selection. When reading the timer, the current countdown value is returned.

CLKOUT output

A programmable square wave is available at the CLKOUT pin. Operation is controlled by the CLKOUT register at address 0D. Frequencies of 32.768 kHz (default), 1024 Hz, 32 Hz and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator. CLKOUT is a push-pull output and enabled at power on. If disabled it becomes logic 0.

Reset

The PCF8563 includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I^2C bus logic is initialized and all registers, including the address pointer, are cleared with the exception of bits FE, VL, TD1, TD0, TESTC and AE bits which are set to 1.

Voltage low detector & clock monitor

The PCF8563 has an on-chip voltage low detector. When V_{DD} drops below V_{LOW} the 'Voltage Low' (VL, bit 7 in the seconds register) is set to indicate that the integrity of the clock information is no longer guaranteed. The VL flag can only be cleared by software.

Register organization

Bit positions labelled as 'x' are not implemented, those labelled with '0' should always be written with 0.

ADDRESS	FUNCTION	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00	Control/status 1	TEST1	0	STOP	0	TESTC	0	0	0
01	Control/status 2	0	0	0	TI/TP	AF	TF	AIE	TIE
02	Seconds	VL	4	2	1	8	4	2	1
03	Minutes	x	4	2	1	8	4	2	1
04	Hours	x	x	2	1	8	4	2	1
05	Days	x	x	2	1	8	4	2	1
06	Weekdays	x	x	x	x	x	4	2	1
07	Months/Century	C	x	x	1	8	4	2	1
08	Years	8	4	2	1	8	4	2	1
09	Minute alarm	AE	4	2	1	8	4	2	1
0A	Hour alarm	AE	x	2	1	8	4	2	1
0B	Day alarm	AE	x	2	1	8	4	2	1
0C	Weekday alarm	AE	x	x	x	x	4	2	1
0D	CLKOUT frequency	FE	x	x	x	x	x	FD1	FD0
0E	Timer control	TE	x	x	x	x	x	TD1	TD0
0F	Timer	128	64	32	16	8	4	2	1

Bit assignments

BIT NO.	BIT NAME	BIT VALUE	DESCRIPTION
Control/Status 1		**Address 00**	
3	TESTC	0	Power on reset override facility is disabled. Set to 0 for normal operation.
		1	Power on reset override may be enabled.
5	STOP	0	RTC source clock runs.
		1	All RTC divider chain flip flops are asynchronously set to 0; the RTC clock is stopped (CLKOUT at 32.768 kHz is still available)
7	TEST1	0	Normal mode.
		1	EXT_CLK test mode.
Control/Status 2		**Address 01**	
TIE & AIE		These bits activate or deactivate the generation of an interrupt when TF or AF is asserted, respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set	
0	TIE	0	Timer interrupt disabled
		1	Timer interrupt enabled
1	AIE	0	Alarm interrupt disabled
		1	Alarm interrupt enabled

BIT NO.	BIT NAME	BIT VALUE	DESCRIPTION
TF & AF		When an alarm occurs, AF is set to 1. Similarly, at the end of a timer countdown, TF is set to 1.These bits maintain their value until overwritten by software. If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another a logic AND is performed during a write access.	
2	TF	0 (READ)	Timer flag inactive.
		1 (READ)	Timer flag active.
		0 (WRITE)	Timer flag is cleared.
		1 (WRITE)	Timer flag remains unchanged.
3	AF	0 (READ)	Alarm flag inactive.
		1 (READ)	Alarm flag active.
		0 (WRITE)	Alarm flag is cleared.
		1 (WRITE)	Alarm flag remains unchanged.
4	TI/TP	0	$\overline{INT}$ is active when TF is active (subject to the status of TIE).
		1	$\overline{INT}$ pulses active according to table 1(subject to the status of TIE). Note that if AF and AIE are active then $\overline{INT}$ will be permanently active.
Seconds & VL		**Address 02**	
6..0	Seconds	00 - 59	This register holds the current seconds coded in BCD format. Example: seconds register contains 'x1011001' = 59 seconds.
7	VL	0	Clock integrity is guaranteed.
		1	Integrity of the clock information is no longer guaranteed.
Minutes		**Address 03**	
6..0	Minutes	00 - 59	This register holds the current minutes coded in BCD format.
Hours		**Address 04**	
5..0	Hours	00 - 23	This register holds the current hours coded in BCD format.
Days		**Address 05**	
5..0	Days[1]	01 - 31	This register holds the current day coded in BCD format.
Weekdays		**Address 06**	
2..0	Weekdays[2]	0 - 6	This register holds the current weekday coded in BCD format, see table 4.
Months & Century		**Address 07**	
4..0	Month	01 - 12	This register holds the current month coded in BCD format, see table 5.
7	Century[2]	0	Indicates the century is 20xx.
		1	Indicates the century is 19xx.
		This bit is toggled when the years register overflows from 99 to 00.	
Years		**Address 08**	
7..0	Years	00 - 99	This register holds the current year coded in BCD format.

BIT NO.	BIT NAME	BIT VALUE	DESCRIPTION
Alarm registers		**Address 09 to 0C**	
		When one or more of these registers is loaded with a valid minute, hour, day or weekday and its corresponding 'Alarm Enable' (AE) is '0', then that information will be compared with the current minute, hour, day and weekday. When all enabled comparisons first match, the 'Alarm Flag' (AF) is set. AF will remain set until cleared by software. Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their 'Alarm Enable' bit at '1' will be ignored.	
Alarm: Minute		**Address 09**	
6..0	Alarm minutes	00 - 59	This register holds the minute alarm information coded in BCD format.
7	AE	0	Minute alarm is enabled.
		1	Minute alarm is disabled.
Alarm: Hour		**Address 0A**	
5..0	Alarm hours	00 - 23	This register holds the hour alarm information coded in BCD format.
7	AE	0	Hour alarm is enabled.
		1	Hour alarm is disabled.
Alarm: Day		**Address 0B**	
5..0	Alarm days	01 - 31	This register holds the day alarm information coded in BCD format.
7	AE	0	Day alarm is enabled.
		1	Day alarm is disabled.
Alarm: Weekday		**Address 0C**	
2..0	Alarm weekdays	00 - 00	This register holds the weekday alarm information coded in BCD format.
7	AE	0	Weekday alarm is enabled.
		1	Weekday alarm is disabled.
CLKOUT frequency		**Address 0D**	
1..0	FD1, FD0		These bits control the frequency output on the CLKOUT pin, see table 2.
7	FE	0	The CLKOUT output is inhibited and CLKOUT output is set to logic 0.
		1	The CLKOUT output is activated.

BIT NO.	BIT NAME	BIT VALUE	DESCRIPTION
Countdown Timer		**Address 0E and 0F**	
			The timer register is an 8-bit binary countdown timer. It is enabled and disabled via the timer control register bit TE. The source clock for the timer is also selected by the timer control register. Other timer properties such as interrupt generation are controlled via control/status 2 registers. For accurate read back of the countdown value, the I^2C clock (SDA) must be operating at a frequency of at least twice the selected timer clock.
Timer control		**Address 0E**	
1..0	TD1, TD0		Timer source clock frequency select. These bits determine the source clock for the countdown timer, see table 3. When not in use, TD1 & TD0 should be set to 1/60 Hz for power saving.
7	TE	0	Timer is disabled.
		1	Timer is enabled.
Timer countdown value		**Address 0F**	
7..0	Timer	00..FF	Countdown value, n. $\text{CountdownPeriod} = \frac{n}{\text{SourceClockFrequency}}$

Notes

1. The PCF8563 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.
2. These bits may be re-assigned by the user.

Table 1 $\overline{\text{INT}}$ OPERATION (TI/TP=1)

$\overline{\text{INT}}$ PERIOD		
SOURCE CLOCK	**n = 1**	**n > 1**
4096 Hz	1/8192 s	1/4096 s
64 Hz	1/128 s	1/64 s
1 Hz	1/64 s	1/64 s
1/60 Hz	1/64 s	1/64 s

Notes

1. n = Loaded countdown value.
   Timer stopped when n = 0.
2. TF and $\overline{\text{INT}}$ become active simultaneously.

Table 2 FD1, FD0: CLKOUT frequency selection.

FD1	FD0	CLKOUT FREQUENCY
0	0	32.768 kHz
0	1	1024 Hz
1	0	32 Hz
1	1	1 Hz

Table 3 TD1, TD0: Timer frequency selection.

TD1	TD0	TIMER SOURCE CLOCK FREQUENCY
0	0	4096 Hz
0	1	64 Hz
1	0	1 Hz
1	1	1/60 Hz

Table 4 Weekday assignments.

DAY	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Sunday	x	x	x	x	x	0	0	0
Monday	x	x	x	x	x	0	0	1
Tuesday	x	x	x	x	x	0	1	0
Wednesday	x	x	x	x	x	0	1	1
Thursday	x	x	x	x	x	1	0	0
Friday	x	x	x	x	x	1	0	1
Saturday	x	x	x	x	x	1	1	0

Table 5 Month assignments

MONTH	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
January	C	x	x	0	0	0	0	1
February	C	x	x	0	0	0	1	0
March	C	x	x	0	0	0	1	1
April	C	x	x	0	0	1	0	0
May	C	x	x	0	0	1	0	1
June	C	x	x	0	0	1	1	0
July	C	x	x	0	0	1	1	1
August	C	x	x	0	1	0	0	0
September	C	x	x	0	1	0	0	1
October	C	x	x	1	0	0	0	0
November	C	x	x	1	0	0	0	1
December	C	x	x	1	0	0	1	0

EXT_CLK test mode.

A test mode is available which allows for on board testing. In such a mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting the TEST1 bit in Control/Status1. The CLKOUT pin then becomes an input. The test mode replaces the internal 64 Hz signal with that applied to the CLKOUT pin. Every 64 positive edges applied to CLKOUT will then generate an increment of one second.

The signal applied to the CLKOUT pin should have a minimum pulse width of 300ns and a minimum period of 1000ns. The internal 64 Hz clock, now sourced from CLKOUT, is divide down to 1 Hz by a 2^6 divide chain called a pre-scaler. The pre-scaler can be set into a known state by using the STOP bit. When the STOP bit is set, the pre-scaler is reset to 0. (STOP must be cleared before the pre-scaler can operate again).

From a STOP condition, the first 1 second increment will take place after 32 positive edges on CLKOUT. Thereafter, every 64 positive edges will cause a 1 second increment.

Note. Entry into EXT_CLK test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the pre-scaler can be made.

OPERATION EXAMPLE.

1. Set EXT_CLK test mode (Bit7 Control/Status1 = 1).
2. Set STOP (Bit5 Control/Status1 = 1).
3. Clear STOP (Bit5 Control/Status1 = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to CLKOUT.
8. Read time registers to see the second change.

Repeat 7 & 8 for additional increments.

Power On Reset override.

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up on board test of the device. The setting of this mode requires that the I^2C pins, SDA and SCL, be toggled in a specific order as shown in figure 3. All timings are required minimums.

Once the override mode has been entered, the chip immediately stops being reset and normal operation may commence i.e. entry into the EXT_CLK test mode via I^2C access. The override mode may be cleared by writing a 0 to TESTC. TESTC must be set to 1 before re-entry into the override mode is possible. Setting TESTC to 0 during normal operation has no effect except to prevent entry into the POR override mode.

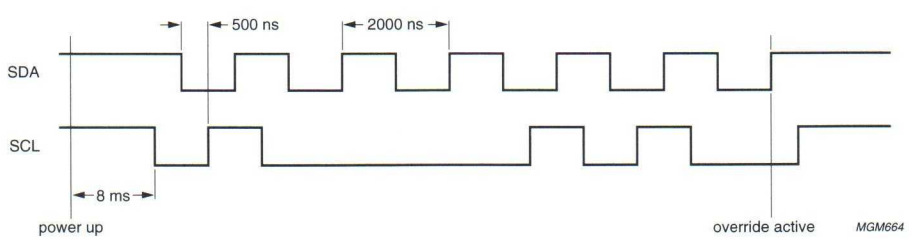


Fig.3 POR override sequence.

LIMITING VALUES.

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_I	input voltage	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
I_{DD}	Supply current	−50	+50	mA
I_{SS}	Supply current	−50	+50	mA
P_{TOT}	total power dissipation	−	300	mW
T_{AMB}	operating ambient temperature	−40	+85	°C
T_{STG}	storage temperature	−65	+150	°C

CHARACTERISTICS OF THE I²C-BUS.

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

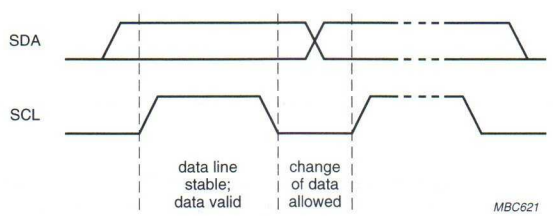


Fig.4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

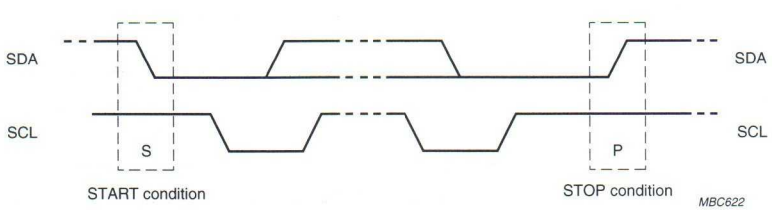


Fig.5 Definition of start and stop conditions.

System configuration (see Fig.6)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

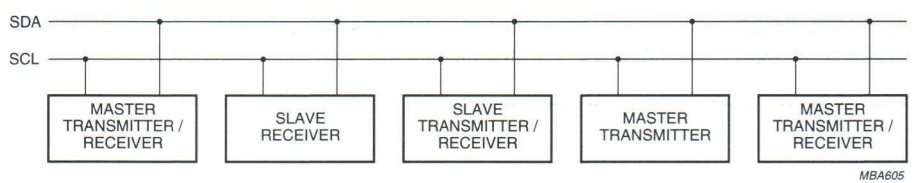


Fig.6 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

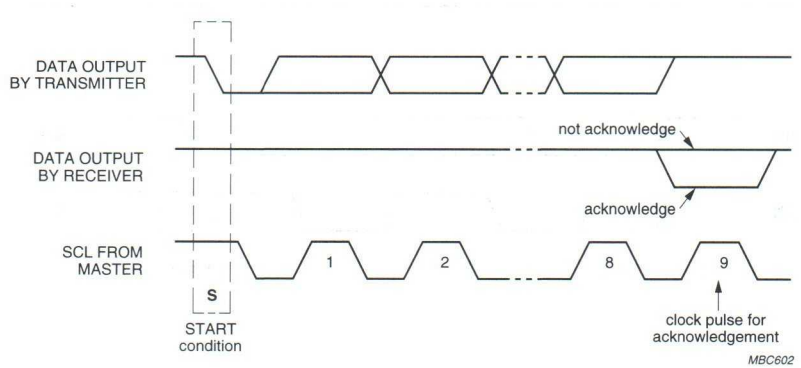


Fig.7 Acknowledgment on the I²C-bus.

I²C-BUS PROTOCOL.

Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The PCF8563 acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

The PCF8563 slave address is shown in Fig.8.

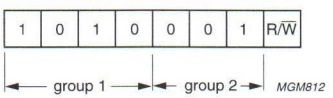


Fig.8 Slave address.

Clock/calendar READ/WRITE cycles

The I²C-bus configuration for the different PCF8563 READ and WRITE cycles is shown below. The word address is four bit value that defines which register is to be accessed next. The upper four bits of the word address are not used.

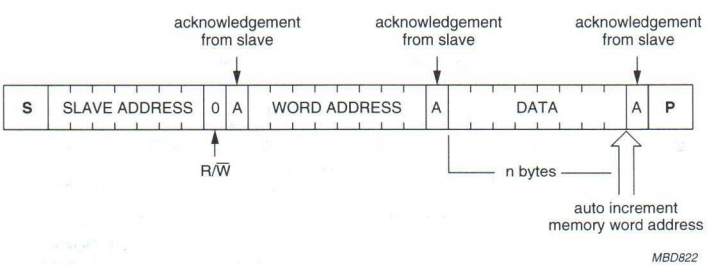


Fig.9 Master transmits to slave receiver (WRITE) mode.

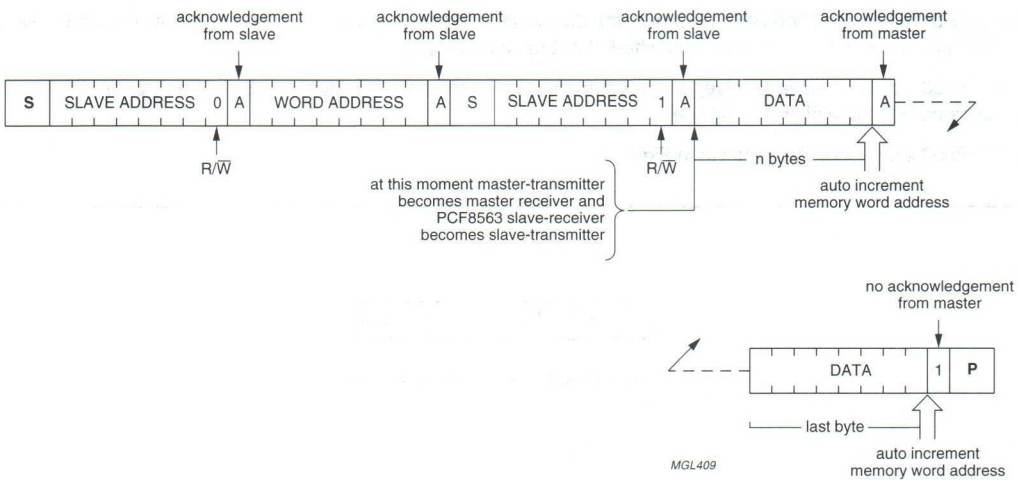


Fig.10 Master reads after setting word address (write word address; READ data).

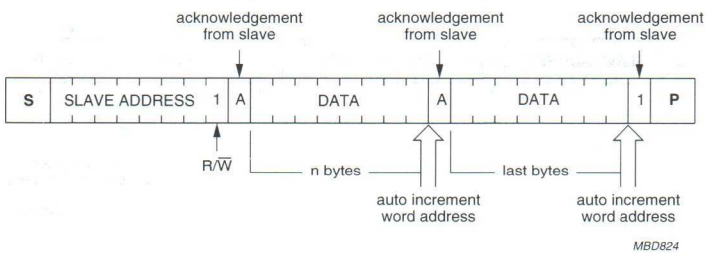


Fig.11 Master reads slave immediately after first byte (READ mode).

DC CHARACTERISTICS.

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{AMB} = −40 to +85 °C; f_{OSC} = 32.768 kHz; quartz R_S = 40 kΩ, C_L = 8 pF unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage (1)	I^2C bus inactive, 25 °C	1.0	–	5.5	V
		400 kHz I^2C bus activity	1.8	–	5.5	V
	clock data integrity	25 °C	V_{LOW}	–	5.5	V
I_{DD}	supply current (2)	f_{SCL} = 400 kHz	–	–	800	μA
		f_{SCL} = 100 kHz	–	–	200	μA
		f_{SCL} = 0 Hz V_{DD} = 5.0 V 25 °C	–	0.3	1.0	μA
		f_{SCL} = 0 Hz V_{DD} = 2.0 V 25 °C	–	0.25	0.75	μA
Inputs						
V_{IL}	LOW level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage	$V_I = V_{DD}$ or V_{SS}	−1	–	1	μA
C_I	input capacitance	(note 3)	–	–	7	pF
Outputs						
$I_{OL(SDA)}$	SDA LOW output current	V_{OL} = 0.4 V, V_{DD} = 5 V	−3	–	–	mA
$I_{OL(\overline{INT})}$	$\overline{INT}$ LOW output current	V_{OL} = 0.4 V, V_{DD} = 5 V	−1	–	–	mA
$I_{OL(CLKOUT)}$	CLKOUT LOW output current	V_{OL} = 0.4 V, V_{DD} = 5 V	−1	–	–	mA
$I_{OH(CLKOUT)}$	CLKOUT HIGH output current	V_{OH} = 4.6 V, V_{DD} = 5 V	1	–	–	mA
I_{LO}	output leakage	$V_O = V_{DD}$ or V_{SS}	−1	–	1	μA
Voltage detector						
V_{LOW}	Low voltage detection	25 °C	–	0.9	1.0	V

Notes

1. When powering up the device, V_{DD} must exceed the specified minimum value by 300 mV to guarantee correct start-up of the oscillator.
2. CLKOUT disabled, (FE = 0). Timer source clock = $1/_{60}$ Hz.
3. Tested on sample basis.

AC CHARACTERISTICS.

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{AMB} = −40 to +85 °C; f_{OSC} = 32.768 kHz; quartz R_S = 40 kΩ, C_L = 8 pF unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
C_L	integrated load capacitance		19	25	31	pF
f/f_{OSC}	oscillator stability	for ΔV_{DD} = 200 mV; 25 °C	–	$2x10^{-7}$	–	–
Quartz crystal parameters (f = 32.768 kHz)						
R_s	series resistance		–	–	40	kΩ
C_L	parallel load capacitance		–	10	–	pF
C_T	trimmer capacitance		5	–	25	pF
CLKOUT output						
T_{CLKOUT}	CLKOUT duty cycle	note 1	–	50	–	%
Timing characteristics: I²C-bus; notes 5 & 6						
f_{SCL}	SCL clock frequency	note 4	–	–	400	kHz
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
t_{LOW}	SCL LOW time		1.3	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
t_r	SCL and SDA rise time		–	–	0.3	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns

Notes

1. Unspecified for f_{CLKOUT} = 32.768 kHz.
2. All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
3. A detailed description of the I²C bus specification, with applications, is given in brochure "The I²C bus and how to use it". This brochure may be ordered using the code 9398 393 40011.
4. I²C access time between two STARTs or between a START and a STOP condition to this device must be less than one second.

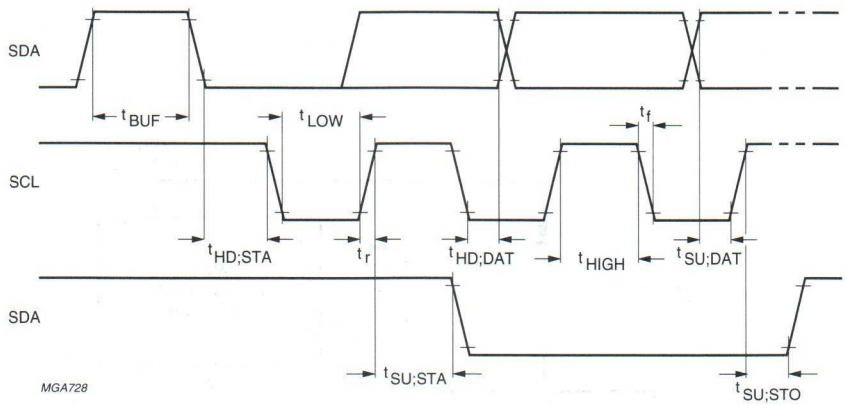


Fig.12 I²C-bus timing waveforms.

APPLICATION INFORMATION

Quartz frequency adjustment

METHOD 1: FIXED OSCI CAPACITOR

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 32.768 kHz signal available after power-on at the CLKOUT pin. The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$). Average deviations of ±5 minutes per year can be easily achieved.

METHOD 2: OSCI TRIMMER

Using the 32.768 kHz signal available after power-on at the CLKOUT pin fast setting of a trimmer is possible.

METHOD 3:

Direct measurement of OSCO out (accounting for test probe capacitance).

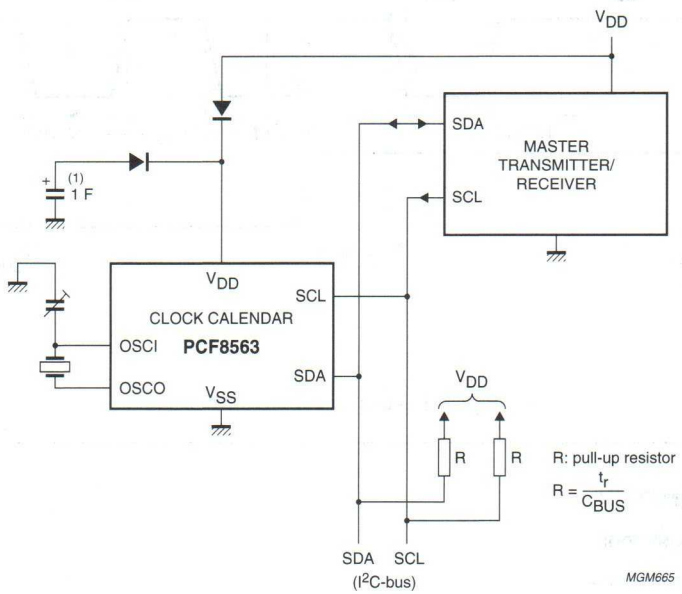


Fig.13 Application diagram.

Universal LCD driver for low multiplex rates

PCF8566

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2, 3 or 4 backplane multiplexing
- Selectable display bias configuration: static, ½ or ⅓
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2.5 to 6 V power supply range
- Low power consumption
- Power saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576C
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40 lead plastic very small outline package (VSO40; SOT158-1)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8566P	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF8566T	VSO40	plastic very small outline package; 40 leads	SOT158-1

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM

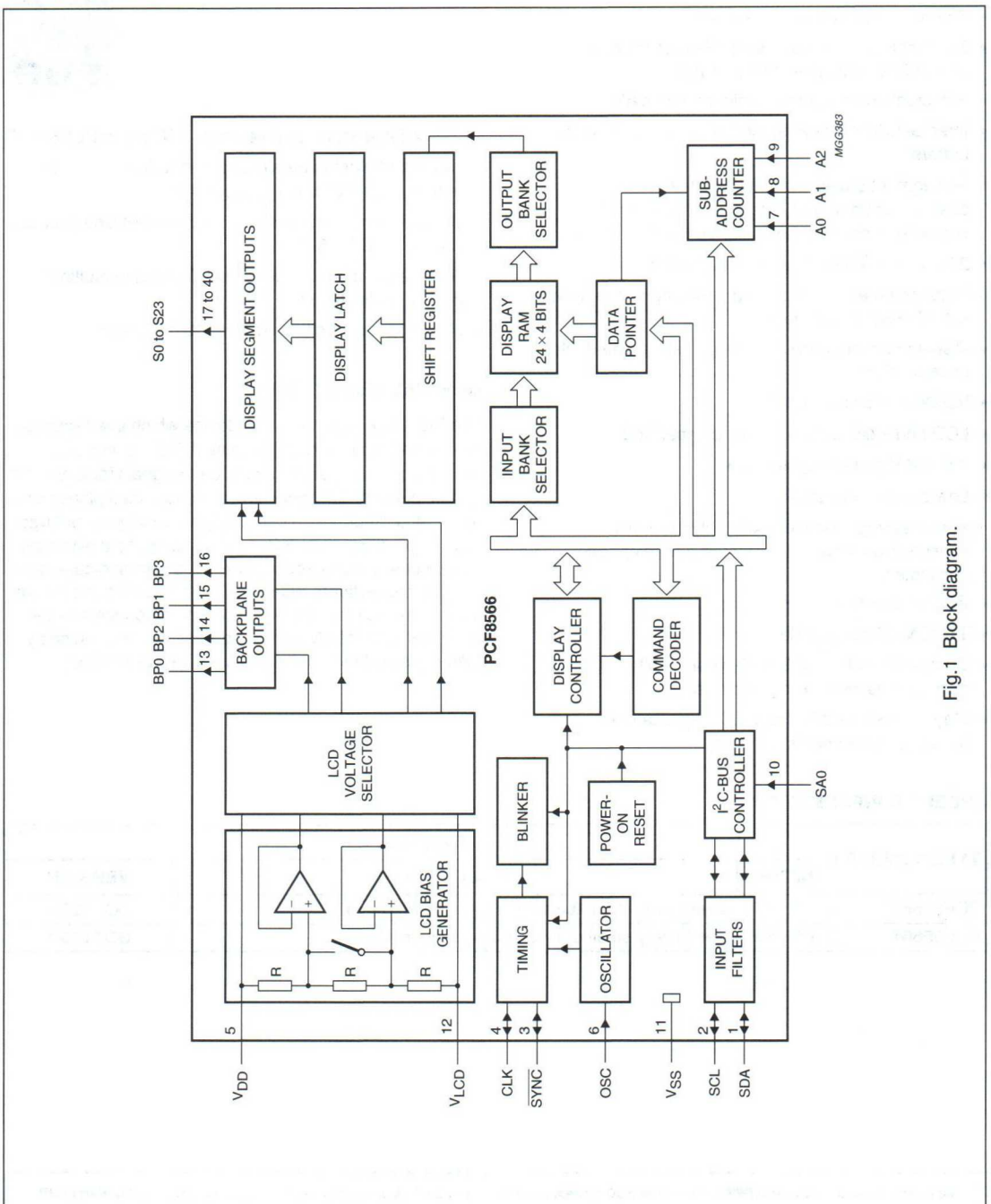


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus data input/output
SCL	2	I²C-bus clock input/output
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	external clock input/output
V_{DD}	5	positive supply voltage
OSC	6	oscillator input
A0	7	I²C-bus subaddress inputs
A1	8	
A2	9	
SA0	10	I²C-bus slave address bit 0 input
V_{SS}	11	logic ground
V_{LCD}	12	LCD supply voltage
BP0	13	LCD backplane outputs
BP2	14	
BP1	15	
BP3	16	
S0 to S23	17 to 40	LCD segment outputs

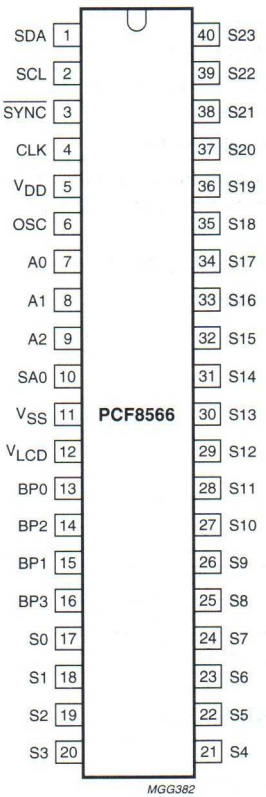


Fig.2 Pin configuration.

Clock/calendar with Power Fail Detector PCF8573

FEATURES

- Serial input/output I²C-bus interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- On-chip power fail detector
- Separate ground pin for the clock allows easy implementation of battery back-up during supply interruption
- Crystal oscillator control (32.768 kHz)
- Low power consumption.

GENERAL DESCRIPTION

The PCF8573 is a low threshold, CMOS circuit that functions as a real time clock/calendar. Addresses and data are transferred serially via the two-line bidirectional I²C-bus.

The IC incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Back-up for the clock during supply interruptions is provided by a 1.2 V nickel cadmium battery. The time base is generated from a 32.768 kHz crystal-controlled oscillator.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DD} - V_{SS1}$	supply voltage, clock (pin 16 to pin 15)	1.1	–	6.0	V
$V_{DD} - V_{SS2}$	supply voltage, I²C-bus (pin 16 to pin 8)	2.5	–	6.0	V
f_{osc}	crystal oscillator frequency	–	32.768	–	kHz

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8573P	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
PCF8573T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM

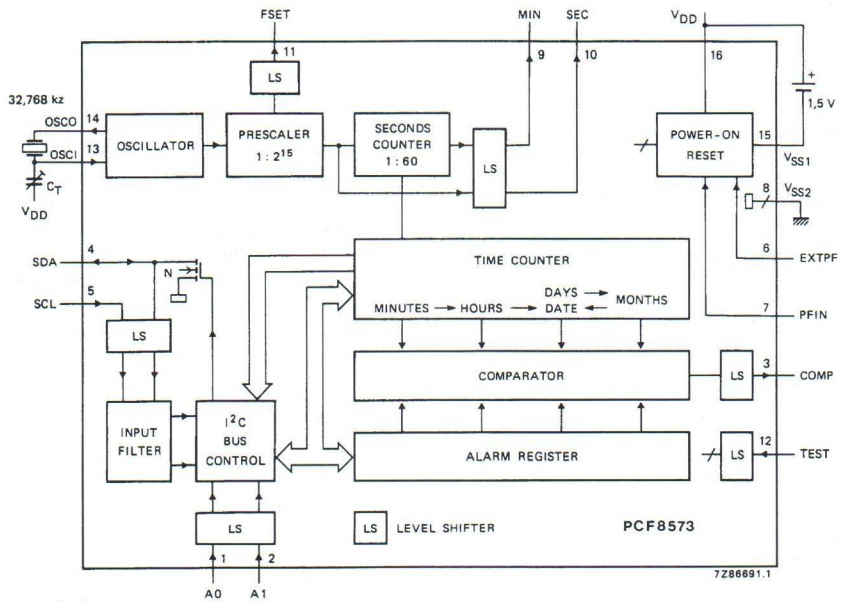


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	address input
A1	2	address input
COMP	3	comparator output
SDA	4	serial data line; I^2C-bus
SCL	5	serial clock line; I^2C-bus
EXTPF	6	enable power fail flag input
PFIN	7	power fail flag input
V_{SS2}	8	negative supply 2 (I^2C interface)
MIN	9	one pulse per minute output
SEC	10	one pulse per second output
FSET	11	oscillator tuning output
TEST	12	test input; connect to V_{SS2} if not in use
OSCI	13	oscillator input
OSCO	14	oscillator input/output
V_{SS1}	15	negative supply 1 (clock)
V_{DD}	16	common positive supply

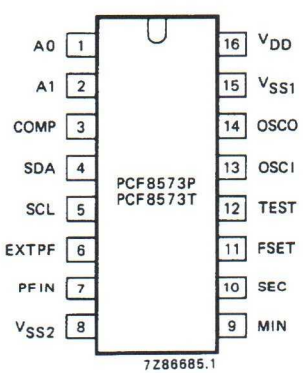


Fig.2 Pinning diagram.

Remote 8-bit I/O expander for I²C-bus PCF8574

FEATURES

- Operating supply voltage 2.5 to 6 V
- Low standby current consumption of 10 μA maximum
- I²C to parallel port expander
- Open-drain interrupt output
- 8-bit remote I/O port for the I²C-bus
- Compatible with most microcontrollers
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)
- DIP16, or space-saving SO16 or SSOP20 packages.

GENERAL DESCRIPTION

The PCF8574 is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I²C).

The device consists of an 8-bit quasi-bidirectional port and an I²C-bus interface. The PCF8574 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line ($\overline{INT}$) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and PCF8574A versions differ only in their slave address.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8574P; PCF8574AP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
PCF8574T; PCF8574AT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCF8574TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM

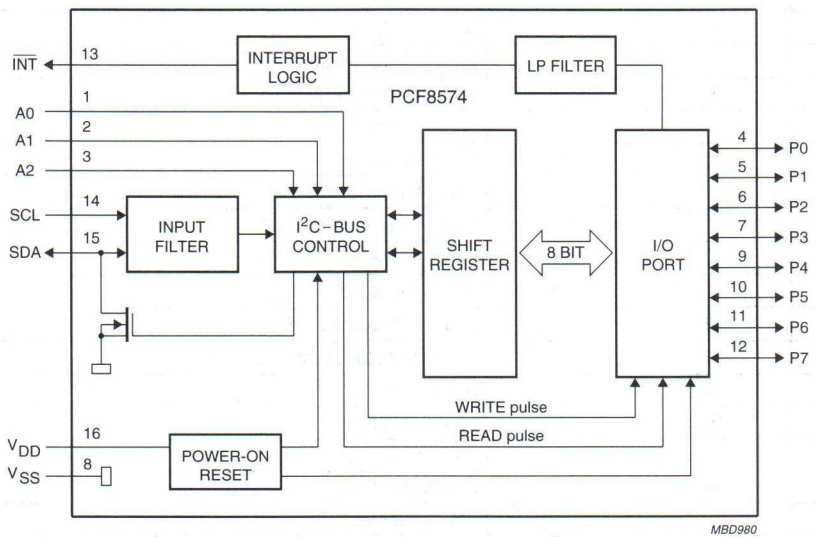


Fig.1 Block diagram (SOT38-1 and SOT162-1).

PINNING

SYMBOL	PIN		DESCRIPTION
	DIP16; SO16	SSOP20	
A0	1	6	address input 0
A1	2	7	address input 1
A2	3	9	address input 2
P0	4	10	quasi-bidirectional I/O 0
P1	5	11	quasi-bidirectional I/O 1
P2	6	12	quasi-bidirectional I/O 2
P3	7	14	quasi-bidirectional I/O 3
V_{SS}	8	15	supply ground
P4	9	16	quasi-bidirectional I/O 4
P5	10	17	quasi-bidirectional I/O 5
P6	11	19	quasi-bidirectional I/O 6
P7	12	20	quasi-bidirectional I/O 7
$\overline{INT}$	13	1	interrupt output (active LOW)
SCL	14	2	serial clock line
SDA	15	4	serial data line
V_{DD}	16	5	supply voltage
n.c.	–	3	not connected
n.c.	–	8	not connected
n.c.	–	13	not connected
n.c.	–	18	not connected

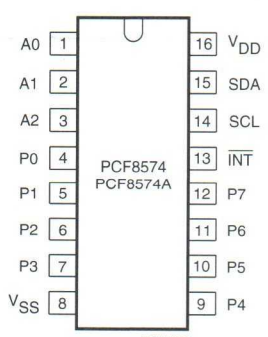


Fig.2 Pin configuration (DIP16; SO16).

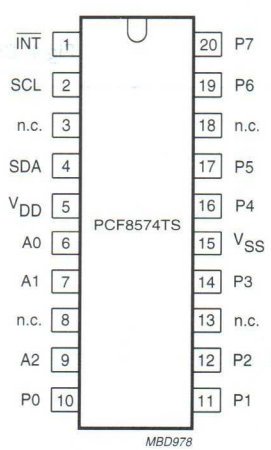


Fig.3 Pin configuration (SSOP20).

Universal LCD driver for low multiplex rates

PCF8576

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$ or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with 24-segment LCD driver PCF8566
- Optimized pinning for plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic very small outline package (VSO56)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8576T	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8576U	–	chip in tray	–
PCF8576U/2	–	chip with bumps in tray	–
PCF8576U/5	–	unsawn wafer	–
PCF8576U/7	–	chip with bumps on tape	–
PCF8576U/10	FFC	chip on film frame carrier (FFC)	–
PCF8576U/12	FFC	chip with bumps on film frame carrier (FFC)	–

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM

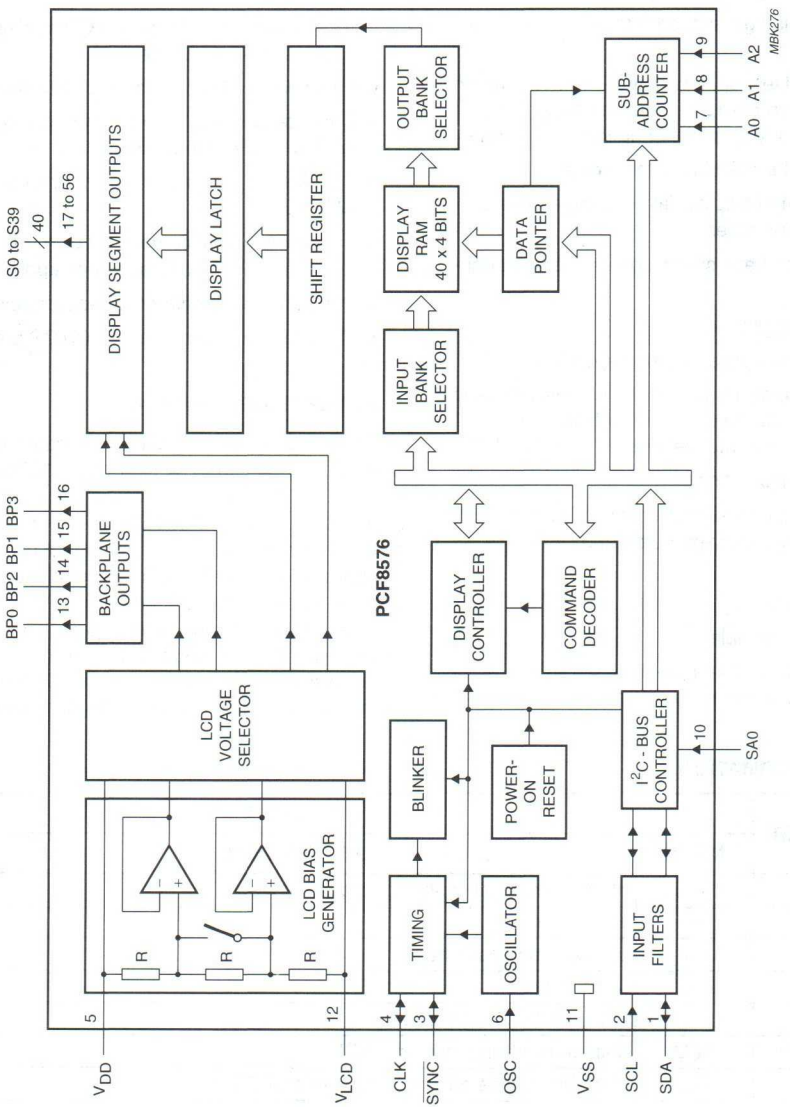


Fig.1 Block diagram (for VSO56 package; SOT190-1).

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I^2C-bus serial data input/output
SCL	2	I^2C-bus serial clock input
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	external clock input/output
V_{DD}	5	supply voltage
OSC	6	oscillator input
A0 to A2	7 to 9	I^2C-bus subaddress inputs
SA0	10	I^2C-bus slave address input; bit 0
V_{SS}	11	logic ground
V_{LCD}	12	LCD supply voltage
BP0, BP2, BP1 and BP3	13 to 16	LCD backplane outputs
S0 to S39	17 to 56	LCD segment outputs

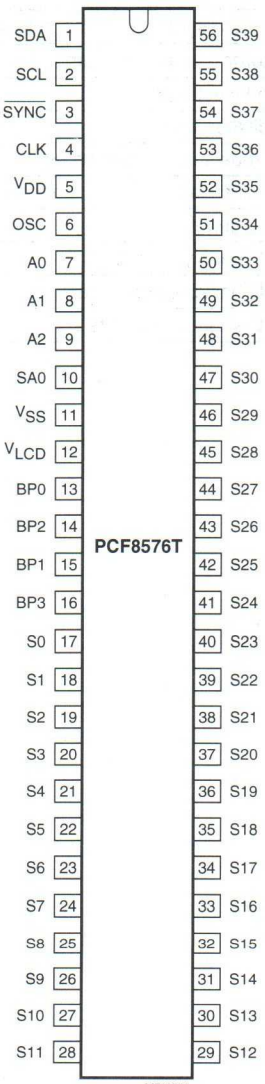


Fig.2 Pin configuration; SOT190-1.

Universal LCD driver for low multiplex rates

PCF8576C

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 6 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs.

  A 9 V version is also available on request.
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with 24-segment LCD driver PCF8566
- Optimized pinning for plane wiring in both and multiple PCF8576C applications
- Space-saving 56-lead plastic very small outline package (VSO56) or 64-lead low profile quad flat package (LQFP64)
- No external components
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The PCF8576C is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576C is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8576CT	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8576CU	–	chip in tray	–
PCF8576CU/2	–	chip with bumps in tray	–
PCF8576CU/5	–	unsawn wafer	–
PCF8576CU/7	–	chip with bumps on tape	–
PCF8576CU/10	FFC	chip-on-film frame carrier	–
PCF8576CU/12	FFC	chip with bumps on film frame carrier	–
PCF8576CH	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

BLOCK DIAGRAM

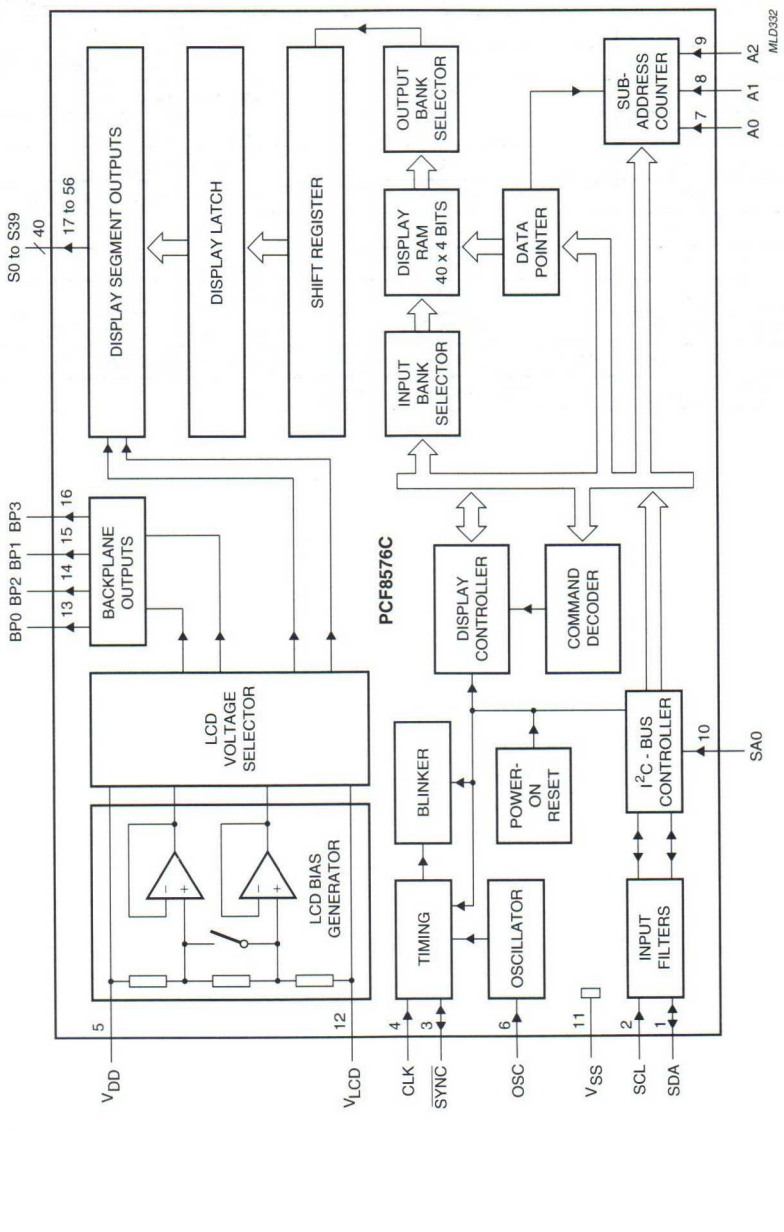


Fig.1 Block diagram; VSO56.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT190	SOT314	
SDA	1	10	I^2C-bus serial data input/output
SCL	2	11	I^2C-bus serial clock input
$\overline{SYNC}$	3	12	cascade synchronization input/output
CLK	4	13	external clock input
V_{DD}	5	14	supply voltage
OSC	6	15	oscillator input
A0 to A2	7 to 9	16 to 18	I^2C-bus subaddress inputs
SA0	10	19	I^2C-bus slave address input; bit 0
V_{SS}	11	20	logic ground
V_{LCD}	12	21	LCD supply voltage
BP0, BP2, BP1, BP3	13 to 16	25 to 28	LCD backplane outputs
S0 to S39	17 to 56	29 to 32, 34 to 47, 49 to 64, 2 to 7	LCD segment outputs
n.c.	–	1, 8, 9, 22 to 24, 33 and 48	not connected

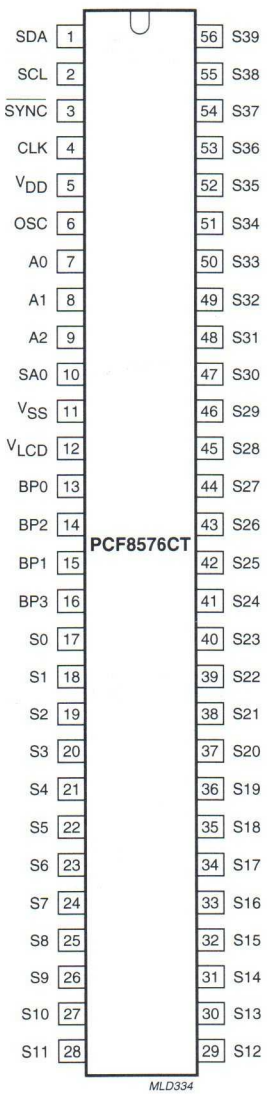


Fig.2 Pin configuration; VSO56.

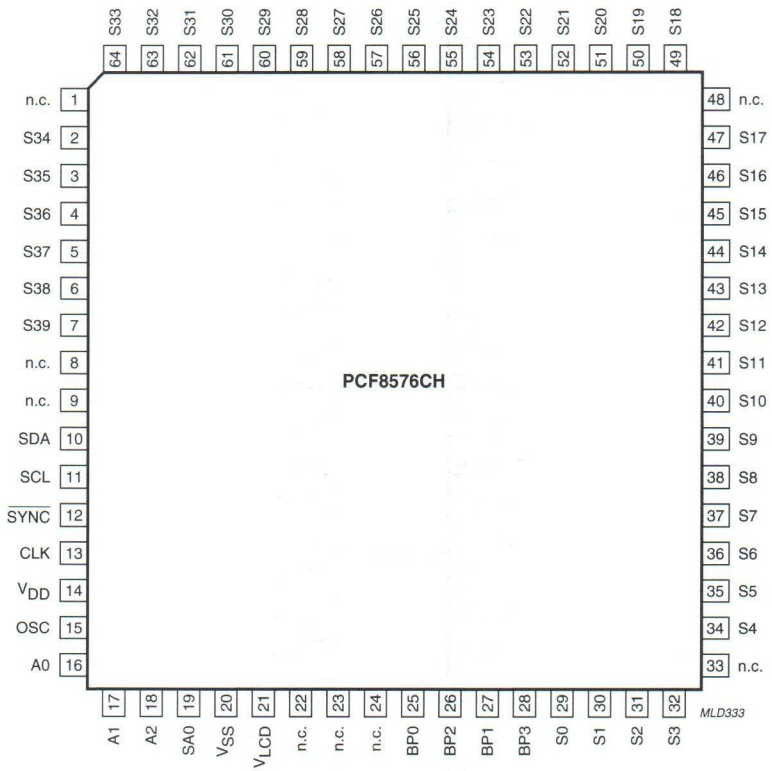


Fig.3 Pin configuration; LQFP64.

LCD direct/duplex driver with I²C-bus interface

PCF8577C

FEATURES

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments
- Power-on reset blanks display
- I²C-bus address: 0111 0100.

GENERAL DESCRIPTION

The PCF8577C is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex configuration.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. I²C-bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware subaddressing and display memory switching (direct drive mode).To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8577CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF8577CT	VSO40	plastic very small outline package; 40 leads	SOT158A
PCF8577CT	–	VS040 in blister tape	–
PCF8577CU/10	–	chip on film-frame-carrier (FFC)	–

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM

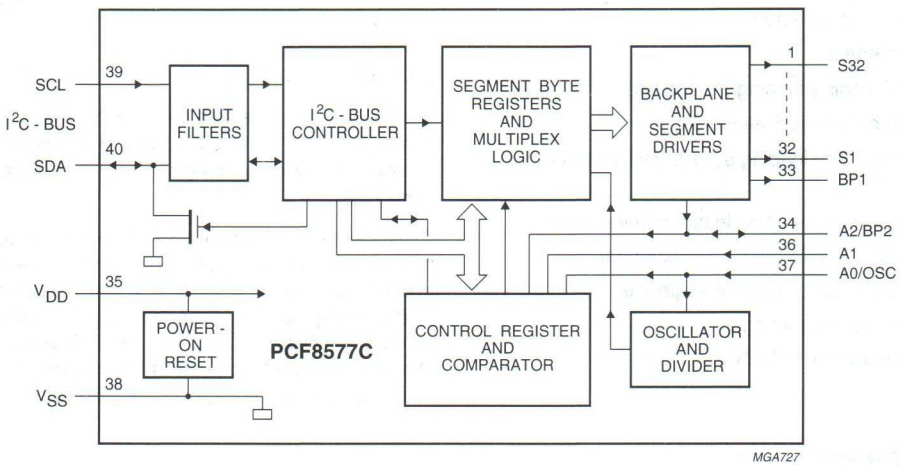


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
S32 to S1	1 to 32	segments outputs
BP1	33	cascade sync input/backplane output
A2/BP2	34	hardware address line and cascade sync input/backplane output
V_{DD}	35	positive supply voltage
A1	36	hardware address line input
A0/OSC	37	hardware address line and oscillator pin input
V_{SS}	38	negative supply voltage
SCL	39	I²C-bus clock line input
SDA	40	I²C-bus data line input/output

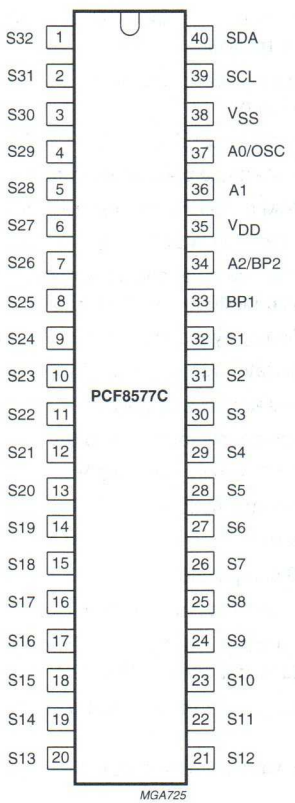


Fig.2 Pin configuration.

LCD row/column driver for dot matrix graphic displays

PCF8578

FEATURES

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40960 dots possible)
- 40 driver outputs, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack and 64 pin quad flat pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

GENERAL DESCRIPTION

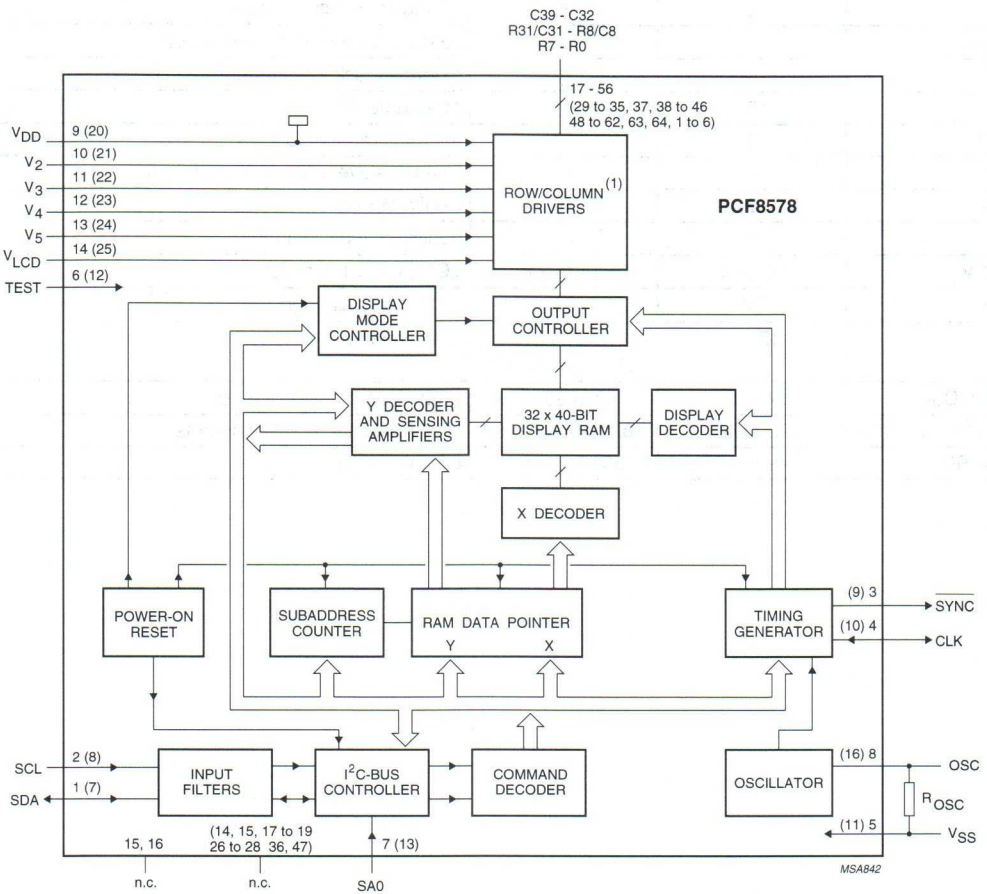
The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs, of which 24 are programmable, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8578T	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8578U7	–	chip with bumps on tape	–
PCF8578H	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM



(1) Operates at LCD voltage levels, all other blocks operate at logic levels.
The pin numbers given in parenthesis refer to the LQFP64 package.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	VSO56	LQFP64	
SDA	1	7	I^2C-bus serial data input/output
SCL	2	8	I^2C-bus serial clock input
$\overline{SYNC}$	3	9	cascade synchronization output
CLK	4	10	external clock input/output
V_{SS}	5	11	ground (logic)
TEST	6	12	test pin (connect to V_{SS})
SA0	7	13	I^2C-bus slave address input (bit 0)
OSC	8	16	oscillator input
V_{DD}	9	20	positive supply voltage
V_2 to V_5	10 to 13	21 to 24	LCD bias voltage inputs
V_{LCD}	14	25	LCD supply voltage
n.c.	15, 16	14, 15, 17 to 19, 26 to 28, 36, 47	not connected
C39 to C32	17 to 24	29 to 35, 37	LCD column driver outputs
R31/C31 to R8/C8	25 to 48	38 to 46, 48 to 62	LCD row/column driver outputs
R7 to R0	49 to 56	63, 64, 1 to 6	LCD row driver outputs

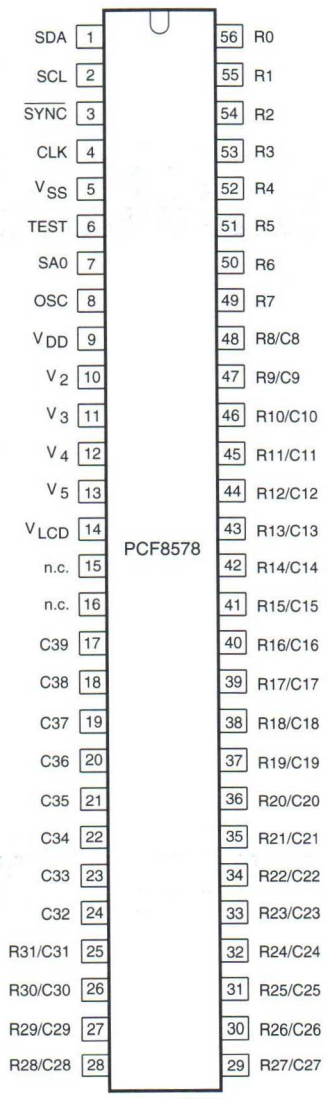


Fig.2 Pin configuration (VSO56).

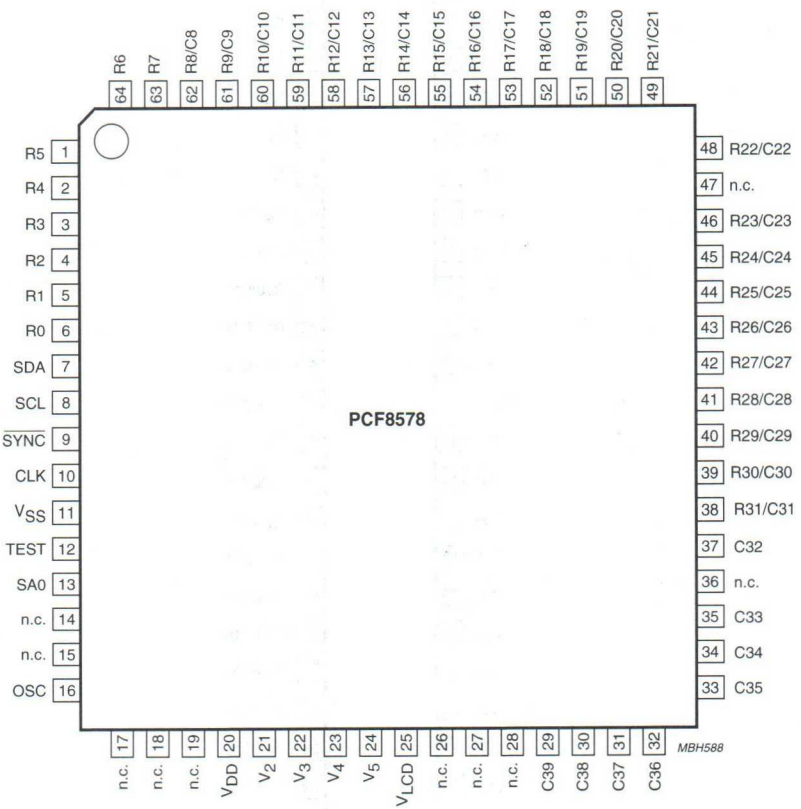


Fig.3 Pin configuration (LQFP64).

LCD column driver for dot matrix graphic displays

PCF8579

FEATURES

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40960 dots
- 40 column outputs
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8578)
- Power-on reset blanks display
- Logic voltage supply range 2.5 to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8578)
- Space saving 56-lead plastic mini-pack and 64-pin plastic low profile quad flat package
- Compatible with chip-on-glass technology
- I²C-bus address: 011110 SA0.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

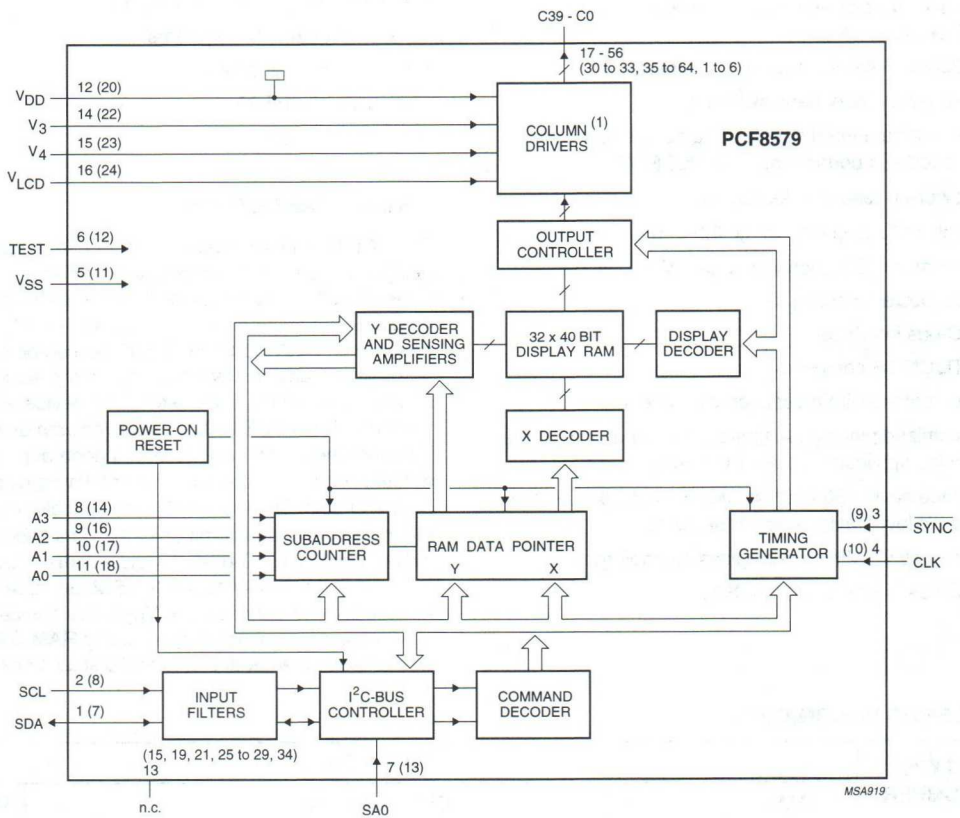
GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs and can drive 32 × 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I²C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}. Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8579T	VSO56	plastic very small outline package; 56 leads	SOT190
PCF8579U7	–	chip with bumps on tape	–
PCF8579H	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

BLOCK DIAGRAM



(1) Operates at LCD voltage levels, all other blocks operate at logic levels.
The pin numbers given in parenthesis refer to the LQFP64 package.

Fig.1 Block diagram.

PINNING

SYMBOL	PINS		DESCRIPTION
	VSO56	LQFP64	
SDA	1	7	I²C-bus serial data input/output
SCL	2	8	I²C-bus serial clock input
$\overline{SYNC}$	3	9	cascade synchronization input
CLK	4	10	external clock input
V_{SS}	5	11	ground (logic)
TEST	6	12	test pin (connect to V_{SS})
SA0	7	13	I²C-bus slave address input (bit 0)
A3 to A0	8 to 11	14, 16 to 18	I²C-bus subaddress inputs
V_{DD}	12	20	supply voltage
n.c.	13[1]	15, 19, 21,25 to 29, 34	not connected
V_3, V_4	14 and 15	22 and 23	LCD bias voltage inputs
V_{LCD}	16	24	LCD supply voltage
C39 to C0	17 to 56	30 to 33, 35 to 64 and 1 to 6	LCD column driver outputs

Note

1. Do not connect, this pin is reserved.

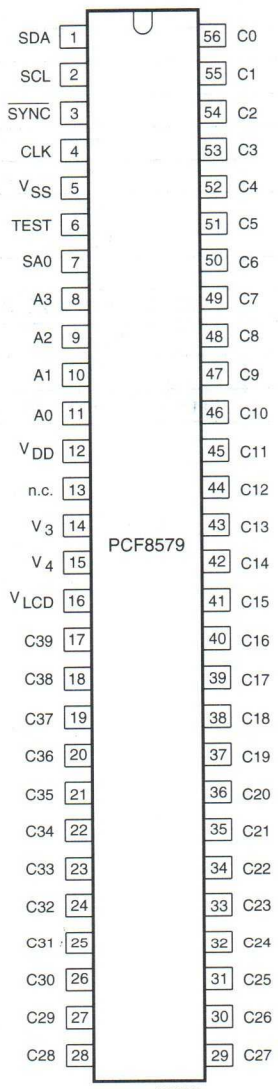


Fig.2 Pin configuration (VSO56).

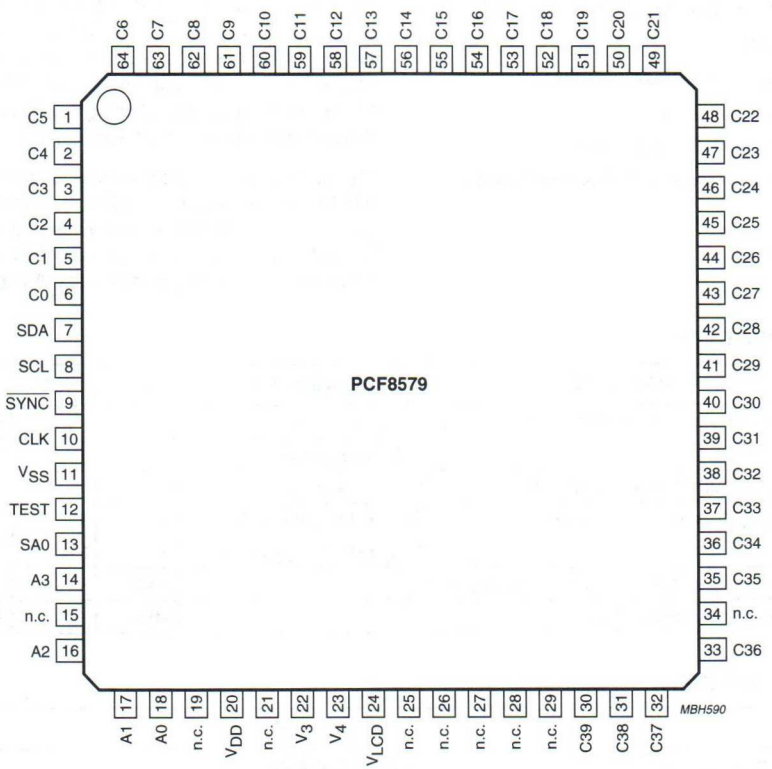


Fig.3 Pin configuration (LQFP64).

Clock/calendar with 240 × 8-bit RAM PCF8583

FEATURES

- I²C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage (0 to +70 °C): 1.0 V to 6.0 V
- 240 × 8-bit low-voltage RAM
- Data retention voltage: 1.0 V to 6 V
- Operating current (at f_{SCL} = 0 Hz): max. 50 μA
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Slave address:
  - READ: A1 or A3
  - WRITE: A0 or A2.

GENERAL DESCRIPTION

The PCF8583 is a clock/calendar circuit based on a 2048-bit static CMOS RAM organized as 256 words by 8 bits. Addresses and data are transferred serially via the two-line bidirectional I²C-bus. The built-in word address register is incremented automatically after each written or read data byte. Address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware.

The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space. The remaining 240 bytes are free RAM locations.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage operating mode	I²C-bus active	2.5	–	6.0	V
		I²C-bus inactive	1.0	–	6.0	V
I_{DD}	supply current operating mode	f_{SCL} = 100 kHz	–	–	200	μA
I_{DDO}	supply current clock mode	f_{SCL} = 0 Hz; V_{DD} = 5 V	–	10	50	μA
		f_{SCL} = 0 Hz; V_{DD} = 1 V	–	2	10	μA
T_{amb}	operating ambient temperature range		−40	–	+85	°C
T_{stg}	storage temperature range		−65	–	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8583P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8583T	SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT176-1

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM

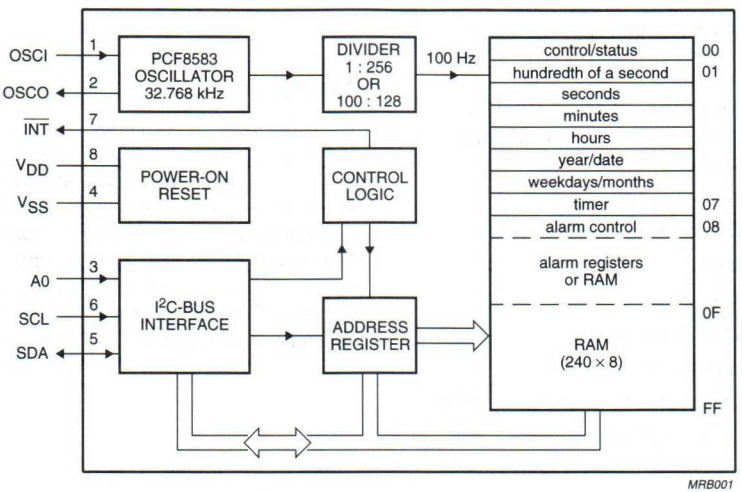


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
A0	3	address input
V_{SS}	4	negative supply
SDA	5	serial data line
SCL	6	serial clock line
$\overline{INT}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

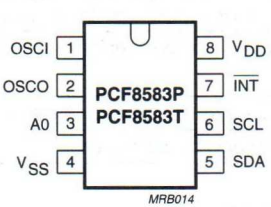


Fig.2 Pinning diagram.

Low power clock/calendar PCF8593

FEATURES

- I^2C-bus interface operating supply voltage: 2.5 to 6.0 V
- Clock operating supply voltage (T_{amb} = 0 to +70 °C): 1.0 to 6.0 V
- 8 bytes scratchpad RAM (when alarm not used)
- Data retention voltage: 1.0 to 6.0 V
- External $\overline{RESET}$ input resets I^2C interface (only)
- Operating current (f_{scl} = 0 Hz, 32 kHz time base, V_{DD} = 2.0 V): typ. 1 µA
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I^2C-bus)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Space-saving SO8 package available
- Slave address:
  - READ A3
  - WRITE A2.

GENERAL DESCRIPTION

The PCF8593 is a CMOS clock/calendar circuit, optimized for low power consumption. Addresses and data are transferred serially via the two-line bidirectional I^2C-bus. The built-in word address register is incremented automatically after each written or read data byte.
The built-in 32.768 kHz oscillator circuit and the first 8 bytes of RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage operating mode	I^2C-bus active	2.5	–	6.0	V
		I^2C-bus inactive	1.0	–	6.0	V
I_{DD}	supply current operating mode	f_{scl} = 100 kHz	–	–	200	µA
I_{DD}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V	–	4.0	15.0	µA
		f_{scl} = 0 Hz; V_{DD} = 2 V	–	1.0	8.0	µA
T_{amb}	operating ambient temperature		−40	–	+85	°C
T_{stg}	storage temperature		−65	–	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8593P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8593T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

Full Data Sheet: on CD-ROM/WWW (Internet) or FOD-system (details in front Section/back of this HB), or updated Loose leaf or Parent HB

BLOCK DIAGRAM

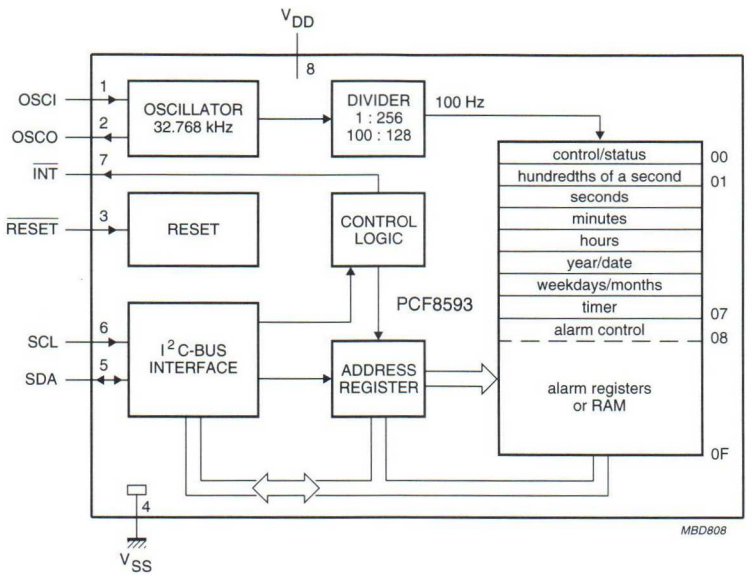


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
$\overline{\text{RESET}}$	3	reset input (active LOW)
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
$\overline{\text{INT}}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

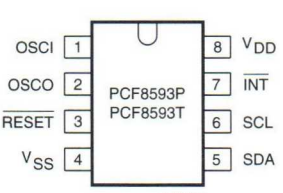


Fig.2 Pin configuration.

PACKAGE INFORMATION

	Page
Index	1326
DIP	1327
LQFP	1337
QFP	1338
SDIP	1341
SO	1342
SSOP	1352
VSO	1354
Soldering	1355

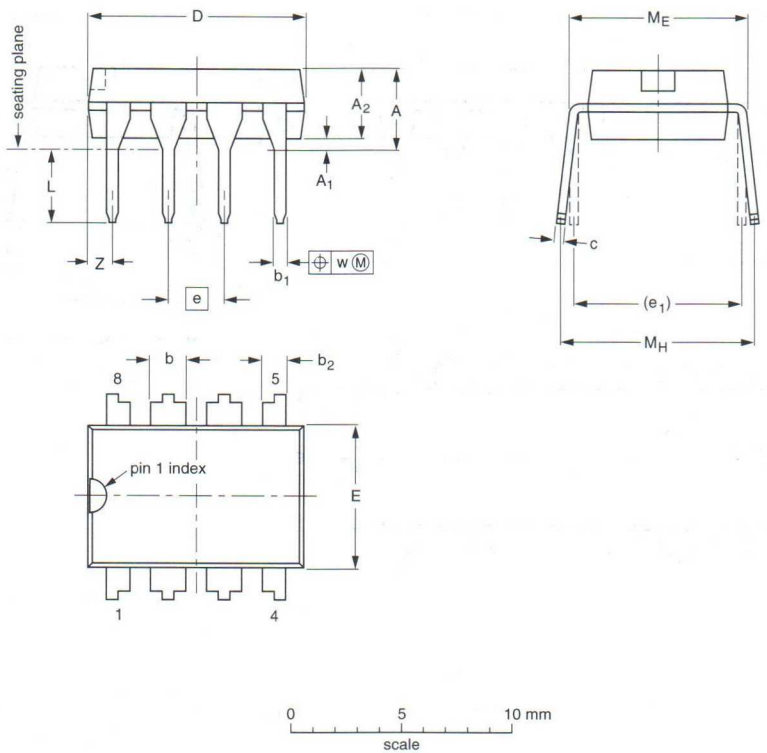
INDEX

NAME	DESCRIPTION	VERSION	PAGE
DIP (dual in-line package)			
DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1	1327
DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1	1328
DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1	1329
DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4	1330
DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-9	1331
DIP18	plastic dual in-line package; 18 leads (300 mil)	SOT102-1	1332
DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1	1333
DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1	1334
DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1	1335
DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	1336
LQFP (low profile quad flat package)			
LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1	1337
QFP (quad flat package)			
QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1	1338
QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2	1339
QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT318-2	1340
SDIP (shrink dual in-line package)			
SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1	1341
SO (small outline)			
SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1	1342
SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT176-1	1343
SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1	1344
SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1	1345
SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1	1346
SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1	1347
SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1	1348
SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1	1349
SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1	1350
SSOP (shrink small outline package)			
SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1	1351
SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1	1352
SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1	1353
VSO (very small outline)			
VSO40	plastic very small outline package; 40 leads	SOT158-1	1354

DIP

DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

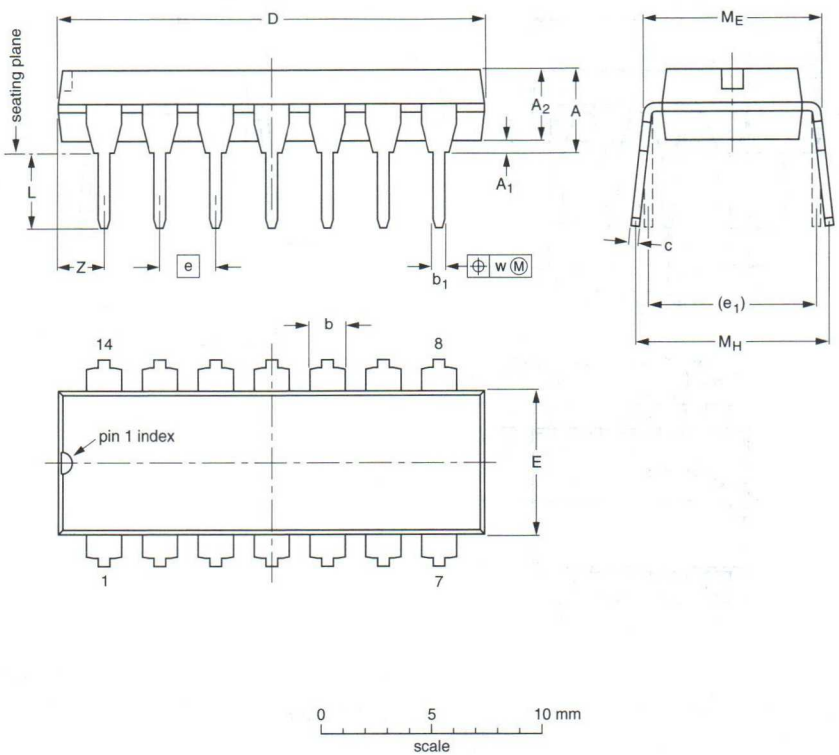
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

DIP14: plastic dual in-line package; 14 leads (300 mil) SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

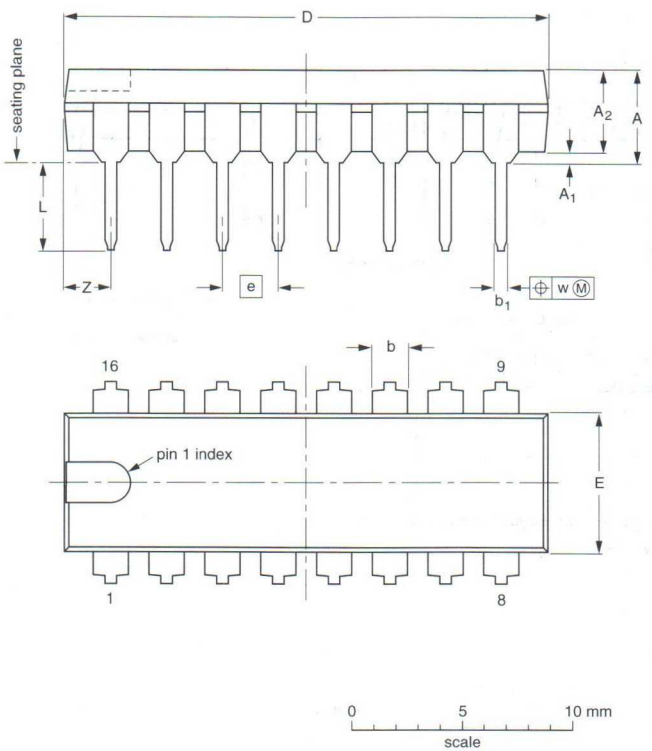
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

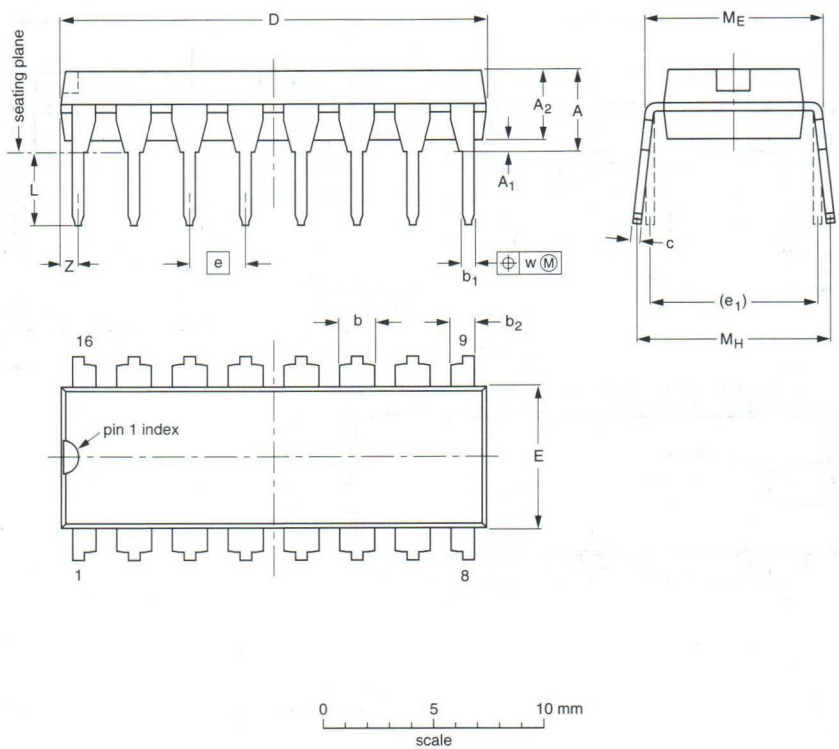
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

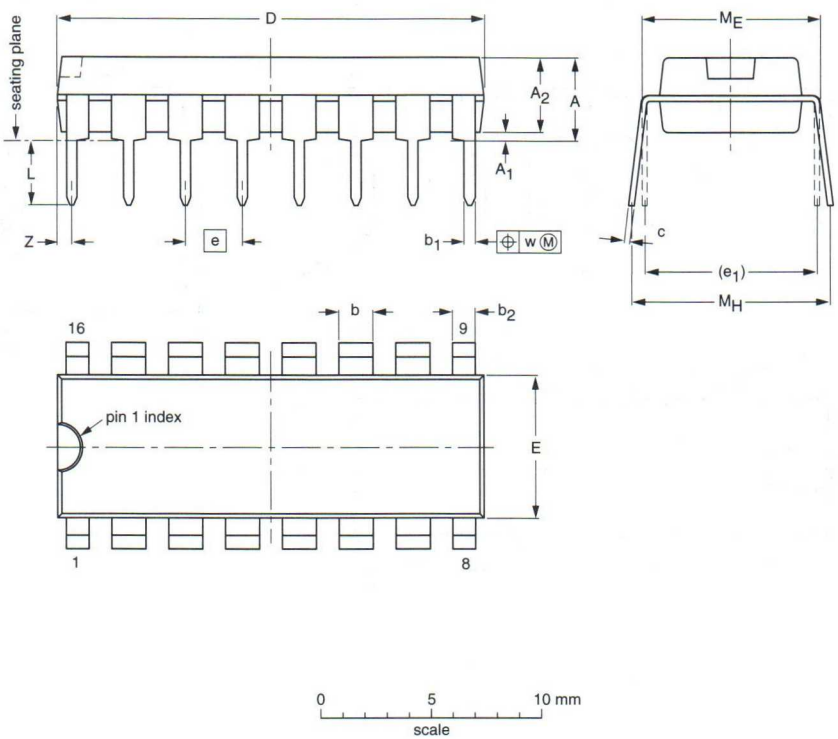
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-9**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

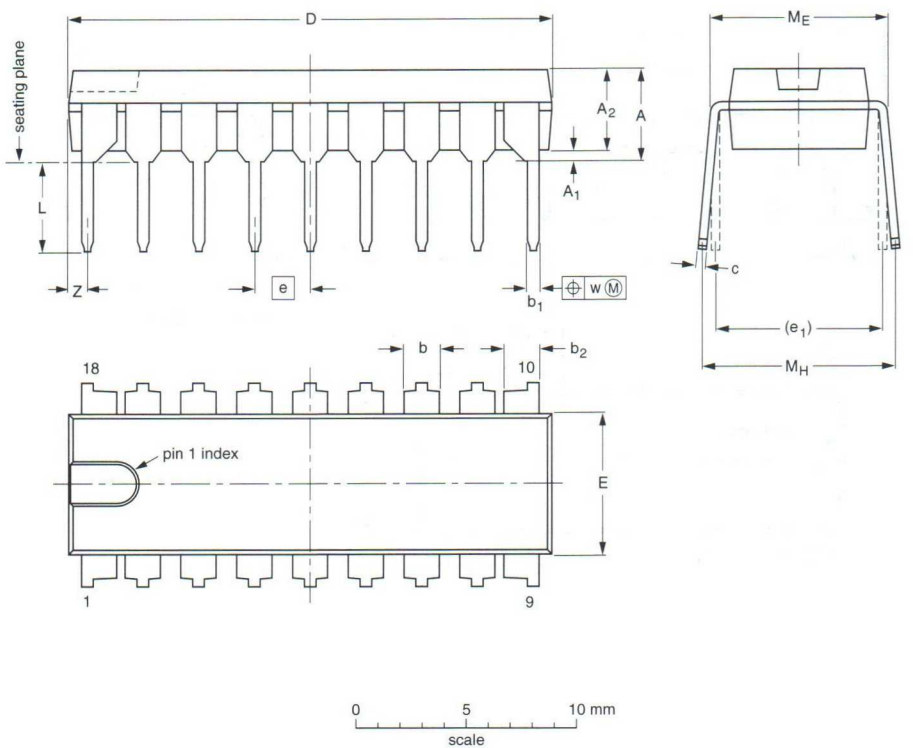
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.32	0.38	3.56	1.65 1.40	0.51 0.41	1.14 0.76	0.36 0.20	19.30 18.80	6.45 6.24	2.54	7.62	3.81 2.92	8.23 7.62	9.40 8.38	0.254	0.76
inches	0.17	0.015	0.14	0.065 0.055	0.020 0.016	0.045 0.030	0.014 0.008	0.76 0.74	0.254 0.246	0.10	0.30	0.150 0.115	0.324 0.300	0.37 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-9						97-07-24

DIP18: plastic dual in-line package; 18 leads (300 mil) **SOT102-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

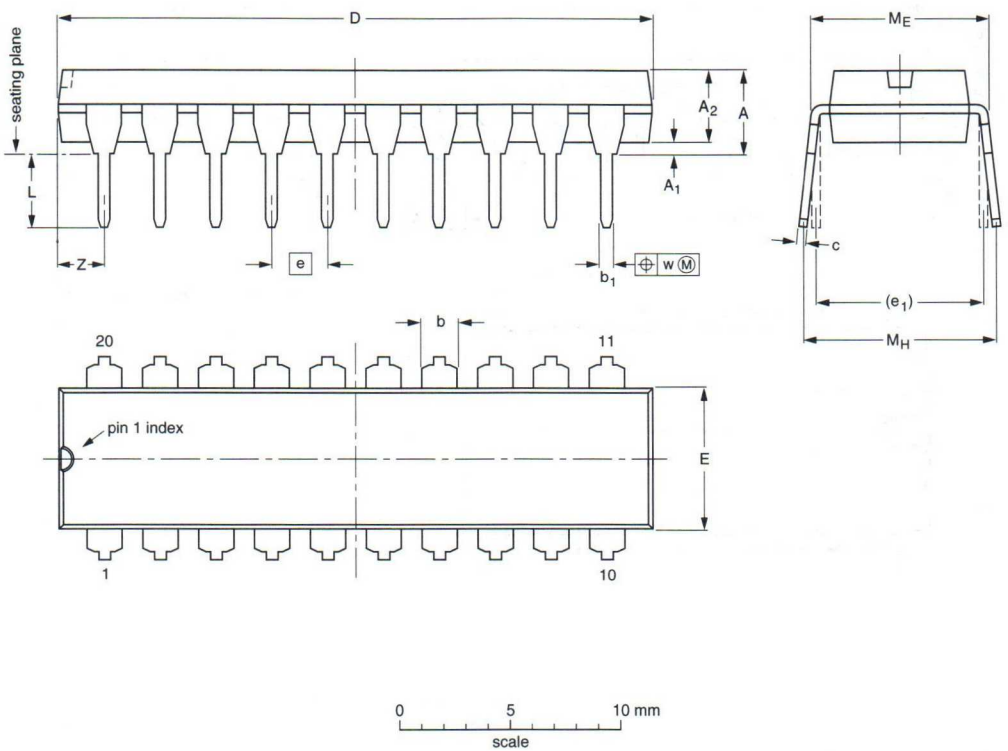
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	1.40 1.14	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	0.85
inches	0.19	0.020	0.15	0.055 0.044	0.021 0.015	0.055 0.044	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.033

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT102-1						~~93-10-14~~ 95-01-23

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

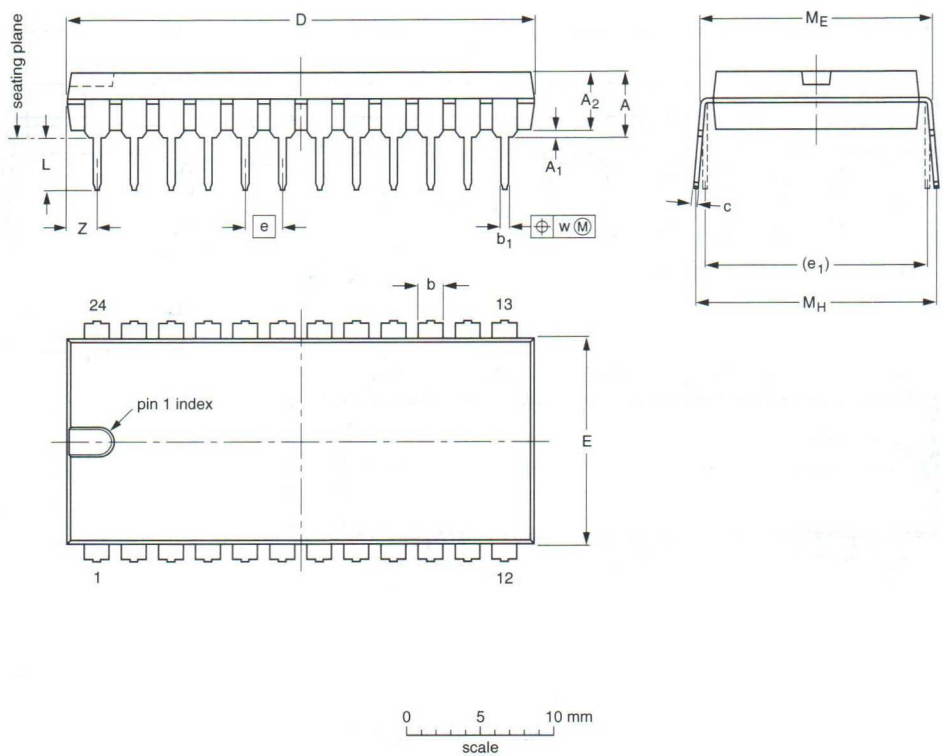
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

DIP24: plastic dual in-line package; 24 leads (600 mil) **SOT101-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

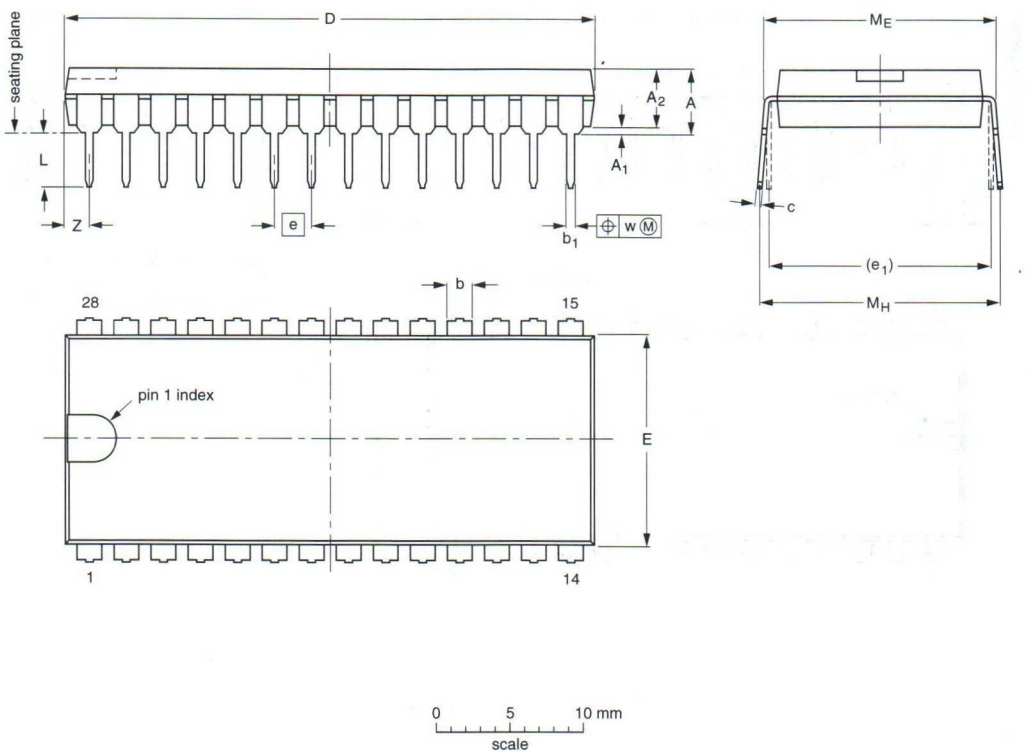
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

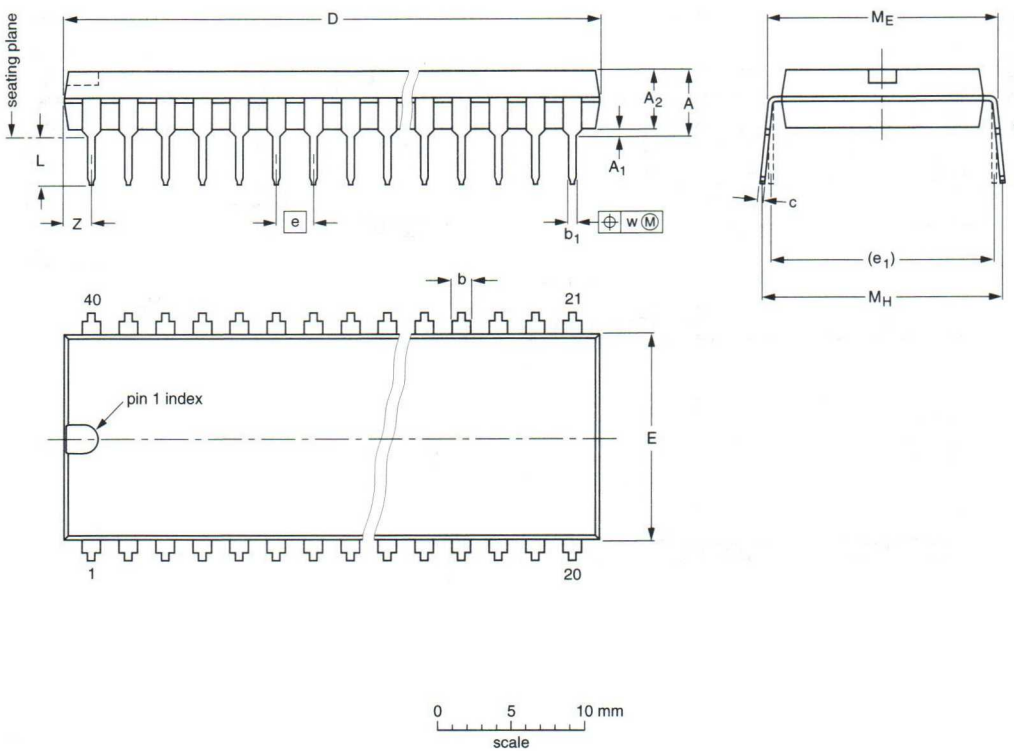
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

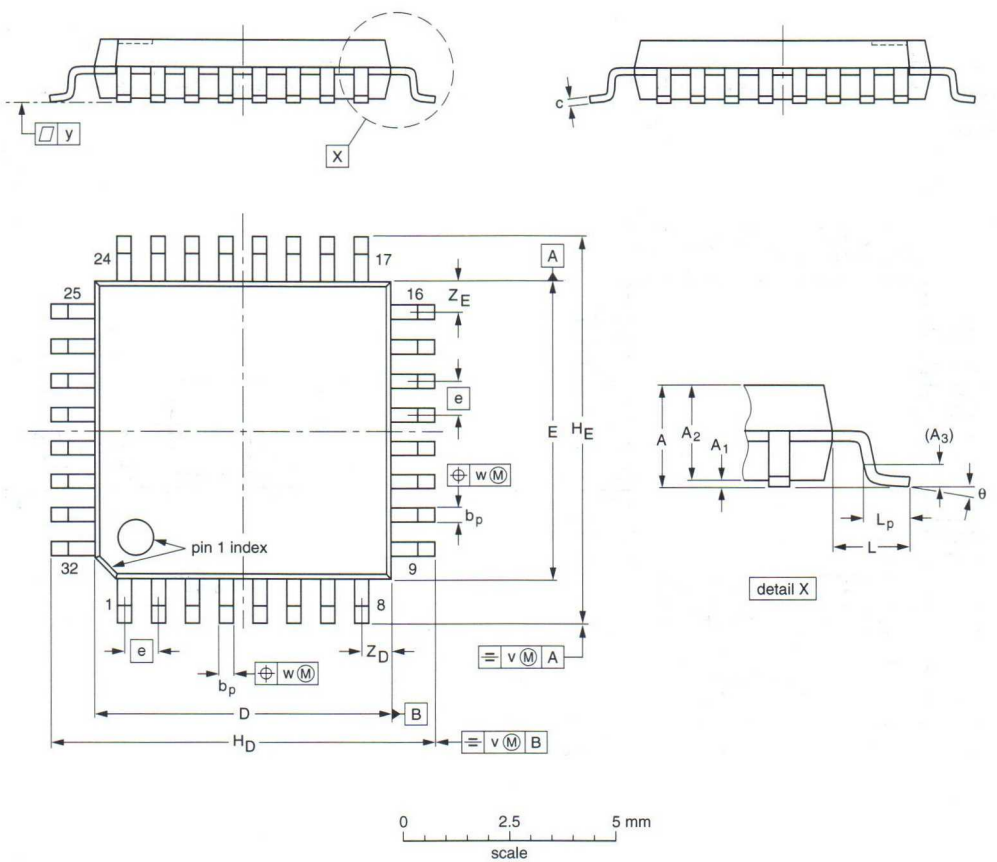
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

LQFP

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm SOT358-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7° 0°

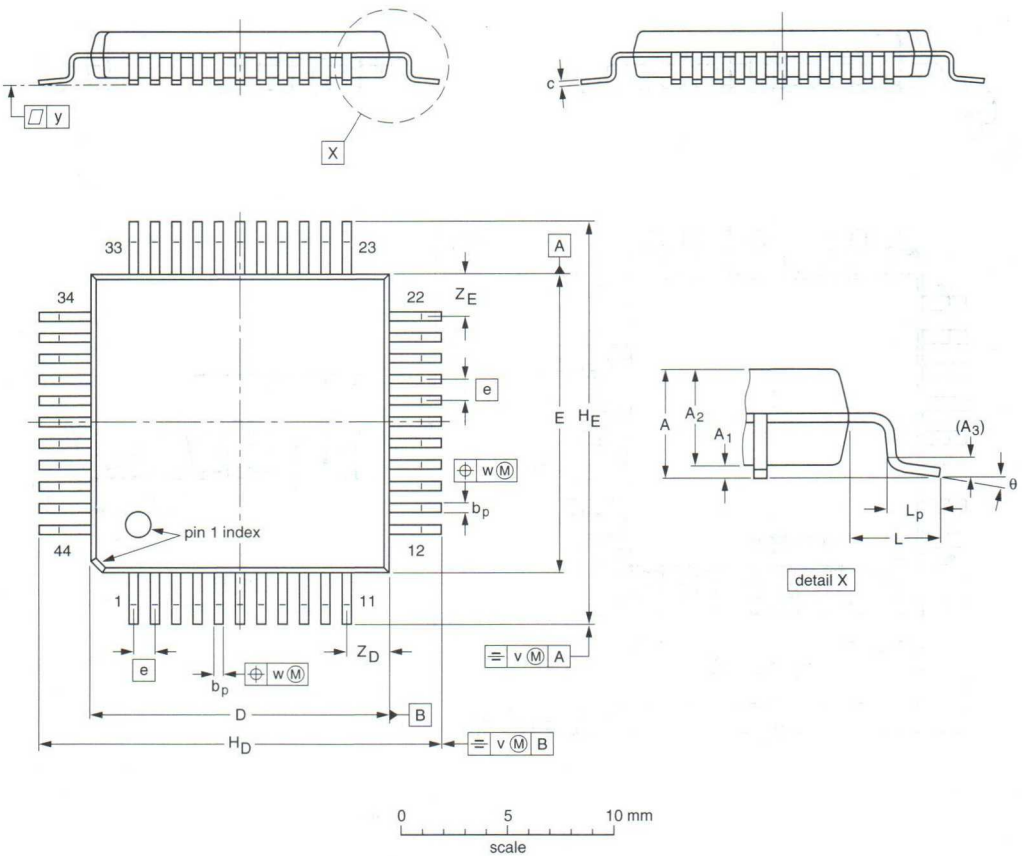
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT358 -1						~~95-12-19~~ 97-08-04

QFP

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm SOT205-1



DIMENSIONS (mm are the original dimensions)

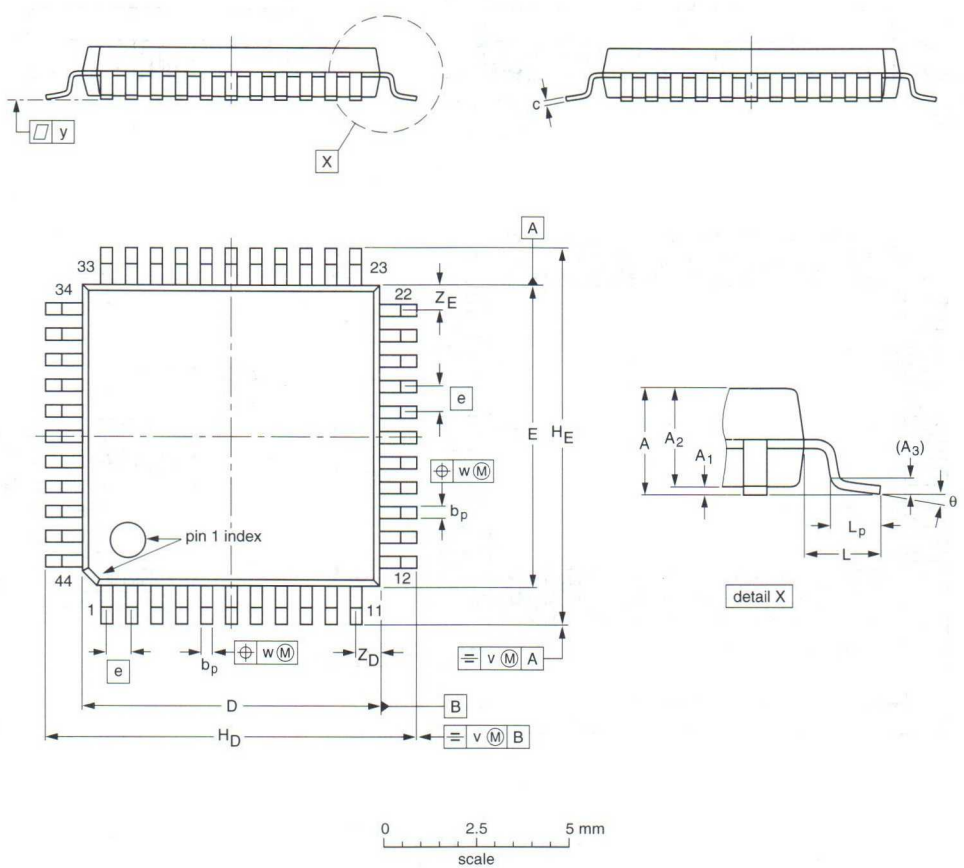
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT205-1	133E01A					~~95-02-04~~ 97-08-01

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

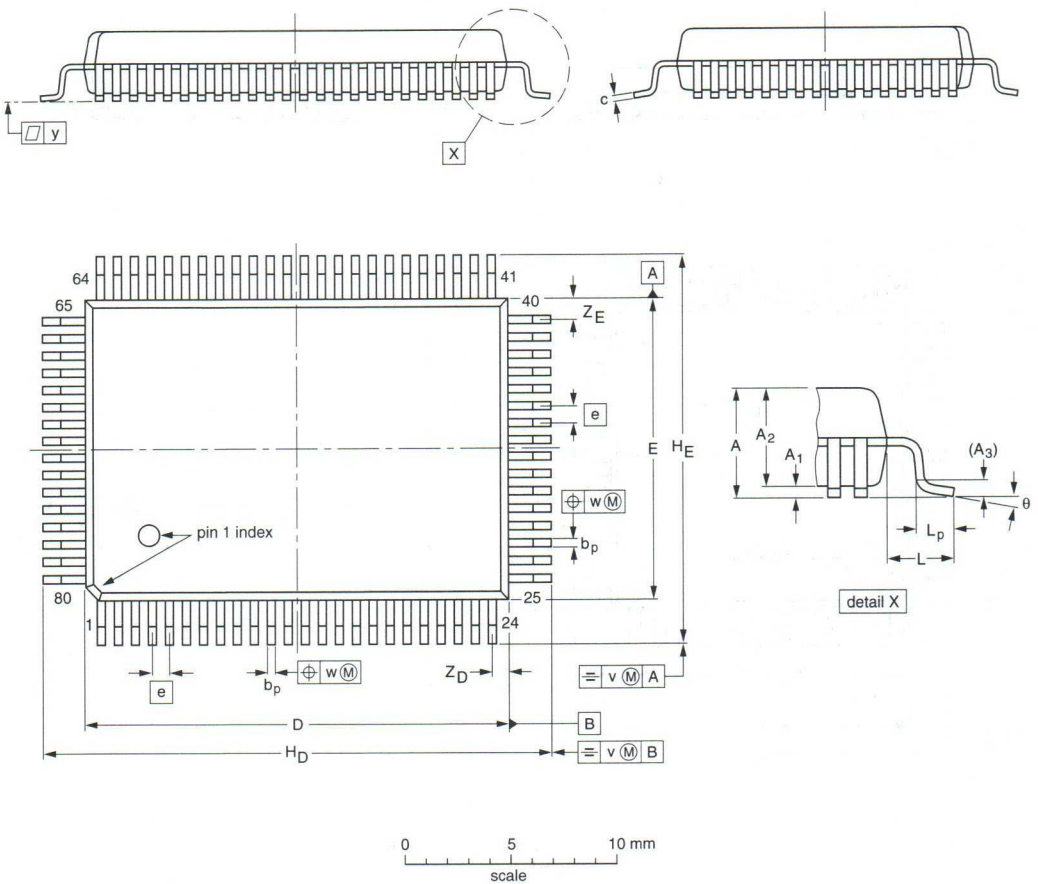
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~95-02-04~~ 97-08-01

QFP80: plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT318-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.2	0.25 0.05	2.90 2.65	0.25	0.45 0.30	0.25 0.14	20.1 19.9	14.1 13.9	0.8	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7° 0°

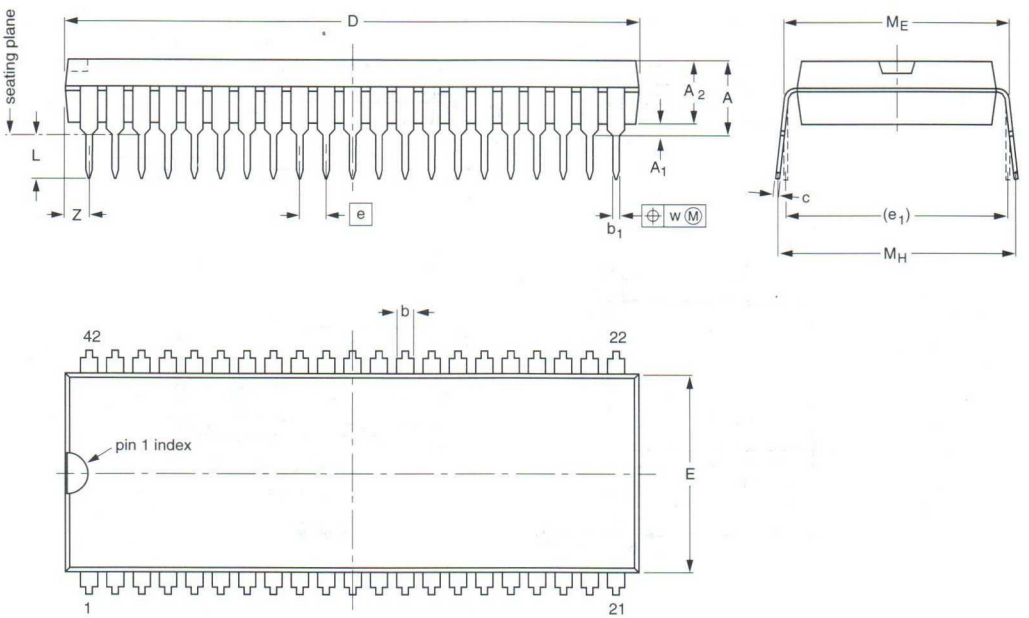
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-2						~~95-02-04~~ 97-08-01

SDIP

SDIP42: plastic shrink dual in-line package; 42 leads (600 mil) SOT270-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	38.9 38.4	14.0 13.7	1.778	15.24	3.2 2.9	15.80 15.24	17.15 15.90	0.18	1.73

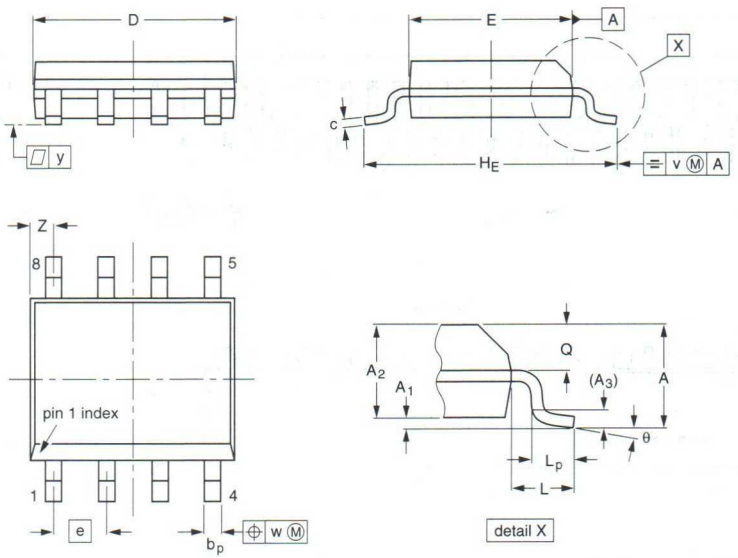
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT270-1						~~90-02-13~~ 95-02-04

SO

SO8: plastic small outline package; 8 leads; body width 3.9 mm SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

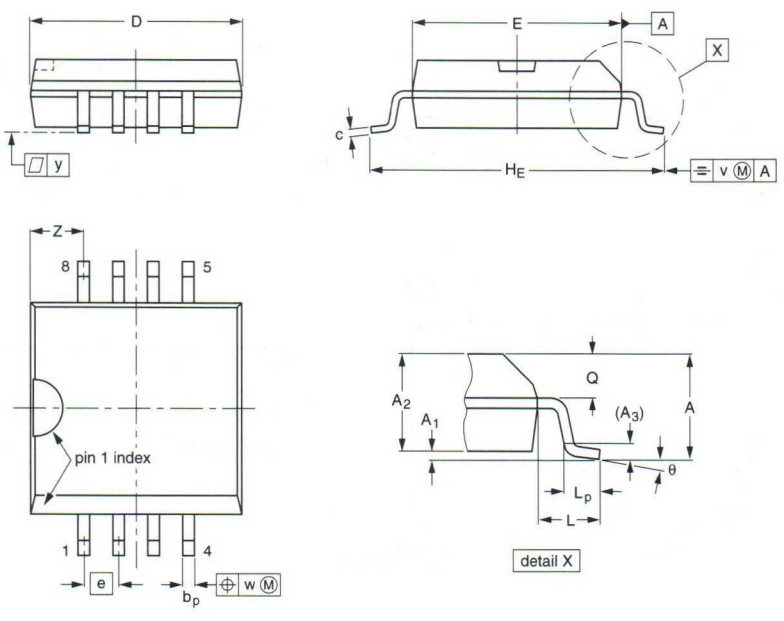
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

SO8: plastic small outline package; 8 leads; body width 7.5 mm **SOT176-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

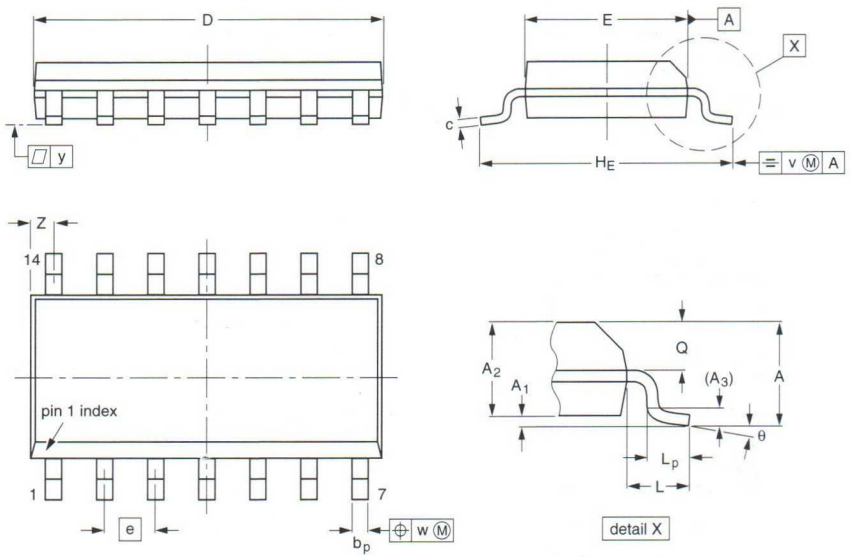
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	7.65 7.45	7.6 7.4	1.27	10.65 10.00	1.45	1.1 0.45	1.1 1.0	0.25	0.25	0.1	2.0 1.8	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.30 0.29	0.30 0.29	0.050	0.419 0.394	0.057	0.043 0.018	0.043 0.039	0.01	0.01	0.004	0.079 0.071	

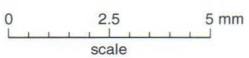
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT176-1						~~95-02-25~~ 97-05-22

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

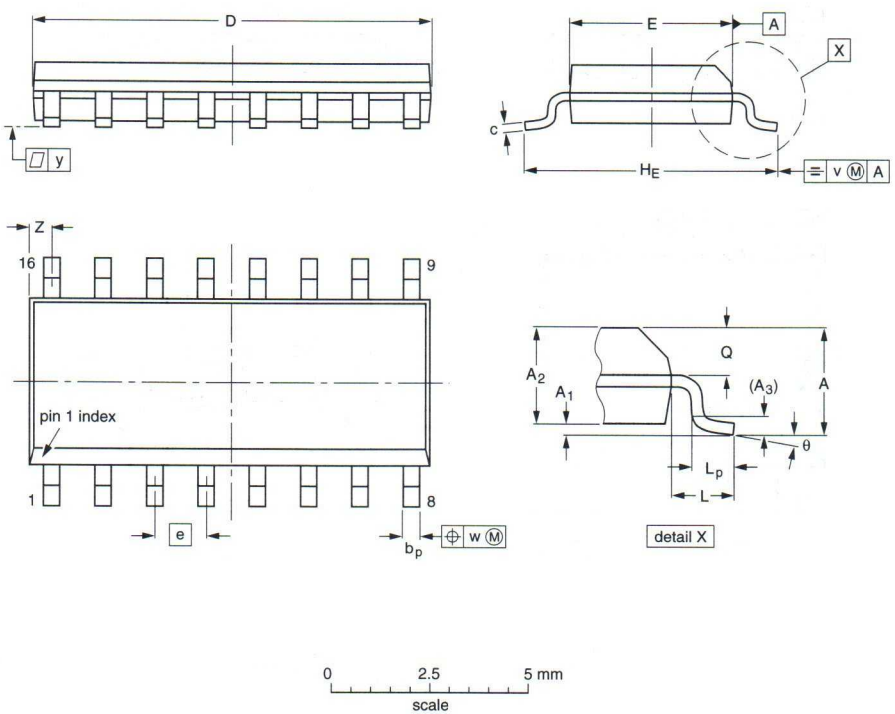
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~95-01-23~~ 97-05-22

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

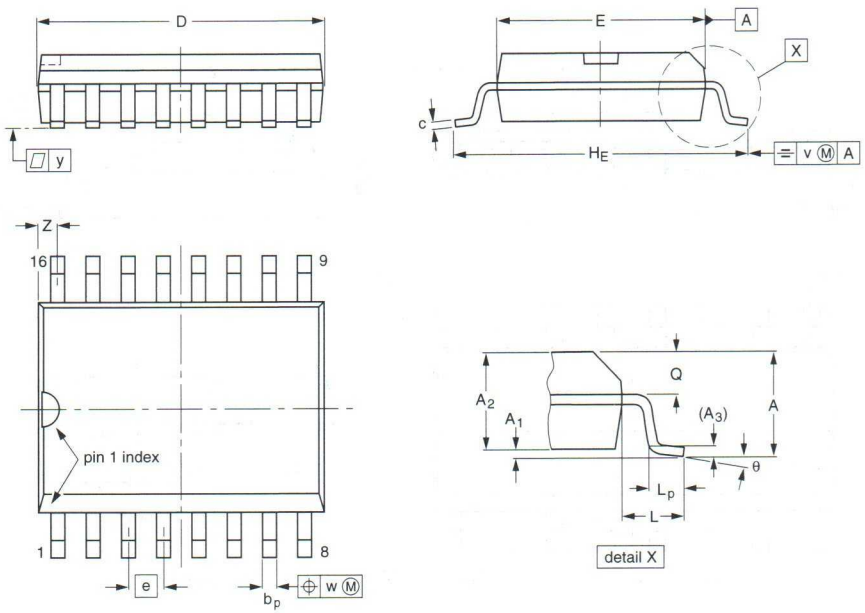
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

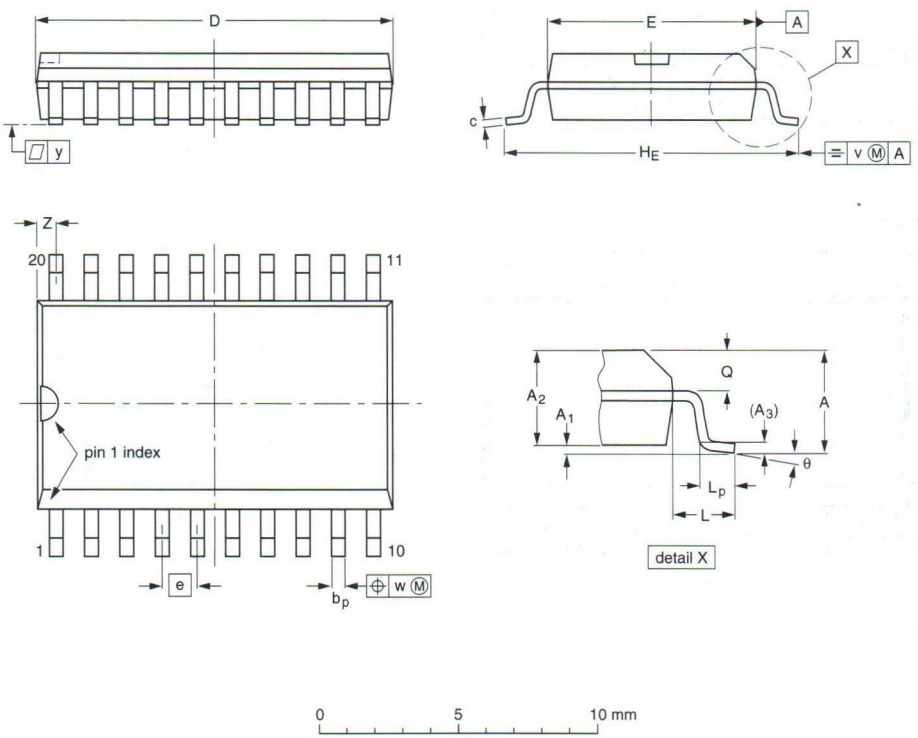
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~95-01-24~~ 97-05-22

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

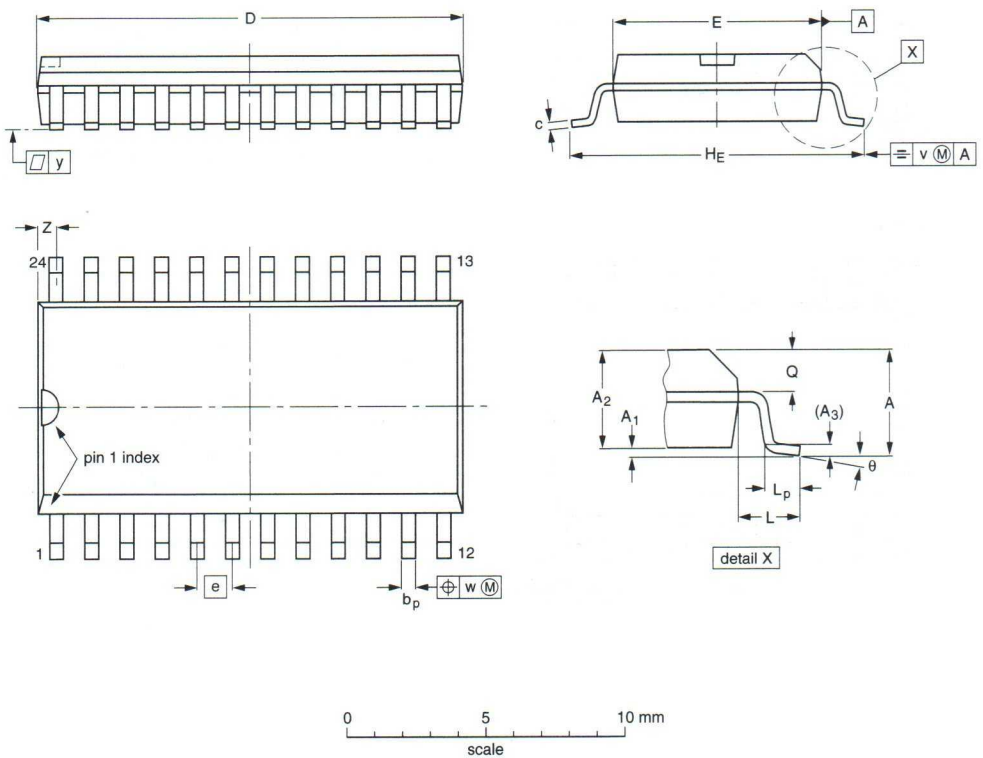
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

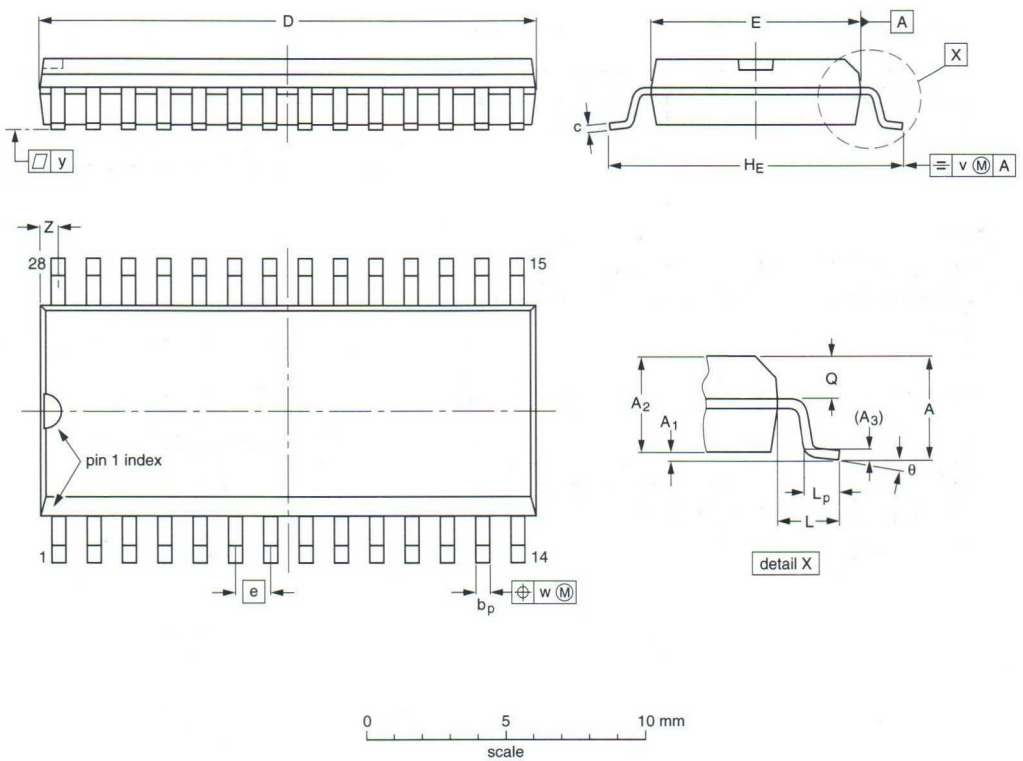
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

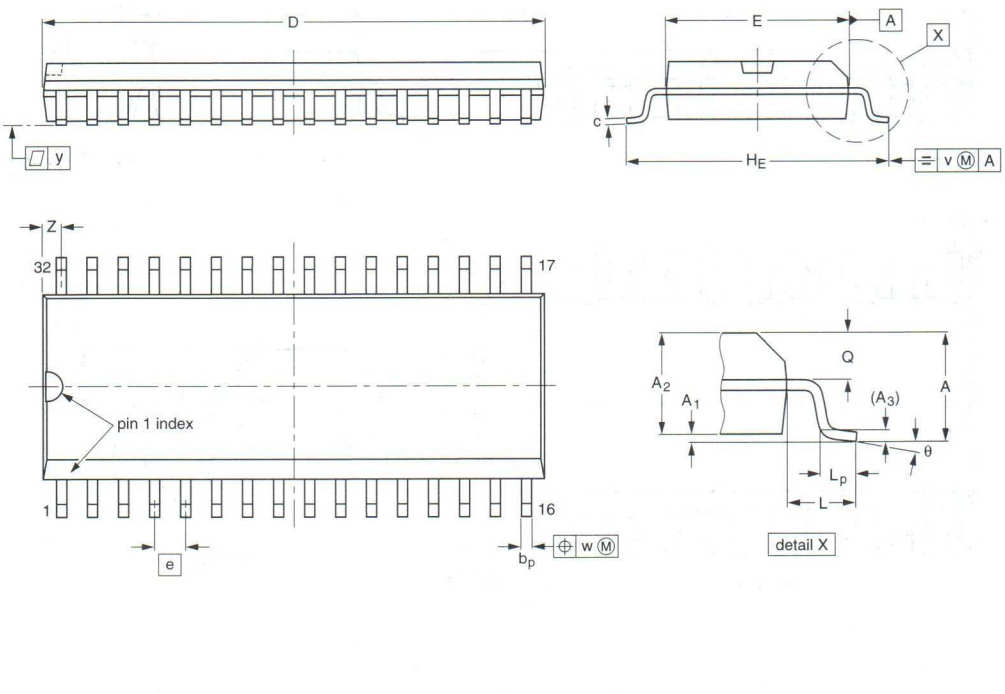
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

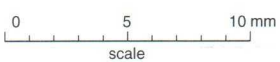
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

SO32: plastic small outline package; 32 leads; body width 7.5 mm SOT287-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8° 0°
inches	0.10	0.012 0.004	0.096 0.086	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

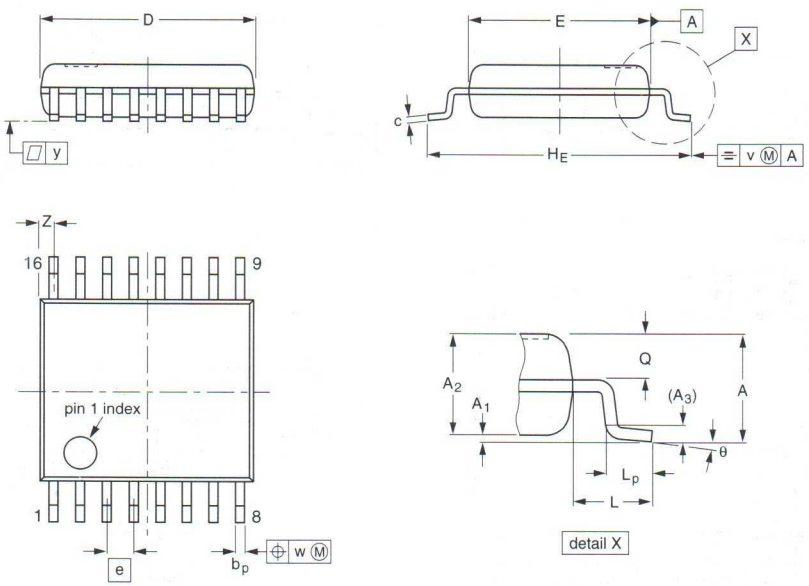
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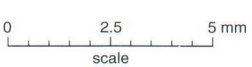
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
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SOT287-1						~~95-01-25~~ 97-05-22

SSOP

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm SOT369-1





DIMENSIONS (mm are the original dimensions)

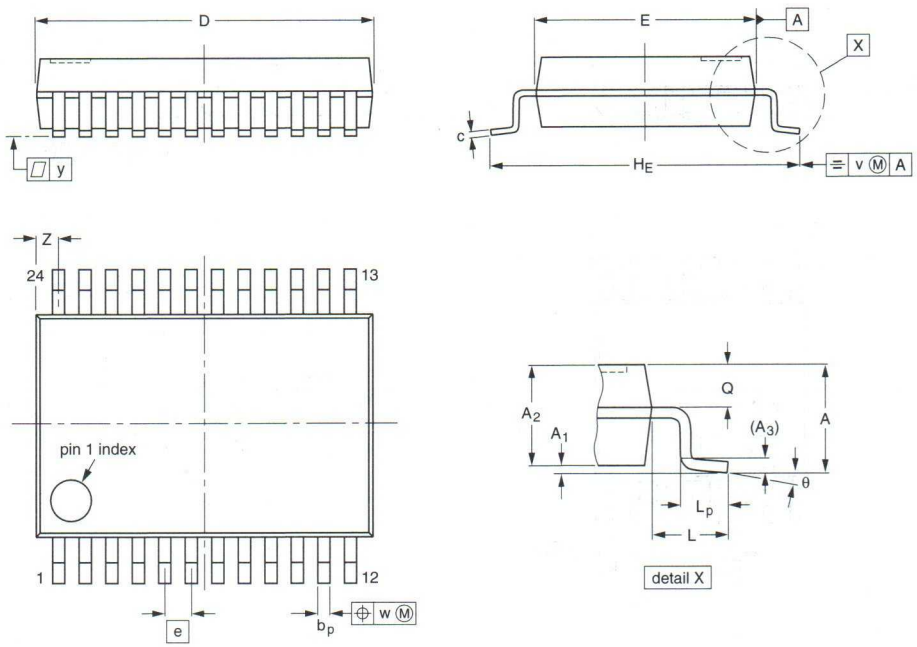
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

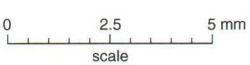
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1						~~94-04-20~~ 95-02-04

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**





DIMENSIONS (mm are the original dimensions)

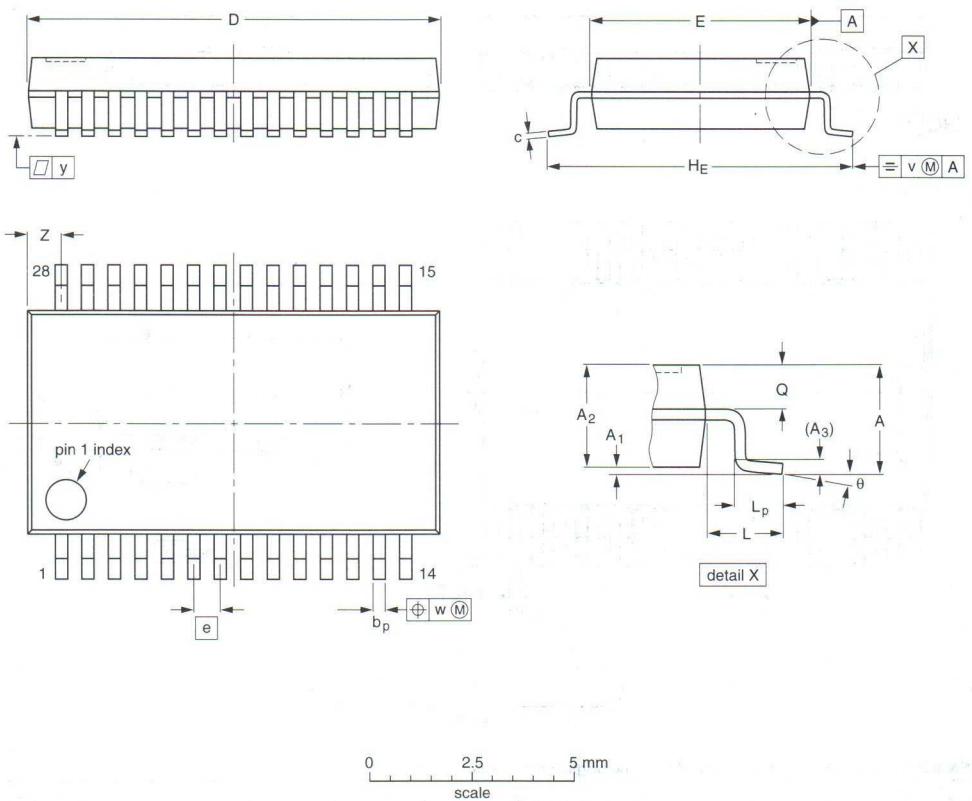
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

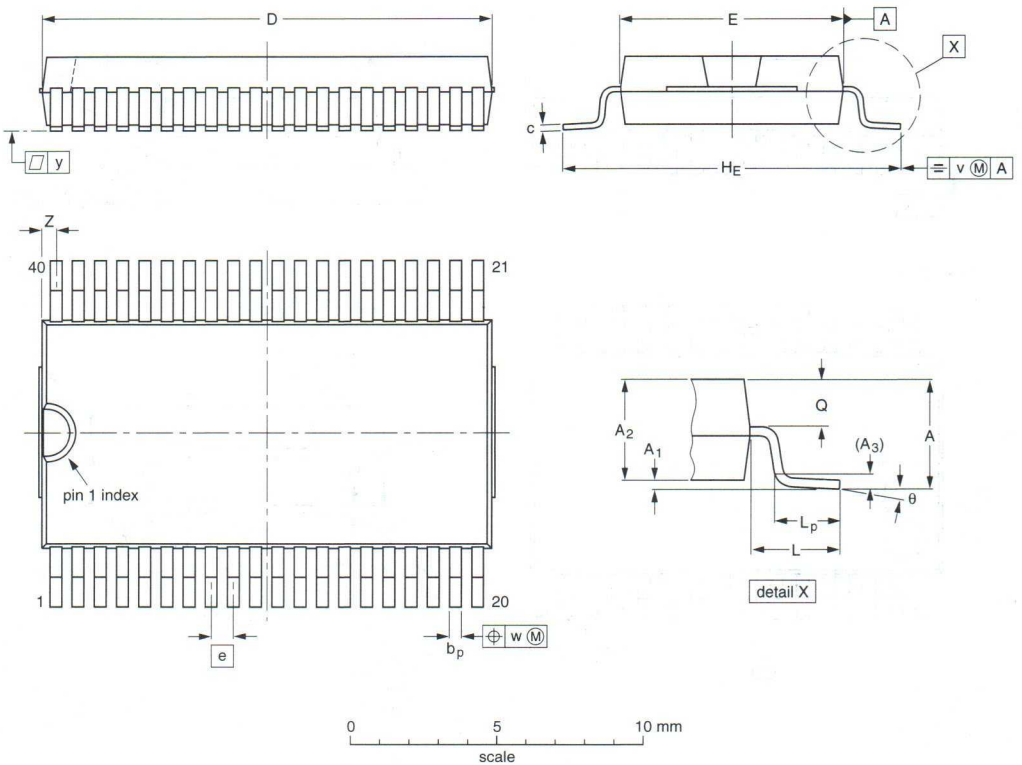
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

VSO

VSO40: plastic very small outline package; 40 leads SOT158-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.70	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7° 0°
inches	0.11	0.012 0.004	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

Notes

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT158-1						~~92-11-17~~ 95-01-24

INTRODUCTION

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9397 750 0011).

THROUGH-HOLE MOUNTED PACKAGES

Table 1 Types of through-hole mounted packages

TYPE	DESCRIPTION
DIP	plastic dual in-line package
SDIP	plastic shrink dual in-line package
HDIP	plastic heat-dissipating dual in-line package
DBS	plastic dual in-line bent from a single in-line package
SIL	plastic single in-line package

Soldering by dipping or wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SURFACE MOUNTED PACKAGES

Table 2 Types of surface mounted packages

TYPE	DESCRIPTION
SO	plastic small outline package
SSOP	plastic shrink small outline package
TSSOP	plastic thin shrink small outline package
VSO	plastic very small outline package
QFP	plastic quad flat package
LQFP	plastic low profile quad flat package
SQFP	plastic shrink quad flat package
TQFP	plastic thin quad flat package
PLCC	plastic leaded chip carrier

Reflow soldering

Reflow soldering techniques are suitable for all SMD packages, ease of soldering varies with the type of package as indicated in Table 3.

The choice of heating method may be influenced by larger plastic packages (QFP or PLCC with 44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information on moisture prevention, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Table 3 Suitability of surface mounted packages for various soldering methods: rating from 'a' to 'd': **'a' indicates most suitable** (soldering is not difficult); **'d' indicates least suitable** (soldering is achievable with difficulty).

PACKAGE TYPE	REFLOW METHOD					DOUBLE WAVE METHOD
	INFRARED	HOT BELT	HOT GAS	VAPOUR PHASE	RESISTANCE	
SO	a	a	a	a	d	a
SSOP	a	a	a	c	d	c
TSSOP	b	b	b	c	d	d
VSO	b	b	a	b	a	b
QFP	b	b	a	c	a	c
LQFP	b	b	a	c	d	d
SQFP	b	b	a	c	d	d
TQFP	b	b	a	c	d	d
PLCC	c	b	b	d	d	b

Wave soldering

Wave soldering is **not** recommended for SSOP, TSSOP, QFP, LQFP, SQFP or TQFP packages, this is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- For SSOP, TSSOP and VSO packages, the longitudinal axis of the package footprint must be parallel to the solder flow **and** must incorporate solder thieves at the downstream end.
- For QFP, LQFP and TQFP packages, the footprint must be at an angle of 45° to the board direction **and** must incorporate solder thieves downstream and at the side corners.

Even with these conditions, consider wave soldering only for the following package types:

- SO
- VSO
- PLCC
- SSOP **only with body width 4.4 mm**, e.g. SSOP16 (SOT369-1) or SSOP20 (SOT266-1).
- QFP **except** QFP52 (SOT379-1), QFP100 (SOT317-1, SOT317-2, SOT382-1) and QFP160 (SOT322-1); these are **not** suitable for wave soldering.
- LQFP **except** LQFP32 (SOT401-1), LQFP48 (SOT313-1, SOT313-2), LQFP64 (SOT314-2), LQFP80 (SOT315-1); these are **not** suitable for wave soldering.
- TQFP **except** TQFP64 (SOT357-1), TQFP80 (SOT375-1) and TQFP100 (SOT386-1); these are **not** suitable for wave soldering.

SQFP are **not** suitable for wave soldering.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DATA HANDBOOK SYSTEM

Data handbook system

DATA HANDBOOK SYSTEM

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