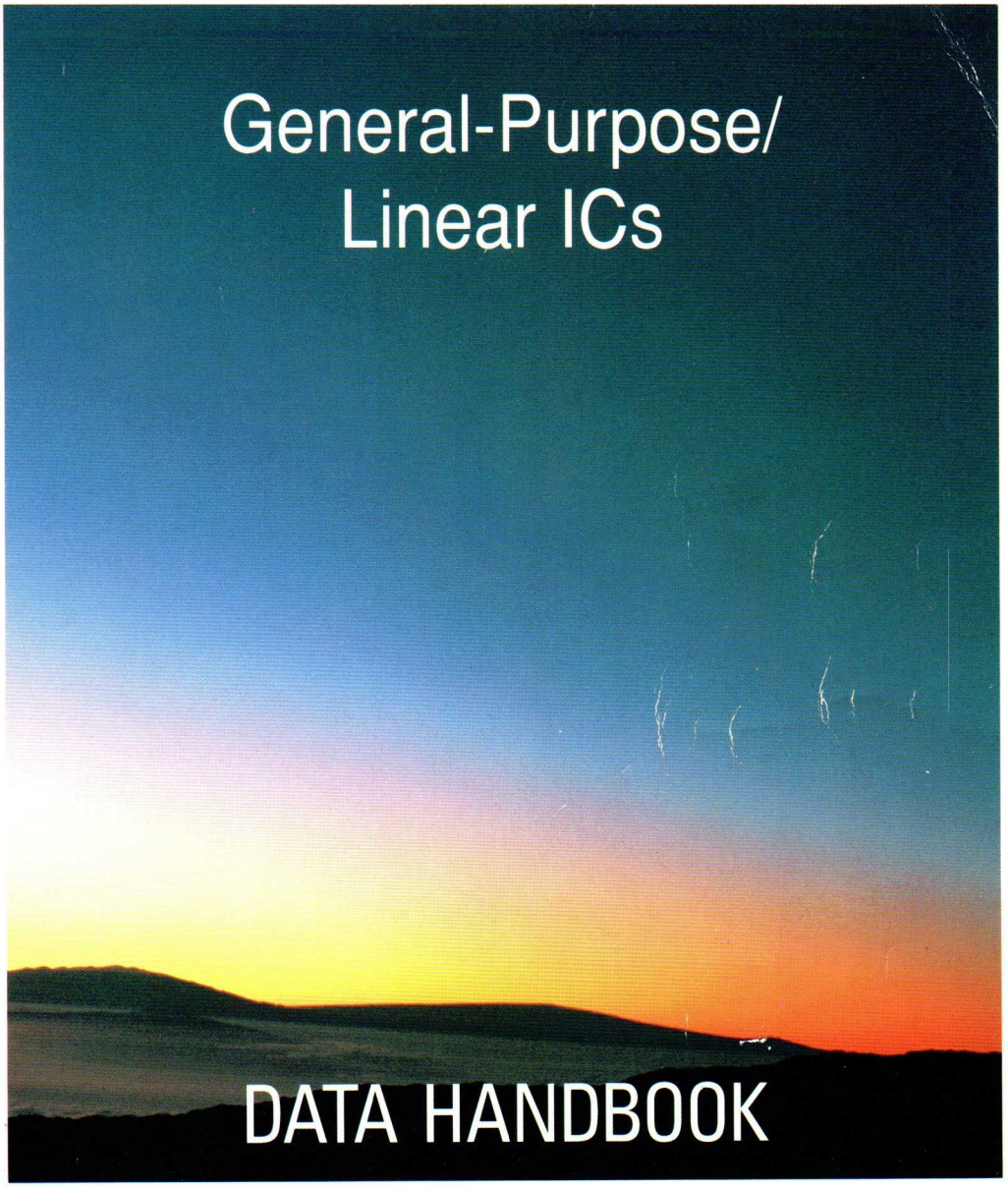
General-Purpose/ Linear ICs



DATA HANDBOOK

BOOK IIC111 1995

Philips Semiconductors

PHILIPS

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

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Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

General Purpose/Linear ICs

CONTENTS

		page
SECTION 1	GENERAL INFORMATION	5
SECTION 2	OPERATIONAL AMPLIFIERS	19
SECTION 3	HI FREQUENCY/VIDEO AMPLIFIERS	179
SECTION 4	COMPARATORS	269
SECTION 5	TIMERS	335
SECTION 6	PHASE-LOCKED LOOPS/FUNCTION GENERATORS	387
SECTION 7	LINE DRIVERS/RECEIVERS, MODEMS	465
SECTION 8	RELAY/PERIPHERAL DRIVERS	509
SECTION 9	DISPLAY DRIVERS	529
SECTION 10	ANALOG-TO-DIGITAL CONVERTERS	553
SECTION 11	DIGITAL-TO-ANALOG CONVERTERS	709
SECTION 12	SAMPLE-AND-HOLD	875
SECTION 13	POSITION MEASUREMENT	899
SECTION 14	BATTERY MANAGEMENT/DC VOLTAGE DETECTION AND CONTROL CIRCUITS	919
SECTION 15	SWITCHED MODE POWER SUPPLY CIRCUITS/TRIGGER CIRCUITS	1021
SECTION 16	MOTOR CONTROL CIRCUITS	1149
SECTION 17	LINE DRIVERS/MODEMS	1259
SECTION 18	PACKAGE OUTLINES	1279
SECTION 19	NORTH AMERICAN SALES OFFICES, REPRESENTATIVES AND DISTRIBUTORS	1323
APPENDIX A	DATA HANDBOOK SYSTEM	1326

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Preface

General Purpose/Linear ICs

Thank you for your interest in General Purpose/Linear IC products from Philips Semiconductors. As a leading supplier to the electronics market, we offer a wide range of linear semiconductor components.

This General Purpose/Linear IC handbook includes information on the current range of General Purpose/Linear products from Philips Semiconductors. The products are used in a wide range of consumer and industrial applications.

This book is one of many data books available from Philips Semiconductors, each one covering a different range of product lines.

For a complete listing of available data books, please refer to the back of this book. For additional information regarding these or any of our other products, please contact your local Philips Semiconductors sales office, also listed in the back of this book.

Section 1
General information

CONTENTS

Functional Index 7
Alphanumeric product list 12
Product Status 15
Ordering information 16
Comparator selector guide 17

Functional Index

General-Purpose/Linear ICs

Preface 3

Section 1 General Information 5

Alphanumeric product list 12
Product status 15
Ordering information 16
Comparator selector guide 17

Section 2 Operational Amplifiers 19

AN165 Integrated operational amplifier theory 21
AN166 Basic feedback theory 31
LM124/224/324/324A/ SA534/LM2902 Low power quad op amps 35
AU2902 Low power quad operational amplifier 42
µA741/µA741C/ SA741C General purpose operational amplifier 47
µA747C Dual operational amplifier 54
MC/SA1458/MC1558 General purpose operational amplifier 59
NE/SA/SE4558 Dual general-purpose operational amplifier 65
NE/SE531 High slew rate operational amplifier 70
NE/SA/SE5512 Dual high-performance operational amplifier 78
NE/SE5514 Quad high-performance operational amplifier 82
AN144 Applications for the NE/SA/SE5512 85
AN1441 Applications for the NE5514 89
NE5517/5517A Dual operational transconductance amplifier 92
AN145 NE5517/A transconductance amplifier applications 105
NE/SE5532/5532A Internally-compensated dual low noise operational amplifier 109
NE5533/5533A/ NE/SA/SE5534/5534A Dual and single low noise op amp 114
AN142 Audio circuits using the NE5532/3/4 122
NE/SA5230 Low voltage operational amplifier 133
AN1511 Low-voltage gated function generator: NE5230 146
NE/SA/SE532/ LM158/258/358/A/2904 Low power dual operational amplifiers 148
AU2904 Low power dual operational amplifier 154
NE/SA5234 Matched quad high-performance low-voltage operational amplifier 159
AN1651 Using the NE/SA5234 amplifier 163

Section 3 Comparators 179

NE/SA5204A Wide-band high-frequency amplifier 181
NE/SA/SE5205A Wide-band high-frequency amplifier 192
NE/SA5209 Wideband variable gain amplifier 202
NE/SA5219 Wideband variable gain amplifier 216
NE/SE5539 High frequency operational amplifier 229
AN140 Compensation techniques for use with the NE/SE5539 237
NE5592 Video amplifier 245
NE592 Video amplifier 250
AN141 Using the NE/SA/SE592 video amplifier 258
µA733/733C Differential video amplifier 262

Section 4 Comparators **269**

Comparator selector guide 271

Symbols and definitions for comparators 272

LM111/211/311/LM311B Voltage comparator 273

LM219/319 Dual voltage comparator 277

LM139/239/239A/339/339A/LM2901/MC3302 Quad voltage comparator 282

AU2901 Quad voltage comparator 289

LM193/A/293/A/393/A/2903 Low power dual voltage comparator 294

AU2903 Low power dual voltage comparator 300

NE/SE521 High-speed dual-differential comparator/sense amp 305

NE522 High-speed dual-differential comparator/sense amp 310

NE527 Voltage comparator 315

NE529 Voltage comparator 320

AN116 Applications for the NE521/522/527/529 325

Section 5 Timers **335**

ICM7555 General purpose CMOS timer 337

NE/SA/SE555/SE555C Timer 346

NE/SA/SE556/NE556-1 Dual timer 353

AN170 NE555 and NE556 applications 358

NE558 Quad timer 378

AN171 NE558 applications 382

Section 6 High Frequency Phase-Locked Loops / Function Generators **387**

NE/SE564 Phase-locked loop 389

NE/SE566 Function generator 398

NE/SE567 Tone decoder/phase-locked loop 403

NE/SA568A 150MHz phase-locked loop 416

AN177 An overview of the phase-locked loop (PLL) 423

AN178 Modeling the PLL 428

AN179 Circuit description of the NE564 442

AN180 Frequency synthesis with the NE564 448

AN1801 10.8MHz FSK decoder with NE564 450

AN181 A 6MHz FSK converter design example for the NE564 453

AN182 Clock regenerator with crystal-controlled phase-locked loop VCO (NE564) 455

Section 7 Line Drivers/Receiver, Modems **465**

MC145406 EIA-232-D/V.28 driver/receiver 467

NE5170 Octal line driver 472

NE5180/NE5181 Octal differential line receiver 478

AM26LS31 Quad high-speed differential line driver 483

AM26LS32/AM26LS33 Quad high-speed differential line receivers 488

NE5080 High-speed FSK modem transmitter 491

NE5081 High-speed FSK modem receiver 496

AN195 Applications using the NE5080, NE5081 499

AN1950 Application of NE5080 and NE5081 with frequency deviation reduction 506

Section 8 Relay/Peripheral Drivers **509**

Symbols and definitions for peripheral and display drivers 510

NE/SA5090 Addressable relay driver 513

NE590/591 Addressable peripheral drivers 519

Section 9 Display Drivers **529**

NE587 LED decoder/driver 531
NE/SA594 Vacuum fluorescent display driver 540
AN112 LED decoder drivers: using the NE587 546

Section 10 Analog-to-Digital Converters **553**

ADC0803/4-1 CMOS 8-bit A/D converters 555
ADC0820 8-Bit, high-speed, µP-compatible A/D converter with track/hold function 568
NE5037 6-Bit A/D converter (parallel outputs) 582
PCF8591 8-Bit A/D and D/A converter 590
TDA8703 8-bit high-speed analog-to-digital converter 607
TDA8706 6-Bit analog-to-digital converter with multiplexer and clamp 620
TDA1534 14-bit analog-to-digital converter 630
TDA8708A Video analog input interface 637
TDA8709A Video analog input interface 654
TDA8713 8-bit high-speed analog-to-digital converter 673
TDA8715 8-bit high-speed analog-to-digital converter 686
TDE8715D 8-bit high-speed analog-to-digital converter (Mil. temp.) 696

Section 11 Digital-to-Analog Converters **709**

AN100 An overview of data converters 711
DAC08 Series 8-Bit high-speed multiplying D/A converter 716
AN101 Applying the DAC08 728
AN105 Digital attenuator 735
MC1508-8/ 1408-8 8-bit multiplying D/A converter 737
MC3410, MC3410C 10-Bit high-speed multiplying D/A converter 743
NE/SE5018/ 5019 8-Bit µp-compatible D/A converter 751
NE5020 10-Bit µP-compatible D/A converter 757
NE/SE5410 10-Bit high-speed multiplying D/A converter 767
AM6012 12-Bit multiplying D/A converter 776
TDA1541A Stereo high-performance 16-bit DAC 787
TDA1543 Dual 16-bit DAC (economy version) (I^2S input format) 796
TDA1543A Dual 16-bit DAC (economy version) (Japanese input format) 805
TDA1545A Stereo continuous calibration DAC 813
TDA1547 Dual top-performance bitstream DAC 825
TDA8444/ AT/T Octuple 6-bit DAC with I^2C-bus 839
TDA8702 8-bit video digital-to-analog converter 848
TDE8712D 8-bit video digital-to-analog converter (Mil. temp.) 862

Section 12 Sample-and-Hold **875**

Symbols and definitions for sample-and-hold circuits 877
LF198/LF298/ LF398 Sample-and-hold amplifiers 879
NE/SE5537 Sample-and-hold amplifier 884
TDA1535B High-speed single sample-and-hold amplifier 892

Section 13 Position Measurement **899**

NE/SA/ SE5521 LVDT signal conditioner 901
AN1182 Using the NE5521 signal conditioner in multi-faceted applications 906

Section 14 Battery Management/DC Voltage Detection and Control Circuits **919**

SAA1500T State-of-charge indicator for NiMH and NiCd powered applications 921
TEA1041T Battery low-level indicator 938
TEA1088T Switched-mode power supply battery charger control circuit 946
TEA1100; TEA1100T Battery monitor for NiCd and NiMH chargers 959

Section 14 (Continued)

TEA1101; TEA1101T	Battery monitor for NiCd and NiMH chargers	972
TEA5500 TEA5500T	Coded locking circuit for security systems	986
TEA5501	Coded locking circuit for security systems (one-shot output; 6.5k codes)	995
74LV4799	Timer for NiCd and NiMH chargers	1005

Section 15 Switched-Mode Power Supply Circuits/Trigger Circuits **1021**

AN120	An overview of switched-mode power supplies	1023
NE/SE5560	Switched-mode power supply control circuit	1028
NE/SE5561	Switched-mode power supply control circuit	1044
AN123	NE5561 applications	1049
AN124	External synchronization for the NE5561/5568	1054
NE/SE5562	Switched-mode power supply control circuit	1055
NE5568	Switched-mode power supply controller	1085
SG3524	SMPS control circuit	1087
AN126	Applications using the SG3524	1092
µA723/723C	Precision voltage regulator	1094
UC3842	Current-mode PWM controller	1100
TCA280B	General-purpose triggering circuit	1108
TDA8380	Control circuit for switched-mode power supplies	1120
TEA1039	Control circuit for switched-mode power supply	1137

Section 16 Motor control circuits **1149**

NE/SA5570	Brushless DC motor controller	1151
AN1281	NE5570: A theory of operation and applications	1156
TDA5140A	Brushless DC motor drive circuit	1169
TDA5141	Brushless DC motor drive circuit	1184
TDA5142T	Brushless DC motor drive circuit	1200
TDA5143T	Brushless DC motor drive circuit	1215
TDA5144	Brushless DC motor drive circuit	1229
TDA5145	Brushless DC motor drive circuit	1243

Section 17 Miscellaneous **1259**

NE5044	Programmable seven-channel RC encoder	1261
NE/SA630	Single pole double throw (SPDT) switch	1268

Section 18 Package outlines **1279**

0404B	8-Pin (300 mils wide) Plastic Dual In-Line (N) Package	1281
0174C	8-Pin (157 mils wide) Plastic SO (Small Outline) Dual In-Line (D) Package	1282
0580A	8-Pin (300 mils wide) Ceramic Dual In-line (F) Package	1283
0405B	14-PIn (300 mils wide) Plastic Dual In-Line (N) Package	1284
0175D	14-Pin (157 mils wide) Plastic SO (Small Outline) Dual In-Line (D) Package	1285
0581B	14-Pin (300 mils wide) Ceramic Dual In-line (F) Package	1286
SOT38Z/ 0406C	16-Pin (300 mils wide) Plastic Dual In-Line (N) Package	1287
0171B	16-Pin (300 mils wide) Plastic SOL (Small Outline Large) Dual In-Line (D) Package	1288
0005D	16-Pin (157 mils wide) Plastic SO (Small Outline) Dual In-Line (D) Package	1289
0582B	16-Pin (300 mils wide) Ceramic Dual In-line (F) Package	1290
0407A	18-Pin (300 mils wide) Plastic Dual In-Line (N) Package	1291
0583A	18-Pin (300 mils wide) Ceramic Dual In-line (F) Package	1292
0408B	20-Pin (300 mils wide) Plastic Dual In-Line (N) Package	1293
0172D	20-Pin (300 mils wide) Plastic SOL (Small Outline Large) Dual In-Line (D) Package	1294
0584B	20-Pin (300 mils wide) Ceramic Dual In-line (F) Package (with Window (FA) Package)	1295
0409B	22-Pin (400 mils wide) Plastic Dual In-Line (N) Package	1296
0585B	22-Pin (400 mils wide) Ceramic Dual In-line (F) Package	1297
SOT101/ 0410D	24-Pin (300 mils wide) Plastic Dual In-Line (N) Package	1298
0411B	24-Pin (400 mils wide) Plastic Dual In-Line (N) Package	1299

Section 17 Package outlines (cont.)

0412A	24-Pin (600 mils wide) Plastic Dual In-Line (N) Package	1300
0173D	24-Pin (300 mils wide) Plastic SOL (Small Outline Large) Dual In-Line (D) Package	1301
0586B	24-Pin (300 mils wide) Ceramic Dual In-line (F) Package (with Window (FA) Package)	1302
0587D	24-Pin (400 mils wide) Ceramic Dual In-line (F) Package	1303
0588B	24-Pin (600 mils wide) Ceramic Dual In-line (F) Package (with Window (FA) Package)	1304
0864D	28-Pin (300 mils wide) Plastic Dual In-Line (N) Package	1305
0413B	28-pin (600 mils wide) Plastic Dual In-Line (N) Package	1306
SOT261/ 0401F	28-Pin (300 mils wide) Plastic Leaded Chip Carrier (A) Package	1307
SOT97-1	Plastic dual in-line package; 8 leads	1308
SOT96-1	Plastic small outline package; 8 leads	1309
SOT110B	9-Pin Plastic Single In-Line (U) Package	1310
SOT162-1	Plastic small outline package; 16 leads; large body	1311
SOT38-1	Plastic dual in-line package; 16 leads (300 mil)	1312
SOT74	16-Pin Ceramic Dual In-Line (F) Package	1313
SOT102	18-Pin Plastic Dual In-Line (N/P) Package with Internal Heatspreader	1314
SOT146-1	Plastic dual in-line package; 20 leads (300 mil)	1315
SOT163-1	Plastic small outline package; 20 leads; large body (SO20L)	1316
SOT101	24-Pin Plastic Dual In-Line (N/P) Package with Internal Heatspreader	1317
SOT137-1	Plastic small outline package; 24 leads; large body	1318
SOT117-1	Plastic dual in-line package; 28 leads (600 mil) with internal heat spreader	1319
SOT136–1	Plastic small outline package; 28 leads; large body	1320
SOT232-1	Plastic shrink dual in-line package; 32 leads (400 mil)	1321

Sales Offices, Representatives and Distributors 1323

Appendix A
Data handbook system 1326

Alphanumeric product list

General-Purpose/Linear ICs

LM124/224/324/324A/ SA534/LM2902	Low power quad op amps	34
AU2902	Low power quad operational amplifier	41
µA741/µA741C/ SA741C	General purpose operational amplifier	46
µA747C	Dual operational amplifier	53
MC/SA1458/MC1558	General purpose operational amplifier	58
NE/SA/SE4558	Dual general-purpose operational amplifier	64
NE/SE531	High slew rate operational amplifier	69
NE/SA/SE5512	Dual high-performance operational amplifier	77
NE/SE5514	Quad high-performance operational amplifier	81
NE5517/5517A	Dual operational transconductance amplifier	91
NE/SE5532/5532A	Internally-compensated dual low noise operational amplifier	108
NE5533/5533A/ NE/SA/SE5534/5534A	Dual and single low noise op amp	113
NE/SA5230	Low voltage operational amplifier	132
NE/SA/SE532/ LM158/258/358/A/2904	Low power dual operational amplifiers	147
AU2904	Low power dual operational amplifier	153
NE/SA5234	Matched quad high-performance low-voltage operational amplifier	158
NE/SA5204A	Wide-band high-frequency amplifier	181
NE/SA/SE5205A	Wide-band high-frequency amplifier	192
NE/SA5209	Wideband variable gain amplifier	202
NE/SA5219	Wideband variable gain amplifier	216
NE/SE5539	High frequency operational amplifier	229
NE5592	Video amplifier	245
NE592	Video amplifier	250
µA733/733C	Differential video amplifier	262
LM111/211/311/ LM311B	Voltage comparator	273
LM219/319	Dual voltage comparator	277
LM139/239/239A/ 339/339A/LM2901/ MC3302	Quad voltage comparator	282
AU2901	Quad voltage comparator	289
LM193/A/293/A/393/A/ 2903	Low power dual voltage comparator	294
AU2903	Low power dual voltage comparator	300
NE/SE521	High-speed dual-differential comparator/sense amp	305
NE522	High-speed dual-differential comparator/sense amp	310
NE527	Voltage comparator	315
NE529	Voltage comparator	320
ICM7555	General purpose CMOS timer	337
NE/SA/SE555/SE555C	Timer	346
NE/SA/SE556/ NE556-1	Dual timer	353
NE558	Quad timer	378
NE/SE564	Phase-locked loop	389
NE/SE566	Function generator	398
NE/SE567	Tone decoder/phase-locked loop	403
NE/SA568A	150MHz phase-locked loop	416

Alphanumeric product list

MC145406	EIA-232-D/V.28 driver/receiver	467
NE5170	Octal line driver	472
NE5180/NE5181	Octal differential line receiver	478
AM26LS31	Quad high-speed differential line driver	483
AM26LS32/AM26LS33	Quad high-speed differential line receivers	488
NE5050	Power line modem	491
NE5080	High-speed FSK modem transmitter	497
NE5081	High-speed FSK modem receiver	502
NE/SA5090	Addressable relay driver	549
NE590/591	Addressable peripheral drivers	555
NE587	LED decoder/driver	567
NE/SA594	Vacuum fluorescent display driver	576
ADC0803/4-1	CMOS 8-bit A/D converters	591
ADC0820	8-Bit, high-speed, mP-compatible A/D converter with track/hold function	604
NE5037	6-Bit A/D converter (parallel outputs)	618
PCF8591	8-Bit A/D and D/A converter	626
TDA8703	8-bit high-speed analog-to-digital converter	643
TDA8706	6-Bit analog-to-digital converter with multiplexer and clamp	656
TDA1534	14-bit analog-to-digital converter	666
TDA8708A	Video analog input interface	673
TDA8709A	Video analog input interface	690
TDA8713	8-bit high-speed analog-to-digital converter	709
TDA8715	8-bit high-speed analog-to-digital converter	722
TDE8715D	8-bit high-speed analog-to-digital converter (Mil. temp.)	732
DAC08 Series	8-Bit high-speed multiplying D/A converter	753
MC1508-8/1408-8	8-bit multiplying D/A converter	774
MC3410,MC3410C	10-Bit high-speed multiplying D/A converter	780
NE/SE5018/5019	8-Bit µp-compatible D/A converter	788
NE5020	10-Bit µP-compatible D/A converter	794
NE/SE5410	10-Bit high-speed multiplying D/A converter	804
AM6012	12-Bit multiplying D/A converter	813
TDA1541A	Stereo high-performance 16-bit DAC	824
TDA1543	Dual 16-bit DAC (economy version) (I^2S input format)	833
TDA1543A	Dual 16-bit DAC (economy version) (Japanese input format)	842
TDA1545A	Stereo continuous calibration DAC	850
TDA1547	Dual top-performance bitstream DAC	862
TDA8444/AT/T	Octuple 6-bit DAC with I^2C-bus	876
TDA8702	8-bit video digital-to-analog converter	885
TDE8712D	8-bit video digital-to-analog converter (Mil. temp.)	899
LF198/LF298/LF398	Sample-and-hold amplifiers	917
NE/SE5537	Sample-and-hold amplifier	922
TDA1535B	High-speed single sample-and-hold amplifier	930
NE/SA/SE5521	LVDT signal conditioner	939
SAA1500T	State-of-charge indicator for NiMH and NiCd powered applications	959
TEA1041T	Battery low-level indicator	976
TEA1088T	Switched-mode power supply battery charger control circuit	984
TEA1100;TEA1100T	Battery monitor for NiCd and NiMH chargers	997
TEA1101;TEA1101T	Battery monitor for NiCd and NiMH chargers	1010
TEA5500TEA5500T	Coded locking circuit for security systems	1024
TEA5501	Coded locking circuit for security systems (one-shot output; 6.5k codes)	1033
NE/SE5560	Switched-mode power supply control circuit	1051
NE/SE5561	Switched-mode power supply control circuit	1067
NE/SE5562	Switched-mode power supply control circuit	1078
NE5568	Switched-mode power supply controller	1108
SG3524	SMPS control circuit	1110
mA723/723C	Precision voltage regulator	1117
UC3842	Current-mode PWM controller	1123
TCA280B	General-purpose triggering circuit	1131
TDA8380	Control circuit for switched-mode power supplies	1143

Alphanumeric product list

TEA1039	Control circuit for switched-mode power supply	1160
NE/SA5570	Brushless DC motor controller	1174
TDA5140A	Brushless DC motor drive circuit	1192
TDA5141	Brushless DC motor drive circuit	1207
TDA5142T	Brushless DC motor drive circuit	1223
TDA5143T	Brushless DC motor drive circuit	1238
TDA5144	Brushless DC motor drive circuit	1252
TDA5145	Brushless DC motor drive circuit	1266
NE5044	Programmable seven-channel RC encoder	1283
NE/SA630	Single pole double throw (SPDT) switch	1290

Product Status

General Purpose/Linear ICs

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Ordering information

DATA COMMUNICATIONS CONTROLLERS

Example: S C N X X X X X C 6 N 4 8

- SC – Philips Designator
- Process/Power Variation
  - N = N – Channel
  - C = C – MOS
  - B = Bipolar
- Basic Part Number
  - See individual data sheets
- Temperature
  - C = 0°C to 70°C (Commercial)
  - A = –40°C to +80°C (Automotive)
  - M = –55°C to +125°C (Military)
  - P = –20°C to +70°C (Philips)
- Timing Variation

Spd	Sym	Spd	Sym	Spd	Sym
01	1	21	1	41	1
02	2	22	2	42	2
03	3	23	3	43	3
04	4	24	4	44	4
05	5	25	5	45	5
06	6	26	6	46	6
07	7	27	7	47	7
08	8	28	8	48	8
09	9	29	9	49	9
10	A	30	0	50	0
11	B	31	1	51	1
12	C	32	2	52	2
13	D	33	3	53	3
14	E	34	4	54	4
15	F	35	5	55	5
16	6	36	6	56	6
17	7	37	7	57	7
18	8	38	8	58	8
19	9	39	9		.
20	0	40	0		.

Unless otherwise noted.

- Package Code
  - A = Plastic Leaded Chip Carrier (PLCC)
  - N = Plastic Dual In-Line
  - F = Ceramic Dual In-Line
- Pin count
  - 14, 16, 20, 24, 28, 40, 48, etc.

FUTUREBUS+ PRODUCTS

Example: FB XXXX BB

- Designates Futurebus+ Product.
  - Temperature Range: 0°C to +70°C
- Device Number
- Package Code:
  - A = Plastic Leaded Chip Carrier (PLCC)
  - BB = Quad Flat Pack (QFP)

LINEAR AND RF PRODUCTS

Example: NE XXXX N

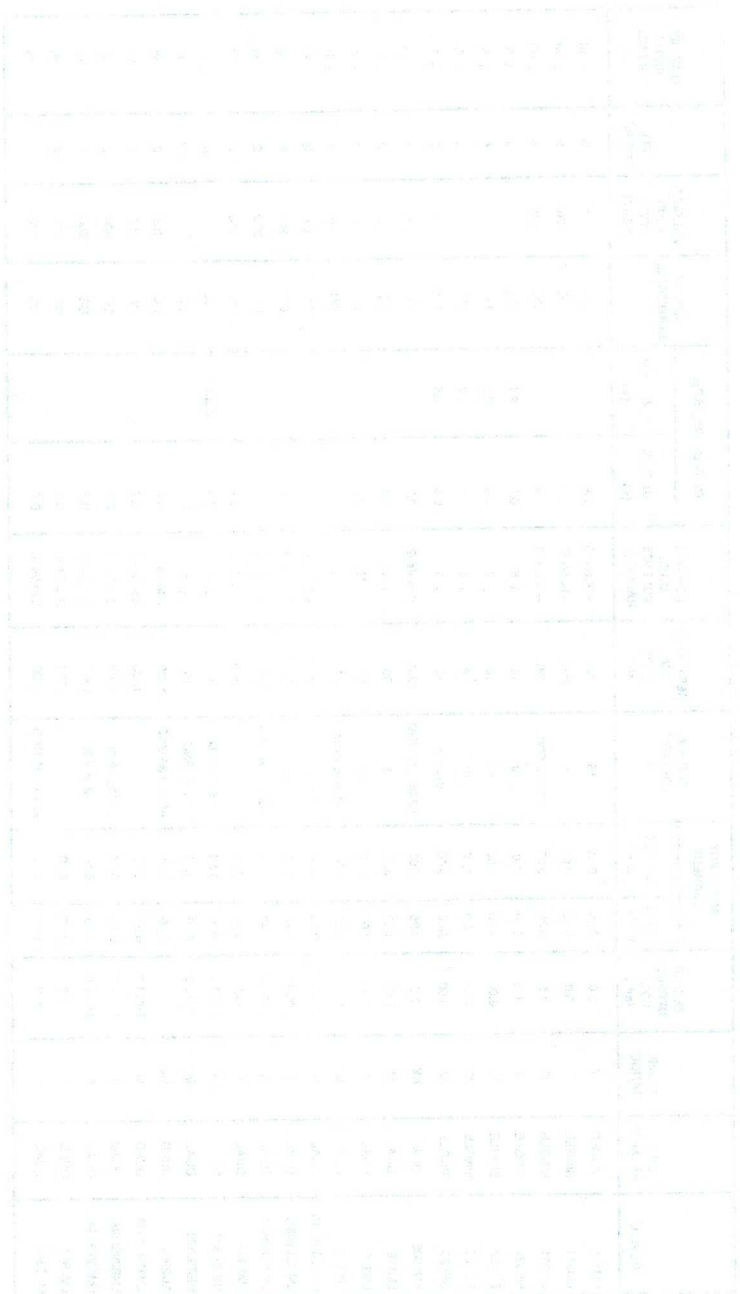
- Device Family and Temperature Range Prefix
  - AU = -40°C to +125°C
  - NE = 0 to +70°C
  - SE = –55°C to +125°C
  - SA = –40°C to +80°C
- Device Number
- Package Code:
  - A = Plastic Leaded Chip Carriers (PLCC)
  - D = Plastic SO
  - DK = Shrink Small Outline Package (SSOP)
  - F = Ceramic Dual In-Line
  - FE = Hermetic Cerdip (8 Lead)
  - N = Plastic Dual In-Line

Comparator selector guide

General Purpose/Linear ICs

DEVICE	COM-PLEXITY	TEMP RANGE*	MAX INP OFFSET VOLT (mV)	MAX INPUT CURRENT		SUPPLY VOLTAGE (V)	RESPONSE TIME (TYP) (ns)	COMMON MODE VOLTAGE RANGE (V)	OUTPUT VOLTAGE		OUTPUT STRUCTURE	VOLTAGE GAIN (TYP) (V/mV)	TTL FANOUT	MAX OFF INPUT VOLTAGE (V)
				BIAS (μ A)	OFFSET (μ A)				V OL MAX (V)	V OH MIN (V)				
LM111	SINGLE	M	3.0	0.10	0.01	± 15	200	−14.5/+13	0.4		OC	200	5	± 30
LM211	SINGLE	I	3.0	0.10	0.01	to	200	−14.5/+13	0.4		OC	200	5	± 30
LM311	SINGLE	C	7.5	0.25	0.05	+5 and GND	200	−14.5/+13	0.4		OC	200	5	± 30
NE527	SINGLE	C	10.0	4.00	1.0	± 10	16	± 5	0.5	2.7	TTL		5	± 5
SE527	SINGLE	M	6.00	4.00	1.00	+5	16	± 5	0.5	2.5	TTL		5	± 5
NE529	SINGLE	C	10.0	50.0	15.0	±10	12	± 5	0.5	2.7	TTL		5	± 5
SE529	SINGLE	M	6.00	36.0	9.00	and +5	12	± 5	0.5	2.5	TTL		5	± 5
AU2903	DUAL	AX	7.0	0.25	0.05	+2 to +36 GND	1300	0 to Vs−2	0.7		OC	100	2	36
LM119	DUAL	M	7.00	1.00	0.10	± 15	80	± 13	0.4		OC	40	2	± 5
LM219	DUAL	I	7.00	1.00	0.10	to	80	± 13	0.4		OC	40	2	± 5
LM319	DUAL	C	10.0	1.20	0.30	+5 and GND	80	± 13	0.4		OC	40	2	± 5
LM193 /193A	DUAL	M	9.00/4.0	0.30	0.10	± 1 to ± 18	1300	0 to Vs−2	0.7		OC	200	2	36
LM293/293A	DUAL	I	9.00/4.0	0.40	0.15	or	1300	0 to Vs−2	0.7		OC	200	2	36
LM393/393A	DUAL	C	9.00/4.0	0.40	0.15	+2 to +36 GND	1300	0 to Vs−2	0.7		OC	200	2	36
LM2903	DUAL	I	15.0	0.50	0.20		1300	0 to Vs−2	0.7		OC	100	2	36
NE/SE521	DUAL	M/C	15/10.0	40.0	12.0	+5 −5 GND	8	± 3	0.5	2.5/2.7	TTL		12	± 6
NE/SE522	DUAL	M/C	15/10.0	40.0	12.0	+5 −5 GND	10	± 3	0.5		OC		12	± 6
AU2901	QUAD	AX	7.0	0.25	0.05	+2 to +36 GND	1300	0 to Vs−2	0.7		OC	100	2	36
LM139 /139A	QUAD	M	9.00/4.0	0.30	0.10		1300	0 to Vs−2	0.7		OC	200	2	36
LM239/239A	QUAD	I	9.00/4.0	0.40	0.15	±1 to± 18 or	1300	0 to Vs−2	0.7		OC	200	2	36
LM339/339A	QUAD	C	9.00/4.0	0.40	0.15	+2 to +36	1300	0 to Vs−2	0.7		OC	200	2	36
LM2901	QUAD	I	15.0	0.50	0.20		1300	0 to Vs−2	0.7		OC	100	2	36
MC3302	QUAD	I	40.0	1.00	0.30	+2 to +28 GND	1300	0 to Vs−2	0.7		OC	100	2	36

* Temperature range
I = Industrial −25°C to +85°C
C = Commercial 0°C to +70°C
M = Military −55°C to +125°C
A = Automotive −40°C to +85°C
AX = Automotive extended −40°C to +125°C



Section 2
Operational Amplifiers

INDEX

AN165	Integrated operational amplifier theory	21
AN166	Basic feedback theory	31
LM124/224/324/324A/ SA534/LM2902	Low power quad op amps	35
AU2902	Low power quad operational amplifier	42
µA741/µA741C/SA741C	General purpose operational amplifier	47
µA747C	Dual operational amplifier	54
MC/SA1458/MC1558	General purpose operational amplifier	59
NE/SA/SE4558	Dual general-purpose operational amplifier	65
NE/SE531	High slew rate operational amplifier	70
NE/SA/SE5512	Dual high-performance operational amplifier	78
NE/SE5514	Quad high-performance operational amplifier	82
AN144	Applications for the NE/SA/SE5512	85
AN1441	Applications for the NE5514	89
NE5517/5517A	Dual operational transconductance amplifier	92
AN145	NE5517/A transconductance amplifier applications	105
NE/SE5532/5532A	Internally-compensated dual low noise operational amplifier	109
NE5533/5533A/ NE/SA/SE5534/5534A	Dual and single low noise op amp	114
AN142	Audio circuits using the NE5532/3/4	122
NE/SA5230	Low voltage operational amplifier	133
AN1511	Low-voltage gated function generator: NE5230	146
NE/SA/SE532/ LM158/258/358/A/2904	Low power dual operational amplifiers	148
AU2904	Low power dual operational amplifier	154
NE/SA5234	Matched quad high-performance low-voltage operational amplifier	159
AN1651	Using the NE/SA5234 amplifier	163

Integrated operational amplifier theory

AN165

INTRODUCTION

The operational amplifier was first introduced in the early 1940s. Primary usage of these vacuum tube forerunners of the ideal gain block was in computational circuits. They were fed back in such a way as to accomplish addition, subtraction, and other mathematical functions.

Expensive and extremely bulky, the operational amplifier found limited use until new technology brought about the integrated version, solving both size and cost drawbacks.

Volumes upon volumes have been and could be written on the subject of op amps. In the interest of brevity, this application note will cover the basic op amp as it is defined, along with test methods and suggestive applications. Also, included is a basic coverage of the feedback theory from which all configurations can be analyzed.

THE PERFECT AMPLIFIER

The ideal operational amplifier possesses several unique characteristics. Since the device will be used as a gain block, the ideal amplifier should have infinite gain. By definition also, the gain block should have an infinite input impedance in order not to draw any power from the driving source. Additionally, the output impedance would be zero in order to supply infinite current to the load being driven. These ideal definitions are illustrated by the ideal amplifier model of Figure 1.

Further desirable attributes would include infinite bandwidth, zero offset voltage, and complete insensitivity to temperature, power supply variations, and common-mode input signals.

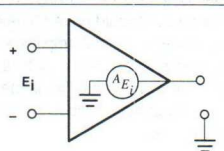


Figure 1. Ideal Operational Amplifier

Keeping these parameters in mind, further contemplation produces two very powerful analysis tools. Since the input impedance is infinite, there will be no current flowing at the amplifier input nodes. In addition, when feedback is employed, the differential input voltage reduces to zero. These two statements are used universally as beginning points for any network analysis and will be explored in detail later on.

THE PRACTICAL AMPLIFIER

Tremendous strides have been made by modern technology with respect to the ideal amplifier. Integrated circuits are coming closer and closer to the ideal gain block. In bipolar devices, for instance, input bias currents are in the pA range for FET input amplifiers while offset voltages have been reduced to less than 1mV in many cases.

Any device has limitations however, and the integrated circuit is no exception. Modern op amps have both voltage and current limitations. Peak-to-peak output voltage, for instance, is generally limited to one or two base-emitter voltage drops below the supply voltage, while output current is internally limited to approximately 25mA. Other limitations such as bandwidth and slew rates are also present, although each generation of devices improves over the previous one.

DEFINITION OF TERMS

Earlier, the ideal operational amplifier was defined. No circuit is ideal, of course, so practical realizations contain some sources of error. Most sources of error are very small and therefore can usually be ignored. It should be noted that some applications require special attention to specific sources of error.

Before the internal circuitry of the op amp is further explored, it would be beneficial to define those parameters commonly referenced.

INPUT OFFSET VOLTAGE

Ideal amplifiers produce 0V out for 0V input. But, since the practical case is not perfect, a small DC voltage will appear at the output, even though no differential voltage is applied. This DC voltage is called the input offset voltage, with the majority of its magnitude being generated by the differential input stage pictured in Figure 2.

An operational amplifier's performance is, in large part, dependent upon the first stage. It is the very high gain of the first stage that amplifies small signal levels to drive remaining circuitry. Coincidentally, the input current, a function of beta, must be as small as possible. Collector current levels are thus made very low in the input stage in order to gain low bias currents. It is this input stage which also determines DC parameters such as offset voltage, since the amplified output of this stage is of sufficient voltage levels to eclipse most subsequent error terms added by the remaining circuitry. Under balanced conditions, the collector currents of Q1 and Q2 are perfectly matched, hence we may say:

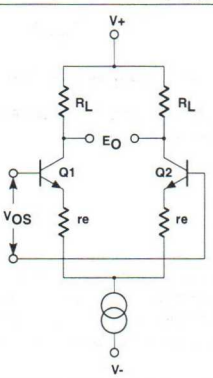


Figure 2. Differential Input Stage

$$E_{OS}=I_{C2}R_L-I_{C1}R_L=0 \quad (1)$$

In practice, small differences in geometries of the base-emitter regions of Q1 and Q2 will cause E_{OS} not to equal 0. Thus, for balance to be restored, a small DC voltage must be added to one V_{BE} or

$$V_{OS}=V_{BE}1-V_{BE}2 \quad (2)$$

where the V_{BE} of the transistor is found by

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_E}{I_S}\right) \quad (3)$$

Reference is made to the input when talking of offset voltage. Thus, the classic definition of input offset voltage is

"that differential DC voltage required between inputs of an amplifier to force its output to zero volts.'

Offset voltage becomes a very useful quantity for the designer because many other sources of error can be expressed in terms of V_{OS}. For instance, the error contribution of input bias current can be expressed as offset voltages appearing across the input resistors.

INPUT OFFSET VOLTAGE DRIFT

Another related parameter to offset voltage is V_{OS} drift with temperature. Present-day amplifiers usually possess V_{OS} drift levels in the range of 5μV/°C to 40μV/°C. The magnitude of V_{OS} drift is directly related to the initial offset voltage at room temperature. Amplifiers exhibiting larger initial offset voltages will also possess higher drift rates with temperature. A rule of thumb often applied is that the drift per °C will be 3.3μV for each millivolt of initial offset. Thus, for tighter control of thermal drift, a low offset amplifier would be selected.

INPUT BIAS CURRENT

Referring to Figure 3, it is apparent that the input pins of this op amp are base inputs. They must, therefore, possess a DC current path to ground in order for the input to function. Input bias current, then, is "the DC current required by the inputs of the amplifier to properly drive the first stage.'

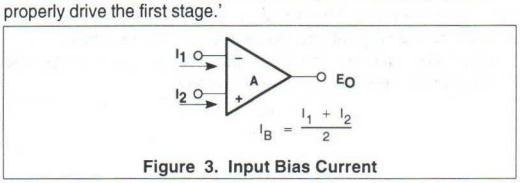


Figure 3. Input Bias Current

The magnitude of I_{BIAS} is calculated as the average of both currents flowing into the inputs and is calculated from

$$I_B = \frac{I_1 + I_2}{2} \quad (4)$$

Bias current requirements are made as small as possible by using high beta input transistors and very low collector currents in the first stage. The trade-off for bias current is lower stage gain due to low collector current levels and lower slew rates. The effect upon slew rate is covered in detail under the compensation section.

INPUT OFFSET CURRENT

The ideal case of the differential amplifier and its associated bias current does not possess an input offset current. Circuit realizations always have a small difference in bias currents from one input to the other, however. This difference is called the input offset current. Actual magnitudes of offset current are usually at least an order of magnitude below the bias current. For many applications this offset may be ignored but very high gain, high input impedance amplifiers should possess as little I_{OS} as possible because the difference in currents flowing across large impedances develops substantial offset voltages. Output voltage offset due to I_{OS} can be calculated by

$$V_{OUT}=A_{CI}(I_{OS}R_S) \quad (5)$$

Hence, high gain and high input impedances magnify directly to the output, the error created by offset current. Circuits capable of nulling the input voltage and current errors are available and will be covered later in this chapter.

INPUT OFFSET CURRENT DRIFT

Of considerable importance is the temperature coefficient of input offset current. Even though the effects of offset are nulled at room temperature, the output will drift due to changes in offset current over temperature. Many popular models now include a typical specification for I_{OS} drift with values ranging in the 0.5nA/°C area. Obviously, those applications requiring low input offset currents also require low drift with temperature.

INPUT IMPEDANCE

Differential and common-mode impedances looking into the input are often specified for integrated op amps. The differential impedance is the total resistance looking from one input to the other, while common-mode is the common impedance as measured to ground. Differential impedances are calculated by measuring the change of bias current caused by a change in the input voltage.

COMMON-MODE RANGE

All input structures have limitations as to the range of voltages over which they will operate properly. This range of voltages impressed upon both inputs which will not cause the output to misbehave is called the common-mode range. Most amplifiers possess common-mode ranges of ±12V with supplies of ±15V.

COMMON-MODE REJECTION RATIO

The ideal operational amplifier should have no gain for an input signal common to both inputs. Practical amplifiers do have some gain to common-mode signals. The classic definition for common-mode rejection ratio of an amplifier is the ratio of the differential signal gain to the common-mode signal gain expressed in dB as shown in equation 6a.

$$\text{CMRR (dB)} = 20 \log \frac{e_O/e_I}{e_O/e_{CM}} \quad (6a)$$

The measurement CMRR as in 6a requires 2 sets of measurements. However, note that if e_o in equation 6a is held constant, CMRR becomes:

$$\text{CMRR (dB)} = 20 \log \frac{e_{CM}}{e_I} \quad (6b)$$

A new alternate definition of CMRR based on 6b is the ratio of the change of input offset voltage to the input common-mode voltage change producing it.

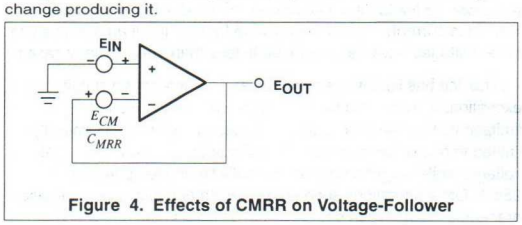


Figure 4. Effects of CMRR on Voltage-Follower

Figure 4 illustrates the application of the equivalent common-mode error generator to the voltage-follower circuit. The gain of the

voltage-follower with error contributions caused by both finite gain and finite common-mode rejection ratio is shown in equation 7.

$$\frac{e_O}{e_{IN}} = \frac{1 \pm 1/CMRR}{1 + 1/A} \quad (7)$$

where A equals open-loop gain and is frequency-dependent.

AC PARAMETERS

Parameter definition has, up to this point, been dealing primarily with DC quantities of voltages currents, etc. Several important AC, or frequency-dependent parameters will now be discussed.

An ideal gain block was defined earlier as one which would provide infinite gain and bandwidth. Real circuits approximate infinite open-loop gain with low frequency gains in excess of 100dB. The very high gains achieved with present designs are possible only by cascading stages. Although providing very high open-loop gain, the cascading of stages results in the need for frequency compensation in closed-loop configurations and reduces the open-loop.

LARGE-SIGNAL BANDWIDTH

The large-signal or power bandwidth of an amplifier refers to its ability to provide its maximum output voltage swing with increasing frequency. At some frequency the output will become slew rate limited and the output will begin to degrade. This point is defined by

$$f_{PL} = \frac{SLEW\ RATE}{2\pi \cdot E_{OUT}} \quad (8)$$

where f_{PL} is the upper power bandwidth frequency and E_{OUT} is the peak output swing of the amplifier.

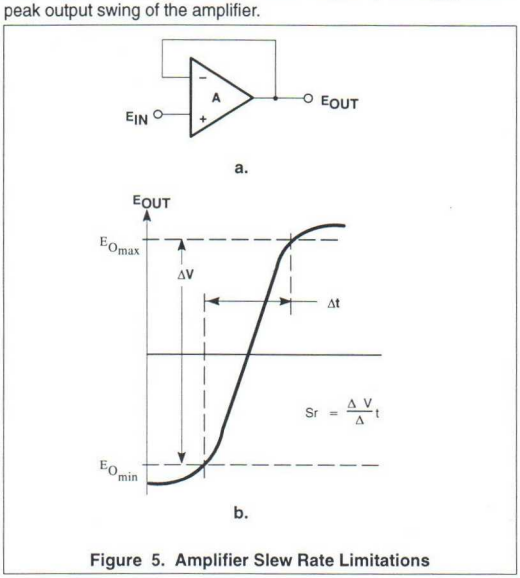


Figure 5. Amplifier Slew Rate Limitations

SLEW RATE

The maximum rate of change of the output in response to a step input signal is termed slew rate. Deviation from the ideal is caused by the limitation in frequency response of the amplifier stages and the phase compensation technique used. Summing node and amplifier output capacitances must be kept to a minimum to guarantee getting the maximum slew rate of the operational amplifier. Circuit board layout must also be of high frequency quality. Power supplies should be adequately bypassed at the pins, with both low and high frequency components, to avoid possible ringing. A selection of a proper capacitor in parallel with the feedback resistor may be necessary. Too small a value could result in excessive ringing and too large a value will decrease frequency response. In general, the worst case slew rate is in the unity gain non-inverting mode (see Figure 5a). Specifications of slew rate should always reflect this worst case condition with the maximum required compensation network.

FREQUENCY RESPONSE

Distributed capacitances and transit times in semiconductors cause an upper frequency limit or pole for each gain stage. Monolithic PNP transistors, used for level shifting, possess poor upper frequency characteristics. Cascaded gain stages, used to approach the highest gain, subtract from the maximum frequency response. As shown in Figure 6, the open-loop frequency

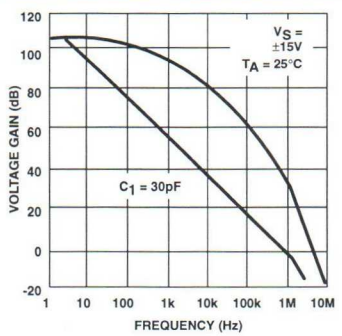
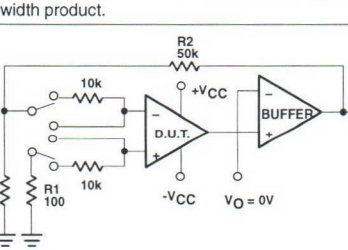


Figure 6. Open-Loop Voltage Gain as a Function of Frequency

response of the op amps shown crosses unity gain at approximately 10MHz. Closed-loop response is unstable without compensation, however, so typical unity gain frequencies are readjusted by the effects of phase compensation, in this case 1MHz.

From Figure 6, it is also apparent that an amplifier has a trade-off between gain and bandwidth. Higher gains are achieved at the expense of bandwidth. This trade-off is a constant figure called the gain bandwidth product.



NOTE:
All resistor values are in ohms.

Figure 7. Circuit Diagram Used for CMRR Measurement

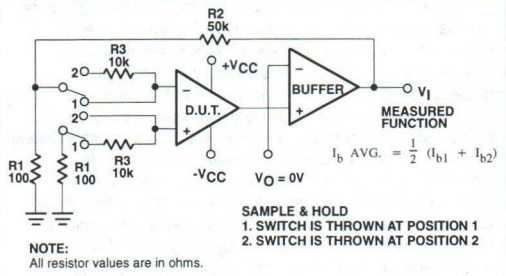


Figure 8. Circuit Diagram Used for Average Bias Current Measurement

TEST METHODS

Product testing of integrated circuits uses automatic test equipment. Large computer-controlled test decks test all data sheet limits in a matter of milliseconds. Each parameter is tested in a specific circuit configuration defined by the test hardware.

A typical simplified op amp test configuration is depicted by Figure 9. Units may be classed in several categories according to selected parameters. Even failures may be classified categorically, depending upon their mode of failure.

Figures 7, 8, 10 and 11 illustrate the general test setups commonly used to measure CMRR, average bias current, offset voltage and current, and open-loop gain, respectively.

In general, the following parameters are tested under the following conditions.

COMMON-MODE REJECTION

The test setup for CMRR is given in Figure 7. Resistor values are chosen to provide sufficient sensitivity and accuracy for the device type being tested and the voltage measuring equipment being used.

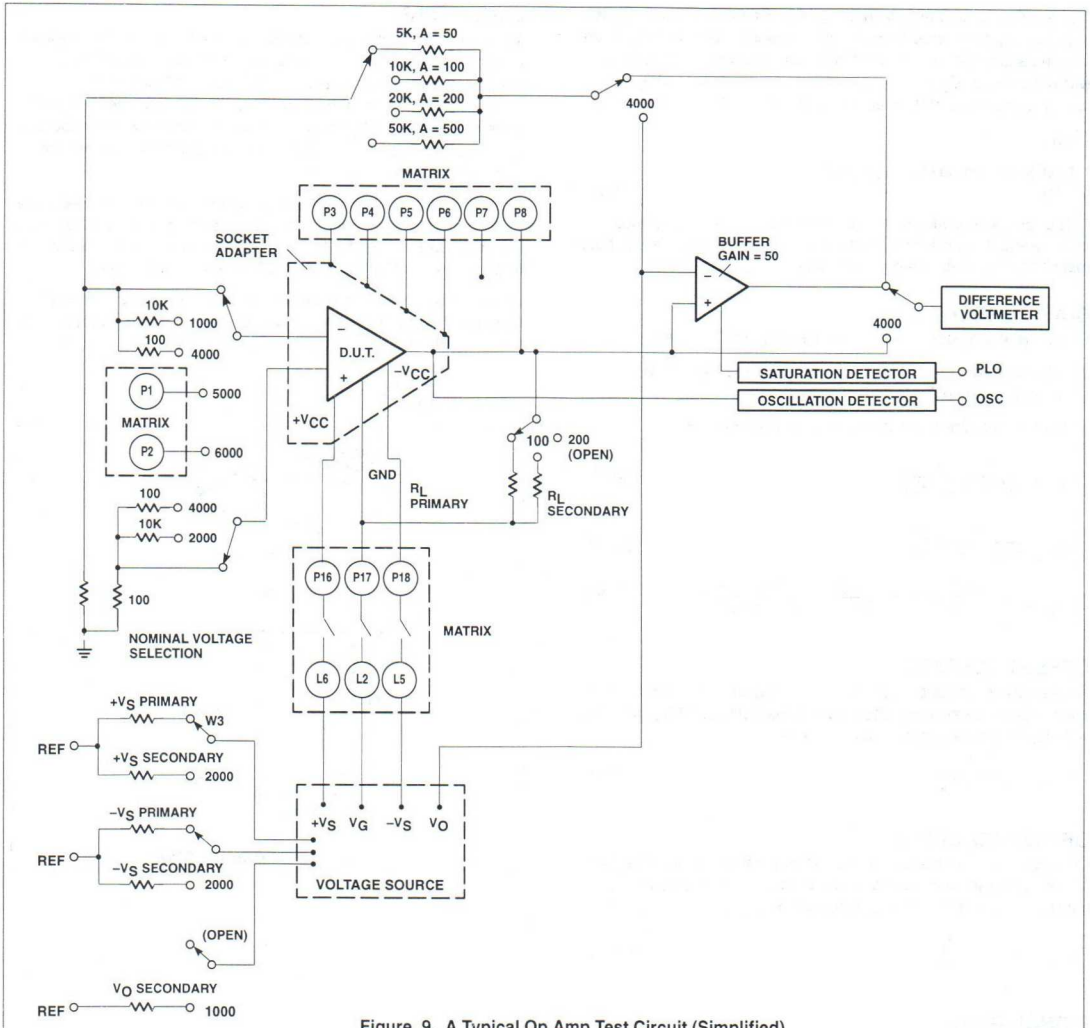


Figure 9. A Typical Op Amp Test Circuit (Simplified)

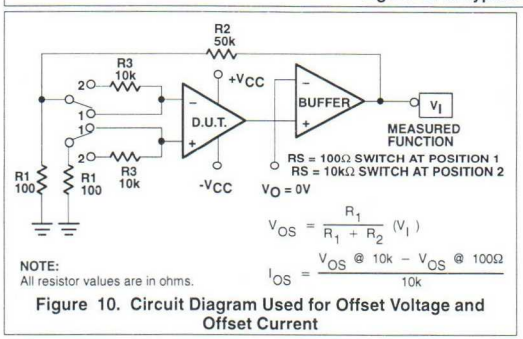


Figure 10. Circuit Diagram Used for Offset Voltage and Offset Current

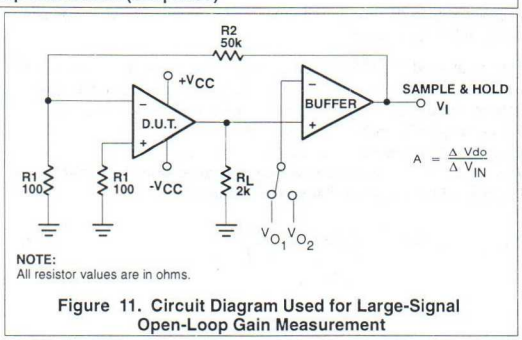


Figure 11. Circuit Diagram Used for Large-Signal Open-Loop Gain Measurement

The positive common-mode input voltage within the range V_{CM1} is algebraically subtracted from all supply voltages and from V_O. Then V_1 is measured (V_{11}). The most negative common-mode voltage within the range, V_{CM2}, is then subtracted from all the supply voltages and V_O, and V_1 is again measured (V_{12}).

Then

$$CMRR=(R1+R2)/R1(V_{CM1}-V_{CM2})/V_{11}-V_{12} \quad (9)$$

This operation is equivalent to swinging both inputs over the full common-mode range, and holding the output voltage constant, but it makes the V_1 measurement much simpler.

BIAS CURRENT

Bias current is measured in the configuration of Figure 8.

With switches at position 1 and V_O=0V, measure V_{11}. Move switches to position 2

and again measure V_{12}. Calculate I_{BIAS} (average), by

$$I_{B1} = \frac{R_1}{R1 + R2}\left(\frac{V1}{R3}\right) \quad (10a)$$

$$I_{B2} = \frac{R_1}{R1 + R2}\left(\frac{V1}{R3}\right) \quad (10b)$$

$$I_{BIAS(avg)} = \frac{I_{B1} + I_{B2}}{2} = \frac{R1}{R1 + R2}\,\frac{V_{11} - V_{12}}{2R3} \quad (10c)$$

OFFSET VOLTAGE

Figure 10 is used for both offset voltage and current. With V_O at 0V and the switches selecting the source impedance of 100Ω, the offset voltage is measured at V_1 and is equal to

$$V_{OS} = \frac{R1V_1}{R1 + R2} \quad (11)$$

OFFSET CURRENT

Offset current is measured by calculation of offset voltage change with a change in source impedance. With switches in position 1, measure V_{12}. Calculate the contribution of I_{OS} by

$$I_{OS} = V_{12} - \frac{V_I}{R3} \quad (12)$$

SIGNAL GAIN

The signal gain of operational amplifiers is most commonly specified for the full output swing.

This is referred to as large signal voltage gain and can be measured by the circuit of Figure 11. Usually specified under a specific load determined by R_L, a signal equal to the maximum swing of the output voltage is applied to V_O in both positive and negative directions. V_{11} and V_{12} are measured values of V_1 and V_O=maximum positive and maximum negative signals, respectively. The gain of the device under test then becomes

$$A_{VO} = \left(\frac{R1 + R2}{R1}\right)\left(\frac{V_{O1} - V_{O2}}{V_{11} - V_{12}}\right) \quad (13)$$

SLEW RATE

Many other parameters are checked automatically by similar means. Only the most important ones have been covered here. Of great interest to the designer are other parameters which do not necessarily carry minimum or maximum limits. One such parameter is slew rate. The configuration used to measure slew rate depends upon the intended application. Worst case conditions arise in the unity gain non-inverting mode.

Figure 12 shows a typical bench setup for measuring the response of the output to a step input. The input step frequency should be of a frequency low enough for the output of the op amp to have sufficient time to slew from limit to limit. In addition, V_{IN} must be less

than absolute maximum input voltage and the waveform should have good rise and fall times. The slew rate is then calculated from the slope of the output voltage versus time or

$$SR = \frac{\Delta V_{OUT}}{\Delta} T \text{ in } V/\mu s \quad (14)$$

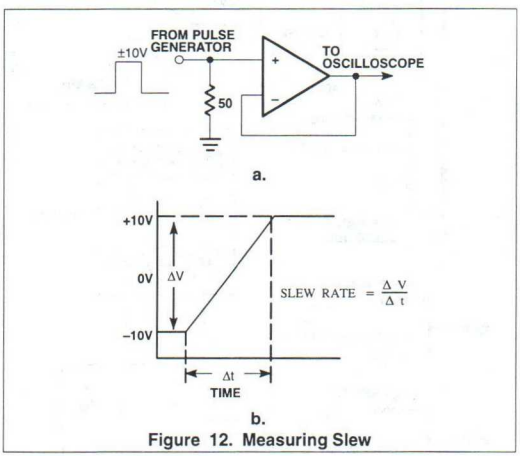


Figure 12. Measuring Slew

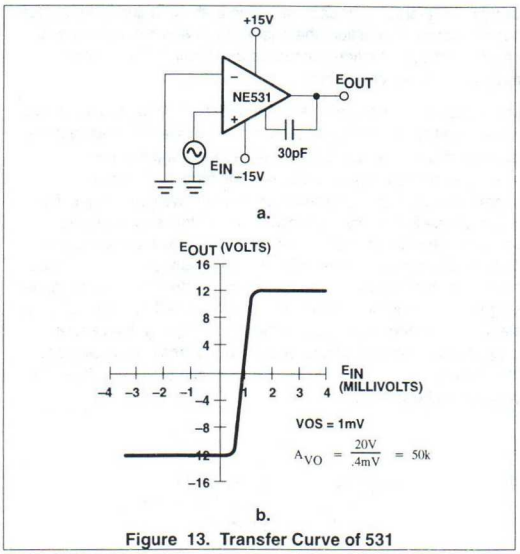


Figure 13. Transfer Curve of 531

OP AMP CURVE TRACER

Two of the most important parameters of linear integrated circuits having differential inputs are voltage gain and input offset voltage. These parameters may be read directly from a plot of the transfer characteristic of the device. This memo will describe a very simple curve tracer which, when used with an oscilloscope, will display the transfer characteristic of most Philips Semiconductors linear devices.

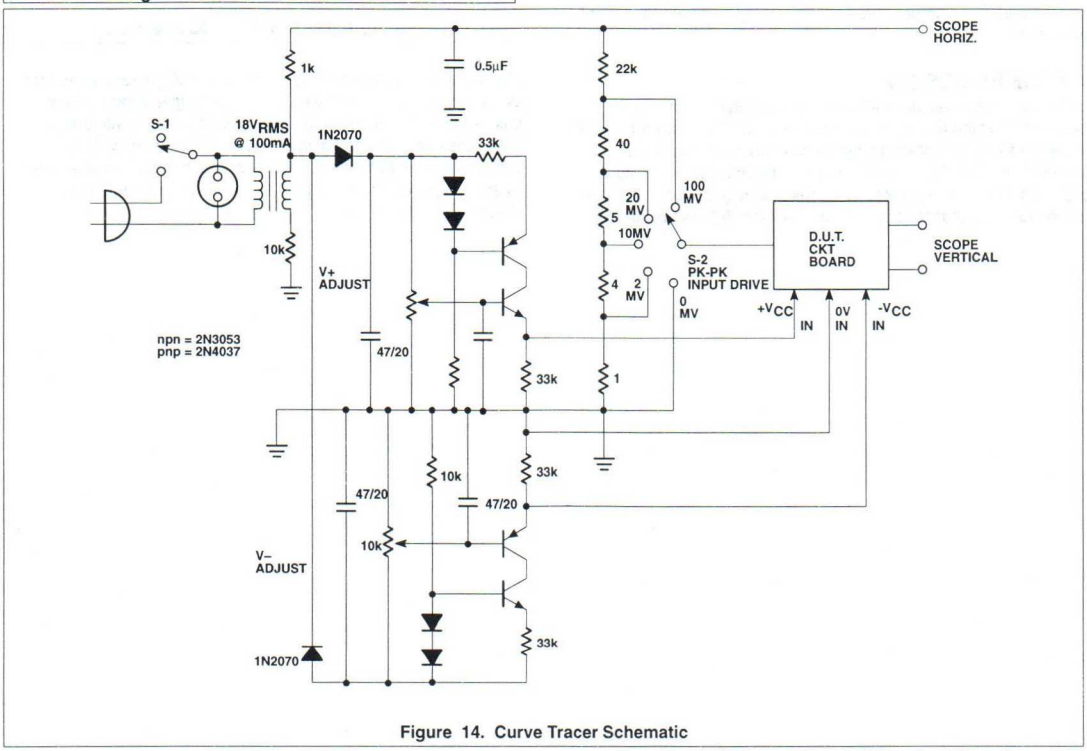


Figure 14. Curve Tracer Schematic

Figure 13 shows the transfer characteristics of a typical linear device, the Philips Semiconductors NE531. Note that the unit saturates at approximately +12V and -12V and exhibits a linear transfer characteristic between -10V and +10V.

From the slope of this linear portion of the transfer characteristic, and from the point and +10V where it crosses the E_{IN} axis, the

voltage gain and offset voltage may be determined. It can be seen that the voltage gain of the device under test, (DUT), is 50,000 and its input offset voltage is 1.0mV.

A simple circuit to display the curves of Figure 13 on an oscilloscope is shown in Figure 14. A 60Hz, $44V_{P-P}$ sinewave is applied to the horizontal input of oscilloscope and an attenuated version of the sinewave is applied to the input of the DUT.

The output of the DUT drives the vertical input of the scope. For providing V+ and V- to the DUT, the tester uses two simple adjustable regulators, both current-limited at 25mA. Input drive to the DUT may be selected by means of S-2 as shown.

To use the curve tracer, first preset the V+ and V- supplies with an accurate meter. The supply voltages are somewhat dependent on AC line regulation and should be checked periodically. The horizontal gain of the scope may be set to give a convenient readout of the peak-to-peak DUT input signal corresponding to the setting of S-2. As some devices have two outputs, a second output line (vertical 2) has been provided for these devices. The transfer function of such devices will be inverted to that of Figure 13.

Simplicity and low cost are the two major attributes of this tester. It is not intended to perform highly rigorous tests for all devices. It is, however, a reasonably accurate means of determining the gains and offset voltages of most amplifiers. It will, in addition, indicate the transfer curves of comparators and sense amplifiers with equivalent accuracies.

AMPLIFIER DESIGN

Linear operational amplifier ICs were introduced soon after the appearance of the first digital integrated circuits. The performance of these early devices, however, left much to be desired until the introduction of the 709 device. Even with its lack of short-circuit protection and its complicated compensation requirements, the 709 gained real acceptance for the IC op amp. The 709 was designed using a three-stage approach requiring both input and output stage compensation. In addition, the output stage was not short-circuit proof and the input stage latched-up under certain conditions, requiring external protection.

Much better designs soon were introduced. Among the contenders were the 741, 748, 101, and 107 devices. All were general purpose devices with single capacitor compensation, (some were internally-compensated), and all heralded input and output overstress protection. The basic design has two gain stages. By rolling off the frequency response of one of these (the second stage), so that the overall gain is unity at a frequency below the point where excess phase becomes significant, the device can be stabilized for all feedback configurations. Further, by making the first stage a voltage-to-current converter, with a small g_M and the second stage a current-to-voltage converter with a high r_M, the second stage can be rolled off at 6dB octave with a small value capacitor in the order of 30pF, which can then be built into the device itself. This concept is shown in Figure 15.

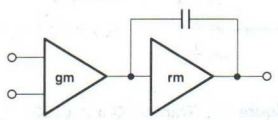


Figure 15. Basic Two-Stage Op Amp Design

The frequency and phase response of the PNP devices in the first stage dictate a roll-off in the second stage to give a loop gain of unity at about 1.0MHz. For the unity gain feedback configuration, this implies an open-loop gain of unity at this frequency. The capacitor C_C controls this parameter by looking much smaller than r_M at frequencies above a few cycles, giving a clean 6dB/octave roll-off over 5 decades.

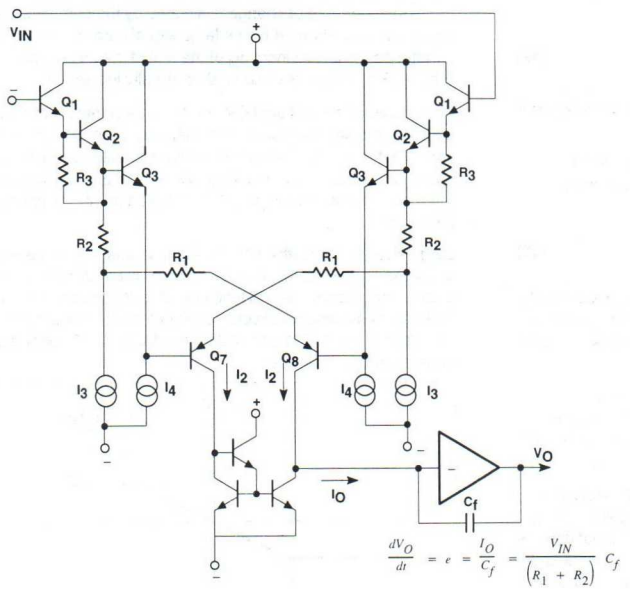


Figure 16. Input Structure of 531

The overall gain at frequencies where the impedance of C_C dominates r_m is given by

$$A_{V(sigma)} = \frac{QI_{S1}}{4kT} \cdot \frac{1}{\sigma C_C} \quad (15)$$

Substituting the value given, we find that a capacitance of C_C=30pF gives a unity gain frequency of about 1.0MHz.

First-stage large signal current also defines the slew rate for a specific compensation technique. It is this current which must charge and discharge the C_C by the expression

$$SR = \frac{dV}{dT} = \frac{I_{LS}}{C_C} \quad (16)$$

where I_{LS} is the largest signal current of the input stage. Obviously, the slew rate can be improved by increasing the first-stage collector current. This would, however, reflect directly upon the bias current by increasing it.

Two serious limitations, then, of these devices for diverse applications are input bias current and slew rate. Both may be overcome with small changes of the input structure to yield higher performance devices.

Reducing the input bias current becomes a matter of raising the transistor beta of the first stage. Several current designs boasting very low input currents use what is termed super beta input devices. These transistors have betas of 1,500 to 7,000. Bias currents under 2nA can be achieved in this way. Even though the B_{VCEO} of such transistors can be as low as 1V, the lower breakdowns are accounted for in the input stage by rearranging the bias technique. Bandwidths and slew rates suffer only slightly as a result of the lower current levels.

The second limitation of 741 devices is slew rate. As previously mentioned, the rate of change is dictated by the compensation capacitance as charged by the large signal current of the first stage. By altering the large signal g_M of the first stage as depicted by Figure 18, the slew rate can be dramatically increased.

The additional current supplied during large signal swings by current source I_4 causes the first-stage transfer function to change as shown in Figure 19. The compensation capacitor is returned to the output of the NE531 structure because the output driving source must be capable of supplying the increased current to charge the capacitor.

Large-signal bandwidths with this input structure will be essentially the same as the small-signal response. Full bandwidth possibilities of this configuration are still limited by the beta and f_t of the lateral PNP devices used for collector loads in the first stage. Even so, the slew rate of the NE531 and NE538 is a factor of 40 better than general purpose devices.

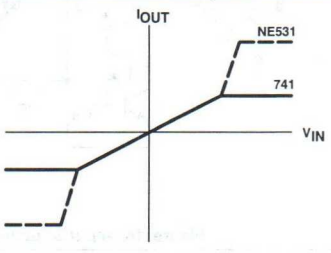


Figure 17. Voltage/Current Curves of First Stage

Basic feedback theory

AN166

BASIC FEEDBACK THEORY

In AN165, the ideal op amp was defined. The ideal parameters are never fully realized but they present a very convenient method for the preliminary analysis of circuitry. So important are these ideal definitions that they are repeated here. The ideal amplifier possesses

1. Infinite gain
2. Infinite input impedance
3. Infinite bandwidth
4. Zero output impedance

From these definitions two important theorems are developed.

1. No current flows into or out of the input terminals.
2. When negative feedback is applied, the differential input voltage is reduced to zero.

Keeping these rules in mind, the basic concept of feedback can be explored.

VOLTAGE-FOLLOWER

Perhaps the most often used and simplest circuit is that of a voltage-follower. The circuit of Figure 1 illustrates the simplicity.

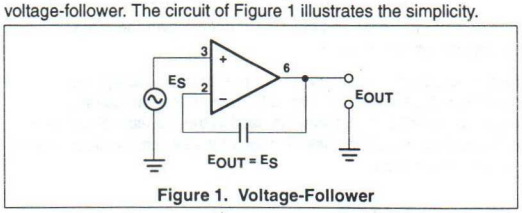


Figure 1. Voltage-Follower

Applying the zero differential input theorem, the voltages of Pins 2 and 3 are equal, and since Pins 2 and 6 are tied together, their voltage is equal; hence, $E_{OUT}=E_{IN}$. Trivial to analyze, the circuit nevertheless does illustrate the power of the zero differential voltage theorem. Because the input impedance is multiplied and the output impedance divided by the loop gain, the voltage-follower is extremely useful for buffering voltage sources and for impedance transformation.

The basic configuration in Figure 1 has a gain of 1 with extremely high input impedance. Setting the feedback resistor equal to the source impedance will cancel the effects of bias current if desired.

However, for most applications, a direct connection from output to input will suffice. Errors arise from offset voltage, common-mode rejection ratio, and gain. The circuit can be used with any op amp with the required unity gain compensation, if it is required.

NON-INVERTING AMPLIFIER

Only slightly more complicated is the non-inverting amplifier of Figure 2.

The voltage appearing at the inverting input is defined by

$$E_2 = \frac{E_{OUT} \cdot R_{IN}}{R_F + R_{IN}} \quad (1a)$$

Since the differential voltage is zero, $E_2=E_S$, and the output voltage becomes

$$E_{OUT} = E_S\left(1 + \frac{R_F}{R_{IN}}\right) \quad (1b)$$

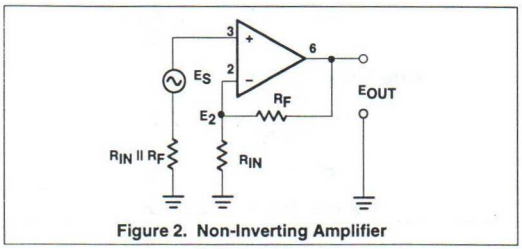


Figure 2. Non-Inverting Amplifier

It should be noted that as long as the gain of the closed-loop is small compared to open-loop gain, the output will be accurate, but as the closed-loop gain approaches the open-loop value more error will be introduced.

The signal source is shown in Figure 2 in series with a resistor equal in size to the parallel combination of R_{IN} and R_F. This is desirable because the voltage drops due to bias currents to the inputs are equal and cancel out even over temperature. Thus overall performance is much improved.

The amplifier does not phase-invert and possesses high input impedance. Again the impedances of the two inputs should be equal to reduce offsets due to bias currents.

INVERTING AMPLIFIER

By slightly rearranging the circuit of Figure 2, the non-inverting amplifier is changed to an inverting amplifier. The circuit gain is found by applying both theorems; hence, the voltage at the inverting input is 0 and no current flows into the input. Thus the following relationships hold:

$$\frac{E_S}{R_{IN}} + \frac{E_O}{R_F} = 0 \quad (2a)$$

Solving for the output E_O

$$E_O = E_S \frac{R_F}{R_{IN}} \quad (2b)$$

As opposed to the non-inverting circuits the input impedance of the inverting amplifier is not infinite but becomes essentially equal to R_{IN}. This circuit has found widespread acceptance because of the ease with which input impedance and gain can be controlled to advantage, as in the case of the summing amplifier.

With the inverting amplifier of Figure 3, the gain can be set to any desired value defined by R divided by R_{IN}. Input impedance is defined by the value of R_{IN} and R should equal the parallel combination of R_{IN} and R to cancel the effect of bias current. Offset voltage, offset current, and gain contribute most of the errors. The ground may be set anywhere within the common-mode range and any op amp will provide satisfactory response.

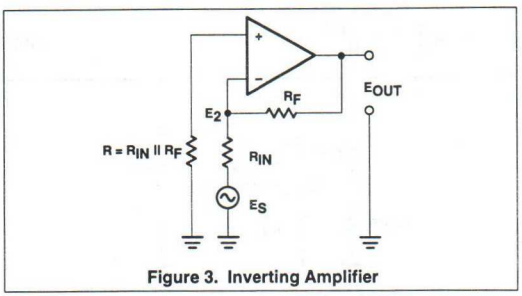


Figure 3. Inverting Amplifier

CURRENT-TO-VOLTAGE CONVERTER

The transfer function of the current-to-voltage converter is

$$V_{OUT} = I_{IN} R_1 \quad (3)$$

Evaluation of the circuit depends upon the virtual ground theorem developed earlier. The current flowing into the input must be the same as that flowing across R1, hence, the output voltage is the IR drop of R1.

Limitations, of course, are output saturation voltage and output current capability. The inputs may be biased anywhere within the common-mode range.

DIFFERENTIAL AMPLIFIER

This circuit of Figure 5 has a gain with respect to differential signals of R2/R1.

The common-mode rejection is dominated by the accuracy of the resistors. Other errors arise from the offset voltage, input offset current, gain and common-mode rejection. The circuit can be used with any op amp discussed in this chapter with the proper compensation.

SUMMING AMPLIFIER

The summing amplifier is a variation of the inverting amplifier. The output is the sum of the input voltages, each being weighed by R_F/R_{IN}.

The value of R4 may be chosen to cancel the effects of bias current and is selected equal to the parallel combination of R_F and all the input resistors.

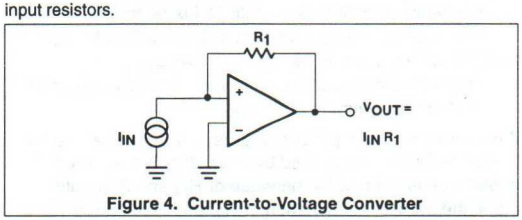


Figure 4. Current-to-Voltage Converter

INTEGRATOR

Integration can be performed with a variation of the inverting amplifier by replacing the feedback resistor with a capacitance. The transfer function is defined by

$$V_{OUT} = -\frac{1}{RC}\int_0^t V_{IN} \cdot dt \quad (4)$$

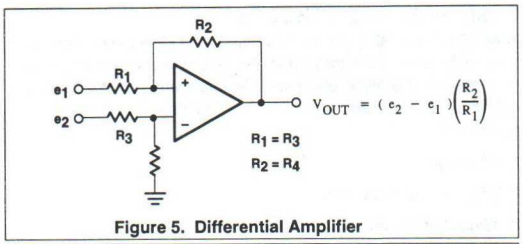


Figure 5. Differential Amplifier

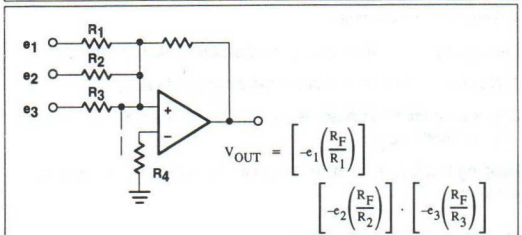


Figure 6. Summing Amplifier

The gain of the circuit falls at 6dB per octave over the range in which strays and leakages are small.

Since the gain at DC is very high a method for resetting initial conditions is necessary. Switch S1 removes the charge on the capacitor. A relay or FET may be used in the practical circuit. Bias and offset currents and offset voltage of the switch should be low in such an application.

DIFFERENTIATOR

The differentiator of Figure 8 is another variation of the inverting amplifier. The gain increases at 6dB per octave until it intersects the amplifier open-loop gain, then decreases because of the amplifier bandwidth. This characteristic can lead to instability and high frequency noise sensitivity.

A more practical circuit is shown in Figure 9. The gain has been reduced by R3 and the high frequency gain reduced by C2, allowing better phase control and less high frequency noise. Compensation should be for unity gain.

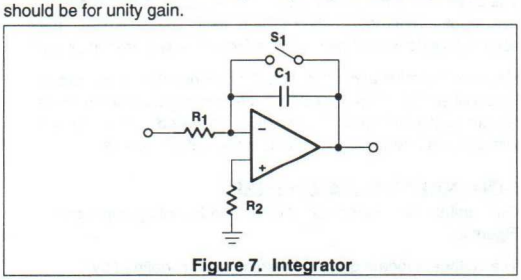


Figure 7. Integrator

COMPENSATION

Present-day operational amplifiers are comprised of multiple stages, each of which has a 3dB point or pole associated with it. Referring to Figure 10, the 3dB breakpoints of a two-stage amplifier are approximated by the Bode plot.

As with any feedback loop, the op amp must be protected from phase shifts in excess of 360°. A steady 180° phase shift is developed by the amplifier from output to inverting input. In addition, the sum of all additional shifts due to amplifier poles or feedback component poles will cause the necessary additional 180° to sustain oscillation if the gain of the amplifier is greater than one for the frequency at which the 180° phase shift is reached. By adding poles and zeros to the amplifier response externally, the phase shift can be controlled to insure stability.

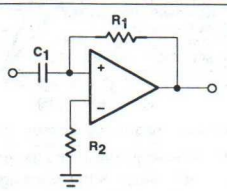


Figure 8. Differentiator

Many op amps now include internal compensation. These are single capacitors of 30pF, typically, and the amplifier will remain stable for all gains. However, since they are unconditionally stable, the compensation is larger than required for most applications. The resultant loss of bandwidth and slew rate may be acceptable in the general case, but selection of an externally-compensated device can add a great deal to the amplifier response if the compensation is handled properly.

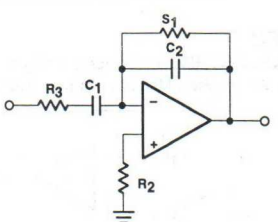


Figure 9. Practical Differentiator

In order to fully develop the point at which instability occurs, a fuller understanding of phase response is necessary.

The diagram of Figure 11 depicts the phase shift of a single pole. Note that at the pole position the phase shift is 45° and that phase shift becomes 0° for a decade below the pole and -90° for a decade above the pole location. This is a Bode approximation which possesses a 5.7° error at 0° and 90°, but this error is usually considered small enough to be ignored. The single pole produces a maximum of 90° phase shift and also produces a frequency roll-off of 20dB per decade.

The addition of the second pole of Figure 12 produces an additional 90° phase shift and increases the roll-off slope to -40dB per decade. At this point, phase shift could exceed 180° because unity gain is reached, causing stability. For gain levels equal to A1 or 1/β, the phase shift is only 90° and the amplifier is stable. However, with a β gain of A2 the phase shift is 180° and the loop is unstable. Gains in between A1 and A2 are marginally stable. As shown in Figure 13, the phase shift as it approaches 180° causes increasing frequency peaking and overshoot until sustained oscillations occur.

It is generally accepted in the interest of minimized frequency peaking to limit the phase shift of the amplifier to 135° or a phase margin of 45°. At this margin the second-order response of the system is critically damped and oscillation is prevented.

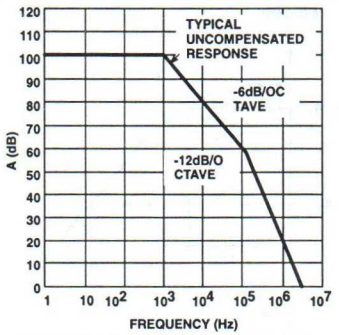


Figure 10. Frequency Compensation

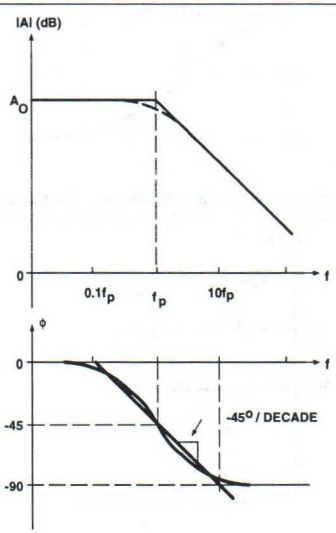


Figure 11. Single-Pole Amplitude and Phase Response

Referring to Figure 14, the required compensation can be determined. Given the open-loop response of the amplifier, the desired gain is plotted until it intercepts the open-loop curve as shown.

The phase shift for minimum peaking is 135°. Remembering that phase shift is 45° at the frequency pole, the example of Figure 14 will be unstable at gains less than 20dB where phase shift exceeds 180°, and will possess excessive overshoot and ringing at gains less than 60dB where phase shift exceeds 135°. Thus, the desired compensation will move the second pole of the amplifier out in frequency until the closed-loop gain intersects the open-loop

response before the second break of the amplifier occurs. Selecting only enough compensation to do the job assures the maximum bandwidths and slew rates of the amplifier. Additional in-depth information on compensation can be found in the reference material.

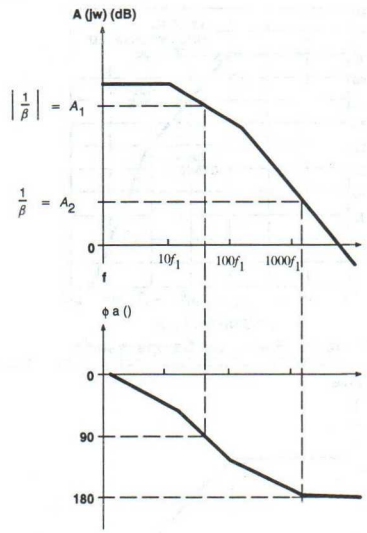


Figure 12. Two-Pole Closed-Loop Response

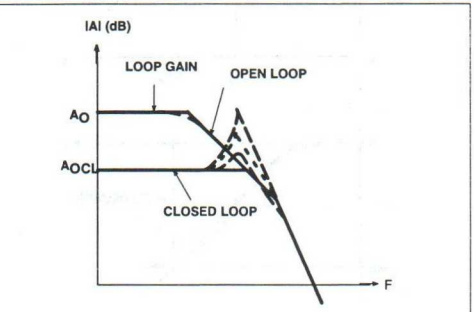


Figure 13. Frequency Peaking Due to Insufficient Phase Margin

FEED-FORWARD COMPENSATION

External compensation has been shown to improve amplifier bandwidth over internal compensation in the preceding section. Additional bandwidth can be realized if feed-forward compensation is used.

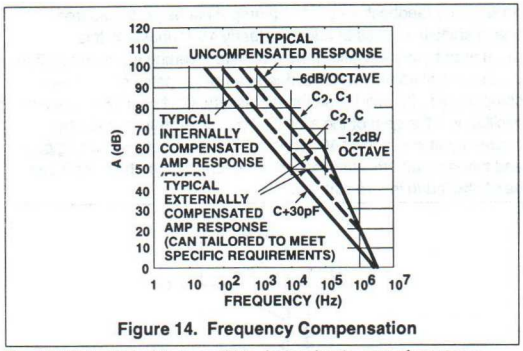


Figure 14. Frequency Compensation

Bandwidth is limited in monolithic design by the poor frequency response of the PNP level shifters of the first stage.

The concept of feed-forward compensation bypasses the input stage at high frequencies driving the higher frequency second stage directly as pictured by Figure 15. The Bode plot of Figure 16 shows the additional response added by the feed-forward technique. The response of the original amplifier requires less compensation at lower frequencies allowing an order of magnitude improvement in bandwidth. Standard compensation and feed-forward are both plotted to illustrate the bandwidth improvement. Unfortunately, the use of feed-forward compensation is restricted to the inverting amplifier mode.

REFERENCES

1. OPERATIONAL AMPLIFIERS-Design & Applications, Jerald Graeme and Gene Tobey, McGraw Hill Book Company.

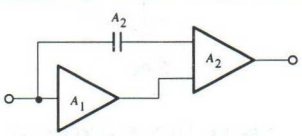


Figure 15. Technique of Feed-Forward Around 1st Stage

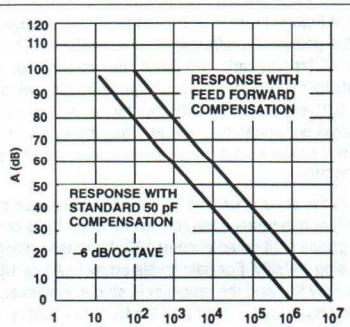


Figure 16. Frequency Response With Feed-Forward Compensation

Low power quad op amps

LM124/224/324/324A/ SA534/LM2902

DESCRIPTION

The LM124/SA534/LM2902 series consists of four independent, high-gain, internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages.

UNIQUE FEATURES

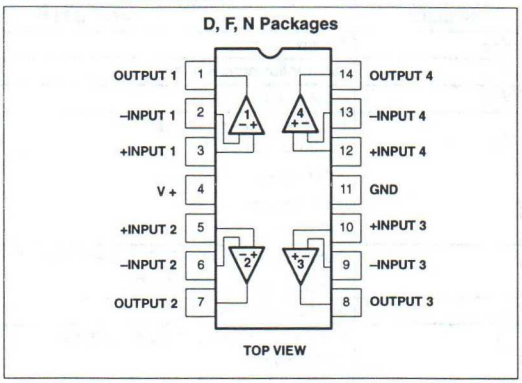
In the linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain crossover frequency and the input bias current are temperature-compensated.

FEATURES

- Internally frequency-compensated for unity gain
- Large DC voltage gain: 100dB
- Wide bandwidth (unity gain): 1MHz (temperature-compensated)
- Wide power supply range Single supply: $3V_{DC}$ to $30V_{DC}$ or dual supplies: $\pm1.5V_{DC}$ to $\pm15V_{DC}$
- Very low supply current drain: essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)
- Low input biasing current: $45nA_{DC}$ (temperature-compensated)
- Low input offset voltage: $2mV_{DC}$ and offset current: $5nA_{DC}$
- Differential input voltage range equal to the power supply voltage
- Large output voltage: $0V_{DC}$ to V_{CC}-$1.5V_{DC}$ swing

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	LM124N	0405B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	LM124F	0581B
14-Pin Plastic Dual In-Line Package (DIP)	-25°C to +85°C	LM224N	0405B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-25°C to +85°C	LM224F	0581B
14-Pin Plastic Small Outline (SO) Package	-25°C to +85°C	LM224D	0175D
14-Pin Plastic Dual In-Line Package (DIP)	0°C to +70°C	LM324N	0405B
14-Pin Ceramic Dual In-Line Package (CERDIP)	0°C to +70°C	LM324F	0581B
14-Pin Plastic Small Outline (SO) Package	0°C to +70°C	LM324D	0175D
14-Pin Plastic Dual In-Line Package (DIP)	0°C to +70°C	LM324AN	0405B
14-Pin Plastic Small Outline (SO) Package	0°C to +70°C	LM324AD	0175D
14-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA534N	0405B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-40°C to +85°C	SA534F	0581B
14-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA534D	0175D
14-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	LM2902D	0175D
14-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	LM2902N	0405B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	32 or ±16	V_{DC}
V_{IN}	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	-0.3 to +32	V_{DC}
P_D	Maximum power dissipation, T_A=25°C (still-air)[1]		
	N package	1420	mW
	F package	1190	mW
	D package	1040	mW
	Output short-circuit to GND one amplifier[2] V_{CC}<15V_{DC} and T_A=25°C	Continuous	
I_{IN}	Input current (V_{IN}<-0.3V)[3]	50	mA
T_A	Operating ambient temperature range		
	LM324/A	0 to +70	°C
	LM224	-25 to +85	°C
	SA534/LM2902	-40 to +85	°C
	LM124	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C at the following rates:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C
2. Short-circuits from the output to V_{CC}+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA, independent of the magnitude of V_{CC}. At values of supply voltage in excess of +15V_{DC} continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input bias clamps. In addition, there is also lateral NPN parasitic transistor action on the IC chip. This action can cause the output voltages of the op amps to go to the V+ rail (or to ground for a large overdrive) during the time that the input is driven negative.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=5V, T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM124/LM224			LM324/SA534/LM2902			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω		±2	±5		±2	±7	mV
		R_S=0Ω, over temp.			±7			±9	
$\Delta V_{OS}/\Delta T$	Temperature drift	R_S=0Ω, over temp.		7			7		µV/°C
I_{BIAS}	Input current[2]	I_{IN}(+) or I_{IN}(-)		45	150		45	250	nA
		I_{IN}(+) or I_{IN}(-), over temp.		40	300		40	500	
$\Delta I_{BIAS}/\Delta T$	Temperature drift	Over temp.		50			50		pA/°C
I_{OS}	Offset current	I_{IN}(+)-I_{IN}(-)		±3	±30		±5	±50	nA
		I_{IN}(+)-I_{IN}(-), over temp.			±100			±150	
$\Delta I_{OS}/\Delta T$	Temperature drift	Over temp.		10			10		pA/°C
V_{CM}	Common-mode voltage range[3]	V_{CC}≤30V	0		V_{CC}-1.5	0		V_{CC}-1.5	V
		V_{CC}≤30V, over temp.	0		V_{CC}-2	0		V_{CC}-2	
CMRR	Common-mode rejection ratio	V_{CC}=30V	70	85		65	70		dB
V_{OUT}	Output voltage swing	R_L=2kΩ, V_{CC}=30V, over temp.	26			26			V
V_{OH}	Output voltage high	R_L≤10kΩ, V_{CC}=30V, over temp.	27	28		27	28		V
V_{OL}	Output voltage low	R_L≤10kΩ, over temp.		5	20		5	20	mV
I_{CC}	Supply current	R_L=∞, V_{CC}=30V, over temp.		1.5	3		1.5	3	mA
		R_L=∞, over temp.		0.7	1.2		0.7	1.2	
A_{VOL}	Large-signal voltage gain	V_{CC}=15V (for large V_O swing), R_L≥2kΩ	50	100		25	100		V/mV
		V_{CC}=15V (for large V_O swing), R_L≥2kΩ, over temp.	25			15			
	Amplifier-to-amplifier coupling[5]	f=1kHz to 20kHz, input referred		-120			-120		dB
PSRR	Power supply rejection ratio	R_S≤0Ω	65	100		65	100		dB
I_{OUT}	Output current source	V_{IN}+=+1V, V_{IN}-=0V, V_{CC}=15V	20	40		20	40		mA
		V_{IN}+=+1V, V_{IN}-=0V, V_{CC}=15V, over temp.	10	20		10	20		
	Output current sink	V_{IN}-=+1V, V_{IN}+=0V, V_{CC}=15V	10	20		10	20		
		V_{IN}-=+1V, V_{IN}+=0V, V_{CC}=15V, over temp.	5	8		5	8		
		V_{IN}-=+1V, V_{IN}+=0V, V_O=200mV	12	50		12	50		µA
I_{SC}	Short-circuit current[4]		10	40	60	10	40	60	mA
GBW	Unity gain bandwidth			1			1		MHz
SR	Slew rate			0.3			0.3		V/µs
V_{NOISE}	Input noise voltage	f=1kHz		40			40		nV/√Hz
V_{DIFF}	Differential input voltage[3]				V_{CC}			V_{CC}	V

DC ELECTRICAL CHARACTERISTICS (Continued)

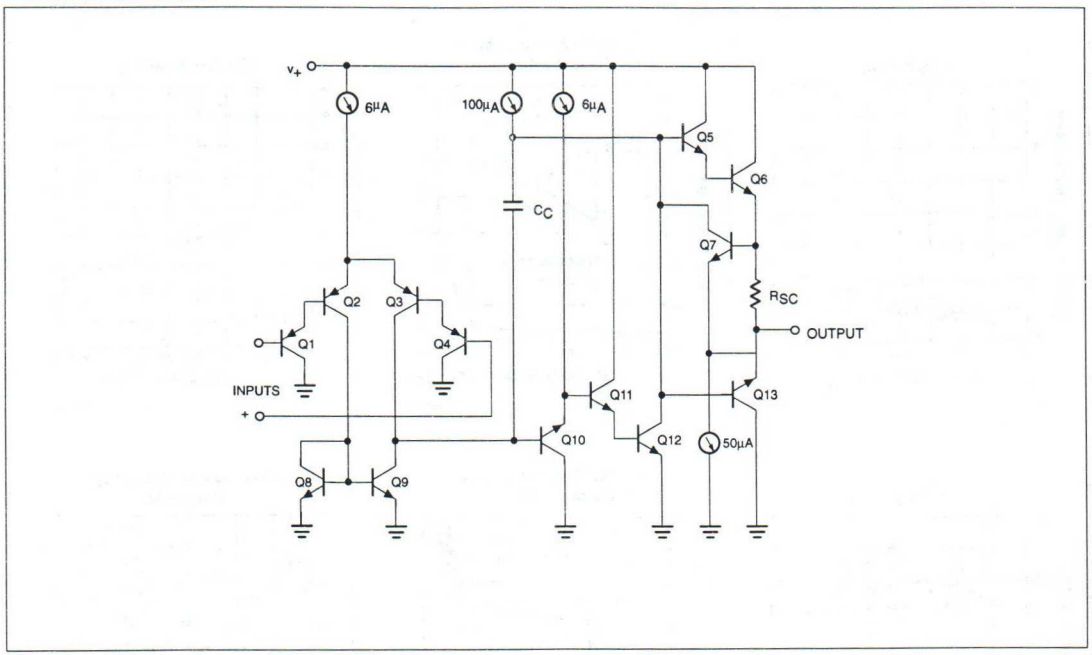
V_{CC}=5V, T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM324A			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω		±2	±3	mV
		R_S=0Ω, over temp.			±5	
$\Delta V_{OS}/\Delta T$	Temperature drift	R_S=0Ω, over temp.		7	30	µV/°C
I_{BIAS}	Input current[2]	I_{IN}(+) or I_{IN}(-)		45	100	nA
		I_{IN}(+) or I_{IN}(-), over temp.		40	200	
$\Delta I_{BIAS}/\Delta T$	Temperature drift	Over temp.		50		pA/°C
I_{OS}	Offset current	I_{IN}(+)-I_{IN}(-)		±5	±30	nA
		I_{IN}(+)-I_{IN}(-), over temp.			±75	
$\Delta I_{OS}/\Delta T$	Temperature drift	Over temp.		10	300	pA/°C
V_{CM}	Common-mode voltage range[3]	V_{CC}≤30V	0		V_{CC}-1.5	V
		V_{CC}≤30V, over temp.	0		V_{CC}-2	V
CMRR	Common-mode rejection ratio	V_{CC}=30V	65	85		dB
V_{OUT}	Output voltage swing	R_L=2kΩ, V_{CC}=30V, over temp.	26			V
V_{OH}	Output voltage high	R_L≤10kΩ, V_{CC}=30V, over temp.	27	28		V
V_{OL}	Output voltage low	R_L≤10kΩ, over temp.		5	20	mV
I_{CC}	Supply current	R_L=∞, V_{CC}=30V, over temp.		1.5	3	mA
		R_L=∞, over temp.		0.7	1.2	mA
A_{VOL}	Large-signal voltage gain	V_{CC}=15V (for large V_O swing), R_L≥2kΩ	25	100		V/mV
		V_{CC}=15V (for large V_O swing), R_L≥2kΩ, over temp.	15			V/mV
	Amplifier-to-amplifier coupling[5]	f=1kHz to 20kHz, input referred		-120		dB
PSRR	Power supply rejection ratio	R_S≤0Ω	65	100		dB
I_{OUT}	Output current source	V_{IN}+=+1V, V_{IN}-=0V, V_{CC}=15V	20	40		mA
		V_{IN}+=+1V, V_{IN}-=0V, V_{CC}=15V, over temp.	10	20		mA
	Output current sink	V_{IN}-=+1V, V_{IN}+=0V, V_{CC}=15V	10	20		mA
		V_{IN}-=+1V, V_{IN}+=0V, V_{CC}=15V, over temp.	5	8		mA
		V_{IN}-=+1V, V_{IN}+=0V, V_O=200mV	12	50		µA
I_{SC}	Short-circuit current[4]		10	40	60	mA
V_{DIFF}	Differential input voltage[3]				V_{CC}	V
GBW	Unity gain bandwidth			1		MHz
SR	Slew rate			0.3		V/µs
V_{NOISE}	Input noise voltage	f=1kHz		40		nV/√Hz

NOTES:

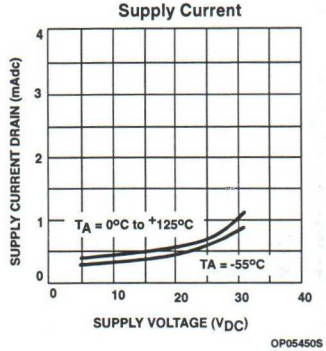
1. $V_O \approx 1.4V_{DC}$, R_S=0Ω with V_{CC} from 5V to 30V and over full input common-mode range ($0V_{DC}$+ to V_{CC} -1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC} -1.5, but either or both inputs can go to +32V without damage.
4. Short-circuits from the output to V_{CC} can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V_{CC}. At values of supply voltage in excess of $+15V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of coupling increases at higher frequencies.

EQUIVALENT CIRCUIT



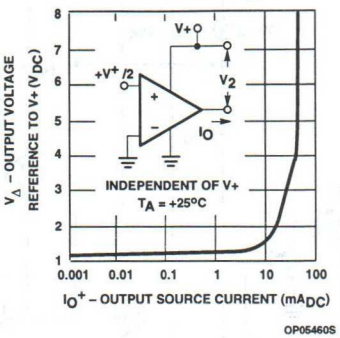
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current



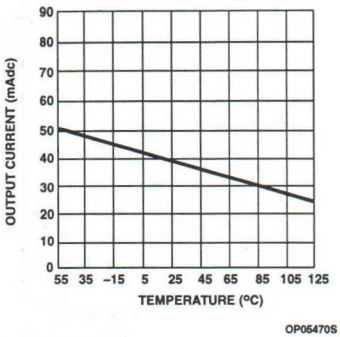
OP05450S

Output Characteristics
Current Sourcing



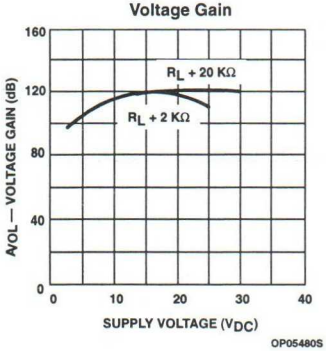
OP05460S

Current Limiting



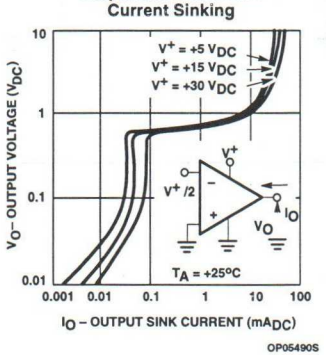
OP05470S

Voltage Gain



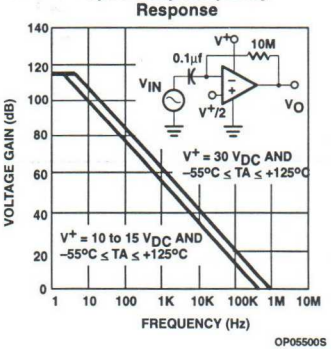
OP05480S

Output Characteristics
Current Sinking



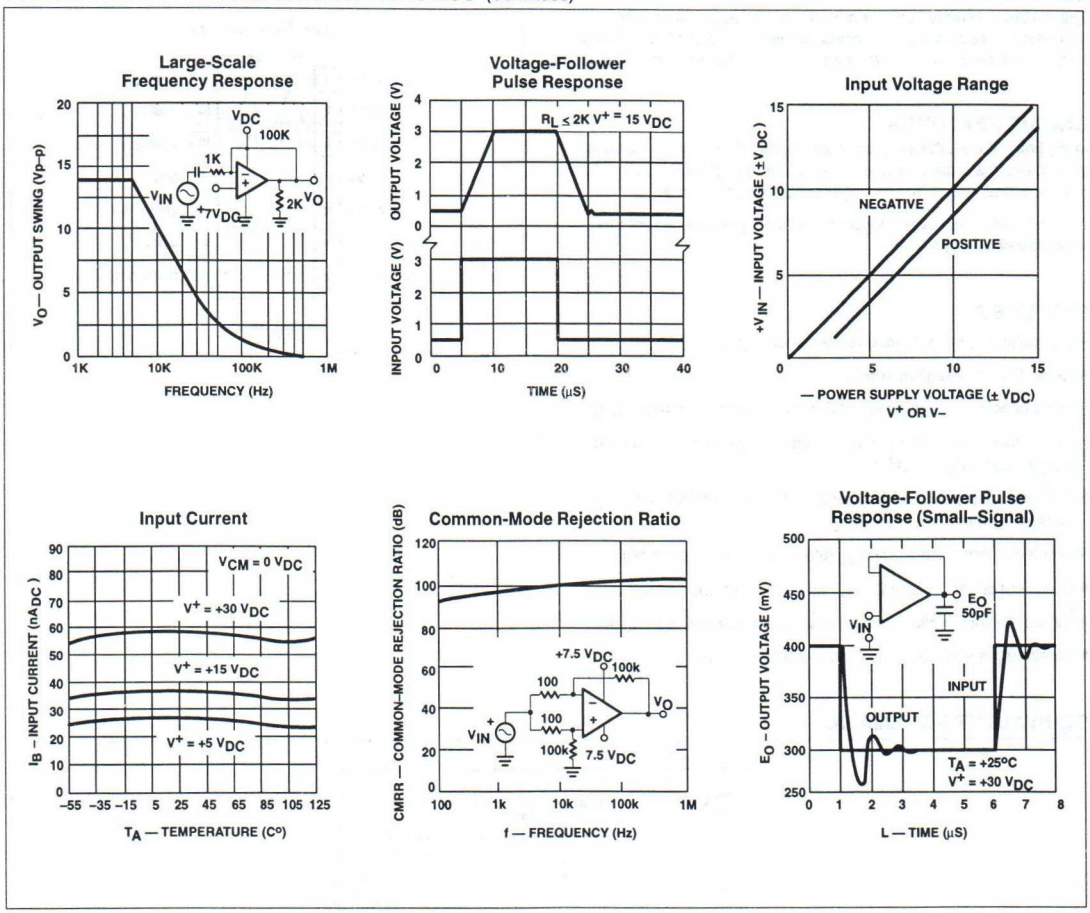
OP05490S

Open–Loop Frequency
Response

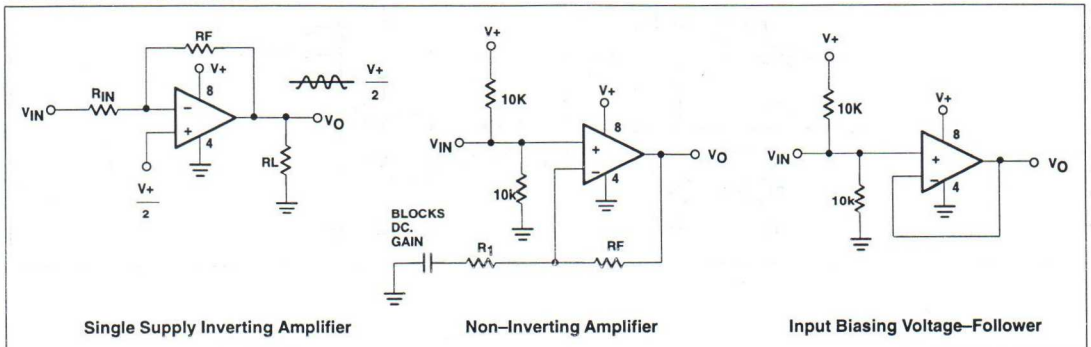


OP05500S

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TYPICAL APPLICATIONS



Single Supply Inverting Amplifier

Non–Inverting Amplifier

Input Biasing Voltage–Follower

Low power quad operational amplifier

AU2902

DESCRIPTION

The AU2902 consists of four independent, high-gain, internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages.

UNIQUE FEATURES

In the linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

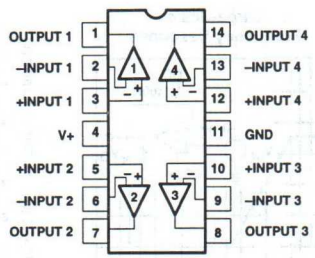
The unity gain crossover frequency and the input bias current are temperature-compensated.

FEATURES

- Internally frequency-compensated for unity gain
- Large DC voltage gain: 100dB
- Wide bandwidth (unity gain): 1MHz (temperature-compensated)
- Wide power supply range Single supply: $3V_{DC}$ to $30V_{DC}$ or dual supplies: $\pm1.5V_{DC}$ to $\pm15V_{DC}$
- Very low supply current drain: essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)
- Low input bias current: $45nA_{DC}$ (temperature-compensated)
- Low input offset voltage: $2mV_{DC}$ and offset current: $5nA_{DC}$
- Differential input voltage range equal to the power supply voltage
- Large output voltage: $0V_{DC}$ to V_{CC}-$1.5V_{DC}$ swing

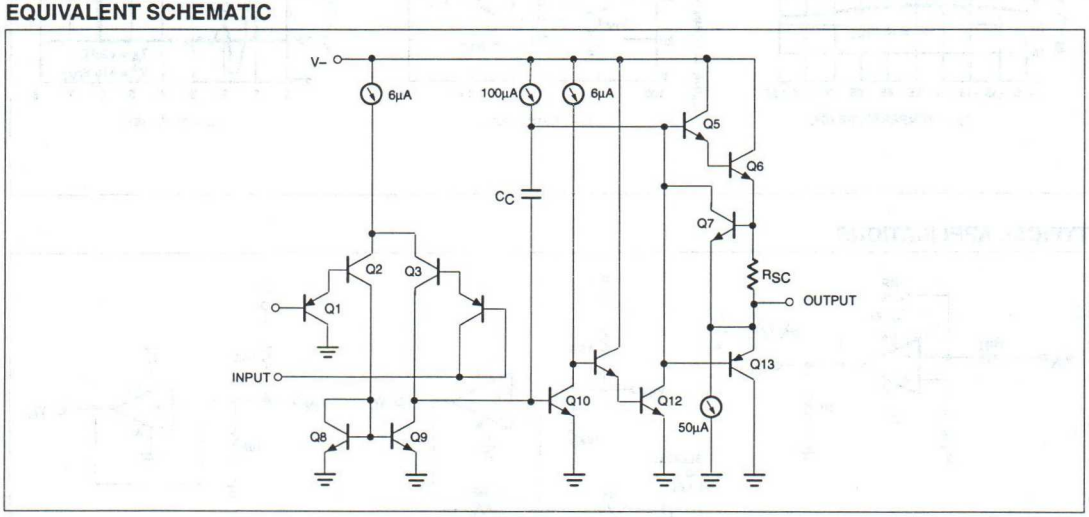
PIN CONFIGURATION

D and N Packages



Top View

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	-40 to +125°C	AU2902N	0405B
14-Pin Plastic Small Outline (SO) Package	-40 to +125°C	AU2902D	0175D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	32 or ±16	V_{DC}
V_{IN}	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	–0.3 to +32	V_{DC}
P_{DMAX}	Maximum power dissipation, T_A=25°C(still–air)[1]		
	N package	1420	mW
	D package	1040	mW
	Output short–circuit to GND one amplifier V_{CC}<15V_{DC} and T_A=25°C	Continuous	
I_{IN}	Input current (V_{IN}<–0.3V)[3]	50	mA
T_A	Operating ambient temperature range		
	AU2902	–40 to +125	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C at the following rates:
   N package at 11.4mW/°C
   D package at 8.3mW/°C
2. Short–circuits from the output to V_{CC}+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA, independent of the magnitude of V_{CC}. At values of supply voltage in excess of +15V_{DC} continuous short–circuits can exceed the power dissipation ratings and cause eventual destruction.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector–base junction of the input PNP transistors becoming forward biased and thereby acting as input bias clamps. In addition, there is also lateral NPN parasitic transistor action on the IC chip. This action can cause the output voltages of the op amps to go to the V+ rail (or to ground for a large overdrive) during the time that the input is driven negative.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=5V, T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	AU2902			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω		±2	±7	mV
		R_S=0Ω, over temp.			±9	
$\Delta V_{OS}/\Delta T$	Temperature drift	R_S=0Ω, over temp.		7		µV/°C
I_{BIAS}	Input current[2]	I_{IN}(+) or I_{IN}(–)		45	250	nA
		I_{IN}(+) or I_{IN}(–), over temp.		40	500	
$\Delta I_{BIAS}/\Delta T$	Temperature drift	Over temp.		50		pA/°C
I_{OS}	Offset current	I_{IN}(+)–I_{IN}(–)		±5	±50	nA
		I_{IN}(+)–I_{IN}(–), over temp.			±150	
$\Delta I_{OS}/\Delta T$	Temperature drift	Over temp.		10		pA/°C
V_{CM}	Common–mode voltage range[3]	V_{CC}≤30V	0		V_{CC}–1.5	V
		V_{CC}≤30V, over temp.	0		V_{CC}–2	V
CMRR	Common–mode rejection ratio	V_{CC}=30V	65	70		dB
V_{OUT}	Output voltage swing	R_L=2kΩ, V_{CC}=30V, over temp.	26			V
V_{OH}	Output voltage high	R_L≥10kΩ, V_{CC}=30V, over temp.	27	28		V

DC ELECTRICAL CHARACTERISTICS (Continued)

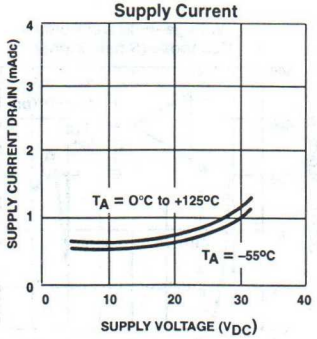
SYMBOL	PARAMETER	TEST CONDITIONS	AU2902			UNIT
			Min	Typ	Max	
V_{OL}	Output voltage low	$R_L \leq 10k\Omega$, V_{CC}=5V, over temp.		5	20	mV
I_{CC}	Supply current	R_L=∞, V_{CC}=30V, over temp.		1.5	3	mA
		R_L=∞, V_{CC}=5V, over temp.		0.7	1.2	
A_{VOL}	Large–signal voltage gain	V_{CC}=15V (for large V_O swing), $R_L \geq 2k\Omega$	25	100		V/mV
		V_{CC}=15V (for large V_O swing), $R_L \geq 2k\Omega$, over temp.	15			
	Amplifier–to–amplifier coupling[5]	f=1kHz to 20kHz, input referred		–120		dB
PSRR	Power supply rejection ratio	R_S=0Ω	65	100		dB
I_{OUT}	Output current Source	V_{IN}+=+1V, V_{IN}–=0V, V_{CC}=15V	20	40		mA
		V_{IN}+=+1V, V_{IN}–=0V, V_{CC}=15V, over temp.	10	20		
	Output current Sink	V_{IN}–=+1V, V_{IN}+=0V, V+=15V	10	20		
		V_{IN}–=+1V, V_{IN}+=0V, V_{CC}=15V, over temp.	5	8		
		V_{IN}–=+1V, V_{IN}+=0V, V_O=200mV	12	50		µA
I_{SC}	Short–circuit current[4]		10	40	60	mA
V_{DIFF}	Differential input voltage[3]				V_{CC}	V
GBW	Unity gain bandwidth			1		MHz
SR	Slew rate			0.3		V/µs
V_{NOISE}	Input noise voltage	f=1kHz		40		nV/√Hz

NOTES:

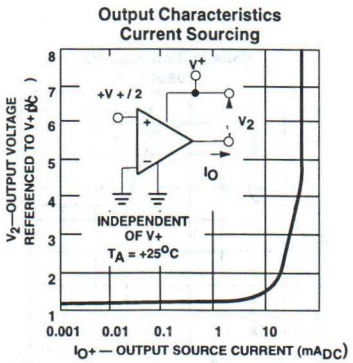
1. $V_O \approx 1.4V_{DC}$, R_S=0Ω with V_{CC} from 5V to 30V and over full input common–mode range ($0V_{DC}$+ to V_{CC} –1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common–mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common–mode voltage range is V_{CC} –1.5, but either or both inputs can go to +32V without damage.
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5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of coupling increases at higher frequencies.

TYPICAL PERFORMANCE CHARACTERISTICS

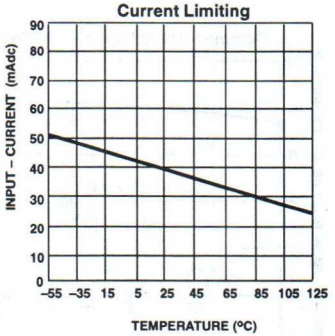
Supply Current



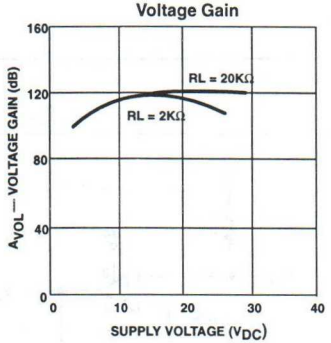
Output Characteristics
Current Sourcing



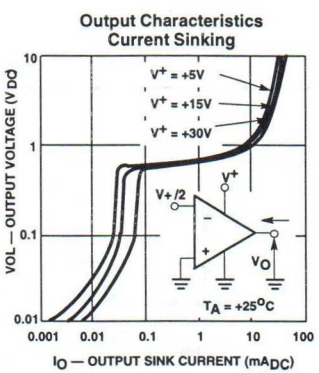
Current Limiting



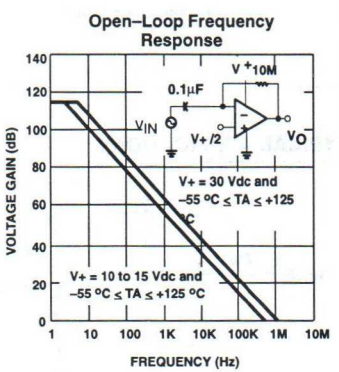
Voltage Gain



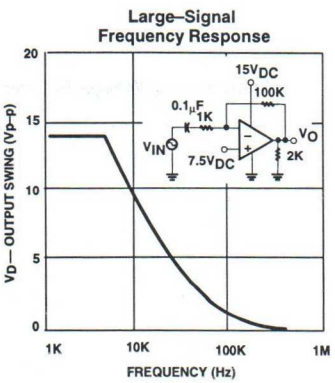
Output Characteristics
Current Sinking



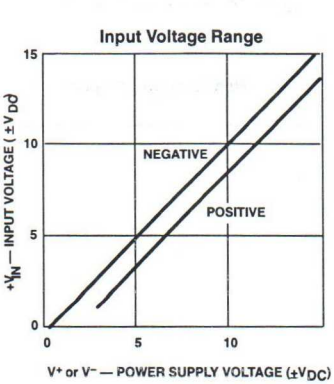
Open–Loop Frequency
Response



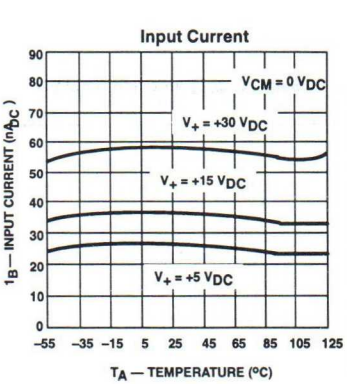
Large–Signal
Frequency Response



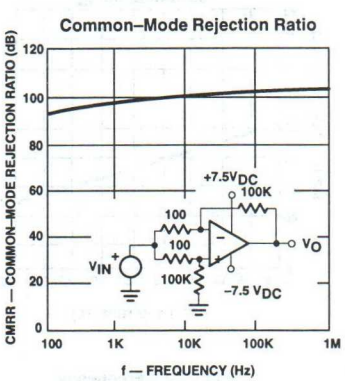
Input Voltage Range

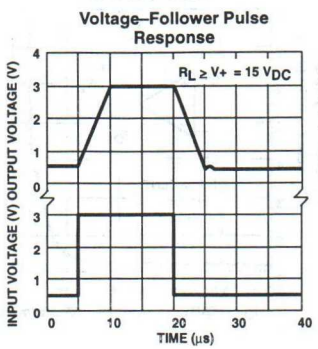


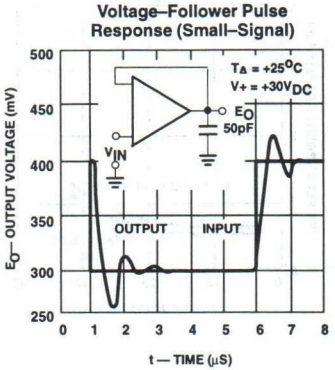
Input Current



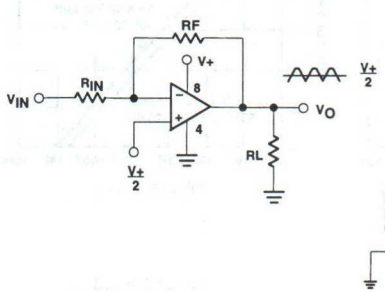
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



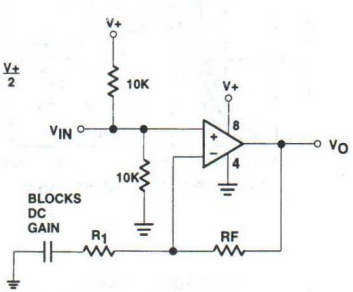




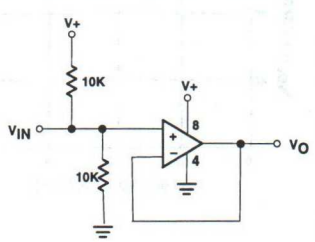
TYPICAL APPLICATIONS



Single Supply Inverting Amplifier



Non–Inverting Amplifier



Output Biasing Voltage–Follower

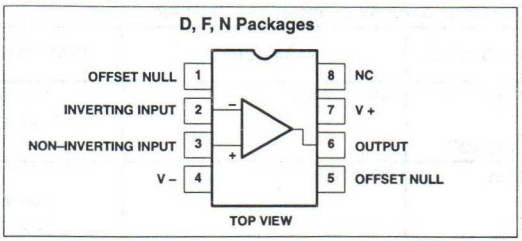
General purpose operational amplifier

μA741/μA741C/SA741C

DESCRIPTION

The μA741 is a high performance operational amplifier with high open-loop gain, internal compensation, high common mode range and exceptional temperature stability. The μA741 is short-circuit-protected and allows for nulling of offset voltage.

PIN CONFIGURATION



FEATURES

- Internal frequency compensation
- Short circuit protection
- Excellent temperature stability
- High input voltage range

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	μA741N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	μA741CN	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA741CN	0404B
8-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	μA741F	0580A
8-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	μA741CF	0580A
8-Pin Small Outline (SO) Package	0 to +70°C	μA741CD	0174C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage		
	μA741C	±18	V
	μA741	±22	V
P_D	Internal power dissipation		
	D package	780	mW
	N package	1170	mW
	F package	800	mW
V_{IN}	Differential input voltage	±30	V
V_{IN}	Input voltage[1]	±15	V
I_{SC}	Output short-circuit duration	Continuous	
T_A	Operating temperature range		
	μA741C	0 to +70	°C
	SA741C	-40 to +85	°C
	μA741	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	μA741			μA741C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	R_S=10kΩ		1.0	5.0		2.0	6.0	mV
		R_S=10kΩ, over temp.		1.0	6.0			7.5	mV
$\Delta V_{OS}/\Delta T$				10			10		μV/°C
I_{OS}	Offset current			20	200		20	200	nA
		Over temp.						300	nA
		T_A=+125°C		7.0	200				nA
		T_A=-55°C		20	500				nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_{BIAS}	Input bias current			80	500		80	500	nA
		Over temp.						800	nA
		T_A=+125°C		30	500				nA
		T_A=-55°C		300	1500				nA
$\Delta I_B/\Delta T$				1			1		nA/°C
V_{OUT}	Output voltage swing	R_L=10kΩ	±12	±14		±12	±14		V
		R_L=2kΩ, over temp.	±10	±13		±10	±13		V
A_{VOL}	Large-signal voltage gain	R_L=2kΩ, V_O=±10V	50	200		20	200		V/mV
		R_L=2kΩ, V_O=±10V, over temp.	25			15			V/mV
	Offset voltage adjustment range			±30			±30		mV
PSRR	Supply voltage rejection ratio	R_S≤10kΩ					10	150	μV/V
		R_S≤10kΩ, over temp.		10	150				μV/V
CMRR	Common-mode rejection ratio					70	90		dB
		Over temp.	70	90					dB
I_{CC}	Supply current			1.4	2.8		1.4	2.8	mA
		T_A=+125°C		1.5	2.5				mA
		T_A=-55°C		2.0	3.3				mA
V_{IN}	Input voltage range	(μA741, over temp.)	±12	±13		±12	±13		V
R_{IN}	Input resistance		0.3	2.0		0.3	2.0		MΩ
P_D	Power consumption			50	85		50	85	mW
		T_A=+125°C		45	75				mW
		T_A=-55°C		45	100				mW
R_{OUT}	Output resistance			75			75		Ω
I_{SC}	Output short-circuit current		10	25	60	10	25	60	mA

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±15V, unless otherwise specified.

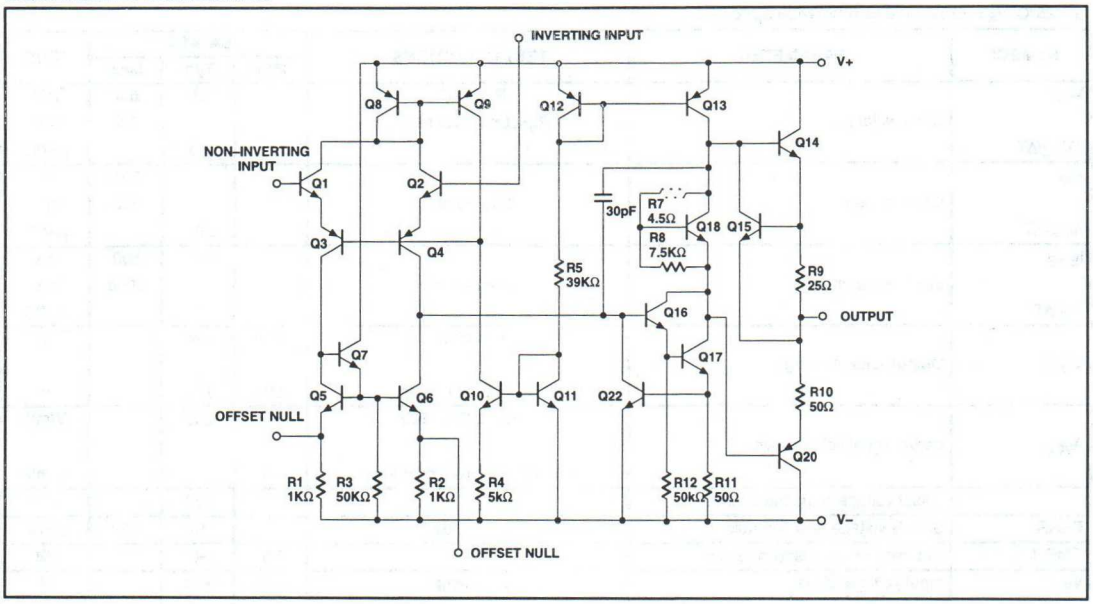
SYMBOL	PARAMETER	TEST CONDITIONS	SA741C			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	R_S=10kΩ		2.0	6.0	mV
		R_S=10kΩ, over temp.			7.5	mV
$\Delta V_{OS}/\Delta T$				10		μV/°C
I_{OS}	Offset current	Over temp.		20	200	nA
					500	nA
$\Delta I_{OS}/\Delta T$				200		pA/°C
I_{BIAS}	Input bias current	Over temp.		80	500	nA
					1500	nA
$\Delta I_B/\Delta T$				1		nA/°C
V_{OUT}	Output voltage swing	R_L=10kΩ	±12	±14		V
		R_L=2kΩ, over temp.	±10	±13		V
A_{VOL}	Large-signal voltage gain	R_L=2kΩ, V_O=±10V	20	200		V/mV
		R_L=2kΩ, V_O=±10V, over temp.	15			V/mV
	Offset voltage adjustment range			±30		mV
PSRR	Supply voltage rejection ratio	R_S≤10kΩ		10	150	μV/V
CMRR	Common mode rejection ration		70	90		dB
V_{IN}	Input voltage range	Over temp.	±12	±13		V
R_{IN}	Input resistance		0.3	2.0		MΩ
P_d	Power consumption			50	85	mW
R_{OUT}	Output resistance			75		Ω
I_{SC}	Output short-circuit current			25		mA

AC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_S = ±15V, unless otherwise specified.

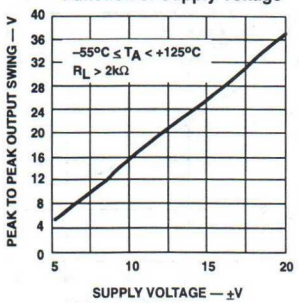
SYMBOL	PARAMETER	TEST CONDITIONS	μA741, μA741C			UNIT
			Min	Typ	Max	
R_{IN}	Parallel input resistance	Open-loop, f=20Hz	0.3			MΩ
C_{IN}	Parallel input capacitance	Open-loop, f=20Hz		1.4		pF
	Unity gain crossover frequency	Open-loop		1.0		MHz
	Transient response unity gain	V_{IN}=20mV, R_L=2kΩ, C_L≤100pF				
t_R	Rise time			0.3		μs
	Overshoot			5.0		%
SR	Slew rate	C≤100pF, R_L≥2kΩ, V_{IN}=±10V		0.5		V/μs

EQUIVALENT SCHEMATIC

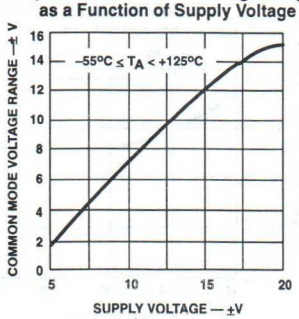


TYPICAL PERFORMANCE CHARACTERISTICS

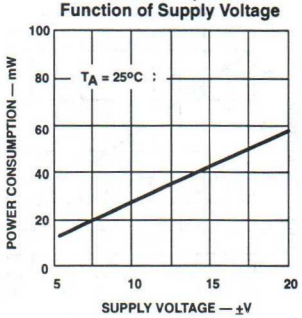
Output Voltage Swing as a Function of Supply Voltage



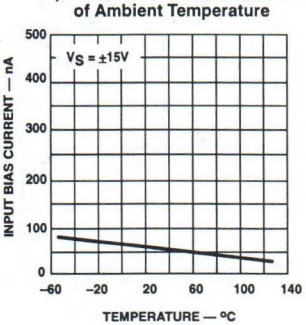
Input Common–Mode Voltage Range as a Function of Supply Voltage



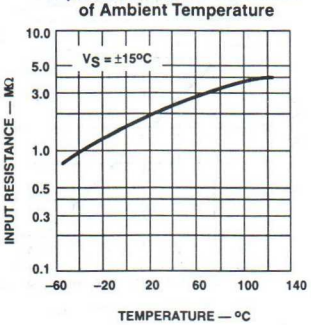
Power Consumption as a Function of Supply Voltage



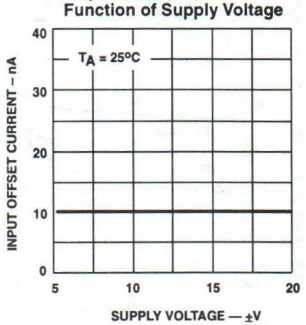
Input Bias Current as a Function of Ambient Temperature



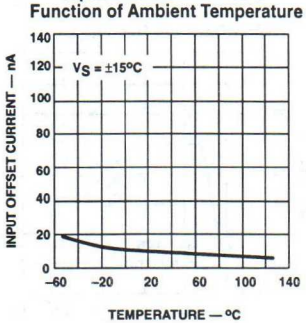
Input Resistance as a Function of Ambient Temperature



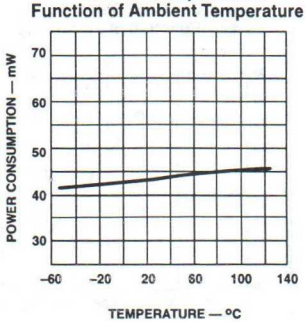
Input Offset Current as a Function of Supply Voltage



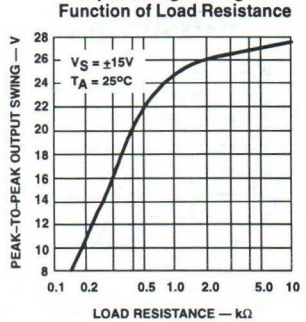
Input Offset Current as a Function of Ambient Temperature



Power Consumption as a Function of Ambient Temperature

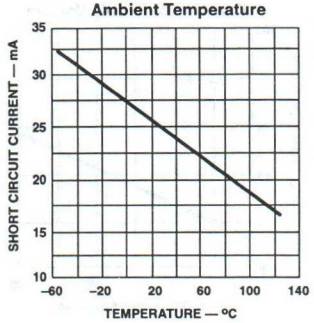


Output Voltage Swing as a Function of Load Resistance

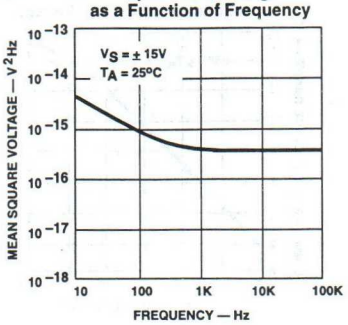


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

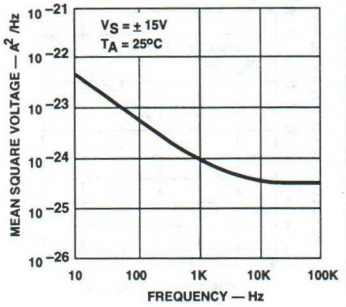
Output Short–Circuit Current as a Function of Ambient Temperature



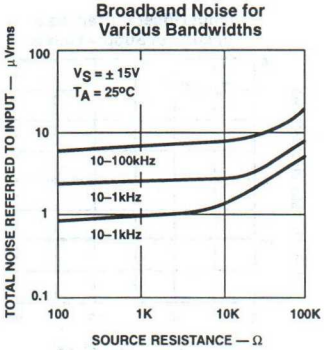
Input Noise Voltage as a Function of Frequency



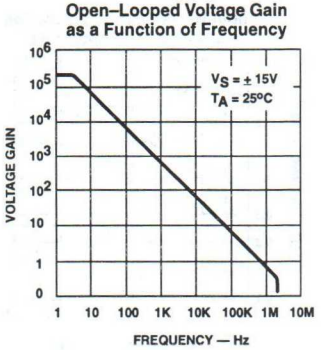
Input Noise Current as a Function of Frequency



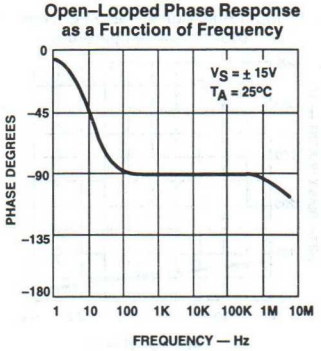
Broadband Noise for Various Bandwidths



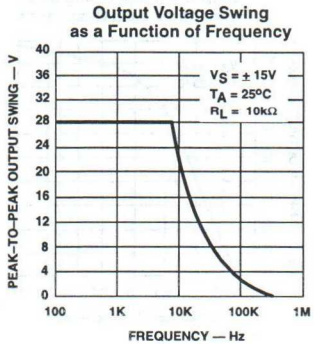
Open–Looped Voltage Gain as a Function of Frequency



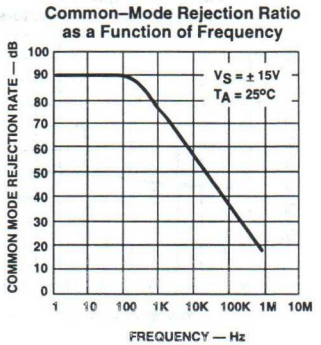
Open–Looped Phase Response as a Function of Frequency



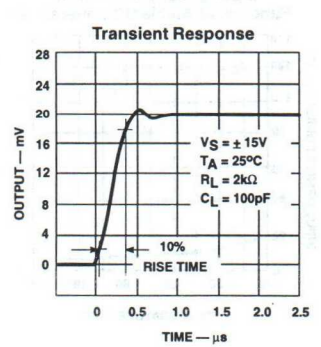
Output Voltage Swing as a Function of Frequency



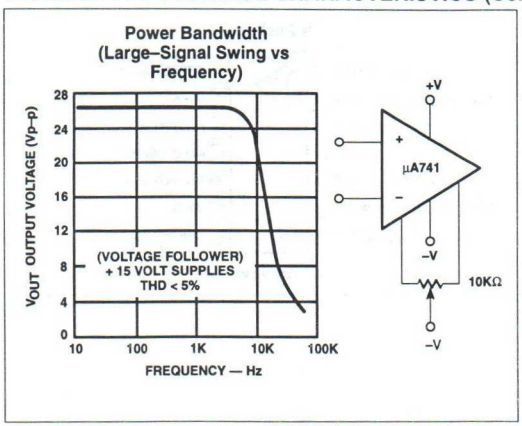
Common–Mode Rejection Ratio as a Function of Frequency



Transient Response



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



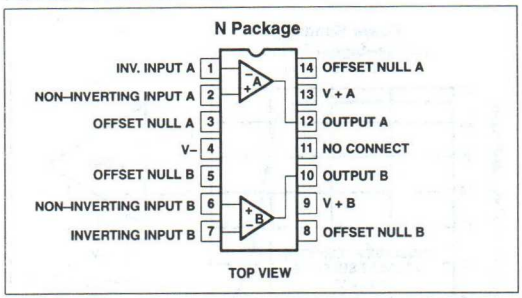
Dual operational amplifier

µA747C

DESCRIPTION

The 747 is a pair of high-performance monolithic operational amplifiers constructed on a single silicon chip. High common-mode voltage range and absence of "latch-up" make the 747 ideal for use as a voltage-follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The 747 is short-circuit protected and requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed-loop applications. For single amplifier performance, see µA741 data sheet.

PIN CONFIGURATION



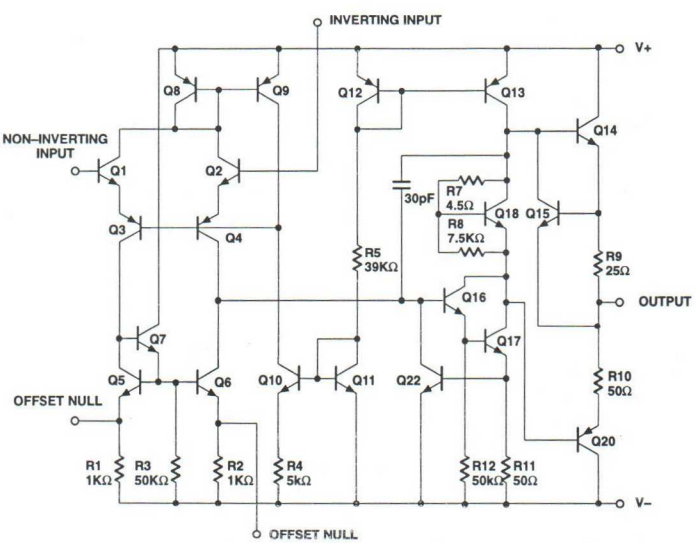
FEATURES

- No frequency compensation required
- Short-circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- Low power consumption
- No latch-up

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic DIP	0°C to 70°C	µA747CN	0405B

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±18	V
$P_{D\ MAX}$	Maximum power dissipation T_A=25°C (still air)[1]	1500	mW
V_{IN}	Differential input voltage	±30	V
V_{IN}	Input voltage[2]	±15	V
	Voltage between offset null and V-	±0.5	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating temperature range	0 to +70	°C
T_{SOLD}	Lead temperature (soldering, 10sec)	300	°C
I_{SC}	Output short-circuit duration	Indefinite	

NOTES:
1. Derate above 25°C at the following rates:
   N package at 12mW/°C
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

DC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC} = ±15V unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	µA747C			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	R_S≤10kΩ		2.0	6.0	mV
		R_S≤10kΩ, over temp.		3.0	7.5	mV
$\Delta V_{OS}/\Delta T$				10		µV/°C
I_{OS}	Offset current			20	200	nA
		Over temperature		7.0	300	nA
$\Delta I_{OS}/\Delta T$				200		pA/°C
I_{BIAS}	Input current			80	500	nA
		Over temperature		30	800	nA
$\Delta I_B/\Delta T$				1		nA/°C
V_{OUT}	Output voltage swing	R_L≥2kΩ, over temp.	±10	±13		V
		R_L≥10kΩ, over temp.	±12	±14		V
I_{CC}	Supply current each side			1.7	2.8	mA
		Over temperature		2.0	3.3	mA
P_d	Power consumption			50	85	mW
		Over temperature		60	100	mW
C_{IN}	Input capacitance			1.4		pF
	Offset voltage adjustment range			±15		mV
R_{OUT}	Output resistance			75		Ω
	Channel separation			120		dB
PSRR	Supply voltage rejection ratio	R_S≤10kΩ, over temp.		30	150	µV/V
A_{VOL}	Large-signal voltage gain (DC)	R_L≥2kΩ, V_{OUT}=±10V	25,000			V/V
		Over temperature	15,000			V/V
CMRR	Common-mode rejection ratio	R_S≤10kΩ, V_{CM}=±12V Over temperature	70			dB

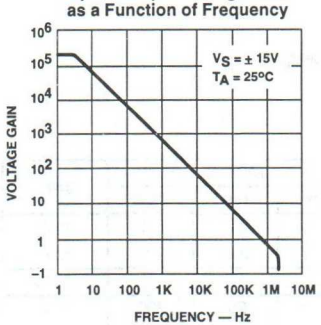
AC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_S = ±15V unless otherwise specified.

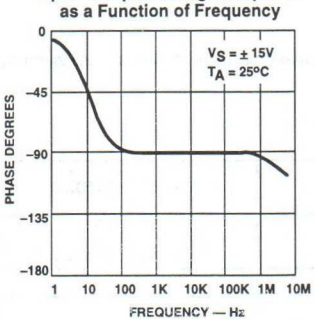
SYMBOL	PARAMETER	TEST CONDITIONS	µA747C			UNIT
			Min	Typ	Max	
t_R	Transient response	V_{IN}=20mV, R_L=2kΩ, C_L<100pF				
	Rise time	Unity gain C_L≤100pF		0.3		µs
	Overshoot	Unity gain C_L≤100pF		5.0		%
SR	Slew rate	R_L>2kΩ		0.5		V/µs

TYPICAL PERFORMANCE CHARACTERISTICS

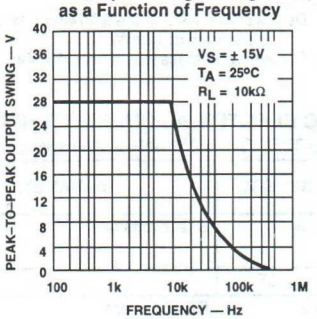
Open–Looped Voltage Gain as a Function of Frequency



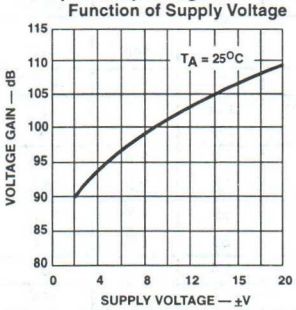
Open–Looped Voltage Response as a Function of Frequency



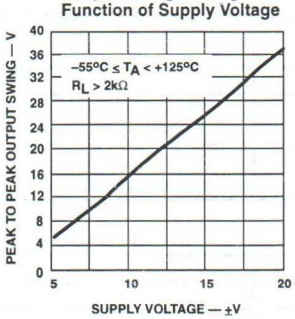
Output Voltage Swing as a Function of Frequency



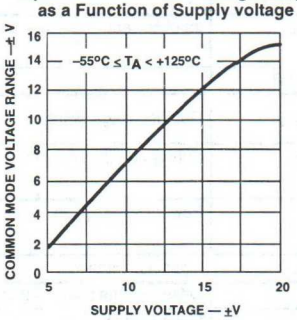
Open–Loop Voltage Gain as a Function of Supply Voltage



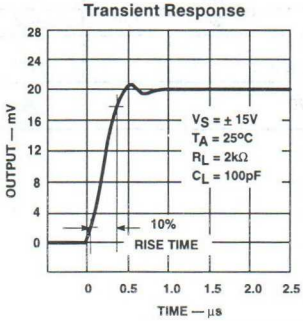
Output Voltage Swing as a Function of Supply Voltage



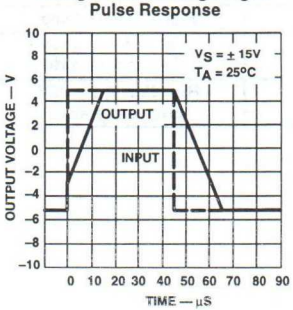
Input Common–Mode Voltage Range as a Function of Supply voltage



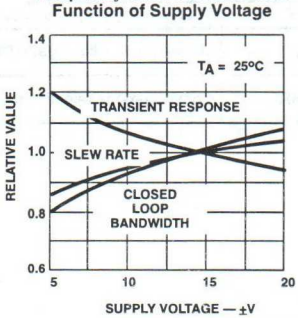
Transient Response



Voltage-follower Large-Signal Pulse Response

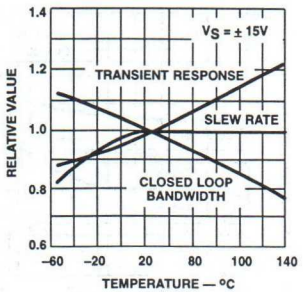


Frequency Characteristics as a Function of Supply Voltage

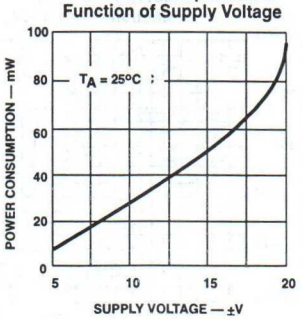


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

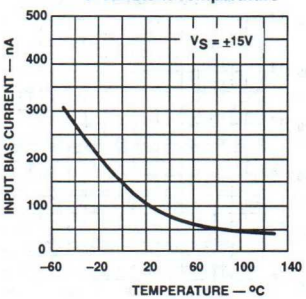
Frequency Characteristics as a Function of Ambient Temperature



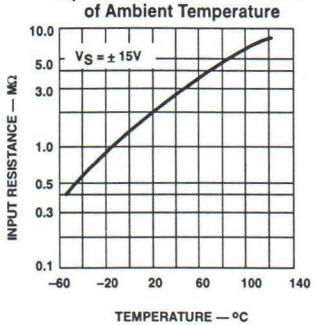
Power Consumption as a Function of Supply Voltage



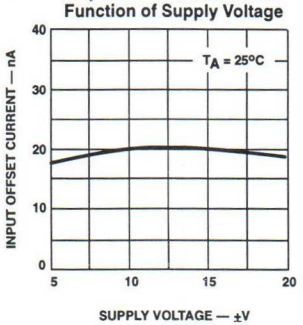
Input Bias Current as a Function of Ambient Temperature



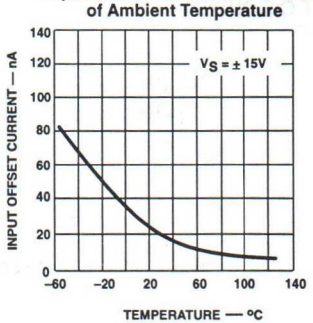
Input Resistance as a Function of Ambient Temperature



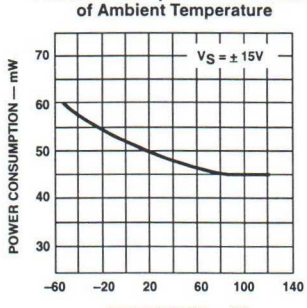
Input Offset Current as a Function of Supply Voltage



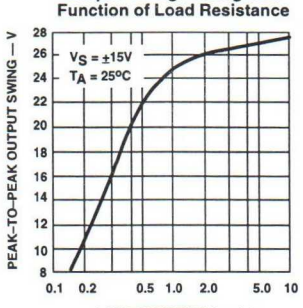
Input Offset Current as a Function of Ambient Temperature



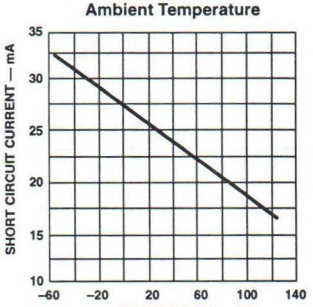
Power Consumption as a Function of Ambient Temperature



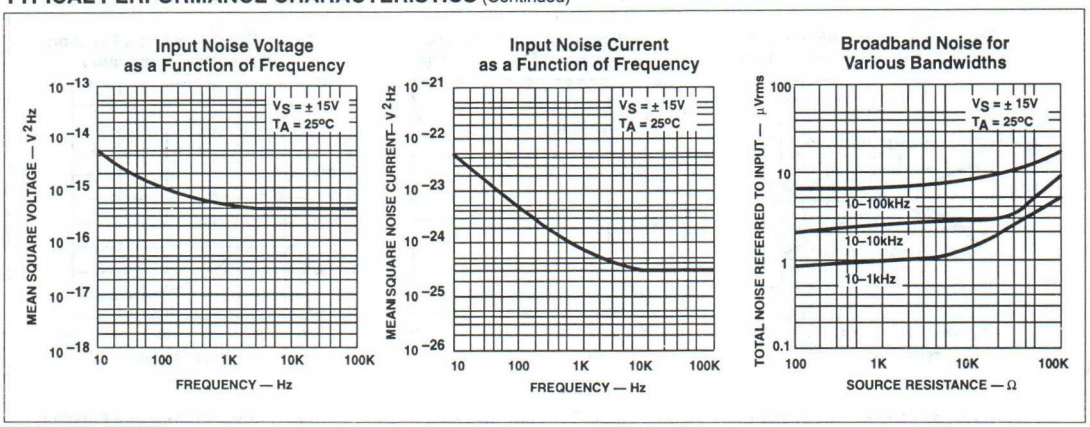
Output Voltage Swing as a Function of Load Resistance



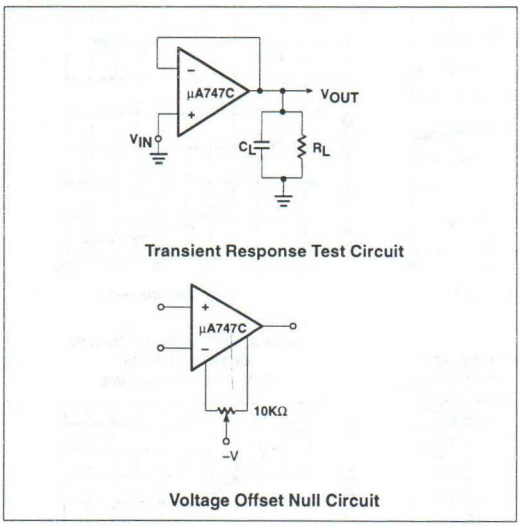
Output Short-Circuit Current as a Function of Ambient Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TEST CIRCUITS



General purpose operational amplifier

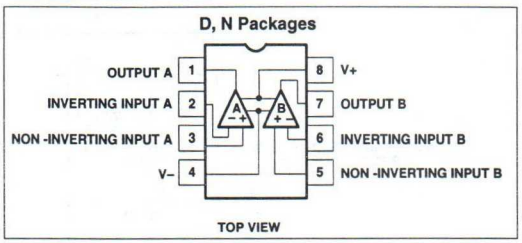
MC/SA1458/MC1558

DESCRIPTION

The MC1458 is a high-performance operational amplifier with high open-loop gain, internal compensation, high common-mode range and exceptional temperature stability. The MC1458 is short-circuit protected.

The MC1458/SA1458/MC1558 consists of a pair of 741 operational amplifiers on a single chip.

PIN CONFIGURATION



FEATURES

- Internal frequency compensation
- Short-circuit protection
- Excellent temperature stability
- High input voltage range
- No latch-up
- 1558/1458 are 2 "op amps" in space of one 741 package

ORDERING INFORMATION

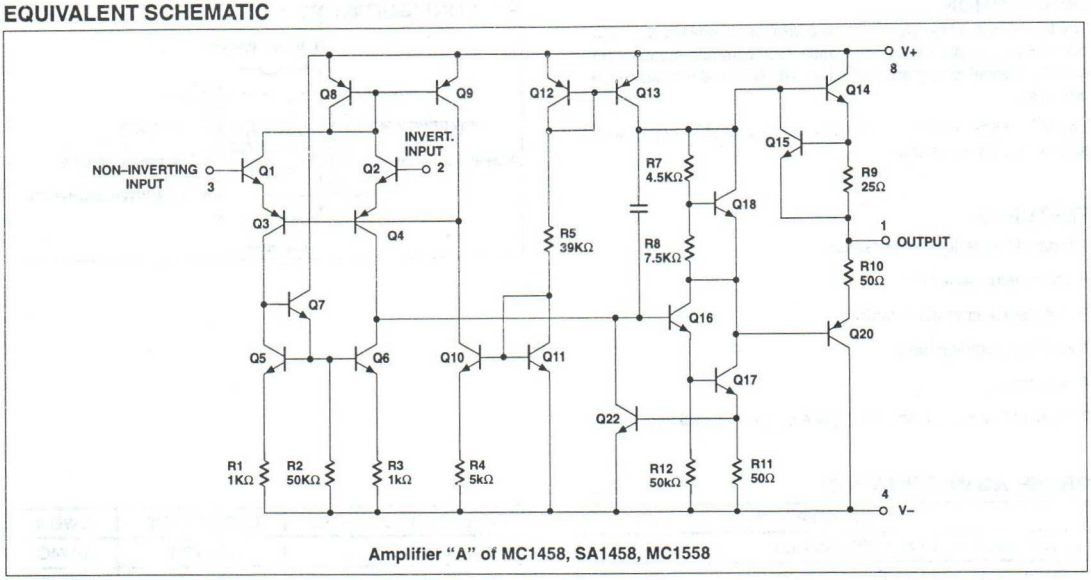
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	MC1458D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	MC1458N	0404B
8-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA1458D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA1458N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	MC1558N	0404B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage		
	MC1458	±18	V
	SA1458	±18	V
	MC1558	±22	V
T_J	Junction temperature	+150	°C
$P_{D\ MAX}$	Maximum power dissipation, T_A=25°C (still-air)[1]		
	N package	1160	mW
	D package	780	mW
V_{DIFF}	Differential input voltage	±30	V
V_{IN}	Input voltage[2]	±15	V
	Output short-circuit duration	Continuous	
T_A	Operating ambient temperature range		
	MC1458	0 to +70	°C
	SA1458	-40 to +85	°C
	MC1558	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. The following derating factors should be applied above 25°C; N package at 9.3mW/°C; D package at 6.2mW/°C
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT SCHEMATIC



Amplifier "A" of MC1458, SA1458, MC1558

DC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_S=±15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1558			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	R_S=10kΩ		1.0	5.0	mV
		R_S=10kΩ, over temperature			6.0	mV
ΔV_{OS}	Offset voltage	Over temperature		10		µV/°C
I_{OS}	Offset current			20	200	nA
		Over temperature			500	nA
ΔI_{OS}	Offset current	Over temperature		0.10		nA/°C
I_{BIAS}	Input bias current			80	500	nA
		Over temperature			1500	nA
ΔI_{BIAS}	Bias current	Over temperature		1.0		nA/°C
V_{OUT}	Output voltage swing	R_L=10kΩ, over temperature	±12	±14		V
		R_L=2kΩ, over temperature	±10	±13		
A_{VOL}	Large-signal voltage gain	R_L=2kΩ,V_O=±10V	50	100		V/mV
		R_L=2kΩ, V_O=± temperature	20			
	Offset voltage adjustment range			±30		mV
PSRR	Power supply rejection ratio	R_S≤10kΩ		30	150	µV/V
CMRR	Common mode rejection ratio		70	90		dB
I_{CC}	Supply current			2.3	5.0	mA
V_{IN}	Input voltage range		±12	±13		V
P_D	Power consumption			70	150	mW
	Channel separation			120		dB
R_{OUT}	Output resistance			75		Ω
I_{SC}	Output short-circuit current		10	25	60	mA

DC ELECTRICAL CHARACTERISTICS (Continued)

T_A=25°C V_{CC}=±15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1458			SA1458			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	R_S=10kΩ		2.0	6.0		2.0	6.0	mV
		R_S=10kΩ, over temp.			7.5			7.5	mV
ΔV_{OS}	Offset voltage	Over temperature		12			12		µV/°C
I_{OS}	Offset current			20	200		20	200	nA
		Over temperature			300			500	nA
ΔI_{OS}	Offset current	Over temperature		0.10			0.10		nA/°C
I_{BIAS}	Input bias current			80	500		80	500	nA
		Over temperature			800			1500	nA
ΔI_{BIAS}	Bias current	Over temperature		1.0			1.0		nA/°C
V_{OUT}	Output voltage swing	R_L=10kΩ, over temp.	±12	±14		±12	±14		V
		R_L=2kΩ, over temp.	±10	±13		±10	±13		
A_{VOL}	Large-signal voltage gain	R_L=2kΩ, V_O=±10V	25	200		20	200		V/mV
		R_L=2kΩ, V_O=±10V, Over temperature	15			15			V/mV
	Offset voltage adjustment range			±30			±30		mV
PSRR	Power supply rejection ratio	R_S≤10kΩ		30	150		30	150	µV/V
CMRR	Common-mode rejection ratio		70	90		70	90		dB
I_{CC}	Supply current			2.3	5.6		2.3	5.6	mA
V_{IN}	Input voltage range		±12	±13		±12	±13		V
R_{IN}	Input resistance		0.3	1		0.3	1		MΩ
P_D	Power consumption			70	170		70	170	mW
	Channel separation			120			120		dB
I_{SC}	Output short-circuit current			25			25		mA

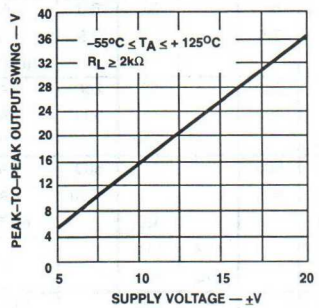
AC ELECTRICAL CHARACTERISTICS

T_A=25°C V_S=±15V, unless otherwise specified.

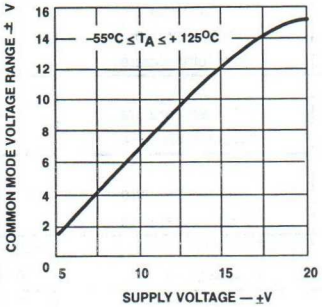
SYMBOL	PARAMETER	TEST CONDITIONS	MC1458, SA1458, MC1558			UNIT
			Min	Typ	Max	
R_{IN}	Parallel input resistance	Open-loop, f=20Hz	0.3			MΩ
	Common-mode input impedance	f=20Hz		200		MΩ
	Equivalent input noise voltage	A_V=100, R_S=10kΩ, BW=1.0kHz, f=1.0kHz		30		nV/$\sqrt{Hz}$
BW	Power bandwidth	A_V=1, R_L=2.0kΩ, THD≤5%, V_{OUT}=20V_{P-P}		14		kHz
	Phase margin			65		degrees
A_V	Gain margin			11		dB
	Unity gain crossover frequency	Open loop		1.0		MHz
	Transient response unity gain	V_{IN}=20mV, R_L=2kΩ, C_L≤100pF				
t_R	Rise time			0.3		µs
	Overshoot			5.0		%
SR	Slew rate	C_L≤100pF, R_L≥2kΩ, V_{IN}=±10V		0.8		V/µs

TYPICAL PERFORMANCE CHARACTERISTICS

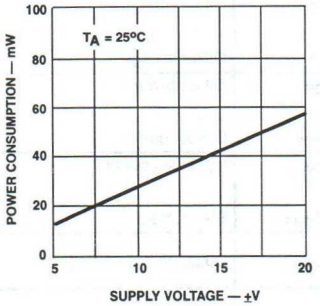
Output Voltage Swing as a Function of Supply Voltage



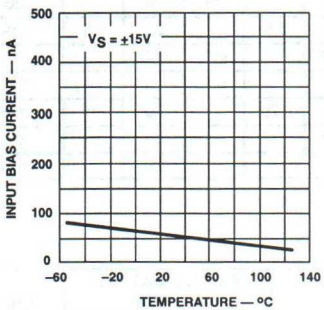
Input Common-Mode Range as a Function of Supply Voltage



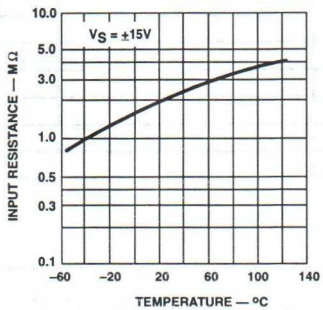
Power Consumption as a Function of Supply Voltage



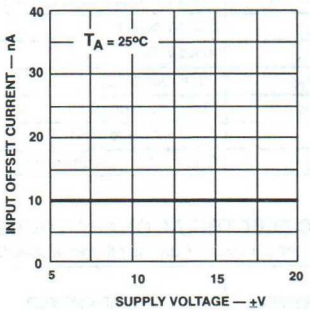
Input Bias Current as a Function Of Ambient Temperature



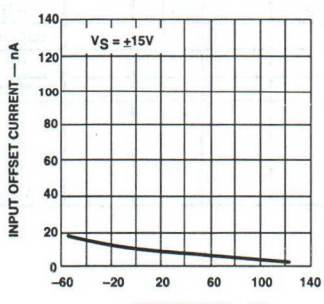
Input Resistance as a Function of Ambient Temperature



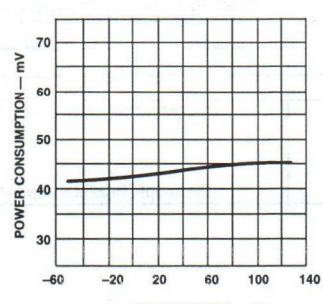
Input Offset Current as a Function of Supply Voltage



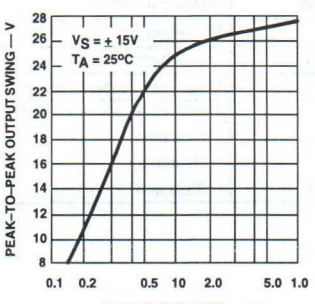
Input Offset Current as a Function of Ambient Temperature



Power Consumption as a Function of Ambient Temperature

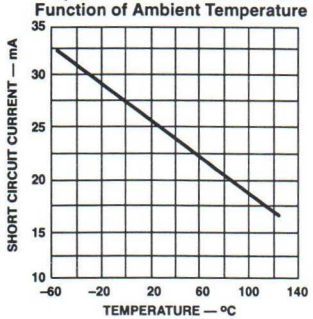


Output Voltage Swing as a Function of Load Resistance

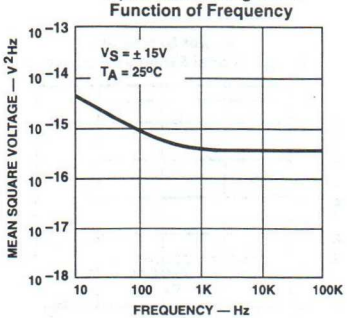


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

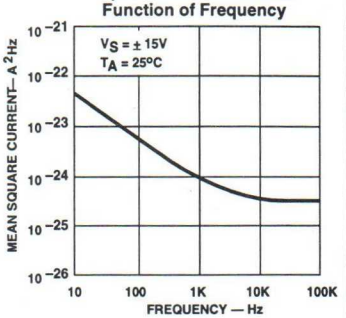
Output Short–Circuit Current as a Function of Ambient Temperature



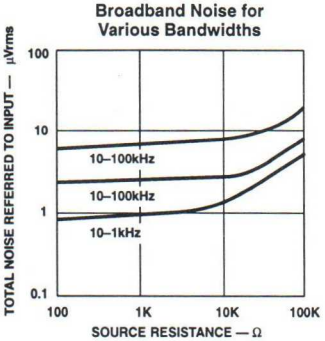
Input Noise Voltage as a Function of Frequency



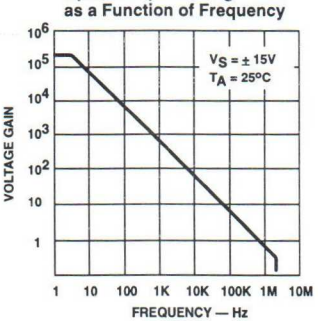
Input Noise Current as a Function of Frequency



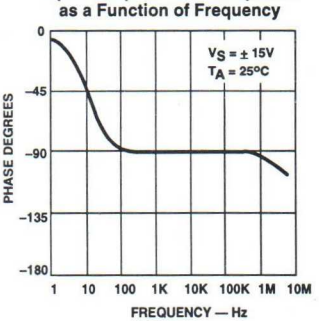
Broadband Noise for Various Bandwidths



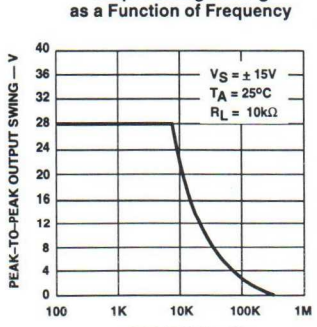
Open–Looped Voltage Gain as a Function of Frequency



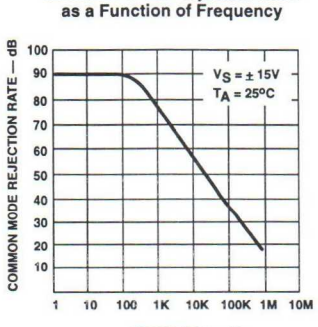
Open-Looped Phase Response as a Function of Frequency



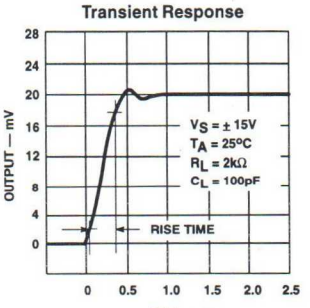
Output Voltage Swing as a Function of Frequency



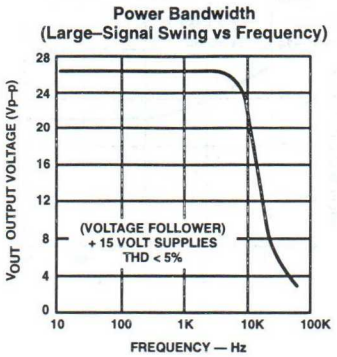
Common–Mode Rejection Ratio as a Function of Frequency



Transient Response



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



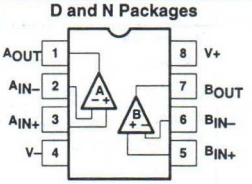
Dual general-purpose operational amplifier NE/SA/SE4558

DESCRIPTION

The 4558 is a dual operational amplifier that is internally compensated. Excellent channel separation allows the use of a dual device in a single amp application, providing the highest packaging density. The NE/SA/SE4558 is a pin-for-pin replacement for the RC/RM/RV4558.

PIN CONFIGURATIONS

D and N Packages



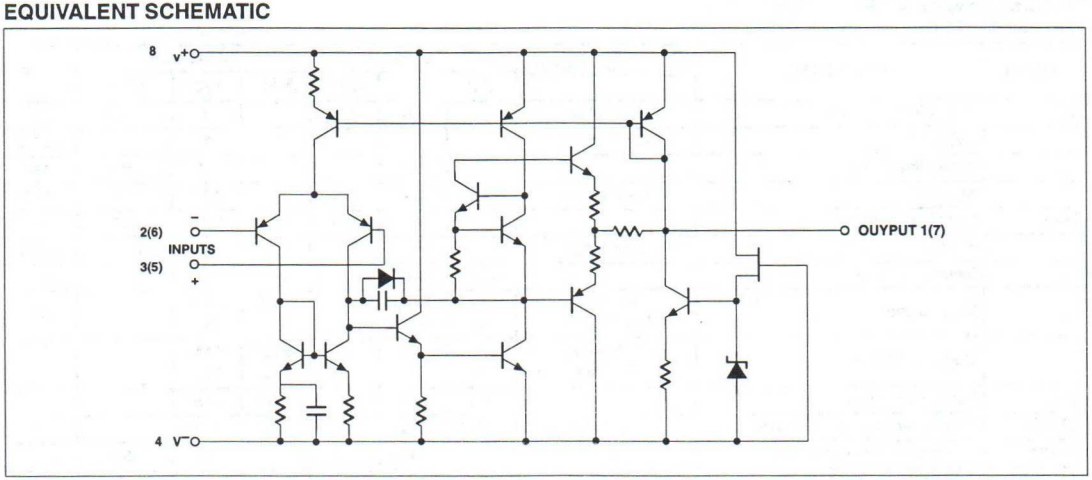
FEATURES

- 2MHz unity gain bandwidth guaranteed
- Supply voltage ±22V for SE4558 and ±18V for NE4558
- Short-circuit protection
- No frequency compensation required
- No latch-up
- Large common-mode and differential voltage ranges
- Low power consumption

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE4558D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE4558N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA4558N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA4558D	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-55 to +125°C	SE4558N	0404B

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	SE4558	±22	V
	NE4558, SA4558	±18	V
$P_{D\ MAX}$	Maximum power dissipation,		
	T_A=25°C (Still air)[1]		
	N package	1160	mW
	D package	780	mW
	Differential input voltage	±30	V
V_{IN}	Input voltage[2]	±15	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range		
	SE4558	-55 to +125	°C
	SA4558	-40 to +85	°C
	NE4558	0 to +70	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
	Output short-circuit duration[3]	Indefinite	

NOTES:
1. Derate above 25°C at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground on one amp only. Rating applies to +125°C case temperature or +75°C ambient temperature for NE4558 and to +85°C ambient temperature for SA4558.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=+15V, TA= 25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE4558			SA/NE4558			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	R_S≤10kΩ		1.0	5.0		2.0	6.0	mV
	$\Delta V_{OS}/\Delta T$	Over temp.		4			4		µV/°C
I_{OS}	Input offset current			50	200		30	200	nA
	$\Delta I_{OS}/\Delta T$	Over temp.		20			20		pA/°C
I_{BIAS}	Input bias current			40	500		200	500	nA
	$\Delta I_B/\Delta T$	Over temp.		40			40		pA/°C
R_{IN}	Input resistance		0.3	1.0		0.3	1.0		MΩ
A_V	Large-signal voltage gain	R_L≥2kΩ V_{OUT}=±10V	50,000	300,000		20,000	300,000		V/V
	Output voltage swing	R_L≥10kΩ R_L≥2kΩ	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
V_{IN}	Input voltage range		±12	±13		±12	±13		V
CMRR	Common-mode rejection ratio	R_S≤10kΩ	70	100		70	100		dB
PSRR	Power supply rejection ratio	R_S≤10kΩ		10	150		10	150	µV/V
I_{SC}	Short-circuit current		5	25	60	5	25	60	mA
	Power consumption (all amplifiers)	R_L=∞		120	170		120	170	mW

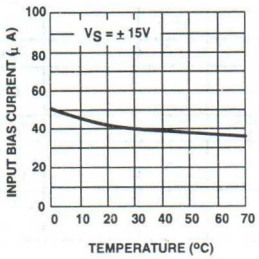
DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	SE4558			SA/NE4558			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_R	Transient response (unity gain)	V_{IN}=20mV R_L=2kΩ C_L≤100pF							
	Rise time			100			100		ns
	Overshoot			15.0			15.0		%
SR	Slew rate (unity gain)	R_L≥2kΩ		1.0			1.0		V/μs
	Channel separation (gain=100)	f=10kHz R_S=1kΩ		90			90		dB
GBW	Unity gain bandwidth (gain=1)		2.0	3.0		2.0	3.0		MHz
θ_M	Phase margin			45			45		De-gree
V_{NOISE}	Input noise voltage	f=1kΩ		25			25		$nV/\sqrt{Hz}$
NOTE: The following specifications apply over operating temperature range.									
V_{OS}	Input offset voltage	R_S≤10kΩ			6.0			7.5	mV
I_{OS}	Input offset current				500			300/500[1]	nA
I_{BIAS}	Input bias current				1500			800/1500[1]	nA
A_V	Large-signal voltage gain	R_L≥2kΩ V_{OUT}=±10V	25,000			15,000			V/V
	Output voltage swing	R_L≥2kΩ	±10			±10			V
P_C	Power consumption	T_A=HIGH T_A=LOW		105 125	150 200		115 120	150 200	mW mW

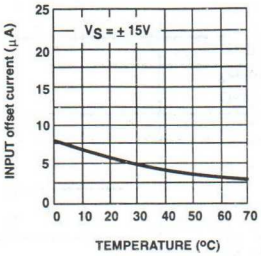
NOTES:
1. SA4558 only.

TYPICAL PERFORMANCE CURVES

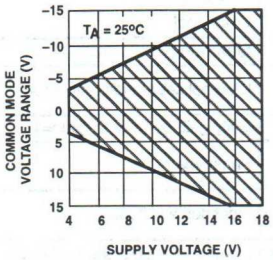
Input Bias as a Function of Ambient Temperature



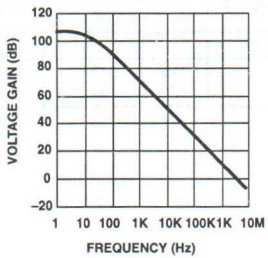
Input Offset Current as as a Function of Ambient Temperature



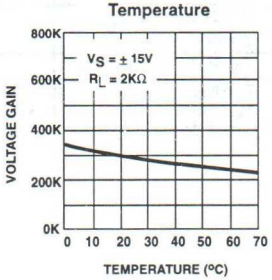
Common–Mode Range as a Function of Supply Voltage



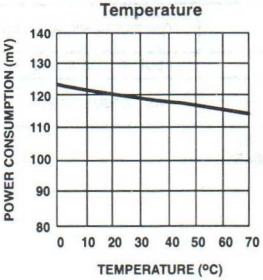
Open–Loop Voltage Gain as a Function of Frequency



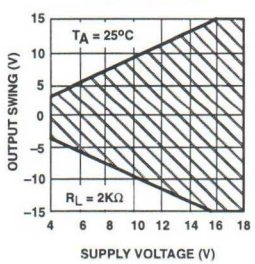
Open–Loop Gain as a Function of Temperature



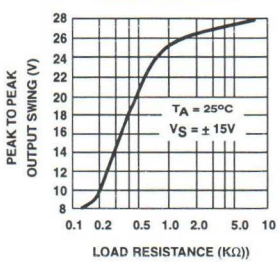
Power Consumption as a Function of Ambient Temperature



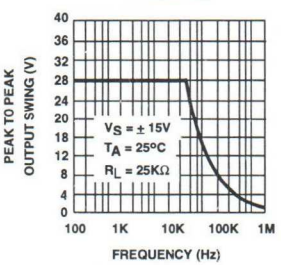
Typical Output Voltage as a Function of Supply Voltage



Output Voltage Swing as a Function of Load Resistance)

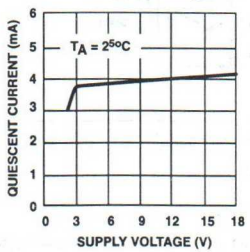


Output Voltage Swing as a Function of Frequency

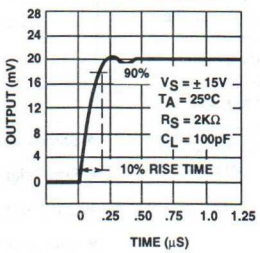


TYPICAL PERFORMANCE CURVES (Continued)

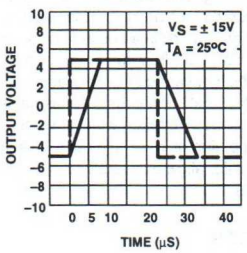
Quiescent Current as a Function of Supply Voltage



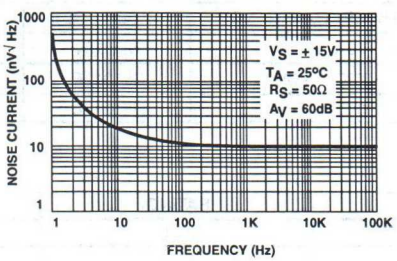
Transient Response



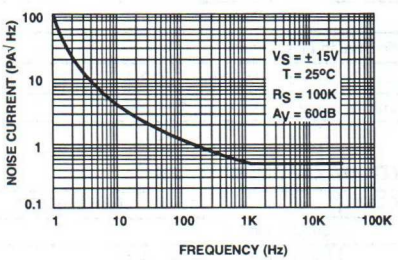
Voltage–Follower Large–Signal Pulse Response



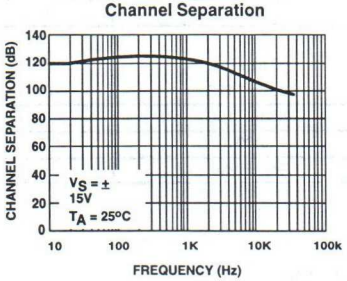
Input Noise Voltage as a Function of Frequency



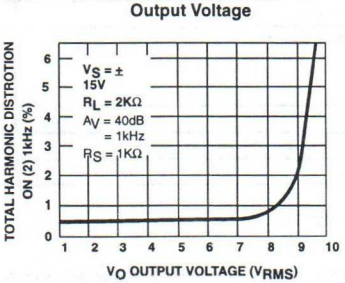
Input Noise Current as a Function of Frequency



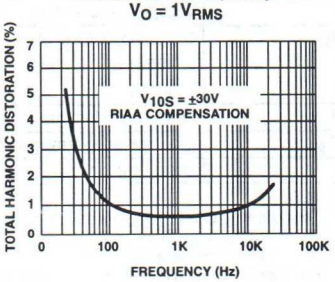
Channel Separation



Total Harmonic Distortion vs Output Voltage



Distortion vs Frequency $V_O = 1V_{RMS}$



High slew rate operational amplifier

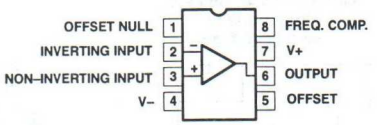
NE/SE531

DESCRIPTION

The 531 is a fast slewing high performance operational amplifier which retains DC performance equal to the best general purpose types while providing far superior large-signal AC performance. A unique input stage design allows the amplifier to have a large-signal response nearly identical to its small-signal response. The amplifier is compensated for truly negligible overshoot with a single capacitor. In applications where fast settling and superior large-signal bandwidths are required, the amplifier out-performs conventional designs which have much better small-signal response. Also, because the small-signal response is not extended, no special precautions need be taken with circuit board layout to achieve stability. The high gain, simple compensation, and excellent stability of this amplifier allow its use in a wide variety of instrumentation applications.

PIN CONFIGURATIONS

N, FE Packages



FEATURES

- 35V/µs slew rate at unity gain
- Pin-for-pin replacement for µA709, µA748, or LM101
- Compensated with a single capacitor
- Same low drift offset null circuitry as µA741
- Small-signal bandwidth 1MHz
- Large-signal bandwidth 500kHz
- True op amp DC characteristics make the 531 the ideal answer to all slew rate limited operational amplifier applications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE531N	0404B
8-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE531FE	0580A
8-Pin Ceramic Dual In-Line Package (CERDIP)	0°C to +70°C	NE531FE	0580A

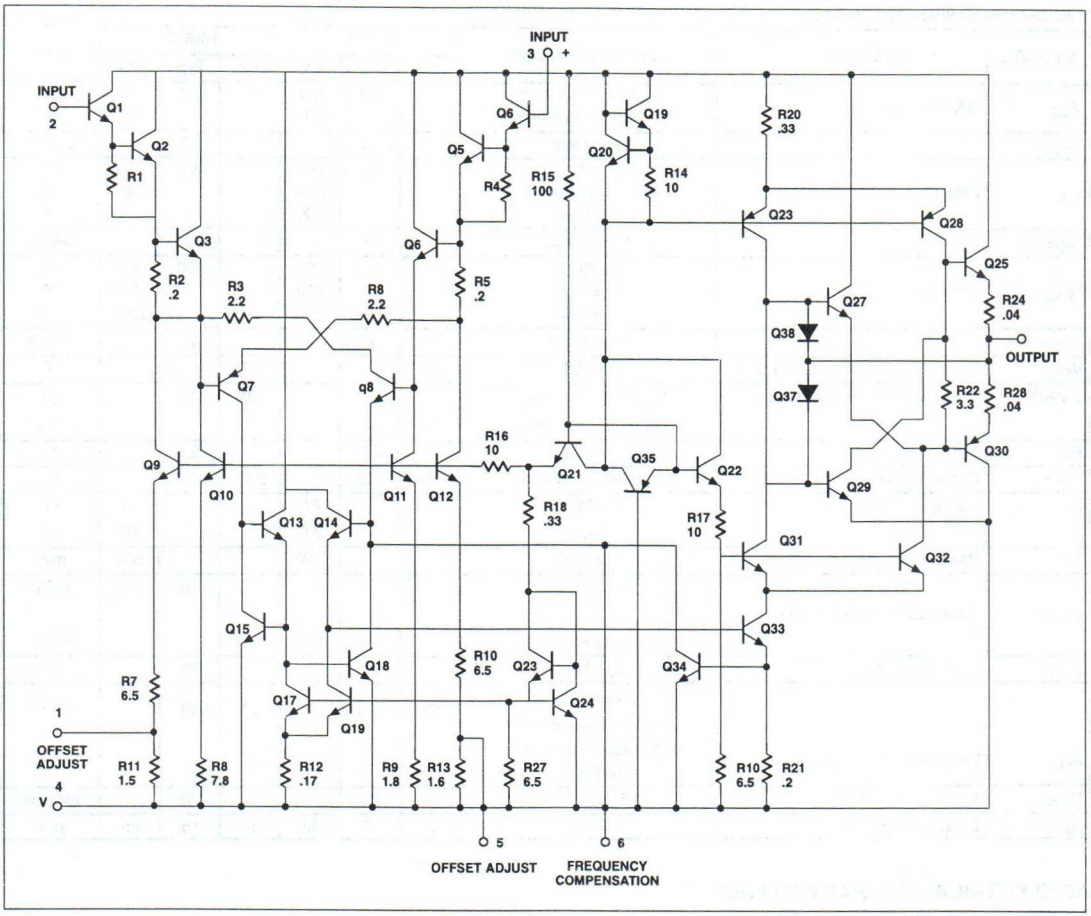
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±22	V
$P_{D\ MAX}$	Maximum power dissipation T_A=25°C (still-air)[1]		
	FE package	780	mW
	N package	1160	mW
	Differential input voltage	±15	V
V_{CM}	Common-mode input voltage[2]	±15	V
	Voltage between offset null and V-	±0.5	V
T_A	Operating ambient temperature range		
	NE531	0 to +70	°C
	SE531	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
	Output short-circuit duration[3]	indefinite	

NOTES:

1. The following derating factors should be applied above 25°C:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground or either supply. Rating applies to +125°C case temperature or to +75°C ambient temperature.

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

V_S=±15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE531			NE531			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	R_S≤10kΩ, T_A=25°C R_S310kΩ, over temp		2.0	5.0 6.0		2.0	6.0 7.5	mV mV
ΔV_{OS}		Over temp		10			10		µV/°C
I_{OS}	Offset current	T_A=25°C T_A=High T_A=Low		30	200 200 500		50	200 200 300	nA nA nA
ΔI_{OS}		Over temp		0.4			0.4		nA/°C
I_{BIAS}	Input bias current	T=25°C T_A=High T_A=Low		300	500 500 1500		400	1500 1500 2000	nA nA nA
ΔI_{BIAS}		Over temp		2			2		nA/°C
V_{CM}	Common-mode voltage range	T_A=25°C	±10			±10			V
CMRR	Common-mode rejection ratio	T_A=25°C, R_S≤10kΩ Over temp R_S≤10kΩ	70	90		70	100		dB dB
R_{IN}	Input resistance	T_A=25°C		20			20		MΩ
V_{OUT}	Output voltage swing	R_L≥10kΩ, over temp	±10	±13		±10	±13		V
I_{CC}	Supply current	T_A=25°C T_{MAX}			7.0 7.0			10 10	mA mA
P_D	Power consumption	T_A=25°C			210			300	mW
PSRR	Power supply rejection ratio	R_S≤10kΩ, T_A=25°C R_S≤10kΩ, over temp		10	150		10	150	µV/V µV/V
R_{OUT}	Output resistance	T_A=25°C		75			75		Ω
A_{VOL}	Large-signal voltage gain	T_A=25°C, R_L≥10kΩ, V_{OUT}=±10V R_L≥10kΩ, V_{OUT}=±10V, over temp	50 25	100		20 15	60		V/mV V/mV
V_{INN}	Input noise voltage	25°C f=1kHz		20			20		nV/√Hz
I_{SC}	Short-circuit current	25°C	5	15	45	5	15	45	mA

AC ELECTRICAL CHARACTERISTICS

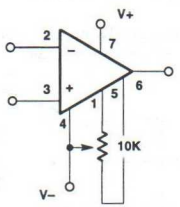
T_A=25°C V_S=+15V, unless otherwise specified.[1]

SYMBOL	PARAMETER	TEST CONDITIONS	SE531			NE531			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Full power bandwidth			500			500		kHz
t_S	Settling time (1%) (0.1%)	A_V=+1, V_{IN}=±10V		1.5 2.5			1.5 2.5		µs µs
	Large-signal overshoot Small-signal overshoot	A_V=+1, V_{IN}=±10V A_V=+1, V_{IN}=400mV		2 5			2 5		% %
t_R	Small-signal rise time	A_V=+1, V_{IN}=400mV		300			300		ns
SR	Slew rate	A_V=100 A_V=10 A_V=1 (non-inverting) A_V=1 (inverting)	 20 25	35 35 30 35			35 35 30 35		V/µs V/µs V/µs V/µs

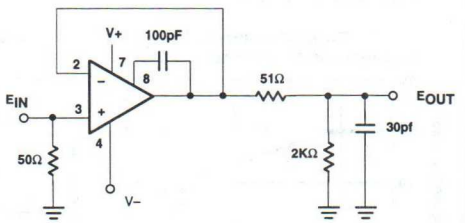
NOTES:

1. All AC testing is performed in the transient response test circuit.

TEST LOAD CIRCUITS



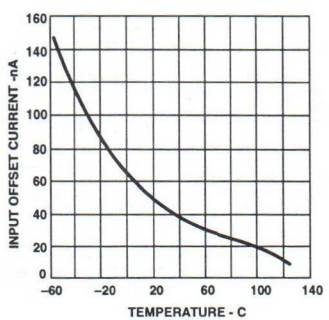
Offset Null Circuit



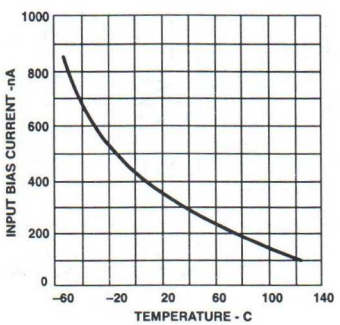
Transient Response Circuit

TYPICAL PERFORMANCE CHARACTERISTICS V_S = +15V, T_A = +255C, unless otherwise specified.

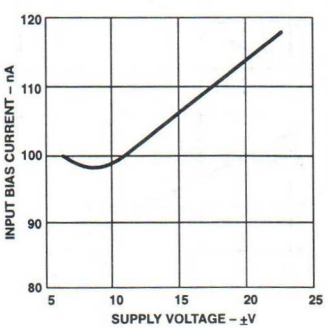
Input Offset Curent as a Function of Ambient Temperature



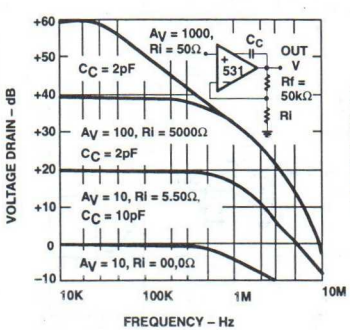
Input Bias Curent as a Function of Ambient Temperature



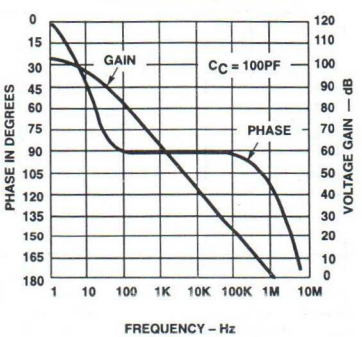
Input Bias Curent as a Function of Supply Voltage



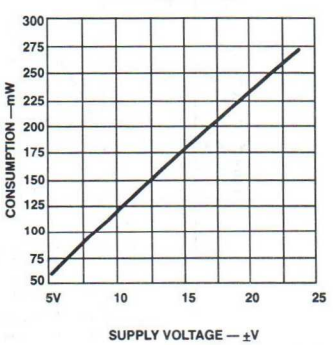
Closed Loop Non-Inverting Voltage Gain as a Function of Frequency



Open-Loop Phase Response and Voltage Gain as a Function of Ambient Temperature



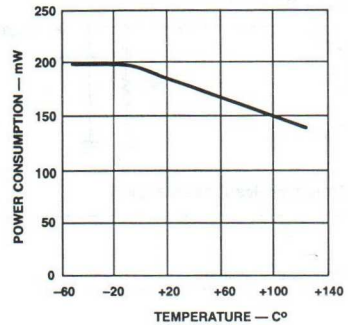
Power Consumption as a Function of Supply Voltage



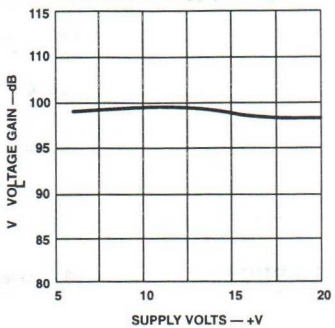
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

V_S = +15V, T_A = 25°C, unless otherwise specified.

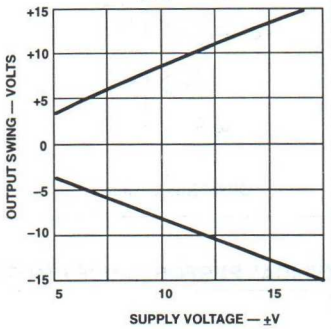
Power Consumption as a Function of Ambient Temperature



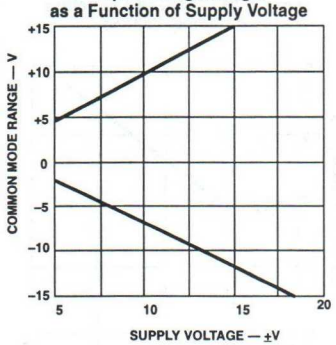
Open-Loop Voltage Gain as a Function of Supply Voltage



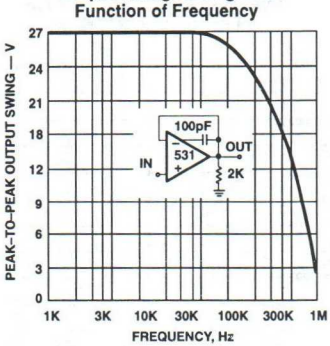
Output Voltage Swing as a Function of Supply Voltage



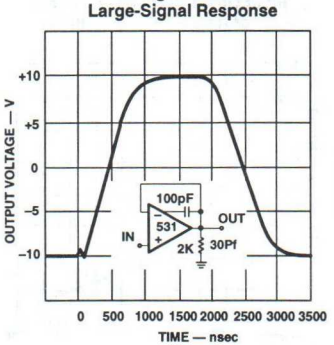
Input Voltage Range as a Function of Supply Voltage



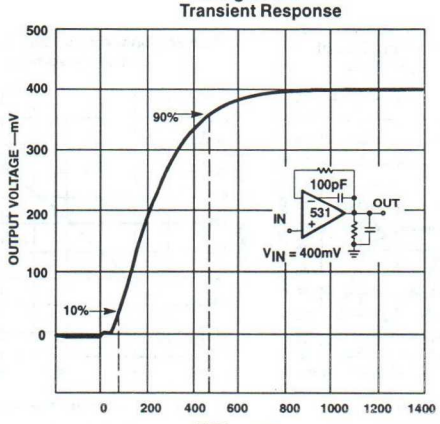
Output Voltage Swing as a Function of Frequency



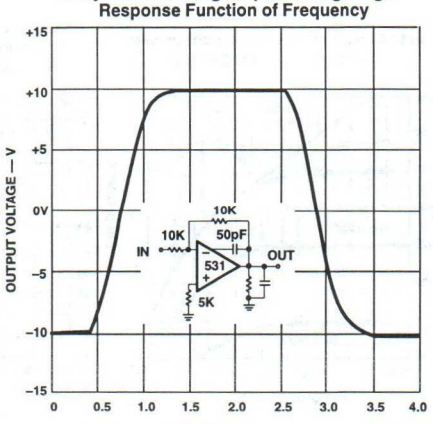
Voltage Follower Large-Signal Response



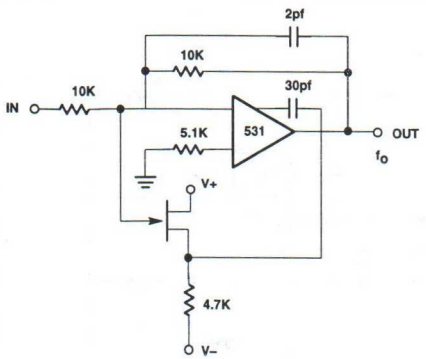
Voltage Follower Transient Response



Unity Gain Inverting Amplifier Large-Signal Response Function of Frequency

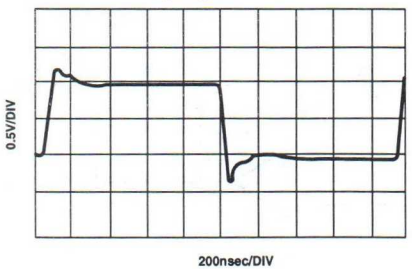


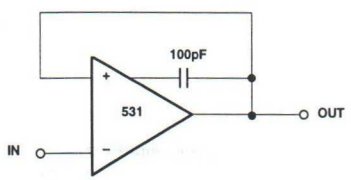
TYPICAL APPLICATIONS



High-Speed Inverter (10MHz Bandwidth)

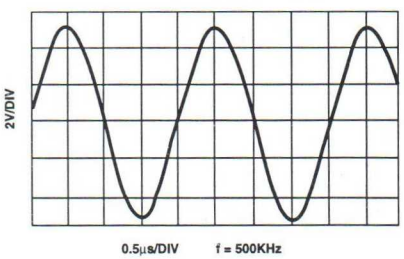
Pulse Response High-Speed Inverter

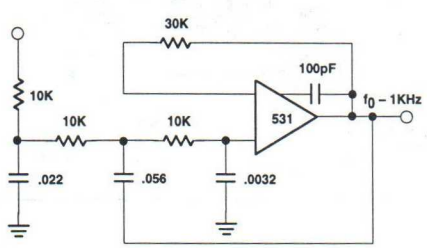




Fast Settling Voltage-Follower

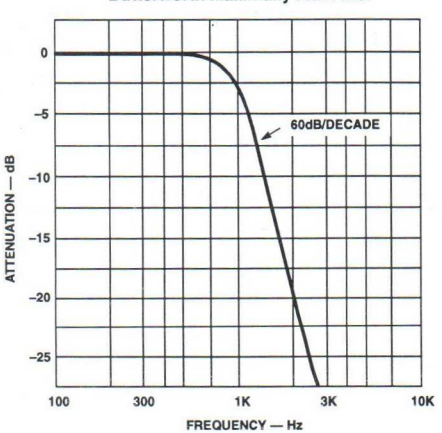
Large-Signal Response Voltage-Follower





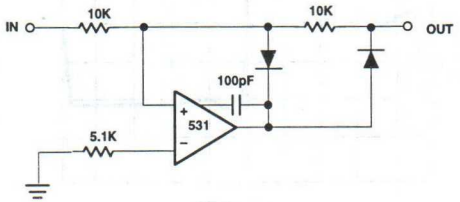
Three-Pole Active Low-Pass Filter Butterworth Maximally Flat Response[1]

Response of 3-Pole Active Butterworth Maximally Flat Filter

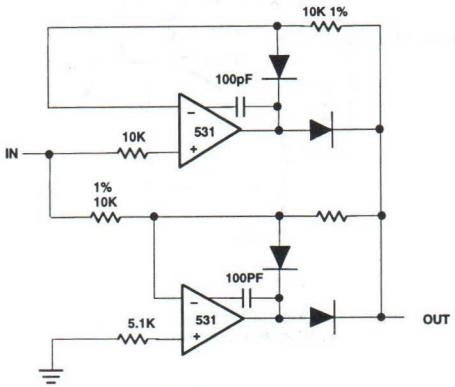


TYPICAL APPLICATIONS (Continued)

Precision Rectifiers

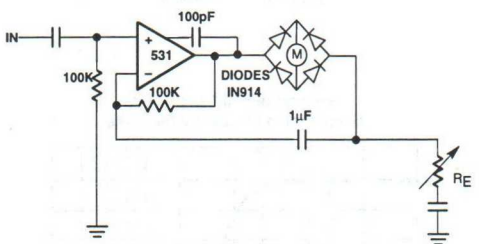


a. Half-Wave

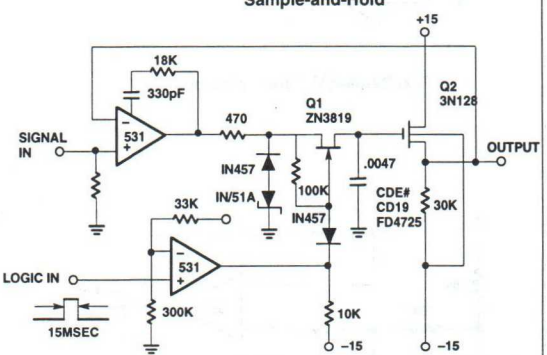


b. Full-Wave

AC Millivoltmeter



Sample-and-Hold



CYCLIC A-TO-D CONVERTER

One interesting, but much ignored, A/D converter is the cyclic converter. This consists of a chain of identical stages, each of which senses the polarity of the input. The stage then subtracts V_{REF} from the input and doubles the remainder if the polarity was correct. In Figure 1, the signal is full-wave rectified and the remainder of V_{IN}-V_{REF} is doubled. A chain of these stages gives the gray code equivalent of the input voltage in digitized form related to the magnitude of V_{REF}. Possessing high potential accuracy, the circuit using NE531 devices settles in 5µs.

TRIANGLE AND SQUARE WAVE GENERATOR

The circuit in Figure 2 will generate precision triangle and square waves. The output amplitude of the square wave is set by the output swing of op amp A-1, and R1/R2 sets the triangle amplitude. The frequency of oscillation in either case is:

$$f = \frac{1}{4RC} \cdot \frac{R2}{R1} \quad (1)$$

The square wave will maintain 50% duty cycle even if the amplitude of the oscillation is not symmetrical.

The use of the NE531 in this circuit will allow good square waves to be generated to quite high frequencies. Since the amplifier A1 runs open-loop, there is no need for compensation. The triangle-generating amplifier must be compensated. The NE5535 device can be used as well, except for the lower frequency response.

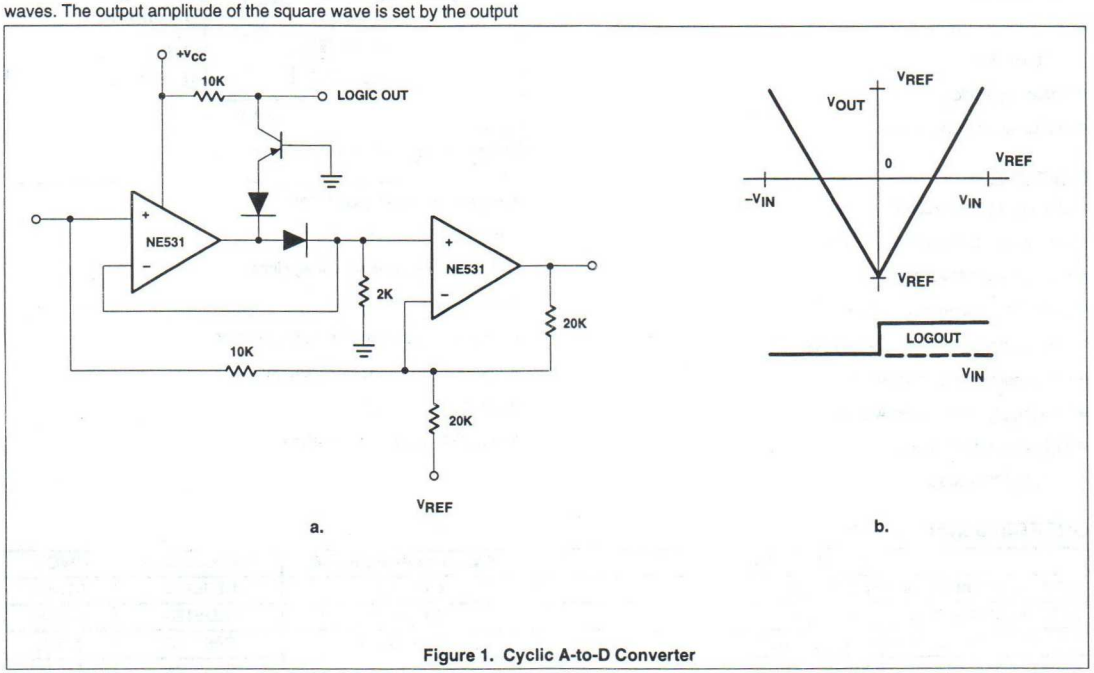


Figure 1. Cyclic A-to-D Converter

Dual high-performance operational amplifier

NE/SA/SE5512

DESCRIPTION

The 5512 series of high-performance operational amplifiers provides very good input characteristics. These amplifiers feature low input bias and voltage characteristics such as a 108 op amp with improved CMRR and a high differential input voltage limit achieved through the use of a bias cancellation and PNP input circuits with collector-to-emitter clamping. The output characteristics are like those of a 741 op amp with improved slew rate and drive capability, yet have low supply quiescent current.

APPLICATIONS

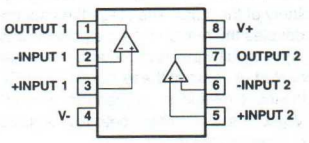
- AC amplifiers
- RC active filters
- Transducer amplifiers
- DC gain block
- Battery operation
- Instrumentation amplifiers

FEATURES

- Low input bias < ±20nA
- Low input offset current < ±20nA
- Low input offset voltage <1mV
- Low VOS temperature drift 5µV/°C
- Low input bias temperature drift 40pA/°C
- Low input voltage noise 30nV/√Hz
- Low supply current 1.5mA/amp
- High slew rate 1.0V/µs
- High CMRR 100dB

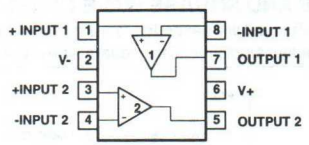
PIN CONFIGURATIONS

N Package



TOP VIEW

D Package[1]



TOP VIEW

NOTE:
1. The D package pinout is not functionally identical to the N pinout.

- High input impedance 100MΩ
- High PSRR 110dB
- High differential input voltage limit
- No crossover distortion
- Indefinite output short circuit protection
- Internally-compensated for unity gain
- 600Ω drive capability
- MIL-STD processing available

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to 70°C	NE5512D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to 70°C	NE5512N	0404B
8-Pin Plastic Small Outline (SO) Package	-40 to +85°C	SA5512D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5512N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-55 to +125°C	SE5512N	0404B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±16	V
$P_{D\ MAX}$	Maximum power dissipation, T_A=25°C (still air)[1]		
	N package	1212	mW
	D package	800	mW
T_A	Operating ambient temperature range		
	NE5512	0 to +70	°C
	SA5512	-40 to +85	°C
	SE5512	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. The following derating factors should be applied above 25°C
   N package at 9.7mW/°C
   D package at 6.4mW/°C

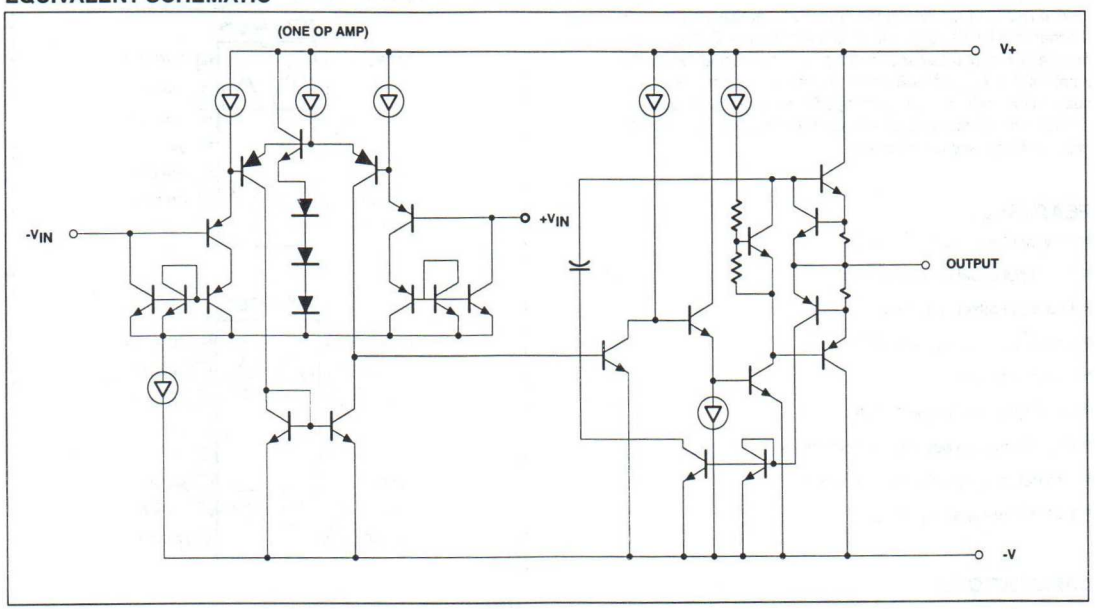
ELECTRICAL PERFORMANCE CHARACTERISTICS

V_{CC} = ±15V, T_A = 25°C over temperature range, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5512			NE/SA5512			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	R_S=100Ω T_A=+25°C Over temp.		0.7 1	2 3		1 1.5	5 6	mV
$\Delta V_{OS}/\Delta T$				4			5		µV/°C
I_{OS}	Input offset current	R_S=100kΩ T_A=+25°C Over temp.		3 4	10 20		6 8	20 30	nA
$\Delta I_{OS}/\Delta T$				30			40		pA/°C
I_{BIAS}	Input bias current	R_S=100kΩ T_A=+25°C Over temp.		3 4	10 20		6 8	20 30	nA
$\Delta I_{BIAS}/\Delta T$				30			40		pA/°C
R_{IN}	Input resistance differential	T_A=+25°C		100			100		MΩ
V_{CM}	Input common mode range	T_A=+25°C Over temp.	±13.5 ±13	±13.7 ±13.2		±13.5 ±13	±13.7 ±13.2		V
CMRR	Input common-mode rejection ratio	V_{CC}=±15V V_{IN}=±13.5V T_A=+25°C V_{IN}=±13V Over temp.	70	100		70	100		dB
A_V	Large-signal voltage gain	R_L=2kΩ T_A=25°C V_O=±10V over temp.	50 25	200		50 25	200		V/mV
SR	Slew rate	T_A=25°C	0.6	1			1		V/µs
GBW	Small-signal unity gain band-width	T_A=25°C		3			3		MHz
θ_M	Phase margin	T_A=25°C		45			45		degree
V_{OUT}	Output voltage swing	R_L=2kΩ T_A=25°C Over temp.	±13 ±12.5	±13.5 ±13		±13 ±12.5	±13.5 ±13		V
V_{OUT}	Output voltage swing	R_L=600Ω[1] T_A=25°C Over temp.	±10 ±7.5	±11.5 ±9		±10 ±8	±11.5 ±9		V
I_{CC}	Power supply current	R_L=Open T_A=25°C Over temp.		3.4 3.6	5 5.5		3.4 3.6	5 5.5	mA
PSRR	Power supply rejection ratio	Over temp.	80	100		80	100		dB
AA	Amplifier-to-amplifier coupling	f=1kHz to 20kHz, T_A=25°C		-120			-120		dB
THD	Total harmonic distortion	f=10kHz T_A=25°C V_O=7V_{RMS}		0.01			0.01		%
V_{NOISE}	Input noise voltage	f=1kHz T_A=25°C		30			30		nV/√Hz
I_{NOISE}	Input noise current	f=1kHz T_A=25°C		0.2			0.2		pA/√Hz
I_{SC}	Short-circuit current	±15V, T_A=25°C		40			40		mA

NOTES:
1. Not to exceed maximum package power dissipation.

EQUIVALENT SCHEMATIC



Quad high-performance operational amplifier

NE/SE5514

DESCRIPTION

The NE/SE5514 family of quad operational amplifiers sets new standards in bipolar quad amplifier performance. The amplifiers feature low input bias current and low offset voltages. Pinout is identical to LM324/LM348 which facilitates direct product substitution for improved system performance in dual supply applications. Output characteristics are similar to a µA741 with improved slew and drive capability.

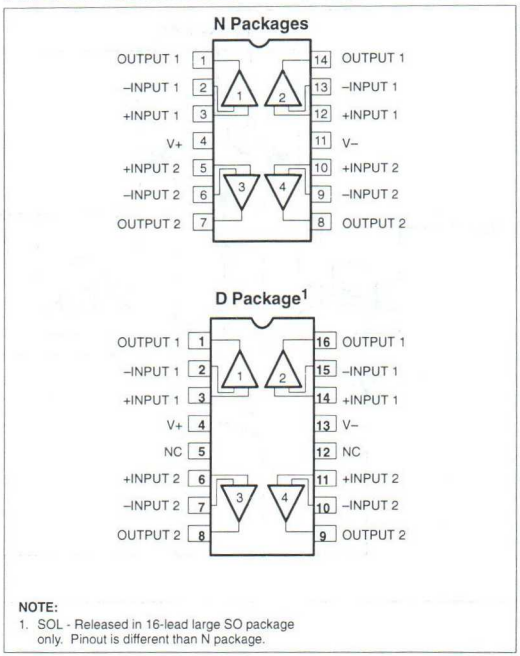
FEATURES

- Low input bias current: < ±3nA
- Low input offset current: < ±3nA
- Low input offset voltage:<1mV
- Low supply current: 1.5mA/A
- 1V/µs slew rate
- High input impedance: 100MΩ
- High common-mode impedance: 10GΩ
- Internal compensation for unity gain
- 600Ω drive capability ($7V_{RMS}$)

APPLICATIONS

- AC amplifiers
- RC active filters
- Transducer amplifiers
- DC gain block
- Instrumentation amplifier

PIN CONFIGURATIONS

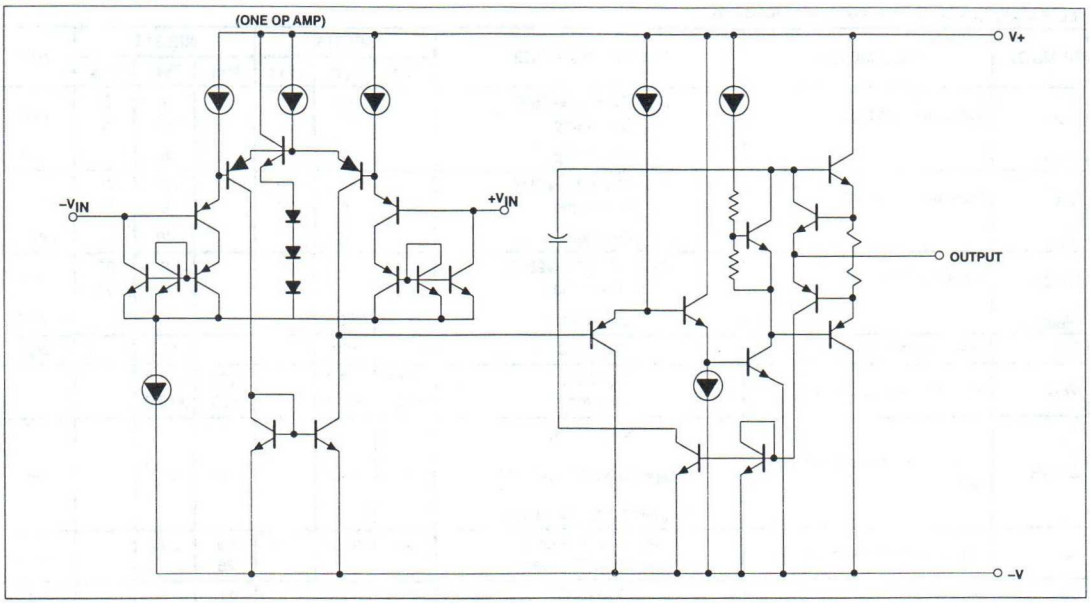


NOTE:
1. SOL - Released in 16-lead large SO package only. Pinout is different than N package.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline Large (SOL) package	0 to +70°C	NE5514D	0171B
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5514N	0405B
14-Pin Plastic Dual In-Line Package (DIP)	-55 to +125°C	SE5514N	0405B

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±16	V
V_{DIFF}	Differential input voltage	32	V
V_{IN}	Input voltage	0 to 32	V
	Output short to ground	Continuous	
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
T_A	Operating ambient temperature range		
	NE5514	0 to 70	°C
	SE5514	-55 to +125	°C
P_{MAX}	Maximum power dissipation		
	T_A=25°C (still-air)[1]		
	N package	1420	mW
	D package	1250	mW

NOTES:

1. The following derating factors should be applied above 25°C
   N package at 11.4mW/°C
   D package at 10.0mW/°C

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_A = 25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5514			NE5514			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	R_S=100Ω, T_A=+25°C		0.7	2		1	5	mV
		Over temp.		1	3		1.5	6	
ΔV_{OS}		Over temp.		4			5		µV/°C
I_{OS}	Input offset current	R_S=100kΩ, T_A=+25°C		3	10		6	20	nA
		Over temp.		4	20		8	30	
ΔI_{OS}		Over temp.		30			40		pA/°C
I_{BIAS}	Input bias current	R_S=100kΩ, T_A=+25°C		3	10		6	20	nA
		Over temp.		4	20		8	30	
ΔI_{BIAS}		Over temp.		30			40		pA/°C
R_{IN}	Input resistance differential	T_A=25°C		100			100		MΩ
V_{CM}	Input common mode range	T_A=25°C	±13.5	±13.7		±13.5	±13.7		V
		Over temp.	±13	±13.2		±13	±13.2		
CMRR	Input common-mode rejection ratio	V_{CC}=±15V, V_{IN}=±13.5V @ T_A=25°C	70	100		70	100		dB
		V_{IN}=±13V @ Over temp.							
A_V	Large-signal voltage gain	R_L=2kΩ, T_A=25°C	50	200		50	200		V/mV
		V_O = ±10V, Over temp.	25			25			
SR	Slew rate	T_A=25°C	0.6	1		0.6	1		V/µs
GBW	Small-signal unity gain band-width	T_A=25°C		3			3		MHz
θ_M	Phase margin	T_A=25°C		45			45		Deg
V_{OUT}	Output voltage swing	R_L=2kΩ, T_A=25°C	±13	±13.5		±13	±13.5		V
		Over temp.	±12.5	±13		±12.5	±13		
V_{OUT}	Output voltage swing	R_L=600Ω[1], T_A=25°C	±10	±11.5		±10	±11.5		V
		Over temp.	±7.5	± 9		± 8	± 9		
I_{CC}	Power supply current	R_L=Open, T_A=25°C		6	10		6	10	mA
		Over temp.		7	12		7	12	
PSRR	Power supply rejection ratio	±5V ≤ V_{CC} ≤ ±15V	80	110		80	110		dB
		Over temp.							
AA	Amplifier to amplifier coupling	f=1kHz to 20kHz, T_A=25°C		-120			-120		dB
THD	Total harmonic distortion	f=10kHz, T_A=25°C		0.01			0.01		%
		V_O=7V_{RMS}							
V_{NOISE}	Input noise voltage	f=1kHz, T_A=25°C		30			30		nV/√Hz
I_{SC}	Short-circuit current	T_A=25°C	10	40	60	10	40	60	mA

NOTES:

1. Not to exceed maximum power dissipation.

Applications for the NE/SA/SE5512

AN144

DESCRIPTION

The NE/SA/SE5512 series of high-performance operational amplifiers provides very good input characteristics. These amplifiers feature low input bias and voltage characteristics such as a 108 op amp with improved CMRR and a high differential input voltage limit achieved through the use of a bias cancellation and PNP input circuits with collector-to-emitter clamping. The output characteristics are like those of a 741 op amp with improved slew rate and drive capability, yet have low supply quiescent current.

BRIDGE TRANSDUCER AMPLIFIER

In applications involving strain gauges, accelerometers and thermal sensors, a bridge transducer is often used. Frequently the sensor elements are high resistance units requiring equally high bridge resistance for good sensitivity. This type of circuit then demands an amplifier with high input impedance, low bias current and low drift. The circuit shown represents a solution to these general requirements (Figure 1).

For V_S=10V, the common-mode voltage is approximately +5V, well within the common-mode limits of the NE5512.

The sensitivity of the input stage is approximately

$$\frac{R_F \cdot V_S}{2R}$$

to a change in transducer resistance ΔR. This gives a gain factor of ≈ 50 for V_S=10V and R=25kΩ. The second stage gain is x100 giving a total gain of ≈ 5000.

Noise is minimized by shielding the transducer leads and taking special care to determine a good signal ground.

Common-mode noise rejection is particularly important, making matched differential impedance critical. The NE5512 typically provides 100dB of common-mode rejection and will considerably reduce this undesirable effect.

The following are sensitivity figures for the transducer circuits.

	ΔR	ΔE_{OUT}
Leg 1	10Ω	-2.6V
	5Ω	-1.3V
Leg 2	10Ω	+2.4V
	5Ω	+1.2V

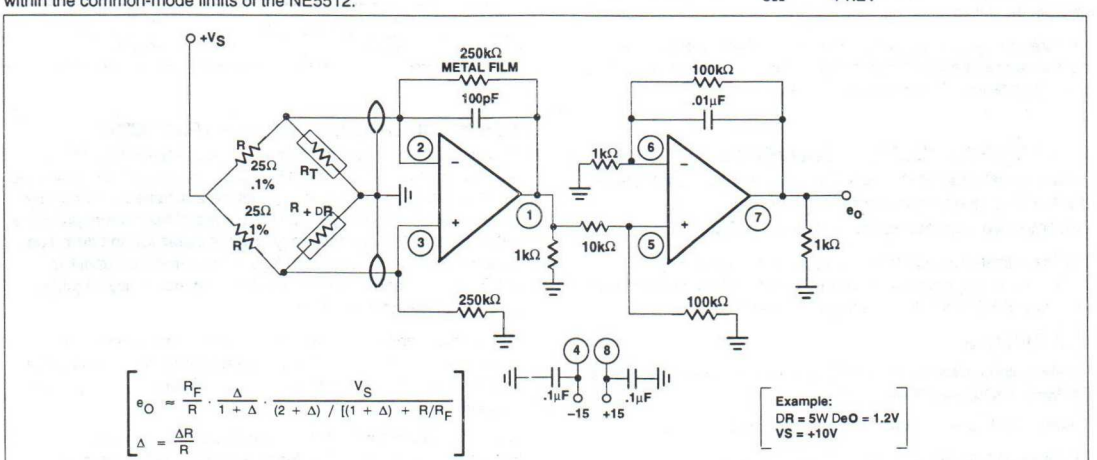


Figure 1. NE/SE5512 Bridge Transducer Amplifier

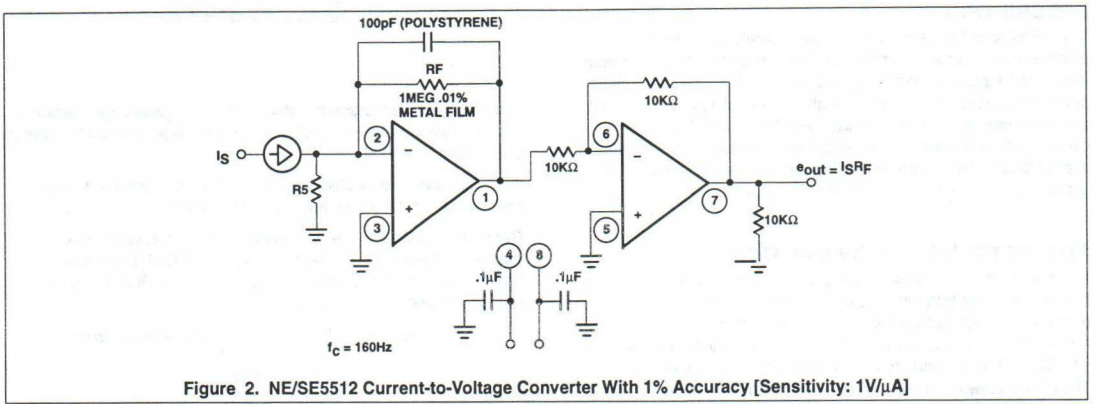


Figure 2. NE/SE5512 Current-to-Voltage Converter With 1% Accuracy [Sensitivity: 1V/μA]

Temperature compensation of the bridge element is accomplished by using low drift metal film resistors and also by providing a complimentary non-active sensor element to thermally track the offset in the active element.

High frequency roll-off provides attenuation of unwanted noise above the pass band of the transducer. The shunt capacitors across both stage feedback resistors are for this purpose.

CURRENT-TO-VOLTAGE CONVERTER

Taking advantage of the very low bias current and offset of the NE5512 is demonstrated in its adaptation to a current-to-voltage converter as shown in Figure 2.

The lower limit of measuring accuracy is determined by I_B (inverting), which is typically 6nA. In order to attain a measurement accuracy of 1%, the following inequality must hold:

$I_B \leq (0.01)\ I_{Smin}$

Where I_B=input bias current and I_{Smin}=minimum measured current. For I_B=6nA and I_{Smin}=1μA,

6nA≤(0.01) 1μA=10nA and the inequality hold.

DC offset and current noise gain is determined by

$$\frac{R_F + R_S}{R_S}$$

which ≈ 1 for $R_S >> R_F$.

The measured results for this circuit appear below (V_{CC} = ±15V).

INPUT CURRENT	OUTPUT VOLTAGE
1μA	1.008V
5μA	5.00V
10.00μA	10.00V

NE5512 OPERATIONAL DIFFERENTIATOR

By utilizing the very high input impedance characteristic of the NE5512, an excellent active differentiator can be realized. Using the circuit shown (Figure 3), good results were obtained as shown by the waveforms in Figures 4, 5 and 6. One of the primary problems with such circuits is the tendency towards instability and distortion either due to loading caused by input bias currents or amplifier non-linearity. In addition, gain increases with frequency, requiring low input noise in the amplifier.

The relative stability is shown by the output signal waveforms mentioned above. Adding R_1 provides added compensation in the form of a zero near the amplifier unity gain frequency. Frequency range is 100Hz to 10kHz.

In order to obtain good differentiation, the network time constant, RC, must be small relative to the period of the highest frequency present at the input. Since the differentiator will attenuate the signal by a factor of ωRC, which may be 100:1 in the operating region, the second amplifier stage is used to compensate for this loss. Various circuits are easily interfaced with the differentiator block due to the inherently low output impedance of the NE5512.

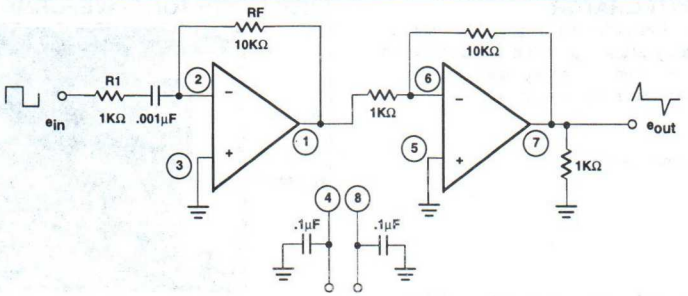


Figure 3. NE/SE5512 Active Differentiator With Inverting x 10 Buffer

DIFFERENTIATOR WAVEFORMS

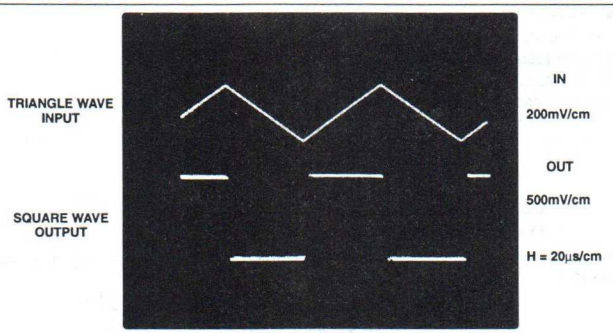


Figure 4.

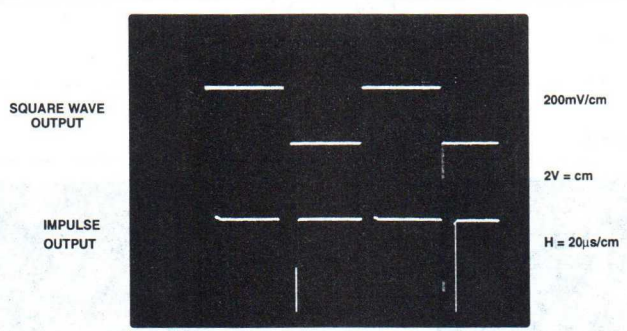


Figure 5.

THE OPERATIONAL INTEGRATOR

The operational complement of the active differentiator is the active integrator. The NE5512 is easily adapted to this function as shown in the circuit below (Figure 7). To obtain satisfactory integration, the time constant must fulfill the following requirement:

$RC \geq 15T$

Where T is the period of the input waveform.

For the ideal integrator

$$e_{OUT} = \frac{1}{RC}\int e_{IN}\, dt$$

The factor 1/RC represents an attenuation of the input signal. The low signal level is increased by using the second half of the NE5512 as a gain stage following the operational integration. The waveforms in Figures 8 and 9 show the input-output relationship for both a sine wave and a square wave function. A good integrator must exhibit a phase shift of ≥89° for sine wave input over the active frequency range. For a square wave, the resultant output must be a linear ramp. The circuit shown fulfills this requirement (see Figure 7). No external compensation is required since the amplifier is unity gain stable.

DIFFERENTIATOR WAVEFORMS

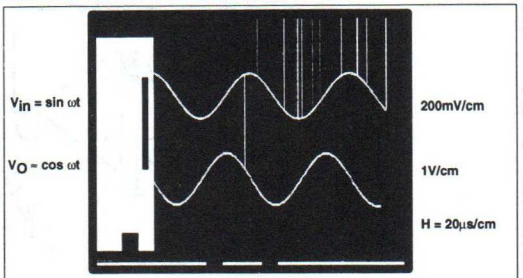


Figure 6.

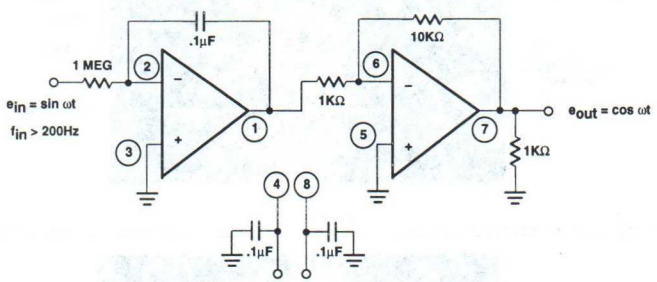


Figure 7. NE/SE5512 Active Integrator

INTEGRATOR WAVEFORMS

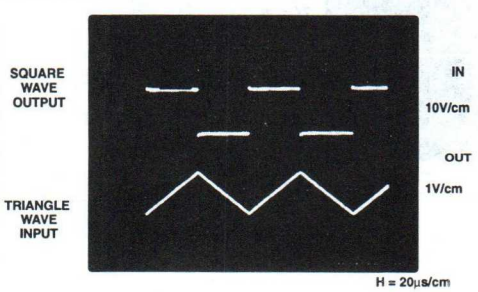


Figure 8.

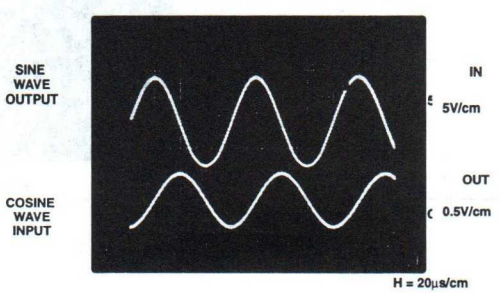


Figure 9.

Applications for the NE5514

AN1441

NE5514 DESCRIPTION

The SE/NE5514 family of Quad Operational Amplifiers sets new standards in Bipolar Quad Amplifier Performance. The amplifiers feature low input bias current and low offset voltages. Pinout is identical to LM324/LM348, which facilitates direct product substitution for improved system performance. Output characteristics are similar to a μA741 with improved slew and drive capability.

FOUR-QUADRANT PHOTO-CONDUCTIVE DETECTOR AMPLIFIER

When operating a photo diode in the photo-conductive mode (reverse-biased) very small currents in the microampere range must be sensed in the photo active operating region. Dark currents in the nanoamperes are common. Generally, for this reason, JFET input preamps are used to prevent interaction and accuracy degradation due to input bias currents.

The 5514 has sufficiently low input bias current (6nA) to allow its use under these circuit constraints as shown in a possible design used to sense four-quadrant motion of a light source. By proper summing of the signals from the X and Y axes, four-quadrant output may be fed to an X-Y plotter, oscilloscope or computer for simulation (see Figure 1).

The wide input common-mode voltage range of the device allows a +10V supply to be used to drive the signal bridge giving high sensitivity and improved signal-to-noise. Obviously, input balancing is critical to achieving

common-mode signal rejection in addition to adequate shielding of the sensor leads. The sensor head itself must be shielded and the shield grounded to signal common to avoid unwanted noise pick-up from power line and other local noise sources. Amplifier response may be shaped to aid in noise reduction by more complex filter configurations. If possible the 5514 should be located in close proximity to the sensor head.

System balance may be done under dark field conditions if adequate photo detector tracking results. However, for high accuracy systems, a bipolar balance adjust added to the non-inverting output stage is more desirable. With this latter method, the signal bridge is balanced for a null output under uniform light field conditions using the bridge balance pot as shown. DC offset is then

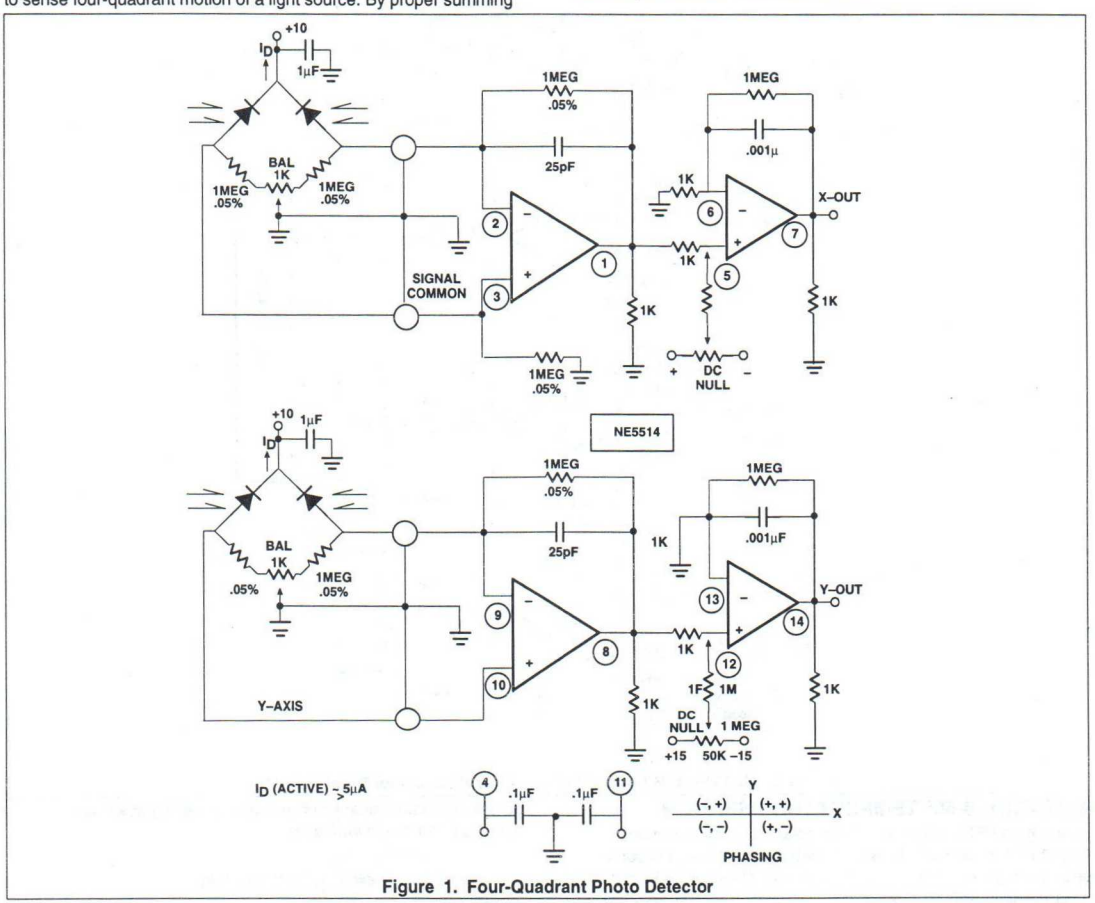


Figure 1. Four-Quadrant Photo Detector

adjusted using the balance pot on the output amplifier under dark field conditions.

MULTI-TONE BANDPASS FILTER FOR PLL TONE DECODER

In the design of a multiple tone signaling system, particularly where signals are transmitted over long lines, noise and adjacent channel interference may be a significant barrier to reliable communications.

By the use of narrow-band active pre-filters to attain selectivity and gain, the effective signal to noise ratio is greatly improved. The NE/SE5514 is easily adapted to such filter configurations due to its inherent stability. In addition, its very high input impedance drastically reduces loading to the passive networks and allows for increased "Q" and large value resistors.

The circuit in Figure 2 demonstrates multiple feedback filters operating at four of the standard signaling frequencies. More channels may be added to increase the capacity of the system.

Test results obtained from the filter configuration were as follows:

Wide-band signal-to-noise	63dB
Gain (Mid band)	30dB
Q (effective)	≈ 30
Output	0dBm ($0.775V_{RMS}$)

Note that the amplifiers are operated from a single +12V supply and are biased to half V_{CC} by a simple resistive divider at point B which connects to all non-inverting inputs.

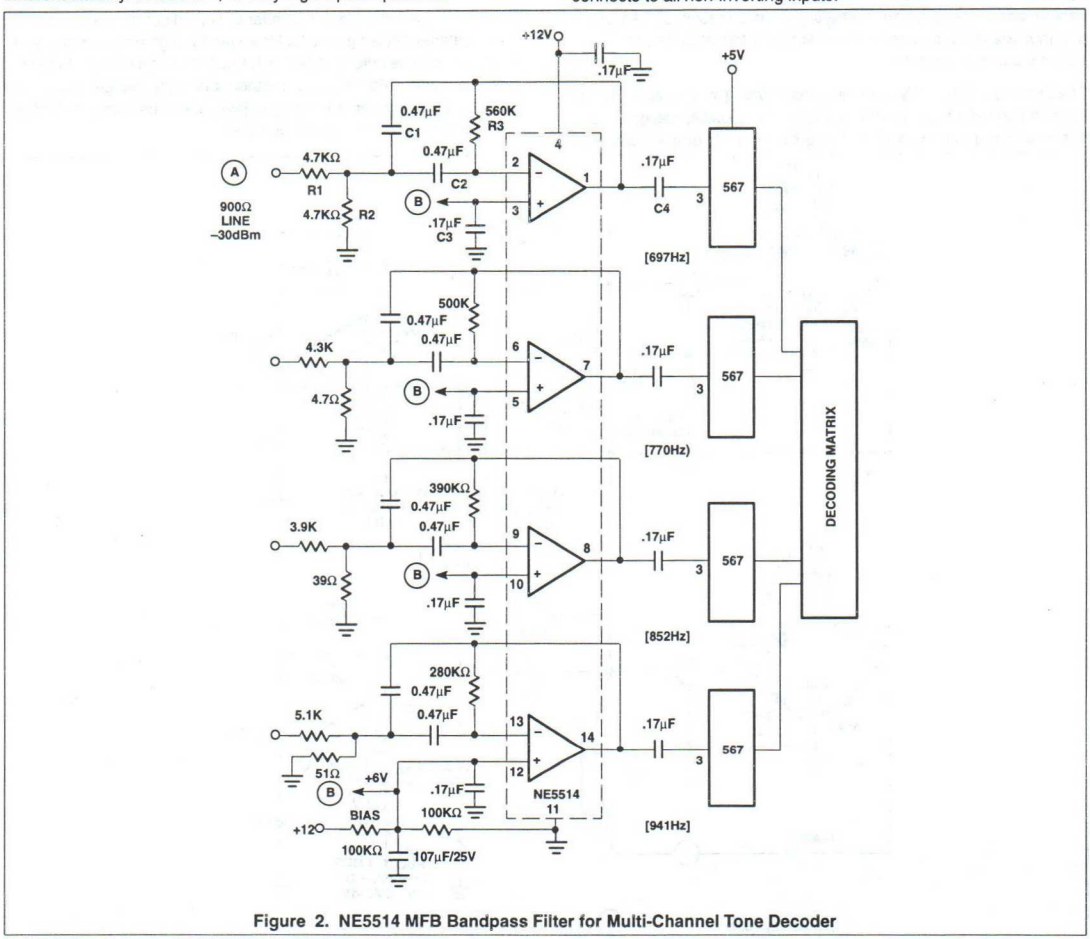


Figure 2. NE5514 MFB Bandpass Filter for Multi-Channel Tone Decoder

4-STATION 0-50° TEMPERATURE SENSOR

By using an NPN transistor as a temperature sensing element, the NE5514 forms the basis for a multi-station temperature sensor as shown in Figure 3. The principle used is fundamental to the current voltage relationship of a forward-biased junction. The current flow across the base-emitter junction is determined by absolute temperature in the following way:

$$I_E = -(I_C + I_B)$$

and $I_E \propto I_S \exp(V_{BE}/V_T)$; $V_T = kt/q$

therefore, $V_{BE} \propto V_T \ln I_E/I_S$

Where I_E is the forward current and I_S is the saturation current inherent in the junction, I_E must be high enough such that the I_S variation with temperature is small relative to I_E ($I_E >> I_S$). I_S is typically 0.05pA, therefore, setting I_E to 1 or 2μA gives the desired condition.

Diode D_1 serves to substantially reduce error due to power supply variation by giving a fixed voltage reference. To calibrate the sensor adjust R_4 for "0" volts output from the NE5514 at 0°C. Adjust R_6 tracking resistor for a scale factor of 100mV/°C output.

Only the transistor need be placed in the temperature-controlled environment. Figure 4 shows the addition of an A/D converter and display to give a digital thermometer.

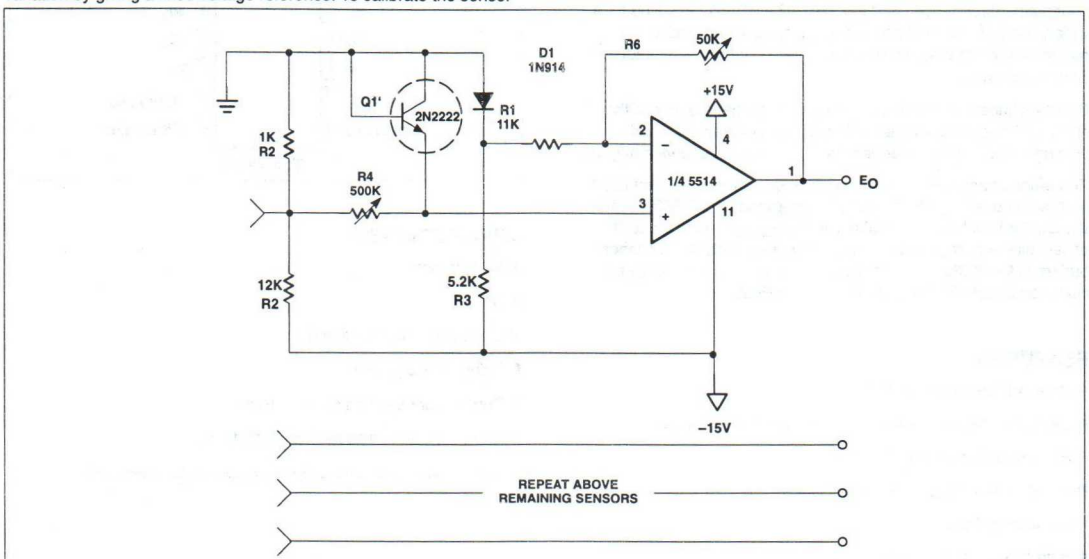


Figure 3. 4-Channel Temperature Sensor (0-50°C)

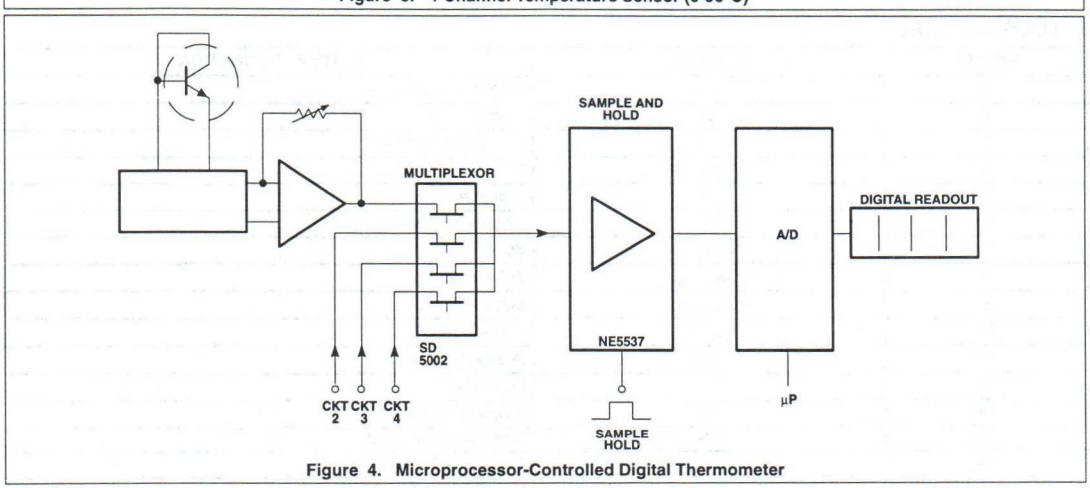


Figure 4. Microprocessor-Controlled Digital Thermometer

Dual operational transconductance amplifier

NE5517/5517A

DESCRIPTION

The NE5517 contains two current-controlled transconductance amplifiers, each with a differential input and push-pull output. The NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10dB signal-to-noise improvement referenced to 0.5% THD. The NE5517 is suited for a wide variety of industrial and consumer applications and is recommended as the preferred circuit in the Dolby* HX (Headroom Extension) system.

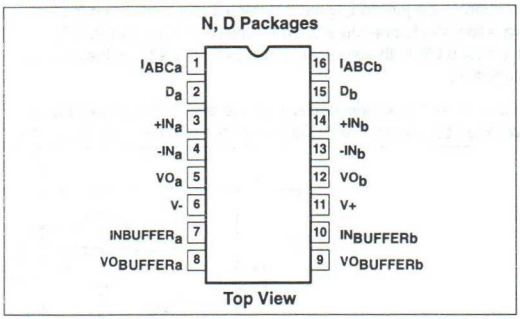
Constant impedance buffers on the chip allow general use of the NE5517. These buffers are made of Darlington transistor and a biasing network which changes bias current in dependence of I_{ABC}.

Therefore, changes of output offset voltages are almost eliminated. This is an advantage of the NE5517 compared to LM13600. With the LM13600, a burst in the bias current I_{ABC} guides to an audible offset voltage change at the output. With the constant impedance buffers of the NE5517 this effect can be avoided and makes this circuit preferable for high quality audio applications.

FEATURES

- Constant impedance buffers
- ΔVBE of buffer is constant with amplifier IBIAS change
- Pin compatible with LM13600
- Excellent matching between amplifiers
- Linearizing diodes
- High output signal-to-noise ratio

PIN CONFIGURATION



APPLICATIONS

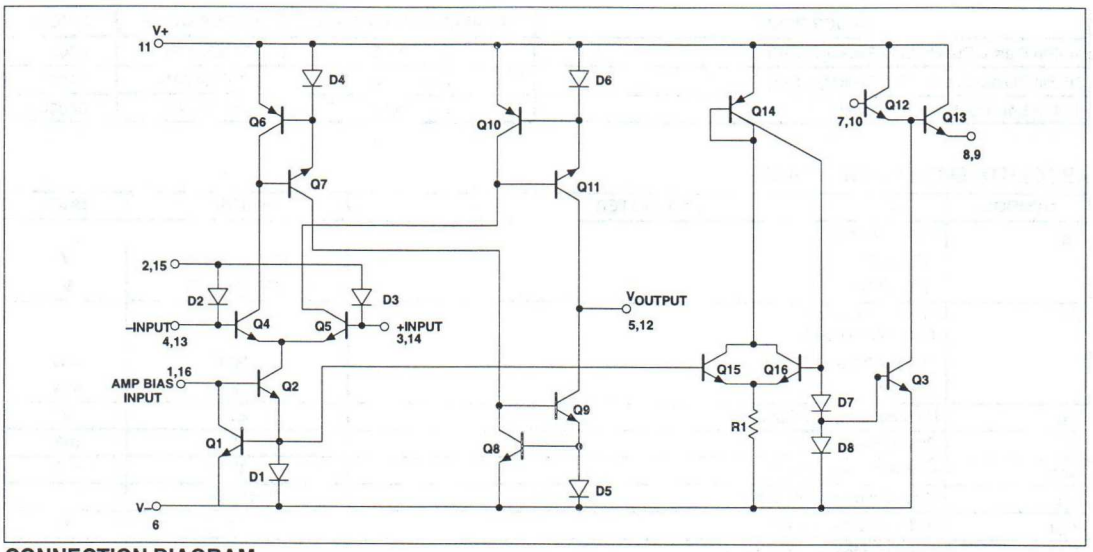
- Multiplexers
- Timers
- Electronic music synthesizers
- Dolby™ HX Systems
- Current-controlled amplifiers, filters
- Current-controlled oscillators, impedances

Dolby is a registered trademark of Dolby Laboratories Inc., San Francisco, Calif.

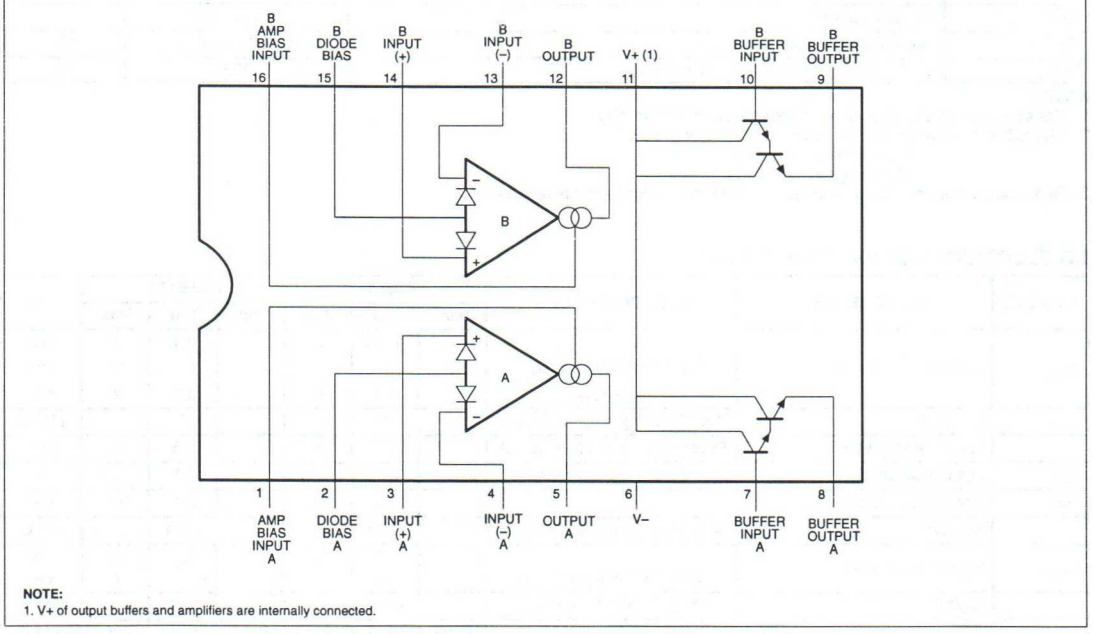
PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	I_{ABC}	Amplifier bias input A
2	D	Diode bias A
3	+IN	Non-inverting input A
4	-IN	Inverting input A
5	V_O	Output A
6	V-	Negative supply
7	IN_{BUFFER}	Buffer input A
8	VO_{BUFFER}	Buffer output A
9	VO_{BUFFER}	Buffer output B
10	IN_{BUFFER}	Buffer input B
11	V+	Positive supply
12	V_O	Output B
13	-IN	Inverting input B
14	+IN	Non-inverting input B
15	D	Diode bias B
16	I_{ABC}	Amplifier bias input B

CIRCUIT SCHEMATIC



CONNECTION DIAGRAM



NOTE:
1. V+ of output buffers and amplifiers are internally connected.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5517N	0406C
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5517AN	0406C
16-Pin Small Outline (SO) Package	0 to +70°C	NE5517D	0005D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage[1]		
	NE5517	36 V_{DC} or ±18	V
	NE5517A	44 V_{DC} or ±22	V
P_D	Power dissipation, T_A=25°C (still air)[2]		
	NE5517N, NE5517AN	1500	mW
	NE5517D	1125	mW
V_{IN}	Differential input voltage	±5	V
I_D	Diode bias current	2	mA
I_{ABC}	Amplifier bias current	2	mA
I_{SC}	Output short-circuit duration	Indefinite	
I_{OUT}	Buffer output current[3]	20	mA
T_A	Operating temperature range		
	NE5517N, NE5517AN	0°C to +70	°C
V_{DC}	DC input voltage	$+V_S$ to $-V_S$	
T_{STG}	Storage temperature range	-65°C to +150°C	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. For selections to a supply voltage above ±22V, contact factory
2. The following derating factors should be applied above 25°C
   N package at 12.0mW/°C
   D package at 9.0mW/°C
3. Buffer output current should be limited so as to not exceed package dissipation.

DC ELECTRICAL CHARACTERISTICS[1]

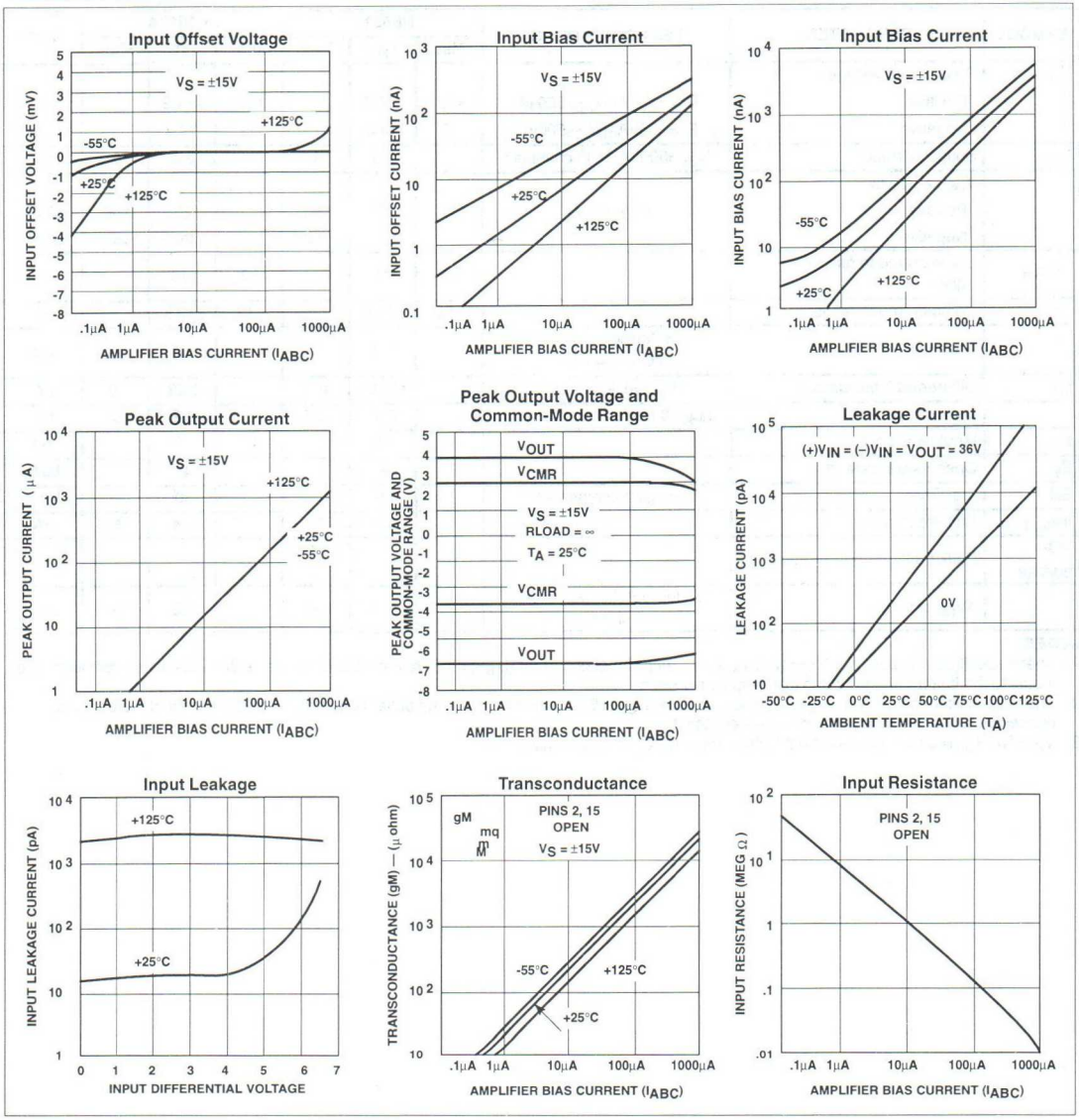
SYMBOL	PARAMETER	TEST CONDITIONS	NE5517			NE5517A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage			0.4	5		0.4	2	mV
		Over temperature range						5	mV
		I_{ABC} 5µA		0.3	5		0.3	2	mV
	$\Delta V_{OS}/\Delta T$	Avg. TC of input offset voltage		7			7		µV/°C
	V_{OS} including diodes	Diode bias current (I_D)=500µA		0.5	5		0.5	2	mV
V_{OS}	Input offset change	5µA ≤ I_{ABC} ≤ 500µA		0.1			0.1	3	mV
I_{OS}	Input offset current			0.1	0.6		0.1	0.6	µA
	$\Delta I_{OS}/\Delta T$	Avg. TC of input offset current		0.001			0.001		µA/°C
I_{BIAS}	Input bias current			0.4	5		0.4	5	µA
		Over temperature range		1	8		1	7	µA
	$\Delta I_B/\Delta T$	Avg. TC of input current		0.01			0.01		µA/°C
g_M	Forward transconductance		6700	9600	13000	7700	9600	12000	µmho
		Over temperature range	5400			4000			µmho
	g_M tracking			0.3			0.3		dB
I_{OUT}	Peak output current	R_L=0, I_{ABC}=5µA		5		3	5	7	µA
		R_L=0, I_{ABC}=500µA	350	500	650	350	500	650	µA
		R_L=0,	300			300			µA

DC ELECTRICAL CHARACTERISTICS[1] (continued)

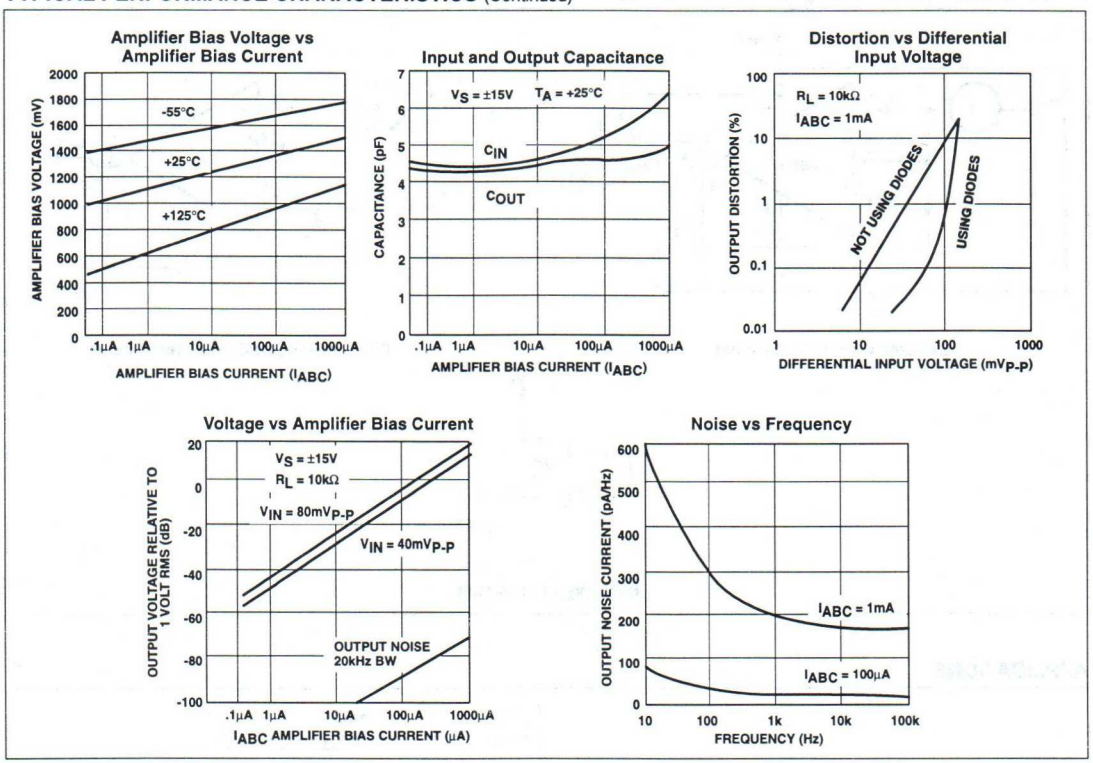
SYMBOL	PARAMETER	TEST CONDITIONS	NE5517			NE5517A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Peak output voltage								
	Positive	R_L=∞, 5μA≤I_{ABC}≤500μA	+12	+14.2		+12	+14.2		V
	Negative	R_L=∞, 5μA≤I_{ABC}≤500μA	-12	-14.4		-12	-14.4		V
I_{CC}	Supply current	I_{ABC}=500μA, both channels		2.6	4		2.6	4	mA
	V_{OS} sensitivity								
	Positive	Δ V_{OS}/Δ V+		20	150		20	150	μV/V
	Negative	Δ V_{OS}/Δ V-		20	150		20	150	μV/V
CMRR	Common-mode rejection ration		80	110		80	110		dB
	Common-mode range		±12	±13.5		±12	±13.5		V
	Crosstalk	Referred to input[2] 20Hz<f<20kHz		100			100		dB
I_{IN}	Differential input current	I_{ABC}=0, input=±4V		0.02	100		0.02	10	nA
	Leakage current	I_{ABC}=0 (Refer to test circuit)		0.2	100		0.2	5	nA
R_{IN}	Input resistance		10	26		10	26		kΩ
B_W	Open-loop bandwidth			2			2		MHz
SR	Slew rate	Unity gain compensated		50			50		V/μs
IN_{BUFFER}	Buff. input current	5		0.4	5		0.4	5	μA
VO-BUFFER	Peak buffer output voltage	5	10			10			V
	ΔV_{BE} of buffer	Refer to Buffer V_{BE} test[3] circuit		0.5	5		0.5	5	mV

NOTES:
1. These specifications apply for V_S=±15V, T_A=25°C, amplifier bias current (I_{ABC})=500μA, Pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
2. These specifications apply for V_S=±15V, I_{ABC}=500μA, R_{OUT}=5kΩ connected from the buffer output to -V_S and the input of the buffer is connected to the transconductance amplifier output.
3. V_S=±15, R_{OUT}=5kΩ connected from Buffer output to -V_S and 5μA ≤I_{ABC} ≤500μA.

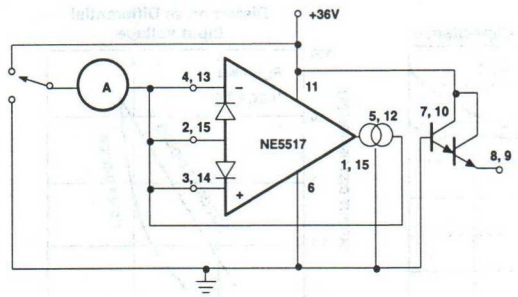
TYPICAL PERFORMANCE CHARACTERISTICS



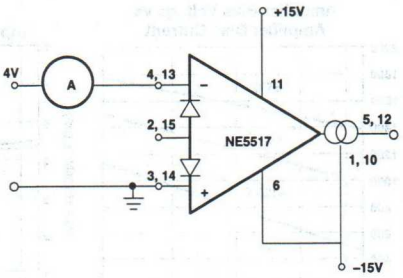
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



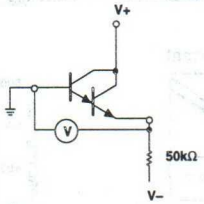
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



Leakage Current Test Circuit

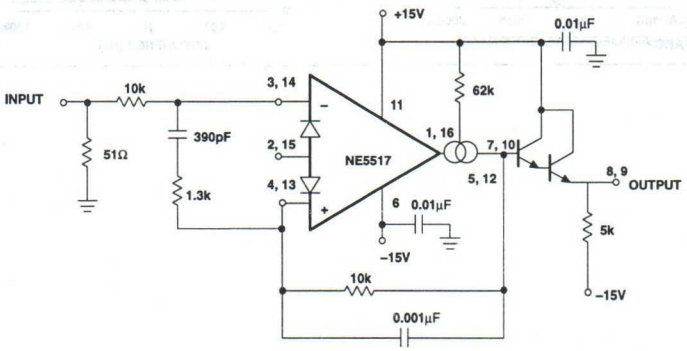


Differential Input Current Test Circuit



Buffer V_{BE} Test Circuit

APPLICATIONS



Unity Gain Follower

CIRCUIT DESCRIPTION

The circuit schematic diagram of one-half of the NE5517, a dual operational transconductance amplifier with linearizing diodes and impedance buffers, is shown in Figure 1.

1. Transconductance Amplifier

The transistor pair, Q_4 and Q_5, forms a transconductance stage. The ratio of their collector currents (I_4 and I_5, respectively) is defined by the differential input voltage, V_{IN}, which is shown in equation 1.

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \qquad (1)$$

Where V_{IN} is the difference of the two input voltages

KT ≡ 26mV at room temperature (300°k).

Transistors Q_1, Q_2 and diode D_1 form a current mirror which focuses the sum of current I_4 and I_5 to be equal to amplifier bias current I_B:

$$I_4 + I_5 = I_B \qquad (2)$$

If V_{IN} is small, the ratio of I_5 and I_4 will approach unity and the Taylor series of ln function can be approximated as

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \qquad (3)$$

and $I_4 \equiv I_5 \equiv I_B$

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{1/2I_B} = \frac{2KT}{q} \frac{I_5 - I_4}{I_B} = V_{IN}^{(4)}$$

$$I_5 - I_4 = V_{IN} \frac{\left(I_B \frac{q}{}\right)}{2KT}$$

The remaining transistors (Q_6 to Q_{11}) and diodes (D_4 to D_6) form three current mirrors that produce an output current equal to I_5 minus I_4. Thus:

$$V_{IN}\left(I_B \frac{q}{2KT}\right) = I_O \qquad (5)$$

The term $\frac{\left(I_B \frac{q}{}\right)}{2KT}$ is then the transconductance

of the amplifier and is proportional to I_B.

2. Linearizing Diodes

For V_{IN} greater than a few millivolts, equation 3 becomes invalid and the transconductance increases non-linearly. Figure 2 shows how the internal diodes can linearize the transfer function of the operational amplifier. Assume D_2 and D_3 are biased with current sources and the input signal current is I_S. Since

$I_4 + I_5 = I_B$ and $I_5 - I_4 = I_O$, that is:

$I_4 = (I_B - I_O)$, $I_5 = (I_B + I_O)$

For the diodes and the input transistors that have identical geometries and are subject to similar voltages and temperatures, the following equation is true:

$$\frac{T}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{KT}{q} \cdot \ln \frac{1/2(I_B + I_O)}{1/2(I_B - I_O)} \qquad (6)$$

$$I_O = I_S \frac{2I_B}{I_D} \text{ for } |I_S| < \frac{I_D}{2}$$

The only limitation is that the signal current should not exceed I_D.

3. Impedance Buffer

The upper limit of transconductance is defined by the maximum value of I_B (2mA). The lowest value of I_B for which the amplifier will function therefore determines the overall dynamic range. At low values of I_B, a buffer with very low input bias current is desired. A Darlington amplifier with constant-current source (Q_{14}, Q_{15}, Q_{16}, D_7, D_8, and R_1) suits the need.

APPLICATIONS

Voltage-Controlled Amplifier

In Figure 3, the voltage divider R_2, R_3 divides the input-voltage into small values (mV range) so the amplifier operates in a linear manner.

It is:

$$I_{OUT} = -V_{IN} \cdot \frac{R_3}{R_2 + R_3} \cdot gM;$$

$$V_{OUT} = I_{OUT} \cdot R_L;$$

$$A = \frac{V_{OUT}}{V_{IN}} = \frac{R_3}{R_2 + R_3} \cdot gM \cdot R_L$$

(3) $g_M = 19.2\, I_{ABC}$

(g_M in µmhos for I_{ABC} in mA)

Since g_M is directly proportional to I_{ABC}, the amplification is controlled by the voltage V_C in a simple way.

When V_C is taken relative to $-V_{CC}$ the following formula is valid:

$$I_{ABC} = \frac{(V_C - 1.2V)}{R_1}$$

The 1.2V is the voltage across two base-emitter baths in the current mirrors. This circuit is the base for many applications of the NE5517.

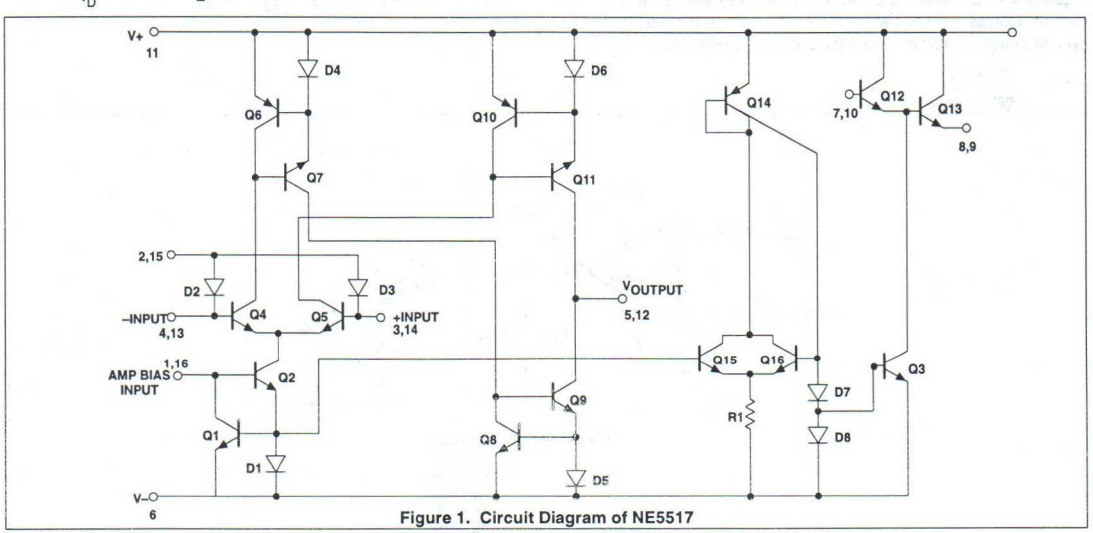


Figure 1. Circuit Diagram of NE5517

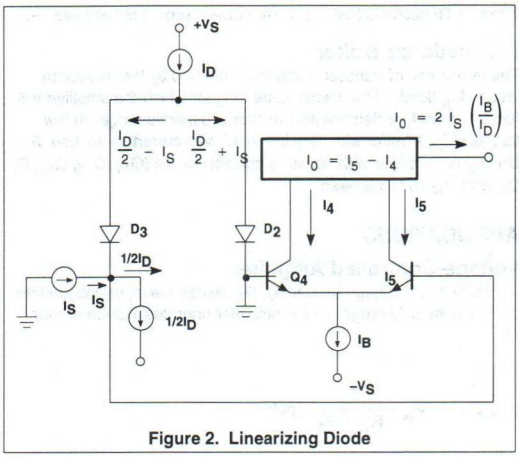


Figure 2. Linearizing Diode

Stereo Amplifier With Gain Control

Figure 4 shows a stereo amplifier with variable gain via a control input. Excellent tracking of typical 0.3dB is easy to achieve. With the potentiometer, R_P, the offset can be adjusted. For AC-coupled amplifiers, the potentiometer may be replaced with two 510Ω resistors.

Modulators

Because the transconductance of an OTA (Operational Transconductance Amplifier) is directly proportional to I_{ABC}, the amplification of a signal can be controlled easily. The output current is the product from transconductance×input voltage. The circuit is effective up to approximately 200kHz. Modulation of 99% is easy to achieve.

Voltage-Controlled Resistor (VCR)

Because an OTA is capable of producing an output current proportional to the input voltage, a voltage variable resistor can be made. Figure 6 shows how this is done. A voltage presented at the R_X terminals forces a voltage at the input. This voltage is multiplied by g_M and thereby forces a current through the R_X terminals:

$$R_X = \frac{R + R_A}{gM + R_A}$$

where g_M is approximately 19.21 μMHOs at room temperature. Figure 7 shows a Voltage Controlled Resistor using linearizing diodes. This improves the noise performance of the resistor.

Voltage-Controlled Filters

Figure 8 shows a Voltage Controlled Low-Pass Filter. The circuit is a unity gain buffer until X_C/g_M is equal to R/R_A. Then, the frequency response rolls off at a 6dB per octave with the -3dB point being defined by the given equations. Operating in the same manner, a Voltage Controlled High-Pass Filter is shown in Figure 9. Higher order filters can be made using additional amplifiers as shown in Figures 10 and 11.

Voltage-Controlled Oscillators

Figure 12 shows a voltage-controlled triangle-square wave generator. With the indicated values a range from 2Hz to 200kHz is possible by varying I_{ABC} from 1mA to 10μA.

The output amplitude is determined by $I_{OUT} \times R_{OUT}$.

Please notice the differential input voltage is not allowed to be above 5V.

With a slight modification of this circuit you can get the sawtooth pulse generator, as shown in Figure 13.

APPLICATION HINTS

To hold the transconductance g_M within the linear range, I_{ABC} should be chosen not greater than 1mA. The current mirror ratio should be as accurate as possible over the entire current range. A current mirror with only two transistors is not recommended. A suitable current mirror can be built with a PNP transistor array which causes excellent matching and thermal coupling among the transistors. The output current range of the DAC normally reaches from 0 to -2mA. In this application, however, the current range is set through R_{REF} (10kΩ) to 0 to -1mA.

$$I_{DACMAX} = 2 \cdot \frac{V_{REF}}{R_{REF}} = 2 \cdot \frac{5V}{10k} = 1mA$$

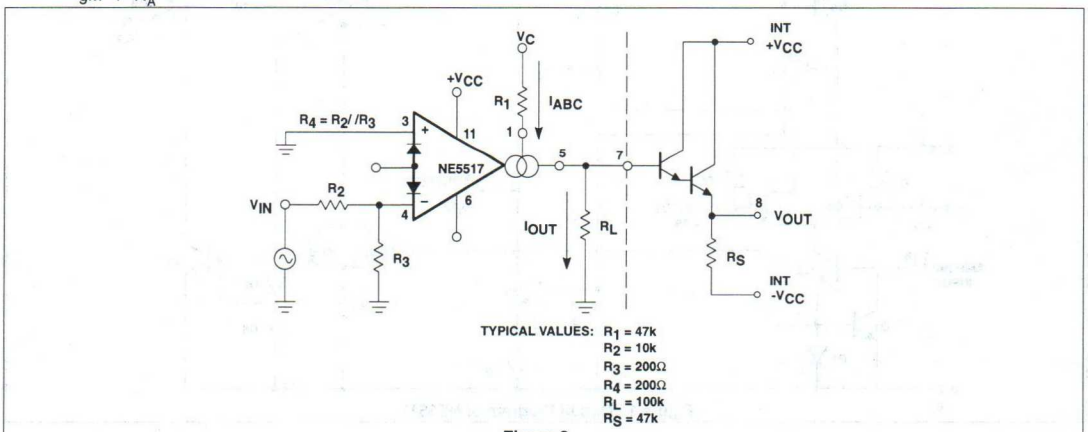


Figure 3.

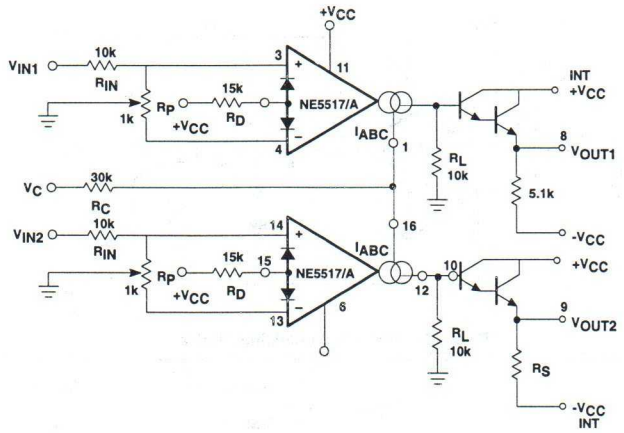


Figure 4. Gain-Controlled Stereo Amplifier

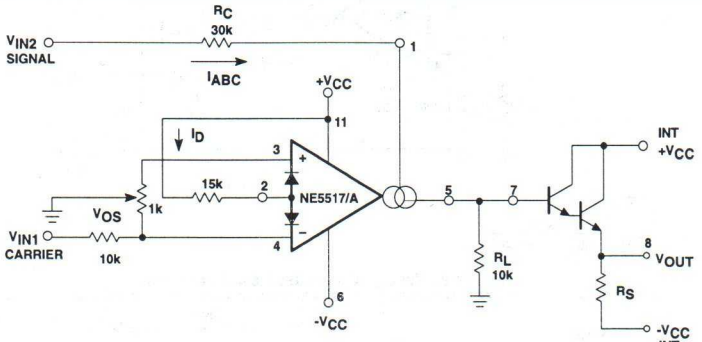


Figure 5. Amplitude Modulator

$$R_X = \frac{R + R_A}{g_M \cdot R_A}$$

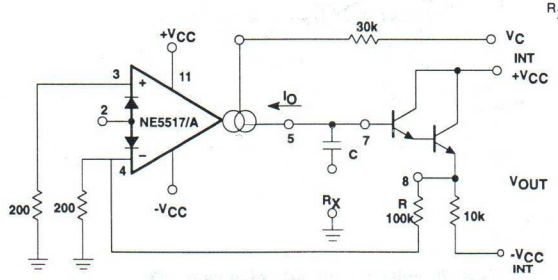


Figure 6. VCR

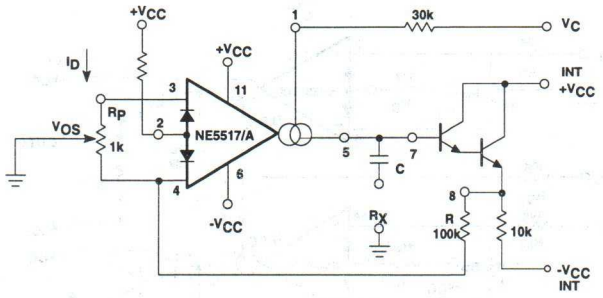
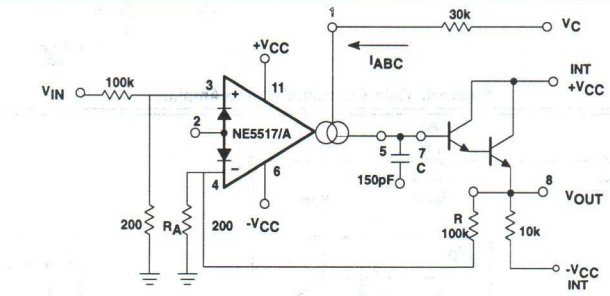


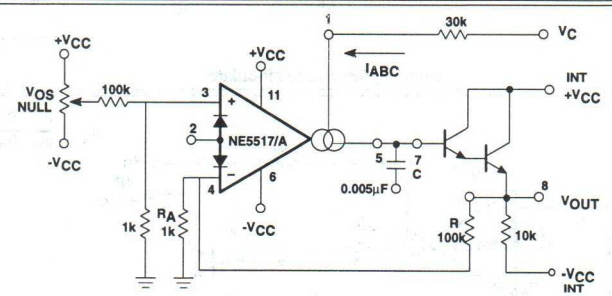
Figure 7. VCR with Linearizing Diodes



NOTE:

$$f_O = \frac{R_A\, g_M}{g(R + RA)\, 2\pi C}$$

Figure 8. Voltage-Controlled Low-Pass Filter



NOTE:

$$f_O = \frac{R_A\, g_M}{g(R + RA)\, 2\pi C}$$

Figure 9. Voltage-Controlled High-Pass Filter

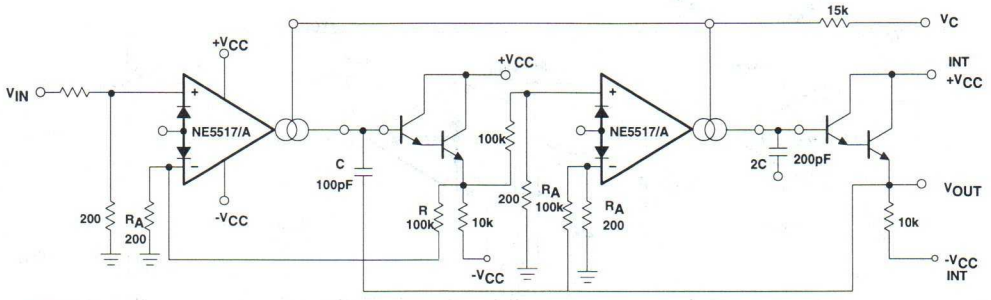


Figure 10. Butterworth Filter – 2nd Order

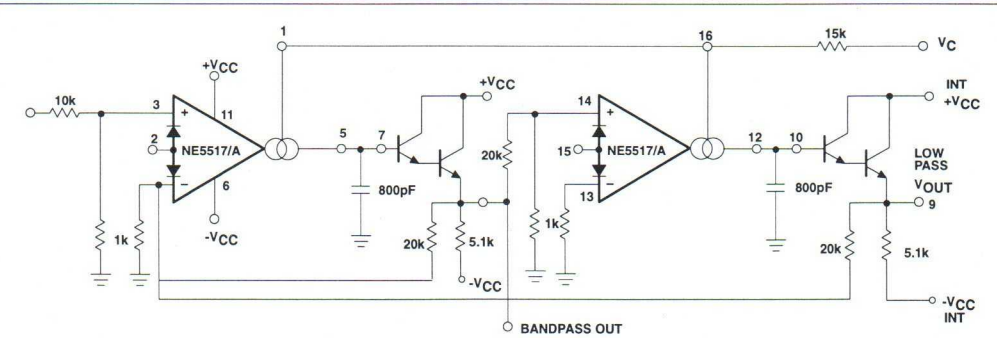


Figure 11. State Variable Filter

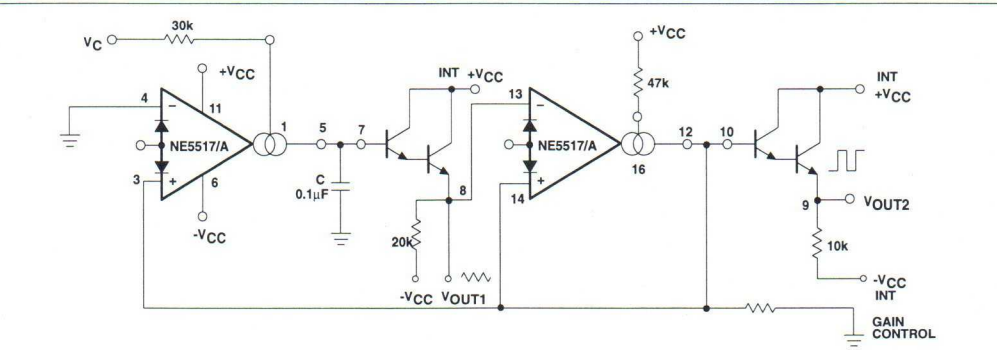


Figure 12. Triangle-Square Wave Generator (VCO)

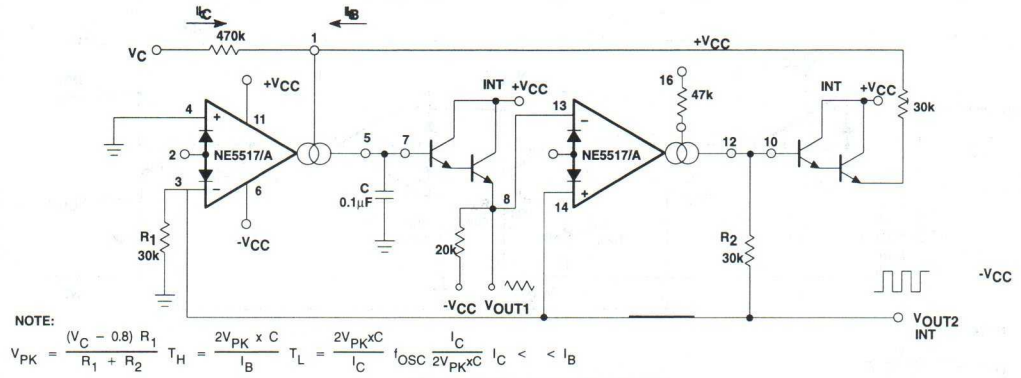


Figure 13. Sawtooth Pulse VCO

NE5517/A transconductance amplifier applications AN145

DESCRIPTION

The Philips Semiconductors NE5517 is a truly versatile dual operational transconductance amplifier. In plain language, it is a voltage–to–current converter governed by the transconductance g_m, which is equivalent to I_{OUT}/V_{IN}. The g_m is increased or decreased linearly by varying the amplifier bias current (I_{ABC}) through an external pin (see Figure 1). From the proper use of the I_{ABC} pin, many control circuits can be realized.

For more insight into the way the part operates, the transconductance can be thought of as gain and is governed by the following equation:

$$g_M = \frac{I_{OUT}}{V_{IN}} = \frac{I_{ABCq}}{2KT} \qquad (1)$$

where the transconductance is dependent on the constant KT/q (which is 26mV at 25°C, and I_{ABC} (which is controlled by the user).

To make the device more universal and adaptable for many functions, two impedance buffers for voltage output applications are also included with the amps so that the part can be used as a programmable operational amplifier.

Linearizing diodes provide another useful option. These should be applied when large input voltages or wide temperature variations are encountered. To show the significance of the diodes, compare the difference between Equation 1 without diodes and Equation 2 with diodes:

$$\frac{I_{OUT}}{V_{IN}} = \frac{2I_{ABC}}{R_{IN}\ I_D} \qquad (2)$$

for I_{IN} greater than $\frac{I_D}{2}$

Here, it can be seen that the transconductance is not temperature dependent. R_{IN} is the signal input resistance and I_{IN} is the signal current. I_{IN} must not exceed half the diode current (I_D, nominally 1mA). The diode current is set by a resistor tied to $+V_{CC}$. A graph showing the output distortion improvement versus differential input voltage when using the diodes is shown in Figure 2.

An advantage that the NE5517 has over similar devices is a special biasing network between the amplifier and output impedance buffers. This network eliminates output offset current changes with a sudden change in the

bias current (I_{ABC}). This is particularly important in audio applications where an audible offset would be produced.

APPLICATIONS

An application employing both amplifiers and buffers internal to the NE5517 is the adjustable triangle–square wave generator shown in Figure 3.

The center oscillating frequency is set by the capacitor C at the output of amplifier A. The output amplitude is set by the resistor R connected between the non–inverting inputs, amplifier B output, buffer B input and ground.

The oscillating frequency is varied by changing V_C, which in turn controls the amplifier bias current (I_{ABC1}). If a positive voltage is applied to V_C, the center frequency will increase linearly with increasing voltage. If a negative is applied, the center frequency will decrease linearly with increasing negative voltage. This makes a very good programmable oscillator with variable amplitude.

By using a large value capacitor and negative control voltage, oscillations in the fractions of Hertz can be realized; a small capacitor and positive control voltage will give frequencies up to 500kHz. Graphs showing the linearity of control voltage versus frequency for different capacitor values are shown in Figure 4.

Pertinent calculations are:

$$f_C = \frac{I_{ABC1}}{2(C)\ (I_{ABC2})\ (R)}$$

Where : f_C = center frequency
I_{ABC1} = oscillator control current
I_{ABC2} = amplitude control current
R = amplitude control resistor
C = oscillator control capacitor

Also : Amplitude = $(I_{ABC2})\ (R)$

Another very useful application is to use the NE5517 as a digitally–programmable amplifier. The entire circuit is shown in Figure 5.

The circuit consists of a Philips Semiconductors microprocessor–compatible DAC, a transistor array, and the NE5517 configured as a voltage–controlled amplifier. This arrangement can also be used with the VCO explained earlier to program its oscillating frequency.

The pertinent equations governing this application are as follows:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{BW(10)}{256} \times \frac{I_{DACMAX} \times q \times R_L}{2 \times KT}$$

Where : BW(10) = binary word decimal
I_{DACMAX} = maximum DAC output current (1mA)
R_L = load resistance (30k)
q/KT = 38.5 at 25°C

Also:

$$I_{DACMAX} = 2 \times \frac{V_{REF}}{R_{REF}} = 2 \times \frac{5k}{10k} = 1mA$$

Where : V_{REF} = supplied by DAC (5V)
R_{REF} = referenced resistor (10kΩ)

The $I_{DAC\ MAX}$ of 1mA is used to keep the transconductance within the linear range.

The current mirror matches the current flow into the DAC and supplies the same amount to the 5517 control pin. Using a current output DAC is much faster than using a voltage output device to control the part. (If speed is not important, this can be done and the current mirror can be replaced with a resistor.) Also, the gain equation pertains to the signal after the input divider.

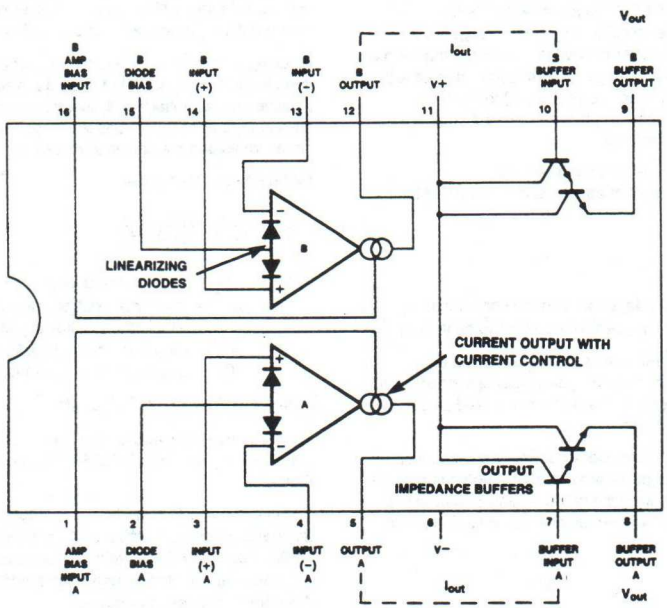


Figure 1. Pin Designation and Functional Diagram

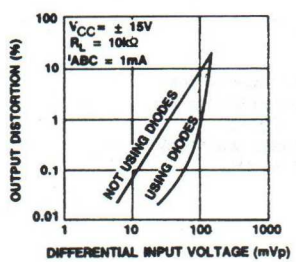


Figure 2. Output Distortion vs Input Voltage Showing Benefit of Diodes

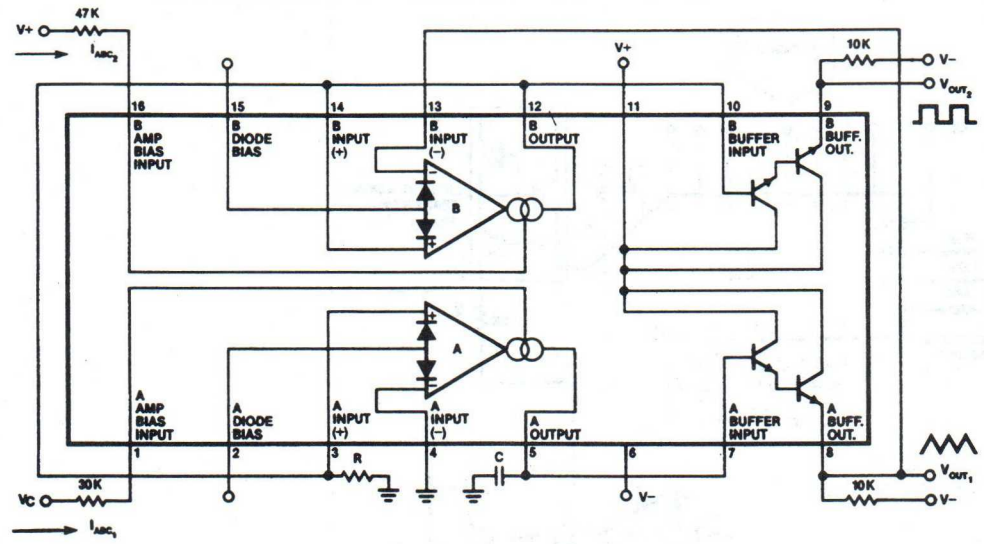
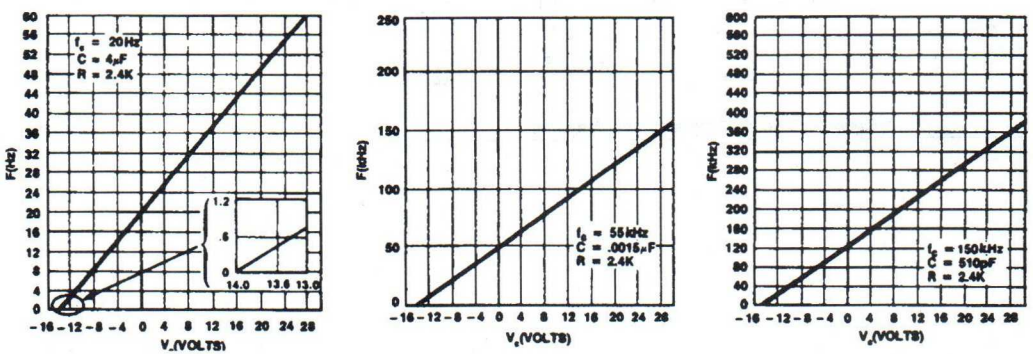


Figure 3. Triangle-Square Wave Generator



NOTE:
V_C Below −13.6V or above +30V will cause distortion.
Changing the C value will vary the frequency range.

Figure 4. Control Voltage (V_C) vs Frequency Data

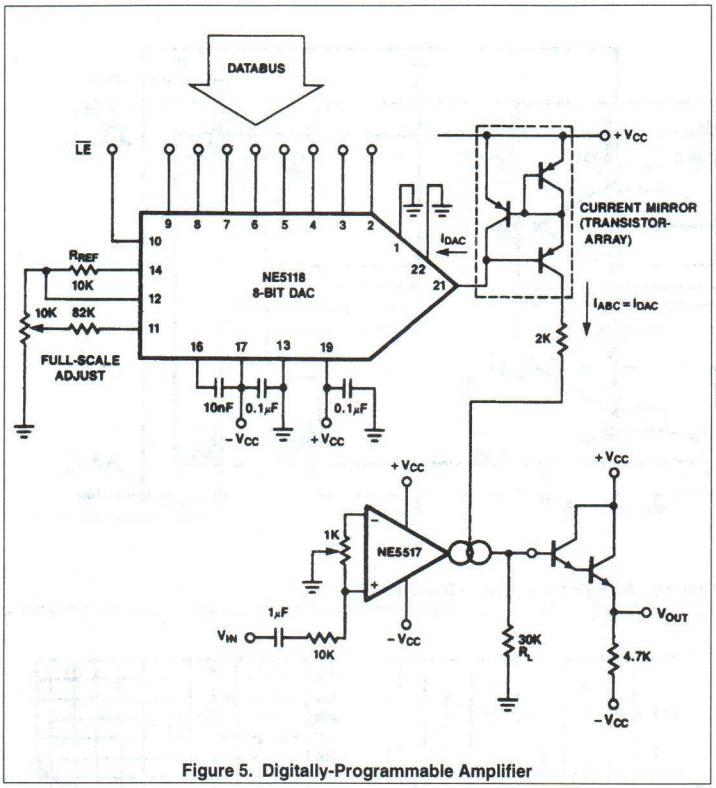


Figure 5. Digitally-Programmable Amplifier

Internally-compensated dual low noise operational amplifier

NE/SE5532/5532A

DESCRIPTION

The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

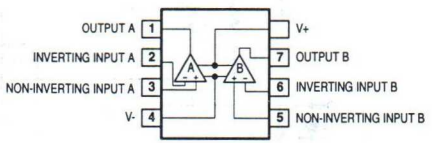
This makes the device especially suitable for application in high-quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used because it has guaranteed noise voltage specifications.

FEATURES

- Small-signal bandwidth: 10MHz
- Output drive capability: 600Ω, $10V_{RMS}$
- Input noise voltage: $5nV/\sqrt{Hz}$ (typical)
- DC voltage gain: 50000
- AC voltage gain: 2200 at 10kHz
- Power bandwidth: 140kHz
- Slew rate: 9V/μs
- Large supply voltage range: ±3 to ±20V
- Compensated for unity gain

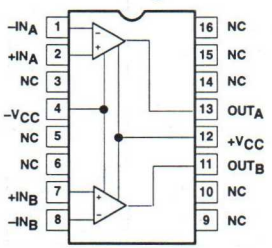
PIN CONFIGURATIONS

FE, N Packages



TOP VIEW

D Package[1]



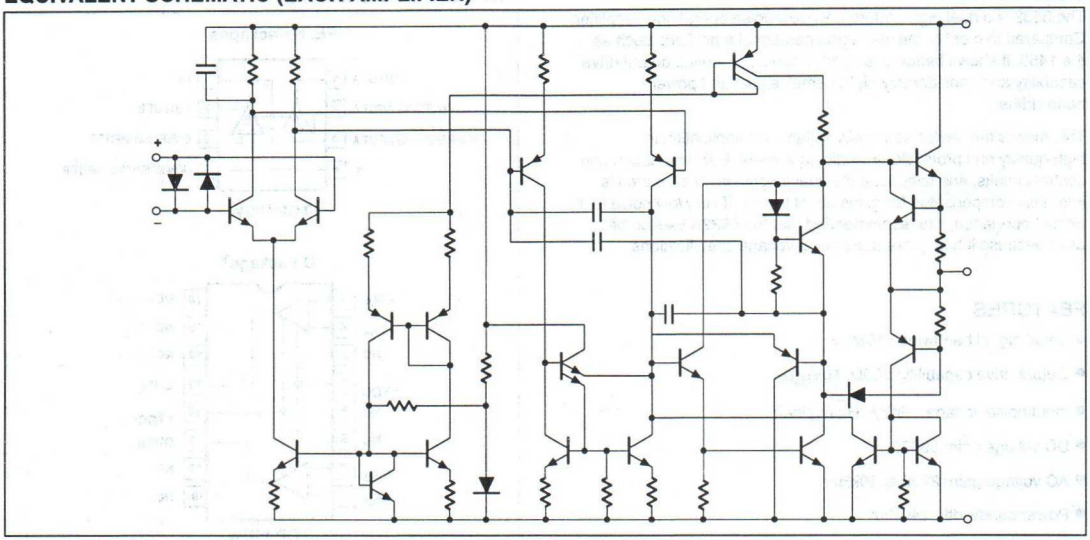
TOP VIEW

NOTE:
1. SOL and non-standard pinout.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to 70°C	NE5532N	0404B
8-Pin Ceramic Dual In-Line Package (CERDIP)	0 to 70°C	NE5532FE	0580A
8-Pin Plastic Dual In-Line Package (DIP)	0 to 70°C	NE5532AN	0404B
8-Pin Ceramic Dual In-Line Package (CERDIP)	0 to 70°C	NE5532AF	0580A
8-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE5532FE	0580A
8-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE5532AF	0580A
16-Pin Plastic Small Outline Large (SOL) Package	0 to 70°C	NE5532D	0171B
16-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE5532N	0406C

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	$\pm V_{SUPPLY}$	V
V_{DIFF}	Differential input voltage[1]	±0.5	V
T_A	Operating temperature range		
	NE5532/A	0 to 70	°C
	SE5532/A	-55 to +125	°C
T_{STG}	Storage temperature	-65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Maximum power dissipation, T_A=25°C (still-air)[2]		
	8 N package	1200	mW
	8 FE package	1000	mW
	16 D package	1200	mW
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. Thermal resistances of the above packages are as follows:
   N package at 100°C/W
   F package at 135°C/W
   D package at 105°C/W

DC ELECTRICAL CHARACTERISTICS

T_A=25°C V_S=±15V, unless otherwise specified. [1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	SE5532/5532A			NE5532/5532A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			0.5	2		0.5	4	mV
		Over temperature			3			5	mV
$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Offset current				100		10	150	nA
		Over temperature			200			200	nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_B	Input current			200	400		200	800	nA
		Over temperature			700			1000	nA
$\Delta I_B/\Delta T$				5			5		nA/°C
I_{CC}	Supply current			8	10.5		8	16	mA
		Over temperature			13				mA
V_{CM}	Common-mode input range		±12	±13		±12	±13		V
CMRR	Common-mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	µV/V
A_{VOL}	Large-signal voltage gain	R_L≥2kΩ, V_O=±10V	50	100		25	100		V/mV
		Over temperature	25			15			V/mV
		R_L≥600Ω, V_O=±10V	40	50		15	50		V/mV
		Over temperature	20			10			V/mV
V_{OUT}	Output swing	R_L≥600Ω	±12	±13		±12	±13		V
		Over temperature	±10	±12		±10	±12		
		R_L≥600Ω, V_S=±18V	±15	±16		±15	±16		
		Over temperature	±12	±14		±12	±14		
		R_L≥2kΩ	±13	±13.5		±13	±13.5		
		Over temperature	±12	±12.5		±10	±12.5		
R_{IN}	Input resistance		30	300		30	300		kΩ
I_{SC}	Output short circuit current		10	38	60	10	38	60	mA

NOTES:

1. Diodes protect the inputs against overvoltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For operation at elevated temperature, derate packages based on the package thermal resistance.
3. Output may be shorted to ground at V_S=±15V, T_A=25°C Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

AC ELECTRICAL CHARACTERISTICS

T_A=25°C V_S=±15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SE5532/5532A			UNIT
			Min	Typ	Max	
R_{OUT}	Output resistance	A_V=30dB Closed-loop f=10kHz, R_L=600Ω		0.3		Ω
	Overshoot	Voltage-follower V_{IN}=100mV_{P-P} C_L=100pF, R_L=600Ω		10		%
A_V	Gain	f=10kHz		2.2		V/mV
GBW	Gain bandwidth product	C_L=100pF, R_L=600Ω		10		MHz
SR	Slew rate			9		V/µs
	Power bandwidth	V_{OUT}=±10V		140		kHz
		V_{OUT}=±14V, R_L=600Ω, V_{CC}=±18V		100		kHz

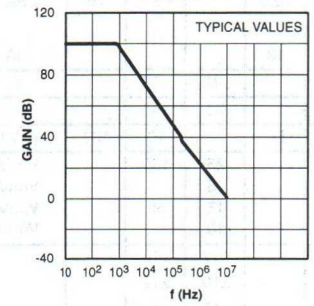
ELECTRICAL CHARACTERISTICS

T_A=25°C V_S=±15V, unless otherwise specified.

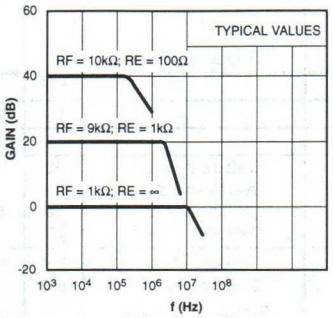
SYMBOL	PARAMETER	TEST CONDITIONS	NE/SE5532			NE/SE5532A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{NOISE}	Input noise voltage	f_O=30Hz		8			8	12	nV/√Hz
		f_O=1kHz		5			5	6	nV/√Hz
I_{NOISE}	Input noise current	f_O=30Hz		2.7			2.7		pA/√Hz
		f_O=1kHz		0.7			0.7		pA/√Hz
	Channel separation	f=1kHz, R_S=5kΩ		110			110		dB

TYPICAL PERFORMANCE CHARACTERISTICS

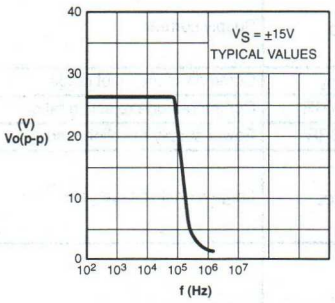
Open-Loop Frequency Response



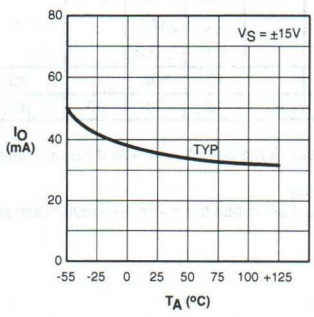
Closed-Loop Frequency Response



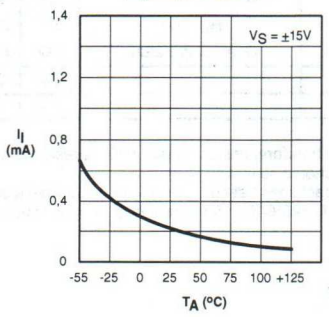
Large-Signal Frequency Response



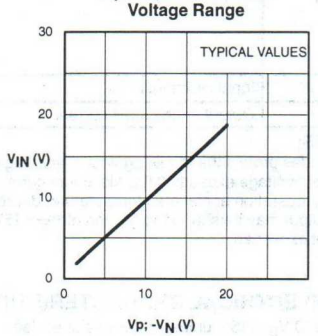
Output Short-Circuit Current



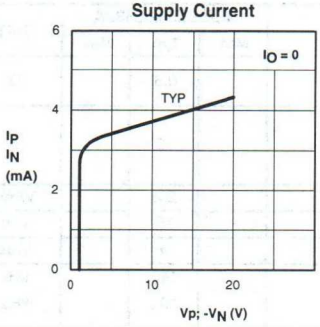
Input Bias Current



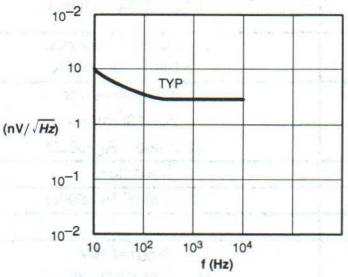
Input Commom-Mode Voltage Range



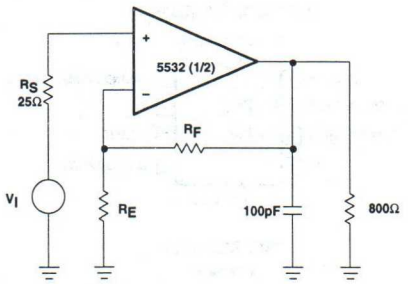
Supply Current



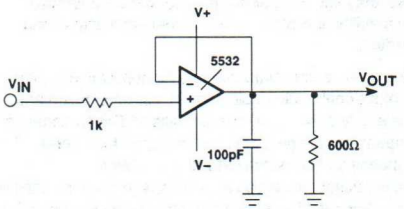
Input Noise Voltage Density



TEST CIRCUITS



Closed-Loop Frequency Response



Voltage-Follower

Dual and single low noise op amp

NE5533/5533A/ NE/SA/SE5534/5534A

DESCRIPTION

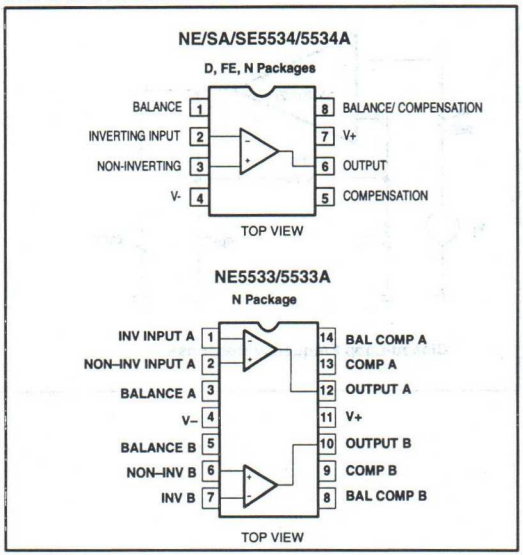
The 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

FEATURES

- Small-signal bandwidth: 10MHz
- Output drive capability: 600Ω, $10V_{RMS}$ at VS=±18V
- Input noise voltage: $4nV/\sqrt{Hz}$
- DC voltage gain: 100000
- AC voltage gain: 6000 at 10kHz
- Power bandwidth: 200kHz
- Slew rate: 13V/µs
- Large supply voltage range: ±3 to ±20V

PIN CONFIGURATIONS



APPLICATIONS

- Audio equipment
- Instrumentation and control circuits
- Telephone channel amplifiers
- Medical equipment

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5533N	0405B
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5533AN	0405B
8-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5534D	0174C
8-Pin Hermetic Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE5534FE	
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5534N	0404B
8-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5534AD	0174C
8-Pin Hermetic Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE5534AF	
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5534AN	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA5534N	0404B
8-Pin Plastic Small Outline (SO) package	-40°C to +85°C	SA5534AD	0174C
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE5534N	0404B
8-Pin Hermetic Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE5534AF	
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE5534AN	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA5534AN	0404B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	±V supply	V
V_{DIFF}	Differential input voltage[1]	±0.5	V
T_A	Operating temperature range		
	SE	-55 to +125	°C
	SA	-40 to +85	°C
	NE	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Power dissipation at 25°C[2]		
	16D Pkg	1350	mW
	16N Pkg	1500	mW
	8D Pkg	750	mW
	8FE Pkg	800	mW
	8N Pkg	1150	mW
	Output short-circuit duration[3]	Indefinite	
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Diodes protect the inputs against over voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For operation at elevated temperature, derate packages based on the following junction-to-ambient thermal resistance:
   8-pin ceramic DIP 150°C/W
   8-pin plastic DIP 105°C/W
   8-pin plastic SO 160°C/W
   16-pin plastic DIP 80°C/W
   16-pin plastic SO 90°C/W
3. Output may be shorted to ground at V_S=±15V, T_A=25°C. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

DC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_S=±15V, unless otherwise specified. [1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5533/5533A NE/SA5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			0.5	2		0.5	4	mV
		Over temperature			3			5	mV
$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Offset current			10	200		20	300	nA
		Over temperature			500			400	nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_B	Input current			400	800		500	1500	nA
		Over temperature			1500			2000	nA
$\Delta I_B/\Delta T$				5			5		nA/°C
I_{CC}	Supply current			4	6.5		4	8	mA
	per op amp	Over temperature			9			10	mA
V_{CM}	Common mode input range		±12	±13		±12	±13		V
CMRR	Common mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	µV/V
A_{VOL}	Large-signal voltage gain	R_L≥600Ω, V_O=±10V	50	100		25	100		V/mV
		Over temperature	25			15			V/mV
V_{OUT}	Output swing	R_L≥600Ω	±12	±13		±12	±13		V
		Over temperature	±10	±12		±10	±12		V
		R_L≥600Ω, V_S=±18V	±15	±16		±15	±16		V
		R_L≥2kΩ	±13	±13.5		±13	±13.5		V
		Over temperature	±12	±12.5		±12	±12.5		V
R_{IN}	Input resistance		50	100		30	100		kΩ
I_{SC}	Output short circuit current			38			38		mA

NOTES:
1. For NE5533/5533A/5534/5534A, T_{MIN} = 0°C, T_{MAX} = 70°C
2. For SE5534/5534A, T_{MIN} = -55°C, T_{MAX} = +125°C
3. For SA5534/5534A, T_{MIN} = -40°C, T_{MAX} = +125°C

AC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_S=±15V, unless otherwise specified.

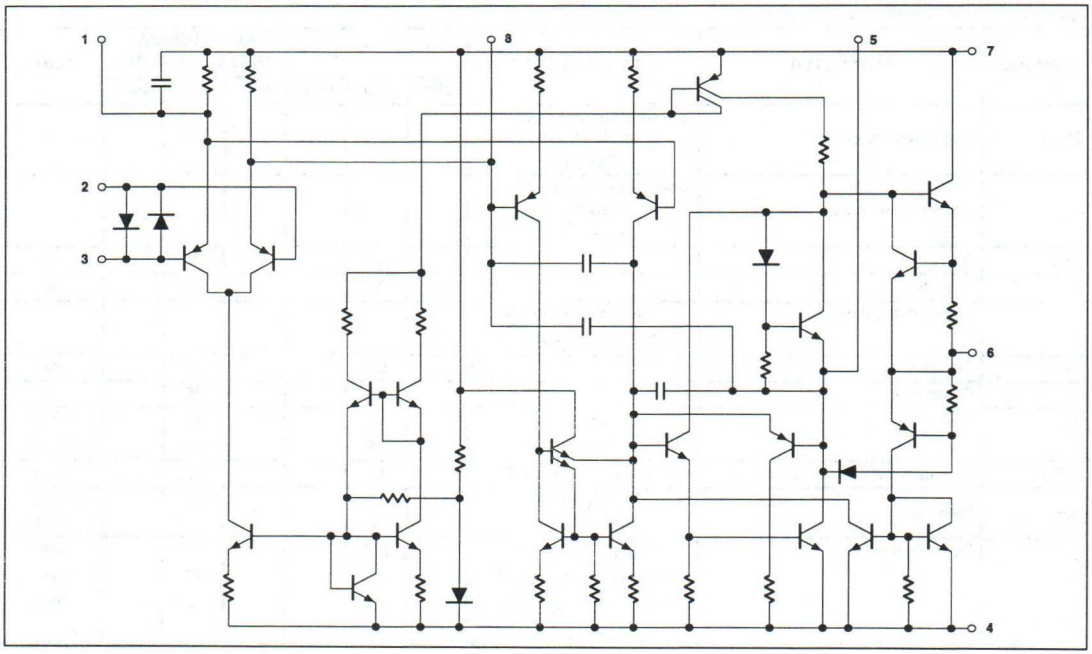
SYMBOL	PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5533/5533A NE/SA5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_{OUT}	Output resistance	A_V=30dB closed-loop f=10kHz, R_L=600Ω, C_C=22pF		0.3			0.3		Ω
	Transient response	Voltage-follower, V_{IN}=50mV R_L=600Ω, C_C=22pF, C_L=100pF							
t_R	Rise time			20			20		ns
	Overshoot			20			20		%
	Transient response	V_{IN}=50mV, R_L=600Ω C_C=47pF, C_L=500pF							
t_R	Rise time			50			50		ns
	Overshoot			35			35		%
A_V	Gain	f=10kHz, C_C=0		6			6		V/mV
		f=10kHz, C_C=22pF		2.2			2.2		V/mV
GBW	Gain bandwidth product	C_C=22pF, C_L=100pF		10			10		MHz
SR	Slew rate	C_C=0		13			13		V/µs
		C_C=22pF		6			6		V/µs
	Power bandwidth	V_{OUT}=±10V, C_C=0		200			200		kHz
		V_{OUT}=±10V, C_C=22pF		95			95		kHz
		V_{OUT}=±14V, R_L=600Ω C_C=22pF, V_{CC}=±18V		70			70		kHz

ELECTRICAL CHARACTERISTICS

T_A=25°C, V_S = 15V, unless otherwise specified.

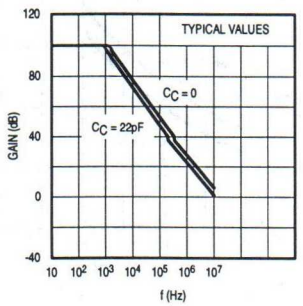
SYMBOL	PARAMETER	TEST CONDITIONS	5533/5534			5533A/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{NOISE}	Input noise voltage	f_O=30Hz		7			5.5	7	nV/√Hz
		f_O=1kHz		4			3.5	4.5	nV/√Hz
I_{NOISE}	Input noise current	f_O=30Hz		2.5			1.5		pA/√Hz
		f_O=1kHz		0.6			0.4		pA/√Hz
	Broadband noise figure	f=10Hz-20kHz, R_S=5kΩ					0.9		dB
	Channel separation	f=1kHz, R_S=5kΩ		110			110		dB

EQUIVALENT SCHEMATIC

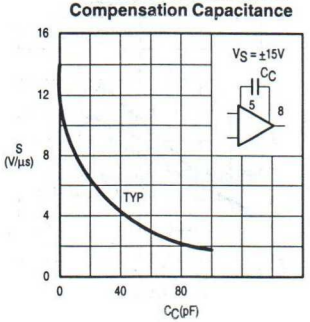


TYPICAL PERFORMANCE CHARACTERISTICS

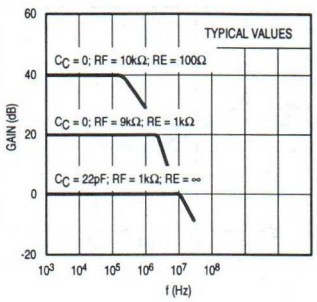
Open-Loop Frequency Response



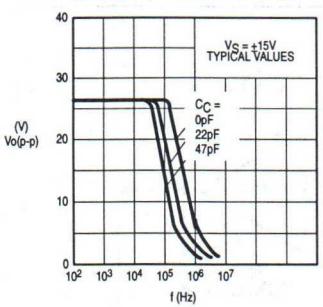
Slew Rate as a Function of Compensation Capacitance



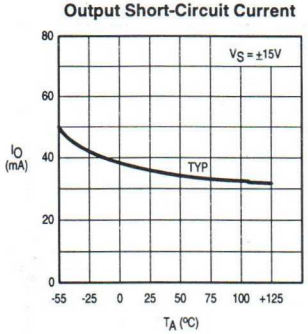
Closed-Loop Frequency Response



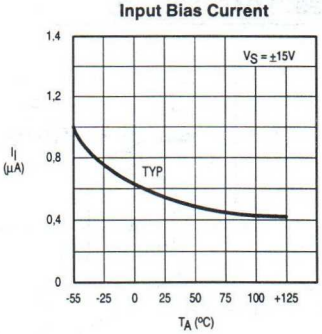
Large-Signal Frequency Response



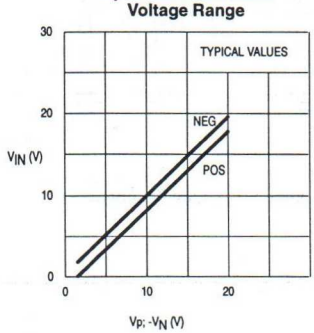
Output Short-Circuit Current



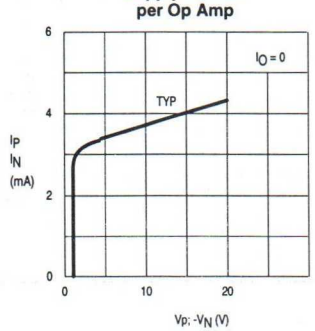
Input Bias Current



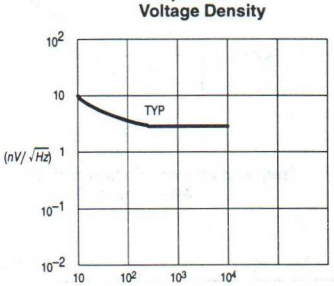
Input Commom-Mode Voltage Range



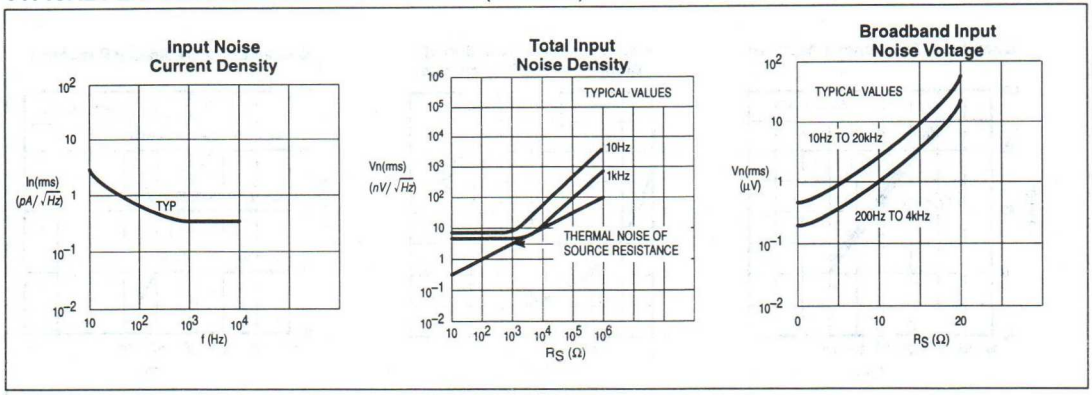
Supply Current per Op Amp



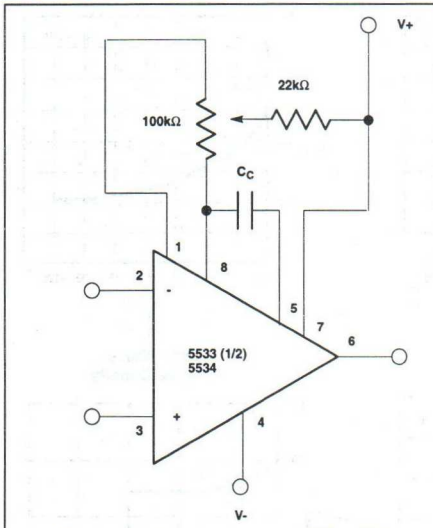
Input Noise Voltage Density



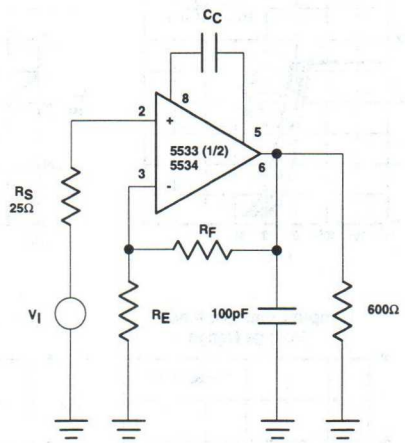
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TEST LOAD CIRCUITS

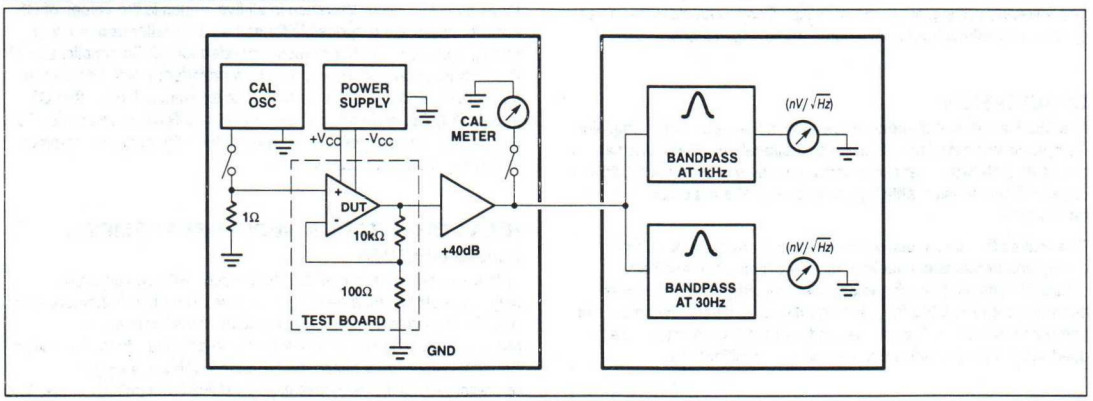


Frequency Compensation and Offset Voltage Adjustment Circuit



Closed-Loop Frequency Response

NOISE TEST BLOCK DIAGRAM



Audio circuits using the NE5532/3/4

AN142

AUDIO CIRCUITS USING THE NE5532/33/34

The following will explain some of Philips Semiconductors low noise op amps and show their use in some audio applications.

DESCRIPTION

The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally-compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used which has guaranteed noise voltage specifications.

APPLICATIONS

The Philips Semiconductors 5532 High-Performance Op Amp is an ideal amplifier for use in high quality and professional audio equipment which requires low noise and low distortion.

The circuit included in this application note has been assembled on a PC board, and tested with actual audio input devices (Tuner and Turntable). It consists of an RIAA (Recording Industry Association of America) preamp, input buffer, 5-band equalizer, and mixer. Although the circuit design is not new, its performance using the 5532 has been improved.

The RIAA preamp section is a standard compensation configuration with low frequency boost provided by the Magnetic cartridge and the RC network in the op amp feedback loop. Cartridge loading is accomplished via R1. 47k was chosen as a typical value, and may differ from cartridge to cartridge.

The Equalizer section consists of an input buffer, 5 active variable band pass/notch (depending on R9's setting) filters, and an output summing amplifier. The input buffer is a standard unity gain design providing impedance matching between the preamplifier and the equalizer section. Because the 5532 is internally-compensated, no external compensation is required. The 5-band active filter section is actually five individual active filters with the same feedback design for all five. The main difference in all five stages is the values of C5 and C6, which are responsible for setting the center frequency of each stage. Linear pots are recommended for R9. To simplify use of this circuit, a component value table is provided, which lists center frequencies and their associated capacitor values. Notice that C5 equals (10) C6, and that the Value of R8 and R10 are related to R9 by a factor of 10 as well. The values listed in the table are common and easily found standard values.

RIAA EQUALIZATION AUDIO PREAMPLIFIER USING NE5532A

With the onset of new recording techniques with sophisticated playback equipment, a new breed of low noise operational amplifiers was developed to complement the state-of-the-art in audio reproduction. The first ultra-low noise op amp introduced by Philips Semiconductors was called the NE5534A. This is a single operational amplifier with less than 4nV/√Hz input noise voltage. The NE5534A is internally-compensated at a gain of three. This device has been used in many audio preamp and equalizer (active filter) applications since its introduction early last year.

Many of the amplifiers that are being designed today are DC-coupled. This means that very low frequencies (2-15Hz) are being amplified. These low frequencies are common to turntables because of rumble and tone arm resonances. Since the amplifiers can reproduce these sub-audible tones, they become quite objectionable because the speakers try to reproduce these tones. This causes non-linearities when the actual recorded material is amplified and converted to sound waves.

The RIAA has proposed a change in its standard playback response curve in order to alleviate some of the problems that were previously discussed. The changes occur primarily at the low frequency range with a slight modification to the high frequency range (See Figure 2). Note that the response peak for the bass section of the playback curve now occurs at 31.5Hz and begins to roll off below that frequency. The roll-off occurs by introducing a fourth RC network with a 7950μs time constant to the three existing networks that make up the equalization circuit. The high end of the equalization curve is extended to 20kHz, because recordings at these frequencies are achievable on many current discs.

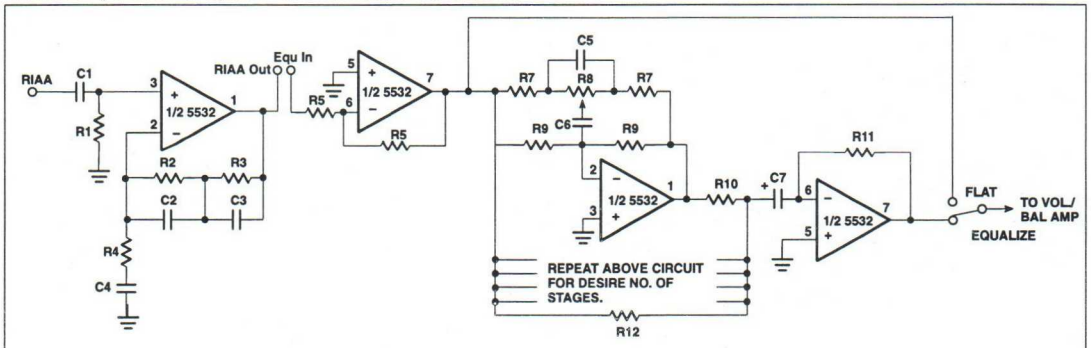


Figure 1. RIAA - Equalizer Schematic

COMPONENT VALUES FOR FIGURE 1

R8=25k R7=2.4k R9=240k			R8=50k R7=5.1k R9=510k			R8=100k R7=10k R9=1meg		
f_O	C5	C6	f_O	C5	C6	f_O	C5	C6
23Hz	1μF	0.1μF	25Hz	0.47μF	0.047μF	12Hz	0.47μF	0.047μF
50Hz	0.47μF	0.047μF	36Hz	0.33μF	0.033μF	18Hz	0.33μF	0.033μF
72Hz	0.33μF	0.033μF	54Hz	0.22μF	0.022μF	27Hz	0.22μF	0.022μF
108Hz	0.22μF	0.022μF	79Hz	0.15μF	0.015μF	39Hz	0.15μF	0.015μF
158Hz	0.15μF	0.015μF	119Hz	0.1μF	0.01μF	59Hz	0.1μF	0.01μF
238Hz	0.1μF	0.01μF	145Hz	0.082μF	0.0082μF	72Hz	0.082μF	0.0082μF
290Hz	0.082μF	0.0082μF	175Hz	0.068μF	0.0068μF	87Hz	0.068μF	0.0068μF
350Hz	0.068μF	0.0068μF	212Hz	0.056μF	0.0056 μF	106Hz	0.056μF	0.0056μF
425Hz	0.056μF	0.0056μF	253Hz	0.047μF	0.0047μF	126Hz	0.047μF	0.0047μF
506Hz	0.047μF	0.0047μF	360Hz	0.033μF	0.0033μF	180Hz	0.033μF	0.0033μF
721Hz	0.033μF	0.0033μF	541Hz	0.022μF	0.0022μF	270Hz	0.022μF	0.0022μF
1082Hz	0.022μF	0.0022μF	794Hz	0.015μF	0.0015μF	397Hz	0.015μF	0.0015μF
1588Hz	0.015μF	0.0015μF	1191Hz	0.01μF	0.001μF	595Hz	0.01μF	0.001μF
2382Hz	0.01μF	0.001μF	1452Hz	0.0082μF	820pF	726Hz	0.0082μF	820pF
2904Hz	0.0082μF	820pF	1751Hz	0.0068μF	680pF	875Hz	0.0068μF	680pF
3502Hz	0.0068μF	680pF	2126Hz	0.0056μF	560pF	1063Hz	0.0056μF	560pF
4253Hz	0.0056μF	560pF	2534Hz	0.0047μF	470pF	1267Hz	0.0047μF	470pF
5068Hz	0.0047μF	470pF	3609Hz	0.0033μF	330pF	1804Hz	0.0033μF	330pF
7218Hz	0.0033μF	330pF	5413Hz	0.0022μF	220pF	2706Hz	0.0022μF	220pF
10827Hz	0.0022μF	220pF	7940Hz	0.0015μF	150pF	3970Hz	0.0015μF	150pF
15880Hz	0.0015μF	150pF	11910Hz	0.001μF	100pF	5955Hz	0.001μF	100pF
23820Hz	0.001μF	100pF	14524Hz	820pF	82pF	7262Hz	820pF	82pF
			17514Hz	680pF	68pF	8757Hz	680pF	68pF
			21267Hz	560pF	56pF	10633Hz	560pF	56pF
						12670Hz	470pF	47pF
						18045Hz	330pF	33pF

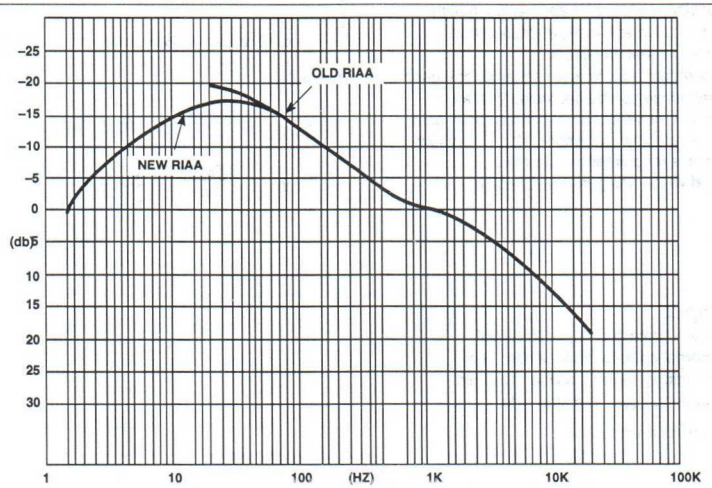


Figure 2. Proposed RIAA Playback Equalization

Audio circuits using the NE5532/3/4

AN142

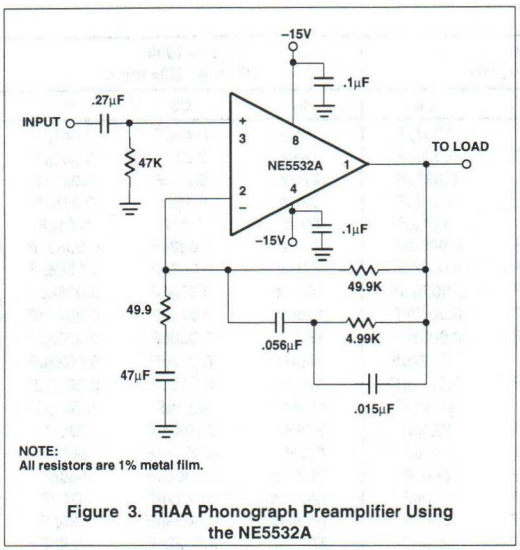


Figure 3. RIAA Phonograph Preamplifier Using the NE5532A

NE5533/34 DESCRIPTION

the 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the devices especially suitable for application in high quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers.
The op amps are internally-compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

APPLICATIONS

Diode Protection of Input

The input leads of the device are protected from differential transients above ±0.6V by internal back-to-back diodes. Their presence imposes certain limitations on the amplifier dynamic characteristics related to closed-loop gain and slew rate.

Consider the unity gain follower as an example:

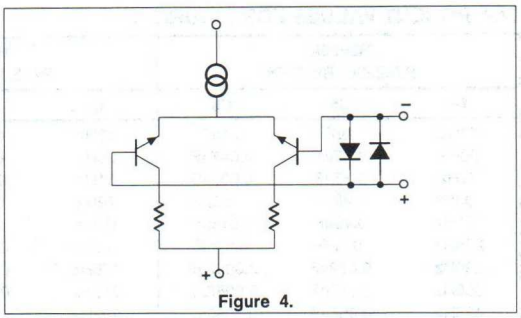


Figure 4.

Assume a signal input square wave with dV/dt of 250V/μs and 2V peak amplitude as shown. If a 22pF compensation capacitor is inserted and the R_1 C_1 circuit deleted, the device slew rate falls to approximately 7V/μs. The input waveform will reach 2V/250V/μs or 8ns, while the output will have changed (8×10^{-3}) only 56mV. The differential input signal is then (V_{IN}-V_O) R_I/R_I+R_F or approximately 1V.

The diode limiter will definitely be active and output distortion will occur; therefore, V_{IN}<1V as indicated.

Next, a sine wave input is used with a similar circuit.

The slew rate of the input waveform now depends on frequency and the exact expression is

$$\frac{dv}{dt} = 2\omega \cos \omega t$$

The upper limit before slew rate distortion occurs for small-signal (V_{IN}<100mV) conditions is found by setting the slew rate to 7V/μs. That is:

$$7 \times 10^6 V/\mu s = 2\omega \cos \omega t$$

at $\omega t = 0$

$$\omega_{LIMIT} = \frac{7\times10^6}{2} = 3.5\times10^6 rad/s$$

$$f_{LIMIT} = \frac{3.5\times10^6}{2\pi} \approx 560kHz$$

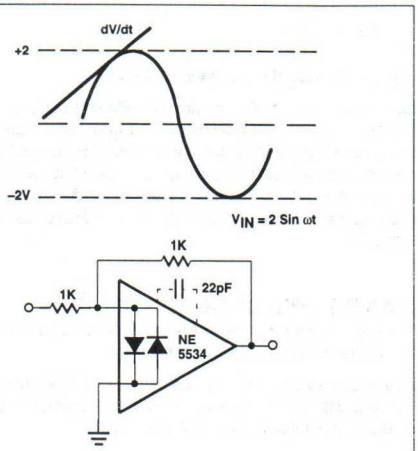


Figure 5.

External Compensation Network Improves Bandwidth

By using an external lead-lag network, the follower circuit slew rate and small-signal bandwidth can be increased. This may be useful in situations where a closed-loop gain less than 3 to 5 is indicated. A number of examples are shown in subsequent figures. The principle benefit of using the network approach is that the full slew rate and bandwidth of the device is retained, while impulse-related parameters such as damping and phase margin are controlled by choosing the appropriate circuit constants. For example, consider the following configuration:

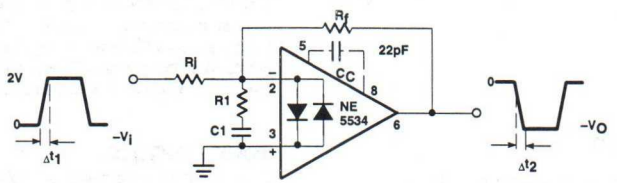


Figure 6.

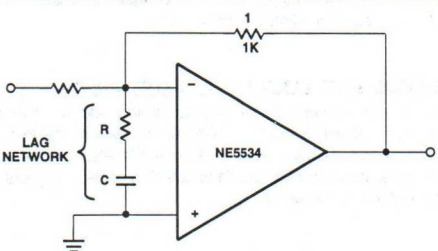


Figure 7.

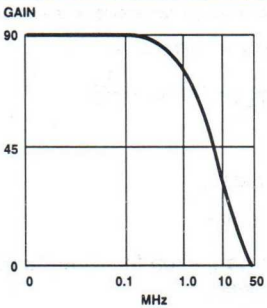


Figure 8.

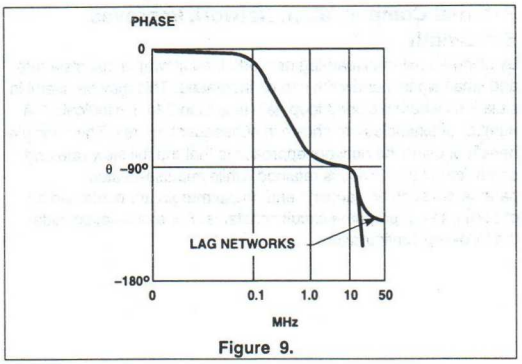


Figure 9.

The major problem to be overcome is poor phase margin leading to instability.

By choosing the lag network break frequency one decade below the unity gain crossover frequency (30-50MHz), the phase and gain margin are improved. An appropriate value for R is 270Ω. Setting the lag network break frequency at 5MHz, C may be calculated

$$C = \frac{1}{2\pi \cdot 270 \cdot 5x10^6}$$

$$= 118pF$$

RULES AND EXAMPLES

Compensation Using Pins 5 and 8 (Limited Bandwidth and Slew Rate)

A single-pole and zero inserted in the transfer function will give an added 45° of phase margin, depending on the network values.

Calculating the Lead-Lag Network

$$C_1 = \frac{1}{2\pi F_1 R_1} \text{ Let } R_1 = \frac{R_{IN}}{10}$$

where

$$F_1 = \frac{1}{10} \text{ (UGBW)}$$

UGBW = 30MHz

External Compensation for Wide-Band Voltage-Follower

Shunt Capacitance Compensation

$$C_F = \frac{1}{2\pi F_F R_F}, \quad F_F \approx 30MHz$$

or

$$C_F \approx \frac{C_{DIST}}{A_{CL}}$$

C_{DIST} ≈ Distributed Capacitance ≈ 2 - 3pF

Many audio circuits involve carefully-tailored frequency responses. Pre-emphasis is used in all recording mediums to reduce noise and produce flat frequency response. The most often used de-emphasis curves for broadcast and home entertainment systems are shown in Figure 13. Operational amplifiers are well suited to these applications because of their high gain and easily-tailored frequency response.

RIAA PREAMP USING THE NE5534

The preamplifier for phono equalization is shown in Figure 14 with the theoretical and actual circuit response.

Low frequency boost is provided by the inductance of the magnetic cartridge with the RC network providing the necessary break points to approximate the theoretical RIAA curve.

RUMBLE FILTER

Following the amplifier stage, rumble and scratch filters are often used to improve overall quality. Such a filter designed with op amps uses the 2-pole Butterworth approach and features switchable break points. With the circuit of Figure 15, any degree of filtering from fairly sharp to none at all is switch-selectable.

TONE CONTROL

Tone control of audio systems involves altering the flat response in order to attain more low frequencies or more high ones, dependent upon listener preference. The circuit of Figure 16 provides 20dB of bass or treble boost or cut as set by the variable resistance. The actual response of the circuit is shown also.

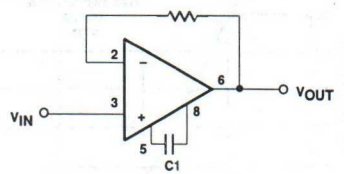
BALANCE AND LOUDNESS AMPLIFIER

Figure 17 shows a combination of balance and loudness controls. Due to the non-linearity of the human hearing system, the low frequencies must be boosted at low listening levels. Balance, level, and loudness controls provide all the listening controls to produce the desired music response.

VOLTAGE AND CURRENT OFFSET ADJUSTMENTS

Many IC amplifiers include the necessary pin connections to provide external offset adjustments. Many times, however, it becomes necessary to select a device not possessing external adjustments. Figures 18, 19, and 20 suggest some possible arrangements for off-circuitry. The circuitry of Figure 20 provides sufficient current into the input to cancel the bias current requirement. Although more

simplified arrangements are possible, the addition of Q2 and Q3 provide a fixed current level to Q1, thus, bias cancellation can be provided without regard to input voltage level.



NOTES

$C_1 = C_C(1)$

C_C = 22pF for NE5533/34

C_C = 22pF [See graph under typical performance characteristics]

Figure 10. Unity Gain Non-Inverting Configuration

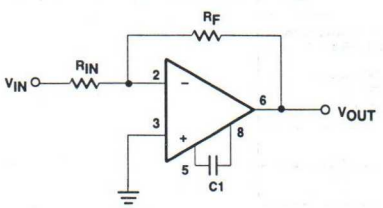
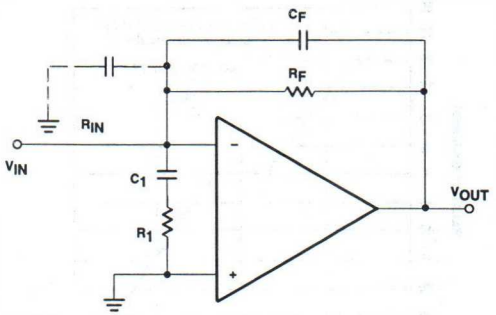


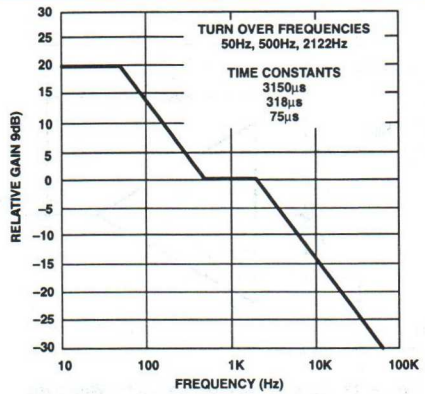
Figure 11. Unity Gain Inverting Configuration



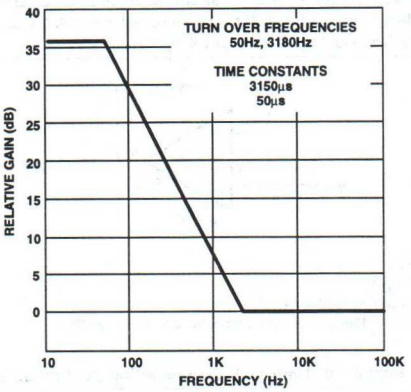
NOTE:

Input diodes limit differential to <0.5V

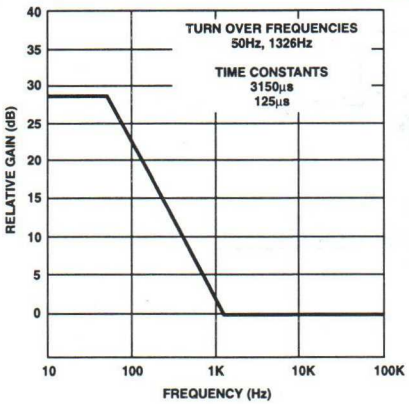
Figure 12. External Compensation for Wideband Voltage Follower



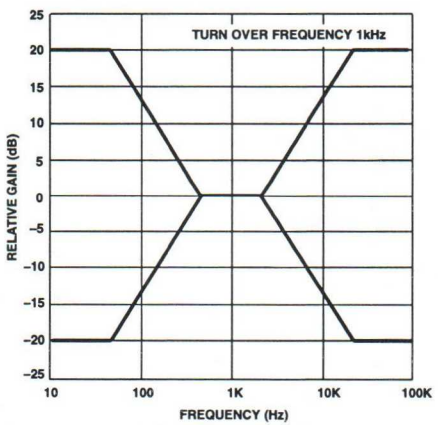
a. RIAA Equalization



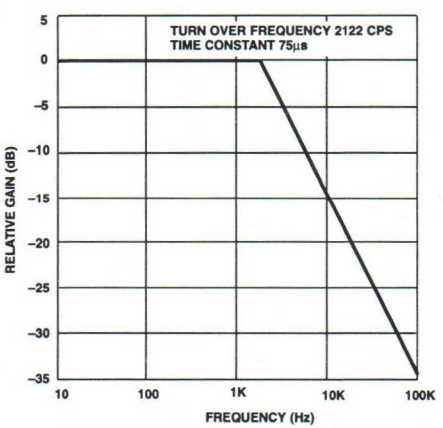
b. NAB Standard Playback 71/2 IPS



c. 3.75 IPS Tape Equalization

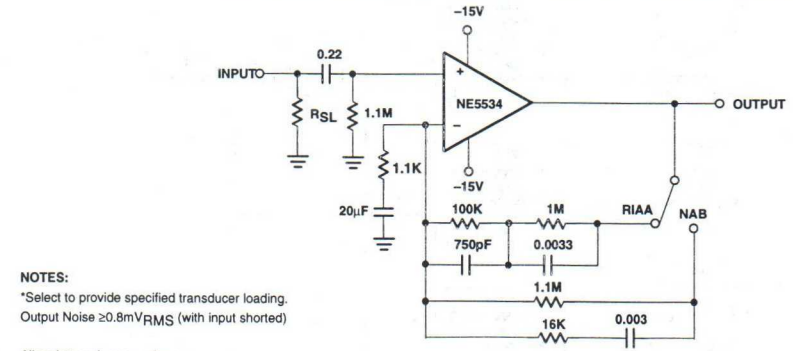


d. Base Treble Curve



e. Standard FM Broadcast Equalization

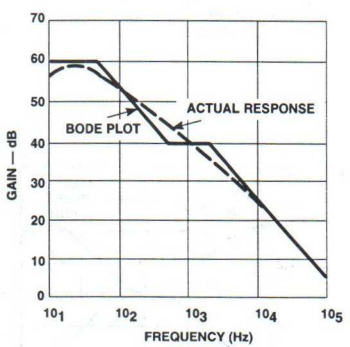
Figure 13.



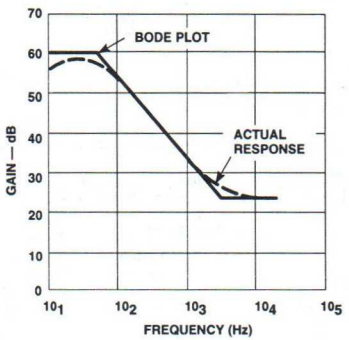
NOTES:
*Select to provide specified transducer loading.
Output Noise ≥0.8mV$_{RMS}$ (with input shorted)

All resistor values are ohms.

a.

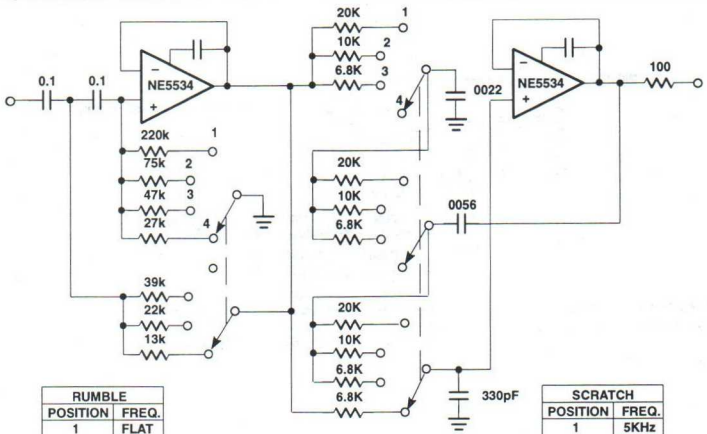


b. Bode Plot of RIAA Equalization and the Response Realized in an Actual Circuit Using the 531.



c. Bode Plot of NAB Equalization and the Response Realized in the Actual Circuit Using the 531.

Figure 14. Preamplifier - RIAA/NAB Compensation

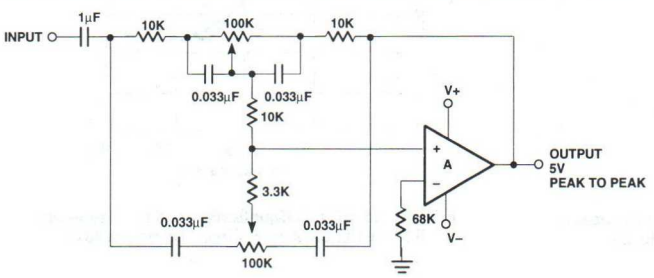


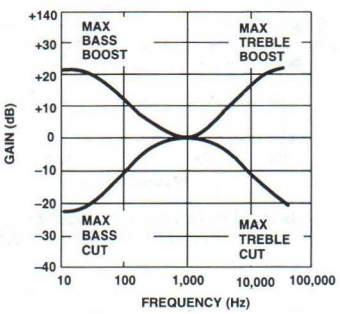
RUMBLE	
POSITION	FREQ.
1	FLAT
2	30MHz
3	50HZ
4	80Hz

SCRATCH	
POSITION	FREQ.
1	5KHz
2	10MHz
3	15HZ
4	FLAT

NOTE:
All resistor values are in ohms.

Figure 15. Rumble/Scratch Filter

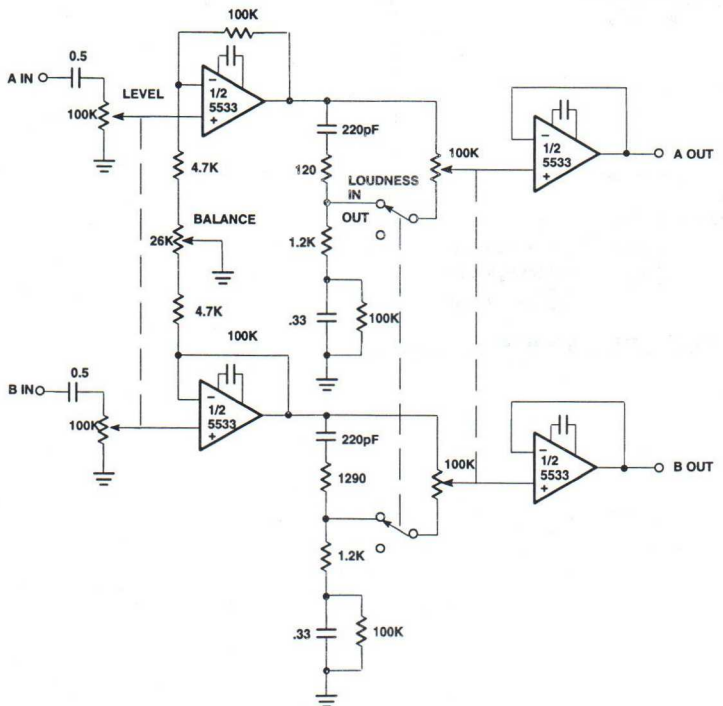




NOTES:
1. Amplifier A may be a NE531 or 301. Frequency compensation, as for unity gain non-inverting amplifiers, must be used.
2. Turn-over frequency - 1kHz.
3. Base boost +20dB, bass cut -20dB, treble boost +19dB at 20Hz, treble cut -19dB at 20Hz.

All resistor values are in ohms.

Figure 16. Tone Control Circuit for Operational Amplifiers



NOTE:
All resistor values are in ohms.

Figure 17. Balance Amplifier with Loudness Control

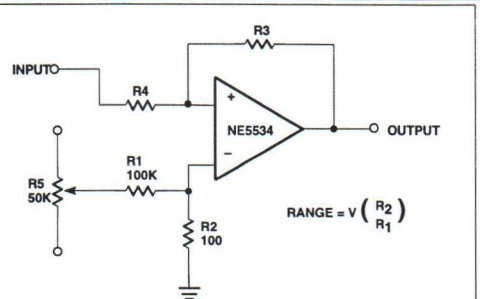
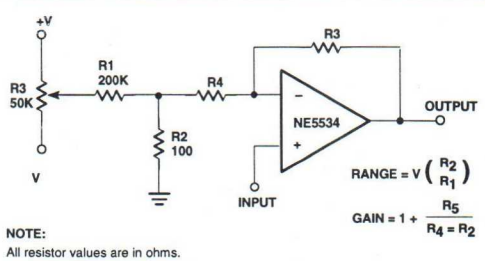


Figure 18. Universal Offset Null for Inverting Amplifiers



NOTE:
All resistor values are in ohms.

Figure 19. Universal Offset Null for Non-Inverting Amplifiers

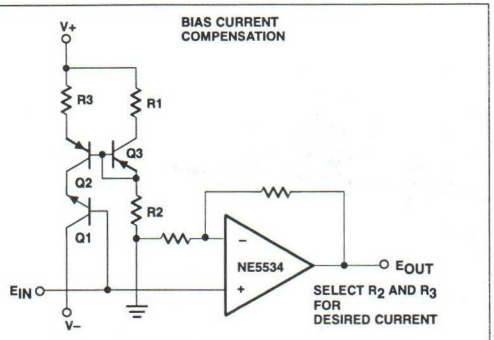


Figure 20. Bias Current Compensation

Low voltage operational amplifier

NE/SA5230

DESCRIPTION

The NE5230 is a very low voltage operational amplifier that can perform with a voltage supply as low as 1.8V or as high as 15V. In addition, split or single supplies can be used, and the output will swing to ground when applying the latter. There is a bias adjusting pin which controls the supply current required by the device and thereby controls its power consumption. If the part is operated at ±0.9V supply voltages, the current required is only 110μA when the current control pin is left open. Even with this low power consumption, the device obtains a typical unity gain bandwidth of 180kHz. When the bias adjusting pin is connected to the negative supply, the unity gain bandwidth is typically 600kHz while the supply current is increased to 600μA. In this mode, the part will supply full power output beyond the audio range.

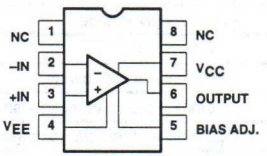
The NE5230 also has a unique input stage that allows the common-mode input range to go above the positive and below the negative supply voltages by 250mV. This provides for the largest possible input voltages for low voltage applications. The part is also internally-compensated to reduce external component count.

The NE5230 has a low input bias current of typically ±40nA, and a large open-loop gain of 125dB. These two specifications are beneficial when using the device in transducer applications. The large open-loop gain gives very accurate signal processing because of the large "excess" loop gain in a closed-loop system.

The output stage is a class AB type that can swing to within 100mV of the supply voltages for the largest dynamic range that is needed in many applications. The NE5230 is ideal for portable audio equipment and remote transducers because of its low power consumption, unity gain bandwidth, and 30nV/$\sqrt{Hz}$ noise specification.

PIN CONFIGURATION

N, D, FE Packages



APPLICATIONS

- Portable precision instruments
- Remote transducer amplifier
- Portable audio equipment
- Rail-to-rail comparators
- Half-wave rectification without diodes
- Remote temperature transducer with 4 to 20mA output transmission

FEATURES

- Works down to 1.8V supply voltages
- Adjustable supply current
- Low noise
- Common-mode includes both rails
- V_{OUT} within 100mV of both rails

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE5230D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5230N	0404B
8-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA5230D	0174C
8-Pin Ceramic Dual In-Line Package (CERDIP)	-40°C to +85°C	SA5230FE	0580A
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA5230N	0404B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Single supply voltage	18	V
V_S	Dual supply voltage	±9	V
V_{IN}	Input voltage[1]	±9 (18)	V
	Differential input voltage[1]	$\pm V_S$	V
V_{CM}	Common-mode voltage (positive)	V_{CC}+0.5	V
V_{CM}	Common-mode voltage (negative)	V_{EE}-0.5	V
P_D	Power dissipation[2]	500	mW
T_J	Operating junction temperature[2]	150	°C
	80Output short-circuit duration to either power supply pin[2, 3]	Indefinite	s
T_{STG}	Storage temperature	-65 to 150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. Can exceed the supply voltages when $V_S \leq \pm 7.5V$ (15V).
2. The maximum operating junction temperature is 150°C. At elevated temperatures, devices must be derated according to the package thermal resistance and device mounting conditions. Derate above 25°C at the following rates:
   FE package at 6.7mW/°C
   N package at 9.5mW/°C
   D package at 6.25mW/°C
3. Momentary shorts to either supply are permitted in accordance to transient thermal impedance limitations determined by the package and device mounting conditions.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING	UNIT
Single supply voltage	1.8 to 15	V
Dual supply voltage	±0.9 to ±7.5	V
Common-mode voltage (positive)	V_{CC}+0.25	V
Common-mode voltage (negative)	V_{EE}-0.25	V
Temperature		
NE grade	0 to 70	°C
SA grade	-40 to 85	°C

DC AND AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $\pm 0.9V \leq V_S \leq +7.5V$ or equivalent single supply, R_L=10kΩ, full input common-mode range, over full operating temperature range.

SYMBOL	PARAMETER		TEST CONDITIONS		BIAS	NE/SA5230			UNIT
						Min	Typ	Max	
V_{OS}	Offset voltage		T_A=25°C		Any		0.4	3	mV
			T_A=25°C		Any		3	4	
V_{OS}	Drift				Any		2	5	µV/°C
I_{OS}	Offset current		T_A=25°C		High		3	50	nA
			T_A=25°C		Low		3	30	
					High			100	
					Low			60	
I_{OS}	Drift				High		0.5	1.4	nA/°C
					Low		0.3	1.4	
I_B	Bias current		T_A=25°C		High		40	150	nA
			T_A=25°C		Low		20	60	
					High			200	
					Low			150	
I_B	Drift				High		2	4	nA/°C
					Low		2	4	
I_S	Supply current		V_S=±0.9V	T_A=25°C	Low		110	160	µA
				T_A=25°C	High		600	750	
					Low			250	
					High			800	
			V_S=±7.5V	T_A=25°C	Low		320	550	µA
				T_A=25°C	High		1.1	1.6	
					Low			600	
					High			1.7	
V_{CM}	Common-mode input range		V_{OS}≤6mV, T_A=25°C		Any	V^- -0.25		V^+ +0.25	V
					Any	V^-		V^+	
CMRR	Common-mode rejection ratio		V_S=±7.5V	R_S=10kΩ, V_{CM}=±7.5V, T_A=25°C	Any	85	95		dB
				R_S=10kΩ, V_{CM}=±7.5V	Any	80			
PSRR	Power supply rejection ratio		T_A=25°C		High	90	105		dB
			T_A=25°C		Low	85	95		
					High	75			
					Low	80			
I_L	Load current	source	V_S=±7.5V		Any	4	10		mA
		sink	V_S=±7.5V		Any	5	15		
		source	V_S=±7.5V		Any	1	5		
		sink	V_S=±7.5V		Any	2	6		
		source	V_S=±0.9V, T_A=25°C		High	4	6		
		sink	V_S=±0.9V, T_A=25°C		High	5	7		
		source	V_S=±7.5V, T_A=25°C		High		16		
		sink	V_S=±7.5V, T_A=25°C		High		32		
A_{VOL}	Large-signal open-loop gain		V_S=±7.5V	R_L=10kΩ, T_A=25°C	High	120	2000		V/mV
				R_L=10kΩ, T_A=25°C	Low	60	750		V/mV
					High	100			
					Low	50			

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS		BIAS	NE/SA5230			UNIT
					Min	Typ	Max	
V_{OUT}	Output voltage swing	V_S=±0.9V	T_A=25°C +SW	Any	750	800		mV
			T_A=25°C -SW	Any	750	800		
			+SW	Any	700			
			-SW	Any	700			
		V_S=±7.5V	T_A=25°C +SW	Any	7.30	7.35		V
			T_A=25°C -SW	Any	-7.32	-7.35		
			+SW	Any	7.25	7.30		
			-SW	Any	-7.30	-7.35		
SR	Slew rate	T_A=25°C		High		0.25		V/µs
		T_A=25°C		Low		0.09		
BW	Inverting unity gain bandwidth	C_L=100pF, T_A=25°C		High		0.6		MHz
		C_L=100pF, T_A=25°C		Low		0.25		
θ_M	Phase margin	C_L=100pF, T_A=25°C		Any		70		Deg.
t_S	Settling time	C_L=100pF, 0.1%		High		2		µs
		C_L=100pF, 0.1%		Low		5		
V_{INN}	Input noise	R_S=0Ω, f=1kHz		High		30		nV/√Hz
		R_S=0Ω, f=1kHz		Low		60		
THD	Total Harmonic Distortion	V_S=±7.5V A_V=1, V_{IN}=500mV, f=1kHz		High		0.003		%
		V_S=±0.9V A_V=1, V_{IN}=500mV, f=1kHz		High		0.002		

THEORY OF OPERATION

Input Stage

Operational amplifiers which are able to function at minimum supply voltages should have input and output stage swings capable of reaching both supply voltages within a few millivolts in order to achieve ease of quiescent biasing and to have maximum input/output signal handling capability. The input stage of the NE5230 has a common-mode voltage range that not only includes the entire supply voltage range, but also allows either supply to be exceeded by 250mV without increasing the input offset voltage by more than 6mV. This is unequalled by any other operational amplifier today.

In order to accomplish the feat of rail-to-rail input common-mode range, two emitter-coupled differential pairs are placed in parallel so that the common-mode voltage of one can reach the positive supply rail and the other can reach the negative supply rail. The simplified schematic of Figure 1 shows how the complementary emitter-coupler transistors are configured to form the basic input stage cell. Common-mode input signal voltages in the range from 0.8V above V_{EE} to V_{CC} are handled completely by the NPN pair, Q3 and Q4, while common-mode input signal voltages in the range of V_{EE} to 0.8V above V_{EE} are processed only by the PNP pair, Q1 and Q2. The intermediate range of input voltages requires that both the NPN and PNP pairs are operating. The collector currents of the input transistors are summed by the current combiner circuit composed of transistors Q8 through Q11 into one output current. Transistor Q8 is connected as a diode to ensure that the outputs of Q2 and Q4 are properly subtracted from those of Q1 and Q3.

The input stage was designed to overcome two important problems for rail-to-rail capability. As the common-mode voltage moves from the range where only the NPN pair was operating to where both of the input pairs were operating, the effective transconductance would change by a factor of two. Frequency compensation for the ranges where one input pair was operating would, of course, not be optimal for the range where both pairs were operating. Secondly, fast changes in the common-mode voltage would abruptly saturate and restore the emitter current sources, causing transient distortion. These problems were overcome by assuring that only the input transistor pair which is able to function properly is active. The NPN pair is normally activated by the current source I_{B1} through Q5 and the current mirror Q6 and Q7, assuming the PNP pair is non-conducting. When the common-mode input voltage passes below the reference voltage, V_{B1}=0.8V at the base of Q5, the emitter current is gradually steered toward the PNP pair, away from the NPN pair. The transfer of the emitter currents between the complementary input pairs occurs in a voltage range of about 120mV around the reference voltage V_{B1}. In this way the sum of the emitter currents for each of the NPN and PNP transistor pairs is kept constant; this ensures that the transconductance of the parallel combination will be constant, since the transconductance of bipolar transistors is proportional to their emitter currents.

An essential requirement of this kind of input stage is to minimize the changes in input offset voltage between that of the NPN and PNP transistor pair which occurs when the input common-mode voltage crosses the internal reference voltage, V_{B1}. Careful circuit layout with a cross-coupled quad for each input pair has yielded a typical input offset voltage of less than 0.3mV and a change in the input offset voltage of less than 0.1mV.

Output Stage

Processing output voltage swings that nominally reach to less than 100mV of either supply voltage can only be achieved by a pair of complementary common-emitter connected transistors. Normally, such a configuration causes complex feed-forward signal paths that develop by combining biasing and driving which can be found in previous low supply voltage designs. The unique output stage of the NE5230 separates the functions of driving and biasing, as shown in the simplified schematic of Figure 2, and has the advantage of a shorter signal path which leads to increasing the effective bandwidth.

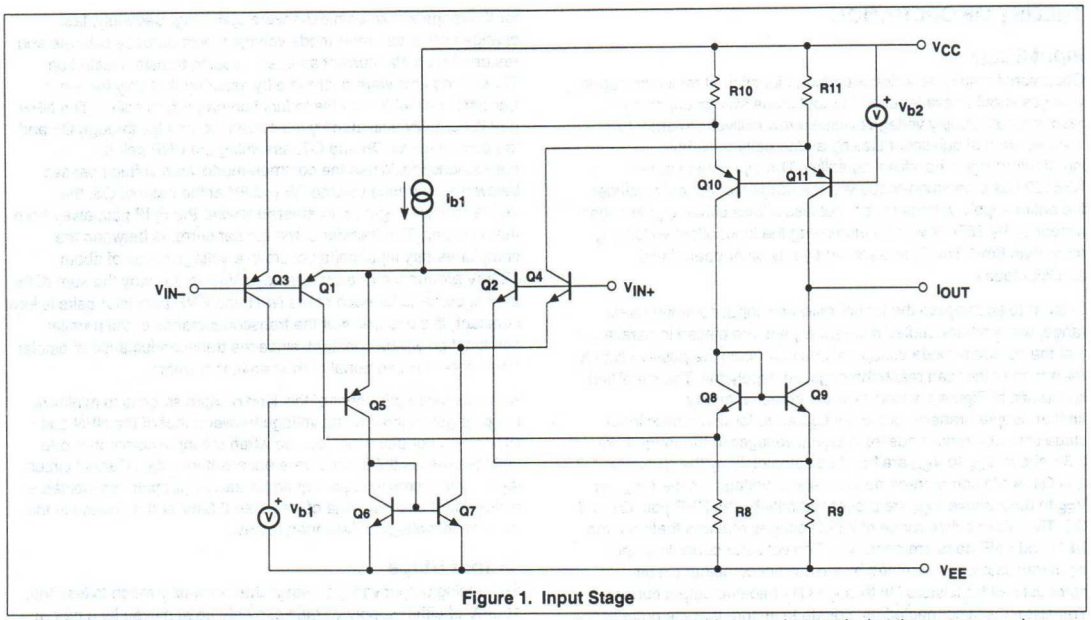


Figure 1. Input Stage

This output stage consists of two parts: the Darlington output transistors and the class AB control regulator. The output transistor Q3 connected with the Darlington transistors Q4 and Q5 can source up to 10mA to an output load. The output of NPN Darlington connected transistors Q1 and Q2 together are able to sink an output current of 10mA. Accurate and efficient class AB control is necessary to insure that none of the output transistors are ever completely cut off. This is accomplished by the differential amplifier (formed by Q8 and Q9) which controls the biasing of the output transistors. The differential amplifier compares the summed voltages across two diodes, D1 and D2, at the base of Q8 with the summed voltages across the base-emitter diodes of the output transistors Q1 and Q3. The base-emitter voltage of Q3 is converted into a current by Q6 and R6 and reconverted into a voltage across the base-emitter diode of Q7 and R7. The summed voltage across the base-emitter diodes of the output transistors Q3 and Q1 is proportional to the logarithm of the product of the push and pull currents I_{OP} and I_{ON}, respectively. The combined voltages across diodes D1 and D2 are proportional to the logarithm of the square of the reference current I_{B1}. When the diode characteristics and temperatures of the pairs Q1, D1 and Q3, Q2 are equal, the relation $I_{OP} \times I_{ON} = I_{B1} \times I_{B1}$ is satisfied.

Separating the functions of biasing and driving prevents the driving signals from becoming delayed by the biasing circuit. The output Darlington transistors are directly accessible for in-phase driving signals on the bases of Q5 and Q2. This is very important for simple high-frequency compensation. The output transistors can be high-frequency compensated by Miller capacitors CM1A and CM1B connected from the collectors to the bases of the output Darlington transistors.

A general-purpose op amp of this type must have enough open-loop gain for applications when the output is driving a low resistance load. The NE5230 accomplishes this by inserting an intermediate common-emitter stage between the input and output stages. The three stages provide a very large gain, but the op amp now has three natural dominant poles — one at the output of each common-emitter stage. Frequency compensation is implemented with a simple scheme of nested, pole-splitting Miller integrators. The Miller capacitors CM1A and CM1B are the first part of the nested structure, and provide compensation for the output and intermediate stages. A second pair of Miller integrators provide pole-splitting compensation for the pole from the input stage and the pole resulting from the compensated combination of poles from the intermediate and output stages. The result is a stable, internally-compensated op amp with a phase margin of 70 degrees.

THERMAL CONSIDERATIONS

When using the NE5230, the internal power dissipation capabilities of each package should be considered. Philips Semiconductors does not recommend operation at die temperatures above 110°C in the SO package because of its inherently smaller package mass. Die temperatures of 150°C can be tolerated in all the other packages. With this in mind, the following equation can be used to estimate the die temperature:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad (1)$$

Where

$T_A \equiv$ AmbientTemperature
$T_J =$ Die Temperature
$P_D \equiv$ Power Dissipation
$= (I_{CC} \times V_{CC})$
$\theta_{JA} \equiv$ Packagethermalresistance
$= 270°C/W$ for SO – 8 in PC board mounting

See the packaging section for information regarding other methods of mounting.

θ_{JA}=100°C/W for the plastic DIP;
θ_{JA}=110°C/W for the ceramic DIP.

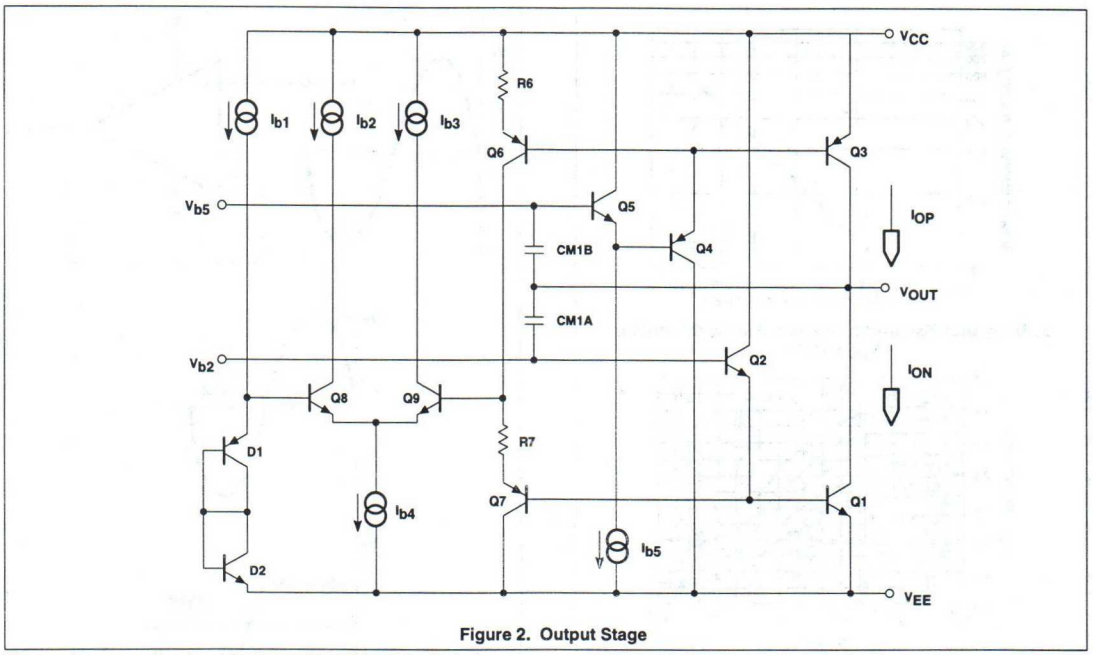


Figure 2. Output Stage

The maximum supply voltage for the part is 15V and the typical supply current is 1.1mA (1.6mA max). For operation at supply voltages other than the maximum, see the data sheet for I_{CC} versus V_{CC} curves. The supply current is somewhat proportional to temperature and varies no more than 100µA between 25°C and either temperature extreme.

Operation at higher junction temperatures than that recommended is possible but will result in lower MTBF (Mean Time Between Failures). This should be considered before operating beyond recommended die temperature because of the overall reliability degradation.

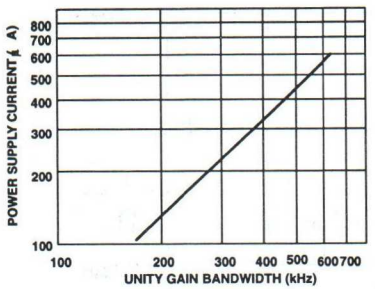
DESIGN TECHNIQUES AND APPLICATIONS

The NE5230 is a very user-friendly amplifier for an engineer to design into any type of system. The supply current adjust pin (Pin 5) can be left open or tied through a pot or fixed resistor to the most negative supply (i.e., ground for single supply or to the negative supply for split supplies). The minimum supply current is achieved by leaving this pin open. In this state it will also decrease the bandwidth and slew rate. When tied directly to the most negative supply, the device has full bandwidth, slew rate and I_{CC}. The programming of the current-control pin depends on the trade-offs which can be made in the designer's application. The graph in Figure 3 will help by showing bandwidth versus I_{CC}. As can be seen, the supply current can be varied anywhere over the range of 100µA to 600µA for a supply voltage of 1.8V. An external resistor can be inserted between the current control pin and the most negative supply. The resistor can be selected between 1Ω to 100kΩ to provide any required supply current over the indicated range. In addition, a small varying voltage on the bias current control pin could be used for such exotic things as changing the gain-bandwidth for voltage controlled low pass filters or amplitude modulation. Furthermore, control over the slew rate and the rise time of the amplifier can be obtained in the same manner. This control over the slew rate also changes the settling time and overshoot in pulse response applications. The settling time to 0.1% changes from 5µs at low bias to 2µs at high bias. The supply current control can also be utilized for wave-shaping applications such as for pulse or triangular waveforms. The gain-bandwidth can be varied from between 250kHz at low bias to 600kHz at high bias current. The slew rate range is 0.08V/µs at low bias and 0.25V/µs at high bias.

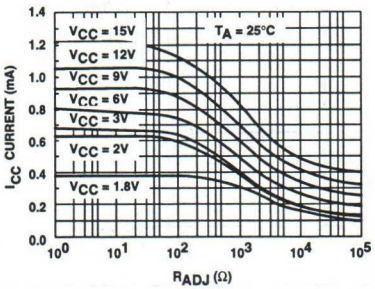
The full output power bandwidth range for V_{CC} equals 2V, is above 40kHz for the maximum bias current setting and greater than 10kHz at the minimum bias current setting.

If extremely low signal distortion (<0.05%) is required at low supply voltages, exclude the common-mode crossover point (V_{B1}) from the common-mode signal range. This can be accomplished by proper bias selection or by using an inverting amplifier configuration.

Most single supply designs necessitate that the inputs to the op amp be biased between V_{CC} and ground. This is to assure that the input signal swing is within the working common-mode range of the amplifier. This leads to another helpful and unique property of the NE5230 that other CMOS and bipolar low voltage parts cannot achieve. It is the simple fact that the input common-mode voltage can go beyond either the positive or negative supply voltages. This benefit is made very clear in a non-inverting voltage-follower configuration. This is shown in Figure 4 where the input sine wave allows



a. Unity Gain Bandwidth vs Power Supply Current for $V_{CC} = \pm 0.9V$



b. I_{CC} Current vs Bias Current Adjusting Resistor for Several Supply Voltages

Figure 3.

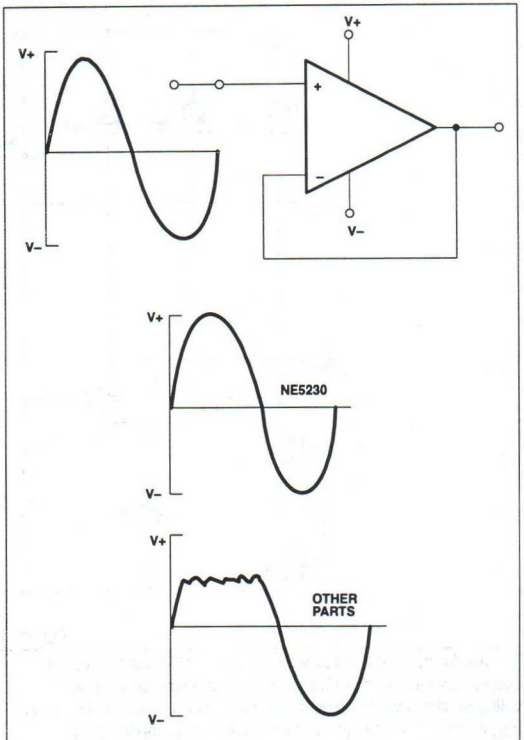


Figure 4. In a Non-Inverting Voltage-Follower Configuration, the NE5230 will Give Full Rail-to-Rail Swing. Other Low Voltage Amplifiers will not Because they are Limited by their Input Common-Mode Range and Output Swing Capability.

an undistorted output sine wave which will swing less than 100mV of either supply voltage. Many competitive parts will show severe clipping caused by input common-mode limitations. The NE5230 in this configuration offers more freedom for quiescent biasing of the inputs close to the positive supply rail where similar op amps would not allow signal processing.

There are not as many considerations when designing with the NE5230 as with other devices. Since the NE5230 is internally-compensated and has a unity gain-bandwidth of 600kHz, board layout is not so stringent as for very high frequency devices such as the NE5205. The output capability of the NE5230 allows it to drive relatively high capacitive loads and small resistive loads. The power supply pins should be decoupled with a low-pass RC network as close to the supply pins as possible to eliminate 60Hz and other external power line noise, although the power supply rejection ratio (PSRR) for the part is very high. The pinout for the NE5230 is the same as the standard single op amp pinout with the exception of the bias current adjusting pin.

REMOTE TRANSDUCER WITH CURRENT TRANSMISSION

There are many ways to transmit information along two wires, but current transmission is the most beneficial when the sensing of remote signals is the aim. It is further enhanced in the form of 4 to 20mA information which is used in many control-type systems. This method of transmission provides immunity from line voltage drops, large load resistance variations, and voltage noise pickup. The zero reference of 4mA not only can show if there is a break in the line when no current is flowing, but also can power the transducer at the

remote location. Usually the transducer itself is not equipped to provide for the current transmission. The unique features of the NE5230 can provide high output current capability coupled with low power consumption. It can be remotely connected to the transducer to create a current loop with minimal external components. The circuit for this is shown in Figure 5. Here, the part is configured as a voltage-to-current, or transconductance amplifier. This is a novel circuit that takes advantage of the NE5230's large open-loop gain. In AC applications, the load current will decrease as the open-loop gain rolls off in magnitude. The low offset voltage and current sinking capabilities of the NE5230 must also be considered in this application.

The NE5230 circuit shown in Figure 5 is a pseudo transistor configuration. The inverting input is equivalent to the "base," the point where V_{EE} and the non-inverting input meet is the "emitter," and the connection after the output diode meets the V_{CC} pin is the collector. The output diode is essential to keep the output from saturating in this configuration. From here it can be seen that the base and emitter form a voltage-follower and the voltage present at R_C must equal the input voltage present at the inverting input. Also, the emitter and collector form a current-follower and the current flowing through R_C is equivalent to the current through R_L and the amplifier. This sets up the current loop. Therefore, the following equation can be formulated for the working current transmission line. The load current is:

$$I_L = V_{IN}/R_C \quad (2)$$

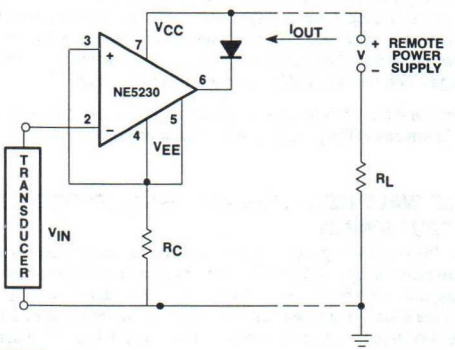
and proportional to the input voltage for a set R_C. Also, the current is constant no matter what load resistance is used while within the operating bandwidth range of the op amp. When the NE5230's supply voltage falls past a certain point, the current cannot remain constant. This is the "voltage compliance" and is very good for this application because of the near rail output voltage. The equation that determines the voltage compliance as well as the largest possible load resistor for the NE5230 is as follows:

$$R_{L\,max} = [V_{remote\ supply}) - V_{CC\,min} - V_{IN\,max}]/I_L \quad (3)$$

Where $V_{CC\,min}$ is the worst-case power supply voltage (approximately 1.8V) that will still keep the part operational. As an example, when using a 15V remote power supply, a current sensing resistor of 1Ω, and an input voltage (V_{IN}) of 20mV, the output current (I_L) is 20mA. Furthermore, a load resistance of zero to approximately 650Ω can be inserted in the loop without any change in current when the bias current-control pin is tied to the negative supply pin. The voltage drop across the load and line resistance will not affect the NE5230 because it will operate down to 1.8V. With a 15V remote supply, the voltage available at the amplifier is still enough to power it with the maximum 20mA output into the 650Ω load.

What this means is that several instruments, such as a chart recorder, a meter, or a controller, as well as a long cable, can be connected in series on the loop and still obtain accurate readings if the total resistance does not exceed 650Ω. Furthermore, any variation of resistance in this range will not change the output current.

Any voltage output type transducer can be used, but one that does not need external DC voltage or current excitation to limit the maximum possible load resistance is preferable. Even this problem can be surmounted if the supply power needed by the transducer is compatible with the NE5230. The power goes up the line to the transducer and amplifier while the transducer signal is sent back via the current output of the NE5230 transconductance configuration.



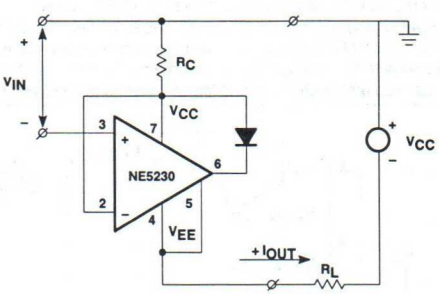
NOTES:

1. $I_{OUT} = V_{IN}/R_C$
2. $R_{L\,MAX} = \dfrac{V_{REMOTE} - 1.8V - V_{INMAX}}{I_{OUT}}$

For $R_C = 1\Omega$

I_{OUT}	V_{IN}
4mA	4mV
20mA	20mV

a. The NE5230 as a Remote Transducer Transconductance Amp With 4-20mA Current Transmission Output Capability



b. The Same Type of Circuit as Figure 5a, but for Sourcing Current to the Load

Figure 5.

The voltage range on the input can be changed for transducers that produce a large output by simply increasing the current sense resistor to get the corresponding 4 to 20mA output current. If a very long line is used which causes high line resistance, a current repeater could be inserted into the line. The same configuration of Figure 5 can be used with exception of a resistor across the input and line ground to convert the current back to voltage. Again, the current sensing resistor will set up the transconductance and the part will receive power from the line.

TEMPERATURE TRANSDUCER

A variation on the previous circuit makes use of the supply current control pin. The voltage present at this pin is proportional to absolute temperature (PTAT) because it is produced by the amplifier bias current through an internal resistor divider in a PTAT cell. If the control pin is connected to the input pin, the NE5230 itself can be used as a temperature transducer. If the center tap of a resistive pot

is connected to the control pin with one side to ground and the other to the inverting input, the voltage can be changed to give different temperature versus output current conditions (see Figure 6). For additional control, the output current is still proportional to the input voltage differential divided by the current sense resistor.

When using the NE5230 as a temperature transducer, the thermal considerations in the previous section must be kept in mind.

HALF-WAVE RECTIFIER WITH RAIL-TO-GROUND OUTPUT SWING

Since the NE5230 input common-mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction becomes a simple task. All that is needed are two external resistors; there is no need for diodes or matched resistors. Moreover, it can have either positive- or negative-going outputs, depending on the way the bias is arranged. This can be seen in Figure 7. Circuit (a) is biased to ground, while circuit (b) is biased to the positive supply. This rather unusual biasing does not cause any problems with the NE5230 because of the unique internal saturation detectors incorporated into the part to keep the PNP and NPN output transistors out of "hard" saturation. It is therefore relatively quick to recover from a saturated output condition. Furthermore, the device does not have parasitic current draw when the output is biased to either rail. This makes it possible to bias the NE5230 into "saturation" and obtain half-wave rectification with good recovery. The simplicity of biasing and the rail-to-ground half-sine wave swing are unique to this device. The circuit gain can be changed by the standard op amp gain equations for an inverting configuration.

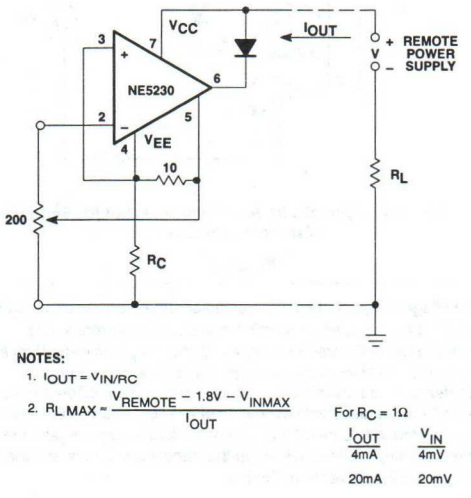


Figure 6. NE5230 Remote Temperature Transducer Utilizing 4-20mA Current Transmission. This Application Shows the use of the Accessibility of the PTAT Cell in the Device to Make the Part, Itself, a Transducer

It can be seen in these configurations that the op amp cannot respond to one-half of the incoming waveform. It cannot respond because the waveform forces the amplifier to swing the output beyond either ground or the positive supply rail, depending on the biasing, and, also, the output cannot disengage during this half cycle. During the other half cycle, however, the amplifier achieves a half-wave that can have a peak equal to the total supply voltage. The photographs in Figure 8 show the effect of the different biasing schemes, as well as the wide bandwidth (it works over the full audio range), that the NE5230 can achieve in this configuration.

By adding another NE5230 in an inverting summer configuration at the output of the half-wave rectifier, a full-wave can be realized. The values for the input and feedback resistors must be chosen so that each peak will have equal amplitudes. A table for calculating values is included in Figure 9. The summing network combines the input signal at the half-wave and adds it to double the half-wave's output, resulting in the full-wave. The output waveform can be referenced to the supply or ground, depending on the half-wave configuration. Again, no diodes are needed to achieve the rectification.

This circuit could be used in conjunction with the remote transducer to convert a received AC output signal into a DC level at the full-wave output for meters or chart recorders that need DC levels.

CONCLUSION

The NE5230 is a versatile op amp in its own right. The part was designed to give low voltage and low power operation without the limitations of previously available amplifiers that had a multitude of problems. The previous application examples are unique to this amplifier and save the user money by excluding various passive components that would have been needed if not for the NE5230's special input and output stages.

The NE5230 has a combination of novel specifications which allows the designer to implement it easily into existing low-supply voltage designs and to enhance their performance. It also offers the engineer the freedom to achieve greater amplifier system design goals. The low input referenced noise voltage eases the restrictions on designs where S/N ratios are important. The wide full-power bandwidth and output load handling capability allow it to fit into portable audio applications. The truly ample open-loop gain and low power consumption easily lend themselves to the requirements of remote transducer applications. The low, untrimmed typical offset voltage and low offset currents help to reduce errors in signal processing designs. The amplifier is well isolated from changes on the supply lines by its typical power supply rejection ratio of 105dB.

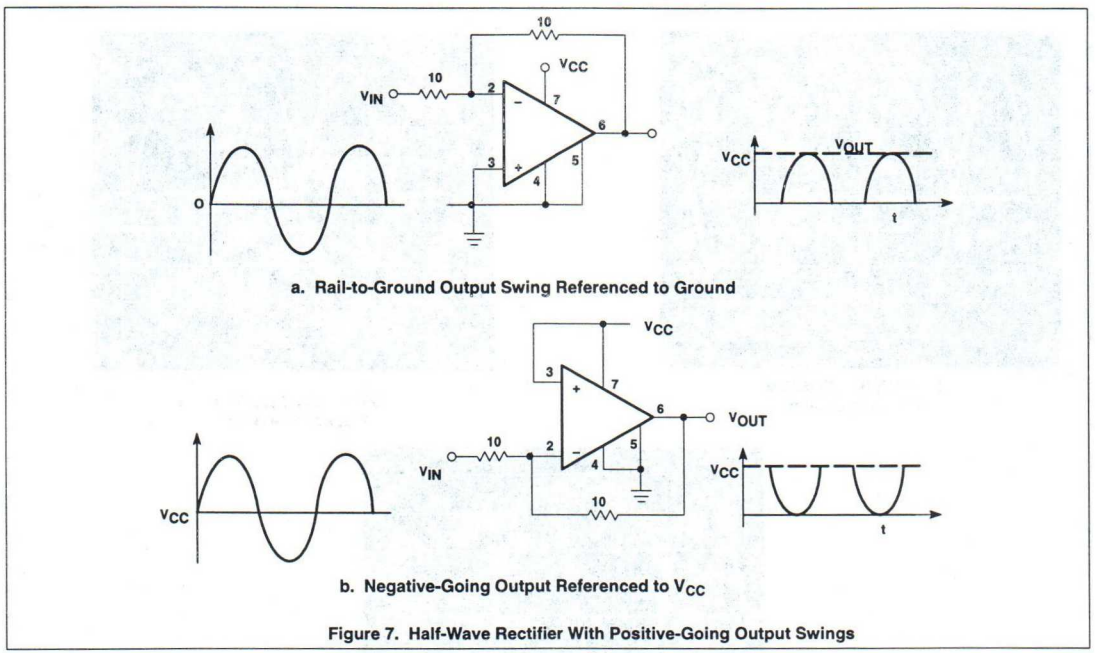
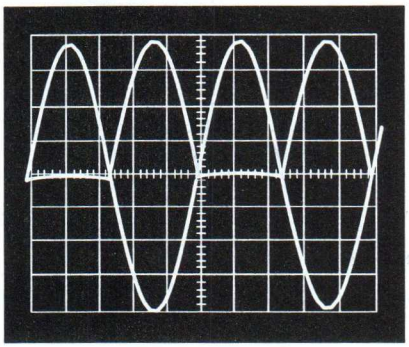
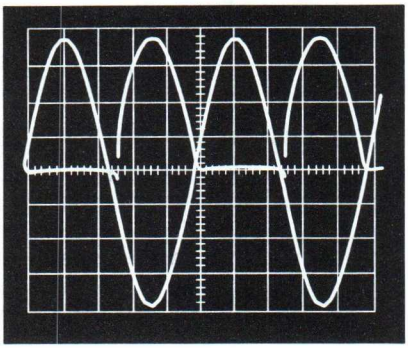


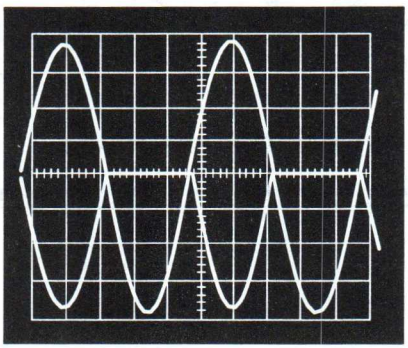
Figure 7. Half-Wave Rectifier With Positive-Going Output Swings



500mV/Div 200μS/Div
Biased to Ground



500mV/Div 20μS/Div
Biased to Ground



500mV/Div 20μS/Div
Biased to Positive Rail

Figure 8. Performance Waveforms for the Circuits in Figure 7. Good Response is Shown at 1 and 10kHz for Both Circuits Under Full Swing With a 2V Supply

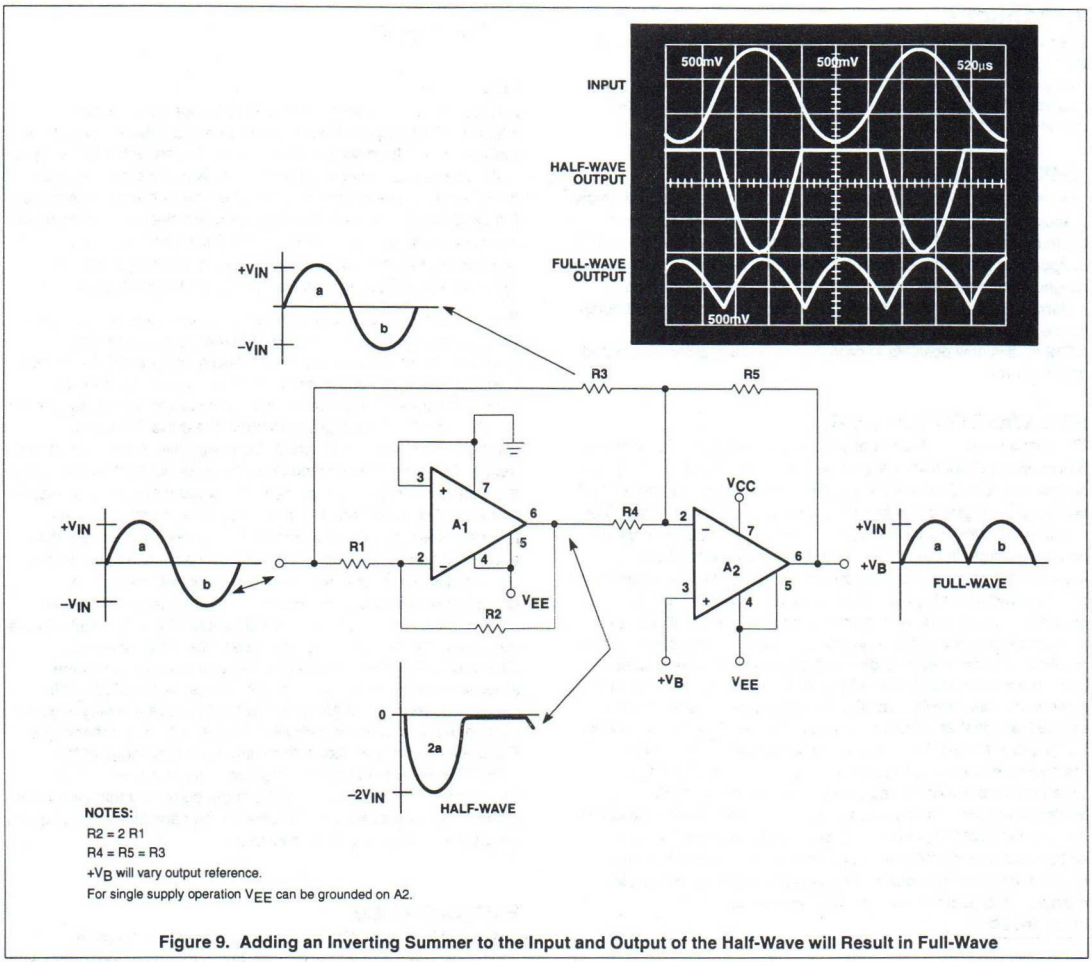


Figure 9. Adding an Inverting Summer to the Input and Output of the Half-Wave will Result in Full-Wave

REFERENCES

Johan H. Huijsing, "Multi-stage Amplifier with Capacitive Nesting for Frequency Compensation," U.S. Patent Application Serial No. 602.234, filed April 19, 1984.

Bob Blauschild, "Differential Amplifier with Rail-to-Rail Capability," U.S. Patent Application Serial No. 525.181, filed August 23, 1983.

Operational Amplifiers - Characteristics and Applications, Robert G. Irvine, Prentice-Hall, Inc., Englewood Cliffs, NJ 07632, 1981.

Transducer Interface Handbook - A Guide to Analog Signal Conditioning, Edited by Daniel H. Sheingold, Analog Devices, Inc., Norwood, MA 02062, 1981.

Low-voltage gated function generator: NE5230

AN1511

INTRODUCTION

Described herein is a low-voltage, gated function generator using the NE5230 and two AA batteries. The outputs are a square, triangular and sine wave. The sine wave-generating circuit and the square and triangular circuits are independent. Some ideas for refinement of the circuits are also presented.

APPLICATIONS

The use of signal sources is universal. Over the years, a great many practical circuits have been developed which have numerous desirable features. These circuits are typified by high power outputs, or speed, or precision, or combinations of these. They are housed in rugged, handsome cases and are available for a few hundred dollars. Most require AC line cords and are somewhat cumbersome to use. With the advent of low-voltage op amps such as the NE5230, it is now possible to design good, stable, battery-operated signal sources.

SINE WAVE GENERATOR

The circuit used is a Wien bridge sine wave oscillator. This circuit has been used since the days of vacuum tubes (see Figure 1). It is simple, stable and requires few components. The circuit utilizes both positive and negative feedback to achieve balanced operation. The oscillator will stop working if too much negative feedback is used and will saturate in both states if too much positive feedback is used. In the practical implementation, some non-linear element must be employed to realize this stable condition. The gain of the amplifier must be large enough at the frequency of oscillation to make the input excursions small enough to be compensable by this non-linear element. Among others, diodes and FETs have been used to accomplish this. One of the most popular is the lamp; small, inexpensive and readily available, its voltage variable resistance makes it an ideal candidate for this application. It works like this: as the negative feedback voltage increases across the lamp, its resistance increases, and thereby reduces the output voltage. When the output voltage decreases, the amount of negative feedback voltage across the lamp decreases and thereby increases the resistance of the lamp. This balancing act continues until a stable condition is achieved. It is important to note that the lamp resistance is changing due to the thermal effects caused by the changing voltage across it. The frequency of oscillation is determined by:

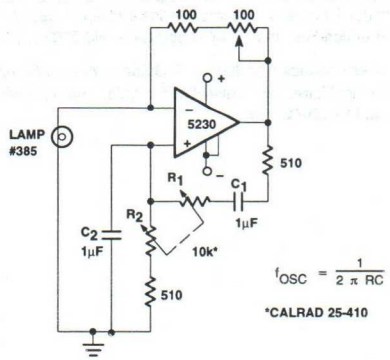


Figure 1. Sine Wave Generator

$$f_{osc} = \frac{1}{2\pi RC}$$

VCO

Another classic oscillator circuit uses a comparator and an integrator. The output of the comparator is fed back to the input of the integrator. The output of the integrator is connected to the input of the comparator. Upon application of power, the comparator output goes into one state or the other. This comparator output voltage is fed back into the input of the integrator which begins ramping up or down, depending on the polarity of the first pulse from the comparator. When the voltage threshold of the comparator is reached, the output changes state. The cycle then repeats.

If an inversion in the feedback loop can be achieved, and external energy can be introduced at the right time, some interesting modifications of the previously described circuit will result—namely, a voltage-controlled oscillator. It works as follows: the transistor inverts the output of the comparator. This voltage is presented to the inverting input of the integrator to begin the cycle. When the comparator threshold is reached, the comparator changes state as before. This time, however, because the external applied voltage to the same inverting input is present, the amount of current available to the input is controlled by the external voltage and not by the feedback voltage. Once the component values are selected, the applied voltage, V_C, sets the frequency of oscillation because the current available to the integrating capacitor determines the charging time constant and, therefore, the frequency. The more positive the V_C, the more current that is available and the higher the frequency of oscillation. The converse is also true with minor differences. It is interesting to note here that other low-voltage amplifiers are not able to perform as well as the NE5230 in this circuit. One reason is that the NE5230 input voltage swing is able to exceed the rails by 250mV and still operate within its linear region. For a given set of conditions, then, the frequency range of the NE5230 is wider than conventional low-voltage op amps. The frequency of this circuit can also be changed by changing the value of the integrating capacitor. The smaller the capacitor, the higher the frequency for a given set of conditions.

PERFORMANCE

The circuit in Figure 2 is the complete low-voltage function generator. The measurements were taken at room temperature with only two AA batteries supplying the power. The outputs were loaded with 200Ω for the sine and triangular wave outputs and 50Ω for the square wave output. The output voltage for the sine wave was ±1V. The square wave output swung from rail to rail while the output voltage of the triangular wave varied with the input voltage, V_C. This was due, of course, to the collector-emitter voltage requirements of the transistor.

Low-voltage gated function generator: NE5230

AN1511

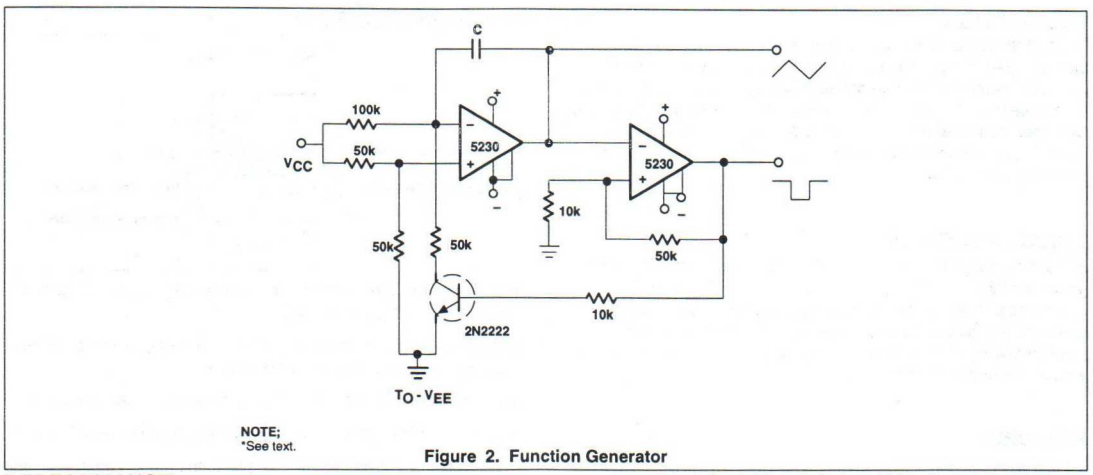


Figure 2. Function Generator

PERFORMANCE

The circuit in Figure 2 is the complete low-voltage function generator. The measurements were taken at room temperature with only two AA batteries supplying the power. The outputs were loaded with 200Ω for the sine and triangular wave outputs and 50Ω for the square wave output. The output voltage for the sine wave was ±1V. The square wave output swung from rail to rail while the output voltage of the triangular wave varied with the input voltage, V_C. This was due, of course, to the collector-emitter voltage requirements of the transistor.

The distortion of the Wien bridge was 0.015% at the lowest frequency and 0.09% at the highest. Using the different capacitor values, the frequency was varied from minimum to maximum using the ganged 10kΩ pot. The frequencies could be changed from 20Hz to 2.5kHz. It was necessary to include a 500Ω resistor in each leg of the bridge to prevent the complete saturation of the amplifier when the potentiometer was in one extreme of its travel. In addition, a small adjustment resistor was used in the negative feedback loop to adjust the gain and to compensate for the slow thermal time constant of the lamp.

The maximum frequency obtained by the VCO was 9.7kHz with V_C=1.65V with ±1.4V batteries. The frequency varied from 8.4kHz to 1.6kHz with ±1 (V_C) applied with a 0.001μF integrating capacitor.

CONCLUSIONS

Some things could have been done differently to improve the operation of these circuits. The thermal time constant of the non-linear elements was an inhibiting factor in the low-frequency operation of the Wien bridge. A diode or FET will work better here. Extreme ambient temperature will change the operating point of the lamp and, therefore, the output amplitude. Some non-symmetrical output was seen when operating the VCO at the lower frequencies. This is due to the influence of the transistor, as described previously.

Finally, the NE5230 has yet another feature: the bias adjust pin. This pin is intended to be used to control the power supply current. The power supply current is controlled by decreasing the internal bias current of the op amp. When the bias current is decreased, the transconductance, g_M, of the input stage is reduced; this, in turn, lowers the -3dB bandwidth. In addition, this pin can be used to turn the op amp on or off. If the voltage at the bias adjust pin is moved to 50mV above the voltage at the V_{EE} pin, the output becomes severely attenuated. The op amp, for all intents and purpose, is off. If, on the other hand, the bias adjust pin is moved to 50mV below the voltage at the V_{EE} pin, the band width and the slew rate are increased. The user should exercise care when doing this.

The NE5230 is a versatile, low-voltage op amp. It has been demonstrated that the device can be used in a variety of different ways. Its ability to swing within 100mV of the output, its input voltage which can exceed the power supply voltage, and its programmable power supply current, make it a leader of low-voltage op amps.

REFERENCES:

Modern Electronic Circuit Reference Manual, John Markus

Raytheon 1984 Data Manual

Low power dual operational amplifiers

NE/SA/SE532/ LM158/258/358/A/2904

DESCRIPTION

The 532/358/LM2904 consists of two independent, high gain, internally frequency-compensated operational amplifiers internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible, and the low power supply current drain is independent of the magnitude of the power supply voltage.

UNIQUE FEATURES

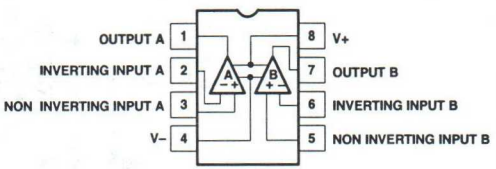
In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature-compensated. The input bias current is also temperature-compensated.

FEATURES

- Internally frequency-compensated for unity gain
- Large DC voltage gain—100dB
- Wide bandwidth (unity gain)—1MHz (temperature-compensated)

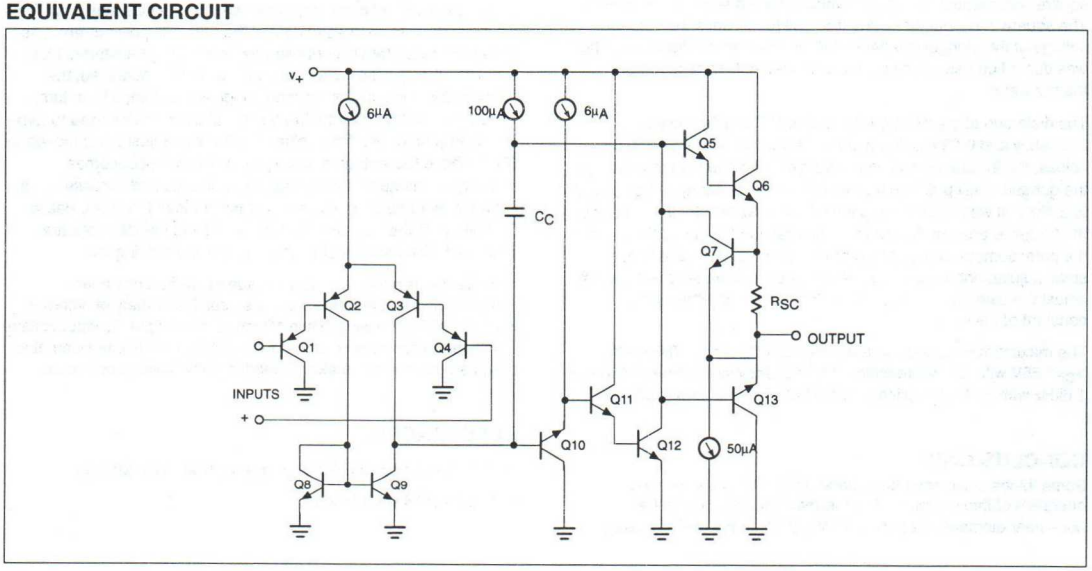
PIN CONFIGURATIONS

D, FE, N Packages



- Wide power supply range single supply—$3V_{DC}$ to $30V_{DC}$ or dual supplies—$\pm1.5V_{DC}$ to $\pm15V_{DC}$
- Very low supply current drain (400μA)—essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)
- Low input biasing current—$45nA_{DC}$ temperature-compensated
- Low input offset voltage—$2mV_{DC}$ and offset current—$5nA_{DC}$
- Differential input voltage range equal to the power supply voltage
- Large output voltage—$0V_{DC}$ to V+ $1.5V_{DC}$ swing

EQUIVALENT CIRCUIT



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE532D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE532N	0404B
8-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA532D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA532N	0404B
8-Pin Ceramic Dual In-Line Package (CERDIP)	-40°C to +85°C	SA532FE	0580A
8-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	LM2904D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	LM2904N	0404B
8-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	LM158FE	0580A
8-Pin Plastic Dual In-Line Package (DIP)	-25°C to +125°C	LM258N	0404B
8-Pin Plastic Small Outline (SO) Package	-25°C to +125°C	LM258D	0174C
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	LM358D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	LM358N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	LM358AN	0404B
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	LM358AD	0174C
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE532N	0404B
8-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE532FE	0580A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage, V+	32 or ±16	V_{DC}
	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	-0.3 to +32	V_{DC}
P_D	Maximum power dissipation T_A=25°C (Still air)[1] FE package N package D package	 780 1160 780	 mW mW mW
	Output short-circuit to GND[5] V+<15 V_{DC} and T_A=25°C	 Continuous	
T_A	Operating ambient temperature range NE532/LM358/LM358A LM258 SA532/LM2904 SE532/LM158	 0 to +70 -25 to +85 -40 to +85 -55 to +125	 °C °C °C °C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. Derate above 25°C, at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V+=+5V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE532, LM158/258			NE/SA532/ LM358/LM2904			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω R_S=0Ω, over temp.		±2	±5 ±7		±2	±7 ±9	mV mV
V_{OS}	Drift	R_S=0Ω, over temp.		7			7		µV/°C
I_{OS}	Offset current	I_{IN} (+)-I_{IN} (-) Over temp.		±3	±30 ±100		±5	±50 ±150	nA nA
I_{OS}	Drift	Over temp.		10			10		pA/°C
I_{BIAS}	Input current[2]	I_{IN} (+) or I_{IN} (-) Over temp., I_{IN} (+) or I_{IN} (-)		45 40	150 300		45 40	250 500	nA nA
I_B	Drift	Over temp.		50			50		pA/°C
V_{CM}	Common-mode voltage range[3]	V+=30V Over temp., V+=30V	0 0		V+-1.5 V+-2.0	0 0		V+-1.5 V+-2.0	V V
CMRR	Common-mode rejection ratio	V+=30V	70	85		65	70		dB
V_{OH}	Output voltage swing	R_L≥2kΩ, V+=30V, over temp. R_L≥10kΩ, V+=30V, over temp.	26 27	28		26 27	28		V V
V_{OL}	Output voltage swing	R_L≥10kΩ, over temp.		5	20		5	20	mV
I_{CC}	Supply current	R_L=∞, V+=30V R_L=∞ on all amplifiers, over temp., V+ =30V		0.5 0.6	1.0 1.2		0.5 0.6	1.0 1.2	mA mA
A_{VOL}	Large-signal voltage gain	R_L≥2kΩ, V_{OUT} ±10V, V+=15V (for large V_O swing) over temp.	50 25	100		25 15	100		V/mV V/mV
PSRR	Supply voltage rejection ratio	R_S=0Ω	65	100		65	100		dB
	Amplifier-to-amplifier coupling[4]	f=1kHz to 20kHz (input referred)		-120			-120		dB
I_{OUT}	Output current Source	V_{IN+}=+1V_{DC}, V_{IN-}=0V_{DC}, V+=15V_{DC}	20	40		20	40		mA
		V_{IN+}=+1V_{DC}, V_{IN-}=0V_{DC}, V+=15V_{DC}, over temp.	10	20		10	20		mA
	Sink	V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC}	10	20		10	20		mA
		V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC}, over temp.	5	8		5	8		mA
		V_{IN+}=0V, V_{IN-}=+1V_{DC}, V_O=200mV	12	50		12	50		µA
I_{SC}	Short circuit current[5]			40	60		40	60	mA
	Differential input voltage[6]				V+			V+	V
GBW	Unity gain bandwidth	T_A=25°C		1			1		MHz
SR	Slew rate	T_A=25°C		0.3			0.3		V/µs
V_{NOISE}	Input noise voltage	T_A=25°C, f=1kHz		40			40		nV/√Hz

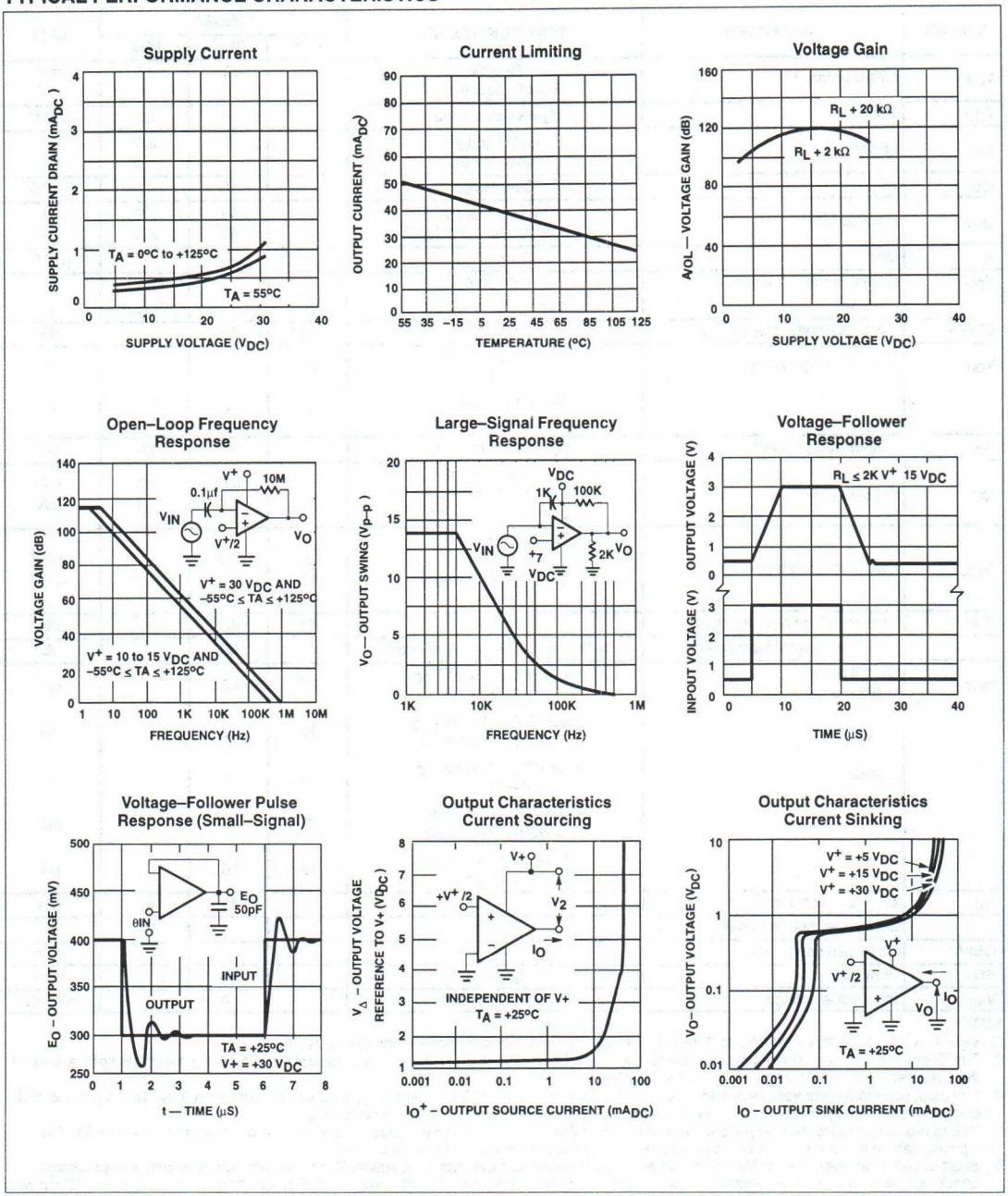
DC ELECTRICAL CHARACTERISTICS T_A=25°C, V+=+5V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM358A			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω R_S=0Ω, over temp.		±2	±3 ±5	mV mV
V_{OS}	Drift	R_S=0Ω, over temp.		7	20	µV/°C
I_{OS}	Offset current	I_{IN} (+)-I_{IN} (-) Over temp.		5	±30 ±75	nA nA
I_{OS}	Drift	Over temp.		10	300	pA/°C
I_{BIAS}	Input current[2]	I_{IN} (+) or I_{IN} (-) Over temp., I_{IN} (+) or I_{IN} (-)		45 40	100 200	nA nA
I_B	Drift	Over temp.		50		pA/°C
V_{CM}	Common-mode voltage range[3]	V+=30V Over temp., V+=30V	0 0		V+-1.5 V+-2.0	V V
CMRR	Common-mode rejection ratio	V+=30V	65	85		dB
V_{OH}	Output voltage swing	R_L≥2kΩ, V+=30V, over temp. R_L≥10kΩ, V+=30V, over temp.	26 27	 28		V V
V_{OL}	Output voltage swing	R_L≥10kΩ, over temp.		5	20	mV
I_{CC}	Supply current	R_L=∞, V+=30V R_L=∞ on all amplifiers, over temp., V+ =30V		0.5 0.6	1.0 1.2	mA mA
A_{VOL}	Large-signal voltage gain	R_L≥2kΩ, V_{OUT} ±10V, V+=15V (for large V_O swing) over temp.	25 15	100		V/mV V/mV
PSRR	Supply voltage rejection ratio	R_S=0Ω	65	100		dB
	Amplifier-to-amplifier coupling[4]	f=1kHz to 20kHz (input referred)		-120		dB
I_{OUT}	Output current Source	V_{IN+}=+1V_{DC}, V_{IN-}=0V_{DC}, V+=15V_{DC} V_{IN+}=+1V_{DC}, V_{IN-}=0V_{DC}, V+=15V_{DC}, over temp.	20 10	40 20		mA mA
	Sink	V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC} V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC}, over temp. V_{IN+}=0V, V_{IN-}=+1V_{DC}, V_O=200mV	10 5 12	20 8 50		mA mA µA
I_{SC}	Short circuit current[5]			40	60	mA
	Differential input voltage[6]				V+	V
GBW	Unity gain bandwidth	T_A=25°C		1		MHz
SR	Slew rate	T_A=25°C		0.3		V/µs
V_{NOISE}	Input noise voltage	T_A=25°C, f=1kHz		40		nV/√Hz

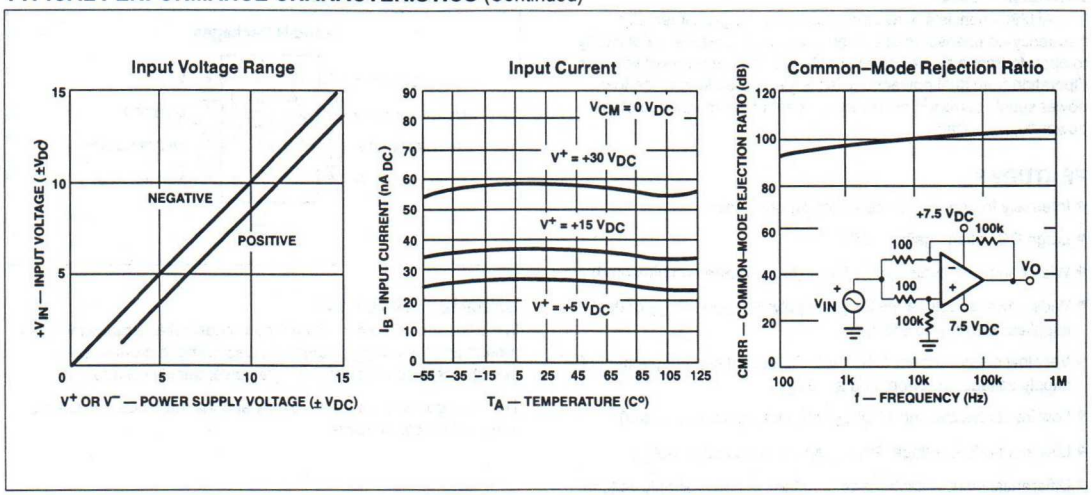
NOTES:

1. V_O ≈ 1.4V, R_S=0Ω with V+ from 5V to 30V; and over the full input common-mode range (0V to V+ -1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to +32V without damage.
4. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance coupling increases at higher frequencies.
5. Short-circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to +32V_{DC} without damage.

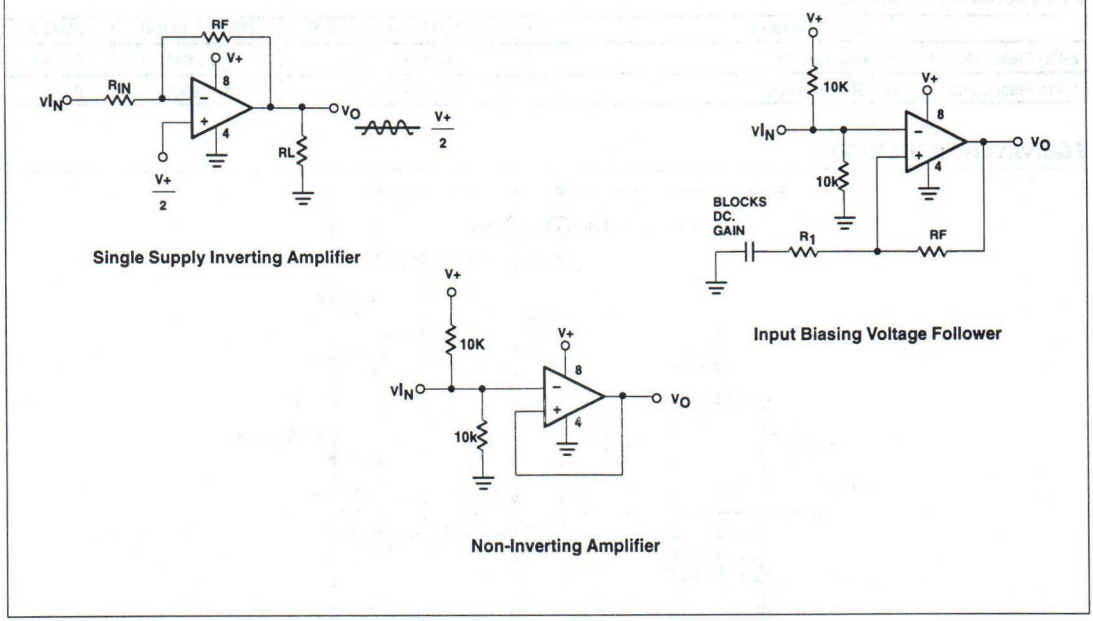
TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TYPICAL APPLICATIONS



Low power dual operational amplifier

AU2904

DESCRIPTION

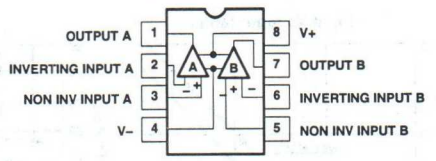
The AU2904 consists of two independent, high-gain, internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible, and the low power supply current drain is independent of the magnitude of the power supply voltage.

FEATURES

- Internally frequency-compensated for unity gain
- Large DC voltage gain: 100dB
- Wide bandwidth (unity gain): 1MHz (temperature-compensated)
- Wide power supply range Single supply: $3V_{DC}$ to $30V_{DC}$ or dual supplies: $\pm1.5V_{DC}$ to $\pm15V_{DC}$
- Very low supply current drain (400μA): essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)
- Low input bias current: $45nA_{DC}$ (temperature-compensated)
- Low input offset voltage: $2mV_{DC}$ and offset current: $5nA_{DC}$
- Differential input voltage range equal to the power supply voltage
- Large output voltage: $0V_{DC}$ to V+-$1.5V_{DC}$ swing

PIN CONFIGURATION

D and N Packages



Top View

UNIQUE FEATURES

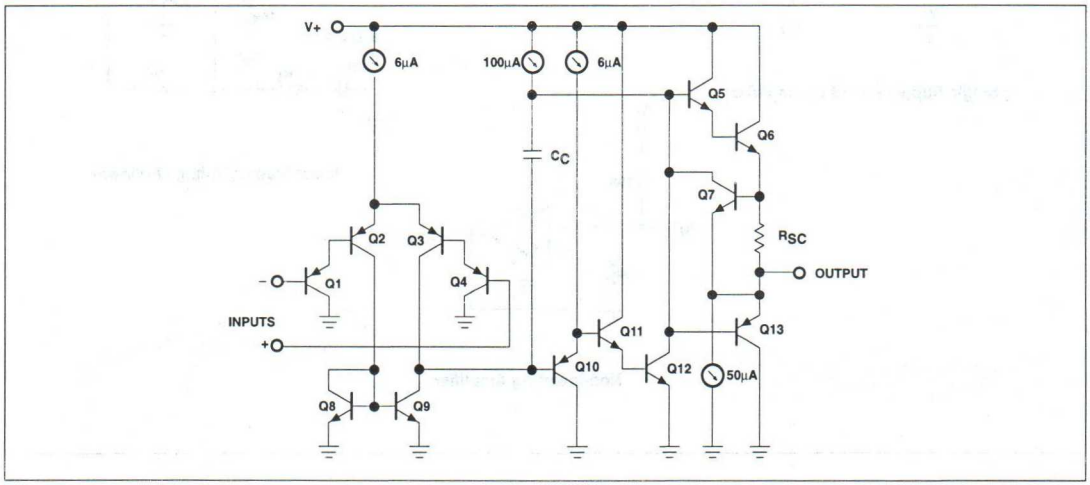
In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain crossover frequency and the input bias current are temperature-compensated.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +125°C	AU2904N	0404B
8-Pin Plastic Small Outline (SO) Package	-40 to +125°C	AU2904D	0174C

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage V+	32 or ±16	V_{DC}
	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	-0.3 to +32	V_{DC}
P_{DMAX}	Maximum power dissipation, T_A=25°C(still-air)[1]		
	N package	1160	mW
	D package	780	mW
	Output short-circuit to GND[5] V+<15V_{DC} and T_A=25°C	Continuous	
T_A	Operating ambient temperature range AU2904	-40 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. Derate above 25°C at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=25°C V+ =+5V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	AU2904			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω		±2	±7	mV
		R_S=0Ω, over temp.			±9	
V_{OS}	Drift	R_S=0Ω, over temp.		7		µV/°C
I_{OS}	Offset current	$I_{IN}(+)$-$I_{IN}(-)$		±5	±50	nA
		Over temp.			±150	nA
I_{OS}	Drift	Over temp.		10		pA/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	250	nA
		Over temp., $I_{IN}(+)$ or $I_{IN}(-)$		40	500	
I_{BIAS}	Drift	Over temp.		50		pA/°C
V_{CM}	Common-mode voltage range[3]	V+=30V	0		V+-1.5	V
		Over temp., V+=30V	0		V+-2.0	V
CMRR	Common-mode rejection ratio	V+=30V	65	70		dB
V_{OH}	Output voltage swing	R_L≥2kΩ, V+=30V, over temp.	26			V
		R_L≥10kΩ, V+=30V, over temp.	27	26		
V_{OL}	Output voltage swing	R_L≥10kΩ, Over temp.		5	20	mV
I_{CC}	Supply current	R_L=∞, V+=30V R_L=∞ on all amplifiers, Over temp., V+=30V		0.5 0.6	1.0 1.2	mA mA
A_{VOL}	Large-signal voltage gain	R_L≥2kΩ, V_{OUT} ±10V, V+=15V	25	100		V/mV
		Over temp.	15			
PSRR	Supply voltage rejection ratio	R_S=0Ω	65	100		dB
	Amplifier-to-amplifier coupling[4]	f=1kHz to 20kHz (input referred)		-120		dB
I_{OUT}	Output current source	V_{IN+}=+1V_{DC}, V_{IN-}=0V_{DC}, V+=15V_{DC}	20	40		mA
		Over temp.	10	20		

DC ELECTRICAL CHARACTERISTICS (continued)

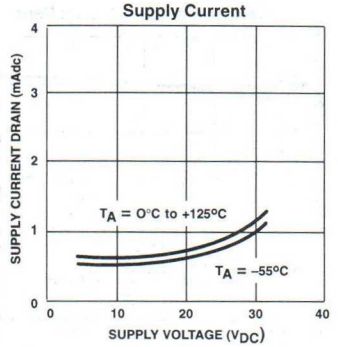
SYMBOL	PARAMETER	TEST CONDITIONS	AU2904			UNIT
			Min	Typ	Max	
I_{OUT}	Output current					
	Sink	V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC}	10	20		mA
		V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC}, over temp.	5	8		mA
		V_{IN+}=0V, V_{IN-}=+1V_{DC}, V_O=200mV	12	50		µA
I_{SC}	Short circuit current[5]			40	60	mA
	Differential input voltage[3]				V+	V
GBW	Unity gain bandwidth	T_A=25°C		1		MHz
SR	Slew rate	T_A=25°C		0.3		V/µs
V_{NOISE}	Input noise voltage	T_A=25°C f=1kHz		40		nV/√Hz

NOTES:

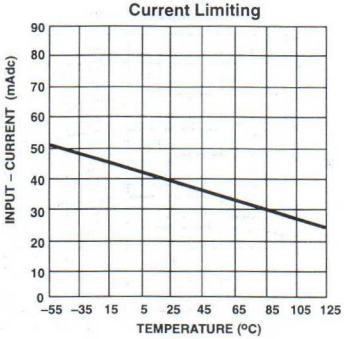
1. V_O ≈ 1.4V, R_S=0Ω with V_{CC} from 5V to 30V and over full input common-mode range (0V_{DC}+ to V_{CC}-1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+-1.5, but either or both inputs can go to +32V without damage.
4. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of coupling increases at higher frequencies.
5. Short-circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.

TYPICAL PERFORMANCE CHARACTERISTICS

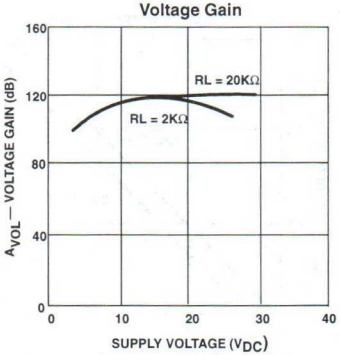
Supply Current



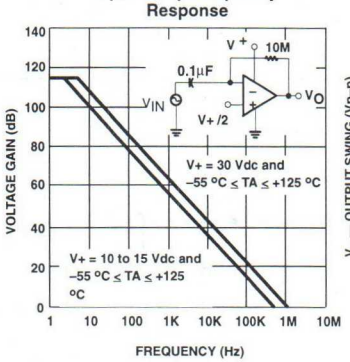
Current Limiting



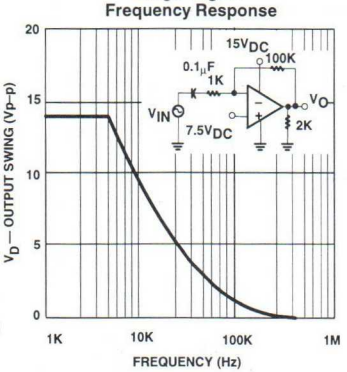
Voltage Gain



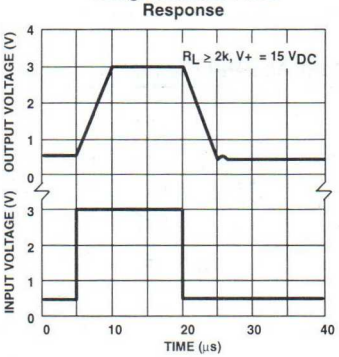
Oper–Loop Frequency Response



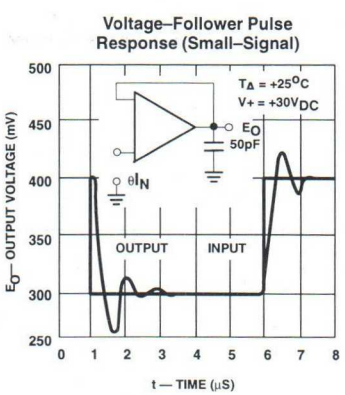
Large–Signal Frequency Response



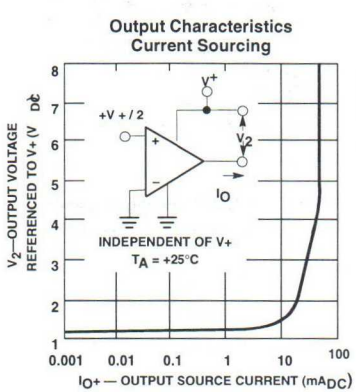
Voltage–Follower Pulse Response



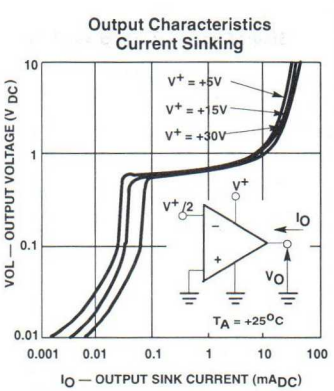
Voltage–Follower Pulse Response (Small–Signal)



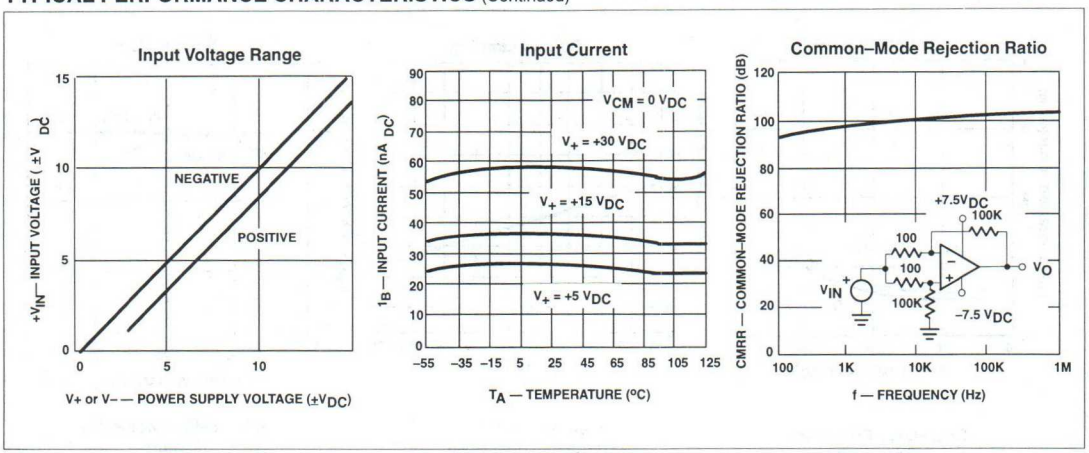
Output Characteristics Current Sourcing



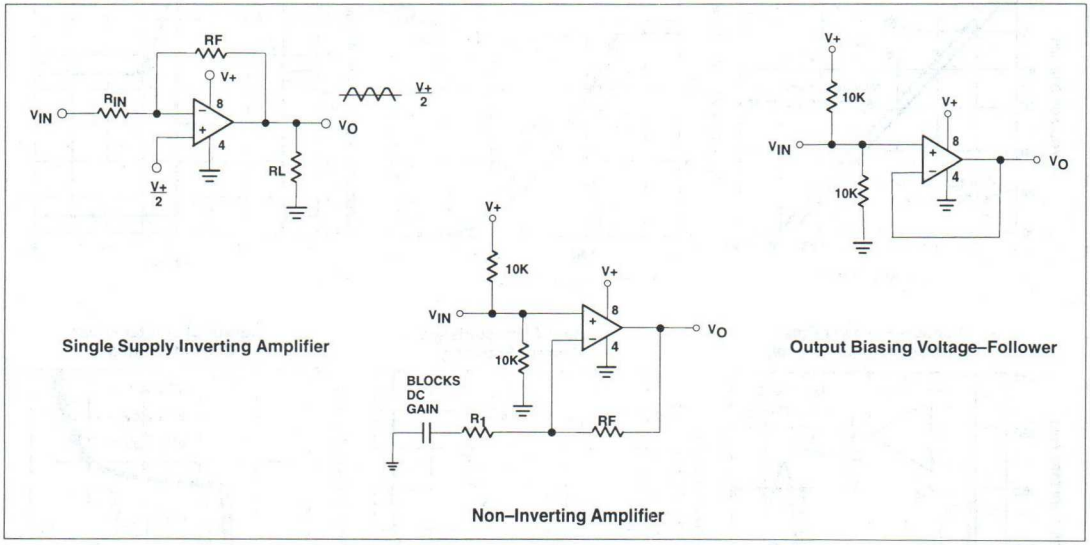
Output Characteristics Current Sinking



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TYPICAL APPLICATIONS



Matched quad high-performance low-voltage operational amplifier

NE/SA5234

DESCRIPTION

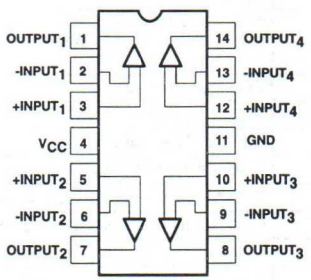
The NE/SA5234 is a matched, low voltage, high performance quad operational amplifier. Among its unique input and output characteristics is the capability for both input and output rail-to-rail operation, particularly critical in low voltage applications. The output swings to less than 50mV of both rails across the entire power supply range. The NE/SA5234 is capable of delivering 5.5V peak-to-peak across a 600Ω load and will typically draw only 700μA per amplifier. The bandwidth is 2.5MHz and the 1% settling time is 1.4μs.

FEATURES

- Wide common-mode input voltage range: 250mV beyond both rails
- Output swing within 50mV of both rails
- Functionality to 1.8V typical
- Low current consumption: 700μA per amplifier
- ±15mA output current capability
- Unity gain bandwidth: 2.5MHz
- Slew rate: 0.8V/μs
- Low noise: 25nV/√Hz
- Electrostatic discharge protection
- Short-circuit protection
- Output inversion prevention

PIN CONFIGURATION

N, and D PACKAGES



APPLICATIONS

- Automotive electronics
- Signal conditioning and sensing amplification
- Portable instrumentation
  - Test and measurement
  - Medical monitors and diagnostics
  - Remote meters
- Audio equipment
- Security systems
- Communications
  - Pagers
  - Cellular telephone
  - LAN
  - 5V Datacom bus
- Error amplifier in motor drives
- Transducer buffer amplifier

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5234D	0175D
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5234N	0405B
14-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5234D	0175D
14-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5234N	0405B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
V_{ESD}	ESD protection voltage at any pin[5] human body model robot model	 2000 200	 V V
V_S	Dual supply voltage	±3.5	V
V_{DP}	Voltage at any device pin[1]	V_S ± 0.5	V
I_{DP}	Current into any device pin[1]	± 50	mA
V_{IN}	Differential input voltage[2]	0.5	V
V_{CM}	Common-mode input voltage (positive)	V_{CC} + 0.5	V
V_{CM}	Common-mode input voltage (negative)	V_{EE} - 0.5	V
P_D	Power dissipation[3]	500	mW
T_J	Operating junction temperature[3]	+150	°C
V_{SC}	Supply voltage allowing indefinite output short circuit to either rail[3,4]	7	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C
θ_{JA}	Thermal impedance 14 pin Plastic DIP 14 pin Plastic SO	 80 115	 °C/W °C/W

NOTES:
1. Each pin is protected by ESD diodes. The voltage at any pin is limited by the ESD diodes.
2. The differential input of each amplifier is limited by two internal diodes, connected in parallel and opposite to each other. For more differential input range, use differential resistors in series with the input pins.
3. The maximum operating junction temperature is +150°C. At elevated temperatures, devices must be derated according to the package thermal resistance and device mounting conditions. Derates above +25°C: F package at 6.7mW/°C; N package at 9.5mW/°C; D package at 6.25mW/°C.
4. Simultaneous short circuits of two or more amplifiers to the positive or negative rail can exceed the power dissipation ratings and cause eventual destruction of the device.
5. Guaranteed by design.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	+2 to +5.5	V
V_S	Dual supply voltage	±1 to ±2.75	V
V_{CM}	Common-mode input voltage (positive)	V_{CC} + 0.25	V
V_{CM}	Common-mode input voltage (negative)	V_{EE} - 0.25	V
T_A	Temperature NE SA	 0 to +70 -40 to +85	 °C °C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2 to 5.5V, V_{EE} = 0V, T_A = 25°C; $V_{EE} < V_{CM} < V_{CC}$; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234			SA5234			
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_{CC} = 5.5V		2.8	4.0		2.8	4.0	mA
		V_{CC} = 5.5V over full temperature range		3.0	4.6		3.2	4.8	
V_{OS}	Offset voltage			±0.2	±4		±0.2	±4	mV
		Over full temperature range		±0.4	±5		±0.6	±5	
$\Delta V_{OS}/\Delta T$	Offset voltage drift with temperature			4			4		µV/°C
ΔV_{OS}	Offset voltage difference between any amplifiers in the same package at the same common mode level[1]			0.4	3		0.4	3	mV
		Over full temperature range		0.8	4		1.2	4	
I_{OS}	Offset current			±3	±20		±3	±30	nA
		Over full temperature range		±4	±30		±6	±60	
$\Delta I_{OS}/\Delta T$	Offset current drift with temperature			0.02	±.3		0.03	±.3	nA/°C
I_B	Input bias current[1]	$V_{EE} < V_{CM} < V_{EE}$ +0.5V	-200	-90		-200	-90		nA
		Over full temperature range	-225	-100		-250	-150		
		V_{EE} +1V < V_{CM} < V_{CC}		25	70		25	75	
		Over full temperature range		35	100		35	120	
$\Delta I_B/\Delta T$	Input bias current drift with temperature			0.5			0.5		nA/°C
ΔI_B	Input bias current difference between any amplifier in the same package at the same common mode level.	$V_{EE} < V_{CM} < V_{EE}$ +0.5V		10	30		10	30	nA
		Over full temperature range		25	50		50	70	
		V_{EE} +1V < V_{CM} < V_{CC}		5	20		5	20	
		Over full temperature range		15	30		25	50	
V_{CM}	Common-mode input range	$V_{OS} \leq$ 6mV	V_{EE}-0.25		V_{CC}+0.25	V_{EE}-0.25		V_{CC}+0.25	V
		$V_{OS} \leq$ 6mV over full temperature range	V_{EE}-0.1		V_{CC}+0.1	V_{EE}-0.1		V_{CC}+0.1	
CMRR	Common-mode rejection ratio, small signal	$V_{EE} < V_{CM} < V_{EE}$+0.5V, V_{EE}+1V < V_{CM} < V_{CC}		100		90	100		dB
		Over full temperature range		100		80	90		
	Common-mode rejection ratio, large signal	$V_{EE} < V_{CM} < V_{CC}$		90			100		
		Over full temperature range		80			90		
PSRR	Power supply rejection ratio	$V_{EE} < V_{CM} < V_{CC}$	80	100		80	100		dB
		Over full temperature range	80	90		80	90		

DC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234			SA5234			
			MIN	TYP	MAX	MIN	TYP	MAX	
I_L	Peak load current, sink and source		10	12		10	12		mA
		Over full temperature range	5	8		5	8		
A_{VOL}	Open-loop voltage gain		90	110		90	110		dB
		Over full temperature range		90			90		
V_{OUT}	Output voltage swing	I_{PEAK} = 0.1mA	V_{EE}+0.05		V_{CC}-0.05	V_{EE}+0.1		V_{CC}-0.1	V
		I_{PEAK} = 10mA	V_{EE}+0.25		V_{CC}-0.25	V_{EE}+0.25		V_{CC}-0.25	
		I_{PEAK} = 5mA over full temp range	V_{EE}+0.2		V_{CC}-0.2	V_{EE}+0.2		V_{CC}-0.2	
	Output voltage swing for V_{CC} = 2.75V, V_{EE} = -2.75V	R_L = 2kΩ	V_{EE}+0.2		V_{CC}-0.2	V_{EE}+0.2		V_{CC}-0.2	V
		R_L = 600Ω,	V_{EE}+0.25		V_{CC}-0.25	V_{EE}+0.25		V_{CC}-0.25	

NOTES:

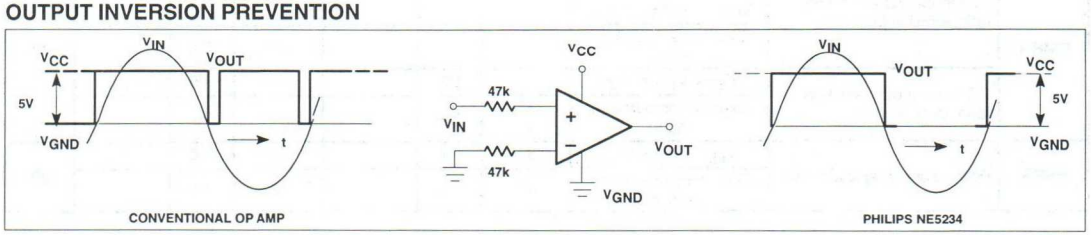
1. These parameters are measured for $V_{EE} < V_{CM} < V_{EE}$+.5V and for V_{EE}+1V < $V_{CM} < V_{CC}$. By design these parameters are intermediate for common mode ranges between the measured regions.

AC ELECTRICAL CHARACTERISTICS

T_A = +25°C; V_{CC} = 2 to 5.5V; R_L = 10k; C_L = 100pF; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234			SA/SE5234			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	Over full temperature range	0.5	0.8		0.5	0.8		V/μs
BW	Unity gain bandwidth: -3dB	Over full temperature range	2	2.5	4.0	2	2.5	4.0	MHz
θ_M	Phase Margin	C_L = 50pF		55			55		deg
t_S	1% settling time	A_V = 1, 1V step		1.4			1.4		μs
V_N	Input referred voltage noise	A_V = 1, R_S = 0Ω, at 1kHz		25			25		nV/Hz$^{1/2}$
THD	Total harmonic distortion	10kHz, $1V_{P-P}$, A_V = 1		0.1			0.1		%

OUTPUT INVERSION PREVENTION



Using the NE/SA5234 amplifier

AN1651

Author: L. Hadley

I. SUMMARY

The NE/SA5234 is a unique low-voltage quad operational amplifier specifically designed to operate in a broadly diverse environment. It is an enhanced pin-for-pin replacement for the LM324 category of devices. Supply conditions can range from 1.8V to 6.0V with a resultant current drain of 2.8mA,-700µA per op amp.

Most notable are the input and output dynamic range characteristics of the individual op amps. The common-mode input voltage can actually exceed the positive and negative supply rails by 250mV with no danger of output latching or polarity reversal. In addition, the output of each op amp will swing to within 50mV of the supply rails over the full supply range.

The frequency related characteristics are also above average for low voltage devices in this class. Internal unity gain compensation makes the NE5234 very resistant to any tendency to oscillate in low closed-loop gain configurations. Even so, a unity-gain bandwidth of 2.5MHz is retained. Slew rate is 0.8V/µs and each op amp will settle to a 1% of nominal level within 1.4µs.

II. DETAILED DESCRIPTION

Input Stage

The input differential amplifier consists of a compound transistor structure of parallel NPN and PNP transistors which account for the unique over-drive characteristics of the NE5234. Referring to Figure 1, it is seen that the NPN pair, Q1 and Q2, allow the input to operate in the common-mode input voltage range of 1V above V_{EE}. This region is designated the N-mode region in Figure 3a. Operation in the common-mode range below 1V transfers the input stage into the P-mode of operation.

In the N-mode operating condition, collector current from Q1 and Q2 is summed in the output emitter node of Q10 and Q12 respectively. Q1's base is the non-inverting input and Q2's base the inverting input node for the amplifier.

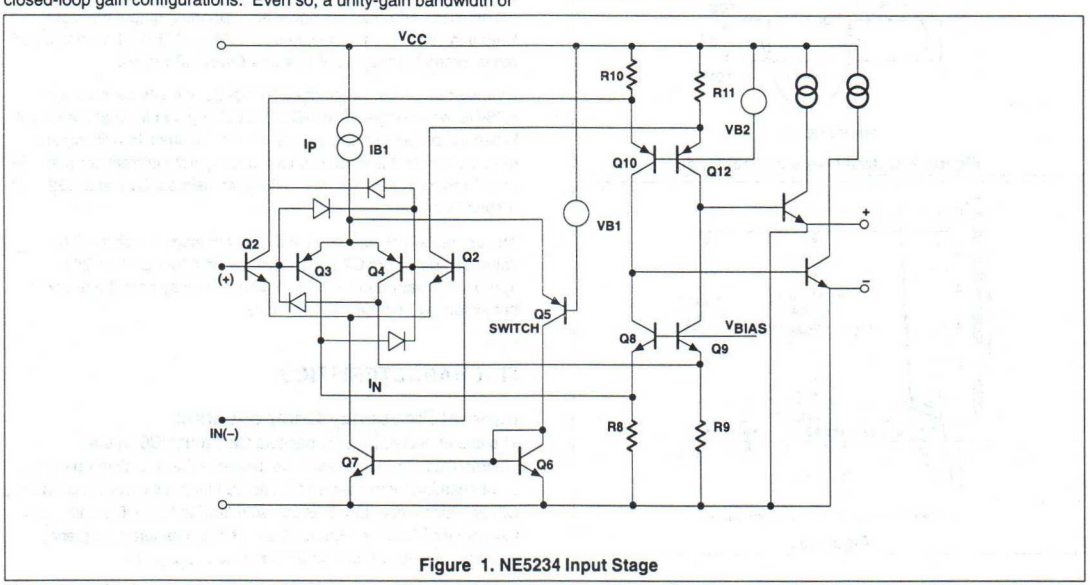


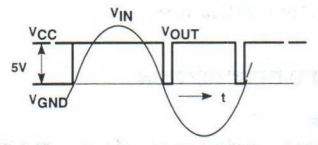
Figure 1. NE5234 Input Stage

Linear operation between the two modes is governed by a current steering circuit consisting of Q5,6 and 7 in conjunction with voltage reference VB1. Operation in the

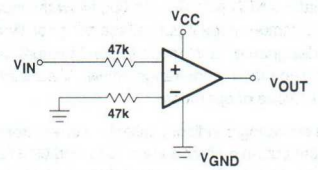
N-region of the common-mode range will automatically cause Q5 to transfer the IB1 current source to Q7 and the NPN transistor pair Q1 and Q2. Operation below the 1V level at the inputs allows the current from IB1 to be fed directly to Q3 and Q4 emitters giving them priority in processing the signal and linearizing their transfer function. (The sum of the NPN and PNP input pair currents remain constant.)

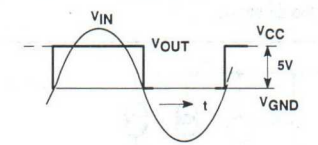
Operation in the common-mode range near the positive supply rail would normally cause the input stage NPN transistor's base collector junction to become forward biased (base current flow directly to the collector circuit) reversing the collector current flow direction. In a conventional op amp, this would have the adverse effect of reversing the output signal polarity as the operating region is traversed by the input signal. (see Figure 2)

To prevent this from occurring, large geometry diode-connected transistors are cross-connected to the opposite NPN collector, (Q1, Q2). This current, in turn, is summed at the emitter of Q12 pulling it above the V_{CC} rail voltage and preventing polarity reversal. The inverse condition occurs when Q2 is driven above the positive rail, with Q10 emitter being pulled up and signal polarity preserved. (See Figure 1)



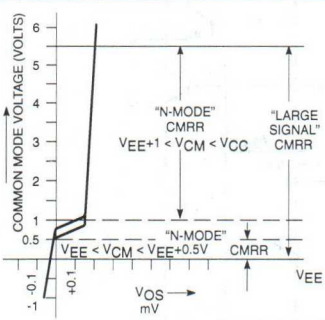
CONVENTIONAL OP AMP





PHILIPS NE5234

Figure 2. Output Inversion Protection



NE5234 Common-Mode Operating Regions

Figure 3.

For negative going input signals, which drive the inputs toward the V_{EE} rail and below, another set of diode-connected transistors come into operation. These steer the current from the input into Q8 or Q9 emitter circuits again preventing the reversal effect.

Figure 3 shows graphically how the N and P mode transitions relate to the common-mode input voltage and the offset voltage V_{OS}.

Intermediate Amplifier and Output Stage (Figure 4)

The intermediate stage is isolated from the input amplifier by emitter followers
to prevent any adverse loading effect. This stage adds gain to the over all amplifier and translates levels for the following class-AB current-control driver. Note that I_2 is the inverting input and I_1 the non-inverting input. The output is taken from multiple collectors on the non-inverting side and provides matching for the following stage.

Class-AB control of the output stage is achieved by Q61 and Q62 with the associated output current regulators. These act to monitor the smallest current of the non-load supporting output transistor to keep it in conduction. Thus, neither Q71 or Q81 is allowed to cutoff but is forced to remain in the proper Class-AB region.

Overload protection is provided by monitor circuits consisting of R76-D2 for sinking and R86-D3 for sourcing condition at the output. When the output current, source or sink, reaches 15 milliamperes, drive current to the stage is shunted away from current sources IB6 or IB9 reducing base current to driver transistors Q72 and Q82 respectively.

The prevention of saturation in the output stage is achieved by saturation detectors Q78 and Q88. When either Q71 or Q81 approaches saturation, current is shunted away from the driver transistors, Q72 or Q83 respectively.

III. CHARACTERISTICS

Internal Frequency Compensation

The use of nested Miller capacitors C2 through C6, in the intermediate and output sections, provides the overall frequency compensation for the amplifier. The dominant pole setting capacitor, C2, provides a constant 6dB/octave roll-off to below the unity gain frequency of 2.5MHz. Figure 5 shows the measured frequency response plot for various values of closed-loop gains.

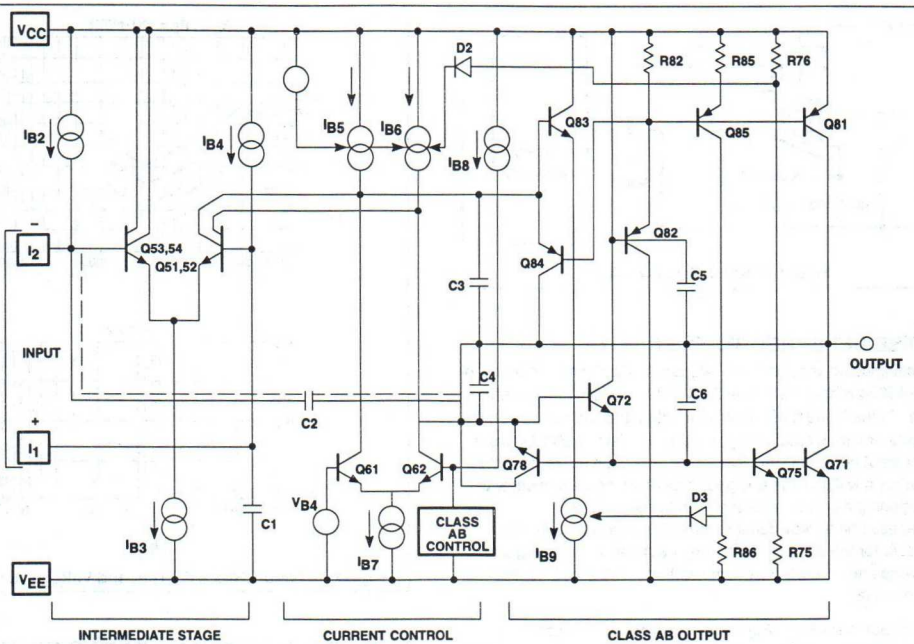


Figure 4.

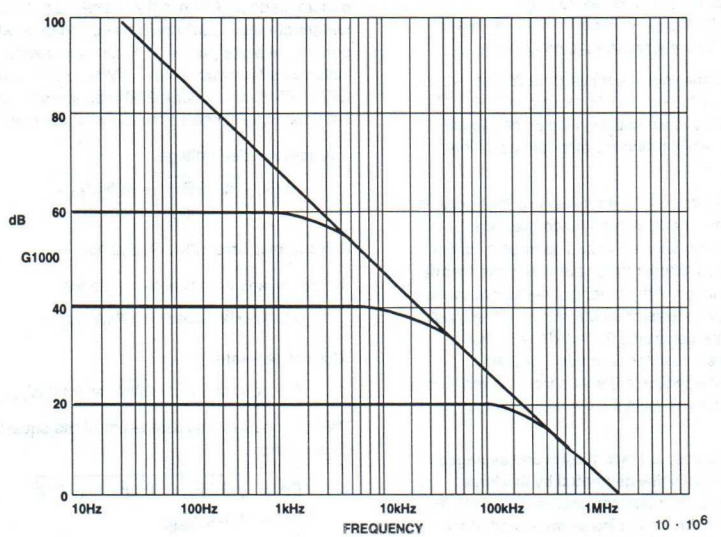


Figure 5. NE5234 Closed Loop Gain vs Frequency

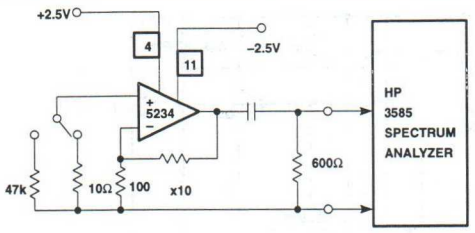


Figure 6. Noise Test Circuit

IV. NOISE REFERRED TO THE INPUT

The typical spectral voltage noise referred to each of the op amps in the NE/SA5234 is specified to be 25nV/√Hz. Current noise is not specified. In the interest of providing a balance of information on the device parameters, a small sample of the standard NE5234s, were tested for input noise current. While this data does not represent a specification, it will give the designer a ball park figure to work with when beginning a particular design with the device. For completeness I have provided the corresponding spectral noise voltage data for the same sample. The data was taken using an HP3585A spectrum analyzer which has the capability of reading noise in nV/√Hz.

The test circuit is shown in Figure 6. As is typical for such measurements the amplifier under test is terminated at its input first with a very low resistance, for the voltage noise reading, followed by the same test with a high value of resistance to register the effect of current noise. The amplifier is set to a non-inverting closed-loop gain of 20dB. Dual supply operation was chosen to allow direct termination of the input resistors to ground.

The measurements were made over the range from 200Hz to 2kHz. Each sample is measured at 200Hz, 500Hz, 1kHz and 2kHz. The data is averaged for each frequency and then the small sample distribution is derived statistically giving the standard deviation relative to the mean.

Referring to the graph in Figure 7a, the equivalent voltage noise is seen to average 18 nV/√Hz. The 95% confidence interval is determined to be approximately one nV/√Hz. The majority of the errors which contribute to this measurement are due to the thermal noise of the parallel combination of the feedback resistor network, in addition to the 10Ω termination resistor on the non-inverting input. At 300° Kelvin a 10Ω resistor generates 0.4 nV/√Hz and the feedback network's equivalent resistance of 90Ω generates 1.2nV/√Hz. Their order-of-magnitude difference from the main noise sources allows them to be neglected in the overall calculation of total stage noise.

Noise current is measured across a 47kΩ resistor and averaged in the same manner. The thermal noise generated by this large resistance is not insignificant. At room temperature it is 28nV/√Hz and must be subtracted from the total noise as measured at the output of the op amp in order to arrive at the equivalent current generated noise voltage. Figure 7b shows the derived current noise distribution for the small sample of 10 NE5234 devices. The result shows that noise current in the 200Hz to 2kHz frequency is typically 0.2pA/√Hz. The 1/f region was not determined for either current or voltage noise.

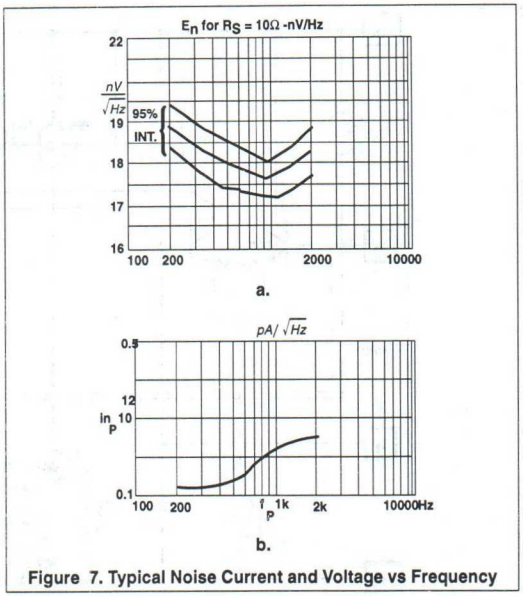


Figure 7. Typical Noise Current and Voltage vs Frequency

V. GUIDE LINES FOR MINIMIZING NOISE

When designing a circuit where noise must be kept to a minimum, the source resistances should be kept low to limit thermally generated degradation in the overall output response. Orders-of-magnitude should be kept in mind when evaluating noise performance of a particular circuit or in planning a new design. For instance, a transducer with a 10kΩ source resistance will generate 2μV of RMS noise over a 20kHz bandwidth. Using the graphical data above, total noise from a gain stage may be calculated.-

Amplifier Noise Voltage (EQ. 1.)

$$25nV/\sqrt{Hz} \cdot \sqrt{BW} = 3.5\mu V_{RMS}$$

$$BW = 10kHz$$

Noise from source 10kΩ Resistance –

Noise Voltage from source resistance (EQ. 2.)

$$14nV/\sqrt{Hz} \cdot \sqrt{BW} = 20\mu V_{RMS}$$

Current generated noise (EQ. 3.)

$$0.2pA/\sqrt{Hz} \cdot 10^3 \cdot \sqrt{BW} = 0.28\mu V_{RMS}$$

The total noise is the root-to-sum-of-the-squares of the individual noise voltages –

$$En = \sqrt{(3.5)^2 + (2.0)^2 + (0.28)^2} \quad \text{(EQ. 4.)}$$

$$= 4.04\mu V_{RMS}$$

To determine the signal-to-noise ratio of the stage we must first choose a stage gain, make it 40dB, and a signal voltage magnitude from the transducer which we will set at $10mV_{RMS}$. The resulting signal-to-noise ratio at the output of this stage is determined by first multiplying the gain times the signal which gives $1V_{RMS}$ with a

resultant noise of 400mV$_{RMS}$. The signal-to-noise ratio is calculated as

$$S/N \quad 20\log_{10}(1.0/4x10^{-4}) = 68dB \qquad \text{(EQ. 5.)}$$

This is quite adequate for good quality audio applications.

Next assume that the bandwidth is cut to 3.0kHz with an input of 1mV$_{RMS}$. The RMS noise is modified by the ratio of the root of the noise channel bandwidths.

$$\left[\frac{\sqrt{3x10^3}}{\sqrt{20x10^3}}\right] \cdot EN = 1.6\mu V_{RMS} \qquad \text{(EQ. 6.)}$$

Amplified Noise = 160μV$_{RMS}$

$$S/N \quad 20\log_{10}\left[\frac{100x10^{-3}}{1.6x10^{-4}}\right] \qquad \text{(EQ. 7.)}$$

$$= 56dB$$

A 56dB S/N will provide superior voice channel communications .

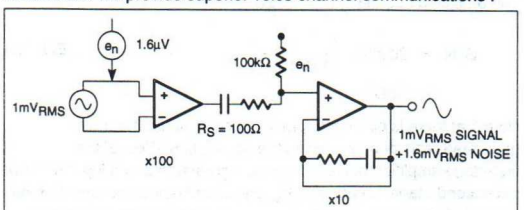


Figure 8.

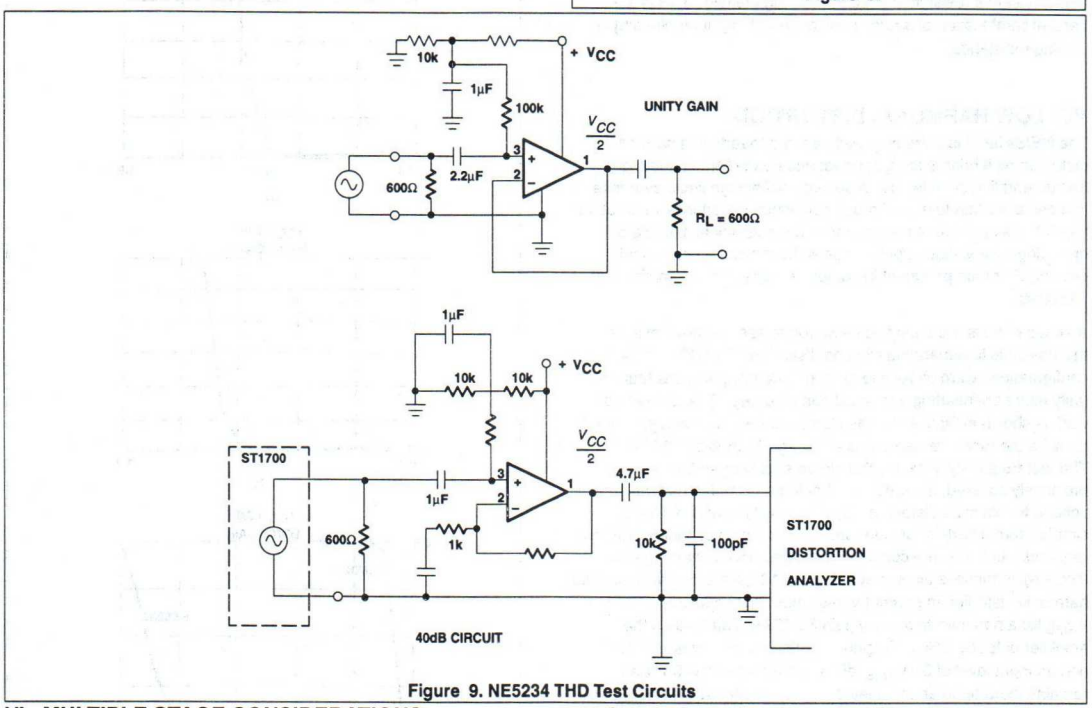


Figure 9. NE5234 THD Test Circuits

VI. MULTIPLE STAGE CONSIDERATIONS

Since multiple noise generators are non-coherent, their total effect is the root-of-the-sum-of-the-squares of the various noise generators at a given amplifier input.

This makes orders-of-magnitude lower noise sources less important than the higher magnitude source. Therefore, when considering the combined signal-to-noise of multiple stages of gain, the first stage in a chain dominates making its design parameters the most critical. For this reason it is good practice to make the preamp stage gain as high as practical to boost signal levels to the second stage allowing at least an order-of-magnitude above the second-stage noise. For instance, a signal input which exceeds the input noise of the following stage by a factor of 10:1 will only be degraded by 0.5% or -46dB, neglecting the first-stage noise. If we use the preceding example with a first-stage output signal of 100mV$_{RMS}$ and a 56dB S/N, and an output noise of 0.16mV. Following this with a 10kHz band limited gain-of-10 second-stage, with a 100kΩ noise source at the non-inverting input, the combined S/N is calculated as follows: (assume a 100Ω source resistance from amplifier #1)

The Second stage output noise is:

$$\left[\sqrt{(0.163x10^{-3})^2 + \left(\sqrt{4KT \cdot 100 \cdot 10,000}\right)^2}\right] \cdot 10 \qquad \text{(EQ. 8.)}$$

$$= 1.6mV$$

$$K = \text{Boltzman'sConstant} = 1.38\text{x}10^{-23}\frac{\text{Joule}}{\text{DegKelvin}} \quad \text{(EQ. 9.)}$$

$$T = 300^{\circ}\text{K} \; ; \; BW = 10\text{kHz}$$

The amplified output signal = $1V_{RMS}$

$$S/N = 20\log_{10}\left(\frac{1}{1.6\text{x}10^{-3}}\right) \quad \text{(EQ. 10.)}$$

$$= 56\text{dB}$$

Note that there is no effect from the second-stage thermally generated resistor noise due to the dominating effect of the first-stage amplified noise being much greater than the input noise of the second-stage. In addition the equivalent noise resistance of the second-stage is essentially the output resistance of the first-stage plus any series resistance used in coupling the two. This is the parallel combination of source resistance with input terminating or biasing resistance.

VII. LOW HARMONIC DISTORTION

The NE/SA5234 is extremely well adapted to reducing harmonic distortion as it relates to signal level and head room in audio and instrumentation circuits. Its unique internal design limits overdrive induced distortion to a level much below that experienced with other low voltage devices. As will be shown, the device is capable of operating over a wide supply range without causing the typical clipping distortion prevalent in companion operational amplifiers of this class.

A series of tests are shown to allow you to see just how resistant this device is to generating clipping distortion. Two different gain configurations were chosen to demonstrate this particular feature: unity gain non-inverting and 40dB non-inverting. The test set-up was as shown in Figure 9. The Harmonic Distortion analyzer used to make the measurements was a Storage Technology ST1700. The test frequency is 1kHz. For single supply operation, as previously covered, the amplifier should be biased to half the supply voltage to minimize distortion. Operation with dual supplies is simpler from a parts count standpoint as isolation capacitors are not required. Also the time constants associated with charging and discharging these is eliminated . Figure 10a,b and c shows the total harmonic distortion in percent versus input voltage level at 1kHz in V_{RMS} for a non-inverting, unity gain NE5234. The load on the amplifier output is 10kΩ. Beginning with a supply voltage of 1.8V and an input level of $0.1V_{RMS}$, distortion is well below 0.2% ad remains there up to an input level just over $0.5V_{RMS}$ ($1.4V_{P-P}$) and increases to 0.4% for for $0.6V_{RMS}$ ($1.7V_{P-P}$).

For a 2V supply, the input levels increase to $0.65V_{RMS}$ and $0.7V_{RMS}$, respectively for similar levels of distortion. With a supply voltage of 3.0V the input may be increased to $1V_{RMS}$ before THD rises to 0.2% and $1.1V_{RMS}$ for only 0.8% THD. Operation with a 600Ω load will only raise the THD figures slightly . By way of comparison, Figure 10c shows the greatly reduced dynamic range experienced when an LM324 is plugged into the test socket in place of the NE5234. Note that The THD is completely off scale for the case of 1.8 and 2.0V supply, then is barely usable for the low level end of the 3.0V supply example. Figure 11a, b, and c demonstrates the effect on harmonic distortion when closed loop gain is increased to 40dB in the non-inverting mode. It is evident that little increase in THD levels result. The graphs for the 2.0 and 3.0V supply case also include additional information on the effect of a 600Ω load on distortion.

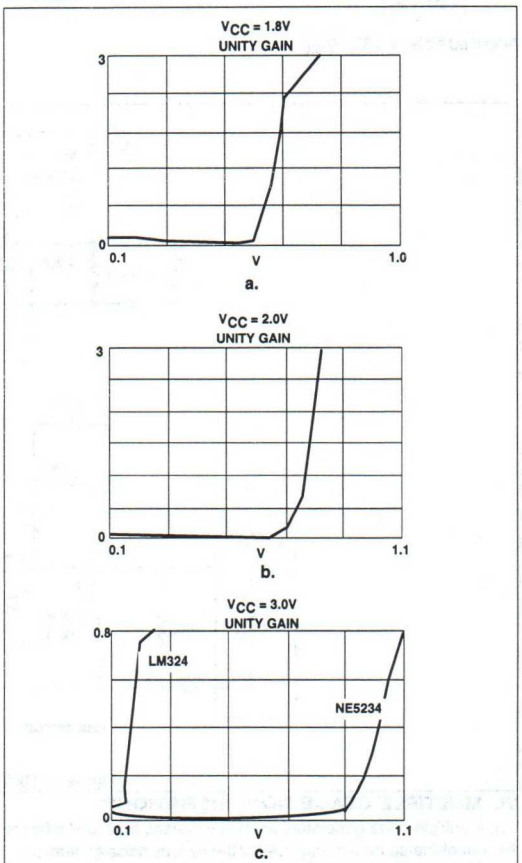


Figure 10. THD vs Supply Voltage for $1V_{RMS}$ Output

Using the NE/SA5234 amplifier

AN1651

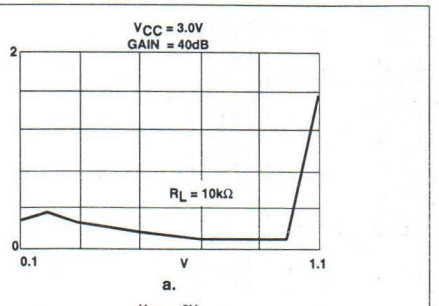


Figure 11. THD vs Load

VIII. GAIN-BANDWIDTH VS CLOSED LOOP FREQUENCY RESPONSE

Figure 5 shows the small signal frequency response of the NE5234 versus closed-loop gain in dB. The test circuit is shown in Figure 6. The plot is taken from measured data and thus shows how each value of closed-loop gain coincides with the open-loop response curve. The NE/SA5234's open-loop gain response has a uniform 6dB/octave roll-off which continues beyond 2.5MHz. This factor guarantees each op amp in the IC a high stability in virtually any gain configuration. In making these measurements, dual supplies of ±2.5V were used in order to allow a grounded reference plane and no coupling capacitors which might cause frequency related errors.

A critical parameter which affects the reproduction quality of complex waveforms is the gain-bandwidth-product of the operational amplifier. Essentially, this is a measure of the maximum frequency handling characteristics of any operational amplifier for a given closed-loop gain. As is evident from the graph, the NE/SA5234 has a 2.5MHz unity gain cross-over frequency — much higher than most other low voltage op amps. For comparison, the μA741 has a gain-bandwidth-product of 1MHz, as do the LM324 and the MC3403.

IX. LOOP-GAIN

The dynamic signal response of any closed-loop amplifier stage is a function of the Loop-gain of that particular stage. Loop-gain is equal to the open-loop gain in dB, at a given frequency, minus the closed-loop gain of the stage. The greater the Loop-gain, the lower the transfer function error of the device. Essentially, any parametric error is reduced by the factor of the Loop-gain. This includes output resistance and output signal voltage accuracy. It is good practice then to maximize Loop-gain to the degree that stage gain may be sacrificed for bandwidth. In some cases it is actually better to use two stages of gain in order to preserve signal quality than to use one high gain stage. Of course, there is a trade-off between the aforementioned factors that affect the signal-to-noise ratio of the stage and optimizing the Loop-gain. For example, a voice-band audio stage which requires 3kHz bandwidth, should be limited to a closed-loop gain of 40dB for lowest distortion in the output signal. For higher quality audio applications requiring a 20kHz bandwidth, the closed-loop gain must be limited to 20dB. This results in a Loop-gain of 20dB at the highest signal frequency.

A second consideration in the list of frequency dependent parameters is the effect of amplifier slew rate. Not only is it frequency dependent but it is also a function of signal amplitude, as we shall see in the next section.

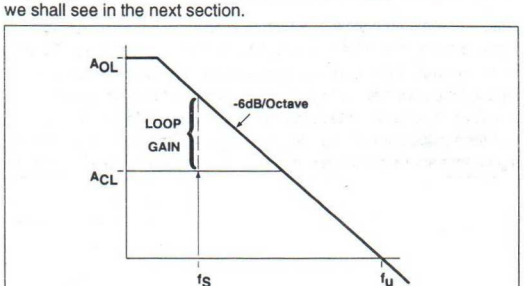


Figure 12.

X. SLEW RATE RESPONSE

The slew rate of an operational amplifier determines how fast it can respond to a signal, and is measured in volts-per-microsecond. The NE5234 has a typical slew rate of 0.8V/μs. Let us see just what this means in terms of signal handling capability. If a sinusoidal input signal, V_S, is used as reference, it is specified by its frequency and peak amplitude, V_P as follows:

$$V_S = V_P \sin (2\pi f t) \qquad \text{(EQ. 11.)}$$

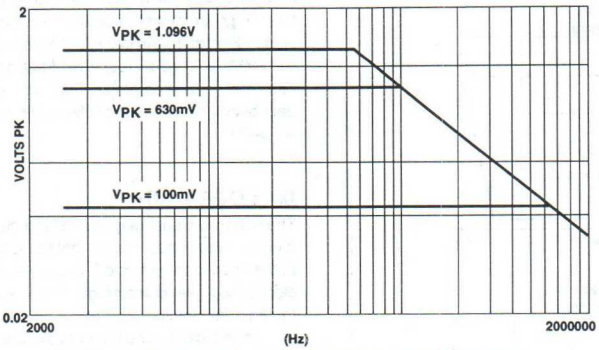


Figure 13. Slew Rate Limiting Amplitude vs Frequency

Slew Rate (SR) is the time-rate-of-change of the signal voltage during any complete cycle, that is over the range of 0 to 2π. This amounts to taking the time derivative of the sine wave which results in multiplying the cosine by the factor '2πf'.

An example of the trade off between signal amplitude and frequency is shown below for the NE5234 slew rate of 0.8V/μs. As shown in Figure 13, the maximum allowable amplitude signal which can be reproduced is determined by the slew rate response line which gives peak output volts versus frequency in Hertz.

Mathematically, slew rate is determined, by the equation below, as the derivative of the sine wave signal. The resultant slew rate function changes with both frequency and amplitude.

Slew Rate $= V_P\ (2\pi\ f)\ \cos\ (2\pi\ f\ t)$

Note that maximum slew rate occurs where the input sine wave signal crosses the values of 0, π, and 2π on the radian axis. To get a feel for what this means in regards to the typical low voltage circuit, let us consider a $1V_{RMS}$ sinusoidal input to a unity gain amplifier. The peak voltage in the above equation is 1.414V. One can then calculate the required slew rate to faithfully reproduce this signal for various signal frequencies. Or with a given slew rate and a required peak signal amplitude, the maximum frequency before slew rate limiting occurs may be determined. For example using the above amplitude of $1V_{RMS}$, and the slew rate of the NE5234 which is 800,000V/sec, one determines that the highest frequency component which may be reproduced before slew rate distortion occurs is:

800,000 V/sec / 2π • 1.414 volts peak = 90,090Hz. A graphical representation of this relationship is shown in Figure 13. By using this graph along with the information in the preceding Figure 10 and Figure 11, which relate usable signal levels versus power supply voltage, the dynamic behavior of a particular design may be predicted. For instance, given a single supply configuration operating at 2.0V, Figure 10b shows an upper limit to input amplitude of $0.7V_{RMS}$, or about 1V peak for 1% THD. Using this level with the data in Figure 13 leads to a figure of 116kHz as an upper frequency limit for a unity gain amplifier stage operating at 2V DC.

$$\frac{dV_S}{d\ t} = V_P\ \omega \cos\ \omega t \qquad \text{(EQ. 12.)}$$
$$= \text{Slew Rate}$$

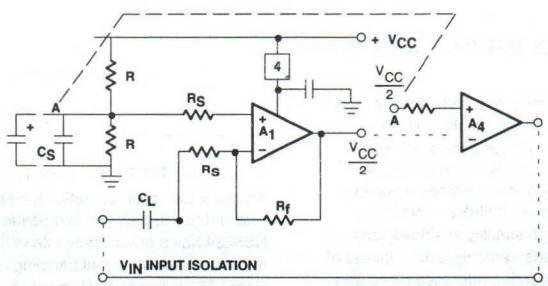


Figure 14. Single Supply Biasing in Cascade

XI. PROCEDURES

Single Supply Operation

When the NE/SA5234 is used in an application where a single supply is necessary, input common-mode biasing to half the supply is recommended for best signal reproduction. Referring to Figure 14, a simplified inverting amplifier input stage is shown with the simplest form of resistive divider biasing. The value of the divider resistance R is not critical and may be increased above the 10kΩ value shown as long as the bias current does not interfere with accuracy due to DC loading error. However the divider junction must be kept at a low AC impedance This is the purpose of bypass

capacitor C_S. Its use provides transient suppression for signals coming from the supply bus. A low cost 0.1μF ceramic disk or chip capacitor is recommended for suppressing fast transients in the microsecond and sub-microsecond region.
Foil capacitors are simply too inductive for any high frequency bypass application and should be avoided. If low frequency noise such as 60Hz or 120Hz ripple is present on the supply bus, an electrolytic capacitor is added in parallel as shown. The common-mode input source resistance, R_S, should also be matched within a reasonable tolerance for maximizing the rejection of induced AC noise.

The output of the first stage is now fixed at the common mode bias voltage and the amplified AC signal is referenced to this constant value. Capacitive coupling to the inverting input is of course required to prevent the bias voltage from being multiplied by the stage gain. Second stage biasing may now be provided by the output voltage of the first stage if non-inverting operation is used in the former. For lowest noise in a high gain input stage, the magnitude of the input source resistance is critical; low values of resistance are preferred over high values to minimize thermally generated noise.

Non-Inverting Stage Biasing

Non-inverting operation of an amplifier stage with single supply is similar to the previous example but the bias resistor R_S must now be sufficiently high to allow the signal to pass
without significant attenuation. The input source resistance reflects the output resistance of the preceding stage or other sourcing device such as a bridge circuit of relatively high impedance. A simple rule of thumb is to make the bias resistor an order of magnitude larger than the generator resistance. Again the feed back network must be terminated capacitively. In this case R1 and the generator resistance should be matched and then R_S is matched to the feedback resistance ,R_F.

In all cases proper bypassing of the NE5234 supply leads (Pins 4 and 11) is very important particularly in a high noise environment. Bypass capacitors must be of ceramic construction with the shortest possible leads to keep inductance low. Chip capacitors are superior in this respect complimenting the increased use of surface mounted integrated devices. Note that both the NE5234D and the automotive grade SA5234D are available and are the surface mount versions of the device.

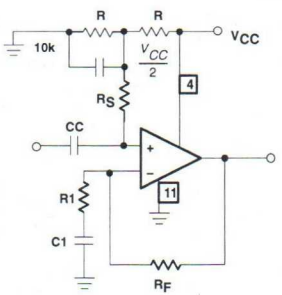


Figure 15. Non-Inverting Biasing

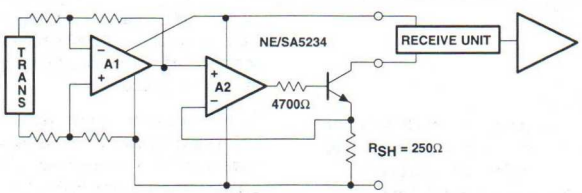
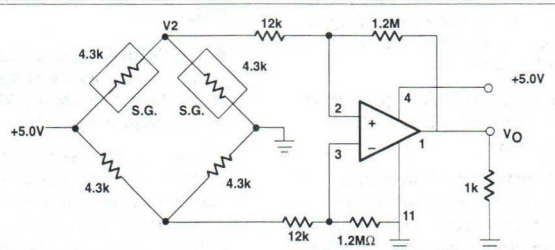


Figure 16. A 4-20mA Current Loop



$\lvert V_2 - V_1 \rvert$	V_O
5.9mV	0.5V
25.6mV	2.50V
46.6mV	4.63V

S.G.: Matched Strain Gauge elements

Figure 17. Strain Gauge Amplifier

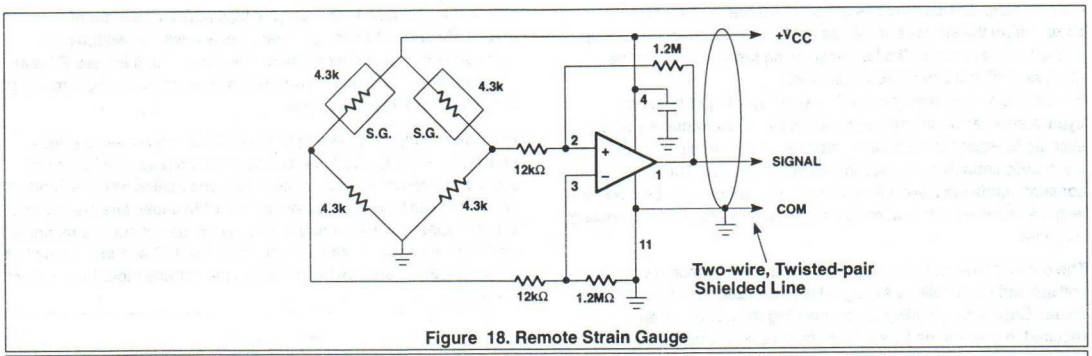


Figure 18. Remote Strain Gauge

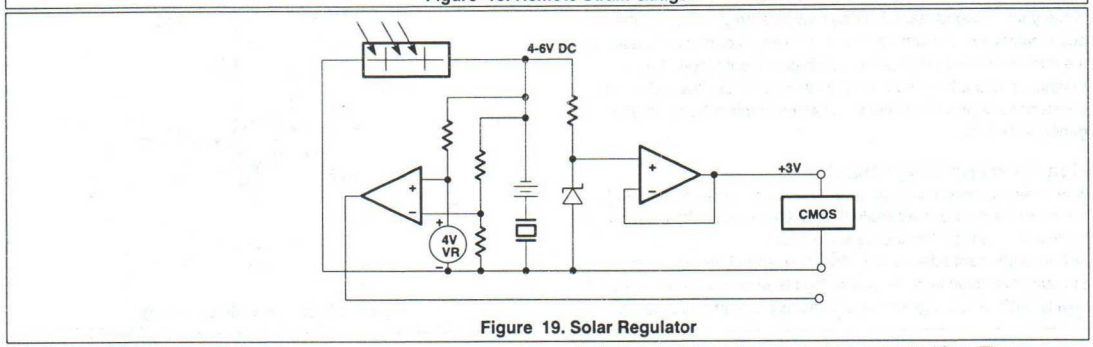


Figure 19. Solar Regulator

APPLICATIONS EXAMPLES

Instrumentation

Strain Gauge Bridge Amplifier

The circuit below shows a simple strain gauge circuit with a gain of 100 (40dB) and operated from a single supply. The chart illustrates the transfer function of the circuit for a single order-of-magnitude signal differential range from the bridge beginning with 5mV up to 50mV. The circuit is operated from a single 5V supply, but could equally as well be configured to use a dual balanced supply. It is immediately evident that the wide common-mode output range of the NE5234 is very advantageous in handling this wide range of signals with good linearity due to this feature.

A variation on this particular idea is the remote strain gauge circuit operating from a three wire line, one of which is the shield. This full-differential input circuit has balanced

input resistance to afford good common-mode noise rejection characteristics. Resistors are metal film or deposited carbon. Supply leads must be carefully bypassed close to the NE/SA5234 with ceramic or chip monolithic capacitors to give optimum noise performance. As shown, an auxiliary sub-regulator may be added to improve the overall DC stability of the bridge signal voltage. A regulator capable of providing the necessary few milliamperes at somewhat reduced voltage for the transducer is shown in one of the following examples. This makes use of one of the op amps in the same device package to provide the voltage regulation. Note that the use of multiple op amps within a single package minimizes the possibility of thermal drift and mismatched response from various DC parameters.

Multiple sets of transducers may be constructed from The NE/SA5234 or the NE5234D surface mount device to form a compact and stable instrumentation package. This is useful for transducer applications in

the measurement of pressure, strain, position and temperature, which have similar circuit configurations. First order temperature compensation of the transducers such as semiconductor strain gauges, or resistive units may be achieved by using one of the gauges as a reference device only. It is thermally coupled to the same member as the active gauge, as shown in the example. (Figure 18)

A 4 to 20mA Current Loop

Some instrumentation installations require the 4-20mA current loop. This addition to the above bridge transducer circuit examples is demonstrated in Figure 16.

This circuit makes use of the remote transducer bridge previously described and adds current loop signaling capability. The voltage-to-current converter consists of an additional op amp from the same NE/SA5234 package combined with a single transistor to drive the current loop. The sensitivity is actually in mA/V, or transconductance, which is equal to $1/R_{SH}$. This sensitivity in this particular example is set to 4mA/V. Thus, with a bridge amplifier having a differential gain of 100, an input of 10mV will produce a 4mA output current and 50mV will produce a 20mA output. Of course the line resistance plus receiver resistance must be within the voltage compliance range of the supply voltage to guarantee linear operation over the total range. A negative supply may be used if it is preferred to have the current loop referenced to ground.

DC Regulators and Servos

Closely related to DC and low frequency AC linear transducers are DC regulators and servo circuits. The proliferation of many battery, and solar powered remote instrumentation packages results in a need for adaptable circuits which may readily be made up from existing stock ICs. The examples given here are quite simple, but can be very useful to the designer when economy and size are at a premium.

Solar Regulator for 3-Volt CMOS

Working with small instrumentation packages which are to operate from solar photovoltaic cells may bring a need for simple sub-regulators for MOS circuits requiring only a few milliamperes of drain current. Figure 19 shows a simple low voltage regulator making use of the particularly excellent DC characteristics of the NE/SA5234. The regulator becomes an integral part of any functional analog signal processing package such as an environmental data instrumentation unit. The low current drain of the the typical 3V or 5V MOS digital IC allows one sub regulator to serve up to 10 or more such devices. If the instrument package is to be subjected to wide temperature variations, the SA5234 is recommended. A second op amp in the package may serve as a low battery alarm with tone modulator as in radio links, or simple logic level comparator. Overcurrent protection is easily added within the regulator loop to detect short circuit failures and automatically limit the current.

DC Servo-amps

Servo control systems for low voltage motor drives require high gain-accuracy and good DC stability for many applications. Applications such as the position control of air flow vanes, servo valves, and optical lenses or apertures, are typical examples. Figure 20 demonstrates one simple DC motor servo application with position control feedback. The motor is a 3V permanent magnet rotor type used in micro-position applications and is adaptable to battery supply environments.

Position information is received from a multi-turn potentiometer to give adequate resolution. The input voltage may be generated from another potentiometer which is remote from the motor drive unit proper, or from a D/A converter output for micro processor controlled systems. The input voltage range is 1.0 to 3.0V and the supply voltage is 4.5V.

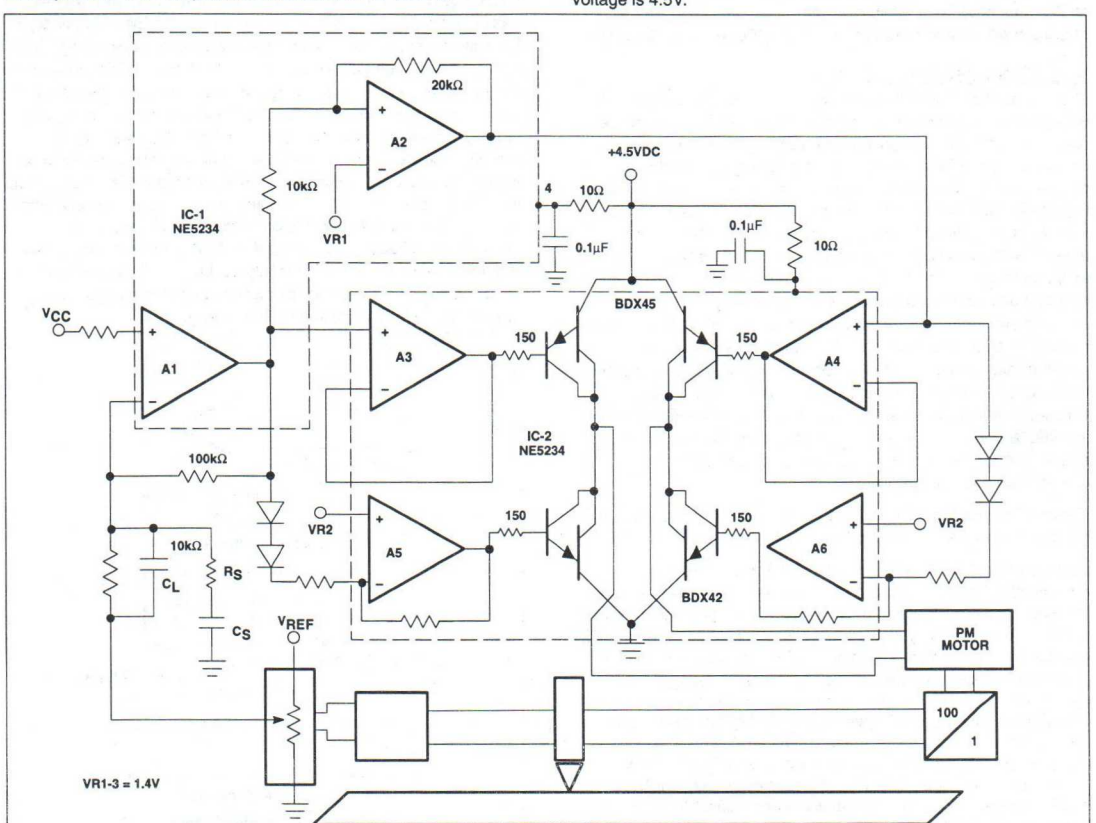


Figure 20. Full Bridge Motor Drive

Using the NE/SA5234 amplifier AN1651

Active filters

The NE5234 is easily adapted to use in a variety of active filter applications. Its high open-loop gain and excellent unity gain stability make it ideal for high-pass, band-pass and low-pass configurations operated with low voltage single supplies. Its low output impedance also makes it capable of obtaining low noise operation without resorting to separate high current buffers.

Figure 21a shows the circuit for a VCVS low-pass filter with dual supply biasing and 600Ω output termination. Figure 21b is a band-pass filter with AC coupled gain network for single supply operation.

Communications and Audio

Stereo Bridge Amplifier

Figure 22 shows two NE5234 ICs in a bridge amplifier application. The choice of split supplies allows DC coupling, both from the input signal source and to the load. The gain is set to a nominal 20dB. Either inverting or non-inverting operation is available. The inverting input impedance is chosen as 600Ω in order to match standard audio impedance lines within a system. The use of two such amplifiers will provide stereo operation to +10dBm for a 600Ω load.

Voice Operated Microphone

The processing of voice transmissions for communications channels is generally coupled with the need for keeping the signal-to-noise ratio high and the intelligibility optimized for a given channel bandwidth. In addition, when a circuit is battery operated and portable, the requirement to obtain maximum battery life becomes important. The circuit example shown here is aimed at filling the need for a portable voice operated transmitter, cordless phone, or tape recorder. It utilizes the Philips Semiconductors NE5234 quad op amp in conjunction with the new low-voltage NE578 compandor to create an audio processor capable of operating in just such an environment. Both devices are operational to a low battery voltage of 2.0V. In addition the design further conserves current by automatically shifting the NE578 compandor to standby during the period when no transmissions are being made. Total current consumption at 3.0V is 2.8mA for the NE5234. In the active mode the NE578 draws 1.4mA and this drops to 170µA in the standby mode. This amounts to reducing the supply current demand by approximately 25% in the 'listen mode'.

Figure 23 shows the VOX audio circuit example. A description of its operation for voice activated transmission follows.

Audio generated by the electret microphone is fed into the non-inverting input of preamp A1 and the signal amplified by 12dB. The biasing is accomplished by the resistive divider which provides a level of half the supply voltage which is connected through a 100k resistor to the non-inverting terminal of A1. This automatically provides ratiometric common mode biasing set at $V_{CC}/2$ for the device. This level is then transferred directly to the following amplifier, A2, setting its DC operating point. The DC gain of both stage A1 and A2 are unity so the cumulative DC error is not multiplied by stage gain. The peak voice level is approximately $100mV_{RMS}$ at the input to A1 from the microphone and this is boosted to $400mV_{RMS}$. The feedback network gain has a low frequency corner at 160Hz and is flat up to the intersection of the closed loop gain with the open loop gain curve at nearly 500kHz. This would increase the noise bandwidth to an excessive degree unnecessary for voice channel communication. A band limiting network is, therefore, inserted across the feedback resistor to limit response to a nominal 5kHz.

Amplifier stage A2 is used to provide high level audio to the rectifier-filter stage for the rapid generation of a DC control signal for operating the voice activated switch function. Stage A2 gain is set to 20dB in order to allow activation of the voice channel on the rising edge of the first voice syllable. An attack time of 20ms is implemented by adjusting the input charging impedance (R_S) between the rectifier and the A2 amplifier output. AC coupling must be used to isolate the DC common-mode voltage of the amplifier from the rectifier/storage capacitor and to allow only audio frequencies to drive the switching circuit. Amplifier A3 provides a high impedance unity gain buffer to allow a very slow decay rate to be applied to the time constant capacitor, C_T. The output of the storage capacitor reaches approximately 3.2V for a 250ms duration 600Hz burst signal. Diode D1 (1N914) provides a negative clamp action which forces the full peak-to-peak voltage from A2 to charge the storage capacitor. D2 then acts to charge the capacitor to the peak input voltage minus one diode drop, 0.7V. Finally, the buffered DC control signal is fed to A4 which acts as a threshold comparator with extremely high gain and controlled hysteresis. This provides a positive going signal for releasing the NE578 from its inhibit mode when voice input is present. The NE578 is switched from standby mode when voice input is present. The NE578 is switched from standby mode to the active state by raising the voltage on Pin 8 of the device above 2V. Shutting the audio channel off requires this pin to be driven below 100mV. This demands the extremely wide output voltage swing of the NE5234 in order to reach this near to the negative rail voltage. The voltage threshold of the comparator, A4, is adjustable by use of the sensitivity control, R_S. It is used to allow the activation level to be raised or lowered depending upon the ambient audio level in the transmitter vicinity.

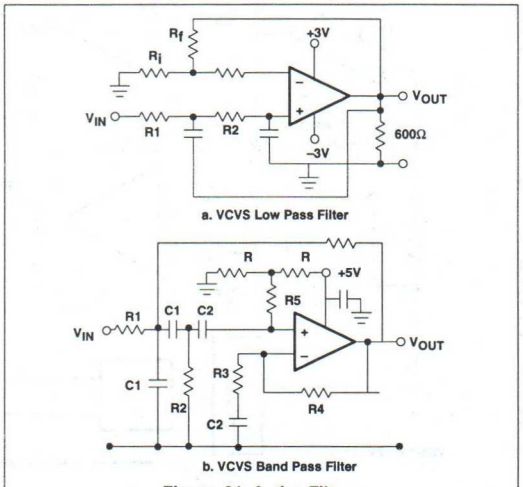


Figure 21. Active Filters

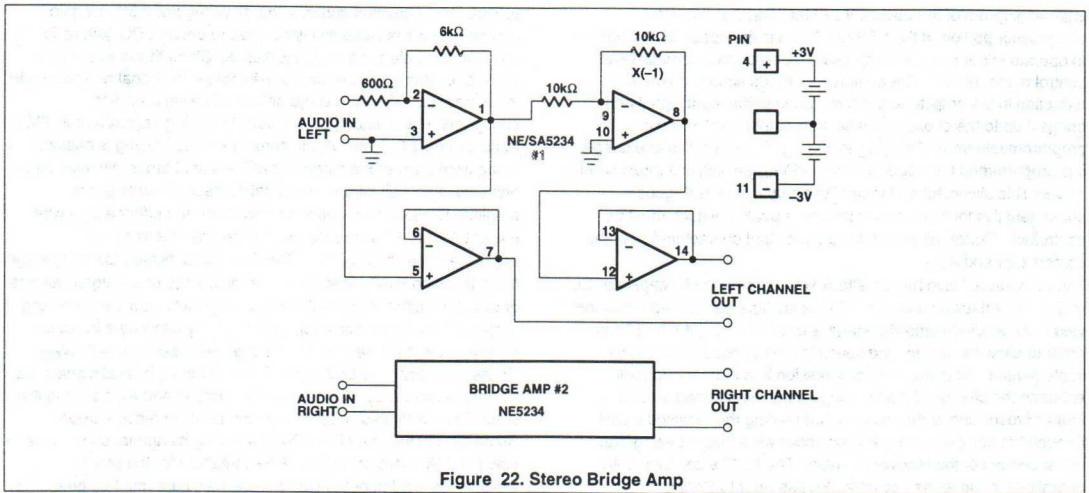


Figure 22. Stereo Bridge Amp

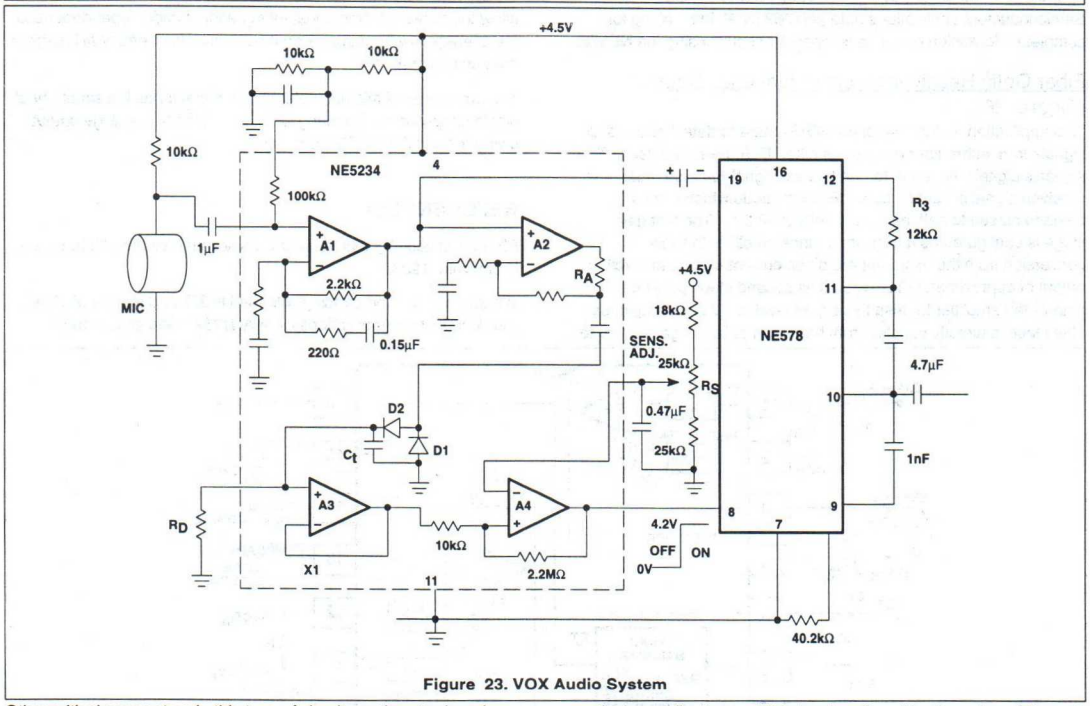


Figure 23. VOX Audio System

Other critical parameters in this type of circuit are the attack and decay times of the RC network which controls the operation of the voice operated switch. Attack time determines how quickly the circuit activates after a quiet period, and the decay time sets how long the transmitter channel stays active between words. It is important to reach an optimum balance between the two time constants in order to allow unbroken transmissions of good quality and no lost syllables. A 100 to 1 attack/decay ratio is used in this particular application and this is primarily set by the value of R_A and R_D. A typical delay of two seconds is easily accomplished. Due to extremely high input impedance of the buffer stage A3, R_D may be in the 1 to 2MΩ range allowing a reasonable value of storage capacitor to be used.

The Audio Channel

Audio input from the preamplifier, A1, is fed directly to Pin 14 of the NE578 compandor. Referring to Figure 24, which shows the

internal diagram of the device, it can be seen that this is the compressor portion of the NE578. There is the option in this system to operate either in a 2:1 compressor mode or an automatic level control mode, (ALC). The compressor mode simply makes a 2:1 reduction in the amplitude dynamic range of the input signal and brings it up to the chosen nominal 0dB output level which is programmable from $10mV_{RMS}$ to $1V_{RMS}$. In this particular example it is programmed for a 0dB level of $0.42V_{RMS}$ which is approximately $1V_{P-P}$. This allows for a standardized output level with good characteristics for FM modulation where peak deviation must be controlled. Figure 25 shows the input-output characteristics of the compressor and ALC.

The compressor also has an attack time determined by capacitor C6 on Pin 11. Attack time is 10k * C6, decay time equals four times this value. An auxiliary amplifier stage is used following the NE578 in order to allow bandwidth and special forms of equalization to be implemented. Note that 2:1 compression in a transmission will enhance the channel dynamic range and may be used with no further processing at the receiver, but feeding the received signal through the complimentary 2:1 expandor will achieve even greater enhancement of the recovered audio. The NE578 contains both operations in the same package. Please refer to Philips Semiconductors applications note AN1762 by Alvin K. Wong for complete information on these compandor circuits using the NE578.

Fiber Optic Receiver for Low Frequency Data (Figure 26)

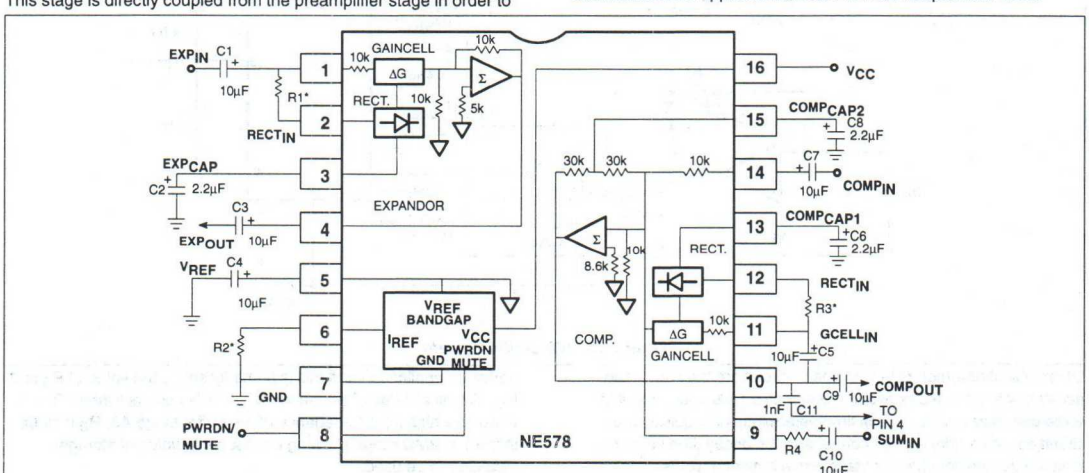
This application makes use of the NE/SA5234 to detect photo-optic signals from either fiber or air transmitted IR (Infra-red) pulses. The signal is digitally encoded for the highest signal-to-noise ratio. The received signal is sensed by an IR photo diode which has its cathode biased to half the supply voltage (2.5V). The first gain stage is configured as a transimpedance amplifier to allow conversion from the microampere diode current signals to a voltage output of approximately $10mV_{0-P}$. The second stage provides a gain-of-ten amplifier to raise this signal level to 1V peak amplitude. This stage is directly coupled from the preamplifier stage in order to provide the necessary common-mode voltage of 2.5V. Its gain control network is capacitively coupled to prevent DC gain as is required in single supply configurations. Since this is essentially a pulse gain stage, low frequency gain below the signal repetition rate is not needed. The third stage acts in a limiting amplifier configuration and its output is squared to swing approximately 5V, the standard TTL level. Again common-mode biasing is passed along from each of the stages up to the last in order minimize parts and simplify circuit layout. The final stage is a simple buffer amplifier to allow the receiver to drive a low impedance long wire line of 600Ω to 900Ω resistance. Some rise time response adjustment may be required. This is easily achieved following stage three by using R_T-C_T to limit the rate of change of the signal voltage prior to the buffer. Note that the last stage acts as a zero-crossing detector. This maximizes noise immunity by allowing a transition only after the third stage output voltage has risen above $2/3V_{CC}$. Phase inversion may be accomplished, if the logic level signals are polarity reversed, by making stage 3 inverting and AC coupling the input signal with a sufficiently large capacitor to reduce droop. Stage 3 must then be biased by connecting its non-inverting node to bias point 'A'. This provides a 2.5V threshold for the proper switching operation of the stage. However, care must be taken not allow the network's time constant to become code dependent as to the average low frequency signal components or errors will result in the output signal.

The advantage of this particular circuit is that it has the simplicity of single supply operation along with the capability of a large output swing making it fully TTL compatible

REFERENCES:

Philips Semiconductors. Linear Data Manual, Volume 2 : Industrial. Sunnyvale: 1988.

Wong, Alvin K. Companding with the NE577 and NE578..Philips Semiconductors Applications Note AN1762 : September 1990.



*R1, R2 and R3 are 1% resistors.

Figure 24. Block Diagram of NE578 Test and Application Circuit

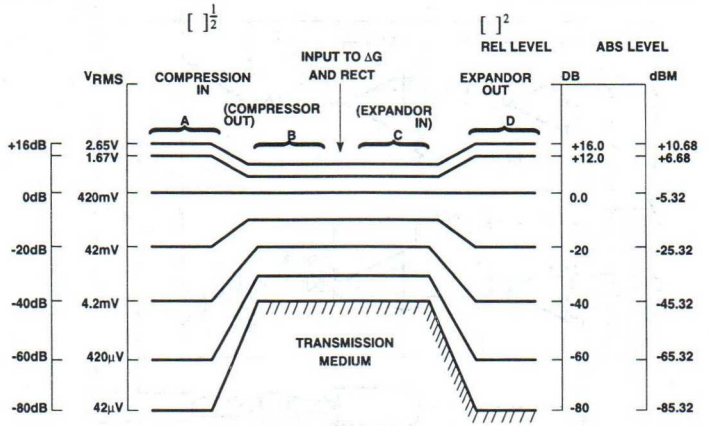


Figure 25. NE570/571/SA571 System Level

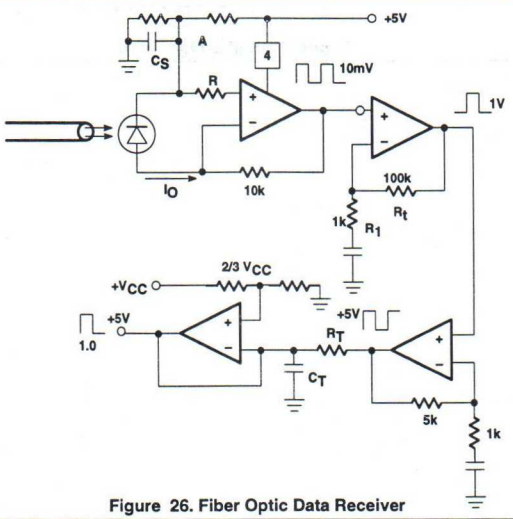


Figure 26. Fiber Optic Data Receiver

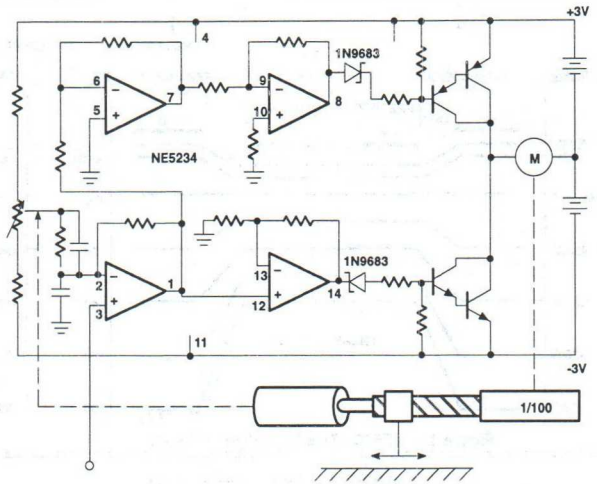


Figure 27. Half Bridge Servo

Section 3
High Frequency/Video Amplifiers

INDEX

NE/SA5204A	Wide-band high-frequency amplifier	181
NE/SA/SE5205A	Wide-band high-frequency amplifier	192
NE/SA5209	Wideband variable gain amplifier	202
NE/SA5219	Wideband variable gain amplifier	216
NE/SE5539	High frequency operational amplifier	229
AN140	Compensation techniques for use with the NE/SE5539	237
NE5592	Video amplifier	245
NE592	Video amplifier	250
AN141	Using the NE/SA/SE592 video amplifier	258
µA733/733C	Differential video amplifier	262

Wide-band high-frequency amplifier — NE/SA5204A

DESCRIPTION

The NE/SA5204A family of wideband amplifiers replaces the NE/SA5204 family. The 'A' parts are fabricated on a rugged 2µm bipolar process featuring excellent statistical process control. Electrical performance is nomically identical to the original parts.

The NE/SA5204A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 200MHz. The -3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The NE/SA5204A operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The NE/SA5204A is a relaxed version of the NE5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA5204A solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

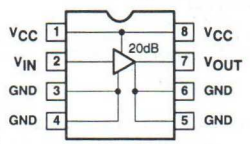
Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

No external components are needed other than AC-coupling capacitors because the NE/SA5204A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA5204As in series as required, without any degradation in amplifier stability.

PIN CONFIGURATION

N, D Packages



TOP VIEW

FEATURES

- Bandwidth (min.)
  200 MHz, ±0.5dB
  350 MHz, -3dB
- 20dB insertion gain
- 4.8dB (6dB) noise figure Z_O=75Ω (Z_O=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface-mount package available
- Cascadable
- 2000V ESD protection

APPLICATIONS

- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broadband LANs
- Networks
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

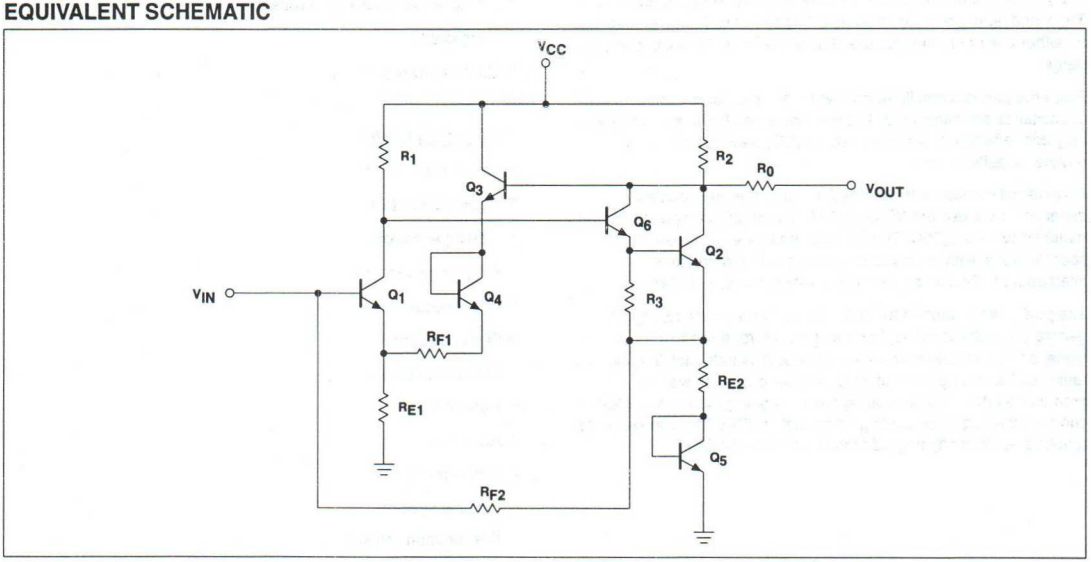
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5204AN	0404B
8-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5204AD	0174C
8-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA5204AN	0404B
8-Pin Plastic Small Outline (SO) package	–40 to +85°C	SA5204AD	0174C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{IN}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	–40 to +85	°C
P_{DMAX}	Maximum power dissipation[1, 2] T_A=25°C(still–air)		
	N package	1160	mW
	D package	780	mW
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	–55 to +150	°C
T_{SOLD}	Lead temperature (soldering 60s)	300	°C

NOTES:
1. Derate above 25°C, at the following rates
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. See "Power Dissipation Considerations" section.

EQUIVALENT SCHEMATIC



Wide-band high-frequency amplifier — NE/SA5204A

DC ELECTRICAL CHARACTERISTICS

V_{CC}=6V, Z_S=Z_L=Z_O=50Ω and T_A=25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5		8	V
I_{CC}	Supply current	Over temperature	19	25	33	mA
S21	Insertion gain	f=100MHz, over temperature	16	19	22	dB
S11	Input return loss	f=100MHz		25		dB
		DC –550MHz		12		
S22	Output return loss	f=100MHz		27		dB
		DC –550MHz		12		
S12	Isolation	f=100MHz		–25		dB
		DC –550MHz		–18		
BW	Bandwidth	±0.5dB	200	350		MHz
BW	Bandwidth	–3dB	350	550		MHz
	Noise figure (75Ω)	f=100MHz		4.8		dB
	Noise figure (50Ω)	f=100MHz		6.0		dB
	Saturated output power	f=100MHz		+7.0		dBm
	1dB gain compression	f=100MHz		+4.0		dBm
	Third–order intermodulation intercept (output)	f=100MHz		+17		dBm
	Second–order intermodulation intercept (output)	f=100MHz		+24		dBm
t_R	Rise time			500		ps
t_P	Propagation delay			500		ps

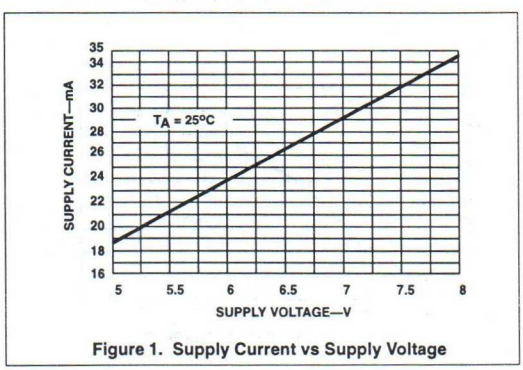


Figure 1. Supply Current vs Supply Voltage

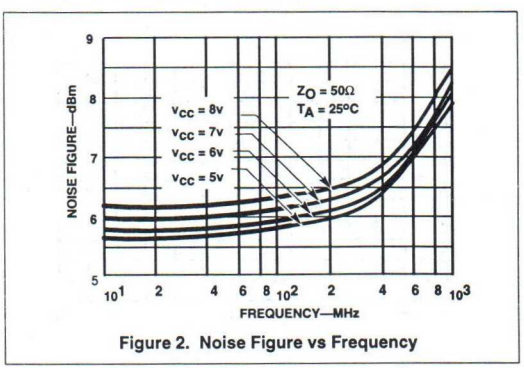


Figure 2. Noise Figure vs Frequency

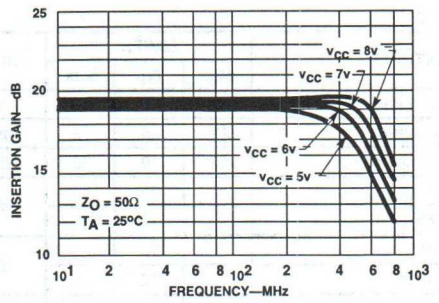


Figure 3. Insertion Gain vs Frequency (S_{21})

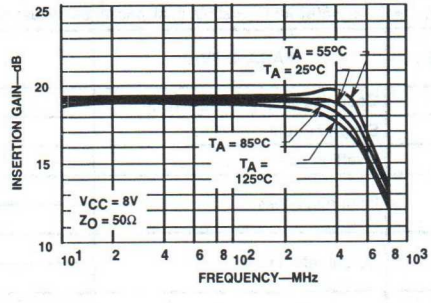


Figure 4. Insertion Gain vs Frequency (S_{21})

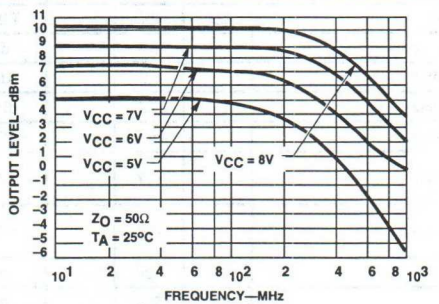


Figure 5. Saturated Output Power vs Frequency

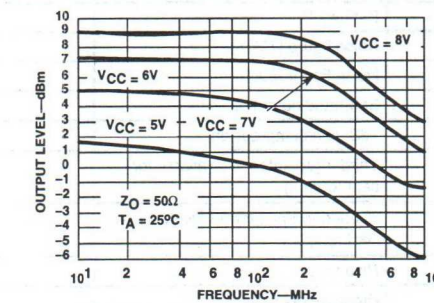


Figure 6. 1dB Gain Compression vs Frequency

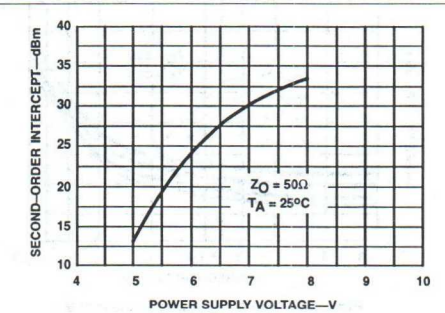


Figure 7. Second-Order Output Intercept vs Supply Voltage

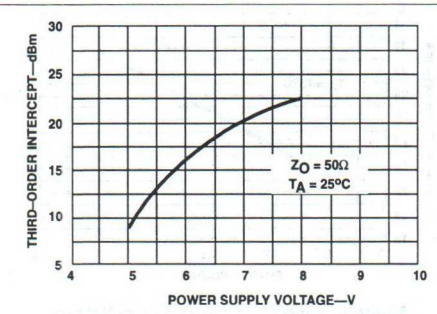


Figure 8. Third-Order Intercept vs Supply Voltage

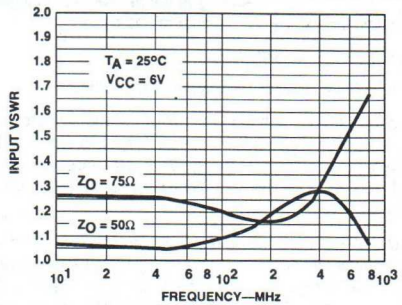


Figure 9. Input VSWR vs Frequency

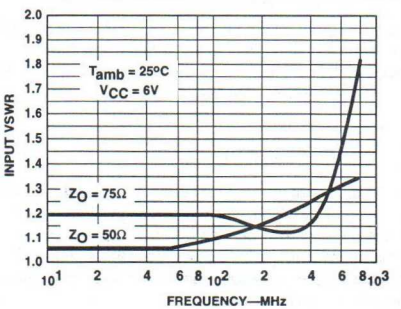


Figure 10. Output VSWR vs Frequency

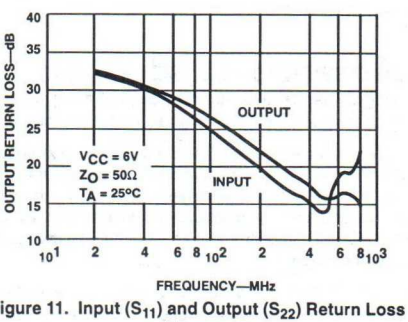


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

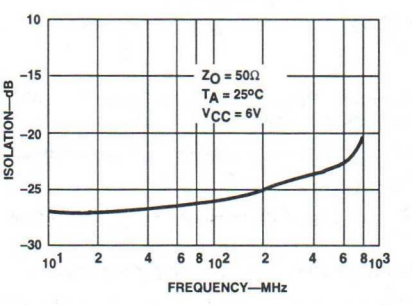


Figure 12. Isolation vs Frequency (S_{12})

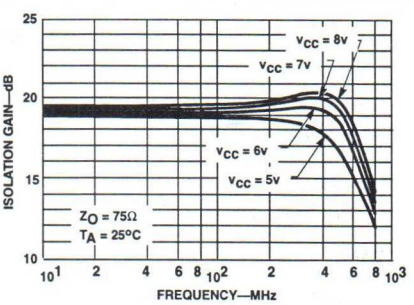


Figure 13. Insertion Gain vs Frequency (S_{21})

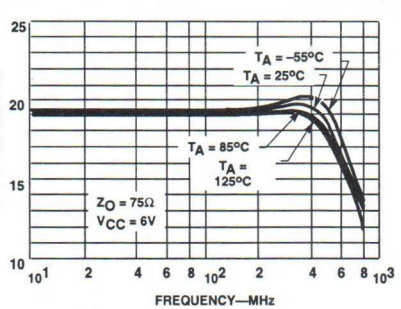


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1}) / R_{E1} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wide-band terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible, while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10Log\left[1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_O}\right] dB \quad (2)$$

where I_{C1}=5.5mA, R_{E1}=12Ω, r_b=130Ω, KT/q=26mV at 25°C and R_0=50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN}=V_{BE1}+(I_{C1}+I_{C3})\ R_{E1} \quad (3)$$

where R_{E1}=12Ω, V_{BE}=0.8V, I_{C1}=5mA and I_{C3}=7mA (currents rated at V_{CC}=6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4, which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt-feedback loading on the output. The value of R_{F1}=140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT}=V_{CC}-(I_{C2}+I_{C6})R2, \quad (4)$$

where V_{CC}=6V, R_2=225Ω, I_{C2}=8mA and I_{C6}=5mA.

From here, it can be seen that the output voltage is approximately 3.1V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (32mA max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat-sinking benefits can be realized by mounting the SO and N package bodies against the PC board plane.

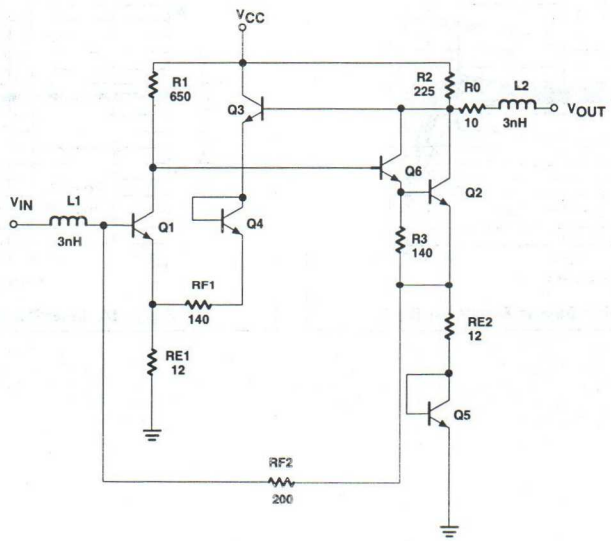


Figure 15. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5204A to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible, and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC-coupled. This is because at V_{CC}=6V, the input is approximately at 1V while the output is at 3.1V. The output must be decoupled into a low-impedance system, or the DC bias on the output of the amplifier will be loaded down, causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high-frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the NE5204A are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier, and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.

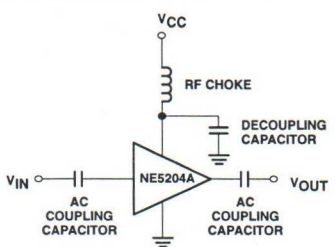


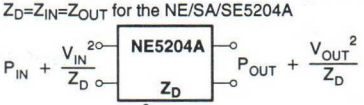
Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5204A to other high-frequency amplifiers.

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D=Z_{IN}=Z_{OUT}$ for the NE/SA/SE5204A



$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$$P_I = V_I^2$$

P_I=Insertion Power Gain

V_I=Insertion Voltage Gain

Measured value for the NE/SA/SE5204A = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

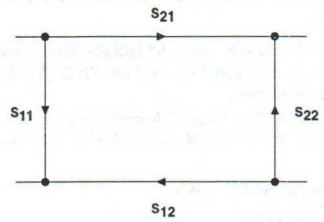
$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20\text{dB}$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:



a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} = \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OSOLATION

$$S_{12} = \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

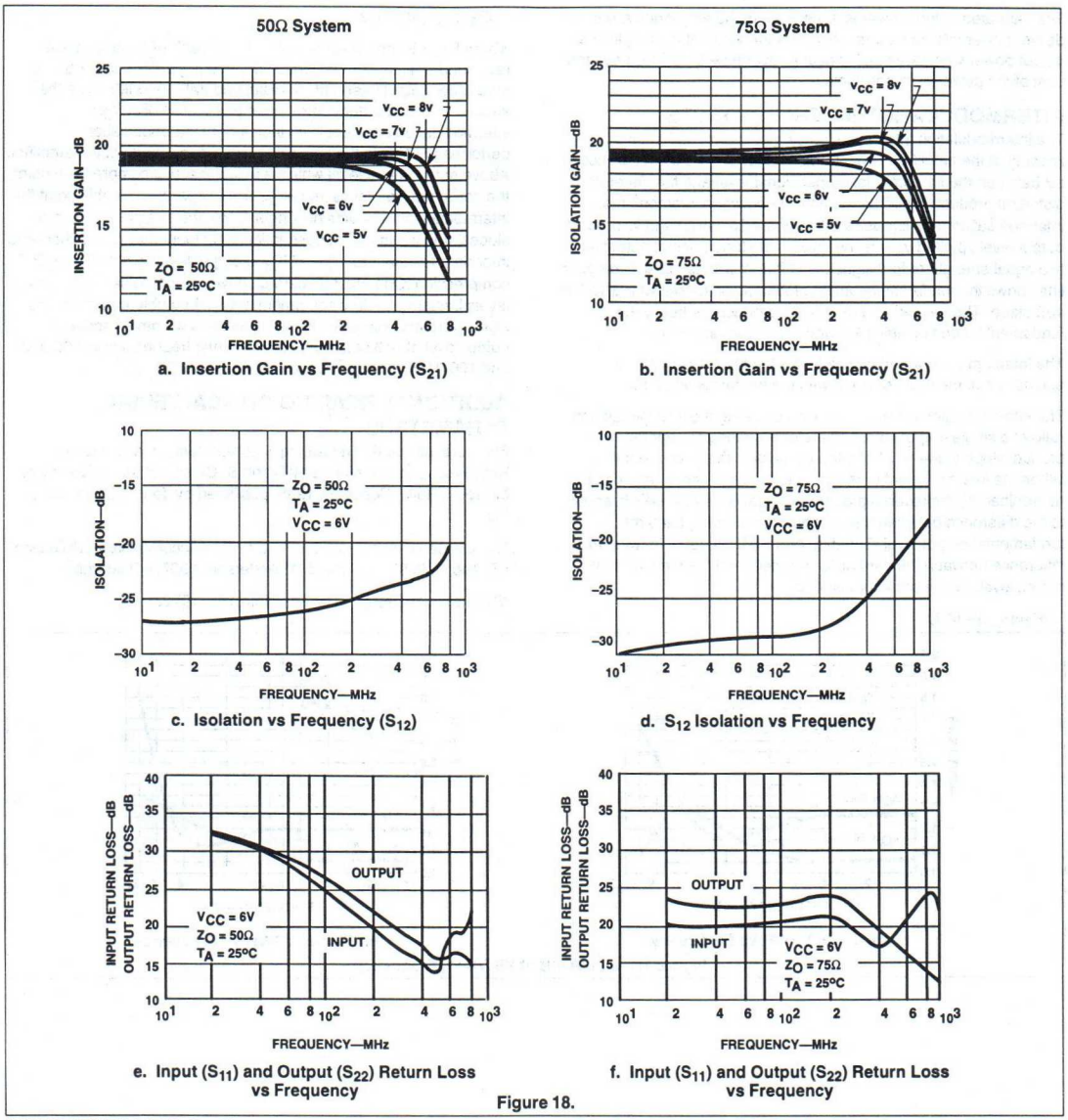
$$S_{21} = \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} = \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

b.

Figure 17.



a. Insertion Gain vs Frequency (S_{21})

b. Insertion Gain vs Frequency (S_{21})

c. Isolation vs Frequency (S_{12})

d. S_{12} Isolation vs Frequency

e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18.

INPUT RETURN LOSS=S_{11}dB
S_{11}dB=20 Log | S_{11} |

OUTPUT RETURN LOSS=S_{22}dB
S_{22}dB=20 Log | S_{22} |

INPUT VSWR=≤1.5

OUTPUT VSWR=≤1.5

1DB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$IP_2=P_{OUT}+IMR_2$

$IP_3=P_{OUT}+IMR_3/2$

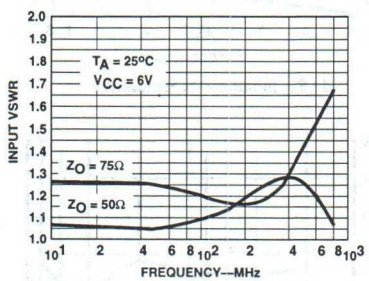
where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA5204A we have chosen an output level of –10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.

ADDITIONAL READING ON SCATTERING PARAMETERS

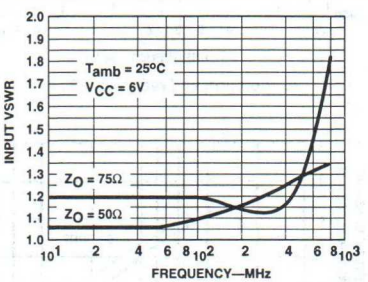
For more information regarding S-parameters, please refer to High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.



a. Input VSWR vs Frequency



b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

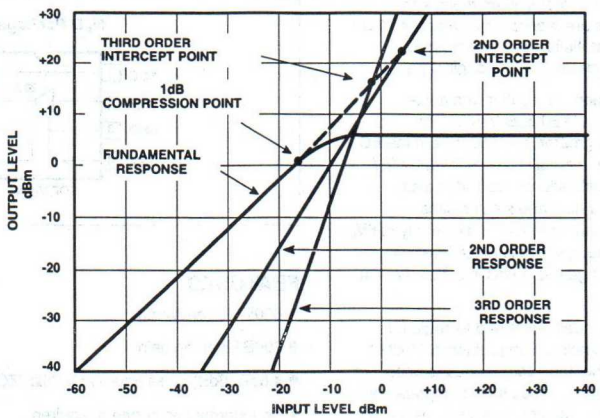

THIRD ORDER
INTERCEPT POINT
2ND ORDER
INTERCEPT
POINT
1dB
COMPRESSION POINT
FUNDAMENTAL
RESPONSE
2ND ORDER
RESPONSE
3RD ORDER
RESPONSE
OUTPUT LEVEL
dBm
+30
+20
+10
0
-10
-20
-30
-40
-60
-50
-40
-30
-20
-10
0
+10
+20
+30
+40
INPUT LEVEL dBm

Figure 20.

Wide-band high-frequency amplifier — NE/SA/SE5205A

DESCRIPTION

The NE/SA/SE5205A family of wideband amplifiers replace the NE/SA/SE5205 family. The 'A' parts are fabricated on a rugged 2µm bipolar process featuring excellent statistical process control. Electrical performance is nominally identical to the original parts.

The NE/SA/SE5205A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the -3dB bandwidth is greater than 600MHz in the EC package. This performance makes the amplifier ideal for cable TV applications. For lower frequency applications, the part is also available in industrial standard dual in-line and small outline packages. The NE/SA/SE5205A operates with a single supply of 6V, and only draws 24mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA/SE5205A solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the -3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

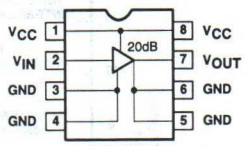
No external components are needed other than AC coupling capacitors because the NE/SA/SE5205A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA/SE5205As in series as required, without any degradation in amplifier stability.

PIN CONFIGURATIONS

N, D Packages



TOP VIEW

FEATURES

- 600MHz bandwidth
- 20dB insertion gain
- 4.8dB (6dB) noise figure ZO=75Ω (ZO=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface mount package available
- MIL-STD processing available
- 2000V ESD protection

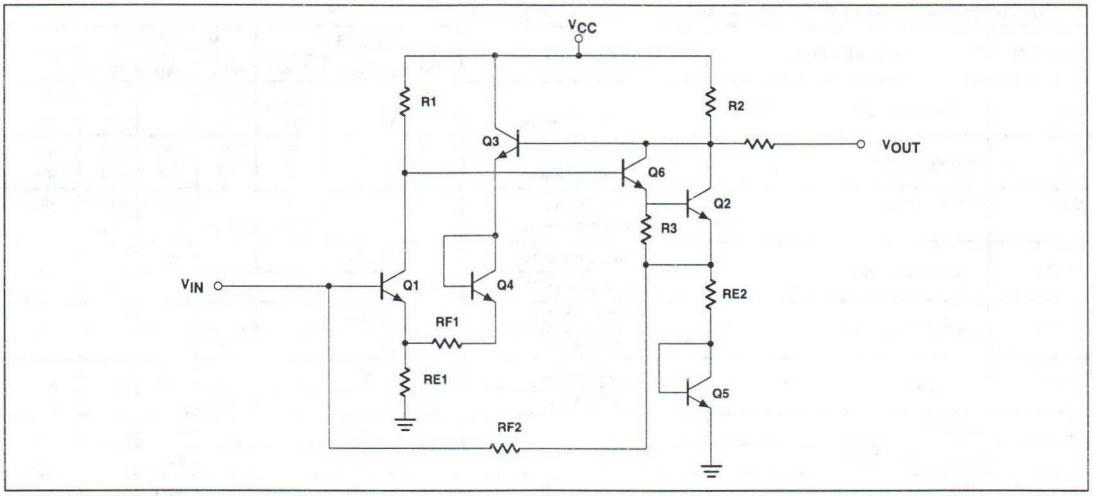
APPLICATIONS

- 75Ω cable TV decoder boxes
- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broad-band LANs
- Fiber-optics
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5205AD	0174
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5205AN	0404
8-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5205AD	0174
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5205AN	0404
8-Pin Plastic Dual In-Line Package (DIP)	-55 to +125°C	SE5205AN	0404

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{AC}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	-40 to +85	°C
	SE grade	-55 to +125	°C
P_{DMAX}	Maximum power dissipation, T_A=25°C (still-air)[1, 2]		
	N package	1160	mW
	D package	780	mW

NOTES:
1. Derate above 25°C, at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. See "Power Dissipation Considerations" section.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=6V, Z_S=Z_L=Z_O=50Ω and T_A=25°C in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205A			NE/SA5205A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5 5		6.5 6.5	5 5		8 8	V V
I_{CC}	Supply current	Over temperature	20 19	25 25	32 33	20 19	25 25	32 33	mA mA
S21	Insertion gain	f=100MHz Over temperature	17 16.5	19	21 21.5	17 16.5	19	21 21.5	dB
S11	Input return loss	f=100MHz D, N		25			25		dB
		DC - f_{MAX} D, N	12			12			
S22	Output return loss	f=100MHz D, N		27			27		dB
		DC - f_{MAX}	12			12			
S12	Isolation	f=100MHz		-25			-25		dB
		DC - f_{MAX}	-18			-18			
t_R	Rise time			500			500		ps
t_P	Propagation delay			500			500		ps
BW	Bandwidth	±0.5dB D, N		300			450		MHz
f_{MAX}	Bandwidth	-3dB D, N				550			MHz
	Noise figure (75Ω)	f=100MHz		4.8			4.8		dB
	Noise figure (50Ω)	f=100MHz		6.0			6.0		dB
	Saturated output power	f=100MHz		+7.0			+7.0		dBm
	1dB gain compression	f=100MHz		+4.0			+4.0		dBm
	Third-order intermodulation intercept (output)	f=100MHz		+17			+17		dBm
	Second-order intermodulation intercept (output)	f=100MHz		+24			+24		dBm

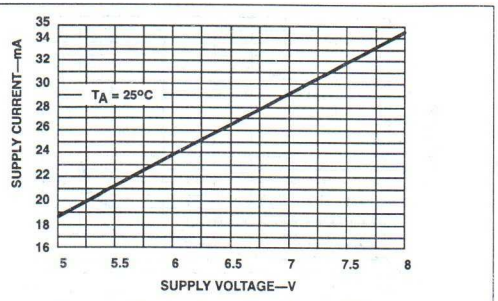


Figure 1. Supply Current vs Supply Voltage

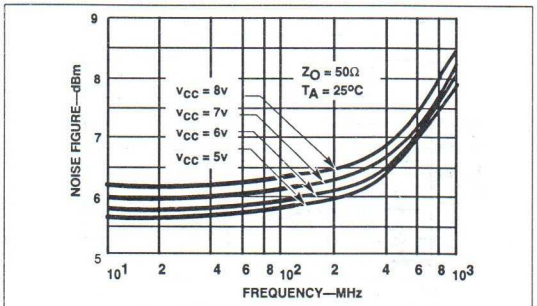


Figure 2. Noise Figure vs Frequency

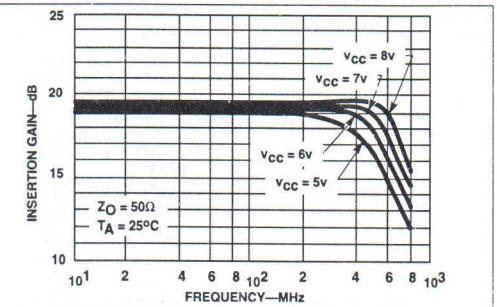


Figure 3. Insertion Gain vs Frequency (S_{21})

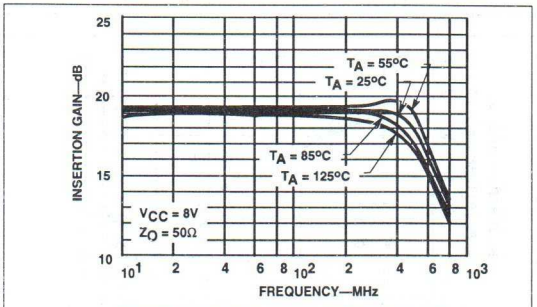


Figure 4. Insertion Gain vs Frequency (S_{21})

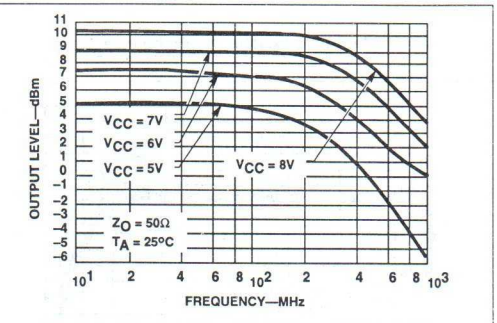


Figure 5. Saturated Output Power vs Frequency

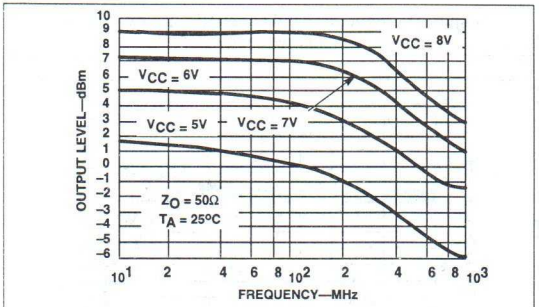


Figure 6. 1dB Gain Compression vs Frequency

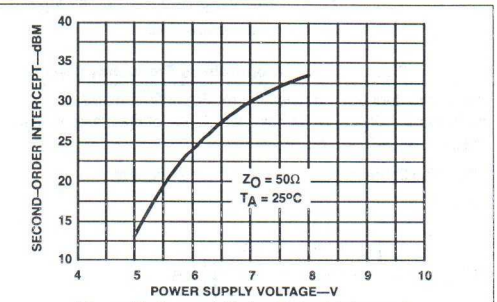


Figure 7. Second-Order Output Intercept vs Supply Voltage

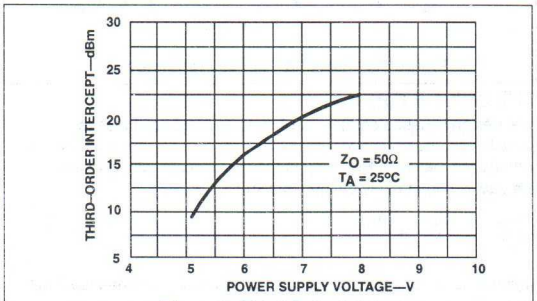


Figure 8. Third-Order Intercept vs Supply Voltage

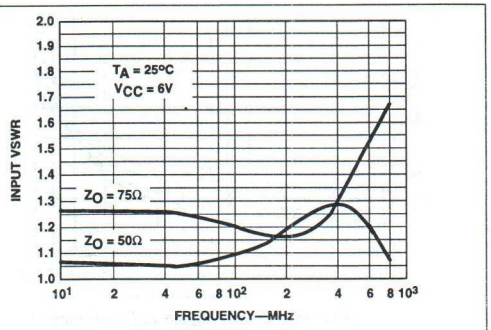


Figure 9. Input VSWR vs Frequency

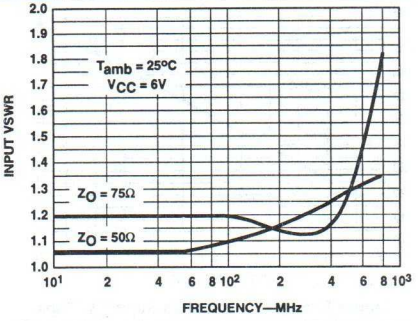


Figure 10. Output VSWR vs Frequency

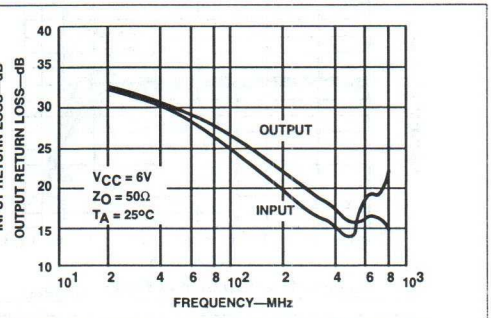


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

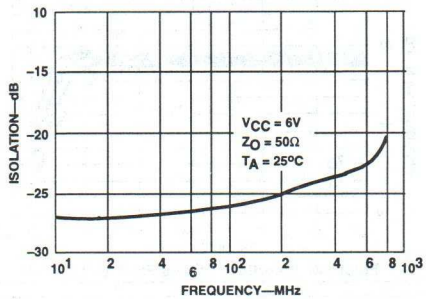


Figure 12. Isolation vs Frequency (S_{12})

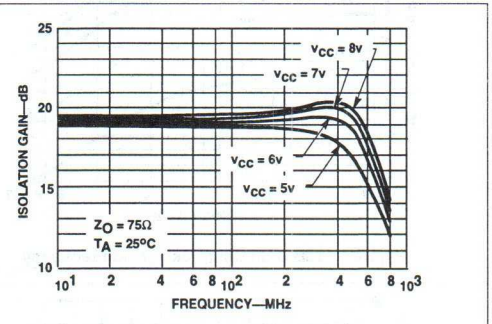


Figure 13. Insertion Gain vs Frequency (S_{21})

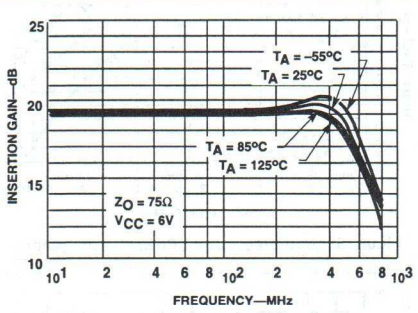


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = \frac{(R_{F1} + R_{E1})}{R_{E1}} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10 \log \left[1 + \left[\frac{r_b + R_{E1} + \frac{KT}{2qI_{C1}}}{R_O} \right] \right] dB \quad (2)$$

where I_{C1}=5.5mA, R_{E1}=12Ω, r_b=130Ω, KT/q=26mV at 25°C and R_0=50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN}=V_{BE1}+(I_{C1}+I_{C3})\ R_{E1}$$

where R_{E1}=12Ω, V_{BE}=0.8V, I_{C1}=5mA and I_{C3}=7mA (currents rated at V_{CC}=6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of R_{F1}=140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT}=V_{CC}-(I_{C2}+I_{C6})R2,(4)$$

where V_{CC}=6V, R_2=225Ω, I_{C2}=8mA and I_{C6}=5mA.

From here it can be seen that the output voltage is approximately 3.1V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

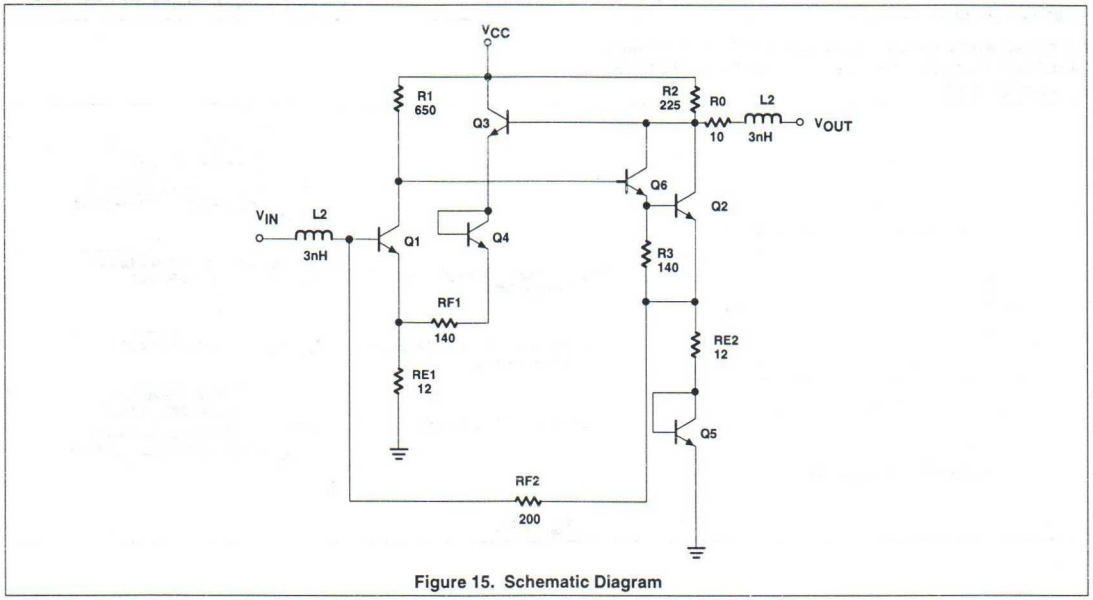


Figure 15. Schematic Diagram

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (32mA Max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the D package body against the PC board plane.

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5205A to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the SO package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection.

Another important consideration is that the input and output should be AC coupled. This is because at V_{CC}=6V, the input is approximately at 1V while the output is at 3.1V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the NE/SA/SE5205A are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5205A to other high-frequency amplifiers.

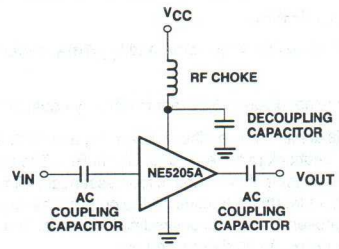
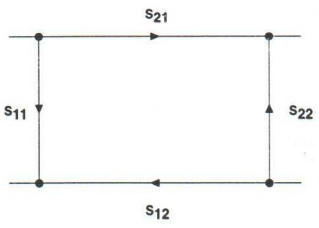


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling



a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} = \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS
OSOLATION

$$S_{12} = \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS
OR INSERTION GAIN

$$S_{21} = \sqrt{\text{TRANSDUCER POWER GAIN}}$$

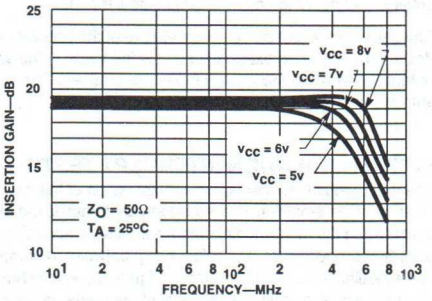
S_{22} — OUTPUT RETURN LOSS

$$S_{22} = \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

b.

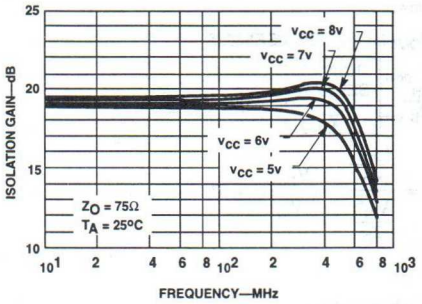
Figure 17.

50Ω System

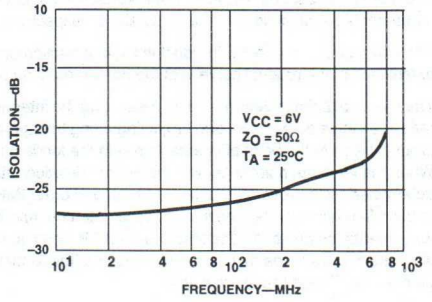


a. Insertion Gain vs Frequency (S_{21})

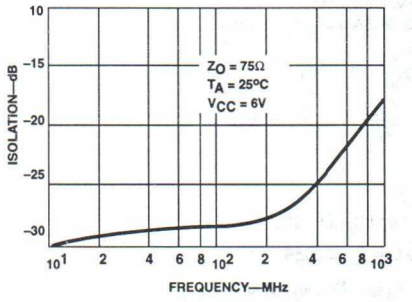
75Ω System



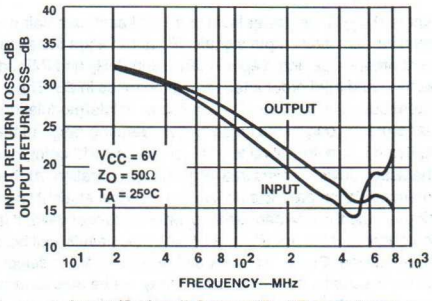
b. Insertion Gain vs Frequency (S_{21})



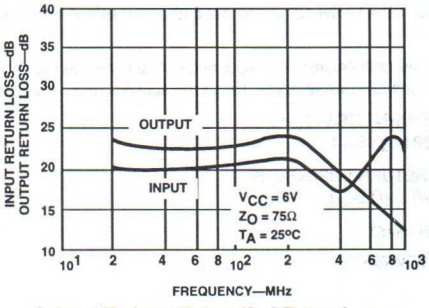
c. Isolation vs Frequency (S_{12})



d. S_{12} Isolation vs Frequency



e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

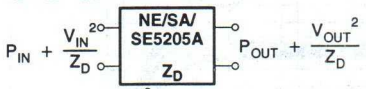


f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18.

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D=Z_{IN}=Z_{OUT}$ for the NE/SA/SE5205A



$$P_{IN} + \frac{V_{IN}^2}{Z_D} \quad P_{OUT} + \frac{V_{OUT}^2}{Z_D}$$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I=V_I{}^2$

P_I=Insertion Power Gain

V_I=Insertion Voltage Gain

Measured value for the NE/SA/SE5205A = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20\text{dB}$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS=S_{11}dB

$S_{11}\text{dB} = 20 \text{ Log } |S_{11}|$

OUTPUT RETURN LOSS=S_{22}dB

$S_{22}\text{dB} = 20 \text{ Log } |S_{22}|$

INPUT VSWR=≤1.5

OUTPUT VSWR=≤1.5

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

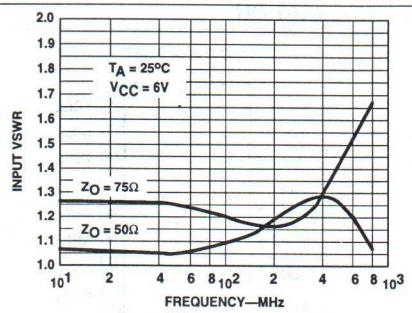
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

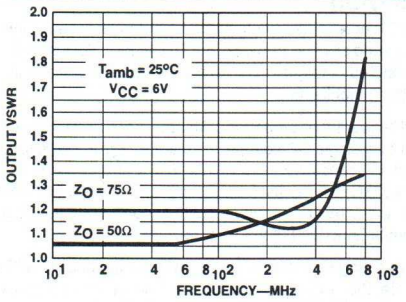
$IP_2=P_{OUT}+IMR_2$

$IP_3=P_{OUT}+IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA/SE5205A we have chosen an output level of -10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.



a. Input VSWR vs Frequency



b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

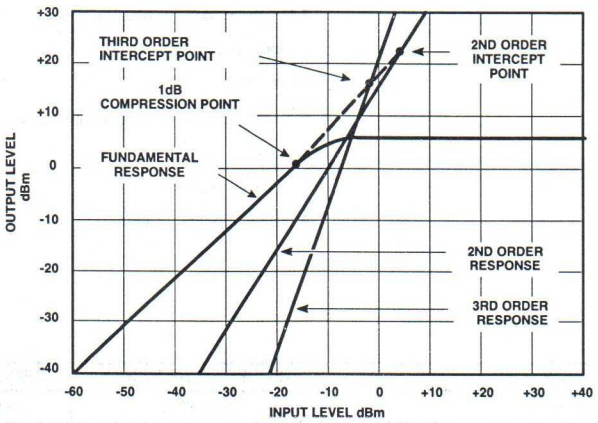


Figure 20.

Wideband variable gain amplifier — NE/SA5209

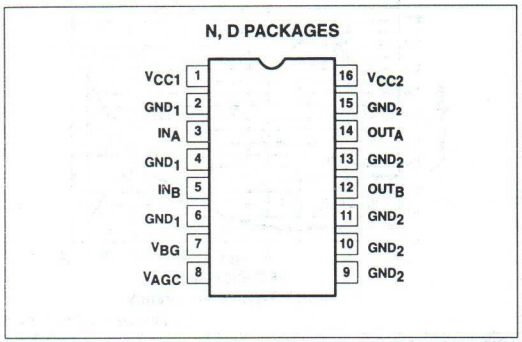
DESCRIPTION

The NE5209 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5209 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5209 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

PIN CONFIGURATION



FEATURES

- Gain to 1.5GHz
- 850MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5209D	0005
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5209N	0406
16-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5209D	0005
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5209N	0406

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   16-Pin DIP: θ_{JA} = 85°C/W
   16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	V_{CC1} = V_{CC2} = 4.5 to 7.0V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	38	43	48	mA
		Over temperature[1]	30		55	
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	17	19	21	dB
		Over temperature[1]	16		22	
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	23	25	27	dB
		Over temperature[1]	22		28	
R_{IN}	Input resistance (single-ended)	DC tested at ±50μA	0.9	1.2	1.5	kΩ
		Over temperature[1]	0.8		1.7	
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	40	60	75	Ω
		Over temperature[1]	35		90	
V_{OS}	Output offset voltage (output referred)			±20	±100	mV
		Over temperature[1]			±250	
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
		Over temperature[1]	1.4		2.6	
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
		Over temperature[1]	1.7		3.1	
PSRR	Output offset supply rejection ratio (output referred)		20	45		dB
		Over temperature[1]	15			
V_{BG}	Bandgap reference voltage	4.5V<V_{CC}<7V R_{BG} = 10kΩ	1.2	1.32	1.45	V
		Over temperature[1]	1.1		1.55	

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
R_{BG}	Bandgap loading	Over temperature[1]	2	10		kΩ
V_{AGC}	AGC DC control voltage range	Over temperature[1]		0-1.3		V
I_{BAGC}	AGC pin DC bias current	0V<V_{AGC}<1.3V		-0.7	-6	µA
		Over temperature[1]			-10	

NOTES:

1. "Over Temperature Range" testing is as follows:
   NE is 0 to +70°C
   SA is -40 to +85°C
   At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	-3dB bandwidth		600	850		MHz
		Over temperature[1]	500			
GF	Gain flatness	DC - 500MHz		±0.4		dB
		Over temperature[1]		±0.6		
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[2]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended) for linear operation[2]	R_L = 50Ω		400		mV_{P-P}
		R_L = 1kΩ		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	R_S = 50Ω, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		$nV/\sqrt{Hz}$
S12	Reverse isolation	f = 100MHz		-60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	R_L = 50Ω		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	-3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		-3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		-10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:

1. "Over Temperature Range" testing is as follows:
   NE is 0 to +70°C
   SA is -40 to +85°C
   At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.
2. With R_L > 1kΩ, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With R_L = 50Ω, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

NE5209 APPLICATIONS

The NE5209 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 1. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The NE5209 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 - 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The NE5209 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5209 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The NE5209 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the NE5209. A maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the NE5209 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the NE5209 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the NE5209 is shown in Figure 2. Three NE5209s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An NE5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three NE5209s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three NE5209s will give a dynamic range in excess of 60dB.

The NE5209 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

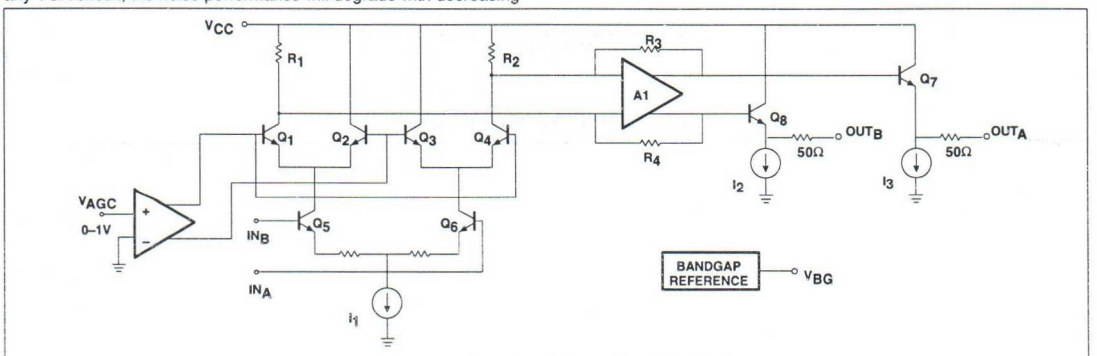


Figure 1. Equivalent Schematic of the VGA

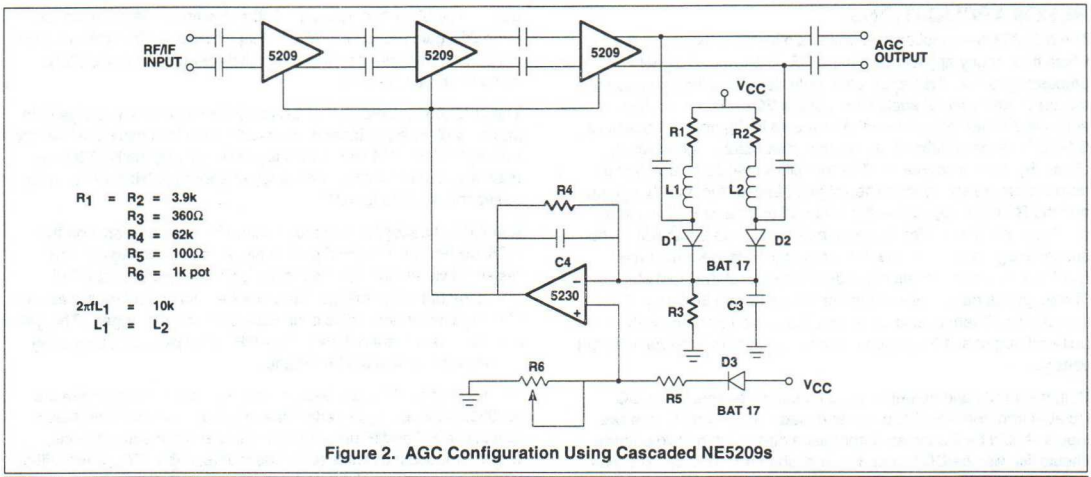


Figure 2. AGC Configuration Using Cascaded NE5209s

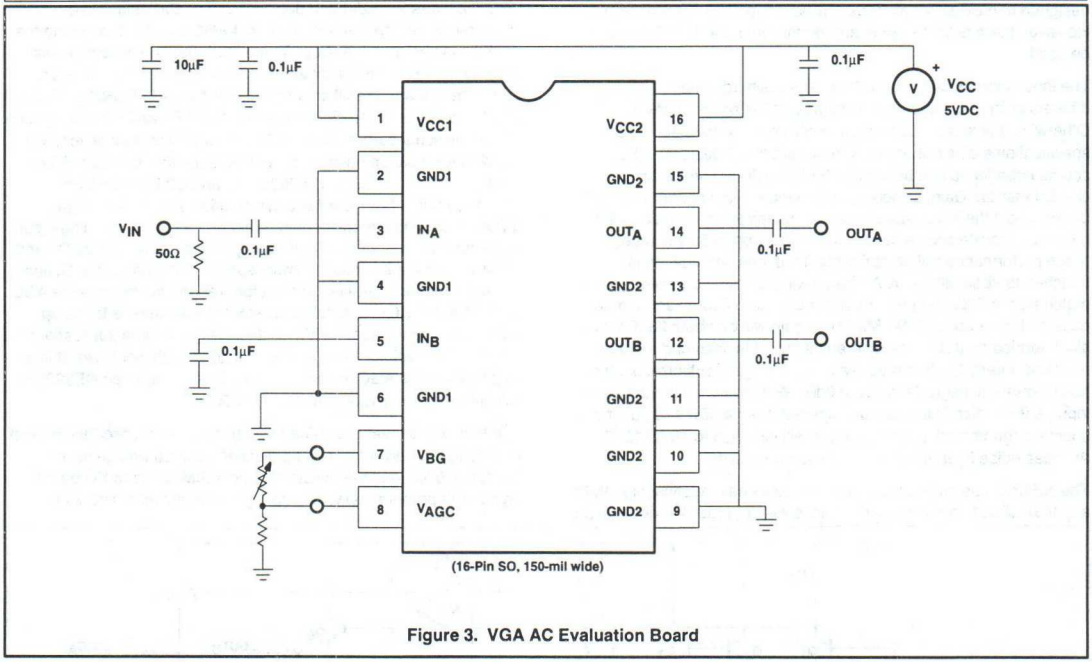
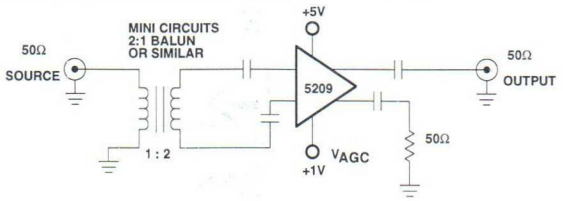
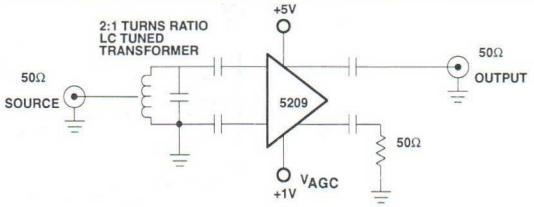


Figure 3. VGA AC Evaluation Board



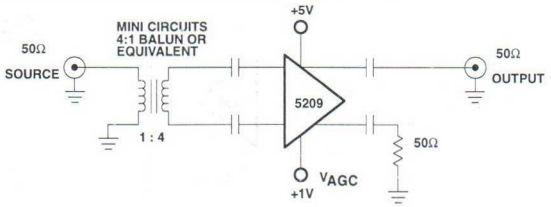
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain.

Figure 4. Broadband Noise Optimization



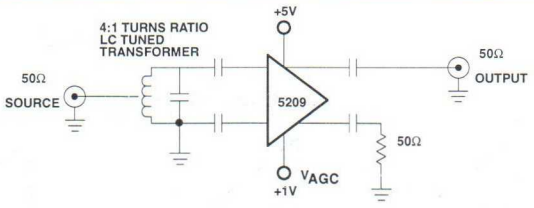
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain. Narrowband circuits have the advantage of greater stability, particularly when multiple devices are cascaded.

Figure 5. Narrowband Noise Optimization



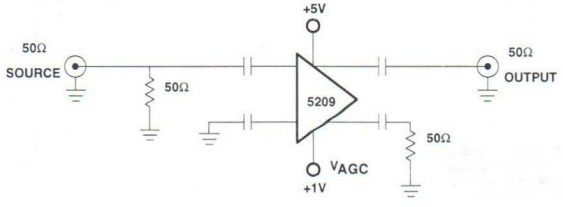
This circuit will exhibit about an 8dB noise figure with 24dB gain.

Figure 6. Broadband Gain Optimization



This circuit will exhibit approximately an 8dB noise figure and 25dB gain.

Figure 7. Narrowband Gain Optimization



The noise figure of this configuration will be approximately 15dB.

Figure 8. Simple Amplifier Configuration

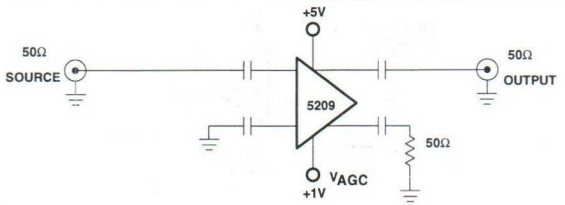


Figure 9. Unterminated Configuration

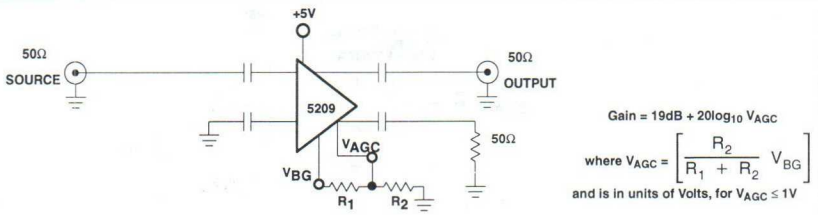


Figure 10. User-Programmable Fixed Gain Block

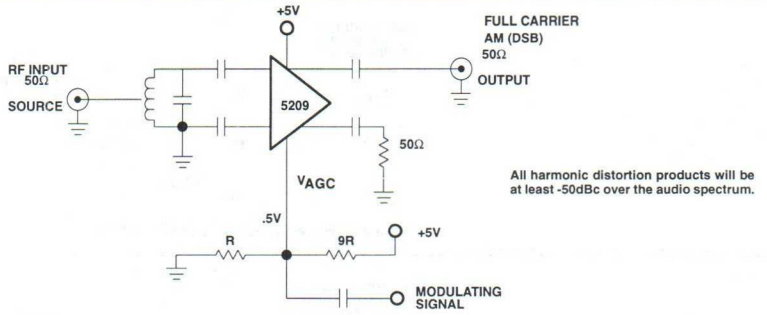
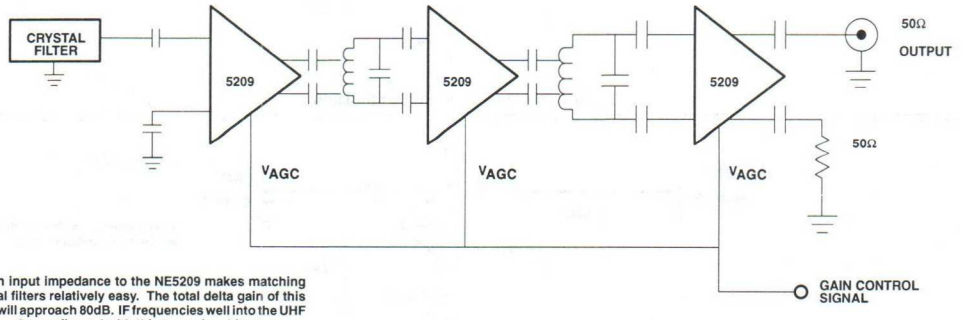


Figure 11. AM Modulator



The high input impedance to the NE5209 makes matching to crystal filters relatively easy. The total delta gain of this system will approach 80dB. IF frequencies well into the UHF region can be configured with this type of architecture.

Figure 12. Receiver AGC IF Gain

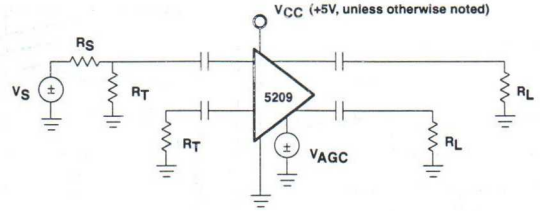


Figure 13. Test Set-up 1 (Used for all Graphs)

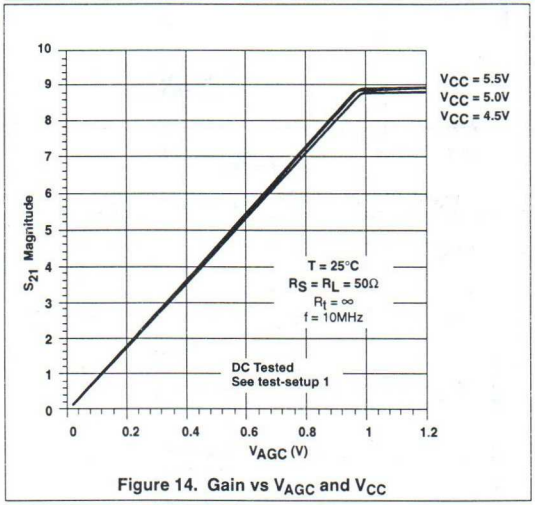


Figure 14. Gain vs V_{AGC} and V_{CC}

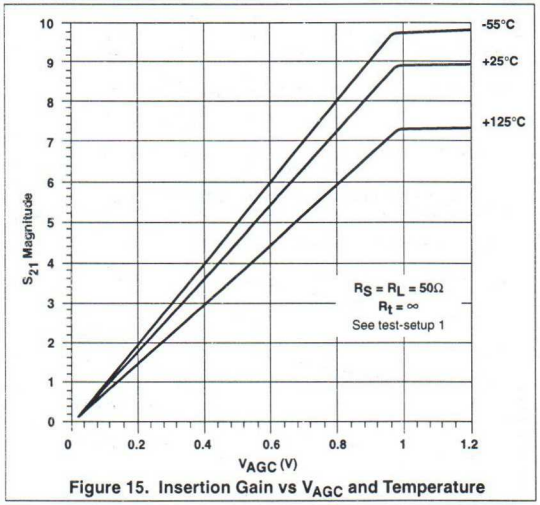


Figure 15. Insertion Gain vs V_{AGC} and Temperature

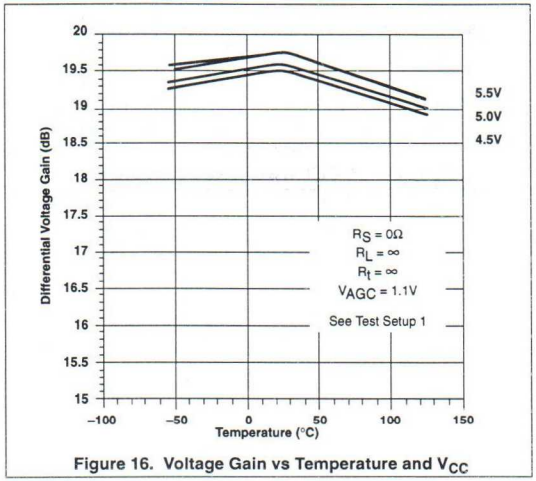


Figure 16. Voltage Gain vs Temperature and V_{CC}

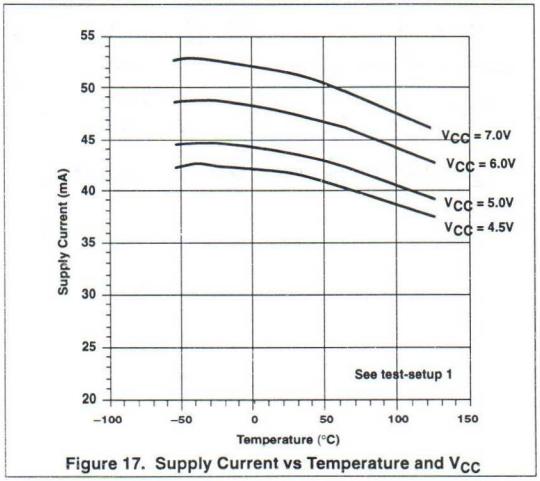


Figure 17. Supply Current vs Temperature and V_{CC}

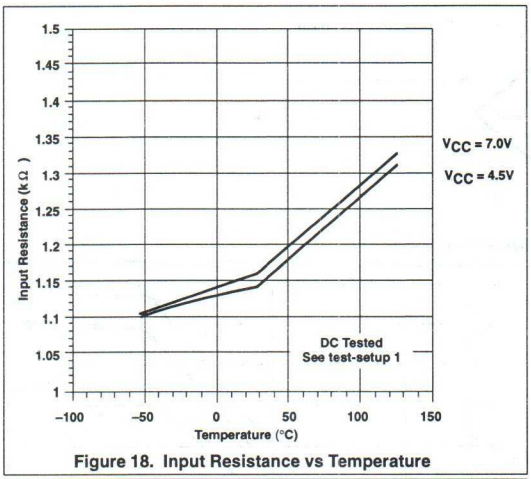


Figure 18. Input Resistance vs Temperature

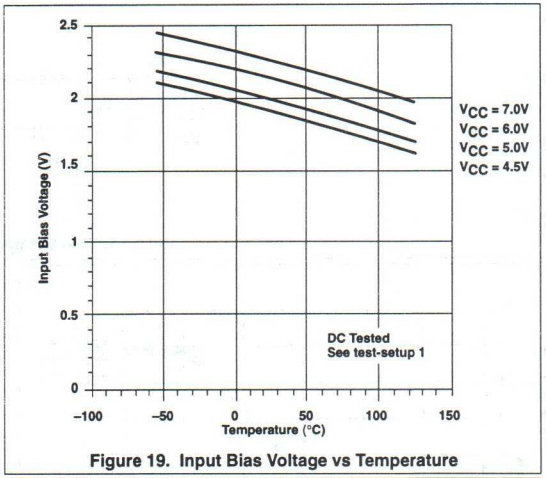


Figure 19. Input Bias Voltage vs Temperature

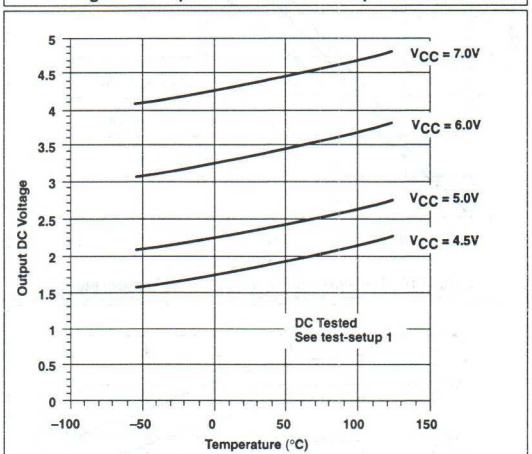


Figure 20. Output Bias Voltage vs Temperature and V_{CC}

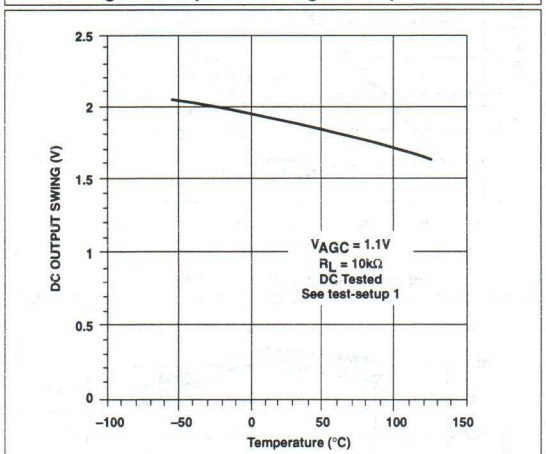


Figure 21. DC Output Swing vs Temperature

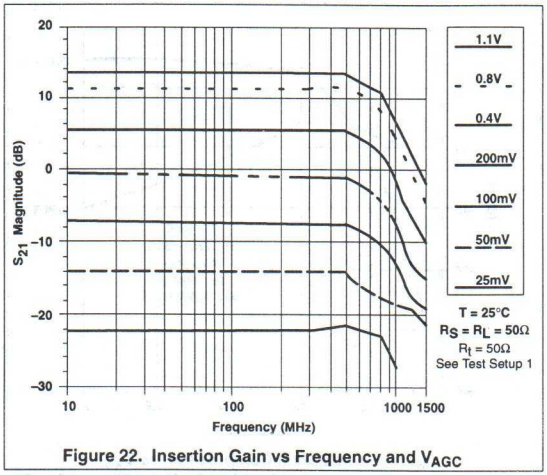


Figure 22. Insertion Gain vs Frequency and V_{AGC}

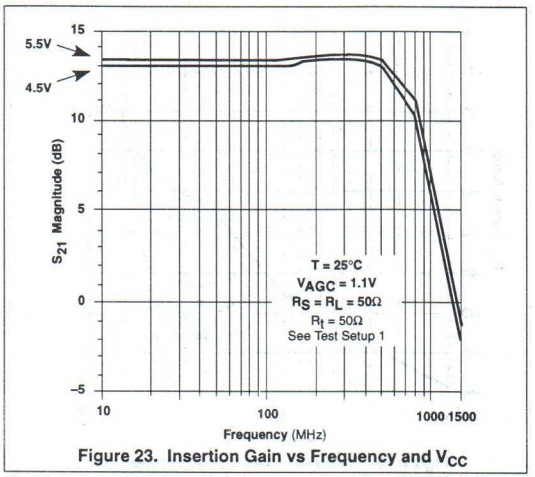


Figure 23. Insertion Gain vs Frequency and V_{CC}

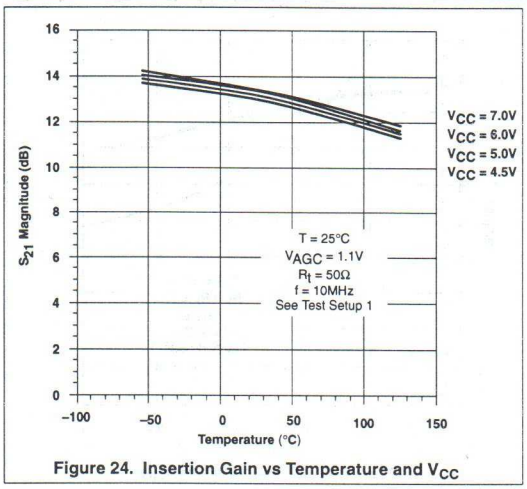


Figure 24. Insertion Gain vs Temperature and V_{CC}

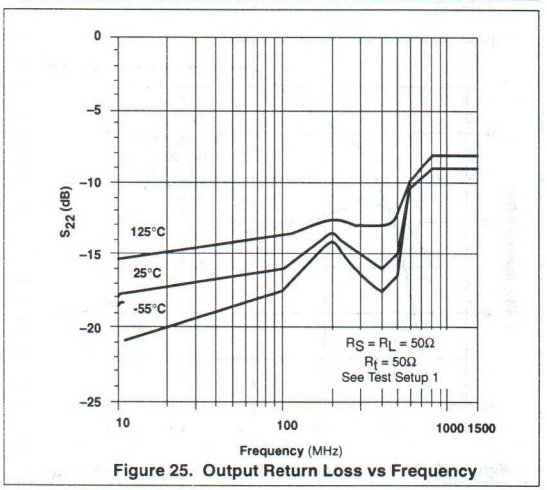


Figure 25. Output Return Loss vs Frequency

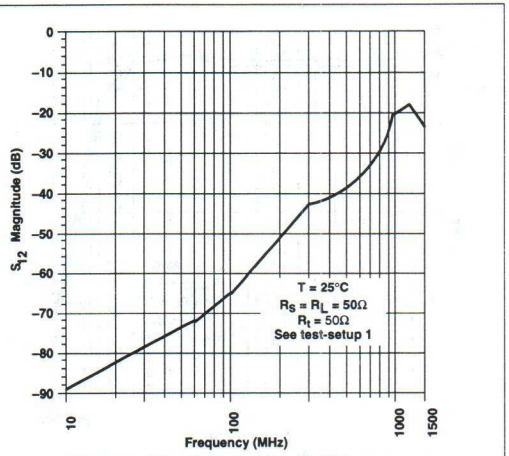


Figure 26. Reverse Isolation vs Frequency

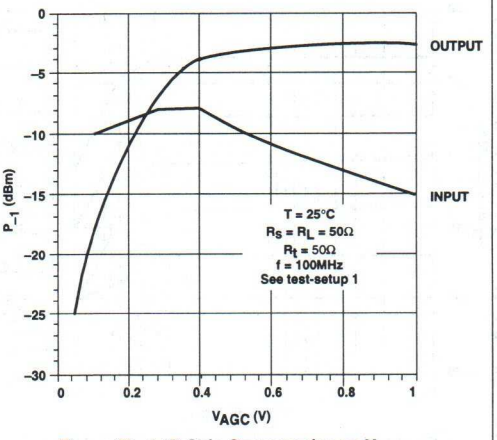


Figure 27. 1dB Gain Compression vs V_{AGC}

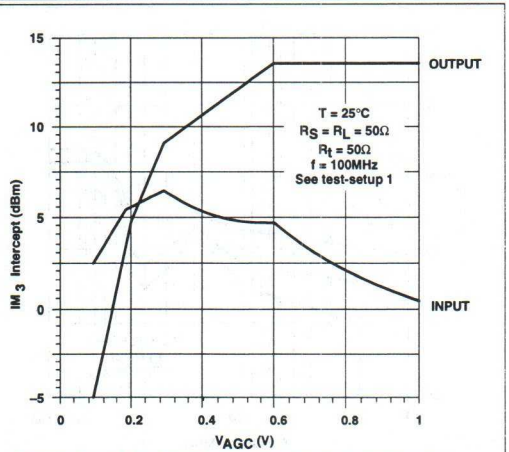


Figure 28. Third-Order Intermodulation Intercept vs V_{AGC}

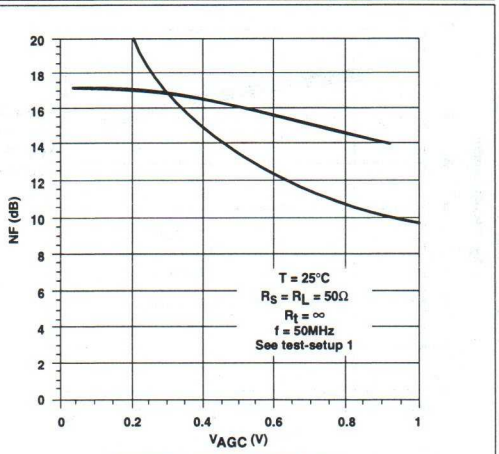


Figure 29. Noise Figure vs V_{AGC}

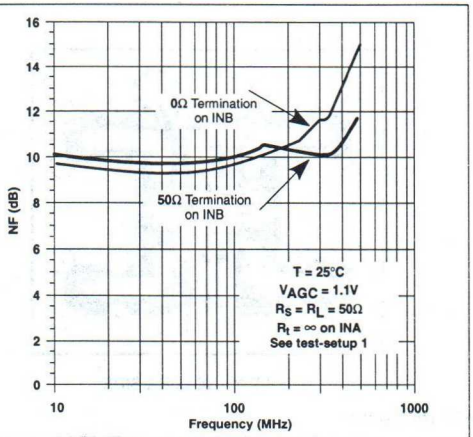


Figure 30. Noise Figure vs Frequency

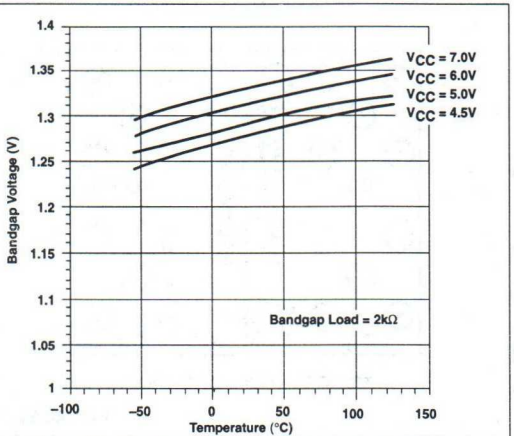


Figure 31. Bandgap Voltage vs Temperature and V_{CC}

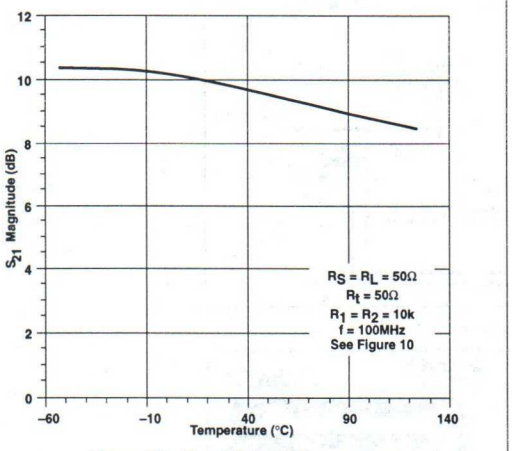
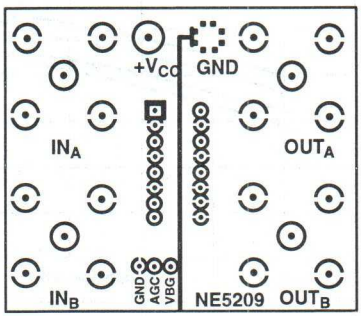
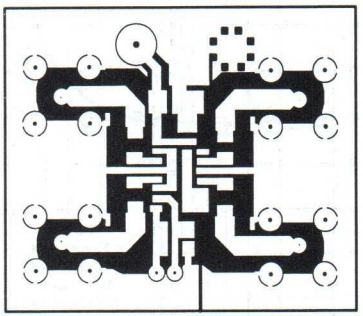


Figure 32. Fixed Gain vs Temperature

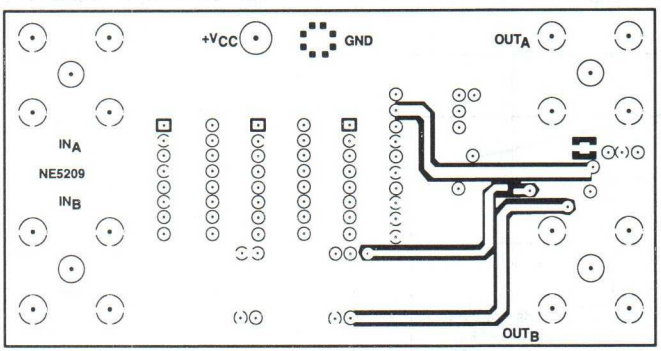


TOP VIEW - COMPONENT SIDE

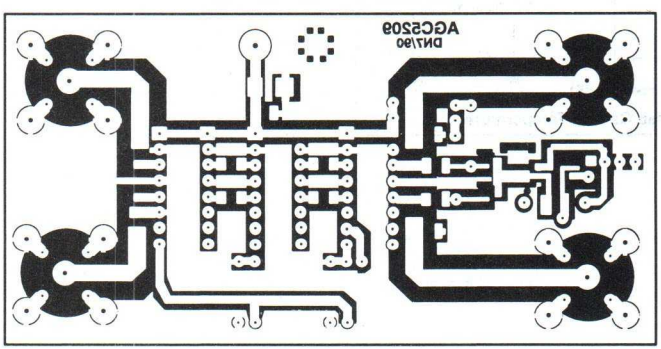


TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout

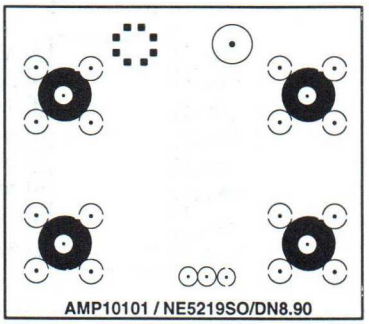


TOP VIEW - COMPONENT SIDE

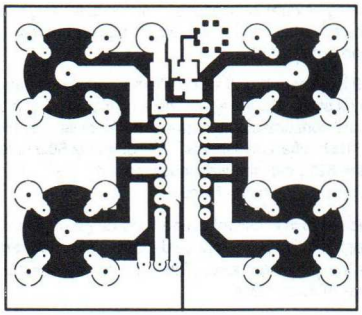


TOP VIEW - SOLDER SIDE

AGC Configuration Using Cascaded NE5209s - Layout



TOP VIEW - COMPONENT SIDE



TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout (DIP Package)

Wideband variable gain amplifier — NE/SA5219

DESCRIPTION

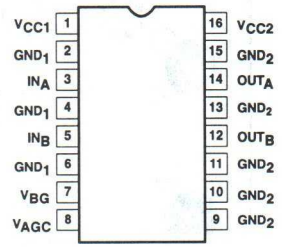
The NE5219 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5219 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5219 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

PIN CONFIGURATION

N, D PACKAGES



FEATURES

- 700MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

ORDERING INFORMATION

Description	Temperature Range	Order Code	DWG #
16-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5219D	0005D
16-Pin Plastic Dual In-Line package (DIP)	0 to +70°C	NE5219N	0406C
16-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5219D	0005D
16-Pin Plastic Dual In-Line package (DIP)	-40 to +85°C	SA5219N	0406C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   16-Pin DIP: θ_{JA} = 85°C/W
   16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	V_{CC1} = V_{CC2} = 4.5 to 7.0V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	36	43	50	mA
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	16	19	22	dB
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	22	25	28	dB
R_{IN}	Input resistance (single-ended)	DC tested at ±50μA	0.8	1.2	1.6	kΩ
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	35	60	80	Ω
V_{OS}	Output offset voltage (output referred)			±20	±150	mV
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
PSRR	Output offset supply rejection ratio		18	45		dB
V_{BG}	Bandgap reference voltage	4.5V<V_{CC}<7V R_{BG} = 10kΩ	1.2	1.32	1.45	V
R_{BG}	Bandgap loading		2	10		kΩ
V_{AGC}	AGC DC control voltage range			0-1.3		V
I_{BAGC}	AGC pin DC bias current	0V<V_{AGC}<1.3V		-0.7	-6	μA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	-3dB bandwidth			700		MHz
GF	Gain flatness	DC - 500MHz		±0.4		dB
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[1]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended) for linear operation[1]	R_L = 50Ω		400		mV_{P-P}
		R_L = 1kΩ		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	R_S = 50Ω, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		$nV/\sqrt{Hz}$
S12	Reverse isolation	f = 100MHz		-60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	R_L = 50Ω		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	-3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		-3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		-10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:

1. With R_L > 1kΩ, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With R_L = 50Ω, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

NE5219 APPLICATIONS

The NE5219 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 1. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The NE5219 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 - 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The NE5219 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5219 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The NE5219 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the NE5219. A

maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the NE5219 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the NE5219 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the NE5219 is shown in Figure 2. Three NE5219s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An NE5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three NE5219s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three NE5219s will give a dynamic range in excess of 60dB.

The NE5219 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

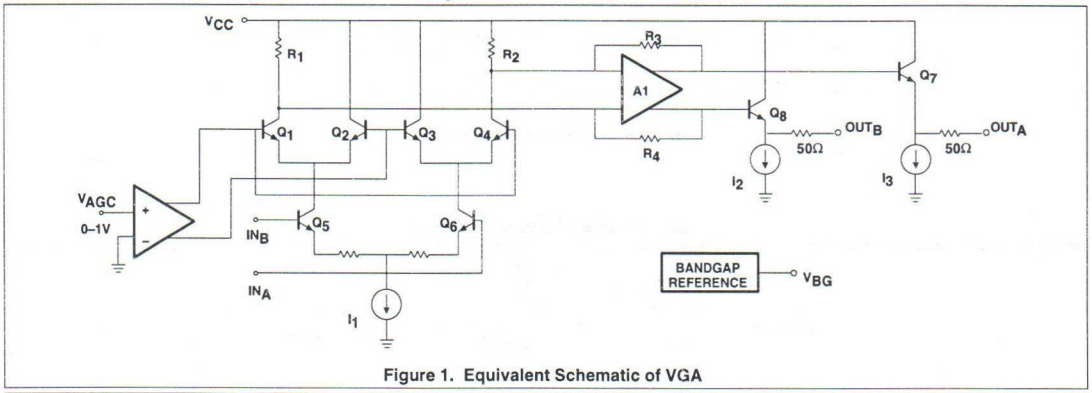


Figure 1. Equivalent Schematic of VGA

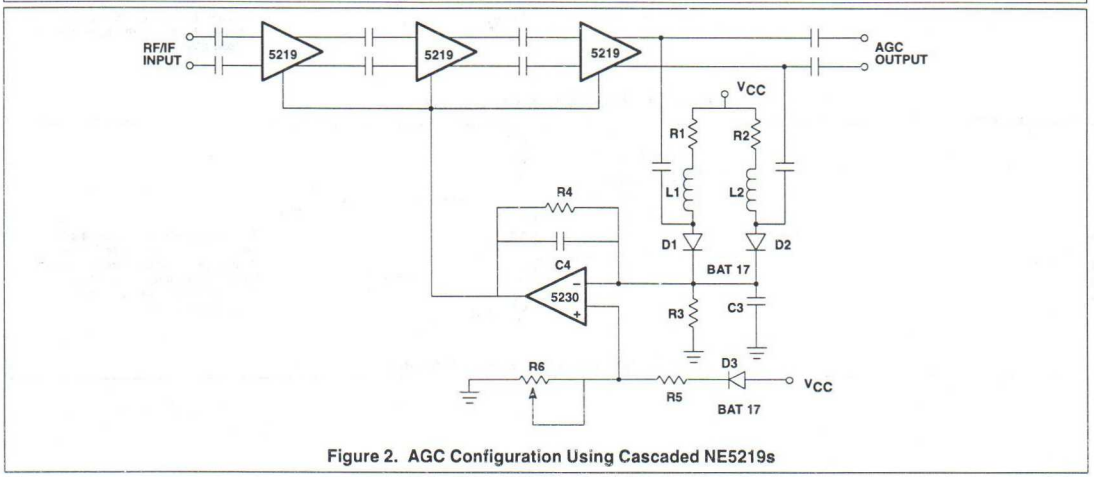


Figure 2. AGC Configuration Using Cascaded NE5219s

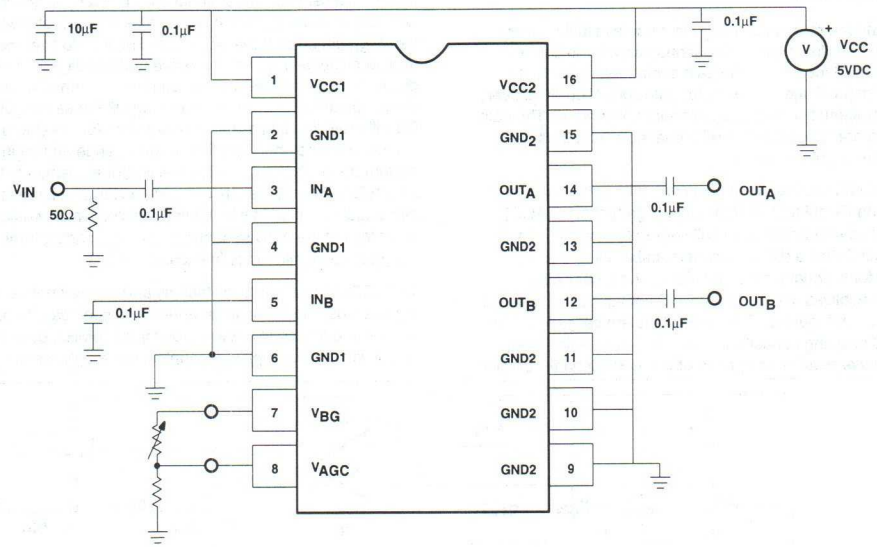
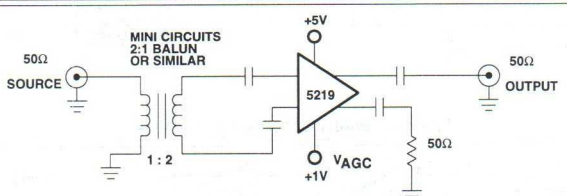
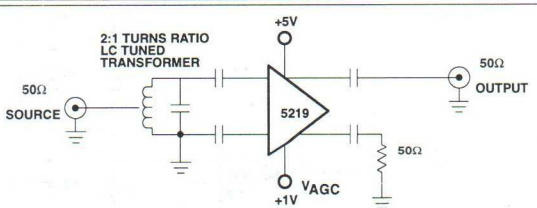


Figure 3. VGA AC Evaluation Board



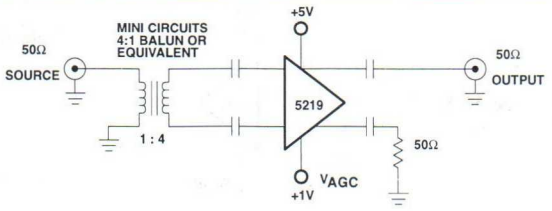
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain.

Figure 4. Broadband Noise Optimization



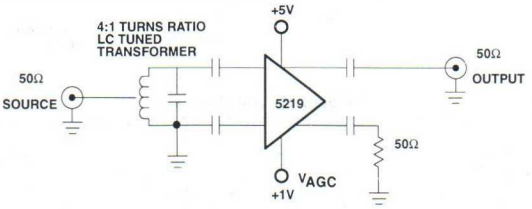
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain. Narrowband circuits have the advantage of greater stability, particularly when multiple devices are cascaded.

Figure 5. Narrowband Noise Optimization



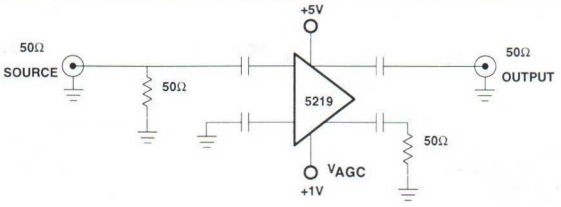
This circuit will exhibit about an 8dB noise figure with 24dB gain.

Figure 6. Broadband Gain Optimization



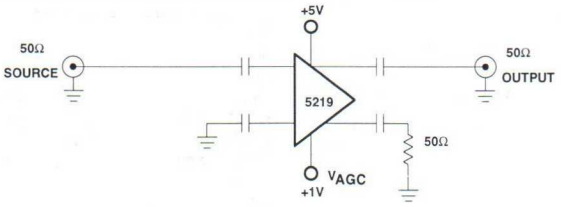
This circuit will exhibit approximately an 8dB noise figure and 25dB gain.

Figure 7. Narrowband Gain Optimization



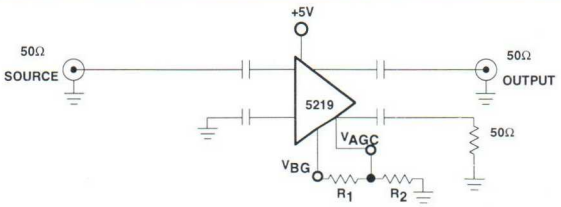
The noise figure of this configuration will be approximately 15dB.

Figure 8. Simple Amplifier Configuration



With the 50Ω source left unterminated, the noise figure is 9dB.

Figure 9. Unterminated Configuration



$$\text{Gain} = 19\text{dB} + 20\log_{10} V_{AGC}$$

$$\text{where } V_{AGC} = \left[\frac{R_2}{R_1 + R_2} V_{BG}\right]$$

and is in units of Volts, for $V_{AGC} \leq 1V$

Figure 10. User-Programmable Fixed Gain Block

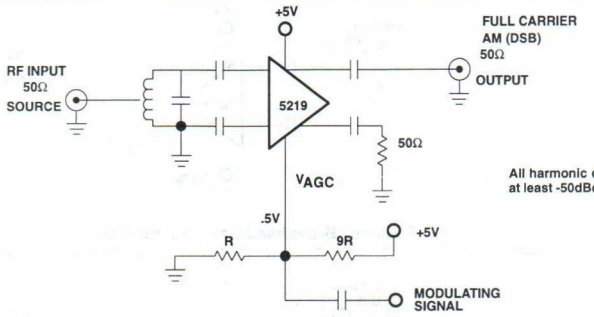
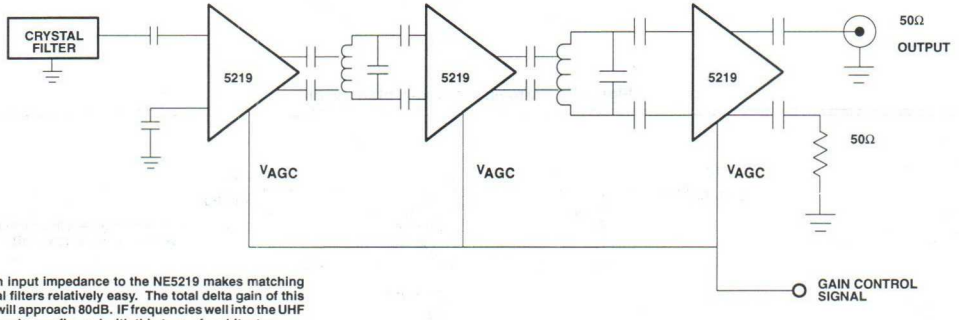


Figure 11. AM Modulator



The high input impedance to the NE5219 makes matching to crystal filters relatively easy. The total delta gain of this system will approach 80dB. IF frequencies well into the UHF region can be configured with this type of architecture.

Figure 12. Receiver AGC IF Gain

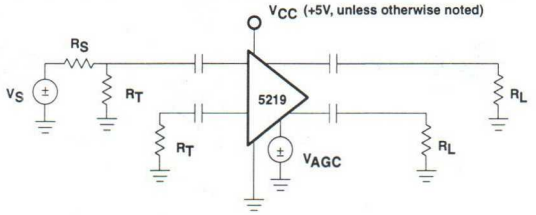


Figure 13. Test Set-up 1 (Used for all Graphs)

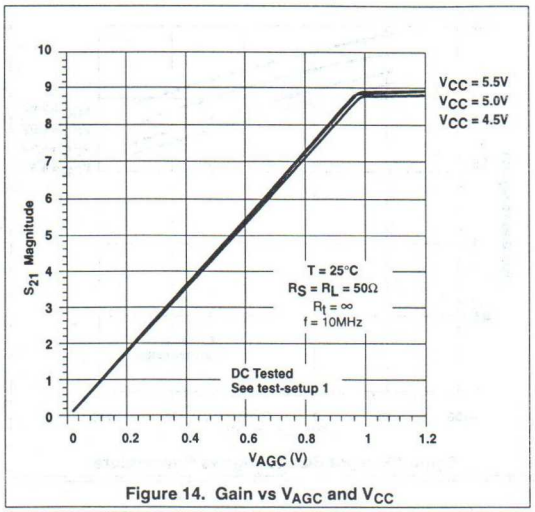


Figure 14. Gain vs V_{AGC} and V_{CC}

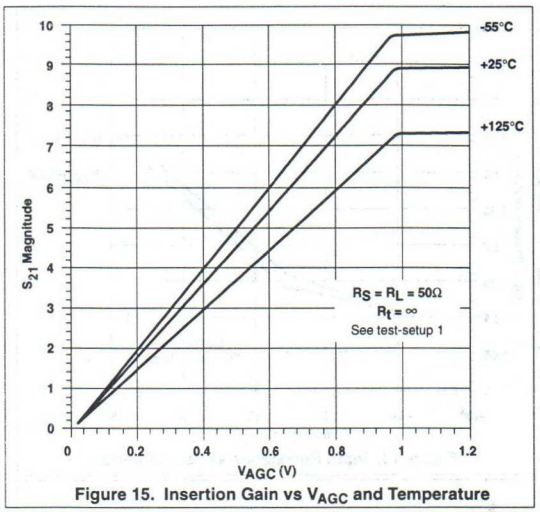


Figure 15. Insertion Gain vs V_{AGC} and Temperature

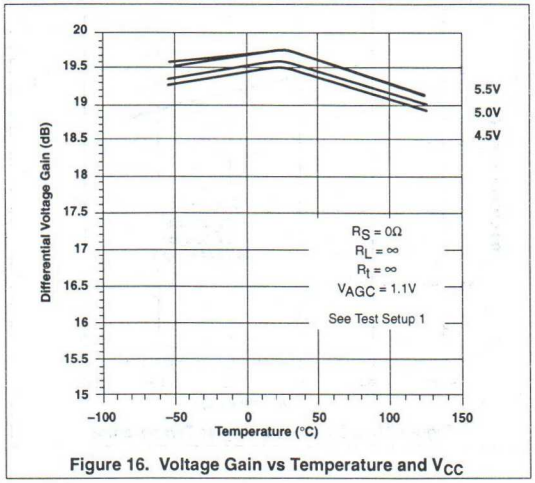


Figure 16. Voltage Gain vs Temperature and V_{CC}

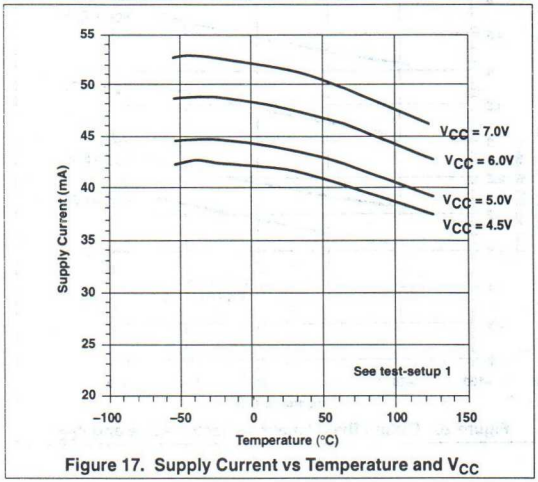


Figure 17. Supply Current vs Temperature and V_{CC}

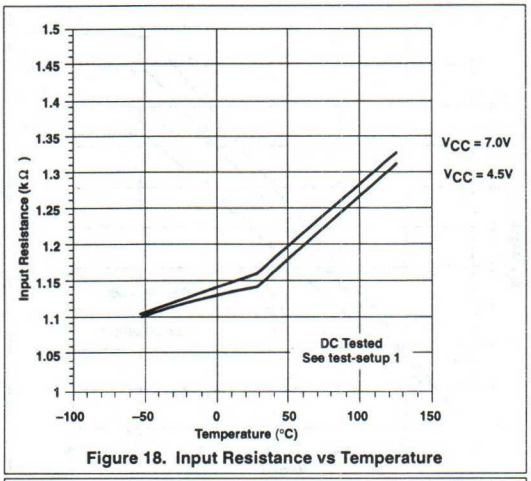


Figure 18. Input Resistance vs Temperature

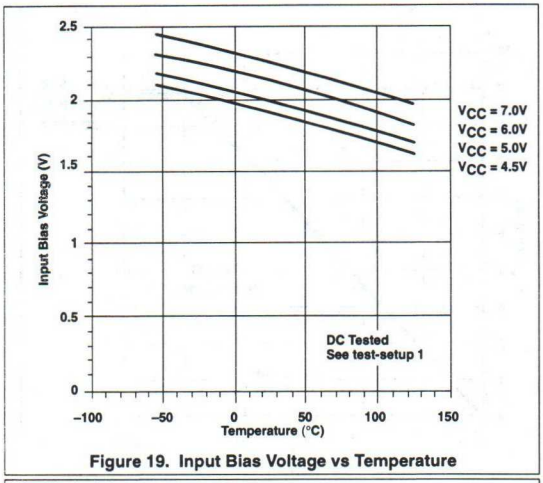


Figure 19. Input Bias Voltage vs Temperature

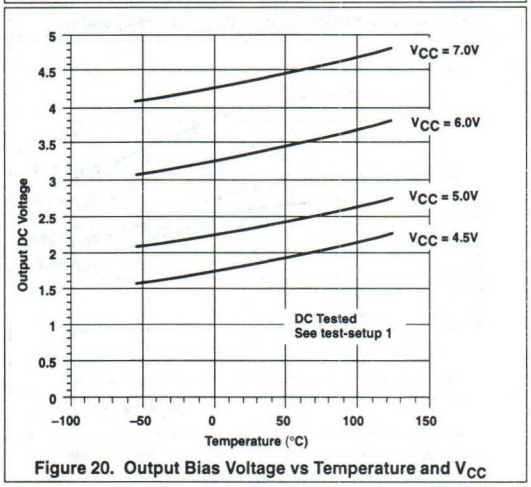


Figure 20. Output Bias Voltage vs Temperature and V_{CC}

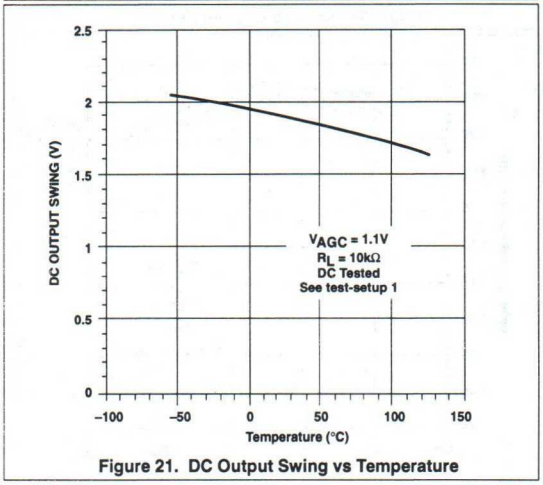


Figure 21. DC Output Swing vs Temperature

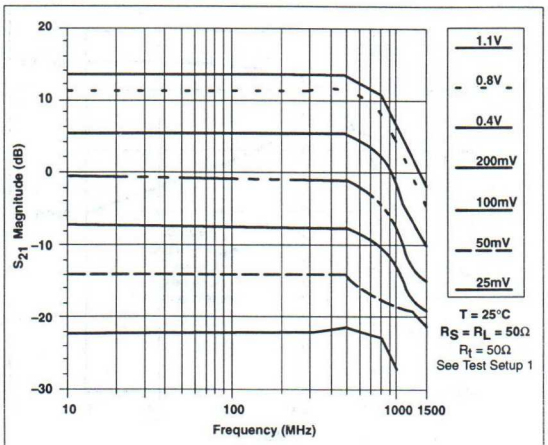


Figure 22. Insertion Gain vs Frequency and V_{AGC}

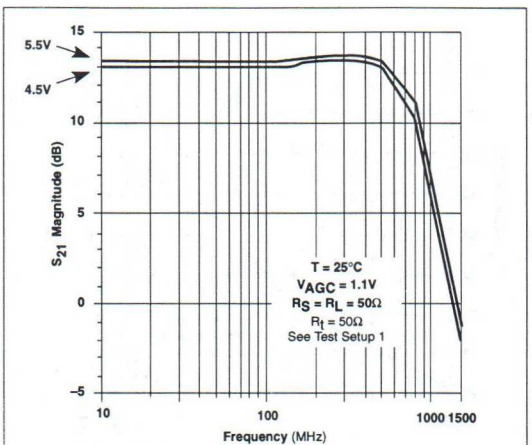


Figure 23. Insertion Gain vs Frequency and V_{CC}

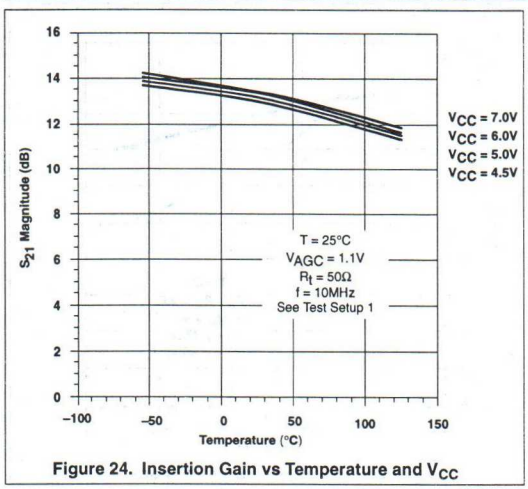


Figure 24. Insertion Gain vs Temperature and V_{CC}

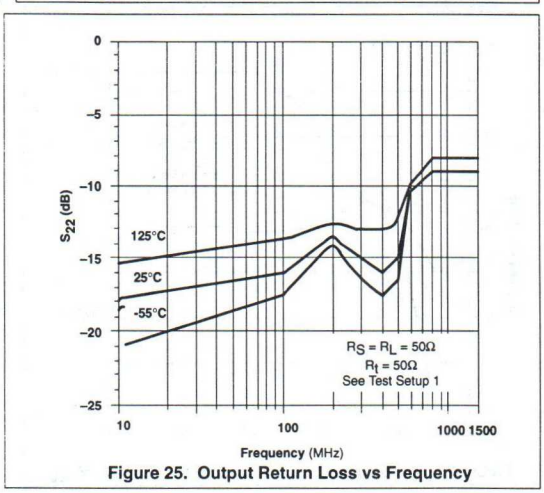


Figure 25. Output Return Loss vs Frequency

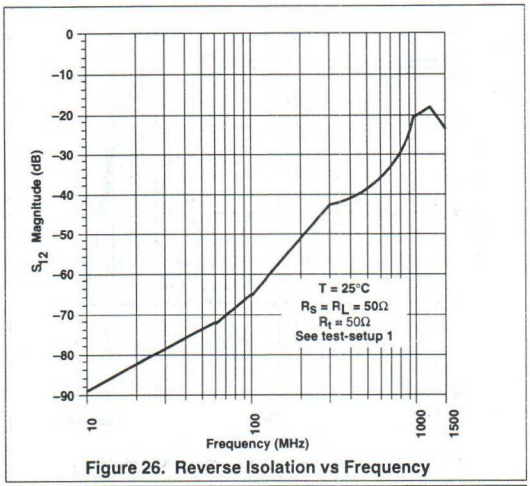


Figure 26. Reverse Isolation vs Frequency

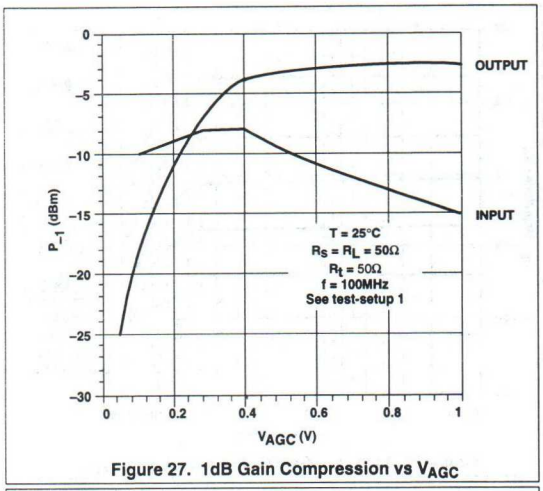


Figure 27. 1dB Gain Compression vs V_{AGC}

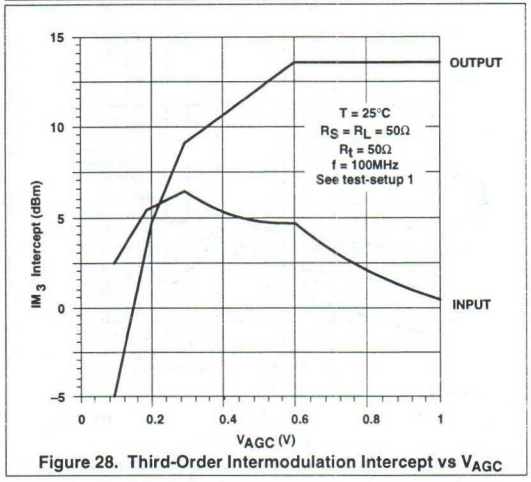


Figure 28. Third-Order Intermodulation Intercept vs V_{AGC}

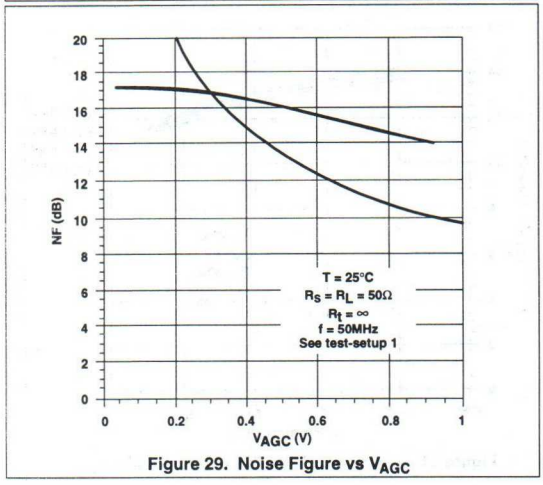


Figure 29. Noise Figure vs V_{AGC}

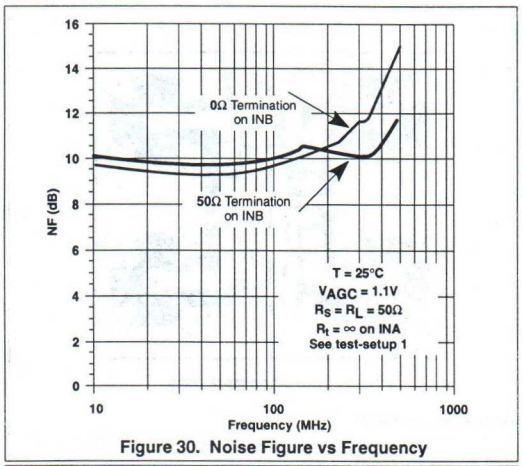


Figure 30. Noise Figure vs Frequency

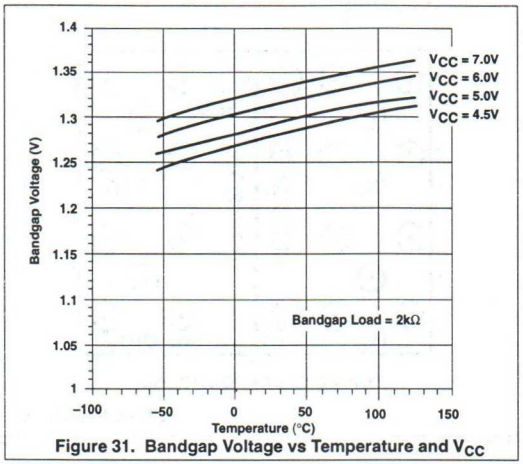


Figure 31. Bandgap Voltage vs Temperature and V_{CC}

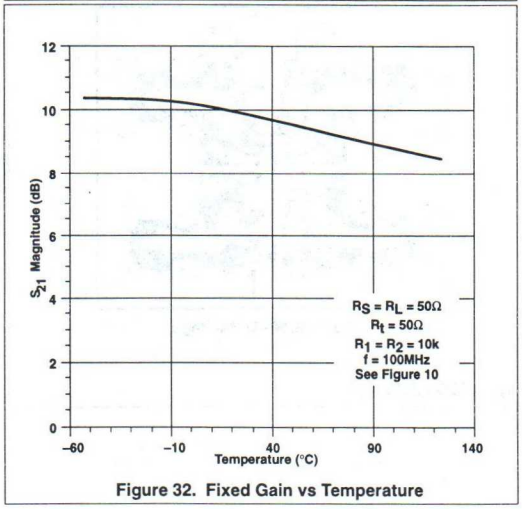
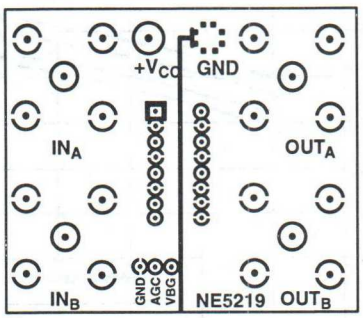
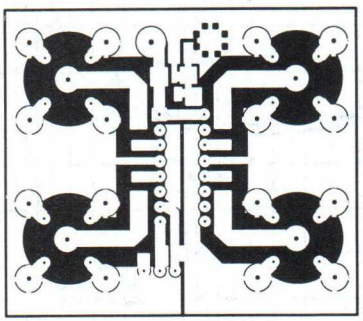


Figure 32. Fixed Gain vs Temperature

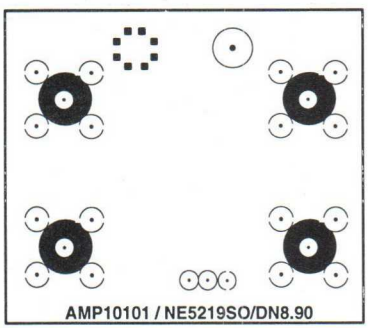


TOP VIEW - COMPONENT SIDE



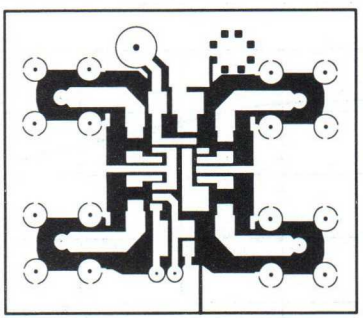
TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout (DIP Package)



AMP10101 / NE5219SO/DN8.90

BOTTOM VIEW - D Package



TOP VIEW - D Package

VGA AC Evaluation Board Layout (SO Package)

High frequency operational amplifier — NE/SE5539

DESCRIPTION

The NE/SE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter-follower inputs provide a true differential input impedance device. Proper external compensation will allow design operation over a wide range of closed-loop gains, both inverting and non-inverting, to meet specific design requirements.

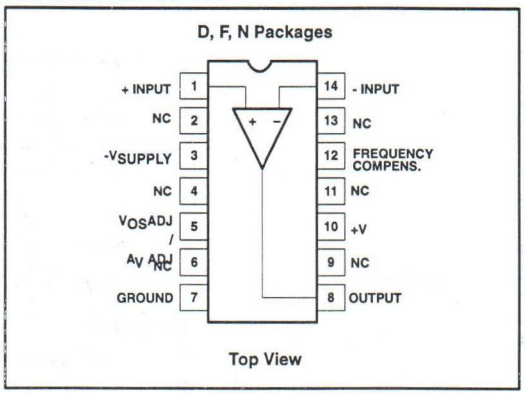
FEATURES

- Bandwidth
  - Unity gain - 350MHz
  - Full power - 48MHz
  - GBW - 1.2GHz at 17dB
- Slew rate: 600/Vμs
- A_{VOL}: 52dB typical
- Low noise - 4nV√Hz typical
- MIL-STD processing available

APPLICATIONS

- High speed datacom
- Video monitors & TV
- Satellite communications
- image processing
- RF instrumentation & oscillators
- Magnetic storage
- Military communications

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5539N	0405B
14-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5539D	0175D
14-Pin Ceramic Dual In-Line Package	0 to +70°C	NE5539F	0581B
14-Pin Ceramic Dual In-Line Package	-55 to +125°C	SE5539F	0581B

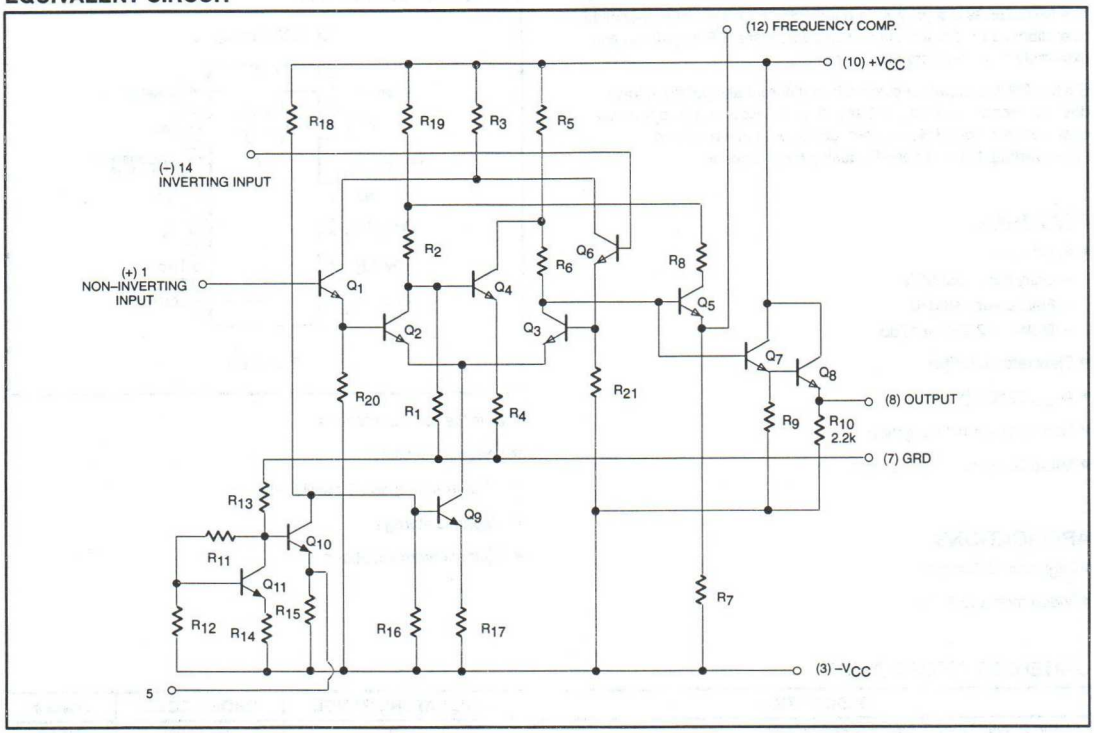
ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	±12	V
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[2] F package N package D package	 1.17 1.45 0.99	 W W W
T_A	Operating temperature range NE SE	 0 to 70 -55 to +125	 °C °C
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Max junction temperature	150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:

1. Differential input voltage should not exceed 0.25V to prevent excesive input bias current and common-mode voltage 2.5V. These voltage limits may be exceeded if current is limited to less than 10mA.
2. Derate above 25°C, at the following rates:
   F package at 9.3mW/°C
   N package at 11.6mW/°C
   D package at 7.9mW/°C

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

V_{CC} = ±8V, T_A = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			NE5539			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input offset voltage	V_O = 0V, R_S = 100Ω	Over temp		2	5				mV
			T_A = 25°C		2	3		2.5	5	
	$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Input offset current		Over temp		0.1	3				µA
			T_A = 25°C		0.1	1			2	
	$\Delta I_{OS}/\Delta T$				0.5			0.5		nA/°C
I_B	Input bias current		Over temp		6	25				µA
			T_A = 25°C		5	13		5	20	
	$\Delta I_B/\Delta T$				10			10		nA/°C
CMRR	Common mode rejection ratio	F = 1kHz, R_S = 100Ω, V_{CM} ±1.7V		70	80		70	80		dB
			Over temp	70	80					
R_{IN}	Input impedance				100			100		kΩ
R_{OUT}	Output impedance				10			10		Ω

DC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = ±8V, T_A = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			NE5539			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OUT}	Output voltage swing	R_L = 150Ω to GND and 470Ω to -V_{CC}	+Swing -Swing				+2.3 -1.7	+2.7 -2.2		V
V_{OUT}	Output voltage swing	R_L = 25Ω to GND Over temp	+Swing -Swing	+2.3 -1.5	+3.0 -2.1					V
		R_L = 25Ω to GND T_A = 25°C	+Swing -Swing	+2.5 -2.0	+3.1 -2.7					
I_{CC+}	Positive supply current	V_O = 0, R_1 = ∞, Over temp			14	18				mA
		V_O = 0, R_1 = ∞, T_A = 25°C			14	17		14	18	
I_{CC-}	Negative supply current	V_O = 0, R_1 = ∞, Over temp			11	15				mA
		V_O = 0, R_1 = ∞, T_A = 25°C			11	14		11	15	
PSRR	Power supply rejection ratio	ΔV_{CC} = ±1V, Over temp			300	1000				µV/V
		ΔV_{CC} = ±1V, T_A = 25°C						200	1000	
A_{VOL}	Large signal voltage gain	V_O = +2.3V, -1.7V, R_L = 150Ω to GND, 470Ω to -V_{CC}					47	52	57	dB
A_{VOL}	Large signal voltage gain	V_O = +2.3V, -1.7V	Over temp							dB
		R_L = 2Ω to GND	T_A = 25°C				47	52	57	
A_{VOL}	Large signal voltage gain	V_O = +2.5V, -2.0V	Over temp	46		60				dB
		R_L = 2Ω to GND	T_A = 25°C	48	53	58				

DC ELECTRICAL CHARACTERISTICS

V_{CC} = ±6V, T_A = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			UNITS
					MIN	TYP	MAX	
V_{OS}	Input offset voltage			Over temp		2	5	mV
				T_A = 25°C		2	3	
I_{OS}	Input offset current			Over temp		0.1	3	µA
				T_A = 25°C		0.1	1	
I_B	Input bias current			Over temp		5	20	µA
				T_A = 25°C		4	10	
CMRR	Common-mode rejection ratio	V_{CM} = ±1.3V, R_S = 100Ω			70	85		dB
I_{CC+}	Positive supply current			Over temp		11	14	mA
				T_A = 25°C		11	13	
I_{CC-}	Negative supply current			Over temp		8	11	mA
				T_A = 25°CmA		8	10	
PSRR	Power supply rejection ratio	ΔV_{CC} = ±1V		Over temp		300	1000	µV/V
				T_A = 25°C				
V_{OUT}	Output voltage swing	R_L = 150Ω to GND and 390Ω to –V_{CC}	Over temp	+Swing	+1.4	+2.0		V
				–Swing	–1.1	–1.7		
			T_A = 25°C	+Swing	+1.5	+2.0		
				–Swing	–1.4	–1.8		

AC ELECTRICAL CHARACTERISTICS

V_{CC} = ±8V, R_L = 150Ω to GND and 470Ω to -V_{CC}, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
BW	Gain bandwidth product	A_{CL} = 7, V_O = 0.1 V_{P-P}		1200			1200		MHz
	Small signal bandwidth	A_{CL} = 2, R_L = 150Ω[1]		110			110		MHz
t_S	Settling time	A_{CL} = 2, R_L = 150Ω[1]		15			15		ns
SR	Slew rate	A_{CL} = 2, R_L = 150Ω[1]		600			600		V/µs
t_{PD}	Propagation delay	A_{CL} = 2, R_L = 150Ω[1]		7			7		ns
	Full power response	A_{CL} = 2, R_L = 150Ω[1]		48			48		MHz
	Full power response	A_V = 7, R_L = 150Ω[1]		20			20		MHz
	Input noise voltage	R_S = 50Ω, 1MHz		4			4		nV/√Hz
	Input noise current	1MHz		6			6		pA/√Hz

NOTES:
1. External compensation.

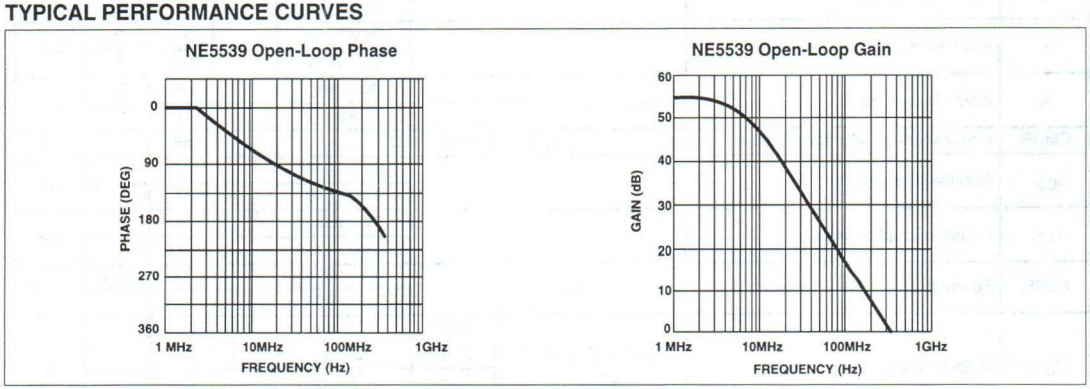
AC ELECTRICAL CHARACTERISTICS

V_{CC} = ±6V, R_L = 150Ω to GND and 390Ω to -V_{CC}, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			UNITS
			MIN	TYP	MAX	
BW	Gain bandwidth product	A_{CL} = 7		700		MHz
	Small signal bandwidth	A_{CL} = 2[1]		120		
t_S	Settling time	A_{CL} = 2[1]		23		ns
SR	Slew rate	A_{CL} = 2[1]		330		V/µs
t_{PD}	Propagation delay	A_{CL} = 2[1]		4.5		ns
	Full power response	A_{CL} = 2[1]		20		MHz

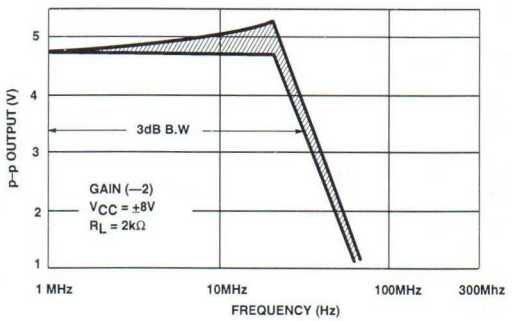
NOTES:
1. External compensation.

TYPICAL PERFORMANCE CURVES

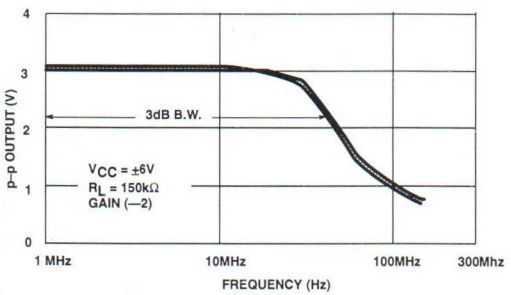


TYPICAL PERFORMANCE CURVES (Continued)

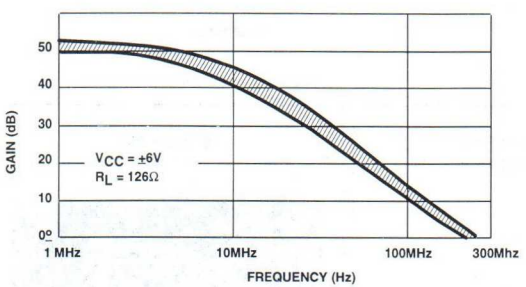
Power Bandwidth (SE)



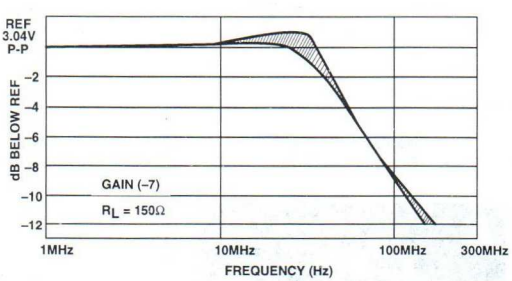
Power Bandwidth (NE)



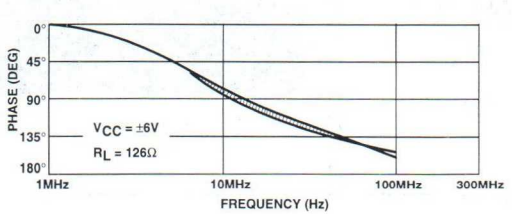
SE5539 Open-Loop Gain vs Frequency



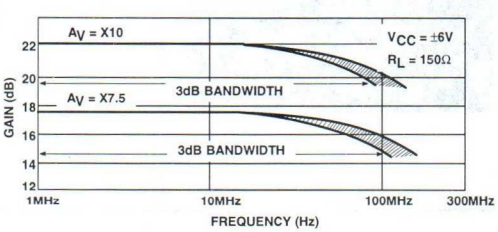
Power Bandwidth



SE5539 Open-Loop Phase vs Frequency



Gain Bandwidth Product vs Frequency

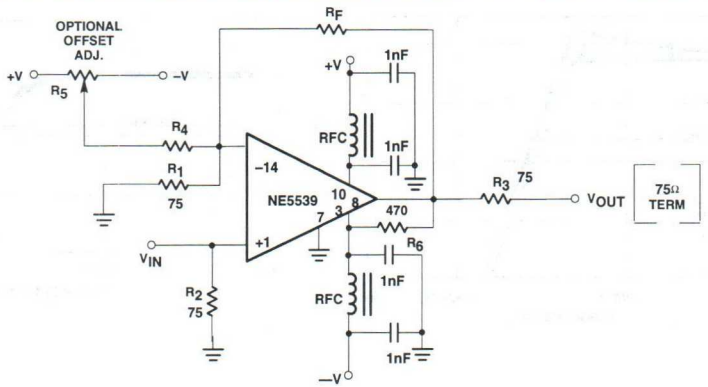


NOTE:

Indicates typical distribution $-55°C \leq T_A \leq 125°C$

CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide-gain bandwidth amplifier, the physical circuit is extremely critical. Bread-boarding is not recommended. A double-sided copper-clad printed circuit board will result in more favorable system operation. An example utilizing a 28dB non-inverting amp is shown in Figure 1.

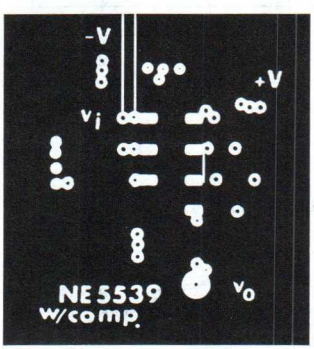


R_1 = 75Ω 5% CARBON
R_2 = 75Ω 5% CARBON
R_3 = 75Ω 5% CARBON
R_4 = 36K 5% CARBON

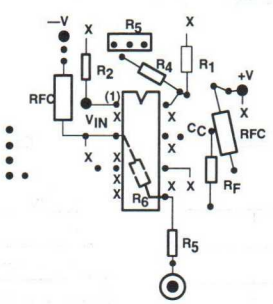
R_5 = 20k TRIMPOT (CERMET)
R_F = 1.5k (28dB GAIN)
R_6 = 470Ω 5% CARBON

RFC 3T # 26 BUSS WIRE ON
FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)

Top Plane Copper[1] (Component Side)



Component Side (Component Layout)



Bottom Plane Copper[1]

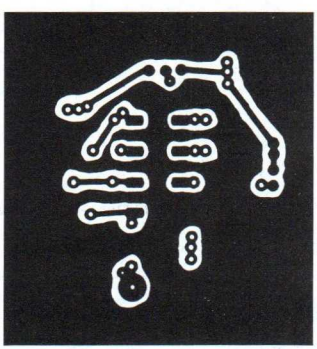


Figure 1. 28dB Non-Inverting Amp Sample PC Layout

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wideband operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown in Figure 2 along with vector-scope1 photographs showing the amplifier differential gain and phase response to a standard five-step modulated staircase linearity signal (Figures 3, 4 and 5). As can be seen in Figure 4, the gain varies less than 0.5% from the bottom to the top of the staircase. The maximum differential phase shown in Figure 5 is approximately +0.1°.

The amplifier circuit was optimized for a 75Ω input and output termionation impedance with a gain of approximately 10 (20dB).

NOTE:

1. The input signal was 200mV and the output 2V. V_{CC} was ±8V.

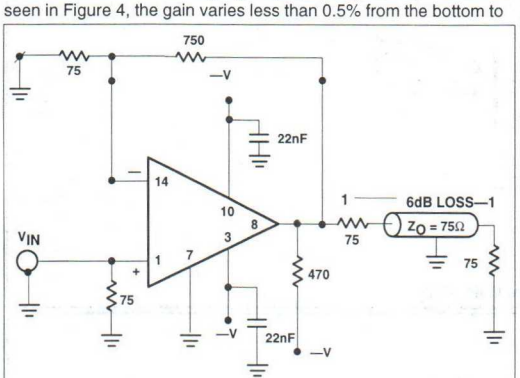


Figure 2. NE5539 Video Amplifier

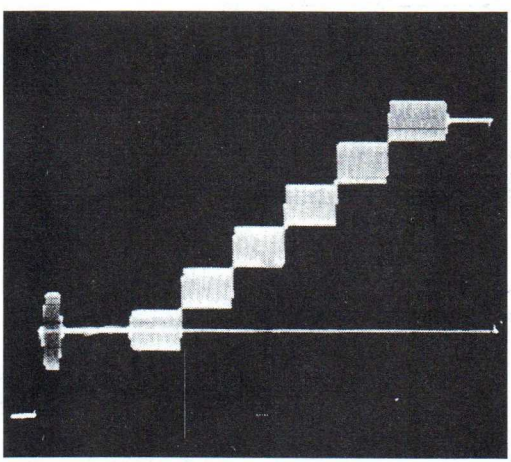


Figure 3. Input Signal

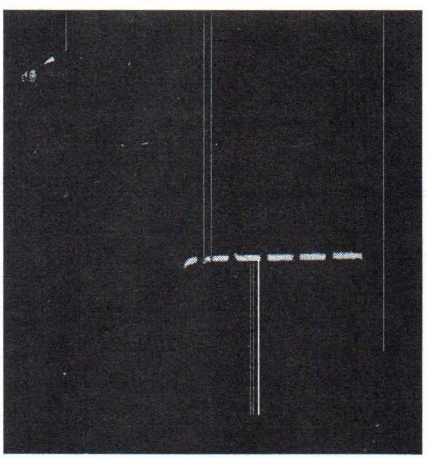


Figure 4. Differential Gain <0.5%

NOTE:

Instruments used for these measurements were Tektronix 146 NTSC test signal generator, 520A NTSC vectorscope, and 1480 waveform monitor.

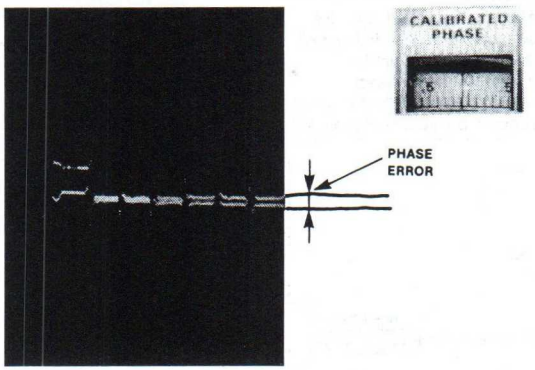


Figure 5. Differential Gain +0.1°

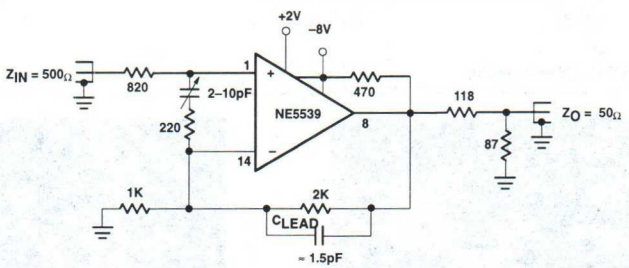


Figure 6. Non-Inverting Follower

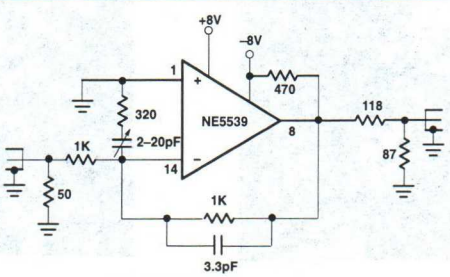


Figure 7. Inverting Follower

Compensation techniques for use with the NE/SE5539 AN140

Author: Tom DeLurio

NE5539 DESCRIPTION

The Philips Semiconductors NE/SE5539 ultra-high frequency operational amplifier is one of the fastest monolithic amplifiers made today. With a unity gain bandwidth of 350MHz and a slew rate of 600V/μs, it is second to none. Therefore, it is understandable that to attain this speed, standard internal compensation would have to be left out of its design. As a consequence, the op amp is not unconditionally stable for all closed-loop gains and must be externally compensated for gains below 17dB. Properly done, compensation need not limit slew rate. The following will explain how to use the methods available with the NE/SE5539.

LEAD AND LAG-LEAD COMPENSATION

A useful method for compensating the device for closed-loop gains below seven is to use lag-lead and lead networks as shown in Figure 1. The lead network is primarily concerned with compensating for loss of phase margin caused by distributed board capacitance and input capacitance, while lag-lead is mainly for optimizing transient response. Lead compensation modifies the feedback network and adds a zero to the overall transfer function. This increases the phase, but does not greatly change the gain magnitude. This zero improves the phase margin.

To determine components, it can be shown that the optimal conditions for amplifier stability occur when:

$$(R1)\ (C_{DIST}) = (R_F)\ (C_{LEAD}) \quad (1)$$

However, when the stability criteria is obtained, it should be noted that the actual bandwidth of the closed-loop amplifier will be reduced. Based on using a double-sided copper-clad printed circuit board with a distributed capacitance of 3.5pF and a unity gain configuration, C_{LEAD} would be 3.5pF. Another way of stating the relationship between the distributed capacitance closed-loop gain and the lead compensation capacitor is:

$$C_{LEAD} = C_{DIST}\ \frac{R1}{R_F} \quad (2)$$

When bandwidth is of primary concern, the lead compensation will usually be adequate. For closed-loop gains less than seven, lag-lead compensation is necessary for stability.

If transient response is also a factor in design, a lag-lead compensation network may be necessary (Reference Figure 1). For practical applications, the following equations can be used to determine proper lag-lead components:

$$\frac{R_F}{R1/R_{LAG}} \geq 7 \quad (3)$$

Therefore,

$$R_{LAG} \leq \frac{R_F}{7 - R_F/R1} \quad (4)$$

Using the above equation will insure a closed-loop gain of seven above the network break frequency. C_{LAG} may now be approximated using:

$$W_{LAG} \simeq \frac{2\pi\ (GBW)}{10}\ Rad/Sec \quad (5)$$

$$W_{LAG} = \frac{\pi\ (GBW)}{5}\ Rad/Sec \quad (6)$$

where

$$W_{LAG} = \frac{1}{(R_{LAG})\ (C_{LAG})} \quad (7)$$

therefore,

$$\frac{\pi\ (GBW)}{5} = \frac{1}{(R_{LAG})\ (C_{LAG})} \quad (8)$$

and

$$C_{LAG} = \frac{5}{\pi\ R_{LAG}\ (GBW)} \quad (9)$$

This method adds a pole and zero to the transfer function of the device, causing the actual open-loop gain and phase curve to be reshaped, thus creating a progressive improvement above the critical frequency where phase changes rapidly. (Near 70MHz, see Figures 2a and 2b.) But also, the lag-lead network can be adjusted to optimize gain peaking for transient responses. Therefore, rise time, overshoot, and settling time can be changed for various closed-loop gains. The result of using this technique is shown for a pulse amplifier in Figure 3.

USING PIN 12 COMPENSATION

An alternate method of external compensation is obtained by use of the NE/SE5539 frequency compensation pin. The circuits in Figure 4 show the correct way to use this pin. As can be seen, this method saves the use of one capacitor as compared to standard lag-lead and lead compensation as shown in Figure 1.

But, most importantly, both methods are equally effective; i.e., a good wide-band amplifier below 17dB, with control over ringing and overshoot. For example, inverting and non-inverting amplifier circuits using Pin 12 are shown in Figure 5. The corresponding pulse response for each circuit is shown in Figures 6 and 7 for the network values recommended. As shown by the response photos, the overshoot and settling time can be controlled by adjusting R_C and C_C. In damping the overshoot, rise time is slightly decreased. Also, the non-inverting configuration (Figure 6) gives a very fast response time compared to the inverting mode.

If it is important to reduce output offset voltage and noise, an additional capacitor, C_O, can be added in series with the resistor (R_C) across the inputs. This should be a large value to block DC but not affect the benefits of the compensation components at high frequencies. A value of 0.01μF as shown in Figure 8 is sufficient.

INTERNAL CHARACTERISTICS OF THE NE/SE5539

In order to better understand the compensation procedure, a detailed discussion of the amplifier follows.

The complete amplifier schematic is shown in Figure 9. To clarify the effect of the compensation pin, the schematic is split into five main parts as shown in Figure 10.

Each segment in Figure 10 is defined as follows: starting from the non-inverting input, Section A_1 is the amplification from the input to the base of transistor Q_4. A_2 is from the base of Q_4 to the summation point at the collector of Q_3. Furthermore, A_3 represents the gain from the non-inverting input to the summation point via the common emitter side of Q_2 and Q_3. Finally, B_F is the feedback factor of the positive feedback loop from the collector of Q_3 to the base of Q_4.

From Figure 10, it can be seen that the total gain (A_T) is:

$$A_T = \frac{A_1 A_2}{1 - (B_F A_2)} + A_3 (1 + B_F A_2)$$

Each term in this equation plays a role at different frequencies to determine the total transfer function of the device. Of particular importance is the pole in A_3 (near 340MHz) which causes a roll-off of 12dB/octave and loss of phase margin just before unity gain. This can be seen in the Bode plot in Figure 11a. To overcome this pole, a capacitor and resistor are connected as shown in Figures 12a and 12b. The compensation pin is connected to the emitter of Q_5, which is in an emitter-follower configuration. Therefore, a reactance connected to Pin 12 acts essentially as if it were connected at the base of Q_5. Since the capacitor is connected here, it is now a component of B_F and a zero is added to the transfer function. The resistor across the input pins controls overall gain and causes A_T to cross 0dB at a lower frequency; the capacitor in the feedback loop controls phase shift and gain peaking.

To further explain, Bode plots of open-loop response using varying capacitor values and corresponding pulse responses are shown in Figures 13a through 13f. The changes in gain and phase can readily be seen, as is the effect on bandwidth.

COMPUTER ANALYSIS

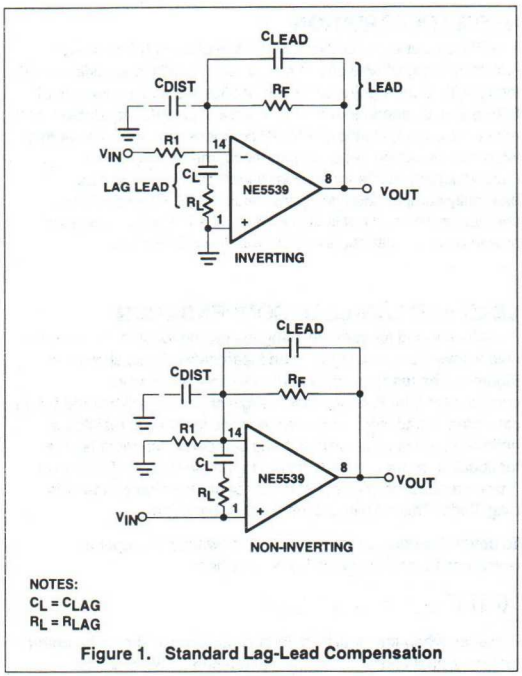
The open-loop and pulse response plots were generated using an IBM 370 computer and SPICE, a general-purpose circuit simulation program. Each transistor in the part is mathematically modeled after actual device parameters, which were measured in the laboratory. These models are then combined with the resistors and voltage sources through node numbers so that the computer knows where each is connected.

To indicate the accuracy of this system, the actual open-loop gain is compared to the computer plots in Figures 14 and 15. The real payoff for this system is that once a credible simulation is achieved, any outside circuit can be modeled around the op amp. This would be used to check for feasibility before breadboarding in the lab. The internal circuit can be treated like a black box and the outside circuit program altered to whatever application the user would like to examine.

1. J. Millman and C. C. Halkias: Integrated Electronics: Analog and Digital Circuits and Systems, McGraw-Hill Book Company, New York, 1972.

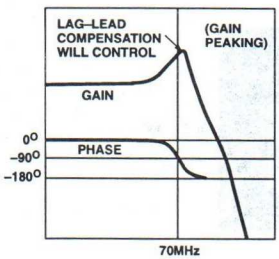
2. A. Vladimirescu, Kaihe Zhang, A. R. Newton, D. O. Peterson, A. Sanquiovanni-Vincentelli: "Spice Version 2G," University of California, Berkeley, California, August 10, 1981.

3. Philips Semiconductors: Analog Data Manual 1983, Philips Semiconductors Corporation, Sunnyvale, California 1983.

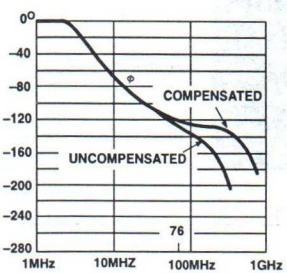


NOTES:
$C_L = C_{LAG}$
$R_L = R_{LAG}$

Figure 1. Standard Lag-Lead Compensation



a. Closed-Loop Inverting Gain of Seven Gain-Phase Response (Uncompensated)



b. Open-Loop Phase

Figure 2.

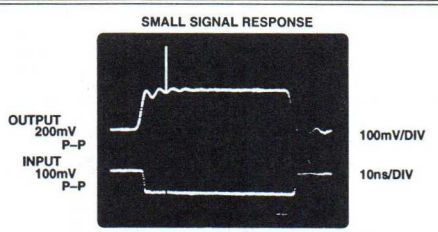
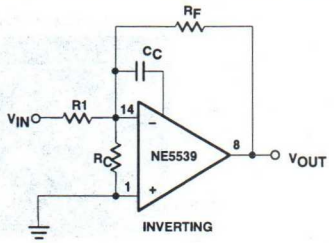


Figure 3. Compensated Pulse Response



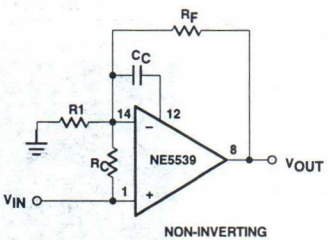


Figure 4. Pin 12 Compensation

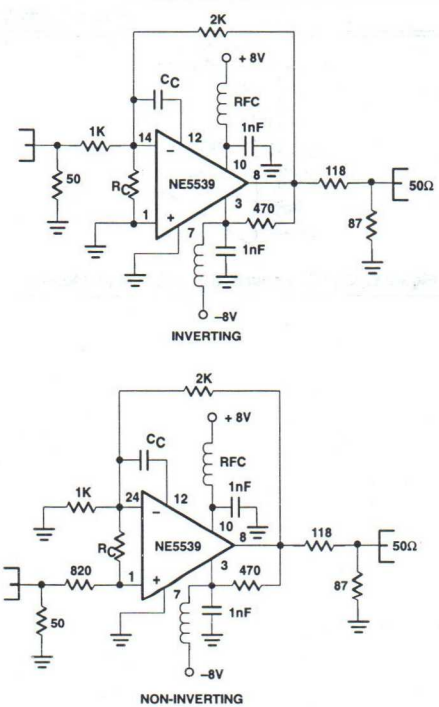


Figure 5. Pulse Response Test Circuits

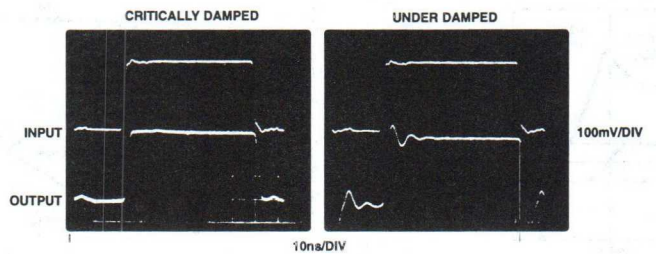


Figure 6. Small Signal Response – Non-Inverting

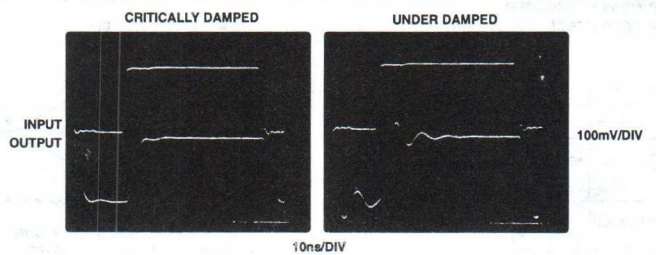


Figure 7. Small Signal Response – Inverting

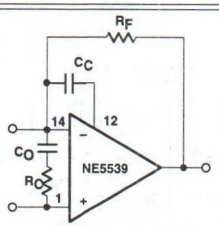


Figure 8. C_O Will Reduce Output Offset and Noise

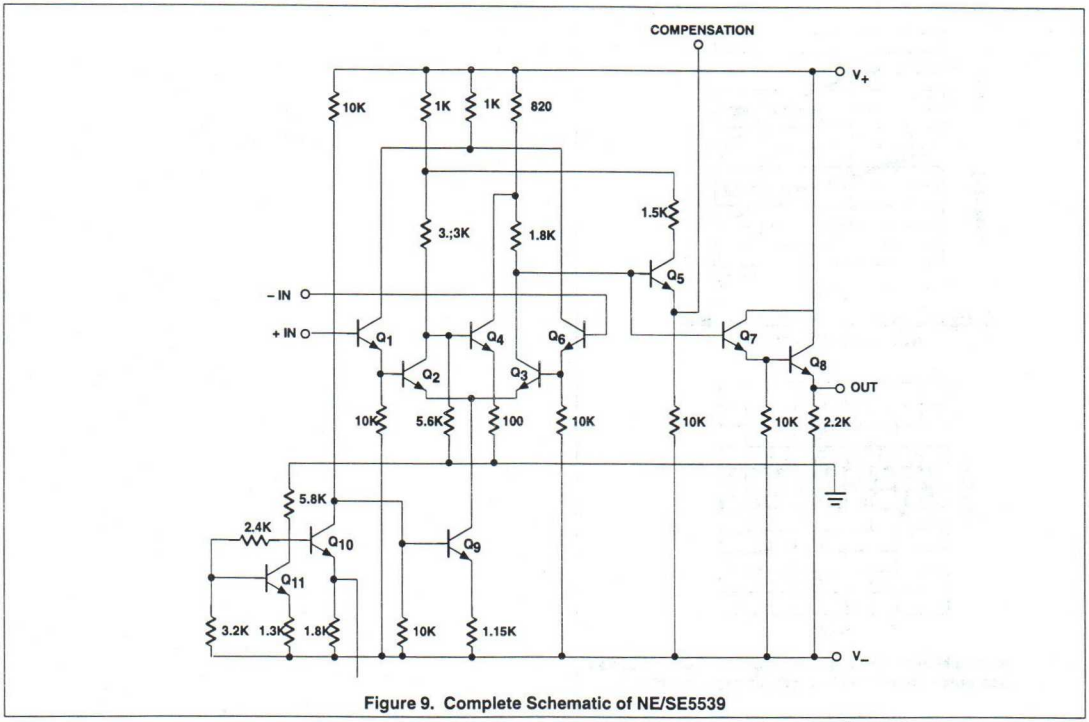


Figure 9. Complete Schematic of NE/SE5539

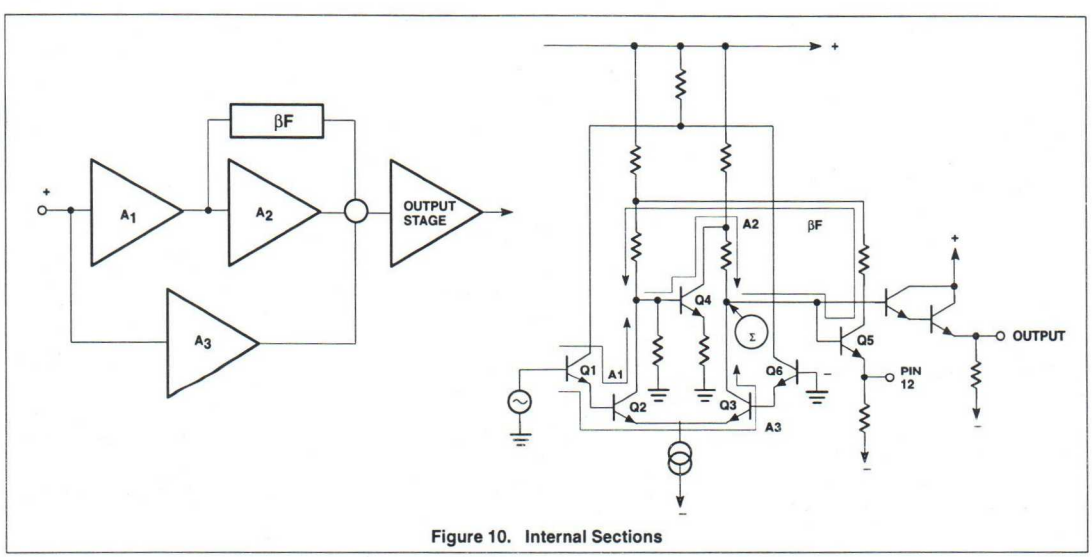
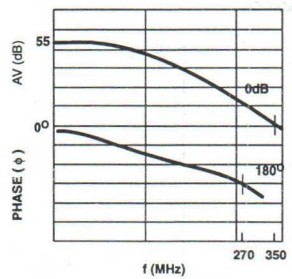
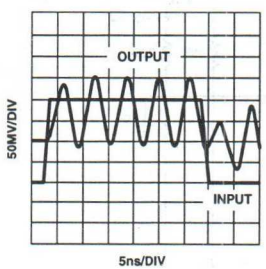


Figure 10. Internal Sections

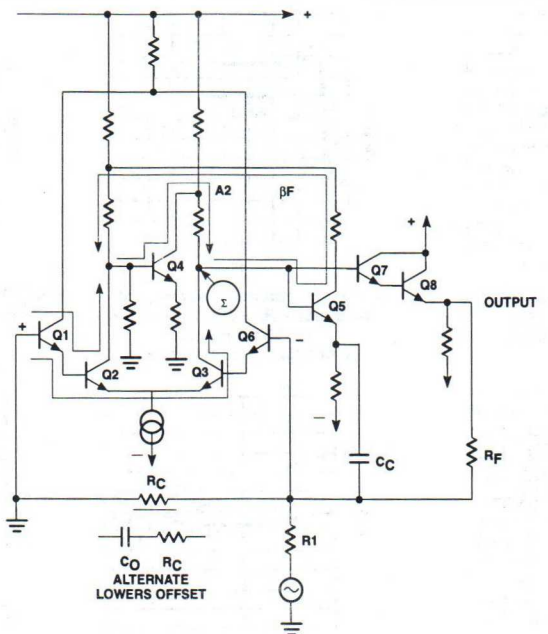


a. Open-Loop Gain – No Compensation
(Computer Simulation)

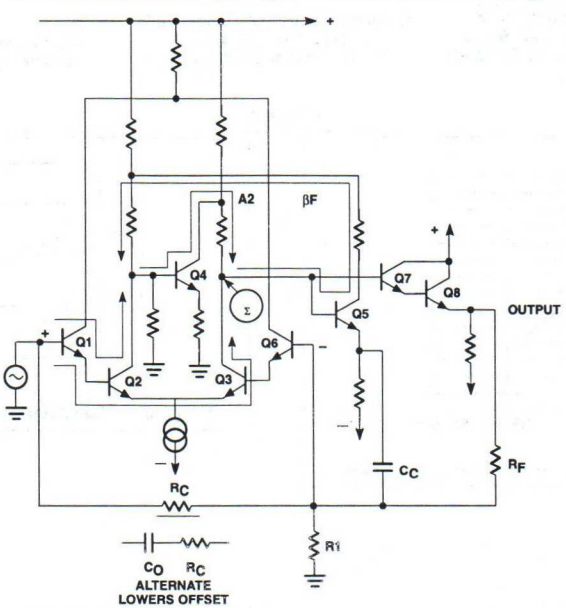


b. Closed-Loop Non-Inverting Response – No Compensation
(Computer Simulation – Oscillation is Evident)

Figure 11.

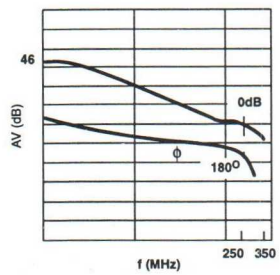


a. Pin 12 Compensation Showing Internal Connections – Inverting

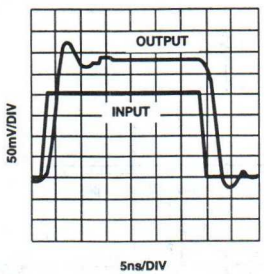


b. Pin 12 Compensation Showing Internal Connections – Non-Inverting

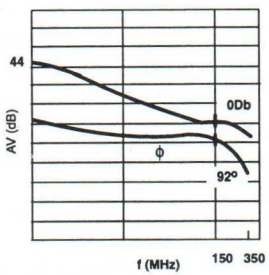
Figure 12.



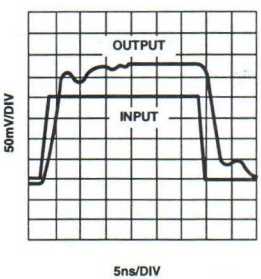
a. Open-Loop Pin 12 Compensation – R_C = 200Ω, C_C = 1pF, (Computer Simulation)



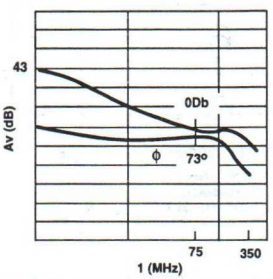
b. Closed-Loop Non-Inverting Pulse Response – R_C = 200Ω, C_C = 1pF, A_V = 3 (Computer Simulation – Underdamped)



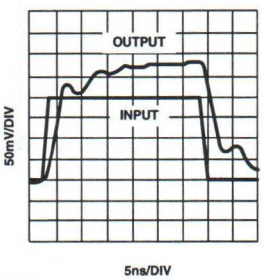
c. Open-Loop Pin 12 Compensation – R_C = 200Ω, C_C = 2pF (Computer Simulation)



d. Closed-Loop Non-Inverting Pulse Response – R_C = 200Ω, C_C = 2pF, A_V = 3 (Computer Simulation – Critically-Damped)



e. Open-Loop Pin 12 Compensation – R_C = 200Ω, C_C = 3pF, (Computer Simulation)



f. Closed-Loop Pulse Response – R_C = 200Ω, C_C = 3pF, A_V = 3 (Computer Simulation – Overdamped)

Figure 13.

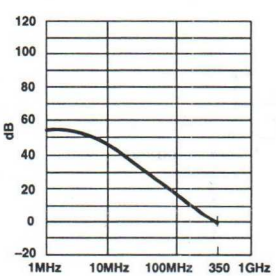


Figure 14. Actual Open–Loop Gain Measured in Lab

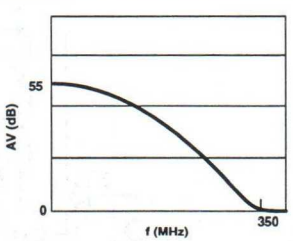


Figure 15. Computer–Generated Open–Loop Gain

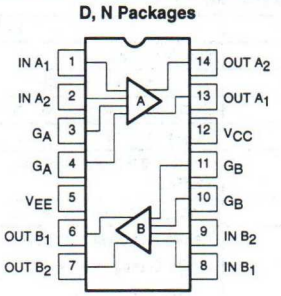
Video amplifier — NE5592

DESCRIPTION

The NE5592 is a dual monolithic, two-stage, differential output, wideband video amplifier. It offers a fixed gain of 400 without external components and an adjustable gain from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.

PIN CONFIGURATION

D, N Packages



FEATURES

- 110MHz unity gain bandwidth
- Adjustable gain from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Wave shaping with minimal external components

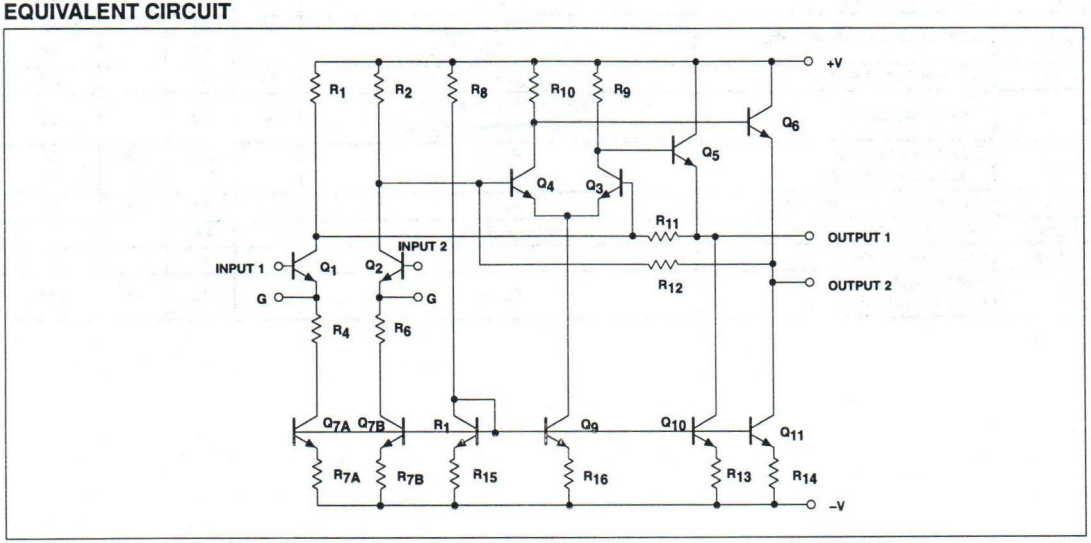
APPLICATIONS

- Floppy disk head amplifier
- Video amplifier
- Pulse amplifier in communications
- Magnetic memory
- Video recorder systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to 70°C	NE5592N	0405B
14-Pin Small Outline (SO) package	0 to 70°C	NE5592D	0175D

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common mode Input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating temperature range NE5592	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
$P_{D\ MAX}$	Maximum power dissipation, T_A=25°C (still air)[1] D package N package	 1.03 1.48	 W W

NOTES:

1. Derate above 25°C at the following rates:
   D package 8.3mW/°C
   N package 11.9mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=+25°C, V_{SS}=±6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltage is V_S = ±6.0V, and gain select pins are connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	R_L=2kΩ, V_{OUT}=3V_{P-P}	400	480	600	V/V
R_{IN}	Input resistance		3	14		kΩ
C_{IN}	Input capacitance			2.5		pF
I_{OS}	Input offset current			0.3	3	µA
I_{BIAS}	Input bias current			5	20	µA
	Input noise voltage	BW 1kHz to 10MHz		4		nV/√Hz
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	V_{CM} ± 1V, f<100kHz V_{CM} ± 1V, f=5MHz	60	93 87		dB dB
PSRR	Supply voltage rejection ratio	ΔV_S= ± 0.5V	50	85		dB
	Channel separation	V_{OUT}=1V_{P-P}; f=100kHz (output referenced) R_L=1kΩ	65	70		dB
V_{OS}	Output offset voltage gain select pins open	R_L=∞ R_L=∞		0.5 0.25	1.5 0.75	V V
V_{CM}	Output common-mode voltage	R_L=∞	2.4	3.1	3.4	V
V_{OUT}	Output differential voltage swing	R_L=2kΩ	3.0	4.0		V
R_{OUT}	Output resistance			20		Ω
I_{CC}	Power supply current (total for both sides)	R_L=∞		35	44	mA

DC ELECTRICAL CHARACTERISTICS

V_{SS}=±6V, V_{CM}=0, 0°C ≤ T_A ≤ 70°C, unless otherwise specified. Recommended operating supply voltage is V_S = ±6.0V, and gain select pins are connected together.

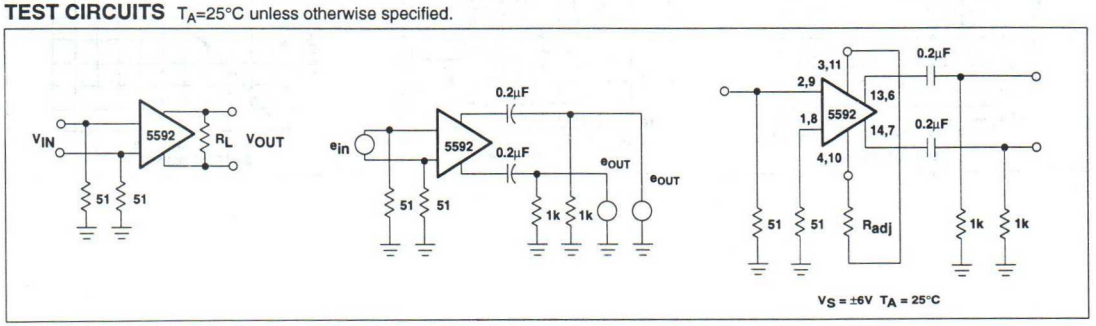
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	R_L=2kΩ, V_{OUT}=3V_{P-P}	350	430	600	V/V
R_{IN}	Input resistance		1	11		kΩ
I_{OS}	Input offset current				5	µA
I_{BIAS}	Input bias current				30	µA
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	V_{CM} ± 1V, f<100kHz R_S=ϕ	55			dB
PSRR	Supply voltage rejection ratio	ΔV_S= ± 0.5V	50			dB
	Channel separation	V_{OUT}=1V_{P-P}; f=100kHz (output referenced) R_L=1kΩ		70		dB
V_{OS}	Output offset voltage					
	gain select pins connected together	R_L=∞			1.5	V
	gain select pins open	R_L=∞			1.0	V
V_{OUT}	Output differential voltage swing	R_L=2kΩ	2.8			V
I_{CC}	Power supply current (total for both sides)	R_L=∞			47	mA

AC ELECTRICAL CHARACTERISTICS

T_A=+25°C V_{SS}=±6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltage V_S=±6.0V. Gain select pins connected together.

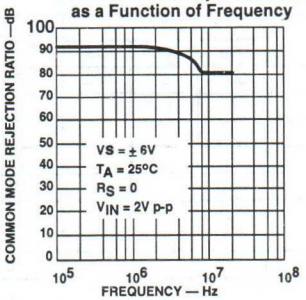
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
BW	Bandwidth	V_{OUT}=1V_{P-P}		25		MHz
t_R	Rise time			15	20	ns
t_{PD}	Propagation delay	V_{OUT}=1V_{P-P}		7.5	12	ns

TEST CIRCUITS T_A=25°C unless otherwise specified.

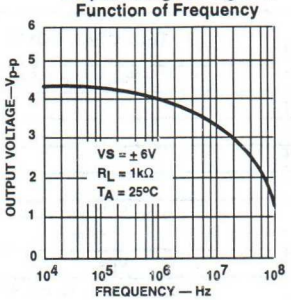


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

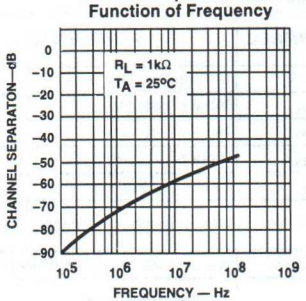
Common-Mode Rejection Ratio as a Function of Frequency



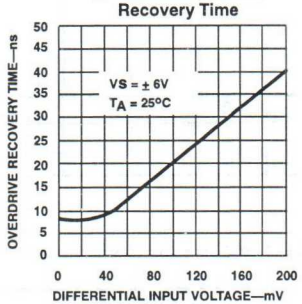
Output Voltage Swing as a Function of Frequency



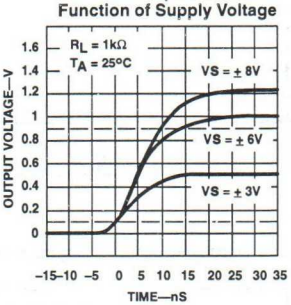
Channel Separation as a Function of Frequency



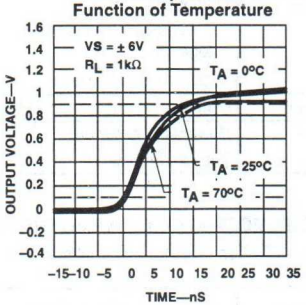
Differential Overdrive Recovery Time



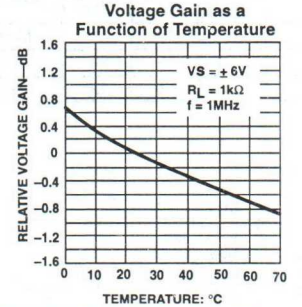
Pulse Response as a Function of Supply Voltage



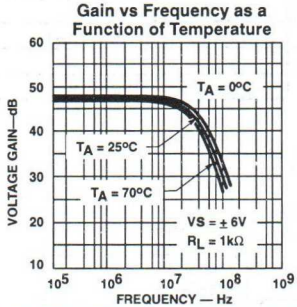
Pulse Response as a Function of Temperature



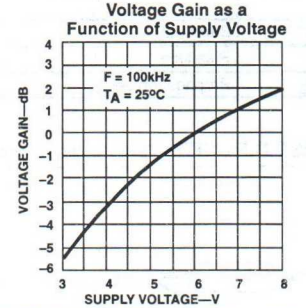
Voltage Gain as a Function of Temperature



Gain vs Frequency as a Function of Temperature

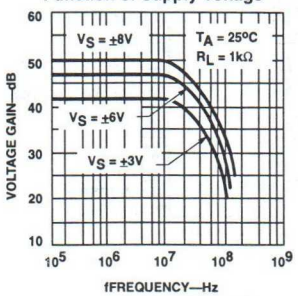


Voltage Gain as a Function of Supply Voltage

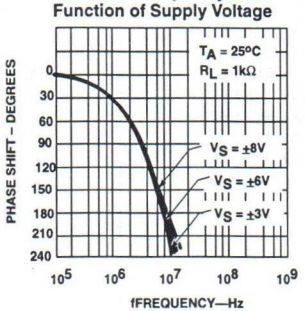


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

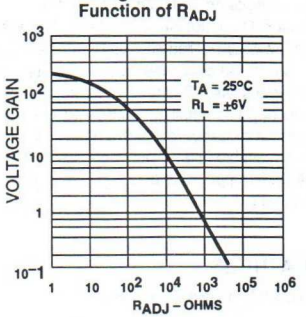
Gain vs Frequency as a Function of Supply Voltage



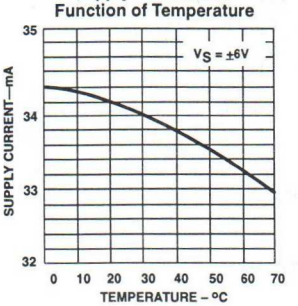
Phase vs Frequency as a Function of Supply Voltage



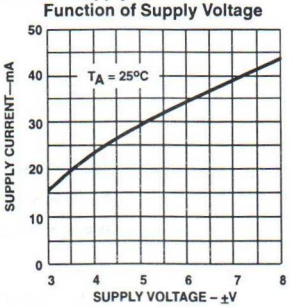
Voltage Gain as a Function of R_{ADJ}



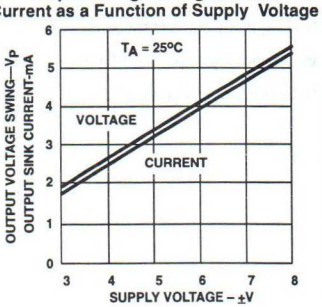
Supply Current as a Function of Temperature



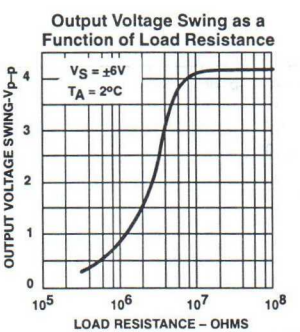
Supply Current as a Function of Supply Voltage



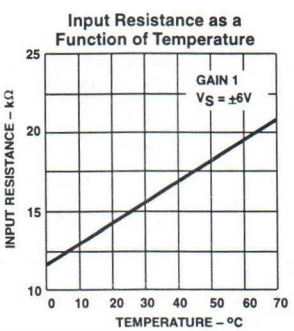
Output Voltage Swing and Sink Current as a Function of Supply Voltage



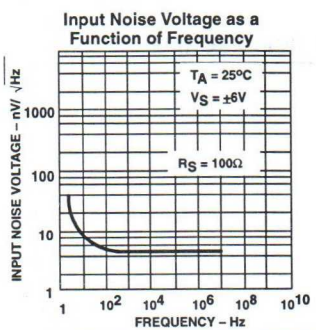
Output Voltage Swing as a Function of Load Resistance



Input Resistance as a Function of Temperature



Input Noise Voltage as a Function of Frequency



Video amplifier

NE592

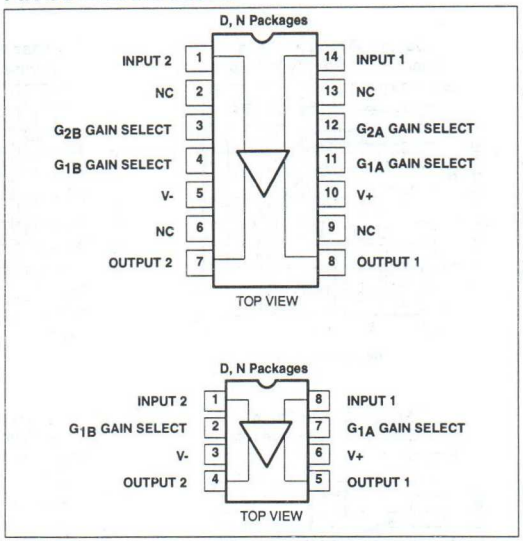
DESCRIPTION

The NE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers. Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor.

FEATURES

- 120MHz unity gain bandwidth
- Adjustable gains from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Wave shaping with minimal external components
- MIL-STD processing available

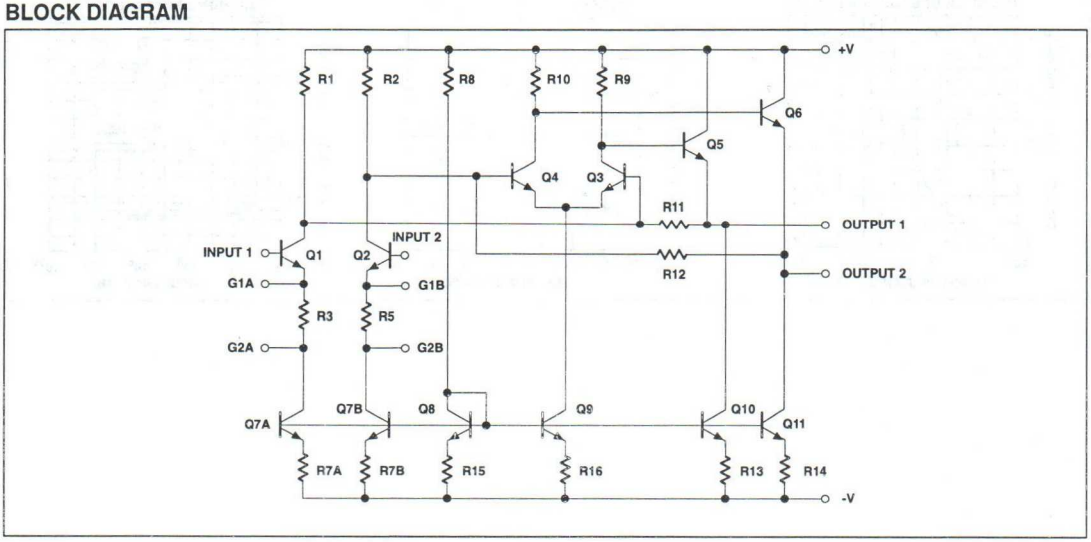
PIN CONFIGURATIONS



APPLICATIONS

- Floppy disk head amplifier
- Video amplifier
- Pulse amplifier in communications
- Magnetic memory
- Video recorder systems

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE592N14	0405B
14-Pin Small Outline (SO) package	0 to +70°C	NE592D14	0175D
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE592N8	0404B
8-Pin Small Outline (SO) package	0 to +70°C	NE592D8	0174C

NOTES:
N8, N14, D8 and D14 package parts also available in "High" gain version by adding "H" before package designation, i.e., NE592HDB

ABSOLUTE MAXIMUM RATINGS

T_A=+25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
$P_{D\ MAX}$	Maximum power dissipation,		
	T_A=25°C (still air)[1]		
	D-14 package	0.98	W
	D-8 package	0.79	W
	N-14 package	1.44	W
	N-8 package	1.17	W

NOTES:
1. Derate above 25°C at the following rates:
   D-14 package at 7.8mW/°C
   D-8 package at 6.3mW/°C
   N-14 package at 11.5mW/°C
   N-8 package at 9.3mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=+25°C V_{SS}=±6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltages V_S=±6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE592			UNIT
			Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part					
	Gain 1[1]	R_L=2kΩ, V_{OUT}=3V_{P-P}	250	400	600	V/V
	Gain 2[2, 4]		80	100	120	V/V
R_{IN}	Input resistance					
	Gain 1[1]			4.0		kΩ
	Gain 2[2, 4]		10	30		kΩ
C_{IN}	Input capacitance[2]	Gain 2[4]		2.0		pF
I_{OS}	Input offset current			0.4	5.0	μA
I_{BIAS}	Input bias current			9.0	30	μA
V_{NOISE}	Input noise voltage	BW 1kHz to 10MHz		12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio					
	Gain 2[4]	V_{CM}±1V, f<100kHz	60	86		dB
	Gain 2[4]	V_{CM}±1V, f=5MHz		60		dB
PSRR	Supply voltage rejection ratio					
	Gain 2[4]	ΔV_S=±0.5V	50	70		dB
V_{OS}	Output offset voltage					
	Gain 1	R_L=∞			1.5	V
	Gain 2[4]	R_L=∞			1.5	V
	Gain 3[3]	R_L=∞		0.35	0.75	V
V_{CM}	Output common-mode voltage	R_L=∞	2.4	2.9	3.4	V
V_{OUT}	Output voltage swing differential	R_L=2kΩ	3.0	4.0		V
R_{OUT}	Output resistance			20		Ω
I_{CC}	Power supply current	R_L=∞		18	24	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 14-pin version only.

DC ELECTRICAL CHARACTERISTICS

DC Electrical Characteristics V_{SS}=±6V, V_{CM}=0, 0°C ≤T_A≤70°C, unless otherwise specified. Recommended operating supply voltages V_S=±6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE592			UNIT
			Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part					
	Gain 1[1]	R_L=2kΩ, V_{OUT}=3V_{P-P}	250		600	V/V
	Gain 2[2, 4]		80		120	V/V
R_{IN}	Input resistance					
	Gain 2[2, 4]		8.0			kΩ
I_{OS}	Input offset current				6.0	µA
I_{BIAS}	Input bias current				40	µA
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio					
	Gain 2[4]	V_{CM}±1V, f<100kHz	50			dB
PSRR	Supply voltage rejection ratio					
	Gain 2[4]	ΔV_S=±0.5V	50			dB
V_{OS}	Output offset voltage					
	Gain 1	R_L=∞			1.5	V
	Gain 2[4]				1.5	
	Gain 3[3]				1.0	
V_{OUT}	Output voltage swing differential	R_L=2kΩ	2.8			V
I_{CC}	Power supply current	R_L=∞			27	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 14-pin versions only.

AC ELECTRICAL CHARACTERISTICS

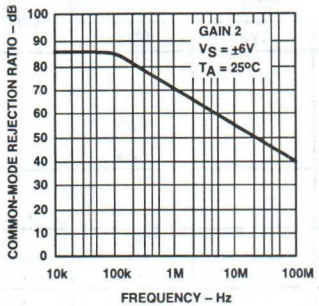
T_A=+25°C V_{SS}=±6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltages V_S=±6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			UNIT
			Min	Typ	Max	
BW	Bandwidth					
	Gain 1[1]			40		MHz
	Gain 2[2, 4]			90		MHz
t_R	Rise time					
	Gain 1[1]	V_{OUT}=1V_{P-P}		10.5	12	ns
	Gain 2[2, 4]			4.5		ns
t_{PD}	Propagation delay					
	Gain 1[1]	V_{OUT}=1V_{P-P}		7.5	10	ns
	Gain 2[2, 4]			6.0		ns

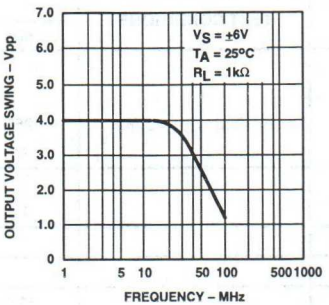
NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 14-pin versions only.

TYPICAL PERFORMANCE CHARACTERISTICS

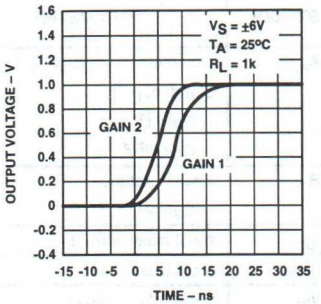
Common-Mode Rejection Ratio as a Function of Frequency



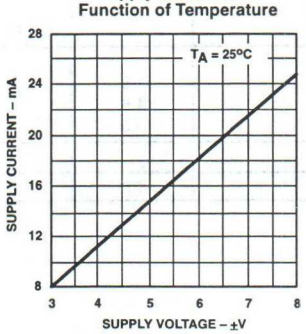
Output Voltage Swing as a Function of Frequency



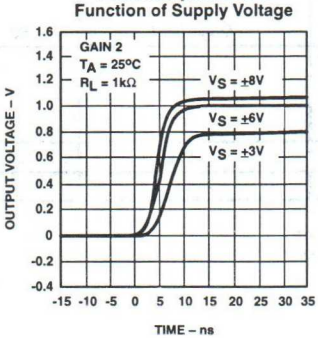
Pulse Response



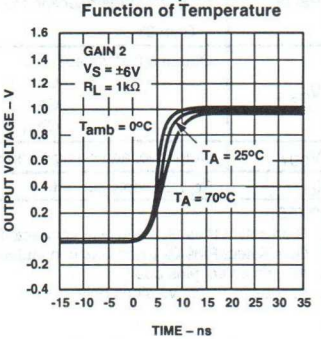
Supply Current as a Function of Temperature



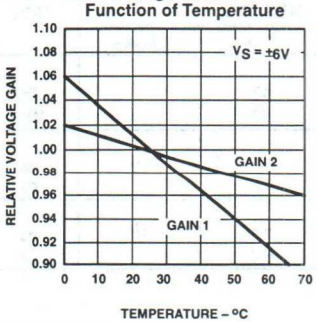
Pulse Response as a Function of Supply Voltage



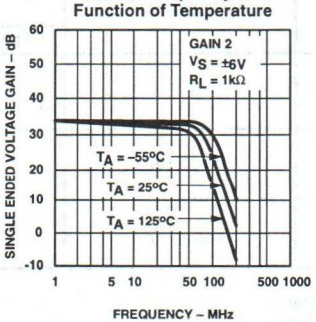
Pulse Response as a Function of Temperature



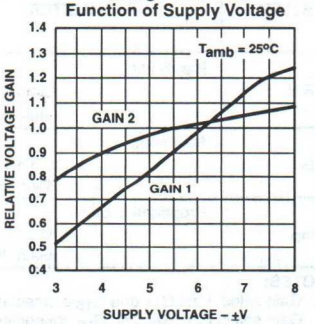
Voltage Gain as a Function of Temperature



Gain vs. Frequency as a Function of Temperature

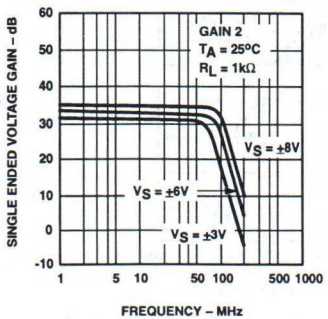


Voltage Gain as a Function of Supply Voltage

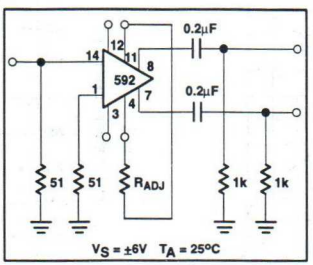


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

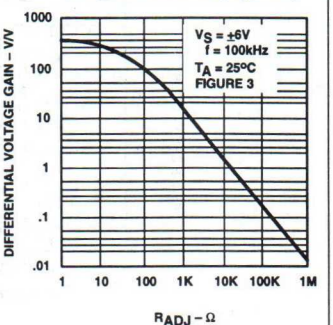
Gain vs. Frequency as a Function of Supply Voltage



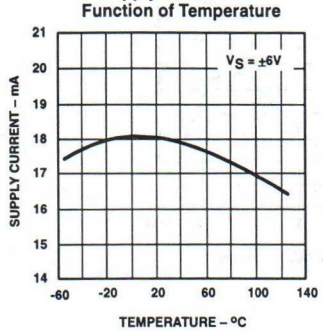
Voltage Gain Adjust Circuit



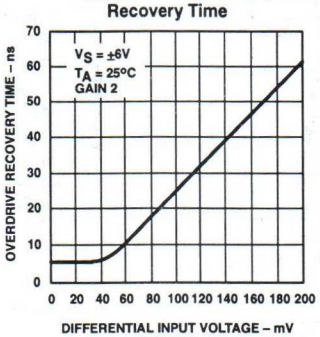
Voltage Gain as a Function of RADJ (Figure 3)



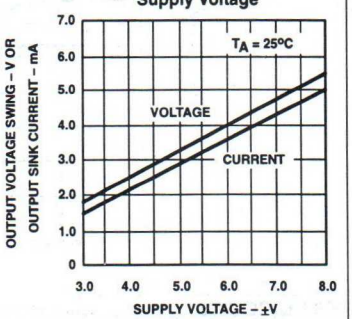
Supply Current as a Function of Temperature



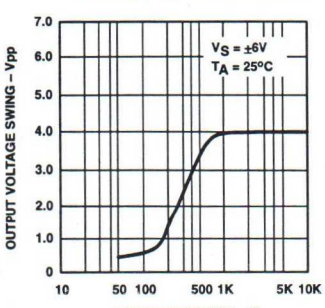
Differential Overdrive Recovery Time



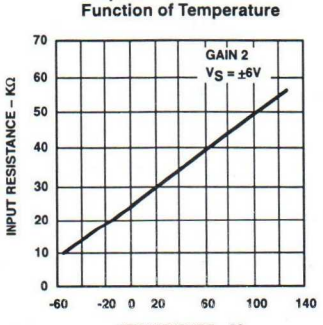
Output Voltage and Current Swing as a Function of Supply Voltage



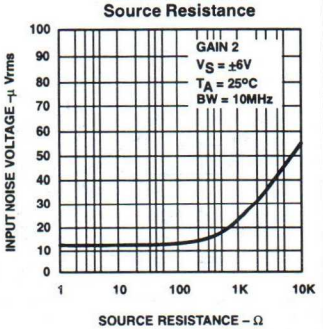
Output Voltage Swing as a Function of Load Resistance

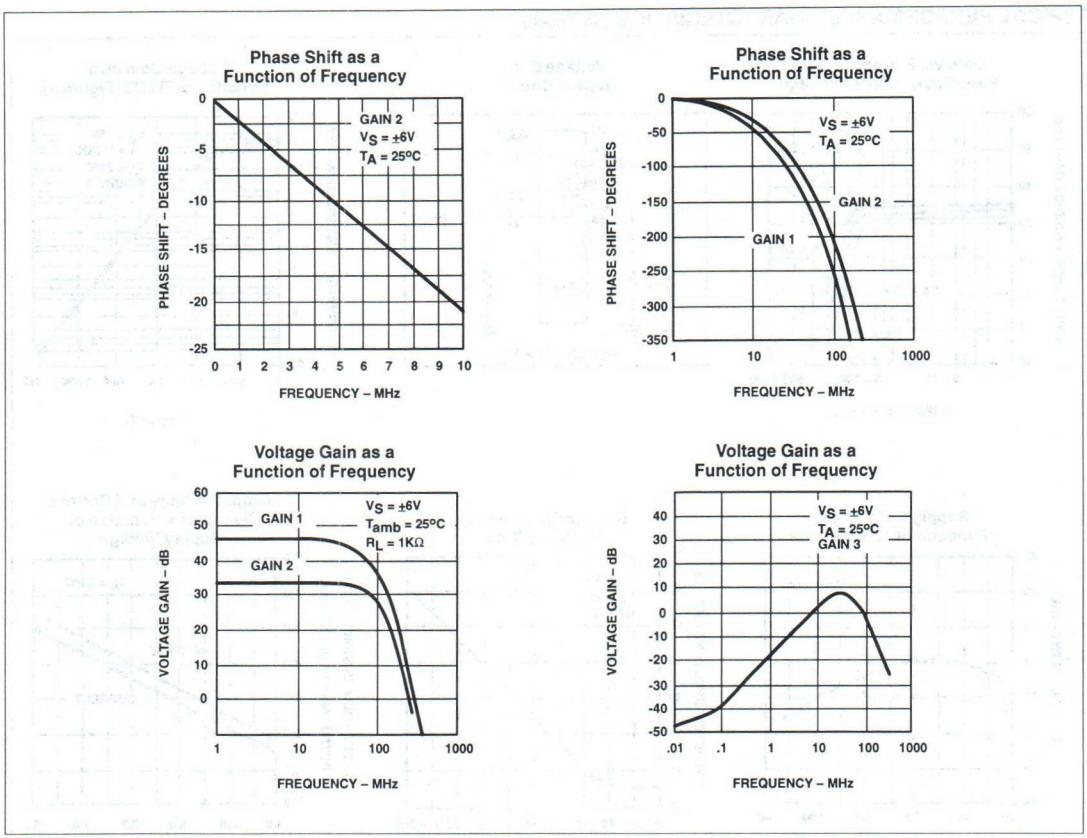


Input Resistance as a Function of Temperature

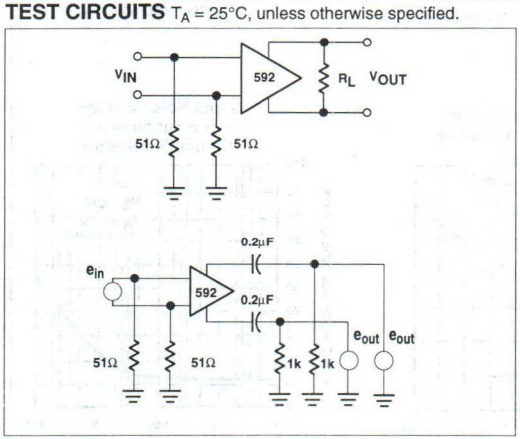


Input Noise Voltage as a Function of Source Resistance





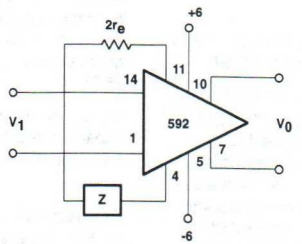
TEST CIRCUITS T_A = 25°C, unless otherwise specified.



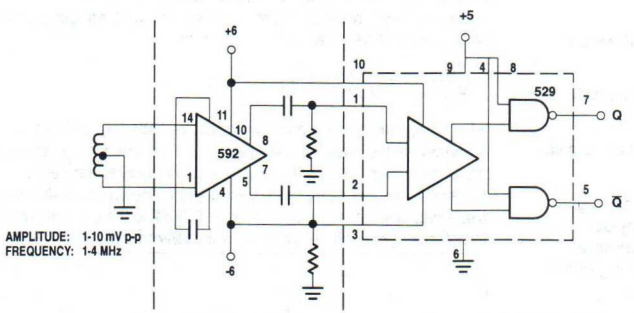
TYPICAL APPLICATIONS

NOTE:

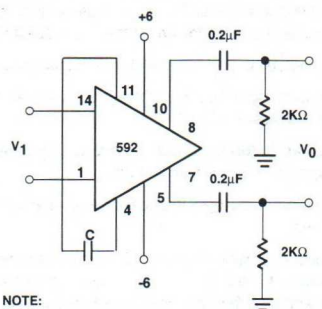
$$\frac{V_0(s)}{V_1(s)} \simeq \frac{1.4 \cdot 10^4}{Z(S) + 2r_e} \simeq \frac{1.4 \cdot 10^4}{Z(S) + 32}$$



Basic Configuration



Disc/Tape Phase-Modulated Readback Systems

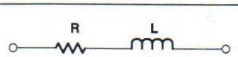
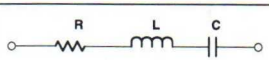
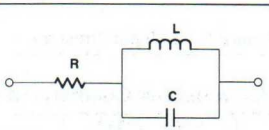


NOTE:
For frequency $F_1 << 1/2\pi$ (32) C

$$V_O \simeq 1.4 \times 10^4 C \frac{dVi}{dT}$$

Differentiation with High Common-Mode Noise Rejection

FILTER NETWORKS

Z NETWORK	FILTER TYPE	V_0 (s) TRANSFER V_1 (s) FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L} \left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R} \left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L} \left[\frac{s}{s^2 + R/Ls + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R} \left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTES:
In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.
$S = j\omega$
$\omega = 2\pi f$

Using the NE/SA/SE592 video amplifier

AN141

VIDEO AMPLIFIER PRODUCTS

NE/SA/SE592 Video Amplifier

The 592 is a two-stage differential output, wide-band video amplifier with voltage gains as high as 400 and bandwidths up to 120MHz.

Three basic gain options are provided. Fixed gains of 400 and 100 result from shorting together gain select pins G_{1A}-G_{1B} and G_{2A}-G_{2B}, respectively. As shown by Figure 1, the emitter circuits of the differential pair return through independent current sources. This topology allows no gain in the input stage if all gain select pins are left open. Thus, the third gain option of tying an external resistance across the gain select pins allows the user to select any desired gain from 0 to 400V/V. The advantages of this configuration will be covered in greater detail under the filter application section.

Three factors should be pointed out at this time:

1. The gains specified are differential. Single-ended gains are one-half the stated value.
2. The circuit 3dB bandwidths are a function of and are inversely proportional to the gain settings.
3. The differential input impedance is an inverse function of the gain setting.

In applications where the signal source is a transformer or magnetic transducer, the input bias current required by the 592 may be passed directly through the source to ground. Where capacitive coupling is to be used, the base inputs must be returned to ground through a resistor to provide a DC path for the bias current.

Due to offset currents, the selection of the input bias resistors is a compromise. To reduce the loading on the source, the resistors should be large, but to minimize the output DC offset, they should be small—ideally 0Ω. Their maximum value is set by the maximum allowable output offset and may be determined as follows:

1. Define the allowable output offset (assume 1.5V).
2. Subtract the maximum 592 output offset (from the data sheet). This gives the output offset allowed as a function of input offset currents (1.5V-1.0V=0.5V).
3. Divide by the circuit gain (assume 100). This refers the output offset to the input.
4. The maximum input resistor size is:

$$R_{MAX} = \frac{\text{Input Offset Voltage}}{\text{Max Input Offset Curent}} \quad (1)$$

$$= \frac{0.005V}{5\mu A}$$

$$= 1.00k\Omega$$

Of paramount importance during the design of the NE592 device was bandwidth. In a monolithic device, this precludes the use of PNP transistors and standard level-shifting techniques used in lower frequency devices. Thus, without the aid of level shifting, the output common-mode voltage present on the NE592 is typically 2.9V. Most applications, therefore, require capacitive coupling to the load.

Filters

As mentioned earlier, the emitter circuit of the NE592 includes two current sources.

Since the stage gain is calculated by dividing the collector load impedance by the emitter impedance, the high impedance contributed by the current sources causes the stage gain to be zero with all gain select pins open. As shown by the gain vs. frequency graph of Figure 2, the overall gain at low frequencies is a negative 48dB.

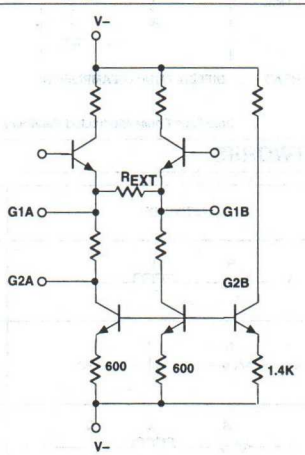
Higher frequencies cause higher gain due to distributed parasitic capacitive reactance. This reactance in the first stage emitter circuit causes increasing stage gain until at 10MHz the gain is 0dB, or unity.

Referring to Figure 3, the impedance seen looking across the emitter structure includes small r_e of each transistor.

Any calculations of impedance networks across the emitters then must include this quantity. The collector current level is approximately 2mA, causing the quantity of 2 r_e to be approximately 40Ω. Overall device gain is thus given by

$$\frac{V_O\ (s)}{V_{IN}\ (s)} = \frac{1.6x10^4}{Z_{IN}(s) + 40} \quad (2)$$

where $Z_{(S)}$ can be resistance or a reactive impedance. Table 2 summarizes the possible configurations to produce low, high, and bandpass filters. The emitter impedance is made to vary as a function of frequency by using capacitors or inductors to alter the frequency response. Included also in Table 2 is the gain calculation to determine the voltage gain as a function of frequency.



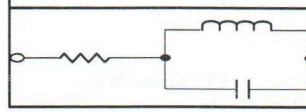
NOTE:
All resistor values are in ohms.

Figure 1. 592 Input Structure

Table 1. Video Amplifier Comparison File

PARAMETER	NE/SA/SE592	733
Bandwidth (MHz)	120	120
Gain	0,100,400	10,100,400
R_{IN} (k)	4-30	4-250
V_{P-P} (V_S)	4.0	4.0

Table 2. Filter Networks

Z Network	Filter Type	$\frac{V_O(s)\ \text{TRANSFER}}{V_1(s)\ \text{FUNCTION}}$
	Low Pass	$\frac{1.6 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	High Pass	$\frac{1.6 \times 10^4}{R}\left[\frac{S}{s + 1/RC}\right]$
	Band Pass	$\frac{1.6 \times 10^4}{L}\left[\frac{S}{s^2 + R/Ls + 1/LC}\right]$
	Band Reject	$\frac{1.6 \times 10^4}{R}\left[\frac{S^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTES:
In the networks above, the R value used is assumed to include 2 r_e, or approximately 40Ω.
S=jΩ
Ω=2πf

Differentiation

With the addition of a capacitor across the gain select terminals, the NE592 becomes a differentiator. The primary advantage of using the emitter circuit to accomplish differentiation is the retention of the high common mode noise rejection. Disc file playback systems rely heavily upon this common-mode rejection for proper operation. Figure 4 shows a differential amplifier configuration with transfer function.

Disc File Decoding

In recovering data from disc or drum files, several steps must be taken to precondition the linear data. The NE592 video amplifier, coupled with the 8T20 bidirectional one-shot, provides all the signal conditioning necessary for phase-encoded data.

When data is recorded on a disc, drum or tape system, the readback will be a Gaussian shaped pulse with the peak of the pulse corresponding to the actual recorded transition point. This readback signal is usually 500μV_{P-P} to 3mV_{P-P} for oxide coated disc files and 1 to 20mV_{P-P} for nickel-cobalt disc files. In order to accurately reproduce the data stream originally written on the disc memory, the time of peak point of the Gaussian readback signal must be determined.

The classical approach to peak time determination is to differentiate the input signal. Differentiation results in a voltage proportional to the slope of the input signal. The zero-crossing point of the differentiator, therefore, will occur when the input signal is at a peak. Using a zero-crossing detector and one-shot, therefore, results in pulses occurring at the input peak points.

A circuit which provides the preconditioning described above is shown in Figure 5. Readback data is applied directly to the input of the first NE592. This amplifier functions as a wide-band AC-coupled amplifier with a gain of 100. The NE592 is excellent for this use because of its high phase linearity, high gain and ability to directly couple the unit with the readback head. By direct coupling of readback head to amplifier, no matched terminating resistors are required and the excellent common-mode rejection ratio of the amplifier is preserved. DC components are also rejected because the NE592 has no gain at DC due to the capacitance across the gain select terminals.

The output of the first stage amplifier is routed to a linear phase shift low-pass filter. The filter is a single-stage constant K filter, with a characteristic impedance of 200Ω. Calculations for the filter are as follows:

$$L = \frac{2R}{\omega C}$$

where

R = charachteristic impedance (Ω)

$$C = \frac{1}{\omega C}$$

where

ωC = cut – off frequency (radians/sec)

The second NE592 is utilized as a low noise differentiator/amplifier stage. The NE592 is excellent in this application because it allows differentiation with excellent common-mode noise rejection.

The output of the differentiator/amplifier is connected to the 8T20 bidirectional monostable unit to provide the proper pulses at the zero-crossing points of the differentiator.

The circuit in Figure 5 was tested with an input signal approximating that of a readback signal. The results are shown in Figure 7.

AUTOMATIC GAIN CONTROL

The NE592 can also be connected in conjunction with a MC1496 balanced modulator to form an excellent automatic gain control system.

The signal is fed to the signal input of the MC1496 and RC-coupled to the NE592. Unbalancing the carrier input of the MC1496 causes the signal to pass through unattenuated. Rectifying and filtering one of the NE592 outputs produces a DC signal which is proportional to

the AC signal amplitude. After filtering; this control signal is applied to the MC1496 causing its gain to change.

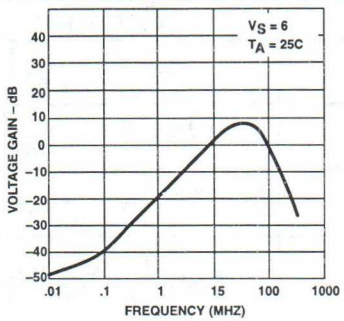
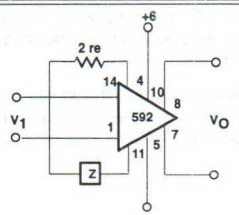


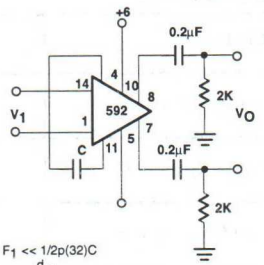
Figure 2. Voltage Gain as a Function of Frequency (All Gain Select Pins Open)



NOTE:

$$\frac{V_O(S)}{V_T(S)} = \frac{1.6 \times 10^4}{Z(s) + 2re} = \frac{1.6 \times 10^4}{Z(s) + 40}$$

Figure 3. Basic Gain Configuration for NE592, N14



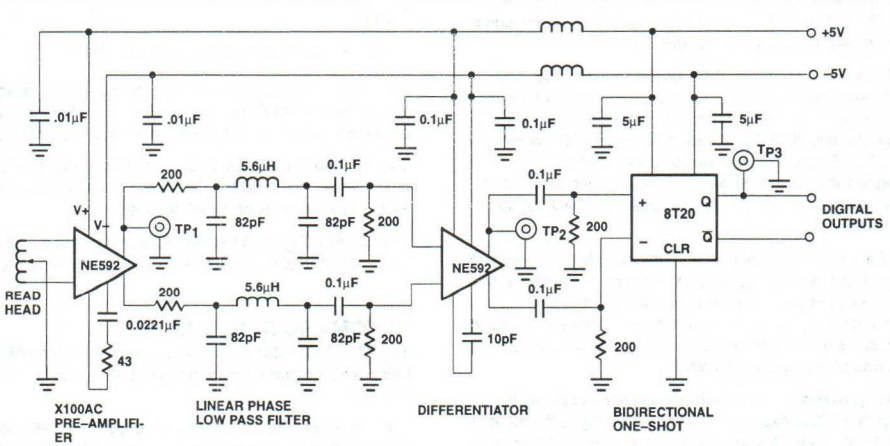
NOTES:

For frequency $F_1 << 1/2p(32)C$

$$V_O \approx 1.6 \times 10^4 C \frac{d_{vi}}{d_T}$$

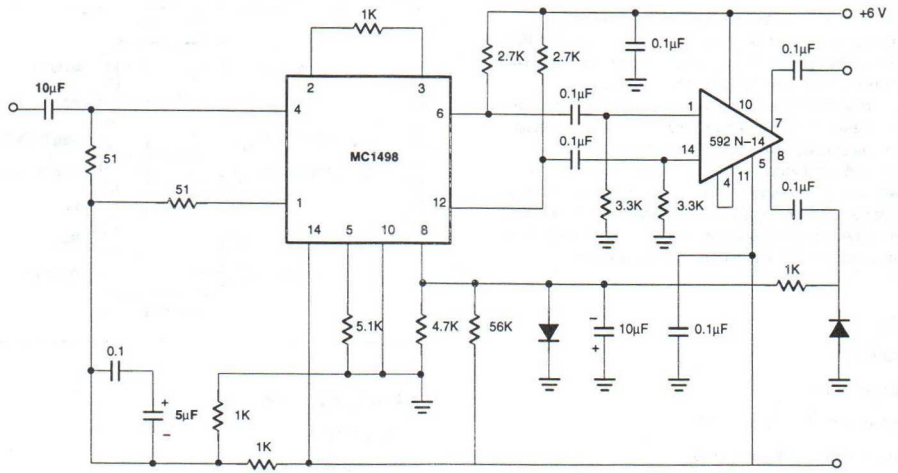
All resistor values are in ohms.

Figure 4. Differential with High Common-Mode Noise Rejection



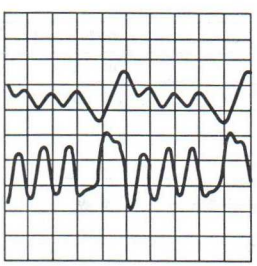
NOTE:
All resistor values are in ohms.

Figure 5. 5MHz Phase-Encoded Data Read Circuitry



NOTE:
All resistor values are in ohms.

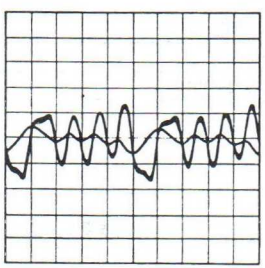
Figure 6. Wide-band AGC Amplifier



PRE-AMPLIFIER OUTPUT
100mV/DIV.

DIFFERENTIATOR
200mV/DIV.

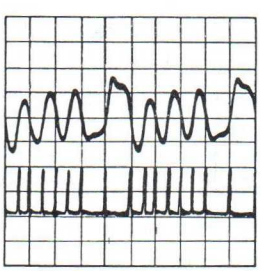
TIME BASE 200ns/DIV.



PRE-AMP AND DIFFERENTIATOR
SUPER IMPOSED

BOTH 200mV/DIV.

TIME BASE 200ns/DIV.



DIFFERENTIATOR
200mV/DIV.

8T20 Q OUTPUT
2V/DIV.

TIME BASE 200ns/DIV.

Figure 7. Test Results of Disc File Decoder Circuit

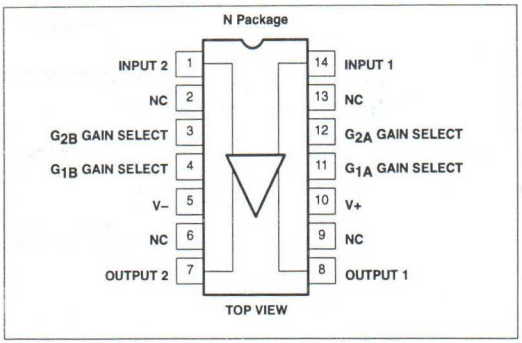
Differential video amplifier

µA733/733C

DESCRIPTION

The 733 is a monolithic differential input, differential output, wide-band video amplifier. It offers fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth, and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter-follower outputs to the inputs of the second stage. The emitter-follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high-performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

PIN CONFIGURATION



FEATURES

- 120MHz bandwidth
- 250kΩ input resistance
- Selectable gains of 10, 100, and 400
- No frequency compensation required
- MIL-STD-883A, B, C available

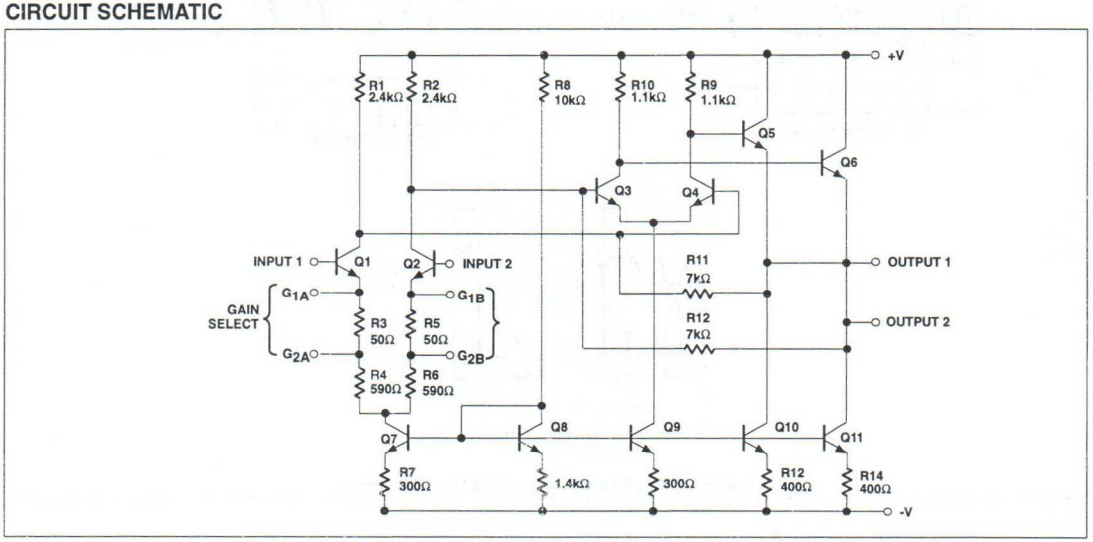
APPLICATIONS

- Video amplifier
- Pulse amplifier in communications
- Magnetic memories
- Video recorder systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE	ORDER CODE	DWG #
14-Pin Plastic Dual In–Line Package (DIP)	-55°C to +125°C	µA733N	0405B
14-Pin Plastic Dual In–Line Package (DIP)	0 to +70°C	µA733CN	0405B

CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DIFF}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
V_{CC}	Supply voltage	±8	V
I_{OUT}	Output current	10	mA
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range		
	µA733C	0 to +70	°C
	µA733	-55 to +125	°C
$P_{D\ MAX}$	Maximum power dissipation, 25°C ambient temperature (still-air)[1]	1420	mW

NOTE:
1. The following derating factors should be applied above 25°C:
   N package at 11.4mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=+25°C, V_S=±6V, V_{CM}=0, unless otherwisespecified. Recommended operating supply voltages V_S=±6.0V.

SYMBOL	PARAMETER	TEST CONDITIONS	µA733C			µA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Differential voltage gain	R_l = 2kΩ, V_{OUT} = 3V_{P-P}							
	Gain 1[2]		250	400	600	300	400	500	V/V
	Gain 2[2]		80	100	120	90	100	110	V/V
	Gain 3[3]		8	10	12	9	10	11	V/V
	Gain 1[1]			40			40		
BW	Gain 2[2]			90			90		MHz
	Gain 3[3]			120			120		
t_R		V_{OUT} = 1V_{P-P}							
	Gain 1[1]			10.5			10.5		ns
	Gain 2[2]			4.5	12		4.5	10	ns
	Gain 3[3]			2.5			2.5		ns
t_{PD}		V_{OUT} = 1V_{P-P}							
	Gain 1[1]			7.5			7.5		ns
	Gain 2[2]			6.0	10		6.0	10	ns
	Gain 3[3]			3.6			3.6		ns
R_{IN}									
	Gain 1[2]			4.0			4.0		kΩ
	Gain 2[2]		10	30		20	30		kΩ
	Gain 3[3]			250			250		kΩ
	Input capacitance[2]	Gain 2		2.0			2.0		pF
I_{OS}	Input offset current			0.4	5.0		0.4	3.0	µA
I_{BIAS}	Input bias current			9.0	30		9.0	20	µA
V_{NOISE}	Input noise voltage	BW=1kHz to 10MHz		12			12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR									
	Gain 2	V_{CM}=±1V, f≤100kHz	60	86		60	86		dB
	Gain 2	V_{CM}=±1V, f=5MHz		60			60		dB

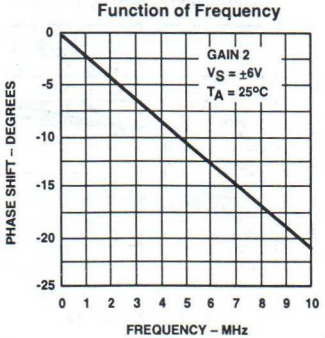
DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	µA733C			µA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
SVRR	Supply voltage rejection ratio Gain 2	$\Delta V_S = \pm 0.5V$	50	70		50	70		dB
	Output offset voltage	$R_L = \infty$							
	Gain 1[1]			0.6	1.5		0.6	1.5	V
	Gain 2 and 3[2, 3]			0.35	1.5		0.35	1.0	V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
	Output voltage swing, differential	R_L=2kΩ	3.0	4.0		3.0	4.0		V_{P-P}
I_{SINK}	Output sink current		2.5	3.6		2.5	3.6		mA
R_{OUT}	Output resistance			20			20		Ω
I_{CC}	Power supply current	$R_L = \infty$		18	24		18	24	mA
THE FOLLOWING SPECIFICATIONS APPLY OVER TEMPERATURE			**0°C ≤ T_A ≤ 70°C**			**-55°C ≤ T_A ≤ 125°C**			
			Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**UNIT**
	Differential voltage gain	R_l = 2kΩ, $V_{OUT} = 3V_{P-P}$							
	Gain 1[1]		250		600	200		600	V/V
	Gain 2[2]		80		120	80		120	V/V
	Gain[3]		8		12	8		12	V/V
R_{IN}	Input resistance								
	Gain 2[2]		8			8			kΩ
I_{OS}	Input offset current				6			5	µA
I_{BIAS}	Input bias current				40			40	µA
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2	V_{CM}=±V, F≤100kHz	50			50			dB
SVRR	Supply voltage rejection ratio								
	Gain 2	ΔV_S=±0.5V	50			50			dB
V_{OS}	Output offset voltage	$R_L = \infty$							
	Gain 1[1]				1.5			1.5	V
	Gain 2 and 3[2, 3]				1.5			1.2	V
V_{DIFF}	Output voltage swing, differential	R_L = 2kΩ	2.8			2.5			V_{P-P}
I_{SINK}	Output sink current		2.5			2.2			mA
I_{CC}	Power supply current	$R_L \pm \infty$			27			27	mA

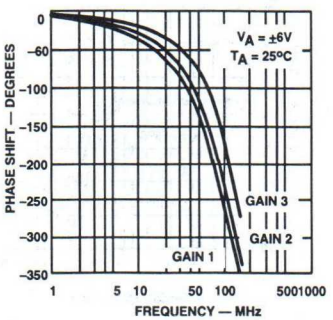
NOTES:
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

TYPICAL PERFORMANCE CHARACTERISTICS

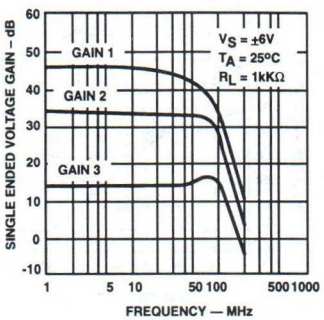
Phase Shift as a Function of Frequency



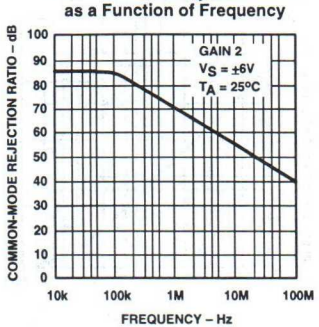
Phase Shift as a Function of Frequency



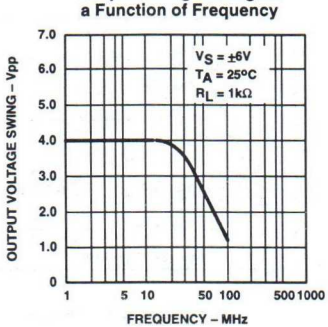
Voltage Gain as a Function of Temperature



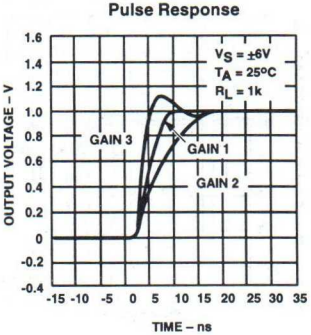
Common-Mode Rejection Ratio as a Function of Frequency



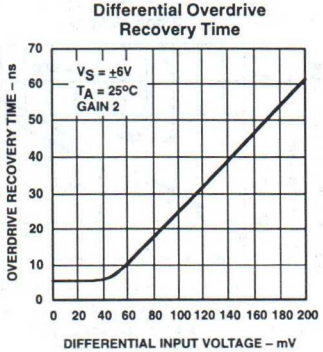
Output Voltage Swing as a Function of Frequency



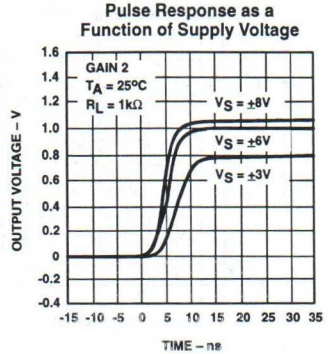
Pulse Response



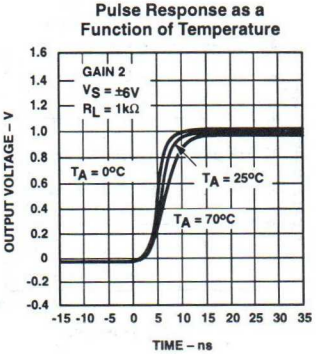
Differential Overdrive Recovery Time



Pulse Response as a Function of Supply Voltage

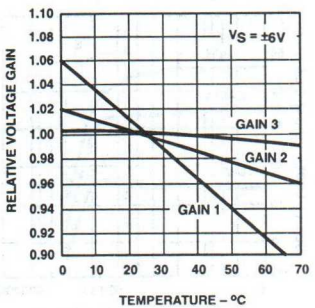


Pulse Response as a Function of Temperature

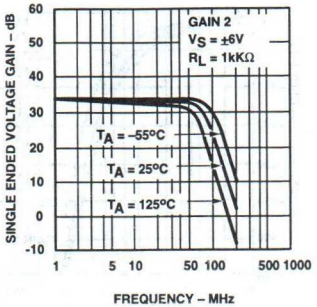


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

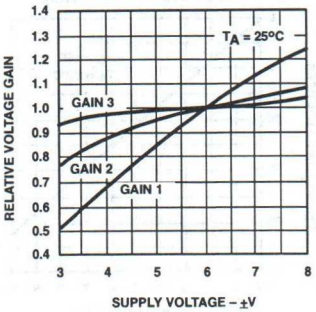
Voltage Gain as a Function of Temperature



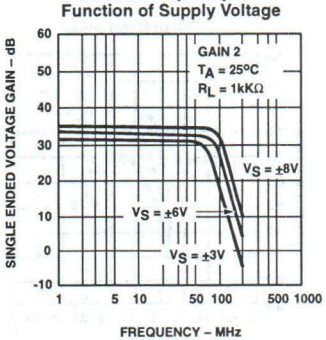
Gain vs. Frequency as a Function of Temperature



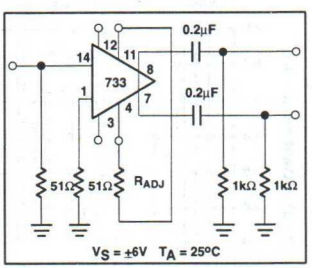
Voltage Gain as a Function of Supply Voltage



Gain vs. Frequency as a Function of Supply Voltage

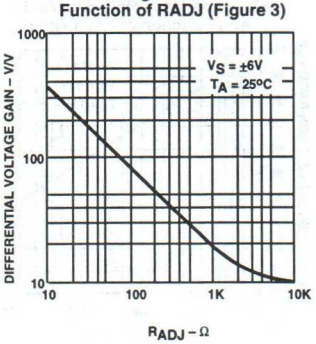


Voltage Gain Adjust Circuit

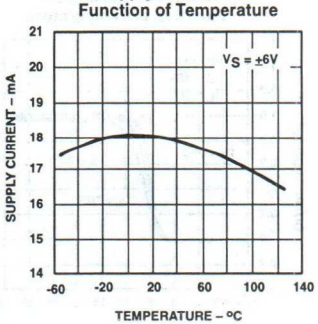


(Pin numbers apply to K Package)

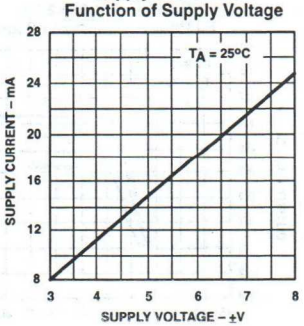
Voltage Gain as a Function of RADJ (Figure 3)



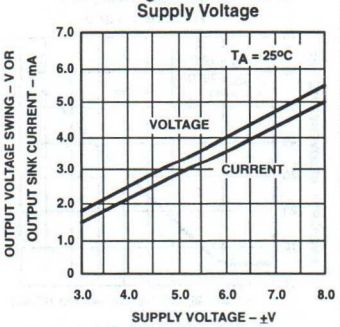
Supply Current as a Function of Temperature



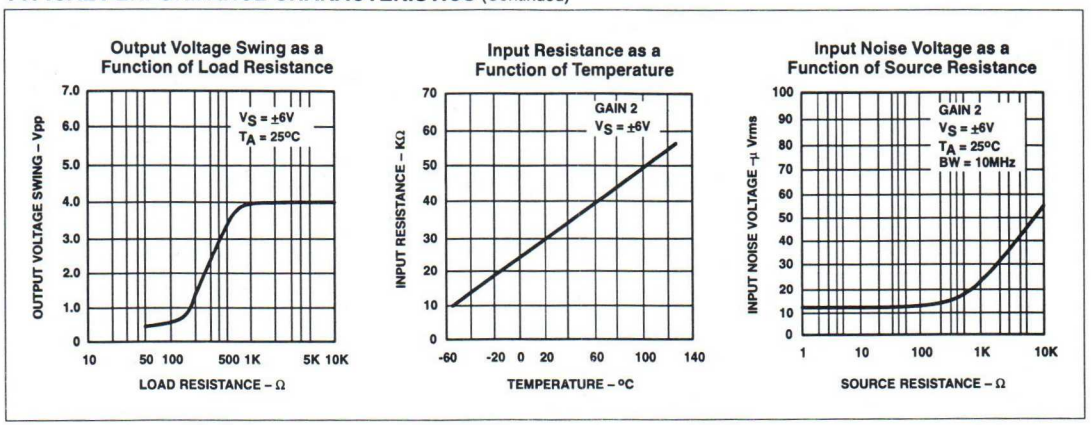
Supply Current as a Function of Supply Voltage



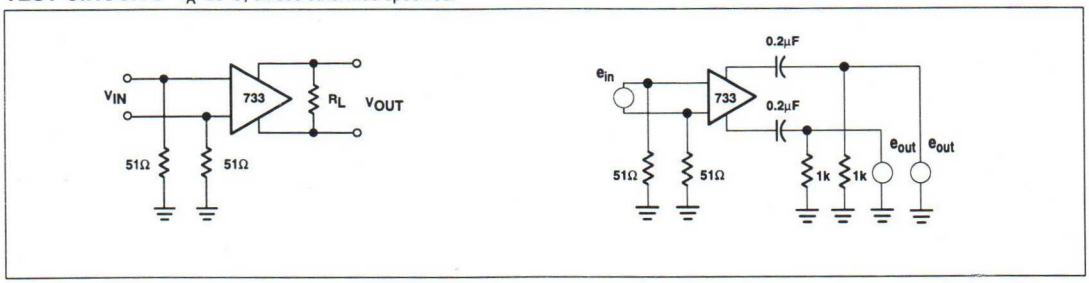
Output Voltage and Current Swing as a Function of Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TEST CIRCUITS T_A=25°C, unless otherwise specified.





Section 4
Comparators

INDEX

Comparator selector guide		271
Symbols and definitions for comparators		272
LM111/211/311/ LM311B	Voltage comparator	273
LM219/319	Dual voltage comparator	277
LM139/239/239A/339/339A/ LM2901/MC3302	Quad voltage comparator	282
AU2901	Quad voltage comparator	289
LM193/A/293/A/393/A/2903	Low power dual voltage comparator	294
AU2903	Low power dual voltage comparator	300
NE/SE521	High-speed dual-differential comparator/sense amp	305
NE522	High-speed dual-differential comparator/sense amp	310
NE527	Voltage comparator	315
NE529	Voltage comparator	320
AN116	Applications for the NE521/522/527/529	325

Comparator selector guide

General Purpose/Linear ICs

DEVICE	COM-PLEXITY	TEMP RANGE*	MAX INP OFFSET VOLT (mV)	MAX INPUT CURRENT		SUPPLY VOLTAGE (V)	RESPONSE TIME (TYP) (ns)	COMMON MODE VOLTAGE RANGE (V)	OUTPUT VOLTAGE		OUTPUT STRUCTURE	VOLTAGE GAIN (TYP) (V/mV)	TTL FANOUT	MAX OFF INPUT VOLTAGE (V)
				BIAS (μ A)	OFFSET (μ A)				V OL MAX (V)	V OH MIN (V)				
LM111	SINGLE	M	3.0	0.10	0.01	± 15	200	−14.5/+13	0.4		OC	200	5	± 30
LM211	SINGLE	I	3.0	0.10	0.01	to	200	−14.5/+13	0.4		OC	200	5	± 30
LM311	SINGLE	C	7.5	0.25	0.05	+5 and GND	200	−14.5/+13	0.4		OC	200	5	± 30
NE527	SINGLE	C	10.0	4.00	1.0	± 10	16	± 5	0.5	2.7	TTL		5	± 5
SE527	SINGLE	M	6.00	4.00	1.00	+5	16	± 5	0.5	2.5	TTL		5	± 5
NE529	SINGLE	C	10.0	50.0	15.0	±10	12	± 5	0.5	2.7	TTL		5	± 5
SE529	SINGLE	M	6.00	36.0	9.00	and +5	12	± 5	0.5	2.5	TTL		5	± 5
AU2903	DUAL	AX	7.0	0.25	0.05	+2 to +36 GND	1300	0 to Vs−2	0.7		OC	100	2	36
LM119	DUAL	M	7.00	1.00	0.10	± 15	80	± 13	0.4		OC	40	2	± 5
LM219	DUAL	I	7.00	1.00	0.10	to	80	± 13	0.4		OC	40	2	± 5
LM319	DUAL	C	10.0	1.20	0.30	+5 and GND	80	± 13	0.4		OC	40	2	± 5
LM193 /193A	DUAL	M	9.00/4.0	0.30	0.10	± 1 to ± 18	1300	0 to Vs−2	0.7		OC	200	2	36
LM293/293A	DUAL	I	9.00/4.0	0.40	0.15	or	1300	0 to Vs−2	0.7		OC	200	2	36
LM393/393A	DUAL	C	9.00/4.0	0.40	0.15	+2 to +36 GND	1300	0 to Vs−2	0.7		OC	200	2	36
LM2903	DUAL	I	15.0	0.50	0.20		1300	0 to Vs−2	0.7		OC	100	2	36
NE/SE521	DUAL	M/C	15/10.0	40.0	12.0	+5 −5 GND	8	± 3	0.5	2.5/2.7	TTL		12	± 6
NE/SE522	DUAL	M/C	15/10.0	40.0	12.0	+5 −5 GND	10	± 3	0.5		OC		12	± 6
AU2901	QUAD	AX	7.0	0.25	0.05	+2 to +36 GND	1300	0 to Vs−2	0.7		OC	100	2	36
LM139 /139A	QUAD	M	9.00/4.0	0.30	0.10		1300	0 to Vs−2	0.7		OC	200	2	36
LM239/239A	QUAD	I	9.00/4.0	0.40	0.15	±1 to± 18 or	1300	0 to Vs−2	0.7		OC	200	2	36
LM339/339A	QUAD	C	9.00/4.0	0.40	0.15	+2 to +36	1300	0 to Vs−2	0.7		OC	200	2	36
LM2901	QUAD	I	15.0	0.50	0.20		1300	0 to Vs−2	0.7		OC	100	2	36
MC3302	QUAD	I	40.0	1.00	0.30	+2 to +28 GND	1300	0 to Vs−2	0.7		OC	100	2	36

* Temperature range
I = Industrial −25°C to +85°C
C = Commercial 0°C to +70°C
M = Military −55°C to +125°C
A = Automotive −40°C to +85°C
AX = Automotive extended −40°C to +125°C

Symbols and definitions for comparators

Common-Mode Rejection Ratio (CMRR)
The ratio of the change in input common-mode voltage (over a specified input common-mode range) to the corresponding change in V_{OS} (see definition below). CMRR is expressed in dB where CMRR (dB) = $20\log(\Delta CMV/\Delta V_{OS})$.

Differential Input Resistance (R_{IN})
The small-signal resistance looking into either input terminal with the other input terminal connected to a specified voltage.

Input Bias Current (I_{BIAS})
The current into either input terminal with both inputs connected to a common specified voltage.

Input Common-Mode Voltage Range (CMVR)
The range of input common-mode voltage for which operation within the specifications is guaranteed.

Input Offset Current (I_{OS})
The difference between the two input bias currents with both inputs connected to a common specified voltage.

Input Offset Current Drift (TCI_{OS})
The ratio of the change in I_{OS} to the corresponding change in temperature as that temperature deviates from 25°C.

Input Offset Voltage (V_{OS})
The minimum potential difference required between the input terminals to force the output to a specified voltage.

Input Offset Voltage Drift (TCV_{OS})
The ratio of the change in V_{OS} to the corresponding change in temperature as that temperature deviates from 25°C.

Input to Output Propagation Delay (t_{PD})
The propagation delay measured from the time the differential input signal equals V_{OS} to the 50% point of the output transition with the comparator in the compare mode. The propagation delay is specified for a given initial input voltage ($-V_{IN}$) and overdrive (V_{OD}, see definition below) and can also be specified for both positive - (t_{PD+}) and negative -(t_{PD-}) going output transitions and is cpecified for a particular value of V_{OD} (see definition below).

Latch Disable Propagation Delay (t_{LPD})
The propagation delay measured between the 50% point of the latch-to-compare transition of the latch enable signal and the 50% point of the output transition. This propagation delay can be specified for both positive - (t_{lPD+}) and negative - (t_{lPD-}) going output transitions and is specified for a particular value of V_{OD} (see definition below).

Latch Hold Time (t_H)
The minimum time after the compare-to-latch transition of the latch enable signal that the input signal must remain unchanged in order to be acquired and held at the output. Hold time is measured from the 50% transition point of the latch enable signal to the point at which the differential input signal equals V_{OS} and is specified for a particular value of V_{OD} (see definition below).

Latch Pulse Width (t_W)
The minimum time that the latch enable signal must be in the compare mode in order to acquire and subsequently hold an input signal change. Pulse width is measured between the 50% transition points of the latch enable pulse and is specified for a particular value of V_{OD} (see definition below).

Latch Setup Time (t_S)
The minimum time before the compare-to-latch transition of the latch enable signal that the input signal must remain unchanged in order to be acquired and held at the output. Setup time is measured from the point at which the differential input voltage equals V_{OS} to the 50% transition point of the latch enable signal and is specified for a particuiar value of V_{OD} (see definition below).

Output High Current (I_{OH})
The current that can be sourced at the output terminal at a specified output voltage.

Output High Voltage (V_{OH})
The high output voltage at a specified output source current and differential input voltage.

Output High Current (I_{OL})
The current that can be sunk at the output terminal at a specified output voltage.

Output Low Voltage (V_{OL})
The low output voltage at a specified output sink current and differential input voltage.

Overdrive (V_{OD})
The input overdrive (V_{OD}) is the applied differential input voltage (V_{IN}) in excess of the comparator input offset voltage (V_{OS}); i.e., $V_{OD} = V_{IN} - V_{OS}$. The dynamic response of a comparator depends on the input overdrive and, for this reason, such parameters as propagation delay and latch setup time, hold time, and pulse width are specified for a particular value of V_{OD}.

Power Supply Rejection Ratio (PSRR)
The ratio of the change in power supply voltage (over a specified power supply voltage range) to the corresponding change in V_{OS}. PSRR is expressed in dB where $PSRR(dB) = 20\log(\Delta PSV/\Delta V_{OS})$.

Voltage Gain (A_V)
The ratio of the change in output voltage (over a specified output voltage range) to the change in differential input voltage.

Voltage comparator

LM111/211/311/ LM311B

DESCRIPTION

The LM111 series are voltage comparators that have input currents approximately a hundred times lower than devices like the µA710. They are designed to operate over a wider range of supply voltages; from standard ±15V op amp supplies down to a single 3V supply. Their output is compatible with RTL, DTL, and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50mA.

Both the inputs and the outputs of the LM111 series can be isolated from system ground, and the output can drive loads referred to ground, the positive supply, or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire-ORed.

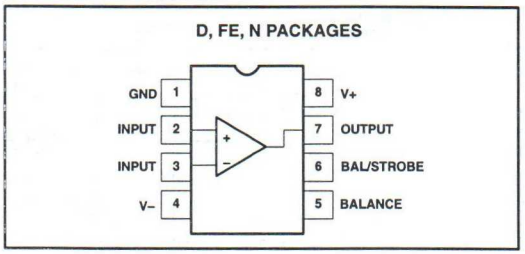
Although slower than the µA710 (200ns response time vs 40ns), the devices are also much less prone to spurious oscillations. The LM111 series has the same pin configuration as the µA710 series.

FEATURES

- Operates from single 3V supply (LM311B)
- Maximum input bias current: 150nA (LM311—250nA)
- Maximum offset current: 20nA (LM311—50nA)
- Differential input voltage range: ±30V
- Power consumption: 135mW at ±15V
- High sensitivity—200V/mV
- Zero crossing detector

PIN CONFIGURATION

D, FE, N PACKAGES



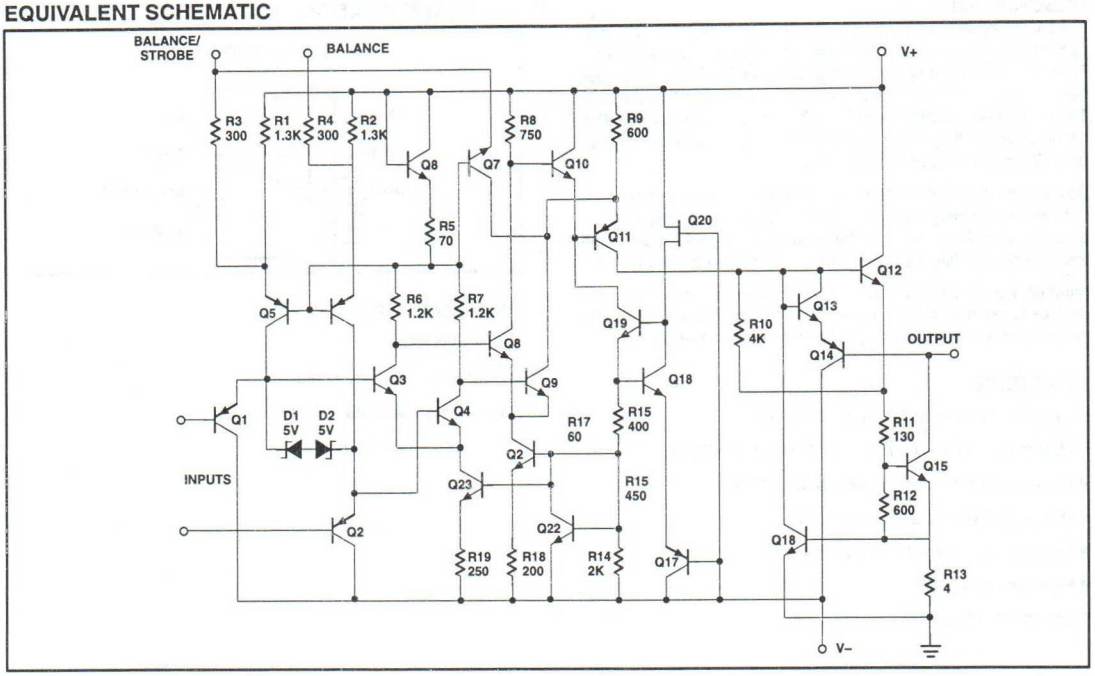
APPLICATIONS

- Precision squarer
- Positive/negative peak detector
- Low voltage adjustable reference supply
- Switching power amplifier

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	LM111N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-25°C to +85°C	LM211N	0404B
8-Pin Plastic Small Outline Package (SO)	0 to +70°C	LM311D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	LM311N	0404B
8-Pin Plastic Small Outline Package (SO)	-25°C to +85°C	LM211D	0174C
8-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	LM111FE	0580A
8-Pin Plastic Small Outline Package (SO)	0 to +70°C	LM311BD	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	LM311BN	0404B

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Total supply voltage	36	V
	Output to negative supply voltage:		
	LM111/LM211	50	V
	LM311/LM311B	40	V
	Ground to negative supply voltage	30	V
	Differential input voltage	±30	V
V_{IN}	Input voltage[1]	±15	V
$P_{D\ MAX}$	Maximum power dissipation, T_A=25°C (still-air)[2]		
	F package	810	mW
	N package	1190	mW
	D package	780	mW
I	Output short-circuit duration	10	sec
T_A	Operating ambient temperature range		
	LM111	-55 to +125	°C
	LM211	-25 to +85	°C
	LM311/LM311B	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
2. Derate above 25°C, at the following rates: F package at 6.4mW/°C; N package at 9.5mW/°C; D package at 6.2m/W°C

DC ELECTRICAL CHARACTERISTICS[1, 2, 3, 6]

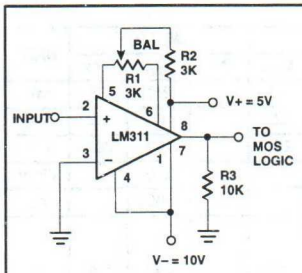
Over temperature range unless otherwise specified.

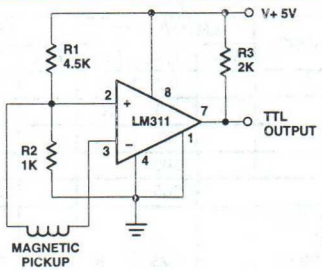
SYMBOL	PARAMETER	TEST CONDITIONS	LM111/LM211			LM311			LM311B			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[3]	T_A=25°C, R_S≤50kΩ		0.7	3.0		2.0	7.5		2.0	7.5	mV
I_{OS}	Input offset current[3]	T_A=25°C		4.0	10		6.0	50		6	25	nA
I_{BIAS}	Input bias current	T_A=25°C		60	100		100	250		100	200	nA
A_V	Voltage gain	T_A=25°C		200			200			200		V/mV
	Response time[4]	T_A=25°C		200			200			500		ns
V_{SAT}	Saturation voltage	LM111/211 V_{IN}≤-5mV, I_{OUT}=50mA LM311/B V_{IN}≤-10mV, I_{OUT}=50mA T_A=25°C		0.75	1.5		0.75	1.5		0.75	1.5	V
$I_{BAL/STR}$	Strobe on current	T_A=25°C		3.0			3.0			3.0		mA
$I_{LEAKAGE}$	Output leakage current[6]	LM111/211 V_{IN}≥5mV, V_{OUT}=35V LM311/B V_{IN}≥10mV, V_{OUT}=35V T_A=25°C, I_{STROBE}=3mA (V– = V_{GND} = –5V)		0.2	10		0.2	50		0.2	50	nA
V_{OS}	Input offset voltage[3]	R_S≤50kΩ			4.0			10			10	mV
I_{OS}	Input offset current[3]				20			70			50	nA
I_{BIAS}	Input bias current				150			300			250	nA
V_{IN}	Input voltage range	V=±15V (Pin 7 may go to 5V)	-14.5	13.8 to -14.7	13.0	-14.5	13.8 to -14.7	13.0	V– +0.5		V+ –1.5	V
V_{OL}	Saturation voltage[6]	V+ ≥ 4.5V, V- = 0 LM111/211 V_{IN}≤-6mV, I_{SINK}≤8mA LM311/B V_{IN}≤-10mV, I_{SINK}≤8mA		0.23	0.4		0.23	0.4		0.23	0.4	V
I_{OH}	Output leakage current	V_{IN}≥5mV, V_{OUT}=35V		0.1	0.5							µA
I_{CC}	Positive supply current	T_A=25°C		5.1	6.0		5.1	7.5		1.6	3.5	mA
I_{EE}	Negative supply voltage	T_A=25°C		4.1	5.0		4.1	5.0				mA

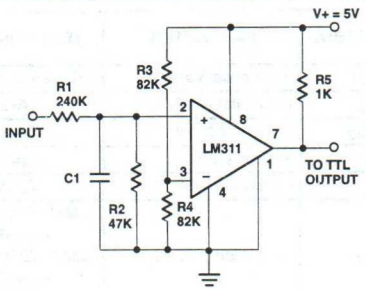
NOTES:

1. This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
2. These specifications apply for V_S=±15V and 0°C < T_A < 70°C unless otherwise specified. With the LM211, however, all temperature specifications are limited to -25°C ≤ T_A ≤ 85°C and for the LM111 is limited to -55°C T_A < 125°C. The offset voltage, offset current, and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.
3. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
4. The response time specified is for a 100mV input step with 5mV over-drive.
5. Do not short the strobe pin to ground; it should be current driven at 3mA to 5mA.
6. LM311B, all parameters are at V+ = 3V ±10%, V– = GND = 0V.

TYPICAL APPLICATIONS







* Values shown are for a 0 to 30V logic swing and a 15V threshold.

** May be added to control speed and reduce susceptibility to noise spikes.

Zero Detector Driving MOS Logic

Detector for Magnetic Transducer

TTL Interface with High Level Logic

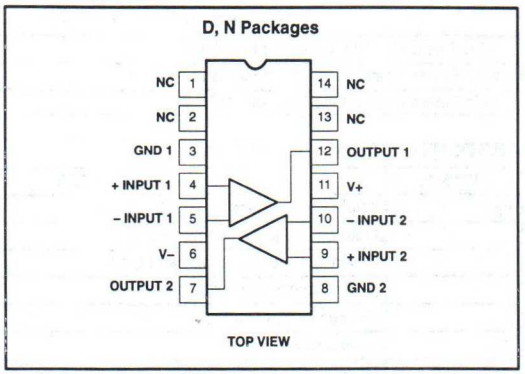
Dual voltage comparator | LM219/319

DESCRIPTION

The LM319 series are precision high-speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the µA710. The uncommitted collector of the output stage makes the LM319 compatible with RTL, DTL, and TTL as well as capable of driving lamps and relays at currents up to 25mA.

Although designed primarily for applications requiring operation from digital logic supplies, the LM319 series are fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high-speed, wide operating voltage range and low package count make the LM319 much more versatile than older devices like the µA711.

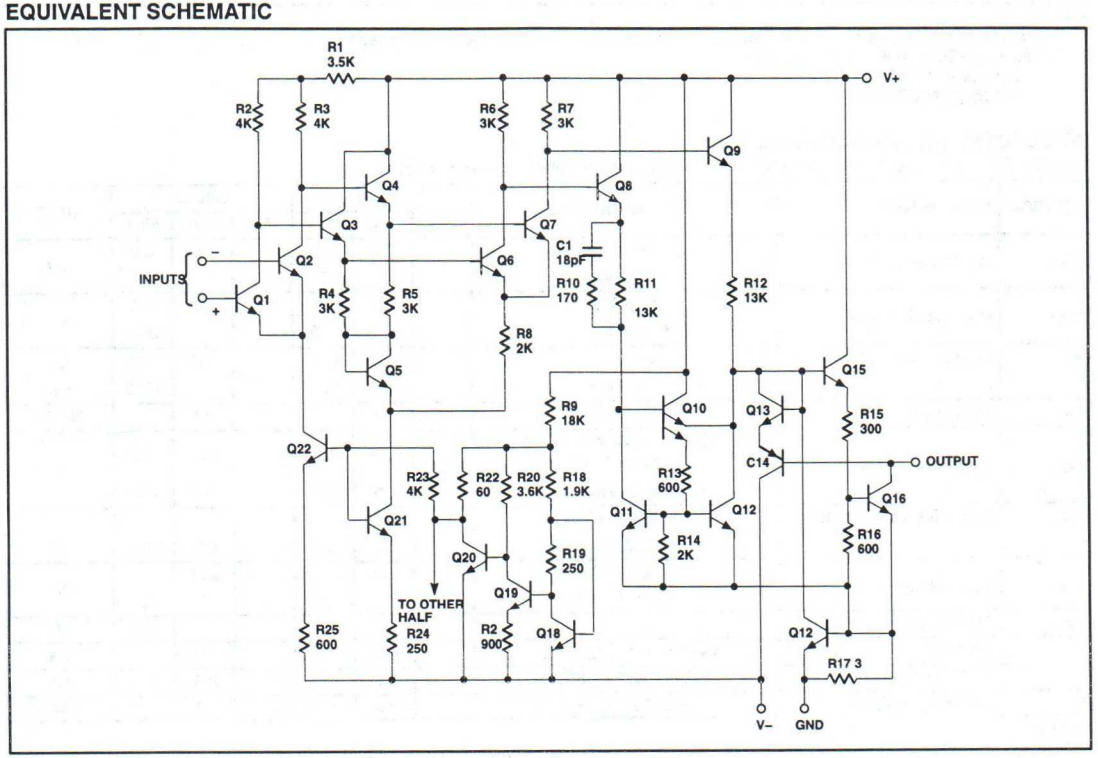
PIN CONFIGURATION



FEATURES

- Two independent comparators
- Operates from a single 5V supply
- Typically 80ns response time at ±15V
- Minimum fanout of 3 (each side)
- Maximum input current of 1µA over temperature
- Inputs and outputs can be isolated from system ground
- High common-mode slew rate

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO) Package	-25 to +85°C	LM219D	0175D
14-Pin Plastic Small Outline (SO) Package	0 to +70°C	LM319D	0175D
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	LM319N	0405B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Total supply voltage	36	V
	Output to negative supply voltage	36	V
	Ground to negative supply voltage	25	V
	Ground to positive supply voltage	18	V
	Differential input voltage	±5	V
V_{IN}	Input voltage[1]	±15	V
	Maximum power dissipation, T_A=25°C (still-air)[2]		
	N package	1420	mW
	D package	1040	mW
	Output short-circuit duration	10	s
T_A	Operating temperature range LM219	-25 to +85	°C
	LM319	0 to +70	
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. For supply voltages less than ±15V, the absolute maximum rating is equal to the supply voltage.
2. Derate above 25°C, at the following rates:
   N package at 11.4mW/°C
   D package at 8.3mW/°C

DC ELECTRICAL CHARACTERISTICS

V_S=±15V, -25°C ≤ T_A ≤ 85°C for LM219, 0°C ≤ T_A ≤ 70°C for LM319, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM219			LM319			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[1, 2]	R_S≤5kΩ, T_A=25°C		0.7	4.0		2.0	8.0	mV
		Over temp.			7			10	
I_{OS}	Input offset current[1, 2]	T_A=25°C		30	75		80	200	nA
		Over temp.			100			300	
I_B	Input bias current[1]	T_A=25°C		150	500		250	1000	nA
		Over temp.			1000			1200	nA
A_V	Voltage gain	T_A=25°C	8	40		8	40		V/mV
V_{OL}	Saturation voltage	V_{IN}≤-10mV, I_{OUT}=25mA, T_A=25°C, V+≥4.5V, V-=0		0.75	1.5		0.75	1.5	V
		V_{IN}≤-10mV, I_{OUT}=3.2mA		0.3	0.6		0.3	0.4	
I_{OH}	Output leakage current	V-=0V, V_{IN}≥10mV							
		V_{OUT}=35V, T_A=25°C		0.2	10		0.2	10	µA
V_{IN}	Input voltage range	V_S=±15V		±13			±13		V
		V+=5V, V-=0V	1		3	1		3	
V_{ID}	Differential input voltage				±5			±5	V
I+	Positive supply current	V+=5V, V-=0V, T_A=25°C		4.3			4.3		mA
I+	Positive supply current	V_S=±15V, T_A=25°C		8.0	12.5		8.0	12.5	mA
I-	Negative supply current	V_S=±15V, T_A=25°C		3.0	5.0		3.0	5.0	mA

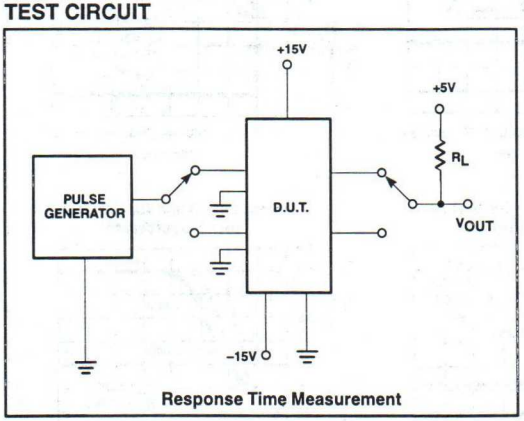
NOTES:
1. V_{OS}, I_{OS} and I_B specifications apply for a supply voltage range of V_S=±15V down to a single 5V supply.
2. The offset voltages and offset currents given are the maximum values required to drive the output to within 1V of either supply with a 1mA load. Thus these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_R	Response time[1]	V_S=±15V, T_A=25°C R_L=500Ω (see test figure)		80		ns

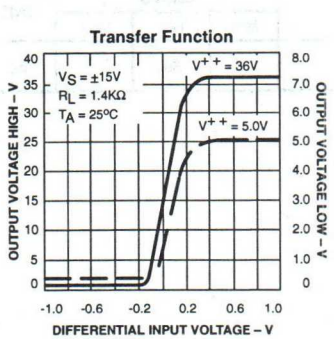
NOTES:
1. The response time specified is for a 100mV step with 5mV overdrive.

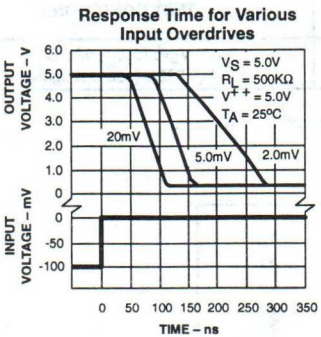
TEST CIRCUIT

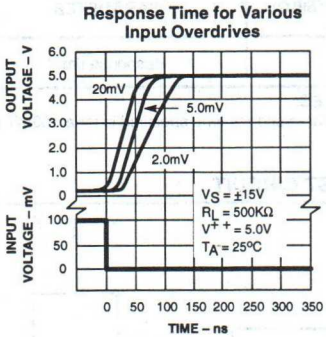


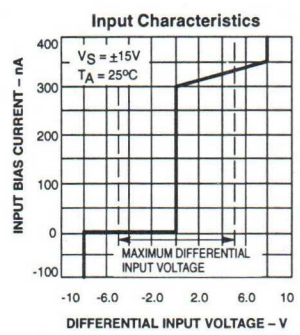
Response Time Measurement

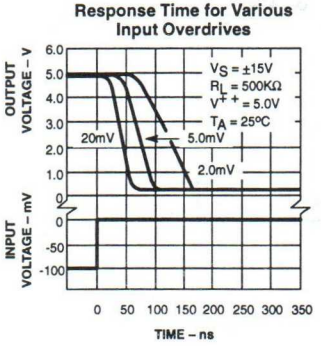
TYPICAL PERFORMANCE CHARACTERISTICS

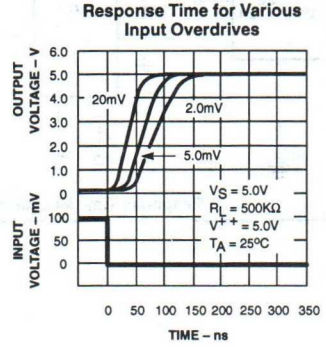


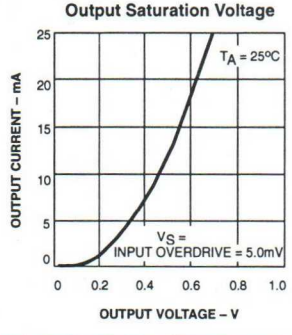


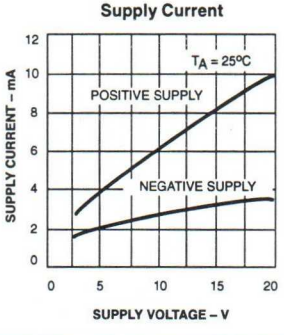


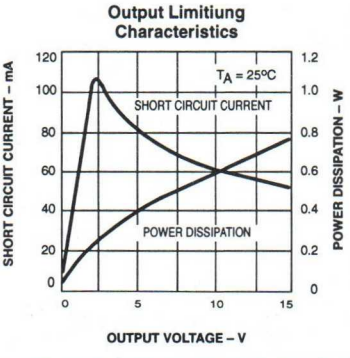




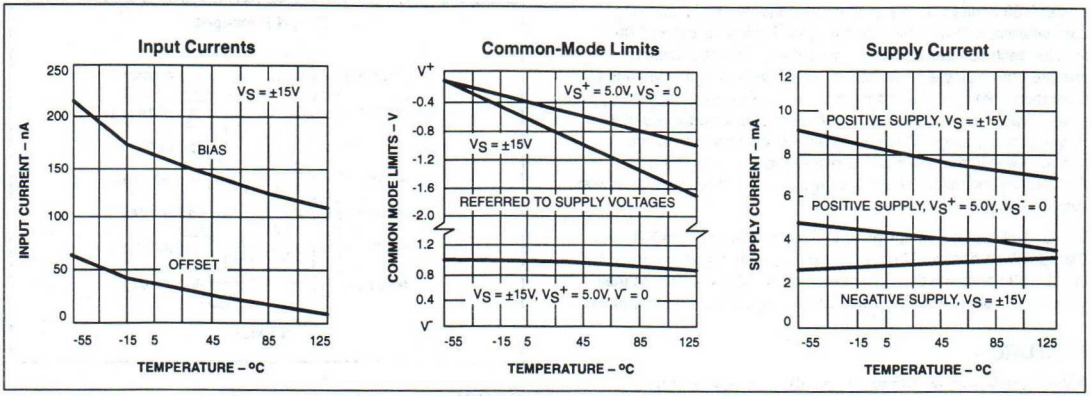




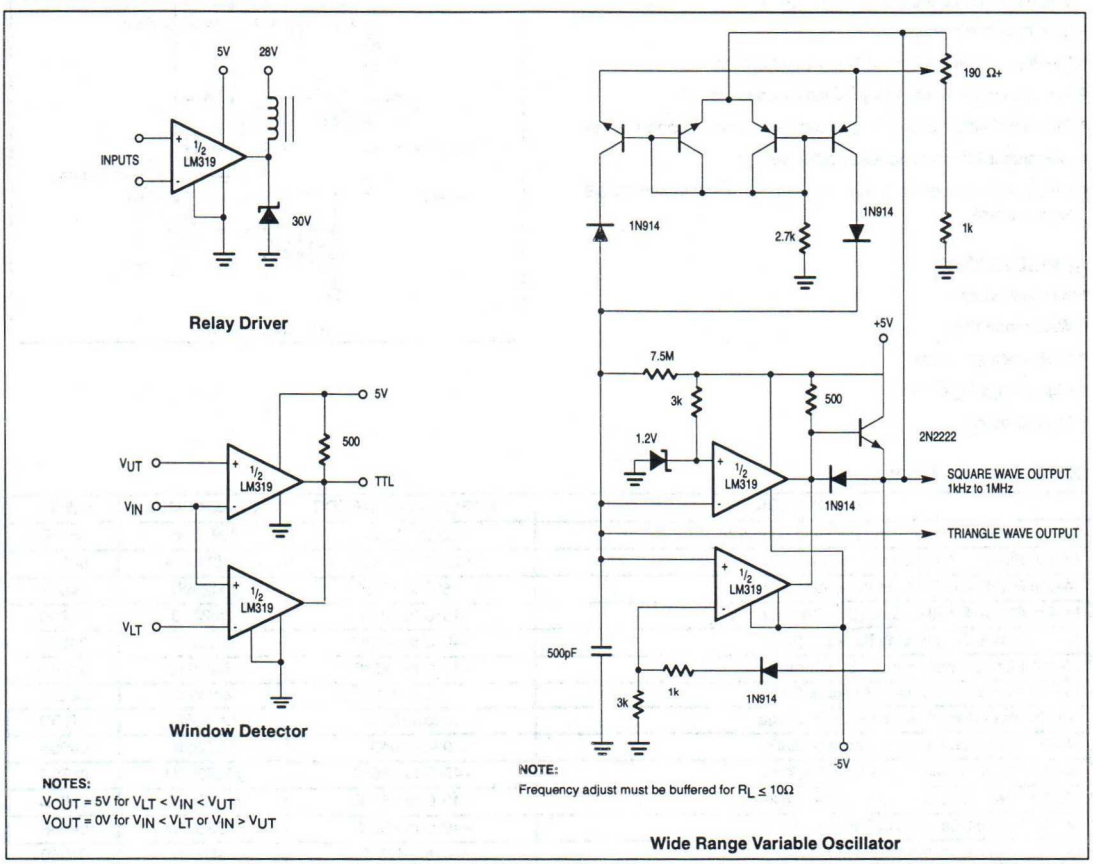




TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TYPICAL APPLICATIONS



Quad voltage comparator

LM139/239/239A/339/339A /LM2901/MC3302

DESCRIPTION

The LM139 series consists of four independent precision voltage comparators, with an offset voltage specification as low as 2.0mV max for each comparator, which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common–mode voltage range includes ground, even though they are operated from a single power supply voltage.

The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM139 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

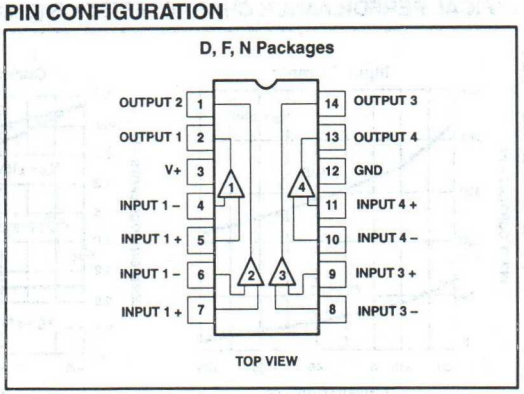
FEATURES

- Wide single supply voltage range 2.0V_{DC} to 36V_{DC} or dual supplies ±1.0V_{DC} to ±18V_{DC}
- Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/comparator at 5.0V_{DC})
- Low input biasing current 25nA
- Low input offset current ±5nA and offset voltage
- Input common–mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 250mV at 4mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

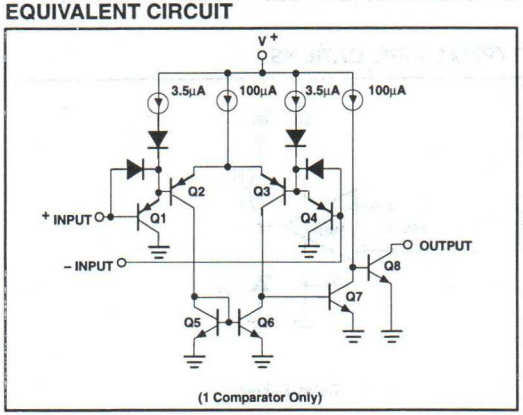
APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

PIN CONFIGURATION



EQUIVALENT CIRCUIT



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14–Pin Ceramic Dual In-Line Package (Cerdip)	–55 to +125°C	LM139F	0581B
14–Pin Plastic Dual In-Line Package (DIP)	–25°C to +85°C	LM239AN	0405B
14–Pin Plastic Dual In-Line Package (DIP)	–25°C to +85°C	LM239N	0405B
14–Pin Plastic Small Outline (SO) Package	–25°C to +85°C	LM239D	0175D
14–Pin Plastic Dual In-Line Package (DIP)	–40°C to +85°C	LM2901N	0405B
14–Pin Plastic Small Outline (SO) Package	–40°C to +85°C	LM2901D	0175D
14–Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	LM339AN	0405B
14–Pin Plastic Small Outline (SO) Package	0 to +70°C	LM339D	0175D
14–Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	LM339N	0405B
14–Pin Plastic Small Outline (SO) Package	–40°C to +85°C	MC3302D	0175D
14–Pin Ceramic Dual In-Line Package (Cerdip)	–40°C to +85°C	MC3302F	0581B
14–Pin Plastic Dual In-Line Package (DIP)	–40°C to +85°C	MC3302N	0405B
14–Pin Plastic Dual In-Line Package (DIP)	–55 to +125°C	LM139N	0405B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	V_{CC} supply voltage	36 or ±18	V_{DC}
V_{DIFF}	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	–0.3 to +36	V_{DC}
P_D	Maximum power dissipation, T_A=25°C (still–air)[1]		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
	Output short–circuit to ground[2]	Continuous	
I_{IN}	Input current (V_{IN}<–0.3V_{DC})[3]	50	mA
T_A	Operating temperature range		
	LM139	–55 to +125	°C
	LM239/239A	–25 to +85	°C
	LM339/339A	0 to +70	°C
	LM2901/MC3302	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C, at the following rates:
   F Package at 9.5mW/°C
   N Package at 11.4mW/°C
   D Package at 8.3mW/°C
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector–base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which was negative, again returns to a value greater than –0.3V_{DC}.

DC AND AC ELECTRICAL CHARACTERISTICS

$V+=5V_{DC}$, LM139: $-55°C \le T_A \le 125°C$; LM239/239A: $-25°C \le T_A \le 85°C$; LM339/339A: $0°C \le T_A \le 70°C$;; LM2901/MC3302: $-40°C \le T_A \le 85°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM239A/339A			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage[2]	T_A=25°C Over temp.		±1.0	±2.0 ±4.0	mV mV
V_{CM}	Input common–mode voltage range[3]	T_A=25°C Over temp.	0 0		V+–1.5 V+–2.0	V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}s≥0V_{DC} (or V– if need)			V+	V
I_{BIAS}	Input bias current[4]	$i_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A=25°C Over temp.		25	250 400	nA nA
I_{OS}	Input offset current	$i_{IN(+)}-i_{IN(-)}$ T_A=25°C Over temp.		±5.0	±50 ±150	nA nA
I_{OL}	Output sink current	$V_{IN(-)}$≥1V_{DC}, $V_{IN}(+)$=0, V_O≤1.5V_{DC}, T_A=25°C	6.0	16		mA
	Output leakage current	$V_{IN(+)}$≥1V_{DC}, $V_{IN}(-)$=0 V_O=5V_{DC}, T_A=25°C V_O=30V_{DC}, over temp.		0.1	 1.0	nA µA
I_{CC}	Supply current	R_L=∞ on comparators, T_A=25°C V+=30V		0.8	2.0	mA
A_V	Voltage gain	R_L≥15kΩ, V+=15V_{DC}	50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)}$≥1V_{DC}, $V_{IN(+)}$=0, I_{SINK}≤4mA T_A=25°C Over temp.		250	400 700	mV mV
t_{LSR}	Large–signal response time	V_{IN}=TTL logic swing, V_{REF}=1.4V_{DC}, V_{RL}=5V_{DC}, R_L=5.1kΩ, T_A=25°C		300		ns
t_R	Response time[5]	V_{RL}=5V_{DC}, R_L=5.1kΩ, T_A=25°C		1.3		µs

See notes at the end of the Electrical Characteristics.

DC AND AC ELECTRICAL CHARACTERISTICS

$V+=5V_{DC}$, LM139: $-55°C \le T_A \le 125°C$; LM239/239A: $-25°C \le T_A \le 85°C$; LM339/339A: $0°C \le T_A \le 70°C$; LM2901/MC3302: $-40°C \le T_A \le 85°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM139			LM239/339			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[2]	$T_A=25°C$ Over temp.		±2.0	±5.0 ±9.0		±2.0	±5.0 ±9.0	mV mV
V_{CM}	Input common–mode voltage range[3]	$T_A=25°C$ Over temp.	0 0		V+–1.5 V+–2.0	0 0		V+–1.5 V+–2.0	V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}'s≥0V_{DC} (or V– if need)			V+			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A=25°C$ Over temp.		25	100 300		25	250 400	nA nA
I_{OS}	Input offset current	$I_{IN(+)}-I_{IN(-)}$ $T_A=25°C$ Over temp.		±3.0	±25 ±100		±5.0	±50 ±150	nA nA
I_{OL}	Output sink current	$V_{IN(-)}$≥1V_{DC}, $V_{IN}(+)=0$, V_O≤1.5V_{DC}, $T_A=25°C$	6.0	16		6.0	16		mA
	Output leakage current	$V_{IN(+)}$≥1V_{DC}, $V_{IN}(-)=0$ $V_O=5V_{DC}$, $T_A=25°C$ $V_O=30V_{DC}$, over temp.		0.1	 1.0		0.1	 1.0	 nA µA
I_{CC}	Supply current	$R_L=\infty$ on comparators, $T_A=25°C$ V+=30V		0.8	2.0		0.8	2.0	mA
A_V	Voltage gain	R_L≥15kΩ, V+=15V_{DC}	50	200		50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)}$≥1V_{DC}, $V_{IN(+)}=0$, I_{SINK}≤4mA $T_A=25°C$ Over temp.		250	400 700		250	400 700	mV mV
t_{LSR}	Large–signal response time	V_{IN}=TTL logic swing, V_{REF}=1.4V_{DC}, V_{RL}=5V_{DC}, R_L=5.1kΩ, $T_A=25°C$		300			300		ns
t_R	Response time[5]	V_{RL}=5V_{DC}, R_L=5.1kΩ, $T_A=25°C$		1.3			1.3		µs

See notes on following page.

DC AND AC ELECTRICAL CHARACTERISTICS

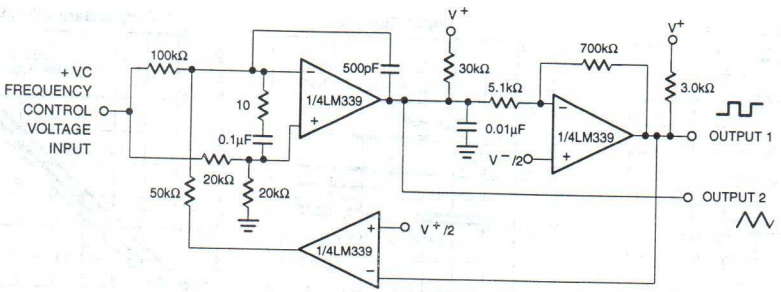
$V+=5V_{DC}$, LM139: $-55°C \le T_A \le 125°C$; LM239/239A: $-25°C \le T_A \le 85°C$; LM339/339A: $0°C \le T_A \le 70°C$; LM2901/MC3302: $-40°C \le T_A \le 85°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM2901			MC3302			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[2]	$T_A=25°C$ Over temp.		±2.0 ±9	±7.0 ±15		±3.0	±20 ±40	mV mV
V_{CM}	Input common–mode voltage range[3]	$T_A=25°C$ Over temp.	0 0		V+–1.5 V+–2.0	0 0		V+–1.5 V+–2.0	V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}'s≥0V_{DC} (or V– if need)			V+			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A=25°C$ Over temp.		 25 200	 250 500		 25	 500 1000	 nA nA
I_{OS}	Input offset current	$I_{IN(+)}-I_{IN(-)}$ $T_A=25°C$ Over temp.		 ±5 ±50	 ±50 ±200		 ±5	 ±100 ±300	 nA nA
I_{OL}	Output sink current	$V_{IN(-)}$≥1V_{DC}, $V_{IN(+)}$=0, V_O≤1.5V_{DC}, $T_A=25°C$	6.0	16		6	16		mA
	Output leakage current	$V_{IN(+)}$≥1V_{DC}, $V_{IN(-)}$=0 $V_O=5V_{DC}$, $T_A=25°C$ $V_O=30V_{DC}$, over temp.		 0.1	 1.0		 0.1	 1.0	 nA µA
I_{CC}	Supply current	$R_L=\infty$ on all comparators,					.8	1.8	mA
		$T_A=25°C$		0.8	2.0				
		$R_L=\infty$ on all comparators, V+=30V		1.0	2.5				mA
A_V	Voltage gain	R_L≥15kΩ, V+=15V_{DC}	25	100		2	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)}$≥1V_{DC}, $V_{IN(+)}$=0, I_{SINK}≤4mA $T_A=25°C$ Over temp.		 400	 400 700		 150	 400 700	 mV mV
t_{LSR}	Large–signal response time	V_{IN}=TTL logic swing, V_{REF}=1.4V_{DC}, V_{RL}=5V_{DC}, R_L=5.1kΩ, $T_A=25°C$		300			300		ns
t_R	Response time[5]	V_{RL}=5V_{DC}, R_L=5.1kΩ, $T_A=25°C$		1.3			1.3		µs

NOTES:

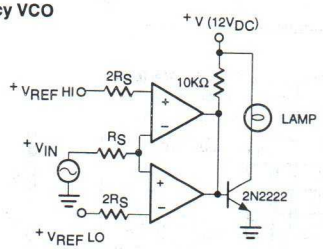
1. Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than –0.3V_{DC} (or 0.3V_{DC} below the magnitude of the negative power supply, if used).
2. At output switch point, $V_O \approx 1.4V_{DC}$, $R_S=0\Omega$ with V+ from 5V_{DC} to 30V_{DC}; and over the full input common–mode range (0V_{DC} to V+ – 1.5V_{DC}). Inputs of unused comparators should be grounded.
3. The input common–mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common–mode voltage range is V+ – 1.5V, but either or both inputs can go to 30V_{DC} without damage.
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The response time specified is for a 100mV input step with a 5mV overdrive. For larger overdrive signals, 300ns can be obtained (see typical performance characteristics section).

EQUIVALENT CIRCUIT

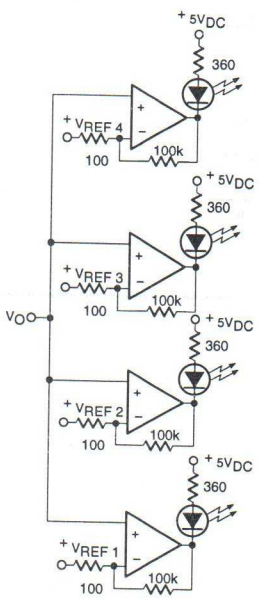


NOTES:
V+ = 30V$_{DC}$
+ 250m V$_{DC}$ ≤ V$_C$ = 50V$_{DC}$
700H ≤ f$_O$ = 100kHz

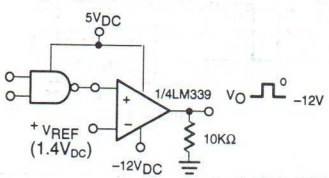
Two–Decade High–Frequency VCO



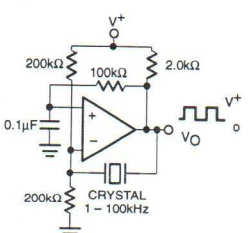
Limit Comparator



Visible Voltage Indicator



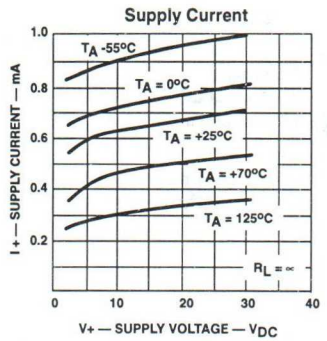
TTL–to–MOS Logic Converter

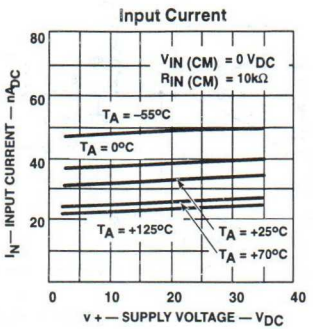


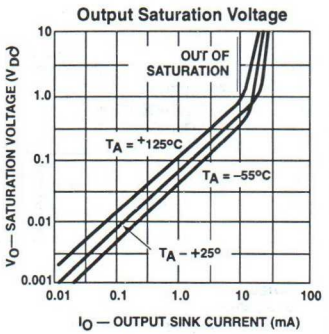
Crystal–Controlled Oscillator

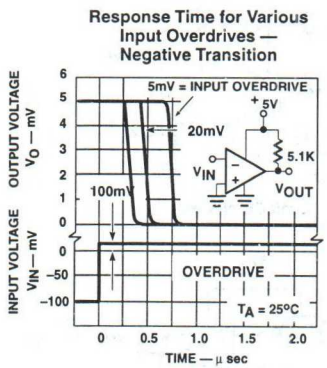
NOTE:
Input of unused comparators should be grounded.

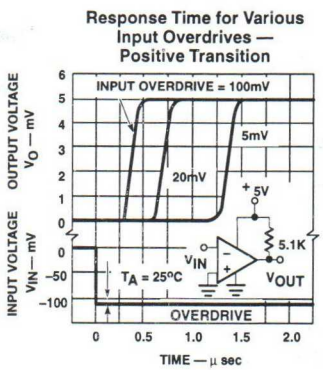
TYPICAL PERFORMANCE CHARACTERISTICS











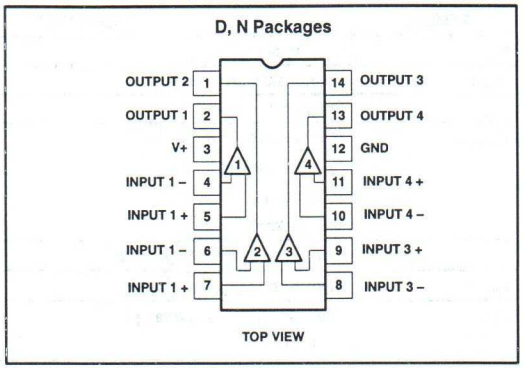
Quad voltage comparator — AU2901

DESCRIPTION

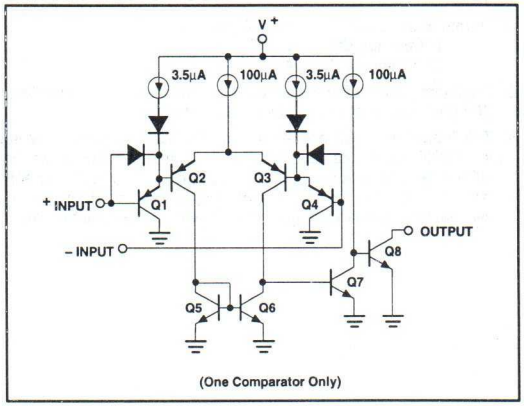
The AU2901 consists of four independent precision voltage comparators, with an offset voltage specification as low as 2.0mV max for each comparator, which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common–mode voltage range includes ground, even though they are operated from a single power supply voltage.

The AU2901 was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the AU2901 will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

PIN CONFIGURATION



EQUIVALENT CIRCUIT



FEATURES

- Wide single supply voltage range 2.0VDC to 36VDC or dual supplies ±1.0VDC to ±18VDC
- Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/comparator at 5.0VDC)
- Low input biasing current 25nA
- Low input offset current ±5nA and offset voltage
- Input common–mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 250mV at 4mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14–Pin Plastic Small Outline (SO) Package	–40°C to +125°C	AU2901D	0175D
14–Pin Plastic Dual In-Line Package (DIP)	–40°C to +125°C	AU2901N	0405B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	V_{CC} supply voltage	36 or ±18	V_{DC}
V_{DIFF}	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	–0.3 to +36	V_{DC}
P_{DMAX}	Maximum power dissipation, T_A=25°C (still–air)[1]		
	N package	1420	mW
	D package	1040	mW
	Output short–circuit to ground[2]	Continuous	
I_{IN}	Input current (V_{IN}<–0.3V_{DC})[3]	50	mA
T_A	Operating temperature range		
	AU2901	–40 to +125	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C, at the following rates:
   N Package at 11.4mW/°C
   D Package at 8.3mW/°C
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector–base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which was negative, again returns to a value greater than –0.3V_{DC}.

ELECTRICAL CHARACTERISTICS

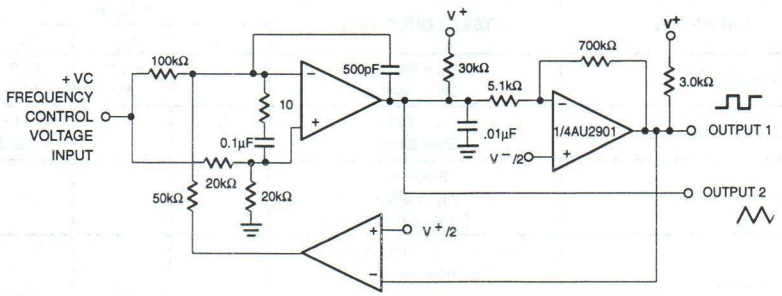
$V+=5V_{DC}$, AU2901: –40°C, $T_A \leq 125°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	AU2901			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage[2]	$T_A = 25°C$ Over temp.		±2.0 ±9	±7.0 ±15	mV
V_{CM}	Input common–mode voltage range[3]	$T_A = 25°C$ Over temp.	0 0		V+–1.5 V+–2.0	V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}s $\geq 0V_{DC}$ (or V– if need)			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		 25 200	 250 500	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		 ±5 ±50	 ±50 ±200	 nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN}(+) = 0$, $V_O \leq 1.5V_{DC}$, $T_A = 25°C$	6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1V_{DC}$, $V_{IN}(-) = 0$, $V_O = 5V_{DC}$, $T_A = 25°C$ $V_O = 30V_{DC}$, Over temp.		0.1	 1.0	nA µA
I_{CC}	Supply current	$R_L = \infty$ on comparators, $T_A = 25°C$ V+ = 30V		0.8 1.0	2.0 2.5	mA
A_V	Voltage gain	$R_L \geq 15k\Omega$, $V+ = 15V_{DC}$	25	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25°C$ Over temp.		 400	 400 700	mV
t_{LSR}	Large–signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4V_{DC}$, $V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300		ns
t_R	Response time[5]	$V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3		µs

NOTES:

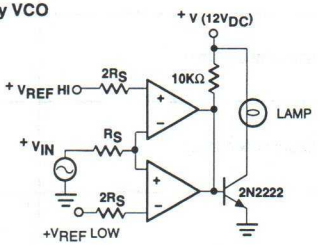
1. Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common–mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V_{DC}$ (or $0.3V_{DC}$ below the magnitude of the negative power supply, if used).
2. At output switch point, $V_O \approx 1.4V_{DC}$, $R_S=0\Omega$ with V+ from $5V_{DC}$ to $30V_{DC}$; and over the full input common–mode range ($0V_{DC}$ to $V+ - 1.5V_{DC}$).
3. The input common–mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common–mode voltage range is V+ – 1.5V, but either or both inputs can go to $30V_{DC}$ without damage.
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The response time specified is for a 100mV input step with a 5mV overdrive. For larger overdrive signals, 300ns can be obtained (see Typical Performance Characteristics section).

EQUIVALENT CIRCUIT

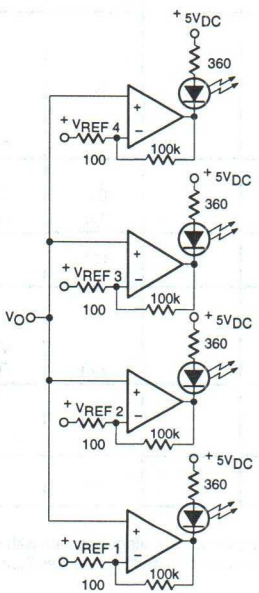


NOTES:
V+ = 30V$_{DC}$
+ 250m V$_{DC}$ ≤ V$_C$ ≤ 50V$_{DC}$
700H ≤ f$_O$ = 100kHz

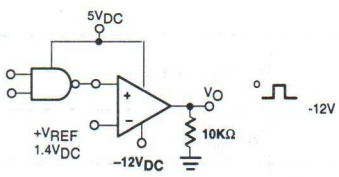
Two–Decade High–Frequency VCO



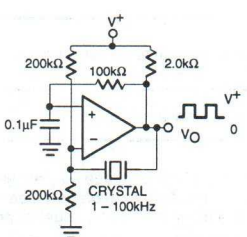
Limit Comparator



Visible Voltage Indicator



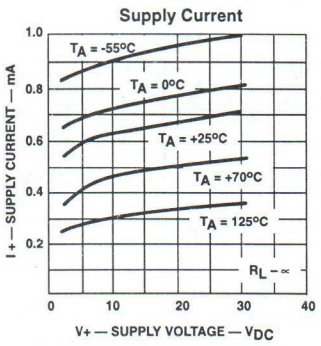
TTL–to–MOS Logic Converter

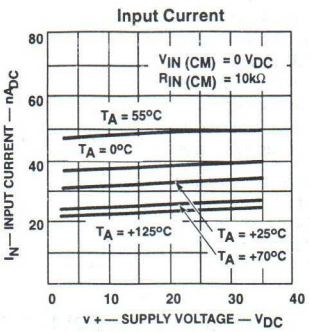


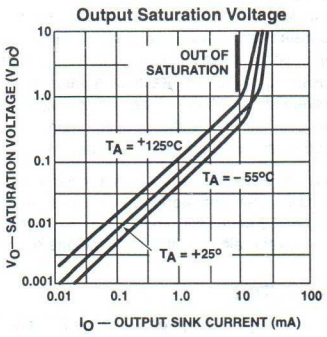
Crystal–Controlled Oscillator

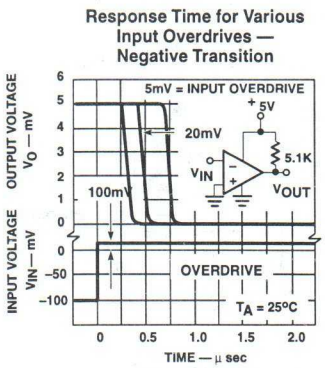
NOTE:
Input of unused comparators should be grounded.

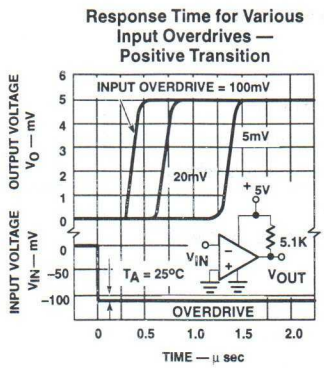
TYPICAL PERFORMANCE CHARACTERISTICS











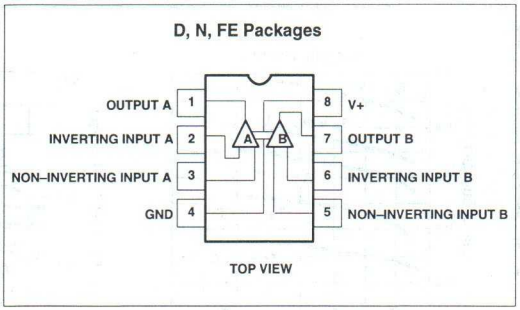
Low power dual voltage comparator — LM193/A/293/A/393/A/2903

DESCRIPTION

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0mV max. for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

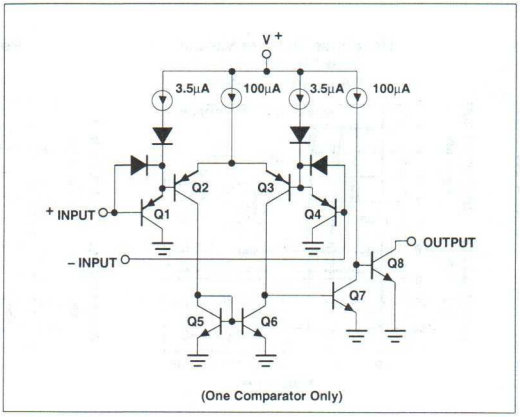
PIN CONFIGURATION



FEATURES

- Wide single supply voltage range 2.0VDC to 36VDC or dual supplies ±1.0VDC, to ±18VDC
- Very low supply current drain (0.8mA) independent of supply voltage (2.0mW/comparator at 5.0VDC)
- Low input biasing current 25nA
- Low input offset current ±5nA and offset voltage ±2mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 250mV at 4mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

EQUIVALENT CIRCUIT



APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Ceramic Dual In-Line Package (Cerdip)	-55°C to +125°C	LM193FE	0580A
8-Pin Ceramic Dual In-Line Package (Cerdip)	-25°C to +85°C	LM293FE	0580A
8-Pin Plastic Dual In-Line Package (DIP)	-25°C to +85°C	LM293N	0404B
8-Pin Plastic Small Outline (SO) Package	-25°C to +85°C	LM293D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	-25°C to +85°C	LM293AN	0404B
8-Pin Ceramic Dual In-Line Package (Cerdip)	0 to +70°C	LM393AFE	0580A
8-Pin Ceramic Dual In-Line Package (Cerdip)	0 to +70°C	LM393FE	0580A
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	LM393D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	LM393N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	LM393AN	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	LM2903N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	LM2903D	0404B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	36 or ±18	V_{DC}
	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	-0.3 to +36	V_{DC}
P_D	Maximum power dissipation, T_A=25°C (still-air)[1]		
	F package	780	mW
	N package	1160	mW
	D package	780	mW
	Output short-circuit to ground[2]	Continuous	
I_{IN}	Input current (V_{IN}<-0.3V_{DC})[3]	50	mA
T_A	Operating temperature range		
	LM193/193A	-55 to +125	°C
	LM293/293A	-25 to +85	°C
	LM393/393A	0 to +70	°C
	LM2903	-40 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C, at the following rates:
   F package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V_{DC}.

DC AND AC ELECTRICAL CHARACTERISTICS

V+=5VDC, LM193/193A: -55°C $T_A \leq +125$°C, unless otherwise specified. LM293/293A: -25°C $T_A \leq +85$°C, unless otherwise specified. LM393/393A: 0°C $T_A \leq +70$°C, unless otherwise specified. LM2903: -40°C $T_A \leq +85$°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM193A			LM293A/393A			LM2903			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[2]	T_A=25°C Over temp.		±1.0	±2.0 ±4.0		±1.0	±2.0 ±4.0		±2.0 ±9	±7.0 ±15	mV mV
V_{CM}	Input common-mode voltage range[3, 6]	T_A=25°C Over temp.	0 0		V+-1.5 V+-2.0	0 0		V+-1.5 V+-2.0	0 0		V+-1.5 V+-2.0	V V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}s ≥0V_{DC} (or V- if need)			V+			V+			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A=25°C Over temp.		25	100 300		25	250 400		25 200	250 500	nA nA
I_{OS}	Input offset current	$I_{IN(+)}$-$I_{IN(-)}$ T_A=25°C Over temp.		±3.0	±25 ±100		±5.0	±50 ±150		±5 ±50	±50 ±200	nA nA
I_{OL}	Output sink current	$V_{IN(-)}$≥1V_{DC}, $V_{IN(+)}$=0, V_O≤1.5V_{DC} T_A=25°C	6.0	16		6.0	16		6.0	16		mA
	Output leakage current	V_O=5V_{DC}, T_A=25°C $V_{IN(+)}$≥1V_{DC}, $V_{IN(-)}$=0 V_O=30V_{DC} Over temp.		0.1	 1.0		0.1	 1.0		0.1	 1.0	nA µA
I_{CC}	Supply current	R_L=∞ on both comparators, T_A=25°C		0.8	1		0.8	1		0.8	1	mA
		R_L=∞ on both comparators, V+=30V		1	2.5		1	2.5		1	2.5	mA
A_V	Voltage gain	R_L≥15kΩ, V+=15V_{DC}, T_A=25°C	50	200		50	200		25	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)}$≥1V_{DC}, $V_{IN(+)}$=0, I_{SINK}≤4mA T_A=25°C Over temp.		250	400 700		250	400 700		400	400 700	mV mV
t_{LSR}	Large-signal response time	V_{IN}=TTL logic swing, V_{REF}=1.4V_{DC} V_{RL}=5V_{DC}, R_L=5.1kΩ, T_A=25°C		300			300			300		ns
t_R	Response time[5]	V_{RL}=5V_{DC}, R_L=5.1kΩ T_A=25°C		1.3			1.3			1.3		µs

DC ELECTRICAL CHARACTERISTICS (Continued)

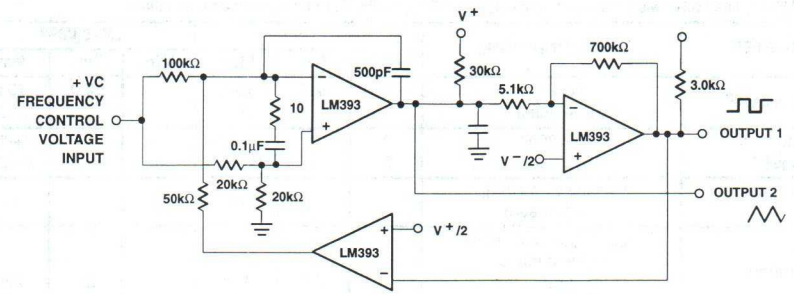
V+=5VDC, LM193/193A: -55°C $T_A \leq +125°C$, unless otherwise specified. LM293/293A: -25°C $T_A \leq +85°C$, unless otherwise specified. LM393/393A: 0°C $T_A \leq +70°C$, unless otherwise specified. LM2903: -40°C $T_A \leq +85°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM193			LM293/393			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[2]	T_A=25°C Over temp.		±2.0	±5.0 ±9.0		±2.0	±5.0 ±9.0	mV mV
V_{CM}	Input common-mode voltage range[3, 6]	T_A=25°C Over temp.	0 0		V±-1.5 V±-2.0	0 0		V+-1.5 V+-2.0	V V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}s ≥0V_{DC} (or V-if need)			V+			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A=25°C Over temp.		25	100 300		25	250 400	nA nA
I_{OS}	Input offset current	$I_{IN(+)}$-$I_{IN(-)}$ T_A=25°C Over temp.		±3.0	±25 ±100		±5.0	±50 ±150	nA nA
I_{OL}	Output sink current	$V_{IN(-)}$≥1V_{DC}, $V_{IN(+)}$=0, V_O≤1.5V_{DC} T_A=25°C	6.0	16		6.0	16		mA
	Output leakage current	$V_{IN(+)}$≥1V_{DC}, $V_{IN(-)}$=0, V_O=5V_{DC} T_A=25°C V_O=30VDC over temp.		0.1	 1.0		0.1	 1.0	nA µA
I_{CC}	Supply current	R_L=∞ on both comparators, T_A=25°C		0.8	1		0.8	1	mA
		R_L=∞ on both comparators, V+=30V			2.5			2.5	mA
A_V	Voltage gain	R_L≥15kΩ, V+=15V_{DC}	50	200		50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)}$≥1V_{DC}, $V_{IN(+)}$=0, I_{SINK}≤4mA T_A=25°C Over temp.		250	400 700		250	400 700	mV mV
t_{LSR}	Large signal response time	V_{IN}=TTL logic swing, V_{REF}=1.4V_{DC}, V_{RL}=5V_{DC} R_L=5.1kΩ, T_A=25°C		300			300		ns
t_R	Response time[5]	V_{RL}=5V_{DC}, R_L=5.1kΩ T_A=25°C		1.3			1.3		µs

NOTES:

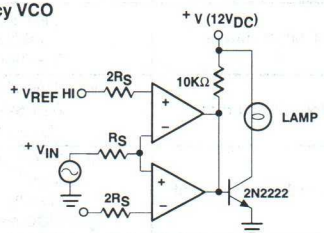
1. Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3V_{DC} (V_{DC} below the magnitude of the negative power supply, if used).
2. At output switch point, $V_O \approx 1.4V_{DC}$, R_S=0Ω with V+ from 5V_{DC} to 30V_{DC} and over the full input common-mode range (0V_{DC} to V+-1.5V_{DC}).
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+-1.5V, but either or both inputs can go to 30V_{DC} without damage.
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The response time specified is for a 100mV input step with a 5mV overdrive.
6. For input signals that exceed V_{CC}, only the over-driven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

EQUIVALENT CIRCUIT

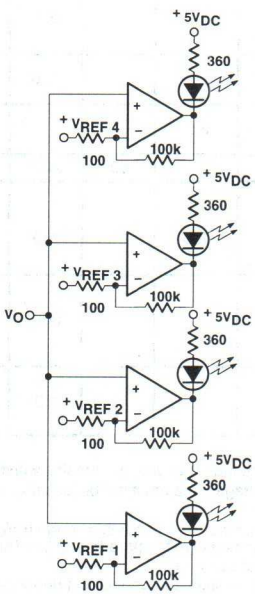


NOTES:
V+ = 30V$_{DC}$
+ 250m V$_{DC}$ ≤ V$_C$ = 50V$_{DC}$
700H ≤ f$_O$ = 100kHz

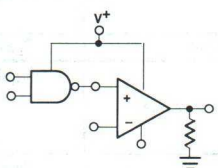
Two–Decade High–Frequency VCO



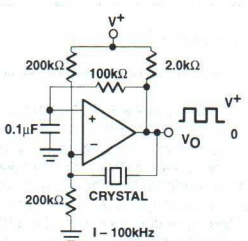
Limit Comparator



Visible Voltage Indicator



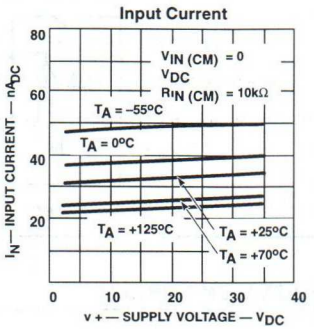
TTL–to–MOS Logic Converter

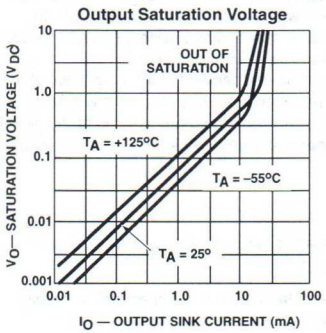


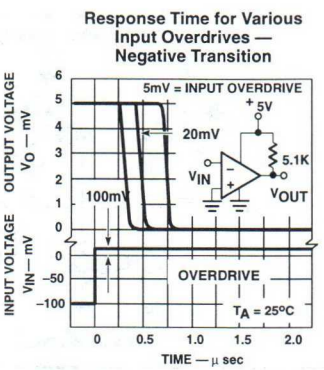
Crystal–Controlled Oscillator

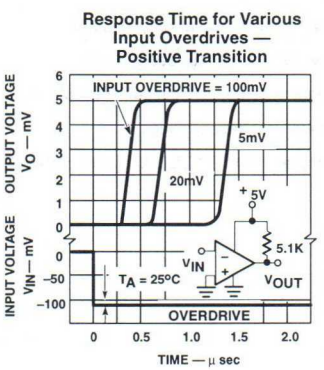
NOTE:
Input of unused comparators should be grounded.

TYPICAL PERFORMANCE CHARACTERISTICS









Low power dual voltage comparator — AU2903

DESCRIPTION

The AU2903 consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0mV max. for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

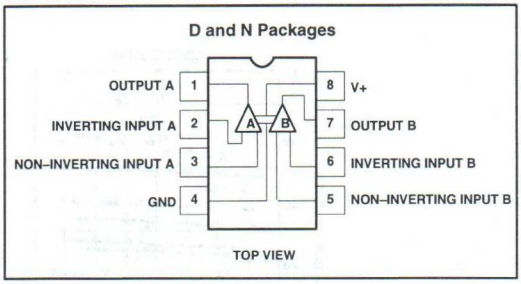
FEATURES

- Wide single supply voltage range 2.0V_{DC} to 36V_{DC} or dual supplies ±1.0V_{DC}, to ±18V_{DC}
- Very low supply current drain (0.8mA) independent of supply voltage (2.0mW/comparator at 5.0V_{DC})
- Low input biasing current 25nA
- Low input offset current ±5nA and offset voltage ±2mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 250mV at 4mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

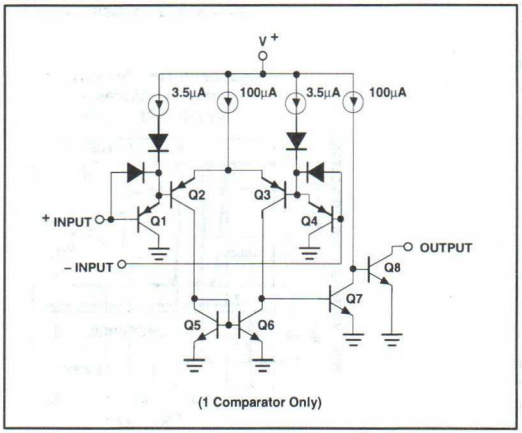
APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

PIN CONFIGURATION



EQUIVALENT CIRCUIT



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	-40°C to +125°C	AU2903D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +125°C	AU2903N	0404B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	36 or ±18	V_{DC}
	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	-0.3 to +36	V_{DC}
P_{DMAX}	Maximum power dissipation, T_A=25°C (still-air)[3]		
	N package	1160	mW
	D package	780	mW
	Output short-circuit to ground[1]	Continuous	
I_{IN}	Input current (V_{IN}<-0.3V_{DC})[2]	50	mA
T_A	Operating temperature range		
	AU2903	-40 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V_{DC}.
3. Derate above 25°C, at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C

DC AND AC ELECTRICAL CHARACTERISTICS

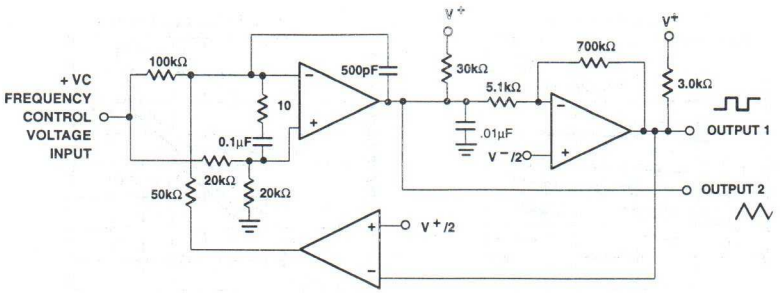
$V+=5V_{DC}$, AU2903; -40°C, $T_A \leq +125°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	AU2903			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage[2]	$T_A = 25°C$ Over temp.		±2.0 ±9	±7.0 ±15	mV
V_{CM}	Input common-mode voltage range[3, 6]	$T_A = 25°C$ Over temp.	0 0		V+-1.5 V+-2.0	V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}s $\geq 0V_{DC}$ (or V- if need)			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A=25°C Over temp.		 25 200	 250 500	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		 ±5 ±50	 ±50 ±200	 nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $V_O \leq 1.5V_{DC}$ $T_A = 25°C$	6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1V_{DC}$, $V_{IN(-)} = 0$ $V_O = 5V_{DC}$, $T_A = 25°C$ $V_O = 30V_{DC}$, over temp.		0.1	 1.0	nA µA
I_{CC}	Supply current	$R_L = \infty$ on both comparators. $T_A = 25°C$ V+ = 30V, over temp.		 0.8 1	 1 2.5	 mA
A_V	Voltage gain	$R_L \geq 15k\Omega$, $V+ = 15V_{DC}$, $T_A = 25°C$	25	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25°C$ Over temp.		 400	 400 700	 mV
t_{LSR}	Large-signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4V_{DC}$ $V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300		ns
t_R	Response time[5]	$V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$ $T_A = 25°C$		1.3		µs

NOTES:

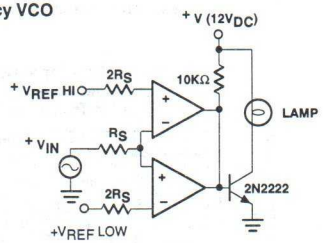
1. Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V_{DC}$ (V_{DC} below the magnitude of the negative power supply, if used).
2. At output switch point, $V_O \approx 1.4V_{DC}$, $R_S = 0\Omega$ with V+ from $5V_{DC}$ to $30V_{DC}$ and over the full input common-mode range ($0V_{DC}$ to $V+-1.5V_{DC}$).
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+-1.5V, but either or both inputs can go to $30V_{DC}$ without damage.
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The response time specified is for a 100mV input step with a 5mV overdrive.
6. For input signals that exceed V_{CC}, only the over-driven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

TYPICAL APPLICATIONS

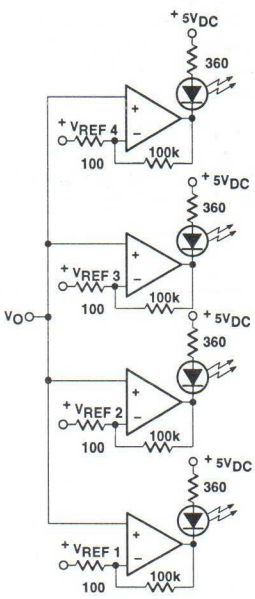


NOTES:
V+ = 30V$_{DC}$
+ 250m V$_{DC}$ ≤ V$_C$ = 50V$_{DC}$
700H ≤ f$_O$ = 100kHz

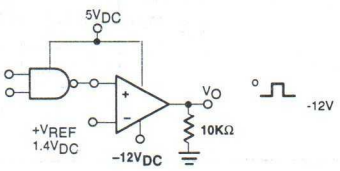
Two–Decade High–Frequency VCO



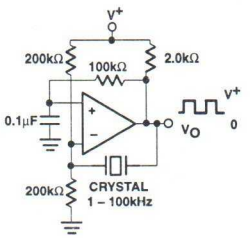
Limit Comparator



Visible Voltage Indicator



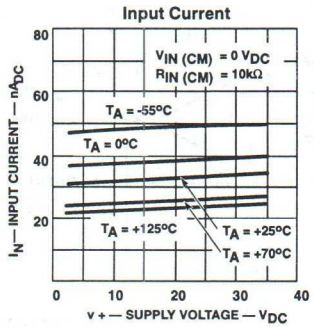
TTL–to–MOS Logic Converter

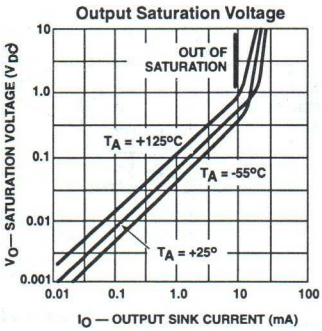


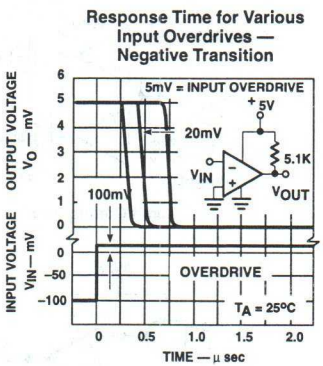
Crystal–Controlled Oscillator

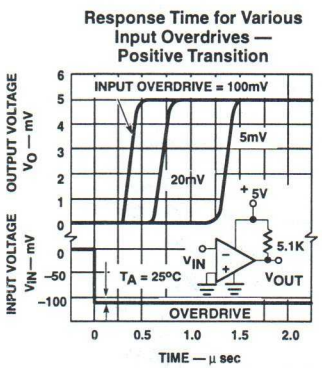
NOTE:
Input of unused comparators should be grounded.

TYPICAL PERFORMANCE CHARACTERISTICS









High-speed dual-differential comparator/sense amp — NE/SE521

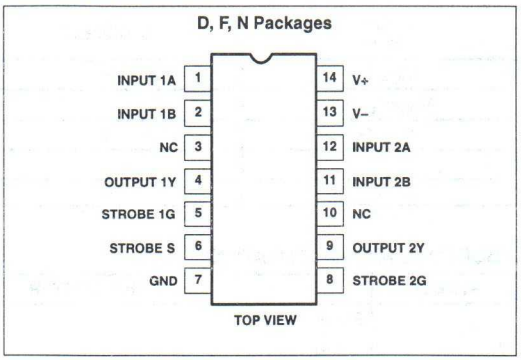
FEATURES

- 12ns maximum guaranteed propagation delay
- 20μA maximum input bias current
- TTL compatible strobes and outputs
- Large common-mode input voltage range
- Operates from standard supply voltages
- Military qualifications pending

APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High-speed line receiver

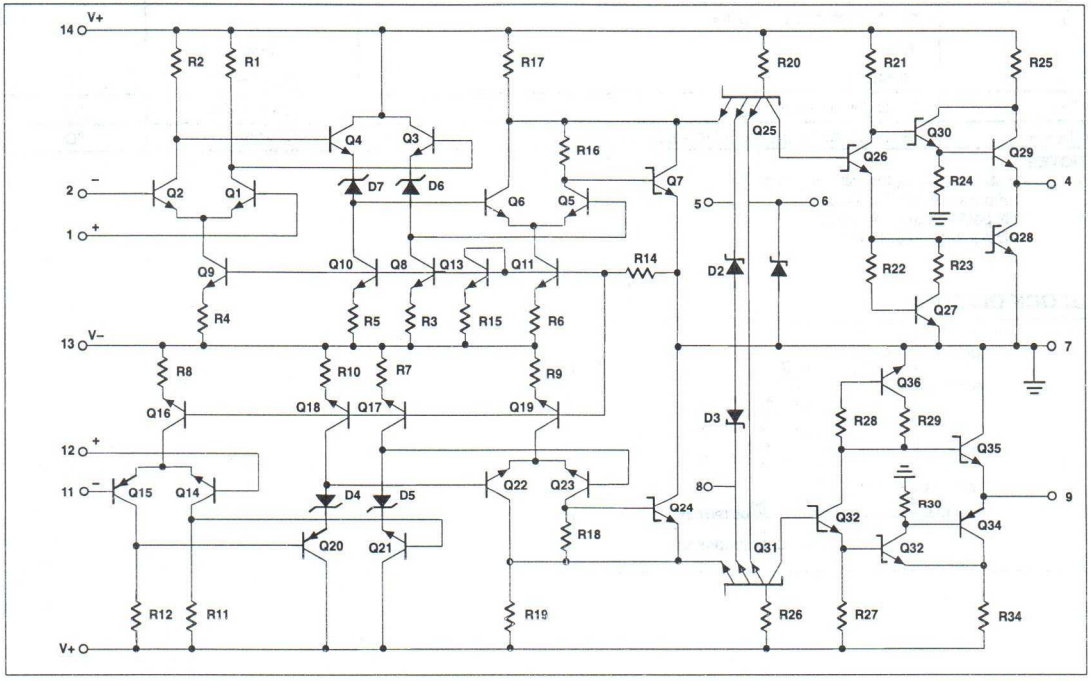
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE521N	0405B
14-Pin SO Package	0 to +70°C	NE521D	0175D
14-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE521F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE521F	0581B

EQUIVALENT SCHEMATIC



High-speed dual-differential comparator/sense amp NE/SE521

LOGIC FUNCTIONS

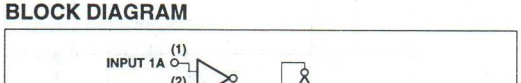
V_{ID} A^+, B^-	STROBE S	STROBE G	OUTPUT (Y)
$V_{ID} \leq -V_{OS}$	H	H	L
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined
$V_{ID} \geq V_{OS}$	H	H	H
X	L	X	H
X	X	L	H

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage		
V+	Positive	+7	V
V-	Negative	-7	V
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage		
	Common mode	±5	V
	Strobe/gate	+5.25	V
P_D	Maximum power dissipation[1] T_A= 25°C (still-air)		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
T_A	Operating temperature range		
	NE521	0 to 70	°C
	SE521	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	+300	°C

NOTES:
1. Derate above 25°C at the following rates:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS (SE521)

V+=+5V, V-=-5V, TA=-55°C to +125°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+=+4.5V, V-=-4.5V				
	At 25°C			6	7.5	mV
	Over temperature range				15	
I_{BIAS}	Input bias current	V+=+5.5V, V-=-5.5V				
	At 25°C			7.5	20	µA
	Over temperature range				40	
I_{OS}	Input offset current	V+=+5.5V, V-=-5.5V				
	At 25°C			1.0	5	µA
	Over temperature range				12	
V_{CM}	Common-mode voltage range	V+=+4.5V, V-=-4.5V	–3		+3	V
V_{IL}	Low level input voltage					
	At 25°C				0.8	V
	Over temperature				0.7	
V_{IH}	High level input voltage		2.0			V
	Input current	V+=+5.5V, V-=-5.5V				
I_{IH}	High	V_{IH}=2.7V				
		1G or 2G strobe			50	µA
		Common strobe S			100	µA
	Input Current					
I_{IL}	Low	V_{IL}=0.5V				
		1G or 2G strobe			-2.0	mA
		Common strobe S			-4.0	mA
	Output voltage	$V_{I(S)}$=2.0V				
V_{OH}	High	V+=+4.5V, V-=-4.5V, I_{LOAD}=-1mA	2.5	3.4		V
V_{OL}	Low	V+=+4.5V, V-=-4.5V, I_{LOAD}=10mA			0.5	
		T_A=25°C, I_{LOAD}=20mA			0.5	
	Supply voltage					
V+	Positive		4.5	5.0	5.5	V
V-	Negative		-4.5	-5.0	-5.5	
	Supply current	V+=5.5V, V-=-5.5V, T_A=25°C				
I_{CC+}	Positive			27	35	mA
I_{CC-}	Negative			-15	-28	
I_{SC}	Short-circuit output current		-35		-115	mA

DC ELECTRICAL CHARACTERISTICS(NE521)

V+=+5V, V-=-5V, TA=0 to 70°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+=+4.75V, V-=-4.75V				
	At 25°C			6	7.5	mV
	Over temperature range				10	
I_{BIAS}	Input bias current	V+=+5.25V, V-=-5.25V				
	At 25°C			7.5	20	µA
	Over temperature range				40	
I_{OS}	Input offset current	V+=+5.25V, V-=-5.25V				
	At 25°C			1.0	5	µA
	Over temperature range				12	
V_{CM}	Common-mode voltage range	V+=+4.75V, V-=-4.75V	-3		+3	V
	Input current	V+=+5.25V, V-=-5.25V				
I_{IH}	High	V_{IH}=2.7V				
		1G or 2G strobe			50	µA
		Common strobe S			100	µA
	Input Current					
I_{IL}	Low	V_{IL}=0.5V				
		1G or 2G strobe			-2.0	mA
		Common strobe S			-4.0	mA
	Output voltage	$V_{I(S)}$=2.0V				
V_{OH}	High	V+=+4.75V, V-=-4.75V, I_{LOAD}=-1mA	2.7	3.4		V
V_{OL}	Low	V+=+5.25V, V-=-5.25V, I_{LOAD}=20mA			0.5	
	Supply voltage					
V+	Positive		4.75	5.0	5.25	V
V-	Negative		-4.75	-5.0	-5.25	
	Supply current	V+=5.25V, V-=-5.25V, T_A=25°C				
I_{CC+}	Positive			27	35	mA
I_{CC-}	Negative			-15	-28	
I_{SC}	Short-circuit output current		-40		-100	mA

AC ELECTRICAL CHARACTERISTICS

T_A=25°C, R_L=280W C_L=15pF V+=5V V-=5V.

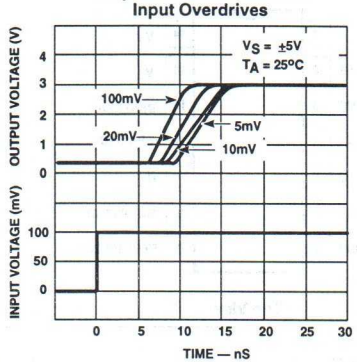
SYMBOL	PARAMETER	FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
Large-signal switching speed							
	Propagation delay						
$t_{PLH(D)}$	Low to high[1]	Amp	Output		8	12	
$t_{PHL(D)}$	High to low[1]	Amp	Output		6	9	ns
$t_{PLH(S)}$	Low to high[2]	Strobe	Output		4.5	10	
$t_{PHL(S)}$	High to low[2]	Strobe	Output		3.0	6	
f_{MAX}	Max. operating frequency			40	55		MHz

NOTES:

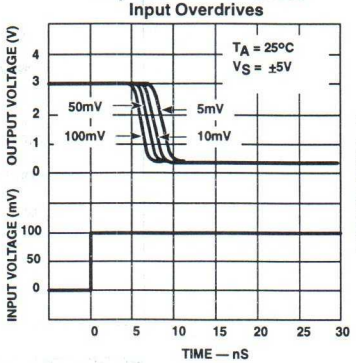
1. Response time measured from 0V point of ±100mV_{P-P} 10MHz square wave to the 1.5V point of the output.
2. Response time measured from 1.5V point of input to 1.5V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS

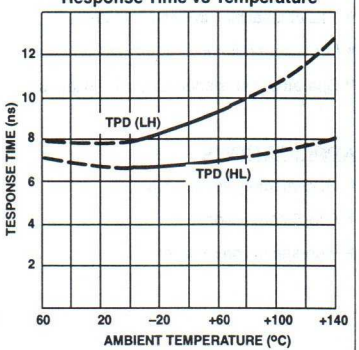
Response Time for Various Input Overdrives



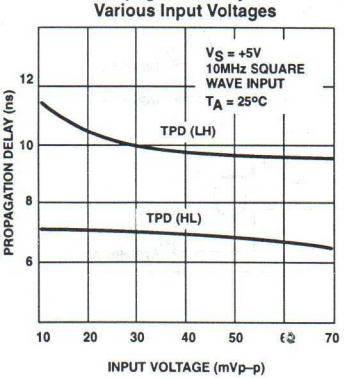
Response Time for Various Input Overdrives



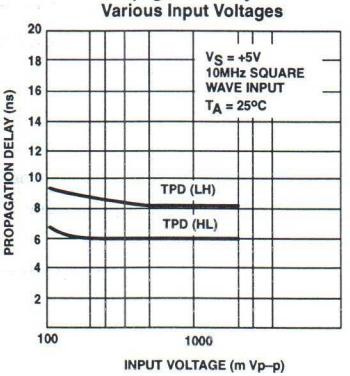
Response Time vs Temperature



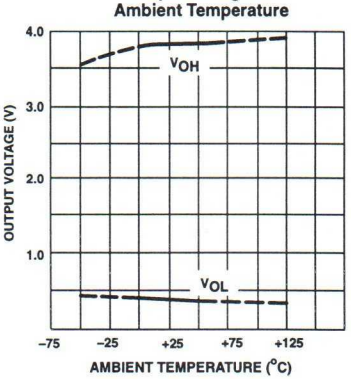
Propagation Delay for Various Input Voltages



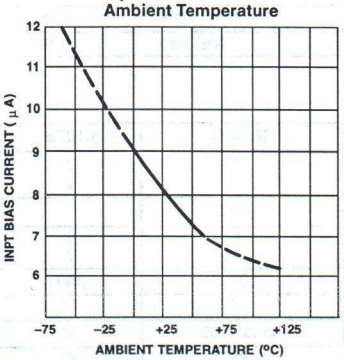
Propagation Delay for Various Input Voltages



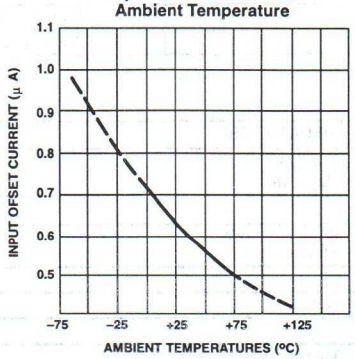
Output Voltage vs Ambient Temperature



Input Bias Current vs Ambient Temperature



Input Offset Current vs Ambient Temperature



High-speed dual-differential comparator/sense amp NE522

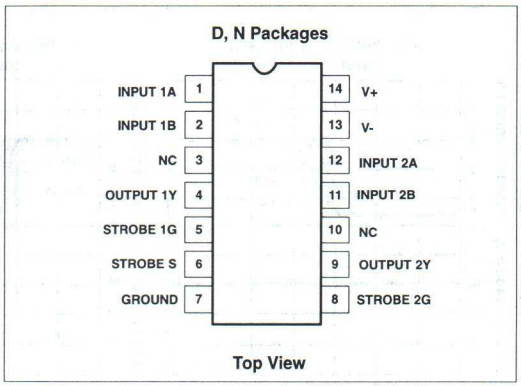
FEATURES

- 15ns maximum guaranteed propagation delay
- 20μA maximum input bias current
- TTL-compatible strobes and outputs
- Large common-mode input voltage range
- Operates from standard supply voltages

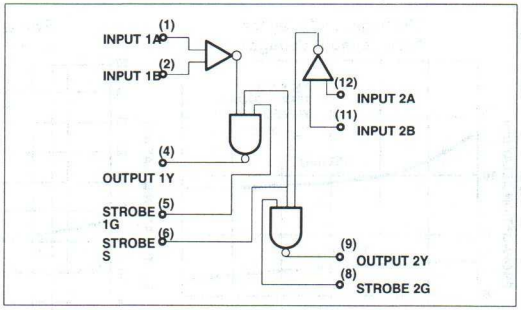
APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High-speed line receiver

PIN CONFIGURATION



BLOCK DIAGRAM



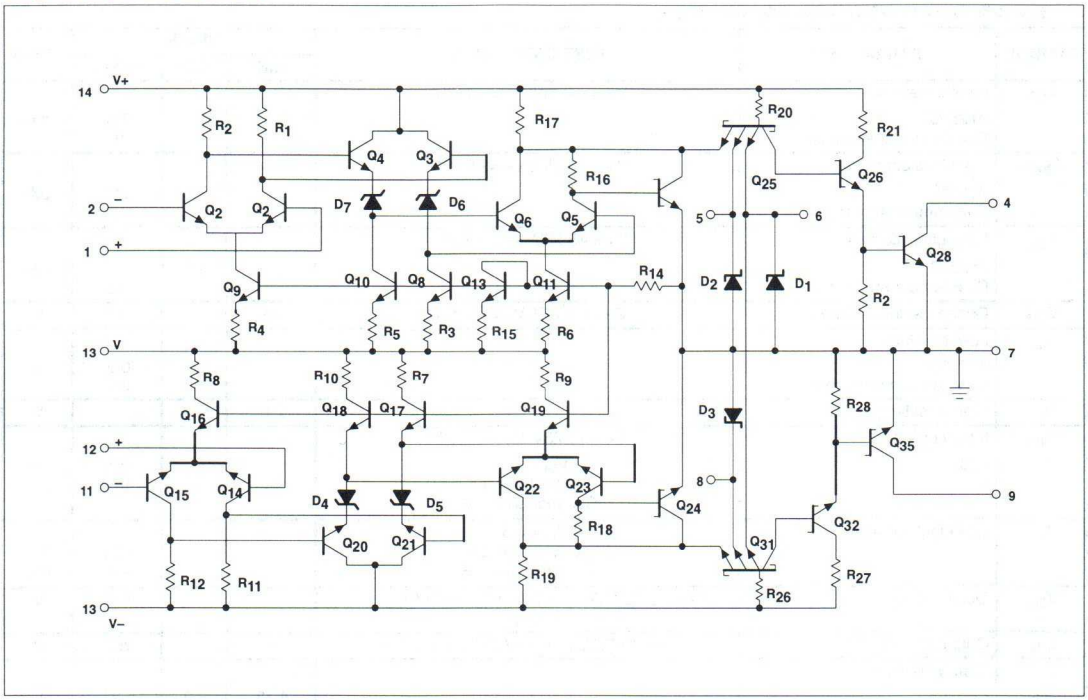
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic DIP	0 to +70°C	NE522N	0405B
14-Pin Plastic SO	0 to +70°C	NE522D	0175D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V+ V–	Single supply voltage	Positive Negative	+7 -7	V V
V_{IDR}	Differential input voltage		±6	V
V_{IN}	Input voltage	Common-mode Strobe/gate	± 5 +5.25	V V
P_D	Power dissipation		600	mW
T_A	Operating temperature range	NE522	0 to 70	°C
T_{STG}	Storage temperature range		-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)		+300	°C

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

$V\pm = \pm5V \pm5\%$, $T_A = 0$ to $+70°C$, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{OS}	Input offset voltage	V+ = +4.75V, V– = –4.75V				
	At 25°C			6	7.5	mV
	Over temperature range				10	
I_{BIAS}	Input bias current	V+ = +5.25V, V– = –5.25V				
	At 25°C			7.5	20	µA
	Over temperature range				40	
I_{OS}	Input offset current	V+ = +5.25V, V– = –5.25V				
	At 25°C			1.0	5	µA
	Over temperature range				12	
V_{CM}	Common-mode voltage range	V+ = +4.75V, V– = –4.75V	–3		+3	V
V_{IL}	Low level input					
	At 25°C				0.8	V
	Over temperature range				0.7	
V_{IH}	High level temperature		2.0			V
I_{IH}	Input current	V+ = +5.25V, V– = –5.25V				
	High	V_{IH} = 2.7V			50	µA
		1G or 2G strobe			100	µA
		Common strobe S				
I_{IL}	Low input current	V_{IL} = 0.5V				
		1G or 2G strobe			–2.0	mA
		Common strobe S			–4.0	mA
V_{OL}	Output voltage Low	V+ = +5.25V, V– = –5.25V, $V_{I(S)}$ = 2.0V, I_{LOAD} = 20mA			0.5	V
I_{OH}	Output current High	V+ = +4.75V, V– = –4.75V, V_{OH} = 5.25V			250	µA
	Supply voltage					
V+	Positive		4.75	5.0	5.25	V
V–	Negative		–4.75	–5.0	–5.25	
	Supply current	V+ = +5.25V, V– = –5.25V, T_A = 25°C				
I_{CC+}	Positive			27	35	mA
I_{CC-}	Negative			–15	–28	

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, R_L = 280Ω, C_L = 15pF, unless otherwise stated.

SYMBOL	PARAMETER	FROM INPUT	TO OUTPUT	LIMITS			UNITS
				MIN	TYP	MAX	
I_R	Input resistance				4		kΩ
I_C	Input capacitance				3		pF
Large-signal switching speed							
	Propagation delay						
$t_{PLH(D)}$	Low to high[1]	Amp	Output		10	15	
$t_{PHL(D)}$	High to low[1]	Amp	Output		8	12	ns
$t_{PLH(S)}$	Low to high[2]	Strobe	Output		6	13	
$t_{PHL(S)}$	High to low[2]	Strobe	Output		5	9	
I_{MAX}	Maximum operating frequency			25	35		MHz

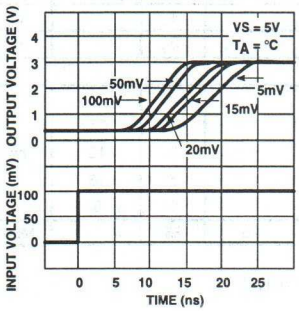
NOTES:
1. Response time measured from 0V point of ÷100mV$_{P-P}$ 10MHz square wave to the 1.5V point of the output.
2. Response time measured from 1.5V point of the input to 1.5V point of the output.

LOGIC FUNCTION TABLE

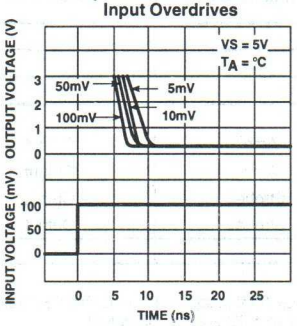
V_{ID} (A^+, B^-)	STRS	STRG	OUTPUT TRANSISTOR
$< -V_{OS}$	H	H	ON
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined
$> V_{OS}$	H	H	OFF
X	L	X	OFF
X	X	L	OFF

EQUIVALENT SCHEMATIC

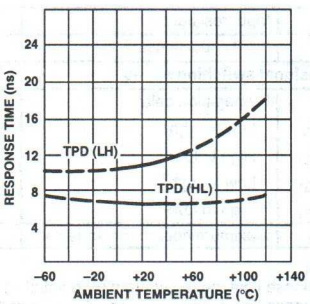
Response Time for Various Input Overdrives



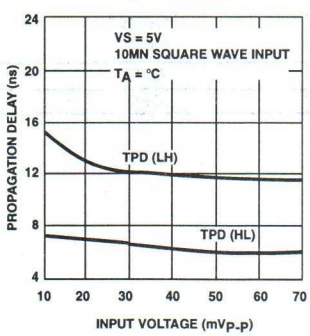
Response Time for Various Input Overdrives



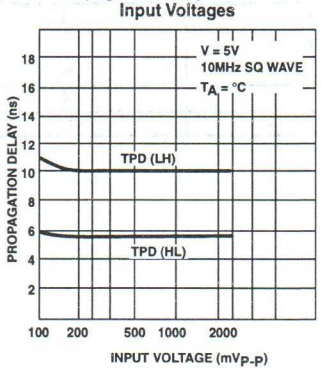
Response Time vs Temperature



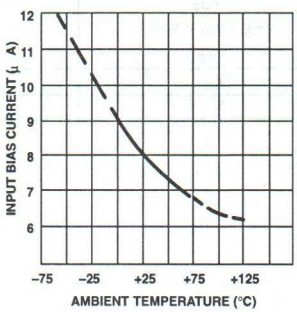
Propagation Delay for Various Input Voltages



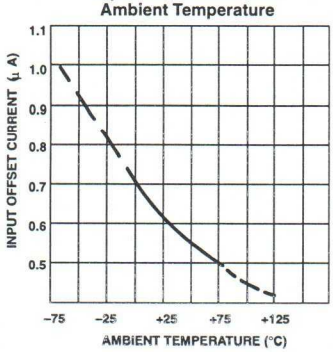
Propagation Delay for Various Input Voltages



Input Bias Current vs Ambient Temperature



Input Offset Current vs Ambient Temperature



Voltage comparator — NE527

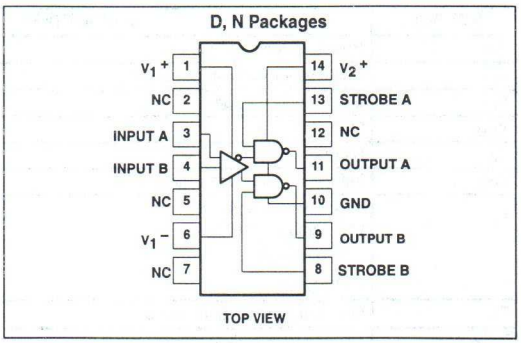
DESCRIPTION

The NE527 is a high-speed analog voltage comparator which, for the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed TTL gates with a precision linear amplifier on a single monolithic chip. The NE527 is similar in design to the Philips Semiconductors NE529 voltage comparator except that it incorporates an "Emitter-Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

FEATURES

- 15ns propagation delay
- Complementary output gates
- TTL or ECL compatible outputs
- Wide common-mode and differential voltage range
- Typical gain of 5000

PIN CONFIGURATIONS



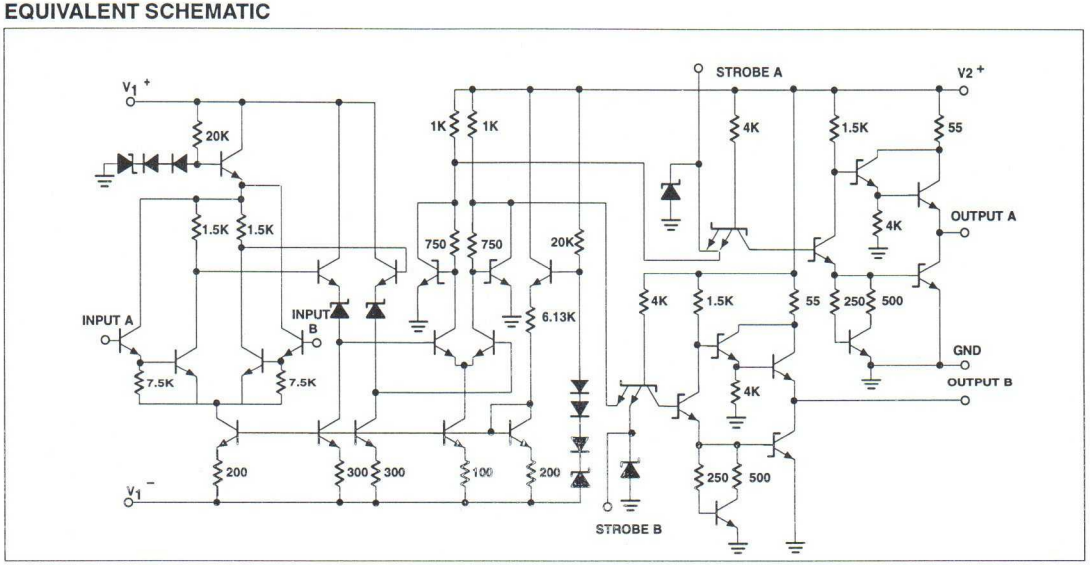
APPLICATIONS

- A/D conversion
- ECL-to-TTL interface
- TTL-to-ECL interface
- Memory sensing
- Optical data coupling

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE527N	0405B
14-Pin Small Outline (SO) Package	0 to +70°C	NE527D	0175D

EQUIVALENT SCHEMATIC

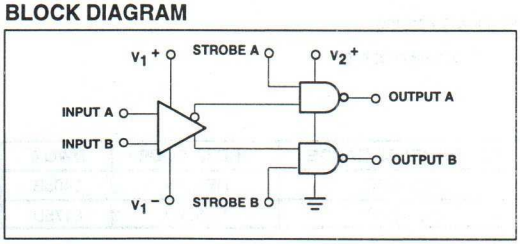


ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_1+	Positive supply voltage	+15	V
V_1-	Negative supply voltage	-15	V
V_2+	Gate supply voltage	+7	V
V_{OUT}	Output voltage	+7	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Input common mode voltage	±6	V
P_D	Max power dissipation[1] 25°C ambient (still air)		
	N package	1420	mW
	D package	1040	mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:
1. Derate above 25°C, at the following rates:
   N package 11.4mW/°C
   D package 8.3mW/°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V1+=10V, V1-=-10V, V2+=+5.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE527			UNIT
			Min	Typ	Max	
Input characteristics						
V_{OS}	Input offset voltage @ 25°C				6	mV
	over temperature range				10	
I_{BIAS}	Input bias current @ 25°C				2	µA
	over temperature range				4	
I_{OS}	Input offset current @ 25°C				0.75	µA
	over temperature range	V_{IN}=0V			1	µA
V_{CM}	Common-mode voltage range		-5		+5	V
Gate characteristics						
V_{OUT}	Output Voltage					
	"1" State	V_2+=4.75V, I_{SOURCE}=-1mA	2.7	3.3		V
	"0" State	V_2+=4.75V, I_{SINK}=10mA			0.5	V
	Strobe inputs					
	"0" Input current[1]	V_2+=5.25V, V_{STROBE}=0.5V			-2	mA
	"1" Input current @ 25°C[1]	V_2+=5.25V, V_{STROBE}=2.7V			100	µA
	Over temperature range	V_2+=5.25V, V_{STROBE}=2.7V			200	µA
	"0" Input voltage	V_2+=4.75V			0.8	V
	"1" Input voltage	V_2+=4.75V	2.0			V
I_{SC}	Short-circuit output current	V_2+=5.25V, V_{OUT}=0V	-18		-70	mA
Power supply requirements						
	Supply voltage					
V_1+			5		10	V
V_1-			-6		-10	V
V_2+			4.75	5	5.25	V
	Supply current	V_1+=10V, V_1-=-10V				
		V_2+=5.25V				
I_1+		Over temp.			5	mA
I_1-		Over temp.			10	mA
I_2+		Over temp.			20	mA

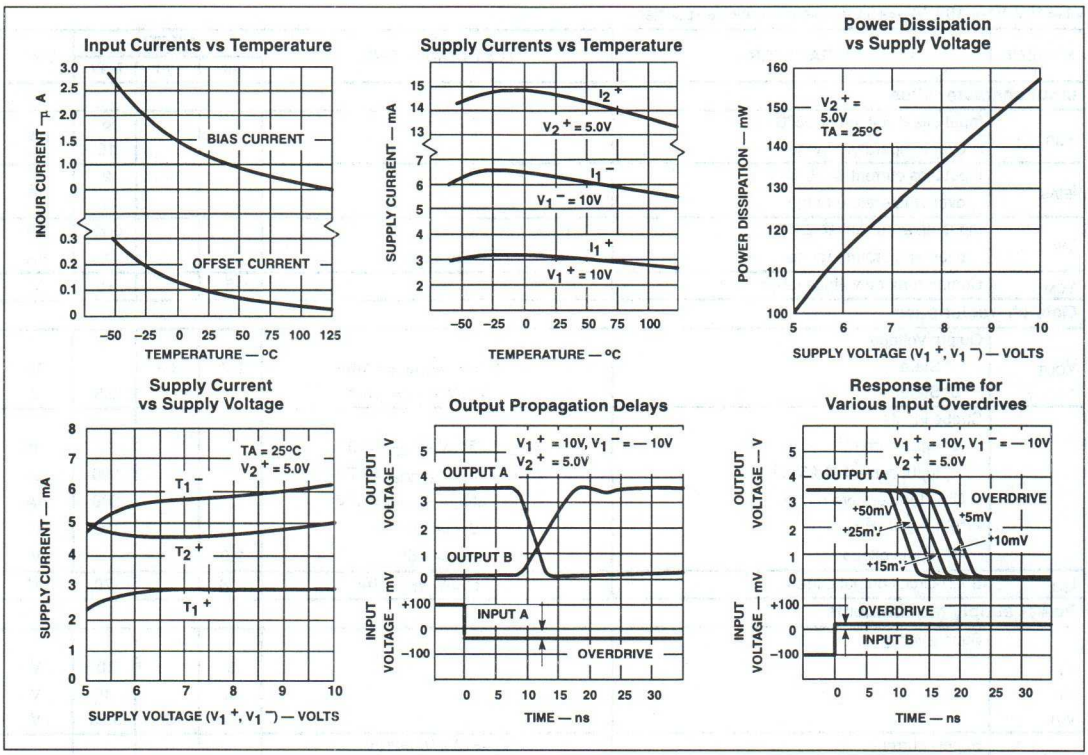
NOTES:
1. See Logic Function Table.

AC ELECTRICAL CHARACTERISTICS

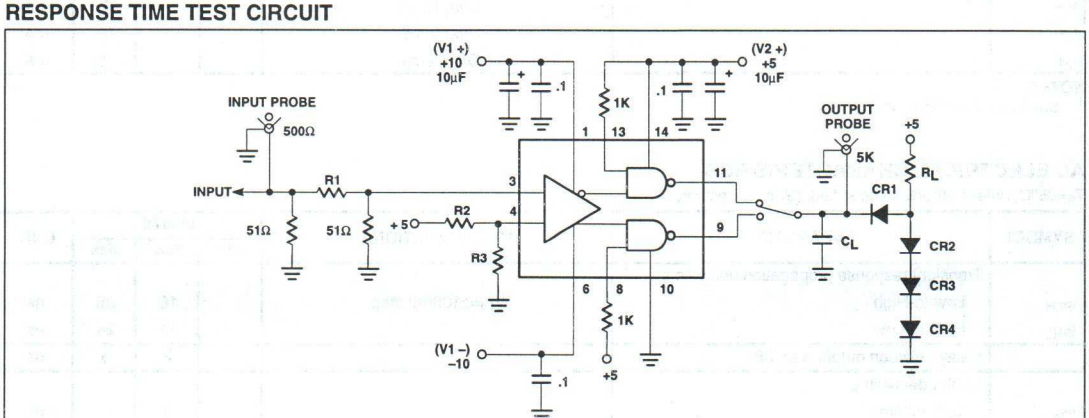
T_A=25°C, unless otherwise specified. (See AC test circuit)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Transient response propagation delay time					
t_{PLH}	Low-to-High	V_{IN}=±100mV step		16	26	ns
t_{PHL}	High-to-Low			14	24	ns
	Delay between output A and B			2	5	ns
	Strobe delay time					
t_{ON}	Turn-on time			6		ns
t_{OFF}	Turn-off time			6		ns

TYPICAL PERFORMANCE CHARACTERISTICS



RESPONSE TIME TEST CIRCUIT



NOTES:
CR1 — CR4 = IN914
R1 selected for 15.1 divider
R2, 3 selected for 100mV at Pin 4

Input
PRR = 1MHz
P_W = 50ns
$T_r = T_f$ = 2ns
Amplitude = 3.00V

Output
R_L = 390Ω
C_L = 25pF (including stray capacitance

Voltage comparator | NE527

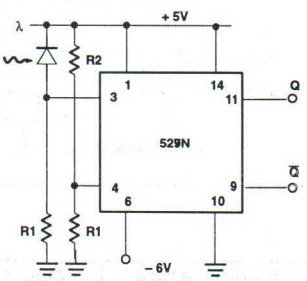
APPLICATIONS

One of the main features of the device is that supply voltages (V_1+, V_1-) need not be balanced, as in the following diagrams. For proper operation, however, negative supply (V_1-) should always be at least 6V more than the ground terminal (Pin 6). Input common-mode range should be limited to values of 2V less than the supply voltages (V_1+ and V_1-) up to a maximum of ±5V as supply voltages are increased. It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

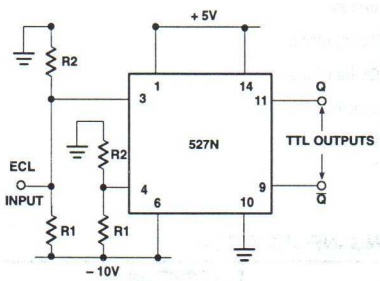
LOGIC FUNCTION

V_{ID} (A^+, B^-)	STROBE A	STROBE B	OUTPUT A	OUTPUT B	COMMENT
$V_{ID} \leq -V_{OS}$	H	X	L	H	Read I_{IHA}, I_{ILB}
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined	Undefined	
$V_{ID} \geq V_{OS}$	X	H	H	L	Read I_{ILA}, I_{IHB}
X	L	L	H	H	

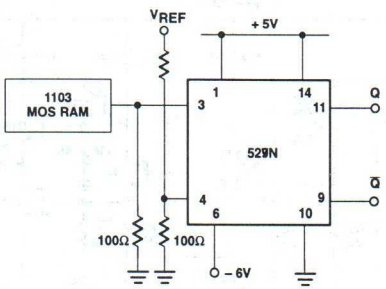
TYPICAL APPLICATIONS



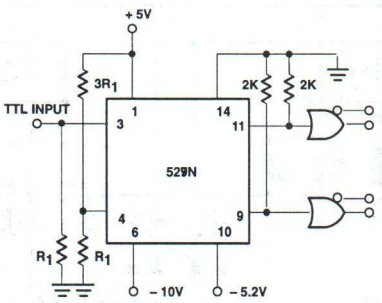
Photodiode Detector



ECL–to–TTL Interface



MOS Memory Sense AMP



TTL–to–ECL Interface

Voltage comparator — NE529

DESCRIPTION

The NE529 is a high-speed analog voltage comparator which, for the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high-speed TTL gates with a precision linear amplifier on a single monolithic chip.

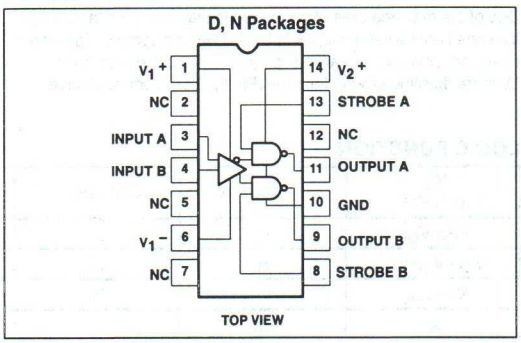
FEATURES

- 10ns propagation delay
- Complementary output gates
- TTL or ECL compatible outputs
- Wide common-mode and differential voltage range
- Typical gain 5000

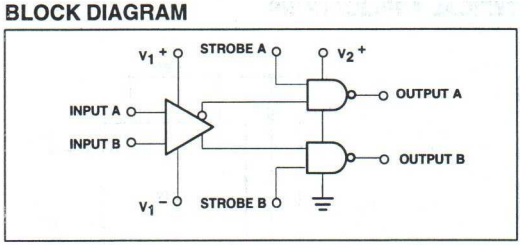
APPLICATIONS

- A/D conversion
- ECL-to-TTL interface
- TTL-to-ECL interface
- Memory sensing
- Optical data coupling

PIN CONFIGURATIONS

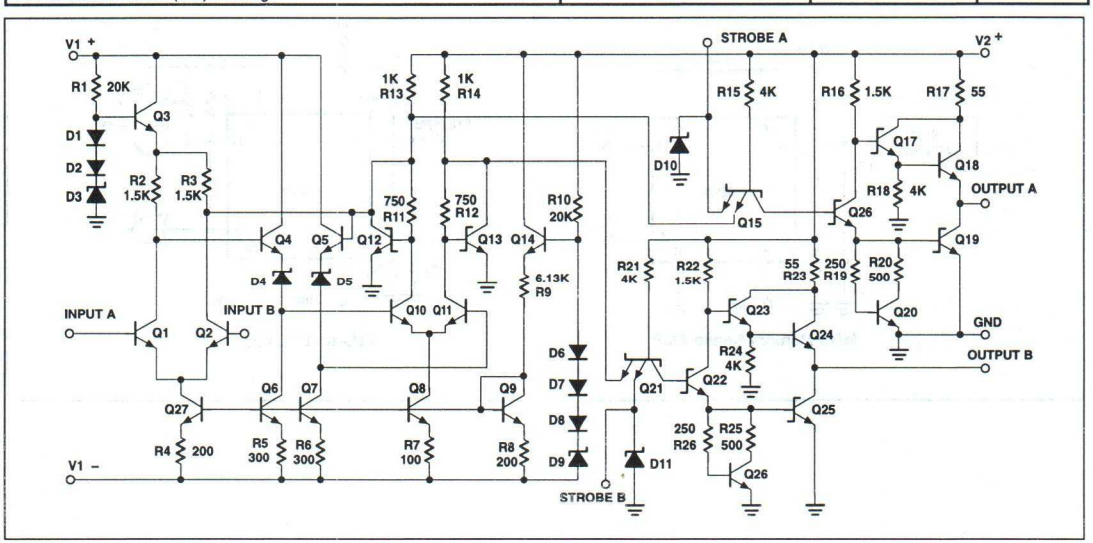


BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE529N	0405B
14-Pin Small Outline (SO) Package	0 to +70°C	NE529D	0175D



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_1+	Positive supply voltage	+15	V
V_1-	Negative supply voltage	-15	V
V_2+	Gate supply voltage	+7	V
V_{OUT}	Output voltage	+7	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Input common mode voltage	±6	V
P_D	Maximum power dissipation[1] T_A=25°C (still-air)		
	N package	1420	mW
	D package	1040	mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec max)	+300	°C

NOTES:
1. Derate above 25°C at the following rates:
   N package at 11.5mW/°C
   D package at 8.3mW/°C

DC ELECTRICAL CHARACTERISTICS

V_1+=+10V, V_2+=+5.0V, V_1-=-10V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE529			UNIT
			Min	Typ	Max	
Input characteristics						
V_{OS}	Input offset voltage @ 25°C				6	mV
	Over temperature range				10	
I_{BIAS}	Input bias current @ 25°C			5	20	µA
	Over temperature range	V_{IN}=0V			50	
I_{OS}	Input offset current @ 25°C			2	5	µA
	Over temperature range	V_{IN}=0V			15	µA
V_{CM}	Common-mode voltage range		-5	0		V
Gate characteristics						
V_{OUT}	Output voltage					
	"1" state	V_2+=4.75V, I_{SOURCE}=-1mA	2.7	3.3		V
	"0" state	V_2+=4.75V, I_{SINK}=10mA			0.5	V
	Strobe inputs					
	"0" Input current[1]	V_2+=5.25V, V_{STROBE}=0.5V			-2	mA
	"1" Input current @ 25°C[1]	V_2+=5.25V, V_{STROBE}=2.7V			100	µA
	Over temperature range	V_2+=5.25V, V_{STROBE}=2.7V			200	µA
	"0" input voltage	V_2+=4.75V			0.8	V
	"1" input voltage	V_2+=4.75V	2.0			V
I_{SC}	Short-circuit output current	V_2+=5.25V, V_{OUT}=0V	-18		-70	mA
Power supply requirements						
	Supply voltage					
V_1+			5		10	V
V_1-			-6		-10	V
V_2+			4.75	5	5.25	V
	Supply current	V_1+=10V, V_1-=-10V				
		V_2+=5.25V				
I_1+		Over temp.			5	mA
I_1-		Over temp.			10	mA
I_2+		Over temp.			20	mA

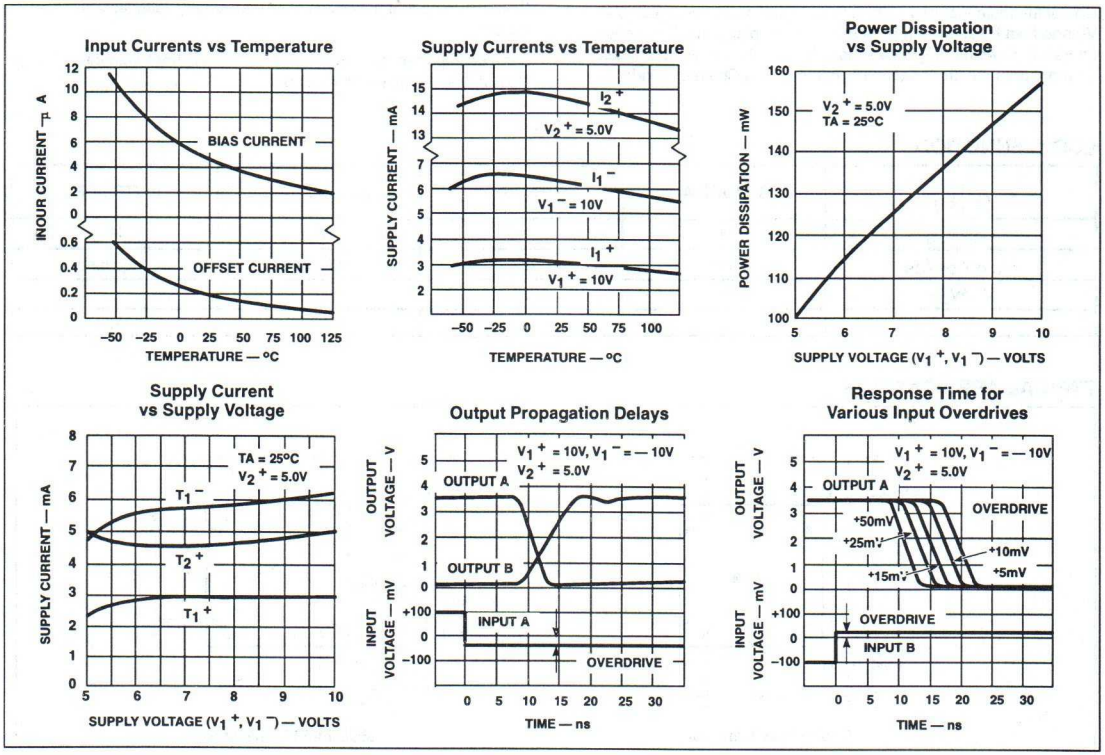
NOTES:
1. See logic function table.

AC ELECTRICAL CHARACTERISTICS

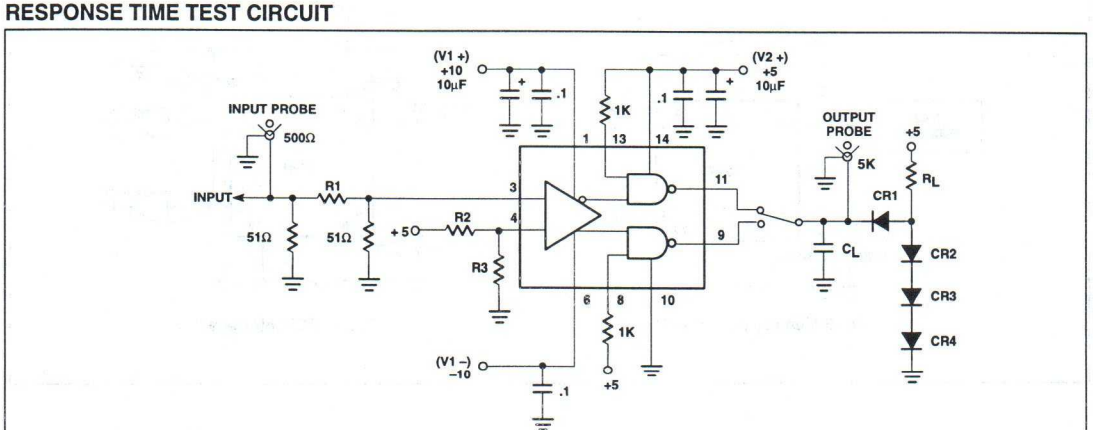
T_A=25°C (See AC test circuit).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_R	Transient response	V_{IN}=±100mV step				
	Propagation delay time					
t_{PLH}	Low-to-high			12	22	ns
t_{PHL}	High-to-low			10	20	ns
	Delay between output A and B			2	5	ns
	Strobe delay time					
t_{ON}	turn-on time			6		ns
t_{OFF}	turn-off time			6		ns

TYPICAL PERFORMANCE CHARACTERISTICS



RESPONSE TIME TEST CIRCUIT



NOTES:
CR1 — CR4 = IN914
R1 selected for 15.1 divider
R2, 3 selected for 100mV at Pin 4

Input
PRR = 1MHz
P_W = 50ns
$T_r = T_f$ = 2ns
Amplitude = 3.00V

Output
R_L = 390Ω
C_L = 25pF (including stray capacitance

APPLICATIONS

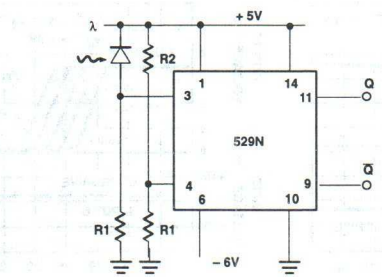
One of the main features of the device is that supply voltages (V+, V-) need not be balanced, as in the following diagrams. For proper operation, however, negative supply (V-) should always be at least 6V more than the ground terminal (pin 6). Input Common-Mode range should be limited to values of 2V less than the supply voltages (V+ and V-) up to a maximum of ±5V as supply voltages are increased.

It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

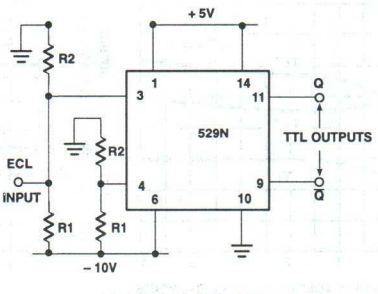
LOGIC FUNCTION

V_{ID} (A^+, B^-)	STROBE A	STROBE B	OUTPUT A	OUTPUT B
$V_{ID} \leq -V_{OS}$	H	X	L	H
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined	Undefined
$V_{ID} \geq V_{OS}$	X	H	H	L
X	L	L	H	H

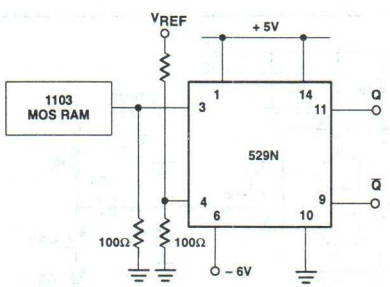
TYPICAL APPLICATIONS



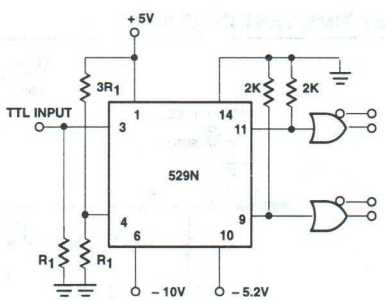
Photodiode Detector



ECL-to-TTL Interface



MOS Memory Sense AMP



TTL-to-ECL Interface

Applications for the NE521/522/527/529 — AN116

COMPARATORS

Voltage comparators are high gain differential input-logic output devices. They are specifically designed for open-loop operation with a minimum of delay time. Although variations of the comparator are used in a host of applications, all uses depend upon the basic transfer function. Device operation is simply a change of output voltage dependent upon whether the signal input is above or below the threshold input.

Comparator inputs are customarily marked with plus or minus signs to indicate their polarity. For example, the circuit of Figure 1 produces a logic 1 level when the non-inverting input is more positive than the reference voltage.

DEFINITIONS

Many similarities exist between operational amplifiers and the amplifier section of voltage comparators. In fact, op amps can be used to implement the comparator function at low frequencies.

Thus, the characteristic definitions presented here are similar to those reviewed for op amps.

Input Offset Voltage

As with operational amplifiers, the non-ideal comparator possesses some offset voltage. The definition differs slightly in that the output structure of comparators is digital rather than linear. Hence, input offset voltage is defined for comparators as the DC voltage required at the input to force the output to the logic threshold of ensuing devices (1.2V for TTL).

Input Offset Current

Imbalances of input bias current arise from small variances of the junction geometry of the differential input amplifier. As for op amps, the imbalance is referred to as input offset current.

Bias Current

As with op amps the input structure of comparators is usually a differential bipolar stage. Input bias current is the average of the two input currents.

Common-Mode Range

When specifying voltage comparators, one of the key parameters is common-mode range, which is defined as the range of voltages over which both inputs can be varied simultaneously without abnormal output voltage transitions or device degradation. This parameter must be kept uppermost in the designer's mind because the reference and signal voltages become common-mode signals at threshold. All ranges of input signals thus must be within the common-mode range of the input amplifier.

Voltage Gain

Specifications of voltage gain refer to the overall gain of the device, the bulk of which occurs in the amplifier section.

In general, higher gains would be advantageous for resolving smaller input signals. Of course, the propagation delay suffers due to the more severe saturation of the transistors. Typical gains for TTL output devices are set for 5000V/V. This gain provides 5V of output swing with 1mV input signal change for reasonable accuracy, but does not contribute severely to the overload recovery delay.

Propagation Delay

Voltage comparisons of analog signals with a reference voltage usually require that the operation take as little time as possible. Long delays in the comparator cause a pulse position error at the output since the analog signal in the meantime has changed value. At low frequencies the delay is of small consequence, but at higher frequencies, transit time becomes intolerable. Design of voltage comparator devices includes, as a prime goal, the minimizing of transit times.

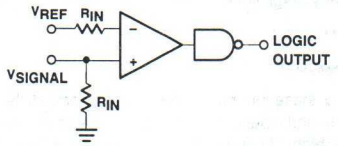


Figure 1. Basic Comparator Circuit

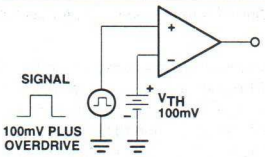


Figure 2. Propagation Delay Test Setup

Propagation delay testing is done under worst-case conditions. The recovery from saturation varies, depending upon the initial state of the amplifier and the overdrive. Worst-case conditions begin by applying a 100mV signal on the reference terminal. With no signal applied, the amplifier is in saturation in one direction. A step input pulse on the signal line of 100mV $\pm V_{OS}$ will bring the amplifier to a threshold level. Propagation delay at this point is undefined since the output has not switched.

To attain output switching, a small overdrive is necessary. Propagation delay is tested in a configuration such as Figure 2. The input is a step function of 100mV plus a specified excess or overdrive signal. This causes the amplifier to be exercised from saturation in one direction to saturation in the other for worst-case propagation delay. Note that larger overdrive reduces delay time as can be seen in Figure 3. An overdrive of 5mV causes 12ns delay, whereas a 100mV overdrive improves transit time to only 6ns.

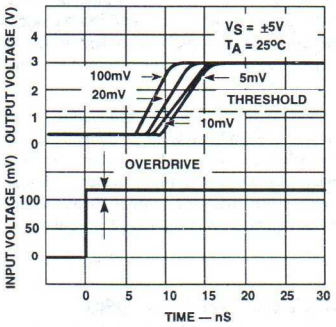


Figure 3. Response Time for NE/SE521 Comparator for Various Input Overdrives

If the measurement were made without initial saturation (less than 100mV/V threshold) the delay time would be less, due to the decreased storage times of unsaturated transistors.

Applications for the NE521/522/527/529 AN116

STATE-OF-THE-ART

Comparator design has always been optimized for four basic parameters. They are:

1. High Speed
2. Wide Input Voltage Range
3. Low Input Current
4. Good Resolution

Unfortunately, these four parameters are not compatible. For instance, gain and input current can be improved by using thinner diffusions for higher beta, but only at the expense of input voltage range. Higher gain also means higher saturation for an increase in delay time. So it becomes obvious that older comparators such as the 710 were designed with the best compromises in mind using standard processing.

One method of improving overall response adds gold doping to the processing flow. The gold dopant causes a decrease in minority carrier lifetime which aids the recombination process and shortens the saturation recovery time. Unfortunately, the transistor beta is adversely affected by gold, causing slightly higher bias and offset currents.

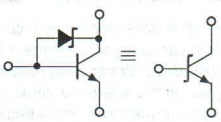


Figure 4. Schottky Clamped Transistor

It was not until the advent of the Schottky clamp that a vast improvement in speed without input degradation was possible. A very familiar term in the semiconductor industry, the Schottky barrier diode's (SBD) location is illustrated in Figure 4.

The Schottky clamped transistor is formed by paralleling the Schottky diode with the base-collector junction of the NPN transistor. Without the clamp, as base drive is increased the collector voltage falls until hard saturation occurs. At this point the collector voltage is very near the emitter voltage, and stored charges in the junctions causes slow recovery from saturation after base drive has been removed. The forward voltage drop of the Schottky diode is 0.4V—less than the forward drop of silicon diodes. This difference in forward drop is used by placing the diode across the transistor base-collector junction.

The Schottky diode becomes forward-biased when the collector voltage falls 0.4V below the base voltage. Excess base drive is then shunted into the collector circuit, prohibiting the transistor from reaching classic saturation. With almost no stored charge in either the SBD or the transistor, there is a large reduction in storage time. Thus, transistor switching time is significantly reduced.

A cross sectional area of the Schottky diode is shown in Figure 5.

COMPARING THE COMPARATORS

Presently available comparator ICs range from the ultra fast SE/NE521 to the general purpose comparator fashioned from an inexpensive op amp. Selection of the device depends upon the application in which it will be used. Speed of conversion is often of primary importance to minimize pulse position errors of high frequency signals. At other times the requirements are much less stringent, allowing the use of a general purpose comparator. A handy reference guide to the major parameters is summarized in Figure 6. The necessary parameters can be chosen to select the proper device.

A general description of the comparator devices is included here to familiarize the user with available devices and their advantages.

NE/SE521/522 Comparators

Processed with state-of-the-art Schottky barrier diodes, the NE521/522 series devices provide good input characteristics while providing the fastest analog-to-TTL conversion to date. Total delay from input to output is typically 6ns with a guaranteed speed of 12ns. Additional features of this device include the dual configuration and individual output strobes to simplify system logic. The NE522, although sacrificing some speed, features open-collector outputs for party line or wired-OR configurations for additional system flexibility.

NE/SE527 Comparator

Featuring Darlington inputs for very low bias current, the NE527 is generically related to the NE529 comparator. Emitter-follower inputs to the differential amplifier are used to trade better input parameters for slightly less speed. As Figure 6 shows, a factor of 10 improvement in I_{BIAS} is gained with a propagation delay increase of only 4ns maximum.

NE529 Comparator

The NE529 is manufactured using Schottky technology. Although a few nanoseconds slower than the NE521, the NE529 features variable supplies from ±5 to ±10V with a high common-mode range of ±6V. Both the NE527 and NE529 Schottky comparators boast complementary logic outputs with output A being in phase with input A. In addition, the supplies of both the NE527 and NE529 may be non-symmetrical to produce a desired shift in the common-mode range.

This technique is illustrated by the ECL-to-TTL and TTL-to-ECL transistor of Figures 16 and 17, respectively. The only major requirement of the supplies is that the negative supply be at least 5V more negative than the ground terminal of the gate. This is necessary to insure that the internal bias arrangement has sufficient voltage to operate normally.

APPLICATIONS

Today's state-of-the-art ultra high-speed comparators are capable of making logic decisions in less than 10ns. They are easily applied and possess good input and power supply noise rejection. As with all linear ICs, however, some preliminary steps should be taken in their use.

GENERAL PRECAUTIONS

Layout

The comparator is capable of resolving sub-millivolt signals. To prevent unwanted signals from appearing at signal ports, good physical layout is required. For any high-speed design, ground planes should be used to guard against ground loops and other sources of spurious signals. At high frequencies, hidden signal paths become dominant. Distributed capacitance is a particular nuisance. If care is not taken to isolate output from input, distributed capacitance can couple a few millivolts into the input, causing oscillation.

Another source of spurious signals is ground current. Input structures are relatively high impedance while the gate structures of comparators run with large signal and ground currents. If this gate

ground current is allowed to pass near the input signal path, the small impedances of the ground circuit will cause millivolt changes in reference or signal voltages producing errors, sustained oscillation, ringing, or excessive V_{OS}. A ground plane arranged such that output currents do not flow near input areas is highly recommended.

Power Supplies

Another general precaution that should always be exercised is power supply bypassing. As mentioned, the name of the game is speed. Very high-speed gates are used to produce the desired output logic levels. Maximizing response speed also requires higher current levels, giving rise to power supply noise. For this reason, good power supply bypassing very close to the device itself is always mandatory. A tantalum capacitor of 1 to 10μF in parallel with 500 to 1000pF will prove effective in most cases. Lead lengths should be as short as physically possible to preserve low impedances at high frequency.

Unused Inputs

Some currently available comparators such as the NE521 and NE522 are dual devices. Most often both sections of these devices will be utilized. Should a system utilize one device, the unused inputs should be biased in a known condition. The high gain-bandwidth may otherwise cause oscillations in the unused comparator section. A low impedance should be provided from both unused inputs to ground. A resistor of relatively high impedance may then be used to supply a differential input on the order of 100mV to insure the comparator assumes a known state.

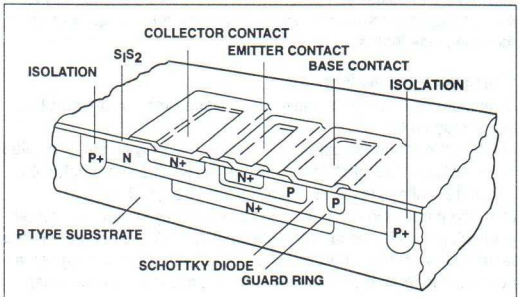


Figure 5. Schottky Clamped Transistor Geometry

DEVICE	PROP DELAY (ns)	V_{OS} (mV)	I_{OS} (μA)	I_{BIAS} (μA)	GAIN	CMR (V)	BENEFITS
NE521	12	7.5	5	20	5000	±3	Dual, very fast, standard supplies TTL compatible, individual & common strobe.
NE522	15	7.5	5	20	5000	±3	Same as NE521 plus open-collector outputs for additional decoding.
NE527	26	6	0.75	2	5000	±6	Fast, very low input current differential outputs, flexible surplus wide common-mode range.
NE529	22	6	5	20	5000	±6	Same as NE527 but with faster response.
LM311	200	7.5	0.05	0.25	200k	±30	High common-mode input range, ±5V to ±15V supply, strobe input, open-collector output.
LM319	80	8	0.2	1.2	40k	±5	Low input bias, dual, +5V to ±15V supply, open-collector output.
LM339	1300	2	0.05	0.25	200k	V+ −1.5V	Low input bias, dual, +5V to ±15V supply, open-collector output.
LM393	1300	2	0.05	0.25	200k	V+ −1.5V	Same as LM339 but dual.

NOTE:
Parameters are based on min/max limits at 25°C as defined in the individual data sheet.

Figure 6. Comparator Selection Guide

If the inverting input is tied to the positive differential voltage the gate output will be low. The strobe inputs then provide a means of utilizing the Schottky gate for other system logic functions.

If the strobe inputs are not used, they should be connected to the output of a logic gate that is always high, or to the +5V supply through a 5 to 10kΩ resistor. They should never be tied directly to the +5V supply as the relatively minor spiking on the supply may damage these inputs.

Common-Mode Signals

Manufacturers specify the maximum voltage range over which the inputs may be taken. In addition, the maximum differential voltage that may be safely applied to the inputs is specified. In the case of the NE529 comparator, the differential voltage is restricted to less than ±5V, with a common-mode of ±6V. That these two quantities interact cannot be overlooked. For instance, with both inputs at ±4V the common-mode restriction is satisfied. If V_{REF} is now left at +4V the signal input may not be taken more than 1V below ground because the differential signal becomes 5V.

It is important to observe this maximum rating since exceeding the differential input voltage limit and drawing excessive current in breaking down the emitter-base junctions of the input transistors could cause gross degradation in the input offset current and bias current parameters.

It is also important to note that response time is specified for a common-mode voltage of zero and may degrade when the common-mode voltage approaches the common-mode specification limits.

Exceeding the absolute maximum positive input voltage limit of the device will saturate the input transistor and possibly cause damage through excessive current. However, even if the current is limited to a reasonable value so that the device is not damaged, erratic operation can result.

Input Impedance

The differential bias and offset currents of comparators are minimized by design. As was pointed out for op amps, the input resistance seen by both inputs should be equal. This reduces to a minimum the contribution of offset current to threshold error. Unbalanced input impedance also adds to the offset error due to the difference in voltage drop across the input resistances.

BASIC APPLICATIONS

The basic comparator circuit and its transfer function were presented by Figure 1.

When the input exceeds the reference voltage, the output switches either positive or negative, depending on how the inputs are connected.

The vast majority of specific applications involve only the basic configuration with a change of reference voltage. A-to-D converters are realized by applying the signal to one terminal and the voltage derived from a ladder network to the other. Limit detectors are likewise made from only the very basic circuit. Both are only a small deviation from the basic level detector.

Hysteresis

Normally saturated high or low, the amplifiers used in voltage comparators are seldom held in their threshold region.

They possess high gain-bandwidth products and are not compensated to preserve switching speed. Therefore, if the compared voltages remain at or near the threshold for long periods of time, the comparator may oscillate or respond to noise pulses. For instance, this is a common problem with successive approximation D/A converters where the differential voltage seen by the comparator becomes successively smaller until noise signals cause indecision. To avoid this oscillation in the linear range, hysteresis can be employed from output to input. Figure 7 defines the arrangement. Both positive and negative feedback is provided by R_{IN} and R_F.

Hysteresis occurs because a small portion of the "one" level output voltage is fed back in phase and added to the input signal. This feedback aids the signal in crossing the threshold. When the signal returns to the threshold, the positive feedback must be overcome by the signal before switching can occur. The switching process is then assured and oscillations cannot occur. The threshold "dead zone" created by this method, illustrated in Figure 8, prevents output chatter with signals having slow and erratic zero crossings.

As shown in Figure 7, the voltage feedback is calculated from the expression:

$$V_{HYST} = \frac{E_{OUT} \cdot R_{IN}}{R_{IN} + R_F}$$

where E_{OUT} is the gate high output voltage.

The hysteresis voltage is bounded by the common-mode range and the ability of the gate to source the current required by the feedback network. If symmetrical hysteresis is desired, an additional inverting gate is required if the comparator does not have differential outputs. The NE527 and NE529 devices provide inverted signals from differential outputs while the NE521 and NE522 devices will require the inverter. Care should be taken in the selection of the inverter that propagation delay is minimum, especially for very high-speed comparators such as the NE521.

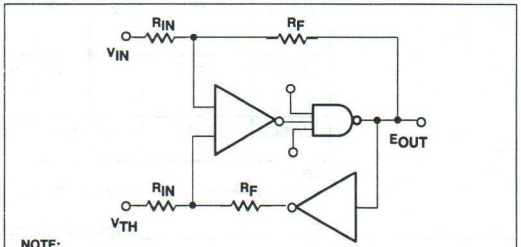


Figure 7. Level Detector With Hysteresis

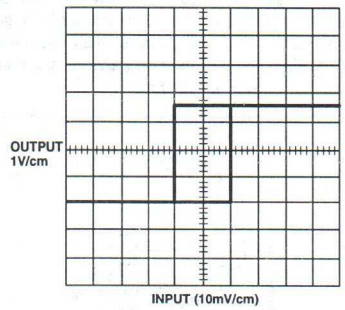


Figure 8. 0V Level Detector With ±10mV Hysteresis

Line Receiver

Retrieving signals which have been transmitted over long cables in the presence of high electrical noise is a perfect application for differential comparators. Such systems as automated production lines and large computer systems must transmit high frequency digital signals over long distances.

If the twisted-pair of the system is driven differentially from ground, the signals can be reclaimed easily via a differential line receiver.

Since the electrical noise imposed upon a pair of wires takes the form of a common-mode signal, the very high common-mode rejection of the NE521/522 makes the unit ideal for differential line receivers. Figure 9 depicts the simple schematic arrangement. The NE521 is used as a differential amplifier having a logic level output. Because common-mode signals are rejected, noise on the cable disappears and only the desired differential signal remains. Figure 10 illustrates the NE521 response to the 200mV$_{P-P}$ 10MHz differential signal. In Figure 11 the same signal has been buried in 5V$_{P-P}$ of 1MHz common-mode "noise."

The circuit suffers no degradation of signal. If desired, several NE522 comparators may be "wire-ORed," or a latched output can be built as shown in Figure 9.

The NE521 and NE529 comparators have the advantage of wider bandwidth to permit higher data rates.

Double-Ended Limit (Window) Detector

Many system designs require that it be known when a signal level lies between two limits. This function is easily accomplished with a single NE522 package. The schematic and transfer curve of the circuit is shown in Figure 12.

Each half of the NE522 is referenced to the desired upper or lower voltage limit producing the desired transfer curve shown. Taking advantage of the dual configuration and the open-collectors of the NE522 minimizes external components and connections.

Crystal Oscillator

Any device with a reasonable gain can be made to oscillate by applying positive feedback in controlled amounts. The NE521 will lend itself to crystal control easily, provided the crystal is used in its fundamental mode. Figure 13 shows a typical oscillator circuit.

The crystal is operated in its series-resonant mode, providing the necessary feedback through the capacitor to the input of the NE521. The resistor R_{ADJ} is used to control the amount of feedback for symmetry. Oscillations will start whenever a circuit disturbance such as turning on the power supplies occurs. The NE521 will oscillate up to 70MHz. However, crystals with frequencies higher than about 20MHz are usually operated in one of their overtones. To build an oscillator for a specific overtone requires tuned circuits in addition to the crystal to provide the necessary mode suppression. If the spurious modes are not tuned out, the crystal will oscillate at the fundamental frequency. Higher frequency oscillators could be realized using input and output mode suppression or tuning. The NE522 is especially desirable since the open-collector topology allows the output to be collector-tuned readily.

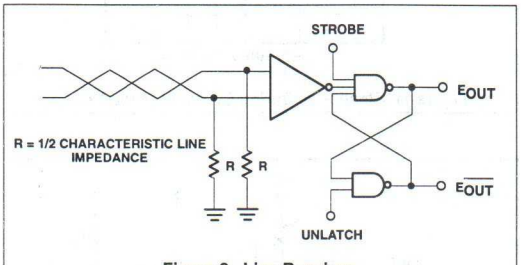


Figure 9. Line Receiver

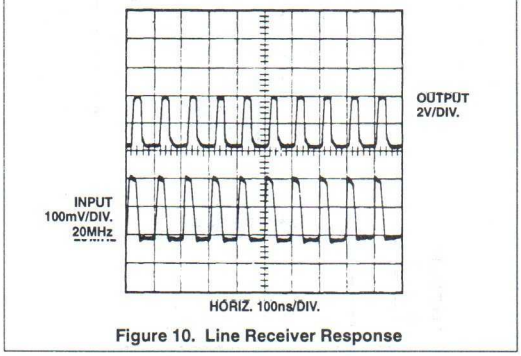


Figure 10. Line Receiver Response

Analog-to-Digital Converter

There are many types of A-to-D converter designs, each having its own merits. However, where speed of conversion is of prime interest, the multi-threshold conversion type is used exclusively. It is apparent from Figure 14 that the conversion speed of this design is the sum of the delay through the comparator and the decoding gates.

The sacrifices which must be made to obtain speed are the number of components, bit accuracy and cost. The number of comparators needed for an N-bit converter is 2n-1. Although the NE521 provides two comparators per package, the length of parallel converters is usually limited to less than 4 bits. Accuracy of multi-threshold A-D

converters also suffers since the integrity of each bit is dependent upon comparator threshold accuracy.

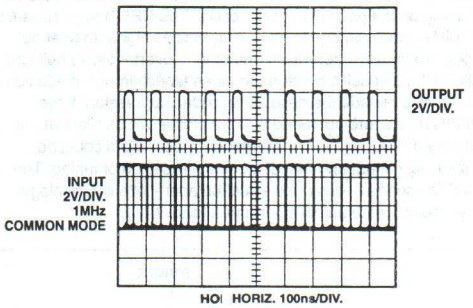


Figure 11. Response During Common-Mode Noise

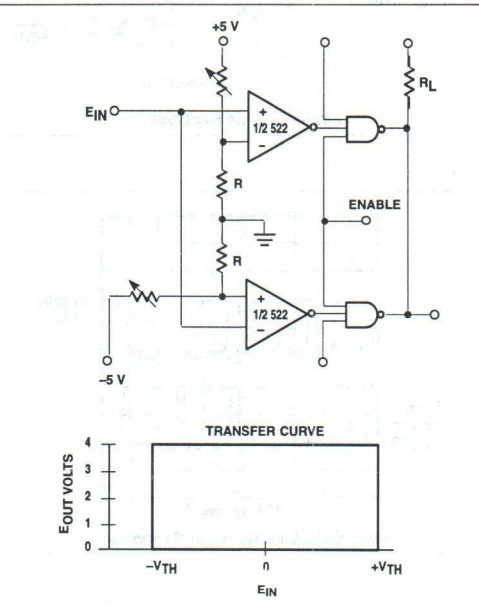


Figure 12. Double-Ended Limit Detector

The implementation of a 3-bit parallel A/D converter is shown in Figure 15 with a 3-bit digital equivalent of an analog input shown in Figure 14.

Reference voltages for each bit are developed from a precision resistor ladder network. Values of R and 2R are chosen so that the threshold is one half of the least significant bit. This assures maximum accuracy of ± bit.

It is apparent from the schematic that the individual strobe line and duality features of the NE521 have greatly reduced the cost and complexity of the design. The speed of the converter is graphically illustrated by the photo of Figure 14. All 3-bit outputs have settled and are true a mere 15ns after the input step of 3V has arrived. The output is usually strobed into a register only after a certain time has elapsed to insure that all data has arrived.

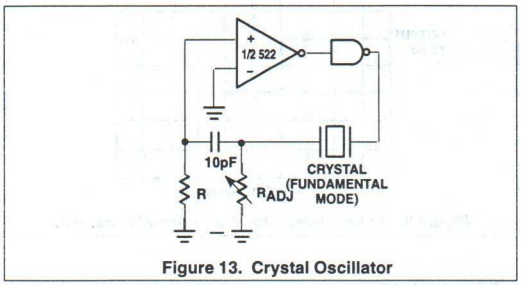


Figure 13. Crystal Oscillator

Logic Interface

During the design of the NE527 and NE529 devices, particular attention was paid to the biasing network so that balanced supplies need not be provided. For example, if the "ground" terminal is set at -5.2V and the other supplies are adjusted accordingly, the output logic 1 state will be at -1.5V and logic 0 will be at -5.0V. With this freedom of power supply voltage, the user may adjust the output swings to match the desired logic levels even if that logic is other than TTL levels.

ECL-to-TTL Interface

Emitter-coupled logic is very popular due to its speed. Systems are often built around standard TTL logic with those portions requiring higher speed being implemented with emitter-coupled logic. As soon as such a decision is made the problem of interfacing TTL-to-ECL logic levels is encountered.

The standard logic output swings of ECL are -0.8V to -1.8V at room temperature. Converting these signals to TTL levels is accomplished simply by using the basic voltage comparator circuit with slight modifications. Figure 16 reveals that the power supplies have been shifted in order to shift the common-mode range more negative.

This insures that the common-mode range is not exceeded by the logic inputs. Since ECL is extremely fast, the NE529 is usually selected because of its superior speed so that a minimum of time is lost in translation.

TTL-to-ECL INTERFACE

Operating in the reverse, TTL levels can also be converted to ECL levels by the NE529. Again the NE529 is selected as the fastest converter with the necessary power supply flexibility to accomplish the level shifting with a minimum of effort and cost.

A check of output voltage for the NE529 reveals that the voltage is slightly less than required by the ECL logic for fast switching. R2 and the diode of Figure 17 raises the gate supply voltage and therefore the NE529 output voltage by 0.7, sufficient to guarantee fast switching of the translator. Resistive pull-up from the NE529 output to V_{CC} can also be used with the gate supply grounded. This method is dependent upon RC time constants of distributed capacitance and is therefore much slower.

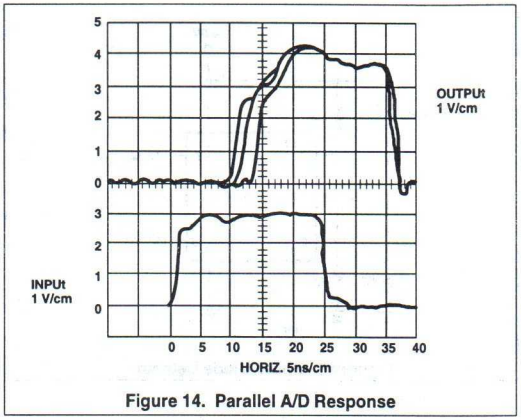


Figure 14. Parallel A/D Response

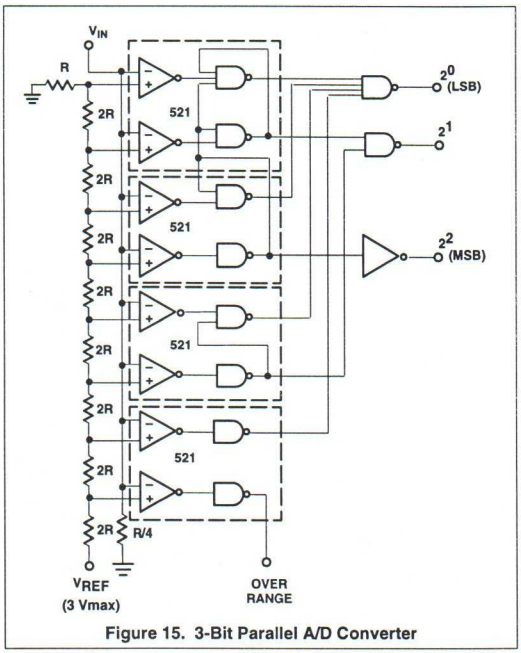


Figure 15. 3-Bit Parallel A/D Converter

Photo Diode Detector

Responding to the presence or absence of light, the photo diode increases or decreases the current through it. Detecting the changes becomes a matter of converting light and dark currents to voltage across a resistor as shown in Figure 18. R1 is selected to be large enough to generate detectable differences between light and dark conditions. Once the signal levels are defined by R1 and the diode characteristics, the average between light and dark signals is used for V reference and is produced by the resistive divider consisting of R1 and R2. The comparator then produces an output dependent upon the presence or absence of light upon the diode.

SENSE AMPLIFIERS

Closely related to the comparator is the sense amplifier. Signals derived from the many sources, such as transducers, are not of sufficient amplitude to be compatible with subsequent logic. It then becomes necessary to amplify and convert the signal to TTL levels, which is the responsibility of the sense amplifier.

Some transducers produce an output current. It remains, then, for the user to convert these currents to TTL levels. A terminating resistor from the drain to ground provides a voltage output proportional to the current and the resistor size. Larger signals can be produced by larger resistors; but in practice, resistors larger than 1kΩ are avoided because of increasing access time. Distributed capacitance forms a time constant with this output resistance causing slow rise and fall times when the resistor is large, adding to the access time.

Virtually any voltage comparator or sense amplifier can be used. Since total time is the sum of all delays, the sense amplifier is most often the fastest available. Philips Semiconductors comparators NE521 and NE522 are ideal in this application because of low input offset voltages and very fast response. Using these Schottky clamped comparators significantly reduces the total cycle time of the memory.

Design of the sense amplifier network depends upon the transducer used and the input characteristics of the sense amplifier. The significant specifications are given in Table 1.

Consideration must first be given to the differential input voltage requirements of the sense amplifier. The required reference voltage is calculated from the relationship:

$$V_{REF} \leq (I_T - I_B)R1 - V_{DIFF}$$

Where I_T is the transducer output current, I_B is sense amplifier bias current and V_{DIFF} is minimum differential voltage to switch the sense amplifier.

In large systems, noise coupled into the sense lines by stray capacitance can be very troublesome. Judicious layout patterns with sense lines as short as possible will help, but will not always be sufficient. One method of eliminating noise is to use a balance sense line as shown in Figure 19.

A dummy line should be run parallel to the actual sense line in as close proximity as possible. One end is connected to the sense amplifier at the V_{REF} point while the other end is left open. The normal sense line is connected as usual. Electrical noise imposed upon the pair of sense lines takes the form of a common-mode signal and will be rejected by the sense amplifier. Signal currents in the sense line, on the other hand, form differential signals at the sense amp, causing the output to switch.

Table 1. Important Sense Amplifier Parameters

DEVICE	V_{OS} (mV)	I_B (μA)	$V_{IN\ (MIN)}$ (mV)	SPEED (ns) (V_{IN}=100mV)	GAIN
521	10	40	15	12	5000
522	10	40	15	15	5000

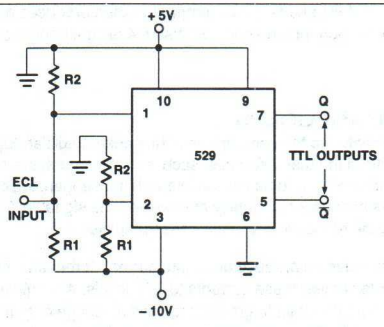


Figure 16. ECL-to-TTL Translator

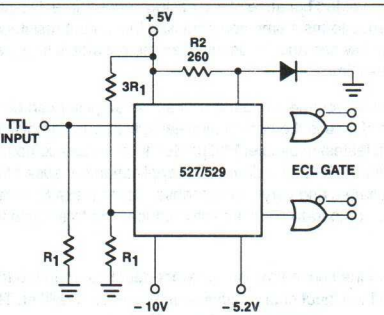


Figure 17. TTL-to-ECL Translator

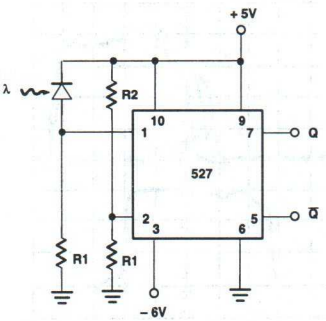


Figure 18. Photo Diode Detector

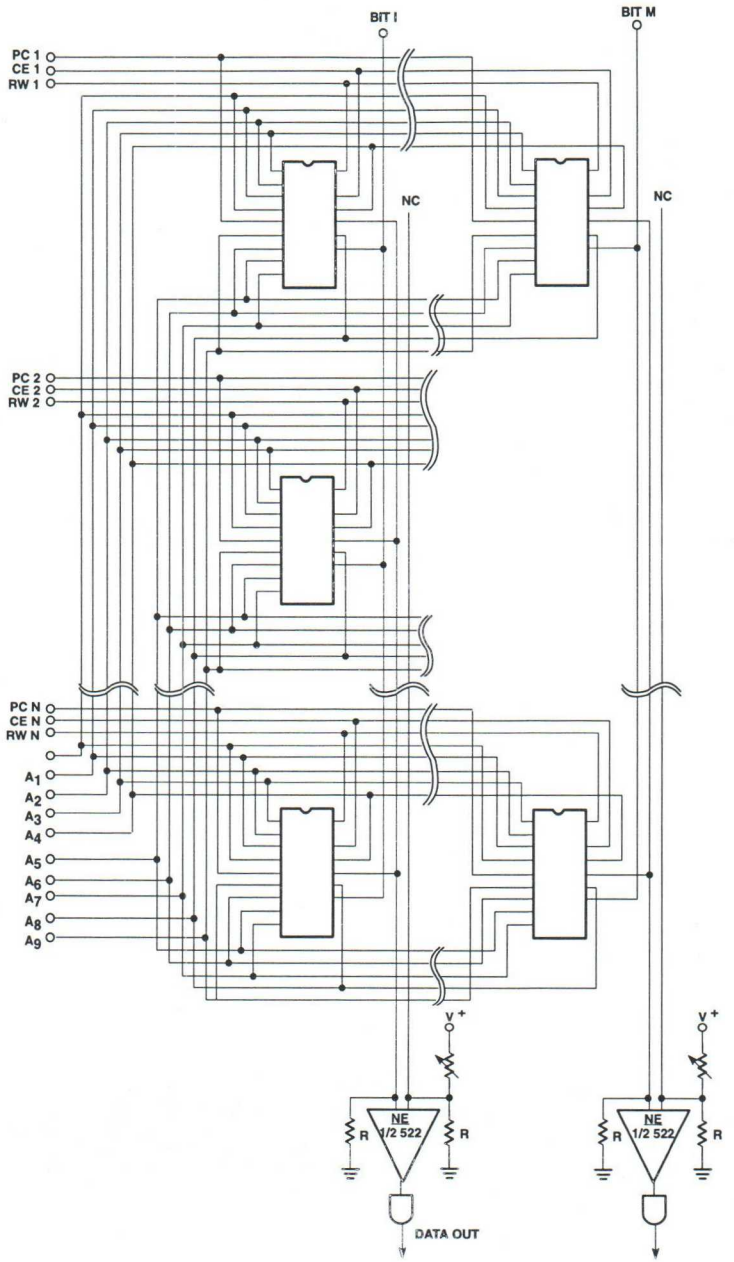


Figure 19. Balanced Sense Line to Reduce Noise

Section 5
Timers

INDEX

ICM7555	General purpose CMOS timer	337
NE/SA/SE555/SE555C	Timer	346
NE/SA/SE556/ NE556-1	Dual timer	353
AN170	NE555 and NE556 applications	358
NE558	Quad timer	378
AN171	NE558 applications	382

General purpose CMOS timer — ICM7555

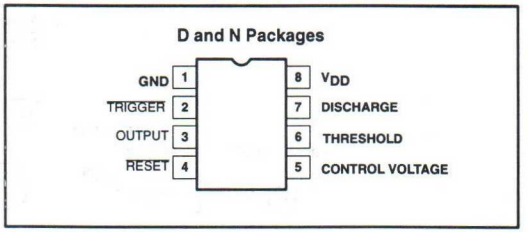
DESCRIPTION

The ICM7555 is a CMOS timer providing significantly improved performance over the standard NE/SE555 timer, while at the same time being a direct replacement for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, TRIGGER, and RESET currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

The ICM7555 is a stable controller capable of producing accurate time delays or frequencies.

In the one-shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the bipolar 555 device, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The TRIGGER and RESET inputs are active low. The output inverter can source or sink currents large enough to drive TTL loads or provide minimal offsets to drive CMOS loads.

PIN CONFIGURATION



- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- High output source/sink driver can drive TTL/CMOS
- Typical temperature stability of 0.005%/°C at 25°C
- Rail-to-rail outputs

FEATURES

- Exact equivalent in most applications for NE/SE555
- Low supply current: 80µA (typ)
- Extremely low trigger, threshold, and reset currents: 20pA (typ)
- High-speed operation: 500kHz guaranteed
- Wide operating supply voltage range guaranteed 3 to 16V over full automotive temperatures
- Normal reset function; no crowbarring of supply during output transition
- Can be used with higher-impedance timing elements than the bipolar 555 for longer time constants

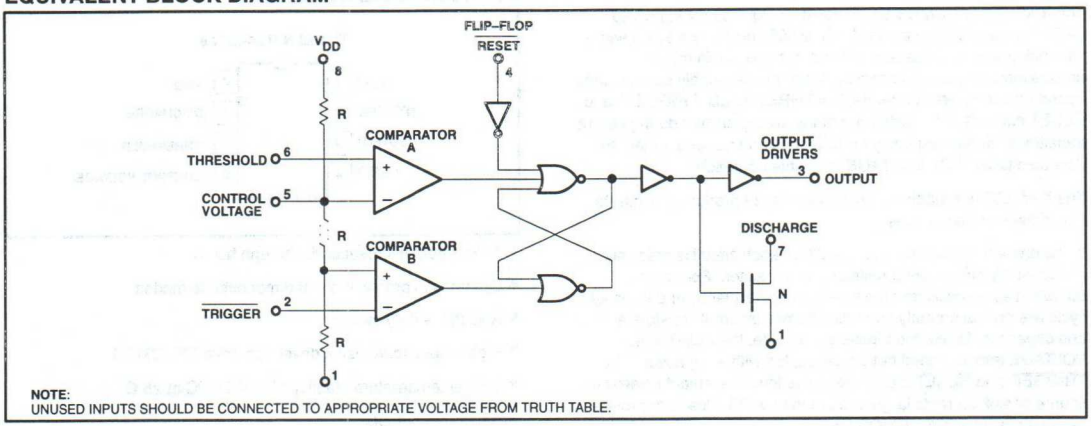
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	ICM7555CN	0404B
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	ICM7555CD	0174C
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	ICM7555IN	0404B
8-Pin Plastic Small Outline (SO) Package	-40 to +85°C	ICM7555ID	0174C

EQUIVALENT BLOCK DIAGRAM



NOTE:
UNUSED INPUTS SHOULD BE CONNECTED TO APPROPRIATE VOLTAGE FROM TRUTH TABLE.

TRUTH TABLE

THRESHOLD VOLTAGE	$\overline{\text{TRIGGER}}$ VOLTAGE	$\overline{\text{RESET}}$[1]	OUTPUT	DISCHARGE SWITCH
DON'T CARE	DON'T CARE	LOW	LOW	ON
>2/3(V+)	> 1/3(V+)	HIGH	LOW	ON
V_{TH} < 2/3	V_{TR} > 1/3	HIGH	STABLE	STABLE
DON'T CARE	<1/3(V+)	HIGH	HIGH	OFF

NOTES:
1. $\overline{\text{RESET}}$ will dominate all other inputs: $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	+18	V
V_{TRIG}[1]	$\overline{\text{Trigger}}$ input voltage		
V_{CV}	Control voltage	> -0.3 to	
V_{TH}	Threshold input voltage	<V_{DD} + 0.3	V
V_{RST}	$\overline{\text{RESET}}$ input voltage		
I_{OUT}	Output current	100	mA
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still air)[2]		
	N package	1160	mW
	D package	780	mW
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead temperature (Soldering 60s)	300	°C

NOTES:
1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} + 0.3V or less than GND -0.3V may cause destructive latch-up. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555 must be turned on first.
2. Derate above 25°C, at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C
3. See "Power Dissipation Considerations" section.

DC AND AC ELECTRICAL CHARACTERISTICS

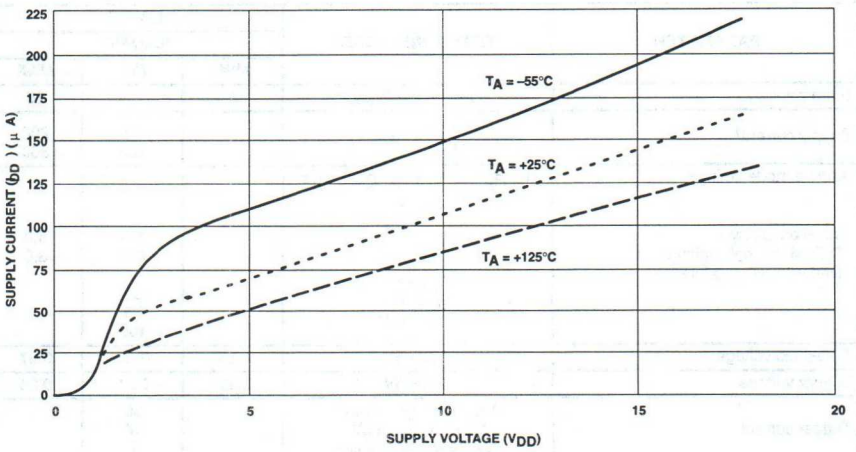
$T_A = 25^{\circ}C$ unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			ICM7555			
			MIN	TYP	MAX	
V_{DD}	Supply voltage	$T_{MIN} \le T_A \le T_{MAX}$	3		16	V
I_{DD}	Supply current[1]	$V_{DD} = V_{MIN}$ $V_{DD} = V_{MAX}$		50 180	200 300	µA µA
	Astable mode timing[2] Initial accuracy Drift with supply voltage Drift with temperature[3]	R_A, R_B = 1k to 100k, C = 0.1µF 5V <V_{DD} <15V V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		 1.0 0.1 50 75 100	 5.0 3.0	 % %/V ppm/°C ppm/°C ppm/°C
V_{TH}	Threshold voltage	V_{DD} = 5V	0.63	0.65	0.67	xV_{DD}
V_{TRIG}	Trigger voltage	V_{DD} = 5V	0.29	0.31	0.34	xV_{DD}
I_{TRIG}	Trigger current	$V_{DD} = V_{TRIG} = V_{MAX}$ $V_{DD} = V_{TRIG}$ = 5V $V_{DD} = V_{TRIG} = V_{MIN}$		50 10 1		pA pA pA
I_{TH}	Threshold current	$V_{DD} = V_{TH} = V_{MAX}$ $V_{DD} = V_{TH}$ = 5V $V_{DD} = V_{TH} = V_{MIN}$		50 10 1		pA pA pA
I_{RST}	Reset current	$V_{DD} = V_{RST} = V_{MAX}$ $V_{DD} = V_{RST}$ = 5V $V_{DD} = V_{RST} = V_{MIN}$		100 20 2		pA pA pA
V_{RST}	Reset voltage	$V_{DD} = V_{MIN}$ and V_{MAX}	0.4	0.7	1.0	V
V_{CV}	Control voltage	V_{DD} = 5V	0.62	0.65	0.67	xV_{DD}
V_{OL}	Output voltage (low)	$V_{DD} = V_{MAX}$, I_{SINK} = 3.2mA V_{DD} = 5V, I_{SINK} = 3.2mA		0.1 0.2	0.4 0.4	V V
V_{OH}	Output voltage (high)	$V_{DD} = V_{MAX}$, I_{SOURCE} = -1.0mA V_{DD} = 5V, I_{SOURCE} = -1.0mA	15.25 4.0	15.7 4.5		V_{DD} V_{DD}
V_{DIS}	Discharge output voltage	V_{DD} = 5V, I_{DIS} = 10.0mA		0.2	0.4	V
t_R	Rise time of output[3]	R_L = 10MΩ, C_L = 10pF, V_{DD} = 5V		45	75	ns
t_F	Fall time of output[3]	R_L = 10MΩ, C_L = 10pF, V_{DD} = 5V		20	75	ns
F_{MAX}	Maximum oscillator frequency (astable mode)		500			kHz

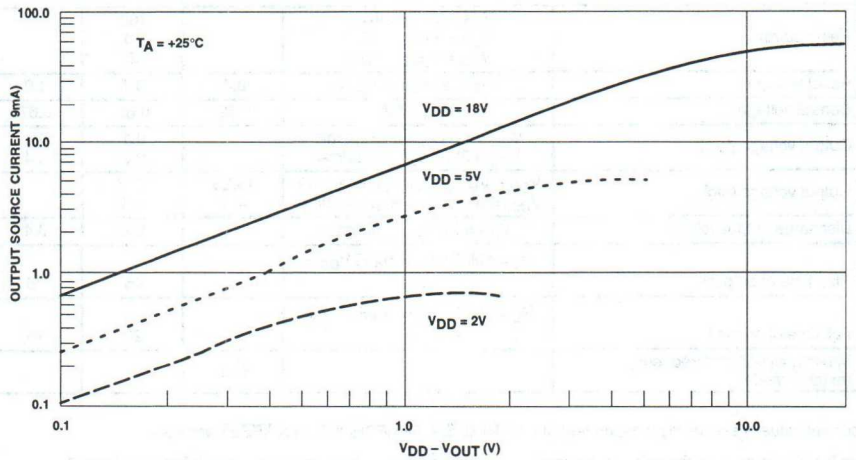
NOTES:

1. The supply current value is essentially independent of the $\overline{\text{TRIGGER}}$, THRESHOLD, and $\overline{\text{RESET}}$ voltages.
2. Astable timing is calculated using the following equation: $f = \frac{1.38}{(R_A + 2R_B)C}$. The components are defined in Figure 2.
3. Parameter is not 100% tested.

TYPICAL PERFORMANCE CHARACTERISTICS

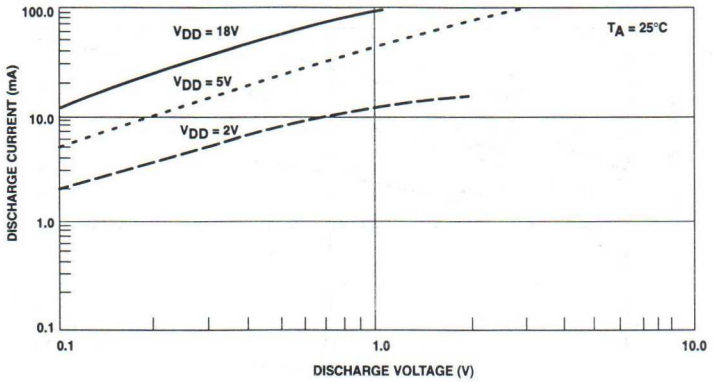


Supply Current vs Supply Voltage

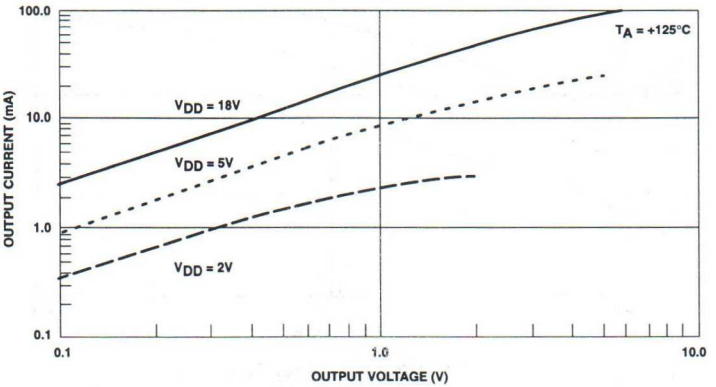


High Output Voltage Drop vs Output Source Current

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

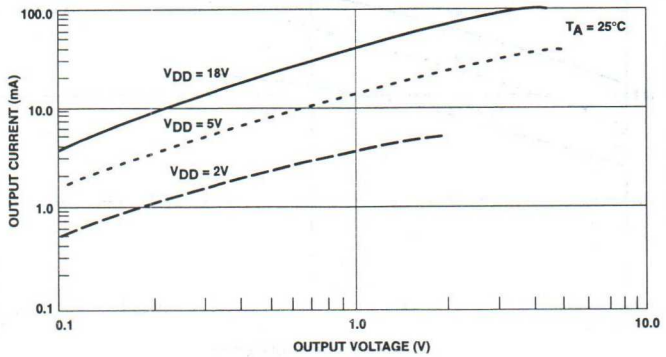


Discharge Low Output Voltage vs Discharge Sink Current

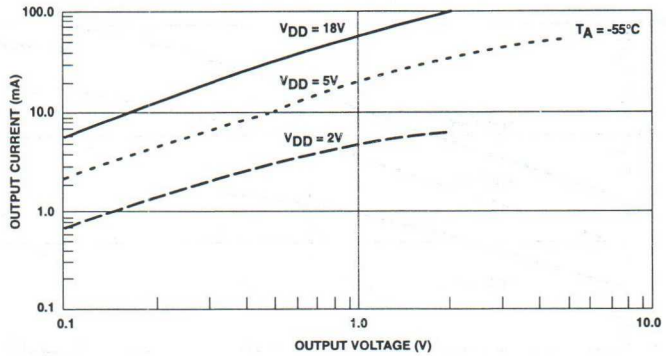


Low Output Voltage vs Output Sink Current

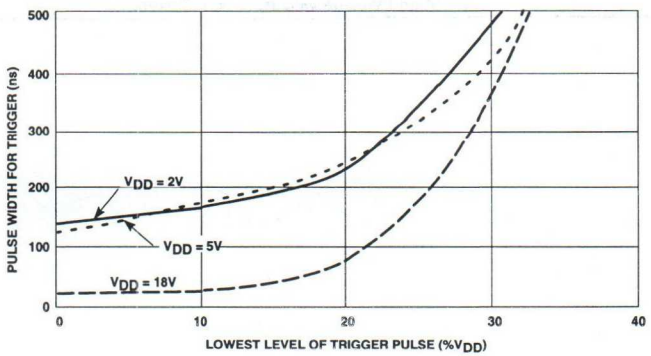
TYPICAL PERFORMANCE CHARACTERISTICS (continued)



Low Output Voltage vs Output Sink Current

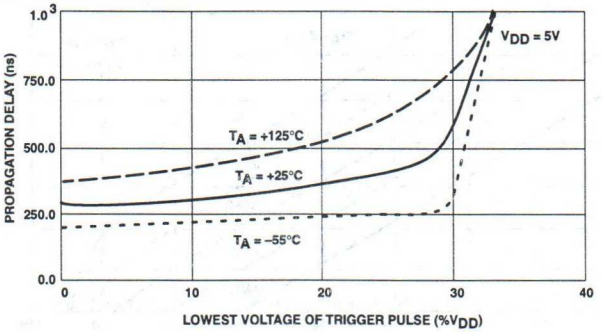


Low Output Voltage vs Output Sink Current

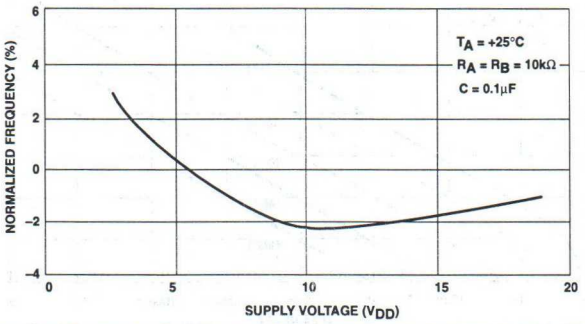


Minimum Pulse Width for Triggering

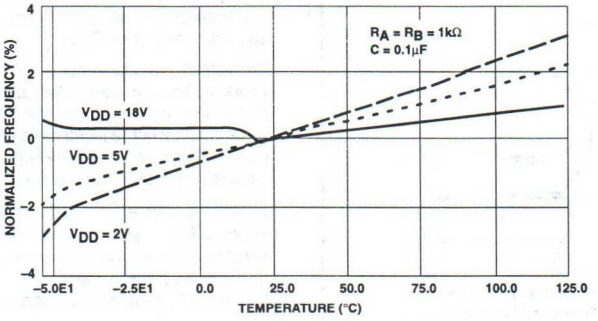
TYPICAL PERFORMANCE CHARACTERISTICS (continued)



Propagation Delay vs Voltage Level of Trigger Pulse

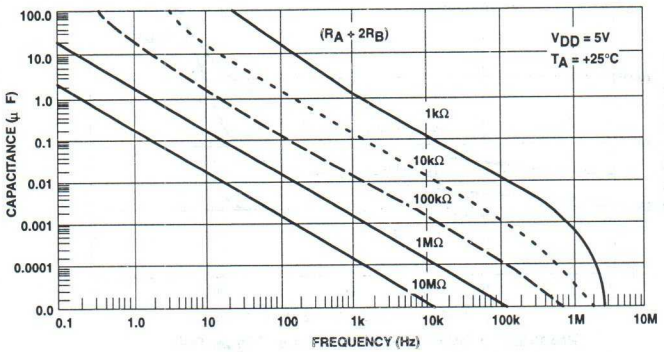


Normalized Frequency Stability as a Function of Supply Voltage (Astable Mode)

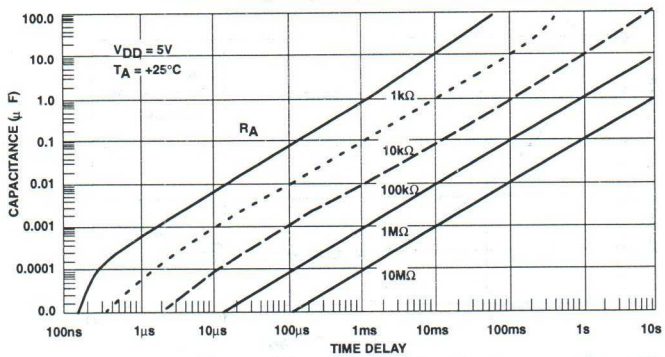


Normalized Frequency Stability as a Function of Temperature (Astable Mode)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)



Free-Running Frequency as a Function of R_A, R_B, and C



Monostable Time Delay vs R_A and C

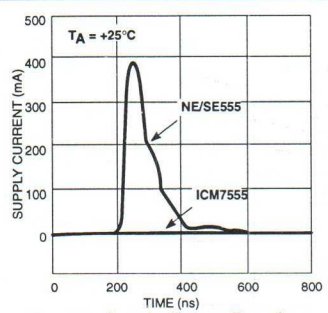


Figure 1. Supply Current Transient Compared With a Standard Bipolar 555 During an Output Transition

APPLICATION NOTES

General

The ICM7555 device is, in most instances, a direct replacement for the NE/SE555 device. However, it is possible to effect economies in the external component count using the ICM7555. Because the bipolar 555 device produces large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555 device produces no such transients. See Figure 1.

The ICM7555 produces supply current spikes of only 2-3mA instead of 300-400mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications, 2 capacitors can be saved using an ICM7555.

Power Supply Considerations

Although the supply current consumed by the ICM7555 device is very low, the total system supply can be high unless the timing components are high impedance. Therefore, high values for R and low values for C in Figures 2 and 3 are recommended.

Output Drive Capability

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5V or more, the ICM7555 will drive at least 2 standard TTL loads.

Astable Operation

If the circuit is connected as shown in Figure 2, it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus, the duty cycle (D) may be precisely set by the ratio of these two resistors. In this mode of operation, the capacitor charges and discharges between 1/3 V_{DD} and 2/3 V_{DD}. Since the charge rate and the threshold levels are directly proportional to the supply voltage, the frequency of oscillation is independent of the supply voltage.

$$F = \frac{1.38}{(R_A + 2R_B)\,C} \qquad D = \frac{R_A + R_B}{R_A + 2R_B}$$

Monostable Operation

In this mode of operation, the timer functions as a one-shot. Initially, the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative pulse to Pin 2, $\overline{\text{TRIGGER}}$, the internal flip-flop is set which releases the low impedance on DISCHARGE; the external capacitor charges and drives the OUTPUT High. The voltage across the capacitor increases exponentially with a time constant $t = R_AC$. When the voltage across the capacitor equals 2/3 V^+, the comparator resets the flip-flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. $\overline{\text{TRIGGER}}$ must return to a high state before the OUTPUT can return to a low state.

Control Voltage

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode, or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ terminal is designed to have essentially the same trip voltage as the standard bipolar 555, i.e., 0.6 to 0.7V. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{RESET}}$ function is, however, much improved over the standard bipolar 555 in that it controls only the internal flip-flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

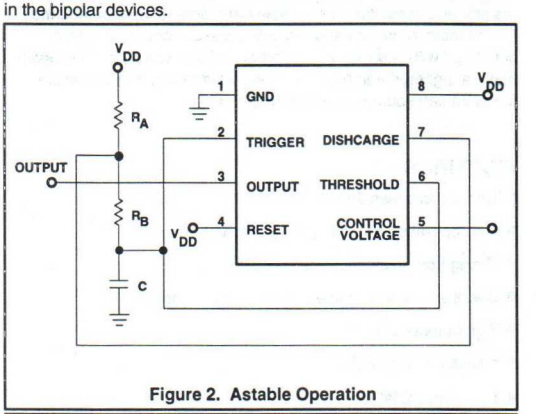


Figure 2. Astable Operation

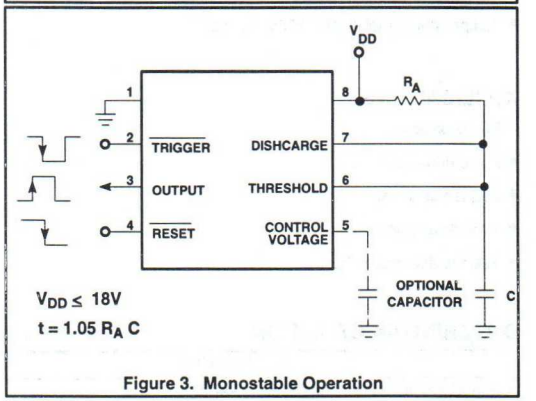


Figure 3. Monostable Operation

DESCRIPTION

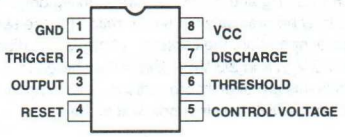
The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

FEATURES

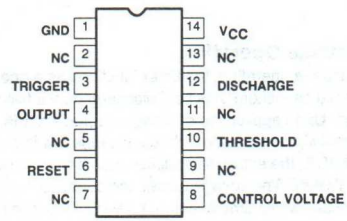
- Turn-off time less than 2μs
- Max. operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

PIN CONFIGURATIONS

D, N, FE Packages



F Package



TOP VIEW

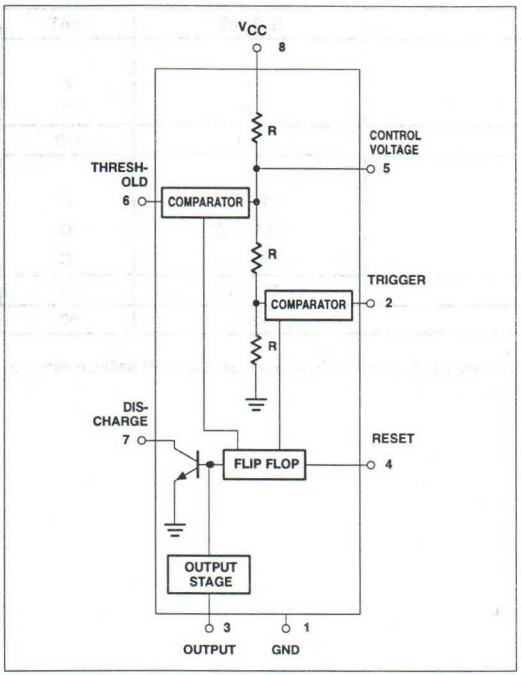
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation

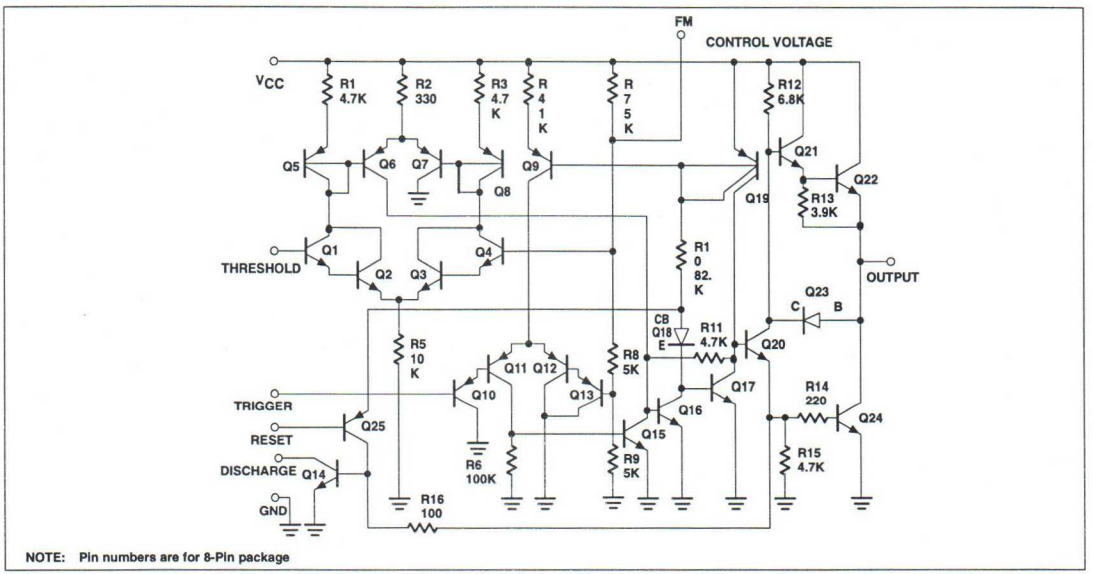
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE555D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE555N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA555N	0404B
8-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA555D	0174C
8-Pin Hermetic Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CFE	
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555CN	0404B
14-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555N	0405B
8-Pin Hermetic Cerdip	-55°C to +125°C	SE555FE	
14-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CF	0581B

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



NOTE: Pin numbers are for 8-Pin package

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	SE555	+18	V
	NE555, SE555C, SA555	+16	V
P_D	Maximum allowable power dissipation[1]	600	mW
T_A	Operating ambient temperature range		
	NE555	0 to +70	°C
	SA555	-40 to +85	°C
	SE555, SE555C	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:

1. The junction temperature must be kept below 125°C for the D package and below 150°C for the FE, N and F packages. At ambient temperatures above 25°C, where this limit would be derated by the following factors:
   D package 160°C/W
   FE package 150°C/W
   N package 100°C/W
   F package 105°C/W

DC AND AC ELECTRICAL CHARACTERISTICS

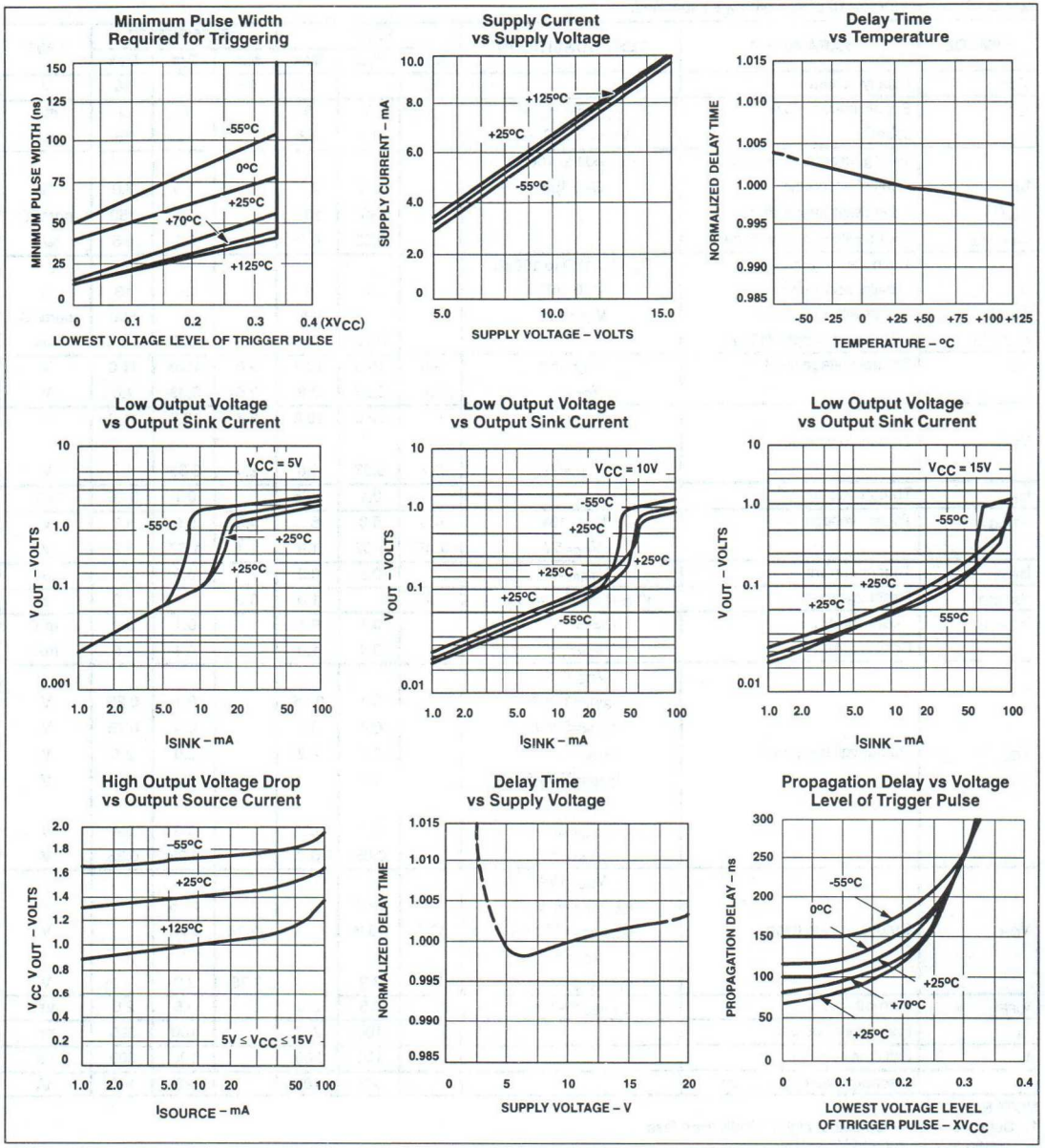
T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low state)[1]	V_{CC}=5V, R_L=∞		3	5		3	6	mA
		V_{CC}=15V, R_L=∞		10	12		10	15	mA
	Timing error (monostable)	R_A=2kΩ to 100kΩ							
t_M	Initial accuracy[2]	C=0.1μF		0.5	2.0		1.0	3.0	%
$\Delta t_M/\Delta T$	Drift with temperature			30	100		50	150	ppm/°C
$\Delta t_M/\Delta V_S$	Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
	Timing error (astable)	R_A, R_B=1kΩ to 100kΩ							
t_A	Initial accuracy[2]	C=0.1μF		4	6		5	13	%
$\Delta t_A/\Delta T$	Drift with temperature	V_{CC}=15V			500			500	ppm/°C
$\Delta t_A/\Delta V_S$	Drift with supply voltage			0.15	0.6		0.3	1	%/V
V_C	Control voltage level	V_{CC}=15V	9.6	10.0	10.4	9.0	10.0	11.0	V
		V_{CC}=5V	2.9	3.33	3.8	2.6	3.33	4.0	V
V_{TH}	Threshold voltage	V_{CC}=15V	9.4	10.0	10.6	8.8	10.0	11.2	V
		V_{CC}=5V	2.7	3.33	4.0	2.4	3.33	4.2	V
I_{TH}	Threshold current[3]			0.1	0.25		0.1	0.25	μA
V_{TRIG}	Trigger voltage	V_{CC}=15V	4.8	5.0	5.2	4.5	5.0	5.6	V
		V_{CC}=5V	1.45	1.67	1.9	1.1	1.67	2.2	V
I_{TRIG}	Trigger current	V_{TRIG}=0V		0.5	0.9		0.5	2.0	μA
V_{RESET}	Reset voltage[4]	V_{CC}=15V, V_{TH} =10.5V	0.3		1.0	0.3		1.0	V
I_{RESET}	Reset current	V_{RESET}=0.4V		0.1	0.4		0.1	0.4	mA
	Reset current	V_{RESET}=0V		0.4	1.0		0.4	1.5	mA
V_{OL}	Output voltage (low)	V_{CC}=15V							
		I_{SINK}=10mA		0.1	0.15		0.1	0.25	V
		I_{SINK}=50mA		0.4	0.5		0.4	0.75	V
		I_{SINK}=100mA		2.0	2.2		2.0	2.5	V
		I_{SINK}=200mA		2.5			2.5		V
		V_{CC}=5V							
		I_{SINK}=8mA		0.1	0.25		0.3	0.4	V
		I_{SINK}=5mA		0.05	0.2		0.25	0.35	V
V_{OH}	Output voltage (high)	V_{CC}=15V							
		I_{SOURCE}=200mA		12.5			12.5		V
		I_{SOURCE}=100mA	13.0	13.3		12.75	13.3		V
		V_{CC}=5V							
		I_{SOURCE}=100mA	3.0	3.3		2.75	3.3		V
t_{OFF}	Turn-off time[5]	V_{RESET}=V_{CC}		0.5	2.0		0.5	2.0	μs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA

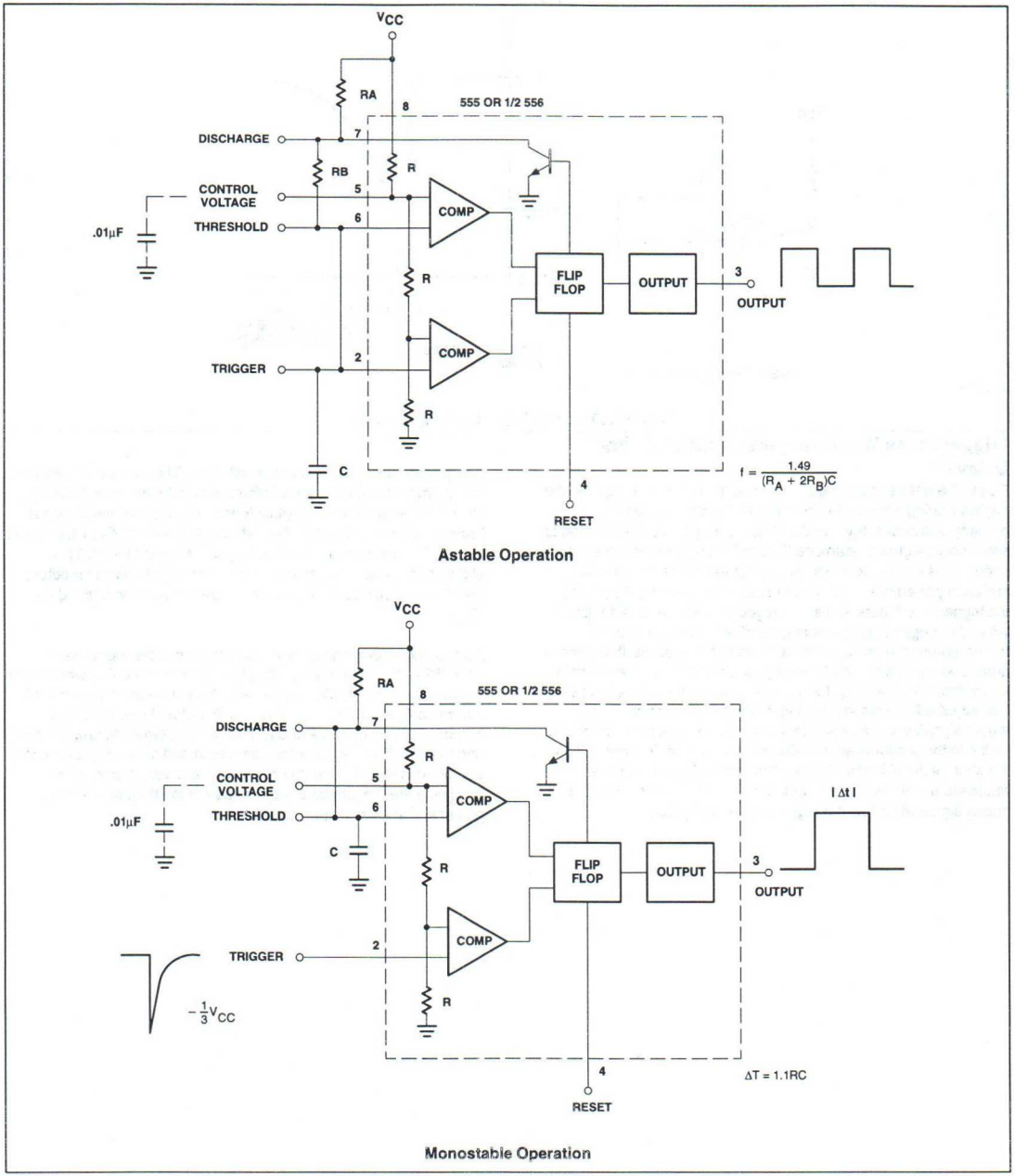
NOTES:

1. Supply current when output high typically 1mA less.
2. Tested at V_{CC}=5V and V_{CC}=15V.
3. This will determine the max value of R_A+R_B, for 15V operation, the max total R=10MΩ, and for 5V operation, the max. total R=3.4MΩ.
4. Specified with trigger input high.
5. Time measured from a positive going input pulse from 0 to 0.8×V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL APPLICATIONS



TYPICAL APPLICATIONS

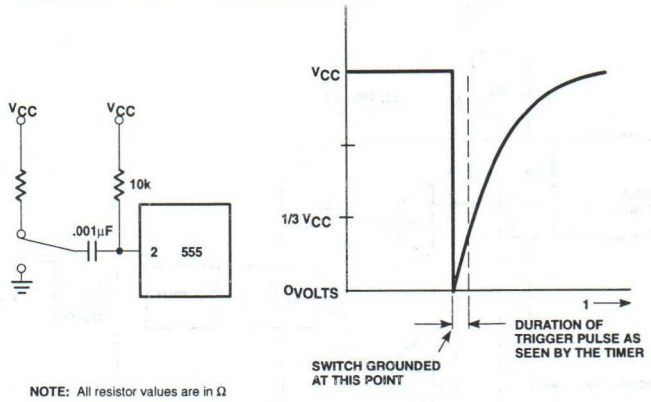


Figure 1. AC Coupling of the Trigger Pulse

Trigger Pulse Width Requirements and Time Delays

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger, see Figure 1, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bi-stable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Another consideration is the "turn-off time". This is the measurement of the amount of time required after the threshold reaches 2/3 V_{CC} to turn the output low. To explain further, Q_1 at the threshold input turns on after reaching 2/3 V_{CC}, which then turns on Q_5, which turns on Q_6. Current from Q_6 turns on Q_{16} which turns Q_{17} off. This allows current from Q_{19} to turn on Q_{20} and Q_{24} to given an output low. These steps cause the 2µs max. delay as stated in the data sheet.

Also, a delay comparable to the turn-off time is the trigger release time. When the trigger is low, Q_{10} is on and turns on Q_{11} which turns on Q_{15}. Q_{15} turns off Q_{16} and allows Q_{17} to turn on. This turns off current to Q_{20} and Q_{24}, which results in output high. When the trigger is released, Q_{10} and Q_{11} shut off, Q_{15} turns off, Q_{16} turns on and the circuit then follows the same path and time delay explained as "turn off time". This trigger release time is very important in designing the trigger pulse width so as not to interfere with the output signal as explained previously.

Dual timer

NE/SA/SE556/NE556-1

DESCRIPTION

Both the 556 and 556-1 Dual Monolithic timing circuits are highly stable controllers capable of producing accurate time delays or oscillation. The 556 and 556-1 are a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other, sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

FEATURES

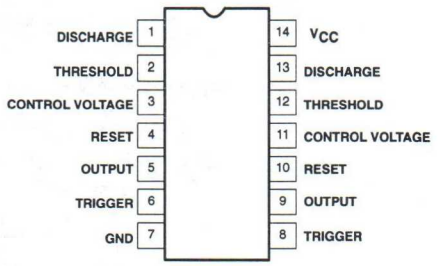
- Turn-off time less than 2µs (556-1)
- Maximum operating frequency >500kHz (556-1)
- Timing from microseconds to hours
- Replaces two 555 timers
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005%/°C
- SE556-1 compliant to MIL-STD or JAN

APPLICATIONS

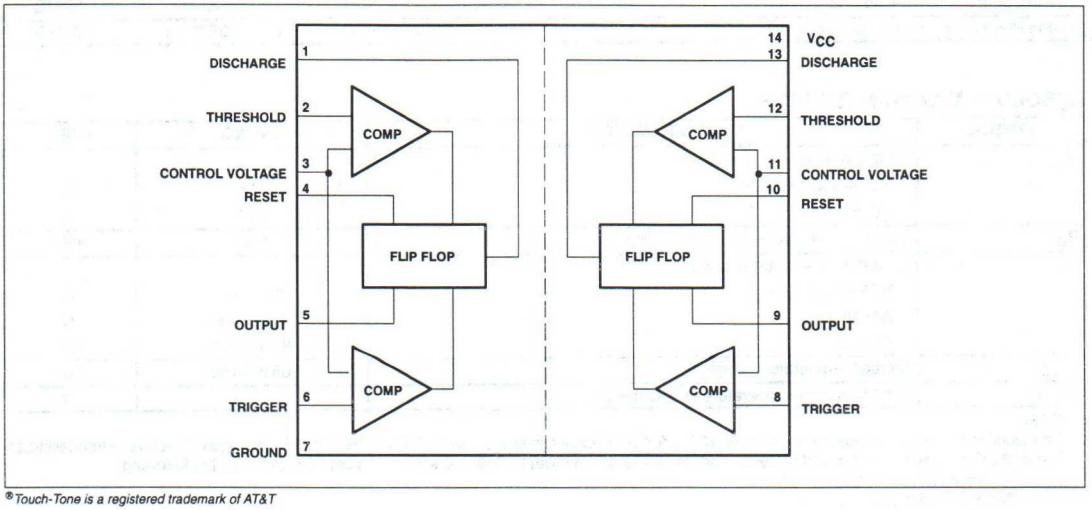
- Precision timing
- Sequential timing
- Pulse shaping
- Pulse generator
- Missing pulse detector
- Tone burst generator
- Pulse width modulation
- Time delay generator
- Frequency division
- Touch-Tone®encoder
- Industrial controls
- Pulse position modulation
- Appliance timing
- Traffic light control

PIN CONFIGURATION

D, F, N Packages

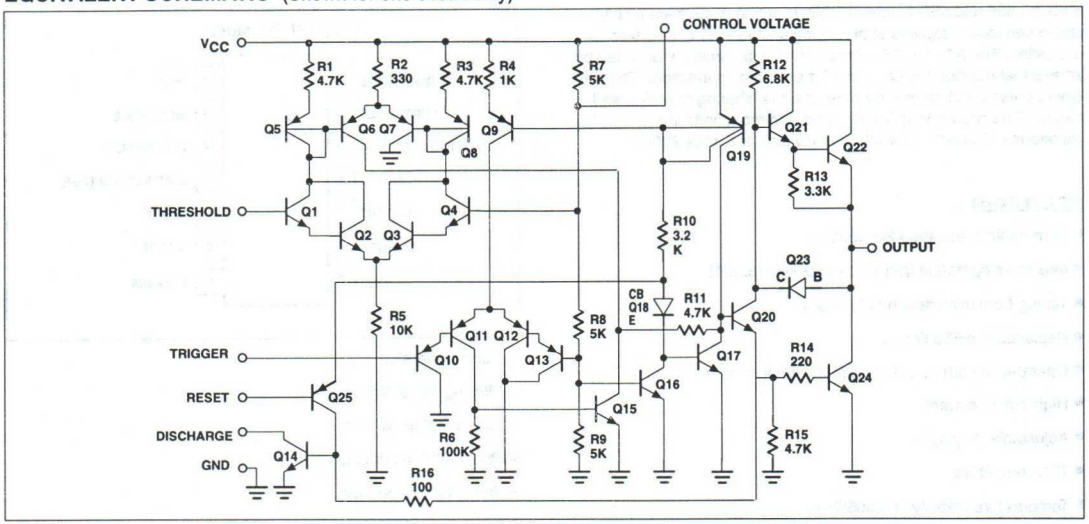


BLOCK DIAGRAM



®Touch-Tone is a registered trademark of AT&T

EQUIVALENT SCHEMATIC (Shown for one circuit only)



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE556D	0175D
14-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE556F	0581B
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE556N	0405B
14-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE556-1F	0581B
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE556-1N	0405B
14-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA556N	0405B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE556F	0581B
14-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE556N	0405B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	NE/SA556, NE556-1	+16	V
	SE556	+18	V
P_D	Maximum allowable power dissipation[1]	800	mW
T_A	Operating temperature range		
	NE556-1, NE556	0 to +70	°C
	SA556	-40 to +85	°C
	SE556	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:

1. The junction temperature must be kept below 125°C for the D package and below 150°C for the N and F packages. At ambient temperatures above 25°C, where this limit would be exceeded, the Maximum Allowable Power Dissipation must be derated by the following:
   D package 115°C/W
   N package 80°C/W
   F package 100°C/W

ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC}=+5V to +15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE556			NE/SA556 NE556-1			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low state)[1]	V_{CC}=5V, R_L=∞		6	10		6	12	mA
		V_{CC}=15V, R_L=∞		20	24		20	30	mA
	Timing error (monostable)	R_A=2kΩ to 100kΩ							
t_M	Initial accuracy[2]	C=0.1μF		0.5	2.0		0.75	3.0	%
$\Delta t_M/\Delta T$	Drift with temperature	T=1.1 RC		30	100		50	150	ppm/°C
$\Delta t_M/\Delta V_S$	Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
	Timing error (astable)	R_A, R_B=1kΩ to 100kΩ							
t_A	Initial accuracy[2]	C=0.μF		4	6		5	13	%
$\Delta t_A/\Delta T$	Drift with temperature	V_{CC}=15V		400	500		400	500	ppm/°C
$\Delta t_A/\Delta V_S$	Drift with supply voltage			0.15	0.6		0.3	1	%/V
V_C	Control voltage level	V_{CC}=15V	9.6	10.0	10.4	9.0	10.0	11.0	V
		V_{CC}=5V	2.9	3.33	3.8	2.6	3.33	4.0	
V_{TH}	Threshold voltage	V_{CC}=15V	9.4	10.0	10.6	8.8	10.0	11.2	V
		V_{CC}=5V	2.7	3.33	4.0	2.4	3.33	4.2	V
I_{TH}	Threshold current[3]	V_{CC} = 15V, V_{TH} = 10.5V		30	250		30	250	nA
V_{TRIG}	Trigger voltage	V_{CC}=15V	4.8	5.0	5.2	4.5	5.0	5.6	V
		V_{CC}=5V	1.45	1.67	1.9	1.1	1.67	2.2	V
I_{TRIG}	Trigger current	V_{TRIG}=0V		0.5	0.9		0.5	2.0	μA
V_{RESET}	Reset voltage[5]		0.4	0.7	1.0	0.4	0.7	1.0	V
	Reset current	V_{RESET}=0.4V	0.4	0.1	0.4	0.4	0.1	0.6	mA
I_{RESET}	Reset current	V_{RESET}=0V		0.4	1.0		0.4	1.5	mA
V_{OL}	Output voltage (low)	V_{CC}=15V							V
		I_{SINK}=10mA		0.1	0.15		0.1	0.25	
		I_{SINK}=50mA		0.4	0.5		0.4	0.75	
	SE556	I_{SINK}=100mA		2.0	2.25				
	NE/SA556						2.0	3.2	
	NE556-1						2.0	2.5	
	Output voltage (low)	I_{SINK}=200mA		2.5			2.5		V
		V_{CC}=5V							
		I_{SINK}=8mA		0.1	0.2		0.25	0.3	
		I_{SINK}=5mA		0.05	0.15		0.15	0.25	
V_{OH}	Output voltage (high)	V_{CC}=15V							V
		I_{SOURCE}=200mA		12.5			12.5		
		I_{SOURCE}=100mA	13.0	13.3		12.75	13.3		
		V_{CC}=5V							
		I_{SOURCE}=100mA	3.0	3.3		2.75	3.3		
t_{OFF}	Turn-off time[6] NE556-1	V_{RESET}=V_{CC}		0.5	2.0		0.5		μs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA

ELECTRICAL CHARACTERISTICS (Continued)

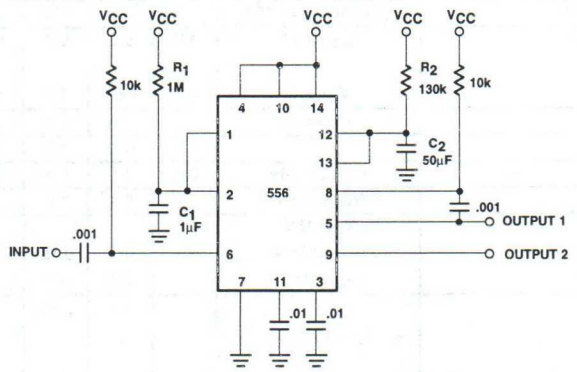
SYMBOL	PARAMETER	TEST CONDITIONS	SE556/556-1			NE/SA556/SE556C NE556-1/SE556-1C			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Matching characteristics[4]								
	Initial accuracy[2]			0.5	1.0		1.0	2.0	%
	Drift with temperature			10			±10		ppm/°C
	Drift with supply voltage			0.1	0.2		0.2	0.5	%/V

NOTES:
1. Supply current when output is high is typically 1.0mA less.
2. Tested at V_{CC}=5V and V_{CC}=15V.
3. This will determine maximum value of R_A+R_B. For 15V operation, the max total R=10MΩ, and for 5V operation, the maximum total R=3.4MΩ.
4. Matching characteristics refer to the difference between performance characteristics for each timer section in the monostable mode.
5. Specified with trigger input high. In order to guarantee reset the voltage at reset pin must be less than or equal to 0.4V. To disable reset function, the voltage at reset pin has to be greater than 1V.
6. Time measured from a positive-going input pulse from 0 to 0.4 V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL APPLICATIONS

One feature of the dual timer is that by utilizing both halves it is possible to obtain sequential timing. By connecting the output of the first half to the input of the second half via a 0.001µF coupling capacitor sequential timing may be obtained. Delay t_1 is determined by the first half and t_2 by the second half delay.

The first half of the timer is started by momentarily connecting Pin 6 to ground. When it is timed out (determined by $1.1R_1C_1$) the second half begins. Its duration is determined by $1.1R_2C_2$.

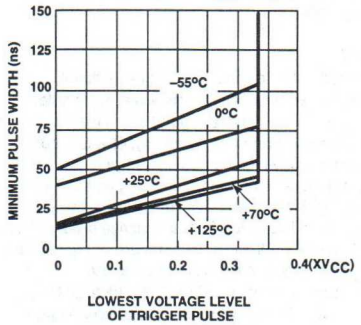


NOTE:
All resistor values are in Ω.

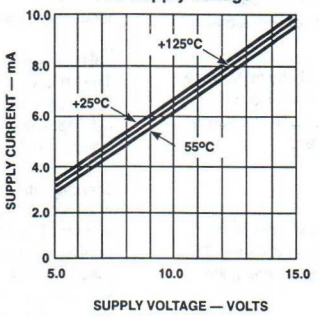
Sequential Timer

TYPICAL PERFORMANCE CHARACTERISTICS

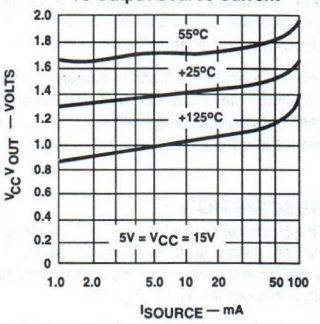
Minimum Pulse Width Required for Triggering



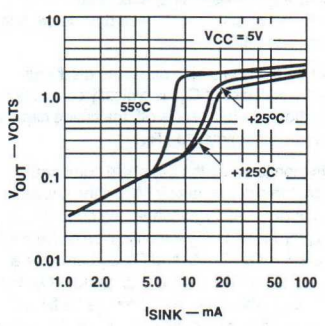
Supply Current VS Supply Voltage



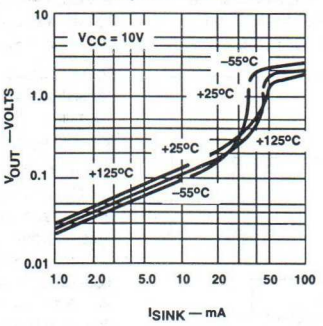
High Output Voltage Drop vs Output Source Current



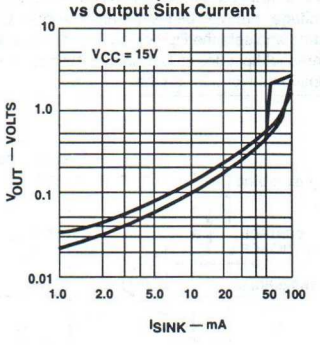
Low Output Voltage vs Output Sink Current



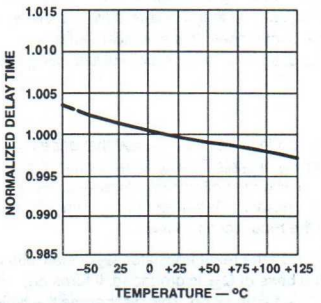
Low Output Voltage vs Output Sink Current



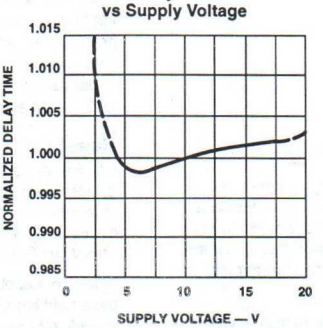
Low Output Voltae vs Output Sink Current



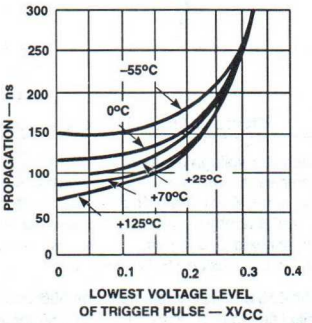
Delay Time vs Temperature



Delay Time vs Supply Voltage



Propagation Delay vs Voltage Level of Trigger Pulse



NE555 and NE556 applications

AN170

INTRODUCTION

In mid 1972, Philips Semiconductors introduced the 555 timer, a unique functional building block that has enjoyed unprecedented popularity. The timer's success can be attributed to several inherent characteristics foremost of which are versatility, stability and low cost. There can be no doubt that the 555 timer has altered the course of the electronics industry with an impact not unlike that of the IC operational amplifier.

The simplicity of the timer, in conjunction with its ability to produce long time delays in a variety of applications, has lured many designers from mechanical timers, op amps, and various discrete circuits into the ever increasing ranks of timer users.

DESCRIPTION

The 555 timer consists of two voltage comparators, a bistable flip-flop, a discharge transistor, and a resistor divider network. To understand the basic concept of the timer let's first examine the timer in block form as in Figure 1.

The resistive divider network is used to set the comparator levels. Since all three resistors are of equal value, the threshold comparator is referenced internally at 2/3 of supply voltage level and the trigger comparator is referenced at 1/3 of supply voltage. The outputs of the comparators are tied to the bistable flip-flop. When the trigger voltage is moved below 1/3 of the supply, the comparator changes state and sets the flip-flop driving the output to a high state. The threshold pin normally monitors the capacitor voltage of the RC timing network. When the

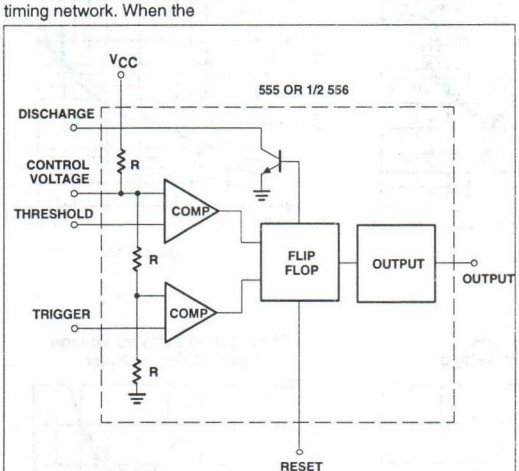


Figure 1. 555/556 Timer Functional Block Diagram

capacitor voltage exceeds 2/3 of the supply, the threshold comparator resets the flip-flop which in turn drives the output to a low state. When the output is in a low state, the discharge transistor is "on", thereby discharging the external timing capacitor. Once the capacitor is discharged, the timer will await another trigger pulse, the timing cycle having been completed.

The 555 and its complement, the 556 Dual Timer, exhibit a typical initial timing accuracy of 1% with a 50ppm/C timing drift with temperature. To operate the timer as a one-shot, only two external components are necessary; resistance & capacitance. For an oscillator, only one additional resistor is necessary. By proper selection of external components, oscillating frequencies from one cycle per half hour to 500kHz can be realized. Duty cycles can be adjusted from less than one percent to 99 percent over the frequency spectrum. Voltage control of timing and oscillation functions is also available.

Timer Circuitry

The timer is comprised of five distinct circuits: two voltage comparators; a resistive voltage divider reference; a bistable flip-flop; a discharge transistor; and an output stage that is the "totem-pole" design for sink or source capability. Q_{10}-Q_{13} comprise a Darlington differential pair which serves as a trigger comparator. Starting with a positive voltage on the trigger, Q_{10} and Q_{11} turn on when the voltage at Pin 2 is moved below one third of the supply voltage. The voltage level is derived from a resistive divider chain consisting of R_7, R_8 and R_9. All three resistors are of equal value (5kΩ). At 15V supply, the triggering level would be 5V.
When Q_{10} and Q_{11} turn on, they provide a base drive for Q_{15}, turning it on. Q_{16} and Q_{17} form a bistable flip-flop. When Q_{15} is saturated, Q_{16} is "off' and Q_{17} is saturated. Q_{16} and Q_{17} will remain in these states even if the trigger is removed and Q_{15} is turned "off'. While Q_{17} is saturated, Q_{20} and Q_{14} are turned off.

The output structure of the timer is a "totem-pole" design, with Q_{22} and Q_{24} being large geometry transistors capable of providing 200mA with a 15V supply. While Q_{20} is "off', base drive is provided for Q_{22} by Q_{21}, thus providing a high output.

For the duration that the output is in a high state, the discharge transistor is "off'. Since the collector of Q_{14} is typically connected to the external timing capacitor, C, while Q_{14} is off, the timing capacitor now can charge through the timing resistor, R_A.

The capacitor voltage is monitored by the threshold comparator (Q_1-Q_4) which is a Darlington differential pair. When the capacitor voltage reaches two thirds of the supply voltage, the current is directed from Q_3 and Q_4 thru Q_1 and Q_2. Amplification of the current change is provided by Q_5 and Q_6. Q_5-Q_6 and Q_7-Q_8 comprise a diode-biased amplifier. The amplified current change from Q_6 now provides a base drive for Q_{16} which is part of the bistable flip-flop, to change states. In doing so, the output is driven "low", and Q_{14}, the discharge transistor, is turned "on", shorting the timing capacitor to ground.

The discussion to this point has only encompassed the most fundamental of the timer's operating modes and circuitry. Several points of the circuit are brought out to the real world which allow the timer to function in a variety of modes. It is essential that one understands all the variations possible in order to utilize this device to its fullest extent.

Reset Function

Regressing to the trigger mode, it should be noted that once the device has triggered and the bistable flip-flop is set, continued triggering will not interfere with the timing cycle. However, there may come a time when it is necessary to interrupt or halt a timing cycle. This is the function that the reset accomplishes.

In the normal operating mode the reset transistor, Q_{25}, is off with its base held high. When the base of Q_{25} is grounded, it turns on, providing base drive to Q_{14}, turning it on. This discharges the timing capacitor, resets the flip-flop at Q_{17}, and drives the output low. The reset overrides all other functions within the timer.

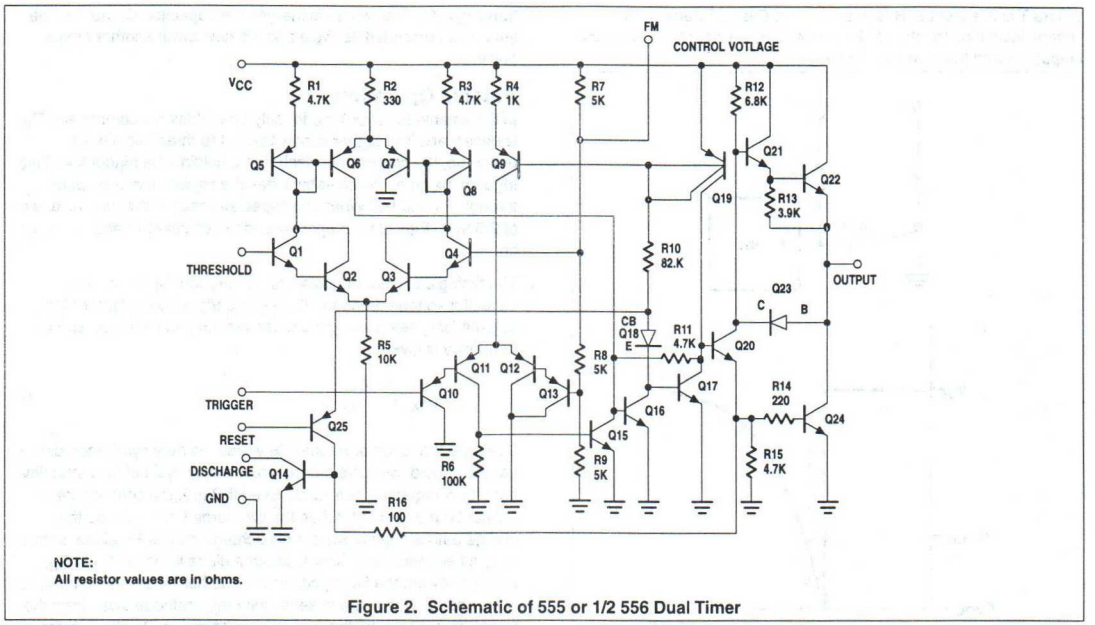


Figure 2. Schematic of 555 or 1/2 556 Dual Timer

Trigger Requirements

Due to the nature of the trigger circuitry, the timer will trigger on the negative-going edge of the input pulse. For the device to time-out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the timeout period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger (see Figure 3), a short negative-going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bistable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Control Voltage

One additional point of significance, the control voltage, is brought out on the timer. As mentioned earlier, both the trigger comparator, Q_{10}-Q_{13}, and the threshold comparator, Q_1-Q_4, are referenced to an internal resistor divider network, R_7, R_8, R_9. This network establishes the nominal two thirds of supply voltage (V_{CC}) trip point for the threshold comparator and one third of V_{CC} for the trigger comparator. The two thirds point at the junction of R_7, R_8 and the base of Q_4 is brought out. By imposing a voltage at this point, the comparator reference levels may be shifted either higher or lower than the nominal levels of one third and two thirds of the supply voltage. Varying the voltage at this point will vary the timing. This feature of the timer opens a multitude of application possibilities such as using the timer as a voltage-controlled oscillator, pulse-width modulator, etc. For applications where the control voltage function is not used, it is strongly recommended that a bypass capacitor (0.01µF) be placed across the control voltage pin and ground. This will increase the noise immunity of the timer to high frequency trash which may monitor the threshold levels causing timing error.

Monostable Operation

The timer lends itself to three basic operating modes:

1. Monostable (one-shot)
2. Astable (oscillatory)
3. Time delay

By utilizing one or any combination of basic operating modes and suitable variations, it is possible to utilize the timer in a myriad of applications. The applications are limited only to the imagination of the designer.

One of the simplest and most widely used operating modes of the timer is the monostable (one-shot). This configuration requires only two external components for operation (see Figure 4). The sequence of events starts when a voltage below one third V_{CC} is sensed by the trigger comparator. The trigger is normally applied in the form of a short negative-going pulse. On the negative-going edge of the pulse, the device triggers, the output goes high and the discharge transistor turns off. Note that prior to the input pulse, the discharge transistor is on, shorting the timing capacitor to ground. At this point the timing capacitor, C, starts charging through the timing resistor, R. The voltage on the capacitor increases exponentially with a time constant T=RC. Ignoring capacitor leakage, the capacitor will reach the two thirds V_{CC} level in 1.1 time constants or

$$T = 1.1\ RC \qquad (1)$$

Where T is in seconds, R is in ohms, and C is in Farads. This voltage level trips the threshold comparator, which in turn drives the output low and turns on the discharge

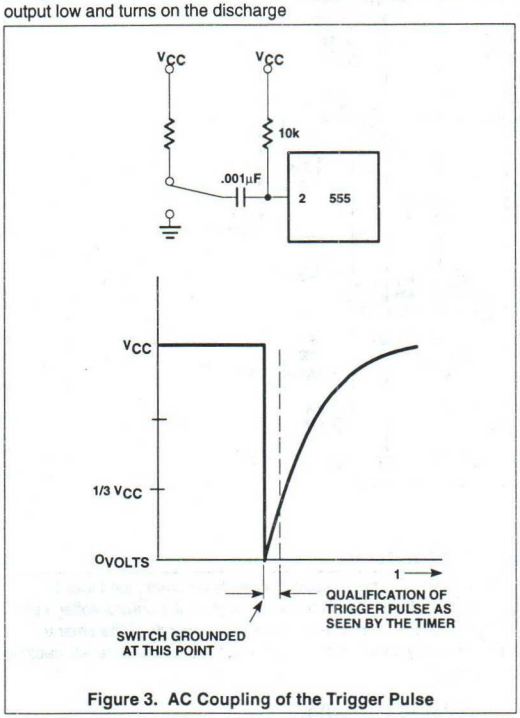


Figure 3. AC Coupling of the Trigger Pulse

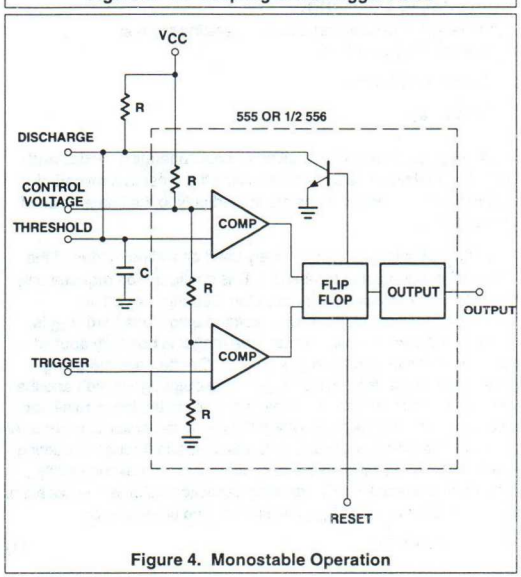


Figure 4. Monostable Operation

transistor. The transistor discharges the capacitor, C, rapidly. The timer has completed its cycle and will now await another trigger pulse.

Astable Operation

In the astable (free-run) mode, only one additional component, R_B, is necessary. The trigger is now tied to the threshold pin. At power-up, the capacitor is discharged, holding the trigger low. This triggers the timer, which establishes the capacitor charge path through R_A and R_B. When the capacitor reaches the threshold level of 2/3 V_{CC}, the output drops low and the discharge transistor turns on.

The timing capacitor now discharges through R_B. When the capacitor voltage drops to 1/3 V_{CC}, the trigger comparator trips, automatically retriggering the timer, creating an oscillator whose frequency is given by:

$$f = \frac{1.49}{(R_A + 2R_B)\,C} \qquad (2)$$

Selecting the ratios of R_A and R_B varies the duty cycle accordingly. Lo and behold, we have a problem. If a duty cycle of less than fifty percent is required, then what? Even if R_A=0, the charge time cannot be made smaller than the discharge time because the charge path is R_A+R_B while the discharge path is R_B alone. In this case it becomes necessary to insert a diode in parallel with R_B, cathode toward the timing capacitor. Another diode is desirable, but not mandatory (this one in series with R_B), cathode away from the timing capacitor. Now the charge path becomes R_A, through the parallel diode into C. Discharge is through the series diode and R_B to the discharge transistor. This scheme will afford a duty cycle range from less than 5% to greater than 95%. It should be noted that for reliable operation a minimum value of 3kΩ for R_B is recommended to assure that oscillation begins.

Time Delay

In this third basic operating mode, we aim to accomplish something a little different from monostable operation. In the monostable mode, when a trigger was applied, immediately changed to the high state, timed out, and returned to its pre-trigger low state. In the time delay mode, we require the output not to change state upon triggering, but at some precalculated time after trigger is received.

The threshold and trigger are tied together, monitoring the capacitor voltage. The

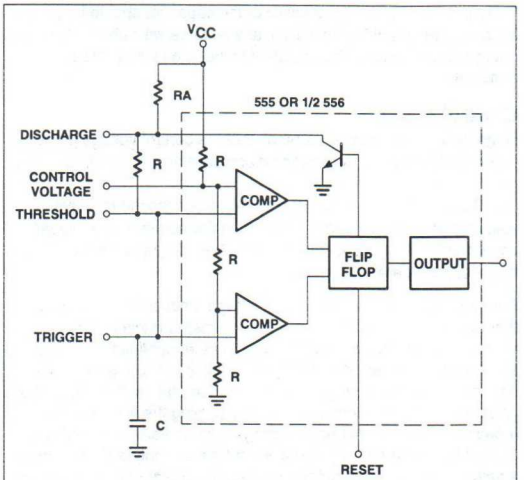


Figure 5. Astable Operation

discharge function is not used. The operation sequence begins as transistor (T_1) is turned on, keeping the capacitor grounded. The trigger sees a low state and forces the timer output high. When the transistor is turned off, the capacitor commences its charge cycle. When the capacitor reaches the threshold level, only then does the output change from its normally high state to the low state. The output will remain low until T_1 is again turned on.

GENERAL DESIGN CONSIDERATIONS

The timer will operate over a guaranteed voltage range of 4.5V to $15V_{DC}$ with $16V_{DC}$ being the absolute maximum rating. Most of the devices, however, will operate at voltage levels as low as $3V_{DC}$. The timing interval is independent of supply voltage since the charge rate and threshold level of the comparator are both directly proportional to supply. The supply voltage may be provided by any number of sources, however, several precautions should be taken. The most important, the one which provides the most headaches if not practiced, is good power supply filtering and adequate bypassing. Ripple on the supply line can cause loss of timing accuracy. The threshold level shifts, causing a change of charging current. This will cause a timing error for that cycle.

Due to the nature of the output structure, a high power totem-pole design, the output of the timer can exhibit large current spikes on the supply line. Bypassing is necessary to eliminate this phenomenon. A capacitor across the V_{CC} and ground, directly across the device, is necessary and ideal. The size of a capacitor will depend on the specific application. Values of capacitance from 0.01µF to 10µF are not uncommon, but note that the bypass capacitor would be as close to the device as physically possible.

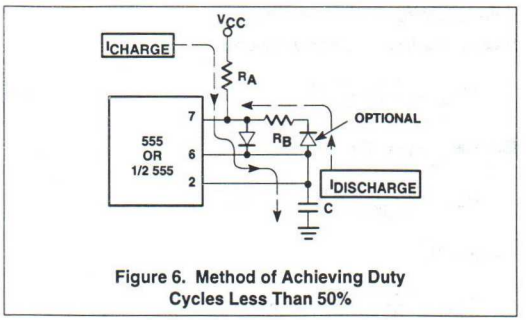


Figure 6. Method of Achieving Duty Cycles Less Than 50%

Selecting External Components

In selecting the timing resistor and capacitor, there are several considerations to be taken into account.

Stable external components are necessary for the RC network if good timing accuracy is to be maintained. The timing resistor(s) should be of the metal film variety if timing accuracy and repeatability are important design criteria. The timer exhibits a typical initial accuracy of one percent. That is, with any one RC network, from timer to timer only one percent change is to be expected. Most of the initial timing error (i.e., deviation from the formula) is due to inaccuracies of external components. Resistors range from their rated values by 0.01% to 10% and 20%. Capacitors may have a 5% to 10% deviation from rated capacity. Therefore, in a system where timing is critical, an adjustable timing resistor or precision components are necessary. For best results, a good quality trim pot, placed in series with the largest feasible resistance, will allow for best adjustability and performance.

The timing capacitor should be a high quality, stable component with very low leakage characteristics. Under no circumstances should ceramic disc capacitors be used in the timing network! Ceramic disc capacitors are not sufficiently stable in capacitance to operate properly in an RC mode. Several acceptable capacitor types are: silver mica, mylar, polycarbonate, polystyrene, tantalum, or similar types.

The timer typically exhibits a small negative temperature coefficient (50ppm/°C). If timer accuracy over temperature is a consideration, timing components with a small positive temperature coefficient should be chosen. This combination will tend to cancel timing drift due to temperature.

In selecting the values for the timing resistors and capacitor, several points should be considered. A minimum value of threshold current is necessary to trip the threshold comparator. This value is 0.25µA. To calculate the maximum value of resistance, keep in mind that at the time the threshold current is required, the voltage potential on the threshold pin is two thirds of supply. Therefore:

$$V_{potential} = V_{CC} - V_{Capacitor}$$

$V_{potential} = V_{CC} - 2/3V_{CC} = 1/3V_{CC}$

Maximum resistance is then defined as

$$R_{MAX} = \frac{V_{CC} - V_{CAP}}{I_{THRESH}} \quad (3)$$

Example: $V_{CC} = 15V$

$$R_{MAX} = \frac{15 - 10}{0.25(10^{-6})} = 20M\Omega$$

$V_{CC} = 5V$

$$R_{MAX} = \frac{5 - 3.33}{0.25(10^{-6})} = 6.6M\Omega$$

NOTE:

If using a large value of timing resistor, be certain that the capacitor leakage is significantly lower than the charging current available to minimize timing error.

On the other end of the spectrum, there are certain minimum values of resistance that should be observed. The discharge transistor, Q_{14}, is current-limited at 35mA to 55mA internally. Thus, at the current limiting values, Q_{14} establishes high saturation voltages. When examining the currents at Q_{14}, remember that the transistor, when turned on, will be carrying two current loads. The first being the constant current through timing resistor, R_A. The second will be the varying discharge current from the timing capacitor. To provide best operation, the current contributed by the R_A path should be minimized so that the majority of discharge current can be used to reset the capacitor voltage. Hence it is recommended that a 5kΩ value be the minimum feasible value for R_A. This does not mean lower values cannot be used successfully in certain applications, yet there are extreme cases that should be avoided if at all possible.

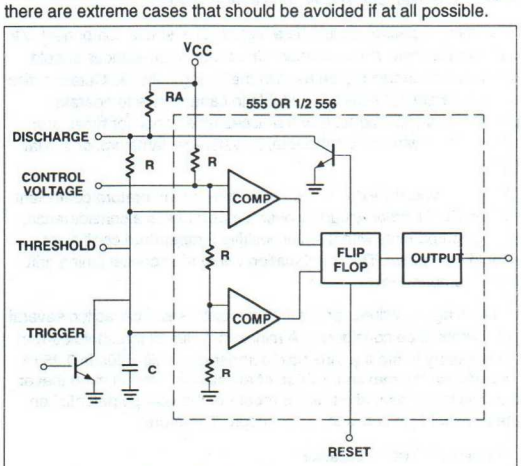


Figure 7. Time Delay Operation

Capacitor size has not proven to be a legitimate design criteria. Values ranging from picofarads to greater than one thousand microfarads have been used successfully. One precaution need be utilized, though. (It should be a cardinal rule that applies to the usage of all ICs.) Make certain that the package power dissipation is not exceeded. With extremely large capacitor values, a maximum duty cycle which allows some cooling time for the discharge transistor may be necessary.

The most important characteristic of the capacitor should be as low a leakage as possible. Obviously, any leakage will subtract from the charge count, causing the calculated time to be longer than anticipated.

Control Voltage

Regressing momentarily, we recall that the control voltage pin is connected directly to the threshold comparator at the junction of R_7, or
R_8. The combination of R_7, R_8 and R_9 comprises the resistive voltage divider network that establishes the nominal V_{CC} trigger comparator level (junction R_8, R_9) and the V_{CC} level for the threshold comparator (junction R_7, R_8).

For most applications, the control voltage function is not used and therefore is bypassed to ground with a small capacitor for noise filtering. The control voltage function, in other applications, becomes an integral part of the design. By imposing a voltage at this pin, it becomes possible to vary the threshold comparator "set" level above or below the 2/3 V_{CC} nominal, thereby varying the timing. In the monostable mode, the control voltage may be varied from 45% to 90% of V_{CC}. The 45-90% figure is not firm, but only an indication to a safe usage. Control voltage levels below and above those stated have been used successfully in some applications.

In the oscillatory (free-run) mode, the control voltage limitations are from 1.7V to V_{CC}. These values should be heeded for reliable operation. Keep in mind that in this mode the trigger level is also important. When the control voltage raises the threshold comparator level, it also raise the trigger comparator level by one-half that amount due to R_8 and R_9 of Figure 2. As a voltage-controlled oscillator, one can expect ±25% around center frequency (f_O) to be virtually linear with a normal RC timing circuit. For wider linear variations around f_O it may be desirable to replace the charging resistor with a constant-current source. In this manner, the exponential charging characteristics of the classical configuration will be altered to linear charge time.

Reset Control

The only remaining function now is the reset. As mentioned earlier, the reset, when taken to ground, inhibits all device functioning. The output is driven low, the bistable flip-flop is reset, and the timing capacitor is discharged. In the astable (oscillatory) mode, the reset can be used to gate the oscillator. In the monostable, it can be used as a timing abort to either interrupt a timing sequence or establish a standby mode (i.e., device off during power-up). It can also be used in conjunction with the trigger pin to establish a positive edge-triggered circuit as opposed to the normal negative edge-trigger mode. One thing to keep in mind when using the reset function is that the reset voltage (switching) point is between 0.4V and 1.0V (min/max). Therefore, if used in conjunction with the trigger, the device will be out of the reset mode prior to reaching 1V. At that point the trigger is in the "turn on" region, below 1/3 V_{CC}. This will cause the device to trigger immediately, effectively triggering on the positive-going edge if a pulse is applied to Pins 4 and 2 simultaneously.

FREQUENTLY ASKED APPLICATIONS QUESTIONS

The following is a harvest of various maladies, exceptions, and idiosyncrasies that may exhibit themselves from time to time in various applications. Rather than cast aspersions, a quick review of this list may uncover a solution to the problem at hand.

1. In the oscillator mode when reset is released the first time constant is approximately twice as long as the rest. Why?
   Answer: In the oscillator mode the capacitor voltage fluctuates between 1/2 and 2/3 of the supply voltage. When reset is pulled down, the capacitor discharges completely. Thus for the first cycle it must charge from ground to 2/3 V_{CC}, which takes twice as long.
2. What is maximum frequency of oscillations?
   Answer: Most devices will oscillate about 1MHz. However, in the interest of temperature stability, one should operate only up to about 500kHz.
3. What is temperature drift for oscillator mode?
   Answer: Temperature drift of oscillator mode is 3 times that of one-shot mode due to the addition of a second voltage comparator. Frequency always increases with an increasing temperature. Therefore it is possible to partially offset this drift with an offsetting temperature coefficient in the external resistor/capacitor combination.
4. Oscillator exhibits spurious oscillations on crossover points. Why?
   Answer: The 555 can oscillate due to feedback from power supply. Always bypass with sufficient capacitance close to the device for all applications.
5. Trying to drive a relay but 555 hangs up. How come?
   Answer: Inductive feedback. A clamp diode across the coil prevents the coil from driving Pin 3 below a negative 0.6V. This negative voltage is sufficient in some cases to cause the timer to malfunction. The solution is to drive the relay through a diode, thus preventing Pin 3 from ever seeing a negative voltage.
6. Double triggering of the TTL loads sometimes occurs. Why?
   Answer: Due to the high current capability and fast rise and fall times of the output, a totem-pole structure different from the TTL classical structure was used. Near TTL threshold this output exhibits a crossover distortion which may double trigger logic. A 1000pF capacitor from the output to ground will eliminate any false triggering.
7. What is the longest time I can get out of the timer?
   Answer: Times exceeding an hour are possible, but not always practical. Large capacitors with low leakage specs are quite expensive. It becomes cheaper to use a countdown scheme (see Figure 15) at some point, dependent on required accuracy. Normally 20 to 30 min. is the longest feasible time.

DESIGN FORMULAS

Before entering the section on specific applications it is advantageous to review the timing formulas. The formulas given here apply to the 555 and 556 devices.

APPLICATIONS

The timer, since introduction, has spurred the imagination of thousands. Thus, the ways in which this device has been used are far too numerous to present each one. A review of the basic operation and basic modes has previously been given. Presented here are some ingenious applications devised by our applications engineers and by some of our customers.

Missing Pulse Detector

Using the circuit of Figure 10a, the timing cycle is continuously reset by the input pulse train. A change in frequency, or a missing pulse, allows completion of the timing cycle which causes a change in the output level. For this application, the time delay should be set to be slightly longer than the normal time between pulses. Figure 10b shows the actual waveforms seen in this mode of operation.

Figure 11b shows the waveforms of the timer in Figure 11a when used as a divide-by-three circuit. This application makes use of the fact that this circuit cannot be retriggered during the timing cycle.

Pulse Width Modulation (PWM)

In this application, the timer is connected in the monostable mode as shown in Figure 12a. The circuit is triggered with a continuous pulse train and the threshold voltage is modulated by the signal applied to the control voltage terminal (Pin 5). This has the effect of modulating the pulse width as the control voltage varies. Figure 12b shows the actual waveform generated with this circuit.

Pulse Position Modulation (PPM)

This application uses the timer connected for astable (free-running) operation, Figure 13a, with a modulating signal again applied to the control voltage terminal. Now the pulse position varies with the modulating signal, since the threshold voltage, and hence the time delay, is varied. Figure 13b shows the waveform generated for triangle-wave modulation signal.

Tone Burst Generator

The 556 Dual Timer makes an excellent tone burst generator. The first half is connected as a one-shot and the second half as an oscillator (Figure 14).

The pulse established by the one-shot turns on the oscillator, allowing a burst to be generated.

Sequential Timing

One feature of the dual timer is that by utilizing both halves it is possible to obtain sequential timing. By connecting the output of the first half to the input of the second half via a 0.001µF coupling capacitor, sequential timing may be obtained. Delay t_1 is determined by the first half and t_2 by the second half delay (Figure 15).

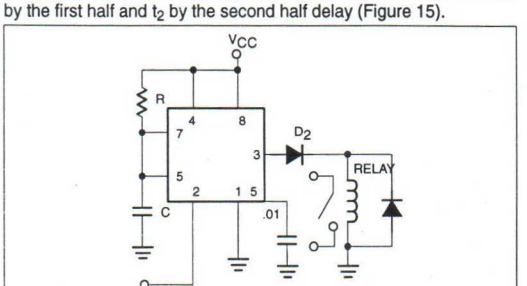


Figure 8. Driving High Q Inductive Loads

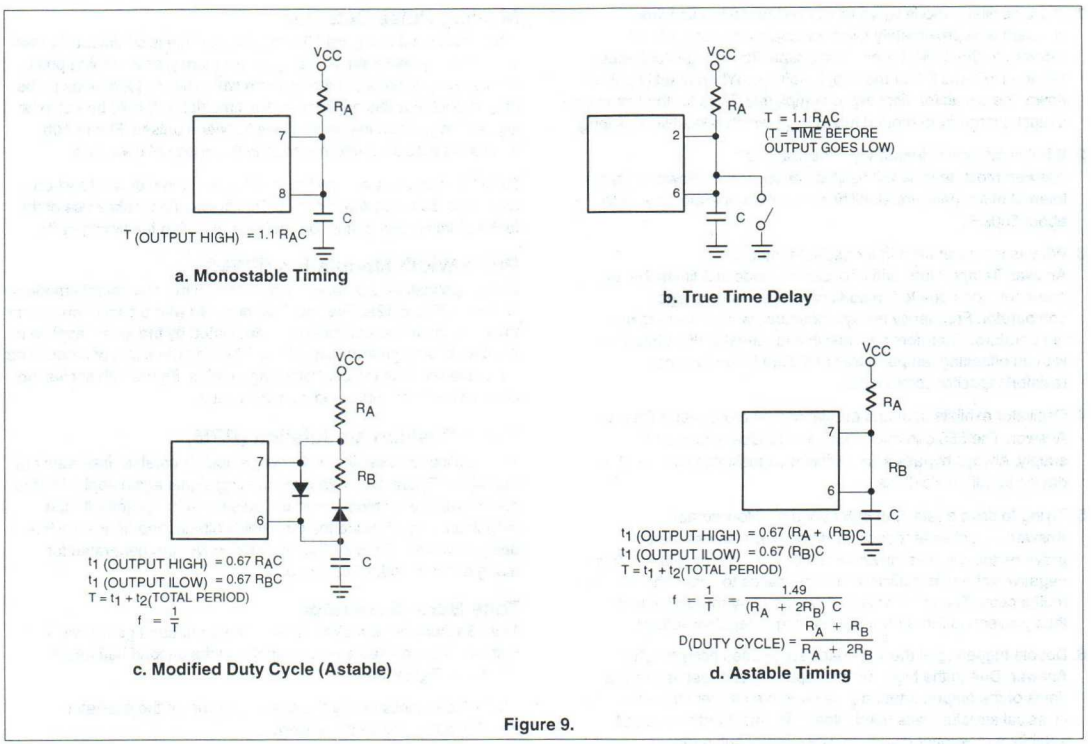

VCC
RA
7
8
C
T (OUTPUT HIGH) = 1.1 RAC
a. Monostable Timing
VCC
RA
2
6
C
T = 1.1 RAC
(T = TIME BEFORE
OUTPUT GOES LOW)
b. True Time Delay
VCC
RA
7
6
RB
C
t1 (OUTPUT HIGH) = 0.67 RAC
t1 (OUTPUT ILOW) = 0.67 RBC
T = t1 + t2(TOTAL PERIOD)
f = 1/T
c. Modified Duty Cycle (Astable)
VCC
RA
7
6
RB
C
t1 (OUTPUT HIGH) = 0.67 (RA + (RB)C
t1 (OUTPUT ILOW) = 0.67 (RB)C
T = t1 + t2(TOTAL PERIOD)
f = 1/T = 1.49 / (RA + 2RB) C
D(DUTY CYCLE) = (RA + RB) / (RA + 2RB)
d. Astable Timing

Figure 9.

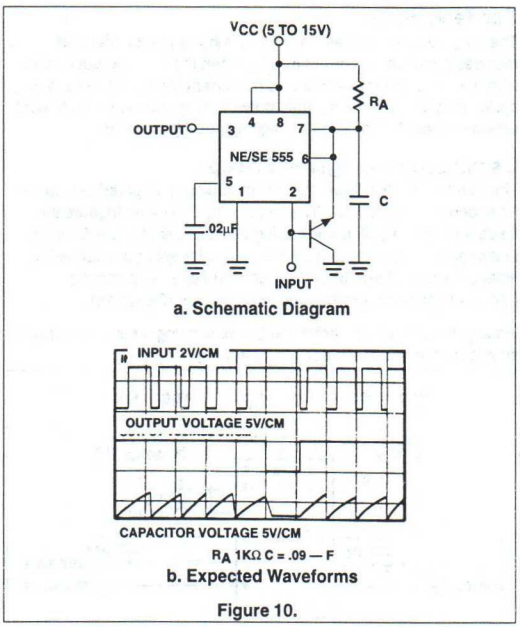


Figure 10.

The first half of the timer is started by momentarily connecting Pin 6 to ground. When it is timed-out (determined by 1.1 R_1C_1) the second half begins. Its duration is determined by 1.1 R_2C_2.

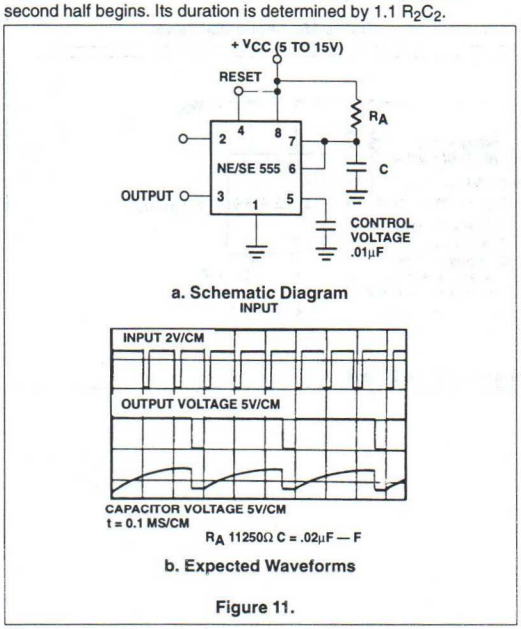


Figure 11.

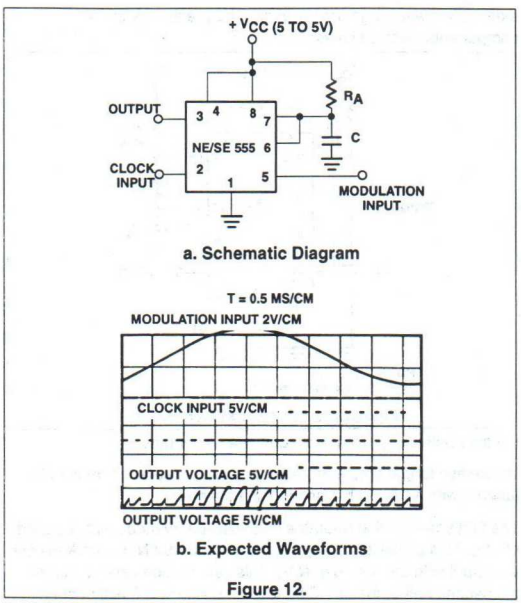


Figure 12.

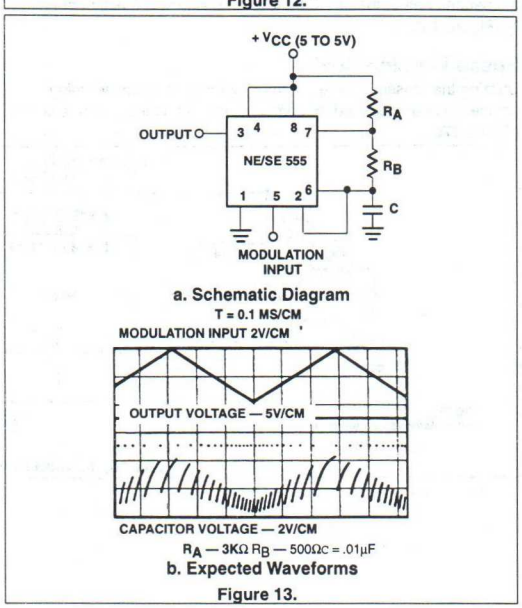


Figure 13.

Long Time Delays

In the 556 timer the timing is a function of the charging rate of the external capacitor. For long time delays, expensive capacitors with

extremely low leakage are required. The practicality of the components involved limits

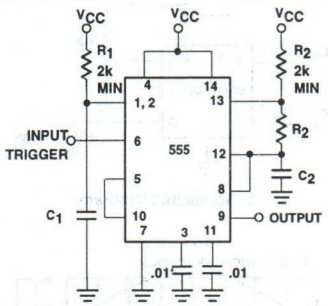


Figure 14. Tone Burst Generator

the time between pulses to around twenty minutes.

To achieve longer time periods, both halves may be connected in tandem with a "divide-by" network in between.

The first timer section operates in an oscillatory mode with a period of $1/f_O$. This signal is then applied to a "divide-by-N" network to give an output with the period of N/f_O. This can then be used to trigger the second half of the 556. The total time is now a function of N and f_O (Figure 16).

Speed Warning Device

Utilizing the "missing pulse detector" concept, a speed warning device, such as depicted, becomes a simple and inexpensive circuit (Figure 17a).

Car Tachometer

The timer receives pulses from the distributor points. Meter M receives a calibrated current thru R_6 when the timer output is high. After time-out, the meter receives no current for that part of the duty cycle. Integration of the variable duty cycle by the meter movement provides a visible indication of engine speed (Figure 18).

Oscilloscope-Triggered Sweep

The 555 timer holds down the cost of adding a triggered sweep to an economy oscilloscope. The circuit's input op amp triggers the timer, setting its flip-flop and cutting off its discharge transistor so that capacitor C can charge. When capacitor voltage reaches the timer's control voltage ($0.33V_{CC}$), the flip-flop resets and the transistor conducts, discharging the capacitor (Figure 19).

Greater linearity can be achieved by substituting a constant-current source for the frequency adjust resistor (R).

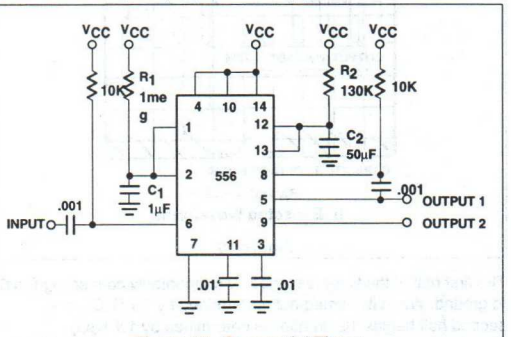


Figure 15. Sequential Timer

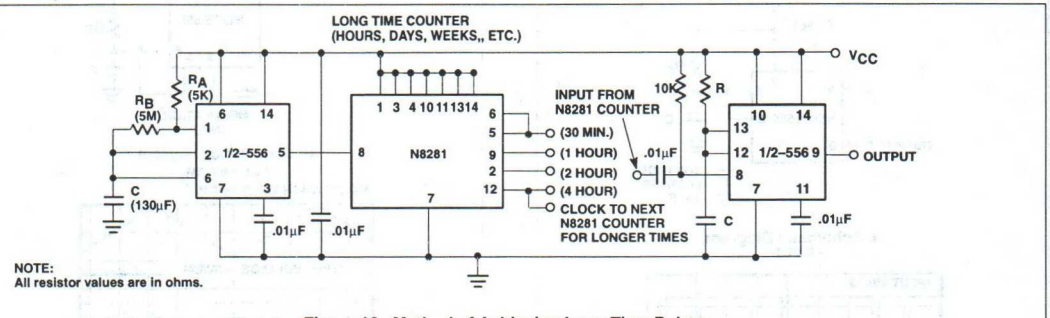
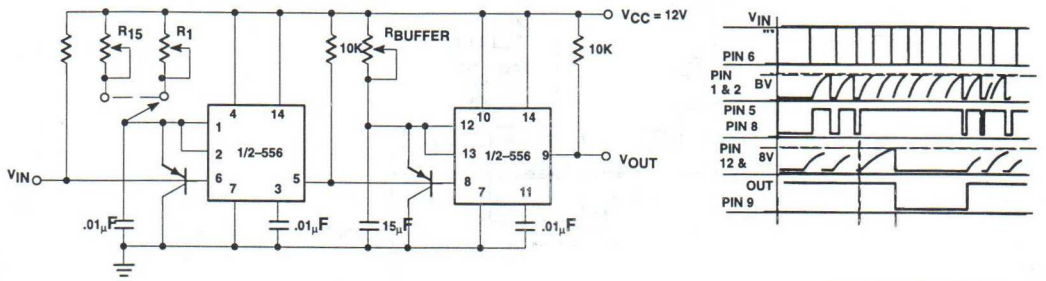


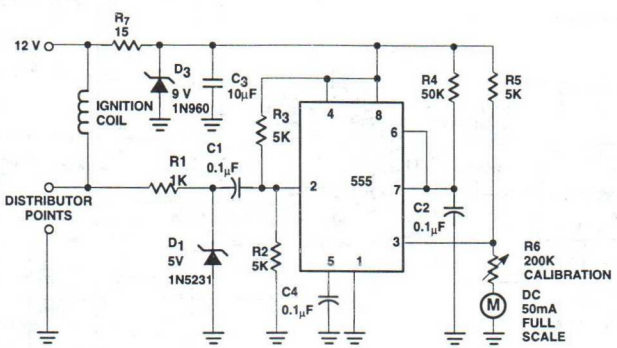
Figure 16. Method of Achieving Long Time Delays



a. Schematic of Speed Warning Device

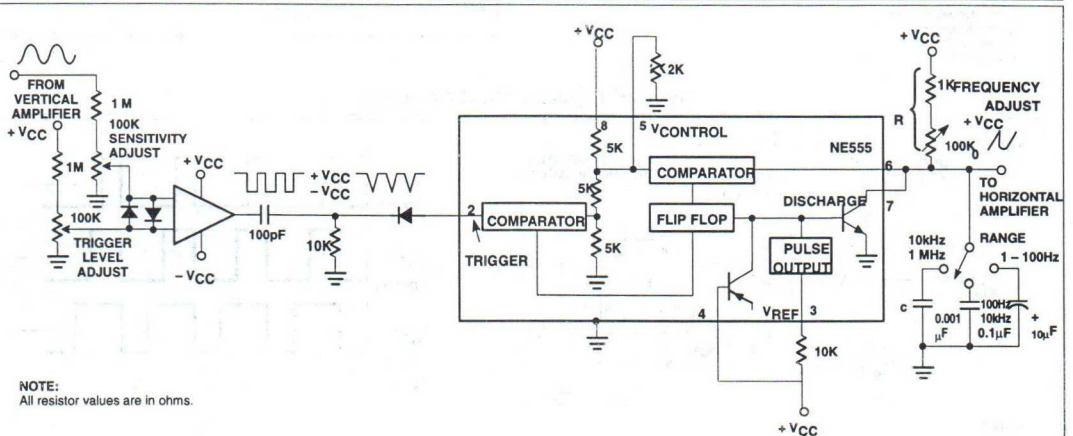
b. Operating Waveforms Speed Warning Device

Figure 17.



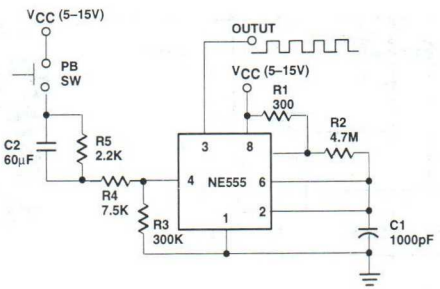
NOTE:
All resistor values are in ohms.

Figure 18. Tachometer



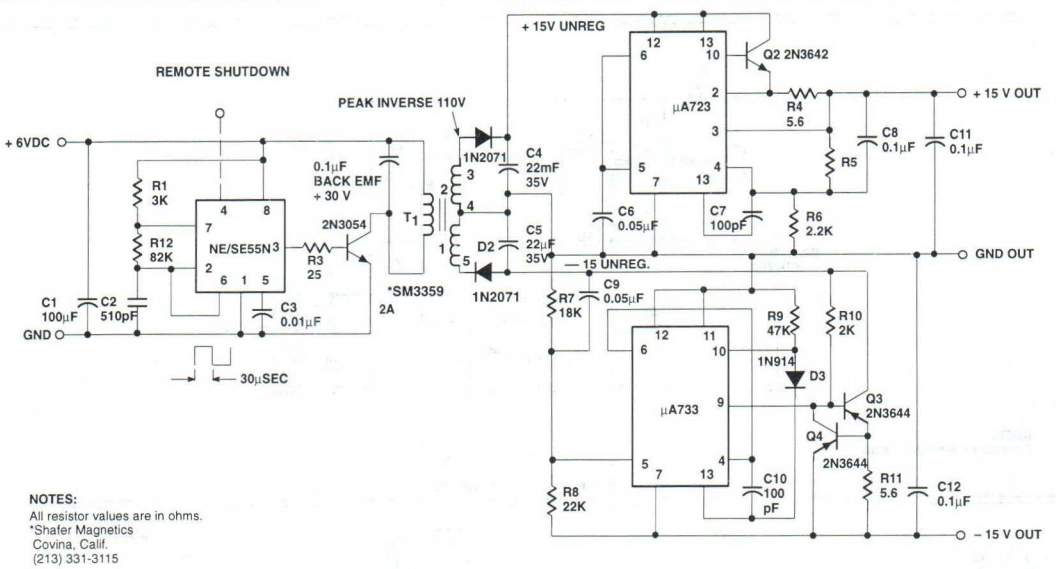
NOTE:
All resistor values are in ohms.

Figure 19. Schematic of Triggered Sweep



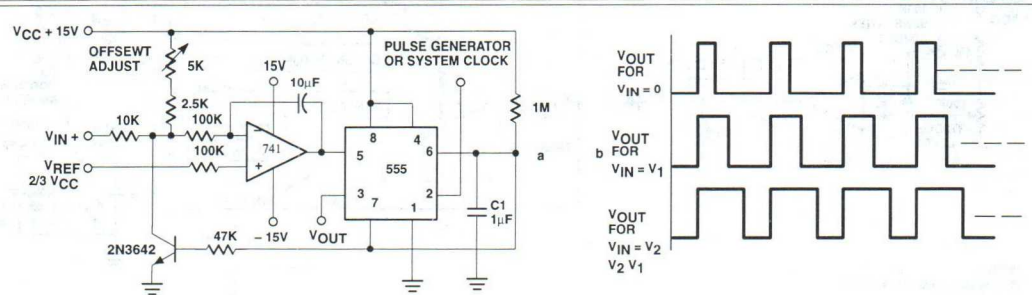
NOTE:
All resistor values are in ohms.

Figure 20. Square Wave Tone Burst Generator



NOTES:
All resistor values are in ohms.
*Shafer Magnetics
Covina, Calif.
(213) 331-3115

Figure 21. Regulated DC-to-DC Converter



NOTES:
All resistor values in ohms.
*V_{IN} is limited to 2 diode drops within ground or below V_{CC}.

Figure 22. Voltage-to-Pulse Duration Converter

Square Wave Tone Burst Generator

Depressing the pushbutton provides square wave tone bursts whose duration depends on the duration for which the voltage at Pin 4 exceeds a threshold. Components R_1, R_2 and C_1 cause the astable action of the timer IC (Figure 20).

Regulated DC-to-DC Converter

Regulated DC-to-DC converter produces $15V_{DC}$ outputs from a $+5V_{DC}$ input. Line and load regulation is 0.1% (Figure 21).

Voltage-to-Pulse Duration Converter

Voltage levels can be converted to pulse durations by combining an op amp and a timer IC. Accuracies to better than 1% can be obtained with this circuit (a), and the output signals (b) still retain the original frequency, independent of the input voltage (Figure 22).

Servo System Controller

To control a servo motor remotely, the 555 needs only six extra components (Figure 23).

Stimulus Isolator

Stimulus isolator uses a photo-SCR and a toroid for shaping pulses of up to 200V at 200μA (Figure 24).

Voltage-to-Frequency Converter (0.2% Accuracy)

Linear voltage-to-frequency converter (a) achieves good linearity over the 0 to -10V range. Its mirror image (b) provides the same linearity over the 0 to +10V range, but is not DTL/TTL compatible (Figure 25).

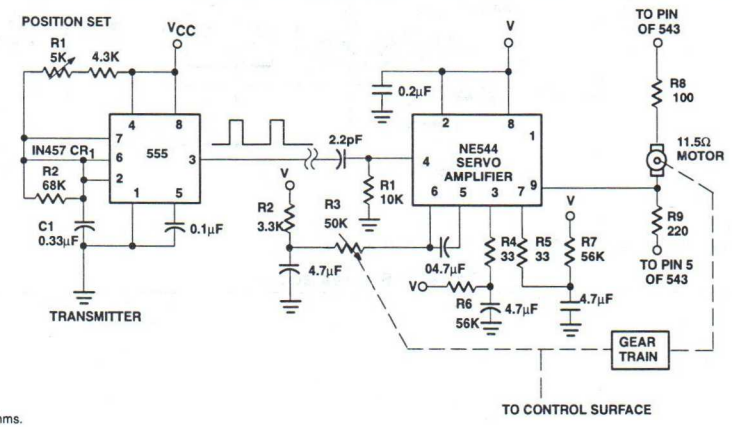
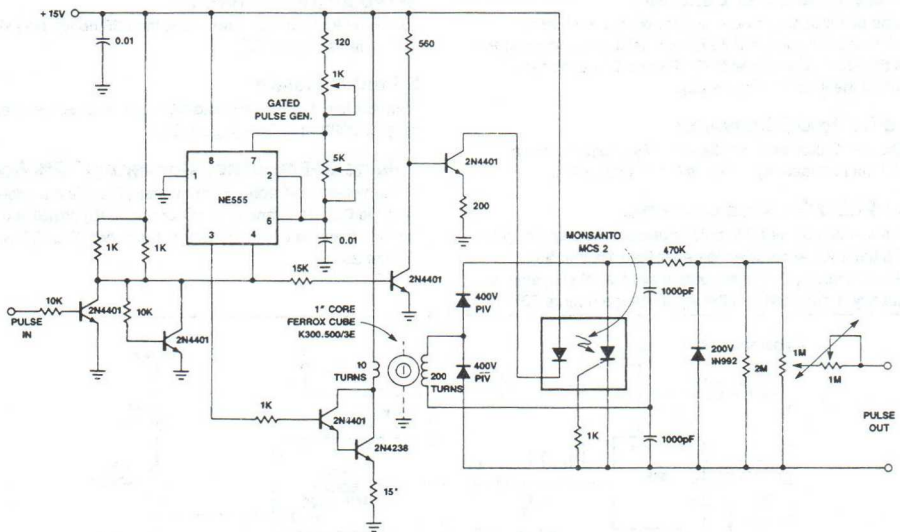
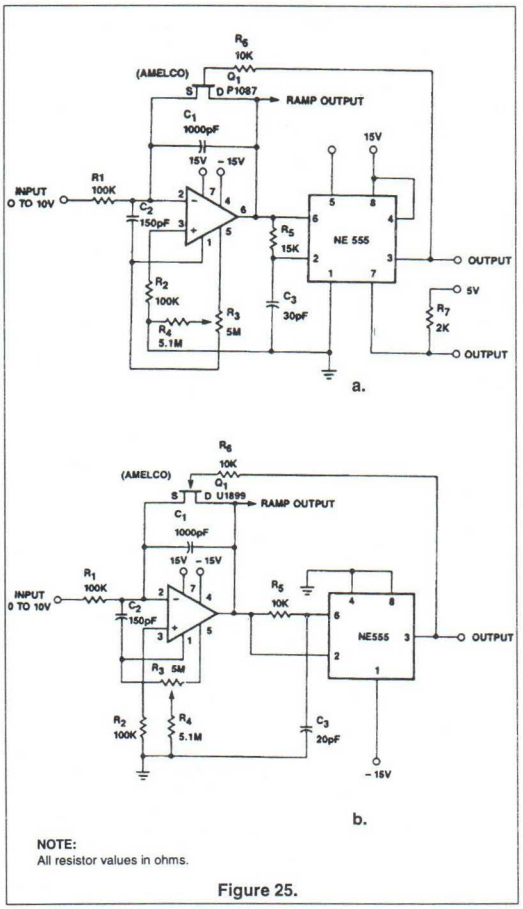


Figure 23. Servo System Controller



NOTE:
All resistor values in ohms.
*Power rating depends on duty cycle from 1/2W for 20-25% duty cycle to 15-20W for 75-90% duty cycle.

Figure 24. Stimulus Isolator



NOTE:
All resistor values in ohms.

Figure 25.

Positive-to-Negative Converter

Transformerless DC-DC converter derives a negative supply voltage from a positive. As a bonus, the circuit also generates a clock signal.

The negative output voltage tracks the DC input voltage linearity (a), but its magnitude is about 3V lower. Application of a 500Ω load, (b), causes 10% change from the no-load value (Figure 26).

Auto Burglar Alarm

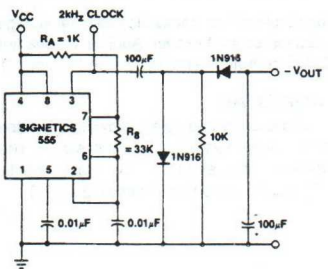
Timer A produces a safeguard delay, allowing driver to disarm alarm and eliminating a vulnerable outside control switch. The SCR prevents timer A from triggering timer B, unless timer B is triggered by strategically-located sensor switches (Figure 27).

Cable Tester

Compact tester checks cables for open-circuit or short-circuit conditions. A differential transistor pair at one end of each cable line remains balanced as long as the same clock pulse-generated by the timer IC appears at both ends of the line. A clock pulse just at the clock end of the line lights a green light-emitting diode, and a clock pulse only at the other end lights a red LED (Figure 28).

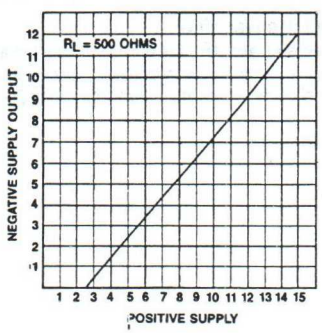
Low Cost Line Receiver

The timer makes an excellent line receiver for control applications involving relatively slow electromechanical devices. It can work without special drivers over single unshielded lines (Figure 29).

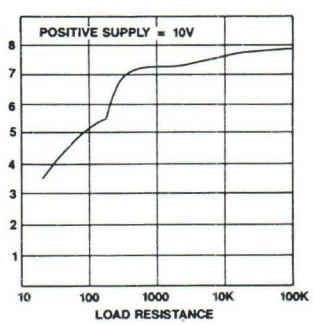


NOTE:
All resistor values in ohms.

a. Positive-to-Negative Converter

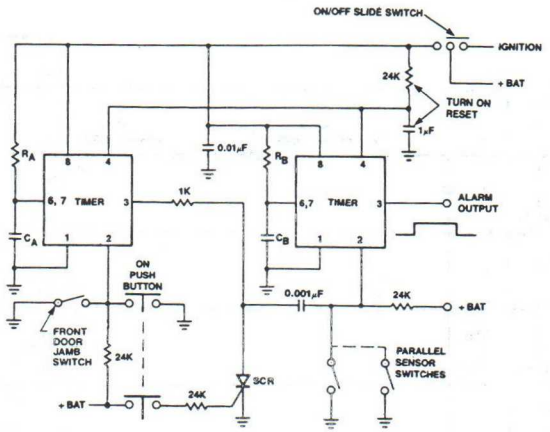


b.



c.

Figure 26.



NOTES:
Timer Philips Semiconductors NE555
All resistor values in ohms.

Figure 27. Auto Burglar Alarm

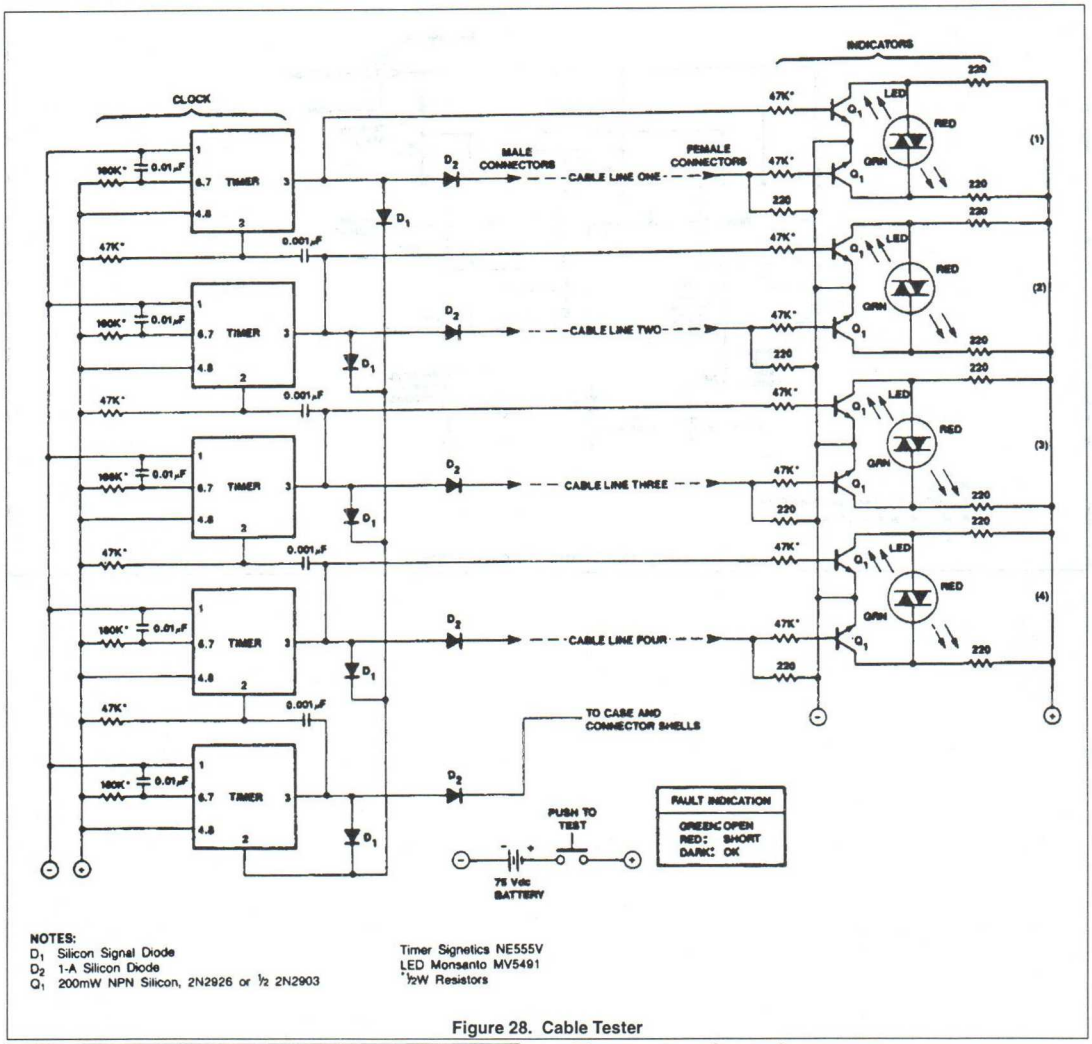


Figure 28. Cable Tester

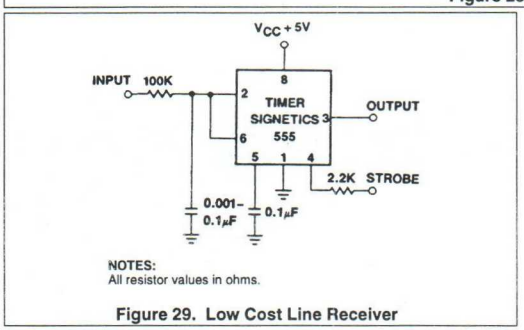


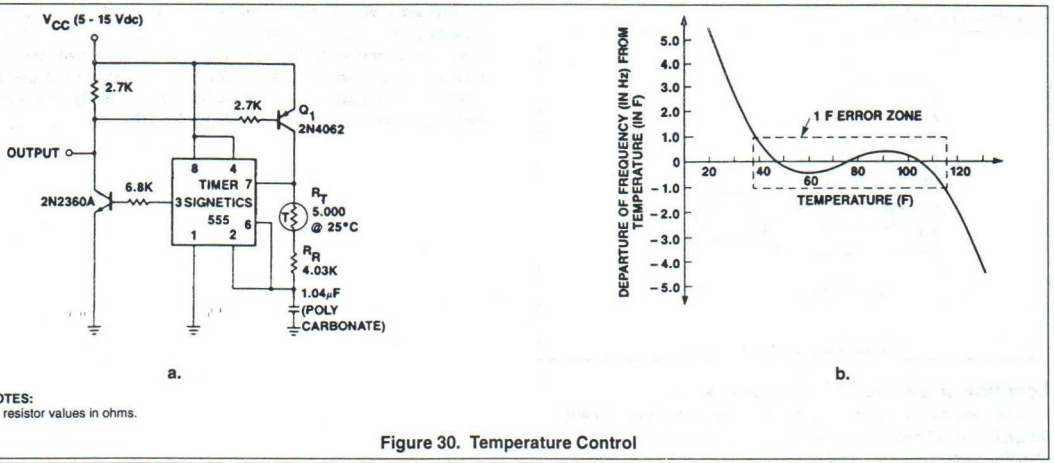
Figure 29. Low Cost Line Receiver

Temperature Control

A couple of transistors and thermistor in the charging network of the 555-type timer enable this device to sense temperature and produce a corresponding frequency output. The circuit is accurate to within ±1Hz over a 78°F temperature range (Figure 30).

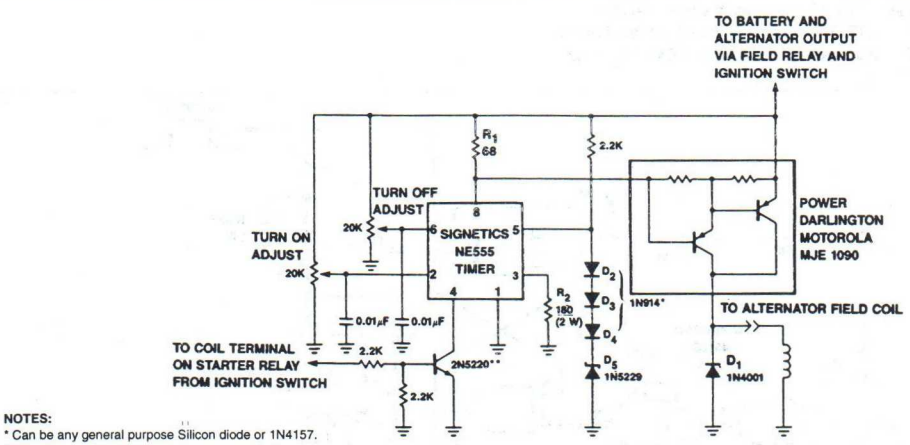
Automobile Voltage Regulator

A monolithic 555-type timer is the heart of this simple automobile voltage regulator. When the timer is off so that its output (Pin 3) is low, the power Darlington transistor pair is off. If battery voltage becomes too low (less than 14.4V in this case), the timer turns on and the Darlington pair conducts (Figure 31).



NOTES:
All resistor values in ohms.

Figure 30. Temperature Control



NOTES:
* Can be any general purpose Silicon diode or 1N4157.
** Can be any general purpose Silicon transistor.
All resistor values are in ohms.

Figure 31. Automobile Voltage Regulator

DC-to-DC Converter

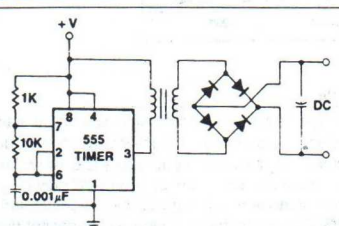


Figure 32. DC-to-DC Converter

Ramp Generator

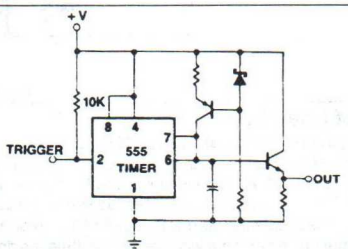


Figure 33. Ramp Generator

Ramp Generator

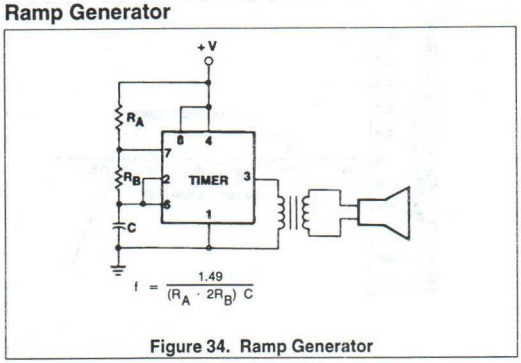


Figure 34. Ramp Generator

Low Power Monostable Operation

In battery-operated equipment where load current is a significant factor, Figure 35 can deliver 555 monostable operation at low standby power. This circuit interfaces directly with CMOS 4000 series and 74L00 series. During the monostable time, the current drawn is 4.5mA for T=1.1RC. The rest of the time the current drawn is less than 50μA. (Circuit submitted by Karl Imhof, Executone Inc., Long Island City, NY.)

In other low power operations of the timer where V_{CC} is removed until timing is needed, it is necessary to consider the output load. If the output is driving the base of a PNP transistor, for example, and its power is not removed, it will sink current into Pin 3 to ground and use excessive power. Therefore, when driving these types of loads, one should recall this internal sinking path of the timer.

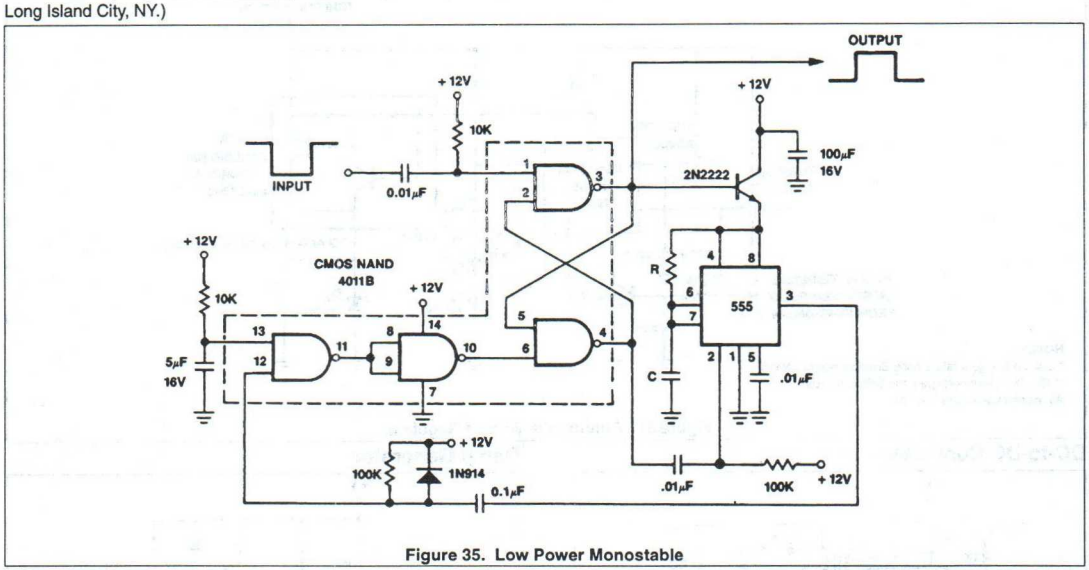


Figure 35. Low Power Monostable

Theory of Operation

The missing pulse detector (see Figure 10) operates as a triggered monostable multivibrator but with the added feature that the output signal remains high for a repetitive pulse condition at the trigger input node. This is accomplished by the addition of a reset inhibit function which prevents the normal time-out of the timer as long as there are input pulses present with period less than the time delay period. The circuit which provides this feature is an external PNP transistor with its base tied in parallel with the trigger input pin.

As the input pulse waveform exceeds the instantaneous timing coapacitor voltage by one V_{BE} in the negative direction, the PNP transistor is turned on momentarily, pulling the capacitor voltage toward ground potential. This incremental discharge action prevents the threshold voltage on Pin 6 from activating the reset action of the timer if the time delay between input pulses is shorter than the programmed time delay set by the external R/C network. This inhibit action occurs whenever the timing capacitor is prevented from exceeding 2/3 V_{CC}. Note that the degree of capacitor discharge is directly proportional to the duration of the turn-on time of the external PNP transistor. The capacitor voltage is equal to charge Q/capacitance C. The amount of delta V_C per input pulse is (I_C x T_P (sec)) / C(F) where T_P is the width of the trigger pulse and IC is the collector current of the PNP transistor during the duration of the trigger pulse. The inhibit condition is fulfilled by making the time

constant of the RC network, connected to Pin 6 and 7, somewhat longer than the interpulse period for normal fault free operation. The output will then remain positive until such a fault is long than the RC time constant. The missing pulse detector then provides a negative going output pulse proportional to the number of missing pulses received at the input.

The Speed Warning Circuit

Figure 17 shows an application which uses two missing pulse detectors in tandem as an aover-speed sensor. A speed transducer pulse signal of negative polarity is fed into the first stage of the NE556 which is actually used in the mode for which the timer is always allowed to time out if the pulse rate is below the desired speed threshold. This occurs, as discussed above, if the pulse input period is longer than the natural time-out period of the timer (as determined by the external RC network). The wavetrain coming from the first stage continually toggles for a speed condition below the set point. Next, stage one output signal is fed directly into the trigger input, Pin 8, of the second stage of the NE556, and simultaneously to the base of the external PNP discharge transistor. The second stage operation is identical to the one described in the missing pulse detector section above. The second stage timer output is held high when the speed transducer pulse train rate is below the critical threshold. This stage of the dual timer acts to alter the dynamic response of the speed detector so that a number of pulses must be missed to activate its output. This gives the detector a form of hysteresis and prevents the occurance of intermittent output signaling due to an instantaneous over speed condition. The length of the stage-two time delay threshold is programmed by adjusting R_{BUFFER}.

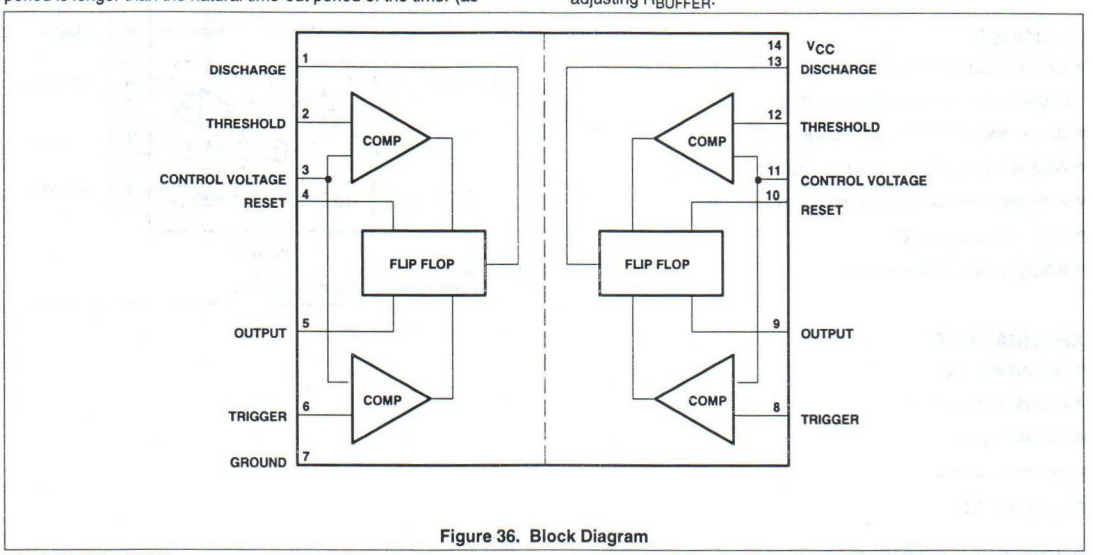


Figure 36. Block Diagram

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2. **"DC-to-DC Converter Uses the IC Timer",** Robert Soloman and Robert Broadway, EDN, September 5, 1973, pp. 87-91.
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4. **"Get Square Wave Tone Bursts With a Single Timer IC",** Sol Black, Electronic Design, September 1973, p. 148.
5. **"Toroid and Photo-SCR Prevent Ground Loops in High-Isolation Biological Pulser",** Joseph Sonsino, Electronic Design, June 21, 1973. p. 128.
6. **"Voltage-to-Frequency Converter Constructed With Few Components is Accurate to 0.2%",** 'Chaim Klement, Electronic Design, June 21, 1973, p. 124.
7. **"Positive Voltage Changed into Negative and No Transformer is Required",** Bert Pearl, Electronic Design, May 24, 1973, p. 164.
8. **"Pair of IC Timers Sounds Auto Burglar Alarm",** Michael Harvey, Electronics, June 21, 1973, p. 131.
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10. **"IC Timer can Function as Low Cost Line Receiver",** John Pate, Electronics, June 21, 1973, p. 132.
11. **"IC Timer Plus Thermister can Control Temperature",** Donald Dekold, Electronics, June 21, 1973, p. 132.
12. **"IC Timer Makes Economical Automobile Voltage Regulator",** T.J. Fusar, Electronics, September 21, 1974, p. 100.
13. **"Switching Regulators, the Efficient Way to Power",** Robert Olla, Electronics, August 16, 1973, pp. 94-95.
14. **"Put the IC Timer to Work in a Myriad of Ways",** Eugene Hnatek, EDN, March 5, 1973, pp. 54-58.

Quad timer — NE558

DESCRIPTION

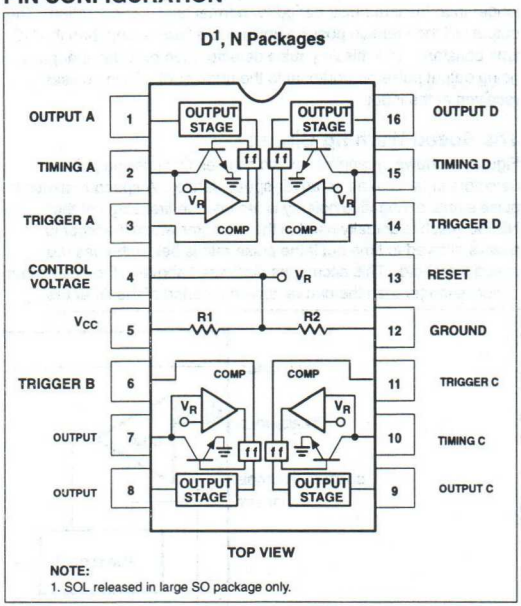
The 558 Quad Timers are monolithic timing devices which can be used to produce four independent timing functions. The 558 output sinks current. These highly stable, general purpose controllers can be used in a monostable mode to produce accurate time delays; from microseconds to hours. In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. A stable operation can be achieved by using two of the four timer sections.

The four timer sections in the 558 are edge-triggered; therefore, when connected in tandem for sequential timing applications, no coupling capacitors are required. Output current capability of 100mA is provided in both devices.

FEATURES

- 100mA output current per section
- Edge-triggered (no coupling capacitor)
- Output independent of trigger conditions
- Wide supply voltage range 4.5V to 16V
- Timer intervals from microseconds to hours
- Time period equals RC
- Military qualifications pending

PIN CONFIGURATION



NOTE:
1. SOL released in large SO package only.

APPLICATIONS

- Sequential timing
- Time delay generation
- Precision timing
- Industrial controls
- Quad one-shot

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline Large (SOL) Package	0 to +70°C	NE558D	0171B
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE558N	0406C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+16	V
P_D	Maximum power dissipation T_A=25°C ambient (still-air)[1]		
	N package	1450	mW
	D package	1090	mW
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:
1. Derate above 25°C, at the following rates:
   N package at 11.6mW/°C
   D package at 8.7mW/°C

DC AND AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE558			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		16	V
I_{CC}	Supply current	V_{CC}=Reset=15V		16	36	mA
	Timing accuracy (t=RC)	R=2kΩ to 100kΩ, C=1μF				
t_A	Initial accuracy			±2	5	%
$\Delta t_A/\Delta T$	Drift with temperature			30	150	ppm/°C
$\Delta t_A/\Delta V_S$	Drift with supply voltage			0.1	0.9	%/V
V_{TRIG}	Trigger voltage[1]	V_{CC}=15V	0.8		2.4	V
I_{TRIG}	Trigger current	Trigger=0V		5	100	μA
V_{RESET}	Reset voltage[2]		0.8		2.4	V
I_{RESET}	Reset current	Reset		50	500	μA
V_{TH}	Threshold voltage			0.63		×V_{CC}
	Threshold leakage			15		nA
V_{OUT}	Output voltage[3]	I_L=10mA		0.1	0.4	V
		I_L=100mA		1.0	2.0	V
	Output leakage			10	500	nA
t_{PD}	Propagation delay			1.0		μs
t_R	Rise time of output	I_L=100mA		100		ns
t_F	Fall time of output	I_L=100mA		100		ns

NOTES:

1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset, the trigger must be brought high and then low to implement triggering.
2. For reset below 0.8V, outputs set low and trigger inhibited. For reset above 2.4V, trigger enabled.
3. The 558 output structure is open-collector which requires a pull-up resistor to V_{CC} to sink current. The output is normally low sinking current.

558 EQUIVALENT CIRCUIT

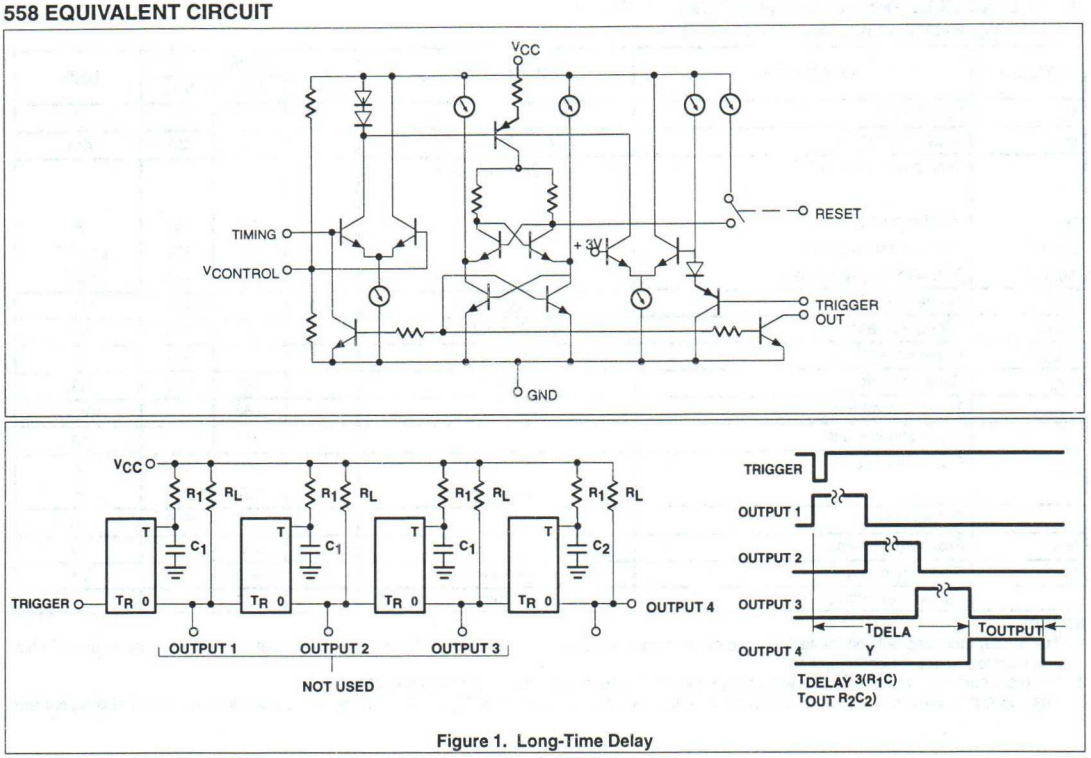
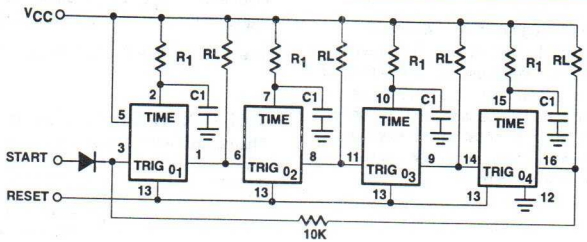
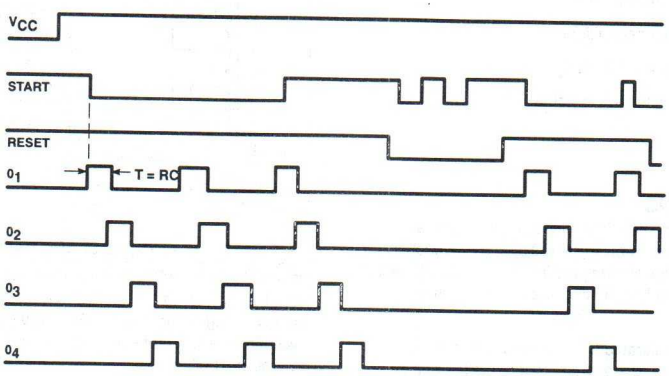


Figure 1. Long-Time Delay



a. Ring Counter



b. Expected Waveforms

Figure 2.

NE558 applications

AN171

INTRODUCTION

The 558 is a monolithic Quad Timer designed to be used in the timing range from a few microseconds to a few hours. Four entirely independent timing functions can be achieved using a timing resistor and capacitor for each section. Two sections of the quad may be interconnected for astable operation. All four sections may be used together, in tandem, for sequential timing applications up to several hours. No coupling capacitors are required when connecting the output of one timer section to the input of the next.

FEATURES

- 100mA output current per section
- Edge-triggered (no coupling capacitor)
- Output independent of trigger conditions
- Wide supply voltage range 4.5V to 16V
- Timer intervals from microseconds to hours
- Time period equals RC

CIRCUIT OPERATIONS

In the one-shot mode of operation, it is necessary to supply a minimum of two external components (the resistor and capacitor) for timing. The time period is equal to the product of R and C. An output load must be present to complete the circuit due to the output structure of the 558.

For astable operation, it is desirable to cross-couple two devices from the 558 Quad. The outputs are direct-coupled to the opposite trigger input. The duty cycle can be set by the ratio of R_1C_1 to R_2C_2, from close to zero to almost 100%. An astable circuit using one timer is shown in Figure 5b.

OUTPUT STRUCTURE 558

The 558 structure is open-collector which requires a pull-up resistor to V_{CC} and is capable of sinking 100mA per unit, but not to exceed the power dissipation and junction temperature rating of the die and package. The output is normally low and is switched high when triggered.

RESET

A reset function has been made available to reset all sections simultaneously to an output low state. During reset the trigger is disabled. After reset is finished, the trigger voltage must be taken high and then low to implement triggering.

The reset voltage must be brought below 0.8V to insure reset.

THE CONTROL VOLTAGE

The control voltage is also made available on the 558 timer. This allows the threshold voltage to be modulated, therefore controlling the output pulse width and duty cycle with an external control voltage. The range of this control voltage is from about 0.5V to V_{CC} minus 1V. This will give a cycle time variation of about 50:1. In a sequential timer with voltage-controlled cycle time, the timing periods remain proportional over the adjustment range.

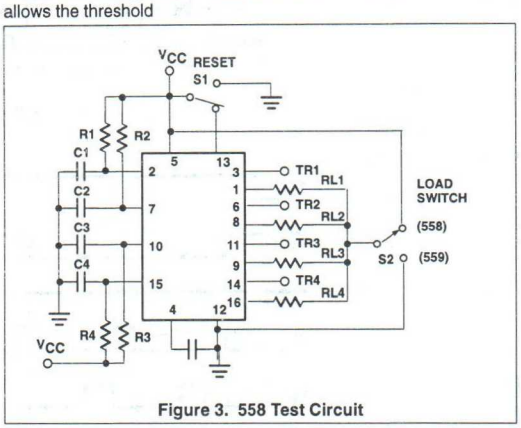
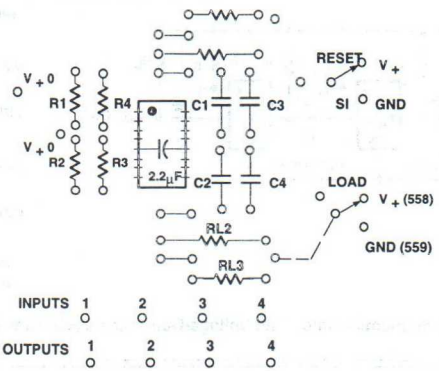


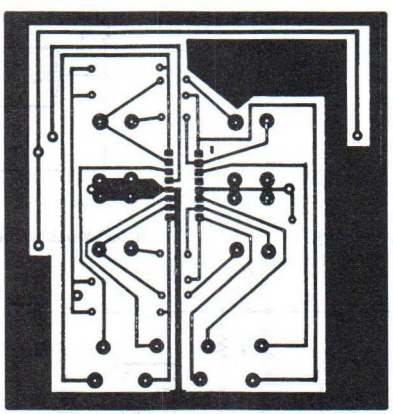
Figure 3. 558 Test Circuit

TEST BOARD FOR 558

The circuit layout can be used to test and characterize the 558 timer. S_2 is used to connect the loads to either V_{CC} or ground. The main precaution, in layout of the 558 circuit, is the path of the discharge current from the timing capacitor to ground (Pin 12). The path must be direct to Pin 12 and not on the ground bus. This is to prevent voltage spikes on the ground bus return due to current switching transient. It is also wise to use good power supply bypassing when large currents are being switched.



a. Test Board Layout



b. Foil Side

Figure 4.

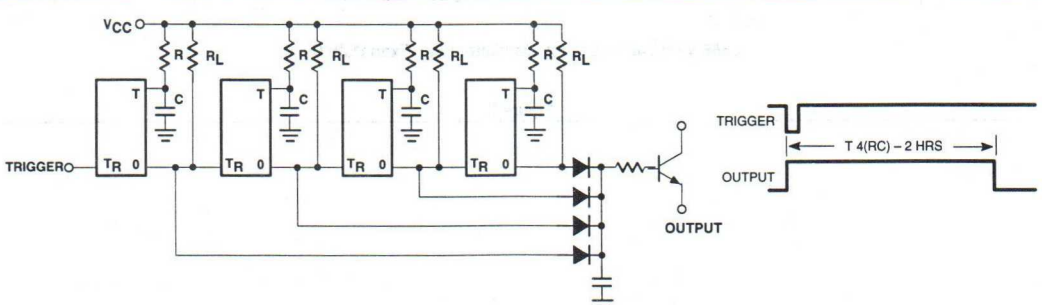


Figure 5. 558 Two-Hour Timer

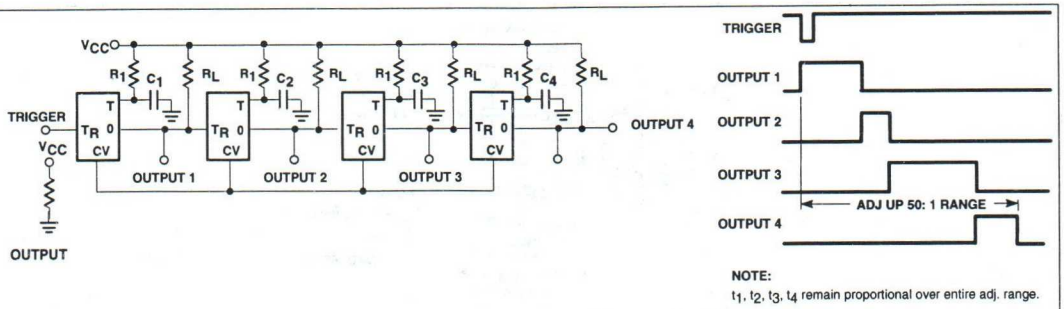


Figure 6. 558 Sequential Timer With Voltage-Controlled Cycle Time (50:1 Range)

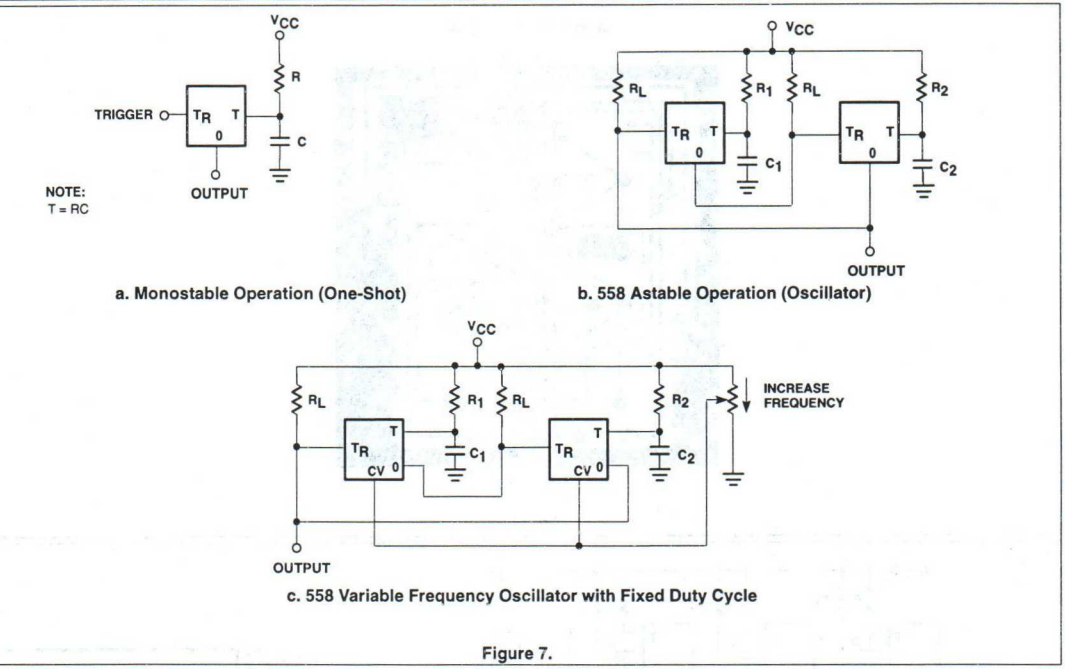


Figure 7.

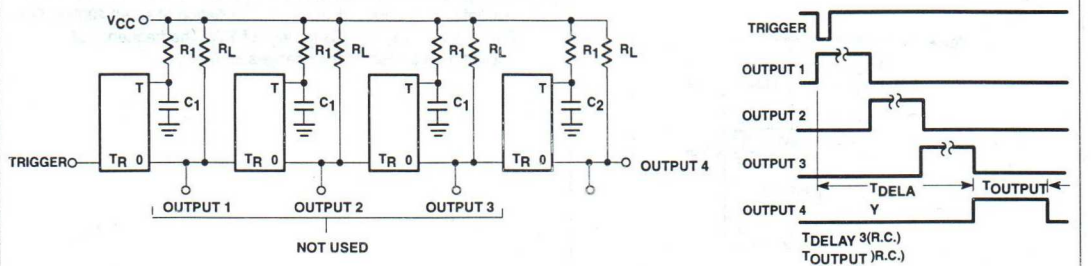
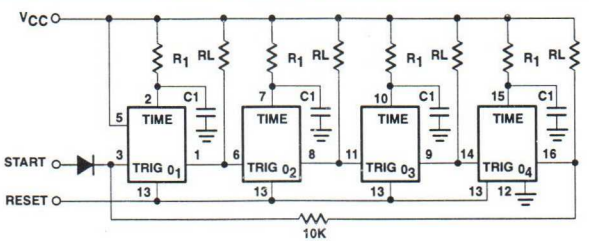
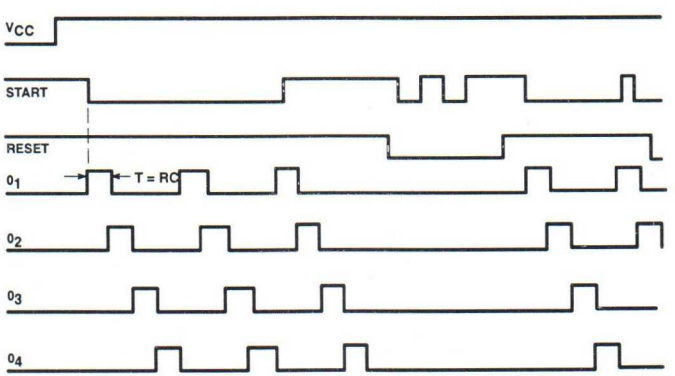


Figure 8. 558 Long Time Delay



a. Ring Counter



b. Expected Waveforms

Figure 9.

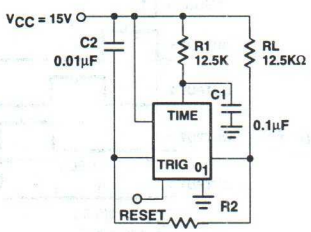


Figure 10. NE558 400Hz Square Wave Oscillator

A single section of the quad time may be used as a non-precision oscillator. The values given are for oscillation at about 400Hz. $T_1 \approx R_1C_1$ and $T_2 \approx 2.25\ R_2C_2$ for V_{CC} of 15V. The frequency of oscillation is subject to the changes in V_{CC}.

Section 6
High Frequency Phase-Locked Loops / Function Generators

INDEX

NE/SE564	Phase-locked loop	389
NE/SE566	Function generator	398
NE/SE567	Tone decoder/phase-locked loop	403
NE/SA568A	150MHz phase-locked loop	416
AN177	An overview of the phase-locked loop (PLL)	423
AN178	Modeling the PLL	428
AN179	Circuit description of the NE564	442
AN180	Frequency synthesis with the NE564	448
AN1801	10.8MHz FSK decoder with NE564	450
AN181	A 6MHz FSK converter design example for the NE564	453
AN182	Clock regenerator with crystal-controlled phase-locked loop VCO (NE564)	455

Phase-locked loop — NE/SE564

DESCRIPTION

The NE/SE564 is a versatile, high guaranteed frequency phase-locked loop designed for operation up to 50MHz. As shown in the Block Diagram, the NE/SE564 consists of a VCO, limiter, phase comparator, and post detection processor.

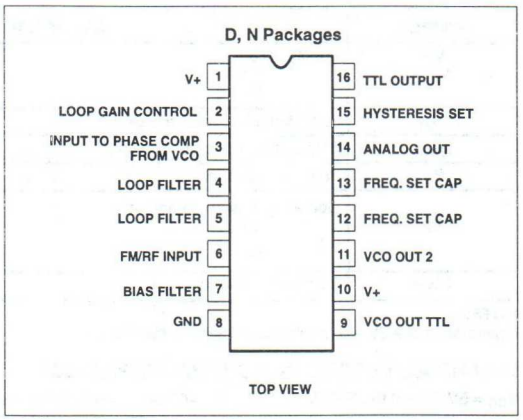
FEATURES

- Operation with single 5V supply
- TTL-compatible inputs and outputs
- Guaranteed operation to 50MHz
- External loop gain control
- Reduced carrier feedthrough
- No elaborate filtering needed in FSK applications
- Can be used as a modulator
- Variable loop gain (externally controlled)

APPLICATIONS

- High speed modems
- FSK receivers and transmitters
- Frequency Synthesizers

PIN CONFIGURATIONS

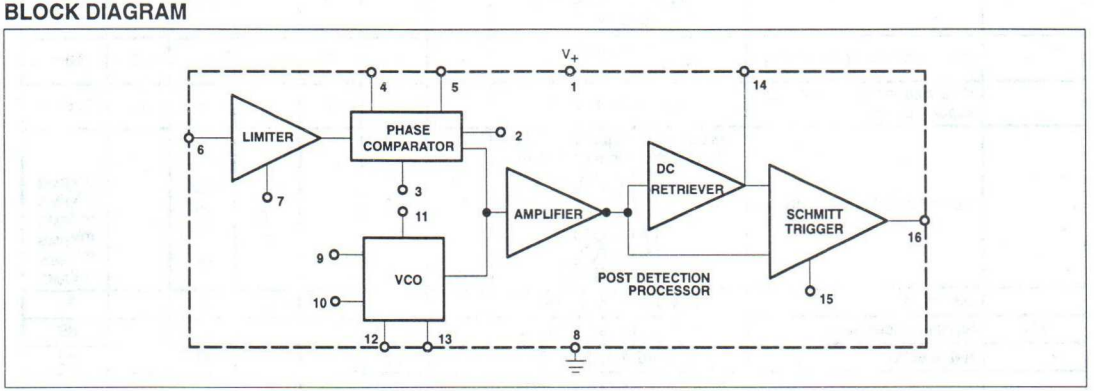


- Signal generators
- Various satcom/TV systems
- pin configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE564D	0005D
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE564N	0406C
16-Pin Plastic Dual In-Line Package (DIP)	-55 to +125°C	SE564N	0406C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V+	Supply voltage Pin 1 Pin 10	 14 6	 V V
I_{OUT}	Sink Max (Pin 9) and sourcing (Pin 11)	11	mA
I_{BIAS}	Bias current adjust pin (sinking)	1	mA
P_D	Power dissipation	600	mW
T_A	Operating ambient temperature NE SE	 0 to +70 -55 to +125	 °C °C
T_{STG}	Storage temperature range	-65 to +150	°C

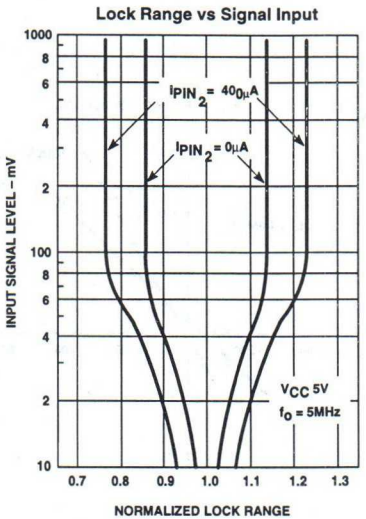
NOTE:
Operation above 5V will require heatsinking of the case.

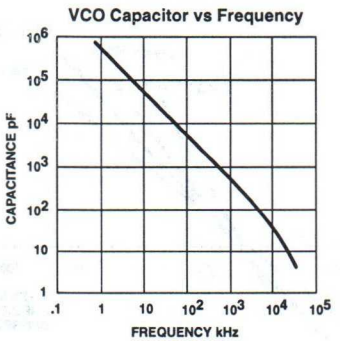
DC AND AC ELECTRICAL CHARACTERISTICS

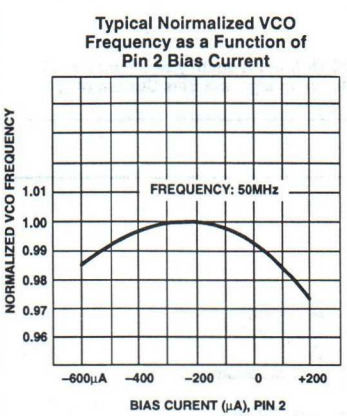
V_{CC} = 5V; T_A = 0 to 25°C; f_O = 5MHz, I_2 = 400µA; unless otherwise specified.

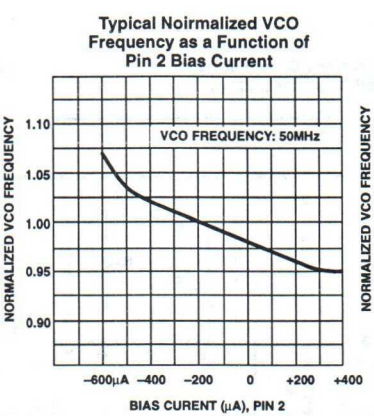
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SE564			LIMITS NE564			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Maximum VCO frequency	C_1 = 0 (stray)	50	65		45	60		MHz
	Lock range	Input ≥ 200mV$_{RMS}$ T_A = 25°C T_A = 125°C T_A = -55°C T_A = 0°C T_A = 70°C	 40 20 50	 70 30 80		 40	 70 70 40		 % of f_O
	Capture range	Input ≥ 200mV$_{RMS}$, R_2 = 27Ω	20	30		20	30		% of f_O
	VCO frequency drift with temperature	f_O = 5MHz, T_A = -55°C to +125°C T_A = 0 to +70°C = 0 to +70°C f_O = 5MHz, T_A = -55°C to +125°C T_A = 0 to +70°C		500 300	1500 800		 600 500		PPM/°C
	VCO free-running frequency	C_1 = 91pF R_C = 100Ω "Internal"	4	5	6	3.5	5	6.5	MHz
	VCO frequency change with supply voltage	V_{CC} = 4.5V to 5.5V		3	8		3	8	% of f_O
	Demodulated output voltage	Modulation frequency: 1kHz f_O = 5MHz, input deviation: 2%T = 25°C 1%T = 25°C 1%T = 0°C 1%T = -55°C 1%T = 70°C 1%T = 125°C	 16 8 6 12	 28 14 10 16		 16 8	 28 14 13 15		 mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$
	Distortion	Deviation: 1% to 8%		1			1		%
S/N	Signal-to-noise ratio	Std. condition, 1% to 10% dev.		40			40		dB
	AM rejection	Std. condition, 30% AM		35			35		dB
	Demodulated output at operating voltage	Modulation frequency: 1kHz f_O = 5MHz, input deviation: 1% V_{CC} = 4.5V V_{CC} = 5.5V	 7 8	 12 14		 7 8	 12 14		 mV$_{RMS}$ mV$_{RMS}$
I_{CC}	Supply current	V_{CC} = 5V I_1, I_{10}		45	60		45	60	mA
	Output "1" output leakage current "0" output voltage	 V_{OUT} = 5V, Pins 16, 9 I_{OUT} = 2mA, Pins 16, 9 I_{OUT} = 6mA, Pins 16, 9	 	 1 0.3 0.4	 20 0.6 0.8	 	 1 0.3 0.4	 20 0.6 0.8	 µA V V

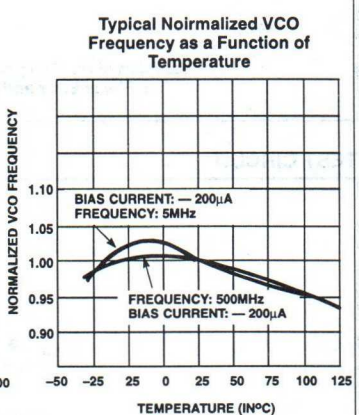
TYPICAL PERFORMANCE CHARACTERISTICS



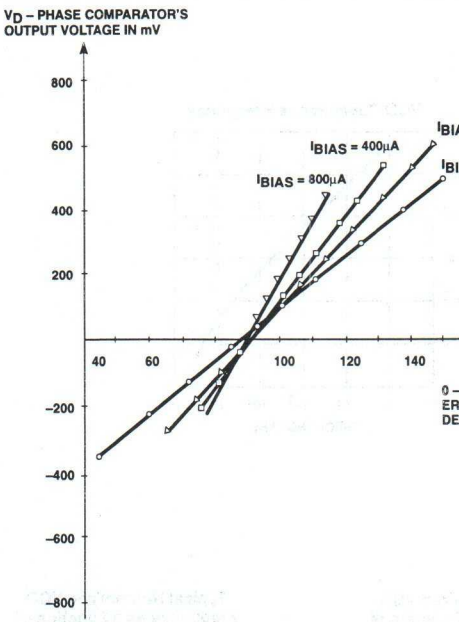




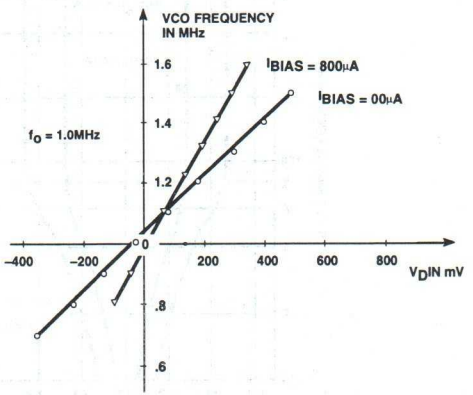




TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

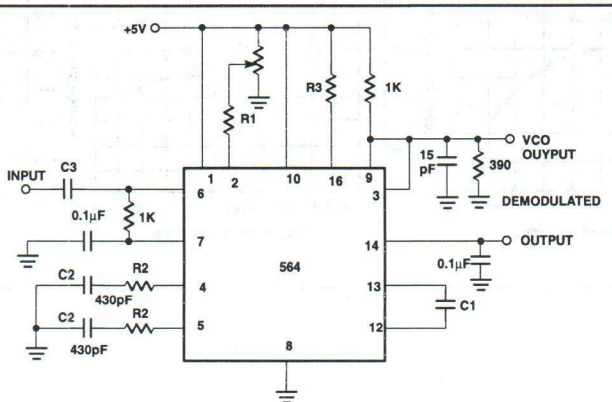


Variation of the Comparator's Output Voltage vs Phase Error and Bias Current (K_D)



VCO Output Frequency as a Function of Input Voltage and Bias Current (K_O)

TEST CIRCUIT



FUNCTIONAL DESCRIPTION

(Figure 1)

The NE564 is a monolithic phase-locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz.

In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{IN} - f_O)}{K_{VCO}} \quad (1)$$

K_{VCO} = conversion gain of the VCO

f_{IN} = frequency of the input signal

f_O = free-running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{IN} from f_O. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at Pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free-running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the DC levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrowband signals where the deviation in f_{IN} itself may be less than the change in f_O due to temperature. This effect can be eliminated if the DC or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the DC levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high-frequency performance, an emitter-coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q21 and Q23 with current sources Q25 - Q26 form the basic oscillator. The approximate free-running frequency of the oscillator is shown in the following equation:

$$f_O \cong \frac{1}{22\ R_C\ (C_1 + C_S)} \quad (2)$$

$R_C = R_{19} = R_{20} = 100\Omega$ (INTERNAL)

C_1 = external frequency setting capacitor

C_S = stray capacitance

Variation of V_D (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase detection processor consists of a doubled-balanced modulator with a limiter amplifier to improve AM rejection. Schottky-clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at Pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a DC retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the DC retriever is formed by the transconductance amplifier Q_{42} - Q_{43} together with an external capacitor which is connected at the amplifier output (Pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$V_O = \frac{g_M}{C_2} \int V_{IN} dt \quad (3)$$

g_M = transconductance of the amplifier

C_2 = capacitor at the output (Pin 14)

V_{IN} = signal voltage at amplifier input

With proper selection of C_2, the integrator time constant can be varied so that the output voltage is the DC or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysteresis is made up of Q_{49} - Q_{50} with positive feedback being provided by Q_{47} - Q_{48}. The hysteresis is varied by changing the current in Q_{52} with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a DC control, provides symmetric variation around the nominal value.

Design Formula

The free-running frequency of the VCO is shown by the following equation:

$$f_O \cong \frac{1}{22\ R_C\ (C_1 + C_S)} \quad (4)$$

$R_C = 100\Omega$

C_1 = external cap in farads

C_S = stray capacitance

The loop filter diagram shown is explained by the following equation:

$$f_S = \frac{1}{1 + sRC_3} \text{ (First Order)} \quad (5)$$

$R = R_{12} = R_{13} = 1.3k\Omega$ (Internal)*

By adding capacitors to Pins 4 and 5, a pole is added to the loop transfer at

$$\omega = \frac{1}{RC_3}$$

NOTE:
*Refer to Figure 1.

EQUIVALENT SCHEMATIC

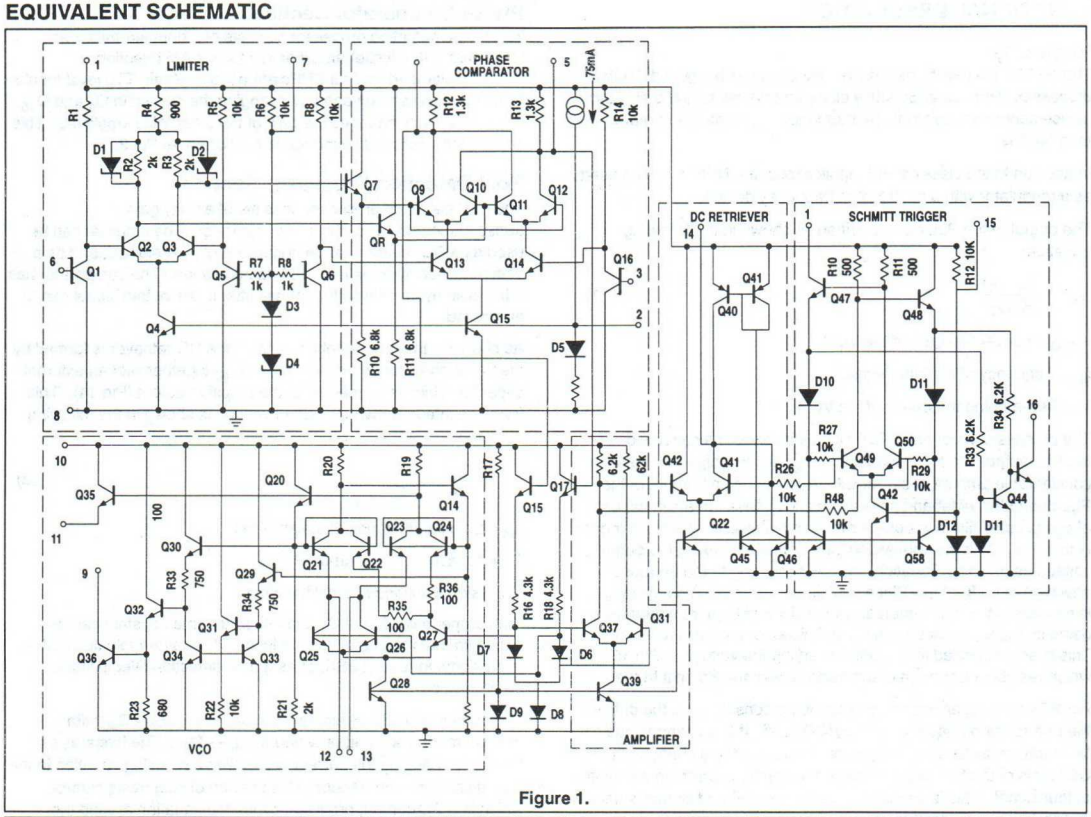


Figure 1.

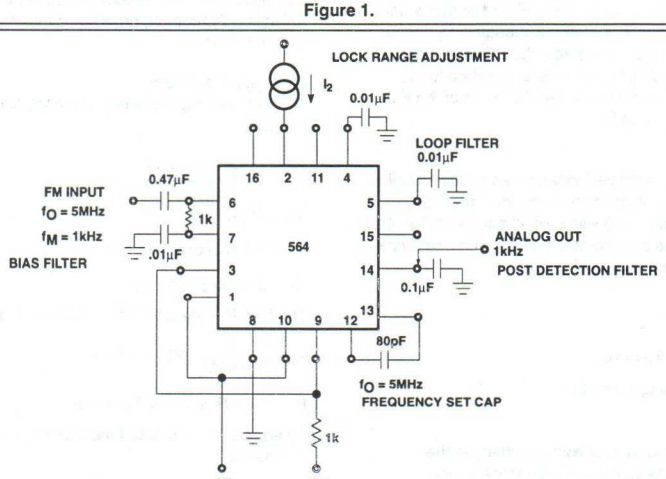


Figure 2. FM Demodulator at 5V

APPLICATIONS

FM Demodulator

The NE564 can be used as an FM demodulator. The connections for operation at 5V and 12V are shown in Figures 2 and 3, respectively. The input signal is AC coupled with the output signal being extracted at Pin 14. Loop filtering is provided by the capacitors at Pins 4 and 5 with additional filtering being provided by the capacitor at Pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be 1% or higher.

Modulation Techniques

The NE564 phase-locked loop can be modulated at either the loop filter ports (Pins 4 and 5) or the input port (Pin 6) as shown in Figure 4. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in Figure 5. This curve will be appropriate for signals injected into Pins 4 and 5 as shown in Figure 4.

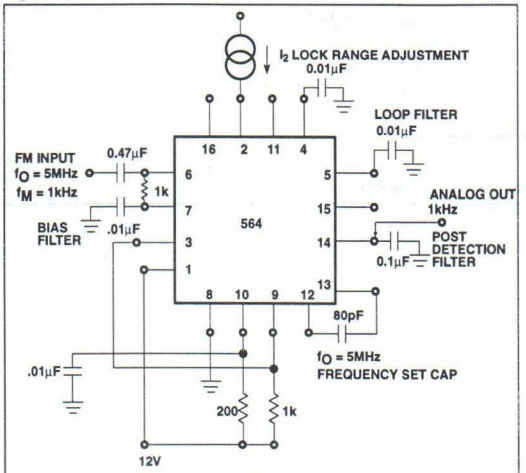


Figure 3. FM Demodulator at 12V

FSK Demodulation

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5V power supply. Demodulated DC voltages associated with the mark and space frequencies are recovered with a single external capacitor in a DC retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high-frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 5 shows a high-frequency FSK decoder designed for input frequency deviations of ±1.0MHz centered around a free-running frequency of 10.8MHz. the value of the timing capacitance required was estimated from Figure 8 to be approximately 40pF. A trimmer capacitor was added to fine tune f_O' 10.8MHz.

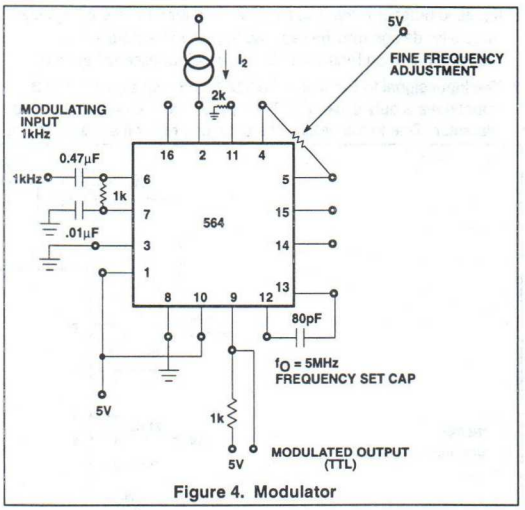


Figure 4. Modulator

The lock range graph indicates that the +1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero Pin 2 bias current. (While strictly this figure is appropriate only for 50MHz, it can be used as a guide for lock range estimates at other f_O' frequencies).

The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in Figure 7 for 20k, 500k, 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparators' output voltages with respect to each other and to the FSK output. The high-frequency sum components of the input and VCO frequency also are viable as noise on the phase comparator's outputs.

OUTLINE OF SETUP PROCEDURE

1. Determine operating frequency of the VCO: IF÷ N in feedback loop, then
   $f_O = N \times f_{IN}$.
2. Calculate value of the VCO frequency set capacitor:

$$C_O \cong \frac{1}{2200\, f_O}$$

3. Set I_2 (current sinking into Pin 2) for ≅ 100µA. After operation is obtained, this value may be adjusted for best dynamic behavior, and replace with fixed resistor value of $R_2 = \frac{V_{CC} - 1.3V}{I_{B_2}}$
4. Check VCO output frequency with digital counter at Pin 9 of device (loop open, VCO to ϕ det.). Adjust C_O trim or frequency adj. Pins 4 - 5 for exact center frequency, if needed.
5. Close loop and inject input signal to Pin 6. Monitor Pins 3 and 6 with two-channel scope. Lock should occur with $\Delta\phi_{3-6}$ equal to 90° (phase error).

6. If pulsed burst or ramp frequency is used for input signal, special loop filter design may be required in place of simple single capacitor filter on Pins 4 and 5. (See PLL application section)
7. The input signal to Pin 6 and the VCO feedback signal to Pin 3 must have a duty cycle of 50% for proper operation of the phase detector. Due to the nature of a balanced mixer if signals are not 50% in duty cycle, DC offsets will occur in the loop which tend to create an artificial or biased VCO.
8. For multiplier circuits where phase jitter is a problem, loop filter capacitors may be increased to a value of 10 - 50µF on Pins 4, 5. Also, careful supply decoupling may be necessary. This includes the counter chain V_{CC} lines.

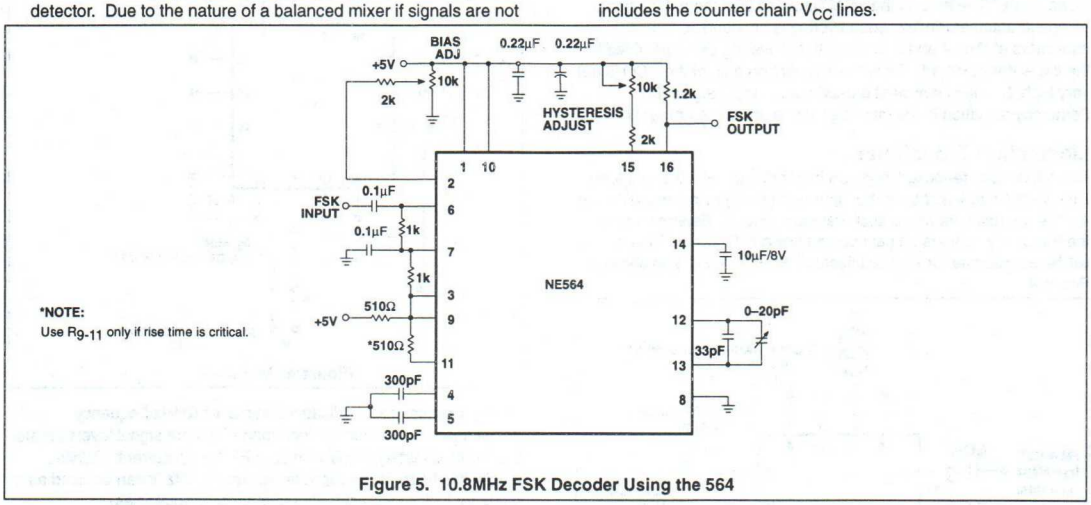
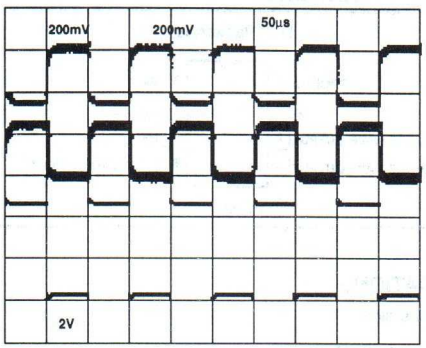
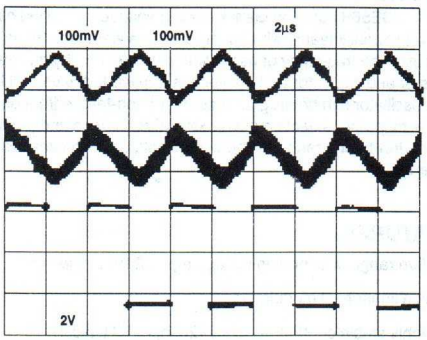


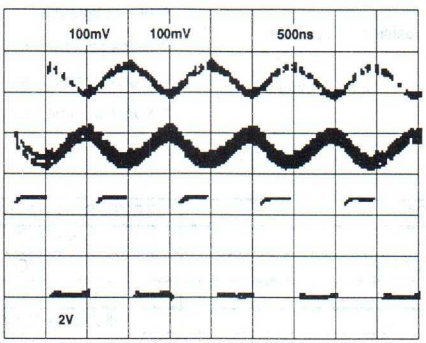
Figure 5. 10.8MHz FSK Decoder Using the 564



a. Data Rate = 20k Baud



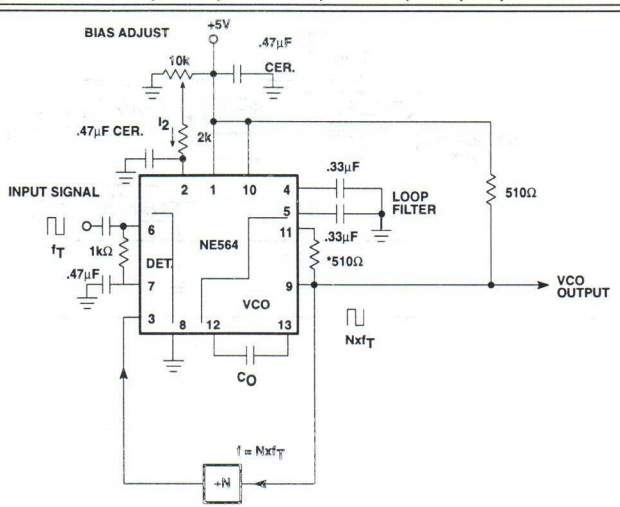
b. Data Rate = 500k Baud



c. Data Rate = 2.0m Baud

NOTES:
1. Top trace = Pin 4
2. Center trace = Pin 5
3. Bottom trace = Pin 16

Figure 6. Phase Comparator (Pins 4 and 5) and FSK (Pin 16) Outputs



*NOTE:
Use R_{9-11} only if rise time is critical.

Figure 7. NE564 Phase-Locked Frequency Multiplier

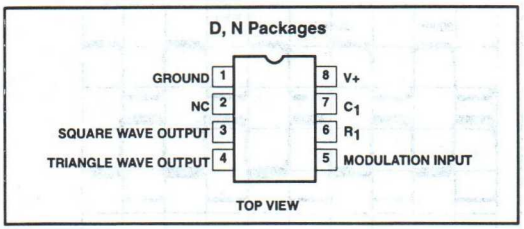
Function generator

NE/SE566

DESCRIPTION

The NE/SE566 Function Generator is a voltage-controlled oscillator of exceptional linearity with buffered square wave and triangle wave outputs. The frequency of oscillation is determined by an external resistor and capacitor and the voltage applied to the control terminal. The oscillator can be programmed over a ten-to-one frequency range by proper selection of an external resistance and modulated over a ten-to-one range by the control voltage, with exceptional linearity.

PIN CONFIGURATIONS



FEATURES

- Wide range of operating voltage (up to 24V; single or dual)
- High linearity of modulation
- Highly stable center frequency (200ppm/°C typical)
- Highly linear triangle wave output
- Frequency programming by means of a resistor or capacitor, voltage or current
- Frequency adjustable over 10-to-1 range with same capacitor

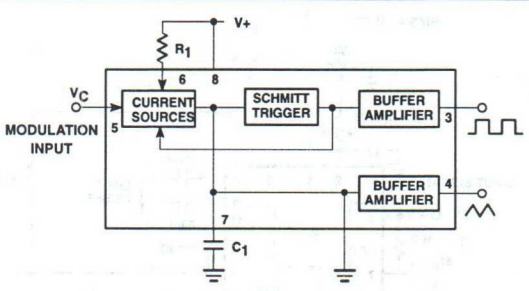
APPLICATIONS

- Tone generators
- Frequency shift keying
- FM modulators
- Clock generators
- Signal generators
- Function generators

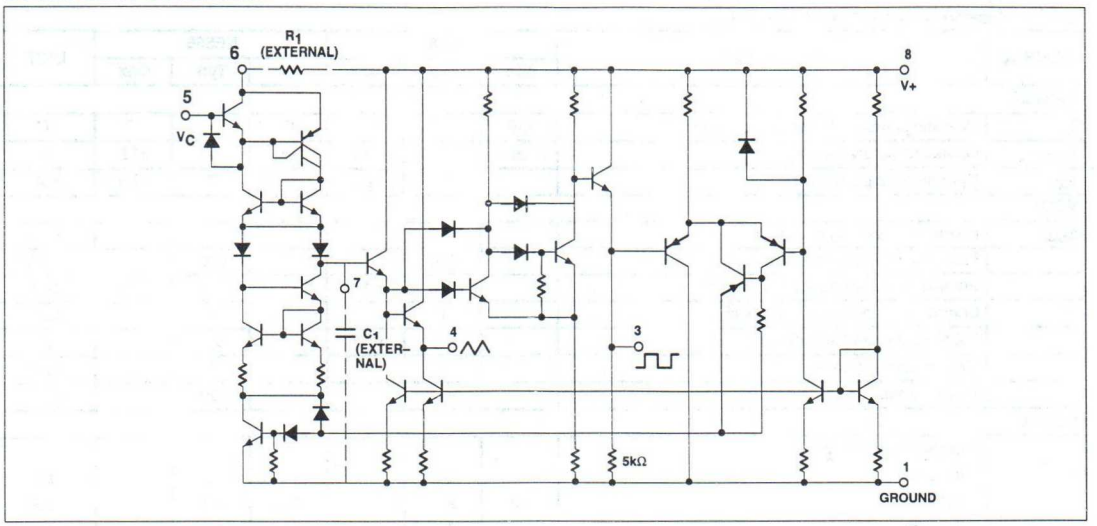
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE566D	0174C
14-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE566F	0581B
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE566N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE566N	0404B

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V+$	Maximum operating voltage	26	V
V_{IN}, V_C	Input voltage	3	V_{P-P}
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range		
	NE566	0 to +70	°C
	SE566	-55 to +125	°C
P_D	Power dissipation	300	mW

DC ELECTRICAL CHARACTERISTICS

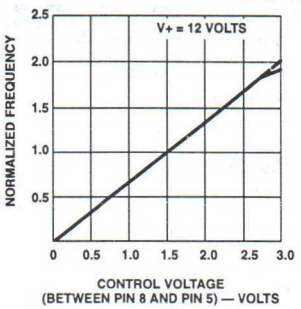
T_A=25°C, V_{CC}=±6V, unless otherwise specified.

SYMBOL	PARAMETER	SE566			NE566			UNIT
		Min	Typ	Max	Min	Typ	Max	
General								
T_A	Operating ambient temperature range	-55		125	0		70	°C
V_{CC}	Operating supply voltage	±6		±12	±6		±12	V
I_{CC}	Operating supply current		7	12.5		7	12.5	mA
VCO[1]								
f_{MAX}	Maximum operating frequency		1			1		MHz
	Frequency drift with temperature		500			600		ppm/°C
	Frequency drift with supply voltage		0.1	1		0.2	2	%/V
	Control terminal input impedance[2]		1			1		MΩ
	FM distortion (±10% deviation)		0.2	0.75		0.4	1.5	%
	Maximum sweep rate		1			1		MHz
	Sweep range		10:1			10:1		
Output								
	Triangle wave output							
	impedance		50			50		Ω
	voltage	1.9	2.4		1.9	2.4		V_{P-P}
	linearity		0.2			0.5		%
	Square wave input							
	impedance		50			50		Ω
	voltage	5	5.4		5	5.4		V_{P-P}
	duty Cycle	45	50	55	40	50	60	%
t_R	Rise time		20			20		ns
t_F	Fall Time		50			50		ns

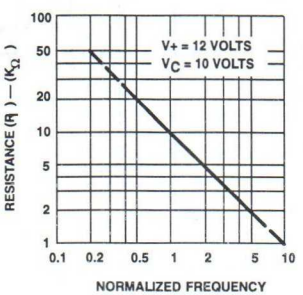
NOTES:
1. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20kΩ.
2. The bias voltage (V_C) applied to the control terminal (Pin 5) should be in the range $V+ \leq V_C \leq V+$.

TYPICAL PERFORMANCE CHARACTERISTICS

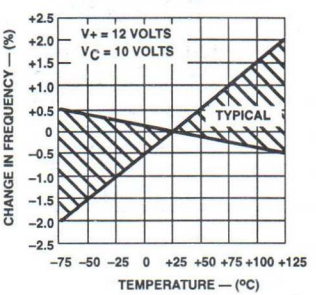
Normalized Frequency as a Function of Control Voltage



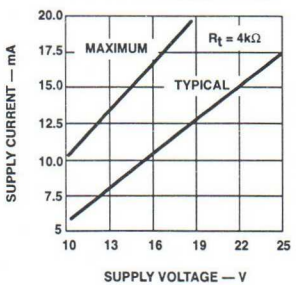
Normalized Frequency as a Function of Resistance (R1)



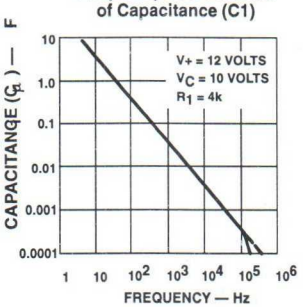
Change in Frequency as a Function of Temperature



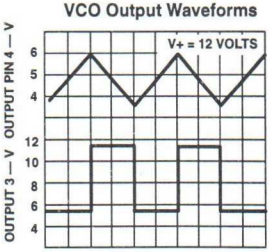
Power Supply Current as a Function of Supply Voltage



Frequency as a Function of Capacitance (C1)



VCO Output Waveforms



OPERATING INSTRUCTIONS

The NE/SE566 Function Generator is a general purpose voltage-controlled oscillator designed for highly linear frequency modulation. The circuit provides simultaneous square wave and triangle wave outputs at frequencies up to 1MHz. A typical connection diagram is shown in Figure 1. The control terminal (Pin 5) must be biased externally with a voltage (V_C) in the range

$$V+ \leq V_C \leq V+$$

where V_{CC} is the total supply voltage. In Figure 1, the control voltage is set by the voltage divider formed with R_2 and R_3. The modulating signal is then AC coupled with the capacitor C_2. The modulating signal can be direct coupled as well, if the appropriate DC bias voltage is applied to the control terminal. The frequency is given approximately by

$$f_O = \frac{2\,[(V+) - (V_C)]}{R_1\,C_1\,V+}$$

and R_1 should be in the range $2k\Omega < R_1 < 20k\Omega$.

A small capacitor (typically 0.001μF) should be connected between Pins 5 and 6 to eliminate possible oscillation in the control current source.

If the VCO is to be used to drive standard logic circuitry, it may be desirable to use a dual supply as shown in Figure 2. In this case the square wave output has the proper DC levels for logic circuitry. RTL can be driven directly from Pin 3. For DTL or TTL gates, which require a current sink of more than 1mA, it is usually necessary to connect a 5kΩ resistor between Pin 3 and negative supply. This increases the current sinking capability to 2mA. The third type of

interface shown uses a saturated transistor between the 566 and the logic circuitry. This scheme is used primarily for TTL circuitry which requires a fast fall time (<50ns) and a large current sinking capability.

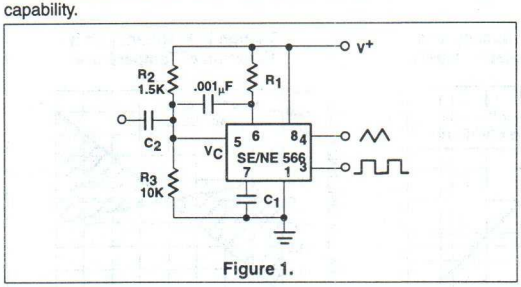


Figure 1.

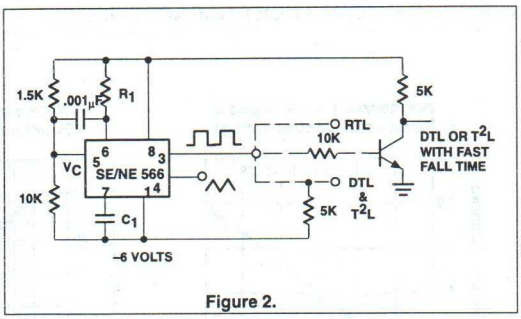


Figure 2.

Tone decoder/phase-locked loop — NE/SE567

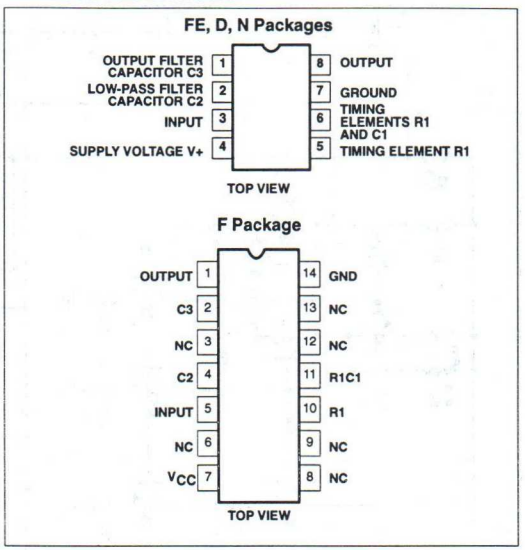
DESCRIPTION

The NE/SE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency and output delay are independently determined by means of four external components.

FEATURES

- Wide frequency range (.01Hz to 500kHz)
- High stability of center frequency
- Independently controllable bandwidth (up to 14%)
- High out-band signal and noise rejection
- Logic-compatible output with 100mA current sinking capability
- Inherent immunity to false signals
- Frequency adjustment over a 20-to-1 range with an external resistor
- Military processing available

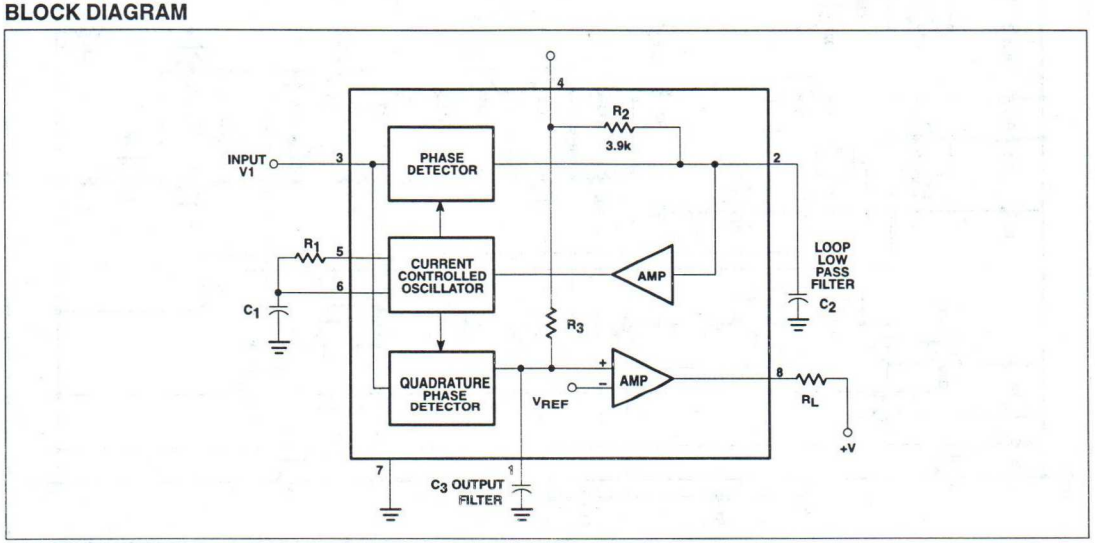
PIN CONFIGURATIONS



APPLICATIONS

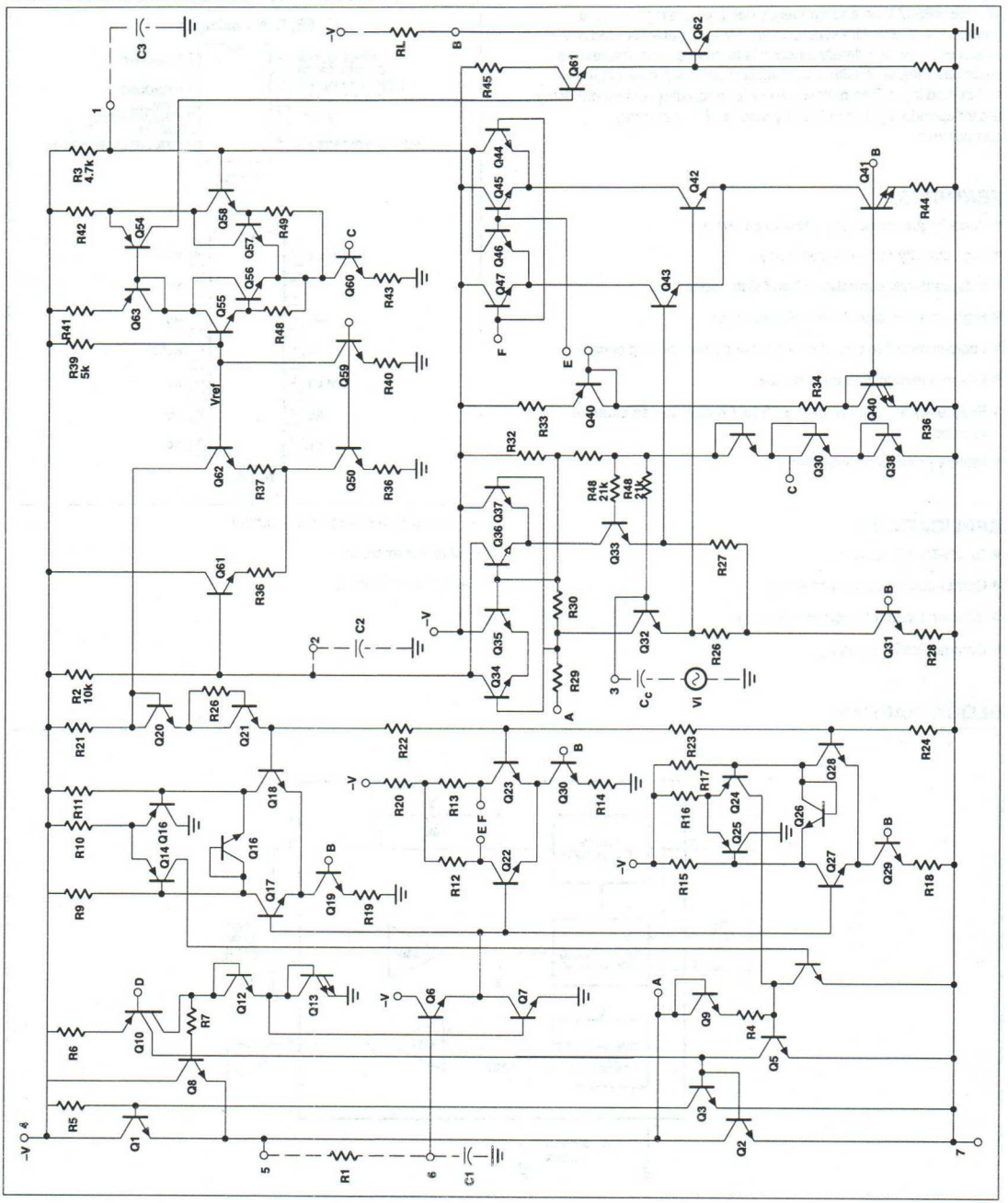
- Touch-Tone® decoding
- Carrier current remote controls
- Ultrasonic controls (remote TV, etc.)
- Communications paging
- Frequency monitoring and control
- Wireless intercom
- Precision oscillator

BLOCK DIAGRAM



®Touch-Tone is a registered trademark of AT&T.

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic SO	0 to +70°C	NE567D	0174C
14-Pin Cerdip	0 to +70°C	NE567F	0581B
8-Pin Plastic DIP	0 to +70°C	NE567N	0404B
8-Pin Plastic SO	-55°C to +125°C	SE567D	0174C
8-Pin Cerdip	-55°C to +125°C	SE567FE	0581B
8-Pin Plastic DIP	-55°C to +125°C	SE567N	0404B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating temperature		
	NE567	0 to +70	°C
	SE567	-55 to +125	°C
V_{CC}	Operating voltage	10	V
V+	Positive voltage at input	0.5 +V_S	V
V-	Negative voltage at input	-10	V_{DC}
V_{OUT}	Output voltage (collector of output transistor)	15	V_{DC}
T_{STG}	Storage temperature range	-65 to +150	°C
P_D	Power dissipation	300	mW

DC ELECTRICAL CHARACTERISTICS

V +=5.0V; T_A=25°C, unless otherwise specified.

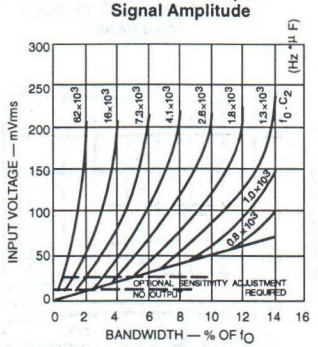
SYMBOL	PARAMETER	TEST CONDITIONS	SE567			NE567			UNIT
			Min	Typ	Max	Min	Typ	Max	
Center frequency[1]									
f_O	Highest center frequency			500			500		kHz
f_O	Center frequency stability[2]	-55 to +125°C		35 ±140			35 ±140		ppm/°C
		0 to +70°C		35 ±60			35 ±60		ppm/°C
f_O	Center frequency distribution	$f_O = 100kHz = \frac{1}{1.1R_1C_1}$	-10	0	+10	-10	0	+10	%
f_O	Center frequency shift with supply voltage	$f_O = 100kHz = \frac{1}{1.1R_1C_1}$		0.5	1		0.7	2	%/V
Detection bandwidth									
BW	Largest detection bandwidth	$f_O = 100kHz = \frac{1}{1.1R_1C_1}$	12	14	16	10	14	18	% of f_O
BW	Largest detection bandwidth skew			2	4		3	6	% of f_O
BW	Largest detection bandwidth—variation with temperature	V_I=300mV$_{RMS}$		±0.1			±0.1		%/°C
BW	Largest detection bandwidth—variation with supply voltage	V_I=300mV$_{RMS}$		±2			±2		%/V
Input									
R_{IN}	Input resistance		15	20	25	15	20	25	kΩ
V_I	Smallest detectable input voltage[4]	I_L=100mA, f_I=f_O		20	25		20	25	mV$_{RMS}$
	Largest no-output input voltage[4]	I_L=100mA, f_I=f_O	10	15		10	15		mV$_{RMS}$
	Greatest simultaneous out-band signal-to-in-band signal ratio			+6			+6		dB
	Minimum input signal to wide-band noise ratio	B_n=140kHz		-6			-6		dB
Output									
	Fastest on-off cycling rate			f_O/20			f_O/20		
	"1" output leakage current	V_8=15V		0.01	25		0.01	25	µA
	"0" output voltage	I_L=30mA		0.2	0.4		0.2	0.4	V
		I_L=100mA		0.6	1.0		0.6	1.0	V
t_F	Output fall time[3]	R_L=50Ω		30			30		ns
t_R	Output rise time[3]	R_L=50Ω		150			150		ns
General									
V_{CC}	Operating voltage range		4.75		9.0	4.75		9.0	V
	Supply current quiescent			6	8		7	10	mA
	Supply current—activated	R_L=20kΩ		11	13		12	15	mA
t_{PD}	Quiescent power dissipation			30			35		mW

NOTES:

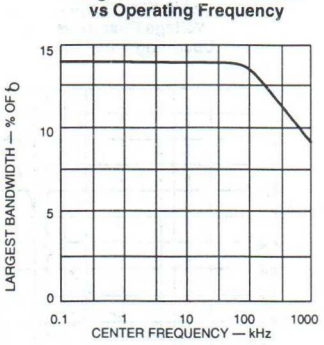
1. Frequency determining resistor R_1 should be between 2 and 20kΩ
2. Applicable over 4.75V to 5.75V. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.
4. With R_2=130kΩ from Pin 1 to V+. See Figure 1.

TYPICAL PERFORMANCE CHARACTERISTICS

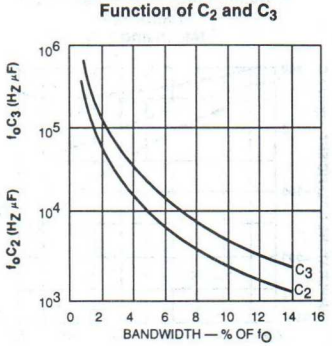
Bandwidth vs Input Signal Amplitude



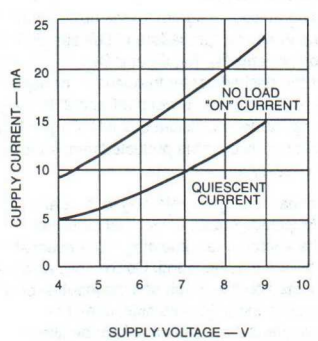
Largest Detection bandwidth vs Operating Frequency



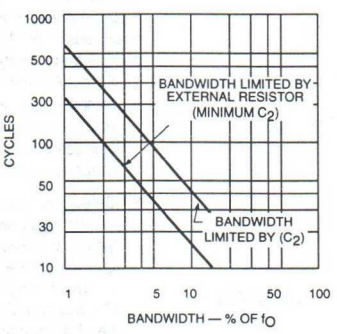
Detection bandwidth as a Function of C_2 and C_3



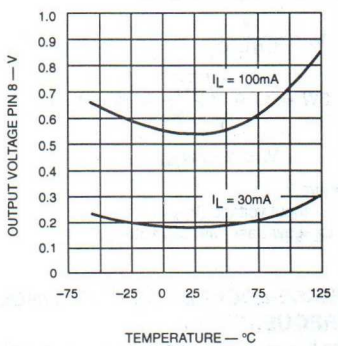
Typical Supply Current vs Supply Voltage



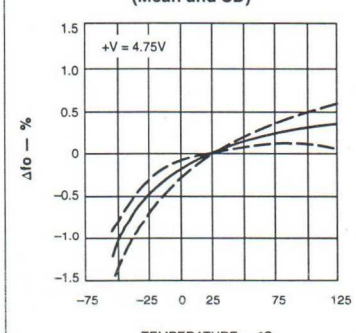
Greatest Number of Cycles Before Output



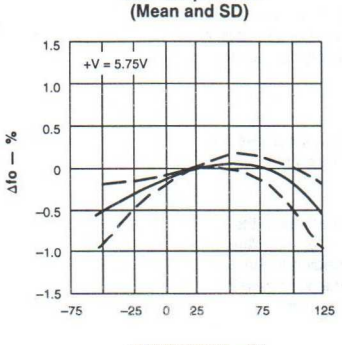
Typical Output Voltage vs Temperature



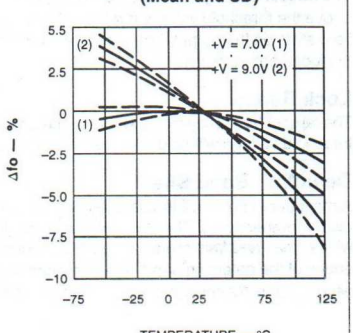
Typical Frequency Drift With Temperature (Mean and SD)



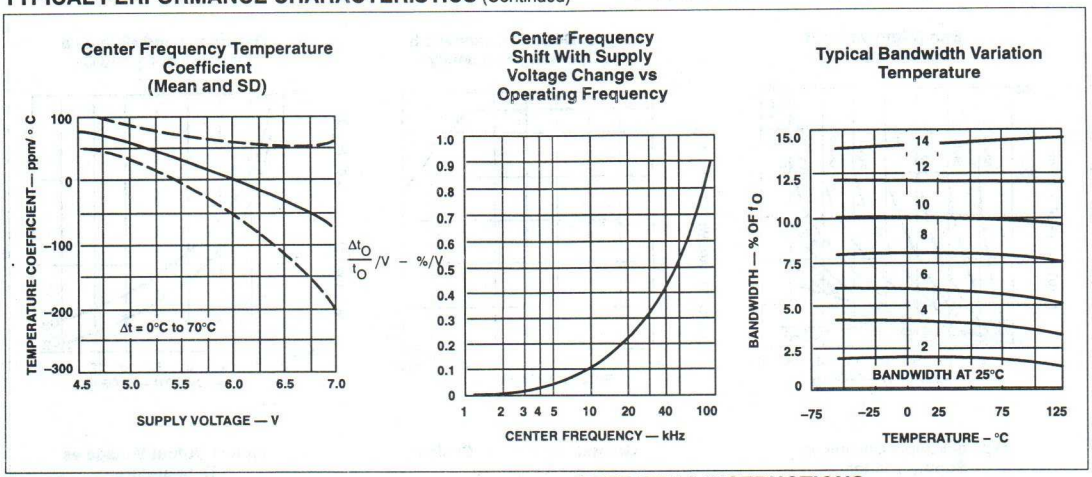
Typical Frequency Drift With Temperature (Mean and SD)



Typical Frequency Drift With Temperature (Mean and SD)



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



DESIGN FORMULAS

$$f_O \approx \frac{1}{1.1R_1 C_1}$$

$$BW \approx 1070 \sqrt{\frac{V_I}{f_O C_2}} \text{ in \% of } f_O$$

$$V_I \leq 200mV_{RMS}$$

Where

V_I=Input voltage (V_{RMS})

C_2=Low-pass filter capacitor (μF)

PHASE-LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (f_O)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection Bandwidth (BW)

The frequency range, centered about f_O, within which an input signal above the threshold voltage (typically $20mV_{RMS}$) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection Band Skew

A measure of how well the detection band is centered about the center frequency, f_O. The skew is defined as $(f_{MAX}+f_{MIN}-2f_O)/2f_O$ where fmax and fmin are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

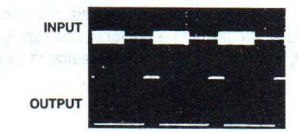
OPERATING INSTRUCTIONS

Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

1. Select R1 and C1 for the desired center frequency. For best temperature stability, R1 should be between 2K and 20K ohm, and the combined temperature coefficient of the R1C1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.

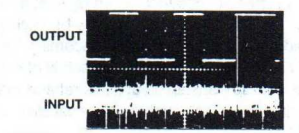
2. Select the low-pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude Variation is known, the appropriate value of $f_O \cdot C_2$ necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above $200mV_{RMS}$. The bandwidth, as noted on the graph, is then controlled solely by the $f_O \cdot C_2$ product (f_O (Hz), C2(μF)).

TYPICAL RESPONSE



NOTE:
R_L = 100Ω

Response to 100mV$_{RMS}$ Tone Burst



NOTES:
S/N = –6dB
R_L = 100Ω
Noise Bandwidth = 140Hz

Response to Same Input Tone Burst With Wideband Noise

3. The value of C3 is generally non-critical. C3 sets the band edge of a low-pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C3 is too large, turn-on and turn-off of the

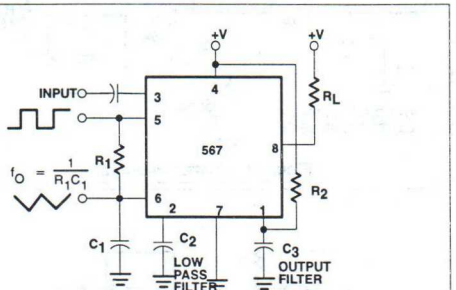


Figure 1.

output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

4. Optional resistor R2 sets the threshold for the largest "no output" input voltage. A value of 130kΩ is used to assure the tested limit of 10mV$_{RMS}$ min. This resistor can be referenced to ground for increased sensitivity. The explanation can be found in the "optional controls" section which follows.

AVAILABLE OUTPUTS (Figure 1)

The primary output is the uncommitted output transistor collector, Pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at Pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_O with a slope of about 20mV per percent of frequency deviation. The average voltage at Pin 1 is, during lock, a function of the in-band input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude (+V -2V_{BE})≡(+V-1.4V) having a DC average of +V/2. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of 1V_{P-P} with an average DC level of +V/2. Only high impedance loads may be

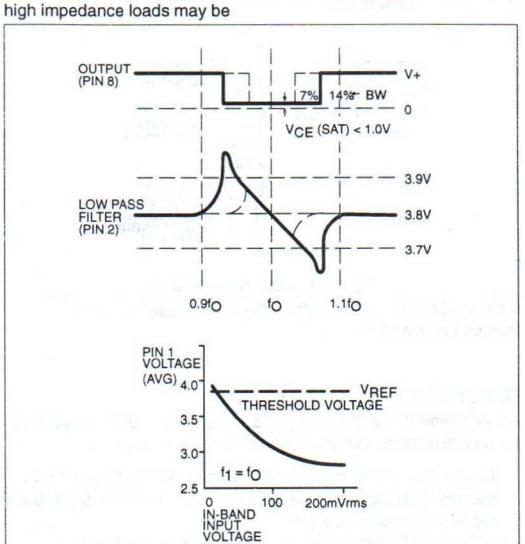


Figure 2. Typical Output Response

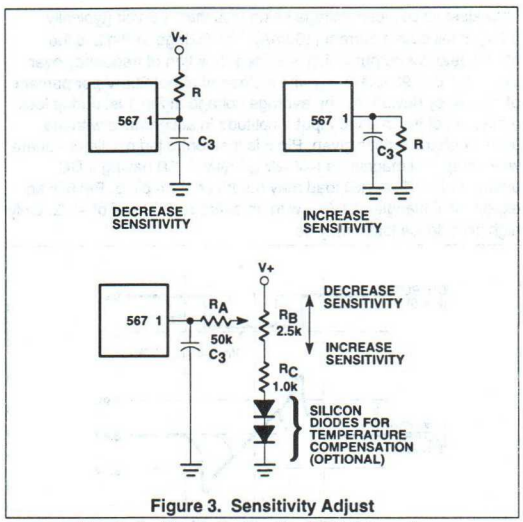


Figure 3. Sensitivity Adjust

connected to pin 6 without affecting the CCO duty cycle or temperature stability.

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the inband signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_O/3$, $f_O/5$, etc.
2. The 567 will lock onto signals near $(2n+1)\ f_O$, and will give an output for signals near $(4n+1)\ f_O$ where n=0, 1, 2, etc. Thus, signals at $5f_O$ and $9f_O$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.
3. Maximum immunity from noise and out-band signals is afforded in the low input level (below $200mV_{RMS}$) and reduced bandwidth operating mode. However, decreased loop damping causes the worst-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.
4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01µF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_O/10$ baud.

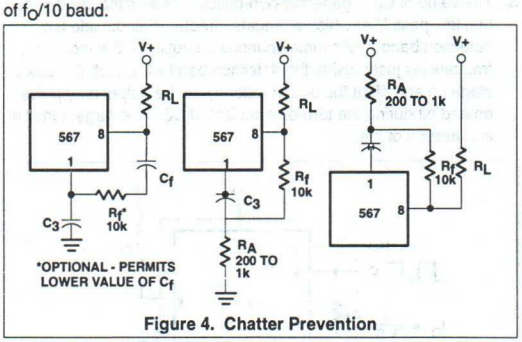


Figure 4. Chatter Prevention

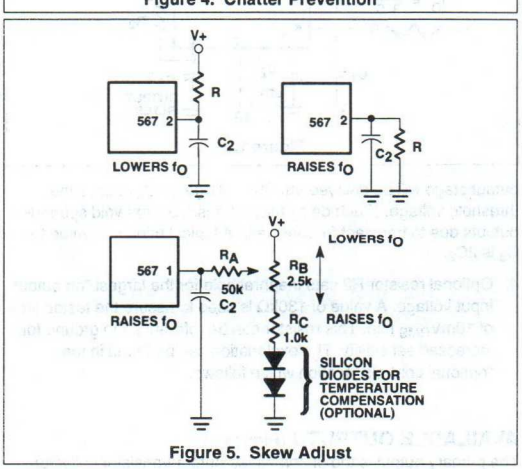


Figure 5. Skew Adjust

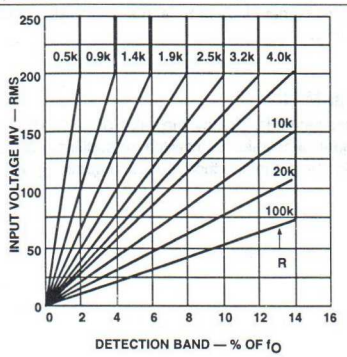
$$C_2 = \frac{130}{f_O}\ \mu F$$

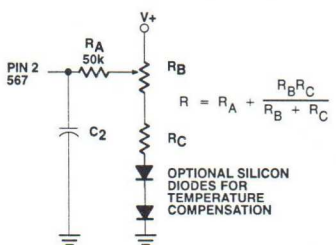
$$C_3 = \frac{260}{f_O}\ \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

OPTIONAL CONTROLS (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.





NOTE:

$$\frac{130}{f_O}\left(\frac{10k + R}{R}\right) < C_2 < \frac{1300}{f_O}\left(\frac{10k + R}{R}\right)$$

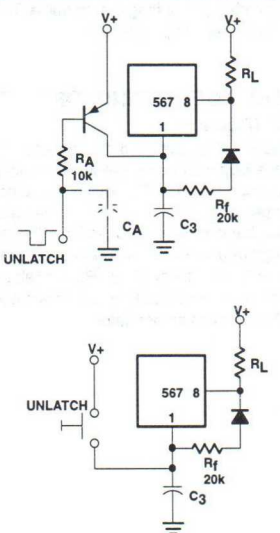
Adjust control for symmetry of detection band edges about f_O.

Figure 6. BW Reduction

SENSITIVITY ADJUSTMENT (Figure 3)

When operated as a very narrow-band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and out-band signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the out-band beat notes do not feed through to the output stage. Since the input level must



NOTE:
C_A prevents latch-up when power supply is turned on.

Figure 7. Output Latching

CHATTER PREVENTION (Figure 4)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (Pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT (Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

ALTERNATE METHOD OF BANDWIDTH REDUCTION (Figure 6)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff
frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

OUTPUT LATCHING (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between Pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

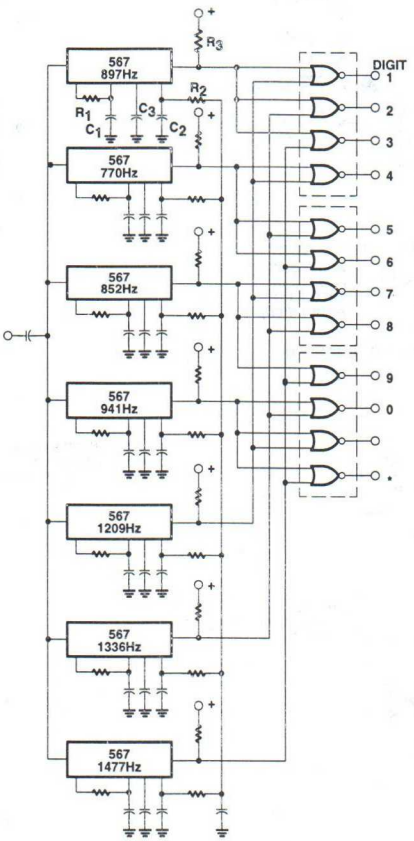
REDUCTION OF C1 VALUE

For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage-follower between the R_1 C_1 junction and Pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

PROGRAMMING

To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating NPN transistors.

TYPICAL APPLICATIONS



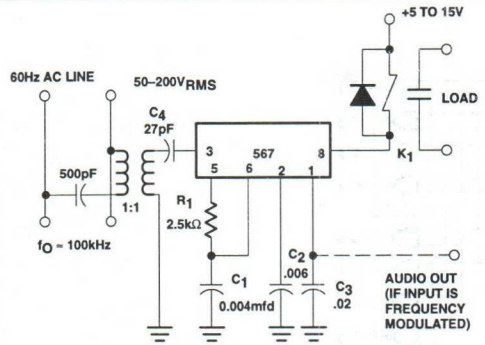
NOTES:

Component values (Typical)

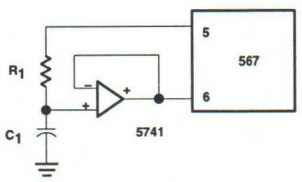
R_1 = 26.8 to 15kΩ
R_2 = 24.7kΩ
R_3 = 20kΩ
C_1 = 0.10mF
C_2 = 1.0mF 5V
C_3 = 2.2mF 6V
C_4 = 250μF 6V

Touch-Tone® Decoder

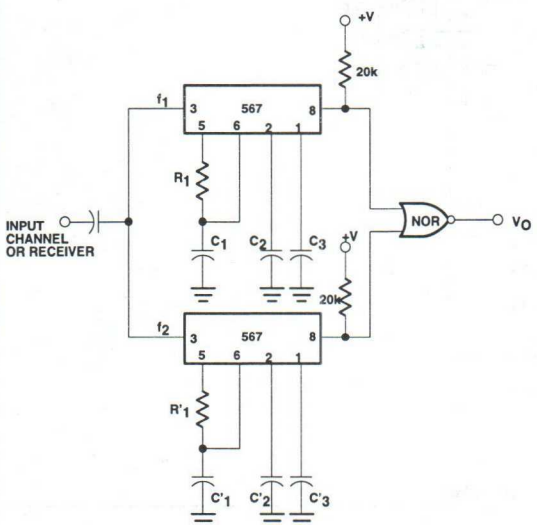
TYPICAL APPLICATIONS (Continued)



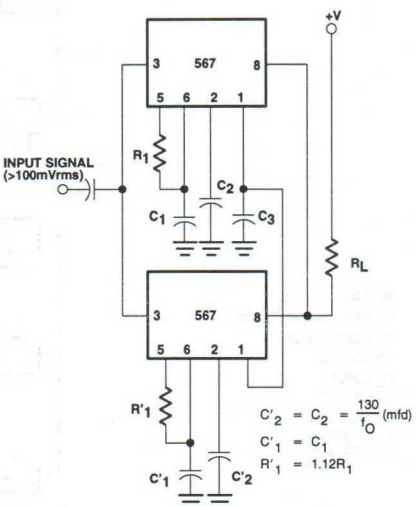
Carrier-Current Remote Control or Intercom



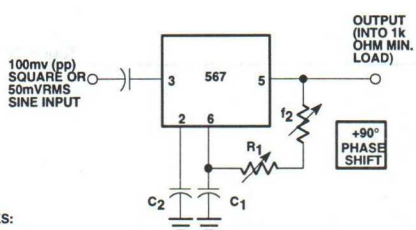
Precision VLF



Dual-Tone Decoder



24% Bandwidth Tone Decoder

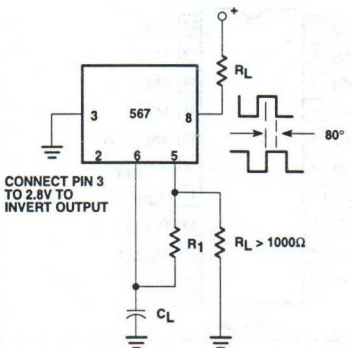


NOTES:
$R_2 = R_1/5$
Adjust R_1 so that $\phi = 90°$ with control midway.

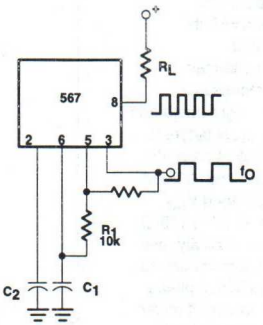
0° to 180° Phase Shifter

NOTES:
1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1 f_2) tones is possible.

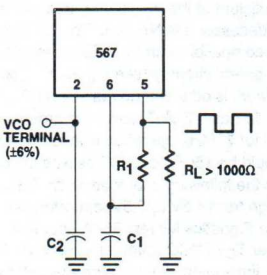
TYPICAL APPLICATIONS (Continued)



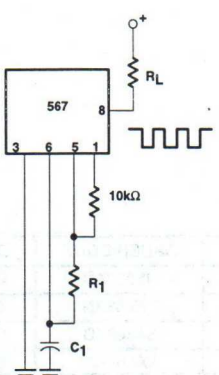
Oscillator With Quadrature Output



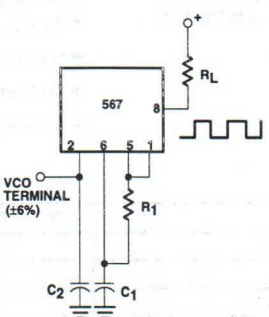
Oscillator With Double Frequency Output



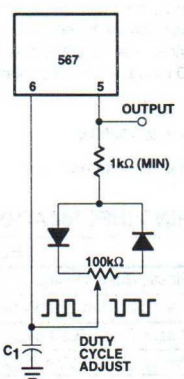
Precision Oscillator With 20ns Switching



Pulse Generator With 25% Duty Cycle



Precision Oscillator to Switch 100mA Loads



Pulse Generator

150MHz phase-locked loop — NE/SA568A

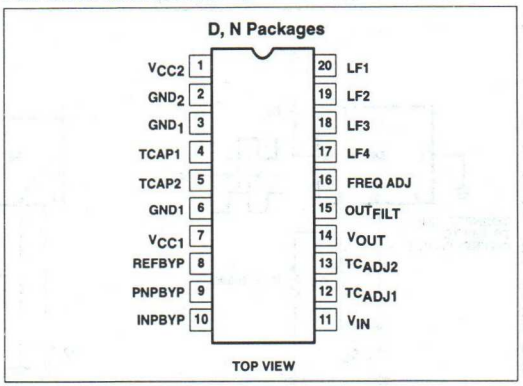
DESCRIPTION

The NE568A is a monolithic phase-locked loop (PLL) which operates from 1Hz to frequencies in excess of 150MHz and features an extended supply voltage range and a lower temperature coefficient of the V_{CO} center frequency in comparison with its predecessor, the NE 568. The NE568A is function and pin-compatible with the NE568, requiring only minor changes in peripheral circuitry (see Figure 1). Temperature compensation network is different, no resistor on Pin 12, needs to be grounded and Pin 13 has a 3.9kΩ resistor to ground. Timing cap, C_2, is different and for 70MHz operation with temperature compensation network should be 16pF, not 34pF as was used in the NE568. The NE568A has the following improvements: ESD protected; extended V_{CC} range from 4.5V to 5.5V; operating temperature range -55 to 125°C (see Signetics Military 568A data sheet); less layout sensitivity; and lower T_C of VCO (center frequency). The integrated circuit consists of a limiting amplifier, a current-controlled oscillator (ICO), a phase detector, a level shift circuit, V/I and I/V converters, an output buffer, and bias circuitry with temperature and frequency compensating characteristics. The design of the NE568A is particularly well-suited for demodulation of FM signals with extremely large deviation in systems which require a highly linear output. In satellite receiver applications with a 70MHz IF, the NE568A will demodulate ±20% deviations with less than 1.0% typical non-linearity. In addition to high linearity, the circuit has a loop filter which can be configured with series or shunt elements to optimize loop dynamic performance. The NE568A is available in 20-pin dual in-line and 20-pin SO (surface mounted) plastic packages.

FEATURES

- Operation to 150MHz
- High linearity buffered output

PIN CONFIGURATION



- Series or shunt loop filter component capability
- External loop gain control
- Temperature compensated
- ESD protected[1]

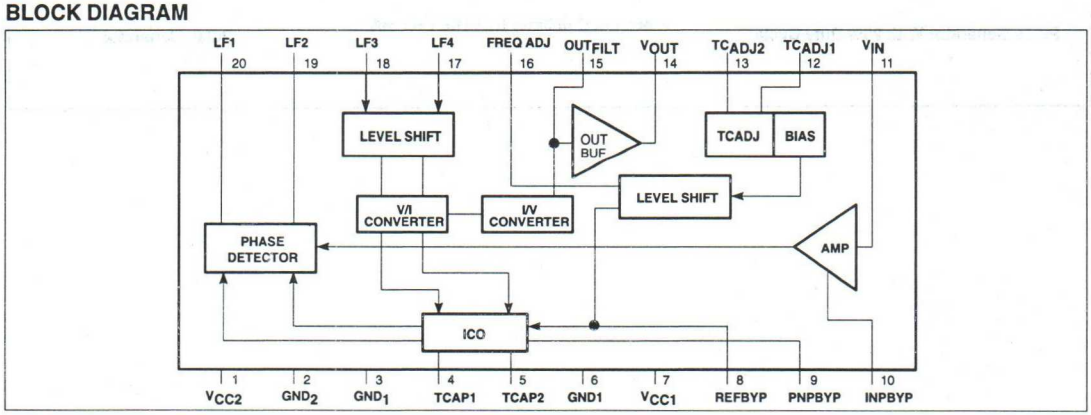
APPLICATIONS

- Satellite receivers
- Fiber optic video links
- VHF FSK demodulators
- Clock Recovery

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) Package	0 to +70°C	NE568AD	0172D
20-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE568AN	0408B
20-Pin Plastic Small Outline Large (SOL) Package	-40 to +85°C	SA568AD	0172D
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA568AN	0408B

BLOCK DIAGRAM



NOTE:

1. Pins 4 and 5 can tolerate 1000V only, and all other pins, greater than 2000V for ESD (human body model).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	6	V
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
P_{DMAX}	Maximum power dissipation	400	mW
θ_{JA}	Thermal resistance	80	°C/W

ELECTRICAL CHARACTERISTICS

The elctrical characteristics listed below are actual tests (unless otherwise stated) performed on each device with an automatic IC tester prior to shipment. Performance of the device in automated test set-up is not necessarily optimum. The NE568A is layout-sensitive. Evaluation of performance for correlation to the data sheet should be done with the circuit and layout of Figures 1, 2, and 3 with the evaluation unit soldered in place. (Do not use a socket!)

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V; T_A = 25°C; f_O = 70MHz, Test Circuit Figure 1, f_{IN} = -20dBm, R_4 = 3.9kΩ, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA568A			UNITS
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
I_{CC}	Supply current			54	70	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA568A			UNITS
			MIN	TYP	MAX	
f_{OSC}	Maximum oscillator operating frequency[3]		150			MHz
	Input signal level		50 -20[1]		2000 +10	mV_{P-P} dBm
BW	Demodulated bandwidth			$f_O/7$		MHz
	Non-linearity[5]	Dev = ±20%, Input = -20dBm		1.0	4.0	%
	Lock range[2]	Input = -20dBm	±25	±35		% of f_O
	Capture range[2]	Input = -20dBm	±20	±30		% of f_O
	TC of f_O	Figure 1		100		ppm/°C
R_{IN}	Input resistance[4]		1			kΩ
	Output impedance			6		Ω
	Demodulated V_{OUT}	Dev = ±20% of f_O measured at Pin 14	0.40	0.52		V_{P-P}
	AM rejection	V_{IN} = -20dBm (30% AM) referred to ±20% deviation		50		dB
f_O	Distribution[6]	Centered at 70MHz, R_2 = 1.2kΩ, C_2 = 16pF, R_4 = 3.9Ω (C_2 + C_{STRAY} = 20pF)	-15	0	+15	%
f_O	Drift with supply	4.5V to 5.5V		2		%/V

NOTE:

1. Signal level to assure all published parameters. Device will continue to function at lower levels with varying performance.
2. Limits are set symmetrical to f_O. Actual characteristics may have asymmetry beyond the specified limits.
3. Not 100% tested, but guaranteed by design.
4. Input impedance depends on package and layout capacitances. See Figures 4 and 5.
5. Linearity is tested with incremental changes in inupt frequency and measurement of the DC output voltage at Pin 14 (V_{OUT}). Non-linearity is then calculated from a straight line over the deviation range specified.
6. Free-running frequency is measured as feedthrough to Pin 14 (V_{OUT}) with no input signal applied.

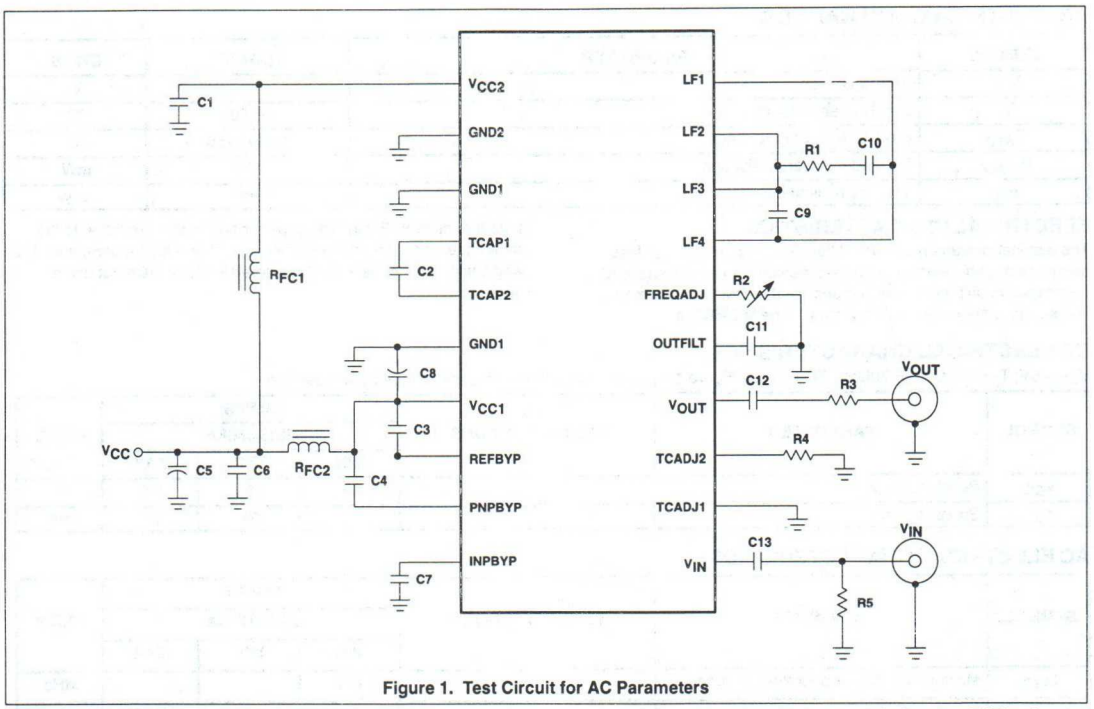


Figure 1. Test Circuit for AC Parameters

FUNCTIONAL DESCRIPTION

The NE568A is a high-performance phase-locked loop (PLL). The circuit consists of conventional PLL elements, with special circuitry for linearized demodulated output, and high-frequency performance. The process used has NPN transistors with $f_T > 6GHz$. The high gain and bandwidth of these transistors make careful attention to layout and bypass critical for optimum performance. The performance of the PLL cannot be evaluated independent of the layout. The use of the application layout in this data sheet and surface-mount capacitors are high recommended as a starting point.

The input to the PLL is through a limiting amplifier with a gain of 200. The input of this amplifier is differential (Pins 10 and 11). For single-ended applications, the input must be coupled through a DC-blocking capacitor with low impedance at the frequency of interest. The single-ended input is normally applied to Pin 11 with Pin 10 AC-bypassed with a low-impedance capacitor. The input impedance is characteristically slightly above 500Ω. Impedance match is not necessary, but loading the signal source should be avoided. When the source is 50 or 75Ω, a DC-blocking capacitor is usually all that is needed.

Input amplification is low enough to assure reasonable response time in the case of large signals, but high enough for good AM rejection. After amplification, the input signal drives one port of a multiplier-cell phase detector. The other port is driven by the current-controlled oscillator (ICO). The output of the phase comparator is a voltage proportional to the phase difference of the input and ICO signals. The error signal is filtered with a low-pass filter to provide a DC-correction voltage, and this voltage is converted to a current which is applied to the ICO, shifting the frequency in the direction which causes the input and ICO to have a 90° phase relationship.

The oscillator is a current-controlled multivibrator. The current control affects the charge/discharge rate of the timing capacitor. It is common for this type of oscillator to be referred to as a voltage-controlled oscillator (VCO), because the output of the phase comparator and the loop filter is a voltage. To control the frequency of an integrated ICO multivibrator, the control signal must be conditioned by a voltage-to-current converter. In the NE568A, special circuitry predistorts the control signal to make the change in frequency a linear function over a large control-voltage range.

The free-running frequency of the oscillator depend on the value of the timing capacitor connected between Pins 4 and 5. The value of the timing capacitor depends on internal resistive components and current sources. When $R_2 = 1.2k\Omega$ and $R_4 = 0\Omega$, a very close approximation of the correct capacitor value is:

$$C^* = \frac{0.0014}{f_O} F$$

where

$$C^* = C_2 + C_{STRAY}$$

The temperature-compensation resistor, R_4, affects the actual value of capacitance. This equation is normalized to 70MHz. See 8 for correction factors.

The loop filter determines the dynamic characteristics of the loop. In most PLLs, the phase detector outputs are internally connected to the ICO inputs. The NE568A was designed with filter output to input

connections from Pins 20 (ϕ DET) to 17 (ICO), and Pins 19 (ϕ DET) to 18 (ICO) external. This allows the use of both series and shunt loop-filter elements. The loop constratints are:

K_D = 0.12V/Radian (Phase Detector Constant

$$K_D = 4.2 \cdot 10^9 \frac{\text{Radians}}{V_{-sec}} \text{ (ICO Constant)}$$

The loop filter determines the general characteristics of the loop. Capacitors C_9, C_{10}, and resistor R_1, control the transient output of the phase detector. Capacitor C_9 suppresses 70MHz feedthrough by interaction with 100Ω load resistors internal to the phase detector.

$$C_9 = \frac{1}{2\pi\ (50)\ (f_O)}\ F$$

At 70MHz, the calculated value is 45pF. Empirical results with the test and application board were improved when a 47pF capacitor was used.

The natural frequency for the loop filter is set by C_{10} and R_1. If the center frequency of the loop is 70MHz and the full demodulated bandwidth is desired, i.e., $f_{BW} = f_O/7 = 10MHz$, and a value for R_1 is chosen, the value of C_{10} can be calculated.

$$C_{10} = \frac{1}{2\pi\ R_1\ f_{BW}}\ F$$

PARTS LIST AND LAYOUT 40MHz APPLICATION NE568AD

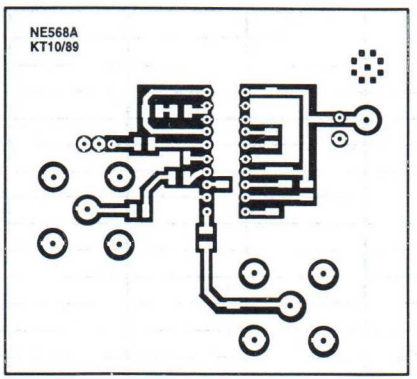
C_1	100nF	±10%	Ceramic chip	1206
C_2[1]	18pF	±2%	Ceramic chip	0805
C_2[2]	16pF	±2%	Ceramic ORChip	
C_3	100nF	±10%	Ceramic chip	1206
C_4	100nF	±10%	Ceramic chip	1206
C_5	6.8µF	±10%	Tantalum	35V
C_6	100nF	±10%	Ceramic chip	1206
C_7	100nF	±10%	Ceramic chip	1206
C_8	100nF	±10%	Ceramic chip	1206
C_9	47pF	±2%	Ceramic chip	0805 or 1206
C_{10}	560pF	±2%	Ceramic chip	0805 or 1206
C_{11}	47pF	±2%	Ceramic chip	0805 or 1206
C_{12}	100nF	±10%	Ceramic chip	1206
C_{13}	100nF	±10%	Ceramic chip	1206
R_1	27Ω	±10%	Chip CR32	1/4W
R_2	1.2kΩ		Trim pot	
R_3[3]	43Ω	±10%	Chip CR32	1/4W
R_4[4]	3.9kΩ	±10%	Chip CR32	1/4W
R_5[3]	50Ω	±10%	Chip CR32	1/4W
RFC_1[5]	10µH	±10%	Surface mount	
RFC_2[5]	10µH	±10%	Surface mount	

NOTES:
1. 18pF with Pin 12 ground and Pin 13 no connect (open).
2. $C_2 + C_{STRAY}$ = 16pF for temperature-compensated configuration with R_4 = 3.9kΩ.
3. For 50Ω setup. R_1 = 62Ω, R_3 = 75Ω for 75Ω application.
4. For test configuration R_4 = 0Ω (GND) and C_2 = 18pF.
5. 0Ω chip resistors (jumpers) may be substituted with minor degradation of performance.

PARTS LIST AND LAYOUT 70MHz APPLICATION NE568AN

C_1	100nF	±10%	Ceramic chip	50V
C_2[1]	18pF	±2%	Ceramic chip	50V
C_2[2]	16pF	±2%	Ceramic chip	0805
C_3	100nF	±10%	Ceramic chip	50V
C_4	100nF	±10%	Ceramic chip	50V
C_5	6.8µF	±10%	Tantalum	35V
C_6	100nF	±10%	Ceramic chip	50V
C_7	100nF	±10%	Ceramic chip	50V
C_8	100nF	±10%	Ceramic chip	50V
C_9	47pF	±2%	Ceramic chip	50V
C_{10}	560pF	±2%	Ceramic chip	50V
C_{11}	47pF	±2%	Ceramic chip	50V
C_{12}	100nF	±10%	Ceramic chip	50V
C_{13}	100nF	±10%	Ceramic chip	50V
R_1	27Ω	±10%	Ceramic chip CR32	1/4W
R_2	1.2kΩ		Trim pot	
R_3[3]	43Ω	±10%	Ceramic chip CR32	1/4W
R_4[4]	3.9kΩ	±10%	Ceramic chip CR32	1/4W
R_5[3]	50Ω	±10%	Ceramic chip CR32	1/4W
RFC_1	10µH	±10%	Surface mount	
RFC_2	10µH	±10%	Surface mount	

NOTES:
1. 18pF with Pin 12 ground and Pin 13 no connect (open).
2. $C_2 + C_{STRAY} = 16pF$ for temperature-compensated configuration with $R_4 = 3.9k\Omega$.
3. For 50Ω setup. $R_1 = 62\Omega$, $R_3 = 75\Omega$ for 75Ω application.
4. For test configuration $R_4 = 0\Omega$ (GND) and $C_2 = 18pF$.



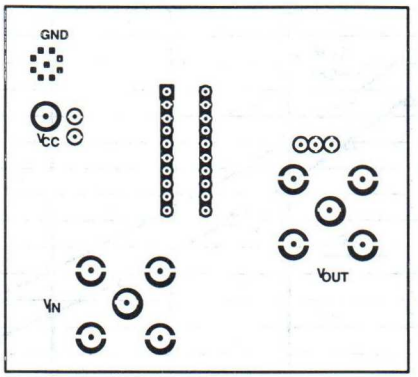
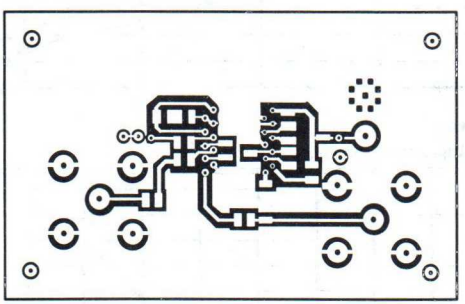


Figure 2. N Package Layout (Not Actual Size)



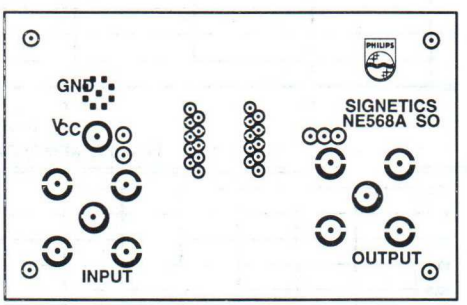


Figure 3. D Package Layout (Not Actual Size)

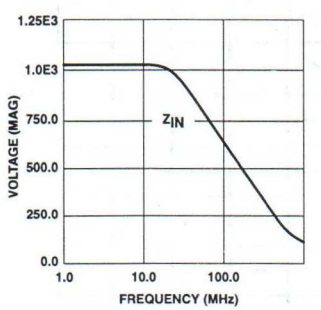


Figure 4. NE568A Input Impedance With CP = 0.5pF 20-Pin SO Package

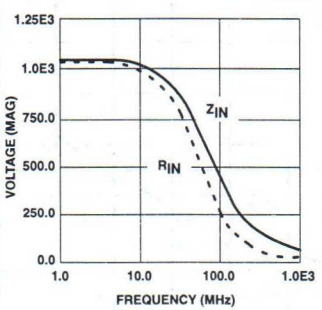


Figure 5. NE568A Input Impedance With CP = 1.49pF 20-Pin Dual In-Line Plastic Package

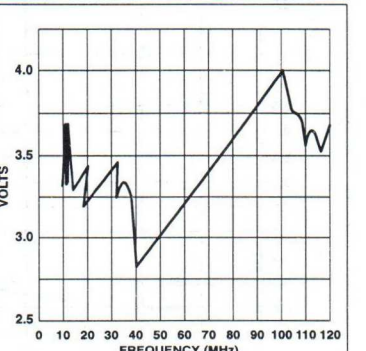


Figure 6. Typical Output Linearity

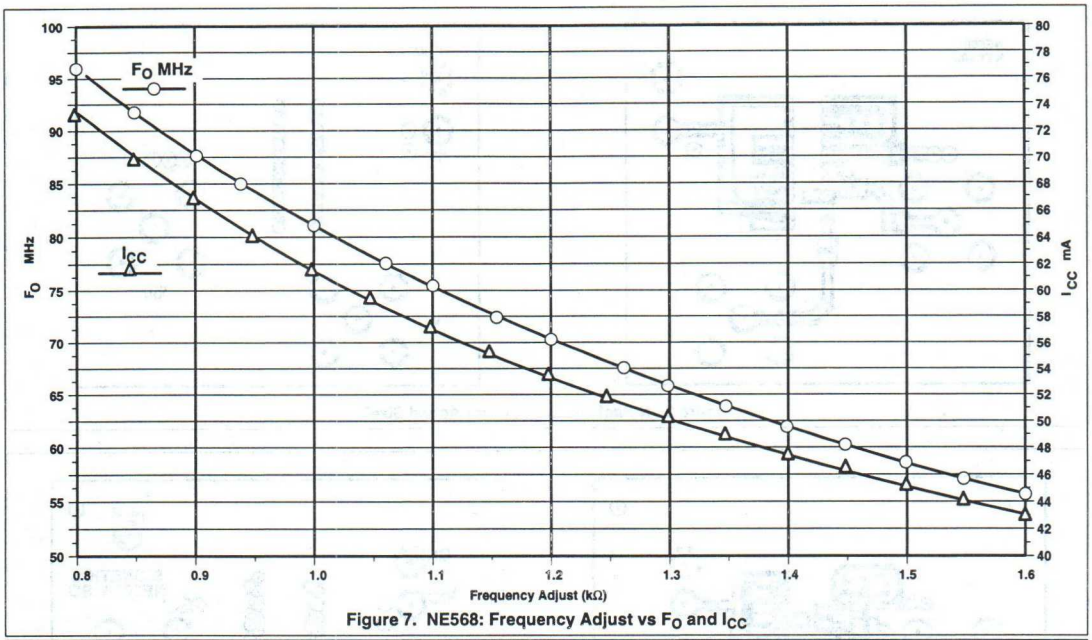


Figure 7. NE568: Frequency Adjust vs F_O and I_{CC}

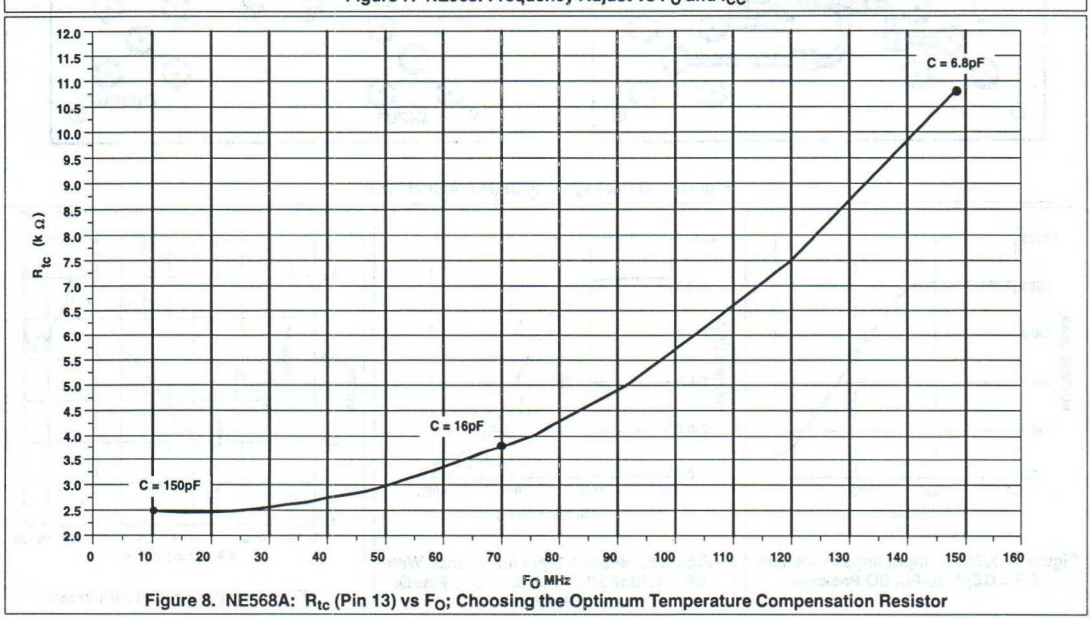


Figure 8. NE568A: R_{tc} (Pin 13) vs F_O; Choosing the Optimum Temperature Compensation Resistor

An overview of the phase-locked loop (PLL)

AN177

Portions of this Phase-Locked Loop section were edited by Dr. J. A. Connelly

INTRODUCTION

The basic phase-locked loop (PLL) concept has been known and widely utilized since first being proposed in 1922. Since that time, PLLs have been used in instrumentation, space telemetry, and many other applications requiring a high degree of noise immunity and narrow bandwidth. Techniques and systems involved in these applications frequently are quite complex, requiring a high degree of sophistication. Many of the PLL applications have been at microwave frequencies and employ complex phase shifters, signal splitters, modulation, and demodulation schemes such as bi-phase and quadra-phase. Because of the high frequencies involved in microwave applications, most all components of these PLL systems are made from discrete as opposed to integrated circuits. However, in other communication system applications such as FSK and FM and AM demodulation where frequencies are below approximately 100MHz, monolithic PLLs have found wide application because of their low cost versus high performance.

A block diagram representation of a PLL is shown in Figure 1. Phase-locked loops operate by producing an oscillator frequency to match the frequency of an input signal, fl. In this locked condition, any slight change in fl first appears as a change in phase between fl and the oscillator frequency. This phase shift then acts as an error signal to change the frequency of the local PLL oscillator to match fl. The locking onto a phase relationship between fl and the local oscillator accounts for the name phase-locked loop.

A MECHANICAL ANALOG TO THE PLL

To better visualize the frequency and phase relationships in a PLL, consider the mechanical system shown in Figure 2 which is a dual to the electronic PLL. This mechanical system has two identical, heavy disks with two separate center shafts attached to each disk. Each shaft is presumed to be mounted on a bearing that allows each massive disk to be rotated in either direction when some external force is applied. The shafts are coupled together by a spring whose end points are fixed to each shaft. This spring can be twisted in either direction, depending upon the relative positions of the shafts. The spring cannot "kink up" due to the shafts passing through the center of the spring.

Now suppose the sequence of events shown in Figure 3 occurs to the mechanical system. The disks are simply represented like clock faces with positional reference markers. Initially, both disks are stationary in a neutral position. Then the left disk, or input, is advanced slowly clockwise through an angle ~~ position. The right disk, or output, initially doesn't move as the spring begins to tighten. As the input continues to move and when it reaches ~2. begins to turn and tracks the input with a positional phase shift error of ~e = ~2 (l)

At any point in time, with both disks slowly turning at the same speed, there will be some inherent phase error between the disks, or ~e = ~3 ~4 (2)

This positional phase error in the mechanical system is analogous to the phase error in the electronic PLL. When the input disk coasts to a stop, the output also gradually comes to a stop with a fixed phase error equal to that in Equation 2 or ~e = ~s ~6 = ~3 ~4 (3)

The spring has a residual stored twist in one direction due to ~e

Now consider that the disks are first returned to their neutral positions. Then the input disk is instantaneously rotated through an angle of ~l as shown in Figure 4. The output disk can't respond instantaneously because of its large mass. It doesn't move instantaneously and the spring develops considerable torque. Then, as shown in the sequence of events in Figure 4, the output disk begins accelerating after some delay due to the large phase error. It swings past the stopped position of the input disk due to its momentum, reaches a peak overshoot, and gradually oscillates about ~~ with a damped response, finally coming to rest with some small residual phase error. The input twist of ~1 represents the application of a step of position or phase to the system, and the response of the output disk is typical for a second-order, underdamped system. This same type of secondorder behavior occurs in the PLL system for an instantaneous change of input phase.

As a final example, consider the events in Figure 5 where both disks are rotating at a constant rate. Applying a strobing light (strobotac) simultaneously to both disks and adjusting its flashing rate to one flash per disk rotation will cause the positional markers to appear stationary. There will be a constant phase error in this case just as there was in Figure 3. Now suppose the revolution rate of the input disk gradually increases by a small amount to a new rate. The positional marker will appear to walk around the disk. The output first senses the increased rate of the input through an increase in the phase error.

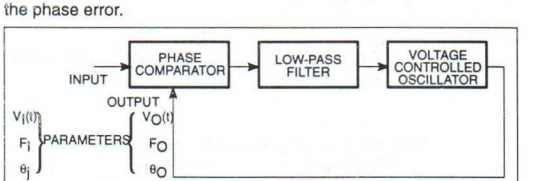


Figure 1. Block Diagram of a Phase-Locked Loop

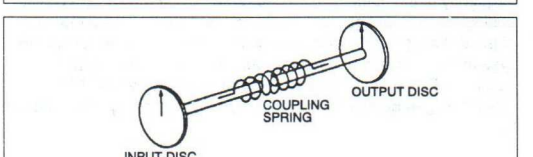


Figure 2. Mechanic Analog to PLL

Then, after some delay, the rate of the output gradually increases to track the input. Both positional markers appear to be walking around each disk at the same rate until the strobotac is adjusted for the higher input and output rate. Then the strobe light again freezes the markers, producing a phase error at this higher rate that is larger than before the input rate was increased. This gradual increase in the input rate to the mechanical system simulates a ramp change in the input frequency to the PLL system. The response to the output disk simulates the behavior of the oscillator in the PLL.

If the rate of the input disk is alternately increased and decreased by some small amount compared to the nominal revolution rate, the positional markers will appear to walk both clockwise and counter clockwise, momentarily appearing stationary when the strobing light rate equals the disk revolution rate. This "walking" represents a changing phase error which is occurring at the modulation rate. Thus the phase error can be thought of as a useable demodulated output signal.

The disk-spring mechanical system is a helpful analog for visualizing frequency, phase, transient, and steady-state responses in the electronic phase-locked loop system. In this example, the positions of the disk marker and rotation rates are analogous to phase and

frequency in the electronic PLL system. The spring acts as a phase comparator to constantly sense the relative positions or phases of the disks. The torque developed in this spring acts as the driving force or input signal to turn the second disk.

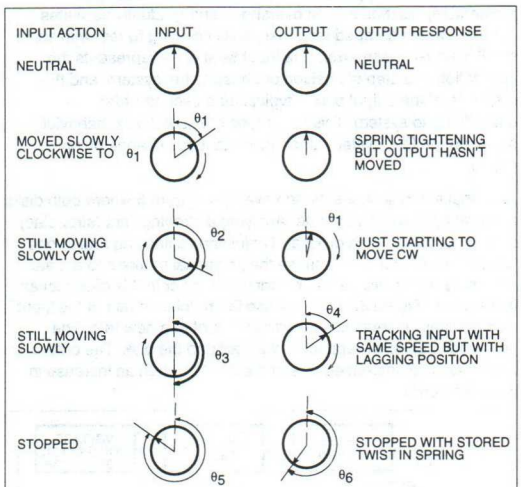


Figure 3. Disk Sequence Showing Output Tracking Input With Phase Error

Thus the spring torque simulates a voltage which controls the rate or frequency of the output disk or oscillator. Hence the second disk is analogous to a voltage-controlled oscillator (VCO). The large mass of the disks together with their angular momentum slows down the systems response time and simulates a low-pass filter in the electronic PLL system. This describes the lagging of the VCO free-running frequency to the input signal in an analog phase-locked loop.

EXAMPLES OF PLL APPLICATIONS

Now consider the action of the voltagecontrolled oscillator, phase comparator and low pass filter in the PLL. The VCO generates a signal that is periodic. Normally, the rate or frequency of the VCO is primarily determined by the value of a capacitance connected to this oscillator. This action of starting the VCO running by itself is analogous to disconnecting the spring from one of the shafts in the mechanical system and starting the output disk rotating at a constant rate through some external means such as a motor. In the PLL system this frequency is called the oscillator's free running frequency, (f_O'), because it occurs when the system is unlocked and there is no coupling between input and output frequencies. With the PLL, the VCO frequency can be shifted above and below f_O' by applying a voltage to the optional fine tune input.This signal generator property is just one of the many uses of the PLL. Specifically with integrated circuit PLLs, frequency ranges from less than 1.0Hz to more than 50MHz can be produced just by selecting the right value of capacitance from a chart on the data sheet.

Selecting f_O' and then changing it by a control voltage makes the VCO well suited for converting digital data that is represented by two different voltage levels into two different frequencies. A "I" voltage level can be related to a frequency called a mark, and an "0" level to a frequency called a space. This technique, called frequency shift keying, or (FSK), is typical of data being transmitted over telephone and radio links where it is impractical to use DC voltage level shifts. Essentially this is what a modem (modulator-demodulator) does as it converts data to tones to 90 out of the system into a transmission link. Then it reverses the process and converts received tones to "1"s and "0"s at the receiver for the system to use. Sometimes confusion arises because different names are used for the same thing. For example,

A shift up in frequency = "1" = Mark

A shift down in frequency = "0" = Space

NOTE: Some oscillators have frequencies controlled by an input current rather than a voltage and are retoned to as current-controlled oscillators (CCO).

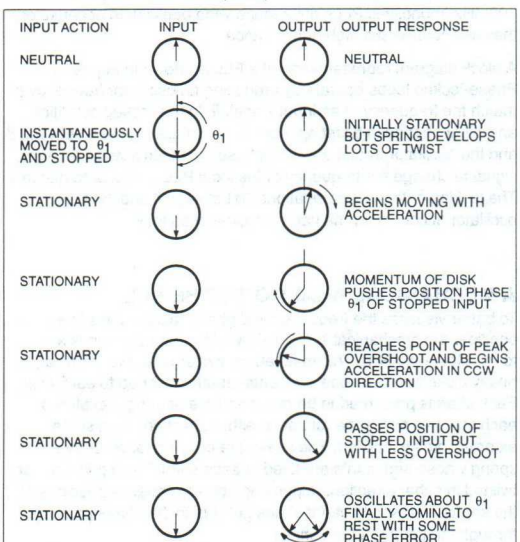


Figure 4. Disk Sequence Showing Output Response to a Sudden Position Input

If voice or music is applied to the VCO instead of digital data, the oscillator's frequency will move or modulate with the voice or music. This is frequency modulation (FM) and is simply moving the frequency in relation to some input voltage which represents intelligence. Of course, as in the modem case, the process has to be reversed and the PLL can do this also. The PLL is a complete working system that can be used to send and receive signals. In fact the PLL can create the signal, or select a signal, decode it and reproduce it. Now let's look at how this works.

The VCO is connected to a section where its frequency is put together with an incoming signal or signals. In a radio this is known as a "mixer" where signals are mixed together. In a PLL it is usually called a Phase Comparator Other names for this function are phase detector or multiplier — either analog or digital. (Differences between analog and digital phase comparators will be explained later in this chapter.) The purpose of this phase comparator is to produce an output which represents how far the VCO frequency is from that of the incoming signal. Comparing these frequencies and producing an error signal proportional to their difference allows the VCO frequency to shift from f_O' and become the same frequency as

the input signal. This is exactly what happens with the VCO frequency — first "capturing" the input frequency, and then locking onto it. A similar type of action can be visualized in the mechanical system by having the coupling spring disconnected at one end with the two disks rotating at different rates. When their rotation rates are approximately equal, the spring is suddenly connected, and the output disk's speed will gradually become equal to and track the inputs rate as in Figure S.

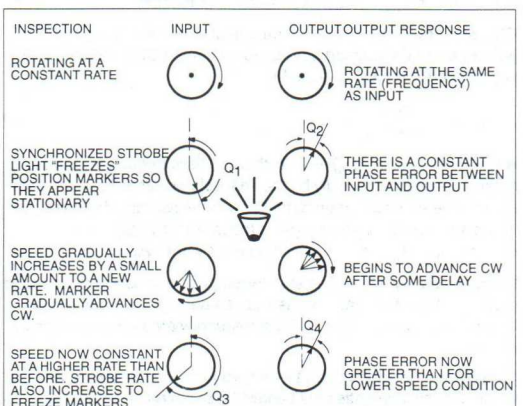


Figure 5. Disk Sequence Showing Output Behavior Due to Changes In Input Speed

When the VCO shifts frequency and locks to the input, the signal frequency is duplicated. If the input signal contains static or noise, the VCO output will be an exact reproduction of the signal frequency without the static or noise. Thus the PLL has accomplished signal reconditioning or reconstitution.

The error signal used to keep the VCO exactly synchronized with an incoming signal can be amplified, filtered, and used to "clock" the signal or give synchronizing information necessary to look at the signal. For example, in some digital memories and transmission systems, data are stored in a code and looked at or strobed at a rate which must be synchronized to the data. This strobing may be at twice or one-half the data rate. By setting f_O' equal to twice or one-half the data rate, the PLL will lock to the data and give an exact synchronized clock. This shows another application of the PLL for multiplying or dividing frequencies.

PLLs can separate a signal of one frequency from among many others as, for example, is done in television and radio reception. This 1 selectivity or capture range is controlled in 2 the PLL by the low-pass filter (LPF) which 3 allows the PLL to only see signals close to the frequency of interest. The time constant 4 of the LPF is set easily by the selection of a S. resistor and capacitor network. This network determines how far away in frequency an 6 input signal can be from f_O' and still permit the PLL to respond and capture. Once locking is activated, the PLL system will continue to track the input frequency unless the instantaneous phase error exceeds the system's capability.

The error signal which drives the VCO and keeps the system locked is a usable output. In the FSK example the oscillator's frequency is shifted with each "I" or "O" digital input. Converting these frequency shifts back to the "I" and "O" signals automatically occurs in a PLL because a mark input generates an error signal to move the VCO up to that frequency. When the mark changes to a space, the error signal jumps suddenly down, forcing the VCO to follow. The error signal then is exactly the data that generated the FSK signals. A PLL for fSK can convert data to tones for transmission to a remote point. Then another PLL can reconvert the data tones back to voltage levels, all without tuned circuits.

The PLL system decodes FM signals in a similar way. The frequency variations caused by voltages from a microphone into one VCO serve as the input signal to another PLL, which reverses the action since the error signal driving the second PLL's VCO is exactly the same as the original microphone voltage.

Decoding of an amplitude-modulated (AM) input signal is another application of the PLL. This application is more involved than FM demodulation because a phase shift network, a second-phase comparator, and another low-pass filter are required. This application is discussed in detail later. However, it should be pointed out that AM demodulation with PLLs offers improved system linearity than the more commonly employed technique of nonlinear diode detection. Tone decoding is a special case of AM demodulation. When performed with PLLs, the second-phase comparator is called a quadrature-phase detector (—PD). The —PD produces a maximum output error voltage whenever the input and oscillator frequencies are locked to the free-running frequency, f_O', unlike the regular phase comparator which has a nominal zero error voltage under this same condition.

These application examples show that with the PLL, a system can: Generate a signal ~. Modulate a signal (encode)

Select a signal from among many, Demodulate (decode) Recreate (reconstitute) a signal frequency with reduced noise Multiply and divide frequency.

TYPES OF PLLS

Generally speaking, the monolithic PLLs can be classified into two groups — digital and analog. While both perform as PLLs, the digital circuits are more suitable for synchronization of digital signals, clock recovery from encoded digital data streams, and other digital applications. Analog monolithic PLLs are used quite extensively in communication systems since they maintain linear relationships between input and output quantities.

The phase comparator is perhaps the most important part of the PLL system since it is here that the input and VCO frequencies are simultaneously compared. Some digital PLLs employ a two-input Exclusive-OR gate as the phase comparator. When the digital loop is locked to f_O', there is an inherent phase error of 90! that is represented by asymmetry in the output waveform. Also, the phase comparator's output has a frequency component of twice the reference frequency. Because of the large logic voltage swings in digital systems, extensive filtering must be performed to remove the harmonic frequencies. For this reason, other types of digital phase comparators achieve locking by synchronizing the "edges" of the input and VCO frequency waveshapes. The phase comparator produces an error voltage that is proportional to the time difference between the edges; i.e., the phase error. This edge-triggering technique for the phase comparator produces lower output noise than with the ExclusiveOR approach. However, time line, on the input and VCO frequencies is translated into phase error line, that may require additional filtering within the loop.

Triggering on the edges of digital signals means that only frequency (or period) is important and not duty cycle. This is a key consideration in PLL applications utilizing counters where waveshapes usually aren't symmetrical; i.e., 50% duty cycle. For the

TTL family, it is easier to provide the edge matching function on the falling edges ("I" to "O") transition of the waveform. CMOS, 12L, and ECL are better suited for leading edge triggering ("O" to "1").

Analog PLLs utilize a phase comparator which functions as a four-quadrant analog multiplier to mix the input and VCO signals. Since this mixing is true analog multiplication, the phase comparator's output is a function of input and VCO signal amplitudes, frequencies, phase relationships, and duty cycles. The inherent linearity afforded by this analog multiplication makes the monolithic analog PLL well suited for many general purpose and communication system applications.

Another way of distinguishing between digital and analog phase comparators is by thinking of the similarities and differences between voltage comparators and operational amplifiers. Voltage comparators are specially designed for digital applications where response time between output levels has been minimized at the expense of system linearity. Feedback is seldom used to maintain linear system relationships, with the comparator normally running open-loop. Op amps, on the other hand, are designed for a linear inputoutput relationship, with negative feedback being employed to further improve the system linearity.

PLL TERMINOLOGY

The following is a brief glossary of frequently encountered terms in PLL literature.

Free-running Frequency (f_O', ω_O') — Also called the center frequency, this is the frequency at which the loop VCO operates when not locked to an input signal. The "prime" superscripts are used to distinguish the free-running frequency from f_O and ω_O which are used for the general oscillator frequency. (Many references use f_O and ω_O for both the free-running and general oscillator frequency and leave the proper choice for the reader to infer from the context.) The appropriate units for f_O' and ω_O' are Hz and radians per second, respectively.

Lock Range ($2f_L$, $2\omega_L$)* — The range of frequencies over which the loop will remain in lock. Normally the lock range is centered at the free-running frequency, unless there is some nonlinearity in the system which limits the frequency deviation on one side of f_O'. The deviations from f_O' are referred to as the *Tracking Range or Hold-in Range*. (See Figure 6). The tracking range is therefore one-half of the lock range.

Capture Range ($2f_C$, $2\omega_C$)** — Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes because of the selectivity afforded by the low-pass filter. The capture range also is centered at f_O' with the equal deviations called the *Lock-in* or *Pull-in Ranges. The capture range can never exceed the lock range.*

Lock-up Time (t_L)*** — The transient time required for a free-running loop to lock. This time depends principally upon the bandwidth selectivity designed into the loop with the lowpass filter. *The lock-up time is inversely proportional to the selectivity bandwidth.* Also, lock-up time exhibits a statistical spreading due to random initial phase relationships between the input and oscillator phases.

Phase Comparator Conversion Gain (K_d) — The conversion constant relating the phase comparator's output voltage to the phase difference between input and VCO signals when the loop is locked. At low input signal levels, K_d is also a function of signal amplitude. K_d has units of volts per radian (V/ rad).

VCO Conversion Gain (K_O) — The conversion constant relating the oscillator's frequency shift from f_O' to the applied input voltage. K_O has units of radians per second per volt (rad/sec/V). K_O is a linear function of ω_O' and must be obtained using a formula or graph provided or experimentally measured at the desired ω_O'.

Loop Gain (K_V) — The product of K_d, K_O, and the low-pass filters gain at DC. K_d is evaluated at the appropriate input signal level and K_O at the appropriate ω_O'. K_V has units of $(sec)^{-1}$.

Closed-Loop Gain (CLG) — The output signal frequency and phase can be determined from a product of the CLG and the input signal where the CLG is given by

$$CLG = \frac{K_V}{1 + K_V} \qquad (4)$$

Natural Frequency (ω_n) — The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane or determined experimentally as the modulation frequency for which an underdamped loop gives the maximum frequency deviation from f_O' and at which the phase error swing is the greatest.

Damping Factor (ζ) — The standard damping constant of a second order feedback system. For the PLL, ζ refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.

Loop Noise Bandwidth (B_L) — A loop property relating ω_n and ζ which describes the effective bandwidth of the received signal. Noise and signal components outside this bandwidth are greatly attenuated.

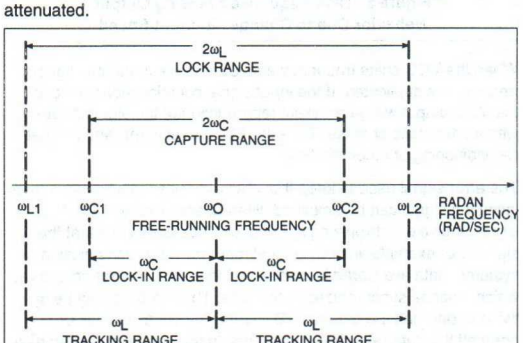


Figure 6. Lock and Capture Range Relationships

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NOTES:

*Also called Synchronization Range.

**Also called Acquisition Range.

***Also called Acquisition Time.

Modeling the PLL

AN178

INTRODUCTION

The phase-locked loop is a feedback system comprised of a phase comparator, a low-pass filter and an error amplifier in the forward signal path and a voltage-controlled oscillator (VCO) in the feedback path. The block diagram of a basic PLL system is shown in Figure 1. Perhaps the single most important point to realize when designing with the PLL is that it is a feedback system and, hence, is characterized mathematically by the same equations that apply to other, more conventional feedback systems. However, the parameters in the equations are somewhat different since the feedback error signal in the phase locked system is a phase rather than a current or voltage signal, as is usually the case in conventional feedback systems.

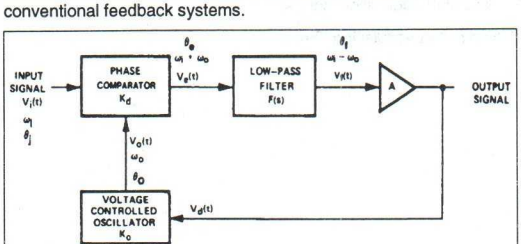


Figure 1. Block Diagram of Phase-Locked Loop

PHASE-LOCKED LOOP OPERATION

The basic principle of the PLL operation can be briefly explained as follows:

With no signal input applied to the system, the VCO control voltage $V_d(t)$ is equal to zero. The VCO operates at a set frequency, f_O' (or the equivalent radian frequency ω_O') which is known as the free-running frequency. When an input signal is applied to the system, the phase comparator compares the phase and the frequency of the input with the VCO frequency and generates an error voltage $V_e(t)$ that is related to the phase and the frequency diHerence between the two signals. This error voltage is then filtered, amplified, and applied to the control terminal of the VCO. In this manner, the control voltage $V_d(t)$ forces the VCO frequency to vary in a direction that reduces the frequency difference between ω_O and the input signal. If the input frequency ω_I is sufficiently close to ω_O, the feedback nature of the PLL causes the VCO to synchronize or lock with the incoming signal. Once in lock, the VCO frequency is identical to the input signal except for a finite phase difference.

This net phase difference of θ_e where

$$\theta_e = \theta_o - \theta_i \qquad (1)$$

is necessary to generate the corrective error voltage V_d to shift the VCO frequency from its free-running value to the input signal frequency ω_I and thus keep the PLL in lock. This selfcorrecting ability of the system also allows the PLL to track the frequency changes of the input signal once it is locked. The range of frequencies over which the PLL can maintain lock with an input signal is defined as the "lock range" of the system. The band of frequencies over which the PLL can acquire lock with an incoming signal is known as the "capture range" of the system and is never greater than the lock range.

Another means of describing the operation of the PLL is to observe that the phase comparator is in actuality a multiplier circuit that mixes the input signal with the VCO signal. This mix produces the sum and difference frequencies $\omega_I \pm \omega_O$ shown in Figure 1. When the loop is in lock, the VCO duplicates the input frequency so that the difference frequency component ($(\omega_I \times \omega_O)$ is zero; hence, the output of the phase comparator contains only a DC component. The low-pass filter removes the sum frequency component ($\omega_I + \omega_O$) but passes the DC component which is then amplified and fed back to the VCO. Notice that when the loop is in lock, the difference frequency component is always DC, so the lock range is independent of the band edge of the low-pass filter.

LOCK AND CAPTURE

Consider now the case where the loop is not yet in lock. The phase comparator again mixes the input and VCO signals to produce sum and difference frequency components. However, the difference component may fall outside the band edge of the low-pass filter and be removed along with the sum frequency component. If this is the case, no information is transmitted around the loop and the VCO remains at its initial free-running frequency. As the input frequency approaches that of the VCO, the frequency of the difference component decreases and approaches the band edge of the low-pass filter. Now some of the difference component is passed, which tends to drive the VCO towards the frequency of the input signal. This, in turn, decreases the frequency of the difference component and allows more information to be transmitted through the low-pass filter to the VCO. This is essentially a positive feedback mechanism which causes the VCO to snap into lock with the input signal. With this mechanism in mind, the term "capture range" can again be defined as 'the frequency range centered about the VCO initial free-running frequency over which the loop can acquire lock with the input signal'. The capture range is a measure of how close the input signal must be in frequency to that of the VCO to acquire lock. The "capture range" can assume any value within the lock range and depends primarily upon the band edge of the low-pass filter together with the closed-loop gain of the system. It is this signal capturing phenomenon which gives the loop its frequency-selective properties.

It is important to distinguish the "capture range" from the "lock range" which can, again, be defined as 'the frequency range usually centered about the VCO initial free–running frequency over which the loop can track the input signal once lock has been achieved'.

When the loop is in lock, the difference frequency component at the output of the phase comparator (error voltage) is DC and will always be passed by the low-pass filter. Thus, the lock range is limited by the range of error voltage that can be generated and the corresponding VCO frequency deviation produced. The lock range is essentially a DC parameter and is not affected by the band edge of the low-pass filter.

THE CAPTURE TRANSIENT

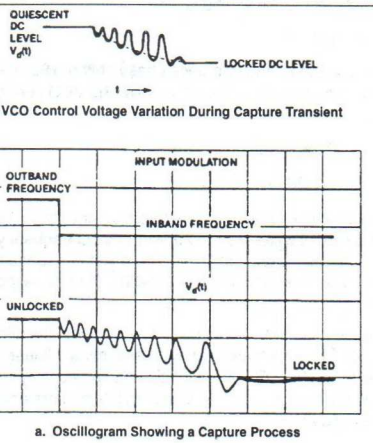
The capture process is highly complex and does not lend itself to simple mathematical analysis. However, a qualitative description of the capture mechanism may be given as follows. Since frequency is the time derivative of phase, the frequency and the phase errors in the loop can be related as

$$\Delta\omega = \frac{d\theta_e}{d_t} \qquad (2)$$

where $\Delta\omega$ is the instantaneous frequency separation between the signal and VCO frequencies and θ_e is the phase difference between the input signal and VCO signals.

If the feedback loop of the PLL were opened between the low-pass filter and the VCO control input, then for a given condition of ω_O and

ω_I the phase comparator output would be a sinusoidal beat note at a fixed frequency $\Delta\omega$. If ω_I and ω_O were sufficiently close in frequency, this beat note would appear at the filter output with negligible anenuation.



a. VCO Control Voltage Variation During Capture Transient

a. Oscillogram Showing a Capture Process

Figure 2. Asynchronous Error Beat Frequency During the Capture Transient

Now suppose that the feedback loop is closed by connecting the low-pass filter output to the VCO control terminal. The VCO frequency will be modulated by the beat note. When this happens, $\Delta\omega$ itself will become a function of time. If, during this modulation process, the VCO frequency moves closer to

$$\omega_I, \text{ (i.e., decreasing } \Delta\omega), \text{ then } \frac{d\theta_e}{dt} \text{ decreases}$$

and the output of the phase comparator becomes a slowly varying function of time. Similarly, if the VCO is modulated away from

$$\omega_I, \frac{d\theta_e}{dt} \text{ increases and the error voltage}$$

becomes a rapidly varying function of time. Under this condition the beat note waveform no longer looks sinusoidal; it looks like a series of aperiodic cusps, depicted schematically in Figure 2a. Because of its asymmetry, the beat note waveform contains a finite DC component that pushes the average value of the VCO toward ω_I and lock is established. When the system is in lock, $\Delta\omega$ is equal to zero and only a steady-state DC error voltage remains.

Figure 2b displays an oscillogram of the loop error voltage $V_d(t)$ in an actual PLL system during the capture process. Note that as lock is approached, $\Delta\omega$ is reduced, the low-pass filter anenuation becomes less, and the amplitude of the beat note increases.

The total time taken by the PLL to establish lock is called the *pull-in time*. Pull-in time depends on the initial frequency and phase differences between the two signals as well as on the overall loop gain and the low-pass filter bandwidth. Under certain conditions, the pull-in time may be shorter than the period of the beat note and the loop can lock without an oscillatory error transient.

A specific case to illustrate this is shown in Figure 3. The 565 PLL is shown acquiring lock within the first cycle of the input signal. The PLL was able to capture in this short time because it was operated as a first-order loop (no low-pass filter) and the input tone-burst frequency was within its lock and capture range.

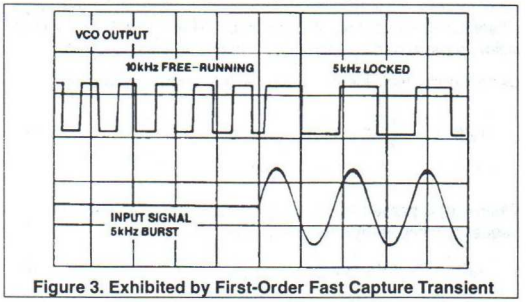


Figure 3. Exhibited by First-Order Fast Capture Transient

EFFECT OF THE LOW-PASS FILTER

In the operation of the loop, the low-pass filter serves a dual function.

First, by anenuating the high frequency error components at the output of the phase comparator, it enhances the interference-rejection characteristics; second, it provides a short-term memory for the PLL and ensures a rapid recapture of the signal if the system is thrown out of lock due to a noise transient. Decreasing the low-pass filter bandwidth has the following effects on system performance (Long Time Constant):

a. The capture process becomes slower, and the pull-in time increases.

b. The capture range decreases.

c. Interference-rejection properties of the PLL improve since the error voltage caused by an interfering frequency is attenuated further by the low-pass filter.

d. The transient response of the loop (the response of the PLL to sudden changes of the input frequency within the capture range) becomes underdamped.

The last effect also produces a practical limitation on the low-pass loop filter bandwidth and roll-off characteristics from a stability standpoint. These points will be explained further in the following analysis.

MATHEMATICALLY DEFINING PLL OPERATION

As mentioned previously, the phase comparator is basically an analog multiplier that forms the product of an RF input signal, $V_i(t)$, and the output signal, $v_o(t)$, from the VCO. Refer to Figure 1 and assume that the two signals to be multiplied can be described by

$$V_i(t) = V_I \sin \omega_I t \quad (3)$$

$$V_o(t) = V_O \sin (\omega_O t + \theta_e) \quad (4)$$

where ω_I, ω_O, and θ_e are the frequency and phase difference (or phase error) characteristics of interest. The product of these two signals is an output voltage given by

$$V_e(t) = K_1 V_I V_O (\sin\omega_I t)\,[\text{sine}(\omega_O t + \theta_e)] \quad (5)$$

where K_1 is an appropriate dimensional constant. Note that the amplitude of $v_e(t)$ is directly proportional to the amplitude of the input signal V_I. The two cases of an unlocked loop ($\omega_I \neq \omega_O$) and of a locked loop ($\omega_I = \omega_O$) are now considered separately.

Modeling the PLL

AN178

Unlocked State ($\omega_I \neq \omega_O$)
When the two frequencies to the phase comparator are not synchronized, the loop is not locked. Furthermore, the phase angle difference θ_e in Equations 4 and 5 is meaningless lor this case since it can be eliminated by appropriately choosing the time origin.

Using trigonometric identities, Equation 5 can be rewritten as

$$v_e(t) = \frac{K_1 V_I V_O}{2} [\cos(\omega_I - \omega_O)t - \cos(\omega_I + \omega_O)t] \quad (6)$$

When $v_e(t)$ is passed through the low-pass filter, F(s), the sum frequency component is removed, leaving

$$v_f(t) = K_2 V_I V_O \cos(\omega_I - \omega_O)t \quad (7)$$

where K_2 is a constant. After amplification, the control voltage for the VCO appears as

$$v_d(t) = AK_2 V_I V_O \cos(\omega_I - \omega_O)t \quad (8)$$

This equation shows that a beat frequency effect is established between ω_I and ω_O, causing the VCO's frequency to deviate by $\pm\Delta\omega$ from ω_O' in proportion to the signal amplitude ($AK_2V_IV_O$) passing through the filter. If the amplitude of V_I is sufficiently large and if signal limiting or saturation does not occur, the VCO output frequency will be shifted from ω_O' by some $\Delta\omega$ until lock is established where

$$\omega_I = \omega_O = \omega_O' \pm \Delta\omega \quad (9)$$

If lock cannot be established, then either V_I is too small to drive the VCO to produce the necessary $\pm\Delta\omega$ deviation or ω_I is beyond the dynamic range of the VCO, i.e., $\omega_I >< \omega_O' \pm\Delta\omega$. Remedies for these no lock conditions are:

1. Increase VI either internally or externally to the loop by providing additional amplification.
2. Increase the internal loop gain by adjusting upward (larger -3dB frequency) the response of the low-pass filter.
3. Shift ω_O' closer to the expected ω_I. Establishing frequency lock leads to the second case where $\omega_I = \omega_O$.

Locked State ($\omega_I = \omega_O$)
When ω_I and ω_O are frequency synchronized, the output signal from the phase comparator for $\omega_I = \omega_O = \omega$ and a phase shift of θ_e is

$$v_e(t) = K_1 V_I V_O(\sin\omega t)\sin(\omega t + \theta_e) = \frac{K_1 V_I V_O}{2}[\cos\theta_e - \cos(2\omega t + \theta_e)] \quad (10)$$

The low-pass filter removes the high frequency, AC component of $v_e(t)$, leaving only the DC component. Thus,

$$v_f(t) = K_2 V_I V_O \cos\theta_e \quad (11)$$

After amplification the DC voltage driving the VCO and maintaining lock within the loop is

$$v_d(t) = V_D = AK_2 V_I V_O \cos\theta_e \quad (12)$$

Suppose ω_I and ω_O are perfectly synchronized to the free-running frequency ω_O'. For this case, V_D will be zero, indicating that θ_e must be ±90°. Thus V_D is proportional to the phase difference or phase error between θ_i and θ_o centered about a reference phase angle of ±90°. If ω_I changes slightly from ω_O', the first effect will be a change in θ_e from ±90°. V_D will adjust and settle out to some non-zero value to correct ω_O; under this condition frequency lock is maintained with $\omega_I = \omega_O$. The phase error will be shifted by some amount $\Delta\theta$ from the reference phase angle of ±90°. This concept can be simplified by redefining θ_e as

$$\theta_e = \theta_r \pm \Delta\theta \quad (13)$$

where θ_r is the inherent, reference phase shift of ±90° and $\Delta\theta$ is the departure from this reference value. Now the VCO control voltage becomes

$$v_D = AK_1 V_I V_O \cos(\theta_r \pm \Delta\theta) = \pm AK_2 v_I V_O \sin\Delta\theta \quad (14)$$

Since the sine function is odd, a momentary change in $\Delta\theta$ contains information about which way to adjust the VCO frequency to correct and maintain the locked condition. The maximum range over which $\Delta\theta$ changes can be tracked is -90° to +90°. This corresponds to a θ_e range from 0 to 180°.

In addition to being an error signal, V_D represents the demodulated output of an FM input applied as $v_{in}(t)$ assuming a linear VCO characteristic. Thus, FM demodulation can be accomplished with the PLL without the inductively-tuned circuits that are employed with conventional detectors.

DETERMINING PLL MODEL PARAMETERS

Since the PLL is basically an electronic servo loop, many of the analytical techniques developed for control systems are applicable to phase-locked systems. Whenever phase lock is established between $v_i(t)$ and $v_o(t)$ the linear model of Figure 4 can be used to predict the performance of the PLL system. Here θ_i and θ_o represent the phase angles associated with the input/output waveshapes, respectively; F(s) represents a generalized voltage transfer function for the low-pass filter in the s complex frequency domain; and K_d and K_o are conversion gains of the phase comparator and VCO, respectively, each having units as shown. The 1/s term associated with the VCO accounts for the inherent 90° phase shift in the loop since the VCO converts a voltage to a frequency and since phase is the integral of frequency. Thus the VCO functions as an integrator in the feedback loop.

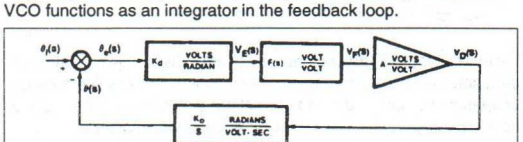


Figure 4. Linear Model of PLL System

Specific values of K_d and K_o for all of Philips Semiconductors general purpose PLLs can be found in the sections describing the particular loop of interest. However, sometimes it may be desired to determine these conversion gains exactly for a specific device. The measurement scheme shown in Figure 5 can be used to determine K_d and Ko for a loop under lock. The function of the Khron-Hite filters is to extract the fundamental sinusoidal frequency component of their square wave inputs for application to the Gain-Phase Meter. If the input signal from the Function Generator is sinusoidal, then the first Khron-Hite filter may be eliminated. It is recommended to use high impedance oscilloscope probes so as to not distort the input of VCO waveshapes, thereby potentially altering their phase relationships. The frequency counter can be driven from the scope as shown, or connected directly to the input or VCO, provided its input impedance is large.

Modeling the PLL

AN178

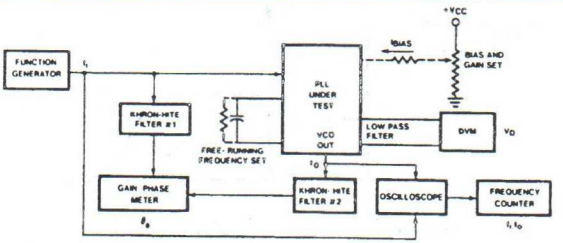


Figure 5. Measurement Scheme for K_d and K_o Determinations

The procedure to follow for obtaining K_d and K_o is as follows:

1. Establish the desired external bias and gain conditions for the PLL under test.
2. With the Function Generator turned off, set the free-running frequency of the loop via the timing capacitor and timing resistor if appropriate. Monitor f_O' with the Frequency Counter.
3. Turn on the Function Generator and check to make sure the amplitude of the input signal is appropriate for the particular loop under test.
4. Adjust the input frequency for lock. Lock is discernable on a dual-trace scope when the input and VCO waveforms are synchronized and stationary with respect to each other. One should be especially careful to check that locking has not occurred between the VCO and some harmonic frequency. Carefully inspect both waveshapes, making sure each has the same period. (If a second Frequency Counter is available, an alternate scheme can be used to confirm frequency locking. One frequency counter is used to monitor the input signal frequency, and the second counter is used for the VCO frequency. When the two counters display the same frequency, the PLL is iocked.)
5. Set the input frequency to the free-running frequency and note the Gain-Phase Meter display. It should be approximately 90° ±10° nominally. Record the phase error, θ_e, the VCO control voltage, V_D, and the input frequency, f_I.
6. Adjust f_I for frequencies above and below f_O' and record θ_e and V_D for each f_I, as appropriate.
7. Making a plot of V_D versus θ_e is useful for checking the measurement data and the system's linearity. The slope of this plot ($\Delta V_D/\Delta\theta_e$) is K_d in units of V/°. Multiplying this slope by $180/\pi$ gives the desired K_d in volts/radian.
8. A plot of $f_I = f_O$ versus V_D while the loop remains locked will check the VCO linearity. The slope of this plot is K_o at the particular free-running frequency. The units of slope taken directly from the graph are Hz/V. Multiplying this slope figure by 2π gives the desired K_o in units of radians/ volt-sec.

K_d is generally constant over wide frequency ranges, but is linearily related to the input signal amplitude. K_o is constant with input signal level but does vary linearily with f_O'. Often it is convenient to specify a normalized K_o as

$$K_{O(norm)} = \frac{K_O \text{ rad}}{f_O' \text{ V}} \quad (15)$$

The K_o value at any desired free-running frequency then can be estimated as

$$K_O \text{ (@ any\% } f_O') = K_{o(norm)} f_O' \quad (16)$$

AThe loop gain for the PLL system is

$$K_v = K_d K_o A \quad (17)$$

(Often when the gain A is due to an amplifier internal to the IC, A will be included in either K_d or K_o. This is further illustrated in the article on the 565 PLL.)

MODELING THE PLL SYSTEM WITH VARIOUS LOW-PASS FILTERS

The open-loop transfer function for the PLL is

$$T(s) = \frac{K_V F(s)}{s} \quad (18)$$

Using linear feedback analysis techniques, and assuming that the VCO is in the forward path, the closed-loop transfer characteristics H(s) can be related to the open-loop performance as

$$H(s) = \frac{T(s)}{1 + T(s)} \quad (19)$$

and the roots of the characteristic system polynomial can be readily determined by root-locus techniques.

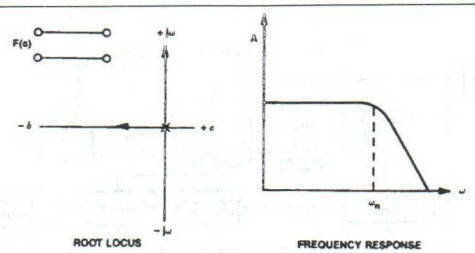
From these equations, it is apparent that the transient performance and frequency response of the loop is heavily dependent upon the choice of filter and its corresponding transfer characteristic, F(s).

Zero-Order Filter — F(s) = 1

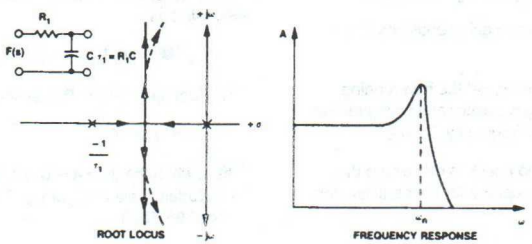
The simplest case is that of the first-order loop where F(s)= 1 (no filter). The closed-loop transfer function then becomes

$$H(s) = \frac{K_V}{S + K_V} \quad (20)$$

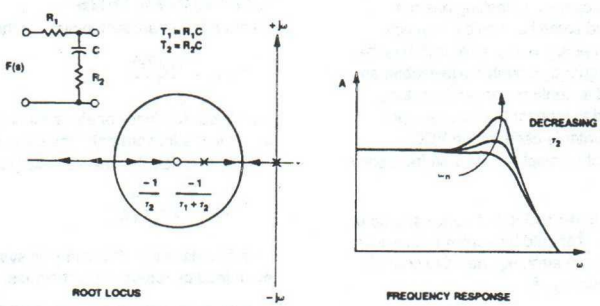
This transfer function gives the root locus as a function of the total loop gain K_v and the corresponding frequency response shown in Figure 6a. The open-loop pole at the origin is due to the integrating action of the VCO. Note that the frequency response is actually the amplitude of the difference frequency component versus modulating frequency when the PLL is used to track a frequency-modulated input signal. Since there is no low-pass filter in this case, sum frequency components are also present at the phase comparator output and must be filtered outside of the loop if the difference frequency component (demodulated FM) is to be measured.



a. Zero-Order Filter



b. First-Order Simple Lag Filter



c. First-Order Lag-Lead Filter

Figure 6. Root Locus and Frequency Response Plots

First-Order Filter

With the addition of a single-pole low-pass filter F(s) of the form

$$F(s) = \frac{1}{1 + \tau_1 s} \qquad (21)$$

where $\tau 1 = R_1C_1$, the PLL becomes a second-order system with the root locus shown in Figure 6b. Again, an open-loop pole is located at the origin because of the integrating action of the VCO. Another open-loop pole is positioned on the real axis at $-1/\tau_1$ where τ_1 is the time constant of the low-pass filter.

One can make the following observations from the root locus characteristics of Figure 6b:

a. As the loop gain K_v increases for a given choice of τ_1, the imaginary part of the closed-loop poles increases: thus, the natural frequency of the loop increases and the loop becomes more and more under-damped.

b. If the filter time constant is increased, the real part of the closed-loop poles becomes smaller and the loop damping is reduced.

As in any practical feedback system, excess shifts or non-dominant poles associated with the blocks within the PLL can cause the root loci to bend toward the right half plane as shown by the dashed line in Figure 6b. This is likely to happen if either the loop gain or the filter time constant is too large and may cause the loop to break into sustained oscillations.

First-Order Lag-Lead Filter

The stability problem can be eliminated by using a lag-lead type of filter, as indicated in Figure 6c. This type of a filter has the transfer lock range. For the simple first-order lag filter function

$$F(s) = \frac{1 + \tau_2 s}{1 + (tau_1 + \tau_2)s} \quad (22)$$

where $\tau_2 = R_2C$ and $\tau_1 = R_1C$. By proper choice of R_2, this type of filter confines the root locus to the left half-plane and ensures stability. The lag-lead filter gives a frequency response dependent on the damping, which can now be controlled by the proper adjustment of τ_1 and τ_2. In practice, this type of filter is important because it allows the loop to be used with a response between that of the firstand second-order loops and it provides an additional control over the loop transient response. If $R_2 = 0$, the loop behaves as a second-order loop and as $R_2 \rightarrow \infty$, the loop behaves as a first-order loop due to a pole-zero cancellation. However, as first-order operation is approached, the noise bandwidth increases and interference rejection decreases since the high frequency error components in the loop are now attenuated to a lesser degree.

Second- and Higher-Order Filters

Second- and higher-order filters, as well as active filters, occasionally are designed and incorporated within the PLL to achieve a particular response not possible or easily obtained with zero or first-order filters. Adding more poles and more gain to the closedloop transfer function reduces the inherent stability of the loop. Thus the designer must exercise extreme care and utilize complex stability analysis if second-order (and higher) filters or active filters are to be considered.

CALCULATING LOCK AND CAPTURE RANGES

In terms of the basic gain expression in the and system, the lock range of the PLL ω_L can be shown to be numerically equal to the DC loop gain (2-sided lock range).

$$2\omega_L + 4\pi f_L + K_V F(0) \quad (23)$$

where F(O) is the value of the low-pass filters transfer function at DC.

Since the capture range ω_C denotes a transient condition, it is not as readily derived as the lock range. However, an approximate expression for the capture range can be wrinen as (2-sided capture range).

$$2\omega_C = 4\pi f_C \approx K_V \mid F(i\omega_C) \mid \quad (24)$$

where $F(i\omega_C)$ is the magnitude of the low-pass filter transfer function evaluated at ω_C. Solution of Equation 24 frequently involves a "trial and error" process since the capture range is a function of itself. Note that at all times the capture range is smaller than the lock rage. For the simple first-order lag filter of Figure 6b, the capture range can be approximated as

$$2\omega_c \approx 2\sqrt{\frac{\omega_L}{\tau_1}} = 2\sqrt{\frac{K_V}{\tau_1}} \quad (25)$$

This approximation is valid for

$$\tau_1 \gg \frac{1}{2\omega_L} \quad (26)$$

Equations 23 and 24 show that the capture range increases as the low-pass filter time constant is decreased, whereas the lock range is unaffected by the filter and is determined solely by the loop gain.

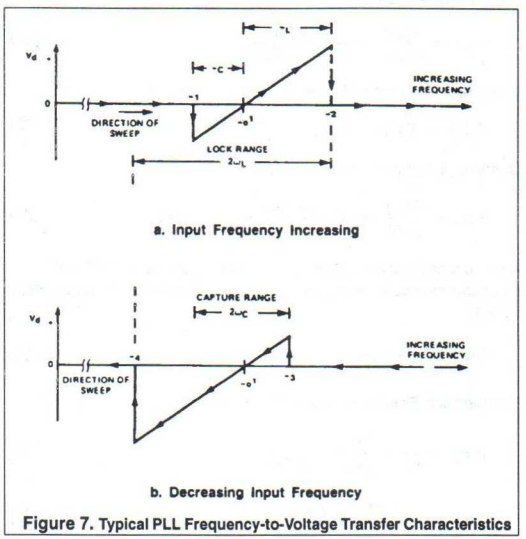


Figure 7. Typical PLL Frequency-to-Voltage Transfer Characteristics

Figure 7 shows the typical frequency-to-voltage transfer characteristics of the PLL. The input is assumed to be a sine wave whose frequency is swept slowly over a broad frequency range. The vertical scale is the corresponding loop error voltage. In Figure 7a, the input frequency is being gradually increased. The loop does not respond to the signal until it reaches a frequency ω_1, corresponding to the lower edge of the capture range. Then, the loop suddenly locks on the input and causes a negative jump of the loop error voltage. Next, V_d varies with frequency with a slope equal to the reciprocal of VCO conversion gain (1/Ko) and goes through zero as $\omega_I = \omega_O'$. The loop tracks the input until the input frequency reaches ω_2, corresponding to the upper edge of the lock range. The PLL then loses lock and the error voltage drops to zero. If the input frequency is swept slowly back, the cycle repeats itself, but is inverted, as shown in Figure 7b. The loop recaptures the signal at ω_3 and tracks it down to ω_4. The total capture and lock ranges of the system are:

$$2\omega_C = \omega_3 - \omega_1 \quad (27)$$

and

$$2\omega_L = \omega_2 - \omega_4 \quad (28)$$

Note that, as indicated by the transfer characteristics of Figure 7, the PLL system has an inherent selectivity about the free-running frequency, ω_O'. It will respond only to the input signal frequencies that are separated from ω_O' by less than ω_C or ω_L, depending on whether the loop starts with or without an initial lock condition. The linearity of the frequency-to-voltage conversion characteristics for the PLL is determined solely by the VCO conversion gain. Therefore, in most PLL applications, the VCO is required to have a highly linear voltage-to-frequency transfer characteristic.

Modeling the PLL

AN178

DETERMINING LOOP RESPONSE

The transient response of a PLL can be calculated using the model of Figure 4 and Equations 18 and 19 as starting points. Combining these equations gives

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_V F(s)}{s + K_V F(s)} \quad (29)$$

The phase error which keeps the system in lock is

$$\theta_e(s) = \theta_i(s) - \theta_o(s) \quad (30)$$

Define a phase error transfer function

$$E(s) + \frac{\theta_e(s)}{\theta_i(s)} = 1 - \frac{\theta_o(s)}{\theta_i(s)} = 1 - H(s) \quad (31)$$

As an example of the utilization of these equations, consider the most common case of a loop employing a simple first-order lag filter where

$$F(s) = \frac{1}{1 + s\tau_1} \quad (32)$$

For this filter, Equations 29 and 31 become

$$H(s) = \frac{K_V/\tau_1}{s + s/\tau_1 + K_V/\pi_1} \quad (33)$$

$$E(s) = \frac{s(s + 1/\tau_1)}{S + s/\tau_1 + K_V/\tau_1} \quad (34)$$

Both equations are second-order and have the same denominator which can be expressed as

$$D(s) = s^2 + s/\tau_1 + K_V/\tau_1 = s^2 + 2\zeta\omega_n s + \omega_n^2 \quad (35)$$

Where ω_n and ζ are, respectively, the system's undamped natural frequency and damping factor defined as

$$\omega_n = \sqrt{K_V/\tau_1} \quad (36)$$

$$\zeta = \frac{1}{K_V\tau_1} = \frac{\omega_n}{2K_V} \quad (37)$$

The system is considered overdamped for $\zeta > 1.0$, and critically damped $\zeta = 1.0$. Now examine this PLL system's response to various types of inputs.

Step-of-Phase Input

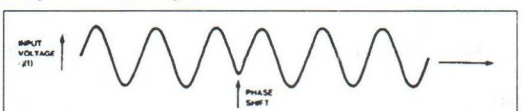


Figure 8. Input Signal Representing a Unit Step of Phase at Constant Frequency

Consider a unit step-of-phase as the input signal. This input is shown in Figure 8 and can be thought of as simply shifting the time axis by a unit step (one radian or one degree, depending upon the working units) while maintaining the same input frequency. Mathematically this input has the form

$$\theta_i(s) = \frac{1}{s} \quad (38)$$

The phase of VCO output and the system's phase error are represented by

$$\theta_o(s) = \frac{H(s)}{s} = \frac{\omega_n^2}{s(s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (39)$$

$$\theta_o(s) = \frac{E(s)}{s} = \frac{s + 2\zeta\omega_n}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (40)$$

(depending upon the working units) while maintaining the same input frequency. Mathematically this input has the form

$$\theta_o(t) = 1 + \frac{e - \zeta\omega_n t}{\sqrt{1 - \zeta^2}} \sin(\omega_n t\sqrt{1 - \zeta^2} + \Psi \quad (41)$$

$$\text{where } \Psi = \arctan\frac{\sqrt{1 - \zeta^2}}{\zeta} \quad (42)$$

and $\zeta \neq 1$.

$$\theta_e(t) = \frac{e - \zeta\omega_n(t)}{1 - \zeta^2} \sin(\omega_n t\sqrt{1 - \zeta^2} + \Psi \quad (43)$$

When $\zeta = 1$, these phase responses are

$$\theta_o(t) = 1 - (1 - \omega_n t)e - \omega_n t \quad (44)$$

and

$$\theta_e(t) = (1 + \omega_n t)e - \omega_n t \quad (45)$$

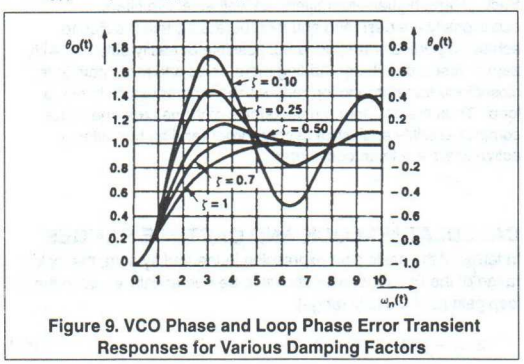


Figure 9. VCO Phase and Loop Phase Error Transient Responses for Various Damping Factors

Figure 9 is a plot of the VCO phase response and the phase error transient for various damping factors. Note from this figure that an underdamped system has overshoot which can cause the loop to break lock if this overshoot is too large. The critical condition for maintaining lock is to keep the phase error within the dynamic range for the phase comparator of $-\pi/2$ to $\pi 2$ radians. For the underdamped case, the peak phase-error overshoot is

$$\theta_e(\max) = e - \zeta\pi/ > \sqrt{1 - \zeta^2} \quad (46)$$

which must be less than $\pi/2$ to maintain lock. Lock can also be broken for the overdamped and critically-damped loops if the input phase shift is too large where the phase error exceeds $\pm\pi/2$ radians.

The analysis and equations given are based upon the small-signal model of Figure 4. If the signal amplitudes become too large, one or more functional blocks in the system can saturate, causing a slew rate type limiting action that may break lock.

The *transient change* in the VCO frequency due to the unit step-of-phase input can be found by taking the time derivative of Equation 41 or alternatively by finding the inverse Laplace transform of

$$\omega_o(s) = s\theta_o(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (47)$$

which is

$$\omega_O(t) = \frac{\omega_n e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} \sin \omega_n t\sqrt{1-\zeta^2} \quad (48)$$

Unit Step-of-Frequency Input

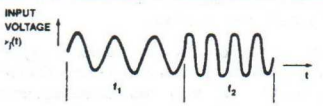


Figure 10. Input Signal for a Unit Step-of-Frequency at Constant Phase

This type of input occurs when the input frequency is instantaneously changed from one frequency to another as is done in FSK and modem applications. For this input, as shown in Figure 10,

$$\theta_i(s) = \frac{1}{s^2} \quad (49)$$

The VCO output phase is

$$\theta_o(s) = \frac{\omega_n^2}{s^2(s^2 + 2\zeta\omega_n s + \omega_n^2)} \quad (50)$$

The time expression for the VCO *phase change* is

$$\theta_o(t) = t - \frac{2\zeta}{\omega_n} + \frac{e^{-\zeta\omega_n t}}{\omega_n\sqrt{1-\zeta^2}} \sin(\omega_n t\sqrt{1-\zeta^2} + 2\Psi \quad (51)$$

for $\zeta \neq 1$.

The time expression for the VCO *frequency change* for a unit step-of-frequency input is the same as the time response VCO phase change due to a step-of-phase input (Equation 41), or

$\omega_O(t)$ for frequency step input = $\theta_o(t)$ for phase step input. Thus

$$\omega_o(t) = 1 + \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} \sin(\omega_n t\sqrt{1-\zeta^2} + \Psi \quad (52)$$

for $\zeta \neq 1$.

Unit Ramp-of-Frequency Input

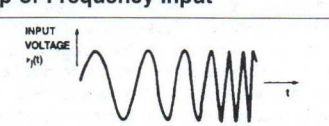


Figure 11. Input Signal for a Unit Ramp-of-Frequency Input

This form of input signal represents sweeping the input frequency at a constant rate and direction as shown in Figure 11. The amplitude and phase of the input remain constant; the input frequency changes linearly with time. Since the input signal to the PLL model is a phase, a unit ramp-of-frequency appears as a phase acceleration type input that can be mathematically described as

$$\theta_i(s) = \frac{1}{s^3} \quad (53)$$

The VCO output phase change is

$$\theta_o(s) = \frac{\omega_n^2}{s^3(s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (54)$$

The time expression for the VCO phase change is

$$\theta_o(s) = \frac{t^2}{2} - \frac{2\zeta t}{\omega_n} + \frac{2\zeta}{\omega_n^2}[2\zeta(1-\omega_n^2) + \left(\frac{1-4\zeta^2\omega_n^2+4\zeta^2\omega_n^4}{1-\zeta^2}\right)^{\frac{1}{2}} \quad (55)$$

$$x\, e^{-\zeta\omega_n t} \sin(\omega_n t\sqrt{1-\zeta^2} + \Psi$$

where $\Psi = \arctan\frac{\sqrt{1-\zeta^2}}{\zeta(1-2\omega_n^2} + \Psi$

and y is given in Equation 42.

PLL BUILDING BLOCKS VCO

Since three different forms of VCO have been used in the Philips Semiconductors PLL series, the VCO details will not be discussed until the individual loops are described. However, a few general comments about VCOs are in order.

When the PLL is locked to a signal, the VCO voltage is a function of the frequency of the input signal. Since the VCO control voltage is the demodulated output during FM demodulation, it is important that the VCO voltage-to-frequency characteristic be linear so that the output is not distorted. Over the linear range of the VCO, the conversin gain is given by K_O (in radian/V-sec)

$$K_O = \frac{\Delta\omega_O}{\Delta V_d} \quad (56)$$

Since the loop output voltage is the VCO voltage, we can get the loop output voltage as

$$\Delta V_d = \frac{\Delta\omega_O}{K_O} \quad (57)$$

The gain K_O can be found from the data sheet. When the VCO voltage is changed, the frequency change is virtually instantaneous.

Phase Comparator

All of Philips Semiconductors analog phase-locked loops use the same form of phase comparator — often called the doubly-balanced multiplier or mixer. Such a circuit is shown in Figure 12.

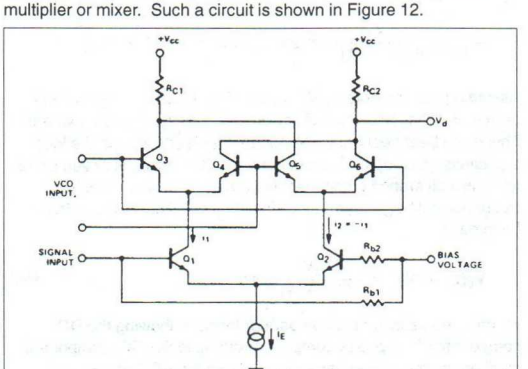


Figure 12. Integrated Phase Comparator Circuit

The input stage formed by transistors Q1 and Q2 may be viewed as a differential amplifier which has an equivalent collector resistance

R_C and whose differential gain at balance is the ratio of R_C to the dynamic emitter resistance, r_e, of Q1 and Q2.

$$A_d = \frac{R_C}{r_e} = \frac{\frac{R_C}{0.026}}{I_F/2} = \frac{R_C I_E}{0.052} \quad (58)$$

where I_E is the total DC bias current for the differential amplifier pair.

The switching stage formed by Q3 – Q6 is switched on and off by the VCO square wave. Since the collector current swing of Q2 is the negative of the collector current swing of Q1, the switching action has the effect of multiplying the differential stage output first by +1 and then by –1. That is, when the base of Q4 is positive, R_{C2} receives I_1 and when the base of Q6 is positive, R_{C2} receives $i_2 = i_1$. Since the circuit is called a multiplier, performing the multiplication will gain further insight into the action of the phase comparator.

Consider an input signal which consists of two added components: a component at frequency ω_I which is close to the free-running frequency and a component at frequency ω_K which may be at any frequency. The input signal is

$$v_i(t) + v_k(t) = V_I \sin(\omega_i t + \theta_i) + v_k \sin(\omega_k t + \omega_k) \quad (59)$$

where θ_i and θ_k are the phase in relation to the VCO signal. The unity square wave developed in the multiplier by the VCO signal is

$$v_o(t) = \sum_{n=0}^{\infty} \frac{4}{\pi(2n+1)} \sin[(2n+1)\omega_o t] \quad (60)$$

where ω_O is the VCO frequency. Multiplying the two terms, using the appropriate trigonometric relationships, and inserting the differential stage gain A_d gives:

$$v_e(t) = \frac{2A_d}{\pi} \quad (61)$$

$$\left[\sum_{n=0}^{\infty} \frac{V_I}{(2n+1)} \cos[(2n+1)\omega_O t - \omega_i t - \theta_i] \right.$$

$$- \sum_{n=0}^{\infty} \frac{V_I}{(2n+1)} \cos[(2n+1)\omega_O t + \omega_i t + \theta_i]$$

$$+ \sum_{n=0}^{\infty} \frac{V_k}{(2n+1)} \cos[(2n+1)\omega_O t - \omega_i t - \theta_i]$$

$$\left. - \sum_{n=0}^{\infty} \frac{V_k}{(2n+1)} \cos[(2n+1)\omega_O t + \omega_i t + \theta_i] \right]$$

Assuming that temporarily V_k is zero, if ω_I is close to ω_O, the first term (n = 0) has a low frequency difference frequency component. This is the beat frequency component that feeds around the loop and causes lock-up by modulating the VCO. As ω_O is driven closer to ω_I, this difference component becomes lower and lower in frequency until $\omega_O = \omega_I$ and lock is achieved. The first term then becomes

$$V_e(t) = V_E = \frac{2A_d V_I}{\pi(2n+1)} \cos\theta_i \quad (62)$$

which is the usual phase comparator formula showing the DC component of the phase comparator during lock. This component must equal the voltage necessary to keep the VCO at ω_O. It is possible for ω_O to equal ω_I momentarily during the lock-up process and, yet, for the phase to be incorrect so that ω_O passes through ω_I without lock being achieved. This explains why lock is usually not achieved instantaneously, even when $\omega_I = \omega_O$ at t=0.

If $n \neq 0$ in the first term, the loop can lock when $\omega_I = (2n+1)\omega_O$, giving the DC phase comparator component

$$V_e(t) = V_E = \frac{2A_d V_I}{\pi(2n+1)} \cos\theta_i \quad (63)$$

showing that the loop can lock to odd harmonics of the free-running frequency. The (2n + 1) term in the denominator shows that the phase comparator's output is lower for harmonic lock, which explains why the lock range decreases as higher and higher odd harmonics are used to achieve lock.

Note also that the phase comparator's output during lock is (assuming A_d is constant) also a function of the input amplitude V_I. Thus, for a given DC phase comparator output V_E, an input amplitude decrease must be accompanied by a phase change. Since the loop can remain locked only for θ_i between 0 and 180°, the lower V_I becomes, the more the lock range is reduced.

Note from the second term that during lock the lowest possible frequency is $\omega_O + \omega_I = 2\omega_I$. A sum frequency component is always present at the phase comparator output. This component is usually greatly attenuated by the low-pass filter capacitor connected to the phase comparator output. However, when rapid tracking is required (as with high-speed FM detection or FSK), the requirement for a relatively high frequency cutoff in the low-pass filter may leave this component unattenuated to the extent that it interferes with detection. At the very least, additional filtering may be required to remove this component. Components caused by $n \neq 0$ in the second term are both attenuated and of much higher frequency, so they may be neglected.

Suppose that other frequencies represented by V_k are present. What is their effect for $V_k \neq 0$?

The third term shows that V_k introduces another difference frequency component. Obviously, if ω_k is close to ω_I, it can interfere with the locking process since it may form a beat frequency of the same magnitude as the desired locking beat frequency. However, suppose lock has been achieved so that $\omega_O = \omega_I$. In order for lock to be maintained, the average phase comparator output must be constant. If $\omega_O = \omega_k$ is relatively low in frequency, the phase θ_i must change to compensate for this beat frequency. Broadly speaking, any signal in addition to the signal to which the loop is locked causes a phase variation. Usually this is negligible since ω_k is often far removed from ω_I. However, it has been stated that the phase θ_i can move only between 0 and 180°. Suppose the phase limit has been reached and V_k appears. Since it cannot be compensated for, it will drive the loop out of lock. This explains why extraneous signals can result in a decrease in the lock range. If V_k is assumed to be an instantaneous noise component, the same effect occurs. When the full swing of the loop is being utilized, noise will decrease the lock or tracking range. This effect can be reduced by decreasing the cutoff frequency of the lowpass filter so that the $\omega_O - \omega_k$ is attenuated to a greater extent, which illustrates that noise immunity and out-band frequency rejection is improved (at the expense of capture range since $\omega_O - \omega_I$ is likewise attenuated when the low-pass filter capacitor is large.

The third term can have a DC component when ω_k is an odd harmonic of the locked frequency so that $(2n+1)(\omega_O - \omega_I)$ is zero and θ_k makes its appearance. This will have an effect on θ_1 which will change the θ_1 versus frequency ω_I. This is most noticeable when the waveform of the incoming signal is, for example, a square wave. The θ_k term will combine with the θ_1 term so that the phase is a linear function of input frequency. Other waveforms will give different phase versus frequency functions. When the input amplitude V_I is large and the loop gain is large, the phase will be close to 90° throughout the range of VCO swing, so this effect is often unnoticed.

The fourth term is of little consequence except that if ω_k approaches zero, the phase comparator output will have a component at the locked frequency ω_O at the output. For example, a DC offset at the input differential stage will appear as a square wave of fundamental ω_O at the phase comparator output. This is usually small and well attenuated by the low-pass filter. Since many out-band signals or noise components may be present, many V_k terms may be combining to influence locking and phase during lock. Fortunately, only those close to the locked frequency need be considered.

Quadrature-Phase Detector (QPD)

The quadrature-phase detector action is exactly the same except that its output is proportional to the sine of the phase angle. When the phase θ_i is 90°, the quadraturephase detector output is then at its maximum, which explains why it makes a useful lock or amplitude detector. The output of the quadrature-phase detector is given by

$$V_q = \frac{2A_qV_I}{\pi}\sin\theta_i \quad (64)$$

where V_I is the constant or modulated AM signal and $\theta_i \approx 90°$ in most cases so that sine $\theta_i = 1$ and

$$V_q = \frac{2A_qV_I}{\pi} \quad (65)$$

This is the demodulation principle of the autodyne receiver and the basis for the 567 tone decoder operation.

INITIAL PLL SETUP CHOICES

In a given application, maximum PLL effectiveness can be achieved if the designer understands the tradeoffs which can be made. Generally speaking, the designer is free to select the frequency, lock range, capture range, and input amplitude.

FREE-RUNNING FREOUENCY SELECTION

Setting the center or free-running frequency is accomplished by selecting one or two external components. The center frequency is usually set in the center of the expected input frequency range. Since the loop's ability to capture is a function of the difference between the incoming and free-running frequencies, the band edges of the capture range are always an equal distance (in Hz) from the center frequency. Typically, the lock range is also centered about the free-running frequency. Occasionally, the center frequency is chosen to be offset from the incoming frequency so that the tracking range is limited on one side. This permits rejection of an adjacent higher or lower frequency signal without paying the penalty for narrow-band operation (reduced tracking speed).

All of Philips Semiconductors loops use a phase comparator in which the input signal is multiplied by a unity square wave at the VCO frequency. The odd harmonics present in the square wave permit the loop to lock to input signals at these odd harmonics. Thus, the center frequency may be set to, say, 1/3 or 1/5 of the input signal. The tracking range, however, will be considerably reduced as the higher harmonics are utilized.

The foregoing phase comparator discussion would suggest that the PLL cannot lock to subharmonics because the phase comparator cannot produce a DC component if ω_i is less than ω_O.

The loop can lock to both odd harmonic and subharmonic signals in practice because such signals often contain harmonic components at ω_O. For example, a square wave of fundamental $\omega_O/3$ will have a substantial component at ω_O to which the loop can lock. Even a pure sine wave input signal can be used for harmonic locking if the PLL input stage is overdriven. (The resultant internal limiting generates harmonic frequencies.) Locking to even harmonics or subharmonics is the least satisfactory, since the input or VCO signal must contain second harmonic distortion. If locking to even harmonics is desired, the duty cycle of the input and VCO signals must be shifted away from the symmetrical to generate substantial, even harmonic, content.

In evaluating the loop for a potential application, it is best to actually compute the magnitude of the expected signal component nearest ω_O. This magnitude can be used to estimate the capture and lock ranges.

All of Philips Semiconductors loops are stabilized against center frequency drift due to power supply variations. Both the 565 and the 567 are temperature-compensated over the entire military temperature range (-55 to +125°C). To benefit from this inherent stability, however, the designer must provide equally stable (or better) external components. For maximum cost effectiveness in some non-critical applications, the designer may wish to trade some stability for lower cost external components.

GUIDELINES FOR LOCK RANGE CONTROL

Two things limit the lock range. First, any VCO can swing only so far; if the input signal frequency goes beyond this limit, lock will be lost. Second, the voltage developed by the phase comparator is proportional to the product of both the phase and the amplitude of the in-band component to which the loop is locked. If the signal amplitude decreases, the phase difference between the signal and the VCO must increase in order to maintain the same output voltage and, hence, the same frequency deviation. The 564 contains an internal limiter circuit between the signal input and one input to the phase comparator. This circuit limits the amplitude of large input signals such as those from TTL outputs to approximately 100mV before they are applied to the phase comparator. The limiter significantly improves the AM rejection of the PLL for input signal amplitudes greater than 100mV.

This happens so often with low input amplitudes that even the full ±90° phase range of the phase comparator cannot generate enough voltage to allow tracking wide deviations. When this occurs, the effective lock range is reduced. Weak input signals cause a reduction of tracking capability and greater phase errors. Conversely, a strong input signal will allow the use of the entire VCO swing capability and keeps the VCO phase (referred to the input signal) very close to 90° throughout the range. Note that the lock range does not depend on the low-pass filter. However, if a low-pass filter is in the loop, it will have the effect of limiting the maximum rate at which tracking can occur. Obviously, the LPF capacitor voltage cannot change instantly, so lock may be lost when large enough step changes occur. Between the constant frequency input and the step-change frequency input is some limiting frequency slew rate at which lock is just barely maintained. When tracking at this rate, the phase difference is at its limit of 0° or 180°. It can be seen that if the LPF cutoff frequency is low, the loop will be unable to track as fast as if the LPF cutoff frequency is higher. Thus, when maximum tracking rate is needed, the LPF should have a high cutoff frequency. However, a high cutoff frequency LPF will attenuate the sum frequencies to a lesser extent so that the output contains a significant and often bothersome signal at twice the input frequency. The phase comparator's output contains both sum and difference frequencies. During lock, the difference frequency is zero, but the sum frequency of twice the locked frequency is still

present. This sum frequency component can then be filtered out with an external low-pass filter.

INPUT LEVEL AMPLITUDE SELECTION

Whenever amplitude limiting of the in-band signal occurs, whether in the loop input stages or prior to the input, the lock and capture ranges become independent of signal amplitude.

Better noise and out-band signal immunity is achieved when the input levels are below the limiting threshold, since the input stage is in its linear region and the creation of cross-modulation components is reduced. Higher input levels will allow somewhat faster operation due to greater phase comparator gain and will result in a lock range which becomes constant with amplitude as the phase comparator gain becomes constant. Also, high input levels will result in a linear phase versus frequency characteristic.

CAPTURE RANGE CONTROL

There are two main reasons for making the low-pass filter time constant large. First, a large time constant provides an increased memory effect in the loop so that it remains at or near the operating frequency during momentary fading or loss of signal. Second, the large time constant integrates the phase comparator's output so that increased immunity to noise and out-band signals is obtained.

Besides the lower tracking rates attendant to large loop filters, other penalties must be paid for the benefits gained. The capture range is reduced and the capture transient becomes longer. Reduction of capture range occurs because the loop must utilize the magnitude of the difference frequency component at the phase comparator to drive the VCO towards the input frequency.

If the LPF cutoff frequency is low, the difference component amplitude is reduced and the loop cannot swing as far. Thus, the capture range is reduced.

LOCK-UP TIME AND TRACKING SPEED CONTROL

In tracking applications, lock-up time is normally of little consequence, but occasions do arise when it is desirable to keep lock-up time short to minimize data loss when noise or extraneous signals drive the loop out of lock. Lock-up time is of great importance in tone decoder type applications. Tracking speed is important if the loop is used to demodulate an FM signal. Although the following discussion dwells largely on lock-up time, the same comments apply to tracking speeds.

No simple expression is available which adequately describes the acquisition or lock-up time. This may be appreciated when we review the following factors which influence lock-up time.

a. Input phase

b. Low-pass filter characteristic

c. Loop damping

d. Deviation of input frequency from center frequency

e. In-band input amplitude

f. Out-band signals and noise

g. Center frequency

Fortunately, it is usually sufficient to know how to improve the lock-up time and what must be sacrificed to get faster lock-up.

Consider an operational loop or tone decoder where occasionally the lock-up transient is too long. What can be done to improve the situation — keeping in mind the factors that influence lock?

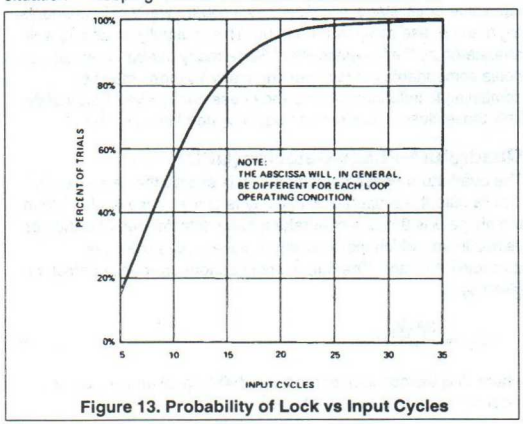


Figure 13. Probability of Lock vs Input Cycles

a. Initial phase relationship between incoming signal and VCO — This is the greatest single factor influencing the lock time. If the initial phase is wrong, it first drives the VCO frequency *away* from the input frequency so that the VCO frequency must walk back on the beat notes. Figure 13 gives a typical distribution of lock-up times with the input pulse initiated at random phase. The only way to overcome this variation is to send phase information all the time so that a favorable phase relationship is guaranteed at t = 0. For example, a number of PLLs or tone decoders may be weakly locked to low amplitude harmonics of a pulse train and the transmitted tone phase related to the same pulse train. Usually, however, the incoming phase cannot be controlled.

b. Low-pass filter — The larger the low-pass filter time constant, the longer will be the lock-up time. The lock-up time can be reduced by decreasing the filter time constant, but in doing so, some of the noise immunity and out-band signal rejection will be sacrificed. This is unfortunate, since this is what necessitated the use of a large filter in the first place. Also present will be a sum frequency (twice the VCO frequency) component at the low pass filter and greater phase jitter resulting from out-band signals and noise. In the case of the tone decoder (where control of the capture range is required since it specifies the device bandwidth) a lower value of low-pass capacitor automatically increases the bandwidth. Speed is gained only at the expense of added bandwidth.

c. Loop damping — A simple first-order lowpass filter of the form

$$F(s) = \frac{1}{1 + s\tau} \quad (66)$$

produces a loop damping of

$$\zeta = 1/2\sqrt{\frac{1}{\pi K_V}} \quad (67)$$

Damping can be increased not only by reducing π, as discussed above, but also by reducing the loop gain K_V. Using the loop gain reduction to control bandwidth or capture and lock ranges achieves better damping for narrow bandwidth operation. The penalty for this damping is that more phase comparator output is required for a given deviation so that phase errors are greater and noise immunity is reduced. Also, more input drive may be required for a given deviation.

d. Input frequency deviation from free-running frequency — Naturally, the further an applied input signal is from the free-running frequency of the loop, the longer it will take the loop to reach that frequency due to the charging time of the low-pass filter capacitor. Usually, however, the effect of this frequency deviation is small compared to the variation resulting from the initial phase uncertainty. Where loop damping is very low, however, it may be predominant.

e. In-band input amplitude — Since input amplitude is one factor in the phase comparator's gain K_d, and since K_d is a factor in the loop gain K_v damping is also a function of input amplitude. When the input amplitude is low, the lock-up time may be limited by the rate at which the low-pass capacitor can charge with the reduced phase comparator output (see d above).

f. Out-band signals and noise — Low levels of extraneous signals and noise have little effect on the lock-up time, neither improving or degrading it. However, large levels may overdrive the loop input stage so that limiting occurs, at which point the in-band signal starts to be suppressed. The lower effective input level can cause the lock-up time to increase, as discussed in e above.

g. Center frequency — Since lock-up time can be described in terms of the number of cycles to lock, fastest lock-up is achieved at higher frequencies. Thus, whenever a system can be operated at a higher frequency, lock will typically take place faster. Also, in systems where different frequencies are being detected, the higher frequencies, on the average, will be detected before the lower frequencies.

However, because of the wide variation due to initial phase, the reverse may be true for any single trial.

PLL MEASUREMENT TECHNIQUES

This section deals with measurements of PLL operation. The techniques suggested are meant to help the designer in evaluating the performance of the PLL during the initial setup period as well as to point out some pitfalls that may obscure loop evaluation. Recognizing that the test equipment may be limited, techniques are described which require a minimum of standard test items.

The majority of the PLL tests described can be done with a signal generator, a scope and a frequency counter. Most laboratories have these. A low cost digital voltmeter will facilitate accurate measurement of the VCO conversion gain. Where the need for a FM generator arises, it may be met in most cases by the VCO of a Philips Semiconductors PLL. Any of the loops may be set up to operate as a VCO by simply applying the modulating voltage to the low-pass filter terminal(s). The resulting generator may be checked for linearity by using the counter to check frequency as a function of modulating voltage. Since the VCOs may be modulated right down to DC, the calibration may be done in steps. Moreover, loop measurements may be made by applying a constant frequency to the loop input and the modulating signal to the low-pass filter terminal to simulate the effect of a FM input so that an FM generator may be omitted for many measurements.

FREE-RUNNING FREQUENCY

Free-running frequency measurements are easily made by connecting a frequency counter or oscilloscope to the VCO output of the loop. The loop should be connected in its final configuration with the chosen values of input, bypass, and low-pass filter capacitors. No input signal should be present. As the free-running frequency is read out, it can be adjusted to the desired value by the adjustment means selected for the particular loop. It is important not to make the frequency measurement directly at the timing capacitor, unless the capacity added by the measurement probe is much less than the timing capacitor value, since the probe capacity will then cause a frequency error.

When the frequency measurement is to be converted to a DC voltage for production readout or automated testing, a calibrated phase-locked loop can be used as a frequency meter.

CAPTURE AND LOCK RANGES

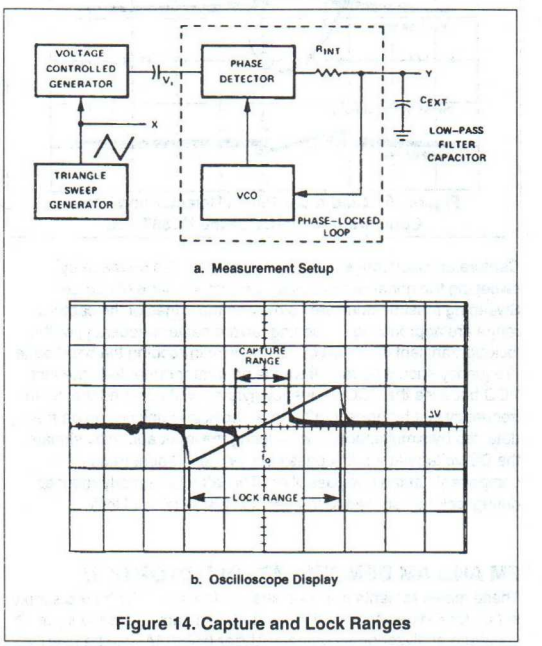


Figure 14. Capture and Lock Ranges

Figure 14a shows a typical measurement setup for capture and lock range measurements. The signal input from a variable frequency oscillator is swept linearly through the frequency range of interest and the loop FM output is displayed on a scope or (at low frequencies) X-Y recorder. The sweep voltage is applied to the X axis.

Figure 14b shows the type of trace which results. The lock range is given by the outer lines on the trace, which are formed as the incoming frequency sweeps away from the center frequency. The inner trace, formed as the frequency sweeps toward the center frequency, designates the capture range. Linearity of the VCO is revealed by the straightness of the trace portion within the lock range. The slope ($\Delta f/\Delta V$) is the conversion gain K_o for the VCO at the particular free-running frequency.

By using the sweep technique, the effect on free-running frequency, capture range, and lock range of the input amplitude, supply voltage, low-pass filter and temperature can be examined.

Because of the lock-up time duration and variation, the sweep frequency must be much lower than the free-running frequency, especially when the capture range is below 10% of the free-running

frequency. Otherwise, the apparent capture and lock range will be functions of sweep frequency. It is best to start sweeping as slowly as possible and, if desired, increase the rate until the capture range begins to show an apparent reduction — indicating that the sweep is too fast. Typical sweep frequencies are in the range of 1/1000 to 1/100,000 of the free-running frequency. In the case of the 567, the quadrature detector output may be similarly displayed on the Y axis, as shown in Figure 15, showing the output level versus frequency for one value of input amplitude.

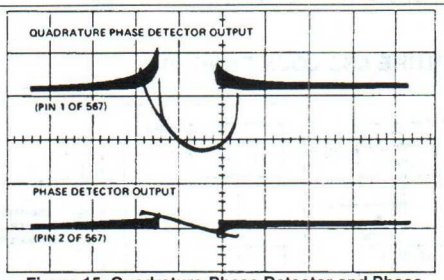


Figure 15. Quadrature-Phase Detector and Phase Comparator Outputs of the NE567 PLL

Capture and lock range measurements may also be made by sweeping the generator manually through the band of interest. Sweeping must be done very slowly as the edges of the capture range are approached (sweeping toward center frequency) or the lock-up transient delay will cause an error in reading the band edge. Frequency should be read from the generator rather than the loop VCO because the VCO frequency gyrates wildly around the center frequency just before and after lock. Lock and unlock can be readily detected by simultaneously monitoring the input and VCO signals, the DC voltage at the low-pass filter, or the AC beat frequency components at the low-pass filter. The latter are greatly reduced during lock as opposed to frequencies just outside of lock.

FM AND AM DEMODULATION DISTORTION

These measurements are quite straight-forward. The loop is simply set up for FM detection and the test signal is applied to the input. A spectrum analyzer or distortion analyzer (HP333A) can be used to measure distortion at the FM output.

For FM demodulation, the input signal amplitude must be large enough so that lock is not lost at the frequency extremes. The data sheets give the lock (or tracking) range as a function of input signal and the optional range control adjustments. Due to the inherent linearity of the VCOs, it makes little difference whether the FM carrier is at the free-running frequency or offset slightly as long as the tracking range limits are not exceeded.

The faster the FM modulation in relation to the center frequency, the lower the value of the capacitor in the low pass filter must be for satisfactory tracking. As this value decreases, however, it attenuates the sum frequency component of the phase comparator output less. The demodulated signal will appear to have greater distortion unless this component is filtered out before the distortion is measured.

NATURAL FREQUENCY AND DAMPING

Circuits and mathematical expressions for the natural frequencies and dampings are given in Figure 16 for two first-order low-pass filters. Because of the integrator action of the PLL in converting frequency to phase, the order of the loop always will be one greater than the order of the LPF. Hence, both these first-order LPFs produce a second-order PLL system.

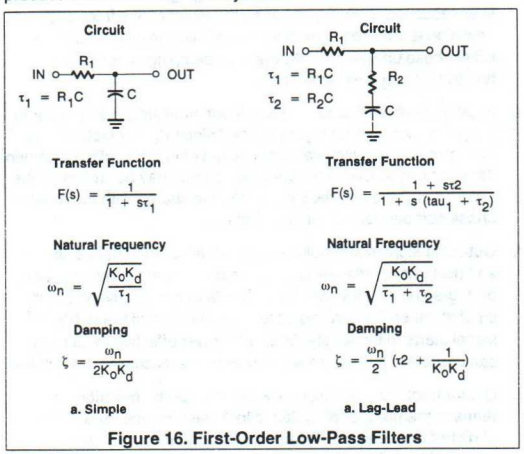


Figure 16. First-Order Low-Pass Filters

The natural frequency (ω_n) of a loop in its final circuit configuration can be measured by applying a frequency-modulated signal of the desired amplitude to the loop. Figure 16 shows that the natural frequency is a function of K_d, which is, in turn, a function of input amplitude. As the modulation frequency (ω_m) is increased, the phase relationship between the modulation and recovered sine wave will go through 90° at $\omega_m = \omega_n$ and the output amplitude will peak.

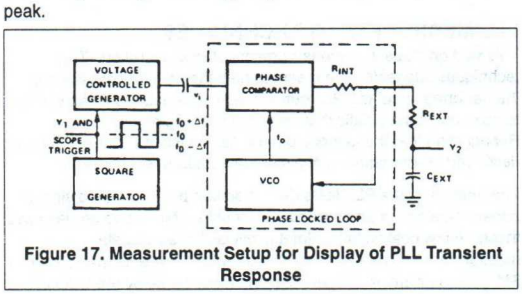
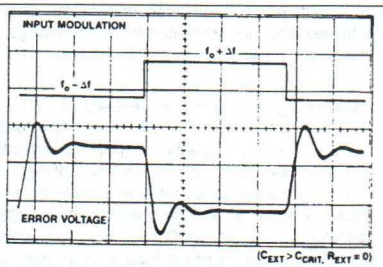


Figure 17. Measurement Setup for Display of PLL Transient Response

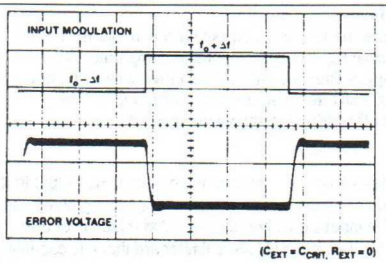
Damping is a function of K_d, K_o, and the lowpass filter. Since K_o and K_d are functions of the free-running frequency and input amplitude, respectively, damping is highly dependent on the particular operating condition of the loop. Damping estimates for the desired operating condition can be made by applying an input signal which is frequency-modulated within the lock range by a square wave. The low-pass filter voltage is then monitored on an oscilloscope which is synchronized to the modulating waveform, as shown in Figure 17. Figure 18 shows typical waveforms displayed. The loop damping can be estimated by comparing the number and magnitude of the overshoots with the graph of Figure 19, which gives the transient phase error due to a step in input frequency.

An expression for calculating the damping for any underdamped second-order system ($\zeta < 1.0$) when the normalized peak overshoot is known is

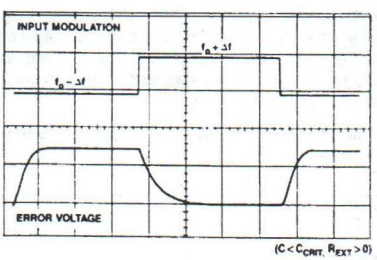
$$M_p = 1 + e^{-\zeta\pi/\sqrt{1-\zeta^2}} \quad (68)$$



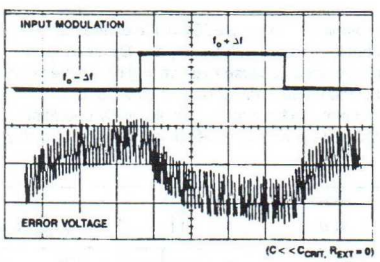
a. Underdamped with $\zeta \approx 0.28$



b. Critically Damped with $\zeta = 1.0$

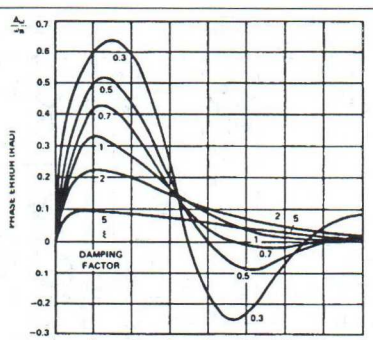


c. Overdamped with $\zeta = 10$



d. Highly Overdamped with $\zeta > 10$

Figure 18. Transient Response of PLL Error Voltage to Square Wave Frequency Modulation for Various Damping Conditions



a. Transient Phase Error as an Indication of Damping

ζ	PEAK AMPLITUDE / LOW FREQUENCY AMPLITUDE	$\frac{\omega - 3dB}{\omega_n}$
0.3	6.0dB	1.8
0.5	3.2dB	2.1
0.7	2.2dB	2.5
1.0	1.3dB	4.3
5.0	0.5dB	10

b. Ratio of Peak Amplitude to Low Frequency Amplitude of Error Voltage From Modulating Frequency Response

Figure 19. Estimating the Damping in a Second-Order PLL

Examination of Figure 18 shows that the normalized peak overshoot of the error voltage is approximately 1.4. Using this value for M_p in Equation 68 gives a damping of $\zeta \approx 0.28$.

Another way of estimating damping is to make use of the frequency response plot measured for the natural frequency (ω_n) measurement. For low damping constants, the frequency response measurement peak will be a strong function of damping. For high damping constants, the 3dB down point will give the damping. Figure 19 tabulates some approximate relationships.

NOISE

The effect of input noise on loop operation is very difficult to predict. Briefly, the input noise components near the center frequency are converted to phase noise. When the phase noise becomes so great that the +905 permissible phse variation is exceeded, the loop drops out of lock or fails to acquire lock. The best techniques is to actually apply the anticipated noise amplitude and badwidth to the input and then perform the capture and lock range measurements as well as perform operating tests with the anticipated input level and modulation deviations. By including a small safety factor in the loop design to compensate for small processing variations, satisfactory operation can be assured.

Circuit description of the NE564

AN179

DESCRIPTION

The NE564 contains the functional blocks shown in Figure 1. In addition to the normal PLL functions of phase comparator, VCO, amplifier and low-pass filter, the NE564 has internal circuitry for an input signal limiter, a DC retriever, and a Schmitt trigger. The complete circuit for the NE564 is shown in Figure 1.

Limiter

The input functions to produce a near constant amplitude output that serves as the input for the phase comparator. Eliminating amplitude variations in the FM input signal improves the AM rejection of the PLL. Additional features of the NE564's limiter are that it is capable of accepting TTL signals, operates at high frequencies up to 50MHz, and remains functional with variable supply voltages between 5 and 12V.*

Signal limiting is accomplished in the NE564 with a differential amplifier whose output is clipped by diodes D_1 and D_2 (see Figure 2). Schottky diodes are used because their limiting occurs between 0.3 to 0.4V instead of the 0.6 to 0.7V for regular IC diodes. This lower limiting level is helpful in biasing, especially for 5V operation. When limiting, the DC voltage across R_2 R_3 remains at the Schottky diode voltage. Good high frequency performance for Q_2 and Q_3 is achieved with current levels in the low mA range. Current-source biasing is established via the current mirror of D_5 and Q_4 (see Figure 1).

Base biasing for Q_3 is of concern because of the nature of the input signal which can be either a TTL digital signal of 0 to 5V amplitude or a low-level, AC coupled analog signal. Compatibility for either type is achieved by modifying the limiter of Figure 2 with the addition of the vertical Schottky PNP transistors Q_1 and Q_5 as shown in Figure 3. The input signal voltage appears as a collector-base voltage for Q_1, which presents no problems for either high TTL level inputs or low-level analog inputs. Q_5 is in turn diode-based by D_3 and D_4 (see Figure 1) which places the base voltages of Q_1 and Q_5 at approximately 1.0V. This same biasing network establishes a 1.3V bias at the base of Q_{13} for biasing the phase comparator section. A differential output signal from the input limiter is applied to one input of the phase comparator (Q_9 through Q_{12}) after buffering the level shifting through the Q_7 - Q_8 emitter-followers.

*Note: When operating above $5V_{DC}$, a limiting resistor must be used from V_{CC} to Pin 10 of the NE564.

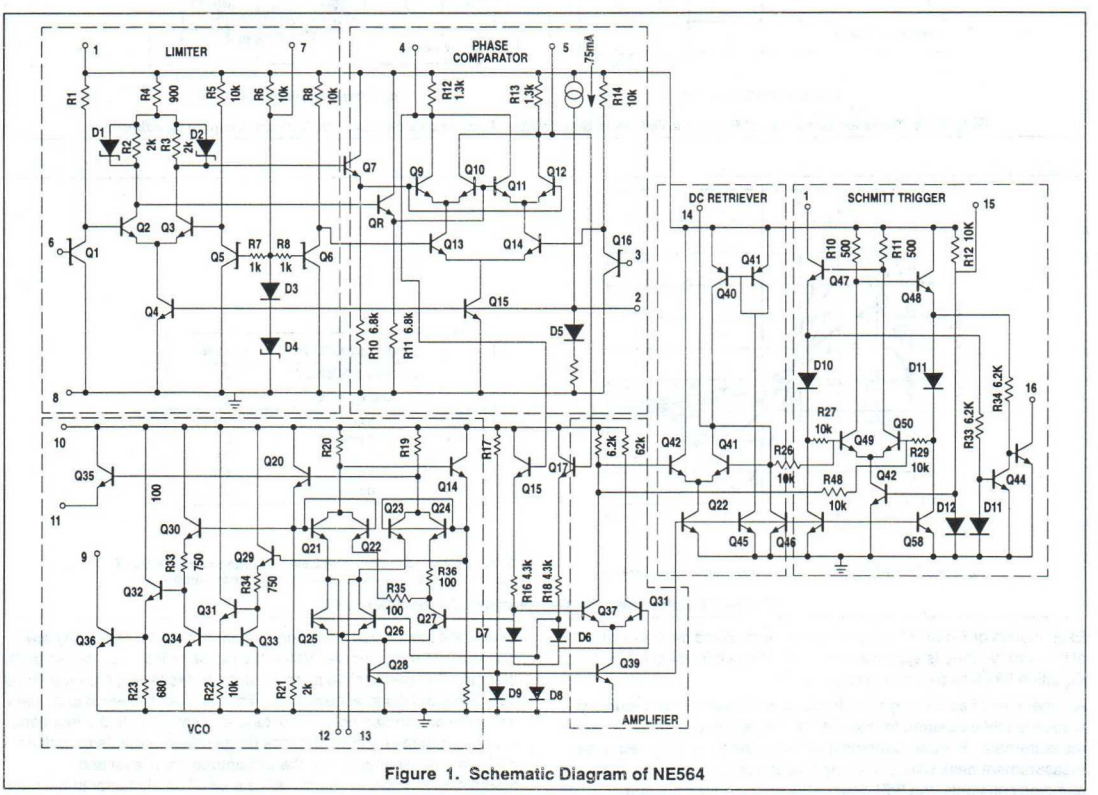


Figure 1. Schematic Diagram of NE564

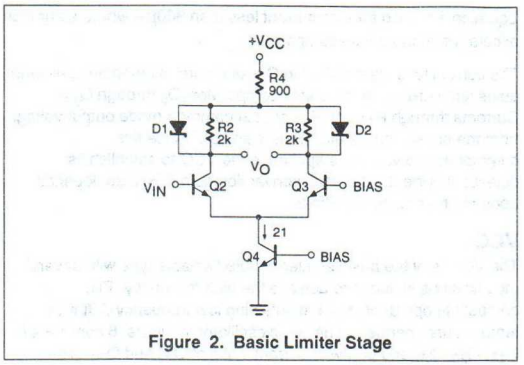


Figure 2. Basic Limiter Stage

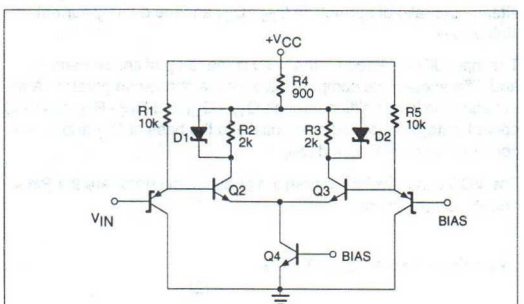


Figure 3. Limiter Stage with Input Buffering

Phase Comparator

The phase comparator section of the NE564 is shown in Figure 4. It is basically the conventional, double-balanced mixer commonly used in PLL circuits, with a few exceptions. The transconductance, g_M, for the Q_{13} - Q_{14} differential amplifier is directly proportional to the mirror current in Q_{15}. Thus, by externally sinking or sourcing current at Pin 2, g_M can be changed to alter the phase comparator's conversion gain, K_d. The nominal current injected into this node by the internal current source is 0.75mA for 5V operation. If the current is externally removed by gating, the phase comparator can be disabled and the VCO will operate at its free-running frequency.

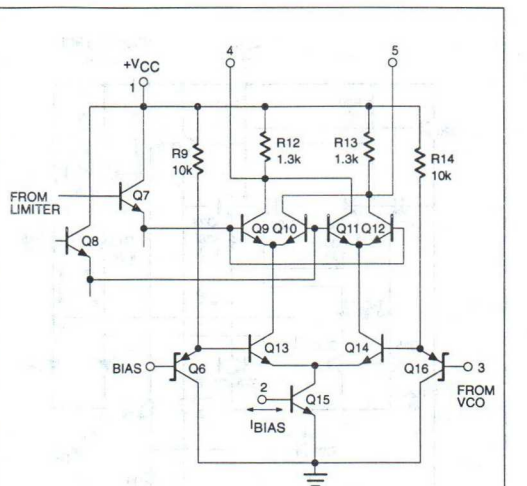


Figure 4. Phase Comparator Section

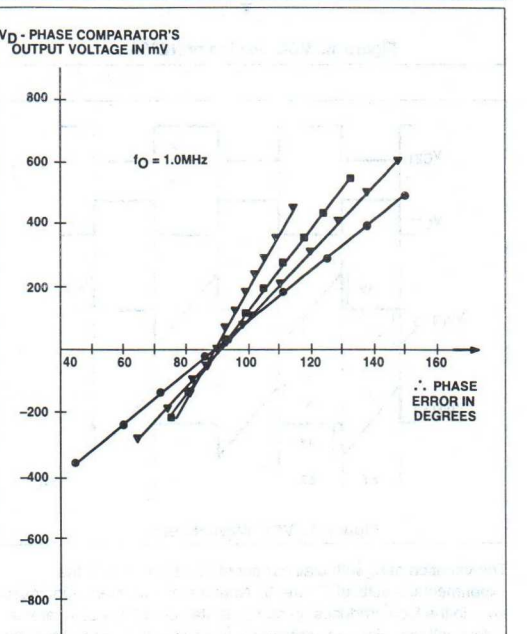


Figure 5. Variation of the Phase Comparator's Output Voltage vs Phase Error and Bias Current

Circuit description of the NE564

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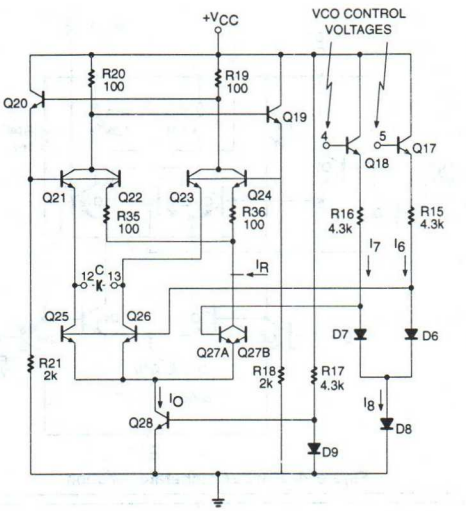


Figure 6. VCO Section of NE564

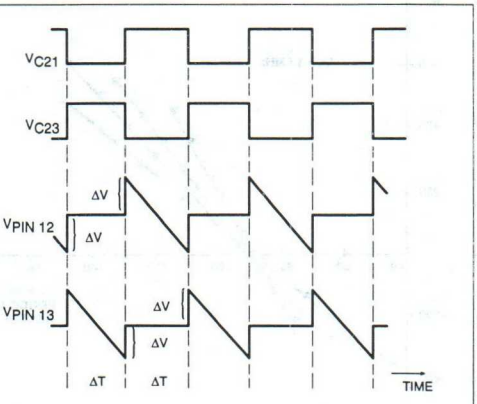


Figure 7. VCO Waveshapes

The variation of K_d with bias current at Pin 2 is shown in the experimental results of Figure 5. Note that the inherent 90o phase error in the loop produces an approximate zero-phase comparator output voltage. For any particular bias current, the slope of the line is the K_d conversion gain for the phase comparator. Numerically the data of Figure 5 can be expressed as:

$$K_d \cong 0.66 \left(\frac{\text{volts}}{\text{rad}}\right) + 9.2 \times 10^{-4} \left(\frac{\text{volts}}{\text{rad} \times \mu A}\right) \times I_{BIAS}\ (\mu A) \quad (1)$$

Equation 1 is valid for bias current less than 800μA where saturation occurs within the phase comparator.

The current level established in Q_{15} of Figure 3 determines all other quiescent currents in the phase comparator (Q_9 through Q_{14}). Currents through R_{12} and R_{13} set the common-mode output voltage from the phase comparator (Pins 4 and 5). Since this common-mode voltage is applied to the VCO to establish its quiescent currents, the VCO conversion gain (K_O) also depends upon the bias current at Pin 2.

VCO

The VCO is of the basic emitter-coupled astable type with several modifications included to achieve the high frequency, TTL compatible operation while maintaining low frequency drift with temperature changes. The basic oscillator in Figure 6 consists of Q_{19}, Q_{20}, Q_{21} and Q_{23} with current sinks of Q_{25} and Q_{26}. The master current sink of Q_{28} keeps the total current constant by altering the ratio of currents in Q_{25} - Q_{26} and the dummy current sink of Q_{27}.

The input drive voltage for the VCO is made up of common-mode and difference-mode components from the phase comparator. After buffering the level shifting through Q_{17} - Q_{18} and R_{15} - R_{16}, the VCO control voltage is applied differentially to the base of Q_{27} and to the common bases of Q_{25} and Q_{26}.

The VCO control voltages from the phase comparator are the Pin 4 and Pin 5 voltages or

$$V_4 = V_{C9} = V_{B18} = V_{CM} + 1/2V_{DM} \quad (2)$$

$$V_5 = V_{C12} = V_{B17} = V_{CM} + 1/2V_{DM} \quad (3)$$

where V_{CM} and V_{DM} are the respective common-mode and difference-mode voltages.

Emitter-followers Q_{17} and Q_{18} convert these control voltages into control currents through D_6 and D_7 of the form

$$I_6 = \left(\frac{1}{R_{15}}\right) [V_{CM} - 1/2V_{DM} - 3\ V_{BE}] \quad (4)$$

$$I_7 = \left(\frac{1}{R_{16}}\right) [V_{CM} - 1/2V_{DM} - 3\ V_{BE}] \quad (5)$$

These individual currents are summed in D_8 and become with $R_{15} = R_{16} = R$.

$$I_8 = I = I_6 + I_7 = 2/R\ (V_{CM} - 3\ V_{BE}) \quad (6)$$

Writing I_6 and I_7 as functions of the total I current gives

$$I_6 = \left(\frac{1}{2}\right)\left(1 - \frac{V_{DM}}{RI}\right) \quad (7)$$

$$I_7 = \left(\frac{1}{2}\right)\left(1 + \frac{V_{DM}}{RI}\right) \quad (8)$$

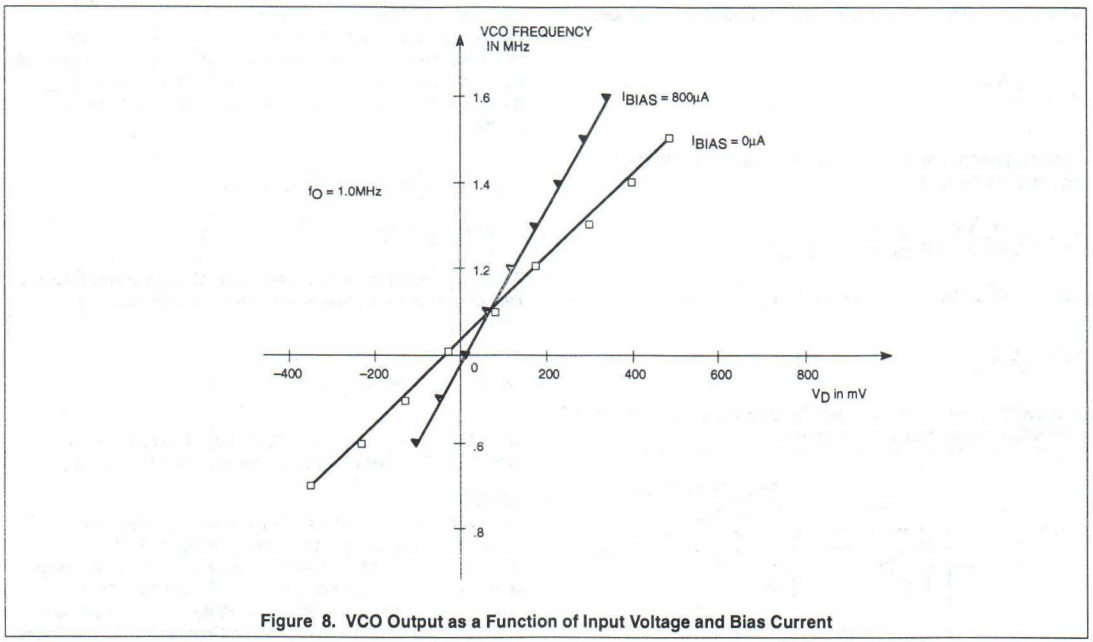


Figure 8. VCO Output as a Function of Input Voltage and Bias Current

Now consider variations in I_6 and I_7 while I remains constant

$$I_6 = (1 - x)\, I = \left(\frac{1}{2}\right)\left(1 - \frac{V_{DM}}{RI}\right) \quad (9)$$

$$I_6 = x\, I = \left(\frac{1}{2}\right)\left(1 + \frac{V_{DM}}{RI}\right) \quad (10)$$

where $0 \leq x \leq 1$. Thus x is defined to be

$$x = \left(\frac{1}{2}\right)\left(1 + \frac{V_{DM}}{RI}\right) \quad (11)$$

Currents I_6 and I_7 establish proportional currents in Q_{25}, Q_{26} and Q_{27} in a manner similar to the analysis above since the current in Q_{28} is a constant, or

$$I_O = I_{C28} = I_{E25} + I_{E26} + I_{E27A} + I_{E27B}$$

It can be shown that the D_7 - D_8 diode pair will cause identical differential currents to be reflected in both the Q_{25} - Q_{26} and the Q_{27A} - Q_{27B} differential amplifier pairs. Consequently, the constant-current of I_O, jointly shared by the differential amplifier pairs, will divide in each pair with the same x factor imbalance as in Equation 11.

$$I_{E25} + I_{E26} = xI_O \quad (12)$$

$$I_{E25} = I_{E26} = \left(\frac{x}{2}\right) I_O \quad (13)$$

$$I_{E27A} + I_{E27B} = (1-x)\, I_O \quad (14)$$

$$I_{E27A} = I_{E27B} = \left(\frac{1-x}{2}\right) I_O \quad (15)$$

Now consider placing a capacitor between the collectors of Q_{25} and Q_{26} (Pins 12 and 13). Oscillation will occur with the capacitor alternately being charged by Q_{21} and Q_{23} and constantly discharged by Q_{25} and Q26. When the Q_{21} and Q_{22} pair conducts, Q_{23} and Q_{24} will be off, causing a negative ramp voltage to appear at Pin 13 and a constant voltage at Pin 12 as shown in Figure 7. During the next half-cycle, the transistor roles and voltages are reversed. Capacitor discharge is via Q_{25} and Q_{26}, which act as constant-current sinks with current amplitudes as in Equation 13.

During each half-cycle, the capacitor voltage changes linearity by $2\Delta V$ volts in ΔT seconds, where

$$\Delta V = 2R_{20}\, I_O\left(\frac{x}{2} + \frac{1-x}{2}\right) = R_{20}\, I_O \quad (16)$$

and

$$\Delta T = \frac{C2\Delta V}{I_{E25}} \quad (17)$$

Combining these two equations with Equation 13 gives a half period of

$$\Delta T = \frac{4C\,R_{20}}{x} \qquad (18)$$

Utilizing Equation 11 with the ΔT expression gives the desired VCO frequency expression of

$$f_O = f_O'\left(\frac{1}{R_{16}}\right)\left[\frac{V_{DM}}{2(V_{CM} - 3\,V_{BE})}\right] \qquad (19)$$

where f_O' is the VCO's free-running frequency given by

$$f_O' = \frac{1}{22\,R_{20}\,C} \qquad (20)$$

Equation 19 shows that the oscillator frequency is a linear function of the differential voltage from the phase

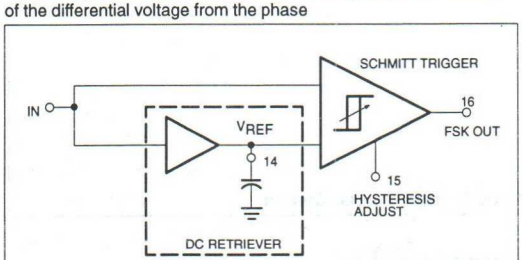


Figure 9. Post Detection Processor for FSK

comparator. Resistors R_{35} and R_{36} function to insure that an initial current imbalance exists between the Q_{25} - Q_{26} transistor pair and the dummy Q_{27}. This imbalance insures that the oscillator is self-starting when power is first applied to the circuit.

The VCO conversion gain is determined as

$$K_O = \frac{\partial f_O}{\partial V_{DM}} = \frac{f_O'}{RI}\ \text{Hz/V} \qquad (21)$$

which is valid as long as the transistor's V_{BE} changes are small with respect to the common-mode voltage. both f_O and K_O are inversely proportional to R, which has a strong positive temperature coefficient. An internal current I_R having an equal and opposite negative temperature coefficient is inserted into the VCO as shown in Figure 6.

Experimental determination of K_O can be found from the data of Figure 8 where K_O is the slope of either line. Numerically these results are for $I_{BIAS} = 0$.

$$K_O = 0.95\,\frac{MHz}{V} = 5.9 \times 10^6\,\frac{rad}{volt/sec} \qquad (22)$$

and for $I_{BIAS} = 800\mu A$

$$K_O = 1.7\,\frac{MHz}{V} = 10.45 \times 10^6\,\frac{rad}{volt/sec} \qquad (23)$$

It must be noted that the specific values obtained for K_O in the manner above are valid only for the 1.0MHz free-running frequency where the data was taken. However, good estimates for K_O at other free-running frequencies can be obtained by linearly scaling K_O to the desired f_O'. Thus, it is sometimes convenient to define a normalized K_O as

$$K_{O(norm)} = \frac{K_O}{f_O'} = 5.9\,\frac{rad}{V}\ (I_{BIAS} = 0)$$
$$= 10.45\,\frac{rad}{V}\ (I_{BIAS} = 800\mu A) \qquad (24)$$

The K_O estimate for any bias then can be obtained by multiplying the normalized conversion gain by the desired free-running frequency, or

$$K_O\ (\text{any } f_O') = K_{O(norm)}\ f_O' \qquad (25)$$

The additional VCO circuitry of Q_{29} through Q_{36} functions to produce the TTL and ECL compatible outputs at Pins 9 and 11.

Amplifier

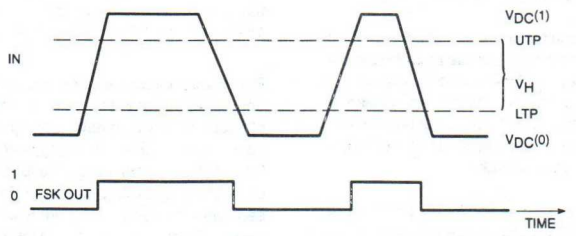
The difference-mode voltage from the phase comparator is extracted and amplified by the amplifier in Figure 1. The single-ended output from this amplifier serves as input signals for both the Schmitt Trigger and a second differential amplifier. Low-pass filtering with a large capacitance at Pin 14 produces a stable DC reference level as the second input to the Schmitt Trigger. When the PLL is locked, the voltage at Pin 14 is directly proportional to the difference between the input frequency and f_O'. thus Pin 14 provides the demodulated output for an FM input signal.

Schmitt Trigger

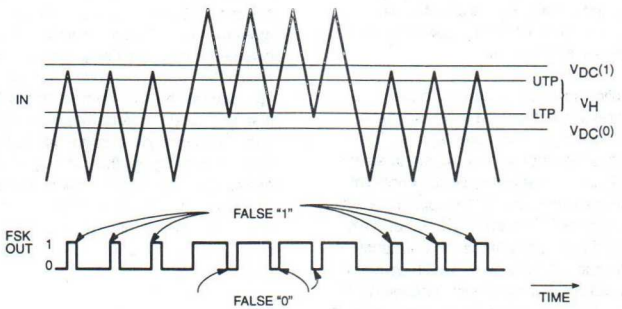
In FSK applications, the Pin 14 voltage will assume two different voltage levels corresponding to the mark and space input frequencies. A voltage comparator could be used to sense and convert these two voltage levels to logic compatible levels. However, at high data rates, V_{DM} will contain a considerable amount of carrier signal which can be removed by extensive filtering. Normally this complex filtering requires quite a few components, most all of which are external to the monolithic PLL. Also, since the control voltage for the comparator depends upon K_O and the deviations of the mark and space frequencies from f_O', the filtering has to be optimized for each different system utilized. However, the necessary DC reference level for the comparator is present in the PLL, but buried in carrier-frequency feedthrough which appears as noise in the system. A Schmitt Trigger with variable hysteresis can be used successfully to decode the FSK data without the need for extensive filtering.

Consider the system shown in Figure 9 where the input signal is the single-ended output derived from the amplifier section of the NE564. The DC retriever functions to establish a DC reference voltage for the Schmitt Trigger. The upper and lower trigger points are adjustable externally around the reference voltage giving the variable hysteresis. For very low data rates, carrier feedthrough will be negligible and the ideal situation depicted in Figure 10 results. Increased data rate produces the carrier feedthrough shown in Figure 10b, where false FSK outputs result because the feedthrough amplitude exceeds the hysteresis voltage. Having the capability to increase the hysteresis, as in Figure 10c, produces the desired FSK output in the presence of carrier feedthrough.

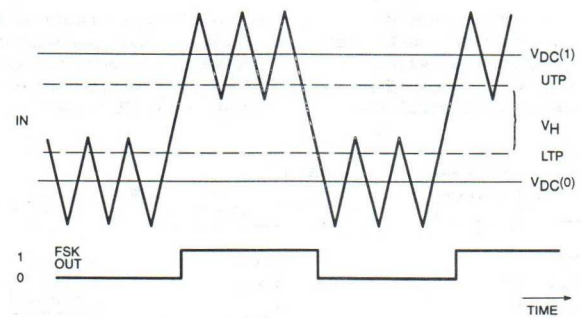
Another important factor to be considered is the temperature drift of the f_O' in the VCO. Small changes in f_O' will change the DC level of the input voltage to the Schmitt trigger. this DC voltage shift would produce errors in the FSK output in narrowband systems where the mark and space deviations in f_{IN} are less than the f_O' change with temperature. However, this effect can be eliminated if the DC or average value of the amplifier signal is retrieved and used as the reference voltage for the Schmitt trigger. In this manner, variations in the f_O' with temperature do not affect the FSK output.



a. Low Data Rates with Negligible Carrier Feedthrough



b. False FSK Outputs Due to Feedthrough and Low Hysteresis



c. Increased Hysteresis Restores Proper FSK Output In the Presence of Feedthrough

Figure 10. Waveshapes for FSK Decoding in the Post Detection Processor

Frequency synthesis with the NE564

AN180

FREQUENCY SYNTHESIS WITH THE NE564

Frequency multiplication can be achieved with the PLL in two ways:

a. Locking to a harmonic of the input signal

b. Insertion of a counter (digital frequency divider) in the loop.

Harmonic locking is simpler and usually can be achieved by setting the VCO free-running frequency to a multiple of the input frequency and allowing the PLL to lock. However, a limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. This limits the practical harmonic locking range to multiples of approximately less than ten. For larger multiples, the second scheme is more desirable.

A block diagram of the second scheme is shown in Figure 1a. Here, the loop is broken between the VCO and the phase comparator and a counter is inserted. In this case, the fundamental of the divided VCO frequency is locked to the input reference frequency so that the VCO is actually running at a multiple of the reference frequency. The amount of multiplication is determined by the counter An obvious practical application of this multiplication property is the use of the PLL in wide range frequency synthesizers.

In frequency multiplication applications, it is important to take into account that the phase comparator is actually a mixer and that its output contains sum and difference frequency components. The difference frequency is DC and is the error voltage which drives the VCO to keep the PLL in lock. The sum frequency components (of which the fundamental is twice the frequency of the input signal), if not well filtered, will induce incidental FM on the VCO output. This occurs because the VCO is running at many times the frequency of the input signal and the sum frequency component which appears on the control voltage to the VCO causes a periodic variation of its frequency about the desired multiple. For frequency multiplication, it is generally necessary to filter quite heavily to remove this sum frequency component. The tradeoff, of course, is a reduced capture range and a more under-damped loop transient response.

Producing a large number of frequencies with close spacing requires a counter with a large N for the system of Figure 1a. Large N values, in turn, require reference frequencies too low to be practical for commercially available crystals. To overcome this difficulty, a second counter (-M) is inserted as a prescaler as in Figure 1b to divide down the reference frequency input. This also gives more programming flexibility, since the synthesized output frequencies are functions of both M and N integers, each of which can be changed separately. As an example of fractional frequency synthesis, the two counters can be set to generate an output frequency exactly 16/3 of the input reference frequency. In this case N = 16, M = 3, and the initial f_O' is set to approximately 16/3 times the reference frequency input. The output always will be exactly 16/3 of the input frequency as long as the PLL remains in lock.

PLL frequency synthesizers based upon Figure 1b find wide applications in many types of communications systems that require precisely spaced channels having narrow bandwidths which are centered around relatively high frequencies. For example, Citizens Band (CB) transceiver applications require forty channels corresponding to forty different reference frequencies, each separated by 10kHz bandwidths and centered in the 26 27MHz range. Channel 4 uses 27.005MHz; Channel 5 uses 27.015MHz; Channel 6 uses 27.025MHz; and so on. These frequencies could be produced by using forty different crystals — one for each channel. However, this becomes expensive and adds unnecessary complexity to the system. Frequency-mixing techniques have been employed to reduce the number of crystals needed to less than one crystal per channel. For example, one common mixer design uses 14 crystals for 23 channels. As a general rule, most practical approaches that use numerous crystals and mixers to produce discrete frequencies require more than one crystal for every two channel frequencies produced. As the number of channels grows large, frequency synthesis using PLLs becomes more attractive, especially since usually only one or two crystals are needed. Frequency stability of all channels will be essentially the same as that of the crystal reference frequency. Reduced system complexity, size, weight, and power consumption are key advantages of PLL synthesizers.

Since the function of frequency synthesizers is to generate frequencies and not to linearly decode or demodulate input signals, digital PLLs are more commonly used than analog loops.

Analog PLLs also can be used for frequency synthesis applications. The 564 is particularly well suited for these applications because the loop is open between the VCO output and the phase comparator input. Also, the phase comparator input and VCO output are compatible with TTL counters.

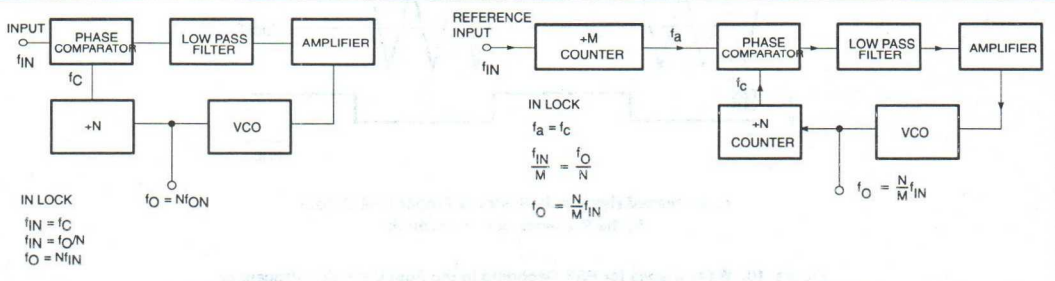
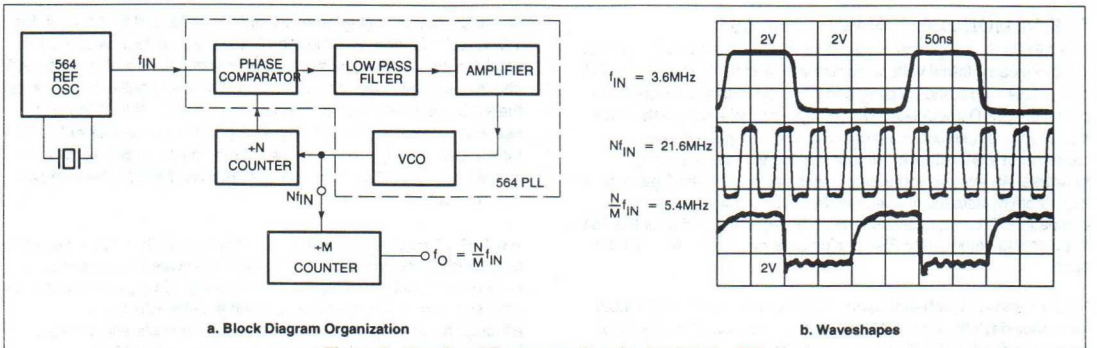


Figure 1. Frequency Synthesis Using PLLs



a. Block Diagram Organization

b. Waveshapes

Figure 2. Fractional Frequency Synthesis With the 564

NE564 FREQUENCY SYNTHESIS WITH CRYSTAL CONTROL

The system shown in Figure 2 has been used to generate frequencies of 5.4MHz and 21.6MHz from a 3.6MHz crystal-controlled source. This reference signal input is produced by using the crystal as the frequencydetermining element in the VCO of a second PLL. The thermal stability of all three frequencies will be the same as the stability afforded by the crystal. It may be necessary to place a small detuning capacitor in parallel with the crystal to precisely tune the PLL to the crystal's resonant frequency and to prevent oscillations at harmonics of the resonant frequency. The value of this tuning capacitance must always be kept considerably less than the value required to produce an f_O' without the crystal present. Otherwise the crystal will lose control and the input reference frequency will be set by the capacitor alone.

A recommendation for improved 564 operation is to utilize a divide-by-N counter in the loop which produces "square" waves for the phase comparator that have as close to a 50% duty cycle as possible. Normally, counters with even N values produce square wave outputs perfectly compatible for the phase comparator. Counters for odd N values more commonly produce unsymmetrical outputs that can be less desirable inputs to the phase comparator. An easy modification to "square up" odd divide-by-N counter outputs is to insert a single toggling flip-flop stage between the counter output and the phase comparator's input. This produces an effective 2N multiplication of the input frequency within the PLL. The extra factor of two is removed by a second toggle flip-flop whose input is the output from the first flip-flop. This is the same system as was previously shown in Figure 2a where the +N counter becomes a +2N and M = 2 for the second counter.

10.8MHz FSK decoder with NE564

AN1801

FSK DEMODULATION WITH THE 564

The NE564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5V power supply. Demodulated DC voltages associated with the mark and space frequencies are recovered with a single external capacitor in a DC retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 1 shows a high–frequency FSK decoder designed for input frequency deviations of +1.0MHz centered around a free-running frequency of 10.8MHz. The value of the timing capacitance required was estimated from Figure 4a to be approximately 40pF. A trimmer capacitor was added to fine tune f_O' to 10.8MHz.

Figure 2b indicates that the +1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero Pin 2 bias current. While strictly this figure is appropriate only for 5MHz, it can be used as a guide for lock range estimates at other f_O' frequencies.

A more thorough analysis confirms these lock range conclusions and serves as a guide for designing other systems. The closed-loop gain of the PLL is equal to the system's lock range and is found as the product of K_d and K_o adjusted to 10.8MHz

$$2\omega_L = K_V = K_d K_o \qquad (1)$$

$$2\omega_L = \left(0.46 \frac{\text{volt}}{\text{radian}}\right)\left(0.875 \frac{\text{MHz}}{\text{volt}}\right) \times \left(2\pi \times 10.8 \times 10^6 \frac{\text{radian}}{\text{sec}}\right)$$

$$2\omega_L = 2.73 \times 10^7 \frac{\text{radian}}{\text{sec}} \text{ (Lock range total)}$$

Thus Pin 2 could be left as an open circuit and the internally set closed-loop gain would be adequate for tracking the mark and space input frequencies. However, to be safe, a bias adjustment as shown in Figure 1 is recommended to allow for K_d and K_o variations from device to device.

Designing for a capture range of approximately 700kHz gives a low-pass filter time constant of

$$\omega_c \approx \sqrt{\frac{\omega_L}{\tau}}\ 2\omega_L = K_V = 2.73 \times 10^7 \qquad (2)$$

$$(2\pi \times 700 \times 10^3) \approx \sqrt{\frac{2.73 \times 10^7}{\tau}}$$

$$\tau = 1.8\text{ms}$$

Therefore, choose the low–pass filter capacitor as

$$C = \frac{\tau}{R} = \frac{1.41\mu\text{s}}{1.3\text{k}} \approx 1\text{nF} \qquad (3)$$

Two 1nF capacitors were selected for the design.

Capacitive coupling was used for the FSK input and is recommended to avoid DC feedthrough. This DC voltage would act as a DC offset to shift f_O' from 1 0.8MHz. Balanced biasing with the 1.0kΩ resistors from Pin 7 to Pins 3 and 6 also is recommended to establish symmetrical, quiescent current conditions in the limiter and phase comparator sections of the 564. The 470Ω pull–up resistor for the VCO output was found to give a rise time less than 10ns. This rise time was further reduced by adding the 100Ω resistor between Pins 9 and 11. Figure 3 shows an unmodulated 10.8MHz input signal and the VCO output. Note the approximate 90° phase lag of the VCO output.

A 0.1μF DC retriever capacitor (Pin 14) has less than 1Ω impedance at f_O, and represents a good compromise between high baud rates (~100k baud) at f_O' and higher-order filtering. If very high baud rates are used, this capacitor could be made smaller with an accompanyIng Increase in the Schmitt trigger hysteresis voltage. The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in Figure 5 for 20k, 500k, and 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparator's output voltages with respect to each other and to the FSK output. The high frequency sum components of the input and VCO frequency also are visible as noise on the phase comparator's outputs.

The phase comparator's outputs exhibit the waveshapes shown in Figure 4 when the FM input is changed from a square wave FSK modulation to a triangular sweep at a 100Hz modulation rate. The amplitude of the triangular sweep was increased from that used with square wave modulation, causing the loop to be driven in and out of lock. The loop is locked during the smooth, linear portions of the phase comparator's waveshapes and locked during the remaining portions. Lock and capture frequencies were measured for a Pin 2 bias current of 375μA and f_O' = 10.8MHz as:

Lock: f_{L1} = 6.2MHz f_{L2} = 16.4MHz

Capture: f_{c1} = 9.3MHz f_{c2} = 12.2MHz *P

When the loop is locked, the phase detector's outputs represent the demodulated FM output. When unlocked, high frequency harmonics are present, increasing in amplitude until lock is achieved.

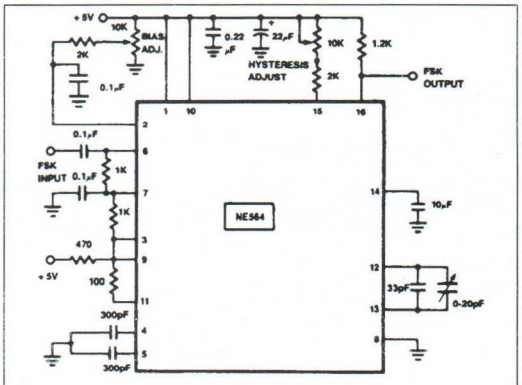
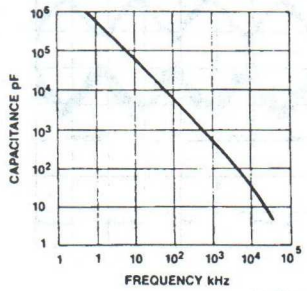
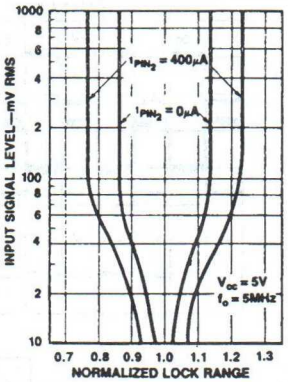


Figure 1. 10.8MHz FSK Decoder Using the NE564



a. VCP Timing Capacitor vs Frequency



b. Lock Range vs Input Signal and Bias Current

Figure 2. NE564 Characteristics

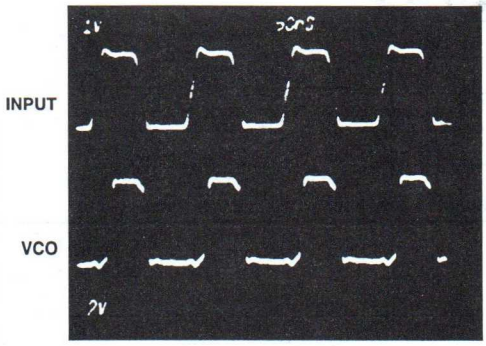


Figure 3. PLL Input and VCO Output for Phase and Frequency Lock at 10.8MHz

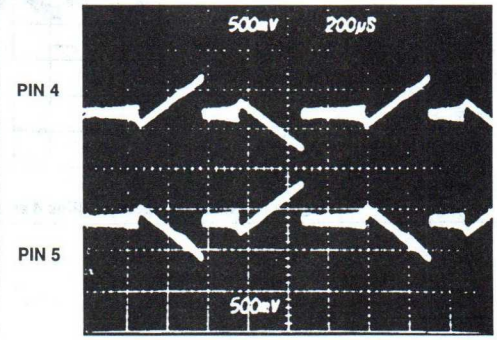
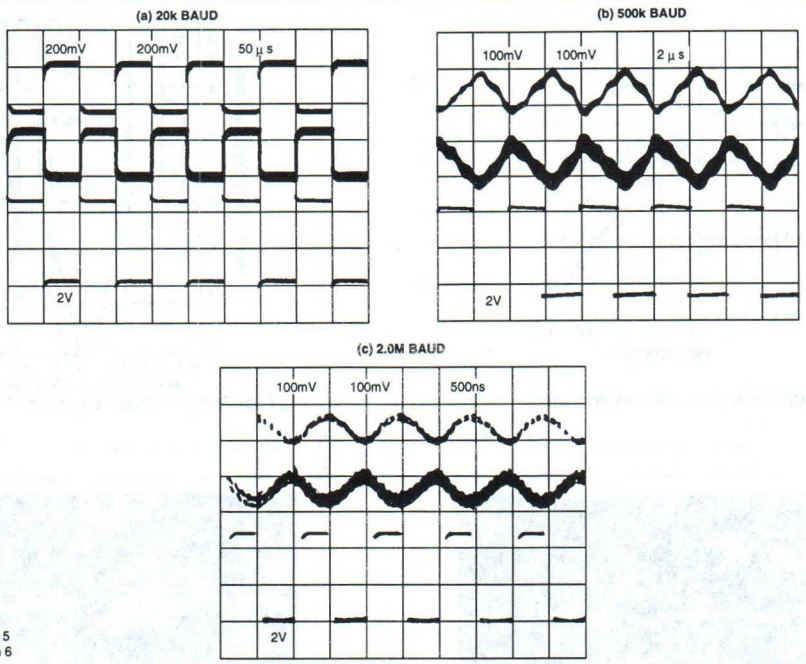


Figure 4. Phase Comparator Outputs Showing Lock and Capture Ranges



NOTE:
Top trace — Pin 4
Center trace — Pin 5
Bottom trace — Pin 6

Figure 5. Phase Comparator (Pins 4 and 5) and FSK (Pin 16) Outputs for Various Data Rates

A 6MHz FSK converter design example for the NE564

AN181

Design Example

It is desired to design an FSK converter operating at 6MHz with deviation of ±1%. Supply voltage is 5V. Input to the 564 is from a radio receiver with an amplitude of $0.5V_{RMS}$. Worst case S/N is 10dB. An overall loop damping factor of 0.5 is specified (ζ).

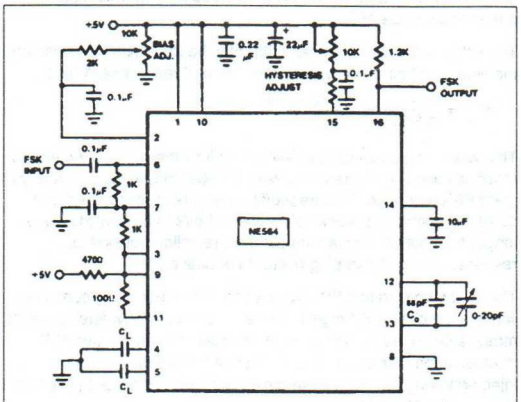


Figure 1. FSK Decoder Using the 564

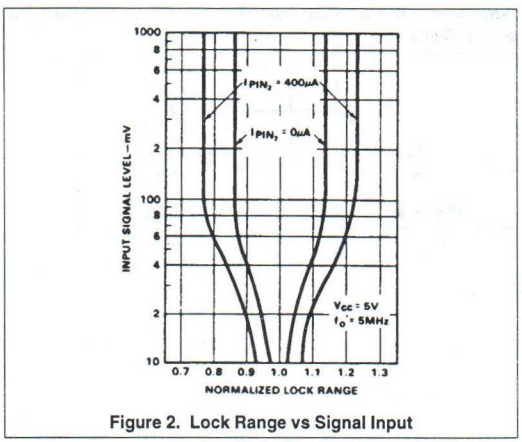


Figure 2. Lock Range vs Signal Input

Using the circuit in Figure 1

First the frequency determining capacitor must be established. Using the equation

$$f_O = \frac{1}{22R_CC_O}$$

where R_C is the internal resistance in the VCO oscillator equal to 100Ω. Given two parameters the third is calculated f_O = 6MHz; therefore

$$C_O = \frac{1}{22 \times 100 \times 6\ 10^6} = 75pF$$

A parallel 2 - 20pF trimmer and a 68pF ±5% fixed mica capacitor is chosen.

Next, signal level versus bias current and lock range is examined.

The signal input to the 564 is specified to be $0.5V_{RMS}$; in the lock range graph, the input level is well within the limiting region of the 564. Thus, no external AM limiter circuit is required and a 10dB S/N (3.1:1) min. should provide reliable communication with a narrow deviation of ±1% (±60kHz) and there is no problem with adequate lock range as it pertains to bias current. We are free to use any loop gain necessary. The bias current sinking into Pin 2 is set to an initial value of 200µA.

It's now possible to determine the damping factor of the closed–loop. First, the natural frequency of the loop is calculated from the relationship

$$\omega_n = \frac{\sqrt{K_OK_D}}{\tau} \qquad (1.)$$

where

K_O = VCO conversion gain in $\frac{\text{radians}}{\text{sec} \cdot \text{volt}}$

K_O = Phase detector conversion gain in $\frac{\text{volts}}{\text{radian}}$

τ = loop filter time constant in seconds.

For f_O = 6MHz and I_B = 200µA, K_O may be derived from Figure 3a by first constructing an extrapolated transfer line with slope one-quarter of the angle between the existing I_B = 0 and I_B = 800 plots.

Interpolation gives

$$K_O \approx \frac{1.48 - 1.25MHz}{0.4 - 0.2V} = \frac{\Delta f_O}{\Delta V_O}$$

Multiplying Δf_O by 2π results in

$$K_O = \frac{1.45 \times 10^6 \text{rad/sec}}{0.2V}$$

$$= 7.2 \times 10^6 \frac{\text{radians}}{\text{sec} \cdot \text{volt}}$$

Next, using the K_D graph (Figure 3b), ±1 radlan (–90° ±57°); i.e., $\Delta\theta$ = 1 radian, results in an output of 0.6V/rad.

Therefore, $K_D = \frac{0.6}{\text{rad}} = 0.6V/\text{rad}$ at I_B = 200µA.

The value obtained for K_O is for data taken at 1MHz and must be multiplied by 6 in order to find the correct value.

Therefore, $K_O = 0.6 \times 7.2 \times 10^6 \frac{\text{radians}}{\text{sec} \cdot \text{volt}}$

$$(6MHz) = 4.34 \times 10^7 \frac{\text{radians}}{\text{sec} \cdot \text{volt}}$$

$$K_OK_D = K_V = (4.34 \times 10^7)(0.6) = 2.6 \times 10^7$$

The damping factor specified (0.5) is now used to determine the necessary filter time constant (Pins 4, 5).

$$\xi = \frac{1}{2\pi\sqrt{\frac{K_OK_D}{\tau}}} = \frac{1}{2\sqrt{K_V\tau}} = \frac{\omega_n}{2K_V} \qquad (2.)$$

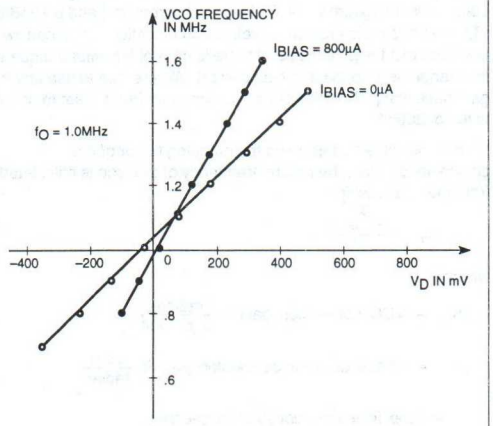
$$\therefore \tau = \frac{1}{(4)\ (2.6\ 10^7)\ (0.5)^2} = 38ns$$

Note that the filters on Pins 4 and 5 operate differentially with the net effect that break frequency is

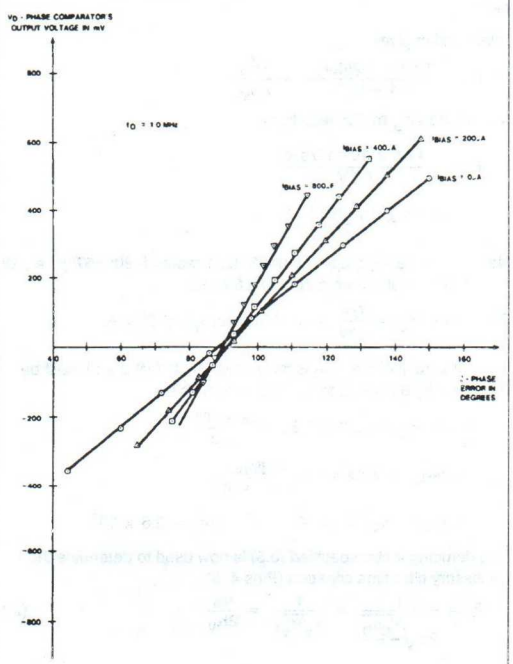
$$\omega_p = \frac{1}{RC} \text{ (single pole filter – 3dB freq.)}$$

A 6MHz FSK converter design example for the NE564

AN181



a. VCO Output Frequency as a Function of Input Voltage and Bias Current (K_O)



b. Variation of the Phase Comparator's Output Voltage vs Phase Error and Bias Current (K_D)

Figure 3.

Now solving for ω_n using (1):

$$\omega_n = \left[\frac{(2.6 \times 10^7)}{(3.8 \times 10^{-8})}\right]^{1/2} = 26 \times 10^6 \frac{\text{radians}}{\text{sec}}$$

f_n = 4.16MHz (natural frequency of the loop and approximate one–sided capture B.W.)

The value of the loop filter capacitor may be determined by dividing the time constant by the value of the internal resistance, 1.3kΩ.

$$C_L = \frac{\tau}{1.3k\Omega} = \frac{3.8 \times 10^{-8}}{1.3 \times 10^3} = 29pF$$

This value filter time constant will give a less than-critically-damped response allowing the fast excursion in VCO frequency necessary to good FSK reception. The tradeoff between response speed and carrier frequency harmonic rejection will have to be considered. A longer time constant gives more carrier rejection but slower response and less damping (Refer to equation 2).

The next step is to test the circuit under actual operating conditions with the specified FSK signal. The level on Pin 15 (hysteresis adjust) must be set in the vicinity of +1.4V in order to attain proper FSK demodulation. Final signal tests may be carried out with noise injected through a resistive summing network at the input (Pin 6) to simulate the 10dB S/N.

Note that the loop filter response actually operates on the frequency spectrum above (+) and below (–) the carrier center frequency, or center of deviation, for a symmetric FM or FSK signal. This may be seen in Figure 4.

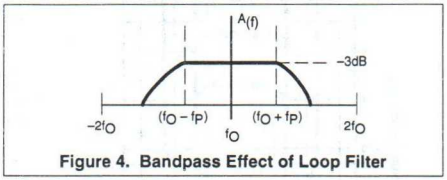


Figure 4. Bandpass Effect of Loop Filter

Clock regenerator with crystal-controlled phase-locked loop VCO (NE564)

AN182

INTRODUCTION

In order to obtain a local clock signal in Multiplexed Data Transmission systems, a phase and frequency coherent method of signal extraction is required. A Master-Slave system using the quartz crystal as the primary frequency determining element in a phase-lock loop VCO is used to reproduce a phase coherent clock from an asynchronous Data Stream.

The NE564, a versatile phase-locked loop (PLL) operating at frequencies of 50MHz, has inputs and outputs designed to be TTL compatible. The Philips Semiconductors NE564 is used to generate the phase-locked, crystal-stabilized clock reference signal.

Its particular adaptation, for use with a crystal-controlled VCO instead of the usual RC control elements, requires a brief review of the principles of the Phase-Lock Loop design.

The NE564 Phase-Locked Loop is a fully contained system, including limiter, phase detector, VCO, DC amplifiers, DC retriever and output comparator (reference Figure 1). For the clock regeneration system to be discussed, the portions of the NE554 implemented are the input limiter, phase detector and VCO.

The signal limiter amplifies low level inputs (until saturation is reached, which is typically 60mV_{P-P} for the NE564). The signal limiter output is fed to the phase detector, where the "unknown" input is compared to the "known" VCO frequency of the NE564. The differential error signal that is generated is fed through a DC amplifier and a voltage-to-current converter. The change in the current generated forces the VCO frequency to vary in its frequency and/or phase relationship, such that a θ of 90° lagging is obtained (the actual phase relationship may be somewhat less than 90° depending upon the K_dK_O (gain) product of the NE564 at the operating frequency and bias current). The external filtering incorporated at Pins 4 and 5 control the dynamic frequency response and loop stability criteria.

The NE564 is a first order system; therefore, the use of single capacitors (at Pins 4 and 5) will automatically create a "second-order" system. An RC series filter combination will cause a lead-lag condition that will permit dynamic selectivity, along with closed-loop stability.

LOOP GAIN FUNCTIONS

The phase detector conversion gain (K_d) and the VCO conversion gain (K_O) determine, in large part, the lock range, capture range and linearity characteristics of the NE564. These device parameters are both dependent upon bias current and operating frequency. Some typical curves for each of the parameters are shown for the NE564 in Figures 2 and 3.

CLOCK REGENERATOR CIRCUIT

The basic building blocks of the clock regenerator circuit are shown in Figure 4. The PLL is shown as a frequency multiplier incorporating a divide by "N" in the VCO phase detector feedback loop. The functions of the ringing circuit and the NE527 high-speed comparator will be discussed later.

The waveforms of Figure 5 indicate the waveforms transmitted over a T1 line. The bipolar signal transmitted has "no" DC components induced in the transmission line (reference should be made to the effect of normal mode and common effects on signal information). When transmitted over telephone wire pairs, the resultant signal (at the receive end) will have been degraded in both waveshape and signal-to-noise ratios. Typical attenuation factors for a T1 line are -30dB per 6000 feet. In addition, pair-to-pair crosstalk can degrade signal-to-noise ratios. The energy transmitted in the bipolar system of signal transfer is centered at 772kHz (generated by the bit format).

At the receiving end the bipolar signal information is converted to a unipolar pulse train after being amplified, filtered and fed through an automatic level control circuit. Some types of PCM systems use the rectified and filtered DC (average) to control the phase of the regenerator clock; however, in newer systems, bipolar signals are processed (or preconditioned) by terminal common equipment resulting in unipolar information.

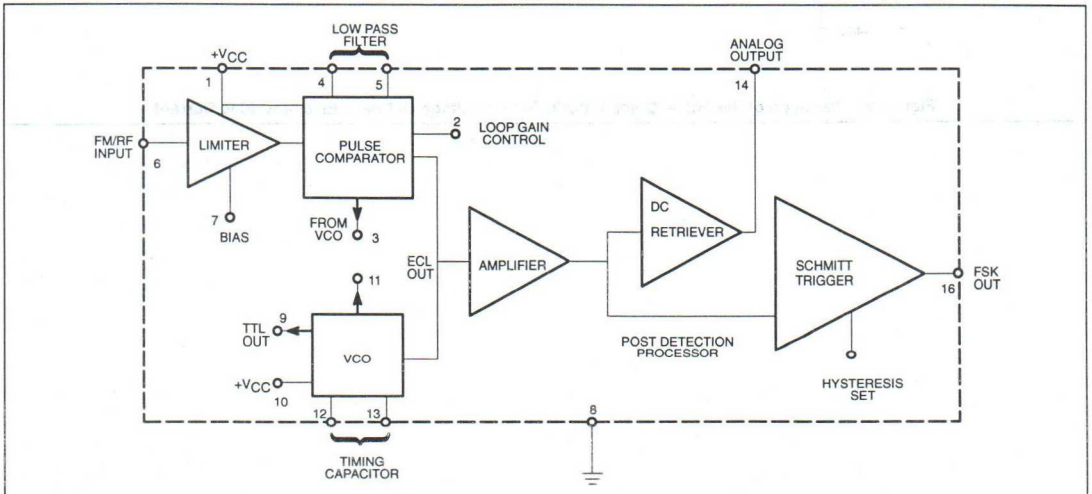


Figure 1.

Clock regenerator with crystal-controlled phase-locked loop VCO (NE564)

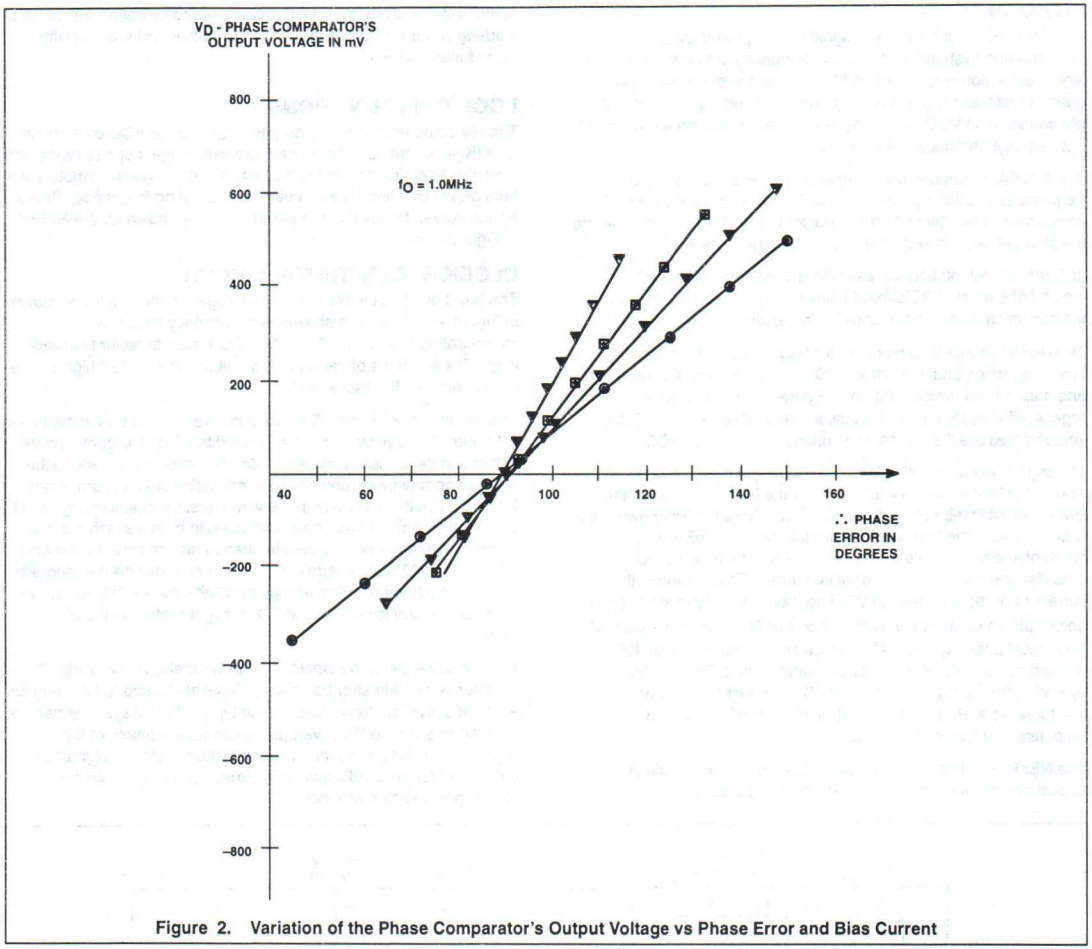


Figure 2. Variation of the Phase Comparator's Output Voltage vs Phase Error and Bias Current

Clock regenerator with crystal-controlled phase-locked loop VCO (NE564)

AN182

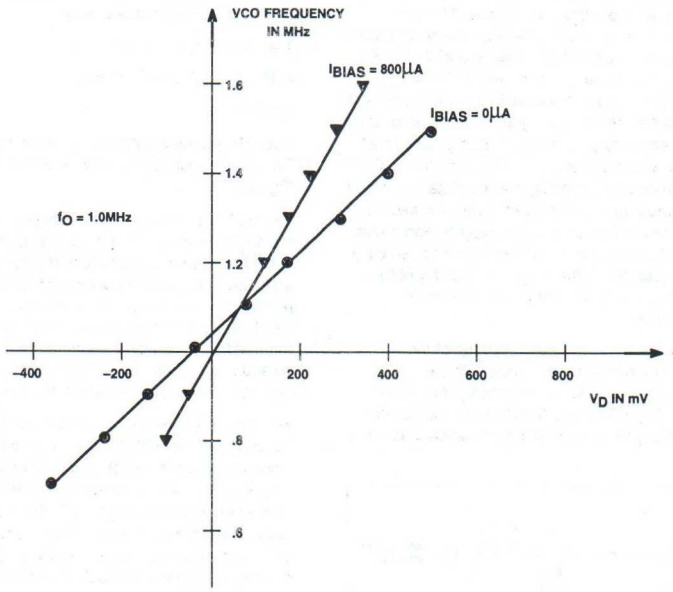


Figure 3. VCO Output Frequency as a Function of Input Voltage and Bias Current

T1 Data Transmission

The bipolar signal, as transmitted on a T1 line, appears below with the original binary, converted unipolar and clock waveform (reference Figure 5).

The bipolar signal, when transmitted over standard wire pairs, will be degraded both in wave shape and signal-to-noise by the time it reaches the signal repeater. This is due to the attenuation factor of the cable which is nearly -30dB for 6000 ft. In addition, pair-to-pair crosstalk degrades signal-to-noise. The energy in the transmitted bipolar signal is centered at 772kHz due to the particular bit format. Bipolar signals have no DC offset.

At each receiving station the bipolar signal is amplified, filtered and fed through an automatic level control circuit. A full wave rectified signal is then sent to the clock regeneration circuit. This is essentially the format followed by some of the original T1 repeater equipment. The clock regeneration circuit described here could be adapted to this system.

THE T1 SPECTRUM

The bipolar signal is similar to NRZ data in that it does not contain carrier information. In order to give the PLL coherent frequency

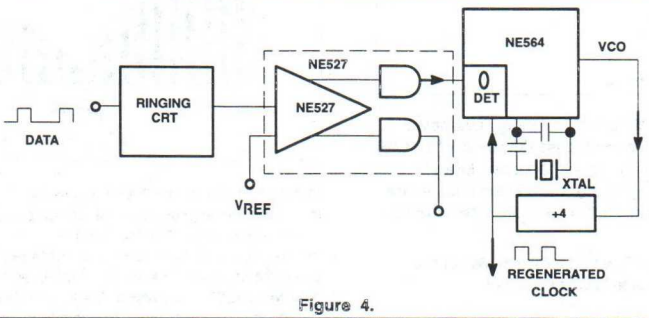


Figure 4.

Clock regenerator with crystal-controlled phase-locked loop VCO (NE564)

AN182

information sufficient to obtain "capture" and lock, carrier components must be obtained from the data stream. The time duration of the frequency information fed to the PLL is also important in order to obtain accurate and stable information to update the PLL. In order to begin the extraction of frequency information, the positive-going portions of the bipolar data signals are used to drive a class "C" transistor tank circuit (reference Figure 4) which is sharply tuned to the basic clock frequency (1.544MHz). Each positive half cycle of data then starts a wave train of coherent information which is phase synchronous with each succeeding positive data bit. When the LC tank is optimally tuned, relatively extended periods without data bits can be tolerated with minimal loss of frequency and phase information. The combination of good short-term frequency stability of the high "Q" LC tank, coupled with the long-term stability of the crystal-controlled VCO, is the foundation of the NE564 clock regeneration system accuracy.

It must be emphasized that dda pulse synchronization of the preprocessing circuit must be frequency coherent with the fundamental period of the time base to be extracted. That is, if the time period of the clock is $1/f_C = T$, where f_C is the clock frequency, then the spacing between any positive code bit sequence must be n x t (reference Figure 6).

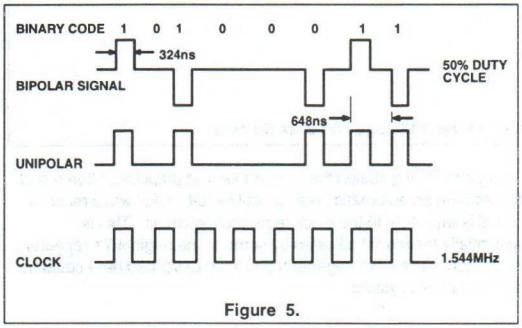


Figure 5.

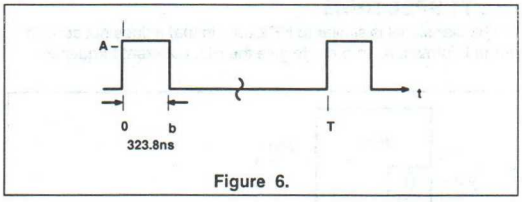


Figure 6.

Looking at the spectral analysis of the relative energy available to the clock extraction circuitry (with a worst-case duty cycle of 1 of 16) will demonstrate the need for enhancing the particular desired frequency component before applying the signal to the Phase-Lock Loop. For f_O = 1.544MHz, the period is T = 647.67ns. The pulse or bit width is 323.8ns.

Here the bit duration 323.8ns = b. The Fourier expansion of the discrete spectrum is related by the following equation:

(Ab)I sin(rt) I FInI T I n~iib In 0,1,2 (1)

The basic frequency component resulting from various bit spacing factors is defined by the equation

f = 1/T

If we consider the special case of a single pulse present out of 16 bipolar or 32NRZ periods, then

T = 16 bipolar bit times

= 16 x 647.67ns = 10.36ms

f = 96.5kHz

Accordingly, the spectral lines will be spaced in multiples of 96.5kHz. The spectrum for this particular worst case condition is shown in Figure 7 below.

It is evident that as the bit spacing increases to the point where f_O is the 16th harmonic of the fundamental, very little f_O energy is available to drive a phase-lock regeneration circuit. $F_{(16)}$ is also ineffective since it is an even subharmonic of f_O. The PLL will not normally lock to even harmonics, in fact, an error signal is produced which tends to force the VCO out of lock. This fact further stresses the need for preprocessing in the frequency domain. The class "C" pulsed resonant tank significantly multiplies the magnitude of the f_O spectral component and filters out unwanted subharmonics.

The loop error voltage available from the phase detector for phase correction of the VCO is directly related to the product of the incoming coherent spectral energy multiplied in the balanced mixer with the reference signal derived from the VCO. Since the phase error information is integrated in the loop filters, the instantaneous magnitude of the DC error voltage is proportional to the time integral of coherent mixer products. Thus, as the magnitude and time duration of the desired frequency component is in creased in the preprocessing circuitry, the VCO phase accuracy is greatly improved. Capture time is obviously enhanced also.

The signal from the tuned tank is buffered by a FET follower N-channel enhancement mode device (reference Figure 12). This provides power gain with virtually no loading on the tank circuit and avoids degrading the "Q". The buffered signal is then fed to a high-speed comparator (Philips Semiconductors' NE527) which allows for waveform symmetry adjustment in addition to providing a standard TTL output to drive the NE564 PLL.

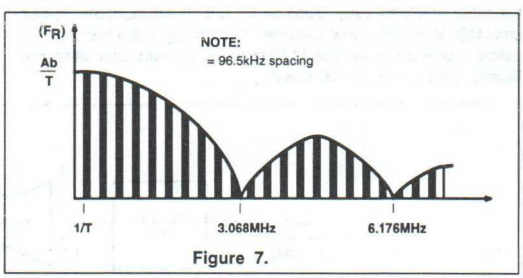


Figure 7.

In the particular circuit shown in Figure 12, the 1.544MHz information is applied to the phase detector input of the NE564 Phase-Lock Loop. The VCO, however, is operated at four (4) times this frequency in order to take advantage of economical and readily available crystals. The VCO signal is fed through a divide-by-four counter (74LS73) to provide the Phase Detector reference and final regenerated clock signal. To avoid loading, the clock signal (1.544MHz) is buffered by the 75451 peripheral driver which provides a high-speed open collector TTL output.. The input signal is AC coupled in order to reduce DC bias errors in the Phase Detector caused by "O" level variations.

Clock regenerator with crystal-controlled phase-locked loop VCO (NE564)

AN182

The Crystal

The crystal used was chosen to match the NE564 VCO drive characteristics. It is an "AT" cut oscillator crystal which operates near the anti-resonate or "parallel" mode in this circuit. The crystal may have to be fine-tuned, as indicated in Figure 8. The pulling characteristic of the crystal is adequate to allow for 0 to 70°C operational drift plus initial and aging accuracy tolerance factors and still retain lock between master and slave station VCXOs. The average lock range at room temperature with one of sixteen data bits present is typically 1000Hz for a 6.176MHz crystal with a capture range greater than 500Hz.

For VCO operation at 6.176MHz, C_S is 22pF, C_C is 18pF, and C_t, a 1 - 8pF trimmer capacitor (reference Figure 8).

NE564 CRYSTAL-CONTROLLED VCO

As shown in Figure 6, the crystal is operated with a series capacitor. When properly trimmed, this allows the crystal to operate near the series resonant mode. A crystal manufactured to operate in the series resonant mode will do so only if it sees a pure resistance looking into the oscillator terminals. The circuit below shows an oscillator which looks inductive with the equivalent crystal circuit and trimmer capacitor C_t (reference Figure 9).

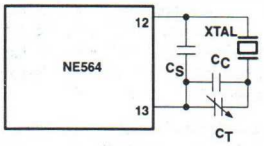
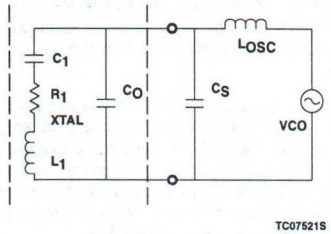
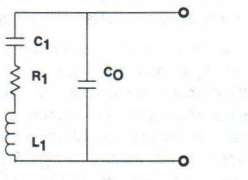


Figure 8.



NOTES:
C_O = XTAL Shunt capacitors
C_1 = Equivalent series resonant arm capacitance
L_1 = Equivalent Motional Inductance
R_1 = Equivalent crystal series resistance
C_S = External shunt or stray capacitance

Figure 9.



NOTES:
C_1 = Motional capacitance
C_0 = Shunt capacitance
R_1 = Equivalent Resistance
L_1 = Equivalent Inductance

Figure 10. Basic Crystal Equivalent Circuit

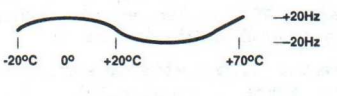


Figure 11. Design Example

If L_O is small and the internal gain of the device high over a wide frequency range, L_O may resonate with the C_O of the crystal at a very high frequency. Under certain conditions the circuit may even tend to operate in the 3rd overtone mode unless measures are taken to roll-off the circuit gain. This is the purpose of C_S in Figure 8. Since the gain or the VCO is a factor in spurious oscillation, the current injected into Pin 2 will also have an effect in this respect. (K_O increases with I_2). At higher operating frequencies this parameter may become more critical in attaining stable start ups in the desired frequency mode. Obviously the size of C_S must be smaller than the value needed to cause free running near the desired frequency without the crystal connected.

CRYSTAL SPECIFICATION

Crystals may be manufactured to operate in either the series mode with no external capacitance (purely resistive load) or in the parallel mode with a specified value of load capacitance. The 564 tends to operate at a frequency above the specified value when a series mode crystal is used, for a design frequency of 6.176000MHz and zero load capacitance. Referring to Figure 8, for C_S = 10pF and C_T = 10pF the average center frequency for an NE564 sample measured in the lab was 6181.192kHz. For the same C_S, but with C_T equal to 60pF, f_O measured 6176.565kHz. A second crystal showed a spread of 6176.600kHz to 6160.855kHz. The effect of the VCO was to pull the crystal to a frequency above its design value. This effect is then nearly tuned out by the external capacitances C_S

Clock regenerator with crystal-controlled phase-locked loop VCO (NE564)

AN182

and C_T. If C_T is sufficiently increased, the crystal will see a purely resistive load and operate at its rated frequency.

A second approach is to specify a crystal which is to operate near the anti-resonate or parallel mode. Normally this is done with a certain value of external load capacitance specified by the customer which matches the existing circuit parameters. The maximum difference between series and parallel resonance for any crystal is 0.5% of f_O (series resonant mode); for f_R = 6.126MHz, 0.5% of f_R = 30kHz. The usual value would be lower than this.

r_O = electromechanical coupling factor, f_a = parallel resonant frequency). The particular cut of the crystal material determines the drift response over temperature. For oscillator applications, the AT cut offers the best over-all stability over a wide frequency and temperature range. Final design uses second approach.

For a stability or total tolerance of ±15ppm over the rated operating range of -20°C to +70°C, a certain manufacturer's crystal actually performed as shown above (Refer to Figure 11).

Calibration accuracy is the allowable frequency tolerance at the reference temperature, i.e., +10ppm @ 25°C.

Third, is a long-term drift spec which determines the customer's maximum allowable drift due to aging effects. An acceptable value in quality crystals is +2ppm/year.

Using our reference crystal of 6.176MHz and the above specifications, the crystal limits over a 1 year period would be:

Temperature stability: ±15ppm x 6.176 = ±93Hz

Calibration tolerance: ±10ppm x 6.176 = ±62Hz

@25°C Long term drift: ±2ppm x 1 x 6.176 = ±12Hz

Total: (+ 1 67Hz)

The above figure of ±167Hz then determines the capture and lock range over which two crystal stabilized VCOs must track under worst case conditions when the exact same crystal specifications are used for master and slave units within an operational system.

Crystal Specifications

'AT' Cut Oscillator Type

Fundamental mode operation HC-33 Case (Standard)

Calibration tolerance: ±15ppm @ 25°C

Temperature stability: ±15ppm; -15°C to +65°C

Circuit operating condition: Parallel resonance

Frequency specified: 6.176000MHz

Part designation: Croven #A330 DEF-32 or equivalent

Setup Procedure

Referring to Figure 12 the following setup procedure will aid the user in establishing proper circuit operation.

Regulated supply voltage of +5V and -6V are required. Current drain on the +5V line is @100mA, and 6mA for the -6V.

With proper voltage applied, (1) First check the supply currents to be sure they are in the range indicated above. (2) Check the operation of the NE564 VCXO by looking at Pln 9 with an oscilloscope (see Figure 13). A reasonably symmetric square wave should be present having a frequency near 6.1MHz. (3) Attach a DVM across the 2k resistor which feeds Pin 2 of the NE564 and adjust for a reading of 2.00V, indicating a $1mA_{DC}$ current flowing into Pin 2 (The (+) lead of the DVM should be connected to the end of t he 2k resistor which ties to the wiper of the 10k pot and the (-) lead to Pin 2 of the 564; reference Figure 14). (4) The exact center frequency is set by adjusting C_t, the crystal trimmer cap, for exactly 6.176000MHz with no signal input (this sets the center frequency of the VCXO to free-run in the center of the capture range). (5) Enable strobe 'A' and 'B' with a +2.7V min. to +5V max. level. Apply a standard 1.544Mb/s NRZ data signal to the input terminal terminated in 50W. The amplitude should be +3 to +5V (0 to peak). Set the duty cycle for 1 bit in a 16-bit period. Note the data generator must be driven from a crystal-controlled master oscillator also adjusted for a center data rate of 1.544000Mb/s. Monitor the buffered output of the ringing circuit with a scope connected to the source of the SD213 (Figure 15). The waveform should appear as in Figure 17. (6) Adjust tank trimmer cap C_T for a maximum amplitude and note that the cycle period should be 647ns. (7) Now monitor the comparator output signal at Pin 7 and adjust R_t for a 50% duty cycle. The same signal will appear at Pin 5 of the NE527 except it will be inverted. The signal on Pin 7 of the NE527 and Pin 6 of the NE564 should appear as shown in Figure 19. Now attach one lead of a dual-trace scope to Pin 7 of the NE527 and the other to Pin 3 of the NE564 as shown (Figure 16).

The two signals should be in phase-locked with an approximate 90° differential as shown in Figure 20 (data signal applied to @ 1.544Mb/s). If lock does not occur a slight trimming of the crystal trimmer CT should connect for slight differences in master-to-slave crystal tolerance. It is recommended that master and slave crystals be of the exact same design and specification to insure optimal tracking over time and temperature. A recommended manufacturer and part number appears at the end of this application note for your convenience.

Once lock is attained, move one lead of the dual-trace scope to the buffered output of the 75451 Pin 3 leaving the other scope probe on Pin 6 of the NE564. The phase-locked waveform should appear as In Figure 25. If a data word generator Is being used, you may check overall operation for various bit patterns by synchronizing the scope trigger on the "end of word" pulse then observe the phase error effect as different combinations are fed in.

PHASE JITTER

When operating with real-time data transmission, the PLL loop filters must be optimized to minimize regenerated clock jitter. A good grade of mylar capacitor is recommended as connected to Pins 4 and 5 of the NE564. A simple pair of shunt-connected loop filter caps of 0.33mF to 0.76mF was found to be adequate.

Clock regenerator with crystal-controlled phase-locked loop VCO (NE564)

AN182

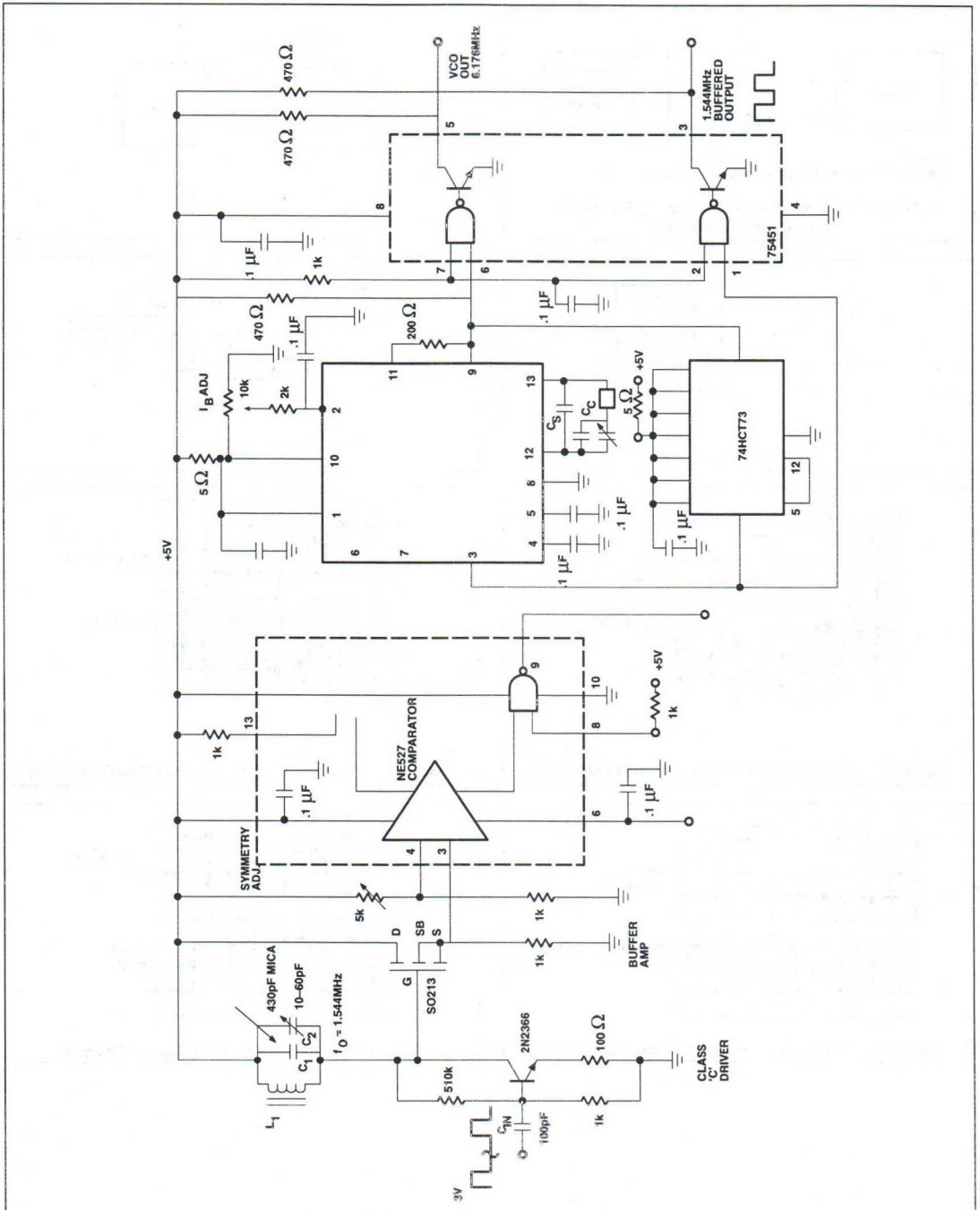
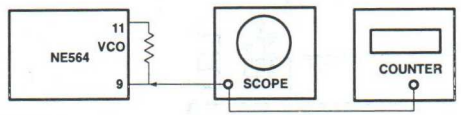


Figure 12. Data Transmission System Clock Regenerator

Clock regenerator with crystal-controlled phase-locked loop VCO (NE564)

AN182



NOTE:
Check VCO free–running frequency and output waveshape.

Figure 13. Check VCO Free-Running Frequency and Output Waveshape

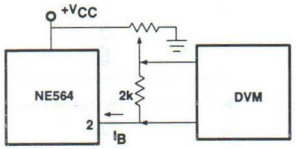


Figure 14.

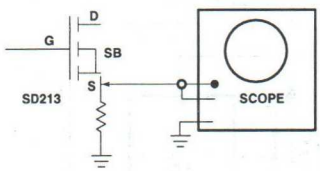


Figure 15.

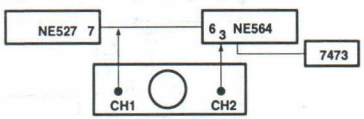


Figure 16.

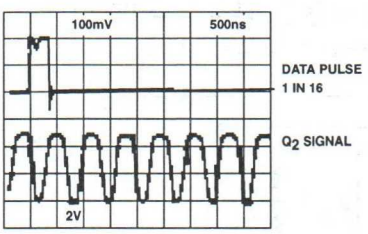


Figure 17. Ringing Circuit Response (1 Data Pulse in 16)

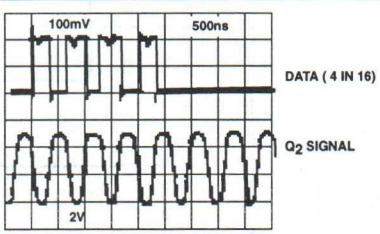


Figure 18. Ringing Circuit Response (4 Data Pulse in 16)

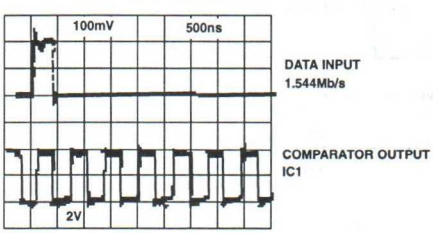


Figure 19. Ringing Circuit to Square Wave Conversion

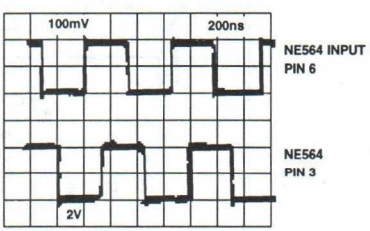


Figure 20. Phase Comparator Signals (in Lock)

Clock regenerator with crystal-controlled phase-locked loop VCO (NE564)

AN182

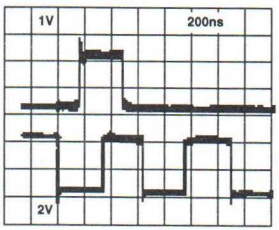


Figure 21. Regenerated Clock Signals

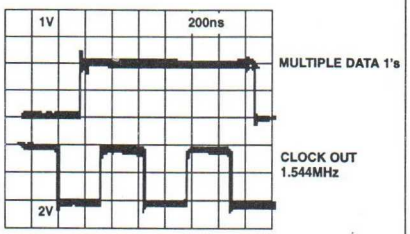


Figure 22. Regenerated Clock Signals

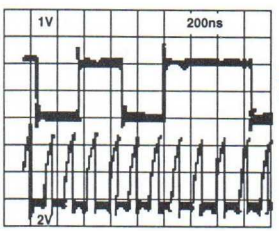


Figure 23. Regenerated Clock Signals Relative to NE564 VCO Signal

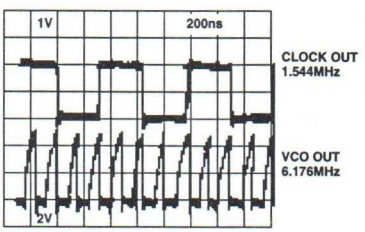


Figure 24. Regenerated Clock Signal Relative to NE564 VCO Signal

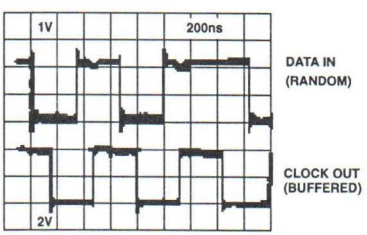


Figure 25. Regenerated Clock Signal Relative to Random NRZ Data Signal

NOTES:

1. Recent versions of this circuit no longer require series capacitors C_C and C_T. See Figure 12.
2. Input levels to the NE564 have been reduced for this application to $\equiv 800mV_{P-P}$. See Figure 12.
3. Improved operation regarding clock jitter is obtained by carefully decoupling the divider counter ICs and the PLLs V_{CC} line. This is accomplished by adding a small series "R" into the V_{CC} line with the bypass capacitor to ground.

References

3. "Fourier Analysis" by Hwei P. Hsu. Simon & Shuster Tech Outlines
4. "Pulse and Digital Circuits" by Millman and Taub. McGraw Hill
5. "Phaselock Techniques" by Floyd M. Gardner. Wiley, 1966

Section 7
Line Drivers/Receivers, Modems

INDEX

MC145406	EIA-232-D/V.28 driver/receiver	467
NE5170	Octal line driver	472
NE5180/NE5181	Octal differential line receiver	478
AM26LS31	Quad high-speed differential line driver	483
AM26LS32/AM26LS33	Quad high-speed differential line receivers	488
NE5080	High-speed FSK modem transmitter	491
NE5081	High-speed FSK modem receiver	496
AN195	Applications using the NE5080, NE5081	499
AN1950	Application of NE5080 and NE5081 with frequency deviation reduction	506

EIA-232-D/V.28 driver/receiver | MC145406

DESCRIPTION

The MC145406 is a silicon-gate CMOS IC that combines 3 drivers and 3 receivers to fulfill the electrical specifications of standards EIA-232-D and CCITT V.28. The drivers feature true TTL input compatibility, slew-rate limited output, 300Ω power-off source impedance, and output typically switching to within 25% of the supply rails. The receivers can handle up to ±25V while presenting 3 to 7kΩ impedance. Hysteresis in the receiver aids reception of noisy signals. By combining both drivers and receivers in a single CMOS chip, the MC145406 provides efficient, low-power solutions for EIA-232-D and V.28 applications.

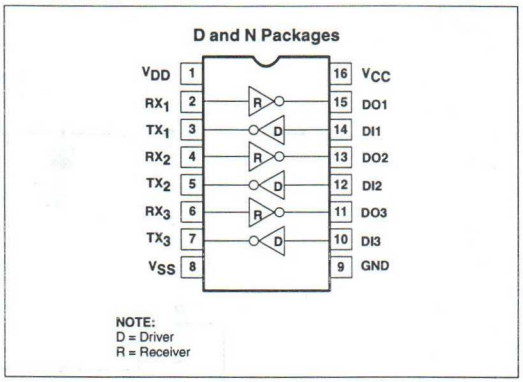
APPLICATIONS

- Modem interface
- Voice/data telephone interface
- Lap-top computers
- UART interface

FEATURES

- **Drivers**
- ±5 to ±12V supply range
- 300Ω power-off source impedance
- Output current limiting
- TTL compatible
- Maximum slew rate = 30V/µs
- **Receivers**
- ±25V input voltage range over the full supply range
- 3 to 7kΩ input impedance
- Hysteresis on input switchpoint
- **General**
- Very low supply currents for long battery life
- Operation is independent of power supply sequencing

PIN CONFIGURATION



ORDERING INFORMATION

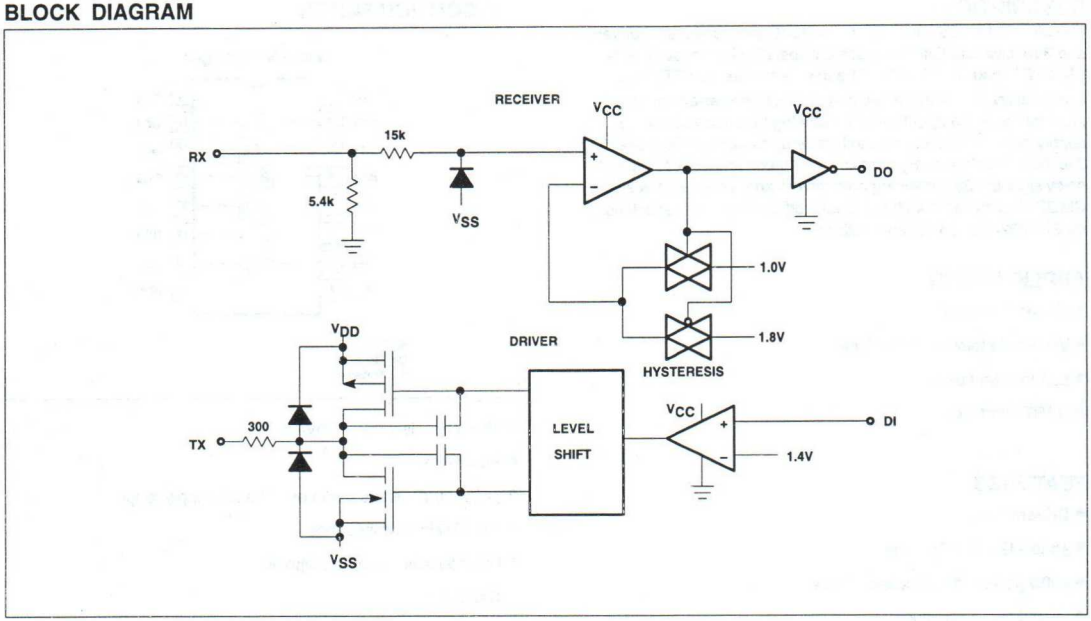
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line (DIP) Package	0 to +70°C	MC145406N	0406C
16-Pin Small Outline Large (SOL) Package	0 to +70°C	MC145406D	0171B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +6.0	V
V_{DD}	Supply voltage	-0.5 to +13.5	V
V_{SS}	Supply voltage	+0.5 to -13.5	V
V_{IR}	Input voltage range RX_{1-3} inputs DI_{1-3} inputs	 $(V_{SS} - 15)$ to $(V_{DD} + 15)$ -0.5 to $(V_{CC} + 0.5)$	V
	DC current per pin	±100	mA
P_D	Power dissipation (package)	1.0	W
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
θ_{JA}	Thermal impedance N package D package	80 105	°C/W

NOTE: This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range GND ≤ V_{DI} ≤ V_{DD} and GND ≤ V_{DO} ≤ V_{CC}. Also, the voltage at the RX pin should be constrained to ±25V, and TX should be constrained to V_{SS} ≤ V_{TX1-3} ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and V_{SS} or V_{DD} for RX).

BLOCK DIAGRAM



PIN #	SYMBOL	PIN DESCRIPTION
1	V_{DD}	**Positive power supply.** The most positive power supply pin, which is typically 5 to 12 volts.
8	V_{SS}	**Negative power supply.** The most negative power supply pin, which is typically -5 to -12 volts.
16	V_{CC}	**Digital power supply.** The digital supply pin, which is connected to the logic power supply (maximum +5.5V).
9	GND	**Ground.** Ground return pin is typically connected to the signal ground pin of the EIA-232-D connector (Pin 7) as well as to the logic power supply ground.
2, 4, 6	RX_1, RX_2, RX_3	**Receive Data Input.** These are the EIA-232-D receive signal inputs whose voltages can range from +25 to -25V. A voltage between +3 and +25 is decoded as a space and causes the corresponding DO pin to swing to ground (0V); a voltage between -3 and -25V is decoded as a mark and causes the DO pin to swing up to V_{CC}. The actual turn-on input switchpoint is typically biased at 1.8V above ground, and includes 800mV of hysteresis for noise rejection. The nominal input impedance is 5kΩ. An open or grounded input pin is interpreted as a mark, forcing the DO pin to V_{CC}.
11, 13, 15	DO1, DO2, DO3	**Data Output.** These are the receiver digital output pins, which swing from V_{CC} to GND. A space on the RX pin causes DO to produce a logic zero; a mark produces a logic one. Each output pin is capable of driving one LSTTL input load.
10, 12, 14	DI1, DI2, DI3	**Data Input.** These are the high-impedance digital input pins to the drivers. TTL compatibility is accomplished by biasing the input switchpoint at 1.4V above ground. However, 5V CMOS compatibility is maintained as well. Input voltage levels on these pins must be between V_{CC} and GND.
3, 5, 7	TX1, TX2, TX3	**Transmit Data Output.** These are the EIA-232-D transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic one at a DI input causes the corresponding TX output to swing toward V_{SS}. A logic zero causes the output to swing toward V_{DD} (the output voltages will be slightly less than V_{DD} or V_{SS} depending upon the output load). Output slew rates are limited to a maximum of 30V/μs. When the MC145406 is off ($V_{DD} = V_{SS} = V_{CC}$ = GND), the minimum output impedance is 300Ω.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +6.0	V
V_{DD}	Supply voltage	-0.5 to +13.5	V
V_{SS}	Supply voltage	+0.5 to -13.5	V
V_{IR}	Input voltage range RX_{1-3} inputs DI_{1-3} inputs	 $(V_{SS} - 15)$ to $(V_{DD} + 15)$ -0.5 to $(V_{CC} + 0.5)$	V
	DC current per pin	±100	mA
P_D	Power dissipation (package)	1.0	W
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
θ_{JA}	Thermal impedance N package D package	80 105	°C/W

NOTE: This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range GND ≤ V_{DI} ≤ V_{DD} and GND ≤ V_{DO} ≤ V_{CC}. Also, the voltage at the RX pin should be constrained to ±25V, and TX should be constrained to $V_{SS} \le V_{TX1-3} \le V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and V_{SS} or V_{DD} for RX).

DC ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; GND = 0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
DC supply voltage						
V_{DD}			4.5	5 to 12	13.2	V
V_{SS}			-4.5	-5 to -12	-13.2	V
V_{CC}			4.5	5.0	5.5	V
Quiescent supply current (outputs unloaded, inputs low)						
I_{DD}		V_{DD} = +12V		20	400	µA
I_{SS}		V_{SS} = -12V		280	600	µA
I_{CC}		V_{CC} = +5V		260	450	µA

RECEIVER ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; GND = 0V; V_{DD} = +5 to +12V; V_{SS} = -5 to -12V; V_{CC} = +5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNITS
				MIN	TYP	MAX	
V_{ON}	Input turn-on threshold	RX_{1-3}	$V_{DO1-3} = V_{OL}$, V_{CC} = 5.0V ±5%	1.35	1.80	2.35	V
V_{OFF}	Input turn-off threshold	RX_{1-3}	$V_{DO1-3} = V_{OH}$, V_{CC} = 5.0V ±5%	0.75	1.00	1.25	V
V_{ON}-V_{OFF}	Input threshold hysteresis	RX_{1-3}	V_{CC} = 5.0V ±5%	0.6	0.8		V
R_{IN}	Input resistance	RX_{1-3}	$(V_{SS}$-15V) ≤ V_{RX1-3} ≤ $(V_{DD}$+15V)	3.0	5.0	7.0	kΩ
V_{OH}	High level output voltage V_{RX1-3} = -3V to $(V_{SS}$-15V)[1]	DO_{1-3}	I_{OH} = -20µA, V_{CC} = +5.0V	4.9	5.0		V
			I_{OH} = -1mA, V_{CC} = +5.0V	3.8	4.4		
V_{OL}	Low level output voltage V_{RX1-3} = +3V to $(V_{DD}$+15V)[1]	DO_{1-3}	I_{OL} = ÷20µA, V_{CC} = +5.0V		0.005	0.1	V
			I_{OL} = +2mA, V_{CC} = +5.0V		0.15	0.5	
			I_{OL} = +4mA, V_{CC} = +5.0V		0.3	0.7	

NOTE:
1. This is the range of input voltages as specified by EIA-232-D to cause a receiver to be in the high or low logic state.

DRIVER ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; GND = 0V; V_{CC} = +5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNITS
				MIN	TYP	MAX	
V_{IL}	Digital input voltage	DI_{1-3}	Logic 0			0.8	V
V_{IH}	Digital input voltage	DI_{1-3}	Logic 1	2.0			V
I_{IN}	Input current	DI_{1-3}	$V_{DI1-3} = V_{CC}$			±1.0	µA
V_{OH}	Output high voltage V_{DI1-3} = Logic 0, R_L = 3.0kΩ	TX_{1-3}	V_{DD} = +5.0V, V_{SS} = -5.0V	3.5	4.1		V
			V_{DD} = +6.0V, V_{SS} = -6.0V	4.3	5.0		
			V_{DD} = +12.0V, V_{SS} = -12.0V	9.2	10.4		
V_{OL}	Output low voltage[1] V_{DI1-3} = Logic 0, R_L = 3.0kΩ	TX_{1-3}	V_{DD} = +5.0V, V_{SS} = -5.0V	-4.0	-4.3		V
			V_{DD} = +6.0V, V_{SS} = -6.0V	-4.5	-5.2		
			V_{DD} = +12.0V, V_{SS} = -12.0V	-10.0	-10.3		
	Off source resistance Figure 1	TX_{1-3}	V_{DD}=V_{SS}=GND=0V, V_{TX1-3} = ±2.0V	300			Ω
I_{SC}	Output short-circuit current	TX_{1-3}	TX_{1-3} shorted to GND[2]		±22	+60	mA
	V_{DD} = +12.0V, V_{SS} = -12.0V		TX_{1-3} shorted to ±15.0V[3]		±60	±100	mA

NOTE:
1. The voltage specifications are in terms of absolute values.
2. Specification is for one TX output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits will be exceeded.
3. This condition could exceed package limitations.

SWITCHING CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; V_{CC} = +5V ±5%, unless otherwise specified. (See Figures 2 and 3)

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNITS
				MIN	TYP	MAX	
Drivers							
t_{PLH}	Propagation delay time	TX_{1-3}	Low-to-High R_L = 3kΩ, C_L = 50pF		300	500	ns
t_{PHL}	Propagation delay time	TX_{1-3}	High-to-Low R_L = 3kΩ, C_L = 50pF		300	500	ns
SR	Output slew rate (minimum load)	TX_{1-3}	R_L = 7kΩ, C_L = 0pF, V_{DD} = 6 to 12.0V, V_{SS} = -6 to -12V		±6	±30	V/µs
	Output slew rate (maximum load)	TX_{1-3}	R_L = 3kΩ, C_L = 2500pF, V_{DD} = 12V, V_{SS} = -12V		±3.0		
Receivers (C_L = 50pF)							
t_{PLH}	Propagation delay time	DO_{1-3}	Low-to-High		150	425	ns
t_{PHL}	Propagation delay time	DO_{1-3}	High-to-Low		150	425	ns
t_R	Output rise time	DO_{1-3}			120	400	ns
t_F	Output fall time	DO_{1-3}			40	100	ns

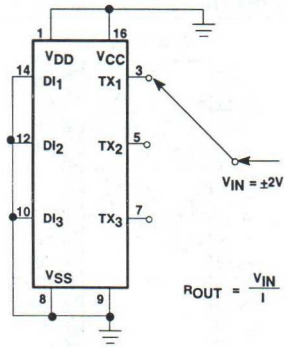


Figure 1. Power-Off Source Resistance (Drivers)

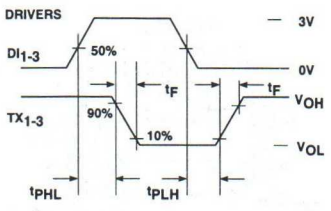


Figure 2. Switching Characteristics

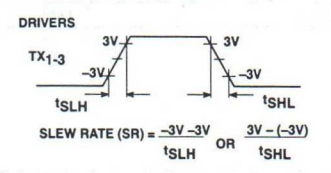


Figure 3. Slew Rate Characteristics

APPLICATIONS INFORMATION

The MC145406 has been designed to meet the electrical specifications of standards EIA-232-D/CCITT V.28 and as such, defines the electrical and physical interface between Data Communication Equipment (DCE) and Data Terminal Equipment (DTE). A DCE is connected to a DTE using a cable that typically carries up to 25 leads, which allow the transfer of timing, data, control, and test signals. The MC145406 provides the necessary level shifting between the TTL/CMOS logic levels and the high voltage levels of EIA-232-D (ranging from ±3 to ±25V).

DRIVERS

As defined by the specification, an EIA-232-D driver presents a voltage of between ±5 to ±15V into a load of between 3 to 7kΩ. A logic one at the driver input results in a voltage of between -5 to -15V. A logic zero results in a voltage between ±5 to ±15V. When operating at ±7 to ±12V, the MC145406 meets this requirement. When operating at ±5V, the MC145406 drivers produce less than ±5V at the output (when terminated), which does not meet the EIA-232-D specification. However, the output voltages when using a ±5V power supply are high enough (around ±4V) to permit proper reception by an EIA-232-D receiver, and can be used in applications where strict compliance to EIA-232-D is not required.

Another requirement of the MC145406 drivers is that they withstand a short to another driver in the EIA-232-D cable. The worst-case condition that is permitted by EIA-232-D is a ±15V source that is current limited to 500mA. The MC145406 drivers can withstand this condition momentarily. In most short circuit conditions the source driver will have a series 300Ω output impedance needed to satisfy the EIA-232-D driver requirements. This will reduce the short circuit current to under 40mA which is an acceptable level for the MC145406 to withstand.

Unlike some other drivers, the MC145406 drivers feature an internally-limited output slew rate that does not exceed 30V/µs.

RECEIVERS

The job of an EIA-232-D receiver is to level-shift voltages in the range of -25 to +25V down to TTL/CMOS logic levels (0 to +5V). A voltage of between -3 and -25V on RX_1 is defined as a mark and produces a logic one at DO_1. A voltage between +3 and +25V is a space and produces a logic zero. While receiving these signals, the RX inputs must present a resistance between 3 and 7kΩ. Nominally, the input resistance of the RX_{1-3} inputs is 5.0kΩ.

The input threshold of the RX_{1-3} inputs is typically biased at 1.8V above ground (GND) with typically 800mV of hysteresis included to improve noise immunity. The 1.8V bias forces the appropriate DO pin to a logic one when its RX input is open or grounded as called for in EIA-232-D specification. Notice that TTL logic levels can be applied to the RX inputs in lieu of normal EIA-232-D signal levels. This might be helpful in situations where access to the modem or computer through the EIA-232-D connector is necessary with TTL devices. However, it is important not to connect the EIA-232-D outputs (TX_1) to TTL inputs since TTL operates off +5V only, and may be damaged by the high output voltage of the MC145406.

The DO outputs are to be connected to a TTL or CMOS input (such as an input to a modem chip). These outputs will swing from V_{CC} to ground, allowing the designer to operate the DO and DI pins from the digital power supply. The TX and RX sections are independently powered by V_{DD} and V_{SS} so that one may run logic at +5V and the EIA-232-D signals at ±12V.

Octal line driver

NE5170

DESCRIPTION

The NE5170 is an octal line driver which is designed for digital communications with data rates up to 100kb/s. This device meets all the requirements of EIA standards RS-232C/RS-423A and CCITT recommendations V.10/X.26. Three programmable features:

(1) output slew rate, (2) output voltage level, and (3) three-state control (high-impedance) are provided so that output characteristics may be modified to meet the requirements of specific applications.

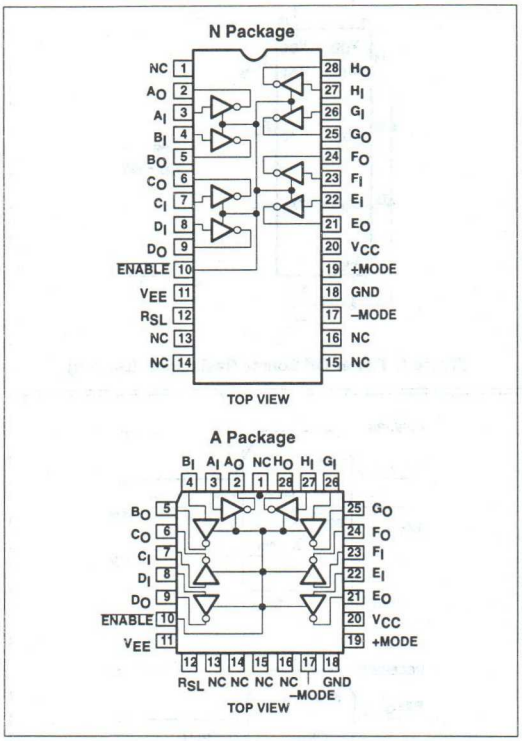
FEATURES

- Meets EIA RS-232C/423A and CCITT V.10/X.26
- Simple slew rate programming with a single external resistor
- 0.1 to 10V/µs slew rate range
- High/low programmable voltage output modes
- TTL compatible inputs

APPLICATIONS

- High-speed modems
- High-speed parallel communications
- Computer I/O ports
- Logic level translation

PIN CONFIGURATION



FUNCTION TABLE

ENABLE	Logic Input	OUTPUT VOLTAGE (V)		
		RS-423A[1]	RS-232C	
			Low Output Mode[1]	High Output Mode[2]
L	L	5 to 6V	5 to 6V	≥ 9V
L	H	–5 to 6V	–5 to 6V	≤ –9V
H	X	High-Z	High-Z	High-Z

NOTES:
1. V_{CC} = +10V and V_{EE} = –10V; R_L = 3kΩ
2. V_{CC} = +12V and V_{EE} = –12V; R_L = 3kΩ

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
28-Pin Plastic Dual In-Line (DIP) Package	0 to +70°C	NE5170N	0408B
28-Pin Plastic Lead Chip Carrier (PLCC) Package	0 to +70°C	NE5170A	0401F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage and + MODE	15	V
V_{EE}	Supply voltage and – MODE	–15	V
I_{OUT}	Output current[1]	±150	mA
V_{IN}	Input voltage ($\overline{\text{Enable}}$, Data)	–1.5 to +7	V
V_{OUT}	Output voltage[2]	±15	V
	Minimum slew resistor[3]	1	kΩ
P_D	Power dissipation	1200	mW

NOTES:
1. Maximum current per driver. Do not exceed maximum power dissipation if more than one output is on.
2. High impedance mode.
3. Minimum value of the resistor used to set the slew rate.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ±10%; V_{EE} = –10V ±10%; ±MODES = 0V; R_{SL} = 2kΩ, 0°C ≤ T_A ≤ 70°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
V_{OH}	Output high voltage	V_{IN} = 0.8V, R_L = 3kΩ[2]	5	6	V
		R_L = 450Ω[2]	4.5	6	
		R_L = 3kΩ[3], C_L = 2500pF	V_{CC}–3		
V_{OL}	Output low voltage	V_{IN} = 2.0V, R_L = 3kΩ[2]	–6	–5	V
		R_L = 450Ω[2]	–6	–4.5	
		R_L = 3kΩ[3], C_L = 2500pF		V_{EE}+3	
V_{OU}	Output unbalance voltage	V_{CC} = |V_{EE}|, R_L = 450Ω[2]		0.4	V
I_{CEX}	Output leakage current	|V_O| = 6V, ENABLE = 2V or V_{CC} = V_{EE} = 0V	–100	100	µA
V_{IH}	Input high voltage		2.0		V
V_{IL}	Input low voltage			0.8	V
I_{IL}	Logic "0" input current	V_{IN} = 0.4V	–400	0	µA
I_{IH}	Logic "1" input current	V_{IN} = 2.4V	0	40	µA
I_{OS}	Output short circuit current[1]	V_O = 0V	–150	150	mA
V_{CL}	Input clamp voltage	I_{IN} = –15mA	–1.5		V
I_{CC}	Supply current	NO LOAD		35	mA
I_{EE}		NO LOAD	–45		mA

NOTES:
1. Maximum current per driver. Do not exceed maximum power dissipation if more than one output is on.
2. V_{OH}, V_{OL} at R_L = 450Ω will be ≥ 90% of V_{OH}, V_{OL} at R_L = ∞.
3. High Output Mode; +MODE pin = V_{CC}; –MODE pin = V_{EE}; 9V ≤ V_{CC} ≤ 13V; –9V ≥ V_{EE} ≥ –13V.

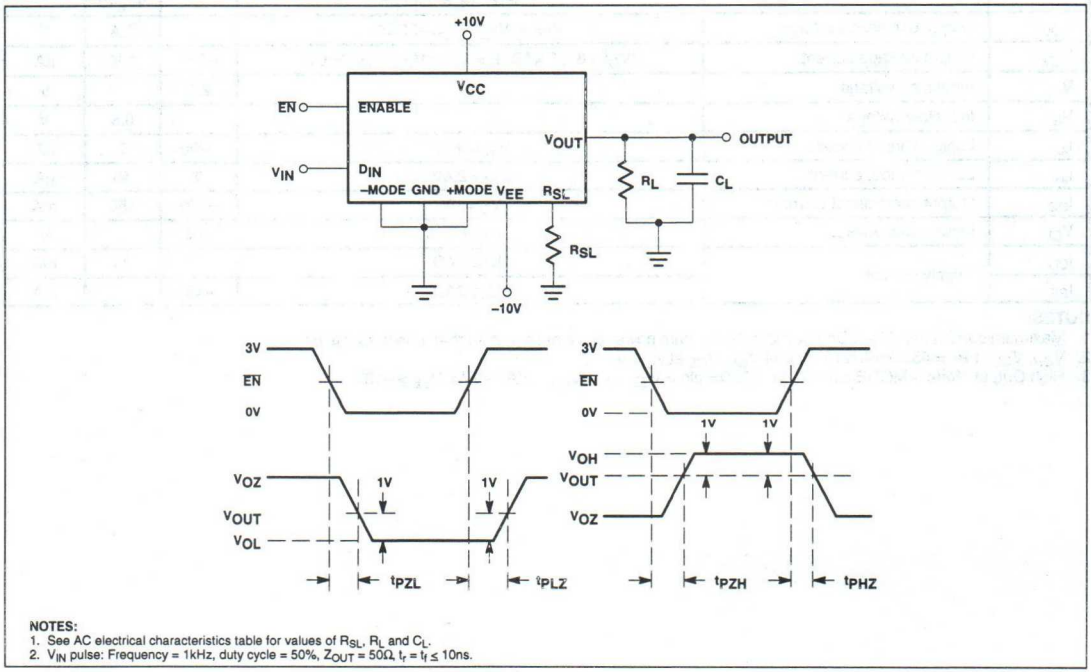
AC ELECTRICAL CHARACTERISTICS

V_{CC} = +10V; V_{EE} = −10V; Mode = GND, 0°C ≤ T_A ≤ 70°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_{PLZ}	Propagation delay output high to high impedance	R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		5	µs
t_{PLZ}	Propagation delay output low to high impedance	R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		5	µs
t_{PZH}	Propagation delay high impedance to high output	R_{SL} = 200k R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		150	µs
t_{PZL}	Propagation delay high impedance to low output	R_{SL} = 200k R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		150	µs
SR	Output slew rate	R_{SL} = 2k	8	12	V/µs
		R_{SL} = 20k	0.8	1.2	
		R_{SL} = 200k	0.06	0.14	

NOTE:
SR: Load condition. (A) For R_{SL} < 4kΩ use R_L = 450Ω; C_L = 50pF; (B) for R_{SL} > 4kΩ use either R_L = 450Ω, C_L = 50pF or R_L = 3kΩ, C_L = 2500pF.

AC PARAMETER TEST CIRCUIT AND WAVEFORMS



NOTES:
1. See AC electrical characteristics table for values of R_{SL}, R_L and C_L.
2. V_{IN} pulse: Frequency = 1kHz, duty cycle = 50%, Z_{OUT} = 50Ω, $t_r = t_f \leq 10$ns.

SLEW RATE PROGRAMMING

Slew rate for the NE5170 is set using a single external resistor connected between the R_{SL} pin and ground. Adjustment is made according to the formula:

$$R_{SL}\ (\text{in k}\Omega) = \frac{20}{\text{Slew Rate}}$$

where the slew rate is in V/µs. The slew resistor can vary between 2 and 200kΩ which gives a slew rate range of 10 to 0.1V/µs. This adjustment of the slew rate allows tailoring output characteristics to recommendations for cable length and data rate found in EIA standard RS–423A. Approximations for cable length and data rate are given by:

Max. data rate (in kb/s) = 300/t

Cable length (in feet) = 100×t

where t is the rise time in microseconds. The absolute maximum data rate is 100kb/s and the absolute maximum cable length is 4000 feet.

OUTPUT MODE PROGRAMMING

The NE5170 has two programmable output modes which provide different output voltage levels. The low output mode meets the specifications of EIA standards RS–423A and RS–232C. The high output mode meets the specifications of RS–232C only, since higher output voltages result from programming this mode. The high output mode provides the greater output voltages where higher attenuation levels must be tolerated. Programming the high output mode is accomplished by connecting the +MODE pin to V_{CC} and the –MODE pin to V_{EE}. The low output mode results when both of these pins are connected to ground.

APPLICATION

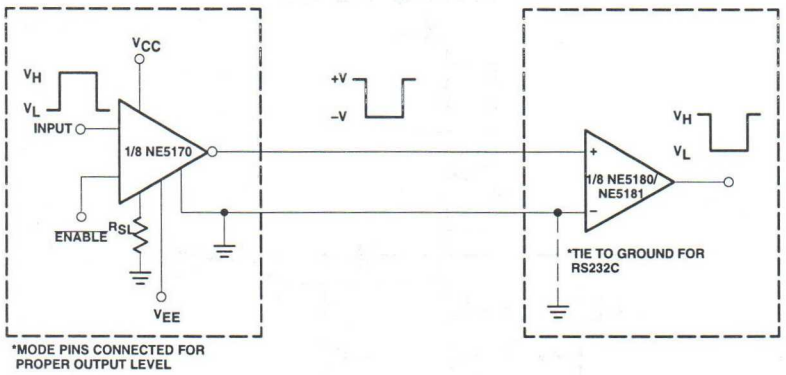


Figure 1. RS-232C/RS-423A Data Transmission

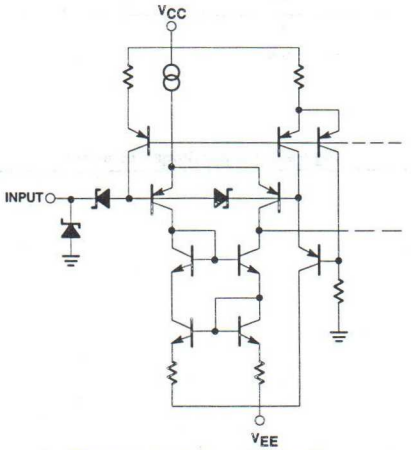


Figure 2. Input Stage Schematic

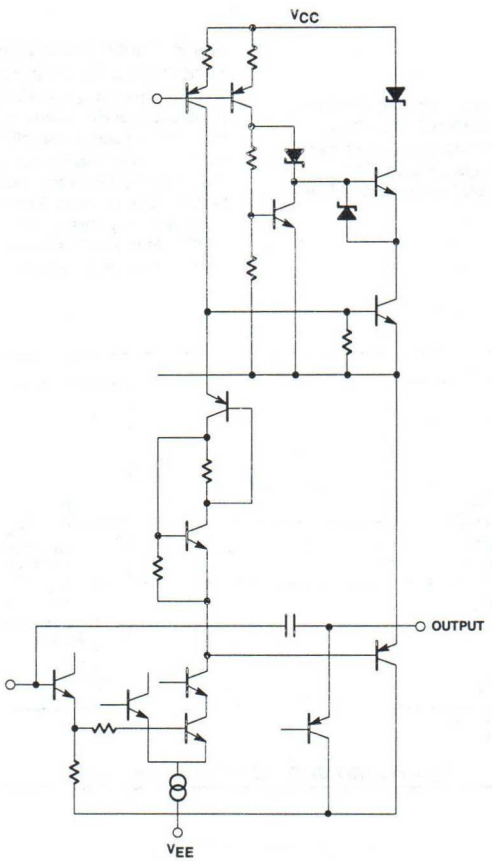


Figure 3. Output Stage Schematic

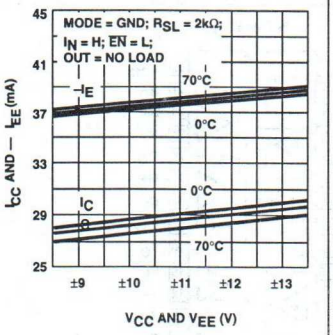


Figure 4. Typical I_{CC} and I_{EE} vs Supply Voltages

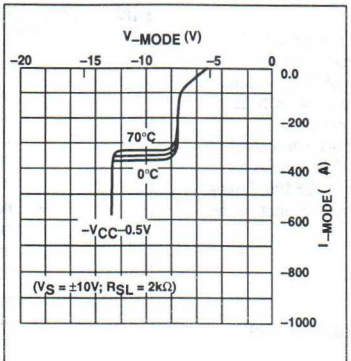


Figure 7. Typical –MODE Current vs –MODE Voltage

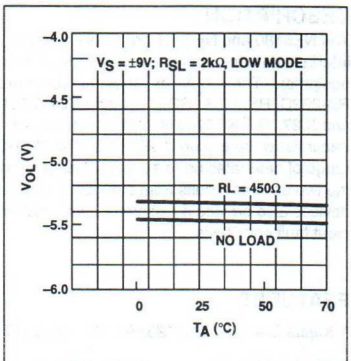


Figure 10. Typical Output Low Voltage vs Temperature

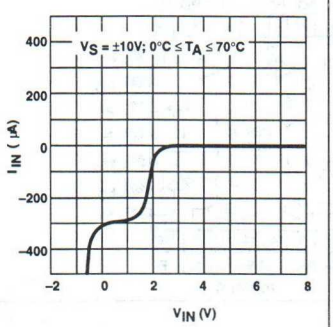


Figure 5. Typical Input Current vs Input Voltage

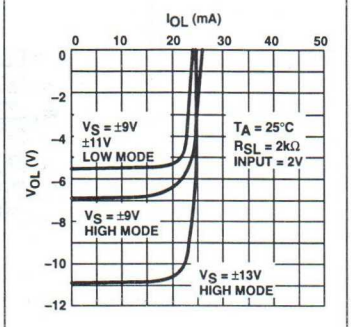


Figure 8. Typical Output Low Voltage vs Load Current

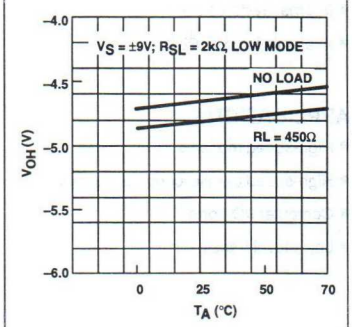


Figure 11. Typical Output High Voltage vs Temperature

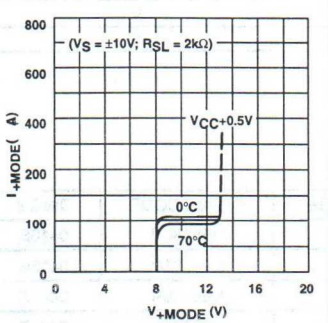


Figure 6. Typical +MODE Current vs +MODE Voltage

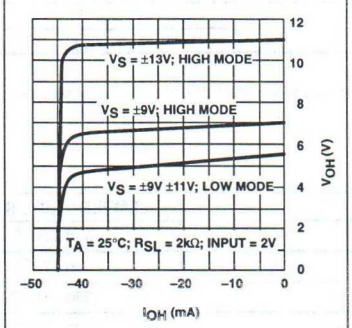


Figure 9. Typical Output High Voltage vs Load Current

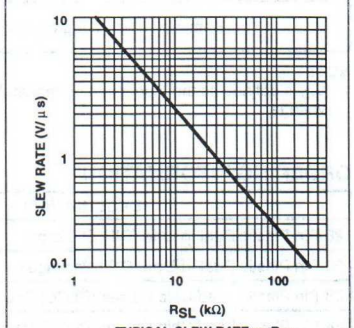


Figure 12. Typical Slew Rate vs R_{SL}

Octal differential line receiver

NE5180/NE5181

DESCRIPTION

The NE5180 and NE5181 are octal line receivers designed to interface data terminal equipment with data communications equipment. These devices meet the requirements of EIA standards RS-232C, RS-423A, RS-422A, and CCITT V.10, V.11, V.28, X.26 and X.27. The NE5180 is intended for use where the data transmission rate is up to 200 kb/s. The NE5181 covers the entire range of data rates up to 10 Mb/s. The difference in data rates for the two devices results from the input filtering of the NE5180. These devices also provide a failsafe feature which protects against certain input fault conditions.

FEATURES

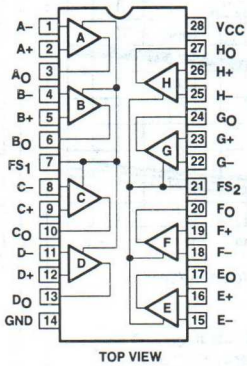
- Meets EIA RS-232C/423A/422A and CCITT V.10, V.11, V.28
- Single +5V supply—TTL compatible outputs
- Differential inputs withstand ±25V
- Failsafe feature
- Input noise filter (NE5180 only)
- Internal hysteresis
- Available in SMD PLCC

APPLICATIONS

- High-speed modems
- High-speed parallel communications
- Computer I/O ports
- Logic level translation

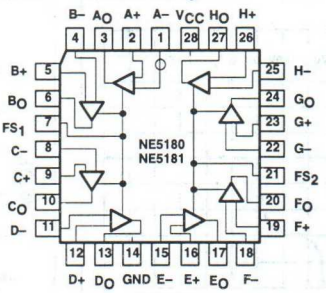
PIN CONFIGURATION

N Package



TOP VIEW

A Package



TOP VIEW

FUNCTION TABLE

INPUT	FAILSAFE INPUT	LOGIC OUTPUT
V_{ID} > 200mV[1]	X	H
V_{ID} < –200mV[1]	X	L
Both inputs open or grounded	0V	L
	V_{CC}	H

NOTE:

1. V_{ID} is defined as the non-inverting terminal input voltage minus the inverting terminal input voltage.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
28-Pin Plastic Dual In-Line (DIP) Package	0 to +70°C	NE5180N	0413B
28-Pin Plastic Dual In-Line (DIP) Package	0 to +70°C	NE5181N	0413B
28-Pin Plastic Lead Chip Carrier (PLCC) Package	0 to +70°C	NE5180A	0401F
28-Pin Plastic Lead Chip Carrier (PLCC) Package	0 to +70°C	NE5181A	0401F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
P_D	Power dissipation	800	mW
V_{CC}	Supply voltage	7	V
V_{CM}	Common mode range	±15	V
V_{ID}	Differential input voltage	±25	V
I_{SINK}	Outputsink current	50	mV
V_{FS}	Failsafe voltage	−0.3 to V_{CC}	V
J_{OS}	Output short-circuit time	1	sec

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V ±5%, 0°C ≤ T_A ≤ +70°C, input common-mode range ±7V

SYMBOL	PARAMETER	TEST CONDITIONS		NE5180		NE5181		UNIT
				Min	Max	Min	Max	
R_{IN}	DC input resistance	3V ≤ |V_{IN}| ≤ 25V		3	7	3	7	kΩ
V_{OFS}	Failsafe output voltage	Inputs open or shorted to GND	0 ≤ I_{OUT} ≤ 8mA, $V_{failsafe}$ = 0V		0.45		0.45	V
			0 ≥ I_{OUT} ≥ −400µA, $V_{failsafe}$ = V_{CC}	2.7		2.7		
V_{th}	Differential input high[4] threshold	V_{OUT} ≥ 2.7V, I_{OUT} = −440µA	R_S = 0[1]		0.2		0.2	V
			R_S = 500[1]		0.4		0.4	
V_{tl}	Differential input low[4] threshold	V_{OUT} ≤ 0.45V, I_{OUT} = 8mA	R_S = 0[1]	−0.2		−0.2		V
			R_S = 500[1]	−0.4		−0.4		
V_H	Hysteresis[4]	FS = 0V or V_{CC} (See Figure 1)		50	140	50	140	mV
V_{IOC}	Open-circuit input voltage				2		2	V
C_I	Input capacitance				30		30	pF
V_{OH}	High level output voltage	V_{ID} = 1V, I_{OUT} = −440µA		2.7		2.7		V
V_{OL}	Low level output voltage	V_{ID} = −1V	I_{OUT} = 4mA[2]		0.4		0.4	V
			I_{OUT} = 8mA[2]		0.45		0.45	
I_{OS}	Short-circuit output current	V_{ID} = 1V [3]		20	100	20	100	mA
I_{CC}	Supply current	4.75V ≤ V_{CC} ≤ 5.25V, V_{ID} = −1V; FS = 0V			100		100	mA
I_{IN}	Input current	Other inputs grounded	V_{IN} = +10V		3.25		3.25	mA
			V_{IN} = −10V	−3.25		−3.25		

NOTES:
1. R_S is a resistor in series with each input.
2. Measured after 100ms warm-up (at 0°C).
3. Only 1 output may be shorted at a time and then only for a maximum of 1 second.
4. See Figure 1 for threshold and hysteresis definitions.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V ±5%, 0°C ≤ T_A ≤ +70°C

SYMBOL	PARAMETER	TEST CONDITIONS	NE5180		NE5181		UNIT
			Min	Max	Min	Max	
t_{PLH}	Propagation delay—low to high	C_L = 50pF, V_{ID} = ±1V		500		100	ns
t_{PHL}	Propagation delay—high to low	C_L = 50pF, V_{ID} = ±1V		500		100	ns
f_a	Acceptable input frequency	Unused input grounded, V_{ID} = ±200mV[1]		0.1		5.0	MHz
f_r	Rejectable input frequency	Unused input grounded, V_{ID} = ±500mV	5.5		NA		MHz

NOTE:
1. V_{ID} = ±1V for NE5181.

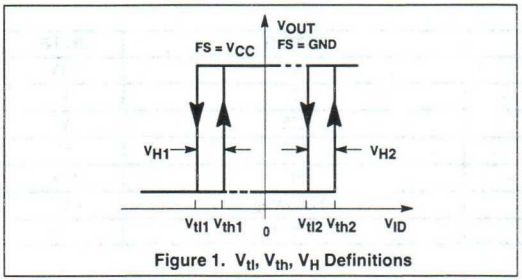
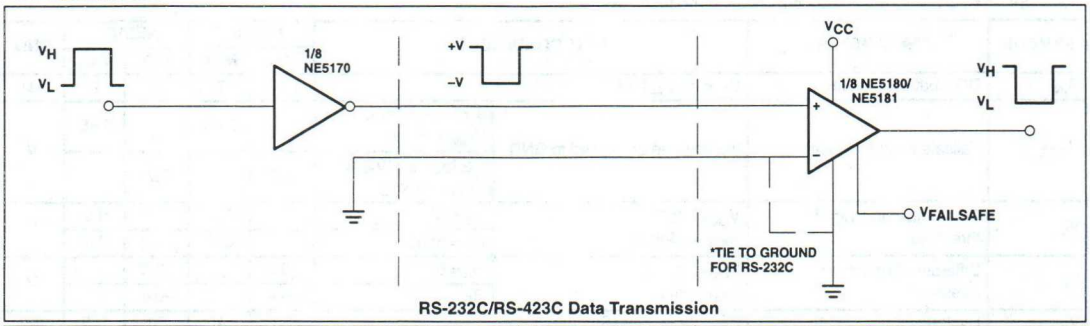


Figure 1. V_{tl}, V_{th}, V_H Definitions

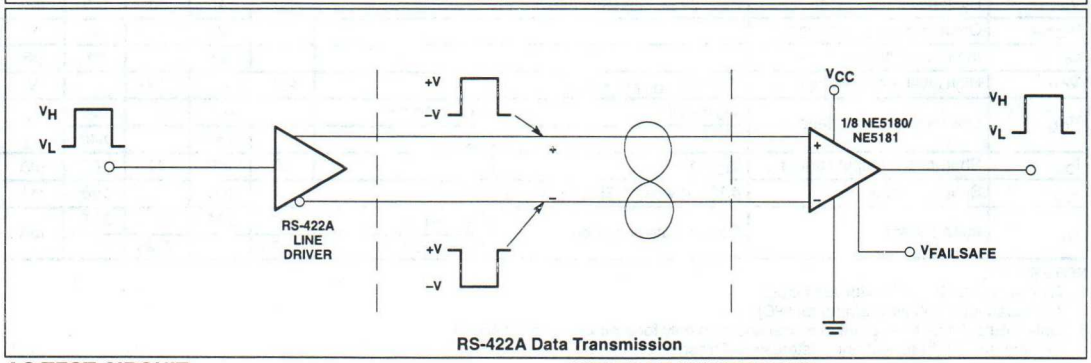
FAILSAFE OPERATION

These devices provide a failsafe operating mode to guard against input fault conditions as defined in RS-422A and RS-423A standards. These fault conditions are (1) driver in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to V_{CC} or ground. A connection to

APPLICATIONS

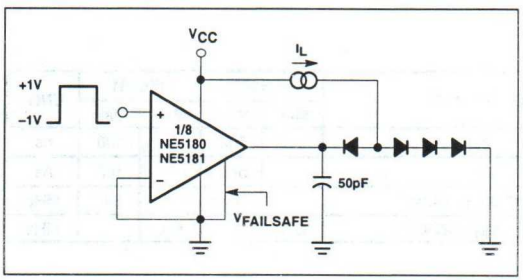


RS-232C/RS-423C Data Transmission

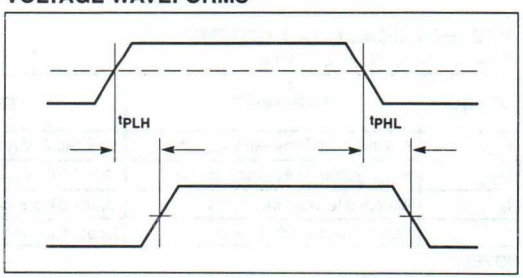


RS-422A Data Transmission

AC TEST CIRCUIT



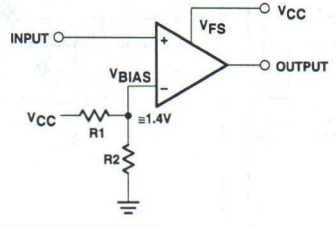
VOLTAGE WAVEFORMS



V_{CC} provides a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (F_{S1} and F_{S2}) on the NE5180 or NE5181 where each provides common failsafe control for four receivers.

RS-232 FAILSAFING

The internal failsafe circuitry works by providing a small input offset voltage which can be polarity-switched by using the failsafe control pins. This offset is kept small (approximately 80mV) to avoid degradation of the ±200mV input threshold for RS-423 or RS-422 operation. If the positive and negative inputs to any receiver are both shorted to ground or open circuited, the internal offset drives that output to the programmed failsafe state. If only one input open circuits (as may be the case for RS-232 operation), that input will rise to the "input open circuit voltage" (approximately 700mV). Since this is much greater than the 200mV threshold, the output will be driven to a state that is independent of the failsafe programming. Failsafe programming can be achieved for non-inverting single-ended applications by raising or lowering the unused input bias voltage as shown in Figure 2. For $V_{BIAS} \equiv 1.4$, an open (or grounded) INPUT line will be approximately 700mV (0V) and the output will failsafe low. If the resistor divider is not used and V_{BIAS} is connected to ground, the output will failsafe high due to the internal failsafe offset for the INPUT grounded and the 700mV "open circuit input voltage" for the INPUT open circuited. Similar operation holds for an inverting configuration, with V_{BIAS} applied to the positive input and V_{FS} = ground.



NOTE:
Two silicon diodes may be used in place of R2.

Figure 2. Single-Input Failsafe Programming

INPUT FILTERING (NE5180)

The NE5180 has input filtering for additional noise rejection. This filtering is a function of both signal level and frequency. For the specified input (5.5MHz at ±500mV) the input stage filter attenuates the signal such that the output stage threshold levels are not exceeded and no change of state occurs at the output. As the signal amplitude decreases (increases) the rejected frequency decreases (increases).

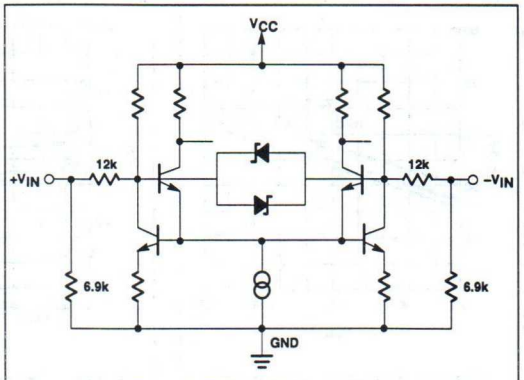


Figure 3. Differential Input Stage

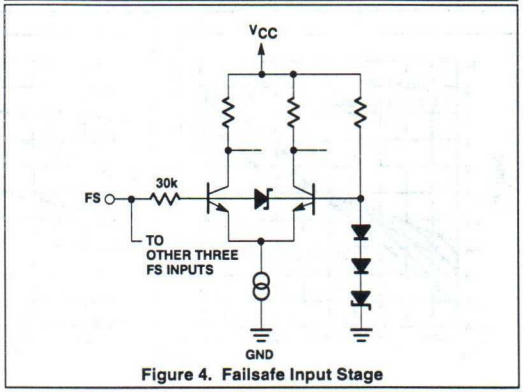


Figure 4. Failsafe Input Stage

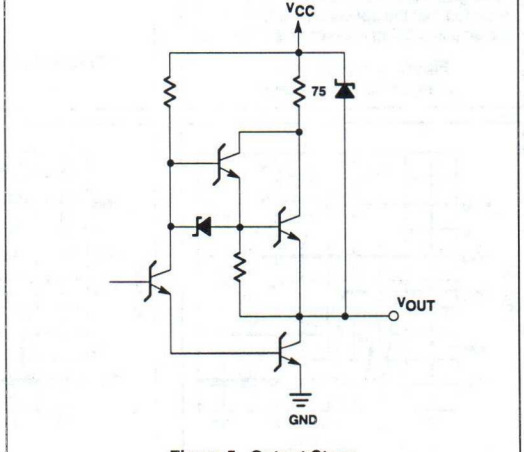


Figure 5. Output Stage

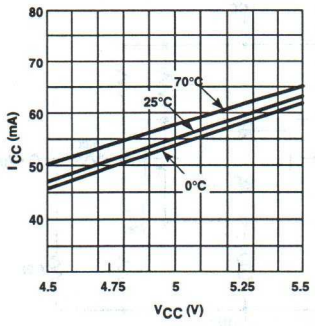


Figure 6. Typical Supply Current vs Supply Voltage

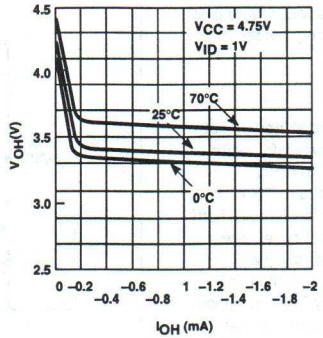


Figure 7. Typical High Level Output Voltage vs Output Current

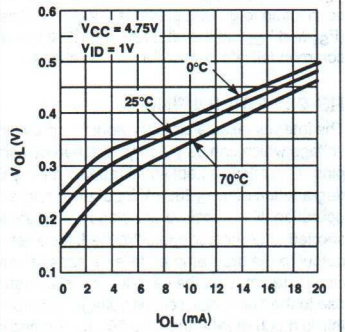
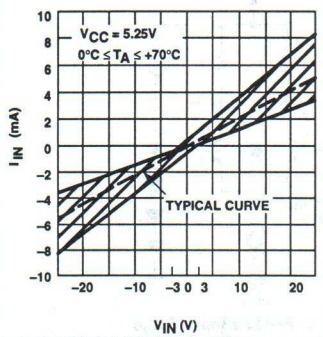


Figure 8. Typical Low Level Output Voltage vs Output Current



*This graph applies for all receiver inputs, provided that the opposite polarity input of the amplifier being measured is grounded.

Figure 9. Input Current vs Input Applied Voltage*

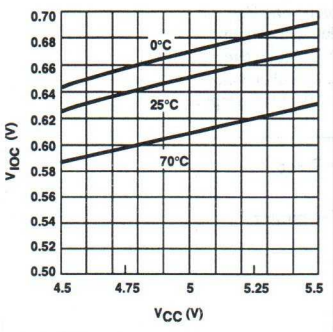


Figure 10. Typical V_{IOC} vs V_{CC}

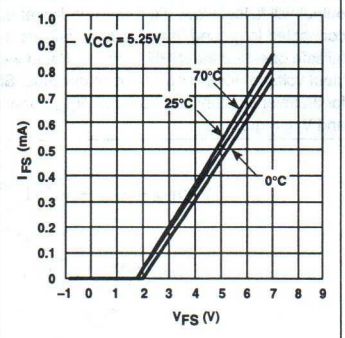


Figure 11. Typical FS Input Current vs FS Applied Voltage

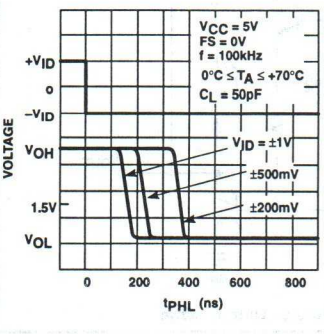


Figure 12. NE5180: Propagation Delay at Various Input Amplitudes

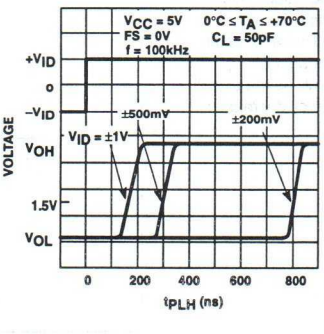


Figure 13. NE5180: Propagation Delay at Various Input Amplitude

Quad high-speed differential line driver — AM26LS31

DESCRIPTION

The AM26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The AM26LS31 meets all the requirements of EIA standard RS-422 and Federal standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines. The circuit provides an enable and disable function common to all four drivers. The AM26LS31 features 3-State outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

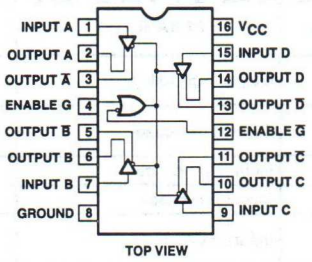
The AM26LS31 is constructed using advanced Low Power Schottky processing.

FEATURES

- Output skew of 2.0ns typical
- Input to output delay: 12ns
- Operation from single +5V
- 16-pin DIP and SO packages
- Four line drivers in one package
- Output short-circuit protection
- Complementary outputs
- Meets EIA standard RS-422
- High output drive capability for 100Ω terminated transmission lines
- Available in military and commercial temperature range
- Advanced low power Schottky processing
- Outputs won't load line when V_{CC} = 0V

PIN CONFIGURATION

D, and N Packages



TOP VIEW

APPLICATIONS

- Data communications equipment
- Computer peripherals
- Workstations
- Automatic test equipment

FUNCTION TABLE (Each Driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	A	$\overline{A}$
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

NOTES:
H = High level
L = Low level
X = Irrelevant
Z = High-impedance (OFF)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0°C to +70°C	AM26LS31CN	0406C
16-Pin Small Outline (SO) Package	0°C to +70°C	AM26LS31CD	0005D
16-Pin Plastic Dual In-Line Package (DIP)	–40°C to +85°C	AM26LS31IN	0406C
16-Pin Small Outline (SO) Package	–40°C to +85°C	AM26LS31ID	0005D
16-Pin Plastic Dual In-Line Package (DIP)	–55°C to +125°C	AM26LS31MN	0406C

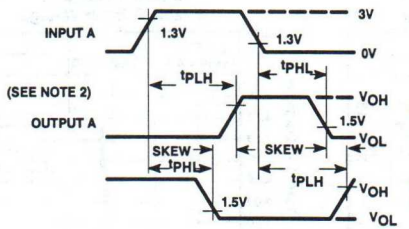
DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%, T_A = –55 to +125°C for AM26LS31MN; V_{CC} = 5V ±5%, T_A = –40 to +85°C for AM26LS31IN and AM26LS31ID; V_{CC} = 5V ±5%, T_A = 0 to +70°C for AM26LS31CN and AM26LS31CD, unless otherwise specified.

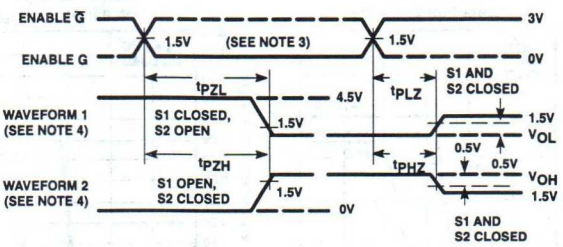
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
V_{OH}	Output High voltage	V_{CC} = Min., I_{OH} = –20mA	2.5	3.0		V
V_{OL}	Output Low voltage	V_{CC} = Min., I_{OL} = 20mA		0.3	0.5	V
V_{IH}	Input High voltage	V_{CC} = Min.	2.0			V
V_{IL}	Input Low voltage	V_{CC} = Max.			0.8	V
I_{IL}	Input Low current	V_{CC} = Max., V_{IN} = 0.4V		–0.26	–0.36	mA
I_{IH}	Input High current	V_{CC} = Max., V_{IN} = 2.7V		0.001	20	µA
I_I	Input reverse current	V_{CC} = Max., V_{IN} = 7.0V		0.001	0.1	mA
I_O	OFF-state (high-impedance) output current	V_{CC} = Max., V_O = 5.5V V_O = 0.5V		0.6 –0.050	20 –20	µA µA
V_I	Input clamp voltage	V_{CC} = Min., I_{IN} = –18mA		–0.8	–1.5	V
I_{SC}	Output short-circuit current	V_{CC} = Max.	–30		–150	mA
I_{CC}	Power supply current	V_{CC} = Max; all outputs disabled		40	80	mA
t_{PLH}	Input to output	T_A = 25°C, load[2]		9	20	ns
t_{PHL}	Input to output	T_A = 25°C, load[2]		9	20	ns
SKEW	Output to output	T_A = 25°C, load[2]		2	6	ns
t_{LZ}	Enable to output	T_A = 25°C, C_L = 10pF		17	35	ns
t_{HZ}	Enable to output	T_A = 25°C, C_L = 10pF		12	30	ns
t_{ZL}	Enable to output	T_A = 25°C, load[2]		14	45	ns
t_{ZH}	Enable to output	T_A = 25°C, load[2]		12	40	ns

NOTES:
1. All typical values are T_A = +25°C; V_{CC} = 5.0V.
2. C_L = 30pF; V_{IN} = 1.3V to V_{OUT} = 1.3V; V_{PULSE} = 0V to 3.0V.

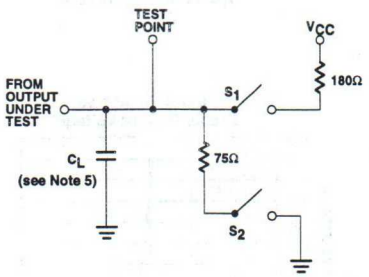
TIMING DIAGRAMS



Propagation Delay Times and Skew



Enable and Disable Times



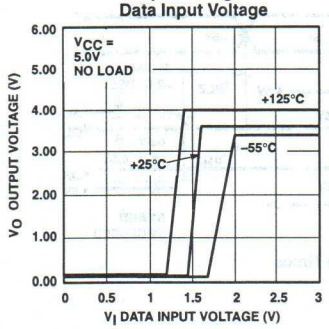
Test Circuit

NOTES:

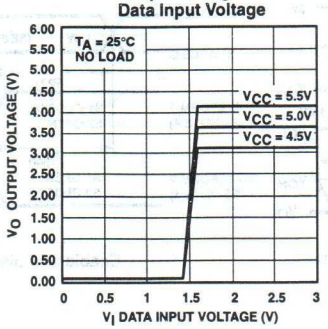
1. All pauses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_{OUT} = 50W, 1R ≤ 15ns, 1F ≤ 6ns
2. When measuring propagation delay times and skew, switches S1 and S2 are open.
3. Each enable is tested separately.
4. Waveform 1 is for an output with internal condition such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal condition such that the output is high except when disabled by the output control.
5. C_L includes probe and jig coapacitance.

TYPICAL PERFORMANCE CHARACTERISTICS

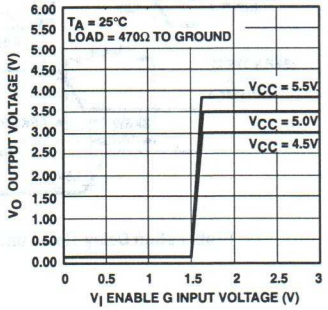
Output Voltage vs Data Input Voltage



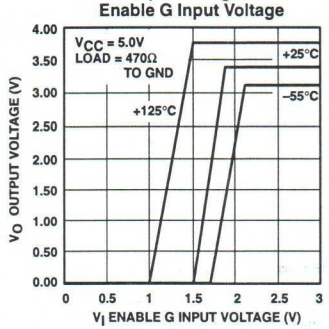
Output Voltage vs Data Input Voltage



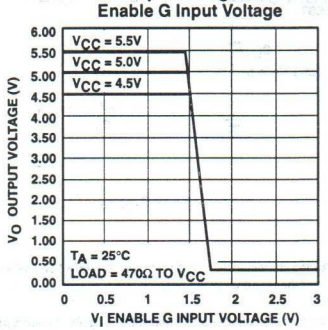
Output Voltage vs Enable G Input Voltage



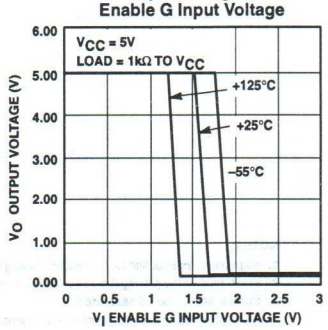
Output Voltage vs Enable G Input Voltage



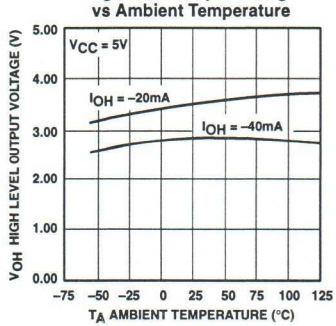
Output Voltage vs Enable G Input Voltage



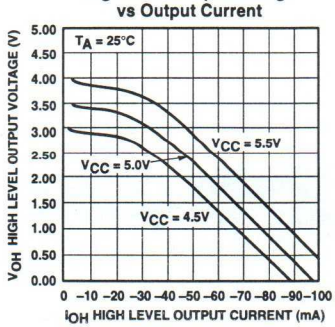
Output Voltage vs Enable G Input Voltage



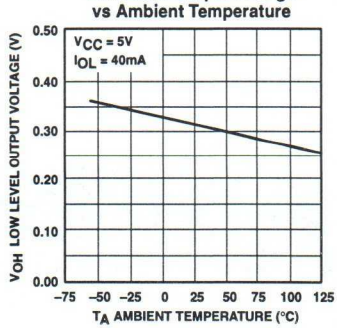
High Level Output Voltage vs Ambient Temperature



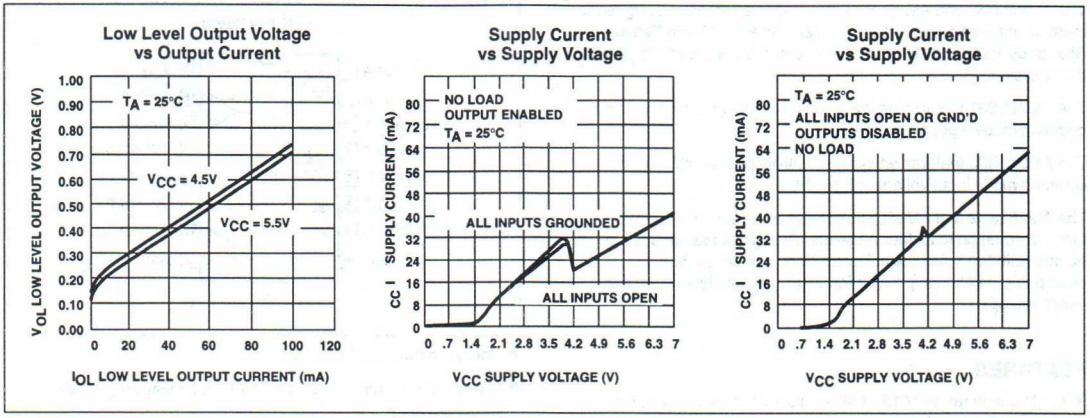
High Level Output Voltage vs Output Current



Low Level Output Voltage vs Ambient Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



Quad high-speed differential line receivers

AM26LS32/ AM26LS33

DESCRIPTION

The AM26LS32 and AM26LS33 are quad line receivers designed to meet all of the requirements of RS-422 and RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

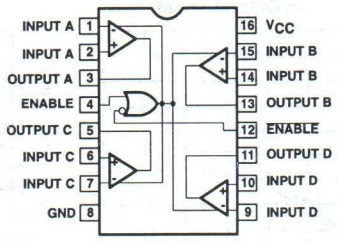
The AM26LS32 features an input sensitivity of ±200mV over the common mode input range of ±7V.

The AM26LS33 features an input sensitivity of ±500mV over the common mode input voltage range of ±15V.

The AM26LS32 and AM26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-State outputs with 8mA sink capability and incorporate a fail-safe input-output relationship which forces the outputs high when the inputs are open.

PIN CONFIGURATION

D and N Packages



TOP VIEW

FEATURES

- Input voltage range of 15V (differential or common mode) on AM26LS33; 7V (differential or common mode) on AM26LS32
- ±0.2V sensitivity over the input voltage range on AM26LS32
- ±0.5V sensitivity on AM26LS33
- 6kΩ minimum input impedance
- The AM26LS32 meets all the requirements of RS-422 and RS-423
- Operation from single +5V supply
- Fail safe input-output relationship. Output always high when inputs are open
- 3-State drive, with choice of complementary output enables, for receiving directly onto a data bus
- 3-State outputs disabled during power up and power down

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0°C to +70°C	AM26LS32CN	0406C
16-Pin Small Outline (SO) Package	0°C to +70°C	AM26LS32CD	0005D
16-Pin Plastic Dual In-Line Package (DIP)	–40°C to +85°C	AM26LS32IN	0406C
16-Pin Small Outline (SO) Package	–40°C to +85°C	AM26LS32ID	0005D
16-Pin Plastic Dual In-Line Package (DIP)	–55°C to +125°C	AM26LS32MN	0406C
16-Pin Plastic Dual In-Line Package (DIP)	0°C to +70°C	AM26LS33CN	0406C
16-Pin Small Outline (SO) Package	0°C to +70°C	AM26LS33CD	0005D
16-Pin Plastic Dual In-Line Package (DIP)	–40°C to +85°C	AM26LS33IN	0406C
16-Pin Small Outline (SO) Package	–40°C to +85°C	AM26LS33ID	0005D
16-Pin Plastic Dual In-Line Package (DIP)	–55°C to +125°C	AM26LS33MN	0406C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	7	V
V_{IN}	Power supply	7	V
	Output sink current	50	mA
	Common mode range	±25	V
V_{TH}	Differential input voltage	±25	V
T_{STG}	Storage temperature range	–65 to +150	°C

DISSIPATION OPERATING TABLE

PACKAGE	POWER DISSIPATION	DERATING FACTOR	ABOVE T_A
N	1,275mW	10.2mW/°C	25°C
D	1,262W	10.1mW/°C	25°C

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10% for AM26LS32/33MX, V_{CC} = 5.0V ±5% for AM26LS32/33CX and AM26LS32/33IX over operating temperature range unless otherwise specified.

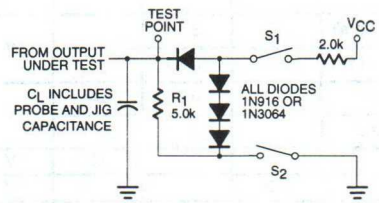
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS AM26LS32/33 Min	LIMITS AM26LS32/33 Typ[1]	LIMITS AM26LS32/33 Max	UNIT
V_{TH}	Differential input voltage	$V_{OUT} = V_{OL}$ or V_{OH} AM26LS32, $-7V \le V_{CM} \le +7V$		–0.2		0.2	V
		AM26LS33, $-15V \le V_{CM} \le +15V$		–0.5		0.5	
R_{IN}	Input resistance	$-15V \le V_{CM} \le +15V$ (One input AC ground)		6.0	9.8		kΩ
I_{IN}	Input current (under test)	$V_{IN} = +15V$ Other input $-15V \le V_{IN} \le +15V$				2.3	mA
I_{IN}	Input current (under test)	$V_{IN} = -15V$ Other input $+15V \le V_{IN} \le -15V$				–2.8	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., I_{OH} = –440µA ΔV_{IN} = +1.0V V_{ENABLE} = 0.8V	Com'l	2.7	3.4		V
			Mil	2.5	3.4		
V_{OL}	Output LOW voltage	V_{CC} = Min., V_{ENABLE} = 0.8V ΔV_{IN} = +1.0V	I_{OL} = 4.0mA		0.3	0.4	V
			I_{OL} = 8.0mA			0.45	
V_{IL}	Enable LOW voltage					0.8	V
V_{IH}	Enable HIGH voltage			2.0			V
V_I	Enable clamp voltage	V_{CC} = Min., I_{IN} = –18mA				–1.5	V
I_O	Off state (high impedance) output current	V_{CC} = Max.	V_O = 2.4V			20	µA
			V_O = 0.4V			–20	
I_{IL}	Enable LOW current	V_{IN} = 0.4V			–0.2	–0.36	mA
I_{IH}	Enable HIGH current	V_{IN} = 2.7V			0.5	20	µA
I_I	Enable input HIGH current	V_{IN} = 5.5V			1	100	µA
I_{SC}	Output short circuit current	V_{CC} = Max., ΔV_{IN} = +1V, V_{OUT} = 0V		–15	–60	–85	mA
I_{CC}	Power supply current	V_{CC} = Max.; All V_{IN} = GND outputs disabled			52	70	mA
V_{HYST}	Input hysteresis	T_A = 25°C, V_{CC} = 5.0V, V_{CM} = 0V	AM26LS32		120		mV
			AM26LS33		120		
t_{PLH}	Input to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF (see test condition)			10	25	ns
t_{PHL}	Input to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF (see test condition)			10	25	ns
t_{LZ}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 5pF (see test condition)			15	30	ns
t_{HZ}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 5pF (see test condition)			12	22	ns
t_{ZL}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF (see test condition)			8	22	ns
t_{ZH}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF			9	22	ns

NOTE:
1. All typical values are T_A = 25°C, V_{CC} = 5.0V.

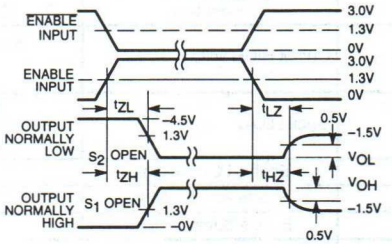
FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUT	ENABLES E	ENABLES $\overline{E}$	OUTPUT
$V_{ID} \geq V_{TH}$	H	X	H
	X	L	H
$V_{TL} \leq V_{ID} \leq V_{TH}$	H	X	?
	X	L	?
$V_{ID} \leq V_{TL}$	X	L	L
	H	X	X
X	L	H	Z

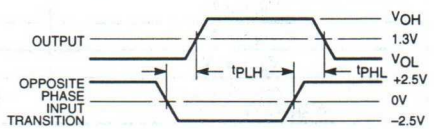
NOTES:
H = High level, L = Low level, X = Irrelevant
Z = High impedance (off), ? = Indeterminate
E = Enable, $\overline{E}$ = $\overline{\text{Enable}}$



Load Test Circuit for 3-State Outputs



Enable and Disable Tmes[2, 3, 4]



Propagation Delay[1, 4]

NOTES:
1. Diagram shown for $\overline{\text{Enable}}$ Low.
2. Enable is tested with $\overline{\text{Enable}}$ High; $\overline{\text{Enable}}$ is tested with Enable Low.
3. S_1 and S_2 of Load Circuit are closed except where shown.
4. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_O = 50Ω; t_r ≤ 15ns; t_f ≤ 6.0ns.

High-speed FSK modem transmitter — NE5080

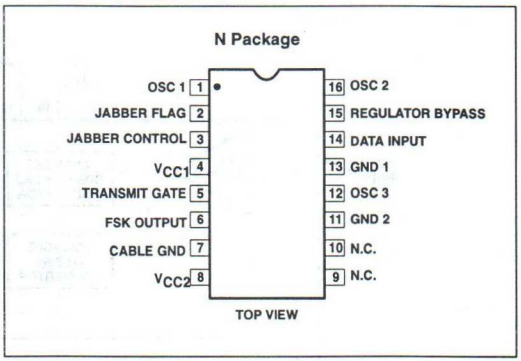
DESCRIPTION

The NE5080 is the transmitter chip, of a two-chip set, designed to be the heart of an FSK modem. (The NE5081 is the receiver chip.) The chips are compatible with the IEEE 802.4 standard for a "Single-Channel" Phase-Continuous-FSK Token Bus." The specifications shown in this data sheet are those guaranteed when the transmitter is tuned for the frequencies given in the 802 standard. However, both the NE5080 and the NE5081 may be used at other frequencies. The ratio of logic high to logic low frequencies is normally at 1.67 to 1.00 at any center frequency; however, it can be varied externally. (See AN1950.)

APPLICATIONS

- Local Area Networks
- Point-to-point communications
- Factory automation
- Process control
- Office automation

PIN CONFIGURATION



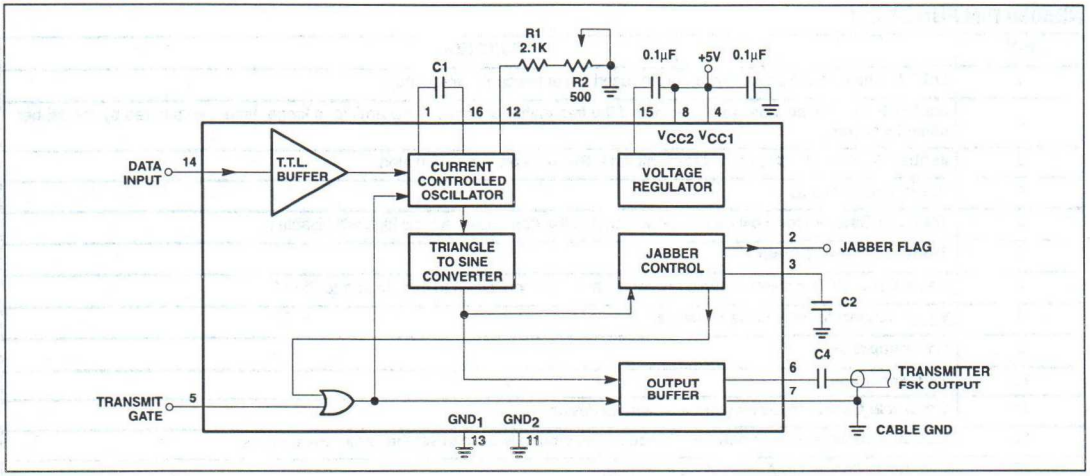
FEATURES

- Meets IEEE 802.4 standard
- Data rates to several Megabaud
- Half- or full-duplex operation
- Jabber function on-chip

ORDERING CODE

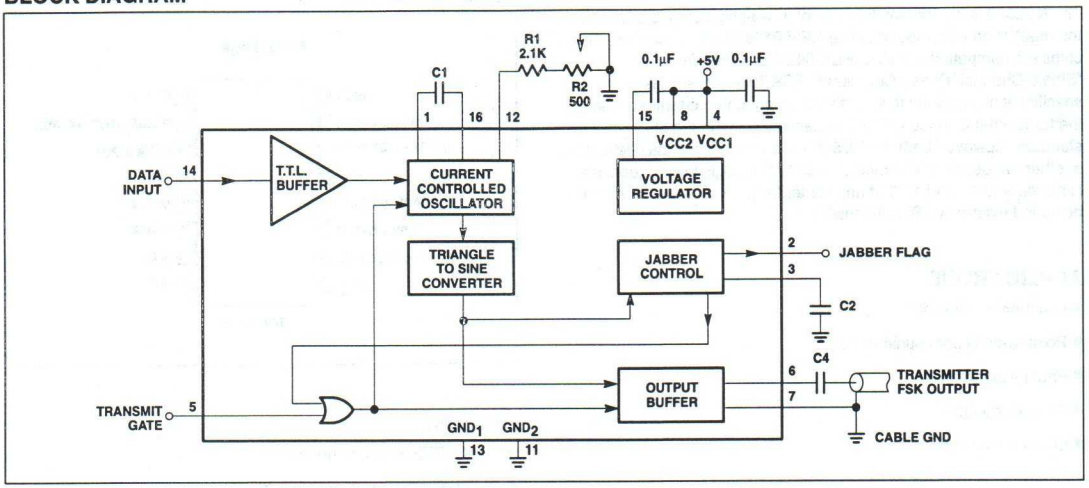
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5080N	0406C

BLOCK DIAGRAM



High-speed FSK modem transmitter | NE5080

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC1} V_{CC2}	Supply voltage	+6	V
V_{IN}	Input voltage range (Data, Gate)	–0.3 to V_{CC}	V
P_D	Power dissipation	800	mW
T_A	Operating temperature range	0 to + 70	°C
T_J	Maximum junction temperature	+150	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead temperature (soldering, 10 sec)	300	°C

NE5080 PIN FUNCTION

PIN	FUNCTION
1	**OSC 1:** One end of the external capacitor used to set the carrier frequency.
2	**Jabber Flag:** This pin goes to a logic high if the transmitter attempts to transmit for a longer time than allowed by the Jabber control function.
3	**Jabber Control:** Used to control transmit time. See note on Jabber function.
4	**V_{CC1}:** Voltage supply.
5	**Transmit Gate:** A logic flow on this pin will enable the transmitter; a logic high will disable it.
6	**Transmitter FSK Output**
7	**Cable Ground:** The shield of the coax cable should be connected to this pin and to Pin 11.
8	**V_{CC2}:** Connect to Pin 4 close to device.
9	**No Connection**
10	**No Connection**
11	**Ground 2:** Connect to Analog ground close to device.
12	**OSC 3:** A variable resistor between this point and ground is used to set the carrier frequencies.
13	**Ground 1:** Connect to Analog close to device.
14	**Data Input**
15	**Regulator Bypass:** A bypass capacitor between this pin and V_{CC1} is required for the internal voltage regulator function.
16	**OSC 2:** One end of a capacitor that is between Pin 1 and Pin 16 and is used to set the carrier frequency.

GENERAL DESCRIPTION

The NE5080 is designed to transmit high frequency asynchronous data on coaxial cable, at rates from DC to 2M baud (see Note 1). The chip accepts serial data and transmits it as a periodic signal whose frequency depends on whether the data is high or low.

The device is meant to operate at a frequency of 6.25MHz for a logic high and 3.75MHz for a logic low (see Note 2). The frequency is set up by external trimming components; however, the ratio of the high and low frequencies is set internally and cannot be altered.

The FSK output can be turned off by use of the transmit gate pin. When turned off, the transmitter has a high output impedance and the oscillator is disabled.

The length of time a transmitter can transmit can be controlled by the use of the Jabber control pin (see description of Jabber Control Pin).

Jabber Control Pin

During the time the transmitter is transmitting, this pin sources a current. This current can be used to set the maximum time that the transmitter can be on. There are three options that can be used:

1. Use the current to charge a capacitor. When the voltage across the cap gets to approximately 1.4V, the transmitter will turn off. A logic low applied to Pin 3 will reset the Jabber function; an open collector output should be used for this purpose. A logic high applied to the pin will disable the transmitter.
2. Use to externally sense the current and have external circuitry to control the length of time the transmitter is on.
3. The pin can be tied to ground and is then not active. Transmission is then controlled solely by the signal at the transmit gate pin.

Jabber Flag Pin

This pin will go to a logic high when the Jabber Control pin is used to shut off the transmitter. It will latch and can be reset by applying a logic low to the Jabber Control pin.

NOTES:
1. The NE5080 is capable of transmitting up to 1M baud of differential Manchester code at a center frequency of 5MHz.
2. Although the chip is designed to meet the requirements of IEEE standard 802.4 (Token-Passing Single-Channel Phase-Continuous-FSK Bus), it can be used at other frequencies.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_S	Setup time	Data in	Gate on	Figure 1	2	0.1		µs
t_A	Delay time	Output freq. change	Data transition	Figure 2			150	ns
t_B	Delay time	Output disabled	Gate off	Figure 3		0.4	2	µs
t_C	Delay time	Output disabled	Jabber control	Figure 4			100	ns
t_D	Delay time	Jabber flag	Jabber control	Figure 5			100	ns
	Jabber control reset Pulse width (Logic low)				100			ns

DC ELECTRICAL CHARACTERISTICS

$V_{CC1,2}$ = 4.75–5.25V, T_A = 0°C to +70°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_1	Output frequency (Logic high)	Data input ≥2.0V (See Note 1)	6.17	6.25	6.33	MHz
f_0	Output frequency (Logic low)	Data input ≤0.8V (See Note 1)	3.67	3.75	3.83	MHz
V_O	Output amplitude	Data input ≥2.0V or ≤0.8V Output Load = 37.5Ω	0.5		1.0	V_{RMS}
R_{OFF}	Output impedance (gated off)	Transmit gate ≥2.0V	100			kΩ
R_{ON}	Output impedance (gated on)	Transmit gate ≤0.8V			37.5	Ω
C_O	Output capacitance	Transmit gate ≥2.0V or ≤0.8V			10	pF
V_F	Feedthrough	Transmit gate ≥2.0V 2.0MHz sq. wave (TTL levels) input			1	mV_{RMS}
I_J	Jabber current	Transmit gate ≤0.8V Input ≥2.0V or ≤0.8V		1.25		µA
I_{CC}	Supply current	V_{CC1} connected to V_{CC2}		75	100	mA
Logic levels						
	Data Input					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V
I_{IH}	Input current	V_{IN} = 2.4V			40	µA
I_{IL}	Input current	V_{IN} = 0.4V			–1.6	mA
	Transmit gate					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V
I_{IH}	Input current	VG = 2.4V			40	µA
I_{IL}	Input current	VG = 0.4V			–1.6	mA
	Jabber flag					
V_{OH}	Logic high	I_{OH} = –400µA	2.4			V
V_{OL}	Logic low	I_{OL} = 4.0mA			0.4	V
	Jabber control					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V

NOTE:
1. Tuned per instructions in AN195.

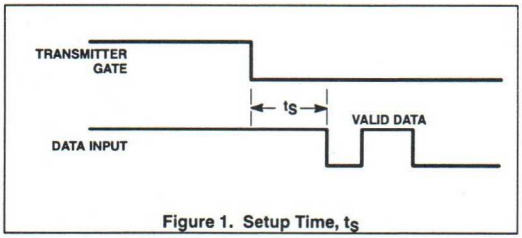


Figure 1. Setup Time, t_S

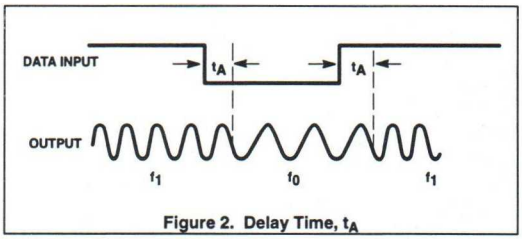


Figure 2. Delay Time, t_A

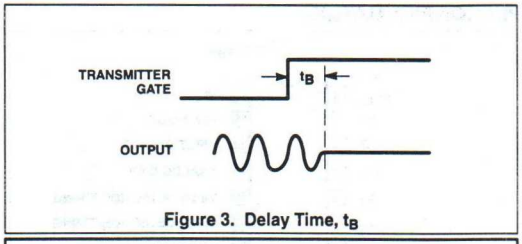


Figure 3. Delay Time, t_B

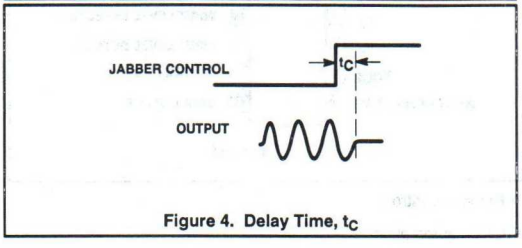


Figure 4. Delay Time, t_C

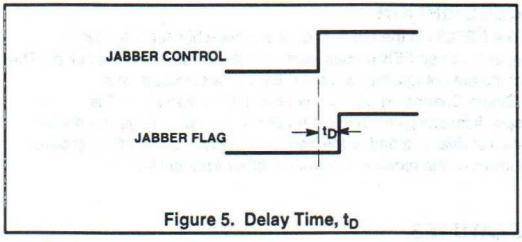


Figure 5. Delay Time, t_D

High-speed FSK modem receiver

NE5081

DESCRIPTION

The NE5081 is the receiver chip of a two-chip set designed to operate as an FSK modem (the NE5080 is the transmitter chip). The chips are compatible with the IEEE 802.4 standard for a "Single-Channel Phase-Continuous-FSK Token Bus." The specifications given in this data sheet are those guaranteed when the receiver is tuned to the frequencies given in the 802 standard. However, the receiver will work at other frequencies.

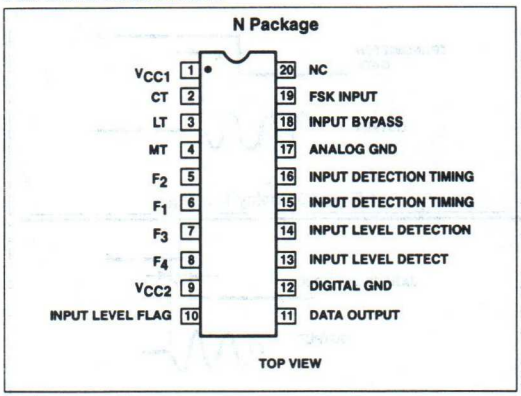
FEATURES

- Meets IEEE 802.4 standard
- Data rates to several Megabaud
- Half- or full-duplex operation
- Low bit rate error (10^{-12} typical)

APPLICATIONS

- Local Area Networks
- Point-to-point communications
- Factory automation
- Process control
- Office automation

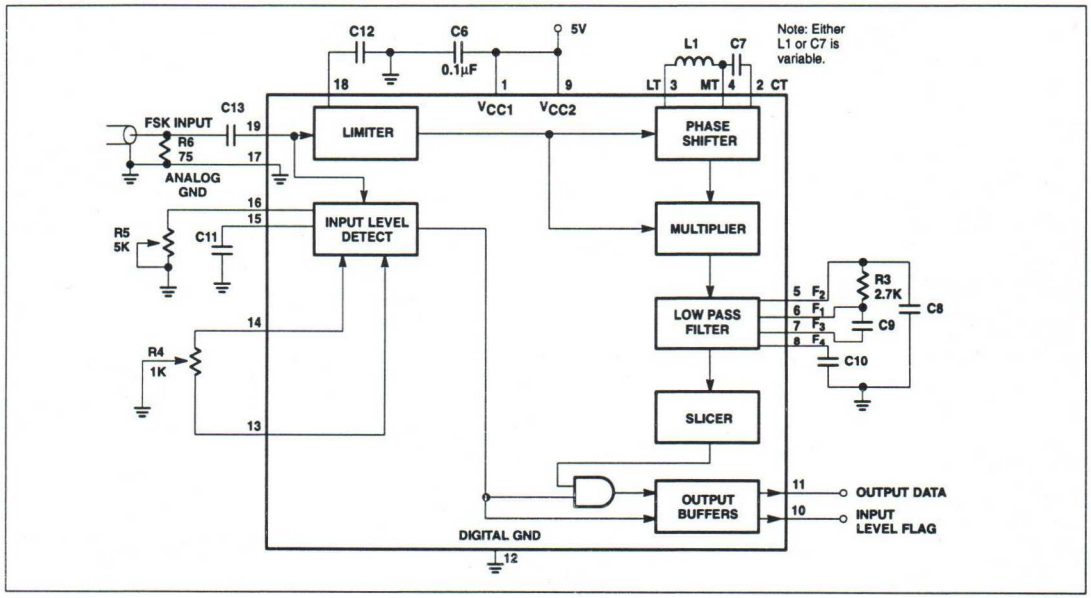
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	0°C to +70°C	NE5081N	0408B

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C

SYMBOL	PARAMETER	RATING	UNIT
V_{CC1} V_{CC2}	Supply voltage	+6	V
V_{IN}	Input voltage range	–0.3 to +V_{CC}	V
I_{DO}	Output (Data, Level detect) Max sink current	20	mA
P_D	Maximum power dissipation, T_A = 25°C, (still-air)[1] N package	1690	mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	300	°C
	Max differential voltage between analog and digital grounds	100	mV

NOTE:
1. Derate above 25°C as follows:
   N package at 13.5mW/°C.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1, 2}$ = 4.75–5.25V. External LC circuit tuned to 5MHz. Input level detect set at 16mV_{RMS}, T_A = 0°C +70°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_0	Logic Low Frequency	External LC tuned to 5MHz	3.67	3.75	3.83	MHz
f_1	Logic High Frequency	External LC tuned to 5MHz	6.17	6.25	6.33	MHz
IN_{DL}	Minimum Input Detect Level	Minimum input level that is detected as carrier (See Note 2 in General Description)	5		50	mV_{RMS}
	Logic Levels:					
V_{OL}	Data Output	I_{OL} = 4.0mA V_{IN} > 16mV_{RMS} Freq = f_0			0.4	V
V_{OH}	Data Output	I_{OH} = –400µA V_{IN} > 16mV_{RMS} Freq = f_1	2.4			V
V_{OH}	Data Output	I_{OH} = –400µA V_{IN} < 5mV_{RMS} Freq = f_0	2.4			V
V_{OL}	Input Detect Flag	I_{OL} = 4.0mA V_{IN} = 0V_{RMS}			0.4	V
V_{OH}		I_{OH} = –400µA V_{IN} > 16mV	2.4			V
I_{CC}	Supply Current	V_{CC} = 5.25V (V_{CC1} connected to V_{CC2}) V_{IN} = 1.0V_{RMS} Freq = f_1 or f_0			50	mA
BER	Bit Error Rate	Input Signal > 16mV_{RMS} maximum in-band noise = 1.6mV_{RMS}		10^{-12}	10^{-9}	

AC ELECTRICAL CHARACTERISTICS (AN195, Figure 5 with a 100KHz 1V_{P-P})

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_B	Delay Time	Input Level Detect Flag	Input On	Figure 1		0.05	1	µs
t_C	Delay Time	Input Level Detect Flag	Input Off	Figure 1	0.5	1.5	2.5	µs
t_D	Delay Time	Output Enabled	Input On	Figure 2			2	µs
t_E	Delay Time	Output Disabled	Input Off	Figure 2	0.5	1.5	2.5	µs
	Required Delay	Carrier Turn Off	Valid Data End		2			µs

High-speed FSK modem receiver | NE5081

GENERAL DESCRIPTION

The NE5081 will accept an FSK-encoded signal and provide the demodulated digital data at the output. It is optimized to work at frequencies specified in IEEE 802.4—Token-Passing Single-Channel Phase-Continuous-FSK Bus—(i.e., 3.75MHz and 6.25MHz). However, it will work at other frequencies.[1]

Its normal acceptable input signal level range is from 16mV$_{RMS}$ to 1V$_{RMS}$. This can be adjusted.[2]

The receiver will yield an undetected "Bit Error Rate" of 10^{-9} or lower when receiving signals with a 20dB signal-to-noise ratio. It has a maximum output Jitter of ± 40ns.[3]

NOTES:

1. The receiver can be tuned to accept different frequencies by adjustment of the LC circuit shown in Figure 7. However, the external components have been optimized for 3.75MHz and 6.25MHz. See "Determining Component Values" for use at other frequencies.
2. Input Level Detect
   This is a method of turning off the output of the receiver when the input signal falls below an acceptable level. This level is adjustable within the range given in the electrical specification section. The purpose of this function is to minimize the effect of noise on receiver performance and to indicate when there is an acceptable signal present at the input. All specifications given in this data sheet are with the input level detection set at 16mV$_{RMS}$.
3. Jitter (Definition)
   This is a measure of the ability of the receiver to accurately reproduce the timing of its FSK-coded digital input. The spec indicates the error band in the timing of a logic level change.

FUNCTION TABLE

PIN	FUNCTION
1	**V$_{CC1}$:** Should be connected to the 5V supply and Pin 9.
2	**CT:** One end of an external capacitor that is used to tune the receiver.
3	**LT:** One end of an indicator that is used to tune the receiver.
4	**MT:** The junction of the capacitor and inductor used for tuning the receiver.
5	**F2**
6	**F1** Pins 5, 6, 7, 8 are used for a low-pass filter to remove carrier
7	**F3** harmonics from the data output.
8	**F4**
9	**V$_{CC2}$:** Connect to Pin 1 (see Pin 1 function) close to the device.
10	**Input Level Flag:** This pin is used to indicate when there is a signal at the input that is greater than the level set by the input level detection circuitry. A logic high indicates an input greater than the set level.
11	**Data Output:** Supplies T^{2}L level data that corresponds to the FSK input received.
12	**Digital Ground:** Should be connected to digital ground.
13, 14	**Input Level Detect:** These pins are used to set the level of input signal that the device will accept as valid.
15	**Input Detection Timing:** An external capacitor between this pin and ground is used to determine the time from carrier turn-off to output disable.
16	**Input Detection Timing:** Same as Pin 15, except that a resistor goes between this pin and ground. The values of the C and R depend on the carrier frequency. The values given in this data sheet are for a 5MHz carrier center frequency.
17	**Analog Ground:** Connect to analog ground close to the device.
18	**Input Bypass:** A capacitor between this pin and ground is used to bypass the input bias circuitry.
19	**Input:** The FSK signal from the cable goes to this pin.
20	**No Connection.**

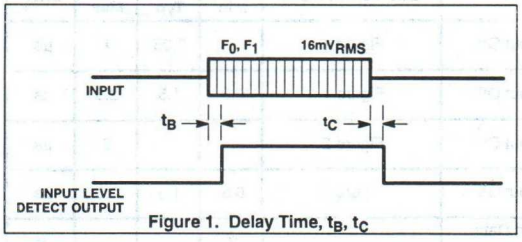


Figure 1. Delay Time, t_B, t_C

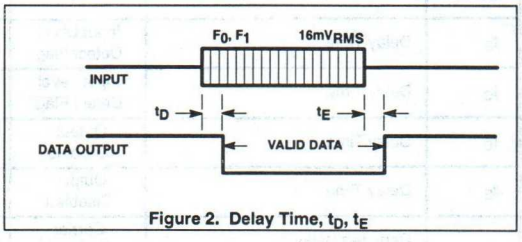


Figure 2. Delay Time, t_D, t_E

Applications using the NE5080, NE5081 — AN195

APPLICATIONS

Figure 1 shows a block diagram of the NE5080 and NE5081 in a simple point-to-point communications scheme Pin 5 of the NE5080 is grounded to permanently enable transmission; grounding Pin 3 disables the jabber function.

An example of a communications system block diagram using the NE5080 and the NE5081 (as in a modem) is shown In Figure 2.

The jabber function is active in this system. The NE5080 Jabber Flag (Pin 2) goes high when the capacitor at Pin 3 of the NE5080 charges to about 1.4V. This fault condition will interrupt the Transmission Controller which will cease transmitting and write to the proper address for the decoder to put out signal to discharge the capacitor. The Controller will then pass the token to the next node.

The transmission medium can be anything from a twisted pair to a fiber optic link. The NE5081 receives the FSK signal and converts it to a digital data stream corresponding to the data sent by the NE5080. Pin 10 of the NE5081 goes high when the signal at its input is above the threshold set by the potentiometer between Pins 13 and 14 of the NE5081.

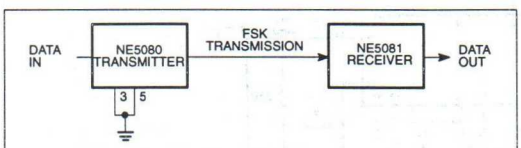


Figure 1. Point-to-Point Communications

DC-to-2 Megabaud Modem Using the NE5080 and NE5081

The NE5080 and NE5081 are designed to be used together as an asynchronous modem. They employ FSK modulation at high carrier frequencies, plus filtering to reject EMI and RFI noise that is frequently encountered in industrial and commercial environments. Figures 4 and 5 show full- and half-duplex modems.

The carrier frequency is externally adjustable and can range from 50kHz to over 20MHz.

The modem can be used in a number of ways:

1. Multidrop party line of data transmitting and receiving devices (local area networks).
2. Point-to-Point operation connecting just two transmitting/receiving devices.
3. Either of the above operated on one cable in the half-duplex mode.
4. Either 1 or 2 above operated on two cables in the full-duplex mode.

The 30dB dynamic range of modems built using the NE5080 and NE5081 makes it possible to attach them at any point on the cable without any gain adjustment. There is no problem with proximity to other similar modems.

The distance that can be driven varies with the type of cables used, the number of modems attached to the cable, and the carrier frequency.

Typical operation can be 100 modems randomly spaced on up to 2000 meters of RG-11 (foam) cable with a center frequency of 5MHz.

In point-to-point operation one can drive further. Table 1 gives obtainable distances when different carrier frequencies and cables are used.

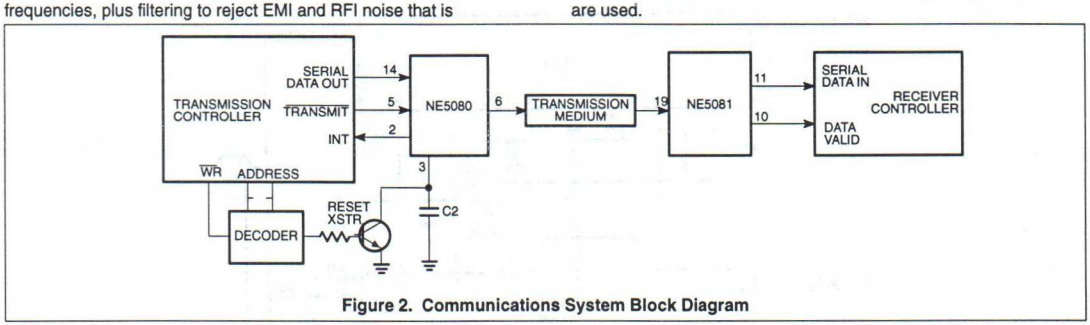


Figure 2. Communications System Block Diagram

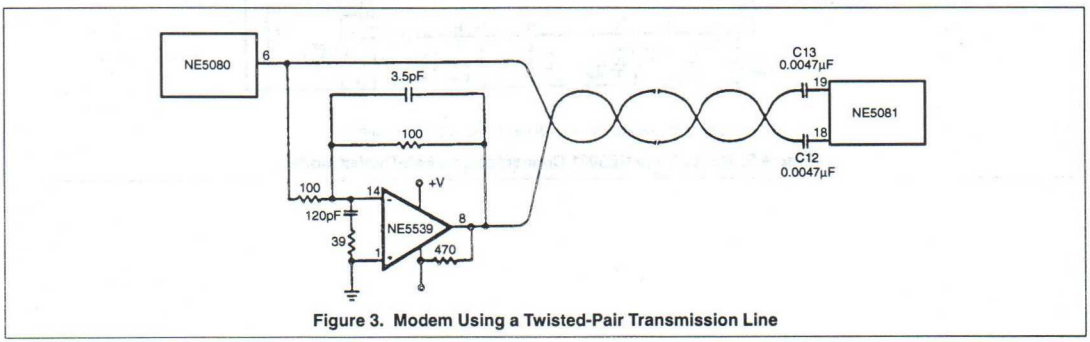
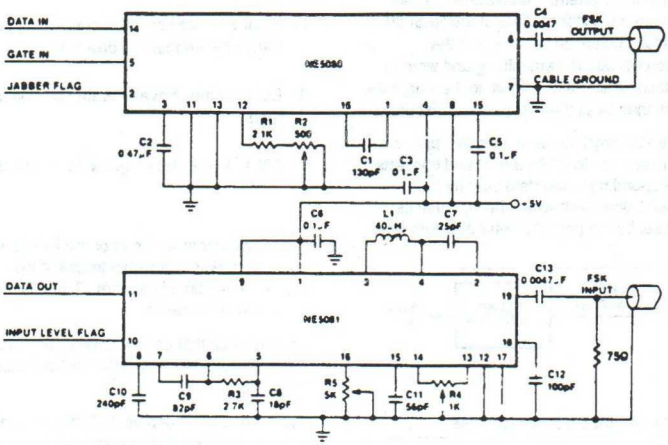


Figure 3. Modem Using a Twisted-Pair Transmission Line

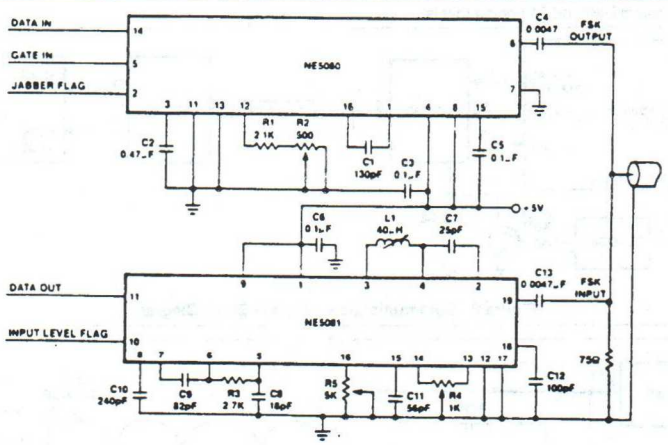
Table 2. Transmission Distance for a Single Receiver as a Function of Center Frequency and Cable Type

Carrier Frequency	Maximum Data Rate	Cable			
		RG-59	RG-11 (Foam)	T4412J	T4750J
1MHz	0.5 Megabaud	6000 Ft	21000 Ft	33000 Ft	50000 Ft
3MHz	1.0 Megabaud	5000 Ft	12000 Ft	20000 Ft	32000 Ft
5MHz	2.0 Megabaud	4200 Ft	9500 Ft	15000 Ft	25000 Ft



EXTERNAL COMPONENTS SHOWN HERE ARE FOR 5MHz CARRIER

Figure 4. NE5080 and NE5081 Connected as a Full-Duplex Modem



EXTERNAL COMPONENTS SHOWN HERE ARE FOR 5MHz CARRIER

Figure 5. NE5080 and NE5081 Connected as a Half-Duplex Modem

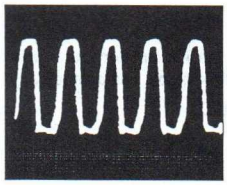


Figure 6. NE5081 Data Output When Correctly Tuned to Incoming 5MHz Carrier

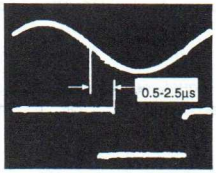


Figure 7. Correct Adjustment of Input Level Detection Timing

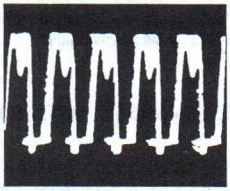


Figure 8. NE5081 Data Output When Tuned Just Below 5MHz Carrier

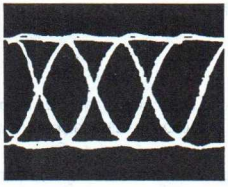


Figure 9. 'Eye' Pattern at NE5081 Pin 8

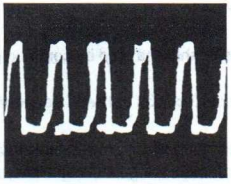


Figure 10. NE5081 Data Output Tuned Just Above 5MHz Carrier

FSK MODEM SETUP PROCEDURES

To set up the modem per IEEE 802.4 specifications, the following sequence should be followed at 25 ±2°C ambient.

TRANSMITTER SETUP:

1. Ground Jabber Control (Pin 3) and the transmit gate (Pin 5) of the NE5080.
2. Turn on the power and allow the circuit to warm up for 3 minutes
3. Hold the Data Input (Pin 14) of the NE5080 at a logic high
4. Measure the frequency at the FSK output of the transmitter (cable should be properly terminated) and adjust R2 for a frequency reading of 6.250MHz ±5kHz.
5. Apply a logic low to the Data Input and check the output frequency. If the reading is not 3.750MHz ±40kHz, readjust R1 until the high frequency is 6.250MHz ±25kHz and the low frequency is 3.750MHz ±40kHz.

Transmitter setup is now complete.

RECEIVER SETUP

6. Set Detection Timing pot R5 and Input Level Detect pot R4 at the NE5081 to mid range.
7. Apply a 5.000MHz 1V_{P-P} sine wave to the receiver FSK Input.
8. Attach an oscilloscope probe to the Data Output pin of the NE5081 and adjust L1 or C7 (whichever is adjustable) until the output state alternates between high and low levels. Figures 7 and 8 indicate examples of improper tuning.
9. Set the generator to 3.750MHz, 35mV_{P-P}.
10. Adjust input Level Detect pot R4 until the Data Output pin is alternating between high and low levels.
11. Increase the generator output to 45mV_{P-P} and verify that the data output is low.
12. Decrease the generator output to 25mV_{P-P} and verify that the data output is high.
13. Apply a 100kHz 1V_{P-P} signal to the FSK input and connect a scope probe to the Input Level Flag and another probe to the FSK Input. Adjust Detection Timing pot R5 so that the delay from the time the FSK Input signal goes through 0 volts on the Positive to negative transition, to the time when the Input Level Flag goes from high to low, is between 0.5 and 2.5µs. See Figure 9.
14. For final adjustment to the tuning of L1/C7 use an adjusted transmitter to transmit pseudo random data and tune the receiver L1/C7 tank circuit for minimum jitter and symmetrical eye pattern observed on the receiver Pin 8 (see Figure 10).

This concludes the receiver setup procedure.

DETERMINING COMPONENT VALUES

Power supply pins of both devices should be bypassed with high quality 0.1µF capacitors close to the devices. Additionally, the

NE5081 V_{CC2} (Pin 5) should be well-decoupled from the power supply by a small inductor (about 10μH) and another 0.1μF capacitor as the NE5081 exhibits large changes in power supply current during switching.

The coupling capacitors C~4 and C13 are needed to maintain input bias when a low DC impedance line is connected to the FSK input. Too small a value for these capacitors could result in excessive signal attenuation. If these capacitors are too large, the receive Input Level Flag may remain high for an excessive amount of time after the input signal is removed. Each transmitter and each receiver should have its own coupling capacitor. This is necessary to prevent any DC terminations from altering biases.

The external resistance at the NE5080 Pin 12 should always be about 2.4kΩ, with some adjustment allowable to compensate for the tolerance of C1 and slight differences between individual ICs.

C11 and R5 are the Carrier Detect timing components and determine how long after the FSK input signal is discontinued before the Input Level Flag goes low. R5 should not exceed 5kΩ. With C11 set at 56pF, a 5kΩ R5 will allow Carrier Detect Timing adjustment to 2μs. R5 can be a fixed resistor if this timing is not critical (perhaps because of the use of an "end of data" signal). This delay is required to allow the signal to propagate through the receiver. Carrier Detect Timing should be adjusted for different center frequencies by choosing C11 according to the relationship:

$$C11 = \frac{1}{3572\ f_C}$$

The Input Level Detect function can be disabled and the receiver be made to hold the Carrier Detect Flag high by removing R5 and C11 and tying Pins 15 and 16 together and pulling them up to V_{CC} with a 10kΩ resistor.

If the Jabber function is not to be used, Jabber control Pin 3 of NE5080 should be grounded. If the Jabber function is to be used a capacitor C2 should be connected between Pin 3 and ground. The value of this capacitor is determined as indicated below:

$$C2 = (0.95 \times 10^{-6})t$$

where t is the maximum allowable transmit time in seconds

The resistance R1, together with capacitor C1, set the transmit frequencies. The logic high frequency is fixed at about 1.67 times the logic low frequency, meaning that the logic low frequency is 0.75 times the center frequency f_C and the logic high frequency is 1.25 times the center frequency. Note that this center frequency is never transmitted in normal operation and is sometimes referred to as the "carrier frequency":

C1 is chosen by the relationship for f_C at or below 7MHz:

$$C1 = \frac{6.5 \times 10^4}{f_C}$$

Above 7MHz center frequency this capacitor is found by modifying this equation to

$$C1 = \frac{5.5 \times 10^4}{f_C}$$

To get the characteristics that are needed for proper operation of the NE5081, it is important to keep the proper relationship between L1 and C7:

$$C7 = \frac{1}{7885\ f_C}$$

$$L1 = \frac{200}{f_C}$$

Capacitor values of the filter are dependent upon operating frequencies to maintain proper characteristics:

$$C8 = \frac{9.0 \times 10^{-5}}{f_C}$$

$$C9 = \frac{4.1 \times 10^{-4}}{f_C}$$

$$C10 = \frac{1.2 \times 10^{-3}}{f_C}$$

$$C12 = \frac{5 \times 10^{-4}}{f_C}$$

Coupling capacitor values also depend upon center frequency

$$C4 = C13 = \frac{5 \times 10^{-2}}{f_C}$$

In all of the above equations, capacitances are in Farads, inductances in Henrys and frequencies in Hertz.

SOME COMMON BAUD RATES

Although intended to be used with a center frequency of 5MHz the NE5080 and NE5081 can be used at other carrier frequencies. Table 2 gives minimum center frequency (f_C) for some common baud rates together with external component values for those carrier frequencies. Note that it is not recommended that these devices be operated at center frequencies below 50kHz.

USING THE NE5080/NE5081 WITH A FIBER–OPTIC LINK

The NE5080/NE5081 chip set is highly suitable for use in low cost fiber-optic links. There are many advantages to fiber links over open-wire or coaxial cable links. These advantages include:

1. Cost savings in conductor weight and size.
2. Immunity to EMI/RFI.
3. Low crosstalk.
4. High communications security; cannot be tapped by electromagnetic induction or surface conduction.
5. Fiber-optic cable does not radiate electromagnetic energy nor disturb other communications media.
6. Extremely wide bandwidth (high channel per conductor density).
7. Low attenuation.
8. No ground loops or shifts caused by common grounds.
9. Complete electrical isolation between transmitter and receiver.
10. Cable breaks cause no shorts, making this technology useful in hazardous environments, e.g., explosive chemical facilities.
11. No damage to equipment is expected due to current surges on adjacent lines.

12. Fiber cable does not act as an antenna to pick up high electromagnetic pulses such as those caused by electrical storms.

13. Low BER (Bit Error Rate).

The circuit of Figure 11 shows a simplex fiber link between the NE5080 transmitter and the NE5081 receiver. The components shown are for a center frequency of 5MHz, although this frequency can be increased to 20MHz with proper selection of external component values. The NE5539 has a 350MHz unity gain bandwidth which may limit maximum operating frequencies in some systems.

Since the NE5081 can adequately accept signals below 10mV at 5MHz carrier, the gain stage (within the dashed lines of Figure 11) may be eliminated if the attenuation in the link is low. If the gain stage is used, be mindful of the bandwidth trade-off at higher gains. Refer to the NE5539 data sheet for details.

The transmitter and receiver are setup as described under FSK Modem Setup Procedure.

LAYOUT PRECAUTIONS

As is the case with any components using high frequencies, good layout practice is essential; poor layout can adversely affect performance. All lead lengths should be as short as is practical for all lines which carry RF including the tuning capacitor and resistors (C1, R1, R2) of the NE5080. Lead length is especially critical with CI which should be mounted as close to the NE5080 as is possible. A printed circuit board with a good ground plane both top and bottom is also recommended (wire-wrap is NOT recommended). The ground plane should extend below tuning capacitor C1 on both top and bottom of the board, with no other trace coming between the leads of this capacitor.

Because of the high speed switching, Pin 9 ($V_{CC}2$) of the NE5081 can exhibit a large current swing causing vertical output line, which may be eliminated by decoupling Pin 9 with a small (10µH) RF choke and a 0.05µF capacitor.

See Figure 12 for an example of a working layout.

Table 3. Recommended Minimum Center Frequency and Component Values for Various Baud Rates

Baud Rate (kBaud)	f_C (kHz)	C1	L1	C4 C13	C7	C8	C9	C10	C11	C12
9.6	50	13nF	4mH	0.50µF	2.4nF	1.8nF	8.2nF	24nF	5.6nF	10nF
19.2	50	13nF	4mH	0.50µF	2.4nF	1.8nF	8.2nF	24nF	5.6nF	10nF
38.4	100	6.8nF	2mH	0.27µF	1.3nF	0.9nF	3.9nF	12nF	2.7nF	5nF
50.1	125	5.1nF	1.6mH	0.20µF	1.0nF	750nF	3.3nF	10nF	2.2nF	3.9nF
64.0	160	3.9nF	1.3mH	0.15µF	800pF	560pF	2.5nF	7.5nF	1.8nF	3nF
128	320	2nF	625µH	0.075µF	390pF	270pF	1.3nF	3.9nF	860pF	1.6nF
256	640	1nF	312µH	0.039µF	200pF	150pF	640pF	1.8nF	430pF	750pF
512	1250	510pF	160µH	0.02µF	100pF	75pF	330pF	1.0nF	220pF	390pF
1500	3750	180pF	53µH	6.9nF	33pF	25pF	110pF	330pF	75pF	130pF
1544	4000	160pF	50µH	6.8nF	33pF	22pF	100pF	300pF	68pF	125pF
2000	5k	130pF	40µH	5.0nF	25pF	18pF	82pF	240pF	56pF	100pF
8000	20k	33pF	10µH	1.2nF	6pF	5pF	20pF	62pF	15pF	25pF

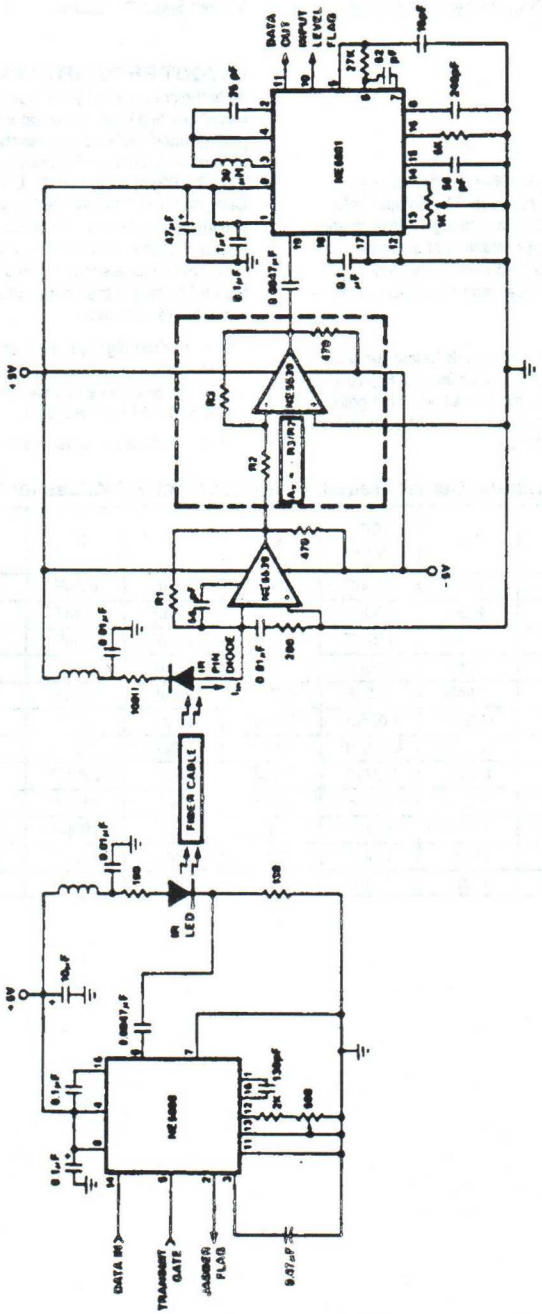
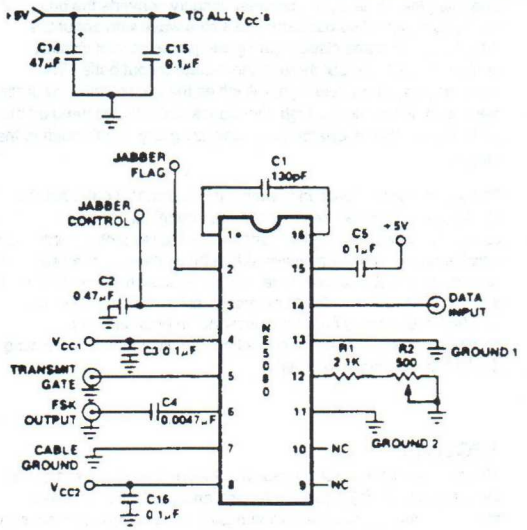
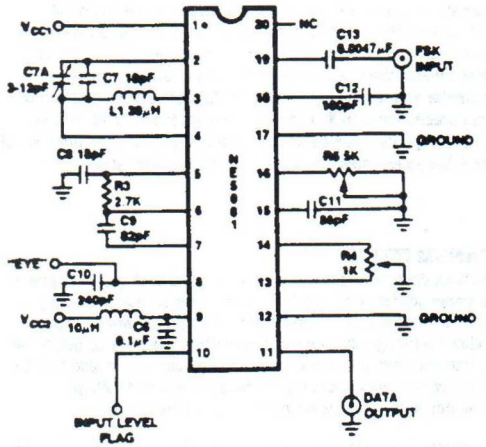


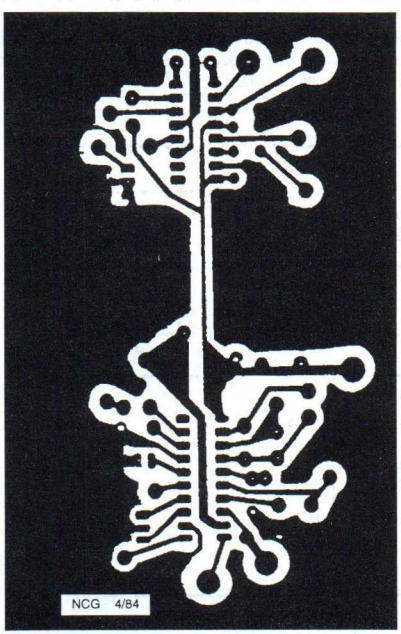
Figure 11. Simplex Fiber-Optic System



NOTE:
See NE5080 and NE5081 Block Diagram(s)



NOTE:
Signetics NE5080/NE5081 Evaluation Board



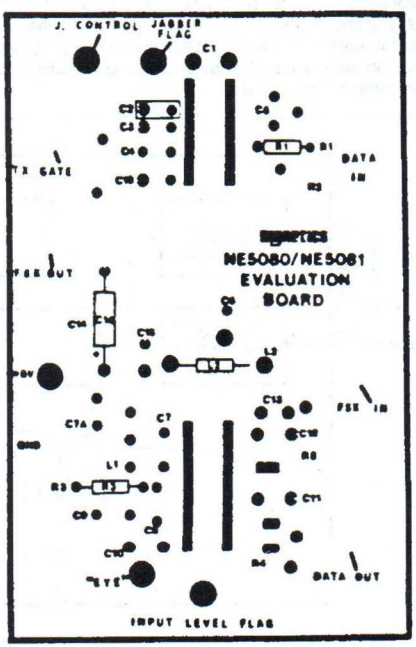


Figure 12. Components and Layout Used for Evaluation Board

Application of NE5080 and NE5081 with frequency deviation reduction

AN1950

Author: Prasanna M. Shah

INTRODUCTION

Application note AN195 discusses numerous applications of NE5080 and NE5081 in point-to-point, half-duplex and full-duplex communications using coaxial, twisted-wire pair, and fiber optic cables. It also discusses several aspects about tuning the transmitter and receiver at various center frequencies and board layout precautions. In this application note, the transmitter and receiver chips themselves are discussed. Following the brief circuit description, a few novel application ideas are discussed.

TRANSM ITTER

The block diagram of the transmitter NE5080 is shown in Figure 1. The transmitter is composed of the following six major building blocks: a TTL input buffer and switch driver, a current controller oscillator, a triangle-to-sine wave converter, a 3-state output buffer, and transmission gating and jabber control circuitry. It also has an on-chip voltage regulator that provides current and voltage references to the various building blocks of the circuit.

The transmitter center frequency can be adjusted by selecting the values of the tuning capacitor, C_O. The switch driver circuitry switches the current sources I in and out of Pins 1 and 16. This effectively changes the total average charging and discharging current into C_O from 1.5I to 2.5I, which causes the output to shift from one frequency to another. This soft switching action keeps the output phase continuous and eliminates discontinuities. The ratio of the two output frequencies is equal to the ratio of the total average current charging and discharging C_O. Since the values of the internal current sources are fixed, it produces a constant frequency ratio of 1.66. An external modification for changing this ratio through extra components is discussed later.

The triangle-to-sine wave converter circuitry converts the output of the current-controlled oscillator into a sine wave with about 2% distortion. The transmission gating and jabber control circuitry controls the FSK output through the 3-state output buffer. The transmit gate, when held high, will inhibit the transmission by putting the output buffer into the high impedance state. It also turns off the current-controlled oscillator. thus minimizing any feedthrough to the output.

The jabber control function is similar to the transmit gate, but the transmission time can be programmed through an external capacitor. There is a small current sourced to the jabber control pin, which charges up the capacitor. When the voltage on the capacitor reaches a preset threshold level, the transmission is stopped. This is a failsafe feature provided to restrict an errant transmitter or the NE5080 itself from tying up the network. In point-to-point communications, the jabber control can be disabled by connecting the jabber control pin to ground.

RECEIVER

The receiver block diagram shown in Figure 2 is composed of the following seven major building blocks: an input limiter, a phase shifter, an analog multiplier, a low-pass filter, a comparator, an input level detector, and a TTL output buffer. The input limiter limits the FSK input signal eliminating any amplitude variations.

The L and C tank circuit of the phase shifter is tuned to resonate with the incoming carrier center frequency. A quadrature detection scheme is used to demodulate the data. The balanced analog multiplier processes the incoming signal with its phase-shifted carrier frequency and generates signals with baseband data and other higher order harmonics.

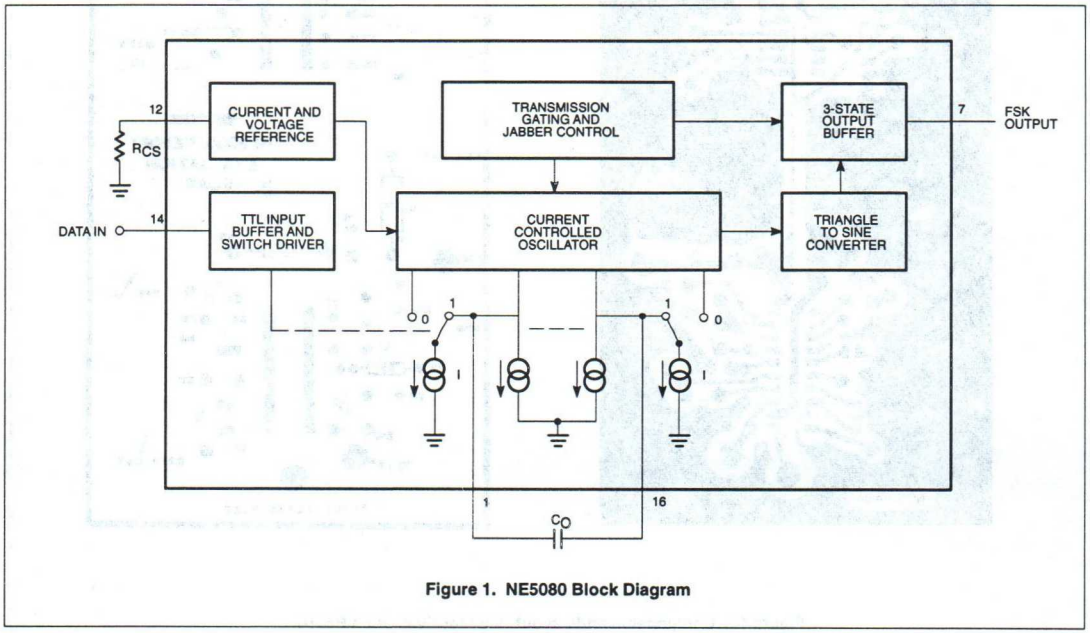


Figure 1. NE5080 Block Diagram

Application of NE5080 and NE5081 with frequency deviation reduction

AN1950

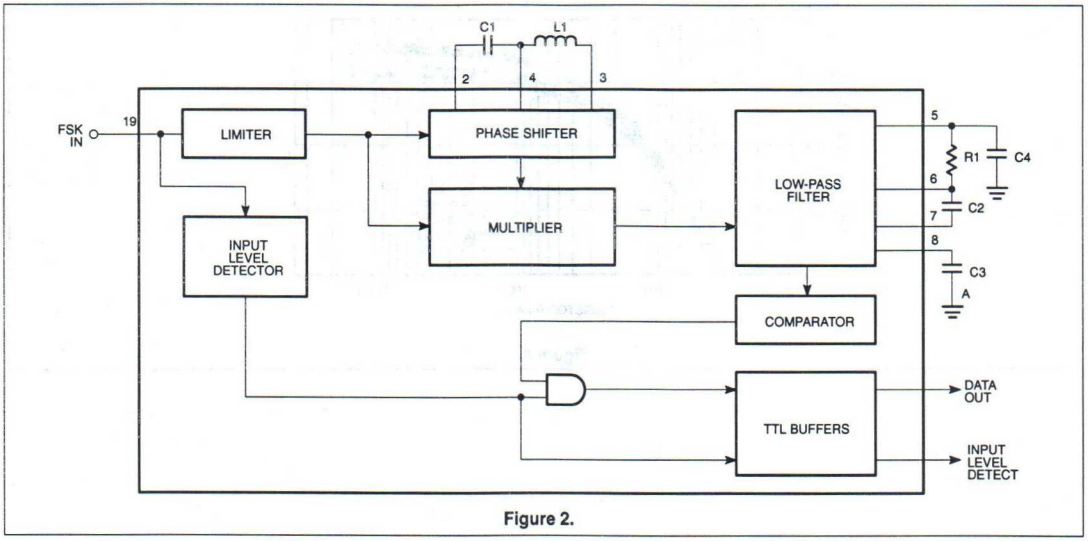


Figure 2.

The low-pass filter is a simple second-order Butterworth filter which eliminates the carrier frequency and higher-order intermodulation frequencies, and gives the baseband data which is equivalent to the signal modulated by the transmitter. The comparator makes the decision based on the output of the low-pass filter with reference to a threshold voltage. The TTL buffers provide the output data at TTL levels. The input detection level can be adjusted through the external resistor to set the threshold for minimum input level. If the input level falls below the set threshold, the output buffers are disabled, preventing the noise from being interpreted as data.

APPLICATIONS

NE5080 and NE5081 chip set encompasses a broad spectrum of data rates and facilitates economical modem design for various applications. The transmitter can be tuned to various center frequencies for different data rates. The wide dynamic range of the receiver and the excellent drive capability of the transmitter make it possible to drive long distances without any signal repeaters. The transmitter is not limited to transmitting on coaxial cable only; it can also drive a twisted-wire pair and optical fibers. All these salient features are discussed in greater detail in AN195.

The major focus of this application note is on reducing the frequency deviation. The reduction in frequency ratio can be achieved by bringing the two frequencies f_O and f_I closer together. This will reduce the overall bandwidth utilized by the modem because the main lobe in the spectrum becomes narrower. This gain in bandwidth reduction is offset by a slight increase in the probability of a bit error due to poor noise margin. As explained in the transmitter block diagram section of this application note, the frequency of the oscillator is controlled by the charging and discharging current into C_O. The two oscillating frequencies can be brought close together either by lowering the higher frequency f1 or by raising the lower frequency f_O. Figure 3 shows the technique for raising the lower frequency f_O. When the logic input is a '1', the two diodes are reversed biased. In this situation, the capacitor is charged and discharged by the current from the internal current sources. As the logic input changes to a '0', the two diodes are forward biased. This will increase the available current from the internal current sources that are charging and discharging the capacitor C_O, thus resulting in a higher frequency of oscillation than would be obtained otherwise. The value of resistor R will determine the amount of excess current available, which will affect the ratio of the higher frequency to the lower frequency (f_1/f_O).

Figure 4 gives a graph of the deviation ratio versus the resistor value R for different values of oscillator capacitor C_O. It can be seen from the graph that the deviation ratio remains constant for a fixed value of resistor R over a wide range of capacitor values C_O. It should be noted that the effective data rates will be lower when the frequency deviation is reduced. A similar scheme can also be applied to increase the frequency ratio and thereby increase the data rate, but this will be done at the cost of extra bandwidth. Using appropriate filters for the transmitters and receivers, a frequency division multiplexing (FDM) can be achieved for more efficient usage of the most expensive resource, namely the coaxial cable.

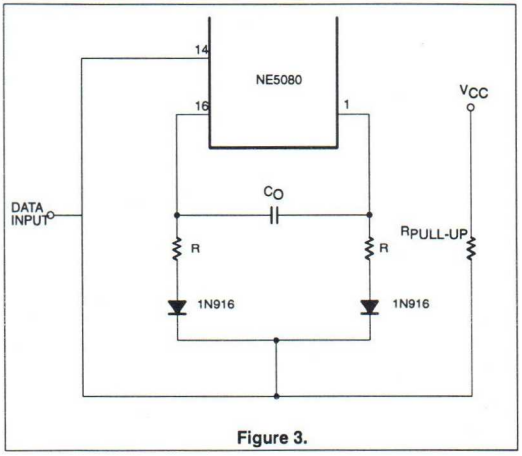


Figure 3.

Application of NE5080 and NE5081 with frequency deviation reduction

AN1950

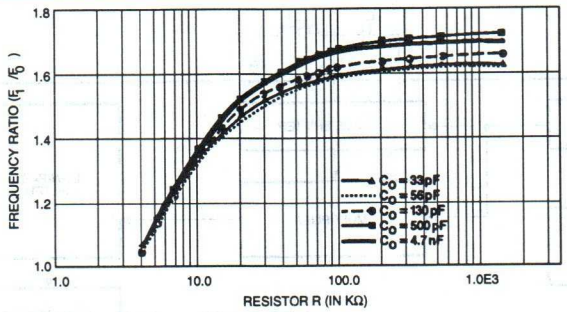


Figure 4.

Section 8
Relay/Peripheral Drivers

INDEX

Symbols and definitions for peripheral and display drivers 510
NE/SA5090 Addressable relay driver 513
NE590/591 Addressable peripheral drivers 519

Symbols and definitions for peripheral and display drivers

General Purpose/Linear ICs

BCD
Binary Coded Decimal.

$\overline{BI}$/RBO
Blanking Input or Ripple Blanking Output.

CE
Chip Enable

CLR
Clear. Clear command will preset all internal circuits to a predetermined state.

Duty Cycle
Ratio of time on to time off. Generally expressed in percentage.

f_{MAX}
The maximum clock frequency; the maximum input frequency at a clock input for the predictable performance. Above this frequency the device may cease to function.

I_{BIAS}
Input Bias Current. Current into an analog circuit input, specified at a particular voltage level.

I_{CC} ($-I_{CC}$)
Supply Current. The current flowing into the $+V_{CC}$ ($-V_{CC}$) supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst case operation unless specified.

I_H
Input High Current. The current flowing into or out of an input when a specified HIGH level voltage is applied to that input.

I_{IL}
Input Low Current. The current flowing out of an input when a specified LOW level voltage is applied to that input.

I_{OH}
Output Current Source the device can supply while maintaining a specified voltage output level.

I_{OL}
Output Low Current. The current flowing into an output when it is in the LOW state.

I_{OS}
Output Short-Circuit Current. The current flowing out of an output which is in the High state when that output is shorted to ground.

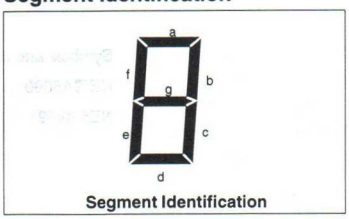
I_S
Source Current. Current flowing into the V_S supply terminal of the device with specified operating conditions.

I_{SEG}
Segment Current. The amount of current supplied to each segment as a display. Current ratios are generally compared to segment 'b'.

LED
Light-Emitting Diode.

$\overline{RBI}$
Ripple Blanking Input.

Segment Identification



Segment Identification

t_H
Hold Time. The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the current logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_{PHL}
Propagation Delay Time. The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.

t_{PLH}
Propagation Delay Time. The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{TREC}
Recovery Time. The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

t_S
Setup Time. The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

Truth Tables
0 = logic level LOW
1 = logic level HIGH
x = don't care condition; has no effect under circuit conditions listed.

Typical Value
The typical value of a particular parameter at 25°C determined by characterization of the device or sampling. Usually indicates that the particular device is not 100% tested for the parameter because it does not vary or can be determined by design and other tested

Symbols and definitions for peripheral and line drivers

variables. Occasionally typical values are given rather than min/max values because 100% testing would raise the cost of the product to a prohibitive level. If a typical value must be guaranteed to ensure specific operation, custom testing can often be provided at an additional cost to the user.

V_{BR}
Output Breakdown Voltage. Maximum voltage applied to a disabled (off) output to ensure a leakage current less than the specified value.

V_{CC} ($-V_{CC}$)
Supply Voltage. The range of power supply voltage over which the device will operate safely.

V_F
Forward voltage drop of a device at a specified current level.

V_{IH}
Input High Voltage. The range of input voltages recognized by the device as a logic HIGH.

V_{IL}
Input High Voltage. The range of input voltages recognized by the device as a logic LOW.

V_{IN}
The range of voltage on any input which the device can safely handle or a specified input voltage to the device.

V_{OH}
Output Low Voltage. The minimum guaranteed High voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.

V_{OL}
Output Low Voltage. The maximum guaranteed low voltage at an output terminal sinking the specified load current I_{OL}.

V_{OUT}
The range of voltage on any output which the device can safely handle or a specified output voltage to the device.

V_S
Source Voltage. A separate V_{CC} line depending on part type.

$\overline{XX}$
Negate Bar. When it appears over a function indicates that the "true" or valid condition of that function is a logic LOW level; i.e., LE would require a logic HIGH level to cause a latch enable; $\overline{LE}$ would require a logic LOW level to cause a latch enable.

Addressable relay driver — NE/SA5090

DESCRIPTION

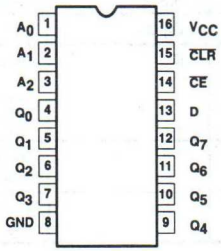
The NE/SA5090 addressable relay driver is a high-current latched driver, similar in function to the 9934 address decoder. The device has 8 open-collector Darlington power outputs, each capable of 150mA load current. The outputs are turned on or off by respectively loading a logic "1" or logic "0" into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a $\overline{CE}$ input line which also serves the function of further address decoding. A common clear input, $\overline{CLR}$, turns all outputs off when a logic "0" is applied. The device is packaged in a 16-pin plastic or Cerdip package.

FEATURES

- 8 high-current outputs
- Low-loading bus-compatible inputs
- Power-on clear ensures safe operation
- Will operate in addressable or demultiplex mode
- Allows random (addressed) data entry
- Easily expandable
- Pin-compatible with 9334 (Siliconix or Fairchild)

PIN CONFIGURATION

D[1], N Packages



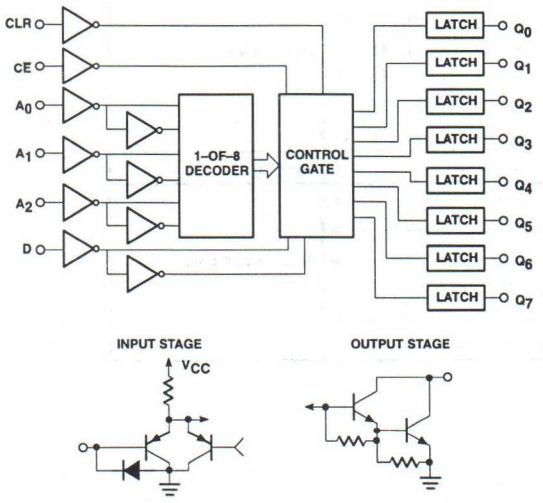
TOP VIEW

NOTE:
1. SOL - Released in Large SO package only.

APPLICATIONS

- Relay driver
- Indicator lamp driver
- Triac trigger
- LED display digit driver
- Stepper motor driver

BLOCK DIAGRAM



Addressable relay driver — NE/SA5090

PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1-3	A_0-A_2	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	Q_0-Q_7	The 8 device outputs.
13	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF"
14	CE	The chip enable. When this input is low, the output latches will accept data. When CE goes high, all outputs will retain their existing state, regardless of address of data input condition.
15	CLR	The clear input. When CLR goes low all output switches are turned "OFF". The high data input will override the clear function on the addressed latch.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline Large (SOL) Package	0 to +70°C	NE5090D	0171B
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5090N	0406C
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5090N	0406C
16-Pin Plastic Small Outline Large (SOL) Package	–40 to +85°C	SA5090D	0171B

TRUTH TABLE

INPUTS						OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	L	L	L	L	L	H	Q_{N-1} →							Addressable Latch
H	L	H	L	L	L	L	Q_{N-1} →							
H	L	L	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	L	H	H	H	Q_{N-1} →							H	
H	L	H	H	H	H	Q_{N-1} →							L	

NOTES:
X=Don't care condition
Q_{N-1}=Previous output state
L=Low voltage level/"ON" output state
H=High voltage level/"OFF" output state

ABSOLUTE MAXIMUM RATINGS

T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V
V_{IN}	Input voltage	-0.5 to +15	V
V_{OUT}	Output voltage	0 to +30	V
I_{GND}	Ground current	500	mA
I_{OUT}	Output current Each output	200	mA
P_D	Maximum power dissipation, T_A=25°C (still-air)[1] N package D package	 1712 1315	 mW mW
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec. max)	300	°C

NOTES:

1. Derate above 25°C at the following rates:
   F package at 11.1mW/°C
   N package at 13.7mW/°C
   D package at 10.5mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75V to 5.25V, 0°C ≤T_A ≤ +70°C, unless otherwise specified.[1]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					
V_{IH}	High		2.0			V
V_{IL}	Low				0.8	
	Output voltage					
V_{OL}	Low	I_{OL}=150mA, T_A=25°C		1.05	1.30	V
		Over temperature			1.50	
	Input current					
I_{IH}	High	V_{IN}=V_{CC}		<1.0	10	µA
I_{IL}	Low	V_{IN}=0V		-3.0	-250	
I_{OH}	Leakage current	V_{OUT}=28V,		5	250	µA
	Supply current					
I_{CCL}	All outputs low	V_{CC}=5.25V		35	60	mA
I_{CCH}	All outputs high			22	50	
P_D	Power dissipation	No output load			315	mW

NOTES:

1. All typical values are at V_{CC}=5V and T_A=25°C

SWITCHING CHARACTERISTICS

V_{CC}=5V, T_A=25°C, V_{OUT}=5V, I_{OUT}=100MA, V_{IL}=0.8V, V_{IH}=2.0V.

SYMBOL	PARAMETER	TO	FROM	MIN	TYP	MAX	UNIT
	Propagation delay time						
t_{PLH}	Low-to-high[1]	Output	$\overline{CE}$		900	1800	ns
t_{PHL}	High-to-low[1]				130	260	
t_{PLH}	Low-to-high[2]	Output	Data		920	1850	ns
t_{PHL}	High-to-low[2]				130	260	
t_{PLH}	Low-to-high[3]	Output	Address		900	1800	ns
t_{PHL}	High-to-low[3]				130	260	
t_{PLH}	Low-to-high[4]	Output	$\overline{CLR}$		920	1850	ns
t_{PHL}	High-to-low[4]						
Switching setup requirements							
$t_{S(H)}$	Setup time high	Chip enable	High data	40			ns
	Setup time low	Chip enable	Low data	50			
$t_{S(A)}$	Address setup time	Chip enable	Address	40			ns
$t_{H(H)}$	Hold time high	Chip enable	High data	10			ns
	Hold time low	Chip enable	Low data	10			
$t_{PW(E)}$	Chip enable pulse width[1]			40			ns

NOTES:
1. See Turn-On and Turn-Off Delays, Enable-to-Output and Enable Pulse Width timing diagram.
2. See Turn-On and Turn-Off Delays, Data-to-Output timing diagram.
3. See Turn-On and Turn-Off Delays, Address-to-Output timing diagram.
4. See Turn-Off Delay, Clear-to-Output timing diagram.
5. See Setup and Hold Time, Data-to-Enable timing diagram.
6. See Setup Time, Address-to-Enable timing diagram.

FUNCTIONAL DESCRIPTION

This peripheral driver has latched outputs which hold the input date until cleared. The NE5090 has active-Low, open-collector outputs, all of which are cleared when power is first applied. This device is identical to the NE590, except the outputs can withstand 28V.

Addressable Latch Function

Any given output can be turned on or off by presenting the address of the output to be set or cleared to the three address pins, by holding the "D" input High to turn on the selected output, or by holding it Low to turn off, holding the $\overline{CLR}$ input High, and bringing the $\overline{CE}$ input Low. Once an output is turned on or off, it will remain so until addressed again, or until all outputs are cleared by bringing the $\overline{CLR}$ input Low while holding the $\overline{CE}$ input High.

Demultiplexer Operation

By holding the $\overline{CLR}$ and $\overline{CE}$ inputs Low and the "D" input High, the addressed output will remain on and all other outputs will be off.

High Current Outputs

The obvious advantage of this device over other drivers such as the 9334 and N74LS259 is the fact that the outputs of the NE5090 are each capable of 200mA and 28V. It must be noted, however, that the total power dissipation would be over 2.5W if all 8 outputs were on together and carrying 200mA each. Since the total power dissipation is limited by the package to 1W, and since power dissipation due to supply current is 0.25W, the total load power dissipation by the device is limited to 0.75W at room temperature, and decreases as ambient temperature rises.

The maximum die junction temperature must be limited to 165°C, and the temperature rise above ambient and the junction temperature are defined as:

$$T_R=\theta_{JA}\times P_D$$
$$T_J=T_A+t_R$$

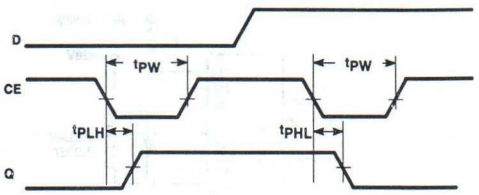
where

For example, if we are using the NE5090 in a plastic package in an application where the ambient temperature is never expected to rise above 50°C, and the output current at the 8 outputs, when on, are 100, 40, 50, 200, 15, 30, 80, and 10mA, we find from the graph of output voltage vs load current that the output voltages are expected to be about 0.92, 0.75, 0.78, 1.04, 0.5, 0.7, 0.9, and 0.4V, respectively. Total device power due to these loads is found to be 473.5mW. Adding the 200mW due to the power supply brings total device power dissipation to 723.5mW. The thermal resistances are 83°C,per W for plastic packages and 100°C per W for Cerdips. Using the equations above we find:

Plastic T_R=83×0.7235=60°C
Plastic T_J=50+60=100°C
Cerdip T_R=100×0.7235=72.4°C
Cerdip T_J=50+72.4=122.4°C

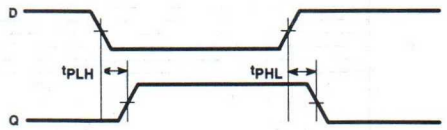
Thus we find that T_J for either package is below the 165°C maximum and either package could be used in this application. The graphs of total load power vs ambient temperature would also give us this same information, although interpreting the graphs would not yield the same accuracy.

TIMING DIAGRAMS



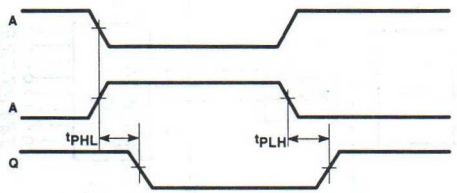
NOTE:
Other Inputs: $\overline{CLR}$ = H, A = Stable

Turn-On and Turn-Off Delays, Enable-to-Output and Enable Pulse Width



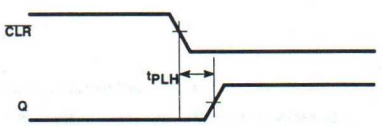
NOTE:
Other Inputs: $\overline{CE}$ = I, $\overline{CLR}$ = H, A = Stable

Turn-On and Turn-Off Delays, Data-to-Output

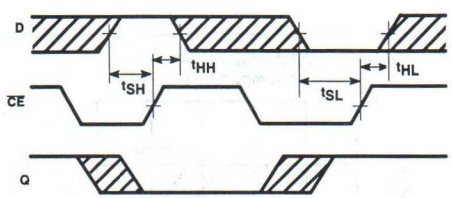


NOTE:
Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = L, D = H

Turn-On and Turn-Off Delays, Address-to-Output

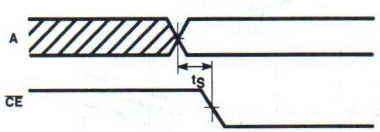


Turn-Off Delays, Clear-to-Output



NOTE:
Other Inputs: $\overline{CLR}$ = H, A = Stable

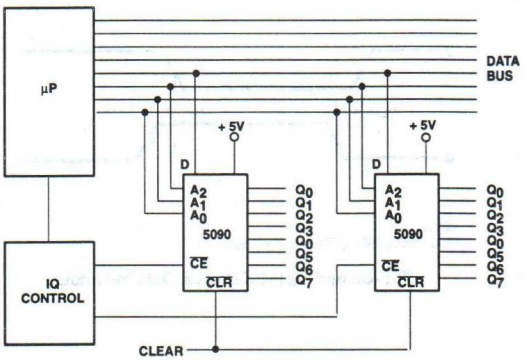
Setup and Hold Time, Data-to-Enable



NOTE:
Other Inputs: $\overline{CLR}$ = H

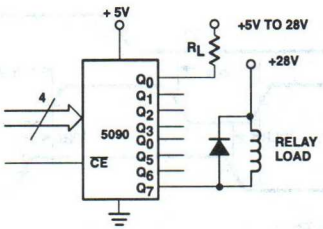
Setup Time, Address-to-Enable

TYPICAL APPLICATIONS

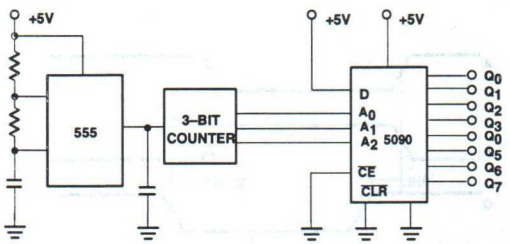


NOTE:
A_0, A_1, A_2 may be connected to the address bus if permitted by system design.

Interfacing With a Microprocessor System



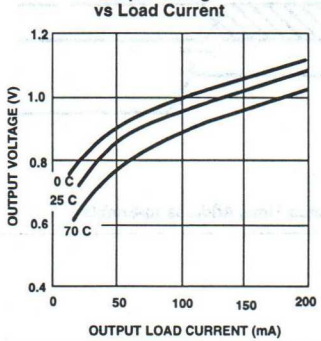
Driving Simple Loads



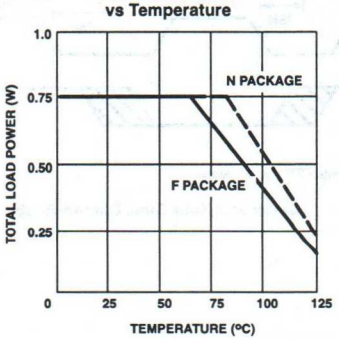
Operating in Demultiplex Mode

TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage vs Load Current



Total Load Power vs Temperature



Addressable peripheral drivers — NE590/591

DESCRIPTION

The NE590/591 addressable peripheral drivers are high current latched drivers, similar in function to the 9334 address decoder. The device has eight Darlington power outputs, each capable of 250mA load current. The outputs are turned on or off by respectively loading a logic high or logic low into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a $\overline{CE}$ input line. A common clear input, $\overline{CLR}$, turns all outputs off when a logic low is applied.

The NE590 has eight open-collector Darlington outputs which sink current to ground. The device is packaged in a 16-pin plastic or Cerdip package.

The NE591 has eight open-emitter Darlington outputs which source current to an external load from a common collector line, V_S. This V_S line need not necessarily be the same as the 5V V_{CC} supply. The device is packaged in an 18-pin plastic or Cerdip package.

FEATURES

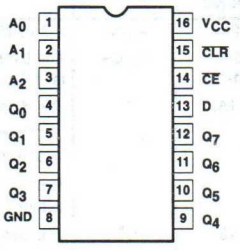
- 8 high current outputs
- Low-loading bus compatible inputs
- Power-on clear ensures safe operation
- NE590 will operate in addressable or demultiplex mode
- Allows random (addressed) data entry
- Easily expandable
- NE590 is pin compatible with 54/74LS259

APPLICATIONS

- Relay driver
- Indicator lamp driver
- Triac trigger
- LED display digit driver
- Stepper motor driver

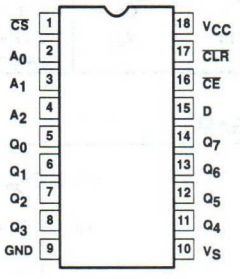
PIN CONFIGURATIONS

N Package



TOP VIEW
NE590

N Package



TOP VIEW
NE591

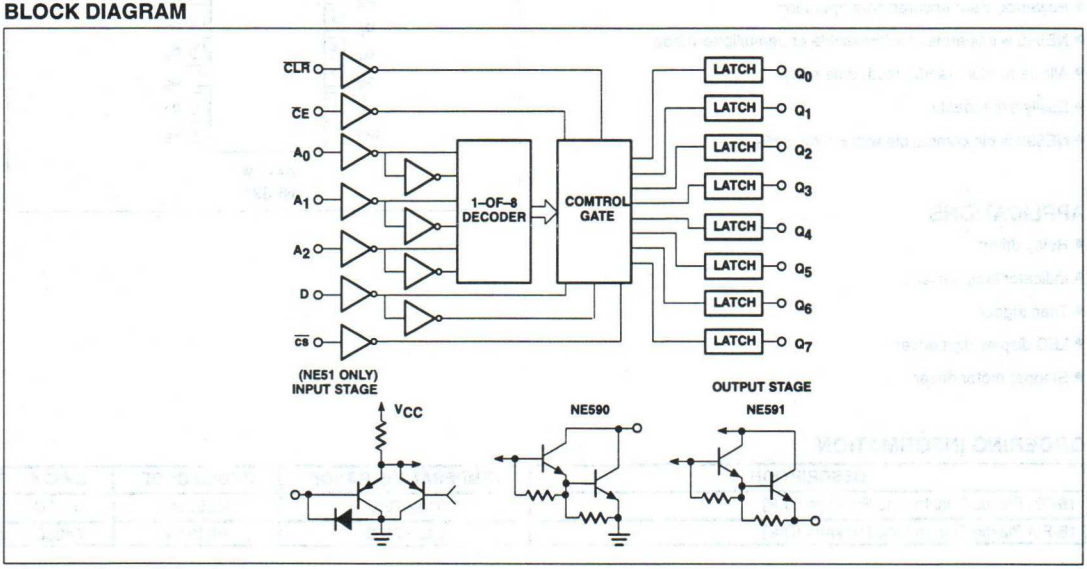
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE590N	0406C
18-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE591N	0406C

PIN DESIGNATION

590 PIN NO.	591 PIN NO.	SYMBOL	NAME & FUNCTION
1-3	2-4	A_0-A_2	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	5-8, 11-14	Q_0-Q_7	The 8 device outputs. The NE590 has open-collector Darlington outputs. The NE591 has open emitter-follower outputs.
13	15	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF" Thus in logic terms, the NE590 inverts data to the relevant output. The NE591 retains true data at the output.
14	16	$\overline{CE}$	The chip enable. When this input is low, the output latches will accept data. When $\overline{CE}$ goes high, all outputs will retain their existing state regardless of address or data input conditions.
15	17	$\overline{CLR}$	The clear input. When $\overline{CLR}$ goes low all output switches are turned "OFF". On the NE590, a high data input will override the clear function on the addressed latch. On the NE591, $\overline{CLR}$ low will override any other condition.
-	1	$\overline{CS}$	The chip select input provides for an additional level of address decoding.
-	10	V_S	The V_S line provides the power to all 8 output devices. It is connected to the collectors of all 8 output transistors. This pin may be connected to the V_{CC} or another supply.

BLOCK DIAGRAM



TRUTH TABLE (NE590)

INPUTS						OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	L	L	L	L	L	H	Q_{N-1} →							
H	L	H	L	L	L	L	Q_{N-1} →							
H	L	L	H	L	L	Q_{N-1}	H	Q_{N-1} →						Addressable Latch
H	L	H	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	L	H	H	H	Q_{N-1} →							H	
H	L	H	H	H	H	Q_{N-1} →							L	

NOTES:
X=Don't care condition
Q_{N-1}=Previous output state
L=Low voltage level/"OFF" output state
H=High voltage level/"ON" output state

TRUTH TABLE (NE591)

INPUTS							OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	$\overline{CS}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	X	X	X	X	X	X	L	L	L	L	L	L	L	L	Clear
H	H	H	X	X	X	X	Q_{N-1} →								
H	H	L	X	X	X	X	Q_{N-1} →								Memory
H	L	H	X	X	X	X	Q_{N-1} →								
H	L	L	L	L	L	L	L	Q_{N-1} →							
H	L	L	H	L	L	L	H	Q_{N-1} →							
H	L	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						Addressable Latch
H	L	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	L	L	H	H	H	Q_{N-1} →							L	
H	L	L	H	H	H	H	Q_{N-1} →							H	

NOTES:
X=Don't care condition
Q_{N-1}=Previous output state
L=Low voltage level/"OFF" output state
H=High voltage level/"ON" output state

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V
V_{IN}	Input voltage	-0.5 to +15	V
V_{OUT}	Output voltage		V
	NE590	0 to +7	
	NE591	0 to V_{CC}	
V_S	Source bus voltage NE591 only	-0.5 to +7	V
V_S-V_{CC}	Source/supply differential voltage NE591 only	-5 to +2	V
I_{OUT}	Output current		
	Each output	300	mA
	All outputs	1000	
P_D	Maximum power dissipation T_A=25°C (still air)		
	NE590[1] N package	1450	mW
	NE591[2] N package	1690	
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature	165	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec max)	300	°C

NOTES:
1. Derate above 25°C at the following rates: N package at 11.6mW/°C
2. Derate above 25°C at the following rates: N package at 13.5mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{CC}=4.75 to 5.25V, 0°C ≥ T_A ≤ 70°C unless otherwise specified. [1,2]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					
V_{IH}	High		2.0			V
V_{IL}	Low				0.8	
	Output voltage					
V_{OL}	Low (NE590 only)	I_{OL}=250mA, T_A=25°C		1.0	1.3	
		Over temperature			1.5	V
V_{OH}	High (NE591 only)	I_{OH}=-250mA, V_{CC}=V_S=5V	2.9			
	Input current					
I_{IH}	High	V_{IN}=V_{CC}		0.1	10	
I_{IL}	Low	V_{IN}=0V				
	$\overline{CE}$ input			-25	-60	µA
	All other inputs			-15	-50	
I_{OH}	Leakage current	V_{OUT}=5.25V		10	250	µA
	Supply current[3]	V_S=V_{CC}=5V				
I_{CCL}	All outputs low					
	NE590			33	50	
	NE591			15	50	
I_{CCH}	All outputs high					mA
	NE590			15	50	
	NE591			30	50	
P_D	Power dissipation	No output load			350	mW

NOTES:
1. All typical values are at V_{CC}=5V and T_A=25°C
2. For the NE591 V_S=V_{CC} in all tests.
3. Supply current for the NE591 is measured with no output load.

SWITCHING CHARACTERISTICS

V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TO	FROM	NE590			NE591			UNIT
				Min	Typ	Max	Min	Typ	Max	
	Propagation delay time									
t_{PLH}	Low-to-High[1]	Output	$\overline{CE}$		65	150		50	80	ns
t_{PHL}	High-to-Low[1]				115	230		70	120	
t_{PLH}	Low-to-High[2]	Output	Data		65	130		45	70	ns
t_{PHL}	High-to-Low[2]				120	240		65	100	
t_{PLH}	Low-to-High[3]	Output	Address		100	200		45	80	ns
t_{PHL}	High-to-Low[3]				130	260		75	140	
t_{PLH}	Low-to-High[4]	Output	$\overline{CLR}$		65	130				ns
t_{PHL}	High-to-Low[4]							45	140	
t_{PLH}	Low-to-High[1]	Output	$\overline{CS}$					40	80	ns
t_{PHL}	High-to-Low[1]							70	120	
Switching setup requirements										
$t_{S(H)}$		Chip enable	High data	210			100			ns
$t_{S(L)}$		Chip enable	Low data	210			100			ns
$t_{S(A)}$		Chip enable	Address	30			30			ns
$t_{H(H)}$		Chip enable	High data	40			10			ns
$t_{H(L)}$		Chip enable	Low data	30			10			ns
$t_{S(CS)}$		Chip enable	Low chip select				100			ns
$t_{PW(E)}$	Chip enable pulse width[1]			120			120			ns

NOTES:
1. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
2. See Turn-On and Turn-Off Delays, Data to Output timing diagram.
3. See Turn-On and Turn-Off Delays, Address to Output timing diagram.
4. See Turn-Off Delay, Clear to Output timing diagram.
5. See Setup and Hold Time, Data to Enable timing diagram.
6. See Setup Time, Address to Enable timing diagram.

FUNCTIONAL DESCRIPTION

These peripheral drivers have latched outputs which hold the input data until cleared. The NE590 has active-Low, open-collector outputs, while the NE591 has active-High, uncommitted (open) emitter outputs. All outputs are cleared when power is first applied.

Addressable Latch Function

Any given output can be turned on or off by presenting the address of the output to be set or cleared to the three address pins, by holding the "D" input High to turn on the selected input, or by holding it Low to turn off, holding the $\overline{CLR}$ input High, and bringing the $\overline{CE}$ input Low. Once an output is turned on or off, it will remain so until addressed again, or until all outputs are cleared by bringing the $\overline{CLR}$, $\overline{CE}$, and "D" inputs Low. For NE591, $\overline{CS}$ must be brought Low any time CE is Low if any outputs are to be changed.

Demultiplexer Operation

By bringing the $\overline{CLR}$ and $\overline{CE}$ inputs Low and the "D" input High, the addressed output will remain on and all other outputs will be off. This condition will remain only as long as the output is addressed. For the NE591, the $\overline{CS}$ input must also be Low.

High Current Outputs

The obvious advantage of these devices over the 9334 and N74LS259 (which provide a similar function) is the fact that the NE590 and NE591 are capable of output currents of 250mA at each of their eight outputs. It should be noted, however, that the load power dissipation would be over 2.5W if all 8 outputs were to carry their full rated load current at one time. Since the total power dissipation is limited by the package to 1W, and since the power dissipation due to supply current is 0.25W, the total load power dissipation by the device is limited to 0.75W, and decreases as ambient temperature rises.

The maximum die junction temperature must be limited to 165°C, and the temperature rise above ambient and the junction temperature are defined as:

$$t_R = \theta_{JA} \times P$$
$$t_J = t_A + t_R$$

where

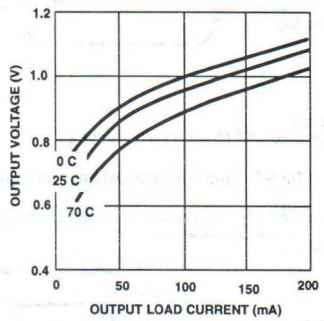
θ_{JA} is die junction to ambient thermal resistance.
P_D is total power dissipation
t_R is junction temperature rise above ambient
t_j is die junction temperature
t_A is ambient (surrounding medium) temperature

For example, if we are using the NE590 in a plastic package in an application where the ambient temperature is never expected to rise above 50°C, and the output current at the 8 outputs, when on, are 100, 40, 50, 200, 15, 30, 80, and 10mA, we find from the graph of output voltage vs load current that the output voltages are expected to be about 0.92, 0.75, 0.78, 1.04, 0.5, 0.7, 0.9, and 0.4V, respectively. Total device power due to these loads is found to be 473.5mW. Adding the 250mW due to the power supply brings total device power dissipation to 723.5mW. The thermal resistances are 83°C per W for plastic packages and 100°C per W for Cerdips. Using the equations above we find:

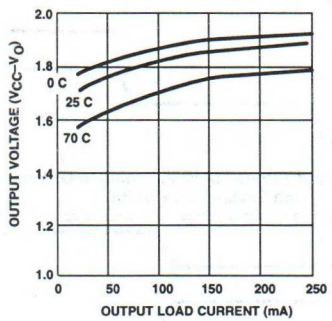
Plastic t_R=83x0.7235=60°C
Plastic t_J=50+60=100°C
Cerdip t_R=100x0.7235=72.40°C
Cerdip t_J=50+72.4=122.4°C

Thus we find that t_J for either package is below the 165°C maximum and either package could be used in this application. The graphs of total load power vs ambient temperature would also give us this same information, although interpreting the graphs would not yield the same accuracy.

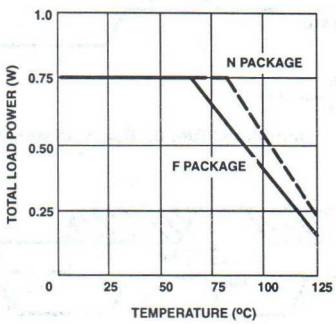
TYPICAL PERFORMANCE CHARACTERISTICS



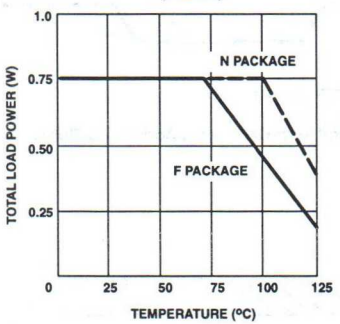
Output Voltage vs Load Current (NE590)



Output Voltage Drop vs Load Current (NE591)

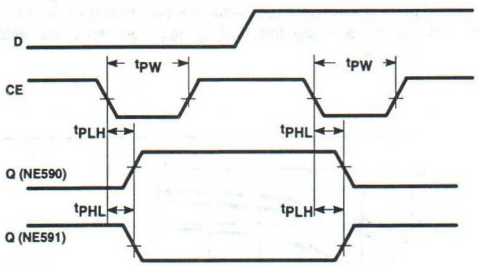


Total Load Power vs Temperature (NE590)



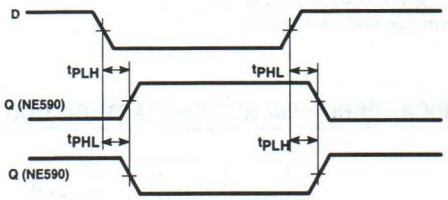
Total Load Power vs Temperature (NE591)

TIMING DIAGRAMS



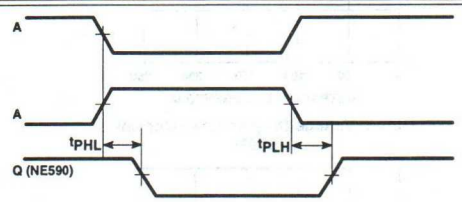
NOTE:
Other inputs $\overline{CLR}$ = H, $\overline{CS}$ = L, A = Stable

Turn-On and Turn-Off Delays, Enable-to-Output and Enable Pulse Width



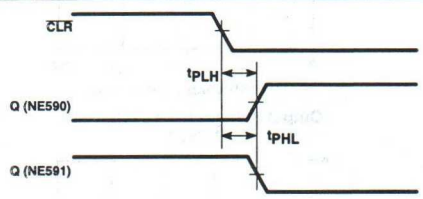
NOTE:
Other inputs $\overline{CE}$ $\overline{CS}$ = L, $\overline{CLR}$ = H, A = Stable

Turn-On and Turn-Off Delays, Data-to-Output



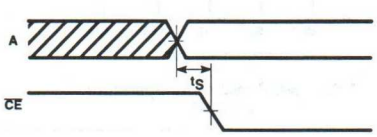
NOTE:
Other inputs $\overline{CE}$ = L, $\overline{CLR}$ = L, D = H

Turn-On and Turn-Off Delays, Address-to-Output



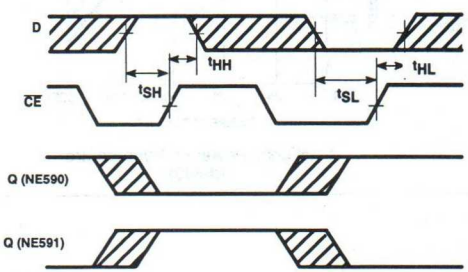
NOTE:
Other inputs $\overline{CS}$ = H, $\overline{CE}$ = H

Turn-On and Turn-Off Delays, Clear-to-Output



NOTE:
Other inputs $\overline{CLR}$ = H, CS = L

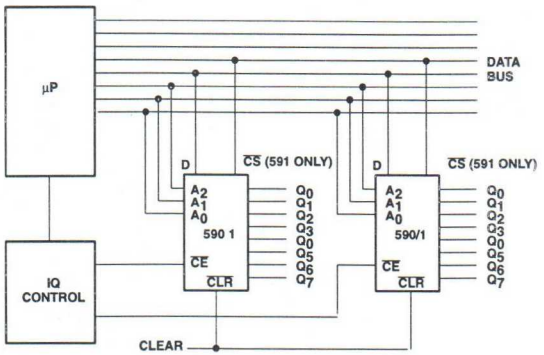
Set-Up Time, Address-to-Enable



NOTE:
Other inputs $\overline{CLR}$ = H, $\overline{CS}$ = L, A = Stable

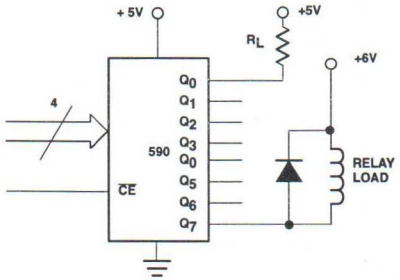
Set-Up and Hold Time, Data-to-Enable

TYPICAL APPLICATIONS

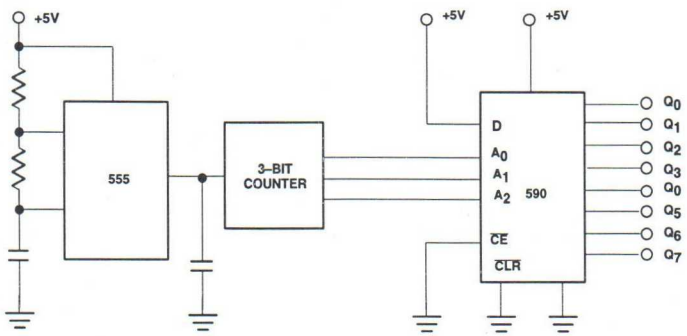


NOTE:
A_0, A_1, A_2, and $\overline{CS}$ may be connected to the address bus if permitted by system design.

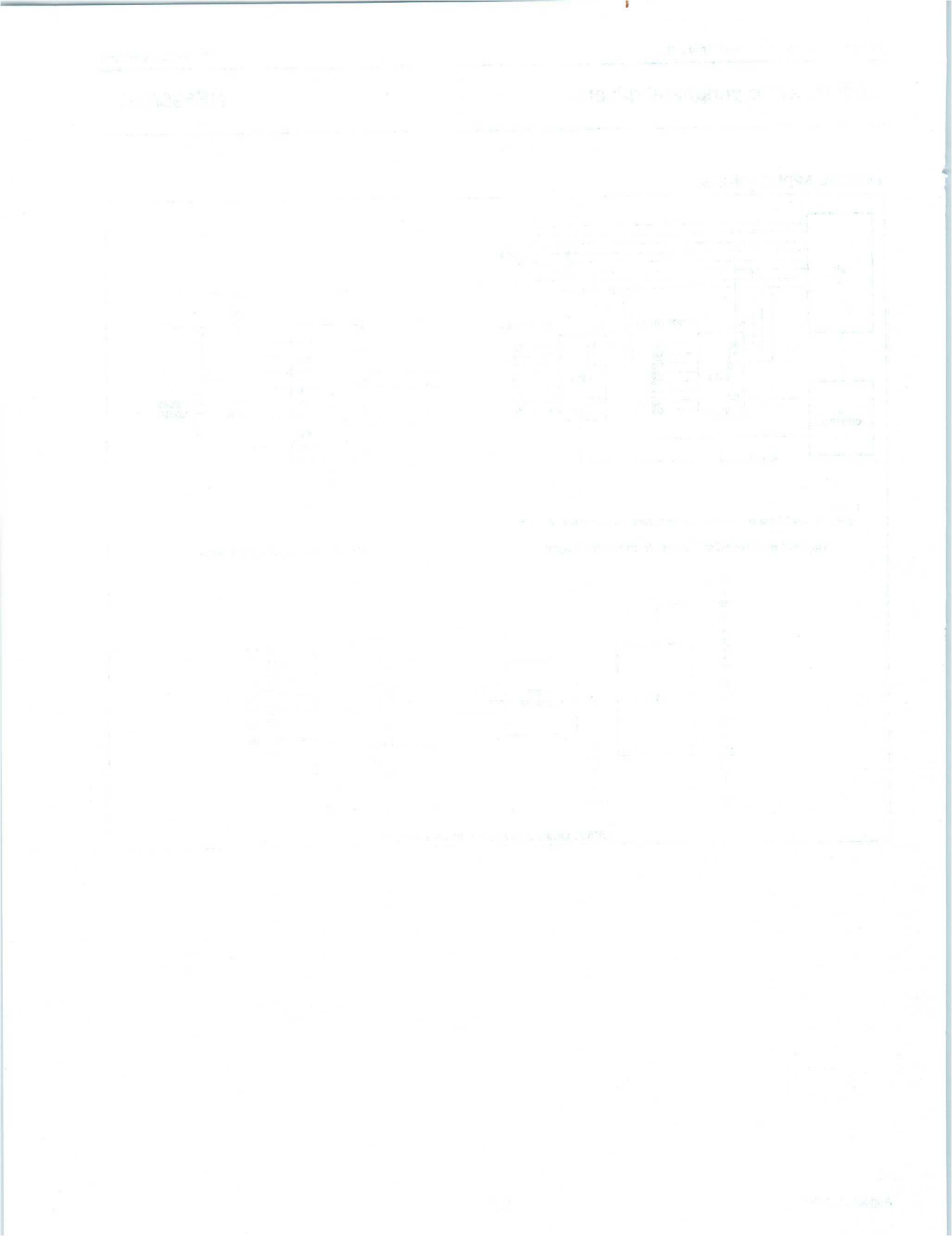
Turn-On and Turn-Off Delays, Address-to-Output



NE590 Driving Simple Loads



NE590 Operating in Demultiplex Mode



Section 9
Display Drivers

INDEX

NE587	LED decoder/driver	531
NE/SA594	Vacuum fluorescent display driver	540
AN112	LED decoder drivers: using the NE587	546

LED decoder/driver — NE587

DESCRIPTION

The NE587 is a latch/decoder/driver for 7-segment common anode LED displays. The NE587 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and $\overline{LE}$ (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

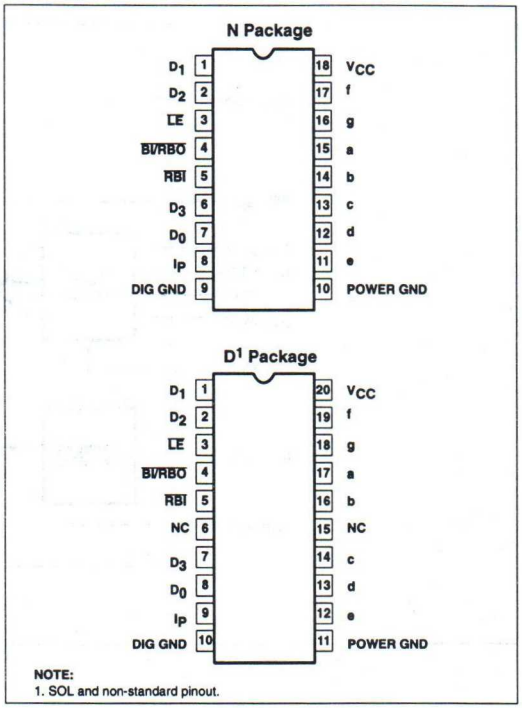
FEATURES

- Latched BCD inputs
- Low loading bus-compatible inputs
- Ripple-blanking on leading- and/or trailing-edge zeros

APPLICATIONS

- Digital panel motors
- Measuring instruments
- Test equipment
- Digital clocks
- Digital bus monitoring

PIN CONFIGURATIONS



NOTE:
1. SOL and non-standard pinout.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) Package	0 to +70°C	NE587D[1]	0172D
18-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE587N	0407A

NOTES:
1. SOL and non-standard pinout

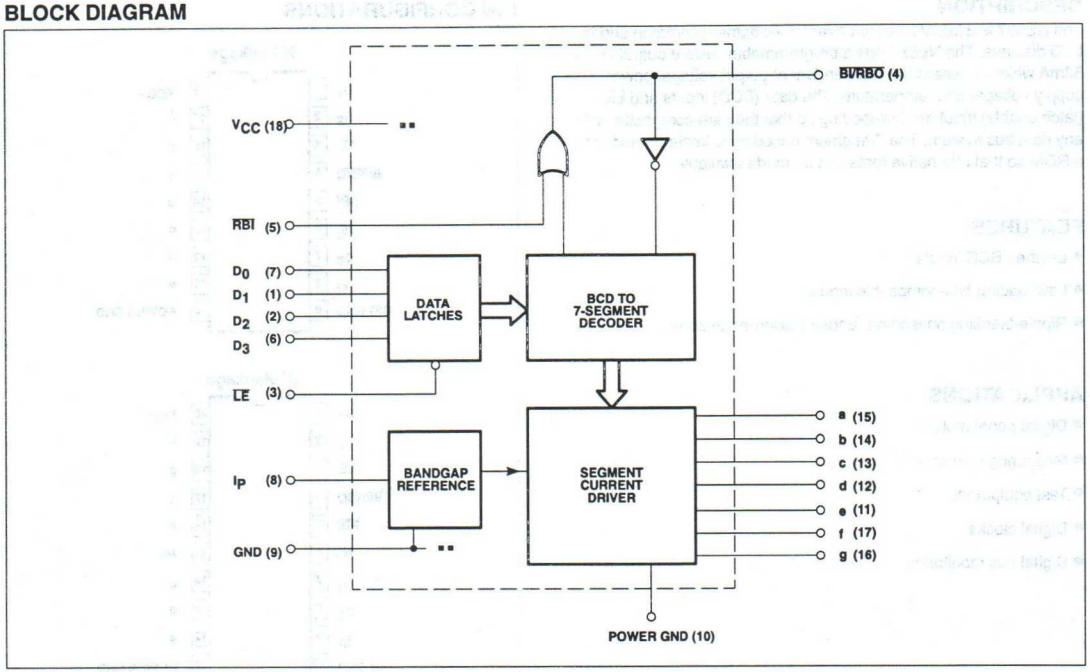
ABSOLUTE MAXIMUM RATINGS

T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V
V_{IN}	Input voltage (D_0-D_3, $\overline{LE}$, $\overline{RBI}$)	-0.5 to +15	V
V_{OUT}	Output voltage (a-g, RBO)	-0.5 to +7	V
P_D	Power dissipation (25°C)[1]	1000	mW
T_A	Ambient temperature range	0 to 70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Soldering temperature (10sec max)	300	°C

NOTES:
1. Derate power dissipation as indicated
   N package—95°C/W above 55°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC}=4.75 to 5.25V, 0°C < T_A < 70°C. Typical values are at V_{CC}=5V, T_A=25°C, R_P=1kΩ (±1%), unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage		4.75	5.00	5.25	V
V_{IH}	Input high voltage	All inputs except $\overline{BI}$	2.0		15	V
		$\overline{BI}$	2.0		5.5	
V_{IL}	Input low voltage				0.8	V
V_{IC}	Input clamp voltage	I_{IN}=-12mA, T_A=25°C			-1.5	V
I_{IH}	Input high current	Inputs D_0-D_3, $\overline{LE}$, $\overline{RBI}$				µA
		V_{IN}=2.4V		1.0	10	
		V_{IN}=15V		15	15	
		Input $\overline{BI}$ (Pin 4)		10	100	µA
		$\overline{RBI}$=H				
		V_{IN}=V_{CC}=5.25V				
I_{IL}	Input low current	V_{IN}=0.4V, Inputs D_0-D_3		-5		
		$\overline{LE}$, $\overline{RBI}$		-200		µA
		input $\overline{BI}$				
		V_{CC}=5.25V		-0.7		mA
		$\overline{RBI}$=H, V_{IN}=0.4V				
V_{OL}	Output low voltage	Output $\overline{RBO}$		0.2	0.5	V
		I_{OUT}=3.0mA				
V_{OH}	Output high voltage	Output $\overline{RBO}$				
		I_{OUT}=-50µA	3.5	4.5		V
		$\overline{RBI}$=H				
I_{OUT}	Output segment "ON" current	Outputs "a" through "g"	20	25	30	mA
		V_{OUT}=2.0V				
ΔI_{OUT}	Output current ratio (all outputs ON)	With reference to "b" segment	0.90	1.00	1.10	
		V_{OUT}=2.0V				
I_{OFF}	Output segment "OFF" current	Outputs "a" through "g"				
		V_{OUT}=5.0V		20	250	µA
I_{CCO}	Supply current	V_{CC}=5.25V				
		All outputs "ON"		33	55	mA
		V_{OUT}>1V				
I_{CCI}	Supply current	V_{CC}=5.25V				
		All outputs blanked		50	70	mA

NOTES:

NE587 Programming:

The NE587 output current can be programmed, provided a program resistor, R_P, be connected between I_P (Pin 8) and Ground (Pin 9). The voltage at I_P (Pin 8) is constant (≈1.3V). Thus, a current through R_P is $I_P \approx 1.3V/R_P$, as shown in Figure 5. I_O/I_P is 20 in the 15 to 50mA output current range.

AC ELECTRICAL CHARACTERISTICS

V_{CC}=5V, T_A=25°C, R_L=130Ω, C_L=30pF including probe capacity.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_{DAV}	Propagation delay (Figure 2)	From data to output		135		ns
t_{DAV}	Propagation delay (Figure 3)	From $\overline{LE}$ to output		135		ns
t_W	Latch enable pulse width (Figure 4)		30			ns
t_S	Latch enable setup time (Figure 4)	From data to $\overline{LE}$	20			ns
t_H	Latch enable hold time (Figure 4)	From $\overline{LE}$ to data	0			ns

NOTES:
t_{DAV}= (t_{HL}+t_{LH})

TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	$\overline{RBO}$	
-	H	*	X	X	X	X	STABLE							**	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	1
2	L	X	L	L	H	L	L	L	H	L	L	H	L	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4
5	L	X	L	H	L	H	L	H	L	L	H	L	L	H	5
6	L	X	L	H	H	L	L	H	L	L	L	L	L	H	6
7	L	X	L	H	H	H	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	8
9	L	X	H	L	L	H	L	L	L	L	H	L	L	H	9
10	L	X	H	L	H	L	H	H	H	H	H	H	L	H	-
11	L	X	H	L	H	H	L	H	H	L	L	L	L	H	E
12	L	X	H	H	L	L	H	L	L	H	L	L	L	H	H
13	L	X	H	H	L	H	H	H	H	L	L	L	H	H	L
14	L	X	H	H	H	L	L	L	H	H	L	L	L	H	P
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	Blank
**BI	X	X	X	X	X	X	H	H	H	H	H	H	H	L**	Blank

NOTES:
H=HIGH voltage level, output is "OFF"
L=LOW voltage level, output is "ON"
X=Don't care
* The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.
** $\overline{RBO}$/$\overline{BI}$ used as an input overrides all other input conditions.

NE587 PROGRAMMING

587 output current can be programmed by using a programming resistor, RP, connected between RP (Pin 8) and GND (Pin 9). The voltage at RP (Pin 8) is constant (K = 1.3V). A partial schematic of the voltage reference used in the NE587 is shown in Figure 1.

Output current to program current ratio, I_O/I_P, is 20 in the 15mA to 50mA range. Note that I_P must be derived from a resistor (R_P), and not from a high-impedance source such as an I_{OUT} DAC used to control display brightness.

POWER DISSIPATION CONSIDERATIONS

LED displays are power-hungry devices, and inevitably, somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDs are not driven too far into saturation; but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

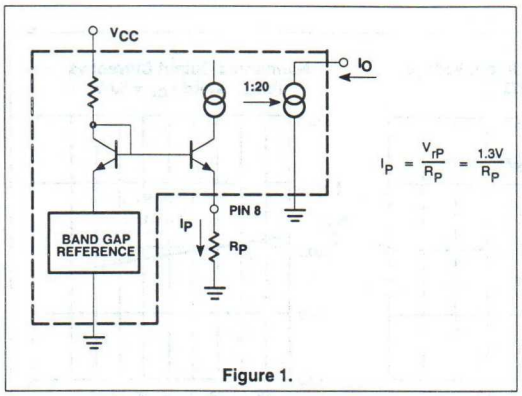


Figure 1.

TIMING DIAGRAMS

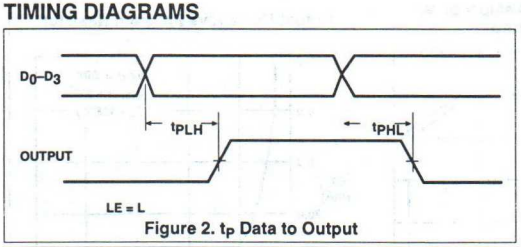


Figure 2. t_P Data to Output

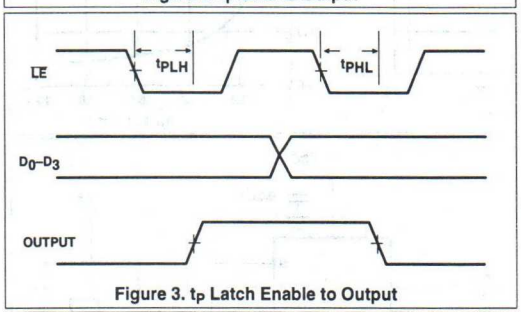
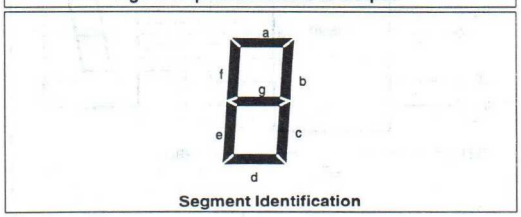


Figure 3. t_P Latch Enable to Output



Segment Identification

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large-size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant-current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible, consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation may be calculated as follows. Referring to Figure 6, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

V_{CC}	Supply voltage to driver
V_S	Supply voltage to display
I_{CC}	Quiescent supply current of driver
I_{SEG}	LED segment current
V_F	LED segment forward voltage at I_{SEG}
K_{DC}	% Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

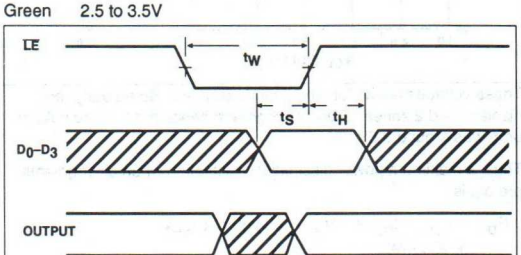
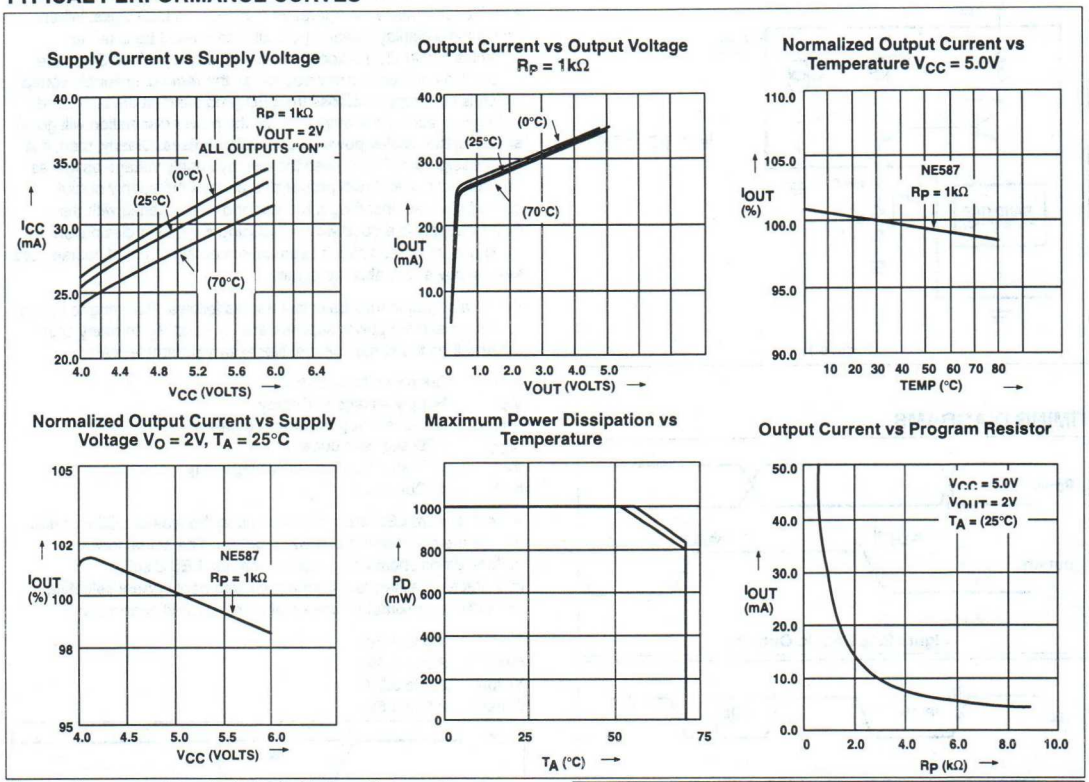


Figure 4. Setup and Hold Times

TYPICAL PERFORMANCE CURVES



These voltages are all for single-diode displays. Some early red displays had 2 series LEDs per segment; hence the forward voltage drop was around 3.5V.

Thus, a maximum power dissipation calculation when all segments are on, is:

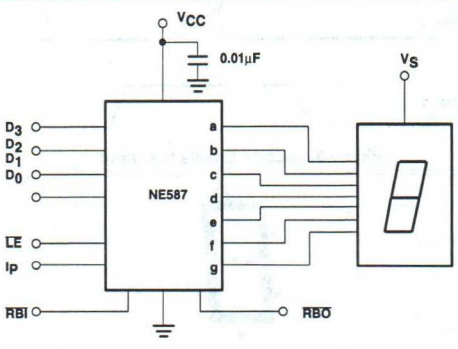
$$P_D = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{SEG} \times K_{DC} mW$$

Assuming $V_S = V_{CC} = 5.25V$
$V_F = 2.0V$
$K_{DC} = 100\%$

$P_{D\,MAX} = 5.25 \times 50 + 3.25 \times 7 \times 30mW = 945mW$
However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$P_{D\,MAX} = 5.0 \times 30 + 3.00 \times 5 \times 25mW = 525mW$

Operating temperature range limitations can be deduced from the power dissipation graph. (See Typical Performance Characteristics.)



NOTE:
Decoupling capacitor on V_{CC} should be 0.01µF ceramic.

Figure 5. Driving a Single Digit

However, a major portion of this power dissipation ($P_{D\ MAX}$) is because the current source output is operating with 3.25V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst-case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{SEG}} \approx 10\Omega \ (\tfrac{1}{2}W \text{ rating})$$

assuming worst case I_{SEG} of 30mA.

Hence now

$$P_{D\ MAX} = V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{SEG}) \times 7 \times I_{SEG} \times K_{DC}$$
$$= 5.25 \times 50 + 1.25 \times 7 \times 30mW$$
$$= 525mW$$

and

$$P_{D\ av} = 5.0 \times 30 + 1.25 \times 5 \times 25 = 306\ mW.$$

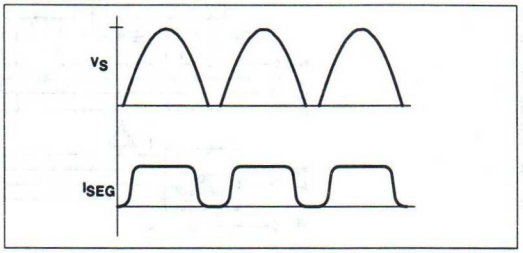
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$V_S - V_F - nV_d$, $V_D \approx 0.8V$

Where n is the number of diodes used, power dissipation can be calculated in a similar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in Figure 9. For example a Darlington PNP or NPN emitter-follower may be preferable. Figure 8 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact, a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about $3\text{-}4.5V_{RMS}$ works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With
$V_S = 4.9V$ peak
$V_F = 2.0V$

The duty cycle is approximately 60%.

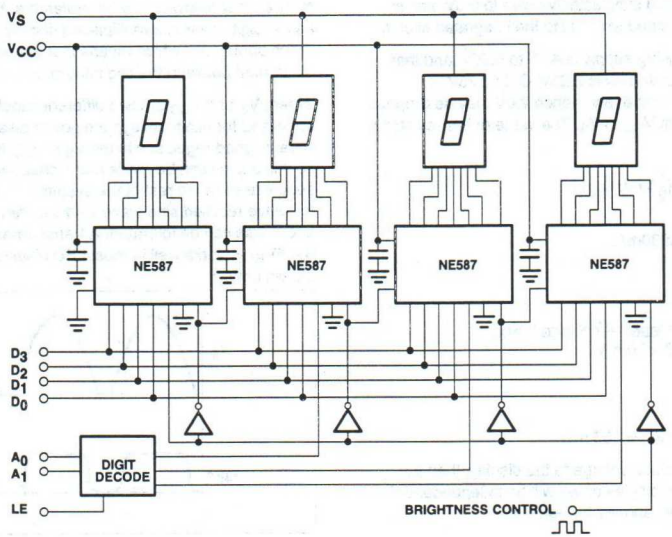


Figure 6. 4-Digit Display with Brightness Control and Leading-Edge Ripple Blanking

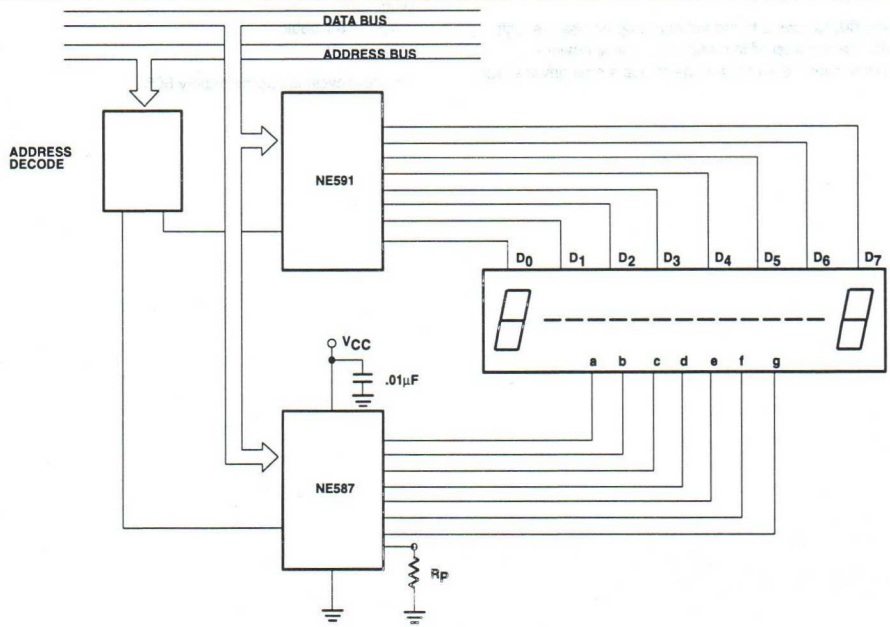


Figure 7. Interfacing 8-Digit LED Display with µP Bus

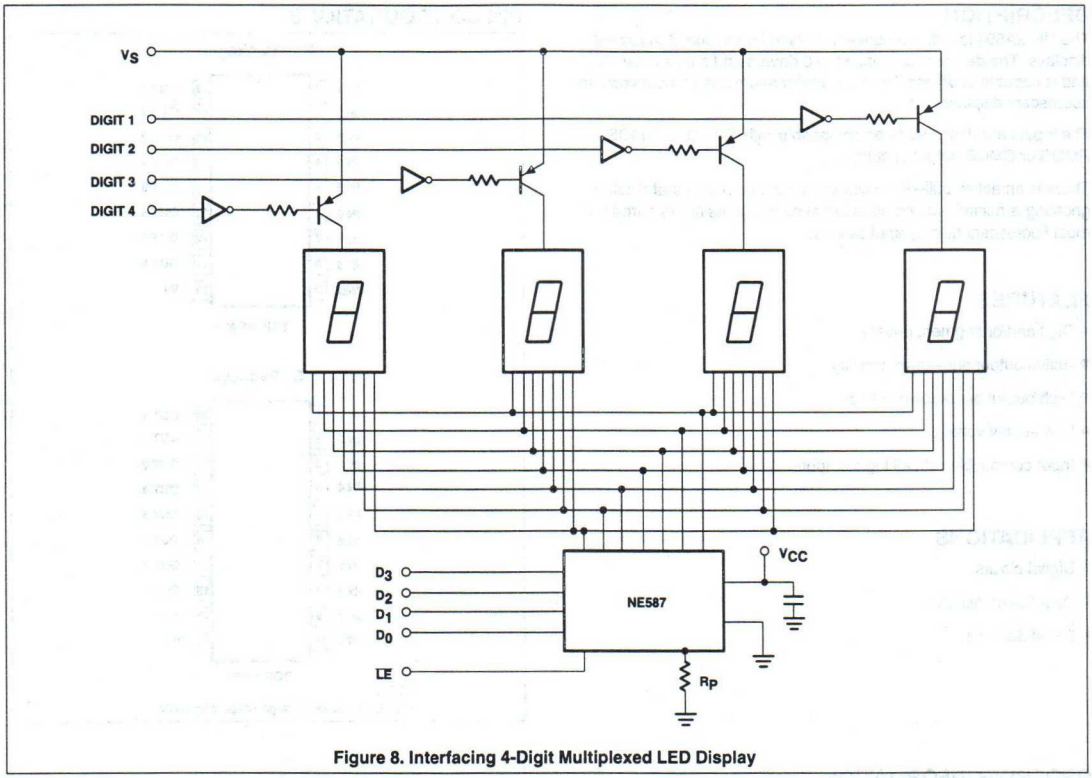


Figure 8. Interfacing 4-Digit Multiplexed LED Display

Vacuum fluorescent display driver — NE/SA594

DESCRIPTION

The NE/SA594 is a display driver interface for vacuum fluorescent displays. The device is comprised of 8 drivers and a bias network, and is capable of driving the digits and/or segments of most vacuum fluorescent displays.

The inputs are designed to be compatible with TTL, DTL, NMOS, PMOS or CMOS output circuitry.

There is an active pull–down circuit on each output so that display ghosting is minimized and no external components are required for most fluorescent display applications.

FEATURES

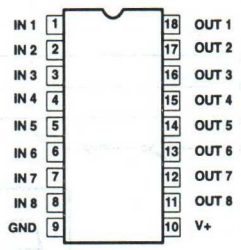
- Digit and/or segment drivers
- Active output pull–down circuitry
- High output breakdown voltage
- Low supply voltage
- Input compatible with all logic outputs

APPLICATIONS

- Digital clocks
- Dashboard displays
- Panel displays

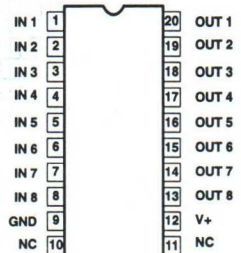
PIN CONFIGURATIONS

N, F Packages



TOP VIEW

D[1] Package



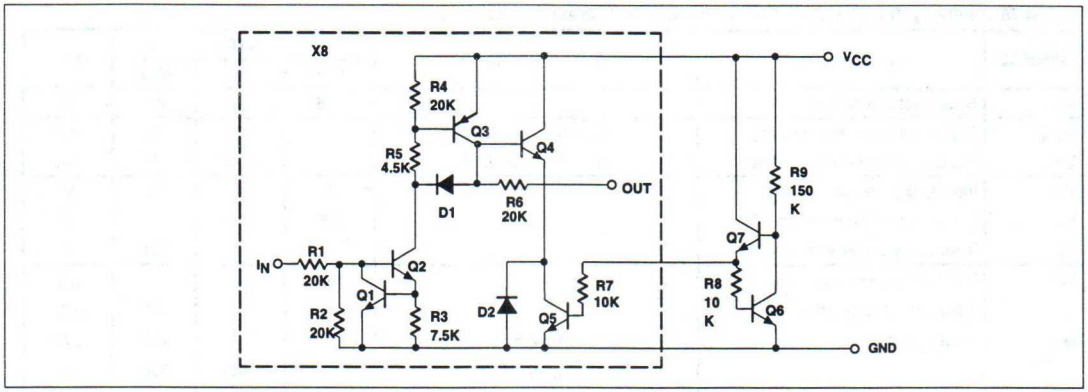
TOP VIEW

NOTE:
1. SOL – Released in large SO package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
18–Pin Plastic DIP	0 to +70°C	NE594N	0407A
18–Pin Ceramic DIP	0 to +70°C	NE594F	0583A
20–Pin Plastic SO	0 to +70°C	NE594D	0408B
18–Pin Plastic DIP	–40°C to +85°C	SA594N	0407A
18–Pin Ceramic DIP	–40°C to +85°C	SA594F	0583A
20–Pin Plastic SO	–40°C to +85°C	SA594D	0408B

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (at 25°C, unless otherwise noted)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	45	V
V_{OUT}	Output voltage	V_{CC}	
V_{IN}	Input voltage	–0.3, +20	V
I_{OUT}	Output current		
	Each output	50	mA
	All outputs	200	mA
P_D	Maximum power dissipation, T_A=25°C (still–air)[1]		
	F package	1500	mW
	N package	1690	mW
	D package	1390	mW
T_A	Operating ambient temperature range		
	NE594	0 to 70	°C
	SA594	–40 to +85	°C
T_{STG}	Storage temperature range	+65 to +150	°C
T_J	Maximum junction temperature	–150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. Derate above 25°C, at the following rates:
   F package at 12.0mW/°C
   N package at 13.5mW/°C
   D package at 11.1mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{CC}=+4.75 to +40V, T_A=0 to 70°C (NE), T_A= –40 to +85°C (SA), unless otherwise stated.

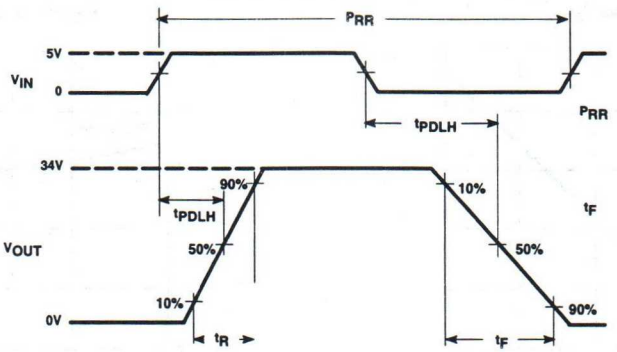
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Min	Typ	Max	
V_{CC}	Supply voltage range			4.75	35	40	V
I_{CCH}	Supply current (all outputs high)	V_{CC}=40V, V_{IN}=3.5V			3	6	mA
I_{CCL}	Supply current (all outputs low)	V_{CC}=40V, V_{IN}=0.4V			0.4	1	mA
V_{IN}	Input voltage range			0		15	V
V_{IH}	Input voltage to ensure logic "1'			2.6			V
V_{IL}	Input voltage to ensure logic "0'					0.8	V
I_{IH}	Input current to ensure logic "1'			100			µA
I_{IL}	Input current to ensure logic "0'					10	µA
I_{IN}	Input current	V_{IN}=2.6V			60	130	µA
		V_{IN}=5.0V			180	330	µA
		V_{IN}=15.0V			.68	1.3	mA
V_{OH}	Output high voltage	V_{IN}=3.5V, I_{OUT}=–25mA	T_A=25°C	V_{CC} –1.5	V_{CC} –1.1		V
			Over temp.	V_{CC} –2	V_{CC} –1.3		V
		V_{OUT} with respect to V_{CC}					
V_{OH}	Output high, no load voltage	V_{IN}=3.5V, I_{OUT}=0, T_A=25°C, V_{OUT} with respect to V_{CC}		V_{CC} –1	V_{CC} –0.8		V
V_{OFF}	Output 'OFF' voltage level	V_{IN}=0.8V, I_{OUT}=0			10	200	mV
I_{OH}	Available output current	V_{CC}=35V, V_{IN}=3.5V, V_{OUT}=30V, T_A=25°C		–35			mA
I_{OUT}	Output pull-down current	V_{CC}=V_{OUT}=35V, Inputs open		100	200	400	µA
I_{CEX}	Output leakage current	T_A=25°C, V_{IN}=0.4V V_{CC}=40V, V_{OUT}=0V			–1 –1		µA

AC ELECTRICAL CHARACTERISTICS

V_{CC}=35V, T_A=25°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_{PLH}	Propagation delay—low–to–high output transition	50% V_{IN} to 50% V_{OUT}		1	5	µs
t_{PHL}	Propagation delay—high–to–low output transition	50% V_{IN} to 50% V_{OUT}		3	10	µs
t_R	Output rise time	10% V_{OUT} to 90% V_{OUT}		0.5	3	µs
t_F	Output fall time	90% V_{OUT} to 10% V_{OUT}		1.5	5	µs

SWITCHING TIMES OF DRIVERS



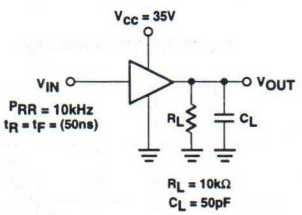
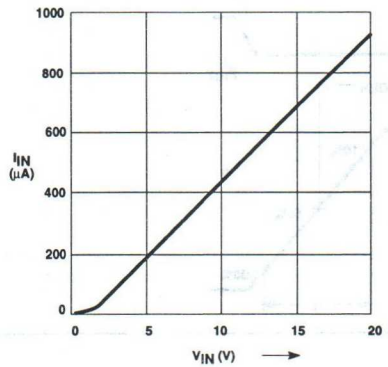


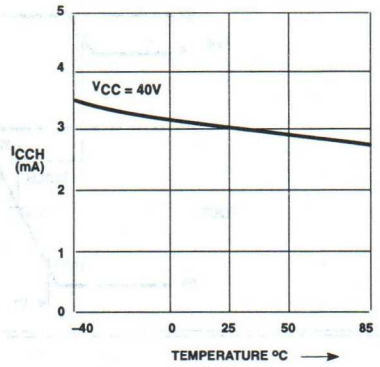
Figure 1. Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

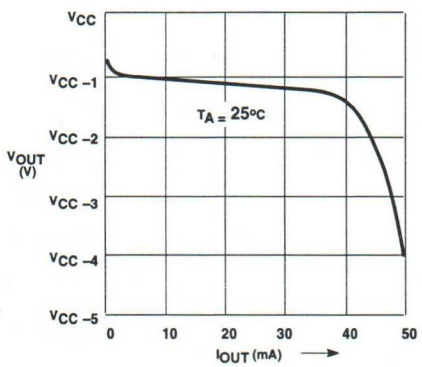
I_{IN} vs V_{IN}



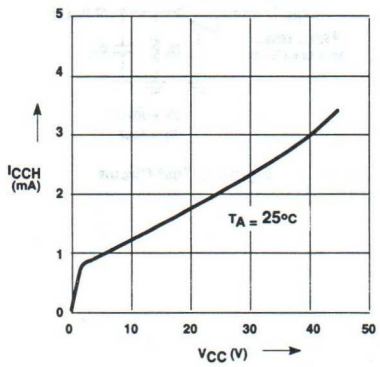
I_{CCH} vs Temperature



Output Voltage vs Output Current



I_{CC} vs V_{CC} (All inputs High)



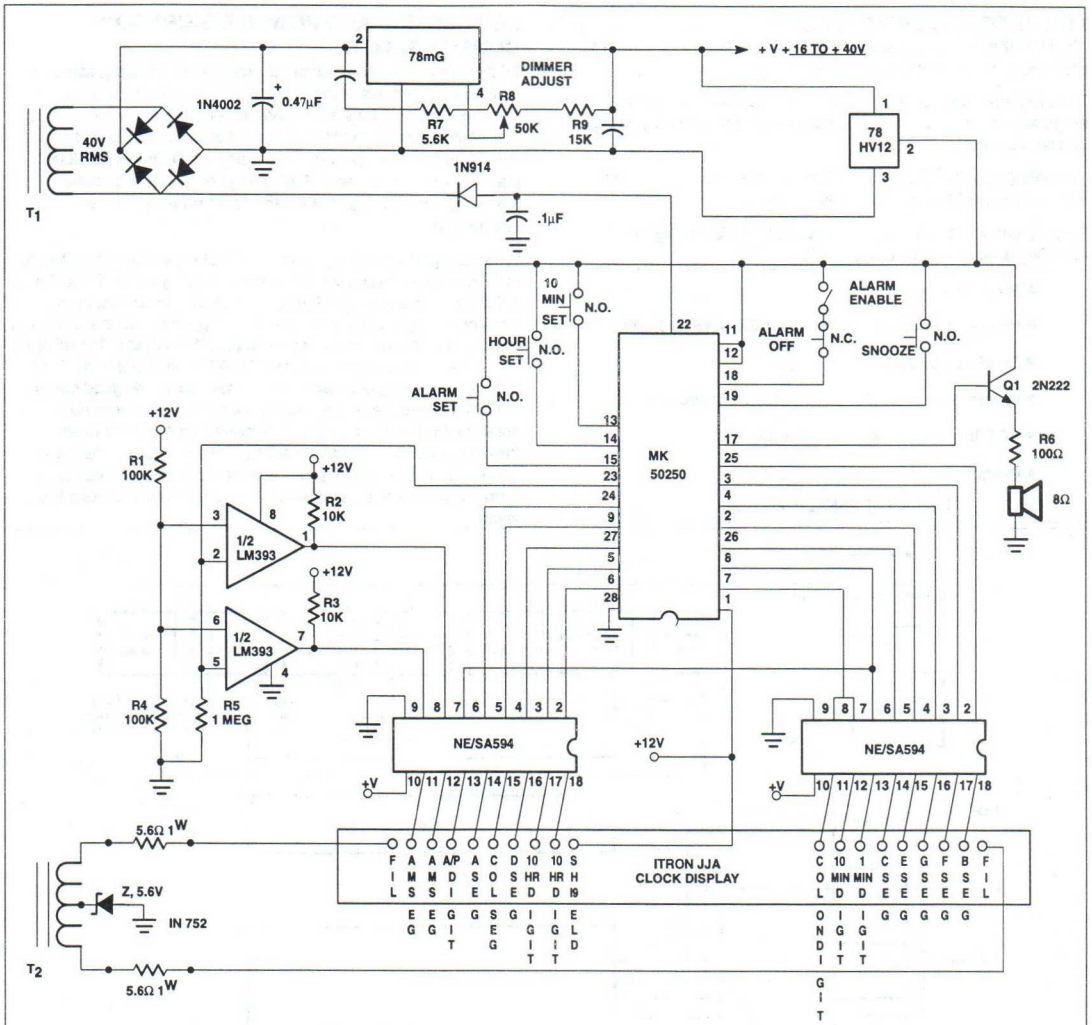


Figure 2. Typical Application: Digital Clock With Alarm

LED decoder drivers: using the NE587

AN112

LED DECODER DRIVER NE587

The NE587 is latchable decoder drivers for LED displays. Figure 1 provides a summary of their features.

The programmable constant-current supplies (fixed or adjustable) are essentially independent of output voltage, power supply voltage, and temperature.

The data (BCD) and $\overline{LE}$ (latch enable) inputs are low loading and thus are compatible with a data bus system.

Figure 2 shows a block diagram of the NE587. Seven-segment decoding is implemented using a ROM.

- **Strobed latch**
- **Inputs compatible with NMOS, CMOS, DMOS, TTL**
- **Single 5V supply**
- **Inputs are compatible with microprocessor bus**
- **BCD inputs — hexadecimal outputs**
- **Programmable seqment current**

Figure 1. NE587 LED Driver

LED DRIVERS AND POWER DISSIPATION CONSIDERATION

LED displays are power hungry devices, and, inevitably, somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDs are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the NE587 output is a constant programmed current source, all the remaining supply voltage which is not dropped across the LED (and the digit driver, if used) will appear across the output of the NE587. Thus, the power dissipation in the NE587 will go up sharply if the display power supply voltage rises. Clearly then, it is good design practice to keep the display supply voltage as low as possible, consistent with proper operation of the output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, total system power remains the same.

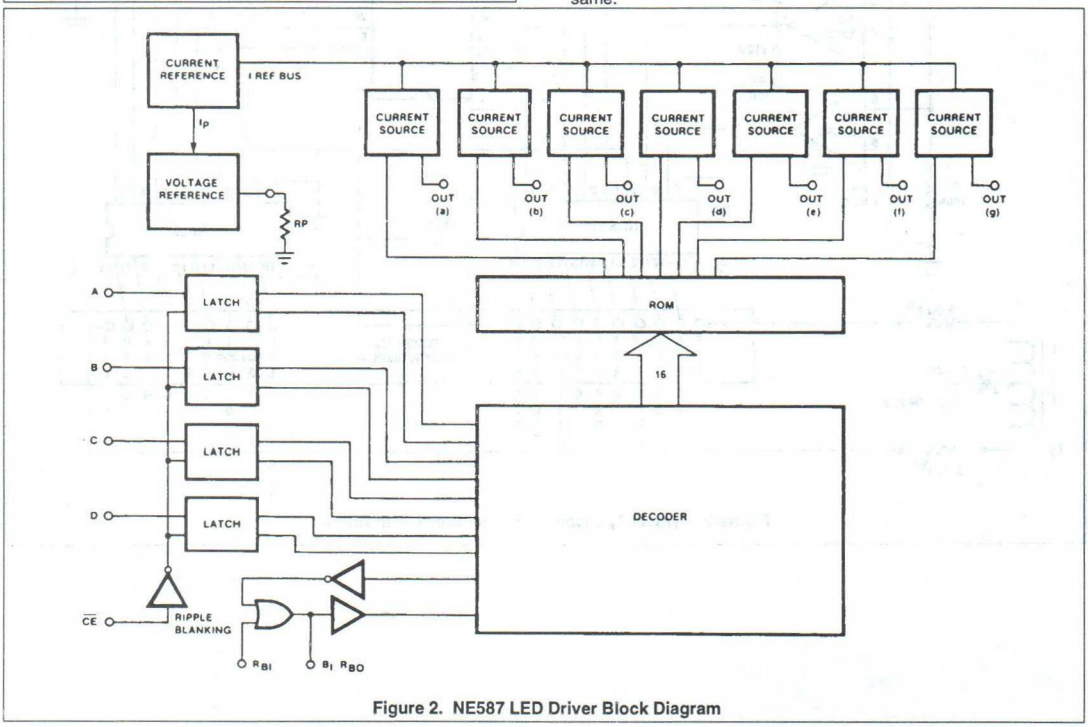


Figure 2. NE587 LED Driver Block Diagram

LED decoder drivers: using the NE587 AN112

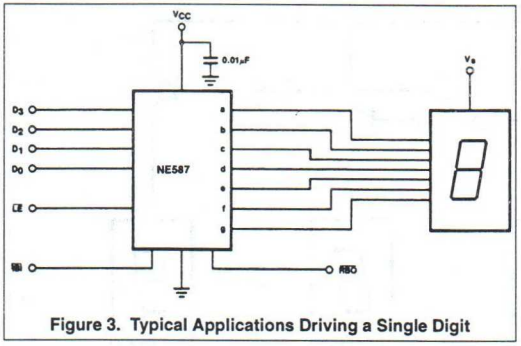


Figure 3. Typical Applications Driving a Single Digit

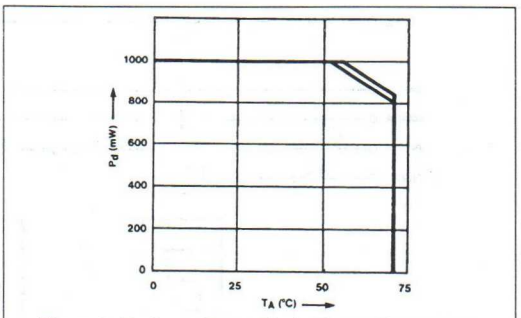


Figure 4. Maximum Power Dissipation vs Temperature

Power dissipation within the NE587 may be calculated as follows. Referring to Figure 3, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

- **V_{CC} Supply voltage to driver**
- **V_S Supply voltage to display**
- **I_{CC} Quiescent supply current of driver**
- **I_{SEG} LED segment current**
- **VFLED segment forward voltage at I_{SEG}**
- **K_{DC} % Duty cycle**

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected. However, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

These voltages are all for single diode displays. Some early red displays had 2 series LEDs per segment, hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation when all segments are on, is:

$$P_D = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{SEG} \times K_{DC} \text{ mW} \quad (1)$$

Assuming $V_S = V_{CC} = 5.25V$
$V_F = 2.0V$
$K_{DC} = 100\%$
$I_{SEG} = 30mA$

$$P_{D\,MAX} = 5.25 \times 50 + 3.25 \times 7 \times 30mW = 945mW$$

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{D\,AV} = 5.0 \times 30 + 3.00 \times 5 \times 25mW = 525mW$$

Operating temperature range limitations can be deduced from the power dissipation graph in Figure 4.

However, a major portion of this power dissipation ($P_{D\,MAX}$) is because the current source output is operating with 3.25V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst-case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_F for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by using equation 2.

$$R_S = \frac{V_{DROP}}{I_{SEG} \text{ x \# of SEG}} \quad (2)$$

or

$$R_S = \frac{2.0}{7 \text{ x } I_{SEG}} \approx 10\Omega(1/2W \text{ rating})$$

assuming worst-case I_{SEG} of 30mA, now:

$$PD_{MAX} = V_{CC} \text{ x } I_{CC} + (V_S - V_V - R_X \text{ x } 7 \text{ x } I_{SEG}) \text{ x } 7 \text{ x } I_{SEG} \text{ x } K_{DC} \quad (3)$$
$$= 5.25 \text{ x } 50 + 1.25 \text{ x } 7 \text{ x } 30mW$$
$$= 525mW$$

and $P_{D\,AV} = 5.0 \times 30 + 1.25 \times 5 \times 25 = 306mW$

If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$$V_S - V_F - nV_D, \quad V_D \approx 0.8V$$

Where n is the number of diodes used, and so power dissipation can be calculated in a similar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in Figure 5. For example, a Darlington PNP or NPN emitter-follower may be preferable. Figure 6 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V, which means that the power dissipation is evenly distributed between the two integrated circuits.

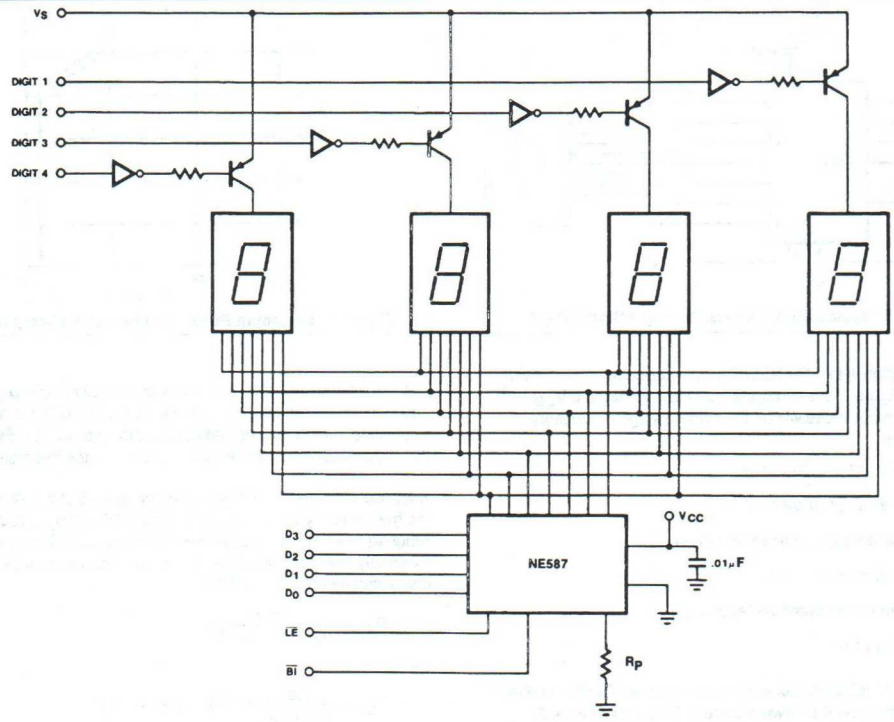


Figure 5. 4-Digit Multiplexed LED Display

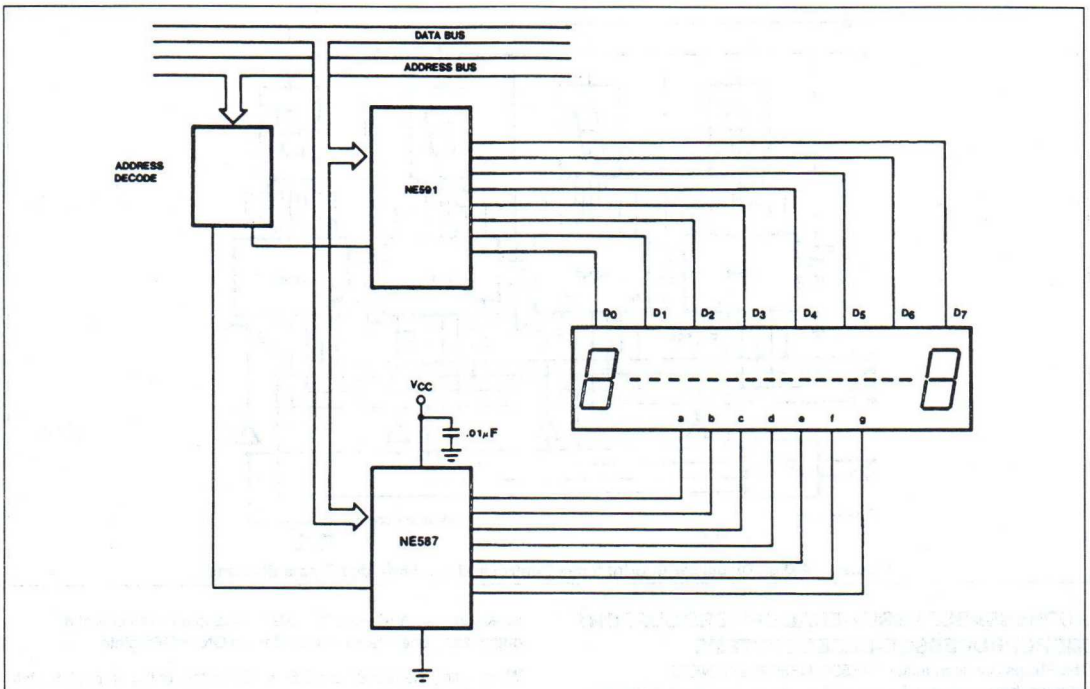


Figure 6. Interfacing 8-Digit LED Display With Microprocessor Bus

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact, a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4.5V_{RMS} works well in most LED display systems. Waveforms are shown in Figure 7.

The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With V_S=4.9V peak
V_F = 2.0V

The duty cycle is approximately 60%.

V_S in this example was derived by the circuit shown in Figure 7. Remember that the forward voltage drop of the rectifying diode must be subtracted to arrive at the exact peak of the V_S voltage.

Figure 8 shows other typical application schemes for multiplexing LED displays.

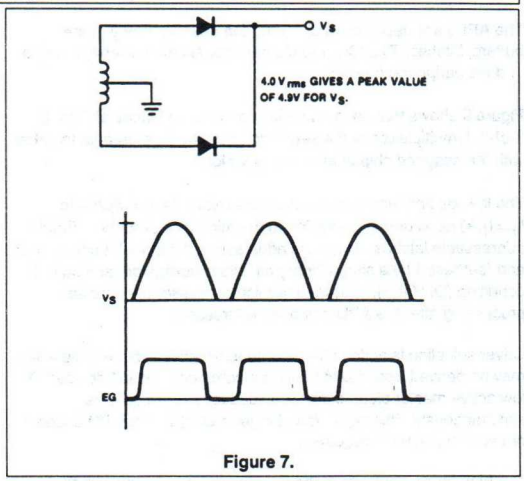


Figure 7.

LED decoder drivers: using the NE587

AN112

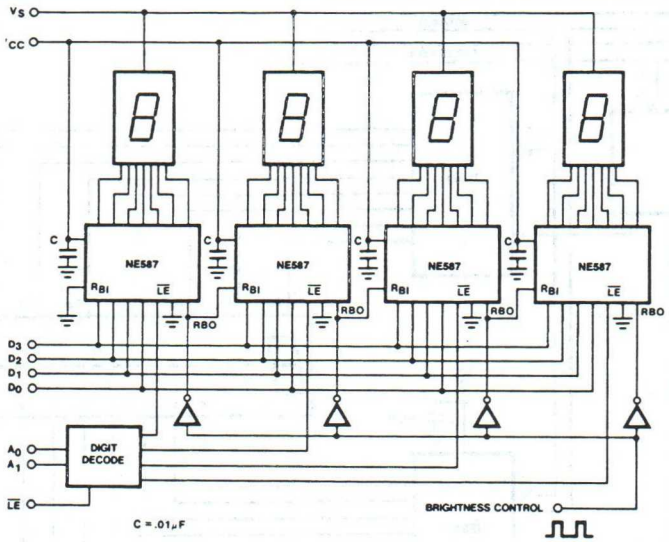


Figure 8. 4-Digit Display With Brightness Control and Leading-Edge Ripple Blanking

ADDRESSABLE PERIPHERAL DRIVERS SUPPORT MICROPROCESSOR-BASED SYSTEMS

The Philips Semiconductors NE590, NE5090 and NE591 addressable peripheral drivers (APDs) greatly facilitate interfacing a variety of support circuits to microprocessor-based systems.

The APDs are designed to eliminate the need for many of the buffers, latches, TTL ICs, and discrete transistors currently needed to drive peripheral devices.

Figure 9 shows that each driver includes a set of input latches, a 1-of-8 demultiplexer, and a set of high current drive outputs together with the assorted chip enable and clear logic.

The low loading inputs of these drivers (typically I_{IL}=15μA and I_{IH}=1μA) allow direct interfacing to the microprocessor bus. Eight addressable latches, which are addressed by a three bit binary code and (set/reset) by a single binary bit, allow storage of each output condition (ON/OFF), allowing the microprocessor to continue processing after the APD has been addressed.

Driver selection is accomplished with a low active chip enable which may be derived from the I/O decoder common to all I/O devices. A low active master clear is also provided to reset all outputs simultaneously. This signal may be generated from the I/O decoder or set high when not required.

The high current outputs of the drivers (250mA sinking with the NE590, 150mA sinking with the NE5090 and 250mA sourcing with the NE591) allow direct interfacing to relays, motors, lamps, LEDs, and other devices or systems requiring high current drive capabilities.

Figure 10 demonstrates the use of APDs in a microprocessor-based system. When driving LED displays, a single 8-bit word contains all the data required for defining both digit location and segment selection. The APD uses four bits—three to address one of 8 outputs and one to set the output to an ON or OFF state.

When using the NE590 or NE5090, ON refers to the output low state in which the output is capable of sinking a maximum of 250mA for the NE590, or 150mA for the NE5090. The clear ($\overline{CL}$) pin may be tied high and would normally not be required in this application.

The four remaining data bits are required by the NE587 which supplies segment data. These four BCD data bits are converted into seven-segment data used for driving the anodes of the LEDs. Data is strobed into the latches by the LATCH ENABLE INPUT at the same time that information is being supplied to the NE590. Since the NE587 provides a constant-current sink, uniform brightness is obtained from each segment in the display. The NE587 is capable of supplying up to 50mA/segment. Segment currents are set by a single programming resistor.

Figure 10 shows several devices connected to the NE591: a relay, a motor, and a D-C subsystem. Each device is selected in the same manner as the LED digits; that is, three bits are used to select the output and one bit is used to turn the output ON or OFF.

An output may be cleared in one of two ways:

1) By direct selection and clearing of the individual latch,

or

2) By clearing all outputs through the use of the clear input.

The latter method does not require addressing.

The examples shown in Figure 10 clearly demonstrate the advantages that can be derived from using the NE590 and NE591 APDs in microprocessor-based systems. These devices provide easy interfacing and minimize the number of interfacing components; they also provide the logic interface to the microprocessor and the switch function and high current drive required by the peripheral units.

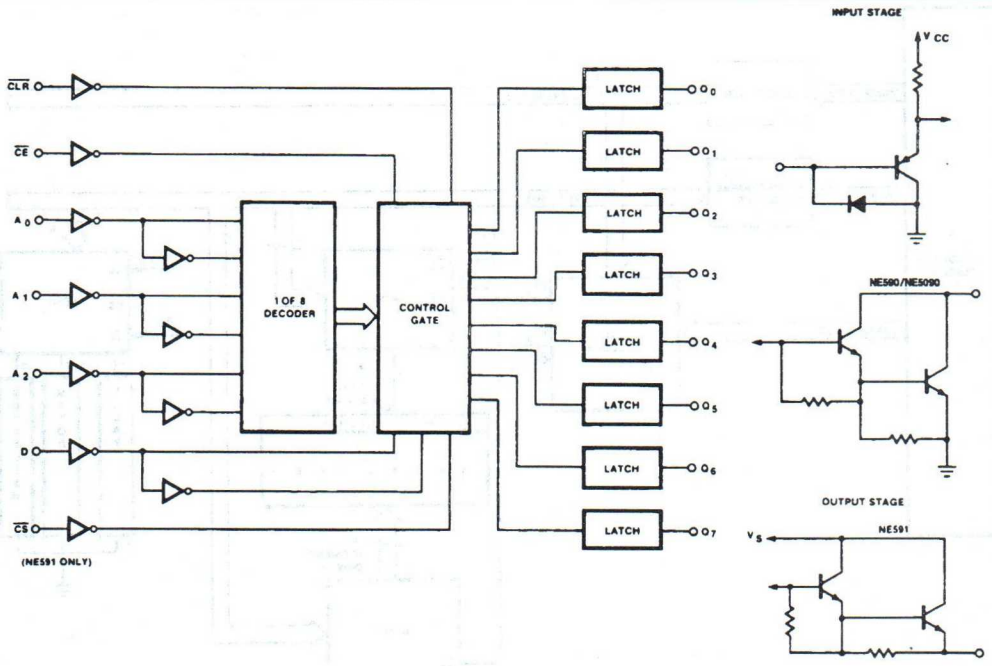


Figure 9. NE590/591/5090 Block Diagram

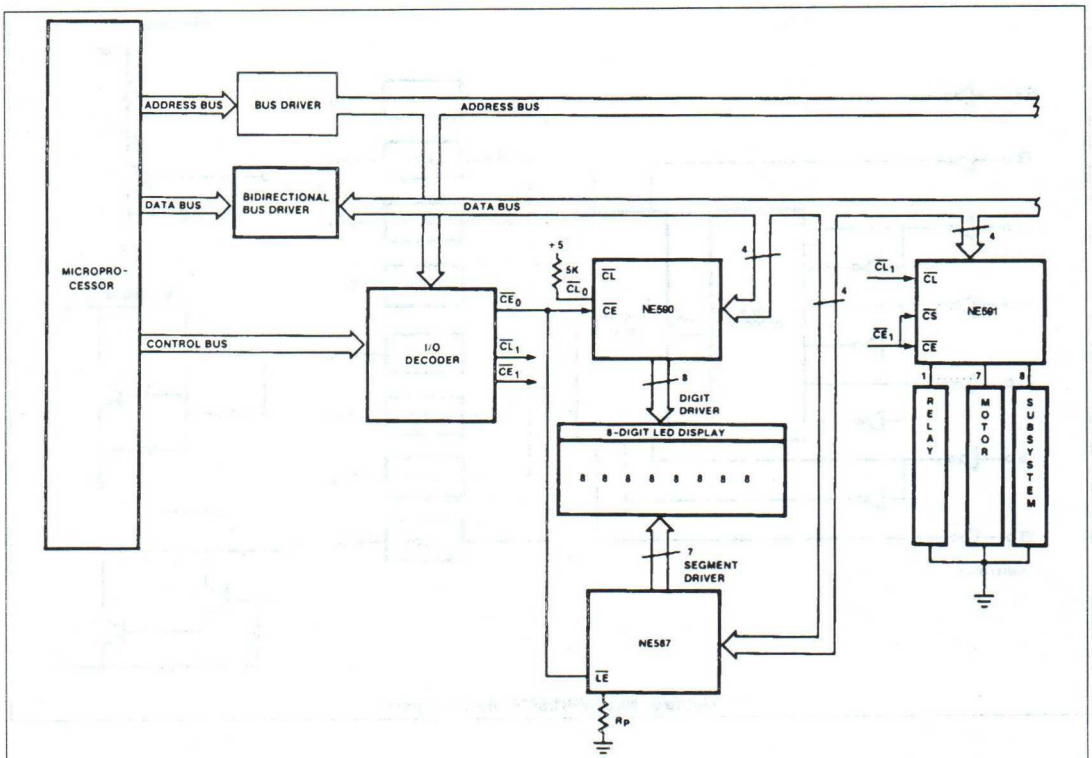


Figure 10. Microprocessor-Based System

Section 10
Analog-to-Digital Converters

INDEX

Symbols and definitions for analog-to-digital converters (ADCs)		554
ADC0803/4-1	CMOS 8-bit A/D converters	555
ADC0820	8-Bit, high-speed, µP-compatible A/D converter with track/hold function	568
NE5037	6-Bit A/D converter (parallel outputs)	582
PCF8591	8-Bit A/D and D/A converter	590
TDA8703	8-bit high-speed analog-to-digital converter	607
TDA8706	6-Bit analog-to-digital converter with multiplexer and clamp	620
TDA1534	14-bit analog-to-digital converter	630
TDA8708A	Video analog input interface	637
TDA8709A	Video analog input interface	654
TDA8713	8-bit high-speed analog-to-digital converter	673
TDA8715	8-bit high-speed analog-to-digital converter	686
TDE8715D	8-bit high-speed analog-to-digital converter (Mil. temp.)	696

Symbols and definitions for analog-to-digital converters (ADCs)

General Purpose/Linear ICs

Absolute Accuracy Error

Absolute Accuracy Error at a given output code is the difference between the theoretical analog input voltage required to produce a given output code and the actual analog input voltage required to produce the same code. Since the same output code is produced by a finite band of input voltages, the "analog input voltage required" is defined as the midpoint of the band of input voltages that will produce that code..

Absolute accuracy error includes gain error, offset error and relative accuracy error and is typically expressed in LSBs or in percent of full-scale range (FSR).

Conversion Time

Conversion Time is the time required for a conversion cycle to be completed while meeting the specification.

Differential Linearity Error

Differential Linearity Error of an ADC is the in the analog value of code width between adjacent digital codes over the full range of digital output values.

Full-Scale Range (FSR)

The Full-Scale Range (FSR) of an ADC is the scale factor that determines the nominal conversion relationship; e.g., 2.5V span for a full-scale change in a fixed reference converter.

In a unipolar ADC of n bits, the ideal first code transition occurs at FSR x 2^{-N} x 1/2 and the final code transition occurs at FSR x (1–2^{-N} x 3/2). The ideal code transition from code C-1 to C occurs at FSR x (C–1/2) x $1/2^{N}$.

In a bipolar ADC, the ideal first code transition occurs at FSR x (2^{N}–1) x 1/2 and the final code transition occurs at FSR x (1–3 x 2^{-N}) x 1/2.

Gain Error

Gain Error is the deviation between the ideal and actual analog input voltage to cause the final code transition to a full-scale output code after nulling offset error. It is usually expressed in LSBs or in percent of FSR.

Integral Non-Linearity

Same as Relative Accuracy.

Least Significant Bit

The Least Significant Bit (LSB) is the lowest-order bit and carries the smallest weight. In an n-bit ADC, the weight of the LSB is FSR/(2^{N}–1). It is the smallest change that can be resolved by an n-bit ADC.

Missing Code

A missing code is a code combination that does not appear at the ADC's output.

Most Significant Bit

The Most Significant Bit (MSB) is the highest order bit and carries the most weight. The weight of the MSB is 1/2 the full-scale range of the ADC.

Offset Error (Unipolar and Bipolar)

In an ADC, unipolar offset is the difference between the actual analog input voltage that causes the first code transition point and the ideal value to cause the first code transition, which is 1/2 LSB above analog ground. Similarly for bipolar offset, it is the difference between the actual analog input voltage that causes the code transition from 1 LSB below half-scale to half-scale and the ideal analog value to cause the same code transition which is 1/2 LSB above Analog Ground

Power Supply Sensitivity

The Power Supply Sensitivity of an ADC is the change in the code transition points with changes in the DC power supply voltages. It is usually expressed in LSBs/V or in %FSR/V.

Quantization Error

ADCs of any resolution exhibit an inherent quantization uncertainty of ±1/2 LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be eliminated.

Relative Accuracy

Relative Accuracy Error is the deviation of the ADCs actual code transition points from the ideal code transition points on a straight line which connects the ideal first code transition point and the final code transition point, after nulling the offset error and gain error. It is generally expressed in LSBs or in percent of FSR.

Resolution

Resolution of an ADC is the number of bits at its output. The number of output states is 2^{N} where N is the resolution of the converter.

Temperature Coefficients

In general, Temperature Coefficients are expressed either in ppm/°C or in LSBs/°C or as a change in the specified parameter over the temperature range. Measurements are usually made at room temperature and at the temperature extremes of the specified temperature range; the Temperature Coefficient is defined as the change in the parameter from its room temperature value divided by the corresponding temperature change.

CMOS 8-bit A/D converters — ADC0803/4-1

DESCRIPTION

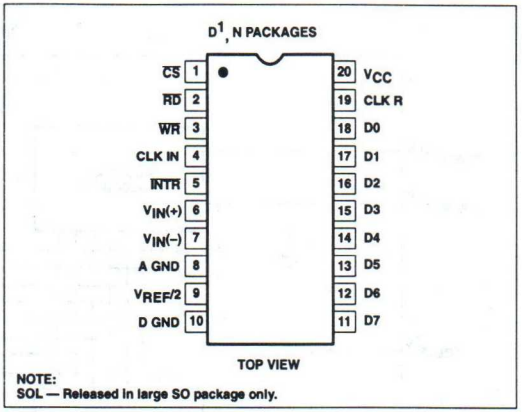
The ADC0803 family is a series of three CMOS 8-bit successive approximation A/D converters using a resistive ladder and capacitive array together with an auto-zero comparator. These converters are designed to operate with microprocessor-controlled buses using a minimum of external circuitry. The 3-State output data lines can be connected directly to the data bus.

The differential analog voltage input allows for increased common-mode rejection and provides a means to adjust the zero-scale offset. Additionally, the voltage reference input provides a means of encoding small analog voltages to the full 8 bits of resolution.

FEATURES

- Compatible with most microprocessors
- Differential inputs
- 3-State outputs
- Logic levels TTL and MOS compatible
- Can be used with internal or external clock
- Analog input range 0V to V_{CC}
- Single 5V supply
- Guaranteed specification with 1MHz clock

PIN CONFIGURATION



APPLICATIONS

- Transducer-to-microprocessor interface
- Digital thermometer
- Digitally-controlled thermostat
- Microprocessor-based monitoring and control systems

ORDERING INFORMATION

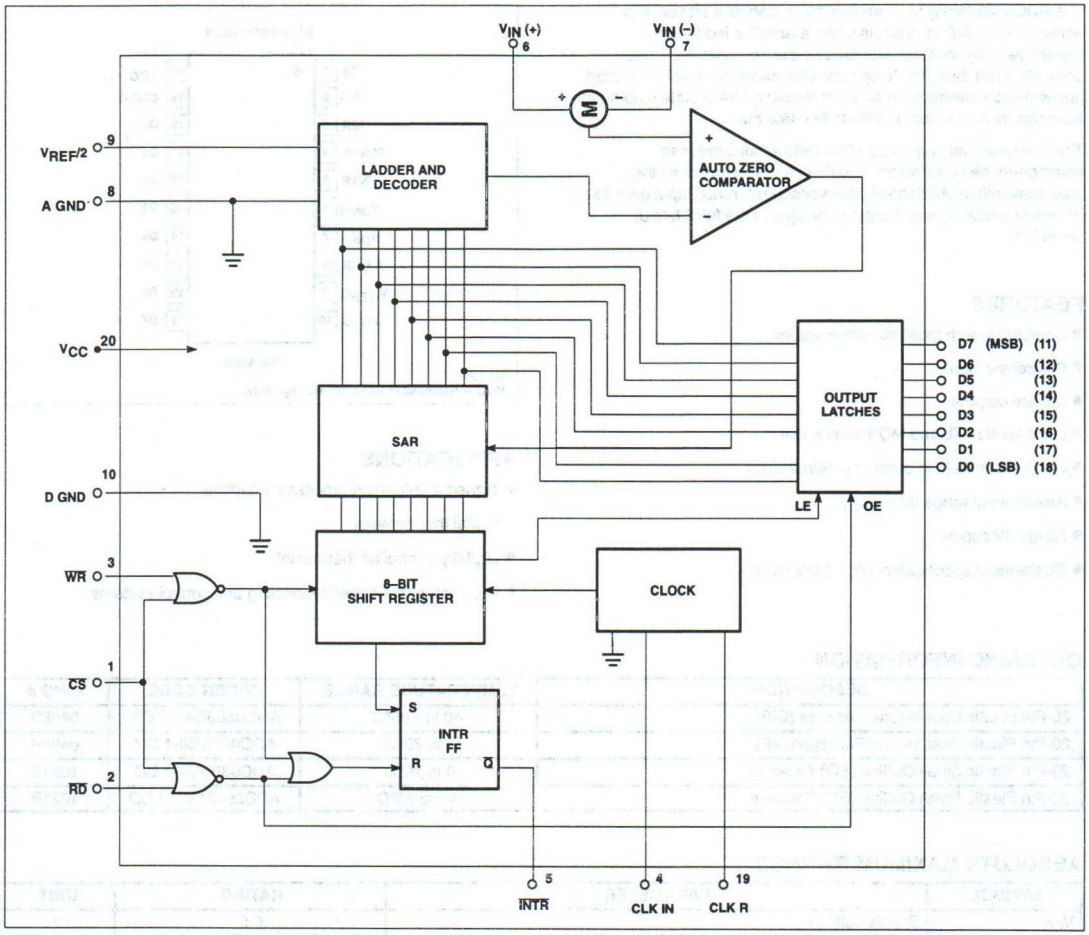
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	ADC0803/04-1 LCN	0408B
20-Pin Plastic Dual In-Line Package (DIP)	0 to 70°C	ADC0803/04-1 CN	0408B
20-Pin Plastic Small Outline (SO) Package	0 to 70°C	ADC0803/04-1 CD	1021B
20-Pin Plastic Small Outline (SO) Package	-40 to 85°C	ADC0803/04-1 LCD	1021B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	6.5	V
	Logic control input voltages	-0.3 to +16	V
	All other input voltages	-0.3 to (V_{CC} +0.3)	V
T_A	Operating temperature range		
	ADC0803/04-1 LCD	-40 to +85	°C
	ADC0803/04-1 LCN	-40 to +85	°C
	ADC0803/04-1 CD	0 to +70	°C
	ADC0803/04-1 CN	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C
P_D	Maximum power dissipation T_A=25°C (still air)[1]		
	N package	1690	mW
	D package	1390	mW

NOTES:
1. Derate above 25°C, at the following rates: N package at 13.5mW/°C; D package at 11.1mW/°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V, f_{CLK} = 1MHz, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	ADC0803/4			UNIT
			Min	Typ	Max	
	ADC0803 relative accuracy error (adjusted)	Full-Scale adjusted			0.50	LSB
	ADC0804 relative accuracy error (unadjusted)	$V_{REF}/2 = 2.500V_{DC}$			1	LSB
R_{IN}	$V_{REF}/2$ input resistance[3]	$V_{CC} = 0V$[2]	400	680		Ω
	Analog input voltage range[3]		–0.05		V_{CC}+0.05	V
	DC common-mode error	Over analog input voltage range		1/16	1/8	LSB
	Power supply sensitivity	V_{CC} = 5V ±10%[1]		1/16		LSB
Control inputs						
V_{IH}	Logical "1" input voltage	$V_{CC} = 5.25V_{DC}$	2.0		15	V_{DC}
V_{IL}	Logical "0" input voltage	$V_{CC} = 4.75V_{DC}$			0.8	V_{DC}
I_{IH}	Logical "1" input current	$V_{IN} = 5V_{DC}$		0.005	1	μA_{DC}
I_{IL}	Logical "0" input current	$V_{IN} = 0V_{DC}$	–1	–0.005		μA_{DC}
Clock in and clock R						
V_{T+}	Clock in positive-going threshold voltage		2.7	3.1	3.5	V_{DC}
V_{T-}	Clock in negative-going threshold voltage		1.5	1.8	2.1	V_{DC}
V_H	Clock in hysteresis (V_{T+})–(V_{T-})		0.6	1.3	2.0	V_{DC}
V_{OL}	Logical "0" clock R output voltage	I_{OL} = 360µA, $V_{CC} = 4.75V_{DC}$			0.4	V_{DC}
V_{OH}	Logical "1" clock R output voltage	I_{OH} = –360µA, $V_{CC} = 4.75V_{DC}$	2.4			V_{DC}
Data output and $\overline{INTR}$						
V_{OL}	Logical "0" output voltage					
	Data outputs	I_{OL} = 1.6mA, $V_{CC} = 4.75V_{DC}$			0.4	V_{DC}
	$\overline{INTR}$ outputs	I_{OL} = 1.0mA, $V_{CC} = 4.75V_{DC}$			0.4	V_{DC}
V_{OH}	Logical "1" output voltage	I_{OH} = –360µA, $V_{CC} = 4.75V_{DC}$	2.4			V_{DC}
		I_{OH} = –10µA, $V_{CC} = 4.75V_{DC}$	4.5			
I_{OZL}	3-state output leakage	$V_{OUT} = 0V_{DC}$, $\overline{CS}$ = logical "1"	–3			μA_{DC}
I_{OZH}	3-state output leakage	$V_{OUT} = 5V_{DC}$, $\overline{CS}$ = logical "1"			3	μA_{DC}
I_{SC}	+Output short-circuit current	V_{OUT} = 0V, T_A = 25°C	4.5	12		mA_{DC}
I_{SC}	–Output short-circuit current	$V_{OUT} = V_{CC}$, T_A = 25°C	9.0	30		mA_{DC}
I_{CC}	Power supply current	f_{CLK} = 1MHz, $V_{REF}/2$ = OPEN, $\overline{CS}$ = Logical "1", T_A = 25°C		3.0	3.5	mA

NOTES:
1. Analog inputs must remain within the range: $-0.05 \le V_{IN} \le V_{CC} + 0.05V$.
2. See typical performance characteristics for input resistance at V_{CC} = 5V.
3. $V_{REF}/2$ and V_{IN} must be applied after the V_{CC} has been turned on to prevent the possibility of latching.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	ADC0803/4			UNIT
					Min	Typ	Max	
	Conversion time			f_{CLK}=1MHz[1]	66		73	µs
f_{CLK}	Clock frequency[1]				0.1	1.0	3.0	MHz
	Clock duty cycle[1]				40		60	%
CR	Free-running conversion rate			$\overline{CS}$=0, f_{CLK}=1MHz $\overline{INTR}$ tied to $\overline{WR}$			13690	conv/s
$t_{W(\overline{WR})L}$	Start pulse width			$\overline{CS}$=0	30			ns
t_{ACC}	Access time	Output	$\overline{RD}$	$\overline{CS}$=0, C_L=100pF		75	100	ns
t_{1H}, t_{0H}	3-State control	Output	$\overline{RD}$	CL=10pF, R_L=10kΩ See 3-State test circuit		70	100	ns
t_{W1}, t_{R1}	$\overline{INTR}$ delay	$\overline{INTR}$	$\overline{WD}$ or $\overline{RD}$			100	150	ns
C_{IN}	Logic input=capacitance					5	7.5	pF
C_{OUT}	3-State output capacitance					5	7.5	pF

NOTES:
1. Accuracy is guaranteed at f_{CLK}=1MHz. Accuracy may degrade at higher clock frequencies.

FUNCTIONAL DESCRIPTION

These devices operate on the Successive Approximation principle. Analog switches are closed sequentially by successive approximation logic until the input to the auto-zero comparator [$V_{IN(+)}$-$V_{IN(-)}$] matches the voltage from the decoder. After all bits are tested and determined, the 8-bit binary code corresponding to the input voltage is transferred to an output latch. Conversion begins with the arrival of a pulse at the $\overline{WR}$ input if the CS input is low. On the High-to-Low transition of the signal at the WR or the CS input, the SAR is initialized, the shift register is reset, and the $\overline{INTR}$ output is set high. The A/D will remain in the reset state as long as the $\overline{CS}$ and $\overline{WR}$ inputs remain low. Conversion will start from one to eight clock periods after one or both of these inputs makes a Low-to-High transition. After the conversion is complete, the $\overline{INTR}$ pin will make a High-to-Low transition. This can be used to interrupt a processor, or otherwise signal the availability of a new conversion result. A read ($\overline{RD}$) operation (with $\overline{CS}$ low) will clear the $\overline{INTR}$ line and enable the output latches. The device may be run in the free-running mode as described later. A conversion in progress can be interrupted by issuing another start command.

Digital Control Inputs

The digital control inputs (CS, WR, $\overline{RD}$) are compatible with standard TTL logic voltage levels. The required signals at these inputs correspond to Chip Select, START Conversion, and Output Enable control signals, respectively. They are active-Low for easy interface to microprocessor and microcontroller control buses. For applications not using microprocessors, the $\overline{CS}$ input (Pin 1) can be grounded and the A/D START function is achieved by a negative-going pulse to the $\overline{WR}$ input (Pin 3). The Output Enable function is achieved by a logic low signal at the $\overline{RD}$ input (Pin 2), which may be grounded to constantly have the latest conversion present at the output.

ANALOG OPERATION

Analog Input Current

The analog comparisons are performed by a capacitive charge summing circuit. The input capacitor is switched between $V_{IN(+)}$4 and $V_{IN(-)}$, while reference capacitors are switched between taps on the reference voltage divider string. The net charge corresponds to the weighted difference between the input and the most recent total value set by the successive approximation register.

The internal switching action causes displacement currents to flow at the analog inputs. The voltage on the on-chip capacitance is switched through the analog differential input voltage, resulting in proportional currents entering the $V_{IN(+)}$ input and leaving the $V_{IN(-)}$ input. These transient currents occur at the leading edge of the internal clock pulses. They decay rapidly so do not inherently cause errors as the on-chip comparator is strobed at the end of the clock period.

Input Bypass Capacitors and Source Resistance

Bypass capacitors at the input will average the charges mentioned above, causing a DC and an AC current to flow through the output resistance of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input at full scale. This current can be a few microamps, so bypass capacitors should NOT be used at the analog inputs of the $V_{REF}/2$ input for high resistance sources (> 1kΩ). If input bypass capacitors are desired for noise filtering and a high source resistance is desired to minimize capacitor size, detrimental effects of the voltage drop across the input resistance can be eliminated by adjusting the full scale with both the input resistance and the input bypass capacitor in place. This is possible because the magnitude of the input current is a precise linear function of the differential voltage.

Large values of source resistance where an input bypass capacitor is not used will not cause errors as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (< 1kΩ) for a passive RC section or add an op amp active filter (low pass). For applications with source resistances at or below 1kΩ, a 0.1μF bypass capacitor at the inputs will prevent pickup due to series lead inductance or a long wire. A 100Ω series resistor can be used to isolate this capacitor (both the resistor and capacitor should be placed out of the feedback loop) from the output of the op amp, if used.

Analog Differential Voltage Inputs and Common-Mode Rejection

These A/D converters have additional flexibility due to the analog differential voltage input. The $V_{IN(-)}$ input (Pin 7) can be used to subtract a fixed voltage from the input reading (tare correction). This is also useful in a 4/20mA current loop conversion. Common-mode noise can also be reduced by the use of the differential input.

The time interval between sampling $V_{IN(+)}$ and $V_{IN(-)}$ is 4.5 clock periods. The maximum error due to this time difference is given by:

$V(max)=(V_P)\ (2f_{CM})\ (4.5/f_{CLK})$,

where:

V=error voltage due to sampling delay

V_P=peak value of common-mode voltage

f_{CM}=common mode frequency

For example, with a 60Hz common-mode frequency, f_{cm}, and a 1MHz A/D clock, F_{CLK}, keeping this error to 1/4 LSB (about 5mV) would allow a common-mode voltage, V_P, which is given by:

$$V_P = \frac{[V(max)\ (f_{CLK})}{(2f_{CM})(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})\ (10^4)}{(6.28)\ (60)\ (4.5)} = 2.95V$$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode voltage levels than this, however.

An analog input span less than the full 5V capability of the device, together with a relatively large zero offset, can be easily handled by use of the differential input. (See Reference Voltage Span Adjust).

Noise and Stray Pickup

The leads of the analog inputs (Pins 6 and 7) should be kept as short as possible to minimize input noise coupling and stray signal pick-up. Both EMI and undesired digital signal coupling to these inputs can cause system errors. The source resistance for these inputs should generally be below 5kΩ to help avoid undesired noise pickup. Input bypass capacitors at the analog inputs can create errors as described previously. Full scale adjustment with any input bypass capacitors in place will eliminate these errors.

Reference Voltage

For application flexibility, these A/D converters have been designed to accommodate fixed reference voltages of 5V to Pin 20 or 2.5V to Pin 9, or an adjusted reference voltage at Pin 9. The reference can be set by forcing it at $V_{REF}/2$ input, or can be determined by the supply voltage (Pin 20). Figure 1 indicates how this is accomplished.

Reference Voltage Span Adjust

Note that the Pin 9 ($V_{REF}/2$) voltage is either 1/2 the voltage applied to the V_{CC} supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. In addition to allowing for flexible references and full span voltages, this also allows for a ratiometric voltage reference. The internal gain of the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at Pin 9.

For example, a dynamic voltage range of the analog input voltage that extends from 0 to 4V gives a span of 4V (4-0), so the $V_{REF}/2$ voltage can be made equal to 2V (half of the 4V span) and full scale output would correspond to 4V at the input.

On the other hand, if the dynamic input voltage had a range of 0.5 to 3.5V, the span or dynamic input range is 3V (3.5-0.5). To encode this 3V span with 0.5V yielding a code of zero, the minimum expected input (0.5V, in this case) is applied to the $V_{IN}(-)$ pin to account for the offset, and the $V_{REF}/2$ pin is set to 1/2 the 3V span, or 1.5V. The A/D converter will now encode the $V_{IN}(+)$ signal between 0.5 and 3.5V with 0.5V at the input corresponding to a code of zero and 3.5V at the input producing a full scale output code. The full 8 bits of resolution are thus applied over this reduced input voltage range. The required connections are shown in Figure 2.

Operating Mode

These converters can be operated in two modes:

1) absolute mode
2) ratiometric mode

In absolute mode applications, both the initial accuracy and the temperature stability of the reference voltage are important factors in the accuracy of the conversion. For $V_{REF}/2$ voltages of 2.5V, initial errors of ±10mV will cause conversion errors of ±1 LSB due to the gain of 2 at the $V_{REF}/2$ input. In reduced span applications, the initial value and stability of the $V_{REF}/2$ input voltage become even more important as the same error is a larger percentage of the $V_{REF}/2$ nominal value. See Figure 3.

In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter, and, therefore, cancels out in the final digital code. See Figure 4.

Generally, the reference voltage will require an initial adjustment. Errors due to an improper reference voltage value appear as full-scale errors in the A/D transfer function.

ERRORS AND INPUT SPAN ADJUSTMENTS

There are many sources of error in any data converter, some of which can be adjusted out. Inherent errors, such as relative accuracy, cannot be eliminated, but such errors as full-scale and zero scale offset errors can be eliminated quite easily. See Figure 2.

Zero Scale Error

Zero scale error of an A/D is the difference of potential between the ideal 1/2 LSB value (9.8mV for $V_{REF}/2$=2.500V) and that input voltage which just causes an output transition from code 0000 0000 to a code of 0000 0001.

If the minimum input value is not ground potential, a zero offset can be made. The converter can be made to output a digital code of 0000 0000 for the minimum expected input voltage by biasing the $V_{IN}(-)$ input to that minimum value expected at the $V_{IN}(-)$ input to that minimum value expected at the $V_{IN}(+)$ input. This uses the

differential mode of the converter. Any offset adjustment should be done prior to full scale adjustment.

Full Scale Adjustment

Full scale gain is adjusted by applying any desired offset voltage to $V_{IN}(-)$, then applying the $V_{IN}(+)$ a voltage that is 1-1/2 LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of $V_{REF}/2$ input voltage (or the V_{CC} supply if there is no $V_{REF}/2$ input connection) for a digital output code which just changes from 1111 1110 to 1111 1111. The ideal $V_{IN}(+)$ voltage for this full-scale adjustment is given by:

$$V_{IN}(+) = V_{IN}(-) - 1.5 \times \frac{V_{MAX} - V_{MIN}}{255}$$

where:

V_{MAX}=high end of analog input range (ground referenced)

V_{MIN}=low end (zero offset) of analog input (ground referenced)

CLOCKING OPTION

The clock signal for these A/Ds can be derived from external sources, such as a system clock, or self-clocking can be accomplished by adding an external resistor and capacitor, as shown in Figure 6.

Heavy capacitive or DC loading of the CLK R pin should be avoided as this will disturb normal converter operation. Loads less than 50pF are allowed. This permits driving up to seven A/D converter CLK IN pins of this family from a single CLK R pin of one converter. For larger loading of the clock line, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the CLK R pin.

Restart During a Conversion

A conversion in process can be halted and a new conversion began by bringing the $\overline{CS}$ and $\overline{WR}$ inputs low and allowing at least one of them to go high again. The output data latch is not updated if the conversion in progress is not completed; the data from the previously completed conversion will remain in the output data latches until a subsequent conversion is completed.

Continuous Conversion

To provide continuous conversion of input data, the $\overline{CS}$ and $\overline{RD}$ inputs are grounded and $\overline{INTR}$ output is tied to the $\overline{WR}$ input. This $\overline{INTR}/\overline{WR}$ connection should be momentarily forced to a logic low upon power-up to insure circuit operation. See Figure 5 for one way to accomplish this.

DRIVING THE DATA BUS

This CMOS A/D converter, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry tied to the data bus will add to the total capacitive loading, even in the high impedance mode.

There are alternatives in handling this problem. The capacitive loading of the data bus slows down the response time, although DC specifications are still met. For systems with a relatively low CPU clock frequency, more time is available in which to establish proper logic levels on the bus, allowing higher capacitive loads to be driven (see Typical Performance Characteristics).

At higher CPU clock frequencies, time can be extended for I/O reads (and/or writes) by inserting wait states (8880) or using clock-extending circuits (6800, 8035).

Finally, if time is critical and capacitive loading is high, external bus drivers must be used. These can be 3-State buffers (low power Schottky is recommended, such as the N74LS240 series) or special higher current drive products designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended as the PNP input offers low loading of the A/D output, allowing better response time.

POWER SUPPLIES

Noise spikes on the V_{CC} line can cause conversion errors as the internal comparator will respond to them. A low inductance filter capacitor should be used close to the converter V_{CC} pin and values of 1µF or greater are recommended. A separate 5V regulator for the converter (and other 5V linear circuitry) will greatly reduce digital noise on the V_{CC} supply and the attendant problems.

WIRING AND LAYOUT PRECAUTIONS

Digital wire-wrap sockets and connections are not satisfactory for breadboarding this (or any) A/D converter. Sockets on PC boards can be used. All logic signal wires and leads should be grouped or kept as far as possible from the analog signal leads. Single wire analog input leads may pick up undesired hum and noise, requiring the use of shielded leads to the analog inputs in many applications.

A single-point analog ground separate from the logic or digital ground points should be used. The power supply bypass capacitor and the self-clocking capacitor, if used, should be returned to digital ground. Any $V_{REF}/2$ bypass capacitor, analog input filter capacitors, and any input shielding should be returned to the analog ground point. Proper grounding will minimize zero-scale errors which are present in every code. Zero-scale errors can usually be traced to improper board layout and wiring.

APPLICATIONS

Microprocessor Interfacing

This family of A/D converters was designed for easy microprocessor interfacing. These converters can be memory mapped with appropriate memory address decoding for $\overline{CS}$ (read) input. The active-Low write pulse from the processor is then connected to the $\overline{WR}$ input of the A/D converter, while the processor active-Low read pulse is fed to the converter $\overline{RD}$ input to read the converted data. If the clock signal is derived from the microprocessor system clock, the designer/programmer should be sure that there is no attempt to read the converter until 74 converter clock pulses after the start pulse goes high. Alternatively, the $\overline{INTR}$ pin may be used to interrupt the processor to cause reading of the converted data. Of course, the converter can be connected and addressed as a peripheral (in I/O space), as shown in Figure 7. A bus driver should be used as a buffer to the A/D output in large microprocessor systems where the data leaves the PC board and/or must drive capacitive loads in excess of 100pF. See Figure 9.

Interfacing the SCN8048 microcomputer family is pretty simple, as shown in Figure 8. Since the SCN8048 family has 24 I/O lines, one of these (shown here as bit 0 or port 1) can be used as the chip select signal to the converter, eliminating the need for an address

decoder. The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing to a dummy address.

Digitizing a Transducer Interface Output

Circuit Description

Figure 10 shows an example of digitizing transducer interface output voltage. In this case, the transducer interface is the NE5521, an LVDT (Linear Variable Differential Transformer) Signal Conditioner. The diode at the A/D input is used to insure that the input to the A/D does not go excessively beyond the supply voltage of the A/D. See the NE5521 data sheet for a complete description of the operation of that part.

Circuit Adjustment

To adjust the full scale and zero scale of the A/D, determine the range of voltages that the transducer interface output will take on. Set the LVDT core for null and set the Zero Scale Scale Adjust Potentiometer for a digital output from the A/D of 1000 000. Set the LVDT core for maximum voltage from the interface and set the Full Scale Adjust potentiometer so the A/D output is just barely 1111 1111.

A Digital Thermostat

Circuit Description

The schematic of a Digital Thermostat is shown in Figure 11. The A/D digitizes the output of the LM35, a temperature transducer IC with an output of 10mV per °C. With $V_{REF}/2$ set for 2.56V, this 10mV corresponds to 1/2 LSB and the circuit resolution is 2°C. Reducing $V_{REF}/2$ to 1.28 yields a resolution of 1°C. Of course, the lower $V_{REF}/2$ is, the more sensitive the A/D will be to noise.

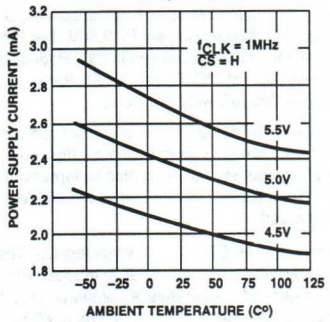
The desired temperature is set by holding either of the set buttons closed. The SCC80C451 programming could cause the desired (set) temperature to be displayed while either button is depressed and for a short time after it is released. At other times the ambient temperature could be displayed.

The set temperature is stored in an SCN8051 internal register. The A/D conversion is started by writing anything at all to the A/D with port pin P10 set high. The desired temperature is compared with the digitized actual temperature, and the heater is turned on or off by clearing setting port pin P12. If desired, another port pin could be used to turn on or off an air conditioner.

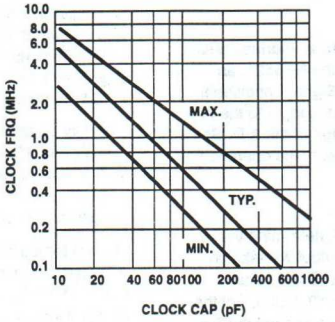
The display drivers are NE587s if common anode LED displays are used. Of course, it is possible to interface to LCD displays as well.

TYPICAL PERFORMANCE CHARACTERISTICS

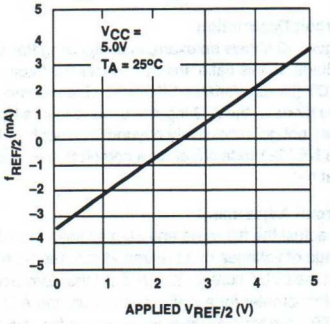
Power Supply Current vs Temperature



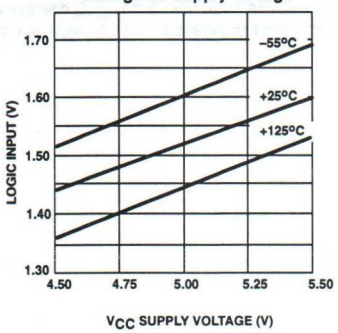
Clock Frequency vs Clock Capacitor



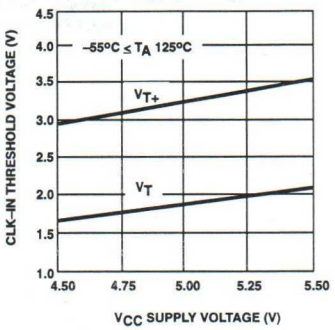
Input Current vs Applied Voltage at $V_{REF/2}$ Pin



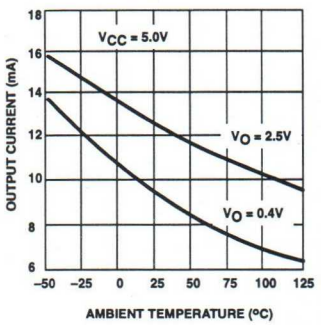
Logic Input Threshold Voltage vs Supply Voltage



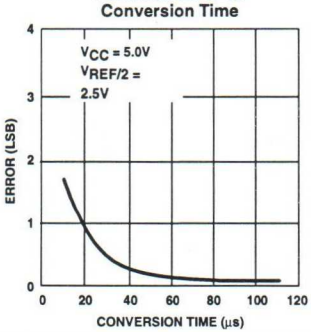
CLK–IN Threshold Voltage vs Supply Voltage



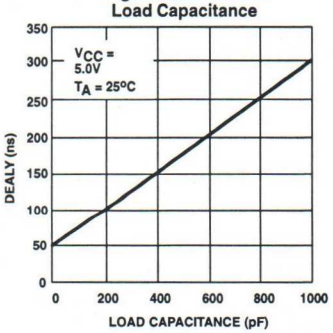
Output Current vs Temperature



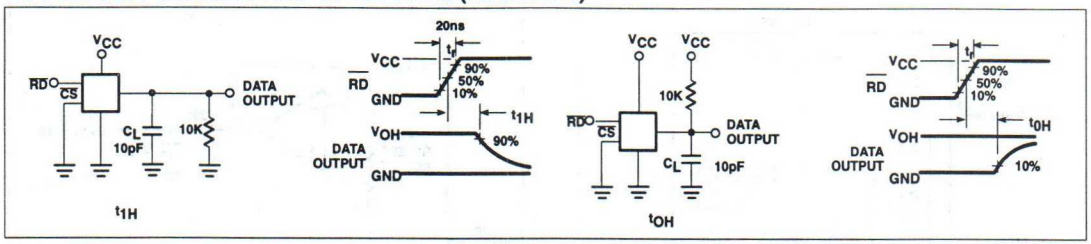
Full Scale Error vs Conversion Time



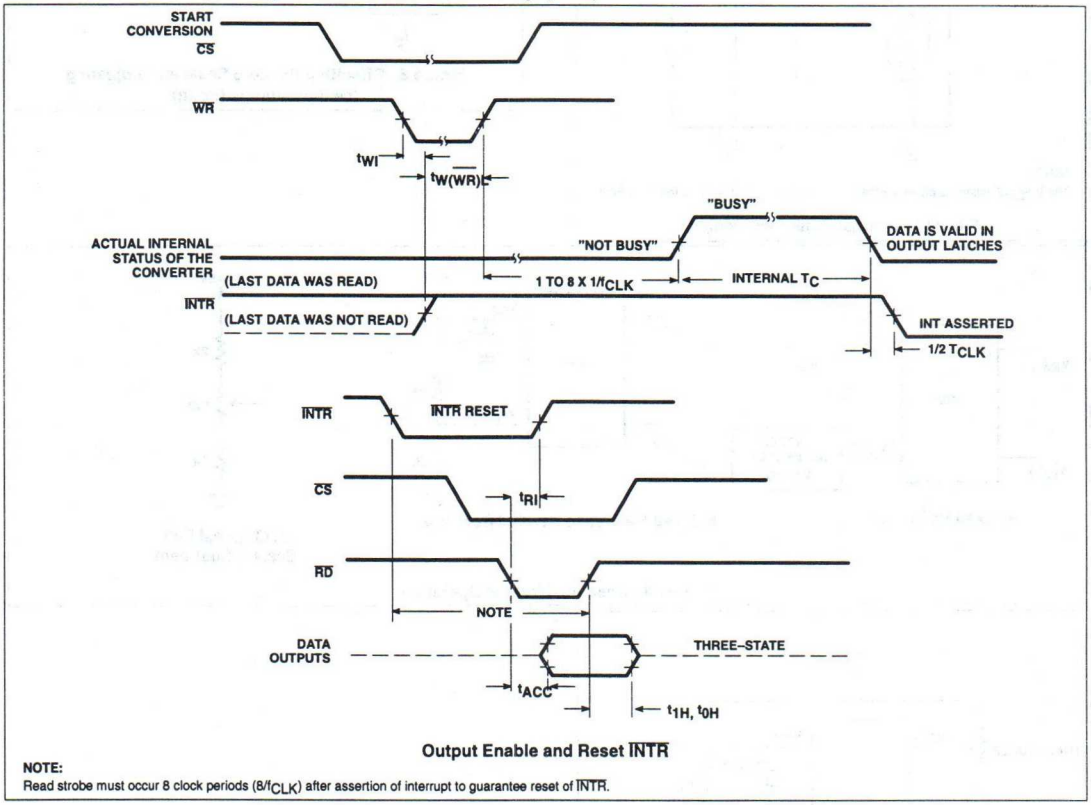
Delay From $\overline{RD}$ Falling Edge to Data Valid vs Load Capacitance



3-STATE TEST CIRCUITS AND WAVEFORMS (ADC0801-1)

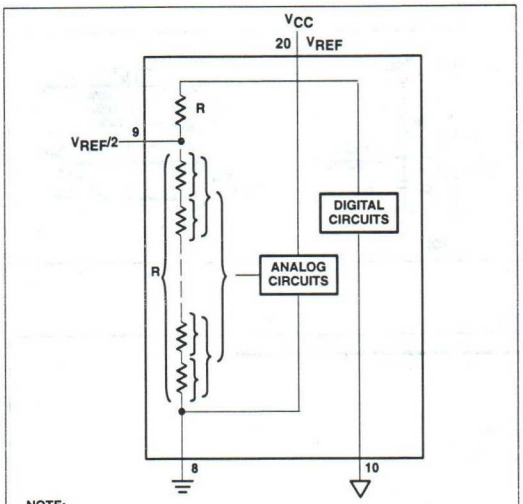


TIMING DIAGRAMS (All timing is measured from the 50% voltage points)



Output Enable and Reset $\overline{INTR}$

NOTE:
Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.



NOTE:
The $V_{REF}/2$ voltage is either 1/2 the V_{CC} voltage or is that which is forced at Pin 9.

Figure 1. Internal Reference Design

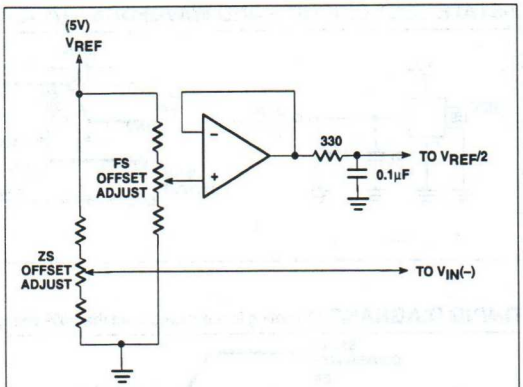


Figure 2. Offsetting the Zero Scale and Adjusting the Input Range (Span)

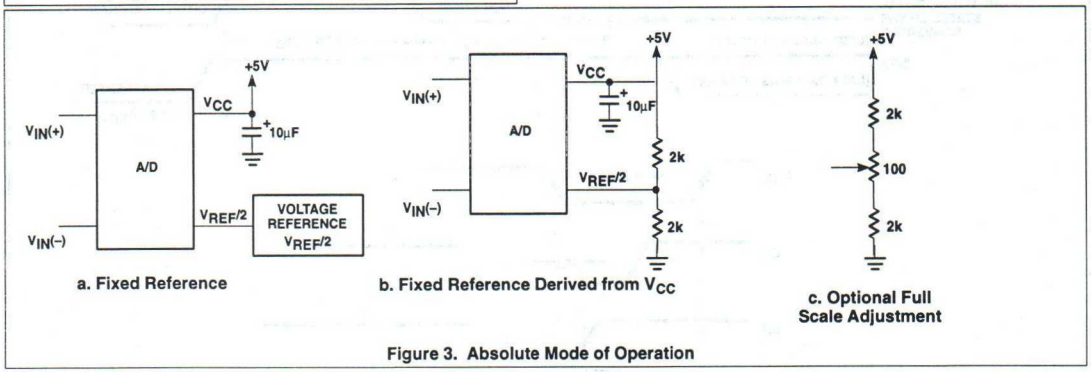


Figure 3. Absolute Mode of Operation

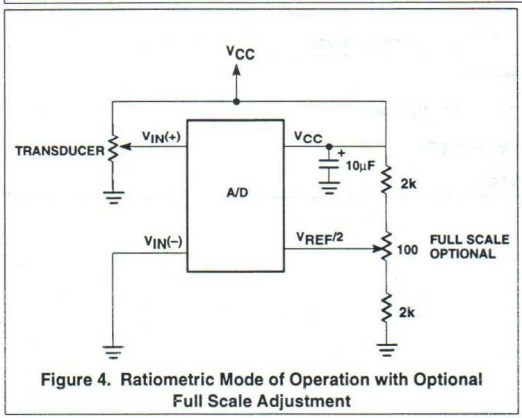


Figure 4. Ratiometric Mode of Operation with Optional Full Scale Adjustment

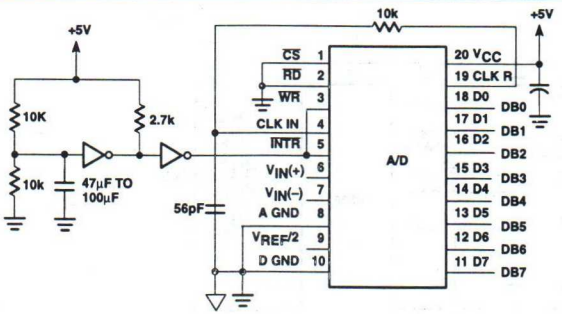


Figure 5. Connection for Continuous Conversion

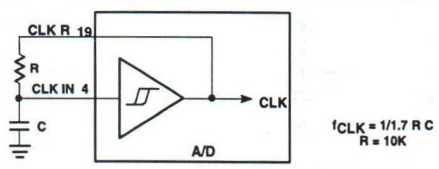


Figure 6. Self-Clocking the Converter

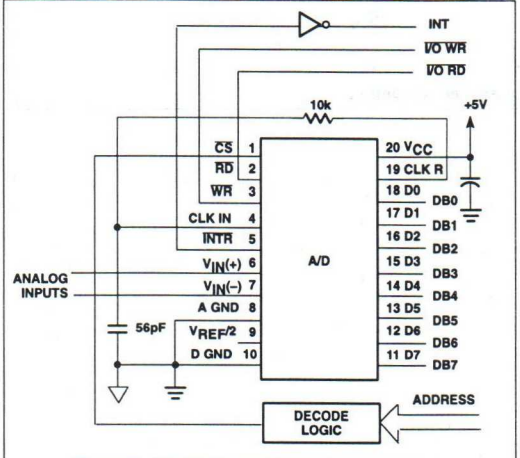


Figure 7. Interfacing to 8080A Microprocessor

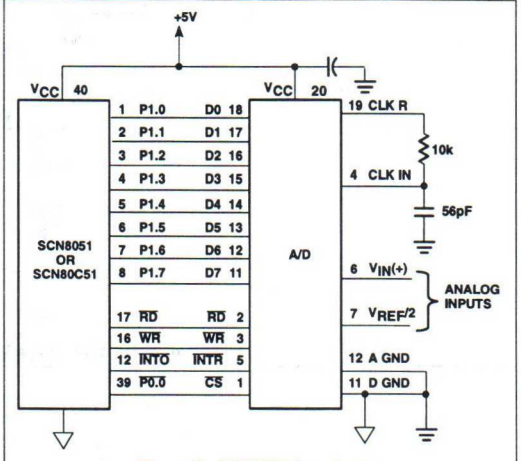


Figure 8. SCN8051 Interfacing

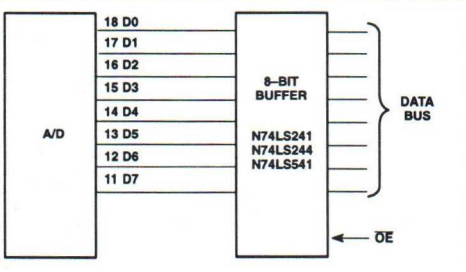


Figure 9. Buffering the A/D Output to Drive High Capacitance Loads and for Driving Off-Board Loads

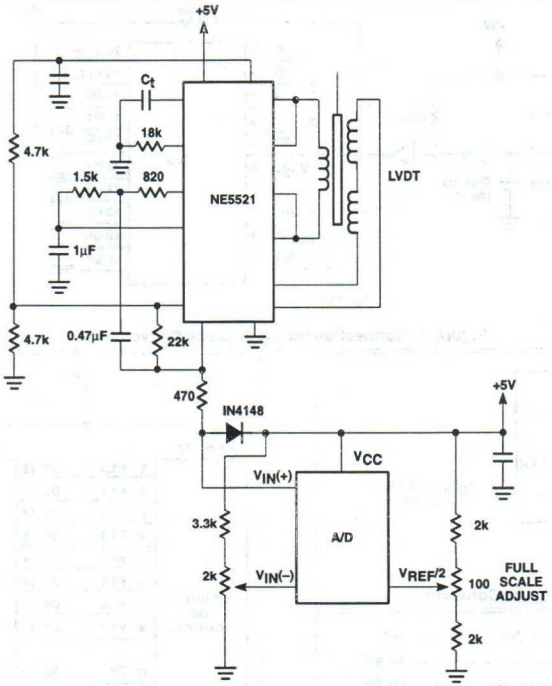


Figure 10. Digitizing a Transducer Interface Output

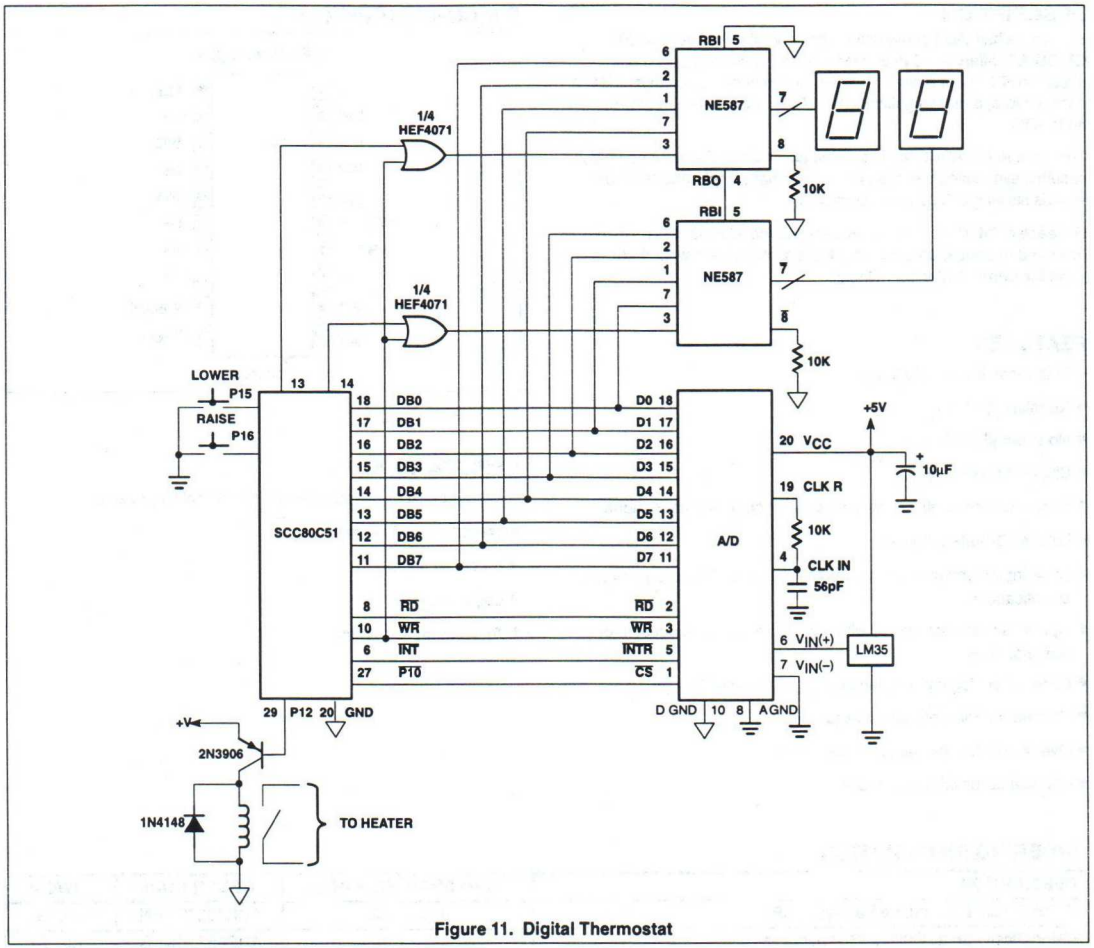


Figure 11. Digital Thermostat

8-Bit, high-speed, μP-compatible A/D converter with track/hold function

ADC0820

DESCRIPTION

By using a half-flash conversion technique, the 8-bit ADC0820 CMOS A/D offers a 1.5μs conversion time while dissipating a maximum 75mW of power. The half-flash technique consists of 31 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

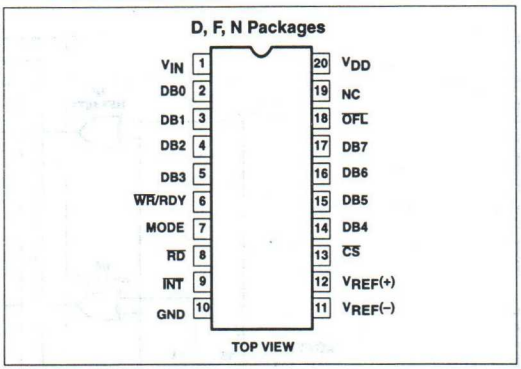
The input to the ADC0820 is tracked and held by the input sampling circuitry, eliminating the need for an external sample-and-hold for signals slewing at less than 100mV/μs.

For ease of interface to microprocessors, the ADC0820 has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

FEATURES

- Built-in track-and-hold function
- No missing codes
- No external clocking
- Single supply—$5V_{DC}$
- Easy interface to all microprocessors, or operates stand-alone
- Latched 3-State outputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Operates ratiometrically or with any reference value equal to or less than V_{DD}
- 0V to 5V analog input voltage range with single 5V supply
- No zero- or full-scale adjust required
- Overflow output available for cascading
- 0.3″ standard width 20-pin DIP

PIN CONFIGURATION



APPLICATIONS

- Microprocessor-based monitoring and control systems
- Transducer/μP interface
- Process control
- Logic analyzers
- Test and measurement

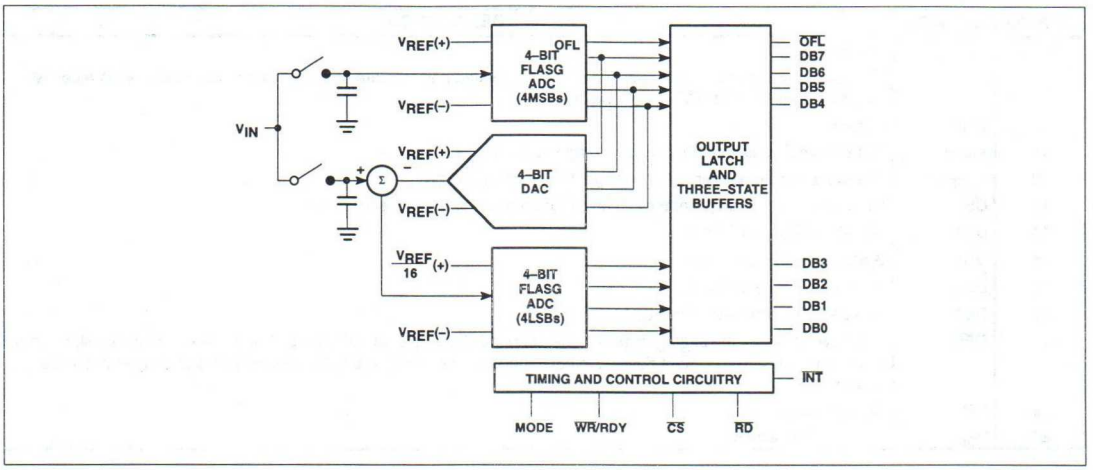
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	ADC0820CNEN	0408B
20-Pin Plastic Small Outline (SO) package	0 to +70°C	ADC0820CNED	1021B

8-Bit, high-speed, µP-compatible A/D converter with track/hold function

ADC0820

BLOCK DIAGRAM



PIN DESCRIPTION

PIN NO	SYMBOL	DESCRIPTION
1	V_{IN}	Analog input; range=GND≤V_{IN}≤V_{DD}
2	DB0	3-state data output—Bit 0 (LSB)
3	DB1	3-state data output—Bit 1
4	DB2	3-state data output—Bit 2
5	DB3	3-state data output—Bit 3
6	$\overline{WR}$/RDY	**WR-RD Mode** $\overline{WR}$: With $\overline{CS}$ Low, the conversion is started on the falling edge of $\overline{WR}$. Approximately 800ns (the preset internal time out, t_I) after the $\overline{WR}$ rising edge, the result of the conversion will be strobed into the output latch, provided that $\overline{RD}$ does not occur prior to this time out (see Figures 3a and 3b). **RD Mode** RDY: This is an open-drain output (no internal pull-up device). RDY will go Low after the falling edge of $\overline{CS}$; RDY will go 3-State when the result of the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system (see Figure 1).
7	Mode	Mode: Mode selection input—it is internally tied to GND through a 30µA current source. RD Mode: When mode is Low. WR-RD Mode: When mode is High.
8	$\overline{RD}$	**WR-RD Mode** With $\overline{CS}$ Low, the 3-State data outputs (DB0-DB7) will be activated when $\overline{RD}$ goes Low. $\overline{RD}$ can also be used to increase the speed of the converter by reading data prior to the preset internal time out (T_I ~ 800ns). If this is done, the data result transferred to output latch is latched after the falling edge of the $\overline{RD}$ (see Figures 3a and 3b). **RD Mode** With $\overline{CS}$ Low, the conversion will start with $\overline{RD}$ going Low; also, $\overline{RD}$ will enable the 3-State data outputs at the completion of the conversion. RDY going 3-State and $\overline{INT}$ going Low indicate the completion of the conversion (see Figure 1).
9	$\overline{INT}$	**WR-RD Mode** $\overline{INT}$ going Low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ will go Low ~ 800ns (the preset internal time out, t_I) after the rising edge of $\overline{WR}$ (see Figure 3a); or $\overline{INT}$ will go Low after the falling edge of $\overline{RD}$, if $\overline{RD}$ goes Low prior to the 800ns time out (see Figure 3b). $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (see Figures 3a and 3b).

PIN DESCRIPTION (Continued)

PIN NO	SYMBOL	DESCRIPTION
		RD Mode $\overline{INT}$ going Low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (see Figure 1).
10	GND	Ground
11	$V_{REF}(-)$	The bottom of resistor ladder, voltage range: $GND \leq V_{REF}(-) \leq V_{REF}(+)$
12	$V_{REF}(+)$	The top of resistor ladder, voltage range: $V_{REF}(-) \leq V_{REF}(+) \leq V_{DD}$.
13	$\overline{CS}$	$\overline{CS}$ must be Low in order for the $\overline{RD}$ or $\overline{WR}$ to be recognized by the converter.
14	DB4	3-State data output—Bit 4
15	DB5	3-State data output—Bit 5
16	DB6	3-State data output—Bit 6
17	DB7	3-State data output—Bit 7 (MSB)
18	$\overline{OFL}$	Overflow output—if the analog input is higher than the $V_{REF}(+)$- LSB, $\overline{OFL}$ will be low at the end of conversion. It can be used to cascade 2 or more devices to have more resolution (9, 10-bit). It is always active and never becomes 3-state.
19	NC	No connection
20	V_{DD}	Power supply voltage

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage	7	V
	Logic control inputs	-0.2 to V_{DD}+0.2	V
	Voltage at other inputs and output	-0.2 to V_{DD}+0.2	V
T_{STG}	Storage temperature range	-65 to +150	°C
P_D	Maximum power dissipation[3] T_A=25°C(still-air)		
	N package	1690	mW
	D package	1390	mW
T_{SOLD}	Lead temperature (soldering, 10sec)	300	°C
T_A	Operating ambient temperature range	$T_{MIN} \leq T_A \leq T_{MAX}$	
	ADC0820CNEN/CNED	0 to +70	°C

NOTES:
1. Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.
2. All voltages are measured with respect to GND, unless otherwise specified.
3. Derate above 25°C at the following rates:
   N package at 13.5mW/°C
   D package at 11.1mW/°C

DC ELECTRICAL CHARACTERISTICS

RD mode (Pin 7=0), V_{DD}=5V, $V_{REF}(+)$=5V, and $V_{REF}(-)$=GND, unless otherwise specified. Limits apply from T_{MIN} to T_{MAX}.

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Min	Typ[3]	Max	
	Resolution			8	8	8	bits
	Unadjusted error[1]	ADC0820C				±1	LSB
R_{REF}	Reference resistance			1	1.6	4	kΩ
$V_{REF}(+)$	Input voltage[5]			$V_{REF}(-)$		V_{DD}	V
$V_{REF}(-)$	Input voltage			GND		$V_{REF}(+)$	V
V_{IN}	Input voltage[5]			GND-0.1		V_{DD}+0.1	V
	Maximum analog input leakage current	$\overline{CS}=V_{DD}$ $V_{IN}=V_{DD}$ V_{IN}=GND		-3		3	µA
	Power supply sensitivity	V_{DD}=5V±5%			±1/16	±1/4	LSB
$V_{IN(1)}$	Logical "1" input voltage	V_{DD}=5.25V	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	2.0		V_{DD}	V
			Mode	3.5		V_{DD}	
$V_{IN(0)}$	Logical "0" input voltage	V_{DD}=4.75V	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	GND		0.8	V
			Mode	GND		1.5	
$I_{IN(1)}$	Logical "1" input current	$V_{IN(1)}$=5V; $\overline{CS}$, $\overline{RD}$				1	µA
		$V_{IN(1)}$=5V; $\overline{WR}$				3	
		$V_{IN(1)}$=5V; Mode			30	200	
$I_{IN(0)}$	Logical "0" input current	$V_{IN(0)}$=0V; $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, Mode		-1			µA
$V_{OUT(1)}$	Logical "1" output voltage	V_{DD}=4.75V, I_{OUT}=-360µA; DB0-DB7, $\overline{OFL}$, $\overline{INT}$		2.4	4.6		V
		V_{DD}=4.75V, I_{OUT}=-10µA DB0-DB7, $\overline{OFL}$, $\overline{INT}$		4.5	4.74		
$V_{OUT(0)}$	Logical "0" output voltage	V_{DD}=4.75V, I_{OUT}=1.6mA; DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY			0.2	0.4	V
I_{OZ}	3-state output current	V_{OUT}=5V; DB0-DB7, RDY				3	µA
		V_{OUT}=0V; DB0-DB7, RDY		-3			
I_{SOURCE}	Output source current	V_{OUT}=0V, DB0-DB7, $\overline{OFL}$		6	12		mA
		$\overline{INT}$		4.5	8		
I_{SINK}	Output sink current	V_{OUT}=5V; DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY		7	20		mA
I_{DD}	Supply current	$\overline{CS}$=$\overline{WR}$=$\overline{RD}$=0			6	15	mA
V_{DD}	Range			4.5		5.5	V

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, $t_R = t_F$ = 20ns, $V_{REF(+)}$ = 5V, $V_{REF(-)}$ = 0V, and T_A = 25°C, unless otherwise specified.

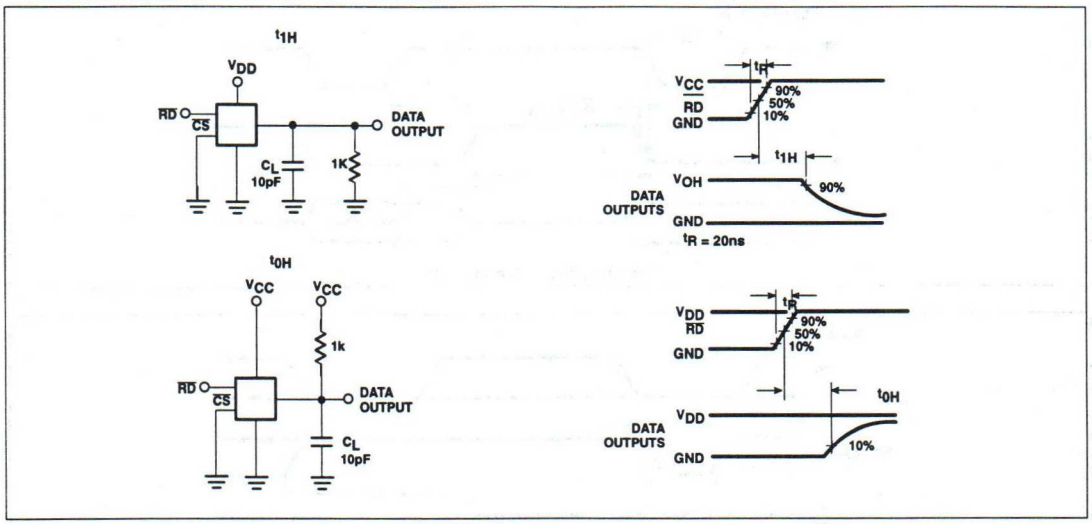
SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS[4]			UNIT
				Min	Typ[3]	Max	
t_{CRD}	Conversion time for RD mode		Mode=0, Figure 1		1.6	2.5	µs
t_{ACCO}	Access time (delay from falling edge of $\overline{RD}$ to output valid)		Mode=0, Figure 1		t_{CRD}+20	t_{CRD}+50	ns
t_{CWR-RD}	Conversion time for WR-RD mode		Mode=V_{DD}, t_{WR}=600ns, t_{RD}=600ns; Figures 3a and 3b			1.52	µs
t_{WR}	Write time	Min	Mode=V_{DD}, Figures 3a and 3b[2]	600			ns
		Max				50	µs
t_{RD}	Read time	Min	Mode=V_{DD}, Figures 3a and 3b[2]	600			ns
t_{ACC1}	Access time (delay from falling edge of $\overline{RD}$ t o output valid)		Mode=V_{DD}, t_{RD}<t_I; Figure 3b, C_L=15pF		190	280	ns
			C_L=100pF		210	320	
t_{ACC2}	Access time (delay from falling edge of $\overline{RD}$ t o output valid)		Mode=V_{DD}, t_{RD}>t_I; Figure 3a, C_L=15pF		70	120	ns
			C_L=100pF		90	150	ns
t_I	Internal comparison time		Mode=V_{DD}; Figures 2 and 3a, C_L=50pF		800	1300	ns
t_{1H}, t_{0H}	Three-state control (delay from rising edge of $\overline{RD}$ to Hi-Z state)		R_L=1kΩ, C_L=10pF		100	200	ns
$t_{\overline{INTL}}$	Delay from rising edge of $\overline{WR}$ to falling edge of $\overline{INT}$		Mode=V_{DD}, C_L=50pF t_{RD}>t_I; Figure 3a t_{RD}<t_I; Figure 3b		 t_{RD}+200	 t_I t_{RD}+290	 ns ns
$t_{\overline{INTH}}$	Delay from rising edge of $\overline{RD}$ to rising edge of $\overline{INT}$		Figures 1, 3a, and 3b, C_L=50pF		125	225	ns
$t_{\overline{INTHWR}}$	Delay from rising edge of $\overline{WR}$ to rising edge of $\overline{INT}$		Figure 2, C_L=50pF		175	270	ns
t_{RDY}	Delay from $\overline{CS}$ to RDY		Figure 1, C_L=50pF, Mode=0		50	100	ns
t_{ID}	Delay from $\overline{INT}$ to output valid		Figure 2		20	50	ns
t_{RI}	Delay from $\overline{RD}$ to $\overline{INT}$		Mode=V_{DD}, t_{RD}<t_I; Figure 3b		200	290	ns
t_P	Delay from end of conversion to next conversion		Figures 1, 2, 3a, and 3b[2]	500			ns
SR	Slew rate, tracking				0.1		V/µs
C_{VIN}	Analog input capacitance				45		pF
C_{OUT}	Logic output capacitance				5		pF
C_{IN}	Logic input capacitance				5		pF

NOTES:

1. Unadjusted error includes offset, full-scale, and linearity errors.
2. Accuracy may degrade if t_{WR} or t_{RD} is shorter than the minimum value specified.
3. Typical values are at 25°C and represent most likely parametric norm.
4. Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

5. V_{REF} and VIN must be applied after V_{CC} has been turned on to prevent possibility of latching.

3-STATE TEST CIRCUITS AND WAVEFORMS



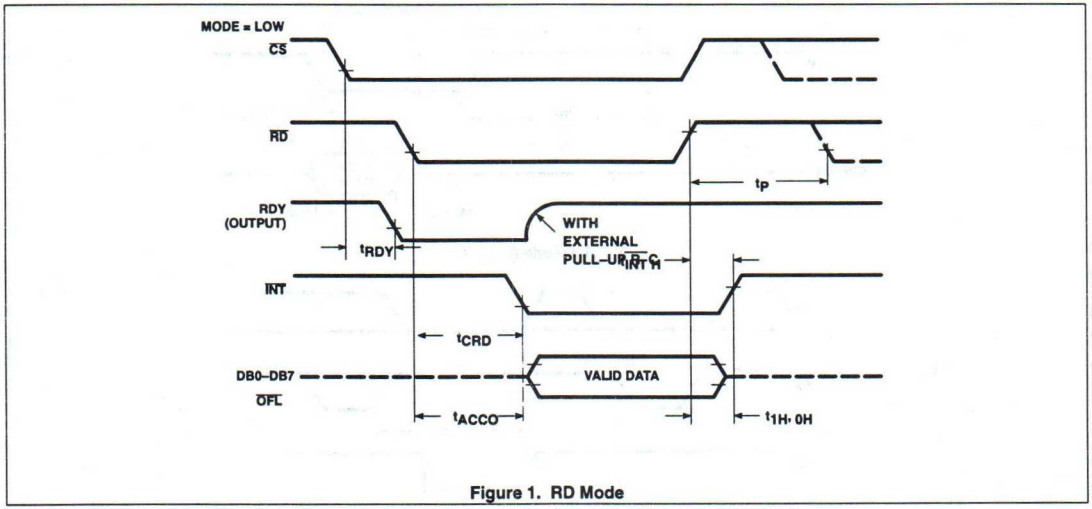


Figure 1. RD Mode

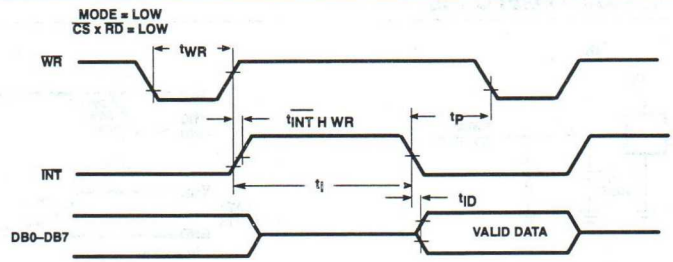
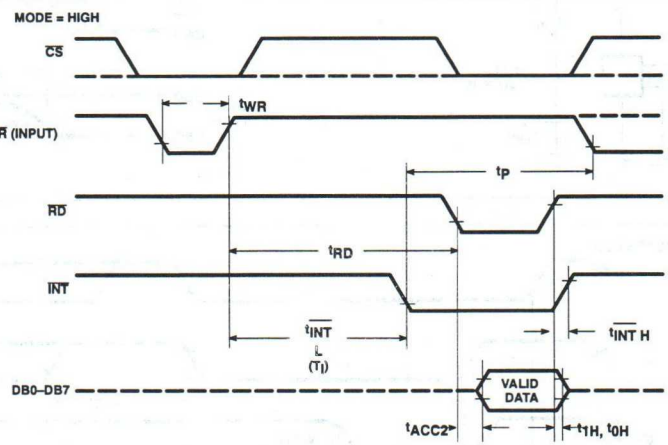
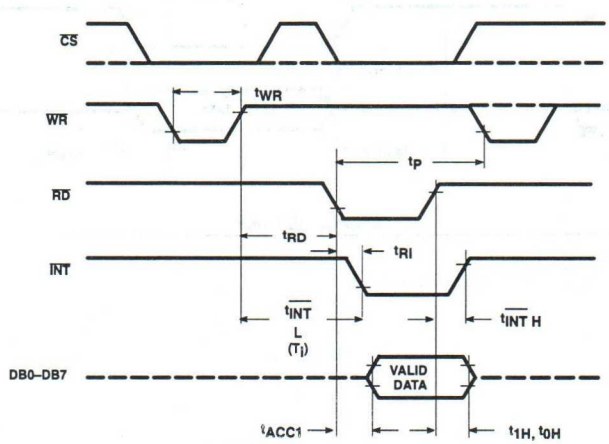


Figure 2. Stand-Alone Mode



a. WR-RD Mode ($t_{RD} > t_I$)



b. WR-RD Mode ($t_{RD} < t_I$)

Figure 3. WR-RD Mode

FUNCTIONAL DESCRIPTION

General Operation

The ADC0820 uses two 4-bit flash A/D converters to make an 8-bit measurement (Block Diagram). Each flash ADC is made up of 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. To take a full 8-bit reading, one flash conversion is done to provide the 4 most significant data bits (via the MS flash ADC). Driven by the 4 MSBs, an internal DAC recreates an analog approximation of the input voltage. This analog signal is then subtracted from the input, and the difference voltage is converted by a second 4-bit flash ADC (the LS ADC), providing the 4 least significant bits of the output data word.

The internal DAC is actually a subsection of the MS flash converter. This is accomplished by using the same resistor ladder for the A/D as well as for generating the DAC signal. The DAC output is actually the tap on the resistor ladder which most closely approximates the analog input. In addition, the "sampled data" comparators used in the ADC0820 provide the ability to compare the magnitudes of several analog signals simultaneously, without using input summing amplifiers. This is especially useful in the LS flash ADC, where the signal to be converted is an analog difference.

The Sampled-Data Comparator

Each comparator in the ADC0820 consists of a CMOS inverter with a capacitively-coupled input (Figure 4). Analog switches connect the two comparator inputs to the input capacitor (C) and also connect the inverter's input and output. This device in effect now has one differential input pair. A comparison requires two cycles, one for zeroing the comparator, and another for making the comparison.

In the first cycle, one input switch and the inverter's feedback switch (Figure 4a) are closed. In this interval, C is charged to the connected input (V1) less the inverter's bias voltage (V_S, approximately 1.6V). In the second cycle (Figure 4b), these two switches are opened and the other (V2) input's switch is closed. The input capacitor now subtracts its stored voltage from the second input and the difference is amplified by the inverter's open loop gain. The inverter's input ($V_{S'}$) becomes

$$V'_{S'} = V_S + (V2 - V1)\frac{C}{C + C_S}$$

and the output will go High or Low depending on the sign of $V'_{S'}$-V_S.

The actual circuitry used in the ADC0820 is a simple but important expansion of the basic comparator described above. By adding a second capacitor and another set of switches to the input (Figure 5), the scheme can be expanded to make dual differential comparisons. In this circuit, the feedback switch and one input switch on each capacitor (Z switches) are closed in the zeroing cycle. A comparison is then made by connecting the second input on each capacitor (S switches) and opening all of the other switches. The change in voltage at the inverter's input, as a result of the change in charge on each input capacitor, will now depend on both input signal differences.

Architecture

In the ADC0820, 15 comparators are used in the MS and LS 4-bit flash A/D converters. The MS (most significant) flash ADC also has one additional comparator to detect input over-range. These two sets of comparators operate alternately, with one group in its zeroing cycle while the other is comparing.

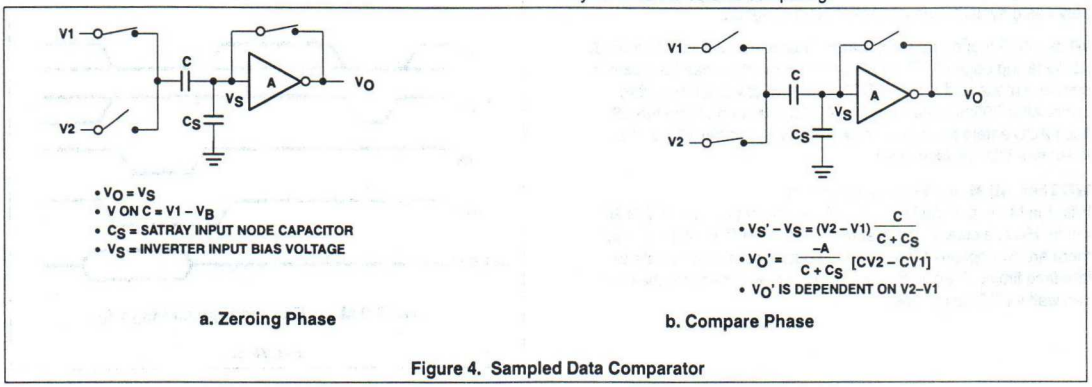


Figure 4. Sampled Data Comparator

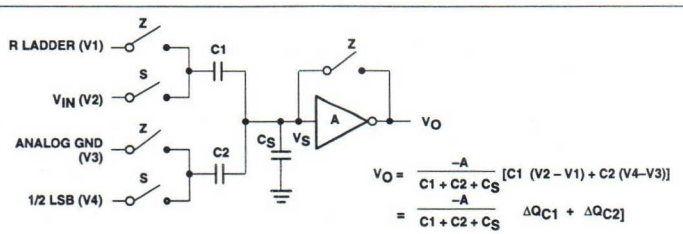


Figure 5. ADC0820 Comparator (From MS Flash ADC)

To start a conversion in the WR-RD mode, the $\overline{WR}$ line is brought Low. At this instant the MS comparators go from zeroing to comparison mode (Figure 8). When $\overline{WR}$ is returned High after at least 600ns, the output from the first set of comparators (the first flash) is decoded and latched. At this point the two 4-bit converters change modes and the LS (least significant) flash ADC enters its compare cycle. No less than 600ns later, the $\overline{RD}$ line may be pulled Low to latch the lower four data bits and finish the 8-bit conversion. When $\overline{RD}$ goes Low, the flash A/Ds change state once again in preparation for the next conversion.

Figure 8 also outlines how the converter's interface timing relates to its analog input (V_{IN}). In WR-RD mode, V_{IN} is measured while $\overline{WR}$ is Low. In RD mode, sampling occurs during the first 800ns of $\overline{RD}$. Because of the input connections to the ADC0820's LS and MS comparators, the converter has the ability to sample V_{IN} at one instant, despite the fact that two separate 4-bit conversions are being done. More specifically, when $\overline{WR}$ is Low the MS flash is in compare mode (connected to V_{IN}, and the LS flash is in zero mode (also connected to V_{IN}). Therefore both flash ADCs sample V_{IN} at the same time.

Digital Interface

The ADC0820 has two basic interface modes which are selected by strapping the Mode pin High or Low.

RD Mode (Figure 6a)

With the Mode pin grounded, the converter is set to Read mode. In this configuration, a complete conversion is done by pulling $\overline{RD}$ Low until output data appears. An $\overline{INT}$ line is provided which goes Low at the end of the conversion as well as a RDY output which can be used to signal a processor that the converter is busy or can also serve as a system Transfer Acknowledge signal.

When in RD mode, the comparator phases are internally triggered. At the falling edge of $\overline{RD}$, the MS flash converter goes from zero to compare mode and the LS ADC's comparators enter their zero cycle. After 800ns, data from the MS flash is latched and the LS flash ADC enters compare mode. Following another 800ns, the lower four bits are recovered.

WR Then RD Mode (Figures 6b and c)

With the Mode pin tied High, the A/D will be set up for the WR-RD mode. Here, a conversion is started with the $\overline{WR}$ input; however, there are two options for reading the output data which relate to interface timing. If an interrupt-driven scheme is desired, the user can wait for $\overline{INT}$ to go Low

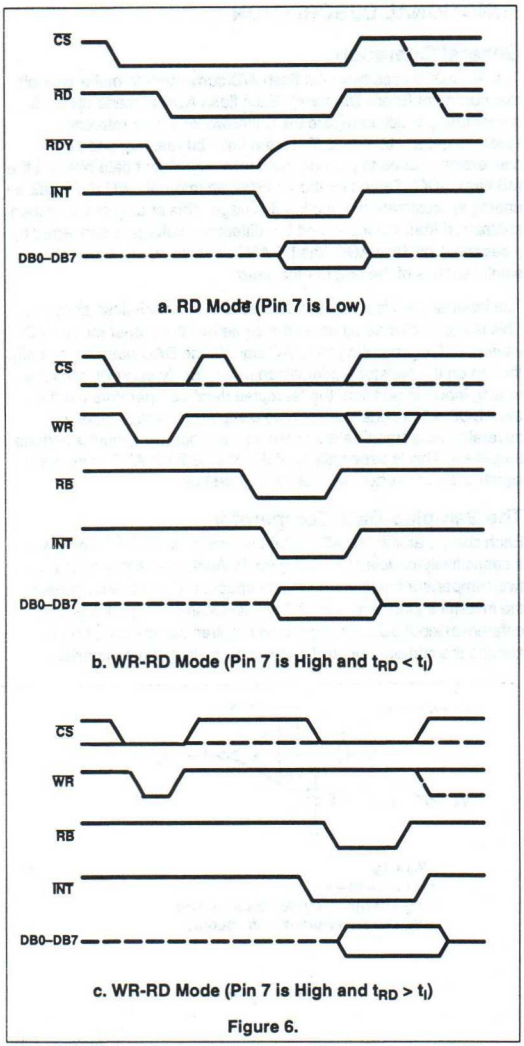


Figure 6.

before reading the conversion result. $\overline{INT}$ will typically go Low 800ns after $\overline{WR}$'s rising edge. However, if a shorter conversion time is desired, the processor need not wait for $\overline{INT}$ and can exercise a Read after only 600ns. If this is done, $\overline{INT}$ will immediately go Low and data will appear at the outputs.

Stand-Alone (Figure 7)
For stand-alone operation in WR-RD mode, $\overline{CS}$ and $\overline{RD}$ can be tied Low and a conversion can be started with $\overline{WR}$. Data will be valid approximately 800ns following $\overline{WR}$'s rising edge.

Other Interface Considerations

In order to maintain conversion accuracy, $\overline{WR}$ has a maximum width spec of 50µs. When the MS flash ADC's sampled data comparators are in comparison mode ($\overline{WR}$ is Low), the input capacitors (C, Figure 5) must hold their charge. Switch leakage can cause errors if the comparator is left in this phase for too long.

Since the MS flash ADC enters its zeroing phase at the end of a conversion, a new conversion cannot be started until this phase is complete. The minimum spec for this time is 500ns (t_P in Figures 1, 2, 3a, and 3b).

ANALOG CONSIDERATIONS

Reference and Input

The two V_{REF} inputs of the ADC0820 are fully differential and define the zero- to full-scale input range of the A/D converter. This allows the designer to easily vary the span of the analog input since this range will be equivalent to the voltage difference between $V_{IN}(+)$ and $V_{IN}(-)$. By reducing $V_{REF}(V_{REF}=V_{REF}(+) - V_{REF}(-))$ to less than 5V, the sensitivity of the converter can be increased (i.e., if V_{REF}=2V, then 1 LSB=7.8mV). The input/reference arrangement also facilitates ratiometric operation and, in many cases, the chip power supply can be used for transducer power as well as the V_{REF} source.

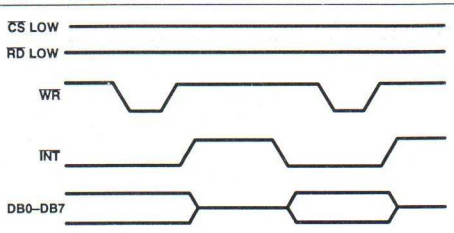


Figure 7. WR-RD Mode (Pin 7 is High) Stand-Alone Operation

This reference flexibility lets the input span not only be varied, but also offset from zero. The voltage at $V_{REF}(-)$ sets the input level which produces a digital output of all zeroes. Though V_{IN} is not itself differential, the reference design affords nearly differential-input capability for most measurement applications. Figure 9 shows some of the configurations that are possible.

Input Current

Due to the unique conversion techniques employed by the ADC0820, the analog input behaves somewhat differently than in conventional devices. The A/D's sampled data comparators take varying amounts of input current depending on which cycle the conversion is in.

The equivalent input circuit of the ADC0820 is shown in Figure 10a. When a conversion starts ($\overline{WR}$ Low, WR-RD mode), all input switches close, connecting V_{IN} to 31 1pF capacitors. Although the two 4-bit flash circuits are not both in their compare cycle at the same time, V_{IN} still sees all input capacitors at once. This is because the MS flash converter is connected to the input during its compare interval and the LS flash is connected to the input during its zeroing phase. In other words, the LS ADC uses V_{IN} as its zero-phase input.

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 5kΩ to 10kΩ). In addition, about 12pF of input stray capacitance must also be charged. For large source resistances, the analog input can be modeled as an RC network as shown in Figure 10b. As R_S increases, it will take longer for the input capacitance to charge.

In RD mode, the input switches are closed for approximately 800ns at the start of the conversion. In WR-RD mode, the time that the switches are closed to allow this charging is the time that $\overline{WR}$ is Low. Since other factors force this time to be at least 600ns, input time constants of 100ns can be accommodated without special consideration. Typical total input capacitance values of 45pF allow R_S to be 1.5kΩ without lengthening $\overline{WR}$ to give V_{IN} more time to settle.

Input Filtering

It should be made clear that transients in the analog input signal, caused by charging current flowing into V_{IN}, will not degrade the A/D's performance in most cases. In effect, the ADC0820 does not "look" at the input when these transients occur. The comparators' outputs are not latched while $\overline{WR}$ is Low, so at least 600ns will be provided to charge the ADC's input capacitance. It is

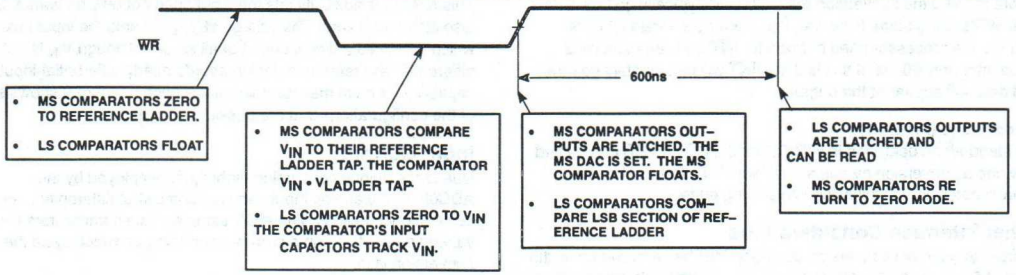
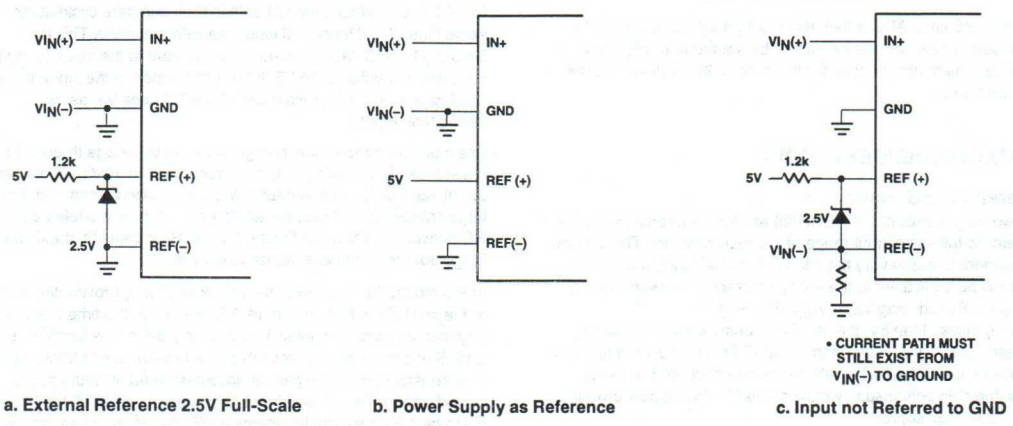


Figure 8. Operating Sequence (WR-RD Mode)



a. External Reference 2.5V Full-Scale

b. Power Supply as Reference

c. Input not Referred to GND

Figure 9. Analog Input Options

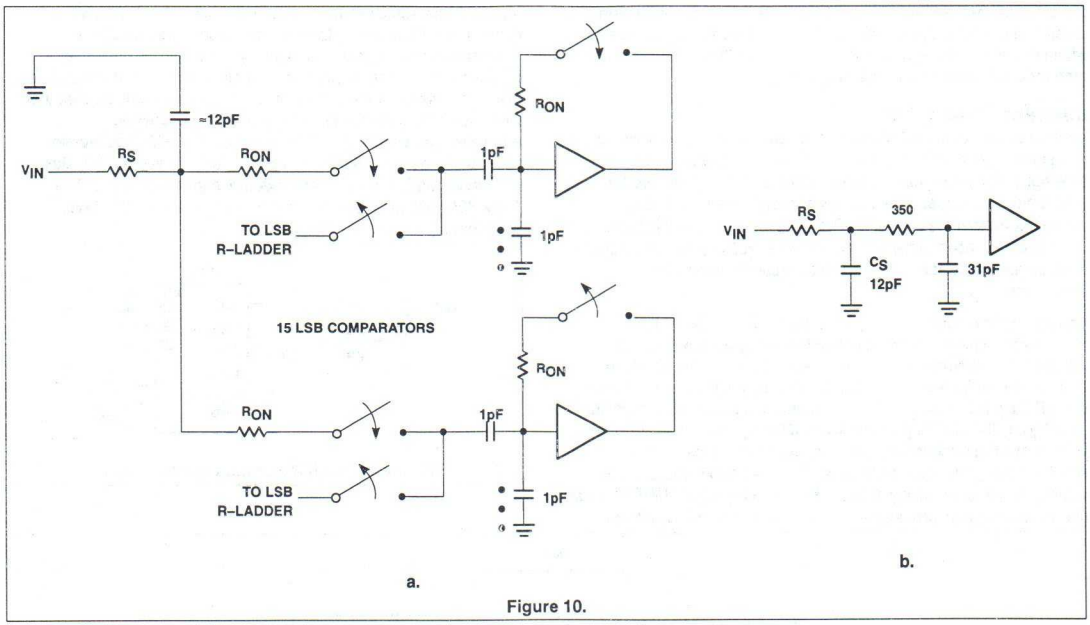

≈12pF
RS
VIN
RON
1pF
TO LSB
R-LADDER
15 LSB COMPARATORS
a.
350
CS
12pF
31pF
b.

Figure 10.

therefore not necessary to filter out these transients by putting an external cap on the V_{IN} terminal, if an input amplifier that can settle within 600ns is used to drive the input. The NE530 is a suitable op amp for driving the input of the ADC0820.

Inherent Sample-Hold

Another benefit of the ADC0820's input mechanism is its ability to measure a variety of high-speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain at least 1/2LSB stable throughout the conversion process if full accuracy is to be maintained. Consequently, for many high-speed signals, this signal must be externally sampled, and held stationary during the conversion.

Sampled data comparators, by nature of their input switching, already accomplish this function to a large degree (Section 1.2). Although the conversion time for the ADC0820 is 1.5µs, the time through which V_{IN} must be 1/2LSB stable is much smaller. Since the MS flash ADC uses V_{IN} as its "compare" input and the LS ADC uses V_{IN} as its "zero" input, the ADC0820 only "samples" V_{IN} when $\overline{WR}$ is Low. Even though the two flashes are not done simultaneously, the analog signal is measured at one instant. The value of V_{IN} approximately 100ns after the rising edge of $\overline{WR}$ (100ns due to internal logic propagation delay) will be the measured value.

Input signals with slew rates typically below 100mV/µs can be converted without error. However, because of the input time constants, and charge injection through the opened comparator input switches, faster signals may cause errors. Still, the ADC0820's loss in accuracy for a given increase in signal slope is far less than what would be witnessed in a conventional successive approximation device. An SAR type converter with a conversion time as fast as 1µs would still not be able to measure a 5V, 1kHz sine wave without the aid of an external sample-and-hold. The ADC0820, with no such help, can typically measure 5V, 7kHz waveforms.

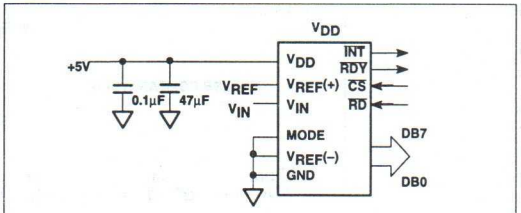


Figure 11. 8-Bit Resolution Configuration

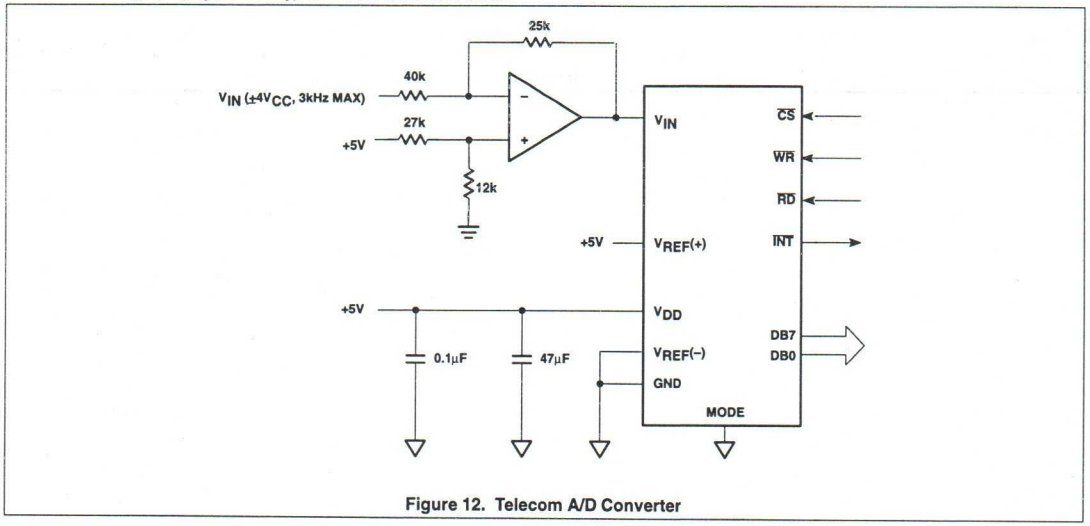


Figure 12. Telecom A/D Converter

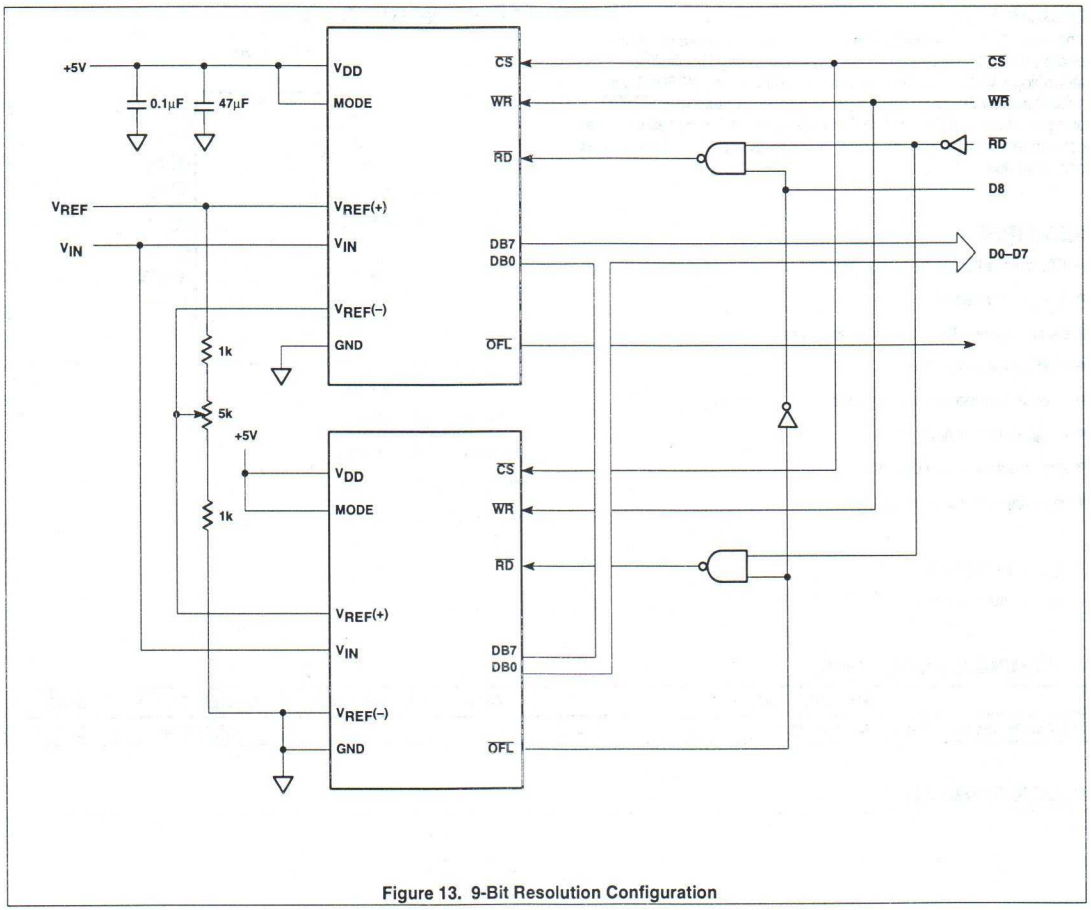


Figure 13. 9-Bit Resolution Configuration

6-Bit A/D converter (parallel outputs) NE5037

DESCRIPTION

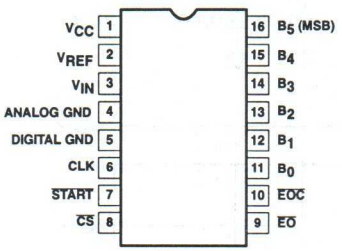
The NE5037 is a low cost, complete successive-approximation analog-to-digital (A/D) converter, fabricated using Bipolar/I^2L technology. With an external reference voltage, the NE5037 will accept input voltages between 0V and V_{REF}. An external $\overline{START}$ pulse of at least 300ns in duration will provide the 6-bit result of the conversion in parallel format. Full conversion with no missing codes occurs in 9µs.

FEATURES

- TTL-compatible inputs and outputs
- 3-State output buffer
- Easy interface to CMOS microprocessors
- Fast conversion—9µs
- Guaranteed no missing codes over full temp range
- Single-supply operation, +5V
- Positive true binary outputs
- High-impedance analog inputs

PIN CONFIGURATION

N Package



TOP VIEW

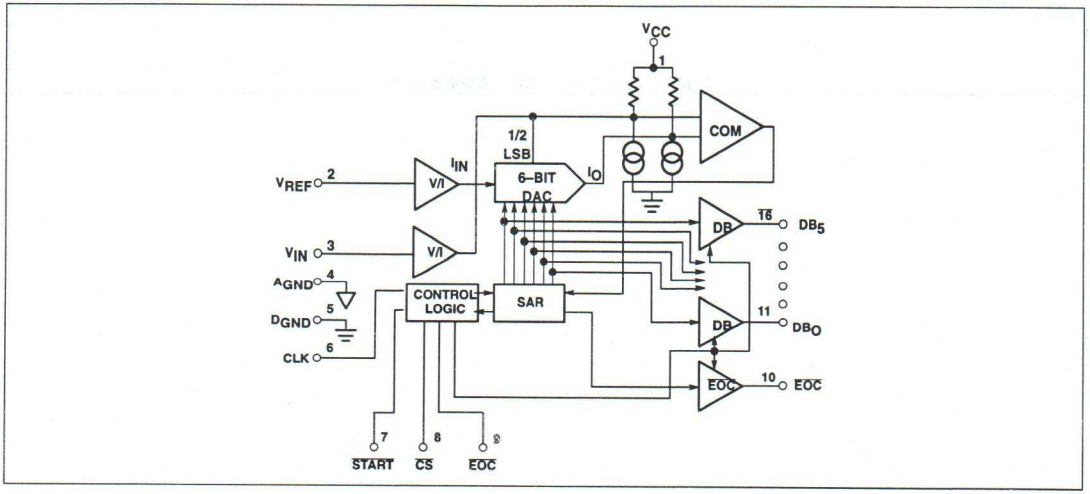
APPLICATIONS

- Temperature control
- µP-based appliances
- Light level monitors
- Head position sensing
- Electronic toys
- Joystick interface

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5037N	0406C

BLOCK DIAGRAM



6-Bit A/D converter (parallel outputs) NE5037

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	7	V
V_{REF}	Reference voltage	7	V
$V_{IN(Analog)}$	Analog input voltage	7	V
$V_{IN(Digital)}$	Digital input voltage ($\overline{CS}$, $\overline{OE}$, $\overline{START}$, CLK)	7	V
D_{OUT}	Data outputs (DB0 to DB5)		
	3-state mode	7	V
	Enabled mode (each output)	5	mA
$\overline{EOC}$	End of conversion	V_{CC}	
Δ_{GND}	Analog GND to digital GND	±1	V
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature range	-65 to 150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C
P_D	Maximum power dissipation, T_A=25°C (still-air)[1]		
	N package	1450	mW

NOTES:
1. Derate above 25°C at the following rates:
   N package=11.6mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{CC}=5.0V; V_{REF}=2.0V; Clock=1MHz; 0°C ≤ T_A ≤ 70°C unless otherwise specified. Typical values are specified at 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution		6	6	6	Bits
	Relative accuracy[1,2]			1/4	1/2	LSB
V_{CC}	Positive supply voltage		+4.75	+5.0	+5.50	V
ε_{FS}	Full-scale gain error[2,3,4]	V_{REF}=2.0V, T_A=25°C		±1	±2	LSB
ε_{ZS}	Zero-scale offset error[2]	V_{REF}=2.0V, T_A=25°C		±1/2	-1/2, +2	LSB
PSR	Power supply rejection, Max change in full-scale[2]	V_{REF}=2.0V, 4.75V≤V_{CC}≤5.5V		±1/2	±1	LSB
I_{IN}	Analog input bias current	0≤V_{IN}≤2.5V		1	10	µA
I_{REF}	Reference bias current	0≤V_{REF}≤2.5V		1	10	µA
R_{IN}	Analog input resistance		3	30		MΩ
V_{IH}	Logic "1' input voltage		2.0			V
V_{IL}	Logic "0' input voltage				0.8	V
I_{IH}	Logic "1' input current				10	µA
I_{IL}	Logic "0' input current			1	10	µA
I_{OH}	Logic "1' output current[5]	2.4V≤V_{OH}	300			µA
I_{OL}	Logic "0' output current[5]	V_{OL}≤0.4V	1.6			mA
I_{OZ}	3-State leakage current			±0.1	±40	µA
I_{CC}	Positive supply current			18	24	mA
P_D	Power dissipation				132	mW

NOTES:
1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on a straight line drawn from zero-scale to full-scale of the device.
2. Specifications given in LSBs refer to the weight of the least significant bit at the 6-bit level which is 1.56% of the full-scale voltage.
3. Full-scale gain error is the deviation of the full-scale code transition point (111110 to 111111) from its ideal value.
4. The analog input voltage (V_{IN}) range is 0V to V_{REF} nominally, with the output remaining at 111111 even though the input may increase from V_{REF} to V_{CC}. (For optimum performance, V_{REF} can be any value from 1.5V to 2.5V.)
5. The data outputs have active pull-ups. The $\overline{EOC}$ line is open-collector with a nominal 5kΩ internal pull-up resistor.

AC ELECTRICAL CHARACTERISTICS

V_{CC}=5.0V; V_{REF}=2.0V; Clock=1MHz; 0°C ≤ T_A ≤ 70°C unless otherwise specified. Typical values are specified at 25°C (Refer to AC test figures.)

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
f_{MAX}	Maximum clock frequency				1			MHz
t_W	Start pulse width				300			ns
	Minimum positive/negative clock pulse width				300			ns
t_{CONV}	Conversion time						9	Clock cycles
$t_{P\ (OUT\ DATA)}$	Propagation delay[1]	Data out	$\overline{OE}$	T_A=25°C t_R=t_F≤20ns			500	ns
$t_{P\ (OUT\ EOC)}$	Propagation delay[2]	$\overline{EOC}$	Clock	T_A=25°C t_R=t_F≤20ns			800	ns
$t_{P\ (3\text{-}STATE)}$	Propagation delay, 3-State	3-State Data	$\overline{OE}$	T_A=25°C t_R=t_F≤20ns			500	ns

NOTES:
1. Propagation delay of data outputs is defined as the delay in the data outputs reading their final value after the low going edge of $\overline{OE}$.
2. Propagation delay of $\overline{EOC}$ is defined as the delay in $\overline{EOC}$ going low, following the low going edge of the 9th clock pulse after the start pulse.

CIRCUIT DESCRIPTION

NE5037 is a complete 6-bit, parallel output, microprocessor compatible, A/D converter which incorporates the successive-approximation method. The chip includes the internal control logic, the successive-approximation register (SAR), 6-bit DAC, comparator and output buffers. An externally-generated clock source (max frequency=1MHz) must be provided to Pin 6. An external reference voltage supplied to Pin 2 sets the full-scale range of the A/D converter.

The $\overline{CS}$ pin must be at a low level prior to the start of the conversion process. Upon receipt of a $\overline{START}$ pulse, the internal control logic resets the SAR. On the first low-going edge of the clock pulse, successive approximation conversion commences. Successive bits beginning with the MSB (D5) are supplied to the input of the internal 6-bit current output DAC by the I^2L successive approximation register.

The comparator determines whether the output current of the DAC is greater or less than the input current, which is converted from the unknown analog input voltage through the V/I converter. If the DAC output is greater, that bit of the DAC is set to "0' and the corresponding output buffer goes to "0' simultaneously. If it is less, it stays at '1' and the output buffer also stays at '1'. On successive clock pulses, successive bits of the DAC are tried and the corresponding output buffer represents the bits of the DAC. On the eighth low-going edge of the clock pulse (after the receipt of the start pulse), the $\overline{EOC}$ pin goes low, thereby indicating that the conversion is complete. The output data is now valid. In order to access the result of the conversion, the $\overline{OE}$ pin must be set to a low level. $\overline{EOC}$ is reset to a high state when $\overline{OE}$ is low. When $\overline{OE}$ is in a "1' state, the output buffers are in a high impedance state.

Refer to Figure 1 for the timing diagram.

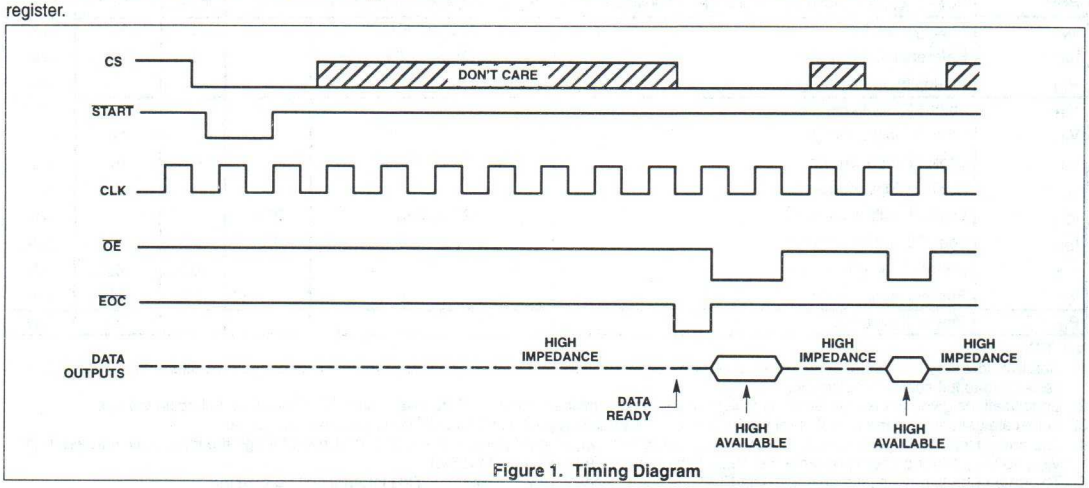


Figure 1. Timing Diagram

TRANSFER CHARACTERISTICS

The ideal transfer characteristic of the NE5037 is shown in Figure 2.

The NE5037 is designed to have a nominal LSB offset so that the code transition points are located LSB on either side of the exact analog inputs for a given code.

Thus the first transition (000000 to 000001) will occur at an input of LSB (15.63mV with a V_{REF} of 2.0V). Subsequent transitions will occur at nominal increments of 1 LSB. The last transition (to full-scale—111111) will occur at 62.5 LSB (1.953V at V_{REF} of 2.0V).

LAYOUT PRECAUTIONS

Analog ground (Pin 4) and digital ground (Pin 5) are not connected internally and should be connected together as close to the device as possible for optimum performance. The circuit will operate with as much as ±200mV between the two grounds but some degradation will occur. The leads to the analog inputs should be kept as short as possible to minimize noise pick-up. Input bypass capacitors from the analog inputs to ground will eliminate noise pick-up. Power supplies should be decoupled with at least 1µF located close to the device to minimize the effects of noise spikes.

The reference input and the analog voltage input must both remain stable during conversion to insure accuracy and proper operation. This can be done by adequately bypassing these inputs and/or keeping the impedance of these inputs at or below 2kΩ.

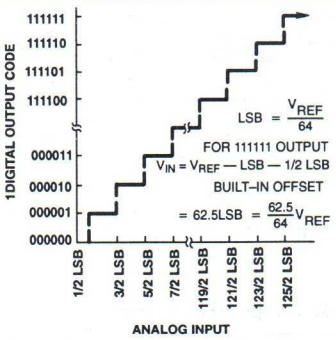
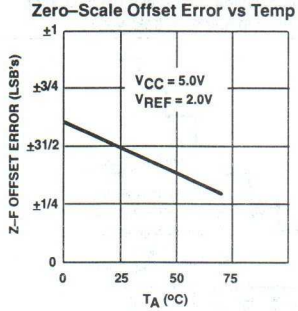


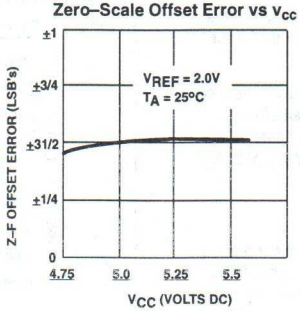
Figure 2. Ideal Transfer Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS

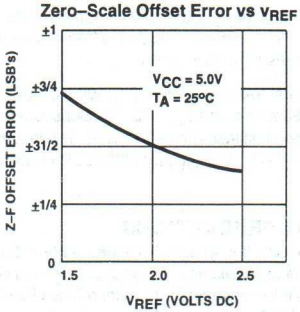
Zero–Scale Offset Error vs Temp



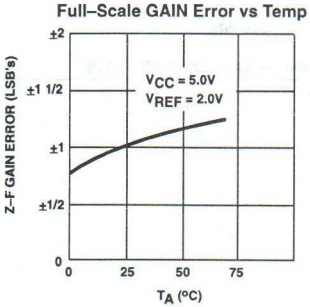
Zero–Scale Offset Error vs V_{CC}



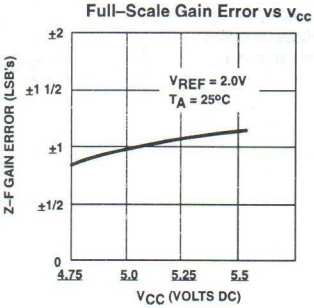
Zero–Scale Offset Error vs V_{REF}



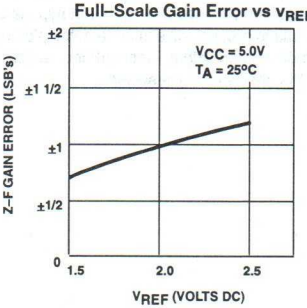
Full–Scale GAIN Error vs Temp



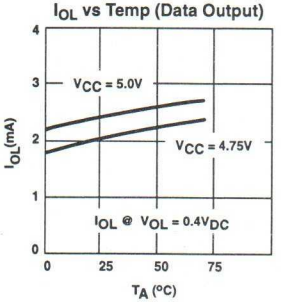
Full–Scale Gain Error vs V_{CC}



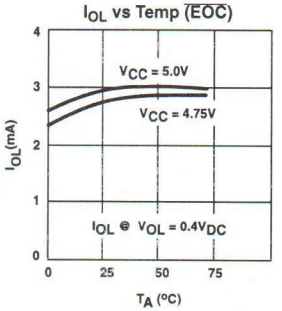
Full–Scale Gain Error vs V_{REF}



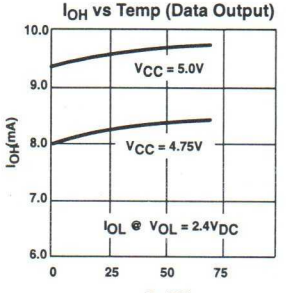
I_{OL} vs Temp (Data Output)



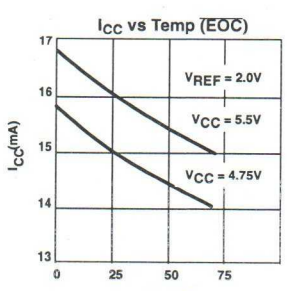
I_{OL} vs Temp ($\overline{EOC}$)



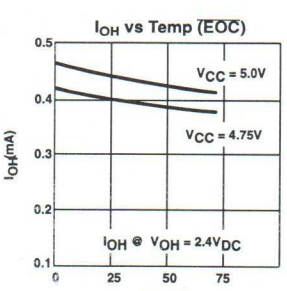
I_{OH} vs Temp (Data Output)



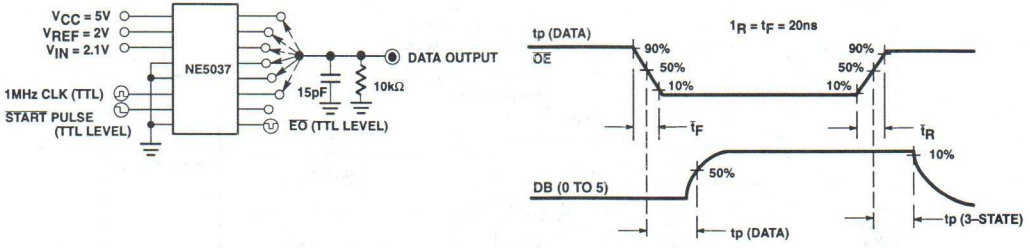
I_{CC} vs Temp ($\overline{EOC}$)



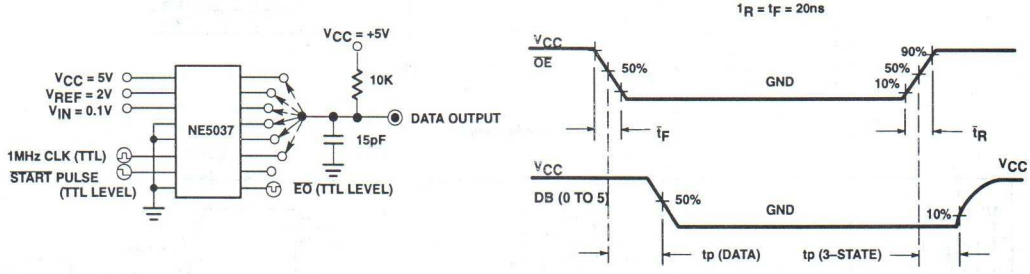
I_{OH} vs Temp ($\overline{EOC}$)



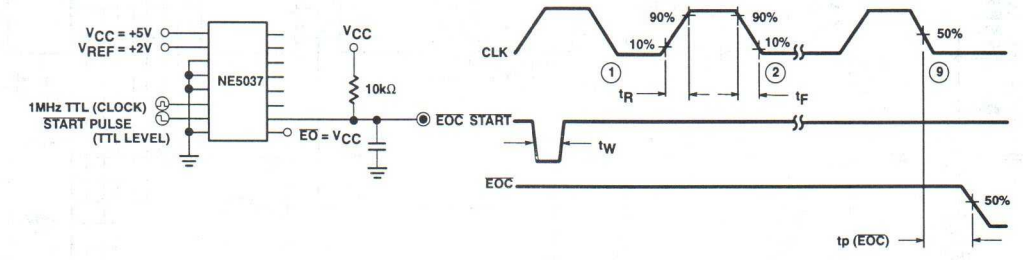
AC TEST CIRCUITS AND WAVEFORMS



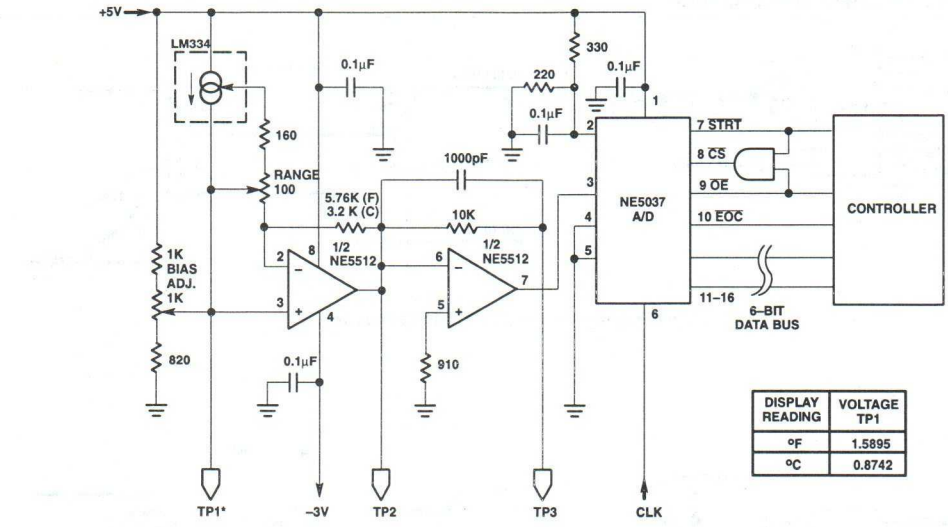
Propagation Delay Time t_P (DATA) and T_P (3-state)



Data Output High

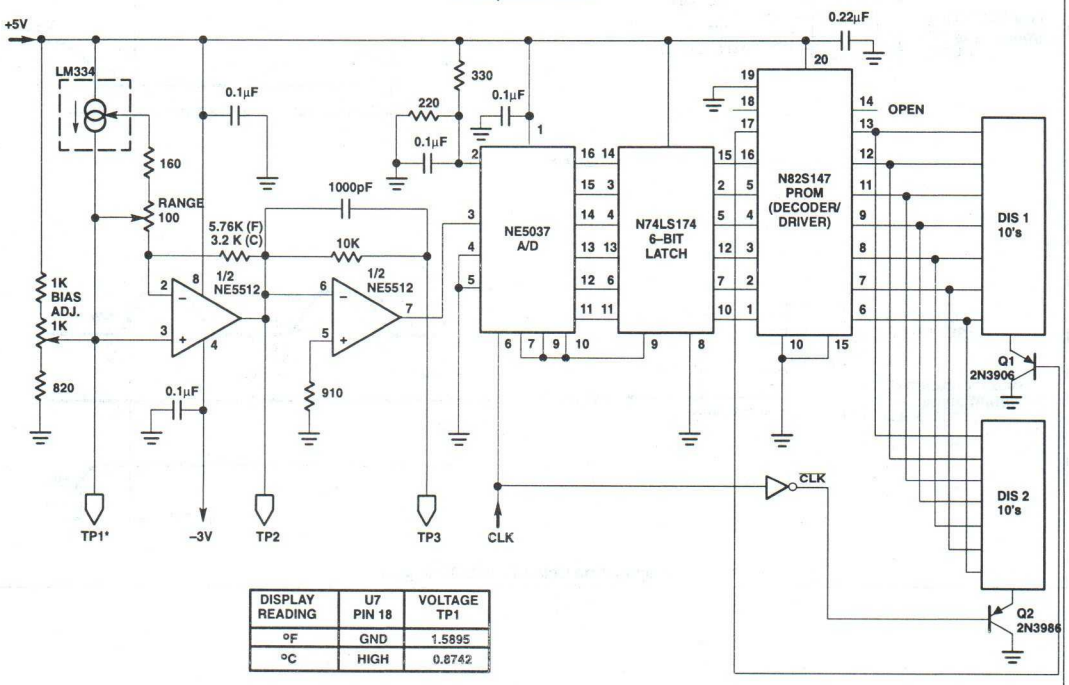


Propagation Delay Time EOC $t_{P(EOC)}$



DISPLAY READING	VOLTAGE TP1
°F	1.5895
°C	0.8742

a. Temperature Sensor



DISPLAY READING	U7 PIN 18	VOLTAGE TP1
°F	GND	1.5895
°C	HIGH	0.8742

b. Digital Thermometer

Figure 3.

6-Bit A/D converter (parallel outputs) NE5037

APPLICATION

- 0 to 63°C Temperature Sensor

CIRCUIT DESCRIPTION

The temperature sensor of Figure 3 provides an input to Pin 3 of the NE5037 of 32mV/°C. This 32mV is the value of one LSB for the NE5037. The LM334 is a three-terminal temperature sensor and provides a current of 1μA for each °Kelvin. The first section of the dual op amp is connected as a trans-impedance amplifier to convert the current from the LM334 to a voltage, which is amplified and inverted by the section amplifier. Note that the first amplifier requires different values of feedback resistance for °C and °F. The NE5512 was chosen for its low temperature coefficient of input bias current as excessive I_{OS} tempco would degrade temperature tracking.

To read temperature, conversion is started by sending a momentary low signal to Pin 7 of the NE5037. When Pin 10 of the NE5037 goes low, conversion is complete and a low is applied to Pin 9 of the NE5037 to read data on Pins 11 through 16. Note that this temperature data is in straight binary format.

The controller can be a microprocessor in a temperature control application, or discrete circuitry in a simple temperature reporting application. A temperature reporting (digital thermometer) circuit is shown in Figure 3b. The NE5037 A/D converter is connected in a continuous conversion mode by connecting together Pins 7, 9, and 10. Should this pin be momentarily shorted to any relatively low impedance point, conversion will stop. Conversion will resume upon interruption and restoration of the power. These pins are also connected to the latch enable of a 6-bit latch because the data at the converter output is available for only a short time when the converter is in the continuous conversion mode. The (P)ROM) must have the correct code for converting the data from the NE5037 (used as address for the (P)ROMs) to the appropriate segment drive codes. Note that the circuit of Figure 3b shows a circuit which can be used to display either Fahrenheit or Centigrade temperatures.

The displayed output could easily be converted to degrees Fahrenheit (°F) by the controller of Figure 3a or through the (P)ROMs of Figure 3b. When doing this, a third (hundreds) digit (P)ROM and display will be needed for displaying temperatures above 99°F.

An inexpensive clock can be made from NAND gates or inverters, as shown in Figure 3c.

CIRCUIT ADJUSTMENT

The circuit should be at a known ambient temperature for a few minutes before making adjustments.

14. Adjust bias adjust potentiometer for the voltage indicated in the chart in Figure 3b.
15. With the circuit (or sensor U3, if it is remotely located) at a known temperature for 2 to 3 minutes, adjust range control for a correct reading on the displays.

This should provide an accuracy of ±3 counts (3° F or C). Higher accuracy may require NE5037 reference voltage regulation.

8-Bit A/D and D/A converter — PCF8591



GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I²C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I²C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I²C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I²C bus.

Features

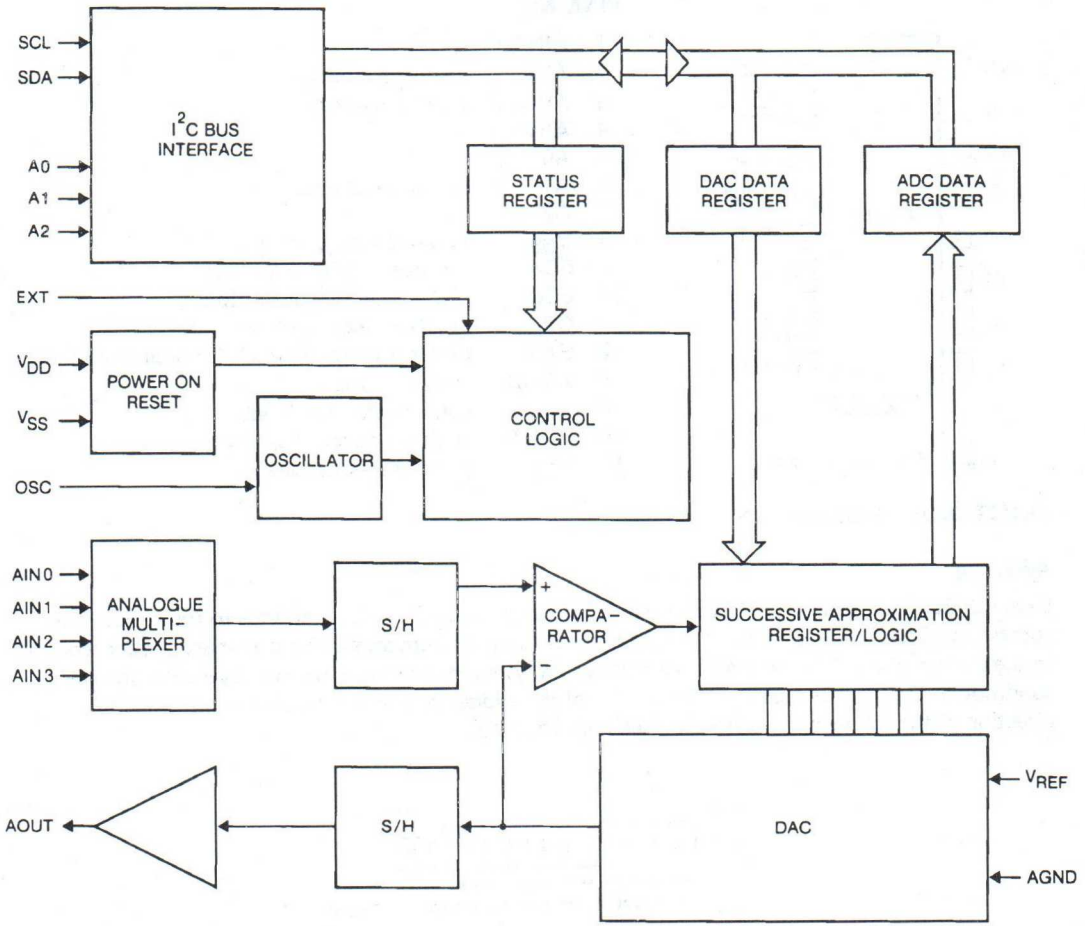
- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I²C bus
- Address by 3 hardware address pins
- Sampling rate given by I²C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT38).
PCF8591T:16-lead mini-pack; plastic (SO16L; SOT162A).


SCL
SDA
A0
A1
A2
I²C BUS INTERFACE
STATUS REGISTER
DAC DATA REGISTER
ADC DATA REGISTER
EXT
VDD
VSS
POWER ON RESET
OSCILLATOR
OSC
CONTROL LOGIC
AIN0
AIN1
AIN2
AIN3
ANALOGUE MULTI-PLEXER
S/H
+
−
COMPA-RATOR
SUCCESSIVE APPROXIMATION REGISTER/LOGIC
AOUT
S/H
DAC
VREF
AGND

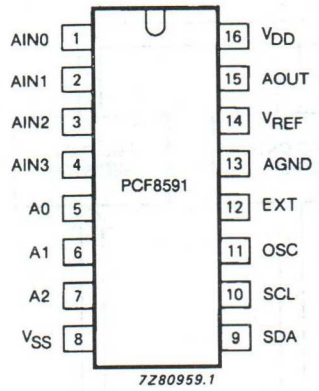


Fig. 2 Pinning diagram.

PINNING

1.	AIN0	analogue inputs (A/D converter)
2.	AIN1	
3.	AIN2	
4.	AIN3	
5.	A0	hardware address
6.	A1	
7.	A2	
8.	V_{SS}	negative supply voltage
9.	SDA	I^2C bus data input/output
10.	SCL	I^2C bus clock input/output
11.	OSC	oscillator input/output
12.	EXT	external/internal switch for oscillator input
13.	AGND	analogue ground
14.	V_{REF}	voltage reference input
15.	AOUT	analogue output (D/A converter)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Adressing

Each PCF8591 device in an I^2C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I^2C bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 3 and 10).

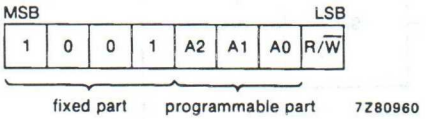


Fig. 3 Address byte.

Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analogue output, and for programming the analogue inputs as single-ended or differential inputs. The lower nibble selects one of the analogue input channels defined by the upper nibble (see Fig. 4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0 The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analogue output is switched to a high impedance state.

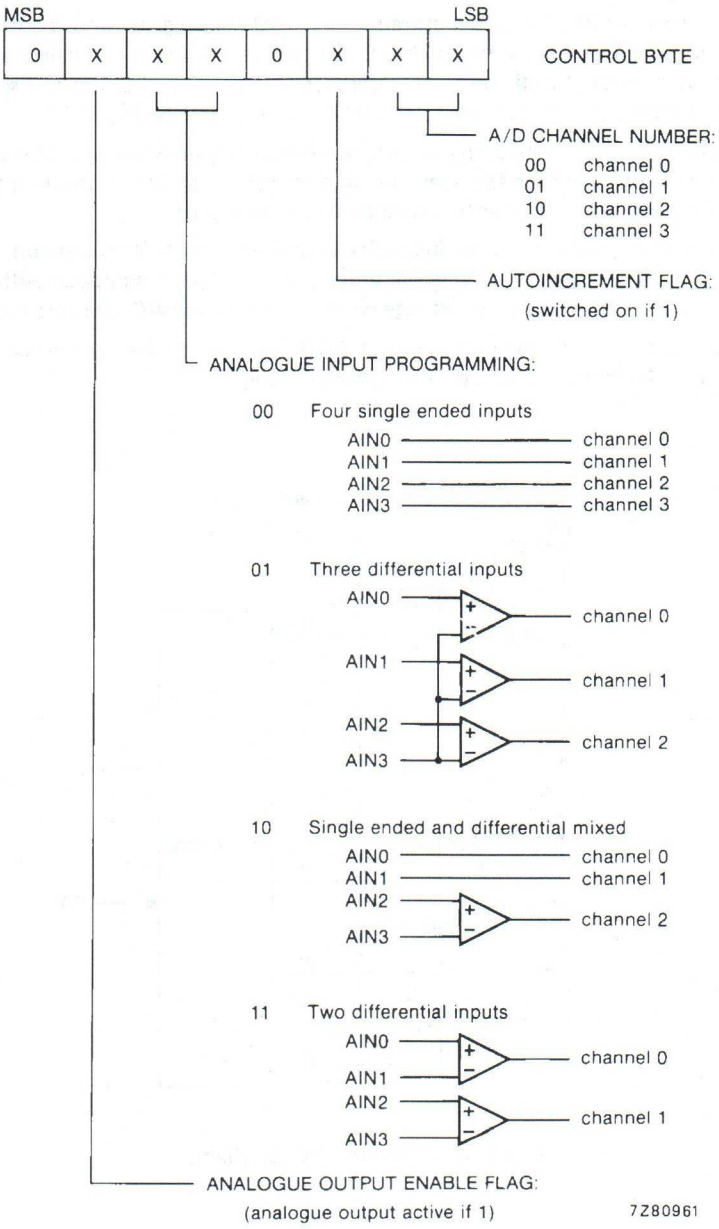


Fig. 4 Control byte.

D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analogue voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Fig. 5).

The analogue output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analogue output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analogue output AOUT is given by the formula shown in Fig. 6. The waveforms of a D/A conversion sequence are shown in Fig. 7.

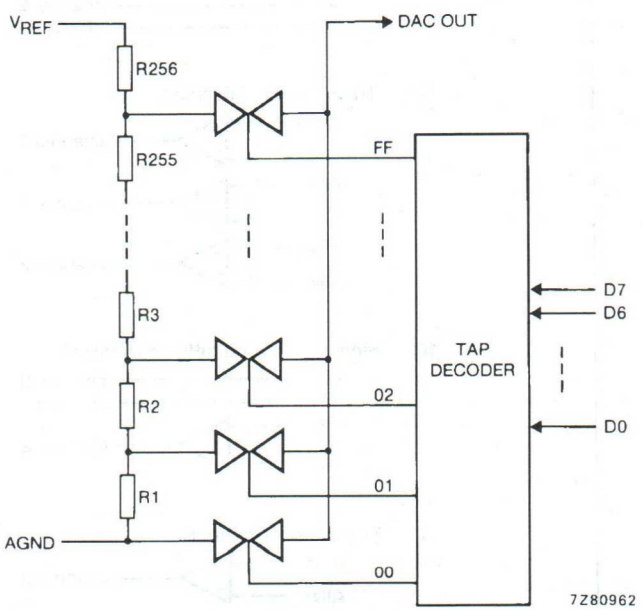


Fig. 5 DAC resistor divider chain.

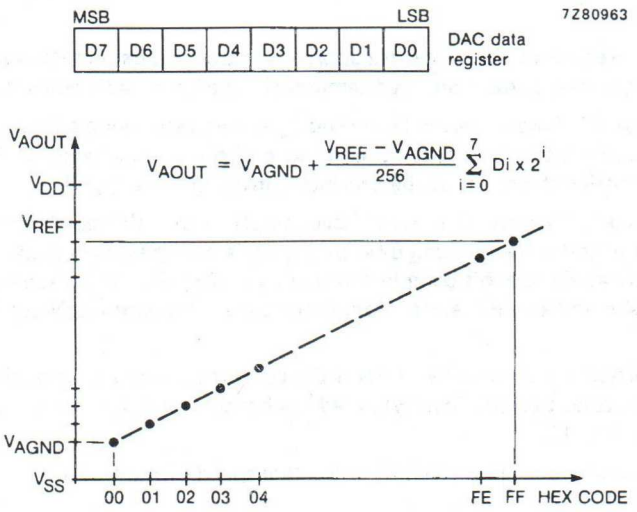


Fig. 6 DAC data and d.c. conversion characteristics.

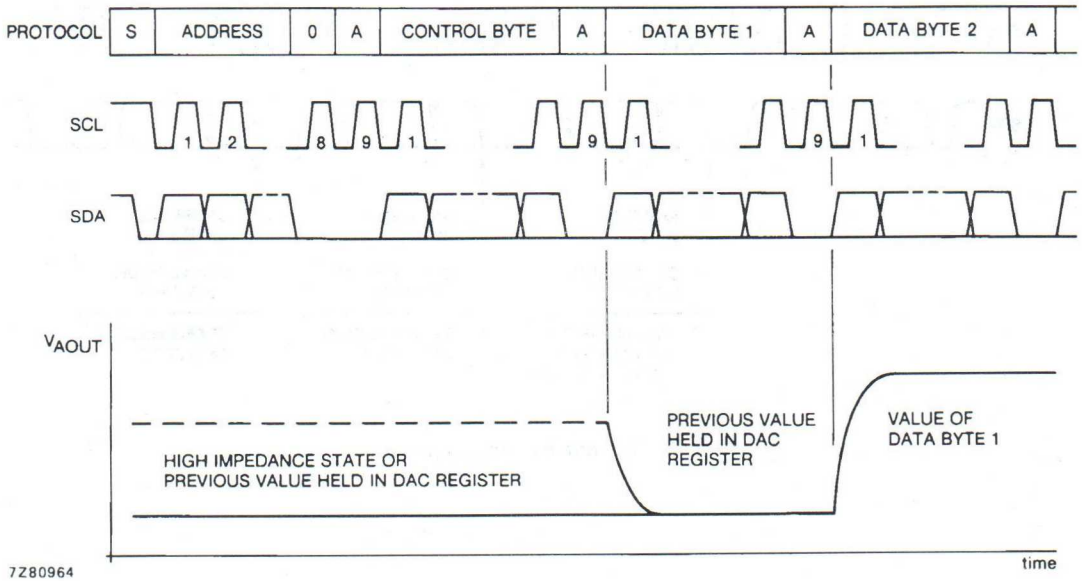


Fig. 7 D/A conversion sequence.

A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig. 8).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Fig. 9). The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle After a power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I^2C bus read cycle is shown in Fig. 10.

The maximum A/D conversion rate is given by the actual speed of the I^2C bus.

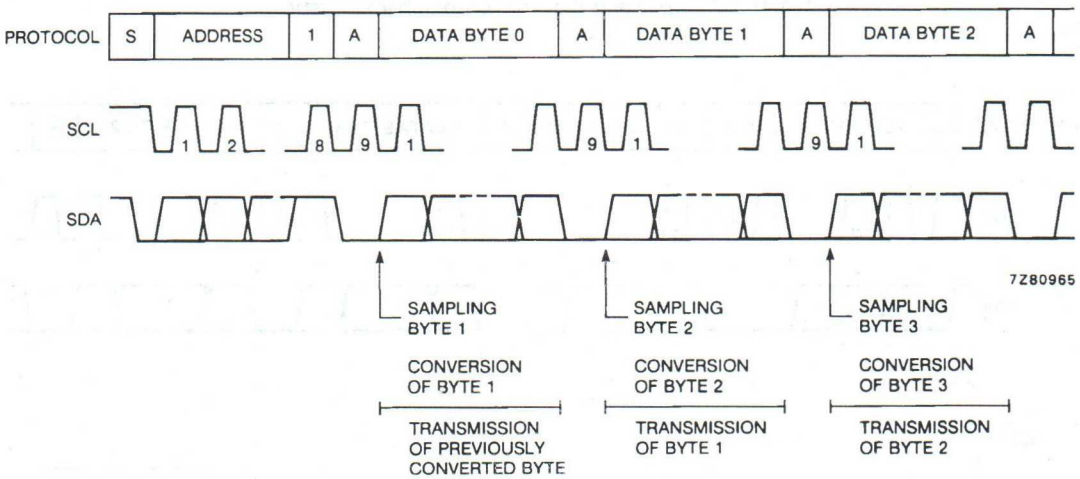


Fig. 8 A/D conversion sequence.

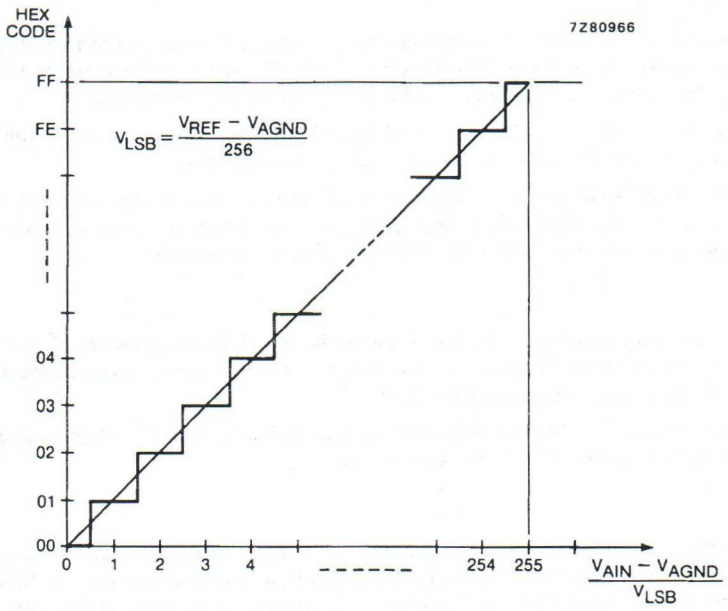


Fig. 9a A/D conversion characteristics of single-ended inputs.

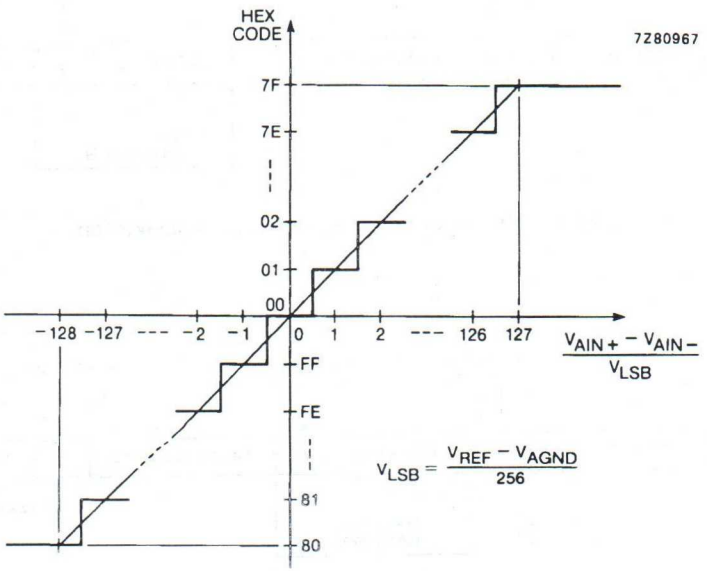


Fig. 9b A/D conversion characteristics of differential inputs.

REFERENCE VOLTAGE

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analogue ground and may have a d.c. off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Application Information and Fig. 6.

The A/D converter may also be used as a one or two quadrant analogue divider. The analogue input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high impedance state allowing the user to feed an external clock signal to OSC.

Bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I^2C bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

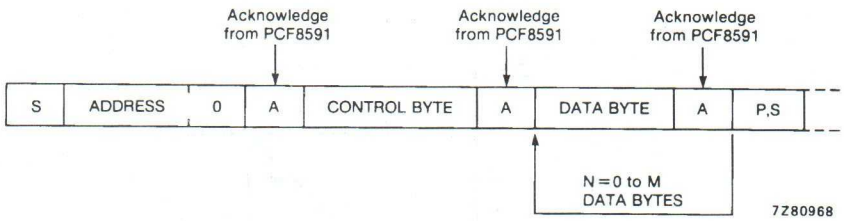


Fig. 10a Bus protocol for write mode, D/A conversion.

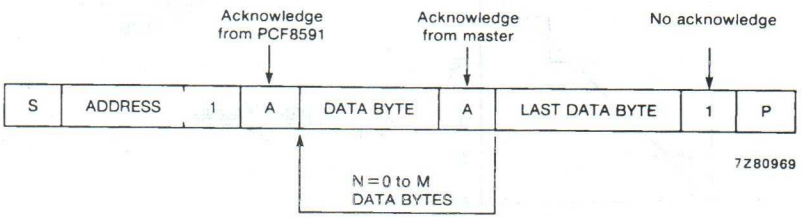


Fig. 10b Bus protocol for read mode, A/D conversion.

CHARACTERISTIVCS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transfered during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

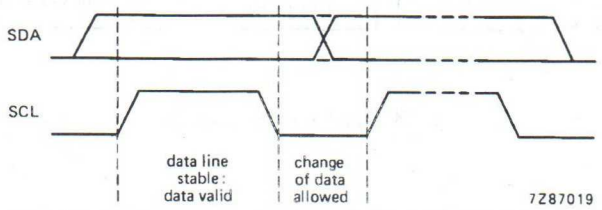


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

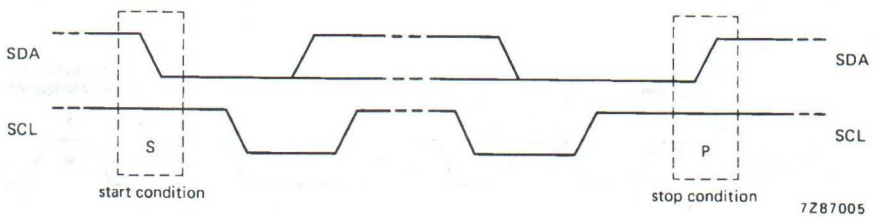


Fig. 12 Definition of start and stop condition.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

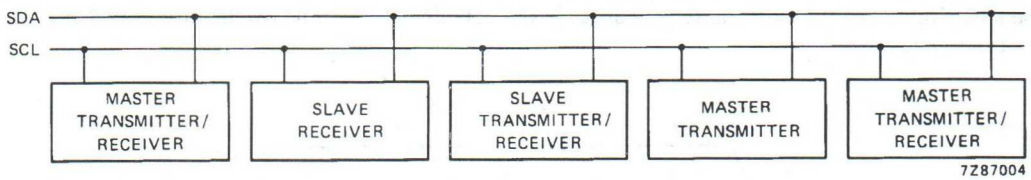


Fig. 13 System configuration.

Acknowledge.

The number of data bytes transfered between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

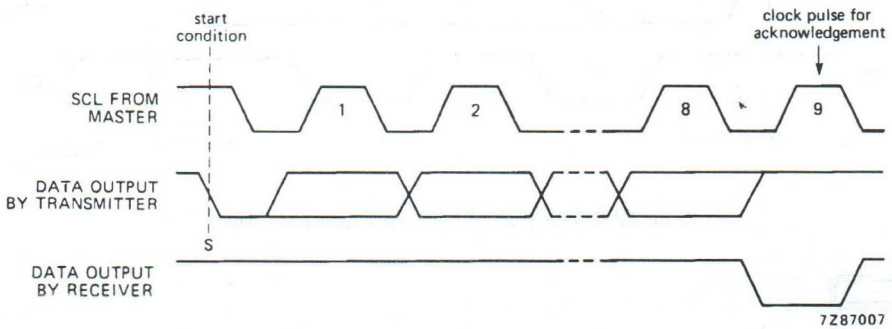


Fig. 14 Acknowledgement on the I^2C bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_R	–	–	1,0	μs
SCL and SDA fall time	t_F	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

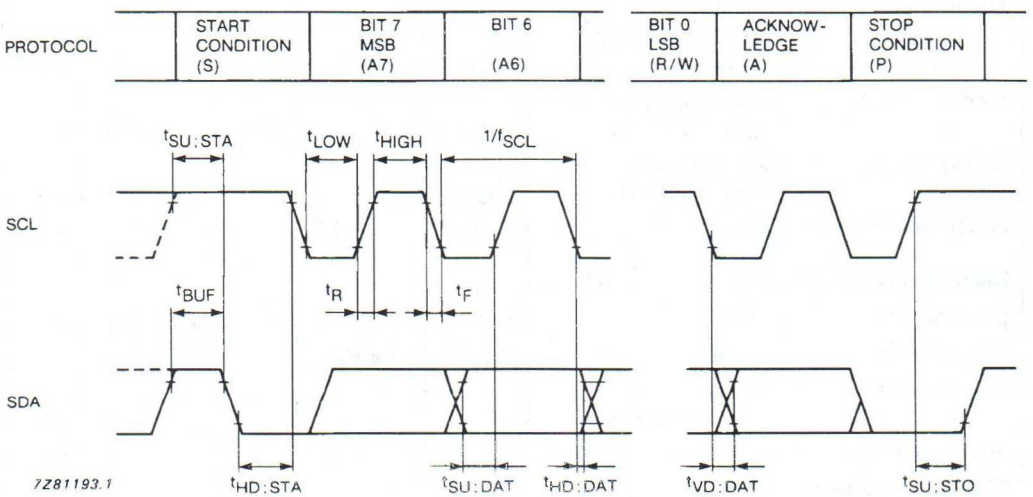


Fig. 15 I^2C bus timing diagram.

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to +8,0 V
Voltage on any pin	V_I		−0,5 to V_{DD} +0,5 V
Input current d.c.	I_I	max.	10 mA
Output current d.c.	I_O	max.	20 mA
V_{DD} or V_{SS} current	I_{DD}, I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	100 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Operating ambient temperature range	T_{amb}		−40 to +85 °C

Note:

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{DD}	2,5	–	6,0	V
Supply current	standby $V_I = V_{SS}$ or V_{DD}; no load	I_{DD0}	–	1	15	μA
Supply current	operating; AOUT off; f_{SCL} = 100 kHz	I_{DD1}	–	125	250	μA
Supply current	AOUT active; f_{SCL} = 100 kHz	I_{DD2}	–	0,45	1,0	mA
Power-on reset level	note 1	V_{POR}	0,8	–	2,0	V
Digital inputs/output	SCL, SDA, A0, A1, A2					
Input voltage	LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage	HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input current	leakage; $V_I = V_{SS}$ to V_{DD}	I_I	–	–	250	nA
Input capacitance		C_I	–	–	5	pF
SDA output current	leakage; HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
SDA output current	LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Reference voltage inputs						
Voltage range*	$V_{REF} > V_{AGND}$	V_{REF}	$V_{SS}+1,6$	–	V_{DD}	V
Voltage range*	$V_{REF} > V_{AGND}$	V_{AGND}	V_{SS}	–	$V_{DD}-0,8$	V
Input current	leakage	I_I	–	–	250	nA
Input resistance	V_{REF} to AGND	R_{REF}	–	100	–	kΩ
Oscillator	OSC, EXT					
Input current	leakage	I_I	–	–	250	nA
Oscillator frequency		f_{OSC}	0,75	–	1,25	MHz

D/A CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{load} = 10 kΩ; C_{load} = 100 pF; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output						
Output voltage range	no resistive load	V_{OA}	V_{SS}	–	V_{DD}	V
Output voltage range	R_{load} = 10 kΩ	V_{OA}	V_{SS}	–	$0,9 \times V_{DD}$	V
Output current	leakage; AOUT disabled	I_{LO}	–	–	250	nA
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	50	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error	no resistive load	G_e	–	–	1	%
Settling time	to ½ LSB full scale step	t_{DAC}	–	–	90	μs
Conversion rate		f_{DAC}	–	–	11,1	kHz
Supply noise rejection	at f = 100 Hz; V_{DD} = 0,1 V_{PP}	SNRR	–	40	–	dB

* A further extension of the range is possible, if the following conditions are fulfilled:

$$\frac{V_{REF} + V_{AGND}}{2} \geqslant 0,8 \text{ V and } V_{DD} - \frac{V_{REF} + V_{AGND}}{2} \geqslant 0,4 \text{ V}.$$

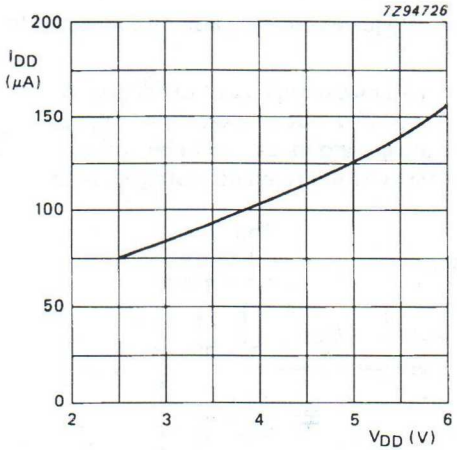
A/D CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{source} = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified

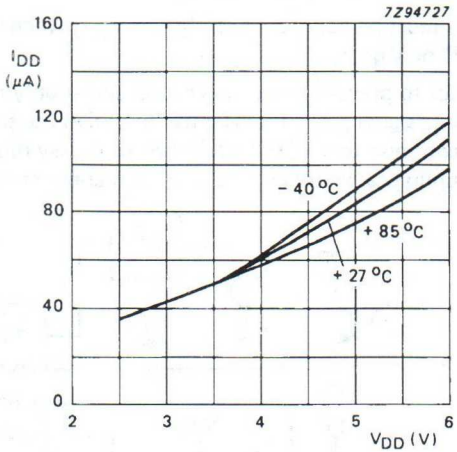
parameter	conditions	symbol	min.	typ.	max.	unit
Analogue inputs						
Input voltage range		V_{IA}	V_{SS}	–	V_{DD}	V
Input current	leakage	I_{IA}	–	–	100	nA
Input capacitance		C_{IA}	–	10	–	pF
Input capacitance	differential	C_{ID}	–	10	–	pF
Single-ended voltage	measuring range	V_{IS}	V_{AGND}	–	V_{REF}	V
Differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	V_{ID}	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	20	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error		G_e	–	–	1	%
Gain error	small-signal; ΔV_{IN} = 16 LSB	GS_e	–	–	5	%
Rejection ratio	common-mode	CMRR	–	60	–	dB
Supply noise rejection	at f = 100 Hz; $V_{DDN} = 0{,}1 \times V_{PP}$	SNRR	–	40	–	dB
Conversion time		t_{ADC}	–	–	90	μs
Sampling/conversion rate		f_{ADC}	–	–	11,1	kHz

Note

1. The power on reset circuit resets the I^2C bus logic when V_{DD} is less than V_{POR}.

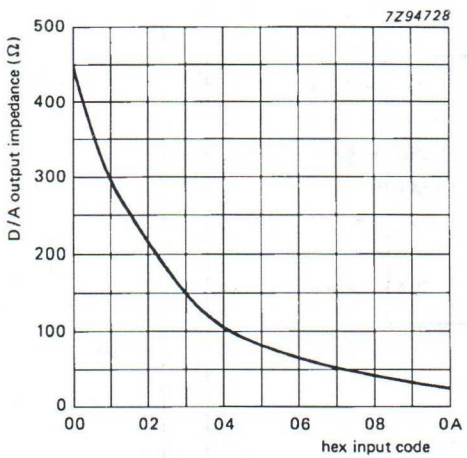


(a) internal oscillator; T_{amb} = + 27 °C.

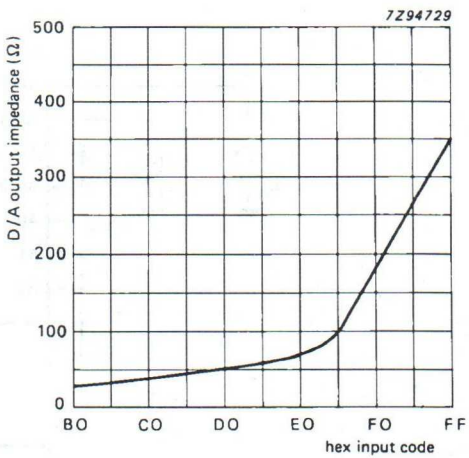


(b) external oscillator.

Fig. 16 Operating supply current against supply voltage (analogue output disabled).



(a) output impedance near negative power rail; T_{amb} = + 27 °C.



(b) output impedance near positive power rail; T_{amb} = + 27 °C.

Fig. 17 Output impedance of analogue output buffer (near power rails).

The x-axis represents the hex input-code equivalent of the output voltage.

APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analogue inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analogue signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors (> 10 μF) are recommended for power supply and reference voltage inputs.

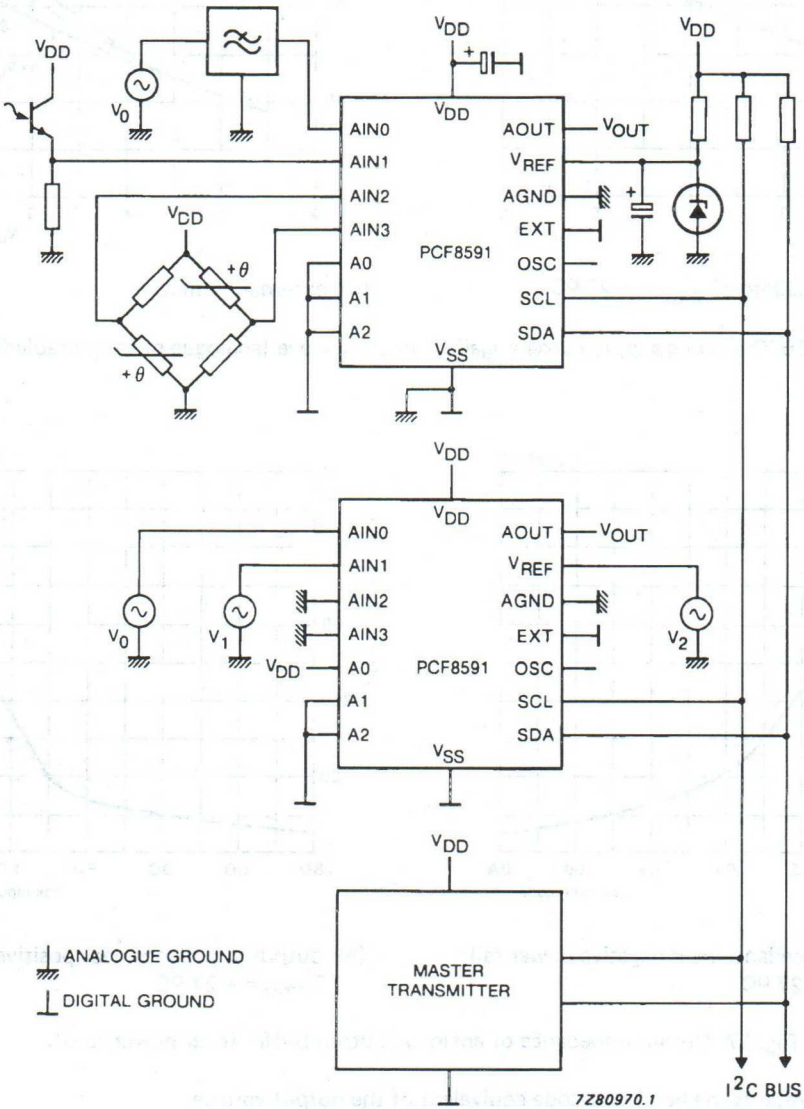


Fig. 18 Application diagram.

8-bit high-speed analog-to-digital converter

TDA8703

FEATURES

- 8-bit resolution
- Sampling rate up to 40 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.1 effective bits at 4.43 MHz full-scale input)
- Binary or two's complement 3-state TTL outputs
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Internal reference voltage generator
- Power dissipation only 290 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

- General purpose high-speed analog-to-digital conversion
- Digital TV, IDTV
- Subscriber TV decoder
- Satellite TV decoders
- Digital VCR.

GENERAL DESCRIPTION

The TDA8703 is an 8-bit high-speed analog-to-digital converter (ADC) for video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are TTL compatible, although a low-level AC clock input signal is allowed.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8703	24	DIL	plastic	SOT101
TDA8703T	24	SO24	plastic	SOT137A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output stages supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	28	36	mA
I_{CCD}	digital supply current		–	19	25	mA
I_{CCO}	output stages supply current		–	11	14	mA
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
AILE	AC integral linearity error	note 1	–	–	±2	LSB
B	–3 dB bandwidth	note 2; f_{CLK} = 40 MHz	–	19.5	–	MHz
$f_{CLK}/f_{\overline{CLK}}$	maximum conversion rate	note 3	40	–	–	MHz
P_{tot}	total power dissipation		–	290	415	mW

Notes

1. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}; $f_{\overline{CLK}}$ = 27 MHz).
2. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at input).
3. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.
   - If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

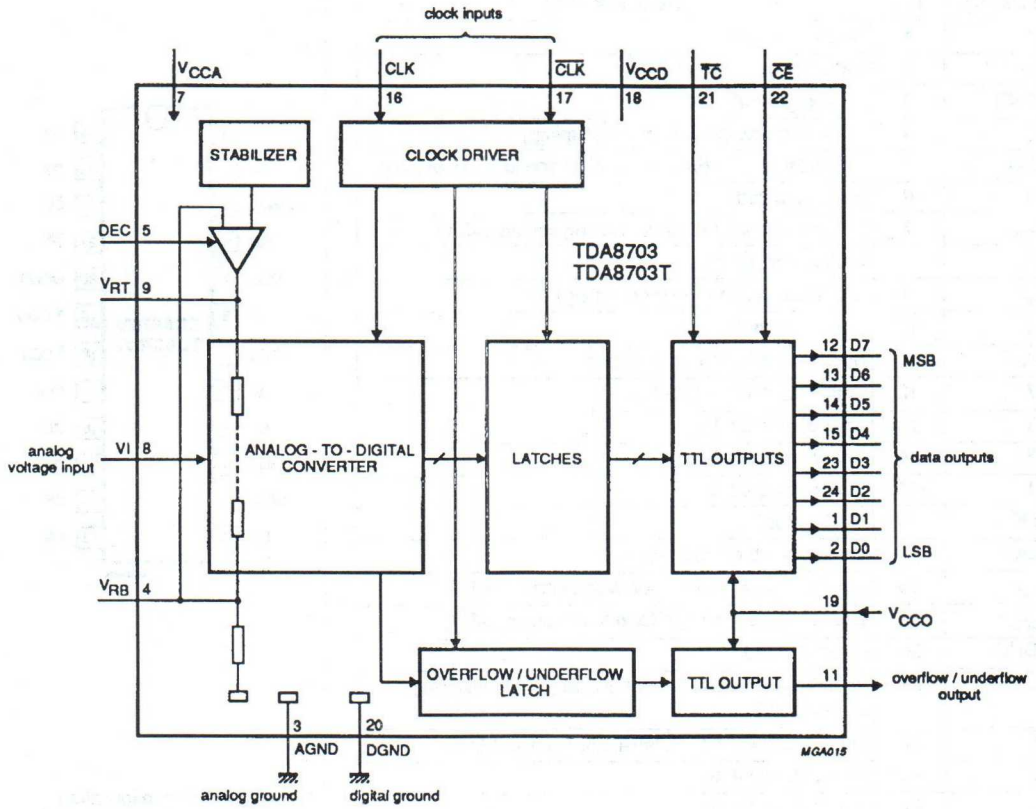


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output; bit 1
D0	2	data output; bit 0 (LSB)
AGND	3	analog ground
V_{RB}	4	reference voltage bottom (decoupling)
DEC	5	decoupling input (internal stabilization loop decoupling)
n.c.	6	not connected
V_{CCA}	7	positive supply voltage for analog circuits (+5 V)
VI	8	analog voltage input
V_{RT}	9	reference voltage top (decoupling)
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output; bit 7 (MSB)
D6	13	data output; bit 6
D5	14	data output; bit 5
D4	15	data output; bit 4
CLK	16	clock input
$\overline{CLK}$	17	complementary clock input
V_{CCD}	18	positive supply voltage for digital circuits (+5 V)
V_{CCO}	19	positive supply voltage for output stages (+5 V)
DGND	20	digital ground
$\overline{TC}$	21	input for two's complement output (TTL level input, active LOW)
$\overline{CE}$	22	chip enable input (TTL level input, active LOW)
D3	23	data output; bit 3
D2	24	data output; bit 2

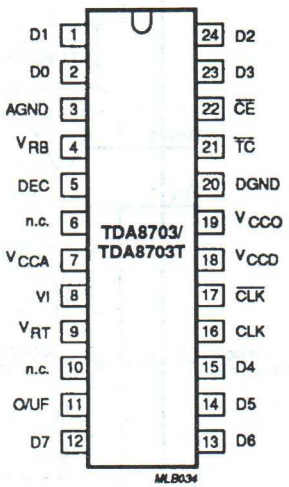


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage		−0.3	7.0	V
V_{CCD}	digital supply voltage		−0.3	7.0	V
V_{CCO}	output stages supply voltage		−0.3	7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCO} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCA} - V_{CCO}$	supply voltage differences		−1.0	1.0	V
V_{VI}	input voltage range	referenced to AGND	−0.3	7.0	V
$V_{CLK}/V_{\overline{CLK}}$	AC input voltage for switching (peak-to-peak value)	note 1; referenced to DGND	−	2.0	V
I_O	output current		−	+10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+125	°C

Note

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition. If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT101	55 K/W
	SOT137A	75 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{CCA} = V_7 - V_3 = 4.5$ V to 5.5 V; $V_{CCD} = V_{18} - V_{20} = 4.5$ V to 5.5 V; $V_{CCO} = V_{19} - V_{20} = 4.5$ V to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $T_{amb} = 0$ °C to +70 °C; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V and $T_{amb} = 25$ °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output stages supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	28	36	mA
I_{CCD}	digital supply current		–	19	25	mA
I_{CCO}	output stage supply current	all outputs LOW	–	11	14	mA
Inputs						
Clock input $\overline{CLK}$ and CLK (note 1; referenced to DGND)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{CLK}/V_{\overline{CLK}} = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_{CLK}/V_{\overline{CLK}} = 0.4$ V	–	–	100	µA
		$V_{CLK}/V_{\overline{CLK}} = V_{CCD}$	–	–	300	µA
Z_i	input impedance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	–	4	–	kΩ
C_i	input capacitance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	–	4.5	–	pF
$V_{CLK} - V_{\overline{CLK}}$	AC input voltage for switching (peak-to-peak value)	note 1; DC level = 1.5 V	0.5	–	2.0	V
$\overline{TC}$ and $\overline{CE}$ (referenced to DGND)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{IL} = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_{IH} = 2.7$ V	–	–	20	µA
VI (analog input voltage referenced to AGND)						
$V_{VI(B)}$	input voltage (bottom)		1.33	1.41	1.48	V
$V_{VI(0)}$	input voltage	output code = 0	1.455	1.55	1.635	V
$V_{OS(B)}$	offset voltage (bottom)	$V_{VI(0)} - V_{VI(B)}$	0.125	–	0.155	V
$V_{VI(T)}$	input voltage (top)		3.2	3.36	3.5	V
$V_{VI(255)}$	input voltage	output code = 255	3.115	3.26	3.385	V
$V_{OS(T)}$	offset voltage (top)	$V_{VI(T)} - V_{VI(255)}$	0.085	–	0.115	V
$V_{VI(P-P)}$	input voltage amplitude (peak-to-peak value)		1.66	1.71	1.75	V
I_{IL}	LOW level input current	$V_{VI} = 1.4$ V	–	0	–	µA
I_{IH}	HIGH level input current	$V_{VI} = 3.6$ V	60	120	180	µA
Z_i	input impedance	$f_i = 1$ MHz	–	10	–	kΩ
C_i	input capacitance	$f_i = 1$ MHz	–	14	–	pF

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference resistance						
R_{ref}	reference resistance	V_{RT} to V_{RB}	–	220	–	Ω
Outputs						
Digital outputs (D7 - D0) (referenced to DGND)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = −0.4 mA	2.7	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	−20	–	+20	µA
Switching characteristics (note 2; see Fig.3)						
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		40	–	–	MHz
Analog signal processing (f_{CLK} = 40 MHz)						
B	−3 dB bandwidth	note 3	–	19.5	–	MHz
G_d	differential gain	note 4	–	0.6	–	%
ϕ_d	differential phase	note 4	–	0.8	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43 MHz	–	−55	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	−28	−25	dB
SVRR2	supply voltage ripple rejection	note 5	–	1	2.5	%/V
Transfer function						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
AILE	AC integral linearity error	note 6	–	–	±2	LSB
EB	effective bits	f_i = 4.43 MHz	–	7.1	–	bits
Timing (note 7; see Figs 3 to 6; f_{CLK} = 40 MHz)						
t_{dS}	sampling delay		–	–	2	ns
t_{HD}	output hold time		6	–	–	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	–	8	10	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	–	16	20	ns
t_{dZH}	3-state output delay times	enable-to-HIGH	–	19	25	ns
t_{dZL}	3-state output delay times	enable-to-LOW	–	16	20	ns
t_{dHZ}	3-state output delay times	disable-to-HIGH	–	14	20	ns
t_{dLZ}	3-state output delay times	disable-to-LOW	–	9	12	ns

Notes

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition. If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.
2. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 2 ns.
3. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).
4. Low frequency ramp signal ($V_{VI(P-P)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(P-P)}$ = 0.5 V, f_i = 4.43 MHz) at the input.
5. Supply voltage ripple rejection:
   - SVRR1; variation of the input voltage producing output code 127 for supply voltage variation of 1 V: $SVRR1 = 20 \log (\Delta V_{VI(127)} / \Delta V_{CCA})$
   - SVRR2; relative variation of the full-scale range of analog input for a supply voltage variation of 1 V: $SVR2 = \{\Delta(V_{VI(0)} - V_{VI(255)}) / (V_{VI(0)} - V_{VI(255)})\} + \Delta V_{CCA}$.
6. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}; $f_{\overline{CLK}}$ = 27 MHz).
7. Output data acquisition:
   - Output data is available after the maximum delay of t_{dHL} and t_{dLH}.

Table 1 Output coding and input voltage (referenced to AGND; typical values).

			BINARY OUTPUT BITS								TWO's COMPLEMENT OUTPUT BITS							
STEP	$V_{VI(p-p)}$	O/UF	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow	< 1.55	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1.55	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
254	•	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	3.26	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow	> 3.26	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

Table 2 Mode selection.

$\overline{TC}$	$\overline{CE}$	D7 - D0	O/UF
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

Where: X = don't care

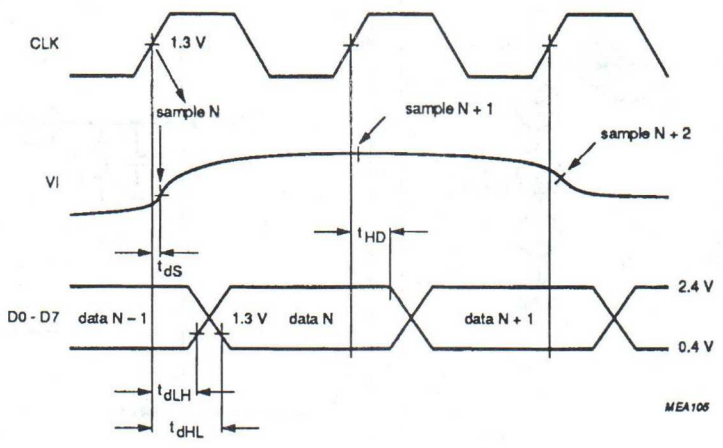


Fig.3 Timing diagram.

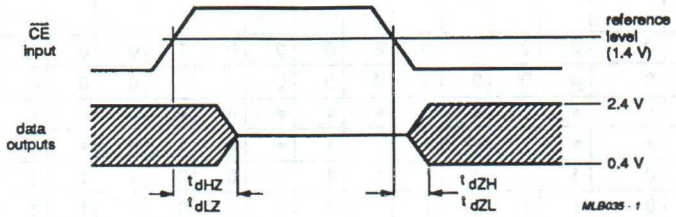


Fig.4 3-state delay timing diagram.

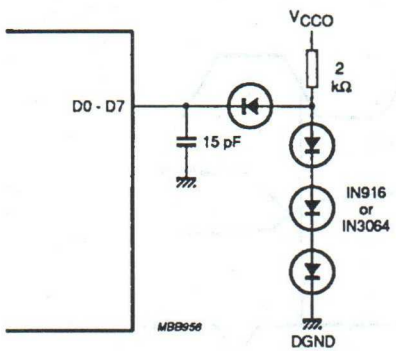


Fig.5 Load circuit for timing measurement; data outputs ($\overline{CE}$ = LOW).

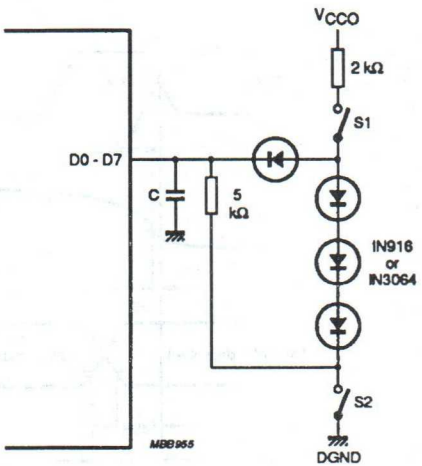


Fig.6 Load circuit for timing measurement; 3-state outputs ($\overline{CE}$: f_i = 1 MHz; V_{VI} = 3 V); see Table 3.

Table 3 Timing measurement for load circuit.

TIMING MEASUREMENT	SWITCH S1	SWITCH S2	CAPACITOR
t_{dZH}	open	closed	15 pF
t_{dZL}	closed	open	15 pF
t_{dHZ}	closed	closed	5 pF
t_{dLZ}	closed	closed	5 pF

INTERNAL PIN CONFIGURATIONS

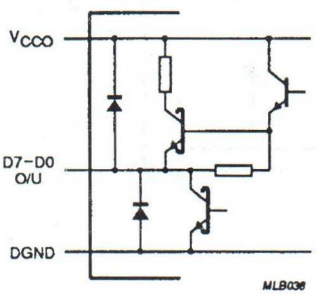


Fig.7 TTL data and overflow/underflow outputs.

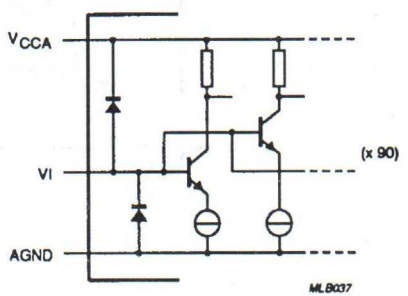


Fig.8 Analog inputs.

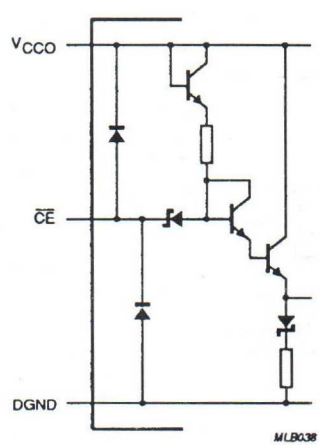


Fig.9 $\overline{CE}$ (3-state) input.

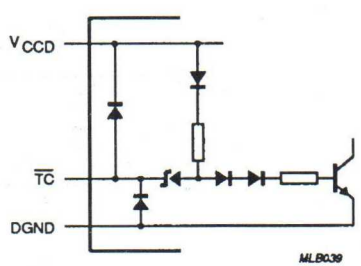


Fig.10 $\overline{TC}$ (two's complement) input.

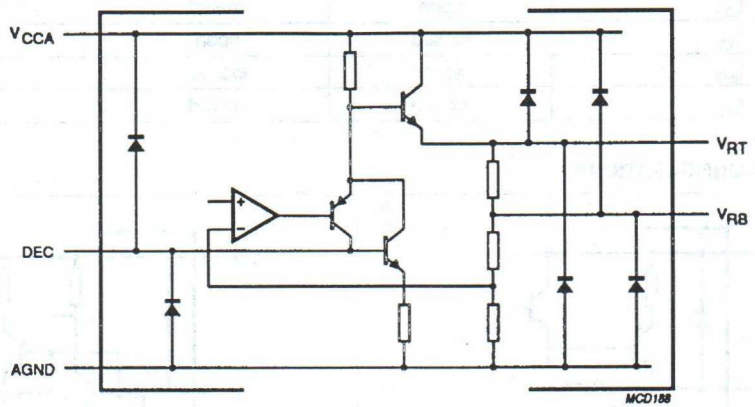


Fig.11 V_{RB}, V_{RT} and DEC.

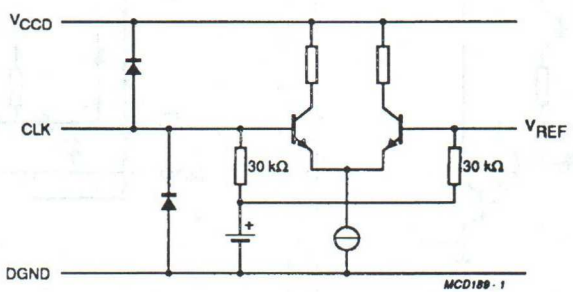


Fig.12 CLK and $\overline{CLK}$ inputs.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).

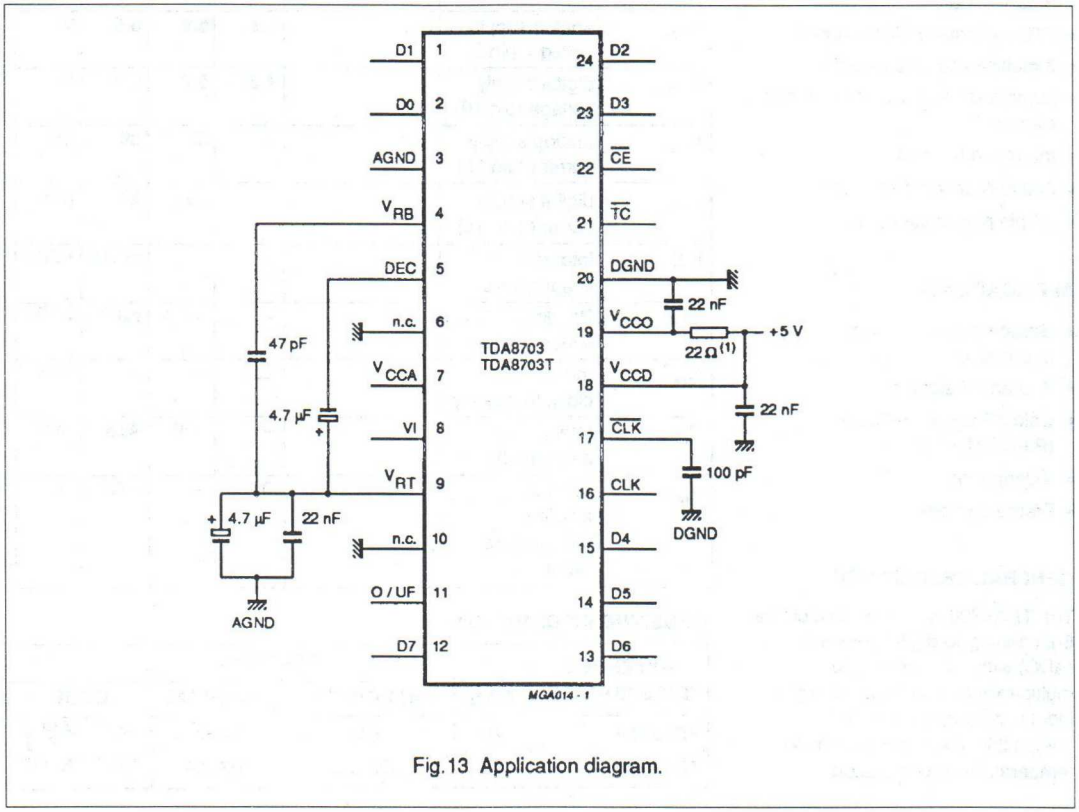


Fig.13 Application diagram.

Notes to Fig.13

1. It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of the TDA8703 interfaces with a capacitive CMOS load device.
2. CLK should be decoupled to the DGND with a 100 nF capacitor, if a TTL signal is used on CLK (see 'Notes to the characteristics', note 1).
3. CLK and $\overline{CLK}$ can be used in a differential mode (see 'Notes to the characteristics', note 1).
4. V_{RB} and V_{RT} are decoupling pins for the internal reference ladder; do not draw current from these pins in order to achieve good linearity.
5. If it is required to use the TDA8703 in a parallel system configuration, the references (V_{RB} and V_{RT}) of each TDA87803 can be connected together. Code 0 will be identical and code 255 will remain in the 1LSB variation for each TDA8703.
6. Analog and digital supplies should be separated and decoupled.
7. Pins 6 and 10 should be connected to AGND in order to prevent noise influence.

6-Bit analog-to-digital converter with multiplexer and clamp

TDA8706

FEATURES

- 6-bit resolution
- Binary 3-state TTL outputs
- TTL compatible digital inputs
- 3 multiplexed video inputs
- Luminance and colour difference clamps
- Internal reference
- 300 mW power dissipation
- 20-pin plastic package

APPLICATIONS

- General purpose video applications
- Y, U and V signals
- Colour Picture-in-Picture (PIPCO) for TV
- Videophone
- Frame grabber

GENERAL DESCRIPTION

The TDA8706 is a monolithic bipolar 6-bit analog-to-digital converter (ADC) with a 3 analog input multiplexer and a clamp. All digital inputs and outputs are TTL compatible. Regulator with good temperature compensation.

FUNCTIONAL DESCRIPTION

The TDA8706 is a "like-flash" converter which produces an output code in one clock period. The device can withstand a duty clock cycle of 50 to 66.6% (clock HIGH). Luminance clamping level is fitted with 00 hex. code (output 000000). Chrominance clamping level is fitted with 20 Hex. code (output 100000).

QUICK REFERENCE DATA

Measured over full voltage and temperature ranges

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage (pin 2)		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage (pin 10)		4.5	5.0	5.5	V
I_{CCA}	analog supply current (pin 20)		–	32	39	mA
I_{CCD}	digital supply current (pin 10)		–	28	37	mA
ILE	integral linearity error		–	–	±0.75	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
f_{CLK}	maximum clock frequency		20	–	–	MHz
P_{tot}	total power dissipation		–	300	418	mW
T_{amb}	operating ambient temperature range		0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8706	20	DIL	plastic	SOT146EF4
TDA8706T	20	SO20L	plastic	SOT163AG7

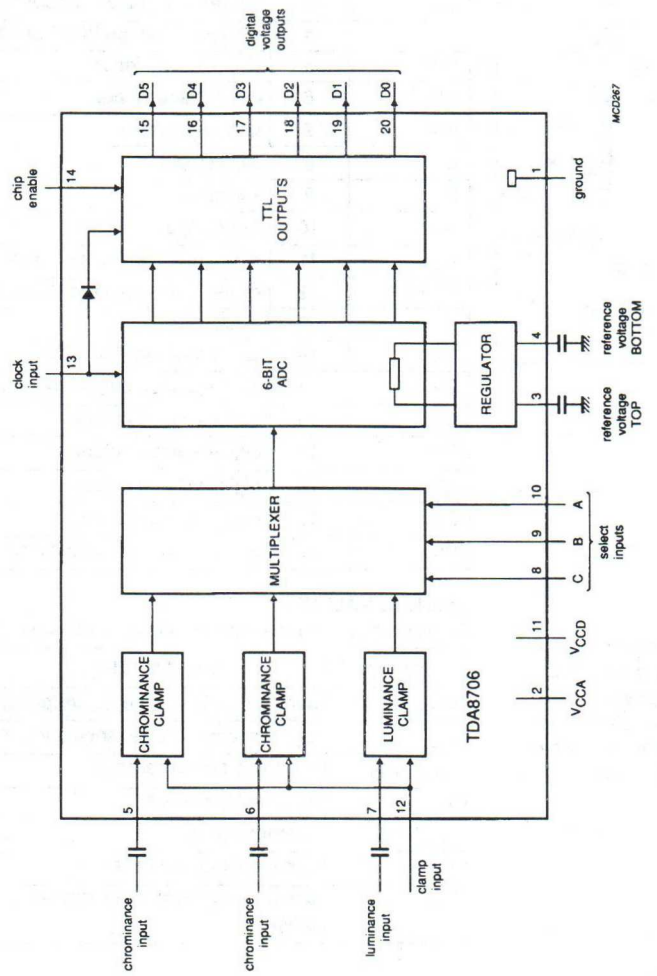


Fig.1 Block diagram.

6-Bit analog-to-digital converter with multiplexer and clamp

TDA8706

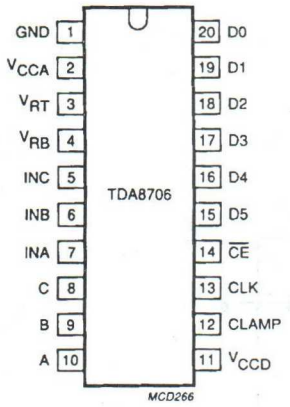


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1	ground
V_{CCA}	2	analog positive supply (+5 V)
V_{RT}	3	reference voltage TOP decoupling
V_{RB}	4	reference voltage BOTTOM decoupling
INC	5	chrominance input
INB	6	chrominance input
INA	7	luminance input
C	8	select input
B	9	select input
A	10	select input
V_{CCD}	11	digital positive supply voltage (+5 V)
CLAMP	12	clamp pulse input (positive pulse)
CLK	13	clock input
$\overline{CE}$	14	chip enable (active LOW)
D5	15	digital voltage output: most significant bit (MSB)
D4	16	digital voltage output
D3	17	digital voltage output
D2	18	digital voltage output
D1	19	digital voltage output
D0	20	digital voltage input: least significant bit (LSB)

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range (pin 2)	−0.3	7.0	V
V_{CCD}	digital supply voltage range (pin 10)	−0.3	7.0	V
V_{CCA}-V_{CCD}	supply voltage difference	1.0	−	V
V_I	input voltage range	−0.3	7.0	V
I_O	output current	−	10	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C

CHARACTERISTICS (see Tables 1 and 2)

V_{CCA} = 4.5 V to 5.5 V; V_{CCD} = 4.5 V to 5.5 V = V_{CCD}; T_{amb} = 0 °C to +70°C; C_{VRB} = C_{VR1} = 100 nF; Typical values measured at V_{CCA} = V_{CCD} = 5 V and T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage (pin 2)		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage (pin 10)		4.5	5.0	5.5	V
I_{CCA}	analog supply current (pin 2)		–	32	39	mA
I_{CCD}	digital supply current (pin 10)	all outputs at LOW level	–	28	37	mA
Inputs						
CLOCK INPUT (PIN 13)						
V_{IL}	LOW level input voltage		0		0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	100	µA
Z_I	input impedance	f_{CLK} = 20 MHz	–	4	–	kΩ
C_i	input capacitance	f_{CLK} = 20 MHz	–	2	–	pF
A, B, C, CLAMP AND CEN INPUTS (PINS 8, 9, 10, 12 AND 14)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	20	µA
Reference voltage (pins 3 and 4)						
V_{RT}	reference voltage TOP decoupling		3.22	3.35	3.44	V
V_{RB}	reference voltage BOTTOM decoupling		1.84	1.9	1.96	V
$V_{RT} - V_{RB}$	reference voltage TOP – BOTTOM decoupling		1.36	1.435	1.48	V
Analog inputs INA, INB, INC (pins 7, 6 and 5)						
$V_{I(p-p)}$	input voltage amplitude (peak-to-peak value)		840	900	940	mV
Z_I	input impedance	f_i = 4.43 MHz	100	–	–	kΩ
C_{clamp}	coupling clamp capacitance		1	10	1000	nF
Analog signal processing (pins 5, 6 and 7) (f_{CLK} = 20 MHz)						
f_1	fundamental harmonics (full scale)	f_i = 4.43 MHz	–	–	0	dB
f_{all}	harmonics (full scale); all components	f_i = 4.43 MHz		–45		dB
G_{diff}	differential gain	note 1	–	0.4	–	%
ϕ_{diff}	differential phase	note 1	–	1.0	–	deg
SVRR	supply voltage ripple rejection	note 2	–	–30	–	dB
Outputs						
DIGITAL VOLTAGE OUTPUTS (PINS 15 TO 20) (SEE TABLE 2)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OH}	HIGH level ouptut voltage	I_O = 0.5 mA	2.7	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	20	µA
Switching characteristics						
CLOCK TIMING (SEE FIG.3)						
f_{CLK}	maximum clock frequency		20	–	–	MHz
f_{mux}	maximum multiplexing frequency		10	–	–	MHz
t_{CLK}	period		50	–	–	ns
	duty cycle	CLK = V_{IH}	45	50	66.6	%
t_{LOW}	LOW time	at 50%	16	–	–	ns
t_{HIGH}	HIGH time	at 50%	22.5	–	–	ns
t_{CLR}	rise time	at 10% to 90%	4	6	–	ns
t_{CLF}	fall time	at 90% to 10%	4	6	–	ns
Select signals, Clamp, Data (see Figs 4 and 5)						
t_S	set-up time select A, B and C		35	–	–	ns
t_r	rise time (A, B and C)	at 10% to 90%	4	6	–	ns
t_f	fall time (A, B and C)	at 90% to 10%	4	6	–	ns
t_{CLPS}	set-up time clamp asynchronous		0	–	–	
t_{CLPH}	hold time clamp asynchronous		0	–	–	
t_{CLPP}	clamp pulse	C_{CLP} = 10 nF	–	3	–	µs
t_d	data output delay time		–	15	24	ns
t_{DH}	data hold time		12	–	–	ns
Transfer function						
ILE	DC integral linearity error		–	–	±0.75	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
AILE	AC integral linearity error	note 3	–	–	±2	LSB
EB	effective bits	note 3	–	5.7	–	bits
Timing						
DIGITAL OUTPUTS						
T_{zd}	3-state delay time	see Fig.6	–	16	25	ns
T_{sto}	sampling time offset		–	2	–	ns

Notes to the characteristics

1. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V and f_i = 4.43 MHz) at the input.
2. Supply voltage ripple rejection (SVRR): variation of the input voltage produces output code 31 for a supply voltage variation of 1 V.

   $$SVRR = 20 \log \frac{\Delta V_{VI31}}{\Delta V_{CCA}}$$

3. Full-scale sinewave; f_i = 4.43 MHz, f_{CLK} = 20 MHz.

Table 1 Output coding

STEP	V_I (note 1)	BINARY OUTPUTS
	(TYP. value)	D5 to D0
Underflow	< 2.2 V	000000
0	2.2 V	000000
1	2.215 V	000001
.		.....
.		.....
.		.....
62	3.072 V	111110
63	3.086 V	111111
Overflow	> 3.1 V	111111

Note

1. With clamping capacitance.

Table 2 Mode selection

CEN	D0 to D5
1	high impedance
0	active Binary

Table 3 Clamp input A

A	CLAMP	DIGITAL OUTPUTS	$V_{in}A$
0	1	X	2.2
1	1	0	2.2

Note

X = don't care.

Table 4 Clamp input B and C

B/C	CLAMP	DIGITAL OUTPUTS	$V_{in}B/V_{in}C$
0	1	X	2.65
1	1	32	2.65

Note

X = don't care.

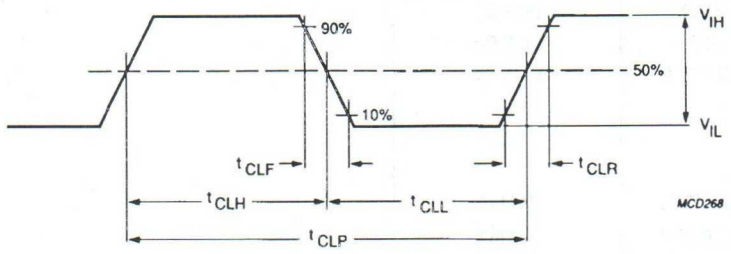


Fig.3 AC clock characteristics.

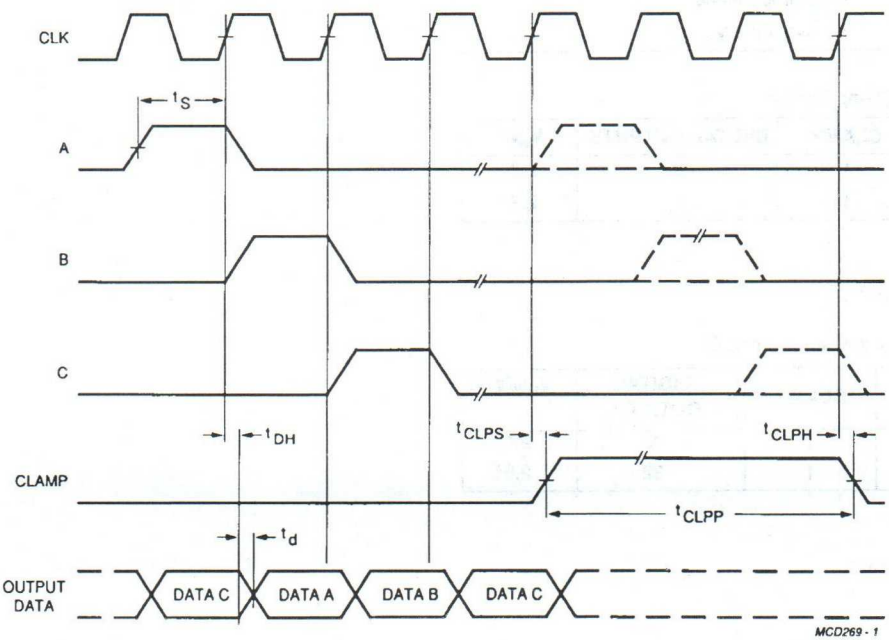


Fig.4 AC characteristics select signals; Clamp, Data.

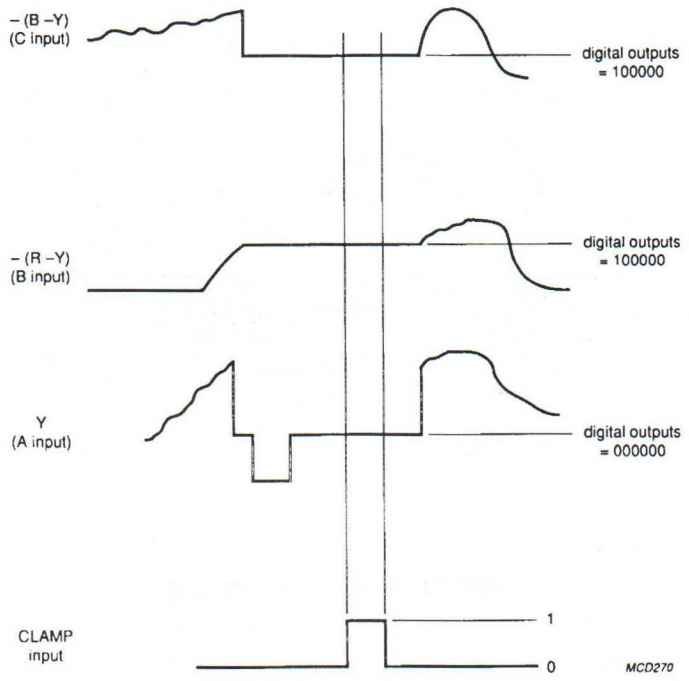


Fig.5 AC characteristics select signals; Clamp, Data.

Table 5 Clamp characteristic related to TV signals

PARAMETER	MIN.	TYP.	MAX.	UNIT
clamping time per line (signal active)	2.2	3.0	3.3	µs
input signals clamped to correct level after	–	3	10	lines

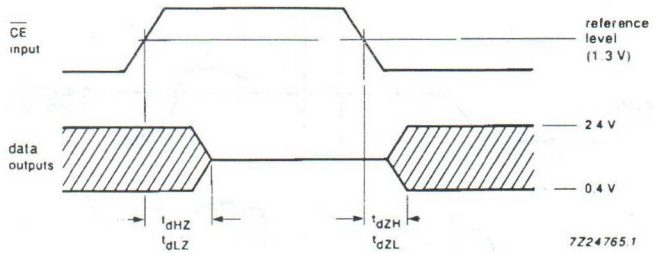


Fig.6 Timing diagram of 3-state delay.

Application information

Additional application information will be supplied on request (please quote reference number FTV/9112).

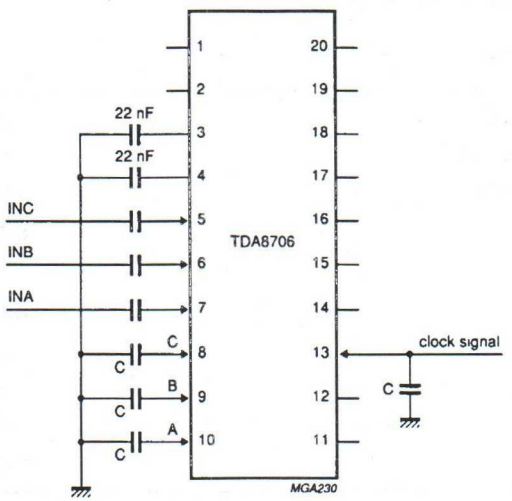


Fig.7 Application diagram.

Notes to figure 7

1. 'C' capacitors must be determined on the output capacitance of the circuits driving A, B and C or CLK pins
2. V_{RB} and V_{RT} are decoupling pins for the internal reference ladder. Do not draw current from these pins in order to achieve good linearity
3. Analog and digital supplies should be separated and decoupled.

14-bit analog-to-digital converter TDA1534

An integrated 14-bit analogue to digital converter (ADC) which uses the successive approximation conversion technique and includes the comparator, reference source and clock on the same chip.
The high linearity makes it very suitable for signal processing while the accurate, temperature-compensated reference source makes it applicable for instrumentation purposes.
The ADC accepts unipolar or bipolar input signals.
Digital output data is in serial form.
All digital outputs are fully TTL compatible.

QUICK REFERENCE DATA

Positive supply voltage (pin 5)	V_P	typ.	5 V
Negative supplu voltage 1 (pin 6)	$-V_{N1}$	typ.	5 V
Negative supply voltage 2 (pin 9)	$-V_{N2}$	typ.	17 V
Signal-to-noise ratio	S/N	typ.	84 dB
Linearity error		typ.	± ½ LSB
Total power dissipation	P_{tot}	typ.	500 mW
Operating ambient temperature range	T_{amb}	−20 to	+ 70 °C
Storage temperature range	T_{stg}	−55 to	+ 150 °C
Resolution			14 bits
Full scale input current	I_{FS}	typ.	4 mA

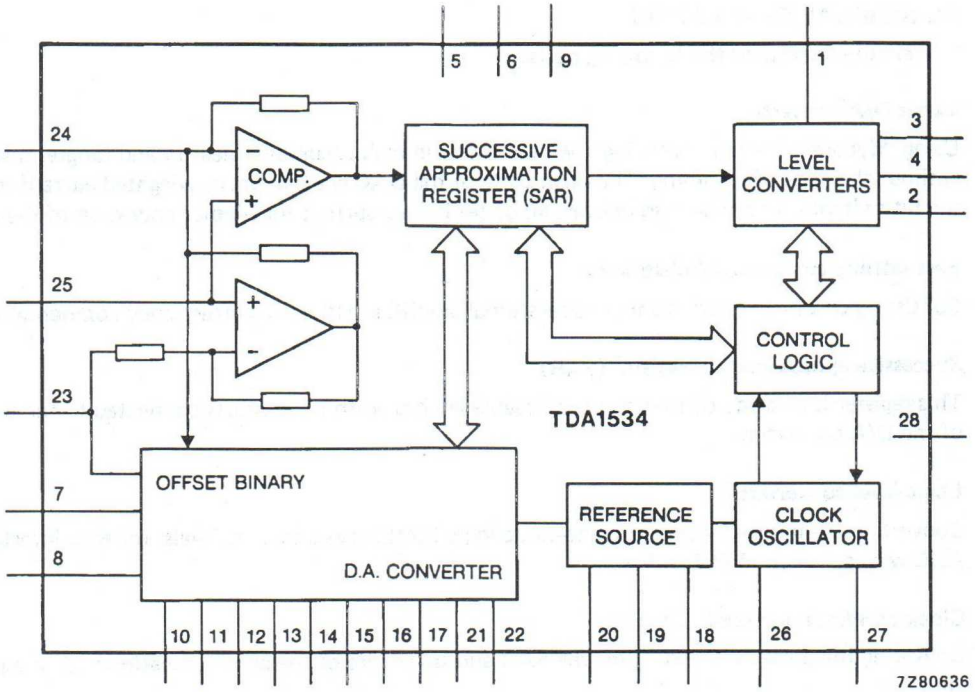


Fig. 1 Block diagram.

PIN DESIGNATION

1	start conversion
2	status out
3	data out
4	data strobe
5	positive supply voltage
6	negative supply voltage 1
7	oscillator input
8	oscillator input
9	negative supply voltage 2
10	decoupling binary weighted current sources
11	
12	
13	
14	
15	decoupling binary weighted current sources
16	
17	
18	I_{ref1}
19	I_{ref2}
20	I_{ref3}
21	decoupling binary weighted current sources
22	
23	offset binary input
24	analogue signal input
25	analogue ground
26	oscillator
27	oscillator
28	digital ground

FUNCTIONAL DESCRIPTION

The circuit consists of the following parts:

14-bit D/A converter

Using "dynamic element matching", which results in high accuracy, linearity and longterm stability, without the need of trimming. The main parts of the DAC are the binary wieghted current sources and the bit switches. The DAC also delivers an offset binary current for bipolar operation of the ADC.

Fast settling comparator/substractor

Consisting of a high speed, clamped operational amplifier with special frequency compensation system.

Successive approximation register (SAR)

This register is an array of fourteen addressable latches, with the outputs connected to the bit switches of the D/A converter.

Logic-level converters

Converting the internally used current-mode-logic (CML) levels to TTL levels, for easy interface of the ADC with standard logic families.

Clock oscillator and control logic

Delivering the pulses and timing for the SAR and takes care of the communication with the peripheral circuits.

Reference source

Based on the bandgap voltage of silicon, with extra temperature compensation circuit.

For the timing of the output signals see Fig. 3. At the leading edge of the start conversion (SC) pulse the ADC starts converting the input voltage. During the conversion cycle the following signals appear at the output pins:

Status (pin 2)

This signal can be used to force the Sample-Hold-Circuit, in front of the ADC, in hold mode.

Data strobe (pin 4)

This signal is used to clock the data-out signal into the peripheral devices.

Data out (pin 3)

The 14 bits serial, binary, output code of the A/D converter starting with the most significant bit (MSB). The data must be considered valid at the trailing edge of the data-strobe signal.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Positive supply (pin 5)	V_P	0 to 7 V
Negative supply voltage (pin 6)	$-V_{N1}$	0 to 7 V
Negative supply voltage (pin 9)	$-V_{N2}$	0 to 20 V
Storage temperature	T_{stg}	−55 to + 150 °C
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Total power dissipation	P_{tot}	derating curve (Fig. 2)

CHARACTERISTICS (see application circuit Fig. 4)

V_P = 5 V; $-V_{N1}$ = 5 V; $-V_{N2}$ = 17 V; T_{amb} = + 25 °C, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Positive supply voltage (pin 5)	V_P	4	5	6	V
Negative supply voltage 1 (pin 6)	$-V_{N1}$	–	5	–	V
Negative supply voltage 2 (pin 9)	$-V_{N2}$	16,5	17	18	V
Positive supply current	I_P	–	30	40	mA
Negative supply current	$-I_{N1}$	–	37	45	mA
Negative supply current	$-I_{N2}$	–	10	13	mA
Total power dissipation	P_{tot}	–	500	–	mW
Resolution		–	14	–	bits
Analogue input					
Full scale input current offset-binary current switched off	I_{FS}	3,8	4,0	4,2	mA
Temperature coefficient pin 23 short-circuited	TC	–	t.b.f.	–	10^{-6}/K
Zero-offset offset-binary current switched off					
Offset voltage	$-V_o$	10	20	30	mV
Temperature coefficient	TC	–	t.b.f.	–	μV/K
Offset current	I_o	–	500	–	nA
Temperature coefficient	TC	–	t.b.f.	–	nA/K
Linearity					
Linearity error		–	± ¼	–	LSB
Linearity from −20 to + 70 °C		–	± ½	–	LSB
Offset binary current	I_{BO}	$0{,}45 \cdot I_{FS}$	$0{,}50 \cdot I_{FS}$	$0{,}55 \cdot I_{FS}$	mA
Temperature coefficient	TC	–	t.b.f.	–	10^{-6}/K
Signal to noise ratio*	S/N	80	84	–	dB

parameter	symbol	min.	typ.	max.	unit
Start conversion (pin 1)					
Input current					
V_{IL} (< 0,8 V)	$-I_1$	–	–	1,6	mA
V_{IH} (> 2,0 V)	I_1	–	–	40	μA
Data, strobe, status (pins 3, 4 and 2)					
Output current					
V_{OL} (< 0,6 V)	$I_{3, 4, 2}$	6,4	16	–	mA
V_{OH} (> 2,4 V)	$-I_{3, 4, 2}$	160	400	–	μA
Conversion time					
$C_{26\text{-}27}$ = 220 pF ± 1%	t_C	–	8,5	–	μs
Signal width (pin 1)					
start conversion	t_{SC}	0,2	–	t_C	μs
Delay time (pin 2)					
status out	t_{SD}	–	60	–	ns
Set-up time (pin 3)					
data out	t_{DS}	–	25	–	ns
Pulse duration (pin 4)					
data strobe high	t_{DSH}	–	125	–	ns

* Signal-to-noise ratio within 10 Hz and 20 kHz bandwidth of a 1 kHz full scale sinewave, generated at a sample rate of 44 kHz.

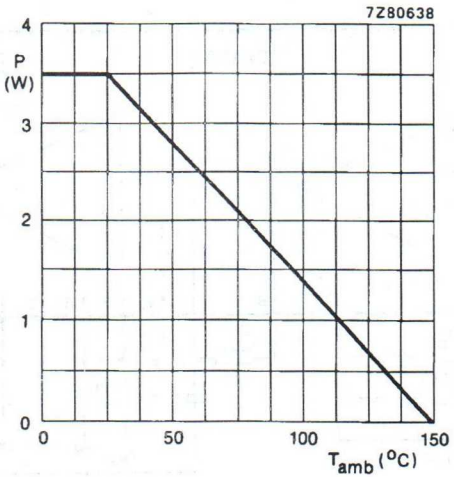


Fig. 2 Power derating curve.

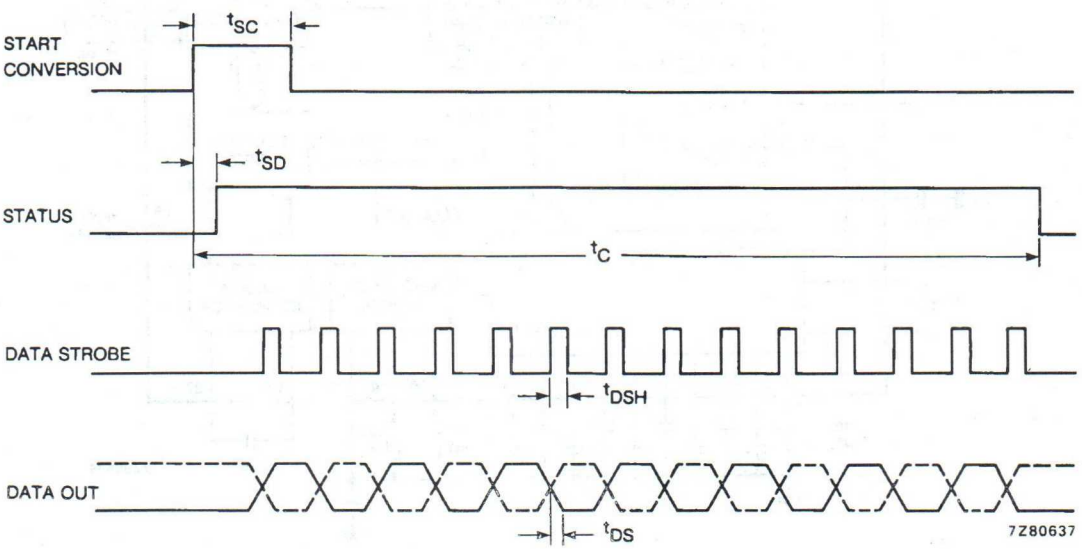


Fig. 3 Switching times waveforms.

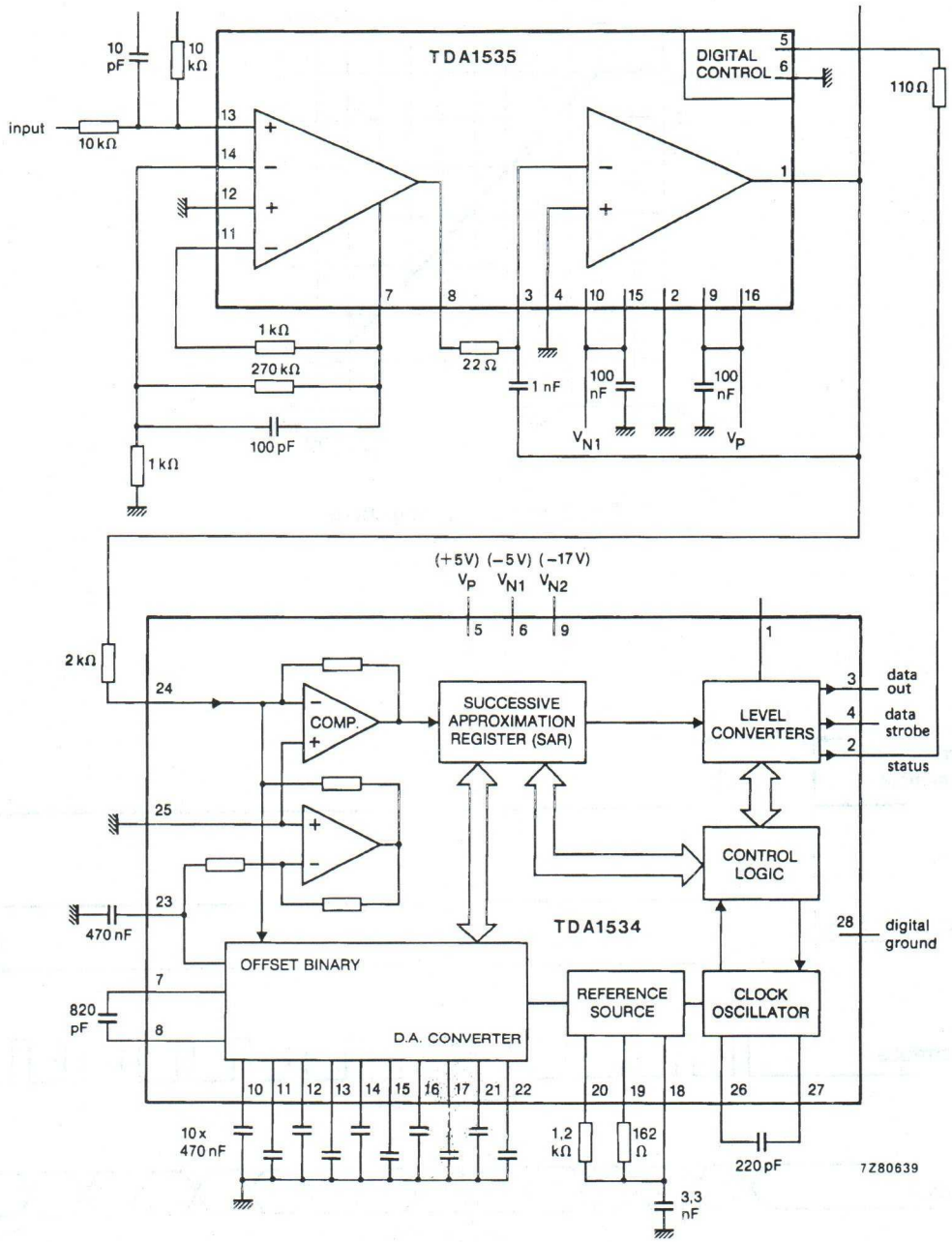


Fig. 4 Application and test circuit.

All earthed components connected to analogue ground (pin 25).

Video analog input interface — TDA8708A

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- Binary or two's complement 3-state TTL outputs
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Power dissipation of 365 mW (typical)
- Input selector circuit (one out of three video inputs)
- Clamp and Automatic Gain Control (AGC) functions for CVBS and Y signals
- No sample-and-hold circuit required.
- The TDA8708A has white peak control in modes 1 and 2 whereas the TDA8708B has control in mode 1 only.

APPLICATIONS

- Video signal decoding
- Scrambled TV (encoding and decoding)
- Digital picture processing
- Frame grabbing.

GENERAL DESCRIPTION

The TDA8708A is an analog input interface for video signal processing. It includes a video amplifier with clamp and gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz and an input selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	37	45	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	TTL output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency	30	32	–	MHz
B	maximum −3 dB bandwidth (AGC amplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	365	500	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8708A	28	DIP	plastic	SOT117-1
TDA8708AT	28	SO28L	plastic	SOT136-1

BLOCK DIAGRAM

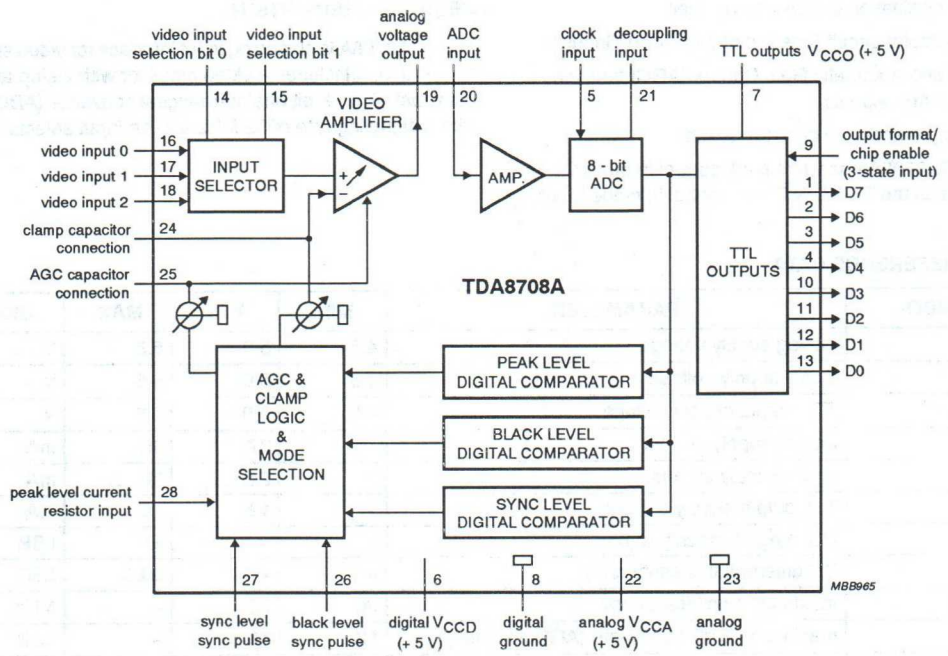


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output; bit 7 (MSB)
D6	2	data output; bit 6
D5	3	data output; bit 5
D4	4	data output; bit 4
CLK	5	clock input
V_{CCD}	6	digital supply voltage (+5 V)
V_{CCO}	7	TTL outputs supply voltage (+5 V)
DGND	8	digital ground
OF	9	output format/chip enable (3-state input)
D3	10	data output; bit 3
D2	11	data output; bit 2
D1	12	data output; bit 1
D0	13	data output; bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
AGC	25	AGC capacitor connection
GATE B	26	black level synchronization pulse
GATE A	27	sync level synchronization pulse
RPEAK	28	peak level current resistor input

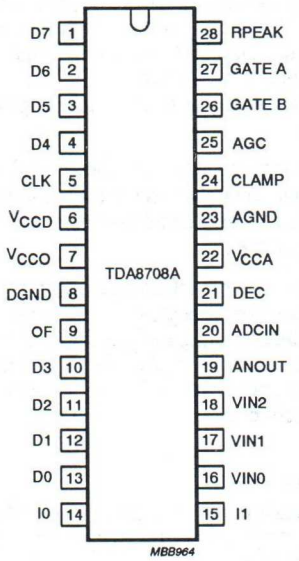


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8708A provides a simple interface for decoding video signals.

The TDA8708A operates in configuration mode 1 (see Fig.4) when the video signals are weak (i.e. when the gain of the AGC amplifier has not yet reached its optimum value). This enables a fast recovery of the synchronization pulses in the decoder circuit. When the pulses at the GATE A and GATE B inputs become distinct (GATE A and GATE B pulses are synchronization pulses occurring during the sync period and rear porch respectively) the TDA8708A automatically switches to configuration mode 2 (see Fig.5).

When the TDA8708A is in configuration mode 1, the gain of the AGC amplifier will be roughly adjusted (sync level to a digital output level of 0 and the peak level to a digital output level of 255).

In configuration mode 2 the digital output of the ADC is compared to internal digital reference levels. The resultant outputs control the charge or discharge current of a capacitor connected to the AGC pin. The voltage across this capacitor controls the gain of the video amplifier. This is the gain control loop.

The sync level comparator is active during a positive-going pulse at the GATE A input. This means that the sync pulse of the composite video signal is used as an amplitude reference. The bottom of the sync pulse is adjusted to obtain a digital output of logic 0 at the converter output. As the black level is at digital level 64, the sync pulse will have a digital amplitude of 64 LSBs.

The peak-white control loop is always active. If the video signal tends to exceed the digital code of 248, the gain will be limited to avoid any over-range of the converter.

The use of nominal signals will prevent the output from exceeding a digital code of 213 and the peak-white control loop will be non-active.

The clamp level control is accomplished by using the same techniques as used for the gain control. The black-level digital comparator is active during a positive-going pulse at the GATE B input. The clamp capacitor will be charged or discharged to adjust the digital output to code 64.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	−0.3	+7.0	V
V_{CCD}	digital supply voltage	−0.3	+7.0	V
V_{CCO}	output supply voltage	−0.3	+7.0	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD}	−1.0	+1.0	V
	supply voltage difference between V_{CCO} and V_{CCD}	−1.0	+1.0	V
	supply voltage difference between V_{CCA} and V_{CCO}	−1.0	+1.0	V
V_I	input voltage	−0.3	V_{CCA}	V
I_O	output current	0	+10	mA
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT117-1	55	K/W
	SOT136-1	70	K/W

CHARACTERISTICS

$V_{CCA} = V_{22}$ to V_{23} = 4.5 to 5.5 V; $V_{CCD} = V_6$ to V_8 = 4.5 to 5.5 V; $V_{CCO} = V_7$ to V_8 = 4.2 to 5.5 V; AGND and DGND shorted together; V_{CCA} to V_{CCD} = −0.5 to +0.5 V; V_{CCO} to V_{CCD} = −0.5 to +0.5 V; V_{CCA} to V_{CCO} = −0.5 to +0.5 V; T_{amb} = 0 to +70 °C; typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	37	45	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	TTL output supply current	TTL load (see Fig.8)	–	12	16	mA
Video amplifier inputs						
VIN(0 TO 2) INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	AGC load with external capacitor; note 1	0.6	–	1.5	V
$\|Z_i\|$	input impedance	f_i = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	−400	–	–	μA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	μA
GATE A AND GATE B TTL INPUTS (SEE FIGS 4 AND 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	−400	–	–	μA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	μA
t_W	pulse width	see Fig.5	2	–	–	μs
RPEAK INPUT (PIN 28)						
$I_{28(min)}$	minimum peak level current	R_{28} = 0 Ω	–	80	150	μA
AGC INPUT (PIN 25)						
$V_{25(min)}$	AGC voltage for minimum gain		–	2.8	–	V
$V_{25(max)}$	AGC voltage for maximum gain		–	4.0	–	V
	AGC output current		see Table 2			
CLAMP INPUT (PIN 24)						
V_{24}	clamp voltage for code 128 output		–	3.5	–	V
I_{24}	clamp output current		see Table 3			

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
$V_{19(p-p)}$	AC output voltage (peak-to-peak value)	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	1.33	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	V_{ANOUT} = 1.33 V (p-p); note 2	–	–	1.0	mA
V_{19}	DC output voltage for black level	note 3	–	V_{CCA} – 2.24	–	V
Z_{19}	output impedance		–	20	–	Ω
Video amplifier dynamic characteristics						
α_{ct}	crosstalk between VIN inputs	V_{CCA} = 4.75 to 5.25 V	–	–50	–45	dB
G_{diff}	differential gain	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	2	–	%
φ_{diff}	differential phase	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	0.8	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 4	60	–	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	45	–	dB
ΔG	gain range	see Fig.10	–4.5	–	+6.0	dB
G_{stab}	gain stability as a function of supply voltage and temperature	see Fig.10	–	–	5	%
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	100	μA
$\|Z_i\|$	input impedance	f_{clk}= 10 MHz	–	4	–	kΩ
C_I	input capacitance	f_{clk} = 10 MHz	–	4.5	–	pF
OF INPUT (3-STATE; SEE TABLE 4)						
V_{IL}	LOW level input voltage		0	–	0.2	V
V_{IH}	HIGH level input voltage		2.6	–	V_{CCD}	V
V_9	input voltage in high impedance state		–	1.15	–	V
I_{IL}	LOW level input current		–370	–300	–	μA
I_{IH}	HIGH level input current		–	300	450	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADCIN INPUT (PIN 20; SEE TABLE 5)						
V_{20}	input voltage	digital output = 00	–	V_{CCA} – 2.42	–	V
V_{20}	input voltage	digital output = 255	–	V_{CCA} – 1.41	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	1.0	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f_i = 6 MHz	–	50	–	MΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
DIGITAL OUTPUTS D0 TO D7						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_{OL} = −0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	−20	–	+20	μA
Switching characteristics						
$f_{clk(max)}$	maximum clock input frequency	see Fig.6; note 6	30	32	–	MHz
Analog signal processing (f_{clk} = 32 MHz; see Fig.8)						
G_{diff}	differential gain	V_{20} = 1.0 V (p-p); see Fig.3; note 7	–	2	–	%
φ_{diff}	differential phase	see Fig.3; note 7	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 7	–	–	0	dB
f_{all}	harmonics (full-scale); all components	f_i = 4.43 MHz; note 7	–	−55	–	dB
SVRR2	supply voltage ripple rejection	note 8	–	1	5	%/V
Transfer function (see Fig.8)						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 9	–	–	±2	LSB
Timing (f_{clk} = 32 MHz; see Figs 6, 7 and 8)						
DIGITAL OUTPUTS (C_L = 15 pF; I_{OL} = 2 mA; R_L = 2 kΩ)						
t_{ds}	sampling delay time		–	2	–	ns
t_h	output hold time		6	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time; output enable		–	19	25	ns
t_{dDZ}	3-state delay time; output disable		–	14	20	ns

Notes

1. 0 dB is obtained at the AGC amplifier when applying $V_{i(p-p)}$ = 1.33 V.
2. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referenced to V_{CCA} and defined as:
   a) AC impedance ≥1 kΩ and the DC impedance >2.7 kΩ.
   b) The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
3. Control mode 2 is selected.
4. Signal-to-noise ratio measured with 5 MHz bandwidth:

   $$\frac{S}{N} = 20 \log \frac{V_{ANOUTC(p-p)}}{V_{ANOUTY\ (RMS\ noise)}}$$ at B = 5 MHz.

5. The voltage ratio is expressed as:

   $$SVRR1 = 20 \log \frac{\Delta V_{CCA}}{V_{CCA}} \times \frac{G}{\Delta G}$$ for V_I = 1 V (p-p), gain at 100 kHz = 1 and 1 V supply variation.

6. It is recommended that the rise and fall times of the clock are ≥2 ns. In addition, a 'good layout' for the digital and analog grounds is recommended.
7. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
8. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

   $$SVRR2 = \frac{\Delta (V_{I(00)} - V_{I(FF)}) + (V_{I(00)} - V_{I(FF)})}{\Delta V_{CCA}}$$

9. Full-scale sine wave (f_i = 4.4 MHz; f_{clk} = 27 MHz).

Table 1 Video input selection (CVBS).

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN2

Table 2 AGC output current.

GATE A	GATE B	DIGITAL OUTPUT	I_{AGC}	MODE[2]
1	1	output < 255	−2.5 μA	1
		output > 255	I_{AGCM}	1
0	X[1]	output < 248	0 μA	2
		output > 248	I_{AGCM}	2
1	0	output < 0	+2.5 μA	2
		0 < output < 248	−2.5 μA	2
		output > 248	I_{AGCM}	2

Note

1. X = don't care.
2. Mode 2 can only be initialized with successive pulses on GATE A and GATE B (see Fig.5).

Table 3 CLAMP output current.

GATE A	GATE B	DIGITAL OUTPUT	I_{CLAMP}	MODE
1	1	output < 0	I_{CLAMPM}	1
		output > 0	−2.5 μA	1
X[1]	0	X[1]	0 μA	2
0	1	output < 64	+50 μA	2
		64 < output	−50 μA	2

Note

1. X = don't care.

Table 4 OF input coding.

OF	D0 TO D7
0	active, two's complement
1	high impedance
open circuit[1]	active, binary

Note

1. Use C ≥ 10 pF to DGND.

Table 5 Output coding and input voltage (typical values).

STEP	V_{ADCIN}	BINARY OUTPUTS								TWO'S COMPLEMENT							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	–	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} − 2.41 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	–	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} − 1.41 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
Overflow	–	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

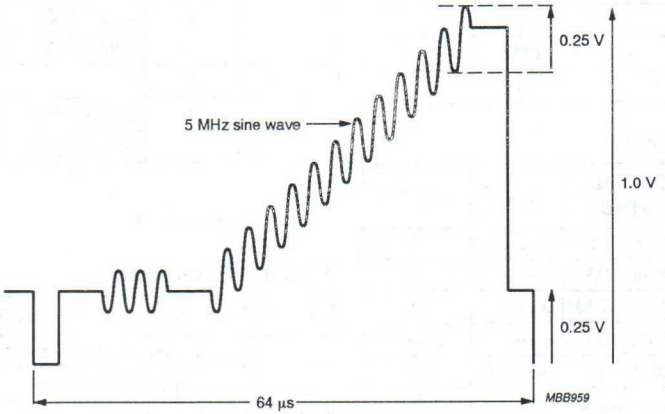


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

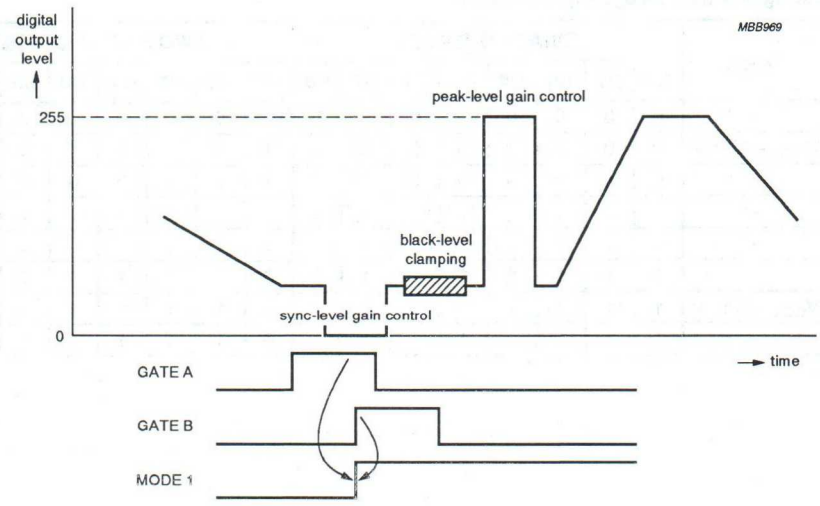


Fig.4 Control mode 1.

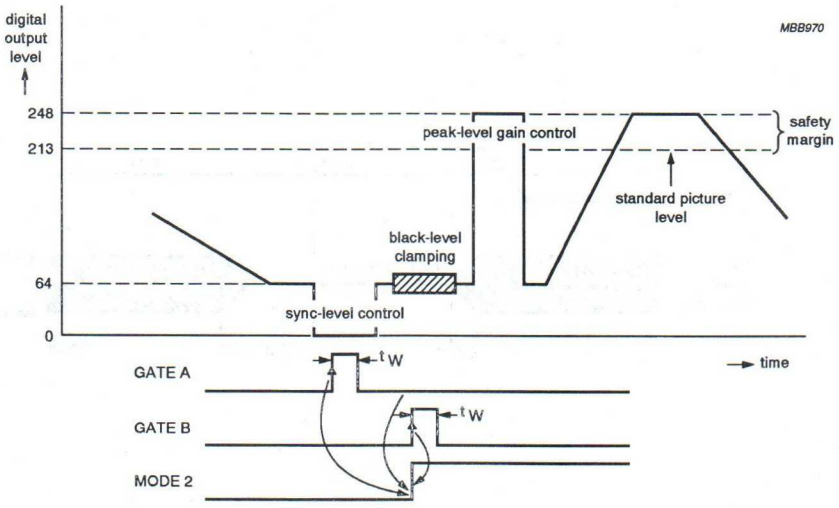


Fig.5 Control mode 2.

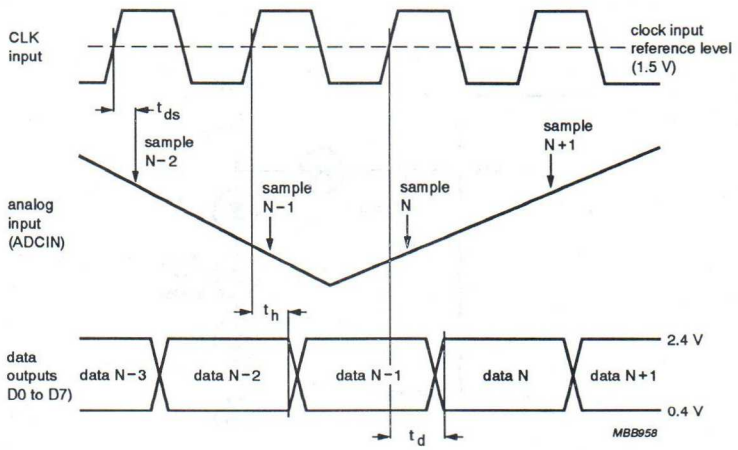


Fig.6 Timing diagram for data output.

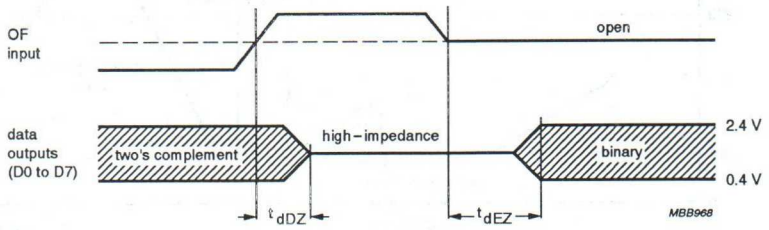


Fig.7 Output format timing diagram.

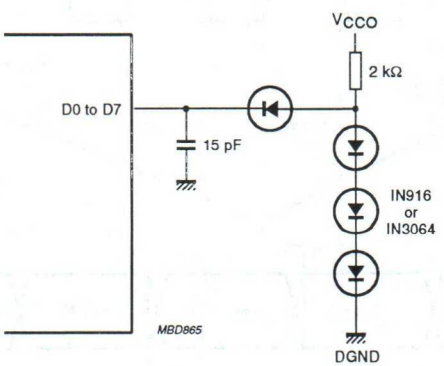


Fig.8 Load circuit for timing measurement; data outputs (OF = LOW or open-circuit).

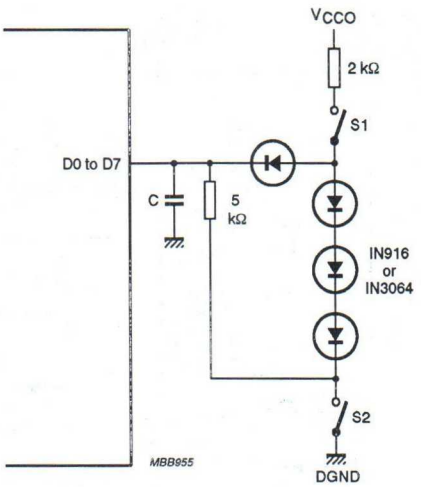
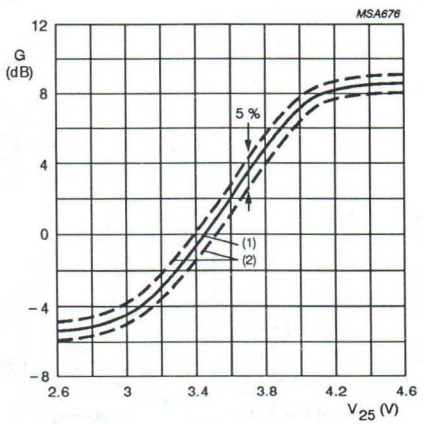


Fig.9 Load circuit for timing measurement; 3-state outputs (OF: f_i = 1 MHz; V_{OF} = 3 V).



(1) Typical value (V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C).
(2) Minimum and maximum values (temperature and supply).

Fig.10 Gain control curve.

INTERNAL PIN CIRCUITRY

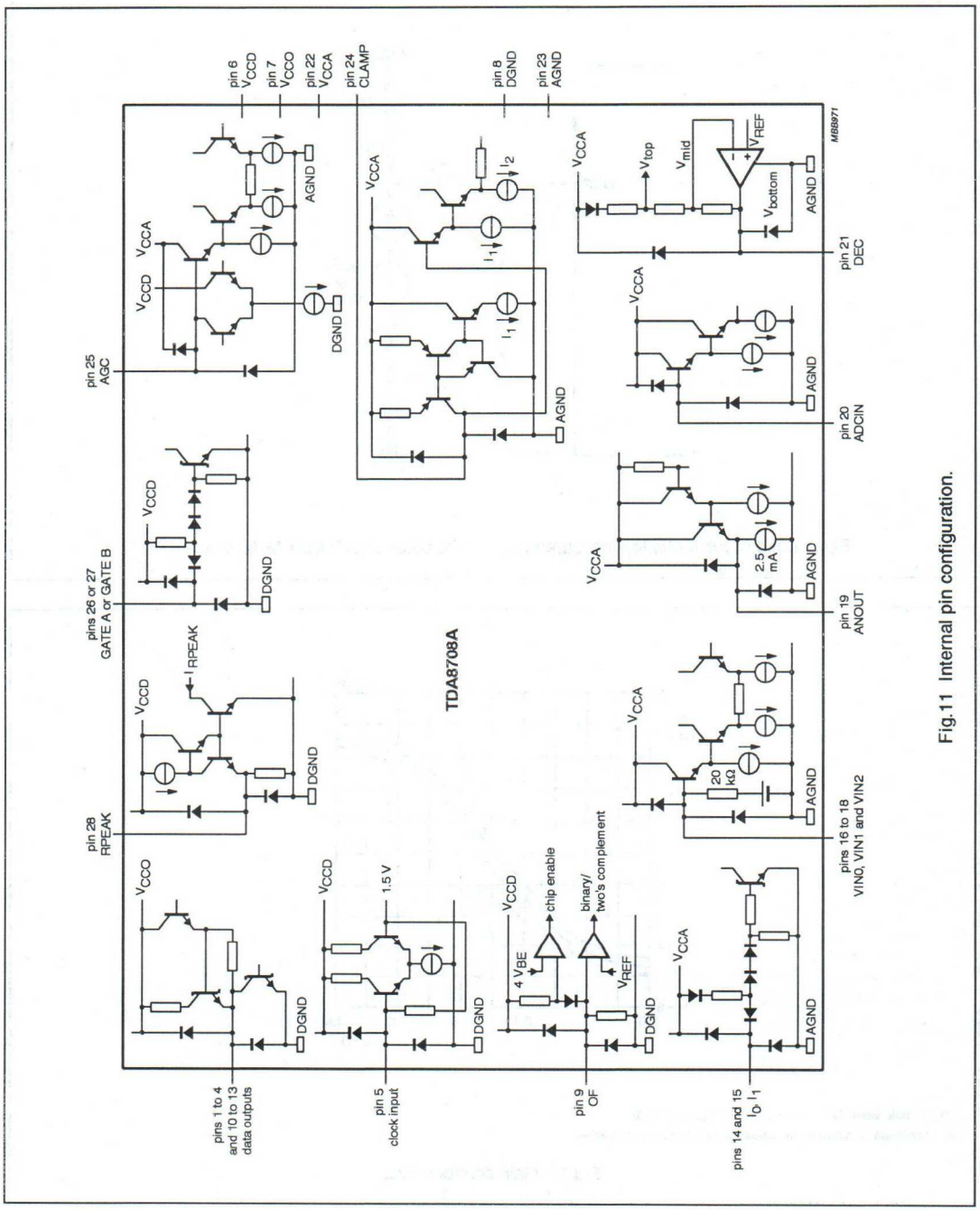
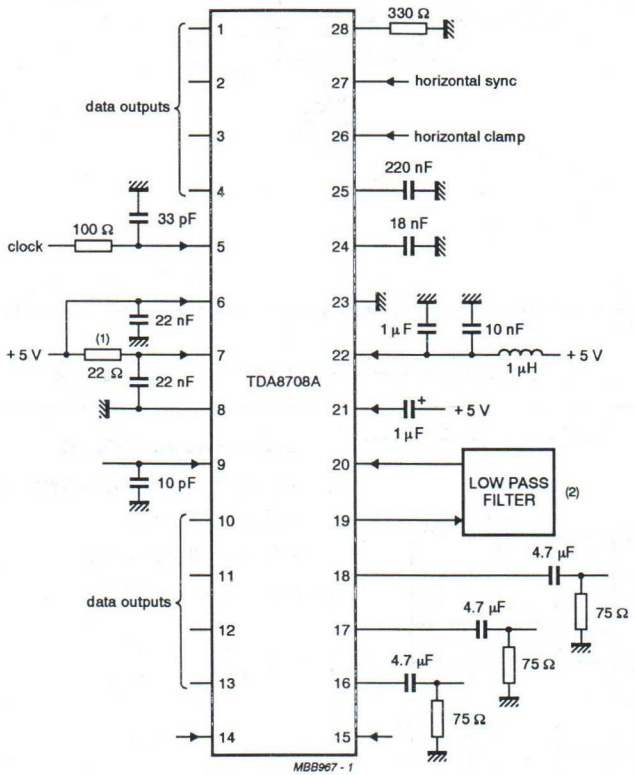


Fig.11 Internal pin configuration.

APPLICATION INFORMATION

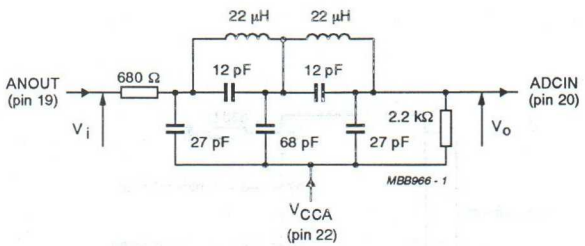
Additional information can be found in the laboratory report *"FBL/AN9308"*.



(1) It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of TDA8708A interfaces with a capacitive CMOS load device.

(2) See Figs 13 and 15 for examples of the low-pass filters.

Fig.12 Application diagram.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.13 Example of a low-pass filter for CVBS and Y signals.

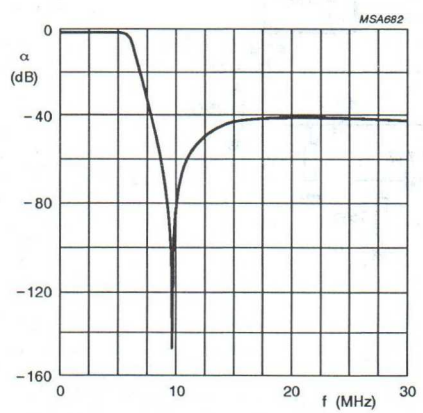
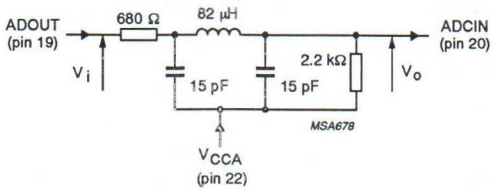


Fig.14 Frequency response for filter shown in Fig.13.

Characteristics of Fig. 13

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at −3 dB
- f_{notch} = 9.75 MHz.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.15 Example of an economical low-pass filter for CVBS and Y signals.

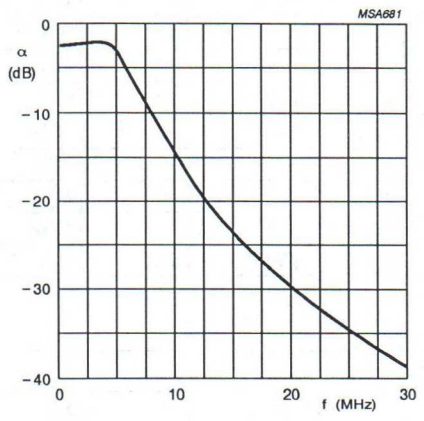


Fig.16 Frequency response for filter shown in Fig.15.

Characteristics of Fig. 15

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at −3 dB.

Video analog input interface | TDA8709A

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Low-level AC clock inputs and outputs
- Clamp function with selection for '16' or '128'
- No sample-and-hold circuit required
- Three selectable video inputs.

APPLICATIONS

- Video signal processing
- Digital picture processing
- Frame grabbing.
- Colour difference signals (U, V)
- R, G, B signals
- Chrominance signal (C).

GENERAL DESCRIPTION

The TDA8709A is an analog input interface for video signal processing. It includes a an input selector (one out-of-three video signals), video amplifier with clamp and external gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz and an input selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	40	47	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	TTL output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency	30	32	–	MHz
B	maximum –3 dB bandwidth (preamplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	380	512	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8709A	28	DIP	plastic	SOT117-1
TDA8709AT	28	SO28L	plastic	SOT136-1

BLOCK DIAGRAM

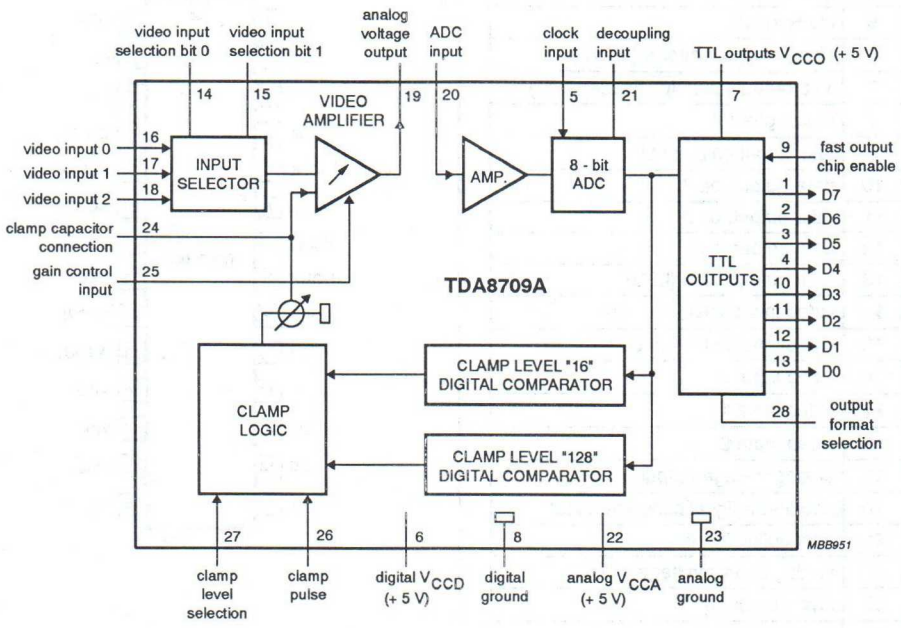


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output; bit 7 (MSB)
D6	2	data output; bit 6
D5	3	data output; bit 5
D4	4	data output; bit 4
CLK	5	clock input
V_{CCD}	6	digital supply voltage (+5 V)
V_{CCO}	7	TTL outputs supply voltage (+5 V)
DGND	8	digital ground
FOEN	9	fast output chip enable
D3	10	data output; bit 3
D2	11	data output; bit 2
D1	12	data output; bit 1
D0	13	data output; bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
GAIN	25	gain control input
CLP	26	clamping pulse
CLS	27	clamping level selection input
OFS	28	output format selection

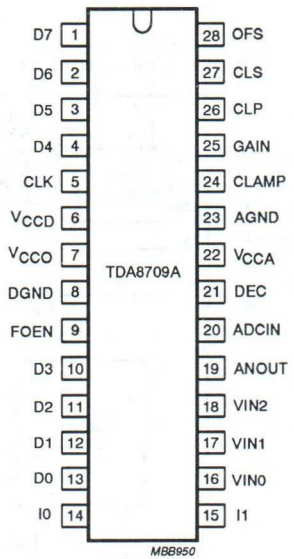


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

TDA8709A is an 8-bit ADC with internal clamping and a preamplifier with adjustable gain.

The clamping value is switched via pin 27 between digital 16 (for R, G, B signals) and digital 128 (for chrominance or colour difference signals). While clamping pulse at pin 27 is logic 1, the device will adjust the clamping level to the chosen value. The output format can be selected between binary and two's complement at pin 28.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	−0.3	+7.0	V
V_{CCD}	digital supply voltage	−0.3	+7.0	V
V_{CCO}	TTL output supply voltage	−0.3	+7.0	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD}	−0.5	+0.5	V
	supply voltage difference between V_{CCO} and V_{CCD}	−0.5	+0.5	V
	supply voltage difference between V_{CCA} and V_{CCO}	−1.0	+1.0	V
V_I	input voltage	−0.3	+7.0	V
I_O	output current	−	+10	mA
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT117-1	55	K/W
	SOT136-1	70	K/W

CHARACTERISTICS

$V_{CCA} = V_{22}$ to V_{23} = 4.5 to 5.5 V; $V_{CCD} = V_6$ to V_8 = 4.5 to 5.5 V; $V_{CCO} = V_7$ to V_8 = 4.2 to 5.5 V; AGND and DGND shorted together; V_{CCA} to V_{CCD} = −0.5 to +0.5 V; V_{CCO} to V_{CCD} = −0.5 to +0.5 V; V_{CCA} to V_{CCO} = −0.5 to +0.5 V; T_{amb} = 0 to +70 °C; typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	40	47	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	TTL output supply current	TTL load (see Fig.7)	–	12	16	mA
Preamplifier inputs						
VIN0 TO VIN2 INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	note 1	0.6	–	1.5	V
$\|Z_i\|$	input impedance	f_i = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	−400	–	–	μA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	μA
CLS, OFS AND CLP TTL INPUTS (SEE FIG.5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	−400	–	–	μA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	μA
t_{CLP}	clamp pulse width		2	–	–	μs
GAIN INPUT (PIN 25)						
$V_{25(min)}$	input voltage for minimum gain	see Fig.9	–	1.8	–	V
$V_{25(max)}$	input voltage for maximum gain	see Fig.9	–	3.8	–	V
I_I	input current		–	1.0	–	μA
CLAMP INPUT (PIN 24)						
V_{24}	clamp voltage for code 128 output		–	3.5	–	V
I_{24}	clamp output current		see Table 2			

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
$V_{19(p-p)}$	AC output voltage (peak-to-peak value)	V_{OF} = 1.33 V (p-p); V_{25} = 3.0 V	–	1.33	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	V_{ANOUT} = 1.33 V (p-p); note 2	–	–	1.0	mA
V_{19}	DC output voltage for black level	CLS = logic 1	–	V_{CCA} – 2.02	–	V
V_{19}	DC output voltage for black level	CLS = logic 0	–	V_{CCA} – 2.6	–	V
Z_{19}	output impedance		–	20	–	Ω
Preamplifier dynamic characteristics						
α_{ct}	crosstalk between VIN inputs	V_{CCA} = 4.75 to 5.25 V; note 3	–	–50	–45	dB
G_{diff}	differential gain	V_{VIN} = 1.33 V (p-p); V_{25} = 3.0 V	–	2	–	%
φ_{diff}	differential phase	V_{VIN} = 1.33 V (p-p); V_{25} = 3.0 V	–	0.8	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 4	60	–	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	45	–	dB
ΔG	gain range	see Fig.9	–4.5	–	+6.0	dB
G_{stab}	gain stability as a function of supply voltage and temperature	see Fig.9	–	–	5	%
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	100	μA
$\lvert Z_i \rvert$	input impedance	f_{clk} = 10 MHz	–	4	–	kΩ
C_I	input capacitance	f_{clk} = 10 MHz	–	4.5	–	pF
FOEN INPUT (SEE TABLE 3)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_9 = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_9 = 2.7 V	–	–	20	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADCIN INPUT (PIN 20; SEE TABLE 4)						
V_{20}	input voltage	digital output = 00	–	V_{CCA} – 2.52	–	V
V_{20}	input voltage	digital output = 255	–	V_{CCA} – 1.52	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	1.0	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f_i = 6 MHz	–	50	–	MΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
DIGITAL OUTPUTS D0 TO D7						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_{OL} = −0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	−20	–	+20	μA
Switching characteristics						
$f_{clk(max)}$	maximum clock input frequency	see Fig.5; note 6	30	32	–	MHz
Analog signal processing (f_{clk} = 32 MHz; see Fig.7)						
G_{diff}	differential gain	V_{20} = 1.0 V (p-p); see Fig.6; note 7	–	2	–	%
φ_{diff}	differential phase	see Fig.6; note 7	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 7	–	–	0	dB
f_{all}	harmonics (full-scale); all components	f_i = 4.43 MHz; note 7	–	−55	–	dB
SVRR2	supply voltage ripple rejection	note 8	–	1	5	%/V
Transfer function						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 9	–	–	±2	LSB
Timing (f_{clk} = 32 MHz; see Figs 5, 6 and 7)						
DIGITAL OUTPUTS (C_L = 15 pF; I_{OL} = 2 mA; R_L = 2 kΩ)						
t_{ds}	sampling delay time		–	2	–	ns
t_h	output hold time		–	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time; output enable		–	16	25	ns
t_{dDZ}	3-state delay time; output disable		–	12	25	ns

Notes to the "Characteristics"

1. 0 dB is obtained at the AGC amplifier when applying $V_{i(p-p)}$ = 1.33 V.
2. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referenced to V_{CCA} and defined as:
   a) AC impedance ≥1 kΩ and the DC impedance >2.7 kΩ.
   b) The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
3. Input signals with the same amplitude. Gain is adjusted to obtain ANOUT = 1.33 V (p-p).
4. Signal-to-noise ratio measured with 5 MHz bandwidth:

   $$\frac{S}{N} = 20 \log \frac{V_{ANOUT(p-p)}}{V_{ANOUT\ (RMS\ noise)}} \text{ at } B = 5 \text{ MHz.}$$

5. The voltage ratio is expressed as:

   $$SVRR1 = 20 \log \frac{\Delta V_{CCA}}{V_{CCA}} \times \frac{G}{\Delta G}$$ for V_I = 1 V (p-p), gain at 100 kHz = 1 and 1 V supply variation.

6. It is recommended that the rise and fall times of the clock are ≥2 ns. In addition, a 'good layout' for the digital and analog grounds is recommended.
7. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
8. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

   $$SVRR2 = \frac{\Delta (V_{I(00)} - V_{I(FF)}) + (V_{I(00)} - V_{I(FF)})}{\Delta V_{CCA}}$$

9. Full-scale sine wave (f_i = 4.4 MHz; f_{clk} = 27 MHz).

Table 1 Video input selection (CVBS).

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN1

Table 2 CLAMP output current.

CLS	CLP	DIGITAL OUTPUT	I_{CLAMP}
1	1	output < 128	+50 μA
		output > 128	−50 μA
X(1)	0	X	0 μA
0	1	output < 16	+50 μA
		16 < output	−50 μA

Note

1. X = don't care.

Table 3 FOEN input coding.

FOEN	D0 TO D7
0	active, two's complement
1	high impedance

Table 4 Output coding and input voltage (typical values).

STEP	V_{ADCIN}	BINARY OUTPUTS								TWO'S COMPLEMENT							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	–	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} − 2.52 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	–	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} − 1.52 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
Overflow	–	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

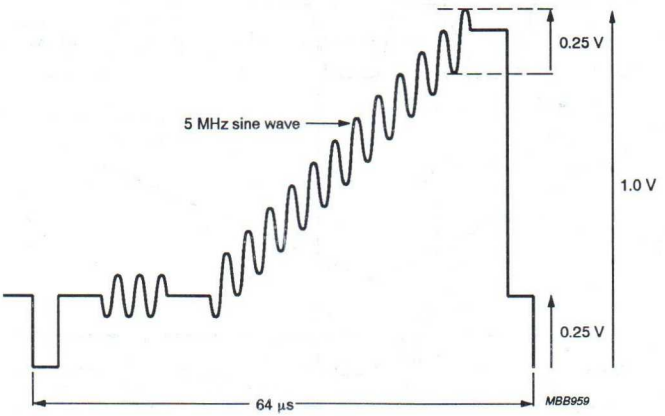


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

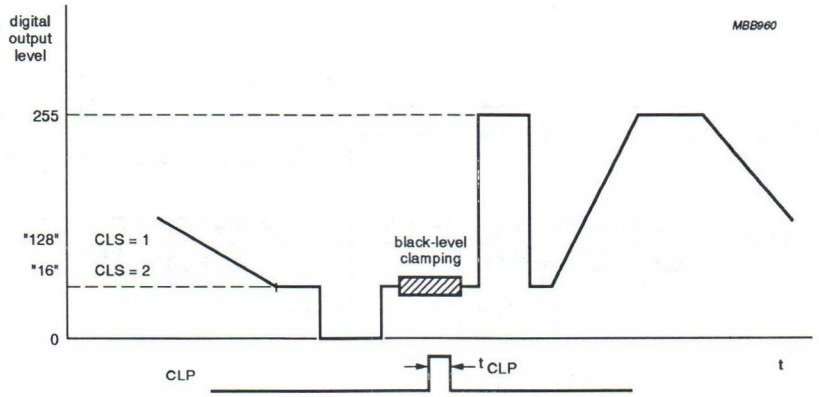


Fig.4 Control mode selection.

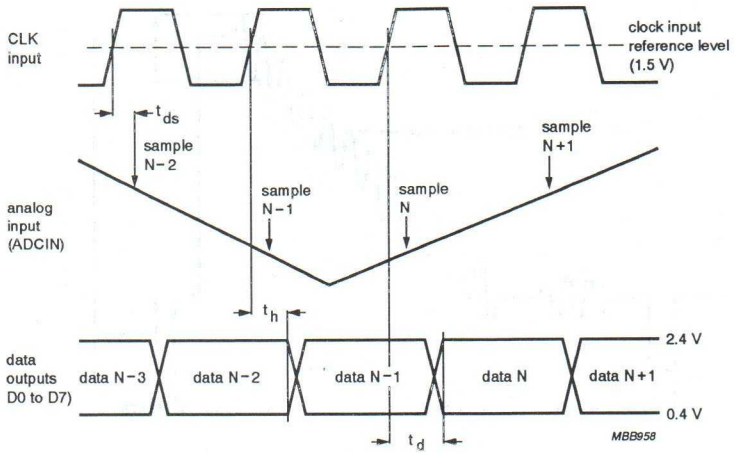


Fig.5 Timing diagram.

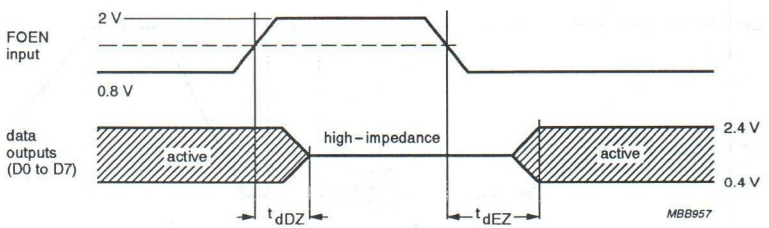


Fig.6 Output format timing diagram.

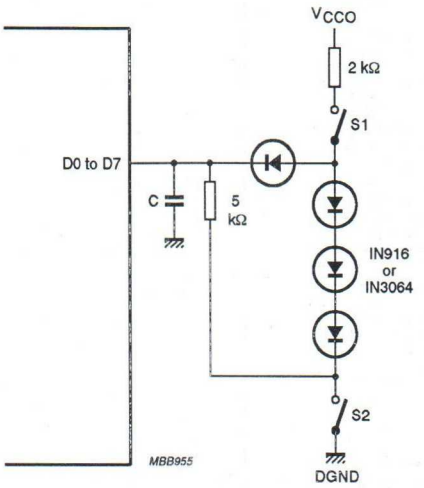


Fig.7 Load circuit for timing measurement; data outputs (FOEN = LOW).

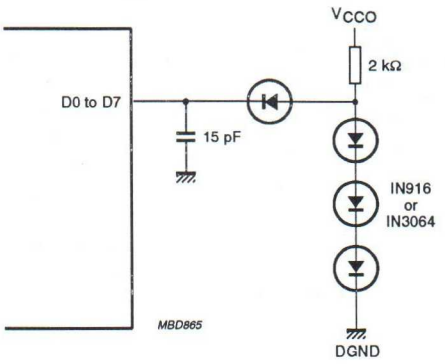
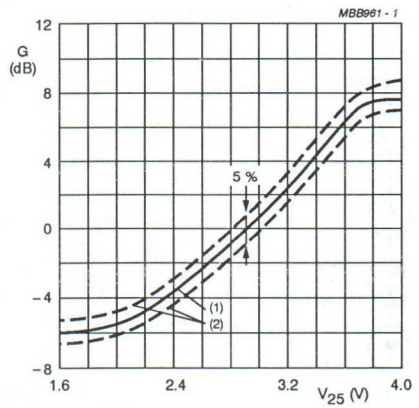


Fig.8 Load circuit for timing measurement; 3-state outputs (FOEN: f_i = 1 MHz; V_{FOEN} = 3 V).



(1) Typical value ($V_{CCA} = V_{CCD} = 5$ V; $T_{amb} = 25$ °C).
(2) Minimum and maximum values (temperature and supply).

Fig.9 Typical gain control curve as a function of gain voltage.

INTERNAL PIN CIRCUITRY

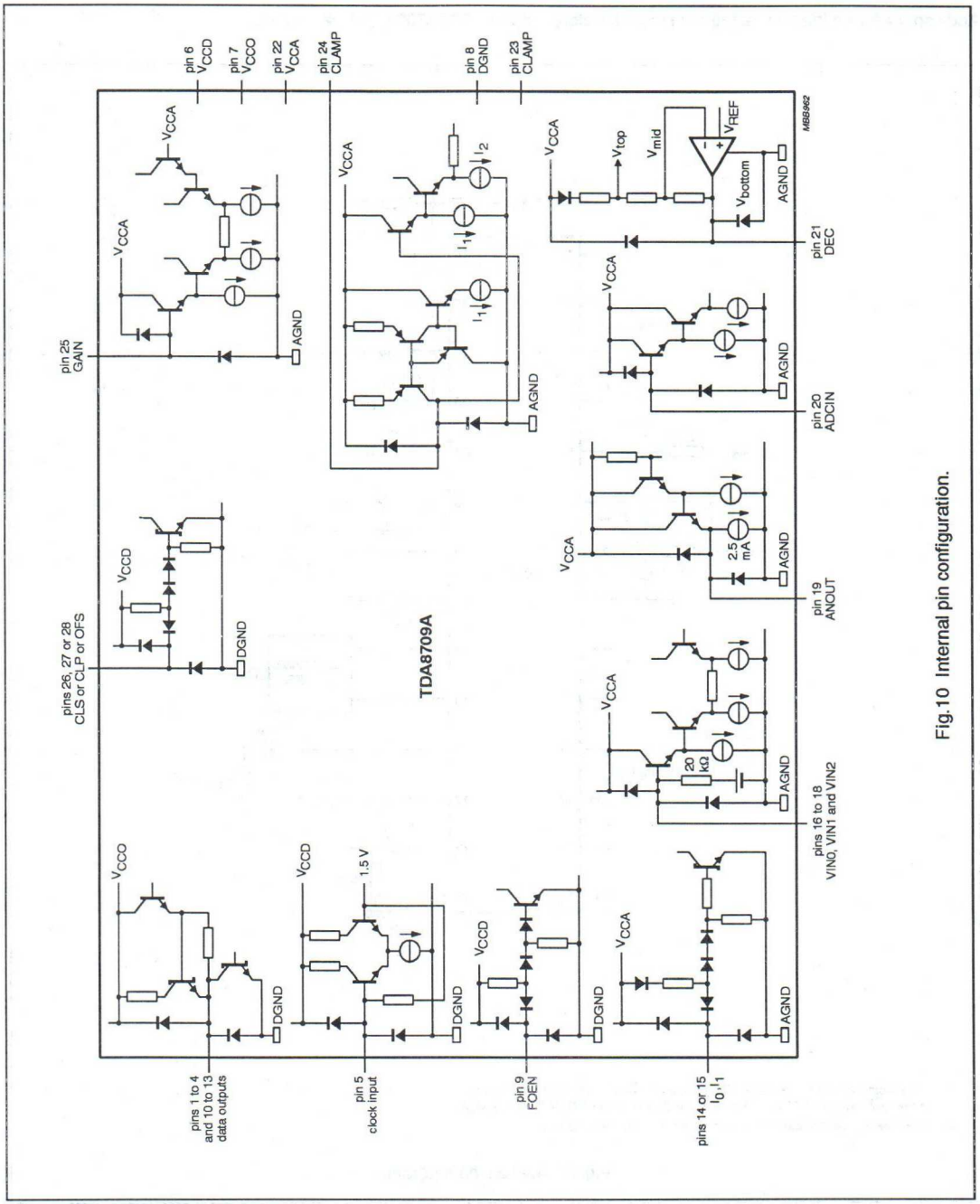
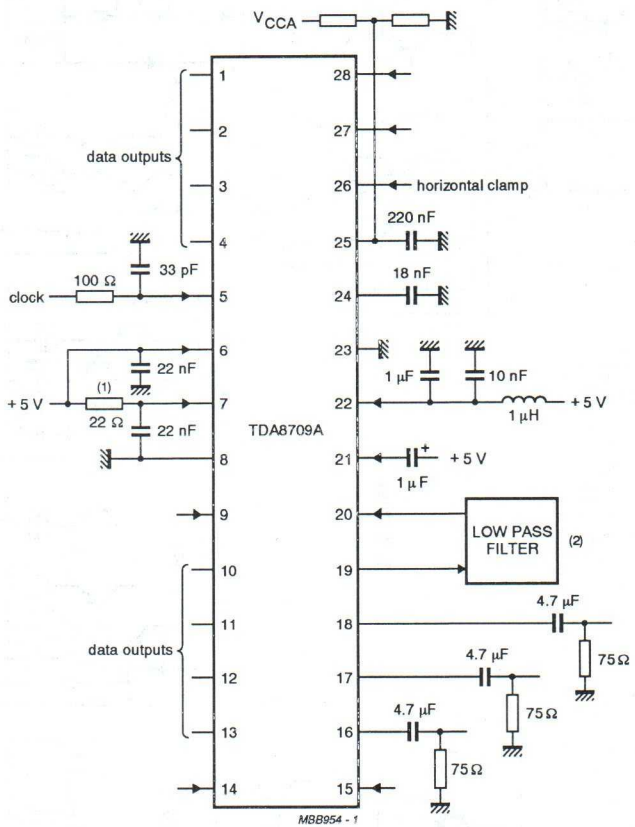


Fig.10 Internal pin configuration.

APPLICATION INFORMATION

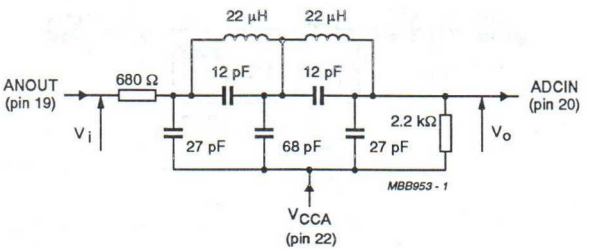
Additional information can be found in the laboratory report of TDA8708A *"FBL/AN9308"*.



(1) It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of TDA8709A interfaces with a capacitive CMOS load device.

(2) See Figs 12, 14, 16 and 18 for examples of the low-pass filters.

Fig.11 Application diagram.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.12 Example of a low-pass filter for RGB and C signals.

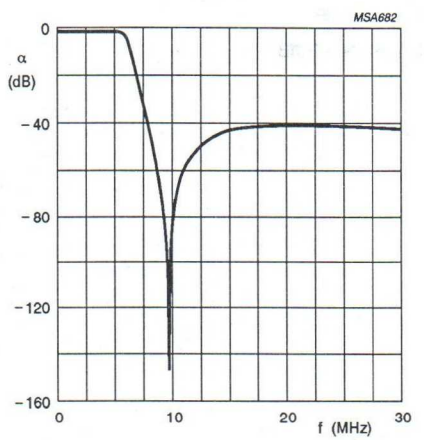
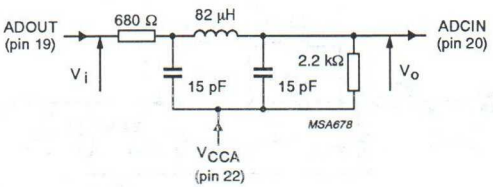


Fig.13 Frequency response for filter shown in Fig.12.

Characteristics of Fig.13

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at –3 dB
- f_{notch} = 9.65 MHz.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.14 Example of an economical low-pass filter for RGB and C signals.

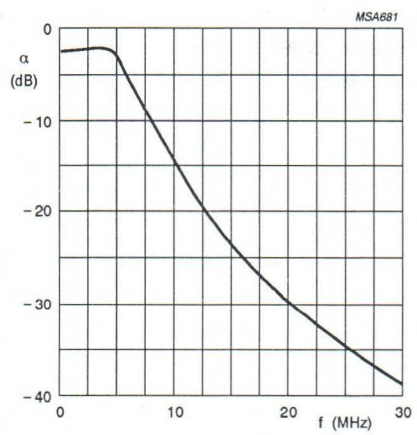
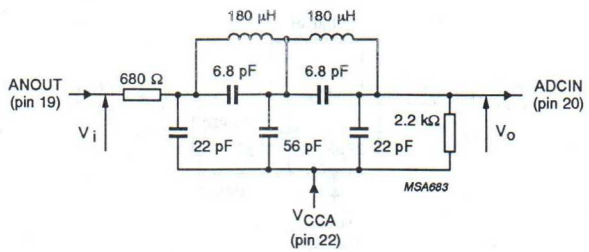


Fig.15 Frequency response for filter shown in Fig.14.

Characteristics of Fig.15

- Order 3; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at −3 dB.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.16 Example of a low-pass filter for U and V signals.

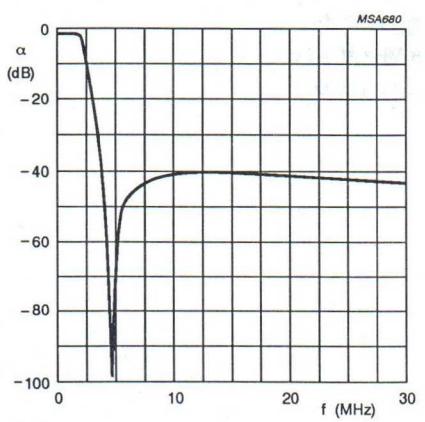
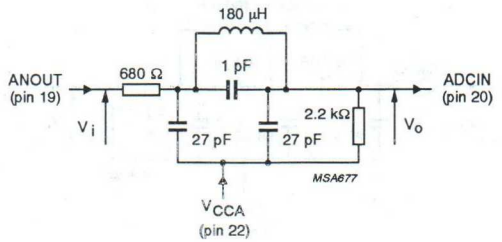


Fig.17 Frequency response for filter shown in Fig.16.

Characteristics of Fig.17

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 2.3 MHz at −3 dB
- f_{notch} = 4.5 MHz.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.18 Example of an economical low-pass filter for U and V signals.

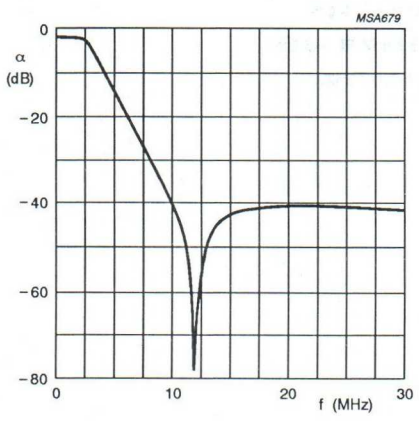


Fig.19 Frequency response for filter shown in Fig.18.

Characteristics of Fig.19

- Order 3; adapted CHEBYSHEV
- Ripple $\rho \leq 0.3$ dB
- f = 2.8 MHz at −3 dB
- f_{notch} = 11.9 MHz.

8-bit high-speed analog-to-digital converter — TDA8713

FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.5 effective bits at 4.43 MHz full-scale input at a 40 MHz clock frequency
- Binary or two's complement 3-state TTL outputs
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- External reference voltage generator
- Power dissipation only 290 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample and hold circuit required

APPLICATIONS

- High-speed analog-to-digital conversion for:
  - video data digitizing
  - radar pulse analysis
  - transient signal analysis
  - high energy physics research
  - ΣΔ modulators
  - medical imaging

DESCRIPTION

The TDA8713 is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8713	24	DIL	plastic	SOT101
TDA8713T	24	SO24	plastic	SOT137A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		-	18	26	mA
I_{CCD}	digital supply current		-	19	25	mA
I_{CCO}	output stages supply current		-	11	14	V
ILE	DC integral linearity error		-	-	±0.75	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
AILE	AC integral linearity error	note 1	-	-	±2	LSB
B	−3 dB bandwidth	note 2; f_{CLK} = 40 MHz	-	19.5	-	MHz
$f_{CLK}/f_{\overline{CLK}}$	maximum clock frequency	note 3	50	-	-	MHz
P_{tot}	total power dissipation		-	290	415	mW

Notes to the Quick Reference Data

1. Full-scale sinewave (f_i = 4.4 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 27 MHz).

2. The −3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at input).

3. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:

   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak- to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

   If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

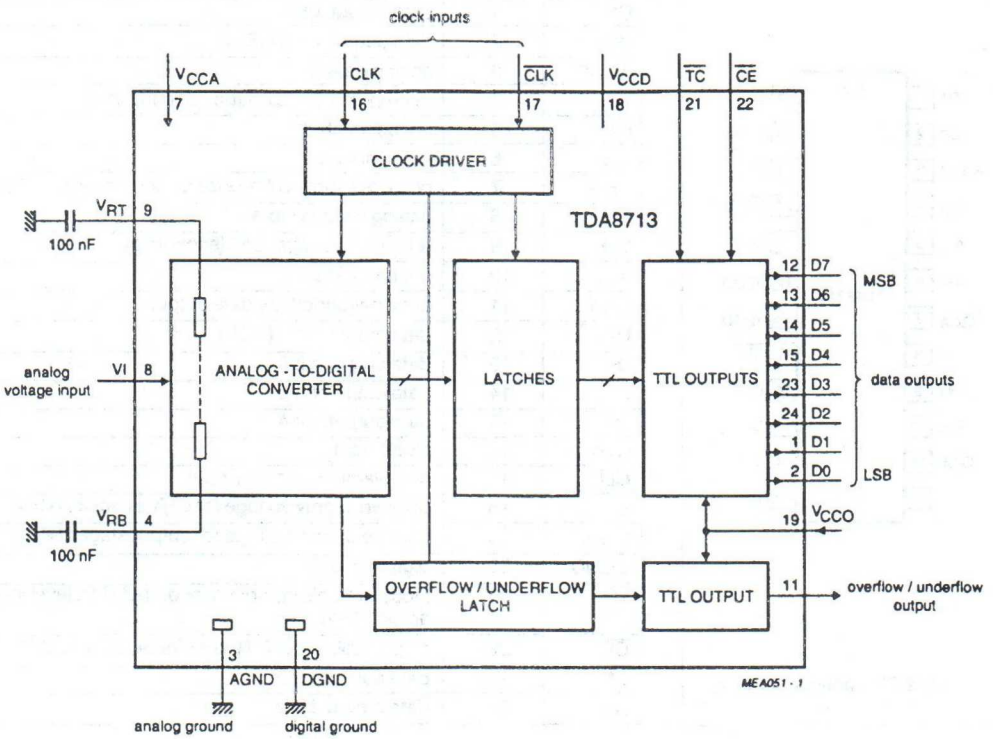


Fig.1 Block diagram.

PIN CONFIGURATION

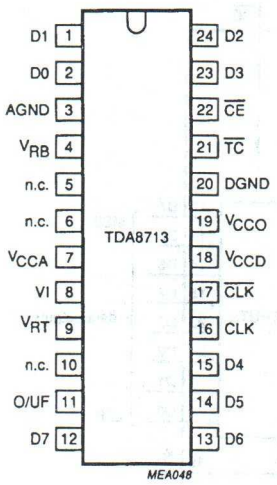


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output, bit 0 (LSB)
AGND	3	analog ground
V_{RB}	4	reference voltage bottom (decoupling)
n.c.	5	not connected
n.c.	6	not connected
V_{CCA}	7	positive supply voltage for analog circuits (+5 V)
VI	8	analog voltage input
V_{RT}	9	reference voltage top (decoupling)
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output, bit 7 (MSB)
D6	13	data output, bit 6
D5	14	data output, bit 5
D4	15	data output, bit 4
CLK	16	clock input
$\overline{CLK}$	17	complementary clock input
V_{CCD}	18	positive supply voltage for digital circuits (+5 V)
V_{CCO}	19	positive supply voltage for output stages (+5 V)
DGND	20	digital ground
$\overline{TC}$	21	input for two's complement output (TTL level input, active LOW)
$\overline{CE}$	22	chip enable input (TTL level input, active LOW)
D3	23	data output, bit 3
D2	24	data output, bit 2

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	see note 1	−0.3	7.0	V
V_{CCD}	digital supply voltage range	see note 1	−0.3	7.0	V
V_{CCO}	output stages supply voltage	see note 1	−0.3	7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCO} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCA} - V_{CCO}$	supply voltage differences		−1.0	1.0	V
V_{VI}	input voltage range	referenced to AGND	1.2	7.0	V
$V_{\overline{CLK}}$ / V_{CLK}	AC input voltage for switching (peak-to-peak value)	see note 2; referenced to DGND	-	2.0	V
I_O	output current		-	+10	mA
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		0	+70	°C
T_j	junction temperature		-	+125	°C

Notes to the Ratings

1. The supply voltages V_{CCA} and V_{CCD} may have any value between −0.3 V and +7.0 V as long as the difference V_{CCA} - V_{CCD} lies between −1 V and + 1 V.

2. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:

- TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
- TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
- AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

  If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT101	+ 55	K/W
$R_{th\ j\text{-}a}$	SOT137A	+ 75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{CCA} = V_7 - V_3 = 4.75$ V to 5.25 V; $V_{CCD} = V_{18} - V_{20} = 4.75$ V to 5.25 V; $V_{CCO} = V_{19} - V_{20} = 4.75$ V to 5.25 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $T_{amb} = 0$ °C to +70 °C; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5.0$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		-	18	26	mA
I_{CCD}	digital supply current		-	19	25	mA
I_{CCO}	output stage supply current	all outputs LOW	-	11	14	mA
Inputs						
CLOCK INPUT CLK AND $\overline{CLK}$ (note 1; referenced to DGND)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_{CLK}/V_{\overline{CLK}} = 0.4$ V	−400	-	-	µA
I_{IH}	input current HIGH	$V_{CLK}/V_{\overline{CLK}} = 2.7$ V	-	-	100	µA
		$V_{CLK}/V_{\overline{CLK}} = V_{CCD}$	-	-	300	µA
Z_o	input impedance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	-	4	-	kΩ
C_i	input capacitance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	-	4.5	-	pF
$V_{CLK(p-p)} - V_{\overline{CLK}(p-p)}$	AC input voltage for switching (peak-to-peak value)	note 1; DC level = 1.5 V	0.5	-	2.0	V
INPUTS $\overline{TC}$ AND $\overline{CE}$ (referenced to DGND)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_{IL} = 0.4$ V	−400	-	-	µA
I_{IH}	input current HIGH	$V_{IH} = 2.7$ V	-	-	20	µA
VI (analog input voltage referenced to AGND)						
I_{IL}	input current LOW	$V_{VI} = 1.6$ V	-	0	-	µA
I_{IH}	input current HIGH	$V_{VI} = 3.8$ V	60	120	180	µA
Z_o	input impedance	$f_i = 1$ MHz	-	10	-	kΩ
C_i	input capacitance	$f_i = 1$ MHz	-	14	-	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference voltages for the resistor ladder						
V_{RB}	reference voltage LOW		1.5	1.6	1.9	V
V_{RT}	reference voltage HIGH		3.5	3.8	3.9	V
V_{REF}	differential reference voltage V_{RT}-V_{RB}		2	2.2	-	V
I_{REF}	reference current		-	10	-	mA
R_{LAD}	resistor ladder		-	200	-	Ω
R_{TLC}	temperature coefficient of the ladder		-	0.24	-	Ω/°C
V_{OB}	voltage offset bottom	note 5	-	258	-	mV
V_{OBTC}	voltage offset bottom temperature coefficient	note 5	-	0.1	-	mV/°C
V_{OT}	voltage offset top	note 5	-	132	-	mV
V_{OTTC}	voltage offset top temperature coefficient	note 5	-	−0.3	-	mV/°C
Outputs DIGITAL OUTPUTS (D7 - D0) (referenced to DGND)						
V_{OL}	output voltage LOW	I_O = 1 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_O = −0.4 mA	2.7	-	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	−20	-	20	µA
Switching characteristics (note 1,2; see Fig.3)						
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		50	-	-	MHz
Analog signal processing (f_{CLK} = 50 MHz)						
B	−3 dB bandwidth	note 3	-	19.5	-	MHz
G_d	differential gain	note 4	-	0.3	2.0	%
ϕ_d	differential phase	note 4	-	0.4	1.5	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	0	0	0	dB
F_{even}	even harmonics (full-scale)	f_i = 4.43 MHz	-	−65	-	dB
F_{odd}	odd harmonics (full scale)	f_i = 4.43 MHz	-	−55	-	dB
Transfer function (f_{CLK} = 50 MHz)						
ILE	DC integral linearity error		-	-	±0.75	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
AILE	AC integral linearity error	note 6	-	-	±2	LSB
EB	effective bits f_i = 1 MHz	f_{CLK} = 20MHZ	-	7.8	-	bits
EB	effective bits f_i = 4.43 MHz	f_{CLK} = 40MHZ	-	7.5	-	bits
EB	effective bits f_i = 4.43 MHz	f_{CLK} = 50MHZ	-	7.2	-	bits
Timing (note 7; see Figs 3 to 6; f_{CLK} = 50 MHz)						
t_{dS}	sampling delay		-	-	2	ns
t_{HD}	output hold time		6	-	-	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	-	8	10	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	-	14	16	ns
t_{dZH}	3-state output delay times	enable-to-HIGH	-	19	25	ns
t_{dZL}	3-state output delay times	enable-to-LOW	-	16	20	ns
t_{dHZ}	3-state output delay times	disable-to-HIGH	-	14	20	ns
t_{dLZ}	3-state output delay times	disable-to-LOW	-	9	12	ns

Notes to the characteristics

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

   If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.
2. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 2 ns.
3. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).
4. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.
5. Analog input voltages producing code 00 up to and including FF
   - V_{OB} (voltage offset bottom) is the difference between the analog input which produces data equal to 00 and the reference voltage bottom (V_{RB}) at T_{amb} = 25 °C.
   - V_{OBTC} (voltage offset bottom temperature coefficient) is the dependence of V_{OB} with temperature.
   - V_{OT} (voltage offset top) is the difference between V_{RT} (reference voltage top) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
   - V_{OTTC} (voltage offset top temperature coefficient) is the dependence of V_{OT} with temperature.
6. Full-scale sinewave (f_i = 4.4 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 27 MHz).
7. Output data acquisition
   - Output data is available after the maximum delay of t_{dHL} and t_{dLH}.
   - Output data is fully stable during the low level of the clock. Thus it is recommended that acquisition of this data is made after the falling edge of the clock, instead of after the maximum (t_{dHL}, t_{dLH}).

Table 1 Output coding and input voltage (typical values; referenced to AGND, V_{RB} = 1.6 V, V_{RT} = 3.8 V)

			BINARY OUTPUT BITS								TWO'S COMPLEMENT OUTPUT BITS							
STEP	$V_{VI(P-P)}$	O/UF	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow	<1.858	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1.858	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	.	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	3.668	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow	>3.668	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

Table 2 Mode selection

$\overline{TC}$	$\overline{CE}$	D7 - D0	O/UF
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

Where: X = don't care.

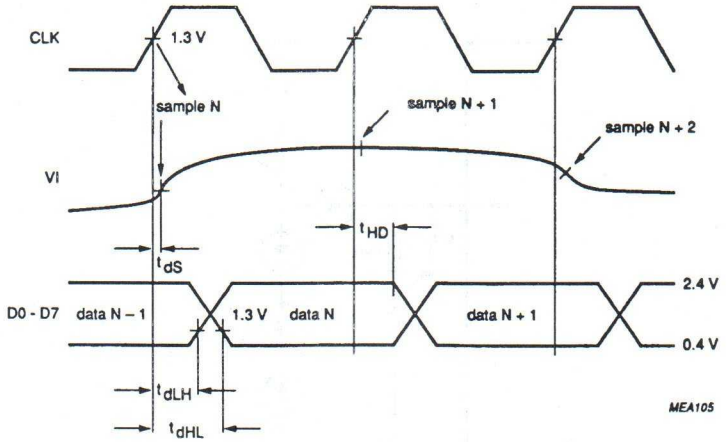


Fig.3 Timing diagram.

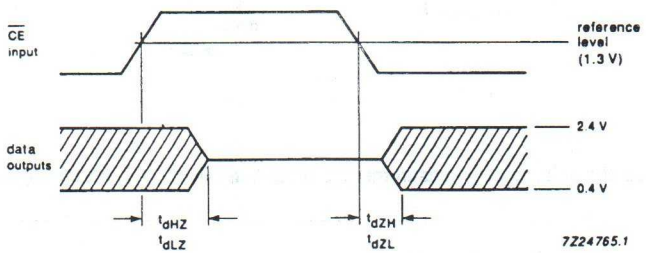


Fig.4 3-state delay timing diagram.

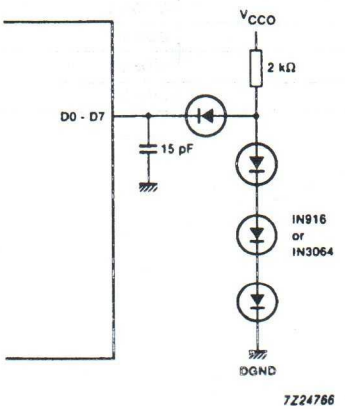


Fig.5 Load circuit for timing measurement; data outputs ($\overline{CE}$ = LOW).

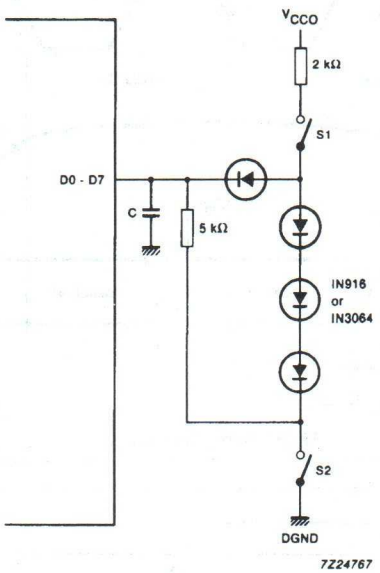


Fig.6 Load circuit for timing measurement; 3-state outputs ($\overline{CE}$: f_i = 1 MHz; V_{VI} = 3 V).

Note to Fig.6

TIMING MEASUREMENT	SWITCH S1	SWITCH S2	CAPACITOR C
t_{dZH}	open	closed	15 pF
t_{dZL}	closed	open	15 pF
t_{dHZ}	closed	closed	5 pF
t_{dLZ}	closed	closed	5 pF

INTERNAL PIN CONFIGURATIONS

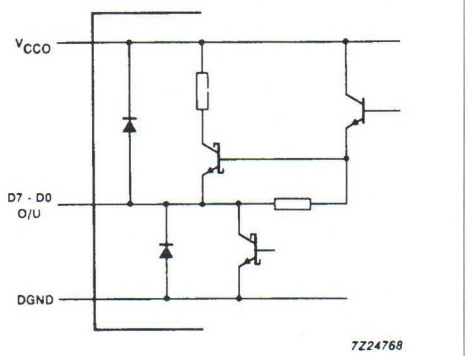


Fig.7 TTL data and overflow/underflow outputs.

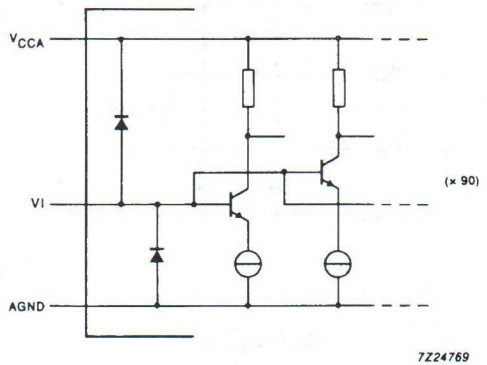


Fig.8 Analog inputs.

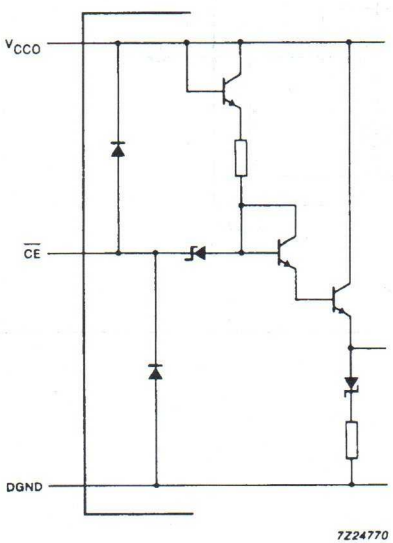


Fig.9 $\overline{CE}$ (3-state) input.

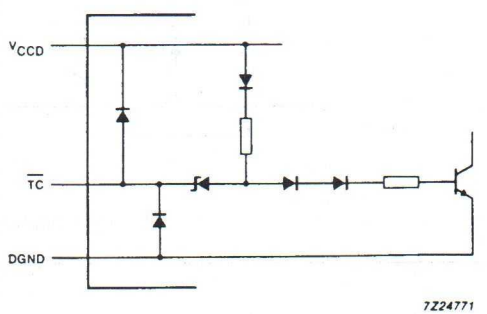


Fig.10 $\overline{TC}$ (two's complement) input.

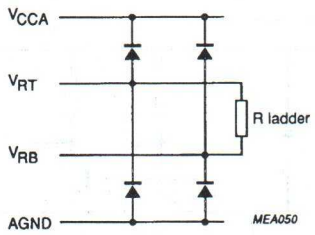


Fig.11 V_{RB}, V_{RT}.

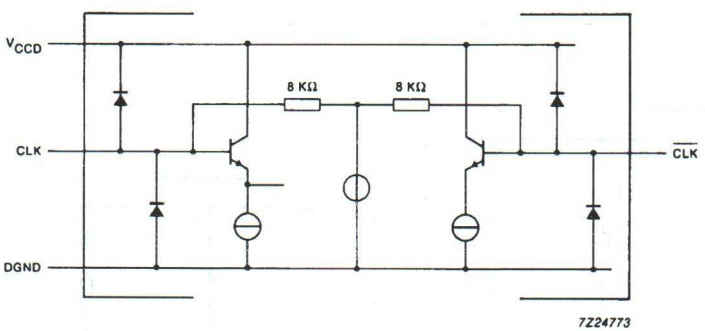


Fig.12 CLK and $\overline{CLK}$ inputs.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/9001).

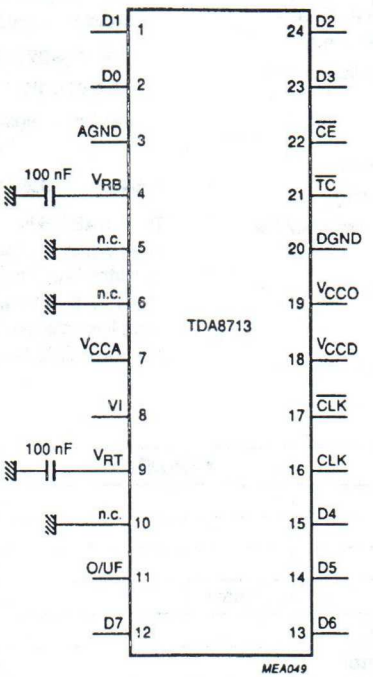


Fig.13 Application diagram.

Notes to Fig.13

1. $\overline{CLK}$ should be decoupled to the DGND with a 100 nF capacitor, if pin CLK is used (see 'Notes to the characteristics', note 1).
2. CLK and $\overline{CLK}$ can be used in a differential mode (see 'Notes to the characteristics', note 1).
3. V_{RB} and V_{RT} are decoupled to AGND.
4. Analog and digital supplies should be separated and decoupled.
5. Pins 5,6 and 10 should be connected to AGND in order to prevent noise influence.
6. The external voltage regulator must be build in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.

8-bit high-speed analog-to-digital converter — TDA8715

FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.5 effective bits at 4.43 MHz full-scale input at a 40 MHz clock frequency)
- ECL (10KH family) compatible digital inputs and outputs
- Overflow/underflow ECL output
- Low-level AC clock input signal allowed
- Power dissipation only 325 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

- High-speed analog-to-digital conversion for:
  video data digitizing
  radar pulse analysis
  transient signal analysis
  high energy physics research
  ΣΔ modulators
  medical imaging.

GENERAL DESCRIPTION

The TDA8715 is a bipolar 8-bit high-speed analog-to-digital converter (ADC) for profesional video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are 10KH ECL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		−4.7	−5.2	−5.7	V
V_{EED}	digital supply voltage		−4.7	−5.2	−5.7	V
I_{EEA}	analog supply current		−	20	25	mA
I_{EED}	digital supply current	see note 1	−	52	60	mA
ILE	DC integral linearity error		−	±0.4	±0.75	LSB
DLE	DC differential linearity error		−	±0.25	±0.5	LSB
EB	effective bits	f_i = 4.43 MHz; f_{CLK} = 50 MHz	−	7.2	−	bits
f_{CLK}; $\overline{f_{CLK}}$	maximum clock frequency		50	−	−	MHz
T_{amb}	operating ambient temperature		0	−	+125	°C
P_{tot}	total power dissipation	see note 1	−	325	425	mW

Note

1. All digital outputs are connected to V_{EED} via 2.2 kΩ resistors.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8715	18	DIL	plastic	SOT102
TDA8715T	20	SO20	plastic	SOT163A

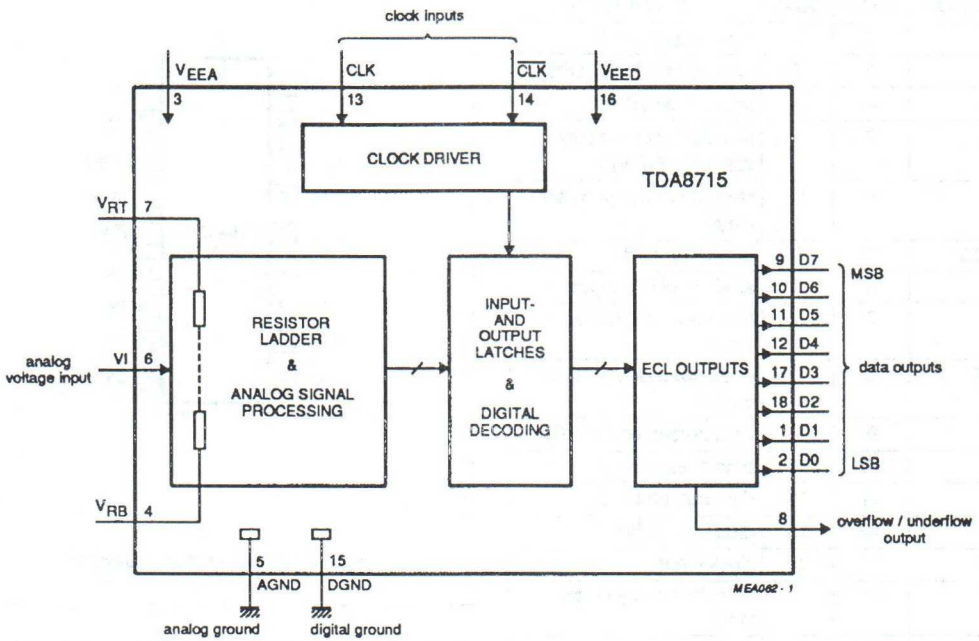


Fig.1 Block diagram.

PINNING

SYMBOL	DIL18	SO20	DESCRIPTION
D1	1	1	data output; bit 1
D0	2	2	data output; bit 0 (LSB)
n.c.	–	3	not connected
V_{EEA}	3	4	analog negative supply voltage (–5.2 V)
V_{RB}	4	5	reference voltage bottom input
AGND	5	6	analog ground
VI	6	7	analog voltage input
V_{RT}	7	8	reference voltage top input
O/UF	8	9	overflow/underflow data output
D7	9	10	data output; bit 7(MSB)
D6	10	11	data output; bit 6
D5	11	12	data output; bit 5
D4	12	13	data output; bit 4
CLK	13	14	clock input
$\overline{CLK}$	14	15	complementary clock input
DGND	15	16	digital ground
V_{EED}	16	17	digital negative supply voltage (–5.2 V)
n.c.	–	18	not connected
D3	17	19	data output; bit 3
D2	18	20	data output; bit 2

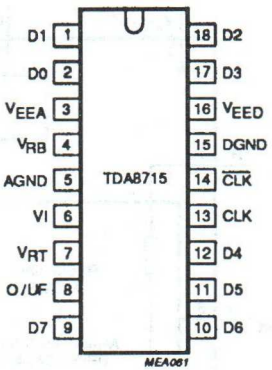


Fig.2 Pin configuration; TDA8715.

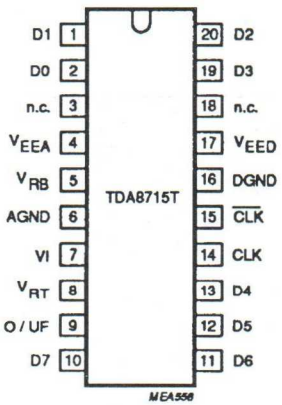


Fig.3 Pin configuration; TDA8715T.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage		−7	0.3	V
V_{EED}	digital supply voltage		−7	0.3	V
VI	analog input voltage		−7	0.3	V
V_{CLK}; $V_{\overline{CLK}}$	AC input voltage for switching (peak-to-peak value)	see note 1	−	2.0	V
I_O	output current		−15	+10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+150	°C

Note

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

   Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals or with two complementary sinewave signals, imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal

   Asymmetrical drive modes; When driving the CLK input directly with an ECL signal or a sinewave signal imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal

   When driving the CLK input with an ECL signal only (Asymmetrical drive modes), it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT102	65 K/W
	SOT163A	80 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{EEA} = V_3 - V_5 = -4.7$ V to -5.7 V; $V_{EED} = V_{16} - V_{15} = -4.7$ V to -5.7 V; AGND and DGND shorted together; $T_{amb} = 0$ °C to +70 °C; unless otherwise specified (typical values measured at $V_{EEA} = -5.2$V; $V_{EED} = -5.2$ V and $T_{amb} = 25$ °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{EEA}	analog supply voltage		−4.7	−5.2	−5.7	V
V_{EED}	digital supply voltage		−4.7	−5.2	−5.7	V
I_{EEA}	analog supply current		–	20	25	mA
I_{EED}	digital supply current	note 1	–	52	60	mA
$V_{EEA}-V_{EED}$	supply voltage difference		−0.5	0	+0.5	V
Reference voltages for the resistor ladder						
V_{RB}	LOW level reference voltage		−3.2	−3.0	−2.7	V
V_{RT}	HIGH level reference voltage		−0.9	−0.6	−0.4	V
V_{REF}	differential reference voltage $V_{RT}-V_{RB}$		2.3	2.4	–	V
I_{REF}	reference current		–	12.6	–	mA
R_{LAD}	resistor ladder		–	200	–	Ω
TC_{RL}	temperature coefficient of the ladder		–	0.24	–	Ω/K
V_{OB}	voltage offset bottom	note 2	–	280	–	mV
TC_{VOB}	temperature coefficient voltage offset bottom	note 2	–	0.1	–	mV/K
V_{OT}	voltage offset top	note 2	–	245	–	mV
TC_{VOT}	temperature coefficient voltage offset top	note 2	–	0.1	–	mV/K
Inputs						
CLK INPUT (NOTE 3)						
V_{IL}	LOW level input voltage		−1.85	−1.77	−1.65	V
V_{IH}	HIGH level input voltage		−0.96	−0.88	−0.81	V
I_{IL}	LOW level input current	$V_{CLK} = -1.77$ V	–	−240	–	µA
I_{IH}	HIGH level input current	$V_{CLK} = -0.88$ V	–	−14	–	µA
R_I	input resistance					
		$f_{CLK} = 10$ MHz	–	7	–	kΩ
		$f_{CLK} = 50$ MHz	–	3.5	–	kΩ
C_I	input capacitance					
		$f_{CLK} = 10$ MHz	–	1.8	–	pF
		$f_{CLK} = 50$ MHz	–	1.55	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\overline{CLK}$ INPUT (NOTE 3)						
V_{IL}	LOW level input voltage		−1.85	−1.77	−1.65	V
V_{IH}	HIGH level input voltage		−0.96	−0.88	−0.81	V
I_{IL}	LOW level input current	$V_{\overline{CLK}}$ = −1.77 V	−	−140	−	μA
I_{IH}	HIGH level input current	$V_{\overline{CLK}}$ = −0.88 V	−	75	−	μA
R_I	input resistance					
		$f_{\overline{CLK}}$ = 10 MHz	−	9.3	−	kΩ
		$f_{\overline{CLK}}$ = 50 MHz	−	4.5	−	kΩ
C_I	input capacitance					
		$f_{\overline{CLK}}$ = 10 MHz	−	2.6	−	pF
		$f_{\overline{CLK}}$ = 50 MHz	−	2.4	−	pF
$V_{CLK} - V_{\overline{CLK}}$	AC input voltage for switching (peak-to-peak value)		0.5	0.9	1.1	V
V_I (ANALOG INPUT; V_{RB} = −3.1 V AND V_{RT} = −0.6 V)						
I_{IL}	LOW level input current	data output 00	−	0	−	μA
I_{IH}	HIGH level input current	data output FF	−	120	−	μA
R_I	input resistance	f_i = 1 MHz	−	9.4	−	kΩ
C_I	input capacitance	f_i = 1 MHz	−	13.7	20	pF
Outputs						
DIGITAL OUTPUTS (D7 TO D0 AND O/UF; DIGITAL 10KH ECL OUTPUTS)						
V_{OL}	LOW level output voltage	T_{amb} = 25 °C	−1.95	−1.77	−1.65	V
V_{OH}	HIGH level output voltage	T_{amb} = 25 °C	−0.96	−0.88	−0.81	V
I_{OL}	LOW level output current		−	1.8	4	mA
I_{OH}	HIGH level output current		−	1.8	4	mA
Switching characteristics						
f_{CLK}; $f_{\overline{CLK}}$	maximum clock frequency		50	−	−	MHz
Analog signal processing (f_{CLK} = 50 MHz)						
B	−3 dB bandwidth	note 4	−	20.5	−	MHz
G_{diff}	differential gain	note 5	−	0.3	2.0	%
ϕ_{diff}	differential phase	note 5	−	0.4	1.5	deg
	harmonics (full-scale)	f_i = 4.43 MHz				
	fundamental		0	0	0	dB
	even		−	−60	−	dB
	odd		−	−50	−	dB
Transfer function (f_{CLK} = 50 MHz)						
ILE	DC integral linearity error		−	−	±0.75	LSB
DLE	DC differential linearity error		−	−	±0.5	LSB
AILE	AC integral linearity error	note 6	−	±0.75	−	LSB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EB	effective bits					
	f_i = 600 kHz	f_{CLK} = 20 MHZ	–	7.8	–	bits
	f_i = 4.43 MHz	f_{CLK} = 50 MHZ	–	7.2	–	bits
	f_i = 7 MHz	f_{CLK} = 50 MHZ	–	6.9	–	bits
Timing (note 7; see Fig.4; R_L 2.2 kΩ, C_L = 7.5 pF)						
t_{dS}	sampling delay		–	1	3	ns
t_{HD}	output hold time		3	4	–	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	–	7	10	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	–	10	13	ns

Notes

1. All digital outputs connected to V_{EED} via 2.2 kΩ resistors.
2. Analog input voltages producing code 00 up to and including FF

   V_{OB} (voltage offset bottom) is the difference between the analog input which produces data equal to 00 and the reference voltage bottom (V_{RB}) at T_{amb} = 25 °C

   TC_{VOB} (voltage offset bottom temperature coefficient) is dependent on V_{OB} with temperature

   V_{OT} (voltage offset top) is the difference between V_{RT} (reference voltage top) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C

   TC_{VOT} (voltage offset top temperature coefficient) is dependent on V_{OT} with temperature.
3. The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

   Differential drive modes; when driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals or with two complementary sinewave signals, imposed on a DC level of –1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal

   Asymmetrical drive modes; when driving the CLK input directly with a ECL signal or a sinewave signal imposed on a DC level of –1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal

   When driving the CLK input with a ECL signal only (asymmetrical drive modes), it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connect to V_{EED} by a 150 kΩ resistor.
4. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).
5. Low frequency ramp signal ($V_{I(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{I(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.
6. Full-scale sinewave (f_i = 4.43 MHz; f_{CLK}; $f_{\overline{CLK}}$ = 50 MHz).
7. Output data acquisition

   Output data is available after the maximum delay of t_{dHL} and t_{dLH}

   TDA8715 can withstand only one or two 10K ECL loads in order to work out timing at maximum sampling frequency. It is recommended to minimize the PCB load by implementing the load device as close as possible to the TDA8715.

Table 1 Output coding.

STEP	VI (TYP. VALUE)	BINARY OUTPUTS D7 to D0	$\overline{O}$/UFL
Underflow	< –2.789 V	00000000	1
0	–2.783 V	00000000	0
1	–2.775 V	00000001	0
.	.	.....	.
.	.	.....	.
.	.	.....	.
254	.	11111110	0
255	–0.774 V	11111111	0
Overflow	> –0.770 V	11111111	1

Note to Table 1

Typical values: V_{RB} = –3 V, V_{RT} = –0.6 V and VI referenced to AGND.

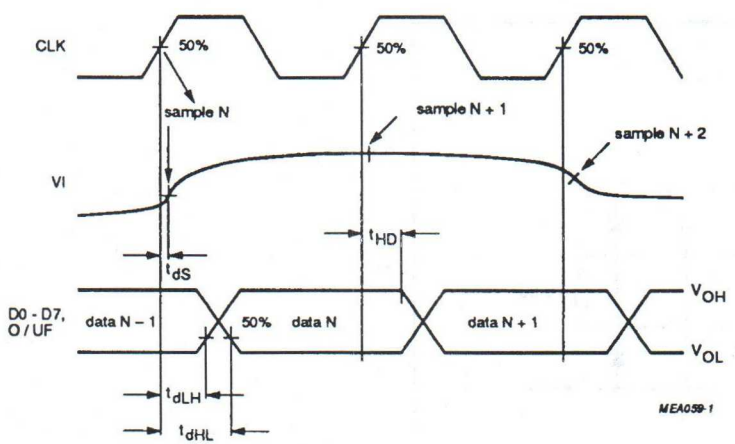


Fig.4 Timing diagram.

INTERNAL PIN CIRCUITRY

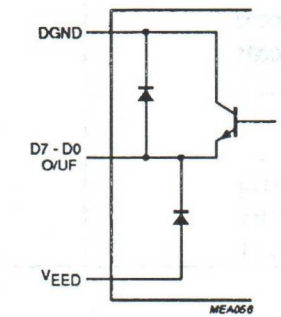


Fig.5 ECL data outputs.

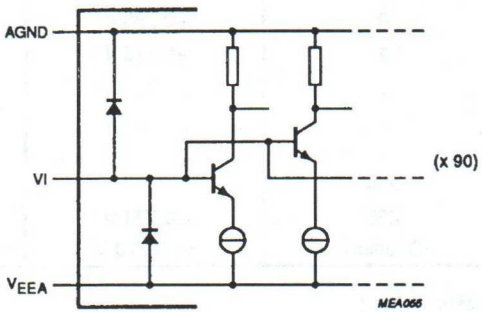


Fig.6 Analog input.

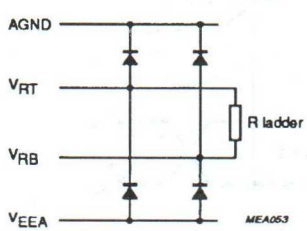


Fig.7 V_{RT} and V_{RB} inputs.

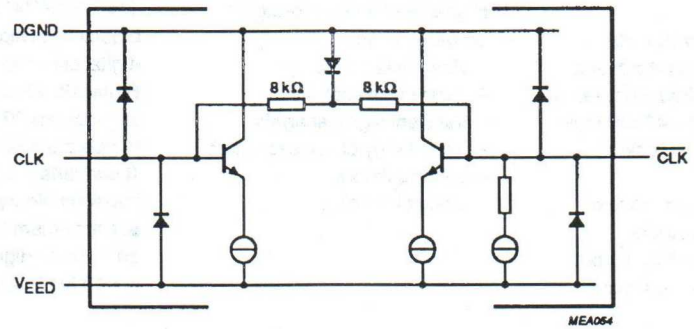
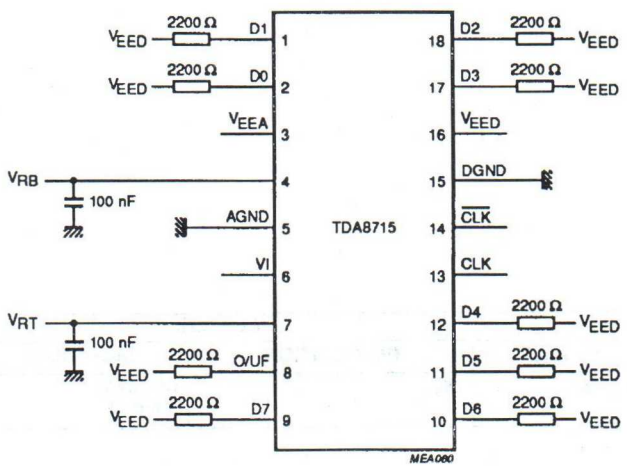


Fig.8 CLK and $\overline{CLK}$ input.

APPLICATION INFORMATION



1. Analog and digital supplies should be separated and decoupled.
2. The external voltage regulator should be configured in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.
3. In the event of a capacitive output load, it is recommended to implement a 22 Ω resistor in series with V_{EED} (pin 16).

Fig.9 Application diagram.

8-bit high-speed analog-to-digital converter (Mil. temp.) TDE8715D

FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.5 effective bits at 4.43 MHz full-scale input at a 50 MHz clock frequency)
- ECL (10KH family) compatible digital inputs and outputs
- Overflow/underflow ECL output
- Low-level AC clock input signal allowed
- Power dissipation only 325 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample and hold circuit required

APPLICATIONS

- High-speed analog-to-digital conversion for:
  - video data digitizing
  - radar pulse analysis
  - transient signal analysis
  - high energy physics research
  - ΣΔ modulators
  - medical imaging

DESCRIPTION

The TDE8715D is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. The operating temperature range is 55 °C up to 125 It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are 10 KH ECL compatible.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDE8715D	18	DIL	ceramic (cerdip)	SOT 133BH3

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		−4.95	−5.2	−5.45	V
V_{EED}	digital supply voltage		−4.95	−5.2	−5.45	V
I_{EEA}	analog supply current		-	20	25	mA
I_{EED}	digital supply current	see note	-	52	60	mA
ILE	DC integral linearity error		-	± 0.4	± 0.75	LSB
DLE	DC differential linearity error		-	± 0.25	± 0.5	LSB
EB	effective bits (f_i = 4.43 MHz)	f_{CLK} = 50 MHz	-	7.2	-	bits
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		50	-	-	MHz
T_{amb}	operating ambient temperature range		−55	-	+125	°C
P_{tot}	total power dissipation	see note	-	325	425	mW

Note to the Quick Reference Data

All digital outputs connected to V_{EED} via 2.2 kΩ resistors.

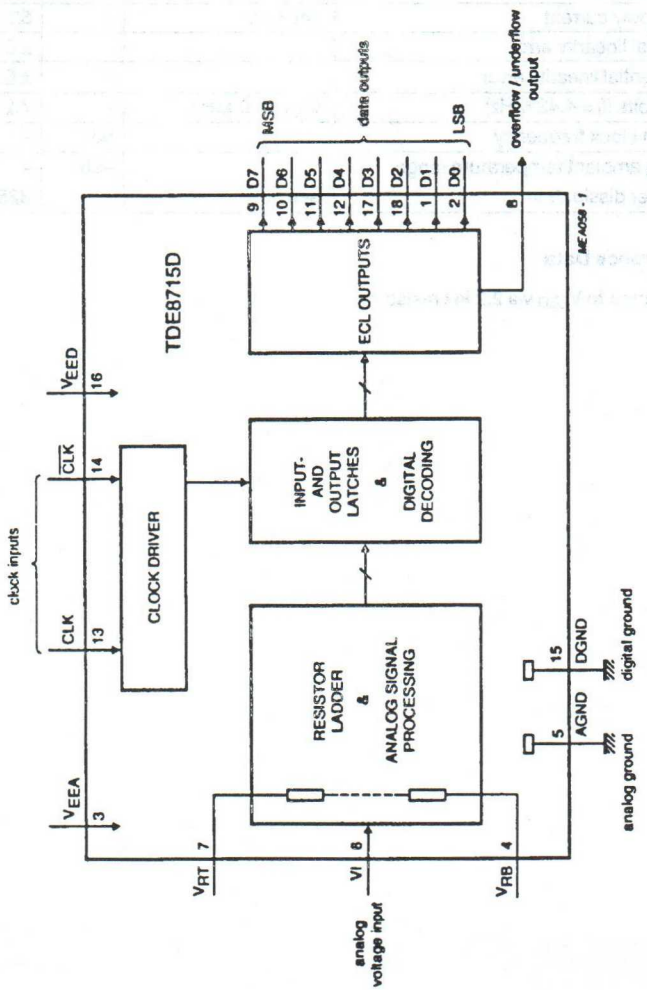


Fig.1 Block diagram.

8-bit high-speed analog-to-digital converter (Mil. temp.) TDE8715D

PIN CONFIGURATION

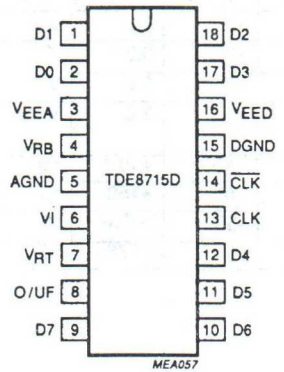


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output, bit 0 (LSB)
V_{EEA}	3	analog negative supply voltage (–5.2 V)
V_{RB}	4	reference voltage bottom input
AGND	5	analog ground
VI	6	analog voltage input
V_{RT}	7	reference voltage top input
O/UF	8	overflow/underflow data output
D7	9	data output, bit 7(MSB)
D6	10	data output, bit 6
D5	11	data output, bit 5
D4	12	data output, bit 4
CLK	13	clock input
$\overline{CLK}$	14	complementary clock input
DGND	15	digital ground
V_{EED}	16	digital negative supply voltage (–5.2 V)
D3	17	data output, bit 3
D2	18	data output, bit 2

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage range		−7	0.3	V
V_{EED}	digital supply voltage range		−7	0.3	V
V_{VI}	input voltage range		−7	0.3	V
$V_{\overline{CLK}}$/ V_{CLK}	AC input voltage for switching (peak-to-peak value)	see note	-	2.0	V
I_O	output current		−15	+10	mA
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		-55	+125	°C
T_j	junction temperature		-	+175	°C

Note to the Ratings

The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

- Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- Asymmetrical drive modes; When driving the CLK input directly with a ECL signal or a sinewave signal imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- When driving the CLK input with a ECL signal only (Asymmetrical drive modes) , it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\,j\text{-}a}$	SOT133BH3	+75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{EEA} = V_3 - V_5 = -4.95$ V to -5.45 V; $V_{EED} = V_{16} - V_{15} = -4.95$ V to -5.45 V; AGND and DGND shorted together; $T_{amb} = -55$ °C to $+125$ °C; unless otherwise specified (typical values measured at $V_{EEA} = -5.2$V; $V_{EED} = -5.2$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{EEA}	analog supply voltage		−4.95	−5.2	−5.45	V
V_{EED}	digital supply voltage		−4.95	−5.2	−5.45	V
I_{EEA}	analog supply current		-	20	25	mA
I_{EED}	digital supply current	note 5	-	52	60	mA
ΔV_{EE}	supply voltage difference $V_{EEA} - V_{EED}$		−0.5	0	+0.5	V
Reference voltages for the resistor ladder						
V_{RB}	reference voltage LOW		−3.4	−3.1	−2.8	V
V_{RT}	reference voltage HIGH		−1.0	−0.6	−0.4	V
V_{ref}	differential reference voltage $V_{RT}-V_{RB}$		2.4	2.5	-	V
I_{ref}	reference current		-	12.6	-	mA
R_{LAD}	resistor ladder		-	200	-	Ω
R_{TLC}	temperature coefficient of the ladder		-	0.24	-	Ω/°C
V_{OB}	voltage offset bottom	note 6	-	317	-	mV
V_{OBTC}	voltage offset bottom temperature coefficient	note 6	-	0.1	-	mV/°C
V_{OT}	voltage offset top	note 6	-	174	-	mV
V_{OTTC}	voltage offset top temperature coefficient	note 6	-	−0.3	-	mV/°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs CLOCK INPUT CLK (note 1)						
V_{IL}	input voltage LOW		−1.85	−1.77	−1.65	V
V_{IH}	input voltage HIGH		−0.96	−0.88	−0.81	V
I_{IL}	input current LOW	V_{CLK} = −1.77 V	-	−240	-	µA
I_{IH}	input current HIGH	V_{CLK} = −0.88 V	-	−14	-	µA
R_i	input resistance	f_{CLK} = 10 MHz	-	7.0	-	kΩ
		f_{CLK} = 50 MHz	-	3.5	-	kΩ
C_i	input capacitance	f_{CLK} = 10 MHz	-	1.8	-	pF
		f_{CLK} = 50 MHz	-	1.55	-	pF
CLOCK INPUT $\overline{CLK}$ (note 1)						
V_{IL}	input voltage LOW		−1.85	−1.77	−1.65	V
V_{IH}	input voltage HIGH		−0.96	−0.88	−0.81	V
I_{IL}	input current LOW	$V_{\overline{CLK}}$ = −1.77 V	-	−140	-	µA
I_{IH}	input current HIGH	$V_{\overline{CLK}}$ = −0.88 V	-	75	-	µA
R_i	input resistance	$f_{\overline{CLK}}$ = 10 MHz	-	9.3	-	kΩ
		$f_{\overline{CLK}}$ = 50 MHz	-	4.5	-	kΩ
C_i	input capacitance	$f_{\overline{CLK}}$ = 10 MHz	-	2.6	-	pF
		$f_{\overline{CLK}}$ = 50 MHz	-	2.4	-	pF
$V_{CLK(p-p)} - V_{\overline{CLK}(p-p)}$	AC input voltage for switching (peak-to-peak value)		0.5	0.9	1.1	V
VI (analog input with V_{RB} = −3.1 V and V_{RT} = −0.6 V)						
I_{IL}	input current LOW	data output 00	-	0	-	µA
I_{IH}	input current HIGH	data output FF	-	120	-	µA
R_i	input resistance	f_i = 1 MHz	-	9.4	-	kΩ
C_i	input capacitance	f_i = 1 MHz	-	13.7	20	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs DIGITAL OUTPUTS (D7 - D0 and 0/UF) (Digital 10KH ECL outputs)						
V_{OL}	output voltage LOW	T_{amb} = 25 °C	−1.9	−1.77	−1.65	V
V_{OH}	output voltage HIGH	T_{amb} = 25 °C	−0.96	−0.88	−0.81	V
I_{OL}	output current LOW		-	1.8	4	mA
I_{OH}	output current HIGH		-	1.8	4	mA
Switching characteristics						
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		50	-	-	MHz
Analog signal processing (f_{CLK} = 50 MHz)						
B	−3 dB bandwidth	note 2	-	20.5	-	MHz
G_d	differential gain	note 3	-	0.3	2.0	%
ϕ_d	differential phase	note 3	-	0.4	1.5	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	0	0	0	dB
F_{even}	even harmonics (full-scale)	f_i = 4.43 MHz	-	−60	-	dB
F_{odd}	odd harmonics (full-scale)	f_i = 4.43 MHz	-	−50	-	dB
Transfer function (f_{CLK} = 50 MHz)						
ILE	DC integral linearity error		-	-	±0.75	LSB
DLE	DC differential linearity error		-	-	±0.5	LSB
AILE	AC integral linearity error	note 4	-	±0.75	-	LSB
EB	effective bits f_i = 600 kHz	f_{CLK} = 20 MHz	-	7.8	-	bits
EB	effective bits f_i = 4.43 MHz	f_{CLK} = 50 MHz	-	7.2	-	bits
EB	effective bits f_i = 7 MHz	f_{CLK} = 50 MHz	-	6.9	-	bits
Timing (note 7; see Fig. 3)						
t_{dS}	sampling delay		-	1	3	ns
t_{HD}	output hold time		3	4	-	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	4	5	8	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	6	7	10	ns

Notes to the characteristics

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

- Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- Asymmetrical drive modes; When driving the CLK input directly with a ECL signal or a sinewave signal imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- When driving the CLK input with a ECL signal only (Asymmetrical drive modes), it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.

2. The −3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).

3. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.

4. Full-scale sinewave (f_i = 4.43 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 50 MHz).

5. All digital outputs connected to V_{EED} via 2.2 kΩ resistors.

6. Analog input voltages producing code 00 up to and including FF

- V_{OB} (voltage offset bottom) is the difference between the analog input which produces data equal to 00 and the reference voltage bottom (V_{RB}) at T_{amb} = 25 °C.
- V_{OBTC} (voltage offset bottom temperature coefficient) is the dependence of V_{OB} with temperature.
- V_{OT} (voltage offset top) is the difference between V_{RT} (reference voltage top) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
- V_{OTTC} (voltage offset top temperature coefficient) is the dependence of V_{OT} with temperature.

7. Output data acquisition

- Output data is available after the maximum delay of t_{dHL} and t_{dLH}.
- Output data is fully stable during the low level of the clock. Thus it is recommended that acquisition of this data is made after the falling edge of the clock, instead of after the maximum (t_{dHL}, t_{dLH}).

Table 1 Output coding and input voltage (typical values; $V_{RB} = -3.1$ V; $V_{RT} = -0.6$ V and V_{VI} referenced to AGND)

STEP	V_{VI}	O/UF	BINARY OUTPUT BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
underflow	<–2.789	1	0	0	0	0	0	0	0	0
0	–2.783	0	0	0	0	0	0	0	0	0
1	–2.775	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0
255	–0.774	0	1	1	1	1	1	1	1	1
overflow	>–0.770	1	1	1	1	1	1	1	1	1

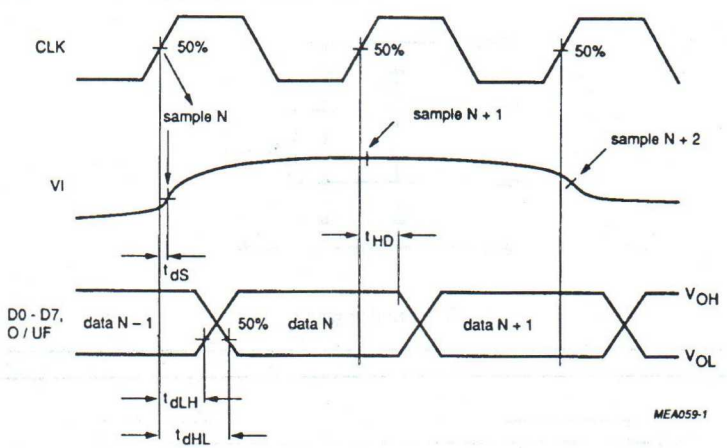


Fig.3 Timing diagram.

INTERNAL PIN CONFIGURATIONS

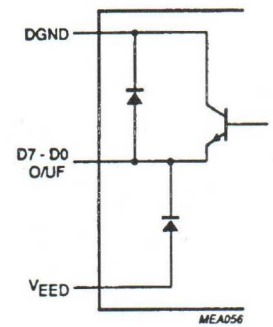


Fig.4 ECL data outputs

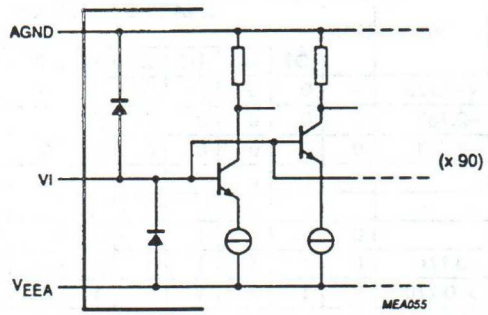


Fig.5 Analog input

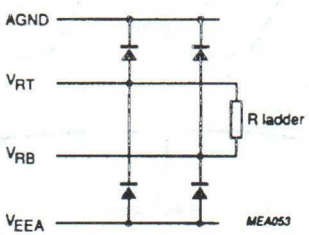


Fig.6 V_{RT} and V_{RB} inputs

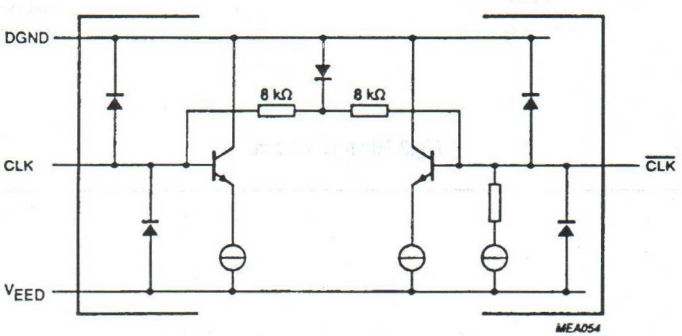


Fig.7 CLK and $\overline{CLK}$ input

APPLICATION INFORMATION

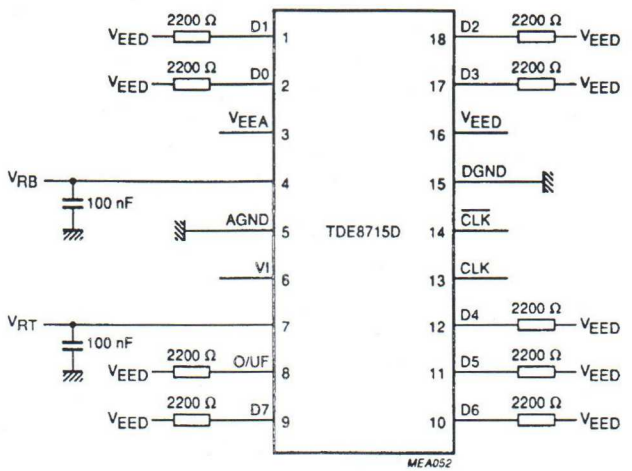


Fig.8 Application diagram.

Notes to Fig.8

- All resistors have a value of 2.2 kΩ; all capacitors have a value of 100 nF
- Analog and digital supplies should be separated and decoupled.
- The external voltage regulator must be build in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.
- $V_{EEA} = V_{EED} = -5.2$ V; $V_{RB} = -3.1$ V; $V_{RT} = -0.6$ V.

Section 11
Digital-to-Analog Converters

INDEX

AN100	An overview of data converters	711
DAC08 Series	8-Bit high-speed multiplying D/A converter	716
AN101	Applying the DAC08	728
AN105	Digital attenuator	735
MC1508-8/1408-8	8-bit multiplying D/A converter	737
MC3410,MC3410C	10-Bit high-speed multiplying D/A converter	743
NE/SE5018/5019	8-Bit µp-compatible D/A converter	751
NE5020	10-Bit µP-compatible D/A converter	757
NE/SE5410	10-Bit high-speed multiplying D/A converter	767
AM6012	12-Bit multiplying D/A converter	776
TDA1541A	Stereo high-performance 16-bit DAC	787
TDA1543	Dual 16-bit DAC (economy version) (I^2S input format)	796
TDA1543A	Dual 16-bit DAC (economy version) (Japanese input format)	805
TDA1545A	Stereo continuous calibration DAC	813
TDA1547	Dual top-performance bitstream DAC	825
TDA8444/AT/T	Octuple 6-bit DAC with I^2C-bus	839
TDA8702	8-bit video digital-to-analog converter	848
TDE8712D	8-bit video digital-to-analog converter (Mil. temp.)	862

Symbols and definitions for digital-to-analog converters (DACs)

General Purpose/Linear ICs

Absolute Accuracy Error

Absolute Accuracy Error of a DAC at an input code is the difference between the theoretical output voltage/current at a digital input code and the actual analog output voltage/current produced at the same code.

Absolute Accuracy Error includes gain error, offset error and relative accuracy error and is typically expressed in LSBs or in percent of full-scale range (FSR).

Differential Linearity Error

Differential Linearity Error of a DAC is the difference between the actual step size between any two adjacent codes and the ideal step size (which is equal to 1 LSB of the DAC). A differential linearity error of greater than 1 LSB can lead to non-monotonicity.

Digital Feedthrough

The amount of digital energy at the digital inputs that appear at the DAC output.

Full-Scale Range (FSR)

The Full-Scale Range (FSR) of a DAC is the scale factor that determines the nominal conversion relationship; e.g., 10V span for a full-scale code change in a fixed reference converter.

In a unipolar DAC of n bits, the output voltage/current is 0V/mA with all bits OFF. With all bits turned ON, the output voltage/current is FSR x $(1-2^{-N})$.

In a bipolar DAC, the output voltage/current is –FSR/2 with all bits OFF. With all bits turned ON, the output voltage/current is FSR x $(1-2^{-(N-1)})$.

Glitch

The transition spike that occurs at the output of a DAC. When the digital input code changes, not all input switches change at precisely the same time, leading to either positive or negative spikes when the input code changes. The energy in these "glitches" is proportional to the area under the glitch; hence, we generally refer to "glitch energy" as the area under the glitch in nV – seconds or LSB – seconds. The largest glitch tends to occur at the transition from the code where the MSB is a logic low with all other bits a logic high to the 1's complement of this word.

Integral Non-Linearity

Same as Relative Accuracy.

Least Significant Bit

The Least Significant Bit (LSB) is the lowest-order bit and carries the smallest weight. In an n-bit DAC, the weight of the LSB is $FSR/(2^N-1)$. It is the smallest discrete step that can be attained in the output of the DAC.

Monotonicity

A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases from any code to the next higher code.

Most Significant Bit

The Most Significant Bit (MSB) is the highest order bit and carries the most weight. The weight of the MSB is 1/2 the FSR of the DAC.

Offset Error (Unipolar and Bipolar)

In a DAC, unipolar offset is the actual analog output voltage/current with all the bits turned OFF. Offset Error causes a shift in the transfer characteristic of the DAC. Similarly for bipolar offset, it is the actual output voltage/current with the digital input at half-scale.

Output Voltage Compliance

For a current output DAC, the maximum range of output voltage for which the output current will be within specifications.

Power Supply Sensitivity

The Power Supply Sensitivity of a DAC is the change in the DAC output with changes in the DC power supply voltages. It is usually expressed in LSBs/V or in %FSR/V.

Relative Accuracy

Relative Accuracy Error is the deviation of the DACs actual output voltage/current from the ideal output voltage/current on a straight line connecting the end points of the transfer characteristic after nulling offset error and gain error. It is generally expressed in LSBs or in %FSR.

Resolution

Resolution of a DAC is the number of bits at its input. The number of discrete output levels is 2^N where N is the resolution of the converter.

Settling Time

The time required, following a prescribed change in the digital inputs, for the output of the DAC to reach and remain within a specified fraction (typically ±1/2 LSB) of its final value. This parameter is usually specified for a full-scale change.

Temperature Coefficients

In general, Temperature Coefficients are expressed either in ppm/°C or in LSBs/°C or as a change in the specified parameter over the temperature range. Measurements are usually made at room temperature and at the temperature extremes of the specified temperature range; the Temperature Coefficient is defined as the change in the parameter from its room temperature value divided by the corresponding temperature change.

An overview of data converters

AN100

INTRODUCTION

Large systems are comprised of many different subsystems, all of which must interface to complete the system. All types of circuits, including linear, digital and discrete, are often used in the subsystems.

Interface circuits provide the necessary function of tying the parts of a system together. These circuits are usually not purely linear or digital but contain both types of circuit functions. For instance, sense amplifiers are designed for interface between low level memory outputs and bipolar levels, while differential comparators are designed for interface between analog systems and logic systems.

CONVERTERS

Digital communications, digital instruments and displays have created a demand for low cost reliable converters. Key factors in this demand are:

- The need to communicate with digital computers and equipment for processing and storage of analog signals.
- Severe limitations encountered in reliable analog data transmission over any considerable distance.
- The need for more easily readable displays.

General application areas for converters include: Data processing, data transmission, graphics and displays, audio systems, control systems and arithmetic operations.

SPECIFIC APPLICATIONS

Test Systems

- Transistor tester (Force IB and IC)
- Resistor matching
- Programmable power supplies
- Programmable pulse generators
- Programmable current source
- Function generators (ROM drive)

Arithmetic Operations

- Analog division by a digital word
- Analog quotient of 2 digital words
- Analog product of 2 digital words – squaring
- Addition and subtraction with analog output
- Magnitude comparison of 2 digital words
- Digital quotient of 2 analog variables
- Arithmetic operations with words from different logic families

Graphics and Displays

- Polar-to-rectangular conversion
- CRT character generation
- Chart recorder driver
- CRT displays

Data Transmission

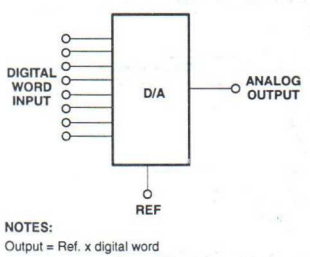
- Modem transmitter
- Differential line driver
- Party line multiplexing of analog signals
- Multilevel 2-wire data transmission
- Secure communications (constant power dissipation)

Control Systems

- Reference level generator for set-point controllers
- Positive peak detector
- Negative peak detector
- Disc drive head positioner
- Microfilm head positioner

Audio Systems

- Digital AVC and reverberation
- Music distribution
- Organ tone generator
- Audio tracking A/D
- Speech compression and expansion
- Audio digitizing and decoding



NOTES:

Output = Ref. x digital word

$$\text{Output} = \text{Ref.} \times \left(\frac{B_1}{2} + \frac{B_2}{4} + \ldots + \frac{B_N}{2^N}\right)$$

Figure 1. Conversion of a Digitally Coded Signal Input Into an Analog Signal Output

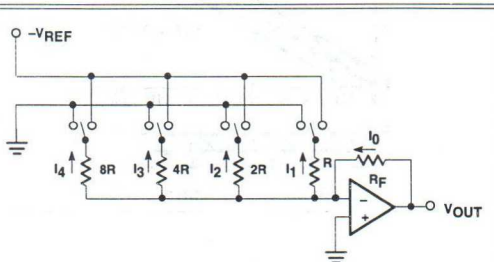


Figure 2. Binary-Weighted Ladder Employing Voltage Switching

DAC Building Blocks

The actual implementation of a D/A system contains four separate parts: A reference quantity; a set of binary switches to simulate binary coefficients $B_1 \ldots B_N$; a weighting network; and an output summing means.

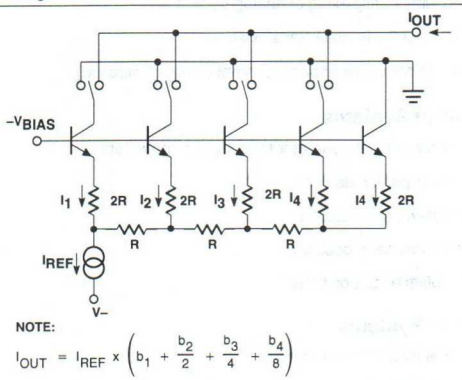


Figure 3. R-2R Ladder Network Employing Current Switching

Binary-Weighted Ladder Employing Voltage Switching

The disadvantages of a binary-weighted ladder employing voltage switching include: a wide range of resistor values which are used in weighting the network, and nodal capacitances which are charged/discharged during conversion (See Figure 2).

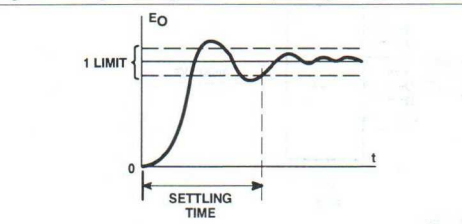


Figure 4. Settling Time

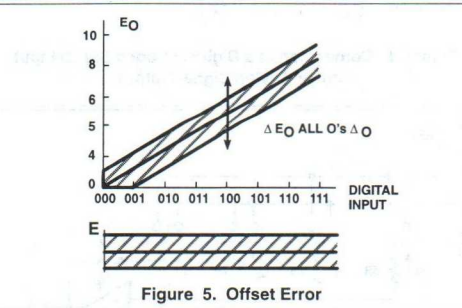


Figure 5. Offset Error

R-2R Ladder Network Employing Current Switching

The advantages of this type of network include: no need for a wide range of resistor values, and current switching eliminates transients in nodal parasite capacitances (See Figure 3).

KEY SPECIFICATIONS

Speed

The conversion process should represent the input signal with the highest fidelity and minimal lag in time (real-time applications).

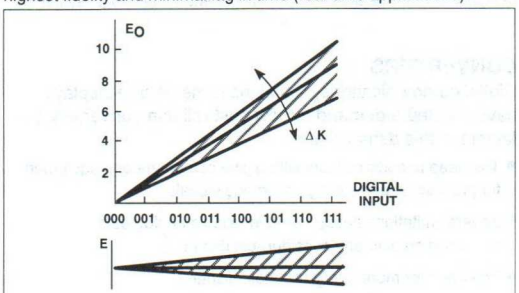


Figure 6. Gain Error

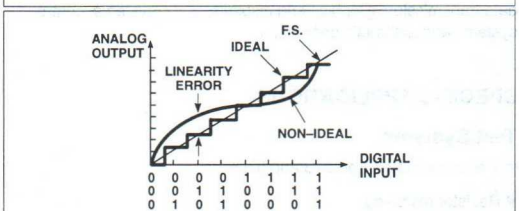


Figure 7. Relative Accuracy

Settling Time

Settling time is a measure of a converter's speed and is defined as the elapsed time after a code transition for DAC output to reach final value within specified limits, usually ± LSB (See Figure 4).

Errors

Offset Error – The output current or voltage of a DAC with zero code input. (See Figure 5). Offset can and usually is trimmed to zero with an offset zero adjust circuit.

Gain Error – Deviation in output voltage from correct level when the input calls for a full-scale output. This error may be trimmed to zero (See Figure 6).

Relative Accuracy – The maximum deviation of the DAC output relative to an ideal straight line drawn from zero scale to full-scale (See Figure 7).

Differential Non-Linearity – Incremental error from any ideal LSB analog output change when the digital input is changed 1 LSB (See Figure 9).

Monotonicity – As the input code is incremented from one code to the next in sequence, the analog output will either increase or remain constant (See Figure 9).

Stability

Stability is a measure of the independence of converter parameters with respect to variations in external conditions such as temperature and supply voltage.

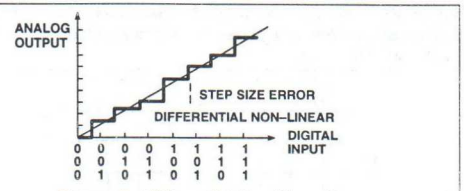


Figure 8. Differential Non-Linearity

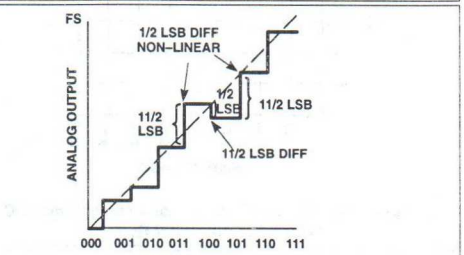


Figure 9. Non-Monotonic (Must be > ± 1/2 LSB Non-Linear)

Temperature Coefficient – The effects of temperature changes of the output. Specified as % full-scale change per degree C.

Supply Rejection – Ability to resist changes in the output with supply changes, specified as % full-scale change per volt of supply change.

Long Term Stability – Measure of how stable the output is over a long period of time.

A/D CONVERTER CIRCUITS

Analog-to-Digital conversion schemes generally fall into one of three categories:

1. Feedback
   - Counting
   - Tracking (up-down)
   - Successive approximation
2. Integrating
   - Single slope
   - Dual slope
   - Triple slope
3. Parallel (Flash)

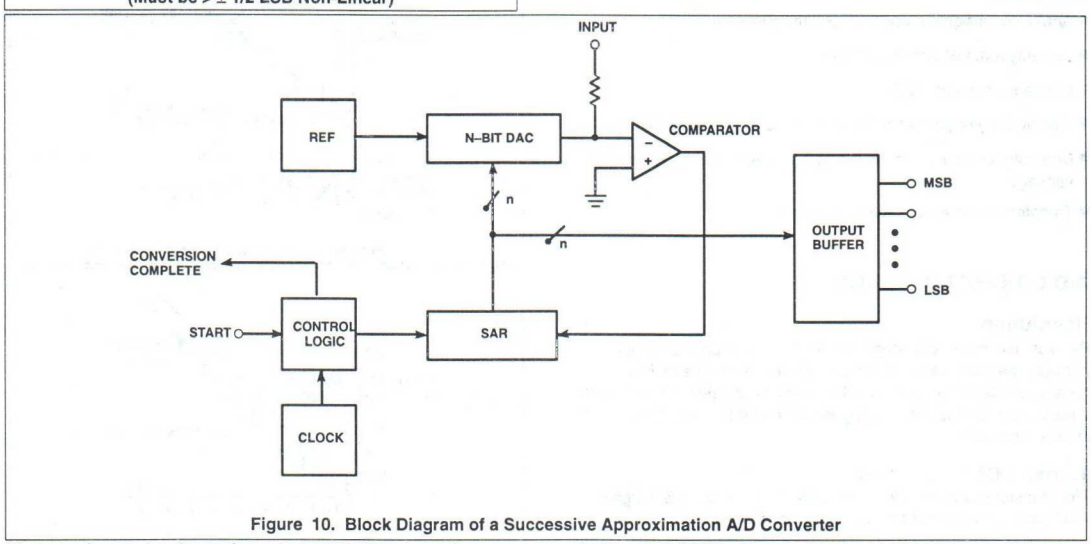


Figure 10. Block Diagram of a Successive Approximation A/D Converter

The type of converter chosen for a given application depends upon many things; the accuracy required, the conversion speed necessary, the necessary immunity to noise, and cost are some of these considerations.

The successive approximation technique is the one most widely used, mainly because of its excellent tradeoffs in resolution, speed, accuracy, and cost.

Figure 10 shows a simplified block diagram of a successive approximation A/D converter. Upon receiving the start signal, the successive approximation register (SAR) is cleared and the most significant bit (MSB) of that register is set. The SAR output is connected to the input of the DAC, the output of which is compared with the unknown input. If the input is less than the DAC output, the MSB is cleared and the next bit is set; if the input is greater than the DAC output, the MSB is left high and the next bit is set. The input is again compared with the DAC output and the second bit cleared or left high, based on the same criteria as for the MSB. This process continues until all bits have been determined.

The analog input should not change appreciably during the conversion time. If it did change during this time, the converted

output would not be a true indication of the analog input. For this reason, it is common practice to use a sample-and-hold circuit at the converter analog input to hold the input value constant during the conversion process. A sample-and-hold circuit is not necessary if the signal at the input of the converter varies slowly enough and has a noise level low enough so that the input will not change a significant amount during the conversion. The allowable input change during this conversion is generally accepted as the value of LSB (for n-bit accuracy).

Accuracy and speed are determined primarily by the properties of the DAC and the comparator. Linearity is determined primarily by the linearity of the DAC. If the DAC is non-monotonic, one or more codes will be missing from the A/D converter's output range.

Figure 11 is the transfer function of a 3-bit binary coded A/D converter with a 0 to +10V input range. A 3-bit ADC is shown for simplicity, but the principle applies to ADCs of any resolution. Note that there is a LSB offset at the input such that the first count occurs when the input is equal to LSB. The center of the range for the first step occurs, therefore, when the input is equal to the value of one LSB, and the error at the switch point is limited to LSB. This error is known as the quantization error as it is derived from the smallest input quantity that can be resolved. If an ADC has a specified error of LSB maximum, this means that any transition point can be as far as LSB from where it should be.

CONSIDERATIONS FOR A/D CONVERTERS

- Analog input signal range and resolution required
- Linearity requirement and stability
- Conversion speed required
- Monotonicity requirement: Can missing codes be tolerated?
- Character of input signal: Is it noisy, sampled, filtered, slowly varying?
- Transfer characteristics (type of coding)

A/D CONVERTER TERMS

Resolution

Resolution is the input change required to increment the output between the two adjacent codes. This term also refers to the number of bits in the output word and, hence, the number of discrete output codes the input analog signal can be broken into. Expressed in "bits" resolution.

Transfer Characteristic

The Transfer Characteristic is the relationship of the output digital word (code) to the input analog signal, i.e., Binary, BCD.

Conversion Speed

The Conversion Speed is the speed at which an ADC can make repetitive data conversions.

Quantizing Error

Quantizing Error is an inherent error in the conversion process due to finite resolution (discrete output). See Figure 12.

Offset Error

An Offset Error is shown in Figure 13.

Gain Error

A Gain Error is shown in Figure 14.

Relative Accuracy

Relative Accuracy is the deviation of an actual bit transition from the ideal transition value at any level over the range of the ADC (% FS). See Figure 15.

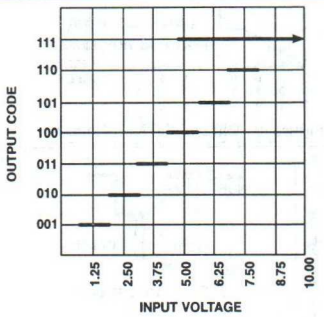


Figure 11. Transfer Function of an Ideal 3-bit ADC With a 0 to 10V Input Range

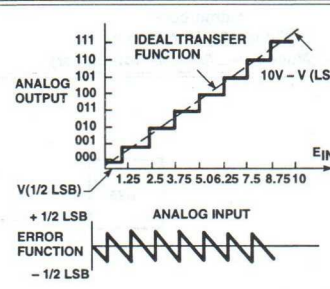


Figure 12. Quantizing Errors

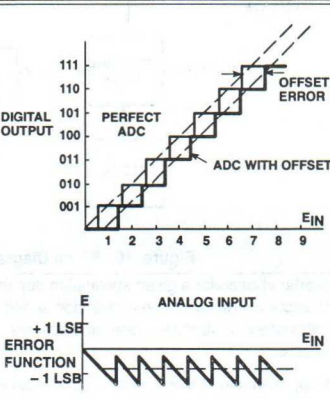


Figure 13. Offset Error

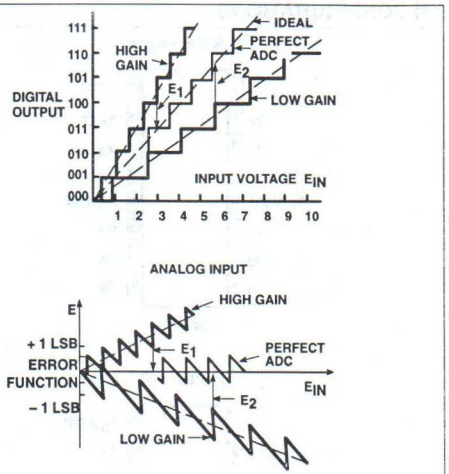


Figure 14. Gain Error

Hysteresis Error

A Hysteresis Error is the code transition voltage dependence relative to the direction from which the transition is approached.

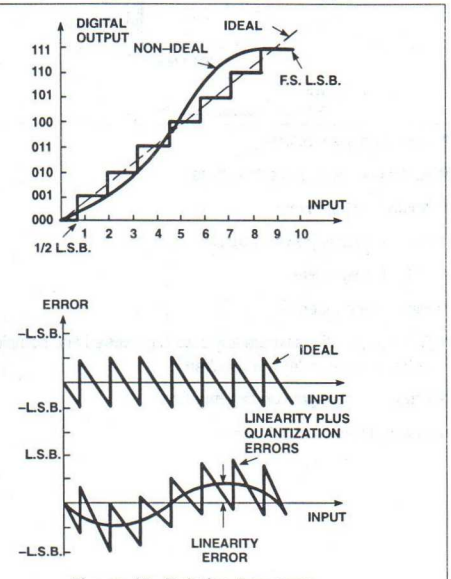


Figure 15. Relative Accuracy

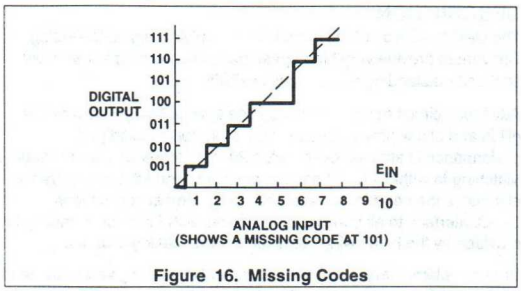


Figure 16. Missing Codes

Monotonicity

Monotonicity is when the output code either increases or remains the same for increasing analog input signals. The opposite is true in the reverse direction.

Missing Codes

A Missing Code is a code combination that is skipped. See Figure 16.

8-Bit high-speed multiplying D/A converter

DAC08 Series

DESCRIPTION

The DAC08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 70ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 20-to-1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full-scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. True high voltage compliance outputs allow direct output voltage conversion and eliminate output op amps in many applications.

All DAC08 series models guarantee full 8-bit monotonicity and linearities as tight as 0.1% over the entire operating temperature range. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 37mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the DAC08 attractive for portable and military aerospace applications.

FEATURES

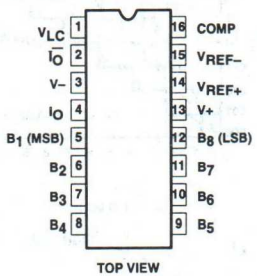
- Fast settling output current—70ns
- Full-scale current prematched to ±1 LSB
- Direct interface to TTL, CMOS, ECL, HTL, PMOS
- Relative accuracy to 0.1% maximum over temperature range
- High output compliance -10V to +18V
- True and complemented outputs
- Wide range multiplying capability
- Low FS current drift — ±10ppm/°C
- Wide power supply range—±4.5V to ±18V
- Low power consumption—37mW at ±5V

APPLICATIONS

- 8-bit, 1µs A-to-D converters
- Servo-motor and pen drivers
- Waveform generators
- Audio encoders and attenuators
- Analog meter drivers
- Programmable power supplies
- CRT display drivers
- High-speed modems
- Other applications where low cost, high speed and complete input/output versatility are required
- Programmable gain and attenuation
- Analog-Digital multiplication

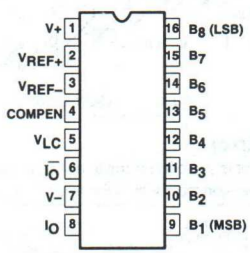
PIN CONFIGURATIONS

F, N Packages



TOP VIEW

D[1] Package



TOP VIEW

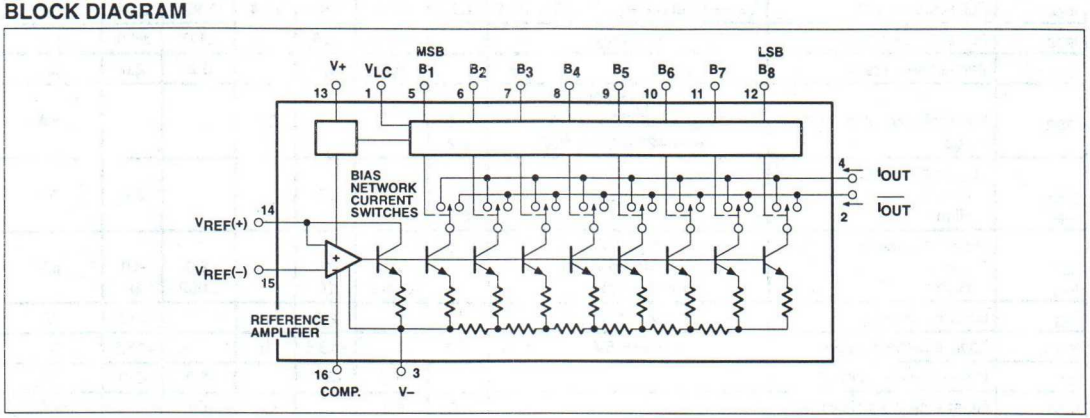
NOTE:
1. SO and non-standard pinouts.

8-Bit high-speed multiplying D/A converter — DAC08 Series

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Hermetic Ceramic Dual In-Line Package (Cerdip)	-55°C to +125°C	DAC08F	0582B
16-Pin Hermetic Ceramic Dual In-Line Package (Cerdip)	-55°C to +125°C	DAC08AF	0582B
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	DAC08CN	0406C
16-Pin Hermetic Ceramic Dual In-Line Package (Cerdip)	0 to +70°C	DAC08CF	0582B
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	DAC08EN	0406C
16-Pin Hermetic Ceramic Dual In-Line Package (Cerdip)	0 to +70°C	DAC08EF	0582B
16-Pin Plastic Small Outline (SO) Package	0 to +70°C	DAC08ED	0005D
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	DAC08HN	0406C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V+ to V-	Power supply voltage	36	V
V_5-V_{12}	Digital input voltage	V- to V- plus 36V	
V_{LC}	Logic threshold control	V- to V+	
V_0	Applied output voltage	V- to +18	V
I_{14}	Reference current	5.0	mA
V_{14}, V_{15}	Reference amplifier inputs	V_{EE} to V_{CC}	
P_D	Maximum power dissipation T_A=25°C (still-air)[1]		
	F package	1190	mW
	N package	1450	mW
	D package	1090	mW
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
T_A	Operating temperature range		
	DAC08, DAC08A	-55 to +125	°C
	DAC08C, E, H	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.6mW/°C
   D package at 8.7mW/°C

DC ELECTRICAL CHARACTERISTICS

Pin 3 must be at least 3V more negative than the potential to which R_{15} is returned. V_{CC}=±15V, I_{REF}=2.0mA. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$ unless otherwise noted. DAC08C, E, H: T_A=0°C to 70°C DAC08/08A: T_A=-55°C to 125°C

SYMBOL	PARAMETER	TEST CONDITIONS	DAC08C			DAC08E DAC08			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy	Over temperature range			±0.39			±0.19	%FS
	Differential non-linearity				±0.78			±0.39	%FS
TCI_{FS}	Full-scale tempco			±10			±10		ppm/°C
V_{OC}	Output voltage compliance	Full-scale current change< 1/2LSB	-10		+18	-10		+18	V
I_{FS4}	Full-scale current	V_{REF}=10.000V, R_{14}, R_{15}=5.000kΩ	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full-scale symmetry	I_{FS4}-I_{FS2}		±2.0	±16		±1.0	±8.0	µA
I_{ZS}	Zero-scale current			0.2	4.0		0.2	2.0	µA
I_{FSR}	Full-scale output current range	R_{14}, R_{15}=5.000kΩ V_{REF}=+15.0V, V-=-10V V_{REF}=+25.0V, V-=-12V	2.1 4.2			2.1 4.2			mA
V_{IL} V_{IH}	Logic input levels Low High	V_{LC}=0V	 2.0		0.8	 2.0		0.8	V
I_{IL} I_{IH}	Logic input current Low High	V_{LC}=0V V_{IN}=-10V to +0.8V V_{IN}=2.0V to 18V		-2.0 0.002	-10 10		-2.0 0.002	-10 10	µA
V_{IS}	Logic input swing	V-=-15V	-10		+18	-10		+18	V
V_{THR}	Logic threshold range	V_S=±15V	-10		+13.5	-10		+13.5	V
I_{15}	Reference bias current			-1.0	-3.0		-1.0	-3.0	µA
dI/dt	Reference input slew rate		4.0	8.0		4.0	8.0		mA/µs
$PSSI_{FS+}$ PSI_{FS-}	Power supply sensitivity Positive Negative	I_{REF}=1mA V+=4.5 to 5.5V, V-=-15V; V+=13.5 to 16.5V, V-=-15V V-=-4.5 to -5.5V, V+=+15V; V-=-13.5 to -16.5, V+=+15V		0.0003 0.002	0.01 0.01		0.0003 0.002	0.01 0.01	%FS/%VS
I+ I-	Power supply current Positive Negative	V_S=±5V, I_{REF}=1.0mA		3.1 -4.3	3.8 -5.8		3.1 -4.3	3.8 -5.8	mA
I+ I-	Positive Negative	V_S=+5V, -15V, I_{REF}=2.0mA		3.1 -7.1	3.8 -7.8		3.1 -7.1	3.8 -7.8	
I+ I-	Positive Negative	V_S=±15V, I_{REF}=2.0mA		3.2 -7.2	3.8 -7.8		3.2 -7.2	3.8 -7.8	
P_D	Power dissipation	±5V, I_{REF}=1.0mA +5V, -15V, I_{REF}=2.0mA ±15V, I_{REF}=2.0mA		37 122 156	48 136 174		37 122 156	48 136 174	mW

DC ELECTRICAL CHARACTERISTICS (Continued)

Pin 3 must be at least 3V more negative than the potential to which R15 is returned. V_{CC} = +15V, I_{REF} = 2.0mA, Output characteristics refer to both I_{OUT} and $I_{\overline{OUT}}$, unless otherwise noted. DAC08C, E, H: T_A = 0°C to 70°C. DAC08/08A: T_A = -55°C to 125°C.

SYMBOL	PARAMETER	TEST CONDITIONS	DAC08H DAC08A			UNIT
			Min	Typ	Max	
	Resolution		8	8	8	Bits
	Monotonicity		8	8	8	Bits
	Relative accuracy	Over temperature range			±0.1	%FS
	Differential non-linearity				±0.19	%FS
TCI_{FS}	Full-scale tempco			±10	±50	ppm/°C
V_{OC}	Output voltage compliance	Full-scale current change 1/2LSB	-10		+18	V
I_{FS4}	Full-scale current	V_{REF}=10.000V, R_{14}, R_{15}=5.000kΩ	1.984	1.992	2.000	mA
I_{FSS}	Full-scale symmetry	I_{FS4}-I_{FS2}		±1.0	±4.0	µA
I_{ZS}	Zero-scale current			0.2	1.0	µA
I_{FSR}	Full-scale output current range	R_{14}, R_{15}=5.000kΩ V_{REF}=+15.0V, V-=-10V V_{REF}=+25.0V, V-=-12V	2.1 4.2			mA
	Logic input levels					
V_{IL}	Low	V_{LC}=0V			0.8	V
V_{IH}	High		2.0			
	Logic input current	V_{LC}=0V				
I_{IL}	Low	V_{IN}=-10V to +0.8V		-2.0	-10	µA
I_{IH}	High	V_{IN}=2.0V to 18V		0.002	10	
V_{IS}	Logic input swing	V-=-15V	-10		+18	V
V_{THR}	Logic threshold range	V_S=±15V	-10		+13.5	V
I_{15}	Reference bias current			-1.0	-3.0	µA
dI/dt	Reference input slew rate		4.0	8.0		mA/µs
	Power supply sensitivity	I_{REF}=1mA				
$PSSI_{FS+}$	Positive	V+=4.5 to 5.5V, V-=-15V; V+=13.5 to 16.5V, V-=-15V		0.0003	0.01	%FS/%VS
PSI_{FS-}	Negative	V-=-4.5 to -5.5V, V+=+15V; V-=-13.5 to -16.5, V+=+15V		0.002	0.01	
	Power supply current					
I+	Positive	V_S=±5V, I_{REF}=1.0mA		3.1	3.8	
I-	Negative			-4.3	-5.8	
I+	Positive	V_S=+5V, -15V, I_{REF}=2.0mA		3.1	3.8	mA
I-	Negative			-7.1	-7.8	
I+	Positive	V_S=±15V, I_{REF}=2.0mA		3.2	3.8	
I-	Negative			-7.2	-7.8	
		±5V, I_{REF}=1.0mA		37	48	
P_D	Power dissipation	+5V, -15V, I_{REF}=2.0mA		122	136	mW
		±15V, I_{REF}=2.0mA		156	174	

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	DAC08C			DAC08E DAC08			DAC08H DAC08A			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_S	Settling time	To ± 1/2LSB, all bits switched on or off, T_A=25°C		70	135		70	135		70	135	ns
	Propagation delay											
t_{PLH}	Low-to-High	T_A=25°C, each bit.										ns
t_{PHL}	High-to-Low	All bits switched		35	60		35	60		35	60	

TEST CIRCUITS

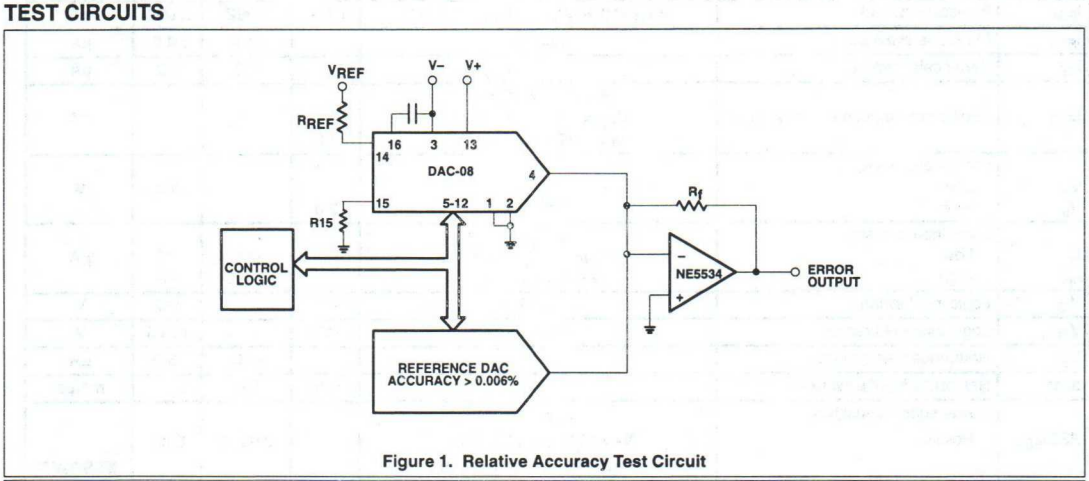


Figure 1. Relative Accuracy Test Circuit

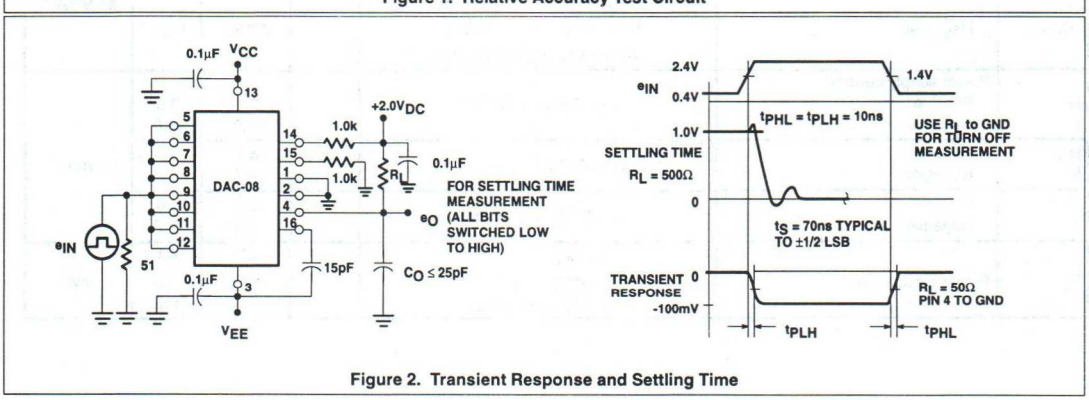


Figure 2. Transient Response and Settling Time

TEST CIRCUITS (Continued)

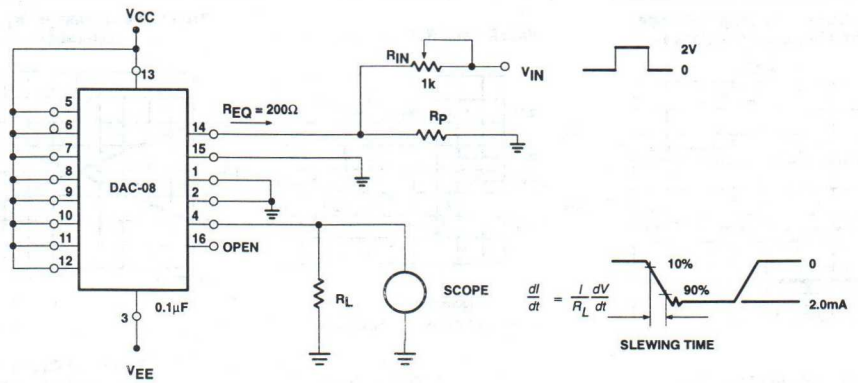
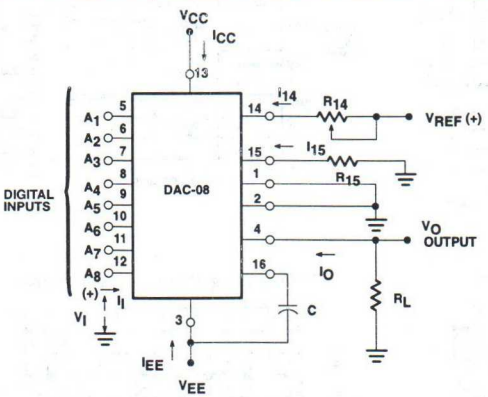


Figure 3. Reference Current Slew Rate Measurement



NOTES:
(See text for values of C.)
Typical values of $R_{14} = R_{15} = 1k$
$V_{REF} = +2.0V$
$C = 15pF$

V_I and I_I apply to inputs A_1 through A_8
The resistor tied to Pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left|\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256}\right|$$

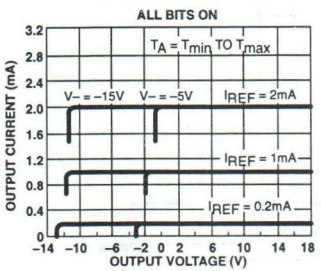
$$\text{where } K \approx \frac{V_{REF}}{R_{14}}$$

and A_N = '1' if A_N is at High Level
A_N = '0' if A_N is at Low Level

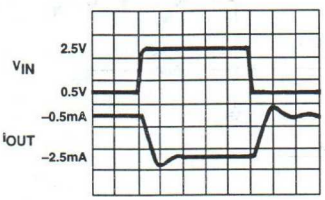
Figure 4. Notation Definitions

TYPICAL PERFORMANCE CHARACTERISTICS

Output Current vs Output Voltage (Output Voltage Compliance)



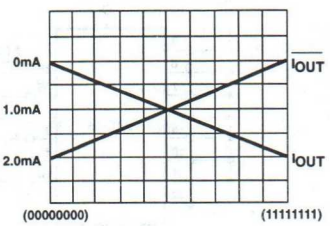
Fast Pulsed Reference Operation



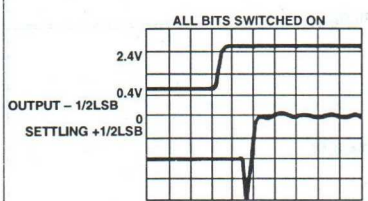
200ns/division

R_{EQ} = 200Ω, R_L = 100Ω, CC = 0

True and Complementary Output Operation



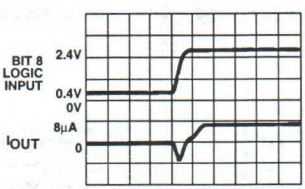
Full-Scale Settling Time



50ns/DIVISIOM

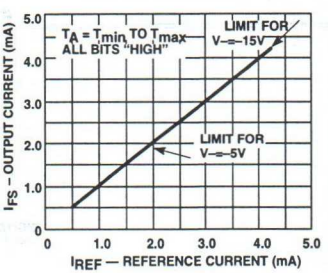
I_{FS}=2mA, R_L=1kΩ 1/2LSB=4μA

LSB Switching

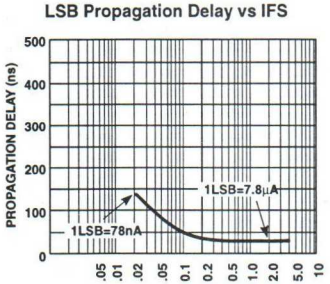


50ns/DIVISIOM

Full-Scale Current vs Reference Current

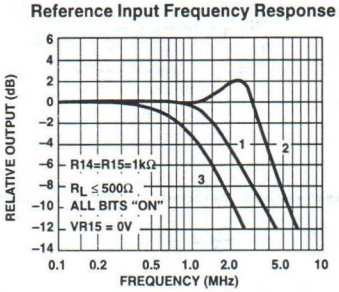


LSB Propagation Delay vs IFS



I_{FS} — OUTPUT FULL SCALE CURRENT (mA)

Reference Input Frequency Response



NOTES:

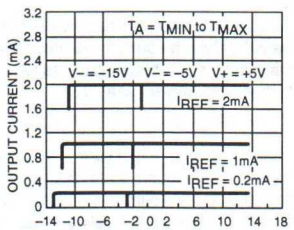
Curve 1: CC = 15pF, V_{IN} = 2.0V_{P-P} centered at +1.0V

Curve 1: CC = 15pF, V_{IN} = 5m0V_{P-P} centered at +200mV

Curve 1: CC = 15pF, V_{IN} = 100m0V_{P-P} centered at 0V and applied through 50Ω connected to Pin 14. +2.0V applied to R_{14}.

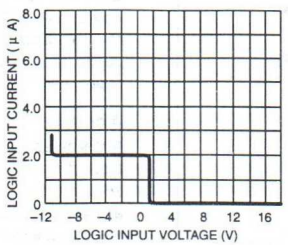
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Reference AMP Common-Mode Range All Bits On

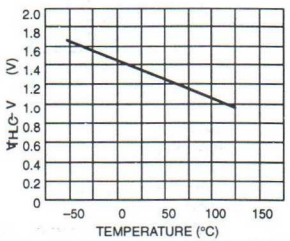


POSITIVE COMMON-MODE RANGE IS ALWAYS (V+) –1.5V.

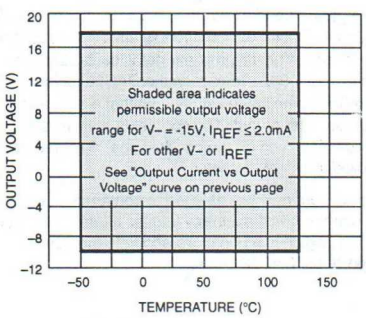
Logic Input Current vs Input Voltage



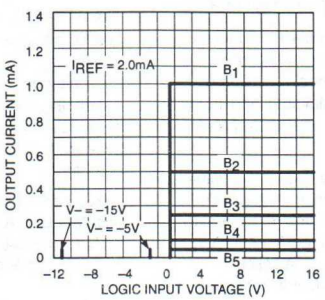
$V_{TH} - V_{LC}$ vs Temperature



Output Voltage Compliance vs Temperature



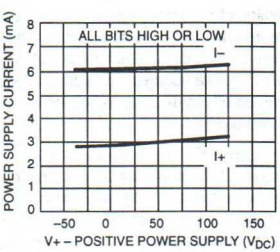
Bit Transfer Characteristics



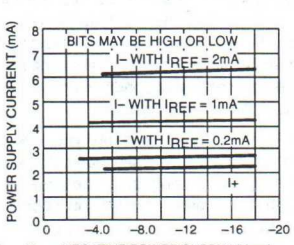
NOTES:

B_1 through B_8 have identical transfer characteristics. Bits are fully switched, with less than 1/2LSB error, at less than ±100mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2.0V over the operating temperature range (V_{LC} = 0.0V).

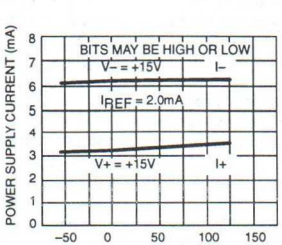
Power Supply Current vs V+



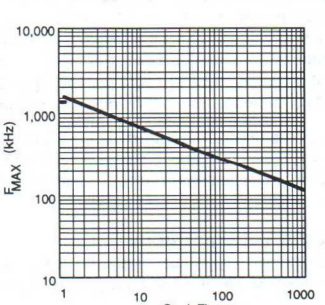
Power Supply Current vs V–



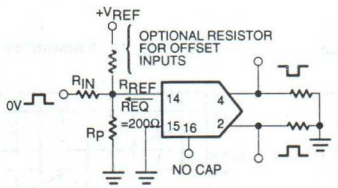
Power Supply Current vs Temperature



Maximum Reference Input Frequency vs Compensation Capacitor Value



TYPICAL APPLICATION



NOTES:
REQ = R_{IN} II R_P
Typical Values
R_{IN} = 5kΩ
$+V_{IN}$ = 10V

Pulsed Referenced Operation

FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier input current must always flow into Pin 14 regardless of the setup method or reference supply voltage polarity.

Connections for a positive reference voltage are shown in Figure 1. The reference voltage source supplies the full reference current. For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. R_{15} may be eliminated with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased as R_{14} value is increased. This is in order to maintain proper phase margin. For R_{14} values of 1.0, 2.5, and 5.0kΩ, minimum capacitor values are 15, 37, and 75pF, respectively. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection. (Fluctuations in the negative supply have more effect on accuracy than do any changes in the positive supply.)

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15} as shown. A high input impedance is the main advantage of this method. The negative reference voltage must be at least 3.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at Pin 15.

When using a DC reference voltage, capacitive bypass to ground is recommended. The 5.0V logic supply is not recommended as a reference voltage, but if a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be formed of two series resistors with the junction of the two resistors bypassed with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between Pin 14 and ground.

If Pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods applies and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage at Pin 4 must always be at least 4.5V more positive than the voltage of the negative supply (Pin 3) when the reference current is 2mA or less, and at least 8V more positive than the negative supply when the reference current is between 2mA and 4mA. This is necessary to avoid saturation of the output transistors, which would cause serious accuracy degradation.

Output Current Range

Any time the full-scale current exceeds 2mA, the negative supply must be at least 8V more negative than the output voltage. This is due to the increased internal voltage drops between the negative supply and the outputs with higher reference currents.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy, full-scale accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current after zero-scale current has been nulled out. The relative accuracy of the DAC08 series is essentially constant over the operating temperature range due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC08 series has a very low full-scale current drift over the operating temperature range.

The DAC08 series is guaranteed accurate to within ± LSB at +25°C at a full-scale output current of 1.992mA. The relative accuracy test circuit is shown in Figure 1. The 12-bit converter is calibrated to a full-scale output current of 1.99219mA, then the DAC08 full-scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on the oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total of ± part in 65,536, or ±0.00076%, which is much more accurate than the ±0.19% specification of the DAC08 series.

Monotonicity

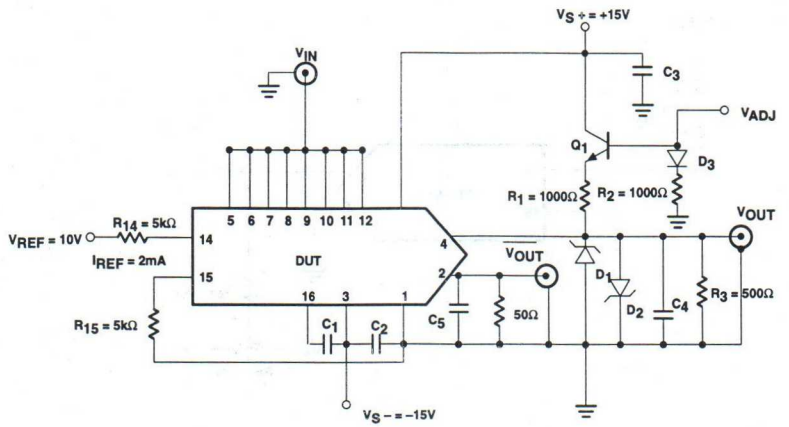
A monotonic converter is one which always provides analog output greater than or equal to the preceding value for a corresponding increment in the digital input code. The DAC08 series is monotonic for all values of reference current above 0.5mA. The recommended range for operation is a DC reference current between 0.5mA and 4.0mA.

Settling Time

The worst-case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all input bits. This time is typically 70ns for settling to within LSB for 8-bit accuracy. This time applies when R_L<500Ω and C_O<25pF. The slowest single switch is the least significant bit, which typically turns on and settles in 65ns. In applications where the DAC functions in a positive-going ramp mode, the worst-case condition does not occur and settling times less than 70ns may be realized.

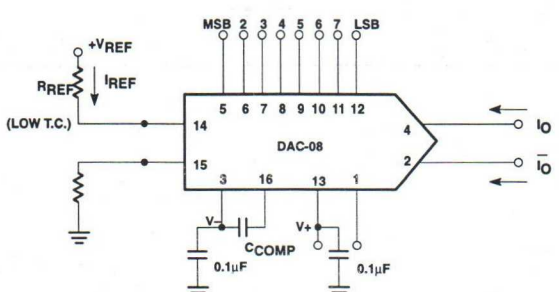
Extra care must be taken in board layout since this usually is the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, minimum scope lead length, and avoidance of ground loops are all mandatory.

SETTLING TIME AND PROPAGATION DELAY



NOTES:
D_1, D_2 = IN6263 or equivalent
D_3 = IN914 or equivalent
C_1 = 0.01μF
C_2, C_3 = 0.1μF
Q_1 = 2N3904
C_4, C_5 = 15pF and includes all probe and fixturing capacitance.

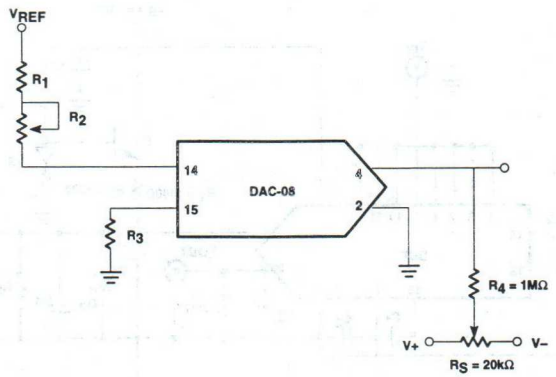
BASIC DAC08 CONFIGURATION



NOTES:

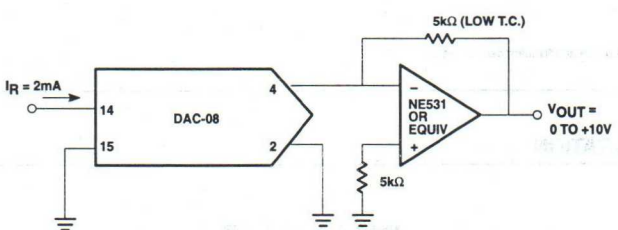
$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256} \; ; \; I_O + \overline{I}_O = I_{FS} \text{ for all logic states}$$

RECOMMENDED FULL-SCALE AND ZERO-SCALE ADJUST

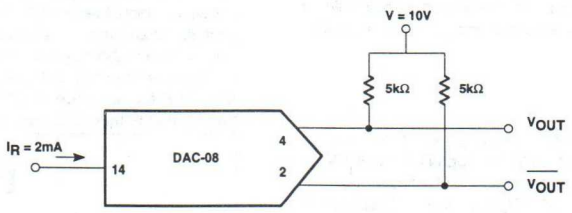


NOTES:
R_1 = low T.C.
$R_3 = R_1 + R_2$
$R_2 = 0.1\ R_1$ to minimize pot. contribution to full-scale drift

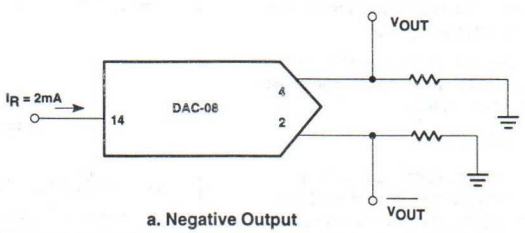
UNIPOLAR VOLTAGE OUTPUT FOR LOW IMPEDANCE OUTPUT



UNIPOLAR VOLTAGE OUTPUT FOR HIGH IMPEDANCE OUTPUT

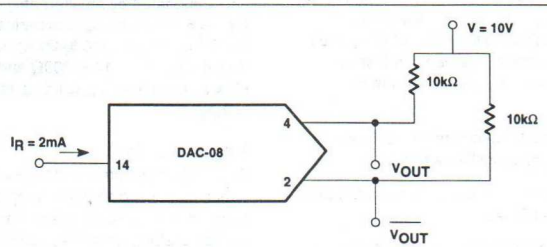


a. Positive Output



a. Negative Output

BASIC BIPOLAR OUTPUT OPERATION (OFFSET BINARY)



	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	V_{OUT}	$\overline{V_{OUT}}$
Positive full-scale	1	1	1	1	1	1	1	1	–9.920V	+10.000
Positive FS – 1LSB	1	1	1	1	1	1	1	0	–9.840V	+9.920
+ Zero-scale + 1LSB	1	0	0	0	0	0	0	1	–0.080V	+0.160
Zero-scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero-scale – 1LSB	0	1	1	1	1	1	1	1	0.080	0.000
Negative full scale – 1LSB	0	0	0	0	0	0	0	1	+9.920	–9.840
Negative full scale	0	0	0	0	0	0	0	0	+10.000	–9.920

Applying the DAC08

AN101

Reference Amplifier Setup

The DAC08 Series are multiplying D-to-A converters in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full-scale output current is a linear function of the reference current and is given by this equalization where $I_{REF}=I_{14}$.

$$I_{FS} = \frac{255}{256} \times I_{REF}$$

In positive reference applications shown in Figure 1, an external positive reference voltage forces current through R14 into the V_{REF} (+) terminal (Pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to V_{REF} (-) at Pin 15, shown in Figure 2. Reference current flows from ground through R14 into V_{REF}(+) as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at Pin 15. The voltage at Pin 14 is equal to and tracks the voltage at Pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors. R15 may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or Pin 15 as shown in Figure 3. The negative common-mode range of the reference amplifier is given by the following equation:

$$V_{CM} - = V - + (I_{REF} \cdot 1k\Omega) + 2.5V$$

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into 2 resistors with the junction bypassed to ground with a 0.1µF capacitor.

For most applications, a +10.0V reference is recommended for optimum full-scale temperature coefficient performance. This will minimize the contributions of reference amplifier V_{OS} and TCV_{OS}. For most applications, the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full-scale trimming which eliminates potentiometer TC effects is shown in Figure 4.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative

common-mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from Pin 16 to V-. For fixed reference operation, a 0.01µF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications".

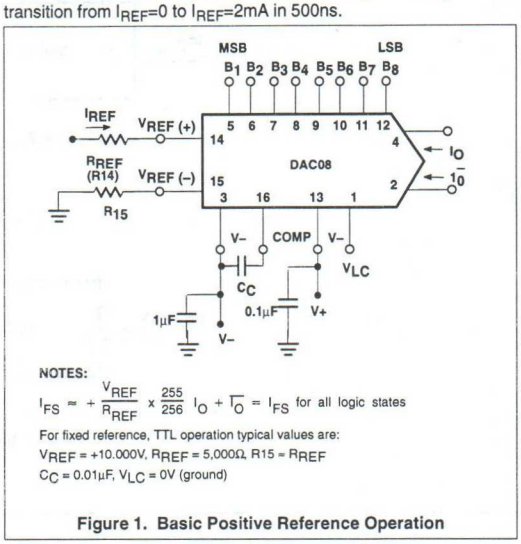
Multiplying Operation

The DAC08 Series provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4mA to 4µA. Monotonic operation is maintained over a typical range of I_{REF} from 100µA to 4.0mA.

Reference Amplifier Compensation for Multiplying Applications

AC reference applications will require the reference amplifier to be compensated using a capacitor from Pin 16 to V-. The value of this capacitor depends on the impedance presented to Pin 14. For R14 values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37 and 75pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin.

For fastest multiplying response, low values of R14 enabling small C_C values should be used. If Pin 14 is driven by a high impedance such as a transistor current source, none of the preceding values will suffice and the amplifier must be heavily compensated, which will decrease overall bandwidth and slew rate. For R14=1kΩ and CC=15pF, the reference amplifier slews at 4mA/µs enabling a transition from I_{REF}=0 to I_{REF}=2mA in 500ns.



NOTES:

$I_{FS} \approx + \frac{V_{REF}}{R_{REF}} \times \frac{255}{256} I_O + \overline{I_O} = I_{FS}$ for all logic states

For fixed reference, TTL operation typical values are:

V_{REF} = +10.000V, R_{REF} = 5,000Ω, R15 = R_{REF}

C_C = 0.01µF, V_{LC} = 0V (ground)

Figure 1. Basic Positive Reference Operation

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme shown in Figure 5. This technique provides lowest full-scale transition times. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at Pin 14 is 200Ω and C_C=0. This yields a reference slew rate of 16mA/µs, which is relatively independent of R_{IN} and V_{IN} values.

Logic Inputs

The DAC08 design incorporates a logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2µA logic input current and completely adjustable logic threshold voltage. For V-=-15V, the logic inputs may swing between -11V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC08 is powered from a +5V supply. Minimum input logic swing is given by the following equation:

$$V - + (I_{REF} \cdot 1k\Omega) + 2.5V$$

The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control in (Pin 1, V_{LC}). Figure 6 shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL and DTL interface, simply ground Pin 1. When interfacing ECL, an I_{REF}=1mA is recommended. For interfacing other logic families, see Figure 7. For general setup of the logic control circuit, it should be noted that Pin 1 may source up to 200µA. External circuitry should be designed to accommodate this current.

Applying the DAC08

AN101

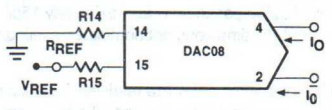


Figure 2. Basic Negative Reference Operation

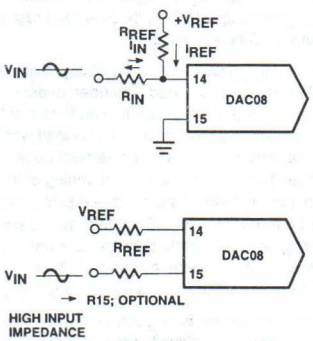


Figure 3. Accommodating Bipolar References

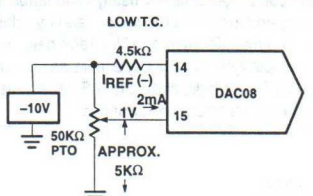


Figure 4. Recommended Full-Scale Adjustment Circuit

Fastest settling times are obtained when Pin 1 sees a low impedance. If Pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

Analog Output Currents

Both true and complemented output sink currents are provided, where $I_O+\overline{I_O}=I_{FS}$. Current appears at the true output when a 1 is applied to each logic input. As the binary count increases, the sink current at Pin 4 increases proportionally, in the fashion of a positive logic D-to-A converter. When a 0 is applied to any input bit, that current is turned off at Pin 4 and turned on at Pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D-to-A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}. Do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V- and is independent of the positive supply. Negative compliance is given by the equation:

$$V - + (I_{REF} \cdot 1k\Omega) + 3.0V$$

Note that lower values of I_{REF} will allow a greater output compliance.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as balanced-bridge A/D circuits, as well as driving center-tapped coils and transformers.

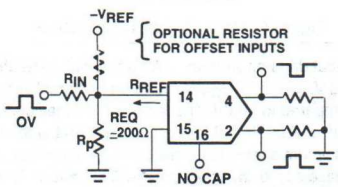


Figure 5. Pulsed Reference Operation

Power Supplies

The DAC08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq 1mA$ is recommended.

Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range. Consult the various figures for guidance. For example, operation at -4.5V with I_{REF}=2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible; however, at least 8V total must be applied between Pins 2 and 4, and Pin 3 to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be useful to insure logic swings, etc., remain between acceptable limits.

Power consumption may be calculated by this equation:

$$P_D = (I+)(V+) + (I+)(V-) + (I_{REF})(V-)$$

A useful feature of the DAC08 design is that supply current is constant and independent of input logic states. This is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

Temperature Performance

The linearity and monotonicity specifications of the DAC08 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is low, typically ±10ppm/°C with zero-scale output current and drift essentially negligible compared to LSB.

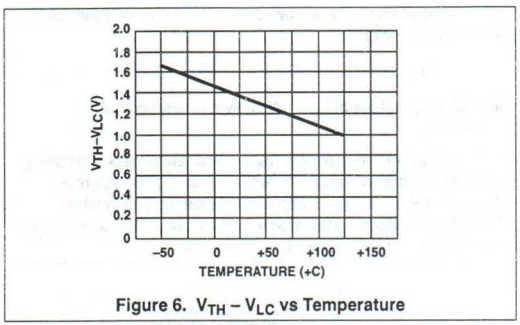


Figure 6. $V_{TH} - V_{LC}$ vs Temperature

Full-scale output drift performance will be best with +10.0V references, as V_{OS} and TCV_{OS} of the reference amplifier will be very small compared to 10.0V. The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC08 decrease approximately 10% at -55°C, and an increase of about 15% at +125°C is typical.

Settling Time

The DAC08 is capable of extremely fast settling times (typically 70ns at I_{REF}=2.0mA).

Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 8 bits. Settling time to within LSB is therefore 35ns, with each progressively larger bit taking successively longer. The MSB settles in 70ns, thus determining the overall settling time of 70ns.

Settling to 6-bit accuracy requires about 55 to 60ns. The output capacitance, including the package, is approximately 15pF. Therefore, the output RC time constant dominates settling time if R_L >500Ω.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4μA. Therefore, a 1kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of Figure 8 uses a cascade design to permit driving a 1kΩ load with less than 5pF of parasite capacitance at the measurement node. At I_{REF} values of less than 1.0mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value; thus, settling time may be observed at lower values of I_{REF}.

The DAC08 switching transients or glitches are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is dependent of input logic states. 0.1μF capacitors at the supply pins provide full transient performance.

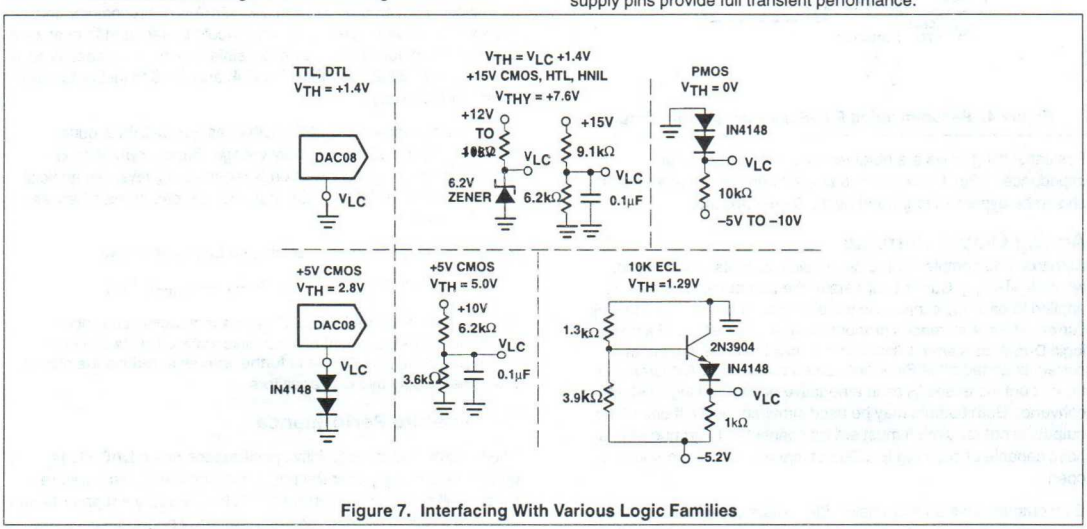


Figure 7. Interfacing With Various Logic Families

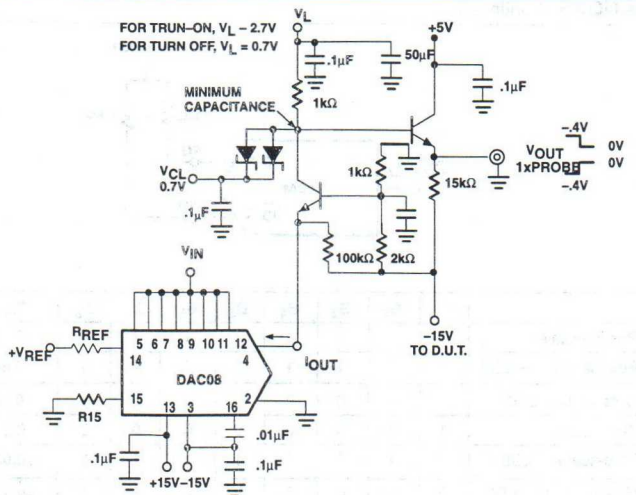
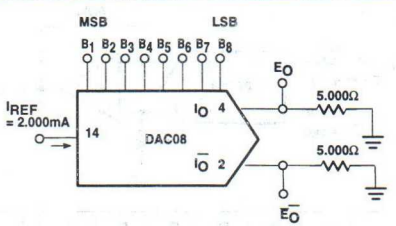


Figure 8. Settling Time Measurement

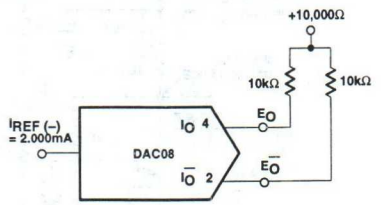
TYPICAL APPLICATIONS



	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	I_O (mA)	$\overline{I_O}$ (mA)	E_O	$\overline{E_O}$
Full-scale	1	1	1	1	1	1	1	1	1.992	0.000	–9.960	0.000
Full-scale — LSB	1	1	1	1	1	1	1	0	1.984	0.008	–9.920	–0.040
Half-scale + LSB	1	0	0	0	0	0	0	1	1.008	0.984	–5.040	–4.920
Half-scale	1	0	0	0	0	0	0	0	1.000	0.992	–5.000	–4.960
Half-scale — LSB	0	1	1	1	1	1	1	1	0.992	1.000	–4.960	–5.000
Zero-scale + LSB	0	0	0	0	0	0	0	1	0.008	1.984	–0.040	–9.920
Zero-scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	–9.960

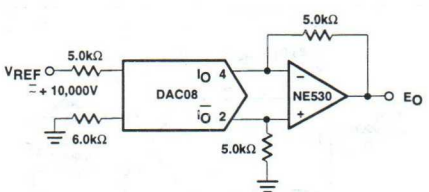
Figure 9. Basic Unipolar Negative Operation

TYPICAL APPLICATIONS (Continued)



	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	E_O	$\overline{E_O}$
Pos full-scale	1	1	1	1	1	1	1	1	–9.920	+10.000
Pos full-scale — LSB	1	1	1	1	1	1	1	0	–9.840	+9.920
Zero-scale + LSB	1	0	0	0	0	0	0	1	–0.080	+0.160
Zero-scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero-scale — LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg full-scale + LSB	0	0	0	0	0	0	0	1	+9.920	–9.840
Neg full-scale	0	0	0	0	0	0	0	0	+10.000	–9.920

Figure 10. Basic Bipolar Output Operation

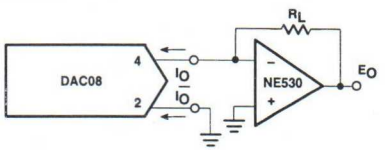


	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	E_O
Pos full-scale	1	1	1	1	1	1	1	1	+9.920
Pos full-scale — LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero-scale	1	0	0	0	0	0	0	0	+0.040
(–) Zero-scale	0	1	1	1	1	1	1	1	–0.040
Neg full-scale + LSB	0	0	0	0	0	0	0	1	–9.840
Neg full-scale	0	0	0	0	0	0	0	0	–9.920

Figure 11. Symmetrical Offset Binary Operation

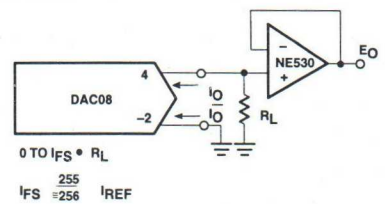
Applying the DAC08

AN101



NOTE:
For complementary output (operation as negative logic DAC), connect inverting input of op amp to I_O (Pin 2); connect $\overline{I_O}$ (Pin 4) to ground.

Figure 12. Positive Low Impedance Output Operation



NOTE:
For complementary output (operation as negative logic DAC), connect inverting input of op amp to I_O (Pin 2); connect $\overline{I_O}$ (Pin 4) to ground.

Figure 13. Negative Low Impedance Output Operation

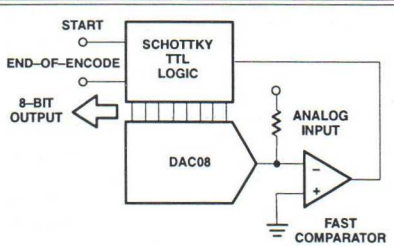
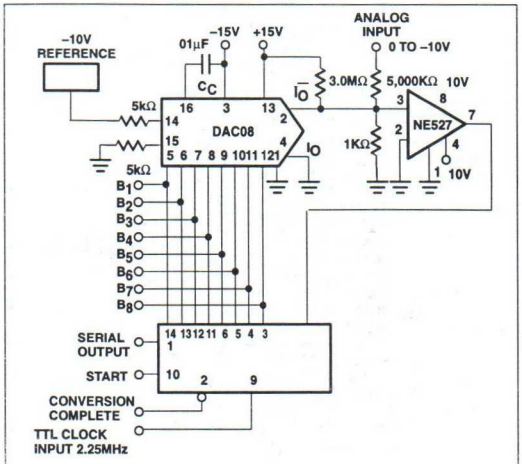
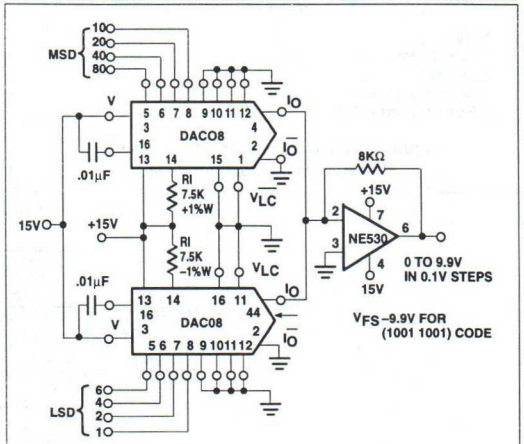


Figure 14. Low Cost 8-Bit 1μs A-to-D Converter



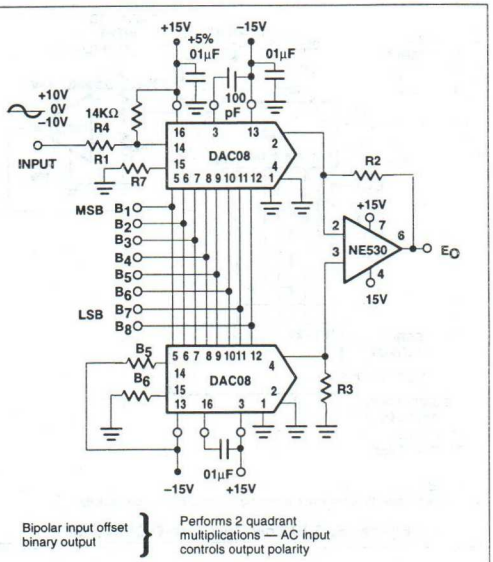
NOTE:
Connect "start" to "conversion complete" for continuous conversions.

Figure 15. 3 IC Low Cost A-to-D Converter



NOTE:
Output is directly proportional to positive power supply.

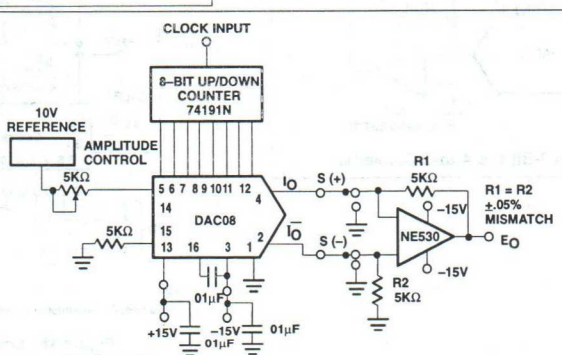
Figure 16. Low Cost 2-Digit BCD DAC



NOTES:

1. R1 = R2 = R3
2. R4 = R5
3. E_O DC to 20kHz = ±5V
4. E_O DC to 10kHz = ±10V

Figure 17. DC-Coupled Digital Attenuator/ Programmable Gain Amplifier



NOTES:

1. Bipolar output is symmetrical around zero, adjustable peak-to-peak amplitude.
2. For triangle wave, count up to full, reverse and count down.
3. For positive-going sawtooth, count up to full, clean, repeat.
4. For negative-going sawtooth, count down, clean, repeat.
5. For other waveforms, use a ROM programmed with the desired function.

Figure 18. High-Speed Waveform Generator

Digital attenuator

AN105

Figure 1 shows a DC-coupled Digital Attenuator or Programmable Gain Amplifier

Pin 14 of the DAC is a Virtual Ground. Current must always flow into Pin 14, so the current through R4 must be greater than that through R1 when the input signal is at its most negative usable value. If the input signal value goes low enough to cause the current through R1 to be greater than that through R4, output clipping will occur.

To extend the operating frequency range, the compensation cap, C_C, needs to be minimized, which implies that the resistance at Pin 14 (R1 and R4) must be minimized. If the voltage to which R4 and R5 are returned has any noise on it at all, R4 and RS should be formed of two series resistors with the junction of them bypassed with 0.1μF to ground. Pin 15 could be grounded with a small sacrifice in accuracy and temperature drift. R6 and R7 compensate for reference amplifier input off set.

R1 and R4 should be chosen such that, when the input is at peak usable signal, the total current into Pin 14 does not exceed 4mA. When the input is most negative, R1 current must be less than R4 current (remember, Pin 14 is always at 0V). Also, when the input is at its absolute positive peak value, current into Pin 14 should not exceed 5mA. Minimum compensation capacitor, (C_C), in pF is 15 times the parallel combination of R1 and R4 in kΩ.

With a single DAC, there is a DC offset at the circuit output that varies with the digital word input. To eliminate this, we use a second DAC to subtract this offset at the sum node of the op amp.

Example 1: Input signal is to be 20Vp p, centered at 0V. Maximum input frequency is to be 15kHz. Power supplies available are ±15V, both regulated. Determine values of all resistors for maximum gain of unity.

Solution 1: At minimum input (-10V), reference current, I_{REF} is

$$I_{REF} = \frac{15V}{R4} + \frac{(-10V)}{R1}$$

If minimum $I_{REF} = 0$, then

$$\frac{15V}{R4} = \frac{10V}{R1}$$

and R4 = (1.5)(R1)

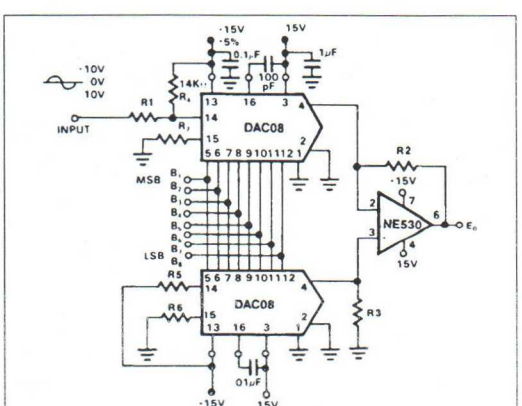


Figure 1.

Therefore, 60% of I_{REF} comes through R4. If we let I_{REF} go to about 3.9mA (4mA is max. recommended), R4 current is found to be I_{R4} = (0.6) (3.9mA) = 2.34mA and R4 = 6.4k.

The balance of the reference current I_{R1} is found to be

$I_{R1} = 3.9mA - I_{R4}$

or

$I_{R1} = 3.9mA - 234mA = 1.56mA$

and

$R1 = 6.4k$

Using commonly available values, and remembering that R4 current must exceed R 1 current, we set

R1 = 6.8k

and R4 = 6.2k.

Maximum reference current is now

$$I_{REF}(max) = \frac{15V}{6.2k} + \frac{10V}{6.8k} = 3.9mA$$

The parallel combination of R1 and R4 is found to be 3.24k, so minimum compensation capacitor value is

$C_C(min) = (3.24)(15)pF = 48.6pF$

If we use 50pF, from the graph we find f_{MAX} to be 370kHz. For unity gain,

R2 = R1 = 6.8k

R3 = R2 = 6.8k

RS = R1 = 6.8k

$$R6 = R7 = \frac{(R1)(R4)}{R1 + R4} = 3.24k$$

Example 2: Usable input signal is $12V_{P-P}$, centered at 0V, with occasional excursion to twice this amplitude, which we do not care about. Maximum input frequency is to be 500kHz. Available power supplies are +5V logic supply, +15V, –15V, all regulated. Determine values of all resistors and C_C for maximum gain of 2.

Solution 2: To extend the frequency response, we want minimum compensation capacitor value; therefore, we need minimum R1 and R4 values, so we want to return R4 to as low a regulated supply as is possible; we will use the 5V logic supply.

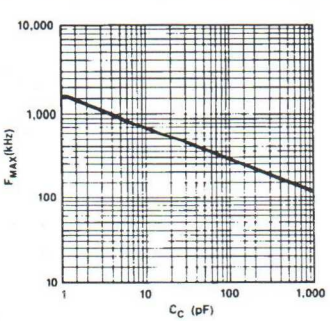


Figure 2.

Digital attenuator

AN105

At minimum usable input,

$$I_{REF} = \frac{5V}{R4} + \frac{6V}{R1}$$

or, for

$$I_{REF} = 0, \frac{5V}{R4} = \frac{6V}{R1}$$

therefore, 55% of I_{REF} comes through R4, and

R4 = (5/6)R1.

Because peak input goes to +12V, this condition should not cause I_{REF} to exceed 5mA, and

$$\frac{12V}{R1} + \frac{5V}{R4} = 5mA$$

Recall that R4 = (5/6)R1.

$$\frac{12V}{R1} = \frac{6V}{R1} = 5mA$$

R1 = 3.6k

and R4 = (5/6)R1 = 3.0k.

Because the reference source will be the 5V logic supply, which will be noisy, we will split R4 into two resistors and bypass their junction with 0.1µF to ground. Furthermore, to be sure that R4 current exceeds R1 current, we will increase R1 to 4.3k. The absolute maximum reference current is now

$$I_{REF}(max) = \frac{12V}{4.3k} + \frac{5V}{3k} = 4.46mA.$$

The parallel combination of R1 and R4 is 1.77k, so minimum compensation capacitor is

$C_C(min) = (15)(1.77) = 26.5pF.$

If we use 27pF, the graph tells us the maximum frequency is about 470kHz, which is 6% lower than desired. If we wanted to further extend this frequency range, we find that we can reduce R4 to two resistors of 1.1k and 1.2k, bringing the absolute maximum reference current to

$$I_{REF}(max) = \frac{12V}{4.3k} + \frac{5V}{2.3k} = 4.96mA.$$

and the maximum usable reference current becomes

$$I_{REF}(max) = \frac{6V}{4.3k} + \frac{5V}{2.3k} = 3.57mA.$$

below the 5mA and 4mA respective desired maximum values. Now the resistance at Pin 14 is the parallel combination of R1 and R4, or 1.5k, and the minimum compensation capacitor becomes

$C_C(min) = (15)(1.5)pF = 22pF.$

The graph tells us we can just go to 500kHz.

8-bit multiplying D/A converter

MC1508-8/1408-8

DESCRIPTION

The MC1508/MC1408 series of 8-bit monolithic digital-to-analog converters provide high-speed performance with low cost. They are designed for use where the output current is a linear product of an 8-bit digital word and an analog reference voltage

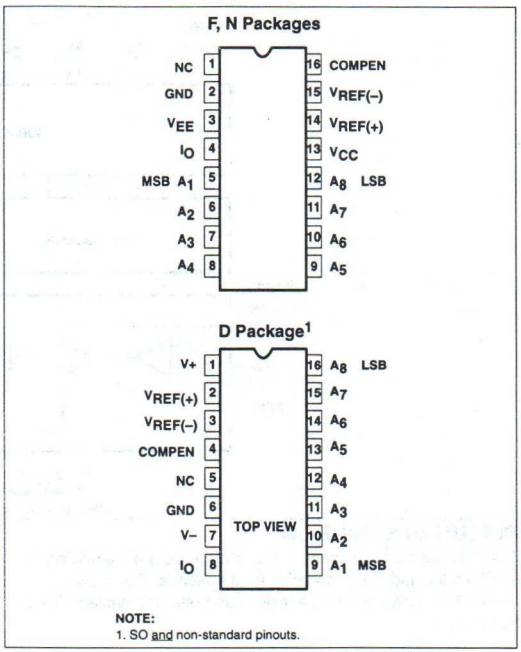
FEATURES

- Fast settling time — 70ns (typ)
- Relative accuracy ±0.19% (max error)
- Non-inverting digital inputs are TTL and CMOS compatible
- High-speed multiplying rate 4.0mA/μs (input slew)
- Output voltage swing +0.5V to –5.0V
- Standard supply voltages +5.0V and –5.0V to –15V
- Military qualifications pending

APPLICATIONS

- Tracking A-to-D converters
- 2 1/2-digit panel meters and DVMs
- Waveform synthesis
- Sample-and-Hold
- Peak detector
- Programmable gain and attenuation
- CRT character generation
- Audio digitizing and decoding
- Programmable power supplies
- Analog-digital multiplication
- Digital-digital multiplication
- Analog-digital division
- Digital addition and subtraction
- Speech compression and expansion
- Stepping motor drive modems
- Servo motor and pen drivers

PIN CONFIGURATIONS

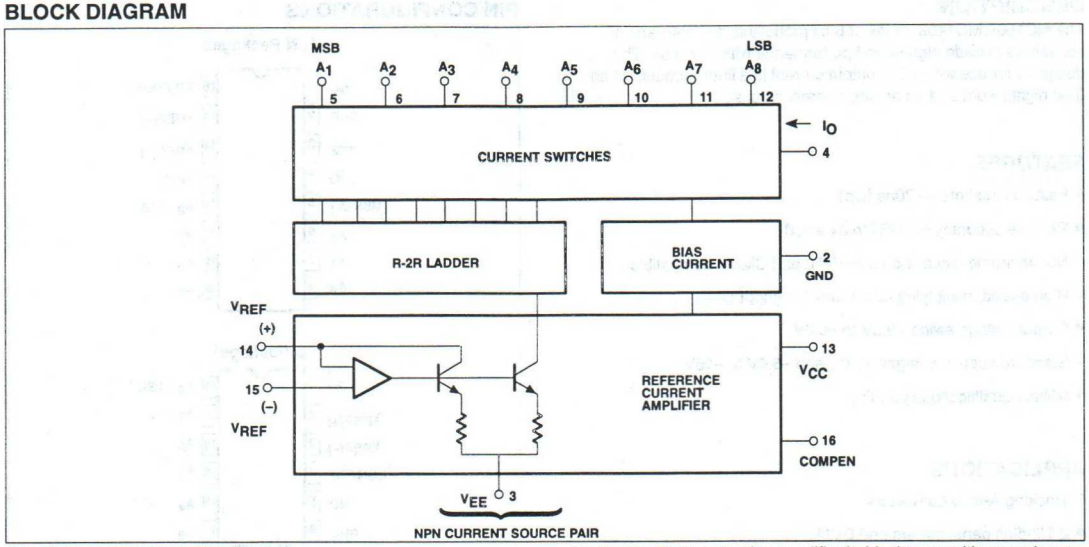


NOTE:
1. SO and non-standard pinouts.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Ceramic Dual In-Line Package (CERDIP)	-55 to +125°C	MC1508-8F	0582B
16-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	MC1408-8F	0582B
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	MC1408-8N	0406C
16-Pin Small Outline (SO) Package	0 to +70°C	MC1408-8D	0005D

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The MC1508/MC1408 consists of a reference current amplifier, an R-2R ladder, and 8 high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are non-inverting in operation; therefore, a high state on the input turns on the specified output current component.

The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992mA for a 2.0mA reference amplifier current if the NPN current source pair is perfectly matched.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Positive power supply voltage	+5.5	V
V_{EE}	Negative power supply voltage	–16.5	V
$V_5 - V_{12}$	Digital input voltage	0 to V_{CC}	V
V_O	Applied output voltage	–5.2 to +18	V
I_{14}	Reference current	5.0	mA
V_{14}, V_{15}	Reference amplifier inputs	V_{EE} to V_{CC}	
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1]		
	F package	1190	mW
	N package	1450	mW
	D package	1080	mW
T_{SOLD}	Lead soldering temperature (10 sec)	300	°C
T_A	Operating temperature range	300	°C
	MC1508	–55 to +125	°C
	MC1408	0 to +75	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Derate above 25°C, at the following rates: F package at 9.5mW/°C; N package at 11.6mW/°C; D package at 8.6mW/°C

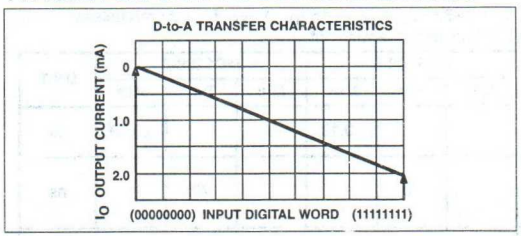
DC ELECTRICAL CHARACTERISTICS

Pin 3 must be 3V more negative than the potential to which R_{15} is returned. V_{CC} = +5.0V_{DC}, V_{EE} = −15V_{DC}, V_{REF}/R_{14} = 2.0mA unless otherwise specified. MC1508: T_A = −55°C to 125°C. MC1408: T_A = 0°C to 75°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1508-8			MC1408-8			UNIT
			Min	Typ	Max	Min	Typ	Max	
E_r	Relative accuracy	Error relative to full-scale I_O, Figure 3			±0.19			±0.19	%
t_S	Settling time[1]	To within 1/2 LSB, includes t_{PLH}, T_A = +25°C, Figure 4		70			70		ns
t_{PLH} t_{PHL}	Propagation delay time Low-to-High High-to-Low	T_A = +25°C, Figure 4		35	100		35	100	ns
TCI_O	Output full-scale current drift			−20			−20		ppm/°C
V_{IH} V_{IL}	Digital input logic level (MSB) High Low	Figure 5	2.0		0.8	2.0		0.8	V_{DC}
I_{IH} I_{IL}	Digital input current (MSB) High Low	Figure 5 V_{IH} = 5.0V V_{IL} = 0.8V		0 −0.4	0.04 −0.8		0 −0.4	0.04 −0.8	mA
I_{15}	Reference input bias current	Pin 15, Figure 5		−1.0	−5.0		−1.0	−5.0	µA
I_{OR}	Output current range	Figure 5 V_{EE} = −5.0V V_{EE} = −7.0V to −15V	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	mA
I_O $I_{O(min)}$	Output current Off-state	Figure 5 V_{REF} = 2.000V, R14 = 1000Ω All bits low	1.9	1.99 0	2.1 4.0	1.9	1.99 0	2.1 4.0	mA µA
V_O	Output voltage compliance	E_r ≤ 0.19% at T_A = +25°C, Figure 5 V_{EE} = −5V V_{EE} below −10V		−0.6 +10 −5.5, +10	−0.55, +0.5 −5.0, +0.5		−0.6 +10 −5.5, +10	−0.55, +0.5 −5.0, +0.5	V_{DC}
SRI_{REF}	Reference current slew rate	Figure 6		8.0			8.0		mA/µs
PSRR(−)	Output current power supply sensitivity	I_{REF} = 1mA		0.5	2.7		0.5	2.7	µA/V
I_{CC} I_{EE}	Power supply current Positive Negative	All bits low, Figure 5		+2.5 −6.5	+22 −13		+2.5 −6.5	+22 −13	mA
V_{CCR} V_{EER}	Power supply voltage range Positive Negative	T_A = +25°C, Figure 5	+4.5 −4.5	+5.0 −15	+5.5 −16.5	+4.5 −4.5	+5.0 −15	+5.5 −16.5	V_{DC}
P_D	Power dissipation	All bits low, Figure 5 V_{EE} = −5.0V_{DC} V_{EE} = −15.0V_{DC}		34 110	170 305		34 110	170 305	mW

NOTES:
1. All bits switched.

TYPICAL PERFORMANCE CHARACTERISTICS



FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier input current must always flow into Pin 14. regardless of the setup method or reference supply voltage polarity.

Connections for a positive reference voltage are shown in Figure 1. The reference voltage source supplies the full reference current. For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. R_{15} may be eliminated and Pin 15 grounded, with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increasing values of R_{14} to maintain proper phase margin. For R_{14} values of 1.0, 2.5, and 5.0kΩ, minimum capacitor values are 15, 37, and 75pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection. (Fluctuations in the negative supply have more effect on accuracy than do any changes in the positive supply.)

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15}, as shown in Figure 2. A high input impedance is the main advantage of this method. The negative reference voltage must be at least 3.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at Pin 15.

Capacitive bypass to ground is recommended when a DC reference voltage is used. The 5.0V logic supply is not recommended as a reference voltage, but if a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be formed of two series resistors and the junction of the two resistors bypassed with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between Pin 14 and ground.

If Pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage at Pin 4 must always be at least 4.5V more positive than the voltage of the negative supply (Pin 3) when the reference current is 2mA or less, and at least 8V more positive than the negative supply when the reference current is between 2mA and 4mA. This is necessary to avoid saturation of the output transistors, which would cause serious degradation of accuracy.

Philips Semiconductors MC1508/MC1408 does not need a range control because the design extends the compliance range down to 4.5V (or 8V — see above) above the negative supply voltage without significant degradation of accuracy. Philips Semiconductors MC1508/MC1408 can be used in sockets designed for other manufacturers' MC1508/MC1408 without circuit modification.

Output Current Range

Any time the full-scale current exceeds 2mA, the negative supply must be at least 8V more negative than the output voltage. This is due to the increased internal voltage drops between the negative supply and the outputs with higher reference currents.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy, full-scale accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current after zero-scale current has been nulled out. The relative accuracy of the MC1508/MC1408 is essentially constant over the operating temperature range because of the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current; however, the MC1508/MC1408 has a very low full-scale current drift over the operating temperature range.

The MC1508/MC1408 series is guaranteed accurate to within ±1/2LSB at +25°C at a full-scale output current of 1.99mA. The relative accuracy test circuit is shown in Figure 3. The 12-bit converter is calibrated to a full-scale output current of 1.99219mA; then the MC1508/MC1408's full-scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on the oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total of ±1/2 part in 65,536, or ±0.00076%, which is much more accurate than the ±0.19% specification of the MC1508/MC1408.

Monotonicity

A monotonic converter is one which always provides an analog output greater than or equal to the preceding value for a corresponding increment in the digital input code. The MC1508/MC1408 is monotonic for all values of reference current above 0.5mA. The recommended range for operation is a DC reference current between 0.5mA and 4.0mA.

Settling Time

The worst case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all input bits. This time is typically 70ns for settling to within 1/2LSB for 8-bit accuracy. This time applies when $R_L < 500Ω$ and $C_O < 25pF$. The slowest single switch is the least significant bit, which typically turns on and settles in 65ns. In applications where the D-to-A converter functions in a positive going ramp mode, the worst-case condition does not occur and settling times less than 70ns may be realized.

Extra care must be taken in board layout since this usually is the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, minimum scope lead length, good ground planes, and avoidance of ground loops are all mandatory.

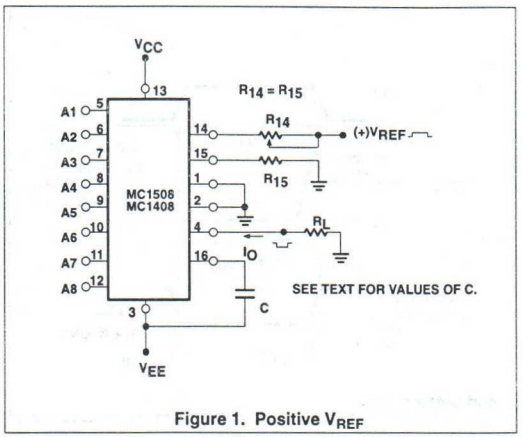


Figure 1. Positive V_{REF}

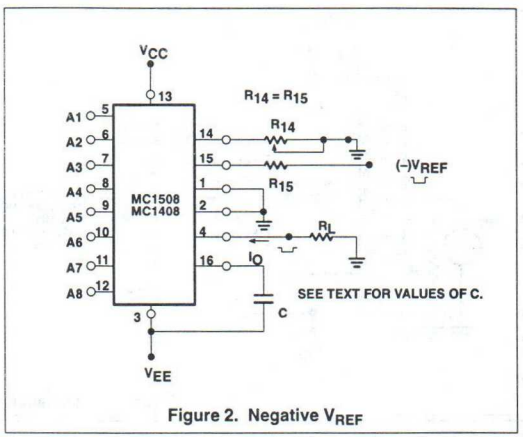


Figure 2. Negative V_{REF}

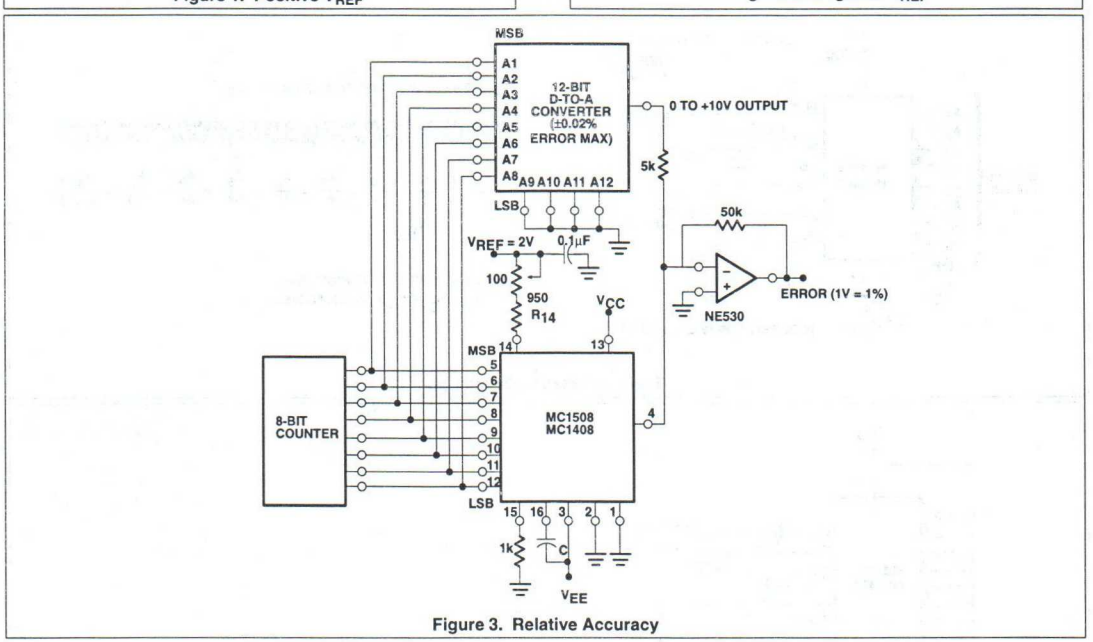
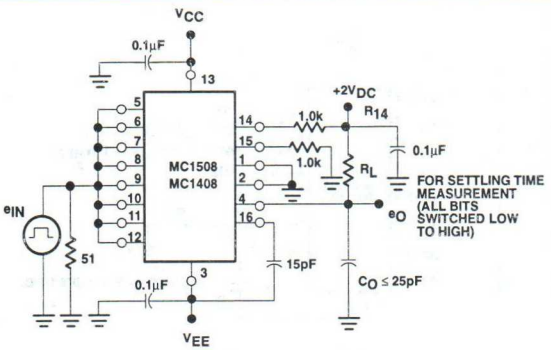


Figure 3. Relative Accuracy



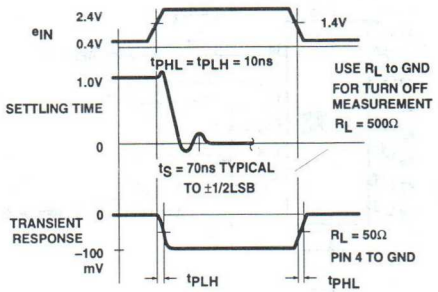
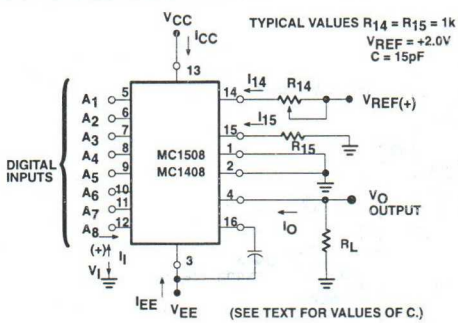


Figure 4. Transient Response and Settling Time



VI AND II APPLY TO INPUTS A1 THROUGH A8

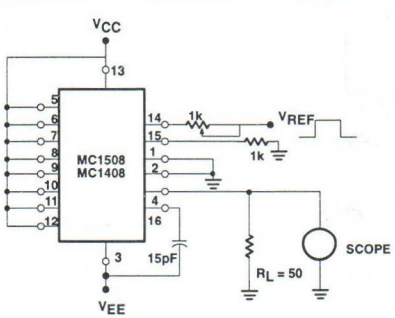
THE RESISTOR TIED TO PIN 15 IS TO TEMPERATURE COMPENSATE THE BIAS CURRENT AND MAY NOT BE NECESSARY FOR ALL APPLICATIONS

$$I_O = K\left\{\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256}\right\}$$

where $K = \frac{V_{REF}}{R_{14}}$

and A_N = "1" IF A_N IS AT HIGH LEVEL
A_N = "0" IF A_N IS AT LOW LEVEL

Figure 5. Notation Definitions



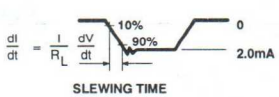


Figure 6. Reference Current Slew Rate Measurement

10-Bit high-speed multiplying D/A converter

MC3410, MC3410C

DESCRIPTION

The MC3410 series are 10-bit Multiplying Digital-to-Analog Converters. They are capable of high-speed performance, and are used as general-purpose building blocks in cost-effective D/A systems.

The Philips Semiconductors design provides complete 10-bit accuracy without laser trimming, and guaranteed monotonicity over temperature. Segmented current sources, in conjunction with an R-2R DAC provides the binary weighted currents. The output buffer amplifier and voltage reference have been omitted to allow greater speed, lower cost, and maximum user flexibility.

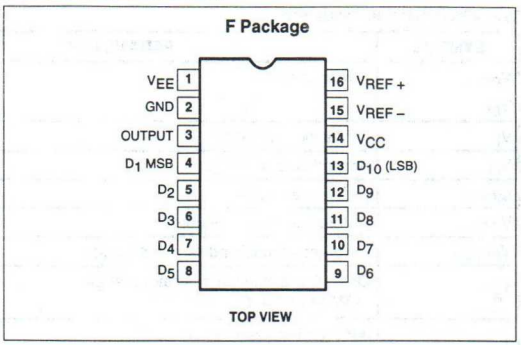
FEATURES

- 10-bit resolution and accuracy (±0.05%)
- Guaranteed monotonicity over temperature
- Fast settling time—250ns typical
- Digital inputs are TTL and CMOS compatible
- Wide output voltage compliance range
- High-speed multiplying input slew rate—20mA/μs
- Reference amplifier internally-compensated
- Standard supply voltages +5V and -15V

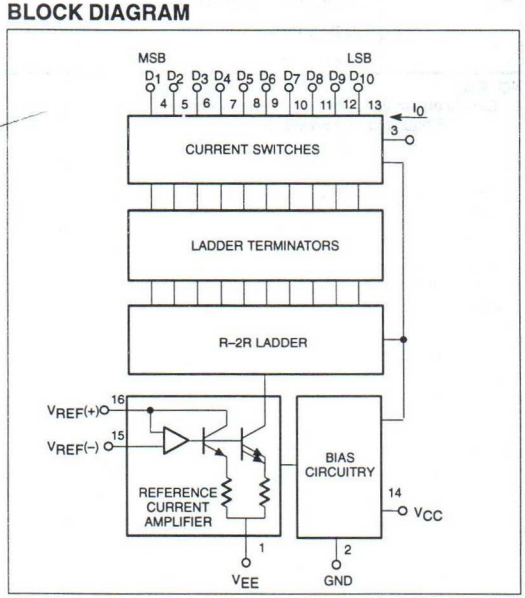
APPLICATIONS

- Successive approximation A/D converters
- High-speed, automatic test equipment
- High-speed modems
- Waveform generators
- CRT displays
- Strip CHART and X-Y plotters
- Programmable power supplies
- Programmable gain and attenuation

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	MC3410F	0582B
16-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	MC3410CF	0582B

ABSOLUTE MAXIMUM RATINGS

T_A=+25°C unless otherwise noted

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	+7.0	V_{DC}
V_{EE}		-18	V_{DC}
V_I	Digital input voltage	+15	V_{DC}
V_O	Applied output voltage	0.5, -5.0	V_{DC}
$I_{REF(16)}$	Reference current	2.5	mA
V_{REF}	Reference amplifier inputs	V_{CC}, V_{EE}	V_{DC}
$V_{REF(D)}$	Reference amplifier differential inputs	0.7	V_{DC}
T_A	Operating ambient temperature range MC3410, 3410C	0 to +70	°C
T_J	Junction temperature, ceramic package	+150	°C
P_D	Maximum power dissipation, T_A=25°C (still-air)[1] F package	1190	mW

NOTES:

1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C

ELECTRICAL CHARACTERISTICS

V_{CC}=+5.0VDC, V_{EE}=-15DC, $\frac{V_{REF}}{R16}$ =2.0mA, all digital inputs at high logic level. MC3410 Series: T_A=0°C to +70°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MC3410			MC3410C			UNIT
			Min	Typ	Max	Min	Typ	Max	
E_r	Relative accuracy (error relative to full-scale I_O)	T_A=25°C			±0.05			±0.1	%
					1/4			1/2	LSB
TCE_r	Relative accuracy drift (relative to full-scale I_O)			2.5			2.5		ppm/°C
	Monotonicity	Over temperature	10			10			Bits
t_S	Settling time to within ± LSB (all bits LOW-to-HIGH)	T_A=25°C		250			250		ns
t_{PLH} t_{PHL}	Propagation delay time	T_A=25°C		35 20			35 20		ns
TCI_O	Output full scale current drift				60			70	ppm/°C
V_{IH}	Digital input logic levels (all bits) HIGH-level, Logic "1" LOW-level, Logic "0"		2.0		0.8	2.0		0.8	V_{DC}
I_{IH} I_{IL}	Digital input current (all bits) HIGH-level, V_{IH}=5.5V LOW-level, V_{IL}=0.8V			 -0.05	+.04 -0.4		 -0.05	+.04 -0.4	mA
$I_{REF(15)}$	Reference input bias current (Pin 15)			-1.0	-5.0		-1.0	-5.0	µA
I_{OR}	Output current range			4.0	5.0		4.0	5.0	mA
I_{OH}	Output current (all bits high)	V_{REF}=2.000V, R_{16}=1000Ω	3.8	3.996	4.2	3.8	3.996	4.2	mA
I_{OL}	Output current (all bits low)	T_A=25°C		0	2.0		0	4.0	µA
V_O	Output voltage compliance	T_A=25°C			-2.5 +0.2			-2.5 +0.2	V_{DC}
SR I_{REF}	Reference amplifier slew rate			20			20		mA/µs
ST I_{REF}	Reference amplifier settling time	0 to 4.0mA, ±0.1%		2.0			2.0		µs
PSRR(-)	Output current power supply sensitivity			0.003	0.01		0.003	0.02	%/%
C_O	Output capacitance	V_O=0		25			25		pF
C_I	Digital input capacitance (all bits high)			4.0			4.0		pF
I_{CC} I_{EE}	Power supply current (all bits low)			 -11.4	+18 -20		 -11.4	+18 -20	mA
V_{CC} V_{EE}	Power supply voltage range	T_A=25°C	+4.75 -14.25	+5.0 -15	+5.25 -15.75	+4.75 -14.25	+5.0 -15	+5.25 -15.75	V_{DC}
	Power consumption (all bits low) (all bits high)			220 200	380		220 200	380	mW

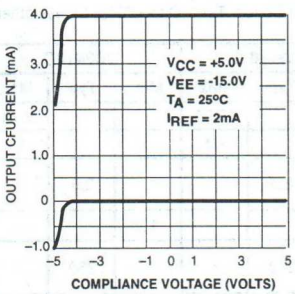


Figure 1. Output Current vs Output Compliance Voltage

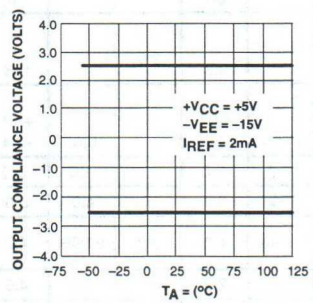


Figure 2. Maximum Output Compliance Voltage vs Temperature

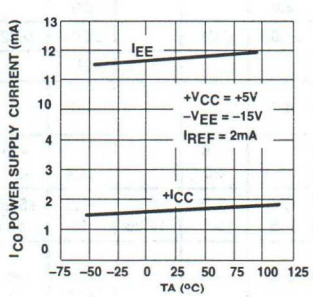


Figure 3. Power Supply Current vs Temperature

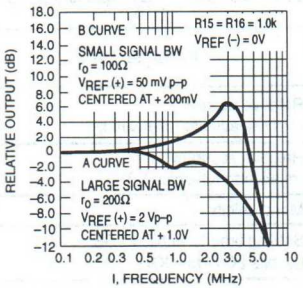


Figure 4. Reference Amplifier Frequency Response

CIRCUIT DESCRIPTION

The MC3410 consists of four segment current sources which generate the two most significant bits (MSBs), and an R-2R DAC implemented with ion-implanted resistors for scaling the remaining eight least significant bits (LSBs) (See Figure 5). This approach provides complete 10-bit accuracy without trimming.

The individual bit currents are switched ON or OFF by fully differential current switches. The switches use current steering for speed.

An on-chip high-slew reference current amplifier drives the R-2R ladder and segment decoder. The currents are scaled in such a way that, with all bits on, the maximum output current is two times 1023/1024 of the reference amplifier current, or nominally 3.996mA for a 2.000mA reference input current. The reference amplifier allows the user to provide a voltage input. Out-board resistor R_{16} (see Figure 6) converts this voltage to a usable current. A current mirror doubles this reference current and feeds it to the segment decoder and resistor ladder. Thus, for a reference voltage of 2.0V and a 1kΩ resistor tied to Pin 16, the full-scale current is approximately 4.0mA. This relationship will remain regardless of the reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6a. For negative reference voltage inputs, or for bipolar reference voltage inputs in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. For a negative reference input, R_{16} should be grounded (Figure 6b). In addition, the negative voltage reference must be at least 3V above the V_{EE} supply voltage for best operation. Bipolar input signals may be handled by connecting R_{16} to a positive voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic, is to be used as the reference, R_{16} should be decoupled by connecting it to the +5.0V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1μF capacitor to ground.

The reference amplifier is internally-compensated with a 10pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R_{16} and reference voltages which supply 2.0mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0mA. As R_{16} increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R_{16}=1.0kΩ, and settling time is ≈ 10μs. The reference amplifier phase margin decreases as the current source value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5mA for stability.

OUTPUT VOLTAGE COMPLIANCE

The output voltage compliance ranges from -2.5 to +0.2V. As shown in Figure 2, this compliance range is nearly constant over temperature. At the temperature extremes, however, the compliance voltage may be reduced if V_{EE}>-15V.

ACCURACY

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full-scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full-scale current. The relative accuracy of the MC3410 is fairly constant over temperature due to the excellent temperature tracking, of the implanted resistors. The full-scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the MC3410 has a low full-scale current drift with temperature.

The MC3410 are accurate to within ±0.05% at 25°C with a reference current of 2.0mA on Pin 16.

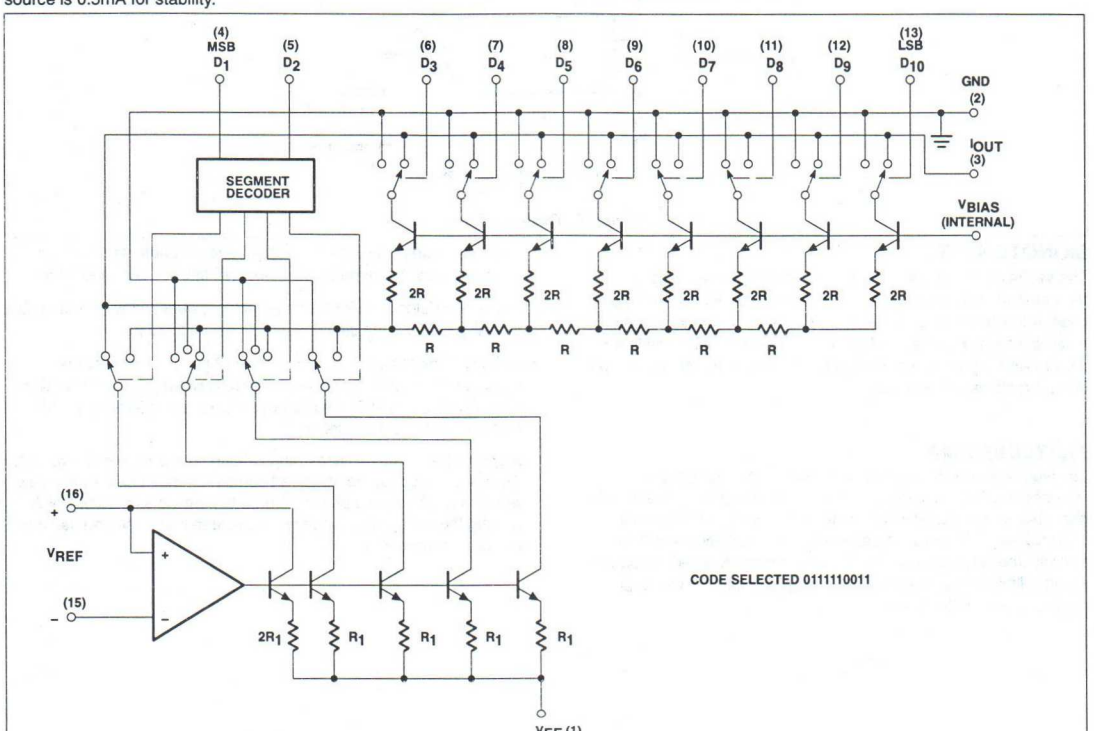


Figure 5. MC3410 Equivalent Circuit

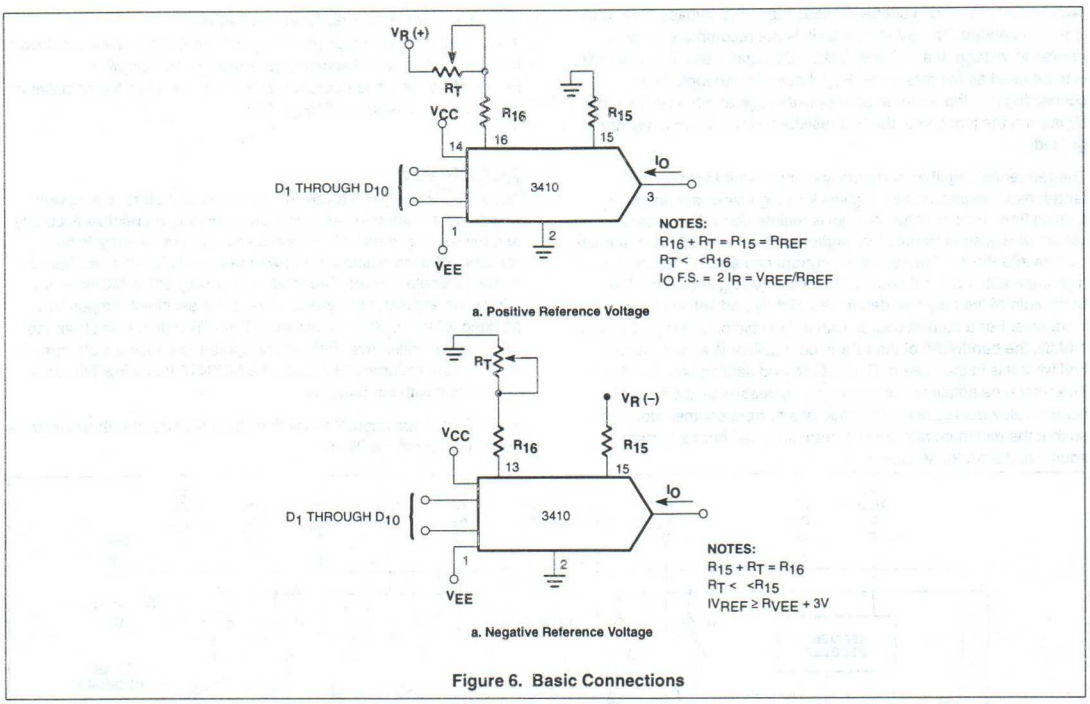


Figure 6. Basic Connections

MONOTONICITY

The MC3410 and MC3410C are guaranteed monotonic over temperature. This means that for every increase in the input digital code, the output current either remains the same or increases but never decreases. In the multiplying mode, where reference input current will vary, monotonicity can be assured if the reference input current remains above 0.5mA.

SETTLING TIME

The worst-case switching condition occurs when all bits are switched "on," which corresponds to a low-to-high transition for all bits. This time is typically 250ns for the output to settle to within ±1/2LSB for 10-bit accuracy, and 200ns for 8-bit accuracy. The turn-off time is typically 120ns. These times apply when the output swing is limited to a small (<0.7V) swing and the external output capacitance is under 25pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

If a load resistor of 625Ω is connected to ground, allowing the output to swing to -2.5V, the settling time increases to 1.5μs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing, and minimum scope lead length are all necessary.

A typical test setup for measuring settling time is shown in Figure 7. The same setup for the most part can be used to measure the slew rate of the reference amplifier (Figure 9) by tying all data bits high, pulsing the voltage reference input between 0 and 2V, and using a 500Ω load resistor R_L.

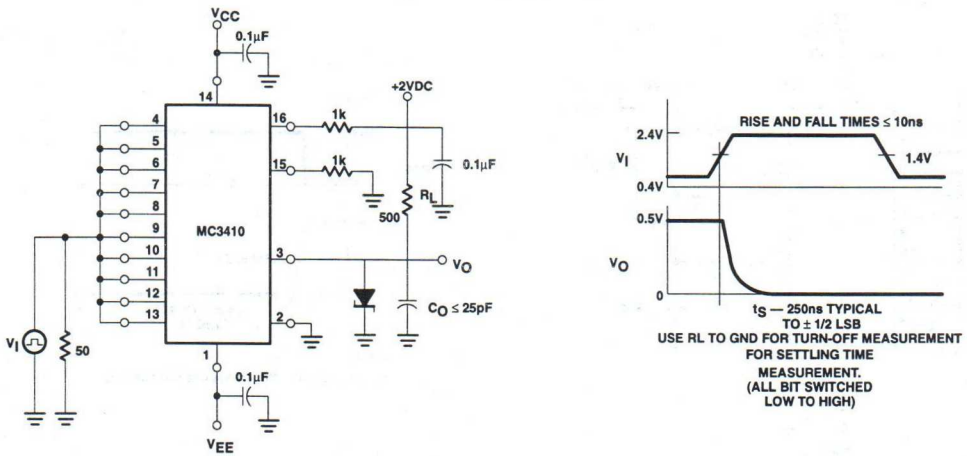


Figure 7. Settling Time

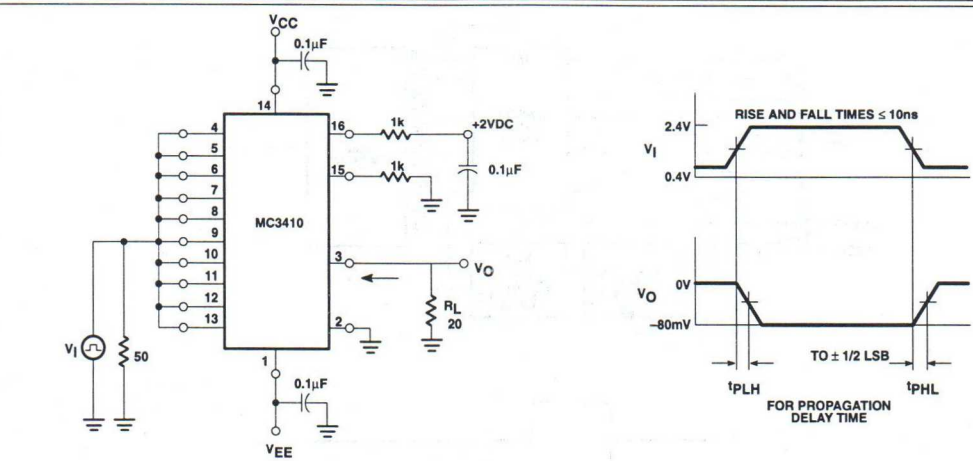


Figure 8. Propagation Delay Time

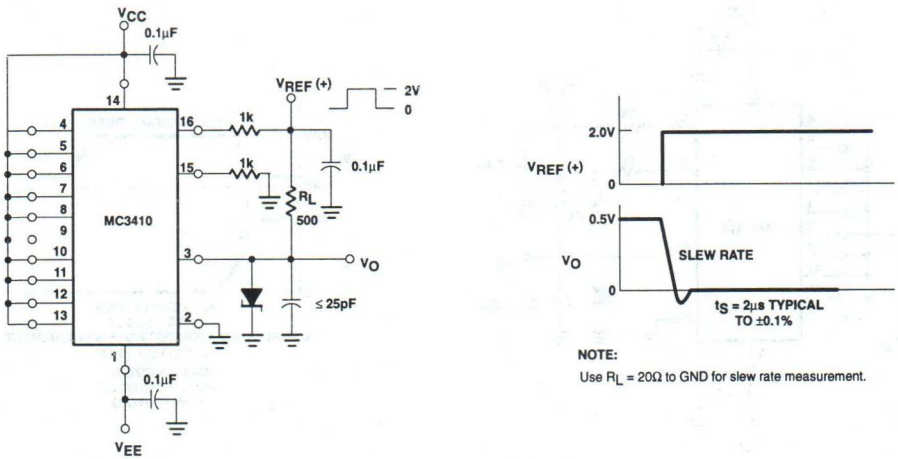


Figure 9. Reference Amplifier Settling Time and Slew Rate

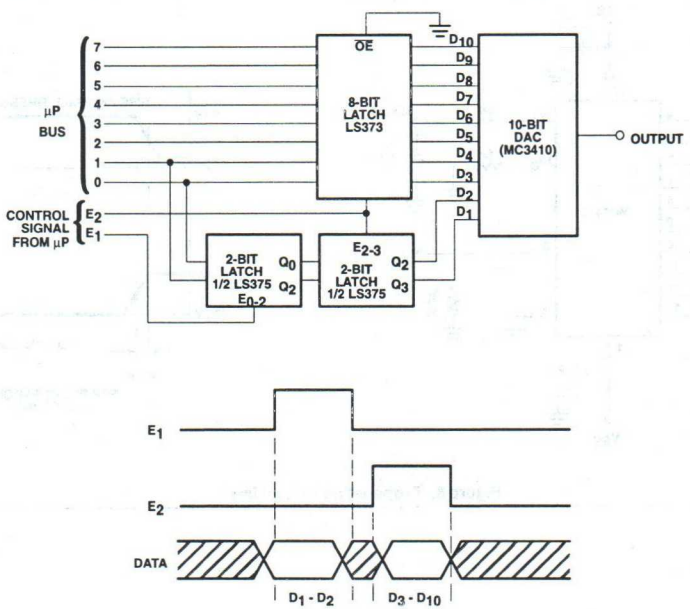


Figure 10. Interfacing 10-Bit DAC With 8-Bit Microprocessor

8-Bit μp-compatible D/A converter

NE/SE5018/5019

DESCRIPTION

The NE/SE5018/19 is a complete 8-bit digital-to-analog converter subsystem on one monolithic chip. The data inputs have input latches which are controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal) and high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full-scale while maintaining a low temperature coefficient.

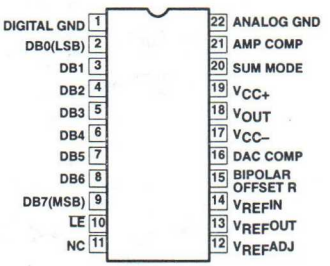
The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

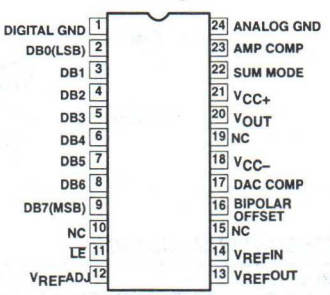
- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Output buffer amplifier
- Accurate to ± LSB (0.19%)
- Monotonic to 8 bits
- Amplifier and reference both short-circuit protected
- Compatible with 8085, 6800 and many other μPs

PIN CONFIGURATIONS

F, N Packages



D Package[1]



NOTE:
1. SOL and non-standard pinout

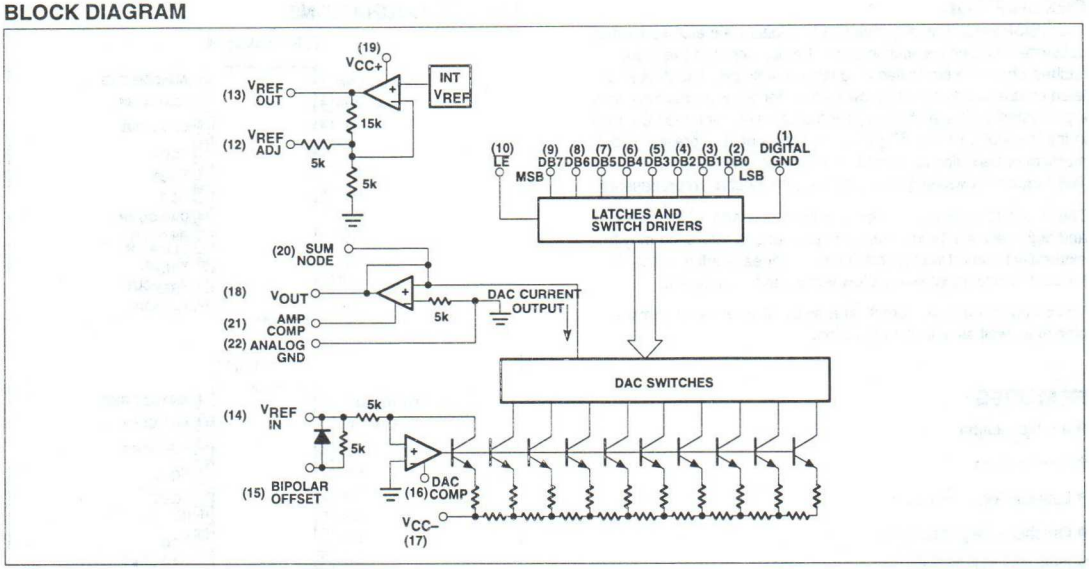
APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
22-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE5018/5019F	0585B
22-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE5018/5019F	0585B
22-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5018/5019N	0409B
22-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE5018/5019N	0409B
24-Pin Small Outline Large (SOL) Package	0 to +70°C	NE5018/5019D	0173D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	-18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF\ IN}$	Voltage at V_{REF} input	12	V
V_{REF} ADJ	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
$I_{REF\ SC}$	Short-circuit current to ground at $V_{REF\ OUT}$	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Maximum power dissipation, T_A=25°C (still-air)[1]		
	F package	1740	mW
	N package	2190	mW
	D package	1600	mW
T_A	Operating temperature range		
	SE5018	-55 to +125	°C
	NE5018	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature		
	(10 seconds)	300	°C

NOTES:

1. Derate above 25°C at the following rates:
   F package at 13.9mW/°C
   N package at 17.5mW/°C
   D package at 12.8mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{CC}+=+15V, V_{CC}-=-15V, SE5018. -55°C≤T_A≤125°C, NE5018. 0°C≤T_A≤70°C, unless otherwise specified. [1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SE5018			NE/SE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.19			±0.1	%FS
V_{CC}+	Positive supply voltage		11.4	15		11.4	15		V
V_{CC}-	Negative supply voltage		-11.4	-15		-11.4	-15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1=0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1=0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1=0V, 2V<V_{IN}<18V		0.1	10		0.1	10	µA
$I_{IN(0)}$	Logic "0" input current	Pin 1=0V, -5V<V_{IN}<0.8V		-2.0	-10		-2.0	-10	µA
V_{FS}	Full-scale output	Unipolar mode, V_{REF}=5.000V, all bits high, T_A=25°C	9.50		10.5	9.50		10.5	V
+V_{FS}	Full-scale output	Bipolar mode, V_{REF}=5.000V all bits high, T_A=25°C	4.75		5.25	4.75		5.25	V
-V_{FS}	Negative full scale	Bipolar mode, V_{REF}=5.000V, all bits low, T_A=25°C	-5.25		-4.75	-5.25		-4.75	V
V_{ZS}	Zero-scale Output	Unipolar mode, V_{REF}=5.000V all bits low, T_A=25°C	-30		+30	-30		+30	mV
I_{OS}	Output short circuit current	T_A=25°C V_{OUT}=0V		15	40		15	40	mA
$PSR+_{(OUT)}$	Output power supply rejection (+)	V-=-15V, 13.5V≤V+≤16.5V, external $V_{REF\ IN}$=5.000V		0.001	0.01		0.001	0.01	%FS %VS
$PSR-_{(OUT)}$	Output power supply rejection (-)	V+=-15V, -13.5V≤V-≤-16.5V, external $V_{REF\ IN}$=5.000V		0.001	0.01		0.001	0.01	%FS %VS
TC_{FS}	Full-scale temperature coefficient	$V_{REF\ IN}$=5.000V		20			20		ppm/°C
TC_{ZS}	Zero-scale temperature coefficient			5			5		ppm/°C
I_{REF}	Reference output current				3			3	mA
I_{REFSC}	Reference short circuit current	T_A=25°C $V_{REF\ OUT}$=0V		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	V-=-15V, 13.5V≤V+≤16.5V, I_{REF}=1.0mA		0.003	0.01		0.003	0.01	%VR/%VS
$PSR-_{(REF)}$	Reference power supply rejection (-)	V+=-15V, -13.5V≤V-≤16.5V,		0.003	0.01		0.003	0.01	%VR/%VS
V_{REF}	Reference voltage	I_{REF}=1.0mA T_A=25°C	4.9	5.0	5.25	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature co-efficient	I_{REF}=1.0mA		60			60		ppm/°C
Z_{IN}	DAC $V_{REF\ IN}$ input impedance	I_{REF}=1.0mA, T_A=25°C	4.15	5.0	5.85	4.15	5.0	5.85	kΩ
I_{CC}+	Positive supply current	V_{CC}+=15V		7	14		7	14	mA
I_{CC}-	Negative supply current	V_{CC}-=-15V		-10	-15		-10	-15	mA
P_D	Power dissipation	I_{REF}=1.0mA, V_{CC}=±15V		255	435		255	435	mW

NOTES:
1. Refer to Figure 1.

AC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = ±15V, T_A = 25°C

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	NE/SE5018/19			UNIT
					Min	Typ	Max	
t_{SLH}	Settling time	±1/2LSB	Input	All bits low-to-high[2]		1.8		µs
t_{SHL}	Settling time	±1/2LSB	Input	All bits high-to-low[3]		2.3		µs
t_{PLH}	Propagation delay	Output	Input	All bits switched low-to-high[2]		300		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched high-to-low[3]		150		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change[2, 3]		150		ns
t_{PLH}	Propagation delay	Output	LE	Low-to-high transition[4]		300		ns
t_{PHL}	Propagation delay	Output	LE	High-to-low transition[5]		150		ns
t_S	Setup time	LE	Input	1, 6	100			ns
t_H	Hold time	Input	LE	1, 6	50			ns
t_{PW}	Latch enable pulse width			1, 6	150			ns

NOTES:
1. Refer to Figure 2.
2. See Figure 5.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.
7. For reference currents>3mA, use of an external buffer is required.

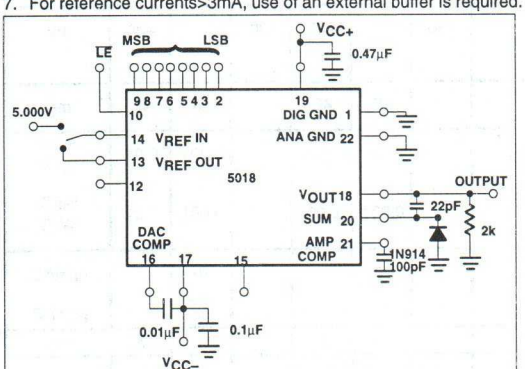


Figure 1. DC Parametric Test Configuration

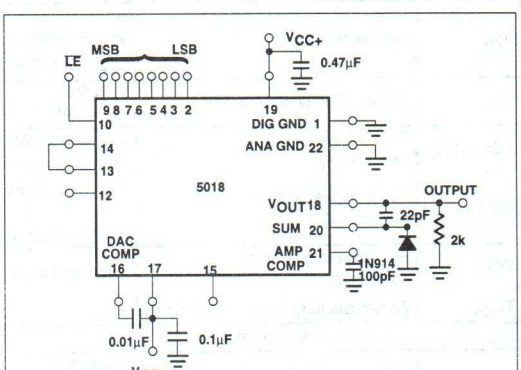


Figure 2. AC Parametric Test Configuration

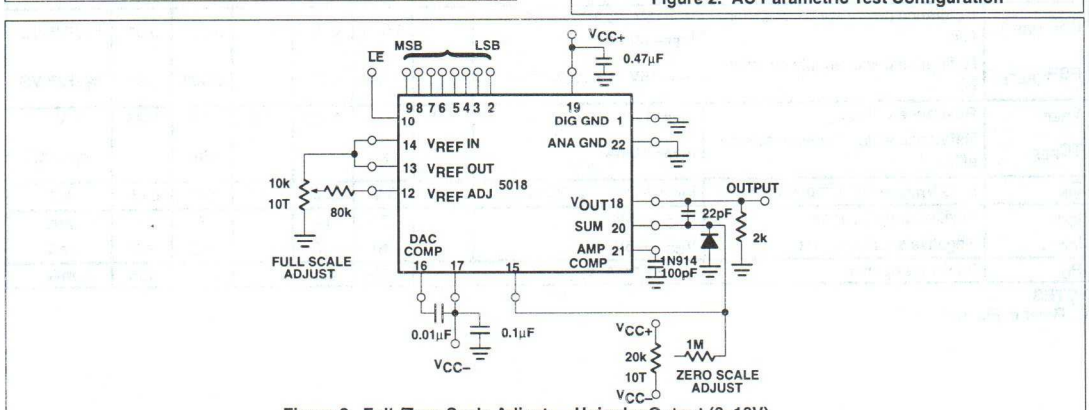


Figure 3. Full-/Zero-Scale Adjust — Unipolar Output (0–10V)

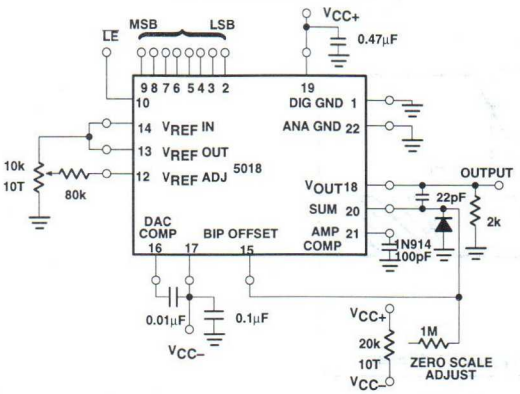


Figure 4. Bipolar Output Operation (–5 to +5V)

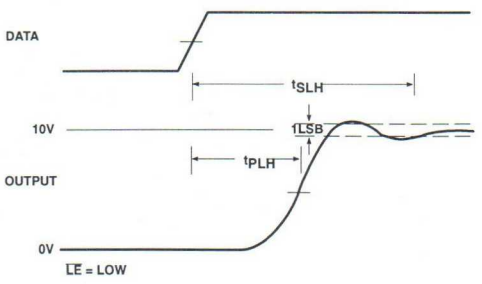


Figure 5. Settling Time and Propagation Delay, Low-to-High Data

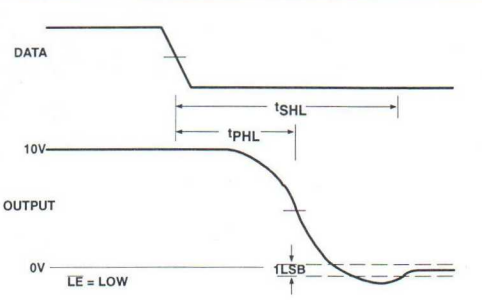


Figure 6. Settling Time and Propagation Delay, High-to-Low Data

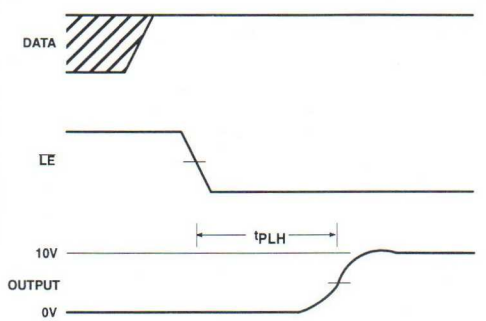


Figure 7. Propagation Delay, Latch Enable to Output

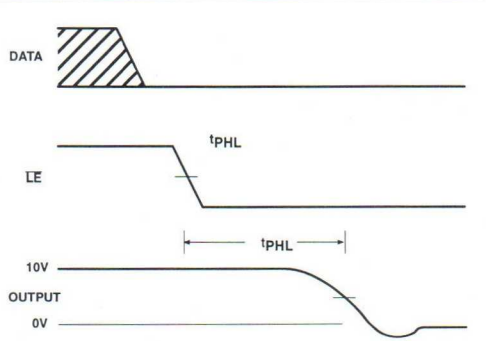


Figure 8. Propagation Delay, Latch Enable to Output

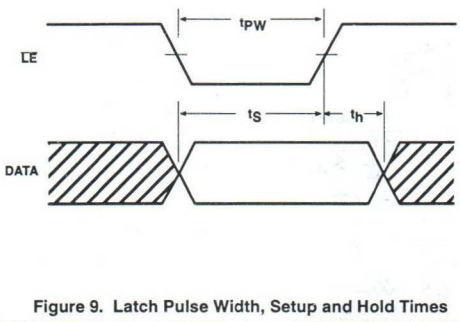


Figure 9. Latch Pulse Width, Setup and Hold Times

10-Bit μP-compatible D/A converter

NE5020

DESCRIPTION

The NE5020 is a microprocessor-compatible monolithic 10-bit digital-to-analog converter subsystem. This device offers 10-bit resolution and ±0.1% accuracy and monotonicity guaranteed over full operating temperature range.

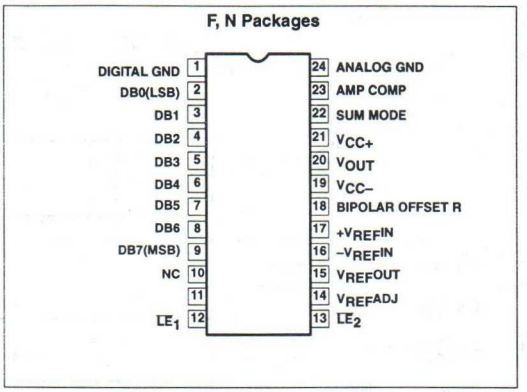
Low loading latches, adjustable logic thresholds, and addressing capability allow the NE5020 to directly interface with most microprocessor- and logic-controlled systems.

The NE5020 contains internal voltage reference, DAC switches and resistor ladder. Also, the input buffer and output summing amplifier are included. In addition, the matched application resistors for scaling either unipolar or bipolar output values are included on a single monolithic chip.

The result is a near minimum component count 10-bit resolution DAC system.

PIN CONFIGURATION

F, N Packages



FEATURES

- 10-bit resolution
- Guaranteed monotonicity over operating range
- ±0.1% relative accuracy
- Unipolar (0V to +10V) and bipolar (± 5V) output range
- Logic bus compatible
- 5μs settling time

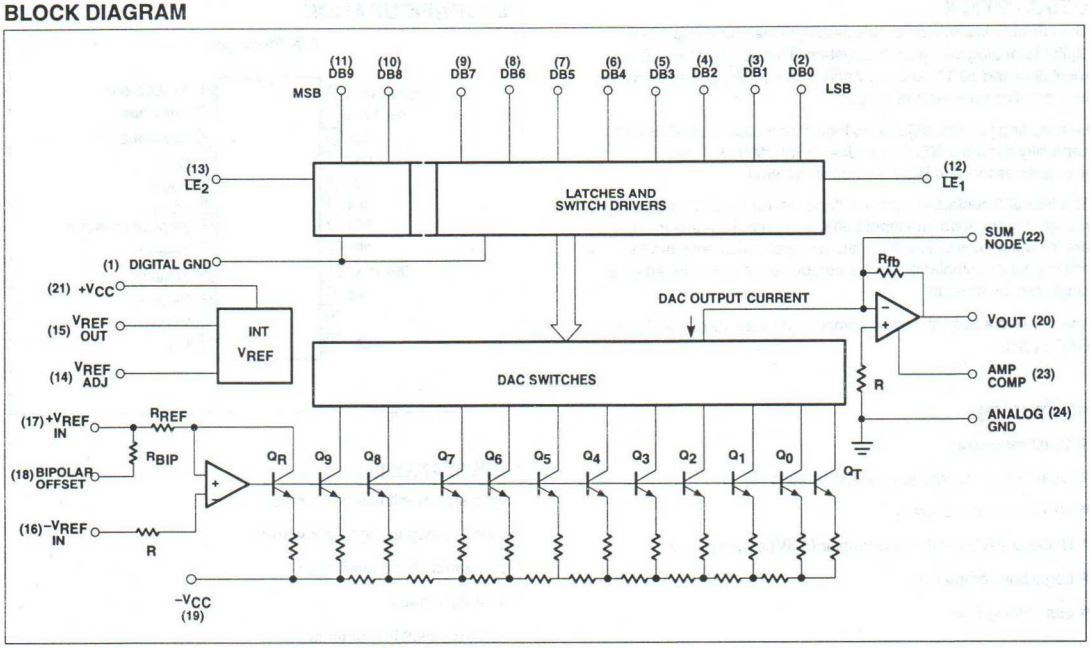
APPLICATIONS

- Precision 10-bit D/A converters
- 10-bit analog-to-digital converters
- Programmable power supplies
- Test equipment
- Measurement instruments

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Ceramic Dual In-Line Package (CERDIP)	0 to 70°C	NE5020F	0588B
24-Pin Plastic Dual In-Line Package (DIP)	0 to 70°C	NE5020N	0412A

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}^+	Positive supply voltage	18	V
V_{CC}^-	Negative supply voltage	-18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF\ IN}$	Voltage at $+V_{REF}$ input	12	V
$V_{REF\ ADJ}$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at $V_{REF\ OUT}$	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Maximum power dissipation T_A=25°C, (still-air)[1]		
	F package	2150	mW
	N package	2150	mW
T_A	Operating temperature range NE5020	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	300	°C

NOTES:
1. Derate above 25°C at the following rates:
   F package at 17.2mW/°C
   N package at 17.2mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{CC}+=+15V, V_{CC}-=-15V, 0 ≤ T_A≤70°C, unless otherwise specified.[1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution				10	Bits
	Monotonicity				10	Bits
	Relative accuracy				±0.1	%FS
V_{CC+}	Positive supply voltage		11.4	15	16.5	V
V_{CC-}	Negative supply voltage		-11.4	-15	-16.5	V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1=0V	2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1=0V			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1=0V, 2<V_{IN}<18V		0.1	10	µA
$I_{IN(0)}$	Logic "0" input current	Pin 1=0V, -5V<V_{IN}<0.8V		-2.0	-10	µA
V_{FS}	Full-scale output	Unipolar mode, V_{REF}=5.000V, all bits high, T_A=25°C	9.5		10.5	V
+V_{FS}	Full-scale output	Bipolar mode, V_{REF}=5.000V, all bits high, T_A=25°C	4.75		5.25	V
-V_{FS}	Negative full-scale	Bipolar mode, V_{REF}=5.000V, all bits low, T_A=25°C	-5.25		-4.75	V

NOTES:
1. Refer to Figure 1.

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{ZS}	Zero-scale output	Unipolar mode, V_{REF}=5.000V, all bits low, T_A=25°C	-30		+30	mV
I_{OS}	Output short-circuit current	T_A=25°C V_{OUT}=0V		±15	±40	mA
$PSR+_{(OUT)}$	Output power supply rejection (+)	V-=-15V, 13.5V≤V+≤16.5V, external $V_{REF\ IN}$=5.000V		0.001	0.01	%FS/%VS
$PSR-_{(OUT)}$	Output power supply rejection (-)	V+=15V, -13.5V≤V-≤-16.5V, external $V_{REF\ IN}$=5.000V		0.001	0.01	%FS/%VS
TC_{FS}	Full-scale temperature coefficient	$V_{REF\ IN}$=5.000V		20		ppmFS/°C
TC_{ZS}	Zero-scale temperature coefficient			5		ppmFS/°C
I_{REF}[2]	Reference output current				3	mA
$I_{REF\ SC}$	Reference short circuit current	T_A=25°C $V_{REF\ OUT}$=0V		15	30	mA
$PSR+_{REF}$	Reference power supply rejection (+)	V-=-15V, 13.5V≤V+≤16.5V, I_{REF}=1.0mA		.003	.01	%VR/%VS
$PSR-_{REF}$	Reference power supply rejection (-)	V+=15V, -13.5V≤V-≤16.5V,		.003	.01	%VR/%VS
V_{REF}	Reference voltage	I_{REF}=1.0mA, T_A=25°C	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	I_{REF}=1.0mA		60		ppm/°C
Z_{IN}	DAC $V_{REF\ IN}$ input impedance	I_{REF}=1.0mA		5.0		kΩ
$I_{CC}+$	Positive supply current	V_{CC}+=15V		7	14	mA
$I_{CC}-$	Negative supply current	V_{CC} -=-15V		-10	-15	mA
P_D	Power dissipation	I_{REF}=1.0mA, V_{CC}=±15V		255	435	mW

NOTES:
1. Refer to Figure 1.
2. For $I_{REF\ OUT}$ greater than 3mA, an external buffer is required.

AC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = +15V, T_A = 25°C.

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_{SLH}	Settling time	±1/2LSB	Input	All bits low-to-high[2]		5		µs
t_{SHL}	Settling time	±1/2LSB	Input	All bits high-to-low[3]		5		µs
t_{PLH}	Propagation delay	Output	Input	All bits switched low-to-high[2]		30		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched high-to-low[3]		150		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change[2,3]		150		ns
t_{PLH}	Propagation delay	Output	$\overline{CE}$	Low-to-high transition[4]		300		ns
t_{PHL}	Propagation delay	Output	$\overline{CE}$	High-to-low transition[5]		150		ns
t_S	Set-up time	$\overline{CE}$	Input	[1,6]	100			ns
t_H	Hold time	Input	$\overline{CE}$	[1,6]	50			ns
t_{PW}	Latch enable pulse width			[1,6]	150			ns

NOTES:
1. Refer to Figure 2.
2. See Figure 5.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.

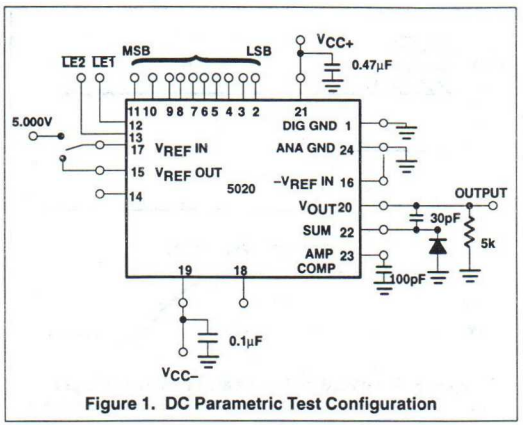


Figure 1. DC Parametric Test Configuration

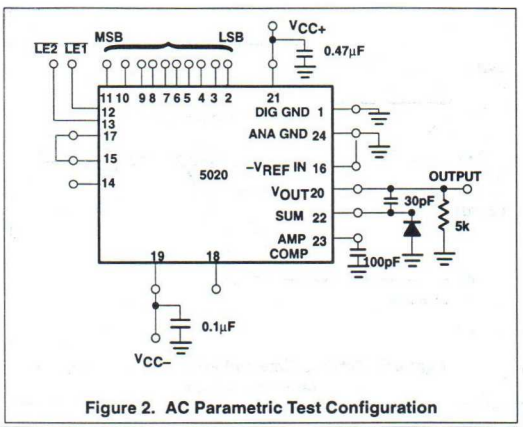


Figure 2. AC Parametric Test Configuration

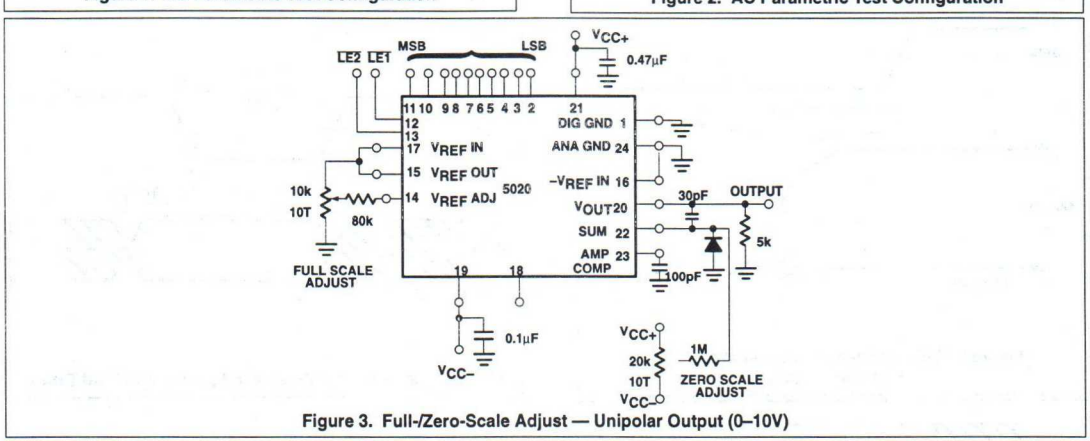


Figure 3. Full-/Zero-Scale Adjust — Unipolar Output (0–10V)

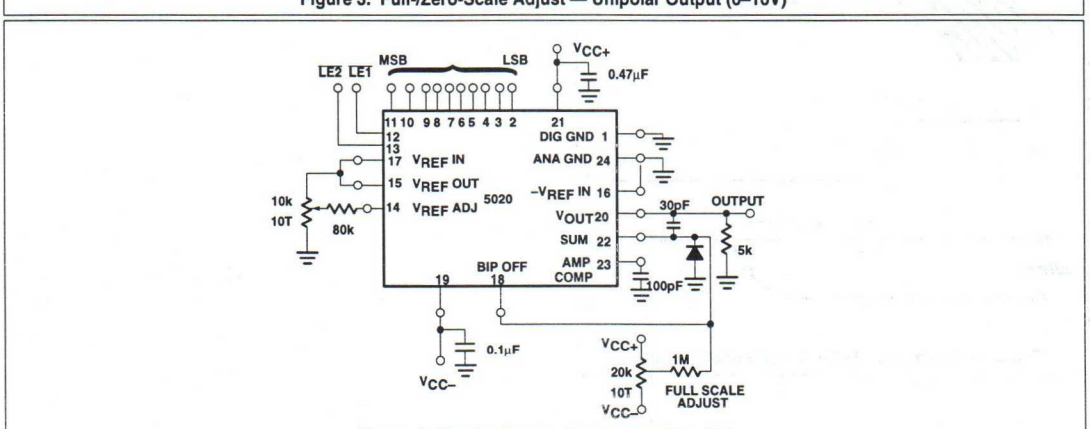


Figure 4. Bipolar Output Operation (–5 to +5V)

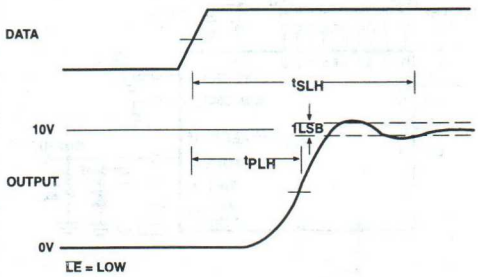


Figure 5. Settling Time and Propagation Delay, Low-to-High Data

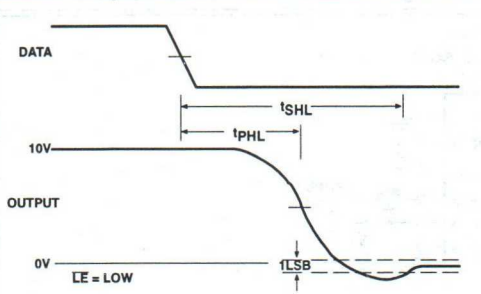


Figure 6. Settling Time and Propagation Delay, High-to-Low Data

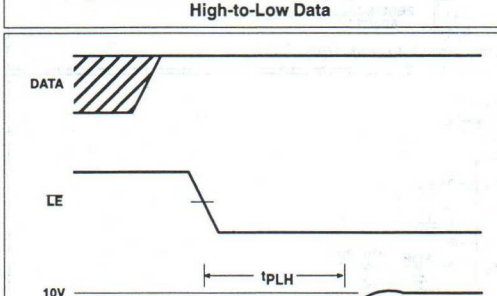


Figure 7. Propagation Delay, Latch Enable to Output

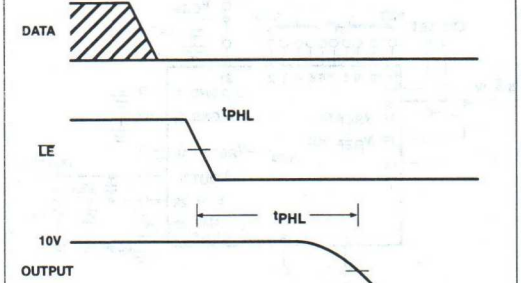


Figure 8. Propagation Delay, Latch Enable to Output

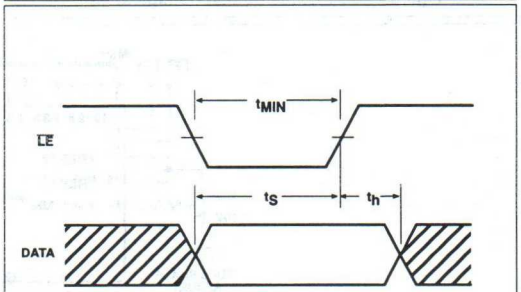


Figure 9. Latch Enable Pulse Width, Setup and Hold Times

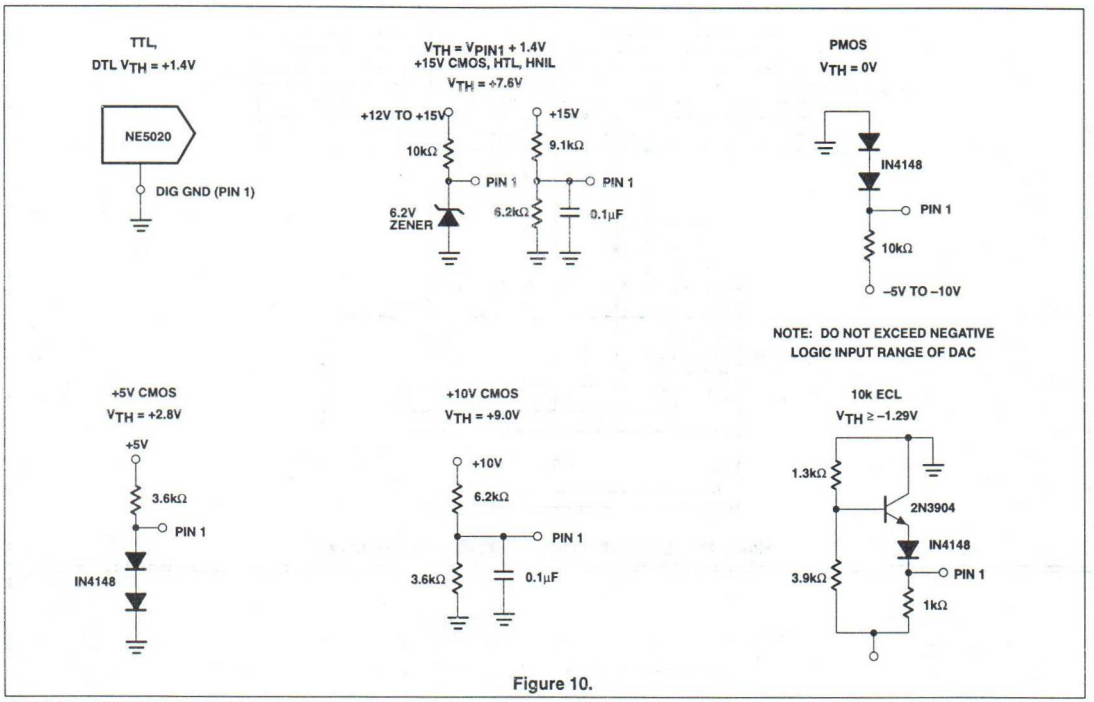


Figure 10.

CIRCUIT DESCRIPTION

The NE5020 provides ten data latches, an internal voltage reference, application resistors, and a scaled output voltage in addition to the basic DAC components (see Block Diagram).

Latch Circuit

Digital interface with the NE5020 is readily accomplished through the use of two latch enable ports ($\overline{LE}_1$ and $\overline{LE}_2$) and ten data input latches. $\overline{LE}_2$ controls the two most significant bits of data (DB9 and DB8) while $\overline{LE}_1$ controls the eight lesser significant bits (DB_7 through DB_0). Both the latch enable ports ($\overline{LE}$) and the data inputs are static- and threshold-sensitive. When the latch enable ports ($\overline{LE}$) are high (Logic '1') the data inputs become very high impedances and essentially disappear from the data bus. Addressing the $\overline{LE}$ with a low static (Logic '0'), the latches become active and adapt the logic states present on the data bus. During this state, the output of the DAC will change to the value proportional to the data bus value. When the latch enable returns to a high state, the selected set of data inputs (i.e., depending on which $\overline{LE}$ goes high) 'memorizes' the data bus logic states and the output changes to the unique output value corresponding to the binary word in the latch.

The data inputs are inactive and high impedance (typically requiring –2µA for low (0.8V max) or 0.1µA for high (2.0V min) when the $\overline{LE}$ is high. Any changes on the data bus with $\overline{LE}$ high will have no effect on the DAC output.

The digital logic inputs ($\overline{LE}$ and DB) for the NE5020 utilize a differential input logic system with a threshold level of +1.4V with respect to the voltage level on the digital ground pin (Pin 1). Figure 10 details several bias schemes used to provide the proper threshold voltage levels for various logic families.

To be compatible with a bus-oriented system, the DAC should respond in as short a period as possible to insure full utilization of the microprocessor, controller and I/O control lines. Figure 9 shows the typical timing requirements of the latch and data lines. This figure indicates that data on the data bus should be stable for at least 50ns after $\overline{LE}$ is changed to a high state.

The independent $\overline{LE}$ ($\overline{LE}_1$ and $\overline{LE}_2$) lines allow for direct interface from an 8-bit bus (see Figure 11). Data for the two MSBs is supplied and stored when $\overline{LE}_2$ is activated low and returned high according to the NE5020 timing requirements. Then $\overline{LE}_1$ is activated low and the remaining eight LSBs of data are transferred into the DAC. With $\overline{LE}_1$ returning high, the loading of 10-bit data word from an 8-bit data bus is complete.

Occasionally the analog output must change to its data value within one data address operation. This is no problem using the NE5020 on a 16-bit bus or any other data bus with 10 or greater data bits.

This can be accomplished from an 8-bit data bus by utilizing an external latch circuit to pre-load the two MSB data values. Figure 12 shows the circuit configuration.

After pre-loading (via $\overline{LE}$ pre-load) the external latch with the two MSB values, $\overline{LE}_2$ is activated low and the eight LSBs and the two MSBs are concurrently loaded into the DAC in one address operation. This permits the DAC output to make its appropriate change at one time.

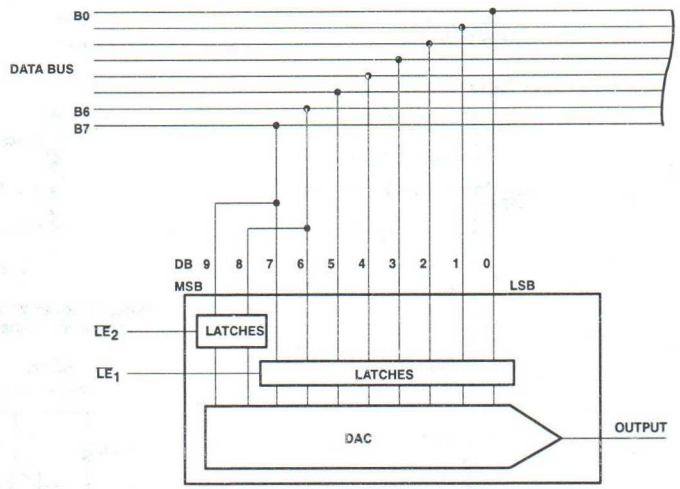


Figure 11. NE5020 μP Interface 8-Bit Data Bus Example

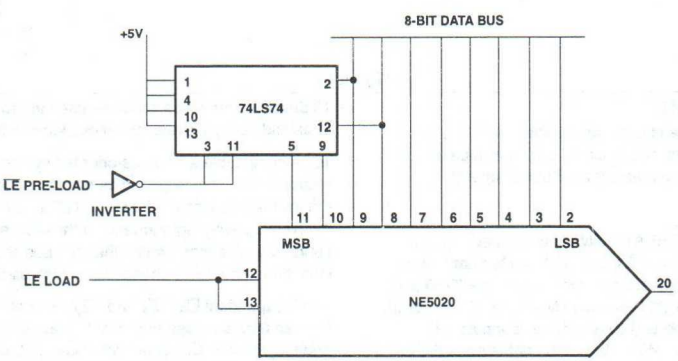


Figure 12. Pre-loading the 2 MSBs to Provide a Single-Step Output

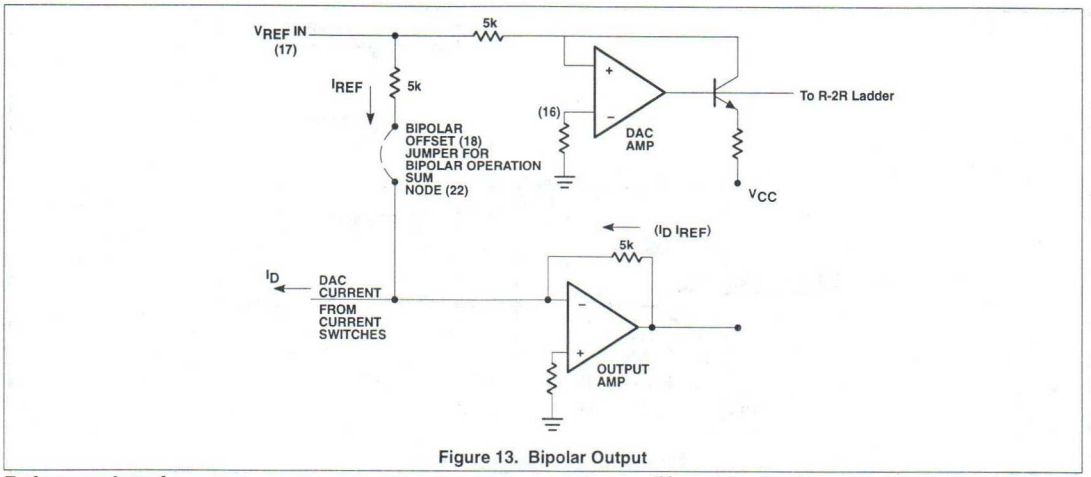


Figure 13. Bipolar Output

Reference Interface

The NE5020 contains an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long-term stability characteristics.

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5V reference output. Providing a $V_{REF\ ADJ}$ (Pin 14) allows trimming of the reference output. Utilization of the adjust circuit shown in Figure 15 performs not only V_{REF} adjustment, but also full-scale output adjust. Notice that the $V_{REF\ ADJ}$ pin is essentially the sum node of an op amp and is sensitive to excessive node capacitance. Any capacitance on the node can be minimized by placing the external resistors as close as possible to the $V_{REF\ ADJ}$ pin and observing good layout

practices.

The $V_{REF\ OUT}$ node can drive loads greater than the DAC V_{REF} input requirements and can be used as an excellent system voltage reference. However, to minimize load effects on the DAC system accuracy, it is recommended that a buffer amplifier be used.

Input Amplifier

The DAC reference amplifier is a high gain internally-compensated op amp used to convert the input reference voltage to a precision bias current for the DAC ladder network.

The Block Diagram details the input reference amplifier and current ladder. The voltage-to-current converter of the DAC amp will generate a 1mA reference current through QR with a 5V V_{REF}. This current sets the input bias to the ladder network. Data bit 9 (DB9)(Q9), when turned on, will mirror this current and will contribute 1mA to the output. DB8 (Q8) will contribute 1/2 of that value or 0.5mA, and so on. These current values act as current sinks and will add at the sum node to produce a DAC ladder to sum node function of:

$$I_{OUT} = \frac{2V_{REF}}{R_{REF}}\left(\frac{DB9}{2} + \frac{DB8}{4} + \frac{DB7}{8} + \frac{DB6}{16} + \frac{DB5}{32} + \frac{DB4}{64} + \frac{DB3}{128} + \frac{DB2}{256} + \frac{DB1}{512} + \frac{DB0}{1024}\right)$$

Because of the fixed internal compensation of the reference amp, the slew rate is limited to typically 0.7V/μs and source impedance at the $V_{REF\ INPUT}$ greater than 5kΩ should be avoided to maintain stability.

The $-V_{REF\ INPUT}$ pin is uncommitted to allow utilization of negative polarity reference voltages. In this mode $+V_{REF\ INPUT}$ is grounded and the negative reference is tied directly to the $-V_{REF\ INPUT}$ contains a 5kΩ resistor that matches a like resistor in the $+V_{REF\ INPUT}$ to reduce voltage offset caused by op amp input bias currents.

Output Amplifier and Interface

The NE5020 provides an on-chip output op amp to eliminate the need for additional external active circuits. Its two-stage design with feed-forward compensation allows it to slew at 15V/μs and settle to within ±1/2LSB in 5μs. These times are typical when driving the rated loads of $R_L \geq 5k$ and C_L 50pF with recommended values of C_{FF} = 1nF and C_{FB} = 30pF. Typical input offset voltages of 5mV and 50kΩ open-loop gain insure that an accurate current-to-voltage conversion is performed when using the on-chip R_{FB} resistor. R_{FB} is matched to R_{REF} and R_{BIP} to maintain accurate voltage gain over operating conditions. The diode shown from ground to sum node prevents the DAC current switches from saturating the op amp during large signal transitions which would otherwise increase the settling time.

The output op amp also incorporates output short circuit protection for both positive and negative excursions. During this fault condition I_{OUT} will limit at ±15mA typical. Recovery from this condition to rated accuracy will be determined by duration of short-circuit and die temperature stabilization.

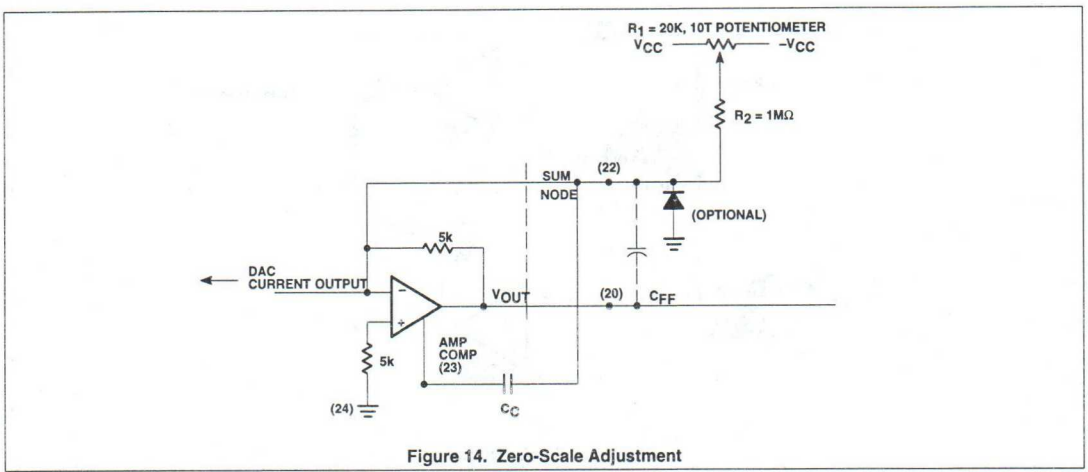


Figure 14. Zero-Scale Adjustment

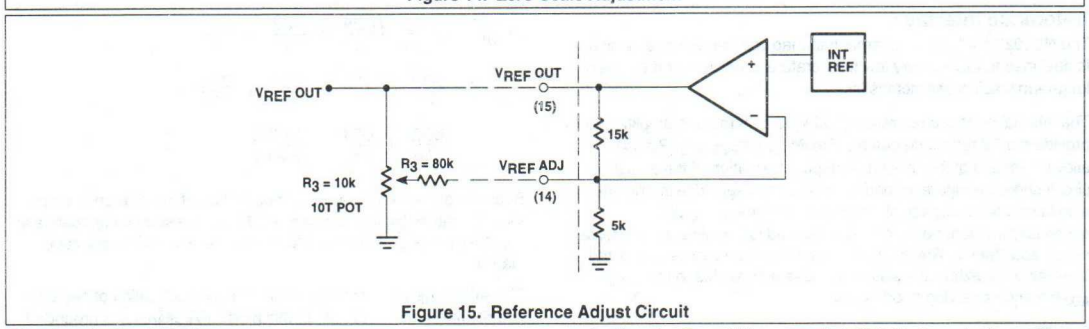


Figure 15. Reference Adjust Circuit

Bipolar Output Voltage

The NE5020 includes a thermally matched resistor, R_{BIP}, to offset the output voltage by 5V to obtain –5V to +5V output voltage range operation. This is accomplished by shorting Pins 18 and 22 (see Figure 13). This connection produces a current equal to (V_{REFIN} – $_{SUM\ NODE}$) ÷ R_{BIP} (1mA nominal), which is injected into the sum node. Since full-scale current out is approximately 2mA (1.9980mA), (2mA – 1mA)5kΩ = 5V will appear at the output. For zero DAC output currents, 1mA is still injected into sum node and V_{OUT} = –(5kΩ) (1mA) = –5V. Zero-scale adjust and full-scale adjust are performed as described below, noting that full-scale voltage is now approximately +5V. Zero-scale adjust may be used to trim V_{OUT} = 0.00 with the MSB high or V_{OUT} = –5.0V with all bits off.

Zero-Scale Adjustment

The method of trimming the small offset error that may exist when all data bits are low is
shown in Figure 14. The trim is the result of injecting a current from resistor R_2 that counteracts the error current. Adjusting potentiometer R_1 until V_{OUT} equals 0.000V in the unipolar mode or –5.000V in the bipolar mode (see bipolar section accomplishes this trim.

Full-Scale Adjustment

A recommended full-scale adjustment circuit, when using the internal voltage reference, is shown in Figure 15. Potentiometer R_3 is adjusted until V_{OUT} equals 9.99023V. In many applications where the absolute accuracy of full-scale is of low importance when compared to the other system accuracy factors this adjustment circuit is optional.

As resistors R_{REF}, R_{FB}, and R_{BIP} shown in the Block Diagram are integrated in close proximity, they match and track in value closely over wide ambient temperature variations. Typical matching is less than ±0.3% which implies that typical full-scale (or gain) error is less than ±0.3% of ideal full-scale value.

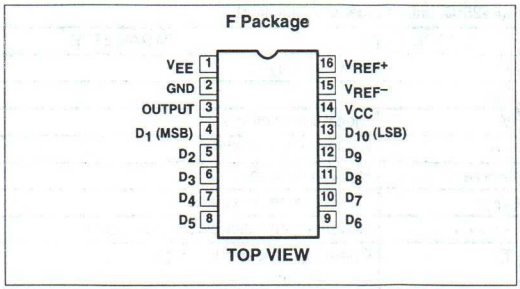
10-Bit high-speed multiplying D/A converter NE/SE5410

DESCRIPTION

The NE5410/SE5410 are 10-bit Multiplying Digital-to-Analog Converters pin- and function-compatible with the industry-standard MC3410, but with improved performance. These are capable of high-speed performance, and are used as general-purpose building blocks in cost effective D/A systems.

The NE/SE5410 provides complete 10-bit accuracy and differential non-linearity over temperature, and a wide compliance voltage range. Segmented current sources, in conjunction with an R/2R DAC, provide the binary weighted currents. The output buffer amplifier and voltage reference have been omitted to allow greater speed, lower cost, and maximum user flexibility.

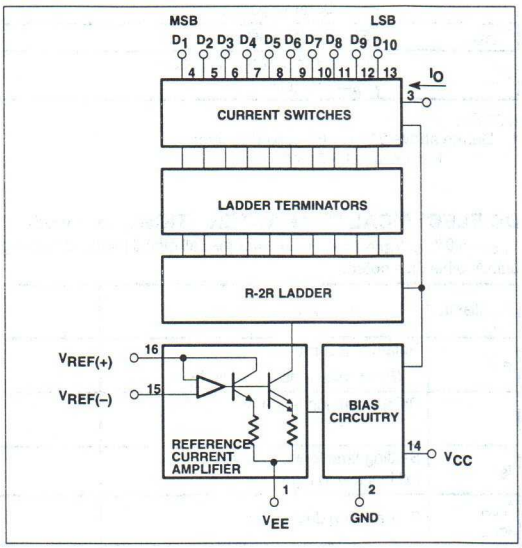
PIN CONFIGURATION



FEATURES

- Pin- and function-compatible with MC3410
- 10-bit resolution and accuracy (±0.05%)
- Guaranteed differential non-linearity over temperature
- Wide compliance voltage range—2.5 to +2.5V
- Fast settling time—250ns typical
- Digital inputs are TTL- and CMOS-compatible
- High-speed multiplying input slew rate—20mA/μs
- Reference amplifier internally-compensated
- Standard supply voltages +5V and -15V

BLOCK DIAGRAM



APPLICATIONS

- Successive approximation A/D converters
- High-speed, automatic test equipment
- High-speed modems
- Waveform generators
- CRT displays
- Strip CHART and X-Y plotters
- Programmable power supplies
- Programmable gain and attenuation

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE5410F	0582B
16-Pin Ceramic Dual In-Line Package (CERDIP)	-55 to +125°C	SE5410F	0582B

ABSOLUTE MAXIMUM RATINGS

T_A=+25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	+7.0	V_{DC}
V_{EE}		-18	V_{DC}
V_I	Digital input voltage	+15	V_{DC}
V_O	Applied output voltage	+4, -5.0	V_{DC}
$I_{REF(16)}$	Reference current	2.5	mA
V_{REF}	Reference amplifier inputs	V_{CC}, V_{EE}	V_{DC}
$V_{REF(D)}$	Reference amplifier differential inputs	0.7	V_{DC}
T_A	Operating temperature range SE5410 NE5410	 -55 to +125 0 to +70	 °C °C
T_J	Junction temperature Ceramic package	 +150	 °C
T_{STG}	Storage temperature	-65 to +150	°C
P_D	Maximum power dissipation T_A=25°C (still-air)[1]	1190	mW

NOTES:
1. Derate above 25°C at the following rate:
   F package at 9.5mW/°C

DC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC}=+5.0V_{DC}, V_{EE}=-15V_{DC}, I_{REF}=2.0mA, all digital inputs at high logic level. SE5410: T_A=-55°C to +125°C, NE5410 Series: T_A=0°C to +70°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
ϵ_R	Relative accuracy (Error relative to full scale I_O)	Over Temperature		±0.025 ±1/4	±0.05 ±1/2	% LSB
	Differential non-linearity	Over temperature		±0.025 ±1/4	±0.05 ±1/2	% LSB
t_S	Settling time to within ±1/2 LSB (all bits low to high)	T_A = 25°C		250		ns
t_{PLH} t_{PHL}	Propagation delay time	T_A = 25°C		35 20		ns
TCI_O	Output full-scale current drift			20	40	ppm/°C
V_{IH}	Digital input logic levels (all bits) High level, Logic "1" Low level, Logic "0"		 2.0		 0.8	V_{DC}
I_{IH} I_{IL}	Digital input current (all bits) High level, V_{IH} = 5.5V Low level, V_{IL} = 0.8V				20 −20	µA
$I_{REF(15)}$	Reference input bias current (Pin 15)			−1.0	−5.0	µA
I_{OH}	Output current (all bits high)	V_{REF} = 2.000V, R16 = 1000Ω	3.937	3.996	4.054	mA
I_{OL}	Output currents (all bits low)	T_A = 25°C		0	0.4	µA
V_O	Output voltage compliance	T_A = 25°C ϵ_R < 0.050% relative to full-scale			−2.5 +2.5	V_{DC}
SR I_{REF}	Reference amplifier slew rate			20		mA/µs
ST I_{REF}	Reference amplifier settling time	0 to 4.0mA, ±0.1%		2.0		µs
PSRR(−)	Output current power supply sensitivity			0.003	0.01	%/%
C_O	Output capacitance	V_O = 0		25		pF

DC ELECTRICAL CHARACTERISTICS

V_{CC}=+5.0V_{DC}, V_{EE}=-15V_{DC}, I_{REF}=2.0mA, all digital inputs at high logic level. SE5410: T_A=-55°C to +125°C, NE5410 Series: T_A=0°C to +70°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
C_I	Digital input capacitance (all bits high)			4.0		pF
I_{CC} I_{EE}	Power supply current (all bits low)			+2 −12	+4 −18	mA
V_{CC} V_{EE}	Power supply voltage range	T_A = 25°C V_O = 0	+4.75 −14.25	+5.0 −15	+5.25 −15.75	V_{DC}
	Power consumption			190	300	mW

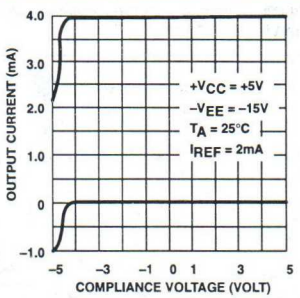


Figure 1. Output Current vs Output Compliance Voltage

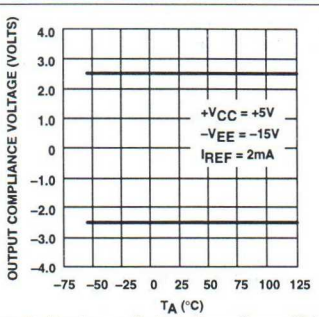


Figure 2. Maximum Output Compliance Voltage vs Temperature

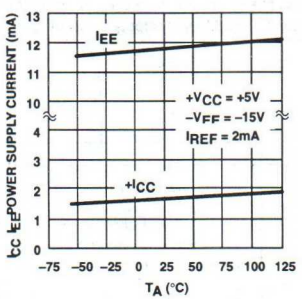


Figure 3. Power Supply Currents vs Temperature

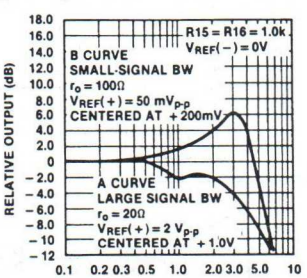


Figure 4. Reference Amplifier Frequency Response

CIRCUIT DESCRIPTION

The NE5410 consists of four segment current sources which generate the 2 Most Significant Bits (MSBs), and an R/2R DAC implemented with ion-implanted resistors for scaling the remaining 8 Least Significant Bits (LSBs) (see Figure 5). This approach provides complete 10-bit accuracy without trimming.

The individual bit currents are switched ON or OFF by fully-differential current switches. The switches use current steering for speed.

An on-chip high slew reference current amplifier drives the R/2R ladder and segment decoder. The currents are scaled in such a way that, with all bits on, the maximum output current is two times 1023/1024 of the reference amplifier current, or nominally 3.996mA for a 2.000mA reference input current. The reference amplifier allows the user to provide a voltage input: out-board resistor R16 (see Figure 6) converts this voltage to a usable current. A current mirror doubles this reference current and feeds it to the segment decoder and resistor ladder. Thus, for a reference voltage of 2.0V and a 1kΩ resistor tied to Pin 16, the full-scale current is

approximately 4.0mA. This relationship will remain regardless of the reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6a. For negative reference voltage inputs, or for bipolar reference voltage inputs in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. For a negative reference input, R16 should be grounded (Figure 6b). In addition, the negative voltage reference must be at least 3V above the V_{EE} supply voltage for best operation. Bipolar input signals may be handled by connecting R16 to a positive voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic, is to be used as the reference, R16 should be decoupled by connecting it to the +5.0V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1µF capacitor to ground.

The reference amplifier is internally-compensated with a 10pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R16 and reference voltages which supply 2.0mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0mA. As R16 increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R16=1.0kΩ, and settling time is ±10µs. The reference amplifier phase margin decreases as the current source value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5mA for stability.

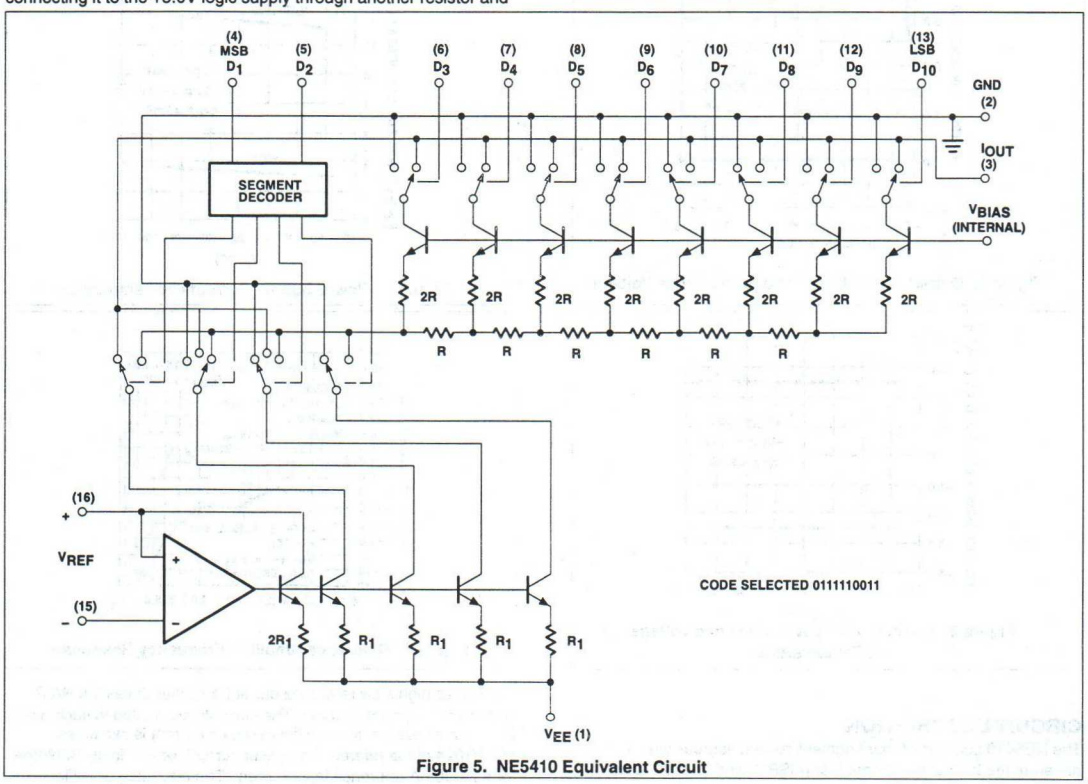


Figure 5. NE5410 Equivalent Circuit

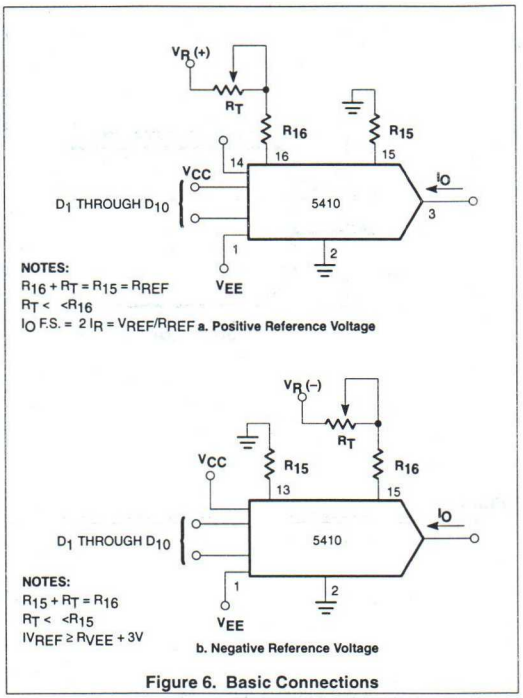


Figure 6. Basic Connections

OUTPUT VOLTAGE COMPLIANCE

The output voltage compliance ranges from -2.5 to +2.5V. As shown in Figure 2, this compliance range is nearly constant over temperature. At the temperature extremes, however, the compliance voltage may be reduced if V_{EE}>-15V.

ACCURACY

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full-scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full-scale current. The relative accuracy of the NE5410 is fairly constant over temperature due to the excellent temperature tracking, of the implanted resistors. The full-scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the NE5410 has a low full-scale current drift with temperature.

The SE5410 and the NE5410 are accurate to within ± LSB at 25°C with a reference current of 2.0mA on Pin 16.

MONOTONICITY

The NE5410 and SE5410 are guaranteed monotonic over temperature. This means that for every increase in the input digital code, the output current either remains the same or increases but never decreases. In the multiplying mode, where reference input current will vary, monotonicity can be assured if the reference input current remains above 0.5mA.

SETTLING TIME

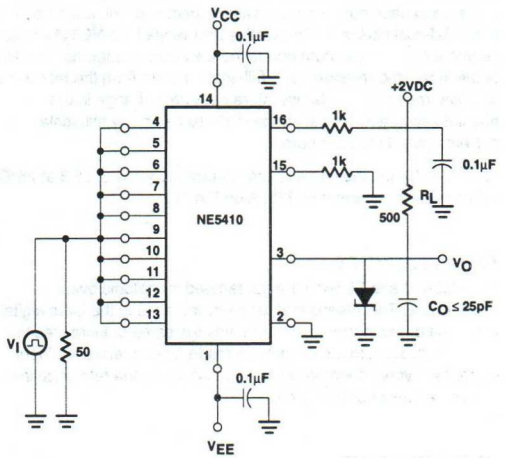
The worst-case switching condition occurs when all bits are switched "on," which corresponds to a LOW-to-HIGH transition for all bits. This time is typically 250ns for the output to settle to within ± 1/2LSB for 10-bit accuracy, and 200ns for 8-bit accuracy. The turn-off time is typically 120ns. These times apply when the output swing is limited to a small (<0.7V) swing and the external output capacitance is under 25pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

If a load resistor of 625Ω is connected to ground, allowing the output to swing to -2.5V, the settling time increases to 1.5μs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing, and minimum scope lead length are all necessary.

A typical test setup for measuring settling time is shown in Figure 7. The same setup for the most part can be used to measure the slew rate of the reference amplifier (Figure 9) by tying all data bits high, pulsing the voltage reference input between 0 and 2V, and using a 500Ω load resistor R_L.



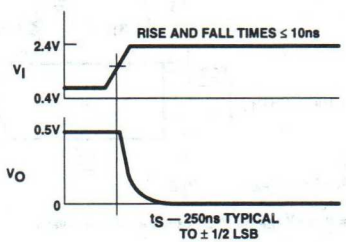
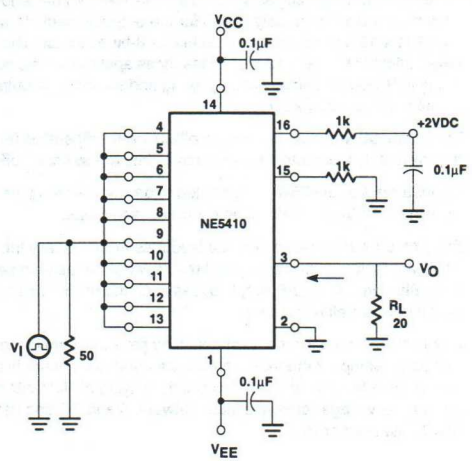


Figure 7. Settling Time



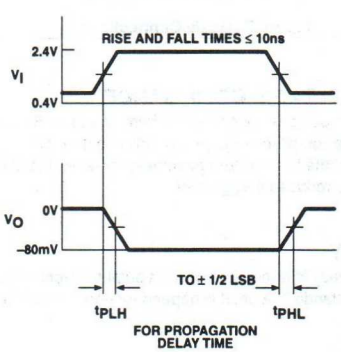


Figure 8. Propagation Delay Time

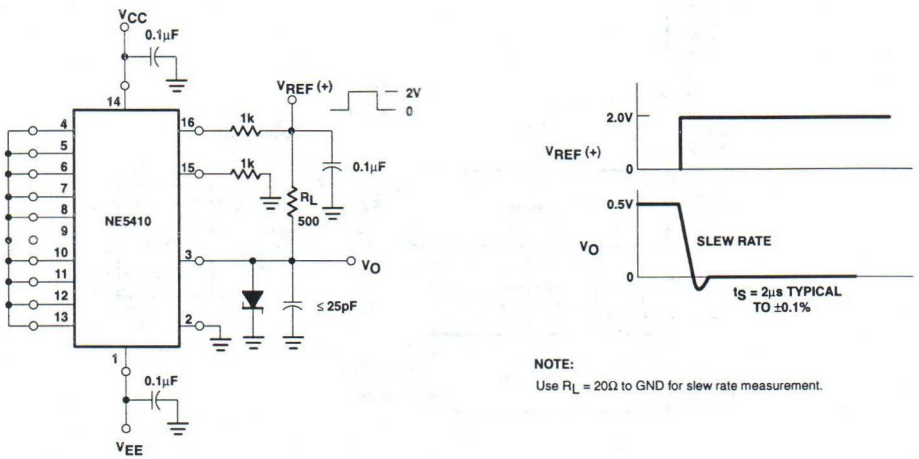


Figure 9. Reference Amplifier Settling Time and Slew Rate

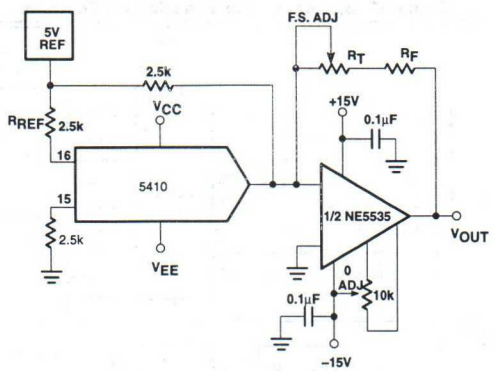
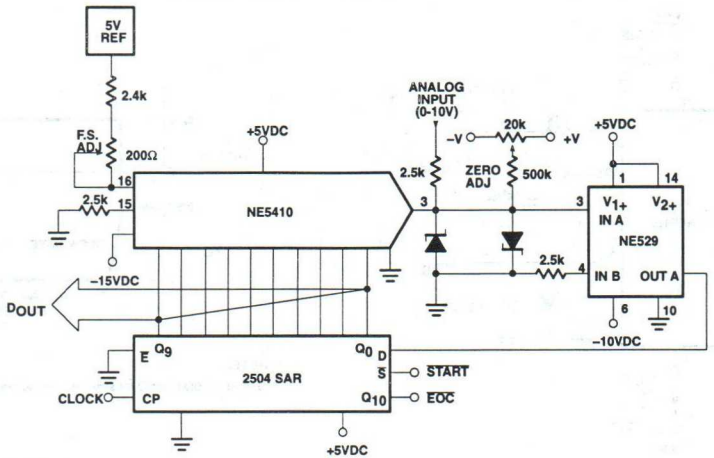
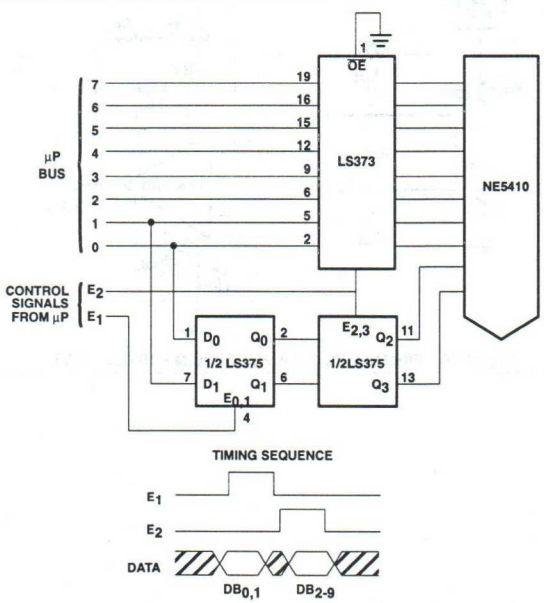


Figure 10. Bipolar Voltage Output Circuits (-10V to +10V)



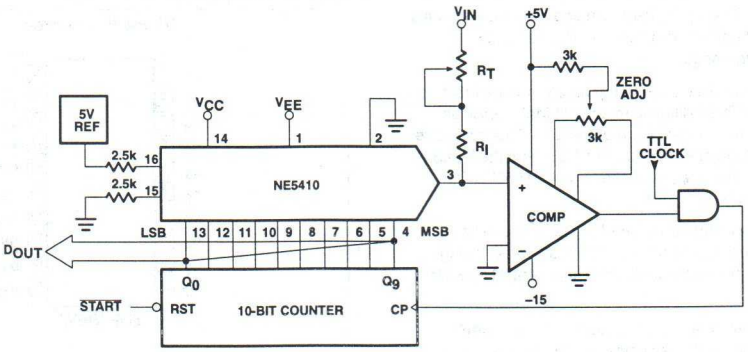
NOTES:
10-bit conversion time = 3.3μs with 3MHz clock.
This converter uses a 2504 12-bit successive approximation register in the short cycle operating mode where the end of conversion signal is taken from the first unused bit of the SAR (Q_{10}).

Figure 11. Successive Approximation A/D Converter



NOTES:
With this double latch technique, valid data will be latched to the DAC until updated with the E_2 pulse. Timing will depend on the processor used.

Figure 12. 8-Bit μP Bus Interface



NOTE:

V_{IN} FULL SCALE = 4mA $(R_1 + R_T)\left(\frac{1023}{1024}\right)$

Figure 13. Staircase A/D

12-Bit multiplying D/A converter — AM6012

DESCRIPTION

The AM6012 12-bit multiplying Digital-to-Analog converter provides high-speed and 0.025% differential nonlinearity over its full commercial temperature range.

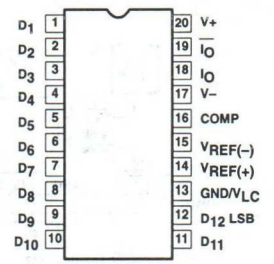
The D/A converter uses a 3-bit segment generator for the MSBs in conjunction with a 9-bit R-2R diffused resistor ladder to provide 12-bit resolution without costly trimming processes. This technique guarantees a very uniform step size (up to ± LSB from the ideal), monotonicity to 12 bits and integral nonlinearity to 0.05% at its differential current outputs.

The dual complementary outputs of the AM6012 increase its versatility, and effectively double the peak-to-peak output swing. Digital inputs, in addition, can be configured to accept all popular logic families.

While the device requires a reference input of 1mA for a 4mA full-scale current, operation is nearly independent of power supply voltage shifts. The power supply rejection ratio is ±0.001% FS/% ΔV. The devices will work from +5, -12V to ±18V rails, with as low as 230mW power consumption typical.

PIN CONFIGURATION

D[1] and F Packages



TOP VIEW

NOTE:
1. Available in large SO (SOL) package only.

FEATURES

- 12-bit resolution
- Accurate to within ±0.05%
- Monotonic over temperature
- Fast settling time, 250ns typical
- Trimless design for low cost
- Differential current outputs
- High-speed multiplying capability
- Full-scale current, 4mA (with 1mA reference)
- High output compliance voltage, -5 to +10V
- Low power consumption, 230mW

APPLICATIONS

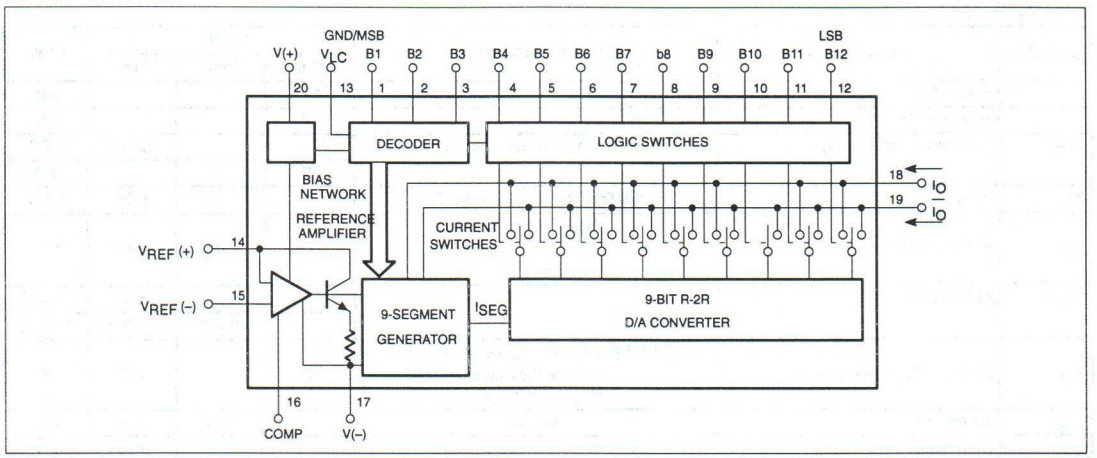
- CRT displays, computer graphics
- Robotics and machine tools
- Automatic test equipment
- Programmable power supplies
- CAD/CAM systems
- Data acquisition and control systems
- Analog-to-digital converter systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	AM6012F	0584B
20-Pin Plastic Small Outline Large (SOL) Package	0 to +70°C	AM6012D	0172D

12-Bit multiplying D/A converter | AM6012

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating temperature		
	AM6012F	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature 10sec max	300	°C
V_S	Power supply voltage	±18	V
	Logic inputs	-5V to +18	V
	Voltage across current outputs	-8V to +12	V
V_{REF}	Reference inputs V_{14}, V_{15}	V- to V+	
V_{REF}	Reference input differential voltage (V_{14} to V_{15})	±18	V
I_{REF}	Reference input current (I_{14})	1.25	mA
P_D	Maximum power dissipation, T_A=25°C, (still-air)[1]		
	F package	1560	mW
	D package	1390	mW

NOTES:
1. Derate above 25°C, at the following rate:
   F package at 12.5mW/°C
   D package at 11.1mW/°C

DC ELECTRICAL CHARACTERISTICS

V+=+15V, V-=-15V, I_{REF}=1.0mA, 0°C ≤ T_A ≤ 70°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution		12			Bits
	Monotonicity		12			Bits
DNL	Differential nonlinearity	Deviation from ideal step size			±0.025	%FS
			12			Bits
NL	Nonlinearity	Deviation from ideal straight line			±.05	%FS
I_{FS}	Full-scale current	V_{REF}=10.000V R_{14}-R_{15}=10.000kΩ T_A=25°C	3.935	3.999	4.063	mA
TCI_{FS}	Full-scale tempco			±10	±40	ppm/°C
				±0.001	±0.004	%FS/°C
V_{OC}	Output voltage compliance	DNL Specification guaranteed over compliance range R_{OUT}>10MΩ typ.	-5		+10	V
I_{FSS}	Symmetry	I_{FS}-$I_{\overline{FS}}$		±0.4	±2.0	µA
I_{ZS}	Zero-scale current				0.10	µA
V_{IL} V_{IH}	Logic input levels — Logic "0"				0.8	V
	Logic input levels — Logic "1"		2.0			
I_{IN}	Logic input current	V_{IN}=-5 to +18V			40	µA
V_{IS}	Logic input swing	V-=-15V	-5		+18	V
I_{REF}	Reference current range		0.2	1.0	1.1	mA
I_{15}	Reference bias current		0	-0.5	-2.0	µA
dI/dt	Reference input slew rate	$R_{14(eq)}$=800Ω C_C=0pF	4.0	8.0		mA/µs
$PSSI_{FS+}$	Power supply sensitivity	V+=+13.5V to +16.5V, V-=-15V		±0.0005	±0.001	%FS/%
$PSSI_{FS-}$		V-=-13.5V to -16.5V, V+=+15V		±0.00025	±0.001	
V+	Power supply range	V_{OUT}=0V	4.5		18	V
V-			-18		-10.8	
I+	Power supply current	V+=+5V, V-=-15V		5.7	8.5	mA
I-				-13.7	-18.0	
I+		V+=+15V, V-=-15V		5.7	8.5	
I-				-13.7	-18.0	
P_D	Power dissipation	V+=+5V, V-=-15V		234	312	mW
		V+=+15V, V-=-15V		291	397	

AC ELECTRICAL CHARACTERISTICS

V+=+15V, V-=-15V, I_{REF}=1.0mA, 0°C ≤ T_A ≤ 70°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_S	Settling time	To ± 1/2LSB, all bits ON or OFF, T_A=25°C		250	500	ns
t_{PLH} t_{PHL}	Propagation delay—all bits	50% to 50%		25	50	ns
C_{OUT}	Output capacitance			20		pF

CIRCUIT DESCRIPTION

The AM6012 is a 12-bit DAC which uses diffused resistors and requires no trimming to guarantee monotonicity over the temperature range. A segmented DAC design guarantees a more uniform step size over the temperature range than is normally available with trimmed 12-bit converters. The converter features differential high compliance current outputs, wide supply range, and a multiplying reference input.

In many converter applications, uniform step size is more important than conformance to an ideal straight line. Many 12-bit converters are used for high resolution rather than high linearity, since few transducers are more linear than ±0.1%. All classic binarily weighted converters require ±1/2LSB (±0.012%) linearity in order to guarantee monotonicity, which requires very tight resistor matching and tracking. The AM6012 uses conventional bipolar processing to achieve high differential linearity and monotonicity without requiring correspondingly high linearity, or conformance to an ideal straight line.

One design approach which provides monotonicity without requiring high linearity is the MOS switch-resistor string. This circuit is actually a full complement to a current-switched R-2R DAC since it is slower, has a voltage output, and, if implemented at the 12-bit level, would use 4096 low tolerance resistors rather than a minimum number of high tolerance resistors as in the R-2R network. Its lack of speed and density for 12 bits are its drawbacks.

With the segmented DAC approach, the 4096 required output levels are composed of 8 groups of 512 steps each. Each step group is generated by a 9-bit DAC, and each of the segment slopes is determined by one of 8 equal current sources. The resistors which determine monotonicity are in the 9-bit DAC. The major carry of the 9-bit DAC is repeated in each of the 8 segments, and requires eight times lower initial resistor accuracy and tracking to maintain a given differential nonlinearity over temperature.

The operation of the segmented DAC may be visualized by assuming an input code of all zeroes. The first segment current I_O is divided into 512 levels by the 9-bit multiplying DAC and fed to the output, I_{OUT}. As the input code increases, a new segment current is selected for each 512 counts. The previous segment is fed to output I_{OUT} where the new step group is added to it, thus ensuring monotonicity independent of segment resistor values. All higher order segments feed $\overline{I_{OUT}}$.

With the segmented DAC approach, the precision of the 8 main resistors determines linearity only. The influence of each of these resistors on linearity is four times lower than that of the MSB resistor in an R-2R DAC. Hence, assuming the same resistor tolerances for both, the linearity of the segmented approach would actually be higher than that of an R-2R design.

The step generator or 9-bit DAC is composed of a master and a slave ladder. The slave ladder generates the four least significant bits from the remainder of the master ladder by active current splitting utilizing scaled emitters. This saves ladder resistors and greatly reduces the range of emitter scaling required in the 9-bit DAC. All current switches in the step generator are high-speed fully-differential switches which are capable of switching low currents at high speed. This allows the use of a binary scaled network all the way to the least significant bit which saves power and simplifies the circuitry.

Diffused resistors have advantages over thin film resistors beyond simple economy and bipolar process compatibility. The resistors are fabricated in single crystal rather than amorphous material which gives them better long term stability and tracking and much higher moisture resistance. They are diffused at 1000°C and so are resistant to changes in value due to thermal and chemical causes. Also, no burn-in is required for stability. The contact resistance between aluminum and silicon is more predictable than between aluminum and an amorphous thin film, and no sandwich metals are required to enhance or protect the contact or limit alloying. The initial match between two diffused resistors is similar to that of thin film since both are defined by photomasks and chemical etching. Since the resistors are not trimmed or altered after fabrication, their tracking and long-term characteristics are not degraded.

DIFFERENTIAL VS INTEGRAL NONLINEARITY

Integral nonlinearity, for the purposes of the discussion, refers to the "straightness" of the line drawn through the individual response points of a data converter. Differential nonlinearity, on the other hand, refers to the deviation of the spacing of the adjacent points from a 1 LSB ideal spacing. Both may be expressed as either a percentage of full-scale output or as fractional LSBs or both. The graphs in Figure 1 define the manner in which these parameters are specified. The left graph shows a portion of the transfer curve of a DAC with 1/2LSB INL and the (implied) DNL spec of 1 LSB. Below this is a graphic representation of the way this would appear on a CRT screen where the AM6012 is used as a display driver. On the right is a portion of the transfer curve of a DAC specified for 1/2LSB INL with LSB DNL specified and the graphic display below it.

One of the characteristics of an R-2R DAC in standard form is that any transition which causes a zero LSB change (i.e., the same output for two different codes) will exhibit the same output each time that transition occurs. The same holds true for transitions causing a 2 LSB change. These two problem transitions are allowable for the standard definition of monotonicity and also allow the device to be specified very tightly for INL. The major problem arising from this error type is in A/D converter implementations. Inputs producing the same output are now represented by ambiguous output codes for an identical input. Also, two LSB gaps can cause large errors at those input levels (assuming 1/2LSB quantizing levels). It can be seen from the two figures that the DNL-specified D/A converter will yield much finer grained data than the INL-specified part, thus improving the ability of the A/D to resolve changes in the analog input.

DIFFERENTIAL LINEARITY COMPARISON

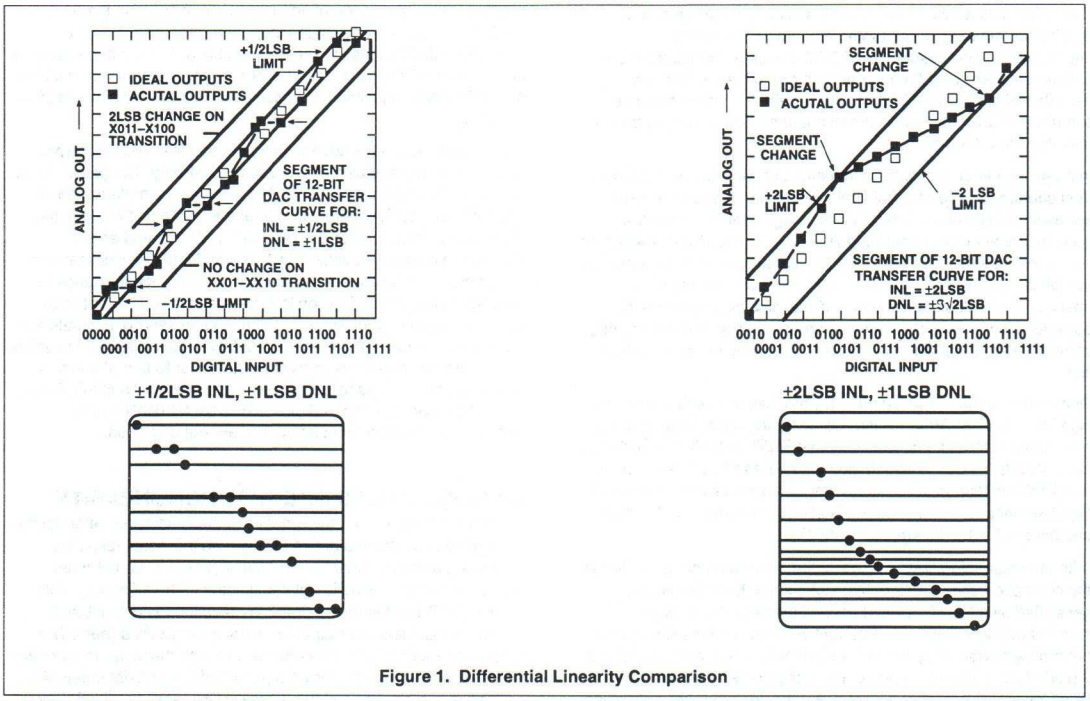


Figure 1. Differential Linearity Comparison

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O+\overline{I}_O=I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at Pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at Pin 18 and turned on at Pin 19. A decreasing logic count increases $\overline{I}_O$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required, it must still be connected to ground or to a point capable of sourcing I_{FR}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25V above V- and is independent of the positive supply. Negative compliance is +10V above V-.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The AM6012 operates over a wide range of power supply voltages from a total supply of 20V to 36V. When operating with V- supplies of -10V or less, $I_{REF}\leq 1$mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at -9V with $I_{REF}=1$mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the AM6012 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc., remain between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the AM6012 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically ±10ppm/°C, with zero-scale output current and drift essentially negligible compared to 1/2LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full-scale drift.

SETTLING TIME

The AM6012 is capable of extremely fast settling times, typically 250ns at $I_{REF}=1.0$mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during

testing and application. The logic switch design enables propagation delays of only 25ns for each of the 12 bits. Settling time to within LSB of the LSB is therefore 25ns, with each progressively larger bit taking successively longer. The MSB settles in 250ns, thus determining the overall settling time of 250ns. Settling to 10-bit accuracy requires about 90 to 130ns. The output capacitance of the AM6012 including the package is approximately 20pF; therefore, the output RC time constant dominates settling time if R_L>500Ω.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±2μA, therefore a 2.5kΩ load is needed to provide adequate drive for most oscilloscopes. At I_{REF} values of less than 0.5mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 011111111111 to 100000000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.1% of the final value, and thus settling times may be observed at lower values of I_{REF}.

AM6012 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

APPLICATIONS INFORMATION

Reference Amplifier Setup

The AM6012 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{4095}{4096} \times 4 \times (I_{REF}) = 3.999\ I_{REF}$$

where $I_{REF} = I_{14}$

In positive reference applications, an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (Pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at Pin 15. Reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at Pin 15. The voltage at Pin 14 is equal to and tracks the voltage at Pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors (Figure 2a).

Bipolar references may be accommodated by offsetting V_{REF} or Pin 15. The negative common-mode range of the reference amplifier is given by: V_{CM}-=V- plus (I_{REF}×3kΩ) plus 1.8V. The positive common-mode range is V+ less 1.23V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications, the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}.

MULTIPLYING OPERATION

The AM6012 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 1.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V-. The value of this capacitor depends on the impedance presented to Pin 14. For R14 values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 5, 12 and 25pF. Larger values of R14 require proportionately increased values of CC for proper phase margin (see Figure 2b).

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If Pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14}=1kΩ and C_C=5pF, the reference amplifier slews at 4mA/ms enabling a transition from I_{REF}=0 to I_{REF}=1mA in 250ns.

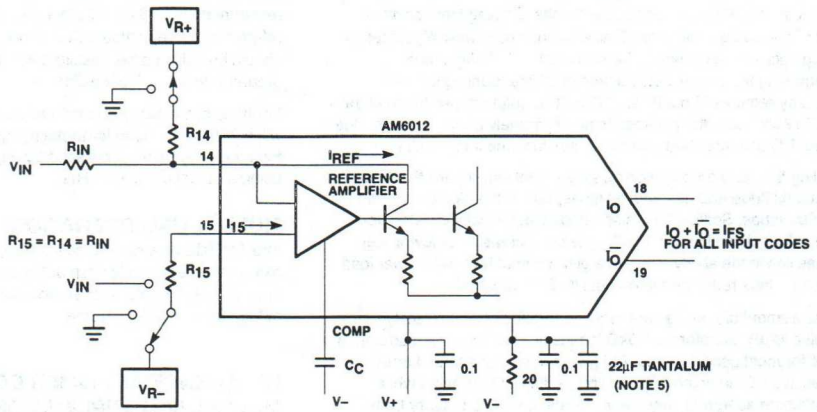
Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF}=0) condition. Full-scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at Pin 14 is 800Ω and C_C=0. This yields a reference slew rate of 8mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The AM6012 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 40μA logic input current, and completely adjustable logic threshold voltage. For V-=-15V, the logic inputs may swing between -5 and +10V. This enables direct interface with +15V CMOS logic, even when the AM6012 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by:

V- plus (I_{REF}×3kΩ) plus 1.8V.

The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (Pin 13, V_{LC}). For TTL interface, simply ground Pin 13. When interfacing ECL, an I_{REF}≤1mA is recommended. For general setup of the logic control circuit, it should be noted that Pin 13 will sink 1.1mA typical. External circuitry should be designed to accommodate this current (Figure 3).



REFERENCE CONFIGURATION	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive reference	V_{R+}	0V	N/C	0.01µF	V_{R+}/R_{14}
Negative reference	0V	V_{R-}	N/C	0.01µF	$-V_{R-}/R_{14}$
Lo impedance bipolar reference	V_{R+}	0V	V_{IN}[1]		$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})^2$
Hi impedance bipolar reference	V_{R+}	V_{IN}	N/C[1]		$(V_{R+} - R_{IN}) / R_{14}$[3]
Pulsed reference[4]	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$

NOTES:

1. The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and must be at least 5pF x $R_{14(eq)}$ in kΩ. For R_{14} < 800Ω no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+} / R_{14} must be greater than $-V_{IN}$ max / R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than $-V_{IN}$ max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at Pin 14 should be 800Ω or less.
5. For optimum settling time, decouple V– with 20Ω and bypass with 22µF tantalum capacitor.
6. Reference current and reference resistor — there is a 1-to-4 scale factor between the reference current (I_{REF}) and the full-scale output current (IFS). If V_{REF} = +10V and I_{FS} = 4mA, the value of the R_{14} is:

$$R_{14} = \frac{4 \times 10V}{4mA} = 10k\Omega \qquad R_{14} = R_{15}$$

a. Reference Amplifier Biasing

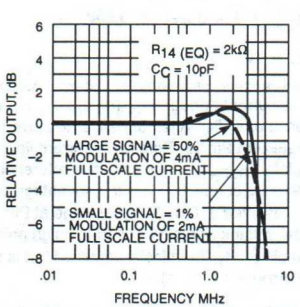
Minimum Size Compensation Capacitor

(I_{FS} = 4mA, I_{REF} = 1.0mA)

$R_{14(EQ)}$ (kΩ)	C_C (pF)
10	50
5	25
2	10
1	5
.5	0

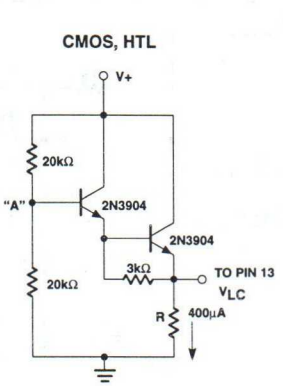
NOTE:
A 0.01µF capacitor is recommended for fixed reference operation.

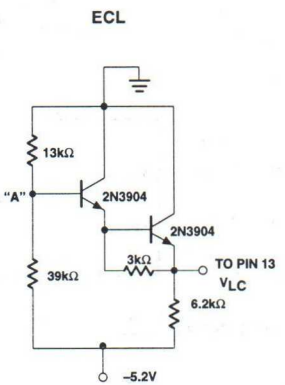
Reference Amplifier Frequency Response



b.

Figure 2.

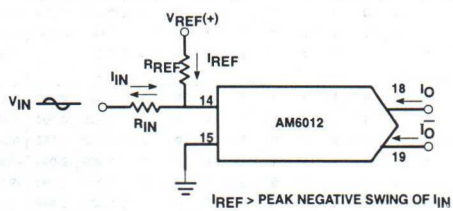




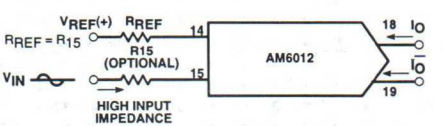
NOTE:
1. Set the voltage 'A' to the desired logic input switching threshold.
2. Allowable range of logic threshold is typically –5V to +13.5V when operating the DAC on ±15V supplies.

Figure 3. Interfacing Circuits for ECL, CMOS, HTL Logic Inputs

ACCOMMODATING BIPOLAR REFERENCE

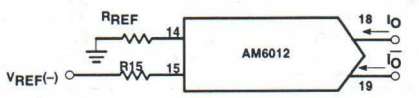


NOTE:
I_{REF} > Peak negative swing of I_{IN}.



NOTE:
$V_{REF(+)}$ Must be above peak positive swing of V_{IN}.

BASIC NEGATIVE REFERENCE OPERATION

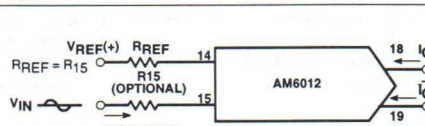


NOTE:

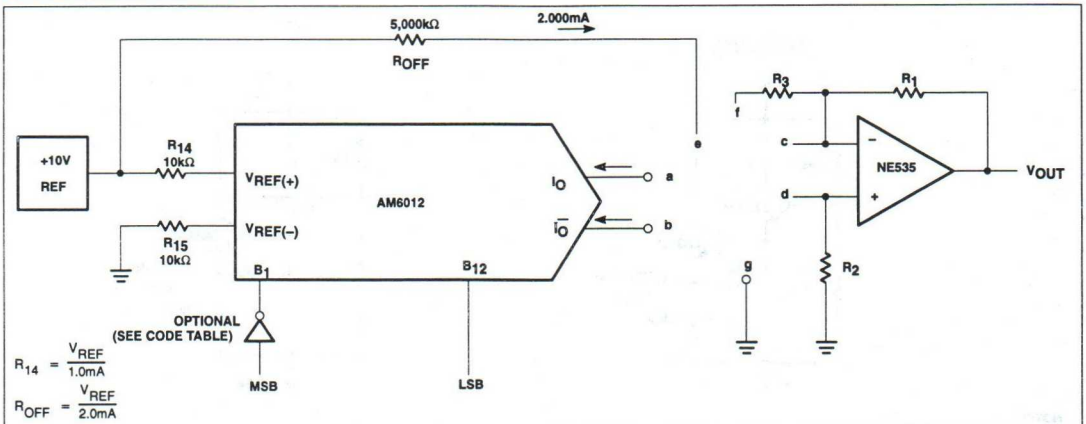
$$I_{FS} \approx \frac{V_{REF(-)}}{R_{REF}} \times 4$$

R_{REF} sets I_{FS}; R15 is for a bias current cancellation.

RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT



APPLICATION CIRCUITS



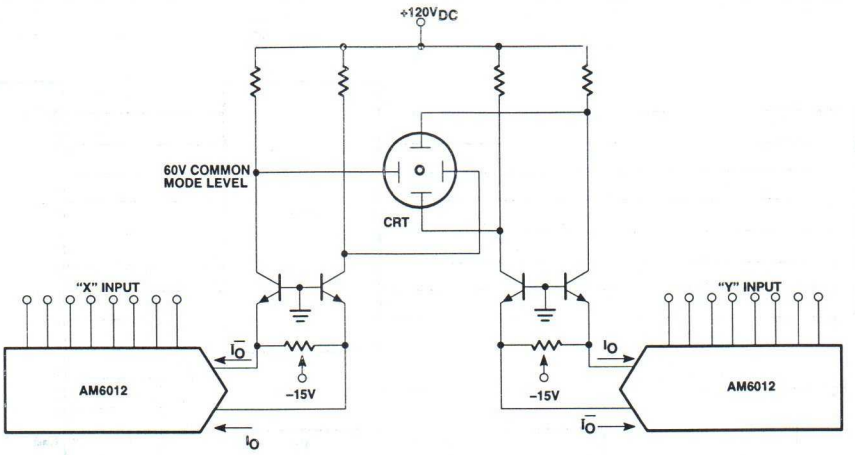
CODE FORMAT		CONNECTIONS	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
Unipolar	Straight binary; one polarity with true input code, true zero output.	a – c	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
		b – g	Positive full-scale – LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9951
		R1 = R2 = 2.5k	Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	0.0000
	Complementary binary; one polarity with complementary input code, true zero output.	a – g	Positive full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	9.9976
		b – c	Positive full-scale – LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	9.9951
		R1 = R2 = 2.5k	Zero-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	0.0000
Symmetrical Offset	Straight offset binary; offset half-scale, symmetrical about zero, no true zero output.	a – c	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
		b – d	Positive full-scale – LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
		f – g	(+) Zero-scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
		R1 = R3 = 2.5k	(–) Zero-scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.0024
		R2 = 1.25k	Negative full-scale – LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9927
			Negative full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–9.9976
	1's complement; offset half-scale, symmetrical about zero, no true zero output, MSB complemented (need inverter at B1).	a – c	Positive full-scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
		b – d	Positive full-scale – LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
		f – g	(+) Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
		R1 = R3 = 2.5k	(–) Zero-scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.0024
		R2 = 1.25k	Negative full-scale – LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9927
			Negative full-scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–9.9976
Offset with True Zero	Offset binary; offset half-scale, true zero output.	e – a – c	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
		b – g	Positive full-scale – LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
		R1 = R2 = 5k	+ LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
			Zero-scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
			– LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.0049
			Negative full-scale + LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9951
			Negative full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–10.000
	2's complement; offset half-scale, true zero output, MSB complemented (need inverter at B1).	e – a – c	Positive full-scale	0	1	1	1	1	1	1	1	1	1	1	1			
		b – g	Positive full-scale – LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
		R1 = R2 = 5k	+ 1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
			Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
			– 1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.049
			Negative full-scale + LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9951
			Negative full-scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–10.000

Figure 4. AM6012 Logic Inputs

ADDITIONAL CODE MODIFICATIONS

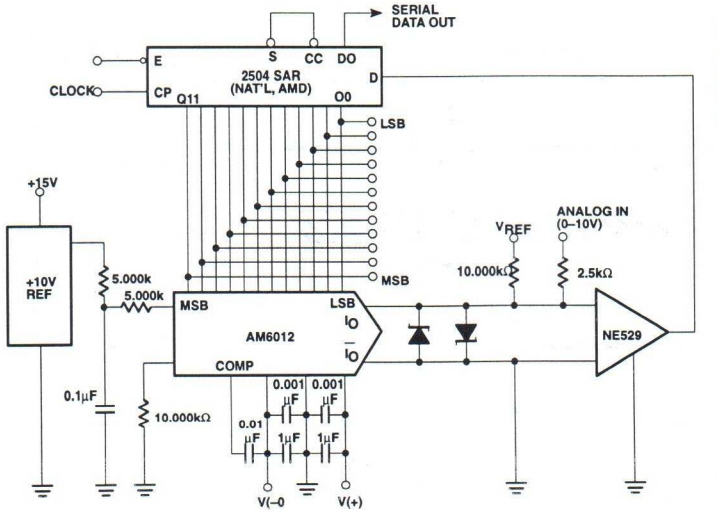
1. Any of the offset binary codes may be complemented by reversing the output terminal pair.

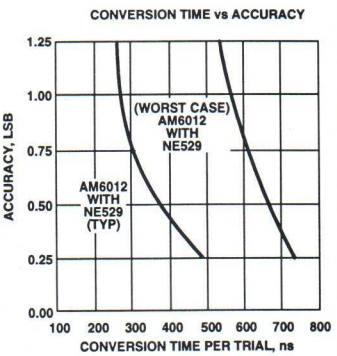
APPLICATION CIRCUITS



NOTES:
1. Full differential drive lowers power supply voltage.
2. Eliminates inverting amplifiers and transformers.
3. Independent beam centering controls.

Figure 5. CRT Display Driver

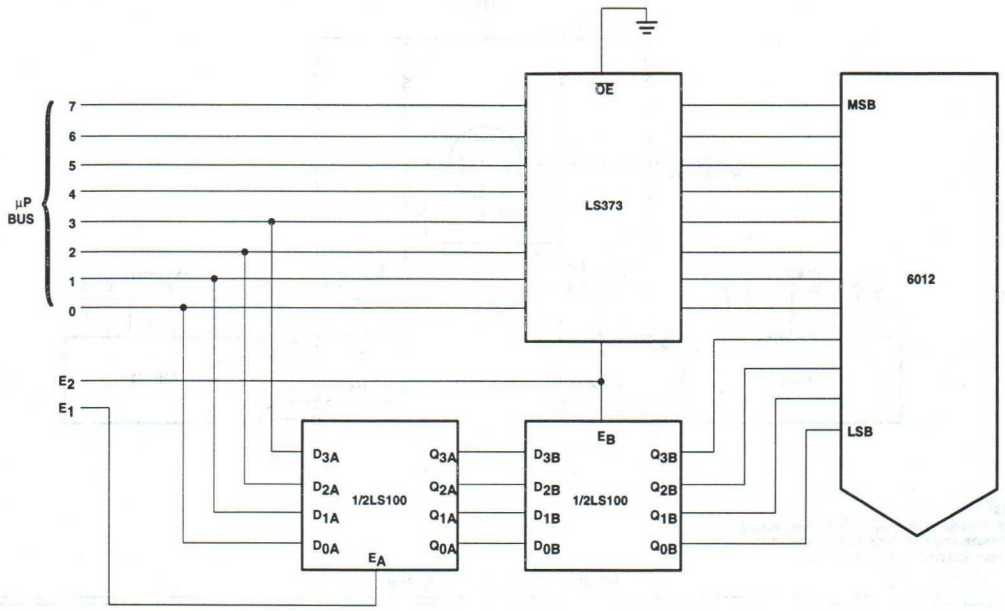




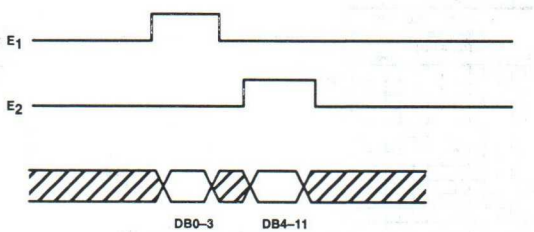
CONVERSION TIME (ns)	TYP	WORST CASE
SAR	33	55
NE529	100	150
TOTAL	383ns	705ns
X 13	5.0μs	9.1μs

Figure 6. 12-Bit High-Speed A/D Converter

APPLICATION CIRCUITS



a. Interface With 8-Bit Microprocessor Bus



a. Timing Sequence

NOTE:
Data remains on inputs of DAC until updated by E2 pulse. Timing will depend on processor used.

Figure 7.

Stereo high-performance 16-bit DAC — TDA1541A

FEATURES

- High sound quality
- High performance: low noise and distortion, wide dynamic range
- 4 x or 8 x oversampling possible
- Selectable two-channel input format
- TTL compatible inputs

GENERAL DESCRIPTION

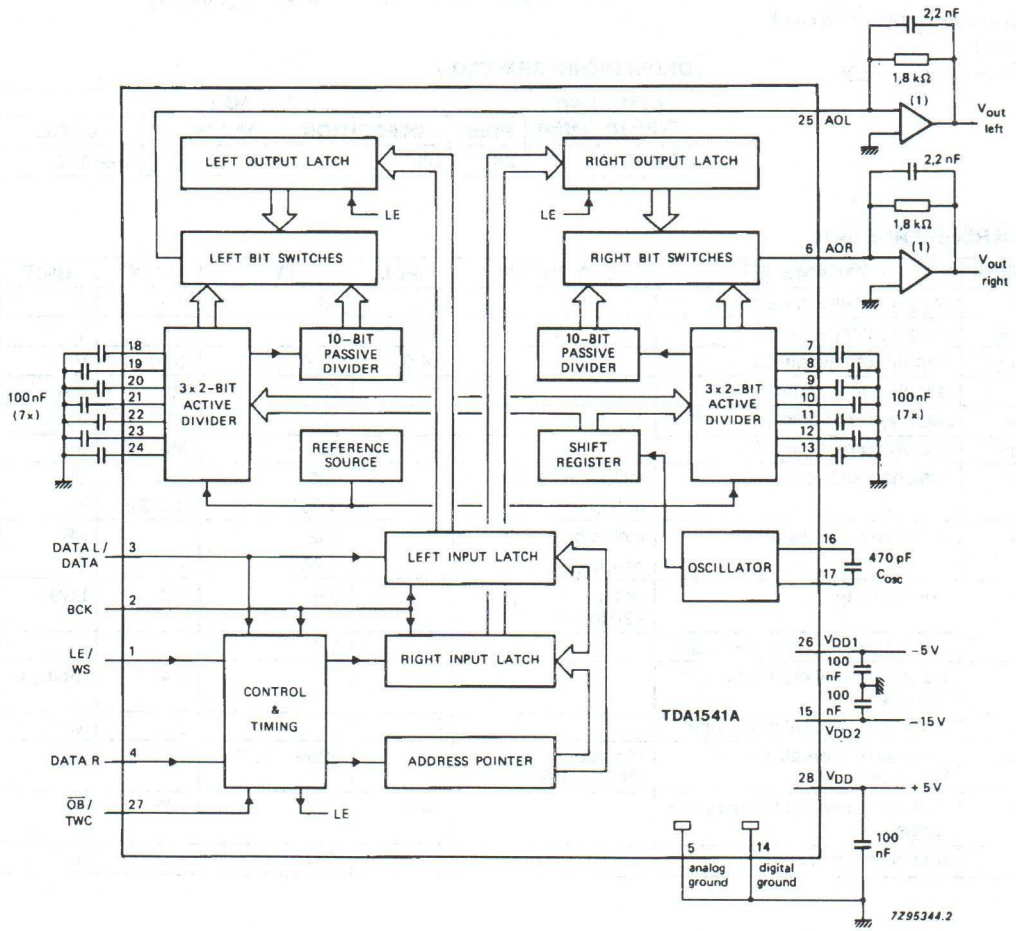
The TDA1541A is a stereo 16-bit digital-to-analog converter (DAC). The ingenious design of the electronic circuit guarantees a high performance and superior sound quality. The TDA1541A is therefore extremely suitable for use in top-end high-fi digital audio equipment such as high quality Compact Disc players or digital amplifiers.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1541A	28	DIL	plastic	SOT117

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage; pin 28		4.5	5.0	5.5	V
$-V_{DD1}$	supply voltage; pin 26		4.5	5.0	5.5	V
$-V_{DD2}$	supply voltage; pin 15		14.0	15.0	16.0	V
I_{DD}	supply current; pin 28		-	27	40	mA
$-I_{DD1}$	supply current; pin 26		-	37	50	mA
$-I_{DD2}$	supply current; pin 15		-	25	35	mA
THD	total harmonic distortion	including noise	-	−95	−90	dB
		at 0 dB	-	0.0018	0.0032	%
THD	total harmonic distortion	including noise	-	−42	-	dB
		at −60 dB	-	0.79	-	%
NL	non-linearity	at T_{amb} = −20 to +85 °C	-	0.5	1.0	LSB
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input; (pin 3 and 4)		-	-	6.4	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	6.4	MHz
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 200 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−40	-	+85	°C
P_{tot}	total power dissipation		-	700	-	mW



(1) TDA1542
(2) 2 x NE5534 or equivalent

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LE/WS*	1	latch enable input / word select input
BCK*	2	bit clock input
DATA L /DATA*	3	data left channel input / data input (selected format)
DATA R*	4	data right channel input
GND(A)	5	analog ground
AOR	6	right channel output
DECOU	7 to 13	decoupling
GND (D)	14	digital ground
V_{DD2}	15	−15 V supply voltage
COSC	16,17	oscillator
DECOU	18 to 24	decoupling
AOL	25	left channel output
V_{DD1}	26	−5 V supply voltage
$\overline{OB}$/TWC*	27	mode select input
V_{DD}	28	+5 V supply voltage

* See Table 1 data selection input.

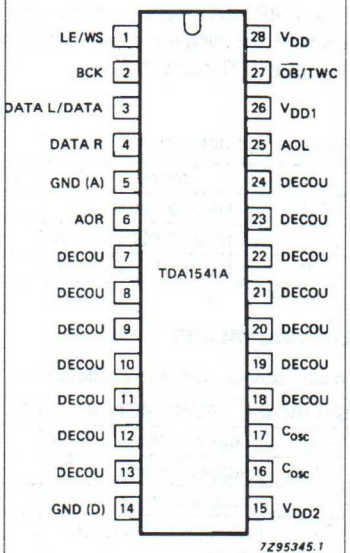


Fig.2 Pin configuration

FUNCTIONAL DESCRIPTION

The TDA1541A accepts input sample formats in time multiplexed mode or simultaneous mode up to 16-bit word length. The most significant bit (MSB) must always be first. This flexible input data format allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits, pulse code modulation adaptors and audio signal processors (ASP).

The high maximum input bit-rate and fast settling facilitates application in 8 x oversampling systems (44.1 kHz to 352.8 kHz or 48 kHz to 384 kHz) with the associated simple analog filtering function (low order, linear phase filter).

Input data selection (see also Table 1)

With the input $\overline{OB}$/TWC connected to ground, data input (offset binary format) must be in time multiplexed mode. It is accompanied with a word select (WS) and a bit clock input (BCK) signal. The converted samples appear at the output, at the first positive going transition of the bit clock signal after a negative going transition of the word select signal.

With $\overline{OB}$/TWC connected to V_{DD} the mode is the same but the data format must be in the two's complement.

When input $\overline{OB}$/TWC input is connected to V_{DD1} the two channels of data (L/R) are input simultaneously via DATA L and DATA R, accompanied with BCK and a latch-enable input (LE). With this mode selected the data must be in offset binary. The converted samples appear at the output at the positive going transition of the latch enable signal.

The format of the data input signals is shown in fig.4 and 5.

True 16-bit performance is achieved by each channel using three 2-bit active dividers, operating on the dynamic element matching principle, in combination with a 10-bit passive current divider, based on emitter scaling. All digital inputs are TTL compatible.

Table 1 Input data selection

$\overline{OB}$/TWC	mode	pin 1	pin 2	pin 3	pin 4
−5 V	simultaneous	LE	BCK	DATA L	DATA R
0 V	time MUX OB	WS	BCK	DATA OB	not used
+5 V	time MUX TWC	WS	BCK	DATA TWC	not used

Where:

LE = latch enable
WS = word select, LOW = left channel; HIGH = right channel
BCK = bit clock
DATA L = data left
DATA R = data right
DATA OB = data offset binary
DATA TWC = data two's complement
MUX OB = mulitplexed offset binary
MUX TWC = multiplexed two's complement = I²S-format

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage; pin 28		0	7	V
$-V_{DD1}$	supply voltage; pin 26		0	7	V
$-V_{DD2}$	supply voltage; pin 15		0	17	V
T_{stg}	storage temperature range		−65	+150	°C
T_{amb}	operating ambient temperature range		−40	+85	°C
V_{es}	electrostatic handling*		−1000	+1000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	30	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; $-V_{DD1}$ = 5 V; $-V_{DD2}$ = 15 V; T_{amb} = +25 °C; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage; pin 28		4.5	5.0	5.5	V
$-V_{DD1}$	supply voltage; pin 26		4.5	5.0	5.5	V
$-V_{DD2}$	supply voltage; pin 15		14.0	15.0	16.0	V
$V_{GND(A)}$ $-V_{GND(D)}$	voltage difference between analog and digital ground		−0.3	0	+0.3	V
I_{DD}	supply current; pin 28		-	27	40	mA
$-I_{DD1}$	supply current; pin 26		-	37	50	mA
$-I_{DD2}$	supply current; pin 15		-	25	35	mA
Inputs						
$-I_{IL}$	input current pins (1, 2, 3 and 4) digital inputs LOW	V_I = 0.8 V	-	-	0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	µA
$\lvert I_{\overline{OB}/TWC}\rvert$	Digital input currents (pin 27) +5 V		-	-	1	µA
$\lvert I_{\overline{OB}/TWC}\rvert$	0 V		-	-	20	µA
$\lvert I_{\overline{OB}/TWC}\rvert$	−5 V		-	-	40	µA
f_{BCK}	input frequency/bit rate clock input pin 2		-	-	6.4	MHz
BR	bit rate data input pin 3 and 4		-	-	6.4	Mbits/s
f_{WS}	word select input pin 2		-	-	200	kHz
f_{LE}	latch enable input 1		-	-	200	kHz
C_I	input capacitance of digital inputs		-	12	-	pF
Analog outputs (AOL; AOR; see note 1)						
Res	resolution		-	16	-	bits
I_{FS}	full scale current		3.4	4.0	4.6	mA
$\lvert I_{ZS}\rvert$	zero scale current		-	25	50	nA
T_{CFS}	full scale temperature coefficient	T_{amb} = −20 to +85 °C	-	±200 x 10^{-6}	-	K^{-1}
Analog outputs (V_{ref})						
E_L	integral linearity error	T_{amb} = 25 °C	-	0.5	1.0	LSB
E_L	integral linearity error	T_{amb} = −20 to +85°C	-	-	1.0	LSB
E_{dL}	differential linearity error	T_{amb} = 20°C, note 2	-	0.5	1.0	LSB
E_{dL}	differential linearity error	T_{amb} = −20 to +85°C	-	-	1.0	LSB
THD	total harmonic distortion	at 0 dB; note 3	−100	-	dB	
			-	0.0010	-	%
THD	total harmonic distortion	including noise at 0 dB;	-	−95	−90	dB
		note 3, Fig.3	-	0.0018	0.0032	%
THD	total harmonic distortion	including noise at −60 dB;	-	−42	-	dB
		note 3, Fig.3	-	0.79	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{cs}	settling time ±1 LSB		-	0.5	-	µs
α	channel separation		90	98	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.1	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	-	0.2	µs
SSVR	supply voltage ripple rejection	V_{DD} = +5 V; note 4	-	−76	-	dB
SSVR	supply voltage ripple rejection	V_{DD1} = −5 V; note 4	-	−84	-	dB
SSVR	supply voltage ripple rejection	V_{DD2} = −15 V; note 4	-	−58	-	dB
S/N	signal-to-noise ratio	at bipolar zero	-	110	-	dB
S/N	signal-to-noise ratio	at full scale	98	104	-	dB
Timing (Fig.4 and 5)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		156	-	-	ns
t_{HB}	bit clock HIGH time		46	-	-	ns
t_{LB}	bit clock LOW time		46	-	-	ns
t_{FBRL}	bit clock fall time to latch enable rise time		0	-	-	ns
t_{RBFL}	bit clock rise time to latch enable fall time		0	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock		0	-	-	ns
$t_{HD;WS}$	word select hold time		0	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. To ensure no performance losses, permitted output voltage compliance is ±25 mV maximum.

2. Selections have been made with respect to the maximum differential linearity error (E_{dL}):

   TDA1541A/N2 bit 1-16 $E_{dL} < 1$ LSB

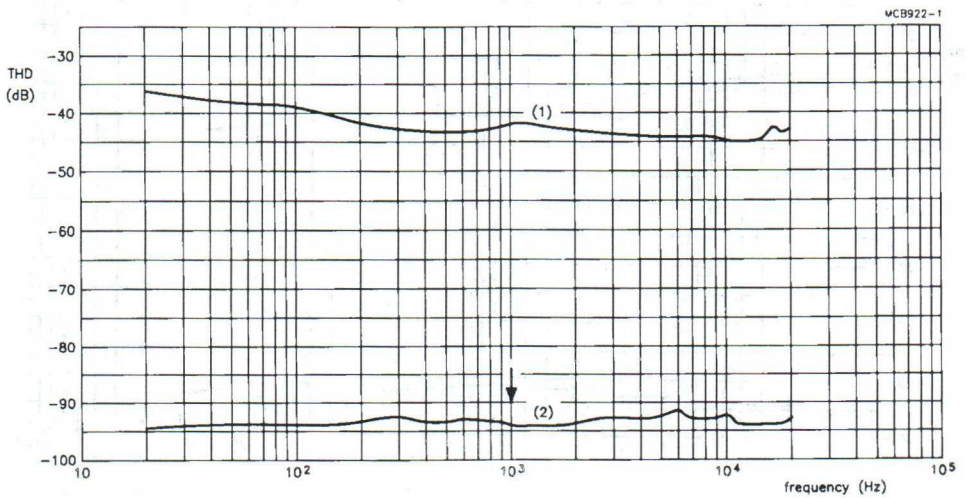
   TDA1541A/N2/R1 bit 1-16 $E_{dL} < 2$ LSB

   TDA1541A/N2/S1 bit 1-7 $E_{dL} < 0.5$ LSB
   bit 8-15 $E_{dL} < 1$ LSB
   bit 16 $E_{dL} < 0.75$ LSB

   The S1 version has been specially selected to achieve extremely good performance even for small signals.

3. Measured using a 1 kHz sinewave generated at a sampling rate of 176.4 kHz.

4. V_{ripple} = 100 mV and f_{ripple} = 100 Hz.

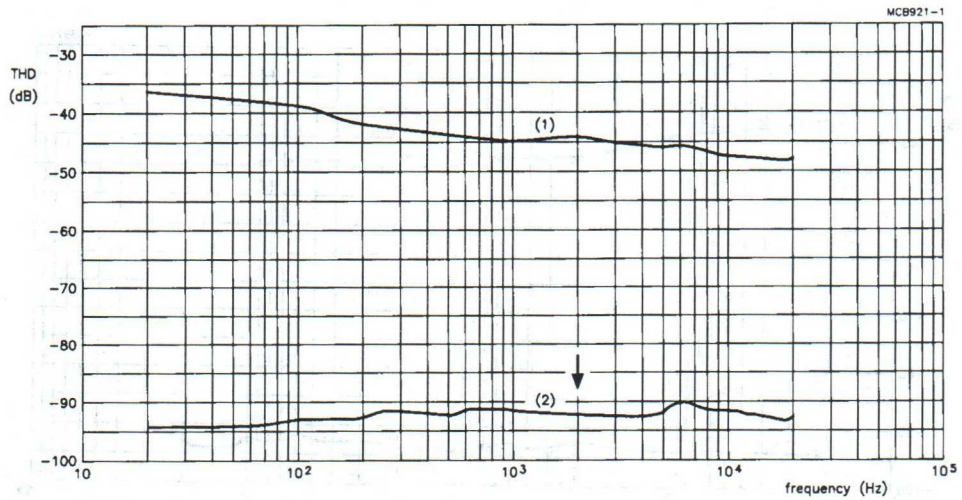


(1) Measured including all distortion plus noise at a signal level of –60 dB
(2) Measured including all distortion plus noise at a signal level of –0 dB

Fig.3a Distortion as a function of frequency (4FS)

Notes to Fig.3a

- The sample frequency 4FS: 176.4 kHz.
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.



(1) Measured including all distortion plus noise at a signal level of −60 dB
(2) Measured including all distortion plus noise at a signal level of −0 dB

Fig.3b Distortion as a function of frequency (8FS)

Notes to Fig.3b

- The sample frequency 8FS: 352.8 kHz.
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.

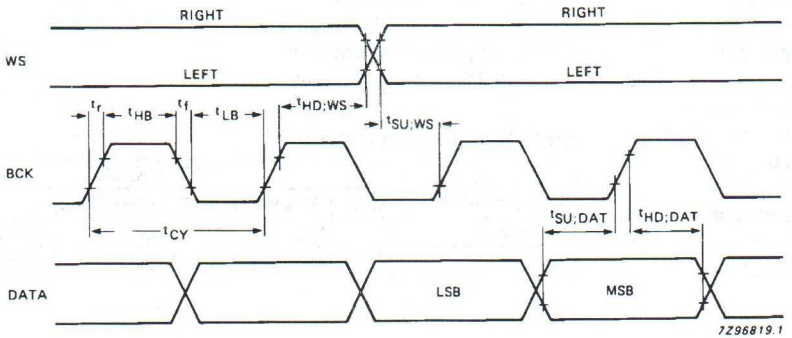
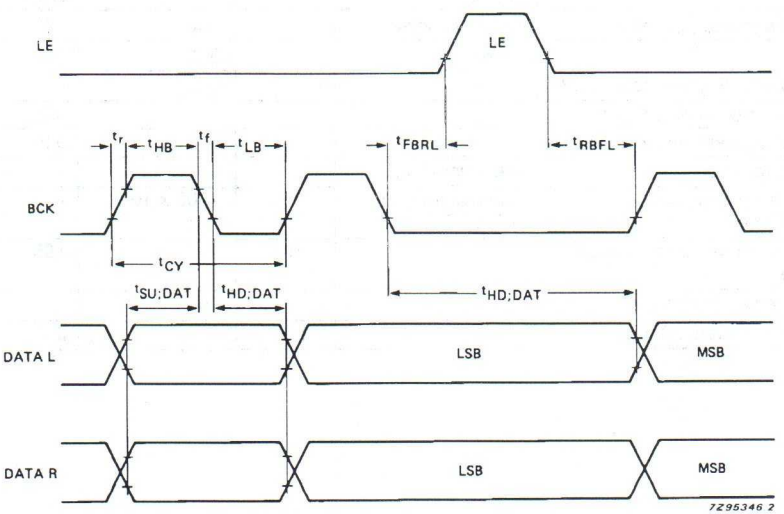


Fig.4 Format of input signals; time multiplexed (I^2S format).



Dual 16-bit DAC (economy version) (I^2S input format) TDA1543

FEATURES

- Low distortion
- 16-bit dynamic range
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- I^2S input format: time multiplexed, two's complement, TTL

GENERAL DESCRIPTION

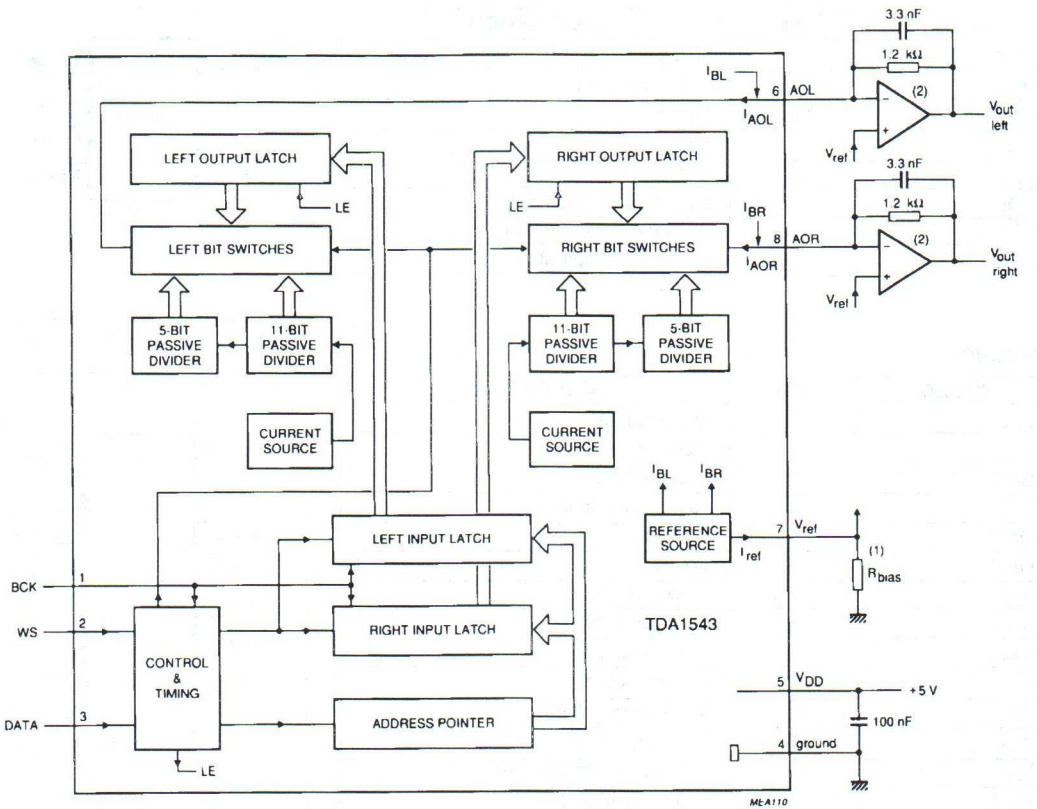
The TDA1543 is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders, digital sound in TV sets and in digital amplifiers.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1543	8	DIL	plastic	SOT97
TDA1543T	16	mini-pack	plastic	SO16L;SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		-	50	60	mA
I_{FS}	full scale output current		1.95	2.30	2.65	mA
THD	total harmonic distortion	including noise	-	−75	−70	dB
		at 0 dB	-	0.018	0.032	%
THD	total harmonic distortion	including noise	-	−30	−23	dB
		at −60 dB	-	3.2	7.9	%
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input		-	-	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	9.2	MHz
S/N	signal-to-noise ratio	at bipolar zero	90	96	-	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 500 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−30	-	+85	°C
P_{tot}	total power dissipation		-	250	-	mW
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA



(1) Optional
(2) 2 x 1/2 NE5532

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	+5 V supply voltage
AOL	6	left channel voltage output
V_{ref}	7	reference voltage output
AOR	8	right channel output

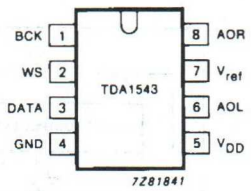


Fig.2(a) Pin configuration TDA1543.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
BCK	3	bit clock input
WS	4	word select input
DATA	5	data input
GND	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DD}	11	+5 V supply voltage
AOL	12	left channel output
V_{ref}	13	reference voltage output
AOR	14	right channel output
n.c.	15	not connected
n.c.	16	not connected

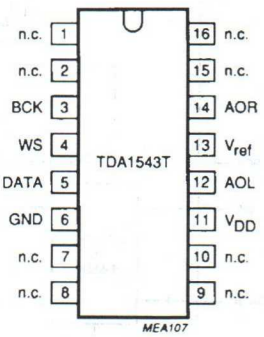
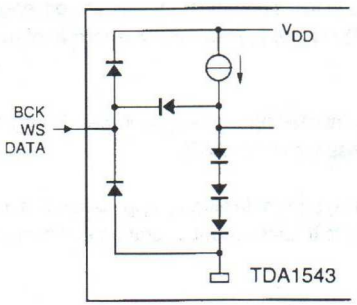
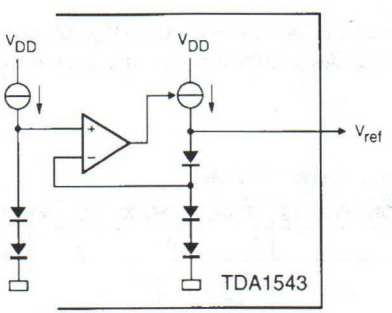


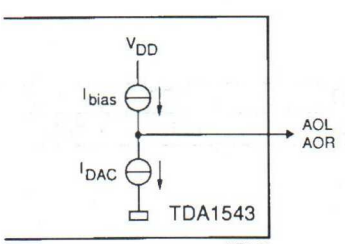
Fig.2(b) Pin configuration TDA1543T.



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig.3 Circuits at the input and output pins.

FUNCTIONAL DESCRIPTION

The TDA1543 accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5.

This flexible input data format (I^2S) allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits and audio signal processor circuits (ASP).

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the left input register and with a HIGH level on the WS input data is placed in the right input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		0	9	V
T_{XTAL}	crystal temperature		-	+150	°C
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		−30	+85	°C
V_{es}	electrostatic handling*		−2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	100	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.0	5.0	8.0	V
I_{DD}	supply current	note 1	-	50	60	mA
RR	ripple rejection	note 2	-	50	-	dB
Digital inputs						
I_{IL}	input current pins (1, 2 and 3) digital inputs LOW	V_I = 0.8 V	-	-	−0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	µA
f_{BCK}	input frequency/bit rate clock input pin 1		-	-	9.2	MHz
BR	bit rate data input pin 3		-	-	9.2	Mbits/s
f_{WS}	word select input pin 2		-	-	192	kHz
Analog outputs (AOL; AOR)						
Res	resolution		-	-	16	bits
	output voltage compliance					
$V_{OC(AC)}$	AC		-	±25	-	mV
$V_{OC(DC)}$	DC		1.8	-	V_{DD}−1.2	V
I_{FS}	full scale current		1.95	2.30	2.65	mA
T_{CFS}	full scale temperature coefficient		-	±500 x 10^{-6}	-	K^{-1}
I_{offset}	offset current	I_{ref} = 0 mA	−0.1	0.0	0.1	mA
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA
AI_{bias}	bias current gain		1.9	2.0	2.1	
Analog outputs (V_{ref})						
V_{ref}	reference voltage output		2.10	2.20	2.30	V
I_{ref}	reference current output		−0.3	-	2.5	mA
THD	total harmonic distortion	including noise at 0 dB;		−75	−70	dB
		note 3, Fig.6		0.018	0.032	%
THD	total harmonic distortion	including noise at −60 dB;	-	−30	−23	dB
		note 3, Fig.6	-	3.2	7.9	%
t_{cs}	settling time ±1 LSB		-	0.5	-	µs
α	channel separation		85	90	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.2	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	< 0.2	-	µs
S/N	signal-to-noise ratio	at bipolar zero; note 5	90	96	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (Fig.4)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		108	-	-	ns
t_{HB}	bit clock HIGH time		22	-	-	ns
t_{LB}	bit clock LOW time		22	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock	note 6	2	-	-	ns
$t_{HD;WS}$	word select hold time	note 6	2	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
5. At code 0000H.
6. At this point $t_{HD;DAT}$ = 0 ns, this value has been fixed on 2 ns due to tolerances.

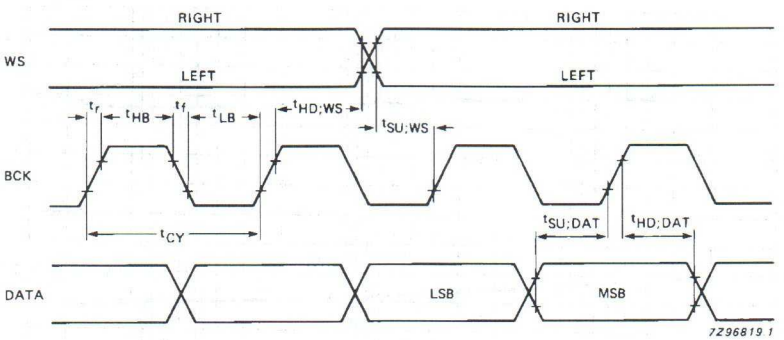


Fig.4 Format of input signals (I^2S format).

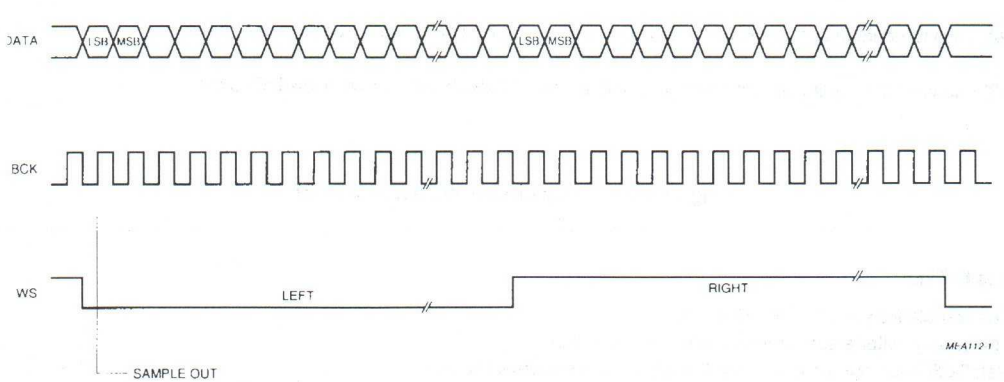
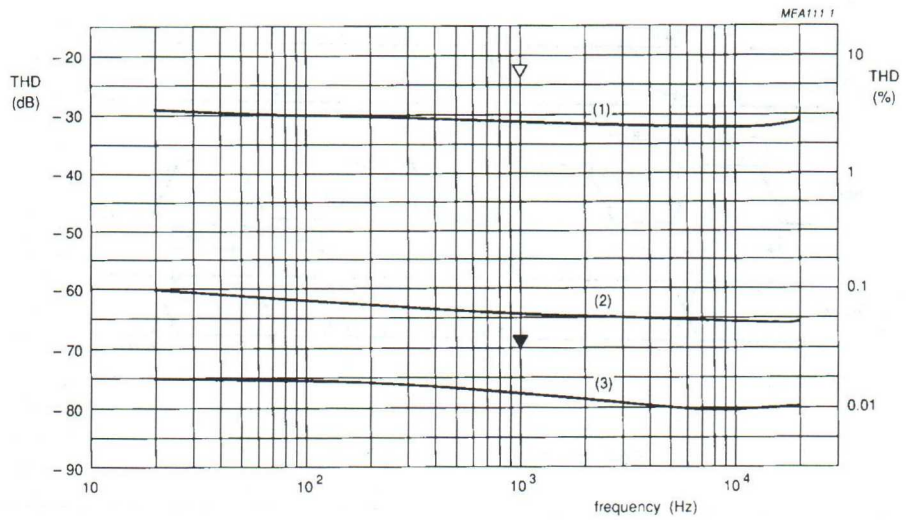


Fig.5 Format of input signals.



(1) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of −60 dB

(2) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of −24 dB

(3) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of −0 dB

Fig.6 Distortion as a function of frequency (4FS)

Notes to Fig.6

- The sample frequency 4FS: 176.4 kHz.
- The supply voltage at the measurement = + 5 V (DC).
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.
- The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied.
- The arrows indicate the specification limits for 0 dB and −60 dB level signals.

Dual 16-bit DAC (economy version) (Japanese input format) TDA1543A

GENERAL DESCRIPTION

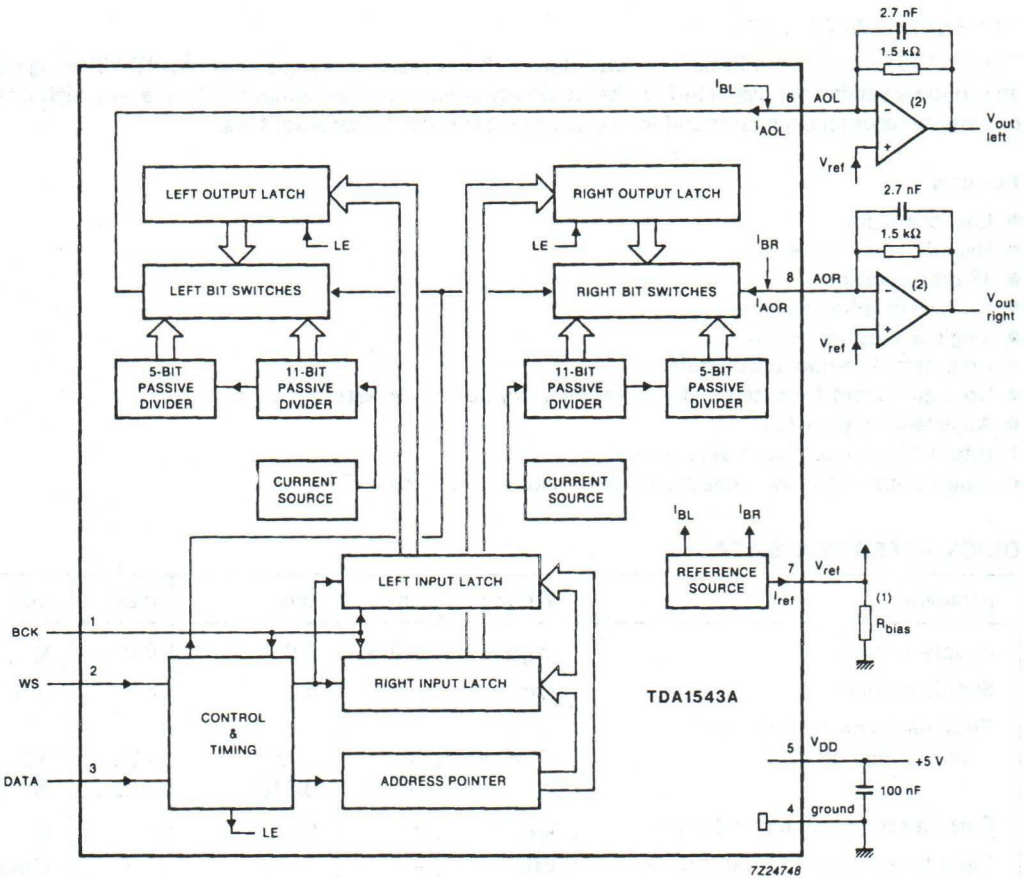
The TDA1543A is a monolithic integrated dual 16-bit digital-to-analogue converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassette recorders, digital sound in television systems and digital amplifiers.

Features

- Low distortion
- High dynamic range
- 16-bit resolution
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- Japanese-input format: time multiplexed, two's complement, TTL

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	3.0	5.0	8.0	V
Supply current	I_{DD}	–	50	60	mA
Total harmonic distortion (including noise)	(D + N)/S	–	–75	–70	dB
		–	0.018	0.032	%
Current settling time to ± 1 LSB	t_{cs}	–	0.5	–	μs
Input bit rate at data input (pin 3)	BR	–	–	9.2	Mbits/s
Clock frequency at clock input (pin 1)	f_{BCK}	–	–	9.2	MHz
Signal-to-noise ratio at bipolar zero	S/N	90	95	–	dB
Full scale temperature coefficient at analogue outputs (AOL; AOR)	TC_{FS}	–	-500×10^{-6}	–	K^{-1}
Operating ambient temperature range	T_{amb}	–30	–	+ 85	°C
Total power dissipation	P_{tot}	–	250	–	mW
Bias current	I_{bias}	–0.6	–	5.0	mA



(1) Optional.
(2) 2 x 1/2 NE5532.

Fig.1 Block diagram.

PINNING

1	BCK	bit clock input
2	WS	word select input
3	DATA	data input
4	GND	ground
5	V_{DD}	+ 5 V supply voltage
6	AOL	left channel output
7	V_{ref}	reference voltage output
8	AOR	right channel output

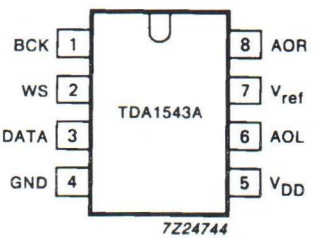
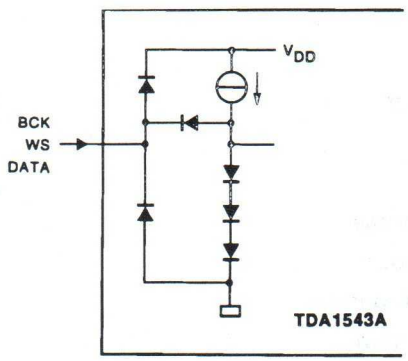
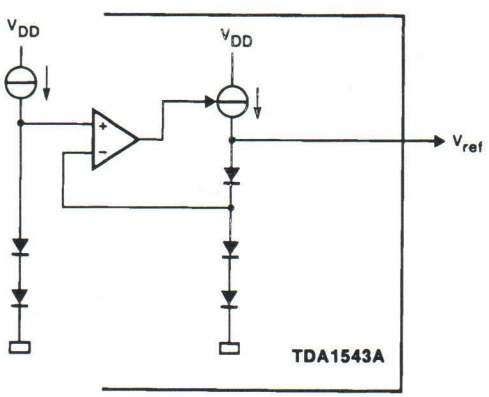


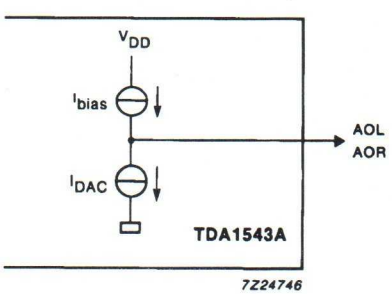
Fig.2 Pinning diagram.



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig.3 Circuits at the input and output pins.

FUNCTIONAL DESCRIPTION

The TDA1543A accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5.

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the right input register and with a HIGH level on the WS input data is placed in the left input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	0	9	V
Crystal temperature	T_{XTAL}	–	150	°C
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	−30	+ 85	°C
Electrostatic handling *	V_{es}	−1000	+ 1000	V

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	100	K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = + 25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	3.0	5.0	8.0	V
Supply current	note 1	I_{DD}	–	50	60	mA
Ripple rejection	note 2	RR	–	50	–	dB
Inputs						
Input current pins (1, 2 and 3)						
digital inputs LOW	V_I = 0.8 V	I_{IL}	–	–	–0.4	mA
digital inputs HIGH	V_I = 2.0 V	I_{IH}	–	–	20	μA
Input frequency/bit rate						
clock input pin 1		f_{BCK}	–	–	9.2	MHz
bit rate data input pin 3		BR	–	–	9.2	Mbits/s
word select input pin 2		f_{WS}	–	–	192	kHz
Input capacitance of digital inputs		C_I	–	*	–	pF
Analogue outputs (AOL; AOR)						
Resolution		Res	–	–	16	bits
Output voltage compliance						
AC		$V_{OC(AC)}$	–	± 25	–	mV
DC		$V_{OC(DC)}$	1.8	–	V_{DD}–1.2	V
Full scale current		I_{FS}	1.95	2.3	2.65	mA
Full scale temperature coefficient		TC_{FS}	–	-500×10^{-6}	–	K^{-1}
Offset current	I_{ref} = 0 mA; $V_{AO} = V_{ref}$	I_{offset}	–0.1	0	0.1	mA
Bias current (adjustable)		I_{bias}	–0.6	–	5.0	mA
Bias current gain		AI_{bias}	1.9	2.0	2.1	

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output (V_{ref})						
Reference voltage output		V_{ref}	2.1	2.2	2.3	V
Reference current output		I_{ref}	−0.3	–	2.5	mA
Total harmonic distortion (including noise)	note 3	(D + N)/S	–	−75	−70	dB
			–	0.018	0.032	%
Settling time ± 1 LSB		t_{cs}	–	0.5	–	μs
Channel separation		α	84	90	–	dB
Unbalance between outputs	note 3	$\lvert d_{IO} \rvert$	–	< 0.2	0.3	dB
Time delay between outputs		t_d	–	< 0.2	–	μs
Signal-to-noise ratio at bipolar zero	note 4	S/N	90	95	–	dB
Timing	Fig.4					
Rise time		t_r	–	–	32	ns
Fall time		t_f	–	–	32	ns
Bit clock cycle time		t_{CY}	108	–	–	ns
Bit clock HIGH time		t_{HB}	22	–	–	ns
Bit clock LOW time		t_{LB}	22	–	–	ns
Data set-up time		$t_{SU;DAT}$	32	–	–	ns
Data hold time to bit clock		$t_{HD;DAT}$	2	–	–	ns
Word select hold time		$t_{HD;WS}$	2	–	–	ns
Word select set-up time		$t_{SU;WS}$	32	–	–	ns

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. With 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
4. At code 0000H.

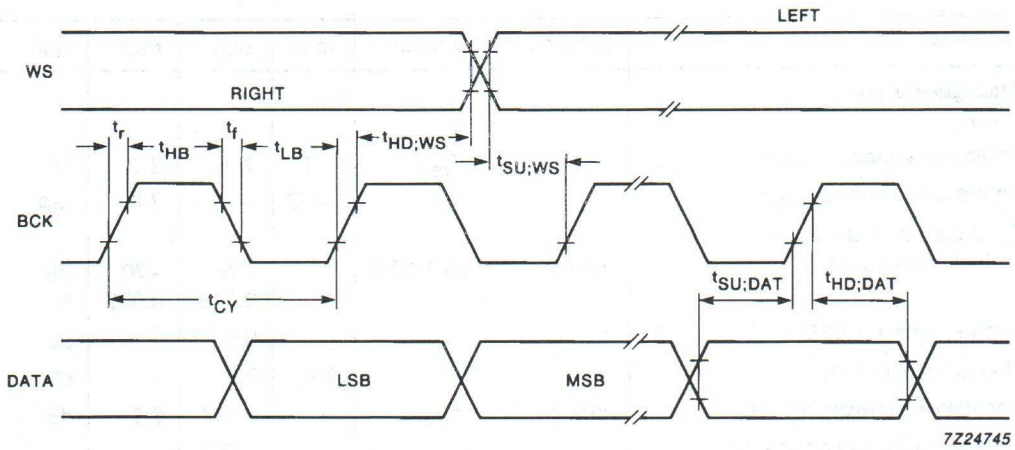


Fig.4 Format of input signals (Japanse format).

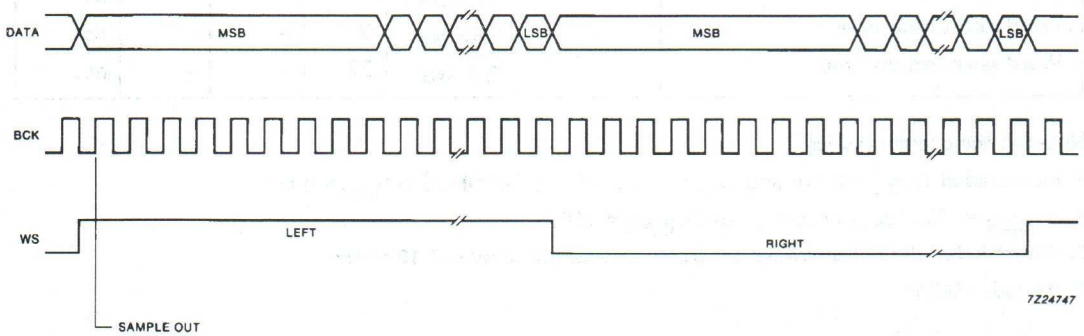


Fig.5 Format of input signals.

Stereo continuous calibration DAC

TDA1545A

FEATURES

- Space saving package (SO8 or DIL8)
- Low power consumption
- Low total harmonic distortion
- Wide dynamic range (16-bit resolution)
- Continuous calibration concept
- Easy application: single 3 to 5.5 V rail power supply and output- and bias current are proportional to the supply voltage
- Fast settling time permits 2 x, 4 x and 8 x oversampling (serial input) or double speed operation at 4 x oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range of −40 °C to +85 °C
- Compatible with most of the Japanese input formats: time multiplexed, two's complement and TTL
- No zero crossing distortion.

GENERAL DESCRIPTION

The TDA1545A is the first device of a new generation of the digital-to-analog convertors which embodies the innovative technique of continuous calibration. The largest bit-currents are repeatedly generated by one single current reference source. This duplication is based upon an internal charge storage principle having an accuracy insensitive to ageing, temperature and process variations.

The device is fabricated in a 1.0 µm CMOS process and features an extremely low power dissipation, small package size and easy application. Furthermore, the accuracy of the high coarse current combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensures high quality audio reproduction. Therefore, the continuous calibration digital-to-analog convertor is eminently suitable for use in (portable) digital audio equipment.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1545A	8	DIL	plastic	SOT97
TDA1545AT	8	mini-pack	plastic	SO8; SOT96A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3	5	5.5	V
I_{DD}	supply current	V_{DD} = 5 V; at code 0000H	–	3.0	4.0	mA
I_{FS}	full scale output current					
		V_{DD} = 5 V	0.9	1.0	1.1	mA
		V_{DD} = 3 V	–	0.6	–	mA
THD	total harmonic distortion	including noise				
		at 0 dB	–	–88	–78	dB
		at 0 dB	–	0.004	0.01	%
		at –60 dB	–	–33	–24	dB
		at –60 dB	–	2.2	6	%
		at –60 dB; A-weighting	–	–35	–	dB
		at –60 dB; A-weighting	–	1.7	–	%
		at –60 dB; A-weighting; R3 = R4 = 11 kΩ; I_{FS} = 2 mA	–	1.4	–	%
S/N	signal-to-noise ratio at bipolar zero					
		A-weighting; at code 0000H	86	98	–	dB
		R3 = R4 = 11 kΩ; I_{FS} = 2 mA	–	101	–	dB
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
BR	input bit rate at data input		–	–	18.4	Mbits/s
f_{BCK}	clock frequency at clock input		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (IOL; IOR)		–	±400	–	ppm
P_{tot}	total power dissipation	at code 0000H				
		V_{DD} = 5 V	–	15	20	mW
		V_{DD} = 3 V	–	6	–	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C

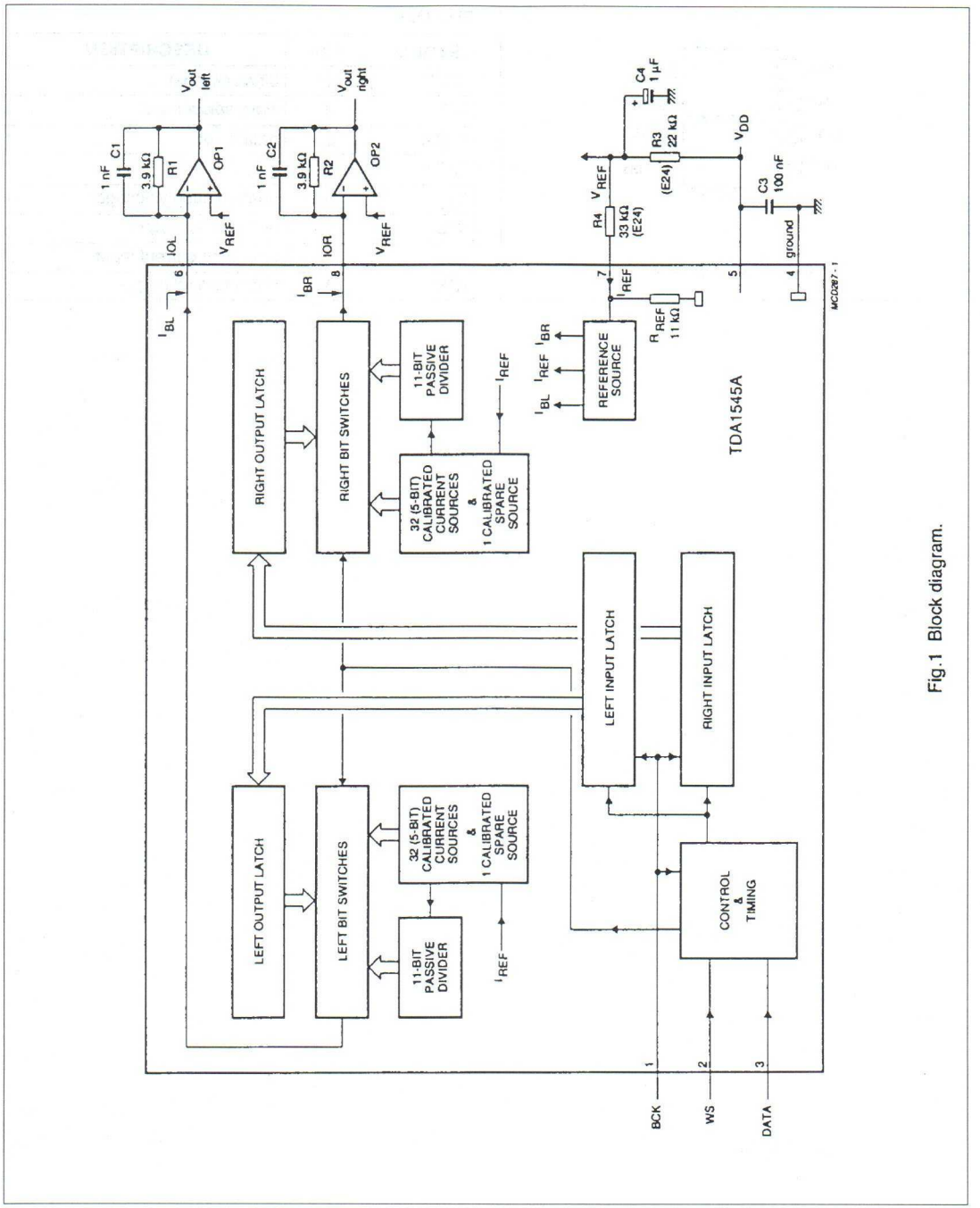


Fig.1 Block diagram.

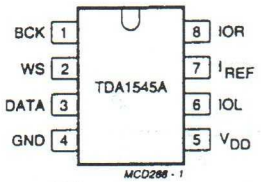


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	positive supply voltage
IOL	6	left channel output
I_{REF}	7	reference current input
IOR	8	right channel output

FUNCTIONAL DESCRIPTION

The basic operation of the continuous calibration DAC is illustrated in Fig.3. The figure shows the calibration principle (Fig.3a) and operation principle (Fig.3b). During calibration of the MOS current source (Fig.3a) transistor M1 is connected as a diode by applying a reference current. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} of M1 is then determined by the transistor characteristics. After calibration of the drain current to the reference value I_{REF}, the switch S1 is opened and S2 is switched to the other position (Fig.3b). The gate-to-source voltage V_{gs} of M1 is not changed because the charge on C_{gs} is preserved. Therefore the drain current of M1 will still be equal to I_{REF} and this exact duplicate of I_{REF} is now available at the I_{out} terminal. The 32 current sources and the spare current source of the TDA1545A are continuously calibrated (see Fig.1). The spare current is included to allow for continuous convertor operation. The output of one calibrated source is connected to an 11-bit binary current divider consisting of 2048 transistors. A symmetrical offset decoding principle is incorporated and arranges the bit switching in such a way that the zero-crossing is performed only by the LSB currents. The TDA1545A accepts input serial data formats of 16-bit word length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5. With a LOW level on the word select input (WS) input data is placed in the right input register and with a HIGH level on the WS input data is placed in the left input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches. An internal bias current Ibias (see IBL and IBR in Fig.1) is added to the full scale output current IFS in order to achieve the maximum dynamic range at the outputs of OP1 and OP2 (see Fig.1). The reference input current IREF controls with gain AFS the current IFS which is a sink current and with gain Abias the I_{bias} which is a source current (note 1). The current I_{REF} is proportional to V_{DD} so the I_{FS} and I_{bias} will also be proportional to V_{DD} (note 2) because A_{FS} and A_{bias} are constant. The reference output voltage V_{REF} in Fig.1 is 2/3 V_{DD}. In this way the maximum dynamic range is achieved over the entire power supply range. The tolerance of the reference input current in Fig.1 depends on the tolerance of the resistors R3, R4 and R_{REF} (note 3).

Notes to the functional description

1. $I_{FS} = A_{FS} \times I_{REF}$ and $I_{bias} = A_{bias} \times I_{REF}$
2. $\frac{V_{DD1}}{V_{DD2}} = \frac{I_{FS1}}{I_{FS2}} = \frac{I_{bias1}}{I_{bias2}}$
3. $\Delta I_{REF} = I_{REF} - \frac{V_{DD}}{R3 + \Delta R3 + R4 + \Delta R4 + R_{REF} + \Delta R_{REF}}$

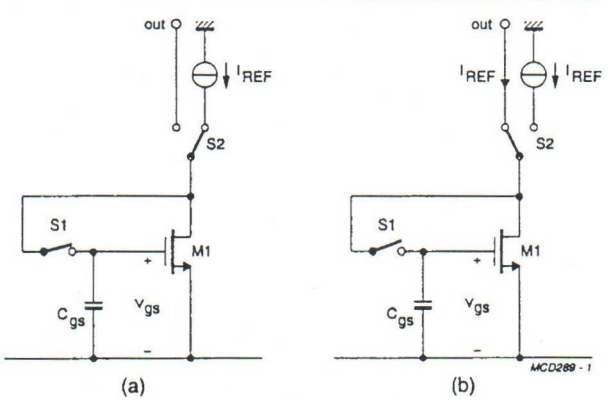


Fig.3 Calibration principle; (a) calibration, (b) operation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	–	6	V
T_{XTAL}	maximum crystal temperature	–	+150	°C
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−40	+85	°C
V_{es}	electrostatic handling (note 1)	−2000	+2000	V
V_{es}	electrostatic handling (note 2)	−200	+200	V

Notes

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
2. Machine model; C = 200 pF, L = 0.5 μH, R = 10 Ω, 3 zaps positive and negative.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	
	SOT97	100 K/W
	SOT96A	210 K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; measured in the circuit of Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	supply current	note 1	–	3.0	4.0	mA
RR	ripple rejection	note 2	–	30	–	dB
Digital inputs (WS; BCK; DATA)						
$\|I_{IL}\|$	input leakage current LOW	V_I = 0.8 V	–	–	10	µA
$\|I_{IH}\|$	input leakage current HIGH	V_I = 2.4 V	–	–	10	µA
f_{BCK}	bit clock input frequency		–	–	18.4	MHz
BR	bit rate data input		–	–	18.4	Mbits/s
f_{WS}	word select input		–	–	384	kHz
Timing (Fig.4)						
t_r	rise time		–	–	12	ns
t_f	fall time		–	–	12	ns
t_{CY}	bit clock cycle time		54	–	–	ns
t_{HB}	bit clock HIGH time		15	–	–	ns
t_{LB}	bit clock LOW time		15	–	–	ns
$t_{SU;DAT}$	data set-up time		12	–	–	ns
$t_{HD;DAT}$	data hold time		2	–	–	ns
$t_{HD;WS}$	word select hold time		2	–	–	ns
$t_{SU;WS}$	word select set-up time		12	–	–	ns
Analog input (I_{REF})						
R_{REF}	reference resistor (see Fig.1)		7.4	11.0	14.6	kΩ
Analog outputs (IOL; IOR)						
Res	resolution		–	–	16	bit
V_{DCC}	DC output voltage compliance		2.0	–	V_{DD}–1	V
I_{FS}	full scale current		0.9	1.0	1.1	mA
T_{CFS}	full scale temperature coefficient		–	±400	–	ppm
I_{bias}	bias current		643	714	785	µA
A_{FS}	reference input current to full scale output current gain		–	13.2	–	
A_{bias}	reference input current to bias current gain		–	9.42	–	
THD	total harmonic distortion	including noise at 0 dB; note 3, see Fig.6	– –	–88 0.004	–78 0.01	dB %
THD	total harmonic distortion	including noise at –60 dB; note 3, Fig.6	– –	–33 2.2	–24 6	dB %

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion	including noise at –60 dB, A-weigthing	–	–35	–	dB
			–	1.8	–	%
		R3 = R4 = 11 kΩ see Fig.1; I_{FS} = 2 mA	–	1.4	–	%
THD	total harmonic distortion	including noise at 0 dB; note 4	–	–84	–70	dB
			–	0.006	0.03	%
t_{cs}	settling time ±1 LSB		–	0.2	–	µs
α	channel separation		86	95	–	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 3	–	0.2	0.3	dB
$\lvert t_d \rvert$	delay time between outputs		–	±0.2	–	µs
S/N	signal-to-noise ratio (A-weighting)	at bipolar zero; note 1	86	98	–	dB
S/N	signal-to-noise ratio (A-weighting)	at bipolar zero; note 5	–	101	–	dB

Notes

1. At code 0000H.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz sinewave over a 20 Hz to 20 kHz bandwidth generated at a sampling rate of 192 kHz.
5. R3 = R4 = 11 kΩ; see Fig.1; I_{FS} = 2 mA.

TEST AND APPLICATION INFORMATION

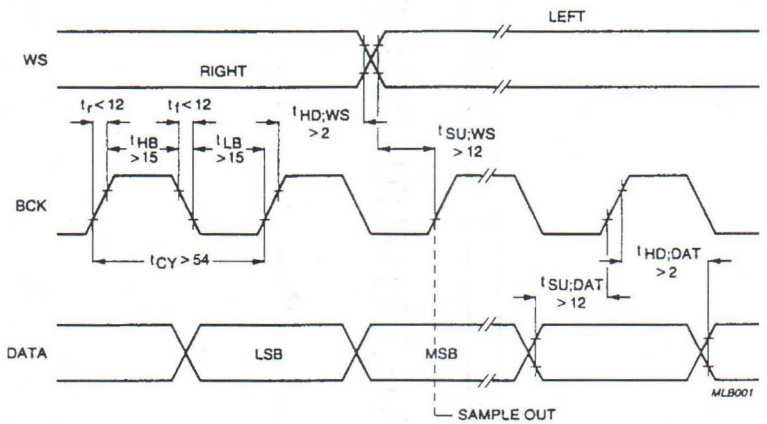


Fig.4 Timing and input signals.

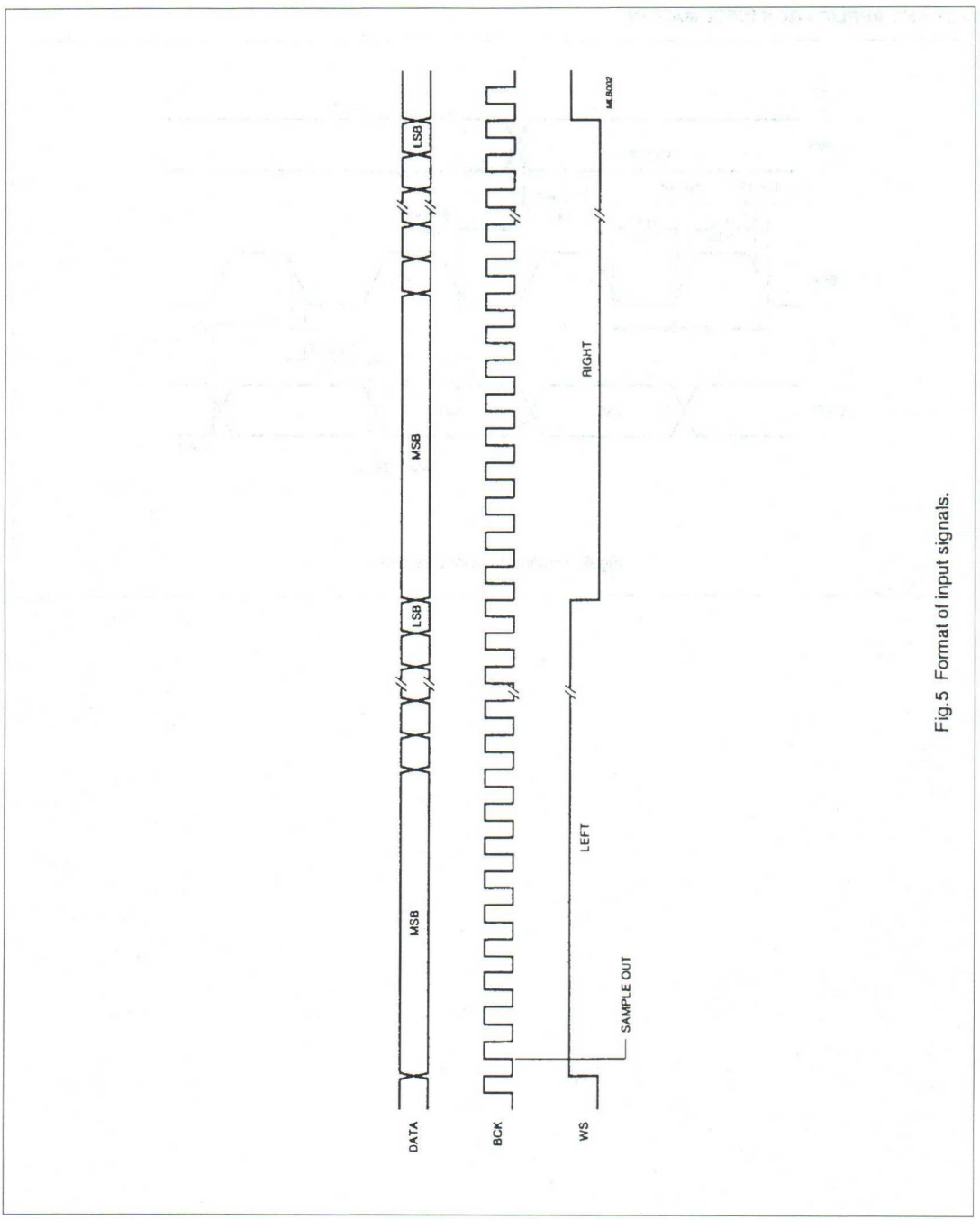
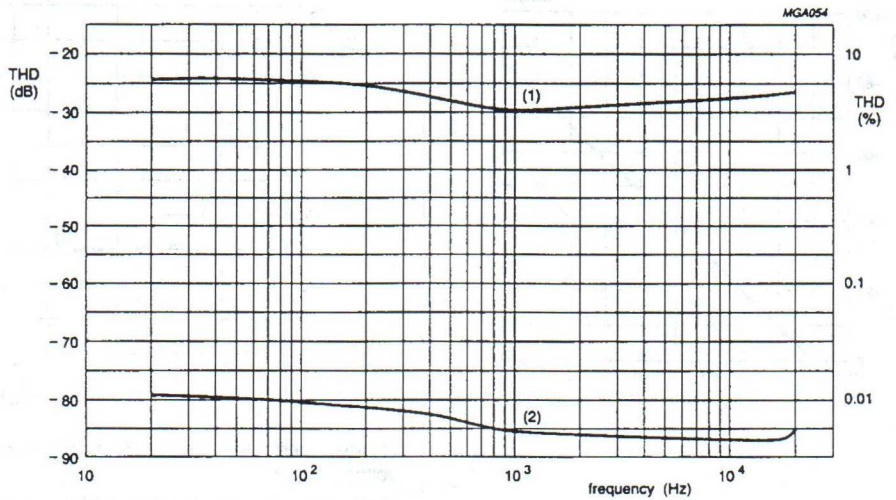


Fig.5 Format of input signals.

APPLICATION INFORMATION



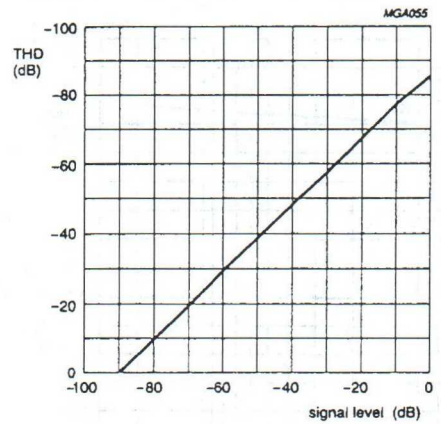
(1) Measured including all distortion plus noise at a level of −60 dB

(2) Measured including all distortion plus noise at a level of −0 dB

The sample frequency 4FS: 176.4 kHz

The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied

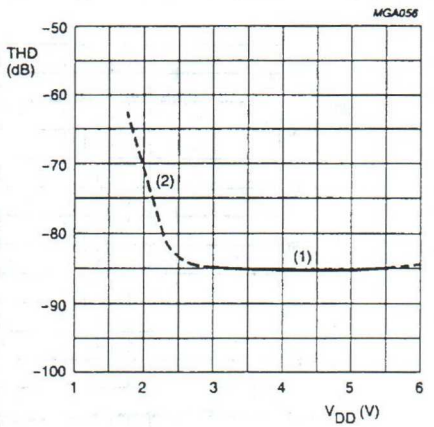
Fig.6 Total harmonic distortion as a function of frequency (4FS).



The sample frequency 4FS: 176.4 kHz

The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied

Fig.7 Total harmonic distortion as a function of signal level (4FS).



(1) Measured within the specified operating supply voltage range

(2) Measured outside the specified operating supply voltage range

The sample frequency 4FS: 176.4 kHz

The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied

Fig.8 Total harmonic distortion as a function of supply voltage V_{DD} (4FS).

Dual top-performance bitstream DAC

TDA1547

FEATURES

- Top-grade audio performance
  - very low harmonic distortion
  - high signal-to-noise ratio
  - wide dynamic range of approximately 108 dB (not A-weighted)
- High crosstalk immunity
- Bitstream concept
  - high over-sampling rate up to 192 f_s
  - pulse-density modulation
  - inherently monotonic
  - no zero-crossing distortion

GENERAL DESCRIPTION

The TDA1547 is a dedicated one-bit digital-to-analog converter to facilitate a high fidelity sound reproduction of digital audio. The TDA1547 is extremely suitable for use in high quality audio systems such as Compact Disc and DAT players, or in digital amplifiers and digital signal processing systems. The TDA1547 is used in combination with the SAA7350 bitstream circuit, which includes the third-order noise shaper. The excellent performance of the SAA7350 and TDA1547 bitstream conversion system is obtained by separating the noise shaping circuit and the one-bit conversion circuit over two IC's, thereby reducing the crosstalk between the digital and analog parts. The TDA1547 one-bit converter is processed in BIMOS. In the digital logic and drivers bipolar transistors are used to optimize speed and to reduce digital noise generation. In the analog part the bipolar transistors are used to obtain high performance of the operational amplifiers. Special layout precautions have been taken to achieve a high crosstalk immunity. The layout of the TDA1547 has fully separated left and right channels and supply voltage lines between the digital and analog sections.



ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1547	32	SDIL	plastic	SOT232A

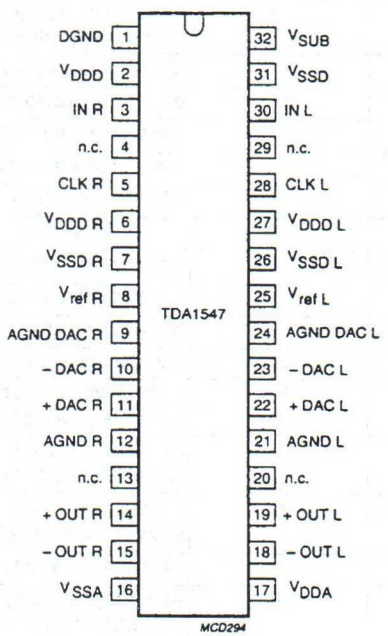


Fig.1 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DGND	1	0 V digital supply
V_{DDD}	2	5 V digital supply for both channels
IN R	3	serial one-bit data input for the right channel
n.c.	4	pin not connected; should preferably be connected to digital ground
CLK R	5	clock input for the right channel
$V_{DDD\ R}$	6	5 V digital supply for the right channel; this voltage determines the internal logic HIGH level in the right channel
$V_{SSD\ R}$	7	−3.5 V digital supply for the right channel; this voltage determines the internal logic LOW level in the right channel
$V_{ref\ R}$	8	−4 V reference voltage for the right channel switched capacitor DAC
AGND DAC R	9	0 V reference voltage for the right channel switched capacitor DAC; this pin should be connected to analog ground
−DAC R	10	output from the right negative switched capacitor DAC; feedback connection for the right negative operational amplifier
+DAC R	11	output from the right positive switched capacitor DAC; feedback connection for the right positive operational amplifier
AGND R	12	0 V reference voltage for both right channel operational amplifiers
n.c.	13	pin not connected; should preferably be connected to analog ground
+OUT R	14	+ output of the switched capacitor operational amplifier
−OUT R	15	− output of the switched capacitor operational amplifier
V_{SSA}	16	−5 V analog supply
V_{DDA}	17	5 V analog supply
−OUT L	18	− output of the switched capacitor operational amplifier
+OUT L	19	+ output of the switched capacitor operational amplifier
n.c.	20	pin not connected; should preferably be connected to analog ground
AGND L	21	0 V reference voltage for both left channel operational amplifiers
+DAC L	22	output from the left positive switched capacitor DAC; feedback connection for the left positive operational amplifier
−DAC L	23	output from the left negative switched capacitor DAC; feedback connection for the left negative operational amplifier
AGND DAC L	24	0 V reference voltage for the left channel switched capacitor DAC; this pin should be connected to analog ground
$V_{ref\ L}$	25	−4 V reference voltage for the left channel switched capacitor DAC
$V_{SSD\ L}$	26	−3.5 V digital supply for the left channel; this voltage determines the internal logic LOW level in the left channel
$V_{DDD\ L}$	27	5 V digital supply for the left channel; this voltage determines the internal logic HIGH level in the left channel

SYMBOL	PIN	DESCRIPTION
CLK L	28	clock input for the left channel
n.c.	29	pin not connected; should preferably be connected to digital ground
IN L	30	serial one-bit data input for the left channel
V_{SSD}	31	−5 V digital supply for both channels
V_{SUB}	32	−5 V substrate voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Supply voltages						
$V_{DDD\ L,\ R}$	positive digital supply voltage for one channel; pins 27 and 6		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage for both channels; pin 2		4.5	5.0	5.5	V
$V_{SSD\ L,\ R}$	negative digital supply voltage for one channel; pins 26 and 7		−4.0	−3.5	−3.0	V
V_{SSD}	negative digital supply voltage for both channels; pin 31		−5.5	−5.0	−4.5	V
V_{DDA}	positive analog supply voltage; pin 17		4.5	5.0	6	V
V_{SSA}	negative analog supply voltage ; pin 16		−6.0	−5.0	−4.5	V
Supply current						
$I_{DDD\ L,\ R}$	positive digital supply current for one channel; pins 27 and 6		-	0.1	-	mA
I_{DDD}	digital supply current for both channels; pin 2		-	29.0	-	mA
$I_{SSD\ L,\ R}$	negative digital supply current for one channel; pins 26 and 7		-	−0.1	-	mA
I_{SSD}	negative supply current for both channels; pin 31		-	−28.0	-	mA
I_{DDA}	positive analog supply current; pin 17		-	51.0	-	mA
I_{SSA}	negative analog supply current; pin 16		-	−51.0	-	mA
P_{tot}	total power dissipation		-	800	-	mW
$V_{OUT(RMS)}$	output voltage (RMS value)	f_{CLK} = 8.46 MHz; notes 1 and 2	0.85	1.0	1.15	V

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Supply current						
(THD + N)/S	THD + Noise; 0 dB	1 kHz; notes 2 and 3	-	−101	−96	dB
			-	0.0009	0.0016	%
(THD + N)/S	THD + Noise; 0 dB	f = 20 Hz to 20 kHz; notes 2 and 4	-	−101	-	dB
			-	0.0009	-	%
(THD + N)/S	THD + Noise; −20 dB	f = 1 kHz; notes 2 and 3	-	−88	−84	dB
(THD + N)/S	THD + Noise; −60 dB	f = 1 kHz; notes 2 and 3	-	−48	−44	dB
S/N	signal-to-noise ratio	pattern 0101..; notes 2 and 5	109	111	-	dB
S/N	signal-to-noise ratio; "A"-weighting	pattern 0101..; notes 2 and 5	-	113	-	dB
f_{CLK}	maximum clock frequency		-	-	10	MHz
α	channel separation	f = 1 kHz	101	115	-	dB
T_{amb}	operating ambient temperature		−20	-	70	°C

Notes to the quick reference data

1. Output level tracks linearly with both the clock frequency and the reference voltage ($V_{ref\ L}$ or $V_{ref\ R}$)
2. Device measured in differential mode with external components as shown in Fig.5.
3. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 1 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
4. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 20 Hz to 20 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
5. The specified signal-to-noise ratio includes noise introduced by the application components as shown in Fig.5.

FUNCTIONAL DESCRIPTION

Both channels are completely separated to reach the desired high crosstalk suppression level.
Each channel consists of the following functional parts:

- One-bit input, which latches the incoming data to the system clock.
- Switch driver circuit, which generates the non-overlapping clock- and data-signals that control the DAC switched capacitor networks.
- Switched capacitor network, this forms the actual DAC function, it supplies charge packets to the low-pass filter, under control of the incoming one-bit code.
- Two high performance operational amplifiers, that perform the charge packet to voltage conversion and deliver a differential output signal. The first pole of the low-pass filter is built around them.

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j-a}$	from junction to ambient	60	K/W

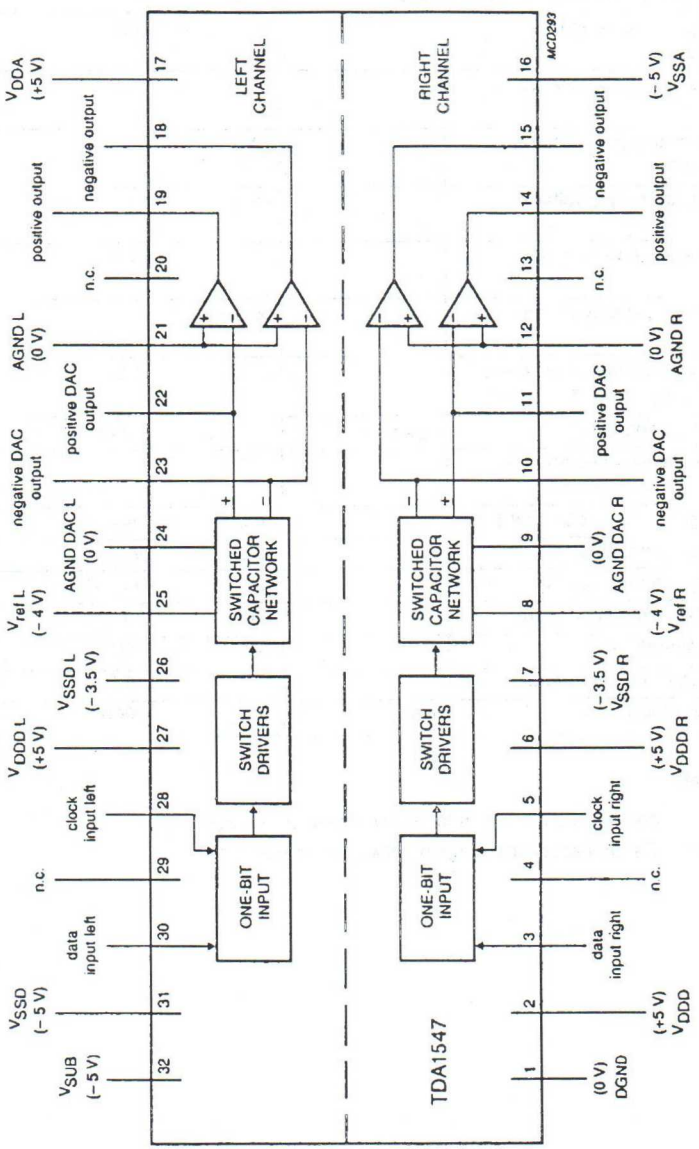


Fig.2 Block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX.	UNIT
V_{SUB}	negative substrate voltage; pin 32	note 1	−7.0	-	V
$V_{DDD\ L,\ R}$	positive digital supply voltage; pins 27 and 6		-	5.5	V
V_{DDD}	positive digital supply voltage; pin 2		-	5.5	V
$V_{SSD\ L,\ R}$	negative digital supply voltage; pins 26 and 7		−4.0	-	V
V_{SSD}	negative digital supply voltage; pin 31		−5.5	-	V
V_{DDA}	positive analog supply voltage; pin 17		-	6.0	V
V_{SSA}	negative analog supply voltage; pin 16		−6.0	-	V
$V_{DDD\ L,\ R}$ - $V_{SSD\ L,\ R}$	supply voltage difference between pins 27, 6 and pins 26, 7		-	9.0	V
P_{tot}	total power dissipation	T_{amb} = 70 °C	-	1300	mW
$V_{ref\ L,\ R}$	input reference voltage; pins 25 and 8		−6.0		V
$V_{CLK\ L,\ R}$	input voltage clock; pins 28 and 5		−0.5	V_{DDD}+0.5	V
$V_{I\ L}$	input voltage channel; pin 30		−0.5	V_{DDD}+0.5	V
$V_{I\ R}$	input voltage channel; pin 3		−0.5	V_{DDD}+0.5	V
T_{amb}	operating ambient temperature		−20	70	°C
T_{stg}	storage temperature		−40	150	°C
T_{XTAL}	maximum crystal temperature		-	150	°C
V_{ES}	electrostatic handling	note 2	-	2000	V

Notes to the limiting values

1. The substrate voltage must be lower than or equal to the lowest supply voltage.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DDD}, $V_{DDD\ L,\ R}$, V_{DDA} = +5 V; V_{SSD}, V_{SSA} = −5 V, $V_{SSD\ L,\ R}$ = −3.5 V; $V_{ref\ L,\ R}$ = −4 V; T_{amb} = 25°C; f_{CLK} = 8.46 MHz; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{SUB}	negative substrate voltage; pin 32	note 1	−7.0	-	−4.5	V
$V_{DDD\ L,\ R}$	positive digital supply voltage for one channel; pins 27 and 6		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage for both channels; pin 2		4.5	5.0	5.5	V
$V_{SSD\ L,\ R}$	negative digital supply voltage for one channel; pins 26 and 7		−4.0	−3.5	−3.0	V
V_{SSD}	negative digital supply voltage for both channels; pin 31		−5.5	−5.0	−4.5	V
V_{DDA}	positive analog supply voltage; pin 17		4.5	5.0	6.0	V
V_{SSA}	negative analog supply voltage; pin 16		−6.0	−5.0	−4.5	V
$V_{DDD\ L,\ R}$ - $V_{SSD\ L,\ R}$	supply voltage difference between pins 27, 6 and pins 26, 7		-	-	9.0	V
$V_{SSD\ L,\ R}$ - V_{SSD}	supply voltage difference between pins 26, 7 and pin 31		1.3	-	-	V
$I_{DDD\ L,\ R}$	positive digital supply current for one channel; pins 27 and 6		-	0.1	-	mA
I_{DDD}	digital supply current for both channels; pin 2			29.0	46	mA
$I_{SSD\ L,\ R}$	negative digital supply current for one channel; pins 26 and 7		-	−0.1	-	mA
I_{SSD}	negative supply current for both channels; pin 31		−45	−28.0	-	mA
$-I_{DDA}$	positive analog supply current; pin 17		-	51.0	63	mA
I_{SSA}	negative analog supply current; pin 16		−63.0	−51.0	-	mA
P_{SSR1}	power supply rejection ratio	$V_{DDD\ L,\ R}$; note 6	50	-	-	dB
P_{SSR2}	power supply rejection ratio	V_{DDD}; note 6	50	-	-	dB
P_{SSR3}	power supply rejection ratio	$V_{SSD\ L,\ R}$; note 6	60	-	-	dB
P_{SSR4}	power supply rejection ratio	V_{SSD}; note 6	50	-	-	dB
P_{SSR5}	power supply rejection ratio	V_{DDA}; note 6	60	-	-	dB
P_{SSR6}	power supply rejection ratio	V_{SSA}; note 6	60	-	-	dB
P_{tot}	total power dissipation		-	800	-	mW
Clock - Input						
V_{IL}	input voltage LOW		-	-	0.5	V
V_{IH}	input voltage HIGH		4.5	-	-	V
I_{IL}	input current LOW	V_i = 0.5 V	−10	-	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Clock - Input						
I_{IH}	input current HIGH	V_i = 4.5 V	−10	-	10	µA
C_i	clock input capacitance		-	5	-	pF
f_{CLK}	clock input frequency		-	-	10	MHz
Channel left/right inputs						
V_{IL}	input voltage LOW		-	-	0.5	V
V_{IH}	input voltage HIGH		-	4.5	-	V
I_{IL}	input current LOW	V_i = 0.5 V	−10	-	10	µA
I_{IH}	input current HIGH	V_i = 4.5 V	−10	-	10	µA
C_i	channel input capacitance; pins 3, 30		-	5	-	pF
V_{ref}	reference input voltage; pins 8, 25	note 2	-	−4 ±0.4	-	V
Audio outputs						
$V_{OUT(RMS)}$	output voltage (RMS value); pins 14, 19; pins 15, 18	notes 2 and 3	0.85	1.0	1.15	V
(THD + N)/S	THD + Noise; 0 dB	f = 1 kHz; notes 3 and 4	-	−101	−96	dB
			-	0.0009	0.0016	%
(THD + N)/S	THD + Noise; 0 dB	20 Hz - 20 kHz; notes 3 and 5	-	−101	-	dB
			-	0.0009	-	%
(THD + N)/S	THD + Noise; −20 dB	f = 1 kHz; notes 3 and 4	-	−88	−84	dB
(THD + N)/S	THD + Noise; −60 dB	f = 1 kHz; notes 3 and 4	-	−48	−44	dB
S/N	signal-to-noise ratio	pattern 0101; notes 3 and 7	109	111	-	dB
S/N	signal-to-noise ratio; "A"-weighting	pattern 0101; notes 3 and 7	-	113	-	dB
α	channel separation	f = 1 kHz	101	115	-	dB
Timing						
t_r	rise time clock input	C_L = 20 pF	-	5	10	ns
t_f	fall time clock input	C_L = 20 pF	-	5	10	ns
$t_{CLK\ L}$	clock input LOW time		45	-	-	ns
$t_{CLK\ H}$	clock input HIGH time		45	-	-	ns
t_r	channel input rise time	C_L = 20 pF	-	10	15	ns
t_f	channel input fall time	C_L = 20 pF	-	10	15	ns
t_{HD}	channel input hold time		25	-	-	ns
t_{SU}	channel input set-up time		0	-	-	ns

Notes to the characteristics

1. The substrate voltage must be lower than or to equal than the lowest supply voltage.
2. Output level tracks linearly with both the clock frequency and the reference voltage ($V_{ref\ L}$ or $V_{ref\ R}$).
3. Device measured in differential mode with external components as shown in Fig.5.
4. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 1 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
5. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 20 Hz to 20 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
6. Power supply rejection ratio measured with f_{ripple} = 1 kHz and V_{ripple} = 100 mV.
7. The specified signal-to-noise ratio includes noise introduced by the application components as shown in Fig.5.

TIMING

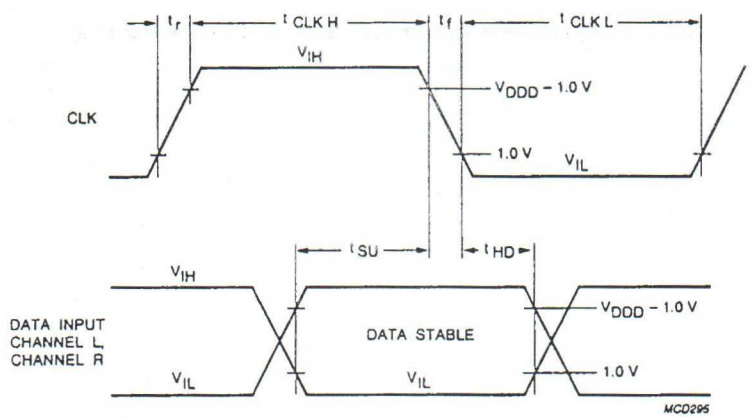


Fig.3 Timing waveform.

APPLICATION INFORMATION

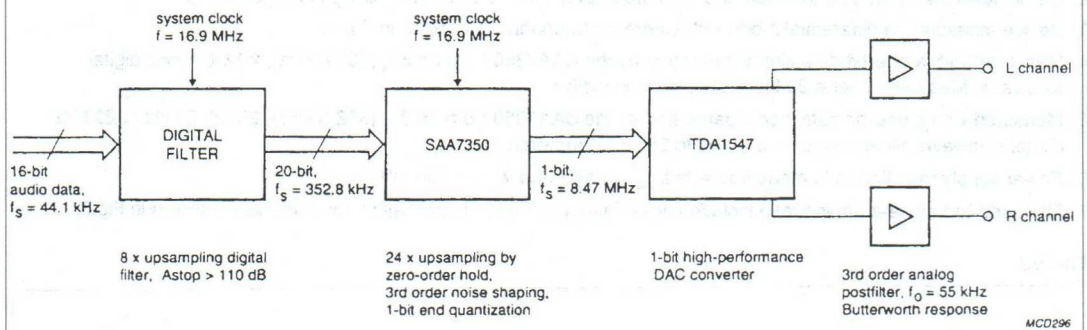


Fig.4 CD-range bitstream reconstruction system (192 f_s over-sampling).

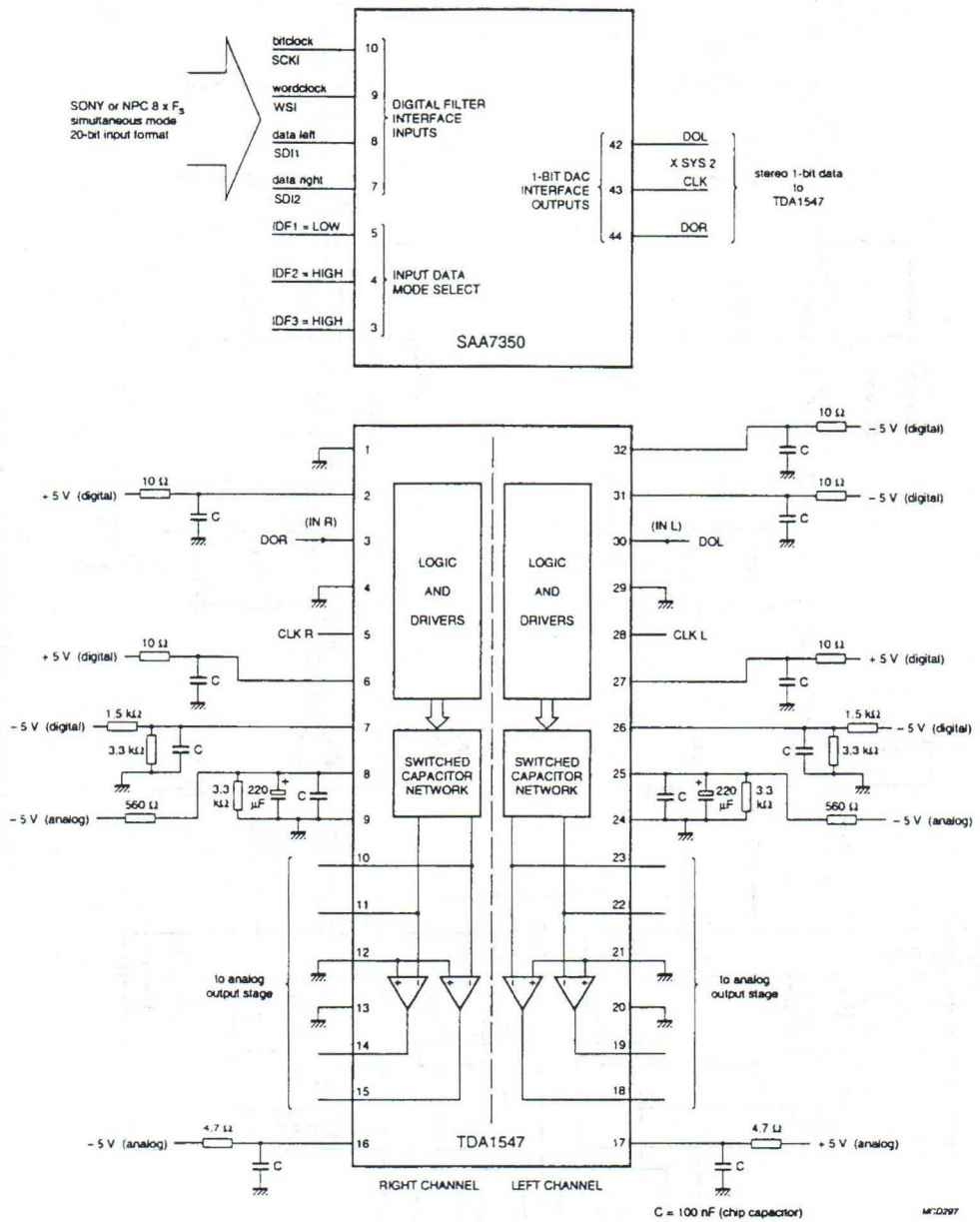


Fig.5 Application diagram.

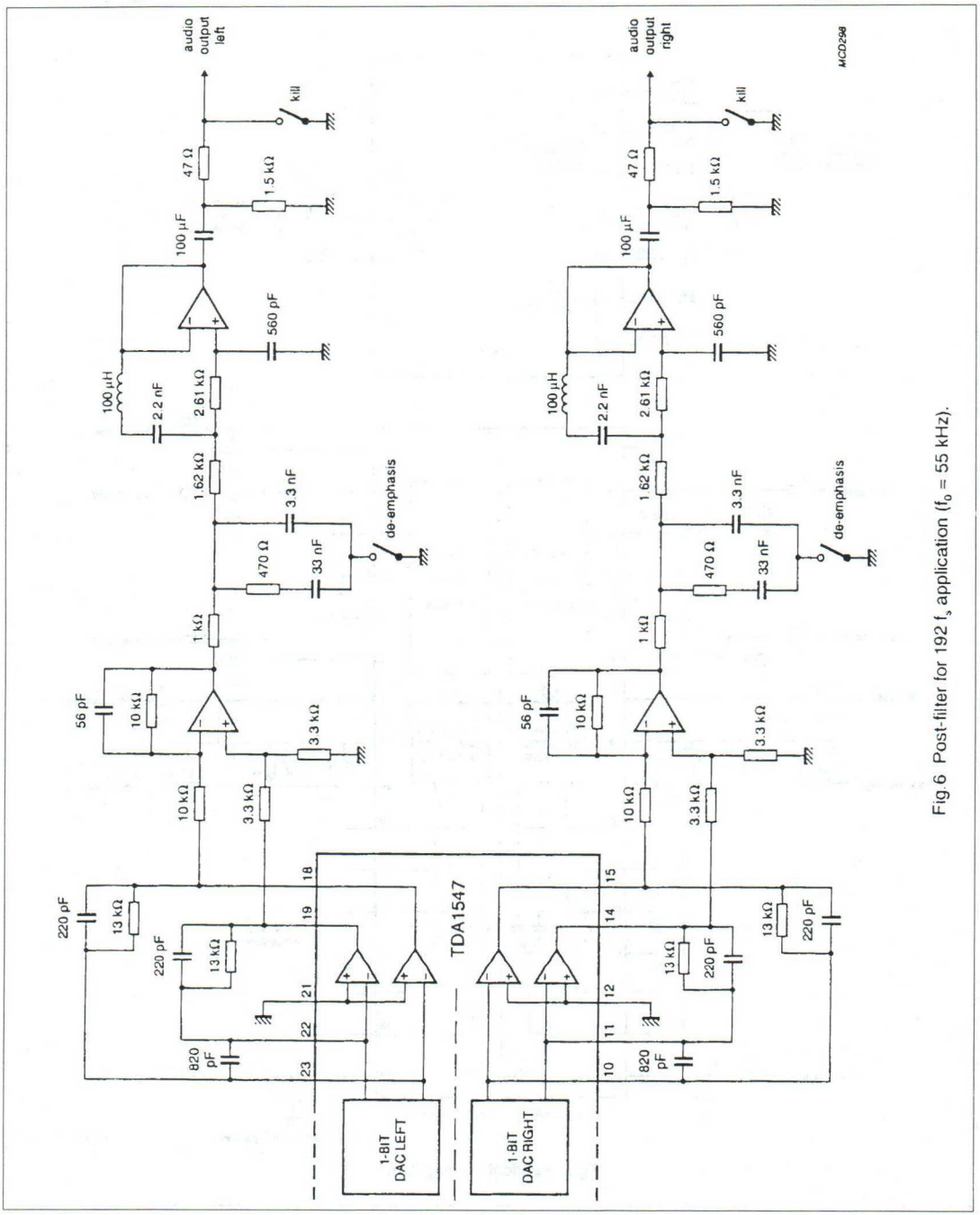


Fig.6 Post-filter for 192 f_s application (f_o = 55 kHz).

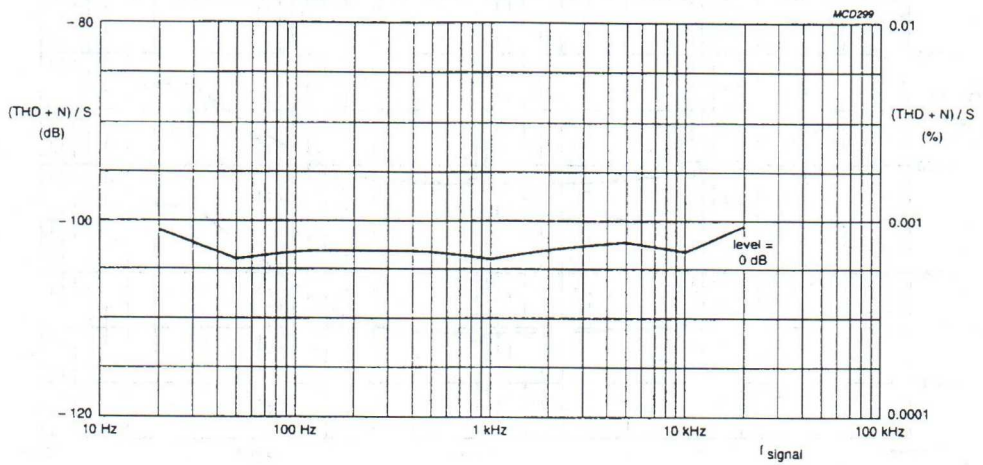


Fig.7 (THD + N)/S as a function of signal frequency.

Note : Graph constructed from average measurements values of a small amount of engineering samples. No guarantee for typical values is implied.

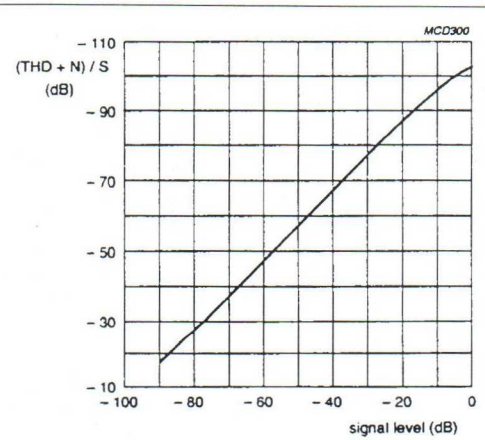


Fig.8 (THD + N)/S as a function of test signal level.

Note : Graph constructed from average measurement values of a small amount of engineering samples. No guarantee for typical values is implied.

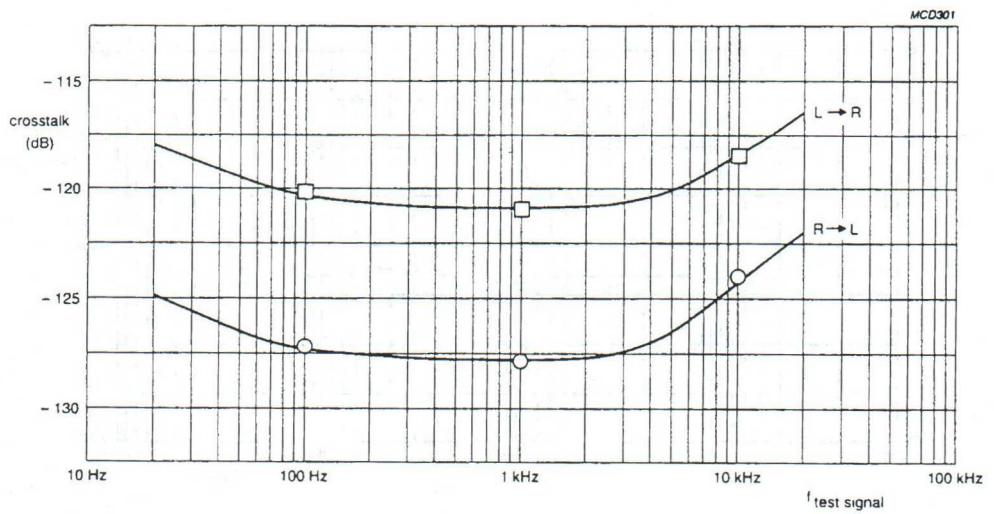


Fig.9 Inter-channel crosstalk as a function of signal frequency.

Note : Graph constructed from average measurements values of a small amount of engineering samples. No guarantee for typical values is implied.

Octuple 6-bit DAC with I²C-bus — TDA8444/AT/T

GENERAL DESCRIPTION

The TDA8444/AT/T comprises eight digital-to-analog converters (DSCs), each controlled via the two-wire I²C-bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$. At power-on all DAC outputs are set to their lowest value. The I²C-bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

FEATURES

- Eight discrete DACs
- I²C-bus slave receiver
- 16-pin DIL package
  16-pin SO package
  20-pin SO package

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	Supply voltage		4.5	12.0	13.2	V
I_{CC}	Supply current	no loads; $V_{max} = V_P$; all data = 00	0	12	15	mA
P_{tot}	Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	–	150	–	mW
V_{max}	Effective range of V_{max} input	V_P = 12V	1	–	10.5	V
V_O	DAC output voltage range		0.1	–	V_P–0.5	V
V_{LSB}	Step value of 1 LSB	$V_{max} = V_P$; I_O = –2mA	70	160	250	mV

PACKAGE OUTLINES

TDA8444 16-lead DIL; plastic (SOT38)
TDA8444T 16-lead SO; plastic (SOT-162)
TDA8444AT 20-lead SO; (SOT-163)

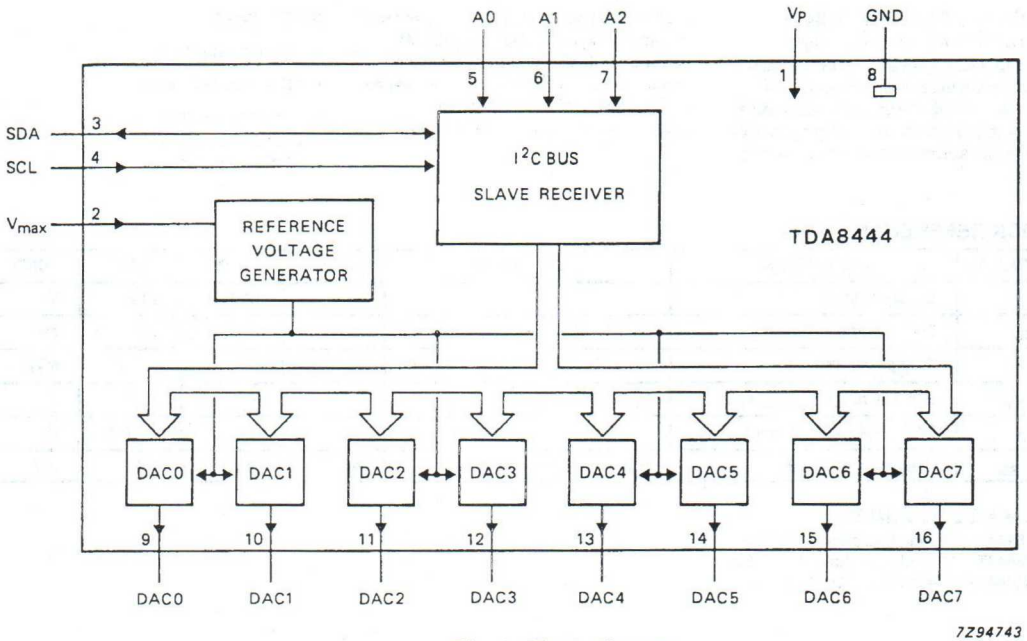


Fig. 1 Block diagram.

PINNING

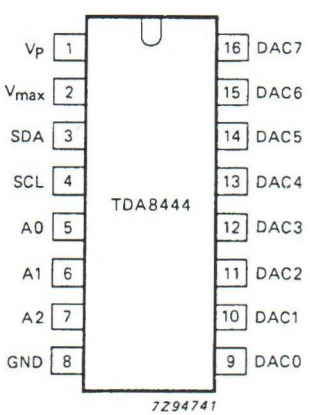
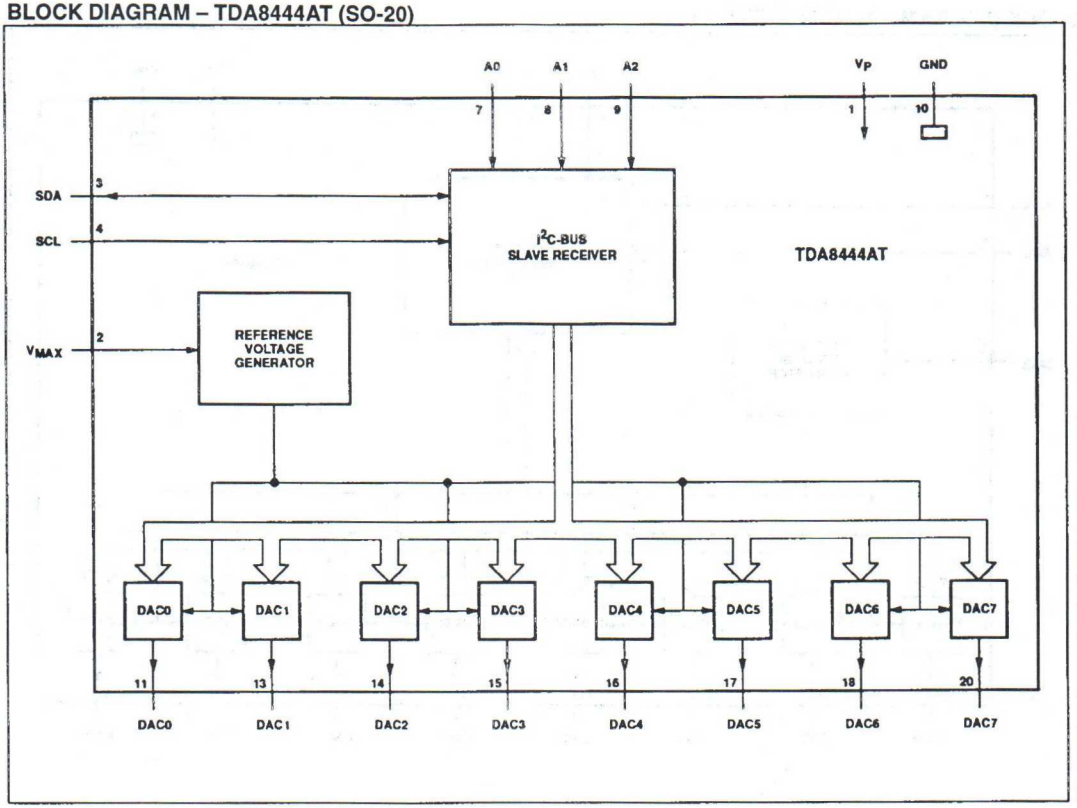


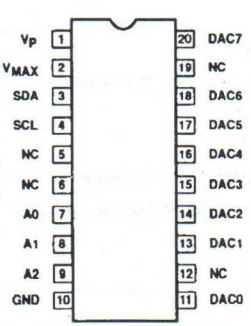
Fig. 2 Pinning diagram.

1	V_P	positive supply voltage
2	V_{max}	control input for DAC maximum output voltage
3	SDA	I²C-bus serial data input/output
4	SCL	I²C-bus serial data clock
5	A0	programmable address bits for I²C-bus slave receiver
6	A1	
7	A2	
8	GND	ground
9-16	DAC0-7	analogue voltage outputs

BLOCK DIAGRAM – TDA8444AT (SO-20)

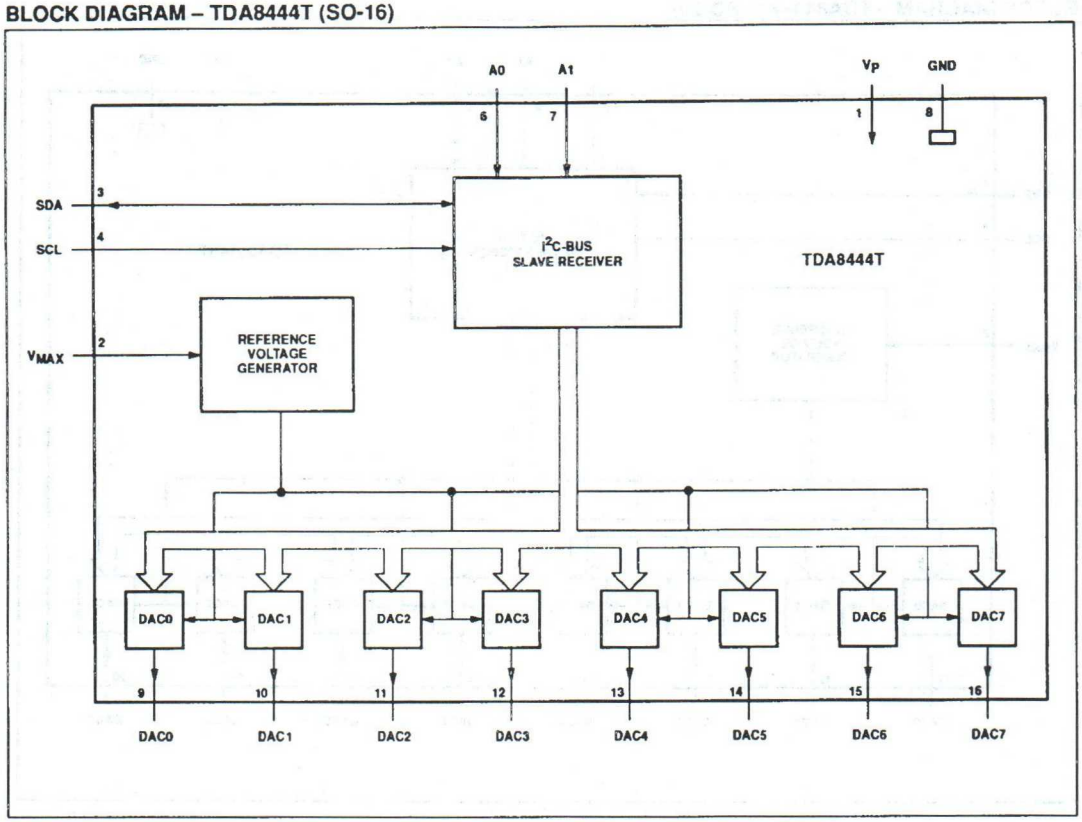


PIN CONFIGURATION AND DESCRIPTION – TDA8444AT (SO-20, SOT-163)

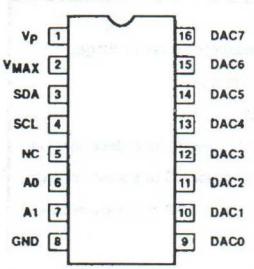


1	V_P	Positive supply voltage
2	V_{MAX}	Control input for DAC maximum output voltage
3	SDA	I²C bus serial data input/output
4	SCL	I²C bus serial data clock
7	A0	Programmable address bits for I²C bus slave receiver
8	A1	Programmable address bits for I²C bus slave receiver
9	A2	Programmable address bits for I²C bus slave receiver
10	GND	Ground
11, 13-18, 20	DAC0-7	Analog voltage outputs

BLOCK DIAGRAM – TDA8444T (SO-16)



PIN CONFIGURATION AND DESCRIPTION – TDA8444T (SO-16, SOT-162)



1	V_P	Positive supply voltage
2	V_{MAX}	Control input for DAC maximum output voltage
3	SDA	I²C bus serial data input/output
4	SCL	I²C bus serial data clock
6	A0	Programmable address bits for I²C bus slave receiver
7	A1	Programmable address bits for I²C bus slave receiver
8	GND	Ground
9-16	DAC0-7	Analog voltage outputs

FUNCTIONAL DESCRIPTION

I²C-bus

The TDA8444 I²C-bus interface is a receive-only slave. Data is accepted from the I²C-bus in the following format:

S	0 1 0 0 A2 A1 A0 0	A	I3 I2 I1 I0 SD SC SB SA	A	X X D5 D4 D3 D2 D1 D0	A	P
	← address byte →		← instruction byte →		← first data byte →		

Where:

S	= start condition	A2, A1, A0	= programmable address bits
P	= stop condition	I3, I2, I1, I0	= instruction bits
A	= acknowledge	SD, SC, SB, SA	= subaddress bits
X	= don't care	D5, D4, D3, D2, D1, D0	= data bits

Fig. 3 Data format.

Address byte

Valid addresses are 40, 42, 44, 46, 48, 4A, 4C, 4E (hexadec), depending on the programming of bits A2, A1 and A0. With these addresses, up to eight TDA8444 ICs can be operated independently from one I²C-bus. No other addresses are acknowledged by the TDA8444.

Instruction and data bytes

Valid instructions are 00 to 0F and F0 to FF (hexadec); the TDA8444 will not respond to other instruction values.

Instructions 00 to 0F cause auto-incrementing of the subaddress (bits SD to SA) when more than one data byte is sent within one transmission. With auto-incrementing, the first data byte is written into the DAC addressed by bits SD to SA and then the subaddress is automatically incremented by one position for the next data byte in the series.

Auto-incrementation does not occur with instructions F0 to FF. Other than auto-incrementation there is no difference between instructions 00 to 0F and F0 to FF. When only one data byte per transmission is present, the DAC addressed by the subaddress will always receive the data.

Valid subaddresses (bits SD to SA) are 0 to 7 (hexadec) relating numerically to DAC0 to DAC7. When the auto-incrementing function is used, the subaddress will sequence through all possible values (0 to F, 0 to F, etc.).

I²C-bus

Input SCL (pin 3) and input/output SDA (pin 4) conform to I²C-bus specifications.* Pins 3 and 4 are protected against positive voltage pulses by internal zener diodes connected to the ground plane and therefore the normal bus line voltage should not exceed 5.5 V.

The address inputs A0, A1, A2 are programmed by a connection to GND for An = 0 or to V_P for An = 1. If the inputs are left floating, An = 1 will result.

FUNCTIONAL DESCRIPTION (continued)

Input V_{max}

Input V_{max} (pin 2) provides a means of compressing the output voltage swing of the DACs. The maximum DAC output voltage is restricted to approximately V_{max} while the 6-bit resolution is maintained, so giving a finer voltage resolution of smaller output swings.

Digital-to-analogue converters

Each DAC comprises a 6-bit data latch, current switches and an output driver. Current sources with values weighted by 2^0 up to 2^5 are switched according to the data input so that the sum of the selected currents gives the required analogue voltage from the output driver. The range of the output voltage is approximately 0.5 to 10.5 V when $V_{max} = V_P$.

The DAC outputs are protected against short-circuits to V_P and GND.

To avoid the possibility of oscillations, capacitive loading at the DAC outputs should not exceed 2 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		$V_P = V_1$	−0.5	18	V
Supply current (source)		$I_P = I_1$	−	−10	mA
		$I_P = I_I$	−	40	mA
I²C-bus line voltage		$V_{3,4}$	−0.5	5.9	V
Input voltage		V_I	−0.5	V_P + 0.5	V
Output voltage		V_O	−0.5	V_P + 0.5	V
Maximum current on any pin (except pins 1 and 8)		$\pm I_{max}$	−	10	mA
Total power dissipation		P_{tot}	−	500	mW
Operating ambient temperature range		T_{amb}	−20	+ 70	°C
Storage temperature range		T_{stg}	−65	+ 150	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	75 K/W

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS

All voltages are with respect to GND; T_{amb} = 25 °C; V_P = 12 V unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	4.5	12.0	13.2	V
Voltage level for power-on reset		V_1	1	–	4.8	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	$I_P = I_1$	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input (pin 2)	V_P = 12 V	$V_{max} = V_2$	1.0	–	10.5	V
Pin 2 current	V_2 = 1 V	I_2	–	–	−10	μA
	$V_2 = V_P$	I_2	–	–	10	μA
SDA, SCL inputs (pins 3 and 4)						
Input voltage range		V_I	0	–	5.5	V
Input voltage LOW		V_{IL}	–	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	–	V
Input current LOW	$V_{3;4}$ = 0.3 V	I_{IL}	–	–	−10	μA
Input current HIGH	$V_{3;4}$ = 6 V	I_{IH}	–	–	±10	μA
SDA output (pin 3)						
Output voltage LOW	I_3 = 3 mA	V_{OL}	–	–	0.4	V
Sink current		I_O	3	8	–	mA
Address inputs (pins 5 to 7)						
Input voltage range		V_I	0	–	V_P	V
Input voltage LOW		V_{IL}	–	–	1	V
Input voltage HIGH		V_{IH}	2.1	–	–	V
Input current LOW		I_{IL}	–	−7	−12	μA
Input current HIGH		I_{IH}	–	–	1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
DAC outputs (pins 9 to 16)						
Output voltage range		V_O	0.1	–	V_P–0.5	V
Minimum output voltage	data = 00; I_O = –2 mA	V_{Omin}	0.1	0.4	0.8	V
Maximum output voltage	data = 3F; I_O = –2 mA					
at $V_{max} = V_P$		V_{Omax}	10	10.5	11.5	V
at $1 < V_{max} < 10.5$ V		V_{Omax}		see note		V
Output sink current	V = V_P; data = 1F	I_O	2	8	15	mA
Output source current	V = 0V; data = 1F	I_O	–2	–	–6	mA
Output impedance	data = 1F; $-2 < I_O < +2$ mA	Z_O	–	4	50	Ω
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV
Deviation from linearity	I_O = –2 mA; N ≠ 32		0	–	50	mV
Deviation from linearity	I_O = –2 mA; N = 32		0	–	70	mV

Note to the characteristics

$V_O = 0.95\ V_{max} + V_{Omin}$.

APPLICATION INFORMATION

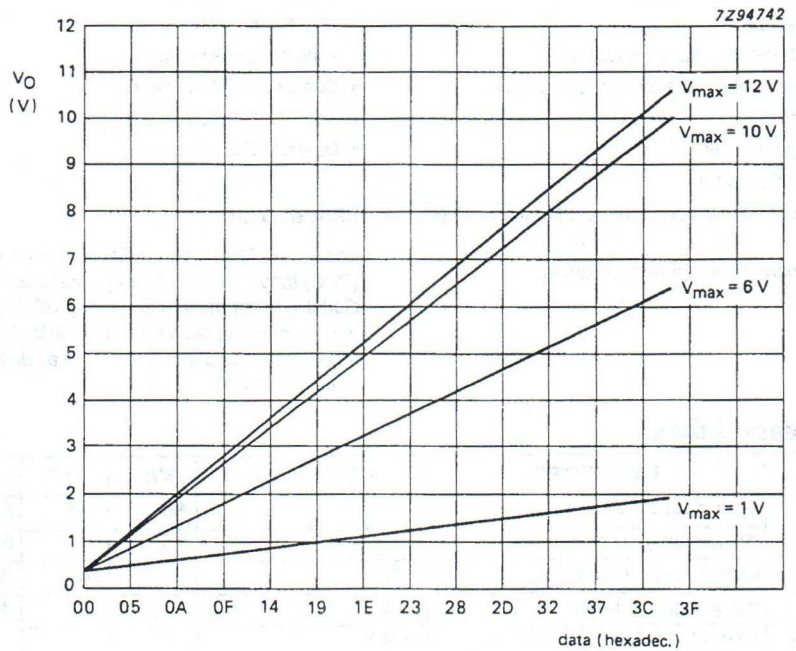


Fig. 4 Graph showing output voltage as a function of the input data value for V_{max} values of 1, 6, 10 and 12 V; V_P = 12 V.

8-bit video digital-to-analog converter — TDA8702

FEATURES

- 8-bit resolution
- Conversion rate up to 30 MHz
- TTL input levels
- Internal reference voltage generator
- Two complementary analog voltage outputs
- No deglitching circuit required
- Internal input register
- Low power dissipation
- Internal 75 Ω output load (connected to the analog supply)
- Very few external components required.

APPLICATIONS

- High-speed digital-to-analog conversion
- Digital TV including:
  - field progressive scan
  - line progressive scan
- Subscriber TV decoders
- Satellite TV decoders
- Digital VCRs.

DESCRIPTION

The TDA8702 is an 8-bit digital-to-analog converter (DAC) for video and other applications. It converts the digital input signal into an analog voltage output at a maximum conversion rate of 30 MHz. No external reference voltage is required and all digital inputs are TTL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	–	26	32	mA
I_{CCD}	digital supply current	note 1	–	23	30	mA
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltage (peak-to-peak value)	note 2				
		Z_L = 10 kΩ	−1.45	−1.60	−1.75	V
		Z_L = 75 kΩ	−0.72	−0.80	−0.88	V
ILE	DC integral linearity error		–	–	±1/2	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
f_{CLK}	maximum conversion rate		–	–	30	MHz
B	−3 dB analog bandwidth	f_{CLK} = 30 MHz; note 3	–	150	–	MHz
P_{tot}	total power dissipation		–	250	340	mW

Notes

1. D0 to D7 connected to V_{CCD} and CLK connected to DGND.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The −3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8702	16	DIL	plastic	SOT38
TDA8702T	16	SO16	plastic	SOT162A

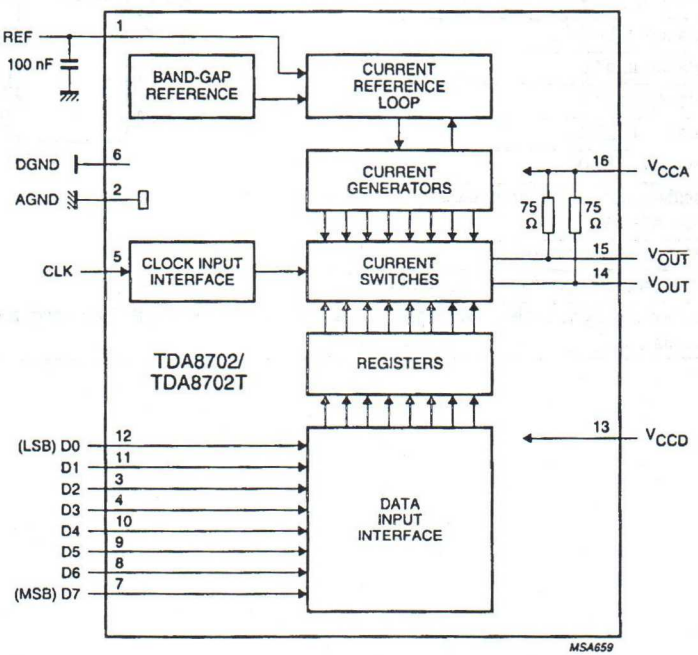


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
REF	1	voltage reference (decoupling)
AGND	2	analog ground
D2	3	data input; bit 2
D3	4	data input; bit 3
CLK	5	clock input
DGND	6	digital ground
D7	7	data input; bit 7
D6	8	data input; bit 6
D5	9	data input; bit 5
D4	10	data input; bit 4
D1	11	data input; bit 1
D0	12	data input; bit 0
V_{CCD}	13	positive supply voltage for digital circuits (+5 V)
V_{OUT}	14	analog voltage output
$V_{\overline{OUT}}$	15	complementary analog voltage output
V_{CCA}	16	positive supply voltage for analog circuits (+5 V)

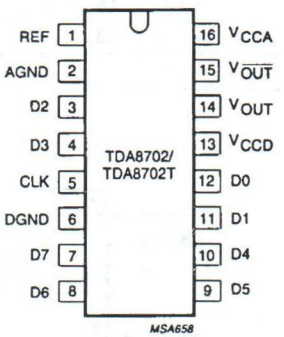


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	−0.3	+7.0	V
V_{CCD}	digital supply voltage	−0.3	+7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differential	−0.5	+0.5	V
AGND − DGND	ground voltage differential	−0.1	+0.1	V
V_I	input voltage (pins 3 to 5 and 7 to 12)	−0.3	V_{CCD}	V
$I_{OUT}/\overline{I_{OUT}}$	total output current (pins 14 and 15)	−5	+26	mA
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambienttemperature	0	+70	°C
T_j	junction temperature	−	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT38	70 K/W
	SOT162A	90 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{CCA} = V_{16} - V_2 = 4.5$ V to 5.5 V; $V_{CCD} = V_{13} - V_6 = 4.5$ V to 5.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; V_{REF} decoupled to AGND by a 100 nF capacitor; $T_{amb} = 0$ °C to +70 °C; AGND and DGND shorted together; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = 5$ V and $T_{amb} = 25$ °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	–	26	32	mA
I_{CCD}	digital supply current	note 1	–	23	30	mA
AGND – DGND	ground voltage differential		−0.1	–	+0.1	V
Inputs						
DIGITAL INPUTS (D7 TO D0) AND CLOCK INPUT (CLK)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–	−0.3	−0.4	mA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	0.01	20	µA
f_{CLK}	maximum clock frequency		–	–	30	MHz
Outputs (note 2; referenced to V_{CCA})						
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltages (peak-to-peak value)	$Z_L = 10$ kΩ	−1.45	−1.60	−1.75	V
		$Z_L = 75$ Ω	−0.72	−0.80	−0.88	V
V_{OS}	analog offset output voltage	code = 0	–	−3	−25	mV
V_{OUT}/TC	full-scale analog output voltage temperature coefficient		–	–	200	µV/K
V_{OS}/TC	analog offset output voltage temperature coefficient		–	–	20	µV/K
B	−3 dB analog bandwidth	note 3; $f_{CLK} = 30$ MHz	–	150	–	MHz
G_{diff}	differential gain		–	0.6	–	%
Φ_{diff}	differential phase		–	1	–	deg
Z_O	output impedance		–	75	–	Ω
Transfer function ($f_{CLK} = 30$ MHz)						
ILE	DC integral linearity error		–	–	±1/2	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB

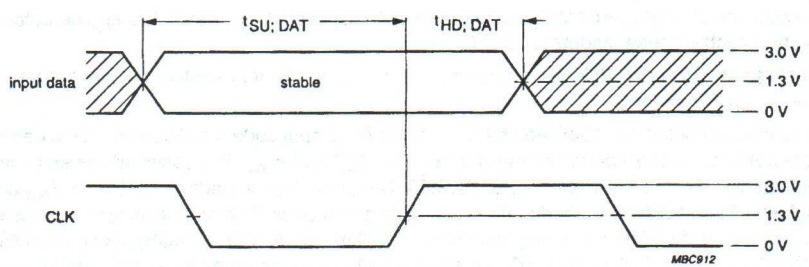
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics (f_{CLK} = 30 MHz; notes 4 and 5; see Figs 3, 4 and 5)						
$t_{SU;DAT}$	data set-up time		−0.3	–	–	ns
$t_{HD;DAT}$	data hold time		2.0	–	–	ns
t_{PD}	propagation delay time		–	–	1.0	ns
t_{S1}	settling time	10% to 90% full-scale change to ±1 LSB	–	1.1	1.5	ns
t_{S2}	settling time	10% to 90% full-scale change to ±1 LSB	–	6.5	8.0	ns
t_d	input to 50% output delay time		–	3.0	5.0	ns
Output transients (glitches; (f_{CLK} = 30 MHz; note 6; see Fig.6)						
E_g	glitch energy from code	transition 127 to 128	–	–	30	LSB.ns

Notes

1. D0 to D7 are connected to V_{CCD}, CLK is connected to DGND.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$ are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is 75 Ω (typ.).
3. The −3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).
4. The worst case characteristics are obtained at the transition from input code 0 to 255 and if an external load impedance greater than 75 Ω is connected between V_{OUT} or $V_{\overline{OUT}}$ and V_{CCA}. The specified values have been measured with an active probe between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data is latched at the rising edge of the clock. The output voltage remains stable (independent of input data variations) during the HIGH level of the clock (CLK = HIGH). During a LOW-to-HIGH transition of the clock (CLK = LOW), the DAC operates in the transparent mode (input data will be directly transferred to their corresponding analog output voltages (see Fig.5).
5. The data set-up ($t_{SU;DAT}$) is the minimum period preceding the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising edge of the clock and still be recognized. The data hold time ($t_{HD;DAT}$) is the minimum period following the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising edge of the clock and still be recognized.
6. The definition of glitch energy and the measurement set-up are shown in Fig.6. The glitch energy is measured at the input transition between code 127 to 128 and on the falling edge of the clock.

Table 1 Input coding and output voltages (typical values; referenced to V_{CCA}, regardless of the offset voltage).

CODE	INPUT DATA (D7 to D0)	DAC OUTPUT VOLTAGES			
		Z_L = 10 kΩ		Z_L = 75 Ω	
		V_{OUT}	$V_{\overline{OUT}}$	V_{OUT}	$V_{\overline{OUT}}$
0	000 00 00	0	−1.6	0	−0.8
1	000 000 01	−0.006	−1.594	−0.003	−0.797
	.....				
128	100 000 00	−0.8	−0.8	−0.4	−0.4
	.....				
254	111 111 10	−1.594	−0.006	−0.797	−0.003
255	111 111 11	−1.6	0	−0.8	0



The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns after the first rising edge of the clock ($t_{SU;DAT}$ is negative; −0.3 ns). Data must be held at least 2 ns after the rising edge ($t_{HD;DAT}$ = +2 ns).

Fig.3 Data set-up and hold times.

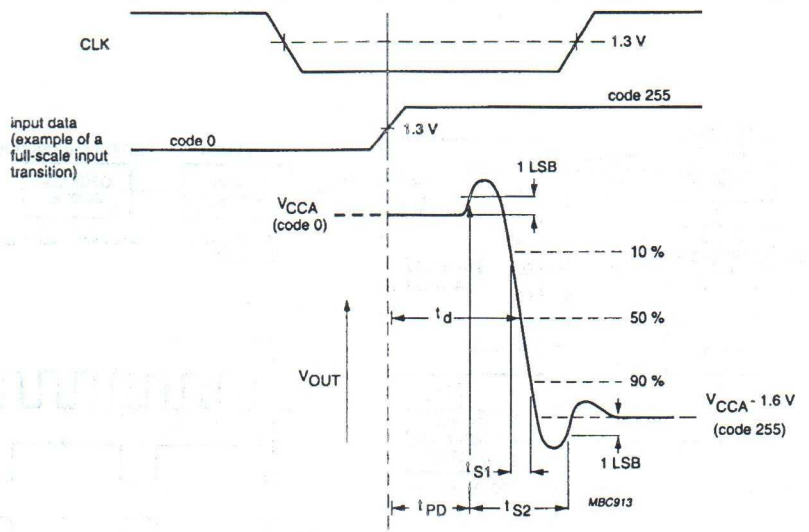
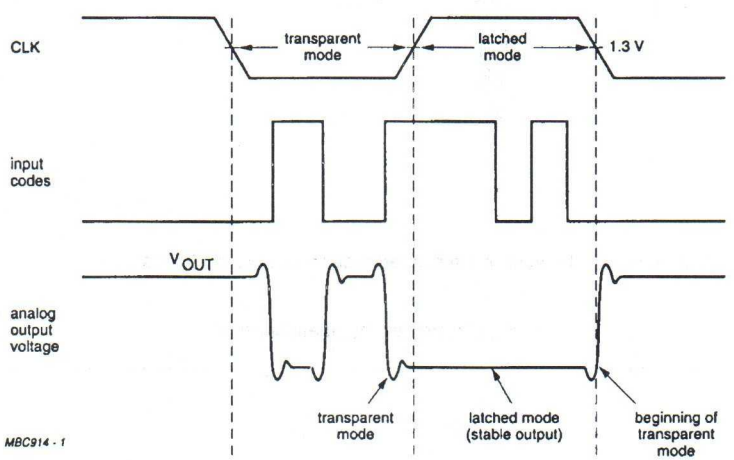
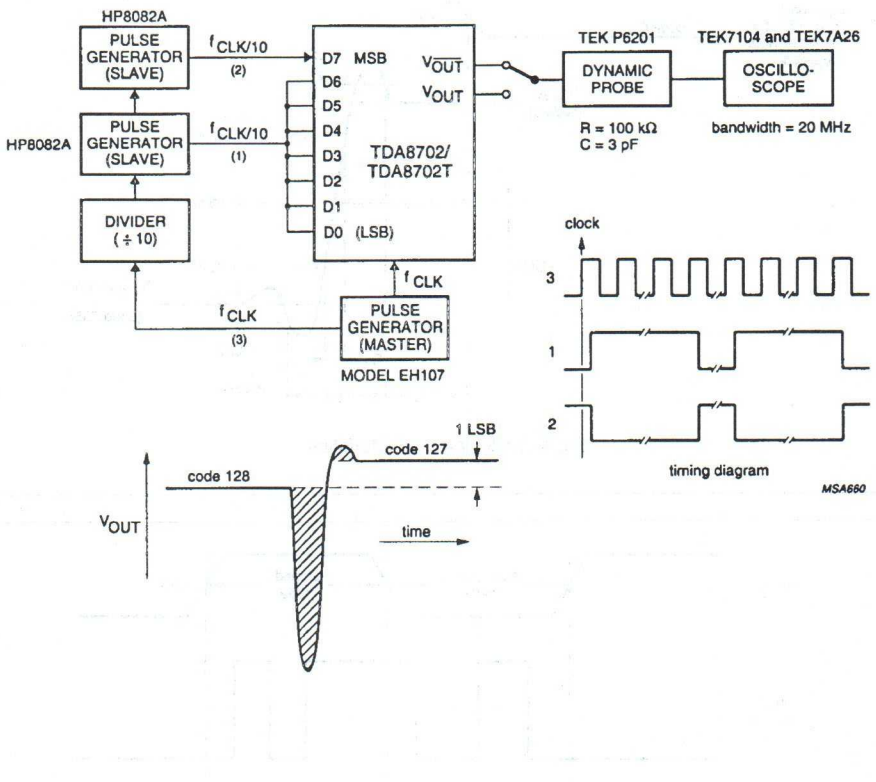


Fig.4 Switching characteristics.



During the transparent mode (CLK = LOW), any change of input data will be seen at the output. During the latched mode (CLK = HIGH), the analog output remains stable regardless of any change at the input. A change of input data during the latched mode will be seen on the falling edge of the clock (beginning of the transparent mode).

Fig.5 Latched and transparent mode.



The value of the glitch energy is the sum of the shaded area measured in LSB.ns.

Fig.6 Glitch energy measurement.

INTERNAL PIN CONFIGURATIONS

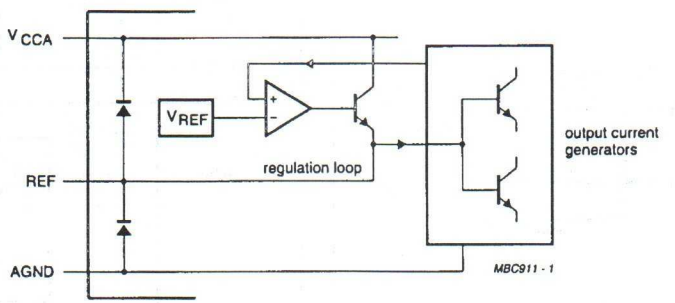


Fig.7 Reference voltage generator decoupling.

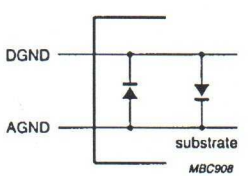


Fig.8 AGND and DGND.

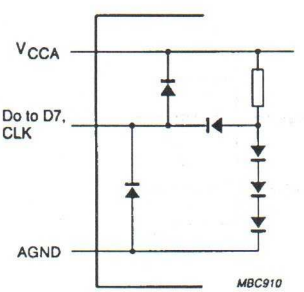


Fig.9 D7 to D0 and CLK.

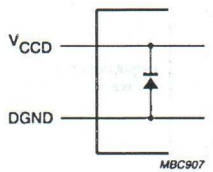


Fig.10 Digital supply.

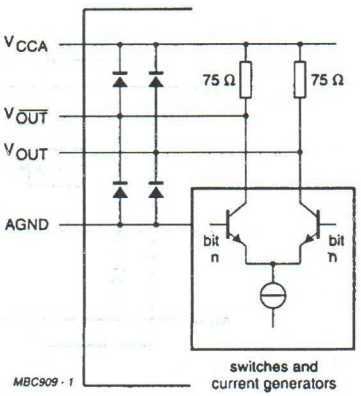


Fig.11 Analog outputs.

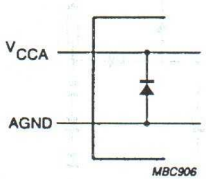
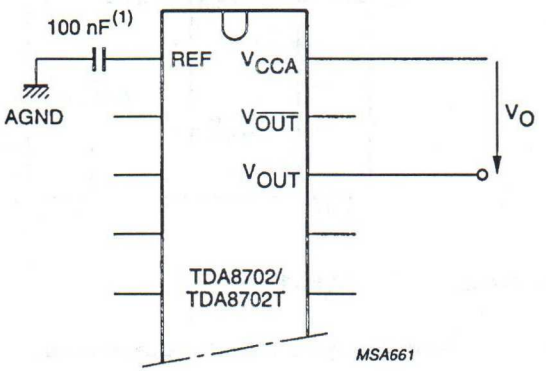


Fig.12 Analog supply.

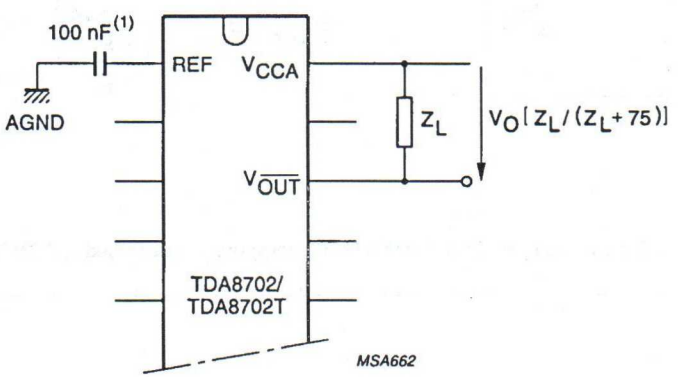
APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).



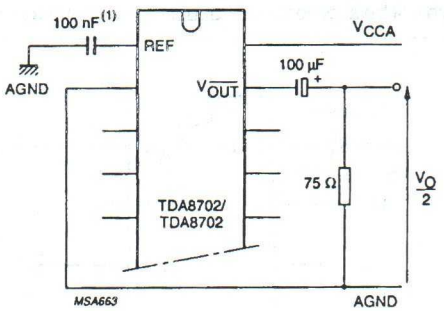
(1) This is a recommended value for decoupling pin 1.

Fig.13 Analog output voltage without external load ($V_O = -V_{\overline{OUT}}$; see Table 1, Z_L = 10 kΩ).



(1) This is a recommended value for decoupling pin 1.

Fig.14 Analog output voltage with external load (external load Z_L = 75 Ω to ∞).



(1) This is a recommended value for decoupling pin 1.

Fig.15 Analog output with AGND as reference.

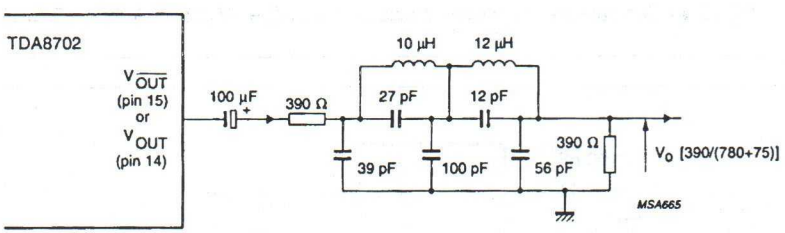
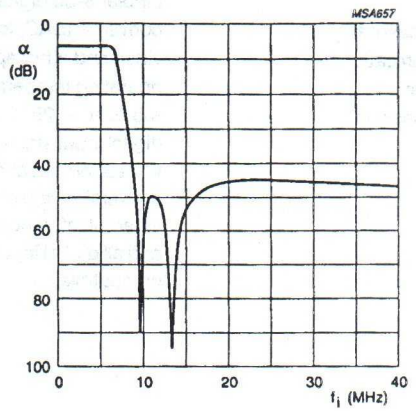


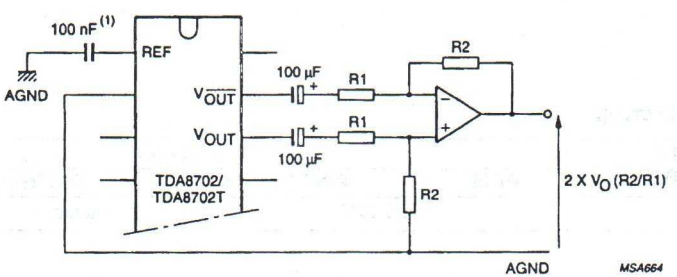
Fig.16 Example of anti-aliasing filter (analog output referenced to AGND).



Characteristics

- Order 5; adapted CHEBYSHEV
- Ripple at ≤ 0.1 dB
- $f_{(-3\ dB)}$ = 6.7 MHz
- $f_{(NOTCH)}$ = 9.7 MHz and 13.3 MHz

Fig.17 Frequency response for filter shown in Fig.16.



(1) This is a recommended value for decoupling pin 1.

Fig.18 Differential mode (improved supply voltage ripple rejection).

8-bit video digital-to-analog converter (Mil. temp.) TDE8712D

FEATURES

- 8-bit resolution
- Conversion rate up to 50 MHz
- TTL input levels
- Internal reference voltage generator
- Two complementary analog voltage outputs
- No deglitching circuit required
- Internal input register
- Low power dissipation (250 mW typical)
- Internal 75 Ω output load (connected to the analog supply)
- Very few external components required.

APPLICATIONS

- High-speed digital-to-analog conversion
- Test and measurement
- Telecommunications
- Radar/sonar
- Image processing

DESCRIPTION

The TDE8712D is a monolithic bipolar 8-bit digital-to-analog converter (DAC) for professional video and other applications. The operating temperature range is -55 °C to +125 °C. It converts the digital input signal into an analog voltage output at a maximum conversion rate of 50 MHz. No external reference voltage is required and all digital inputs are TTL compatible.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDE8712D	16	CERDIP	ceramic	SOT74

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current	note 1	20	26	32	mA
I_{CCD}	digital supply current	note 1	16	23	30	mA
V_{OUT} – $\overline{V_{OUT}}$	full-scale analog output voltage (peak-to-peak value)	Z_L = 10 kΩ	–1.45	–1.60	–1.75	V
		Z_L = 75 Ω	–0.72	–0.80	–0.88	V
ILE	DC integral linearity error		-	-	±1/2	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
f_{CLK}	maximum conversion rate		50	-	-	MHz
B	–3 dB bandwidth	f_{CLK} = 50 MHz	-	150	-	MHz
P_{tot}	total power dissipation		-	250	340	mW

Notes to the Quick Reference Data

1. D0 to D7 connected to V_{CCD} and CLK connected to DGND.

2. The analog output voltages (V_{OUT} and $\overline{V_{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.

3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

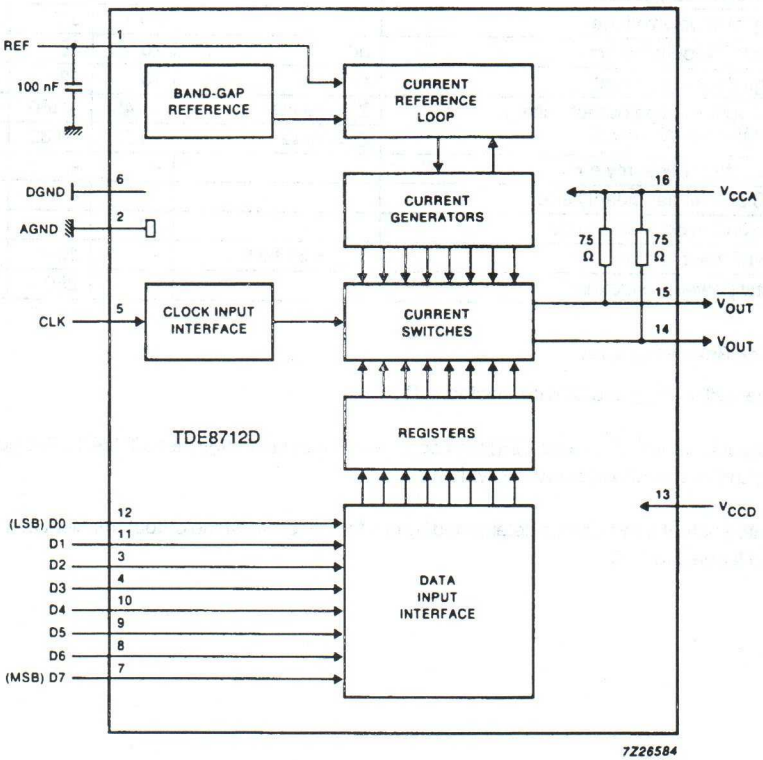


Fig.1 Block diagram.

PIN CONFIGURATION

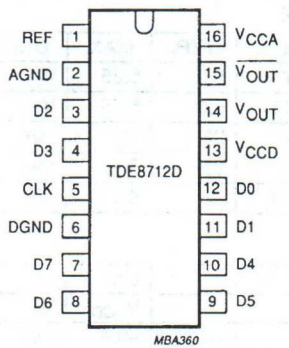


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
REF	1	voltage reference (decoupling)
AGND	2	analog ground
D2	3	data input, bit 2
D3	4	data input, bit 3
CLK	5	clock input
DGND	6	digital ground
D7	7	data input, bit 7
D6	8	data input, bit 6
D5	9	data input, bit 5
D4	10	data input, bit 4
D1	11	data input, bit 1
D0	12	data input, bit 0
V_{CCD}	13	positive supply voltage for digital circuits (+5 V)
V_{OUT}	14	analog voltage output
$\overline{V_{OUT}}$	15	complementary analog voltage output
V_{CCA}	16	positive supply voltage for analog circuits (+5 V)

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	−0.3	+ 7.0	V
V_{CCD}	digital supply voltage range	−0.3	+ 7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differential	−0.5	+ 0.5	V
AGND – DGND	ground voltage differential	−0.1	+ 0.1	V
V_I	input voltage range (pins 3 to 5 and 7 to 12)	−0.3	V_{CCD}	V
I_{OUT}	total output current range (pin 14)	−5	+ 26	mA
$\overline{I_{OUT}}$	total output current range (pin 15)	−5	+ 26	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−55	+125	°C
T_j	junction temperature	-	+175	°C

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT74	112	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{CCA} = V_{16} - V_2 = 4.75$ V to 5.25 V; $V_{CCD} = V_{13} - V_6 = 4.75$ V to 5.25 V; $V_{CCA} - V_{CCD} = -0.25$ V to +0.25 V; V_{REF} decoupled to AGND by a 100 nF capacitor; $T_{amb} = -55$ °C to +125 °C; AGND and DGND shorted together; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = 5.0$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current	note 1	20	26	32	mA
I_{CCD}	digital supply current	note 1	16	23	30	mA
AGND – DGND	ground voltage differential		–0.1	-	0.1	V
Inputs DIGITAL INPUTS (D7 - D0) AND CLOCK INPUT (CLK)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_I = 0.4$ V	-	–0.3	–0.4	mA
I_{IH}	input current HIGH	$V_I = 2.7$ V	-	0.01	20	µA
f_{CLK}	maximum clock frequency		50	-	-	MHz
Outputs (note 2; referenced to V_{CCA})						
$V_{OUT} - \overline{V_{OUT}}$	full-scale analog output voltages (peak- to-peak value)	$Z_L = 10$ kΩ	–1.45	–1.61	–1.75	V
		$Z_L = 75$ Ω	–0.72	–0.80	–0.88	V
V_{offset}	analog offset output voltage	code = 0	-	–3	–25	mV
ΔV_{OUT}	full-scale analog output voltage temperature coefficient		-	-	200	µV/K
ΔV_{offset}	analog offset output voltage temperature coefficient		-	-	20	µV/k
B	–3 dB bandwidth	note 3; $f_{CLK} = 50$ MHz	-	150	-	MHz
G_d	differential gain		-	0.6	-	%
ϕd	differential phase		-	1	-	deg
Z_o	output impedance		-	75	-	Ω
Transfer function ($f_{CLK} = 50$ MHz)						
ILE	DC integral linearity error		-	-	±1/2	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
Switching characteristics (fCLK = 50 MHz; notes 4 and 5; see Figs 3,4 and 5)						
$t_{SU;DAT}$	data set-up time		–0.3	-	-	ns
$t_{HD;DAT}$	data hold time		2	-	-	ns
t_{PD}	propagation delay time		-	-	1.0	ns
t_{S1}	settling time	10% to 90% full-scale change to ±1 LSB	-	1.1	1.5	ns
t_{S2}	settling time	10% to 90% full-scale change to ±1 LSB	-	6.5	8.0	ns
t_d	input to 50% output delay time		-	3.0	5.0	ns
Output transients (glitches; $f_{CLK} = 50$ MHz; note 6; see Fig.6)						
E_g	glitch energy from code	transition 127 to 128	-	-	30	ns

Notes to the characteristics

1. D0 to D7 connected to V_{CCD}, CLK connected to DGND.

2. The analog output voltages (V_{OUT} and $\overline{V_{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.

3. The −3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

4. The worst case characteristics are obtained at the transition from input code 0 to 255 and if an external load impedance greater than 75 Ω is connected between V_{OUT} or $\overline{V_{OUT}}$ and V_{CCA}. The specified values have been measured with an active probe between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data are latched at the rising-edge of the clock. The output voltage remains stable (independent of input data variations) during the high level of the clock (CLK = HIGH). During LOW-to-HIGH transition of the clock (CLK = LOW), the DAC operates in the transparent mode (input data will be directly transferred to their corresponding analog output voltages, see Fig.5).

5. The data set-up ($t_{SU;DAT}$) is the minimum period preceding the rising-edge of the clock, that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising-edge of the clock and still be recognized. The data hold time ($t_{HD;DAT}$) is the minimum period following the rising-edge of the clock, that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising-edge of the clock and still be recognized.

6. The definition of glitch energy and the measurement set-up are shown in Fig.6. The glitch energy is measured at the input transition between code 127 to 128 and on the falling-edge of the clock.

Table 1 Input coding and output voltages (typical values; referenced to V_{CCA}, regardless of offset voltage)

DAC OUTPUT VOLTAGES					
CODE	BINARY INPUT DATA (D7 - D0)	Z_L = 10 kΩ	Z_L = 75 Ω		
		$\overline{V_{OUT}}$ (V)	V_{OUT} (V)	$\overline{V_{OUT}}$ (V)	V_{OUT} (V)
0	000 000 00	0	−1.6	0	−0.8
1	000 000 01	−0.006	−1.594	−0.003	−0.797
.	. . . . .	.	.	.	.
128	100 000 00	−0.8	−0.8	−0.4	−0.4
.	. . . . .	.	.	.	.
254	111 111 10	−1.594	−0.006	−0.797	−0.003
255	111 111 11	−1.6	0	−0.8	0

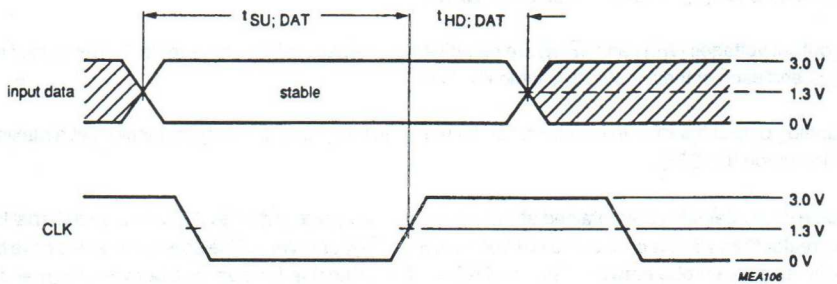


Fig.3 Data set-up and hold times.

Note to Fig.3

The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns, after the first rising-edge of the clock ($t_{SU;\,DAT}$ is negative; −0.3 ns). Data must be held at least 2 ns after the rising-edge ($t_{HD;\,DAT}$ = +2 ns).

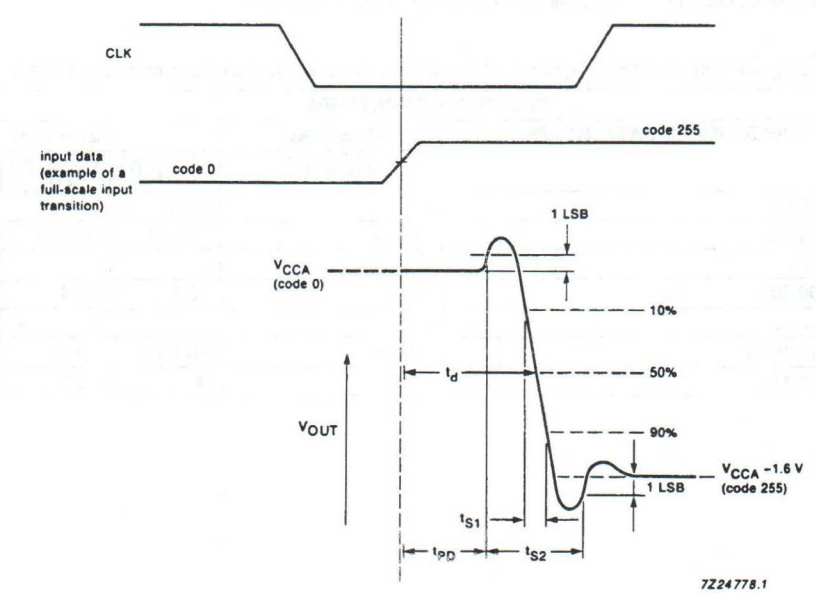


Fig.4 Switching characteristics.

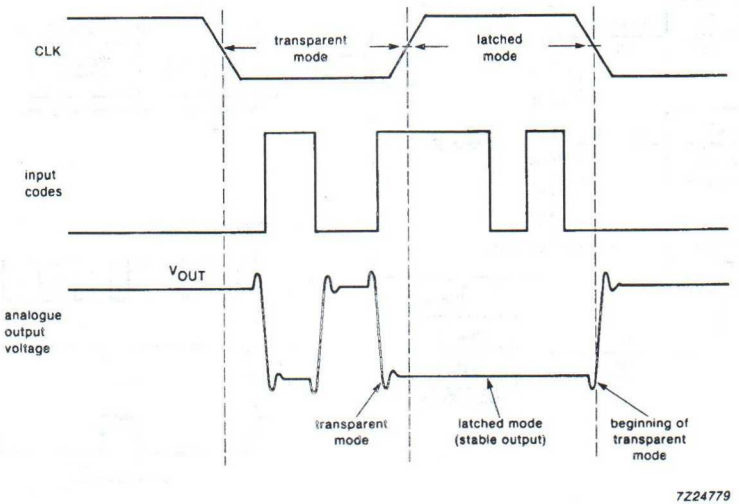


Fig.5 Latched and transparent mode.

Note to Fig.5

During the transparent mode (CLK = LOW), any change of input data will be seen at the output. During the latched mode (CLK = HIGH), the analog output remains stable, regardless of any changes at the input. A change of input data during the latched mode will be seen on the falling-edge of the clock (beginning of the transparent mode).

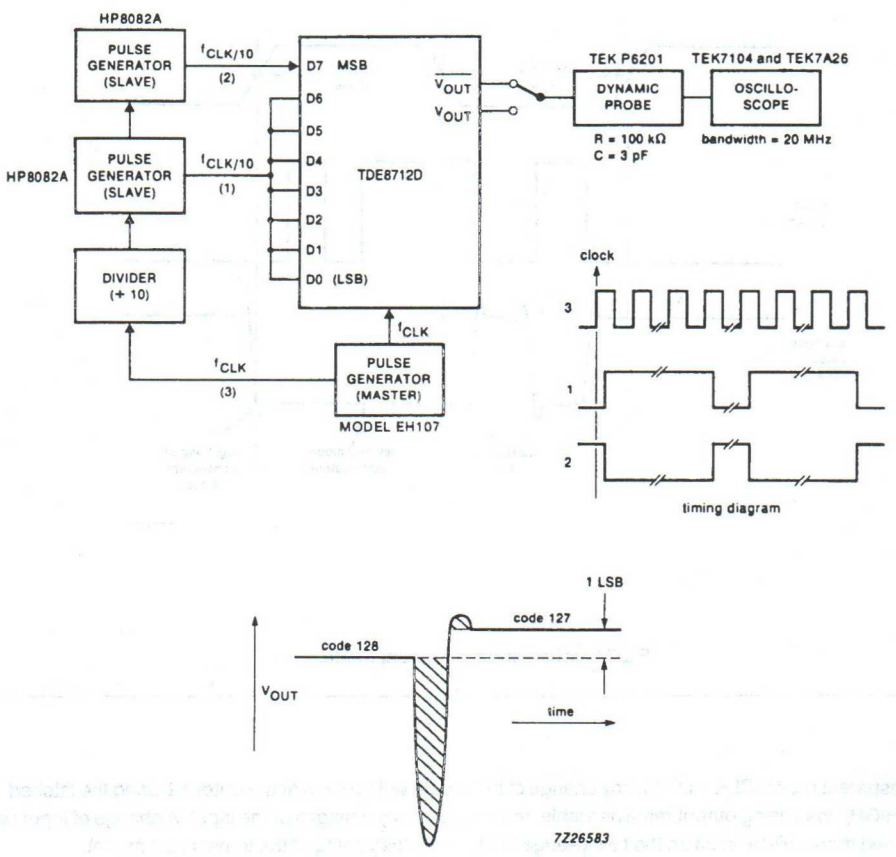


Fig.6 Glitch energy measurement.

Note to Fig.6

The value of the glitch energy is the sum of the shaded area measured in LSB.ns.

INTERNAL PIN CONFIGURATIONS

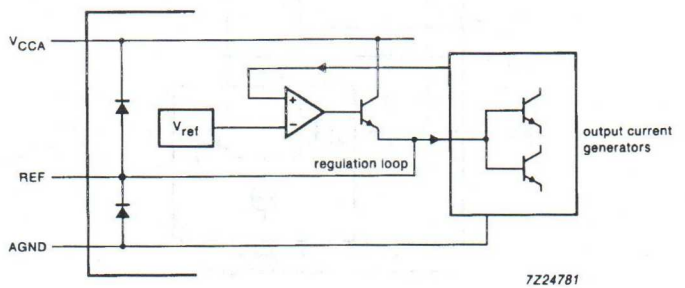


Fig.7 Reference voltage generator decoupling.

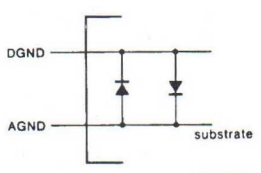


Fig.8 AGND and DGND.

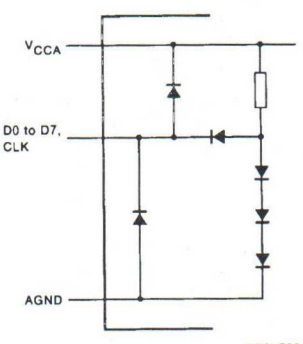


Fig.9 D7 to D0 and CLK.

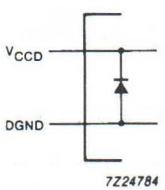


Fig.10 Digital supply.

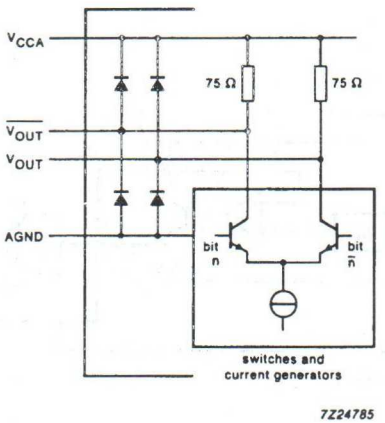


Fig.11 Analog outputs.

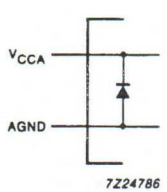


Fig.12 Analog supply.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).

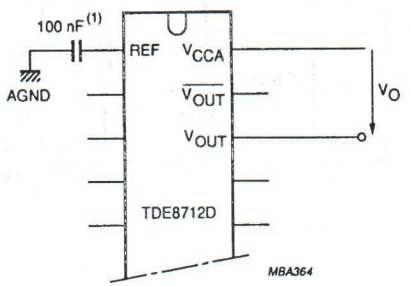


Fig.13 Analog output voltage without external load ($V_O = -\overline{V_{OUT}}$; see Table 1, Z_L = 10 kΩ).

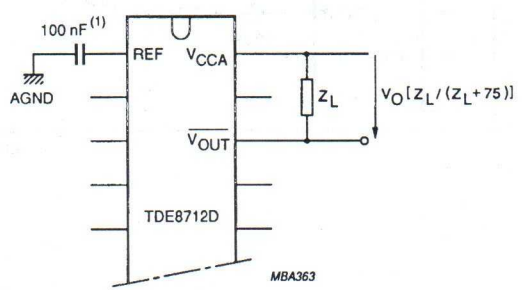


Fig.14 Analog output voltage with external load (external load Z_L = 75 Ω to ∞).

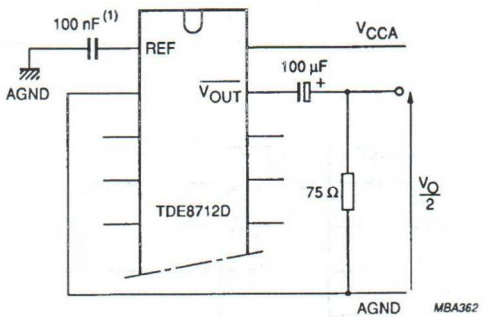


Fig.15 Analog output with AGND as reference.

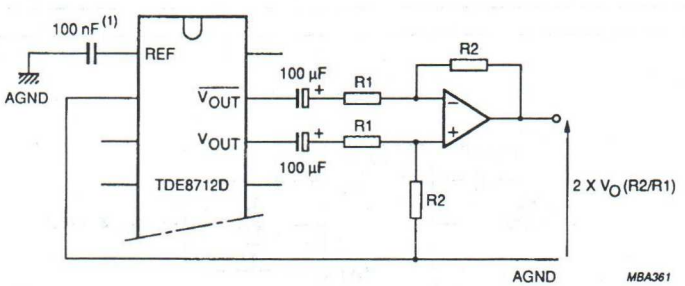


Fig.16 Differential mode (improved supply voltage ripple rejection).

Notes to Figs 13, 14, 15 and 16

1. This is a recommended value for decoupling pin 1.

Section 12
Sample-and-Hold

INDEX

Symbols and definitions for sample-and-hold circuits		877
LF198/LF298/LF398	Sample-and-hold amplifiers	879
NE/SE5537	Sample-and-hold amplifier	884
TDA1535B	High-speed single sample-and-hold amplifier	892

Symbols and definitions for sample-and-hold circuits

General Purpose/Linear ICs

Acquisition Time (t_{AQ})
The time delay between the 50% (or threshold) point of the hold-to-sample transition of the sample/hold signal and the point at which the output voltage begins to track the input voltage to within a specified error band. By convention the acquisition time is defined for sampling positive (or negative) full-scale input voltage after previously holding a negative (or positive) full-scale output voltage.

Aperture Delay (t_{APD})
The time delay between the 50% (or threshold) point of the hold-to-sample transition of the sample/hold signal and the instant at which the switch is just opening. This latter instant can be defined as the time at which the internal control voltage across the switch element has moved by 10% of its full voltage swing, i.e., the instant at which the switch is 10% open.

Aperture Time (t_{AP})
The time required for the sample-and-hold switch to open. The switch opening time can be defined as the interval between the conditions of 10% open and 90% open and does not include any delays of the sample/hold signal through the switch buffer circuitry.

Aperture Uncertainty (t_{APU})
The range of variation of total aperture delay time (see definition below) due to internal circuit noise of all forms.

Charge Transfer (Q_T)
The amount of charge transferred to the holding capacitor (when switching from the sample-to-hold mode) originating from stray or parasitic capacitance associated with the sample-and-hold switch. Charge transfer is directly related to hold step (see definition below) by the following relationship:

$V_{HS}(V)$ = Charge transfer (pC)/C_H(pF)

where V_{HS} is the hold step and C_H is the holding capacitor. It can be seen that increasing C_H will reduce V_{HS}, since the charge transfer is constant for a given circuit.

Input Resistance (R_{IN})
The large-signal input resistance over the specified input voltage range.

Droop Rate (dV_H/dt)
The rate of change of output voltage while the circuit is in the hold mode. It is due to leakage currents to, or from, the holding capacitor and can be positive or negative. It is related to the droop current, I_D (defined below), by the following relationship:

$dV_H/dt = I_D(pA)/C_H(pF)$

Droop Current (I_D)
The current flowing *into* the C_H terminal when the circuit is in the hold mode.

Effective Aperture Delay Time (t_{EAPD})
The difference between the propagation time of the analog input voltage to the sample-and-hold switch and the aperture delay (t_{APD}). The value of t_{EAPD} may be positive, negative or zero. For precise timing of the point on the input voltage to be held, the sample-to-hold transition of the sample/hold signal must be advanced by t_{EAPD}.

Feedthrough Attenuation
A measurement of the isolation of the analog switch when the amplifier is in the HOLD mode. A direct function of feedthrough capacitance, it is the ratio of the output signal level to input signal level when in the HOLD mode. Feedthrough Attenuation is specified at a specific frequency and is usually expressed in dB.

Full Power Bandwidth (f_P)
The maximum frequency at which the full-scale output voltage can be achieved without significant distortion. The full power bandwidth is related to the slew rate, SR (defined below) by the following relationship:

$F_P = SR/2\pi V_{CC}$

where V_{CC} is the peak value of the input signal; i.e., $V_{IN} = V_{CC}\sin(2\pi Fpt)$.

Gain Error
In a unity gain configuration this is the ratio of the difference between the input and output voltages to the input voltage expressed as a percentage of full scale input range capability.

Hold Mode Feedthrough
A measure of the amount of an input sinusoidal voltage that appears at the output of a sample-and-hold circuit when it is in the hold mode. It is usually expressed as a percentage or as an output RMS voltage for a specified input RMS voltage.

Hold Mode Settling Time (t_{HM})
The time delay between the 50% (or threshold) point of the sample-to-hold transition of the sample/hold signal and the point at which the output settles to within a specified error band of its final value before hold mode droop becomes significant.

Hold Step (V_{HS})
The step in the output voltage caused by charge transfer (defined above).

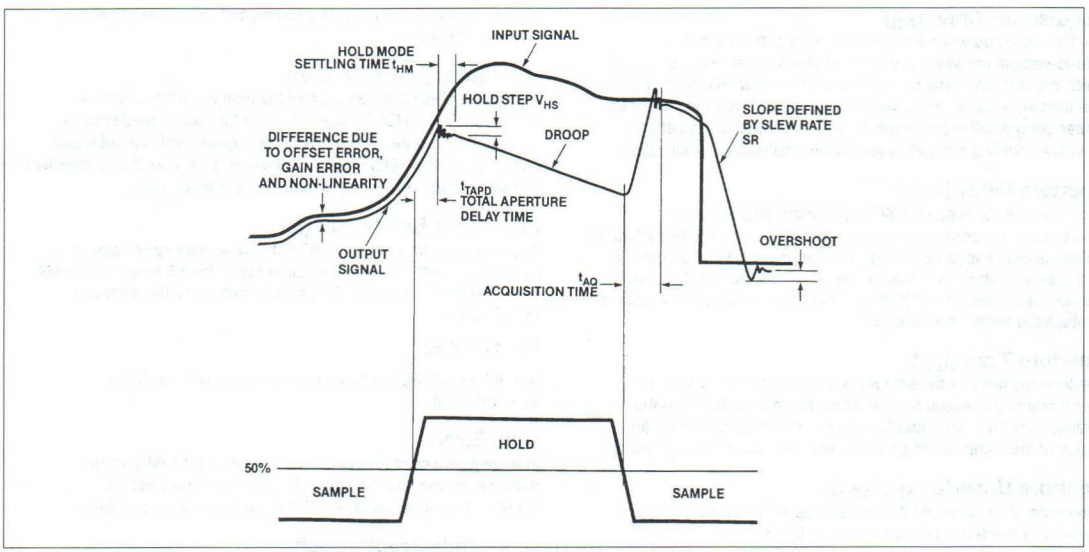
Input Bias Current (I_{BIAS})
The bias current *into* the input terminal.

Linearity Error (E_L)
The maximum deviation of the output voltage from an ideal straight line drawn between the two output voltages corresponding to the extremes of the input voltage range. It is usually expressed as a percentage of the full-scale input voltage range.

Output Resistance (R_O)
The ratio of the change in output voltage to a change in output load current in either the hold mode or for a fixed input voltage in the sample mode.

Overshoot
The maximum overshoot of the output voltage, in the sample mode, when slewing at its maximum rate over the full-scale output voltage range. It is usually expressed as a percentage of the full-scale output voltage range.

Symbols and definitions for sample-and-hold circuits



Power Supply Rejection Ratio (PSRR)

The ratio of the change in power supply voltage (over a specified power supply voltage range DPSV) to the corresponding change in zero-scale error, V_{ZS} (defined below); it is expressed in dB where $PSRR(dB) = 20\log(\Delta PSV/\Delta V_{ZS})$.

Slew Rate (SR)

The maximum possible rate of change of the output voltage, in the sample mode, when changing over the full-scale output voltage range.

Total Aperture Delay Time (t_{TAPD})

The sum of the aperture delay and the aperture time.

$$t_{TAPD} = t_{APD} + t_{AP}$$

Voltage Gain (A_V)

The ratio of the output voltage to the input voltage when operating in the sample mode and over a specified input voltage range.

Zero-Scale Error (V_{ZS}) or Input Offset Voltage (V_{OS})

The difference between the output and input voltages when operating in the sample mode and in a unity gain configuration.

Sample-and-hold amplifiers

LF198/LF298/LF398

DESCRIPTION

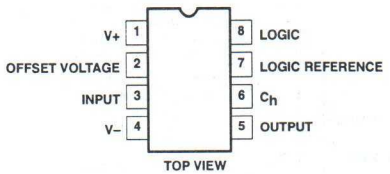
The LF198/LF298/LF398 are monolithic sample-and-hold circuits which utilize high-voltage ion-implant JFET technology to obtain ultra-high DC accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, DC gain accuracy is 0.002% typical and acquisition time is as low as 6μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FETs are combined with bipolar devices in the output amplifier to give droop rates as low as 5mV/min with a 1μF hold capacitor. The JFETs have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feedthrough from input to output in the hold mode even for input signals equal to the supply voltages.

Logic inputs are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS; differential threshold is 1.4V. The LF198/LF298/LF398 will operate from ±5V to ±18V supplies. They are available in 8-pin plastic DIP, 8-pin Cerdip, and 14-pin plastic SO packages.

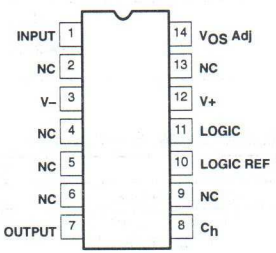
PIN CONFIGURATIONS

FE, N Packages



TOP VIEW

D[1] Package



TOP VIEW

NOTE:
1. SO and non-standard pinouts.

FEATURES

- Operates from ±5V to ±18V supplies
- Less than 10μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5mV typical hold step at CH=0.01μF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

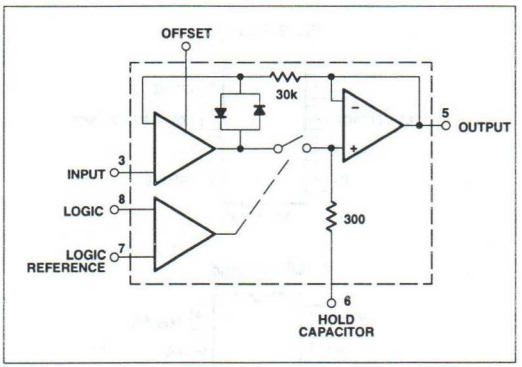
APPLICATION

- The LF198/LF298/LF398 are ideally suited for a wide variety of sample-and-hold applications, including data acquisition, analog-to-digital conversion, synchronous demodulation, and automatic test setup

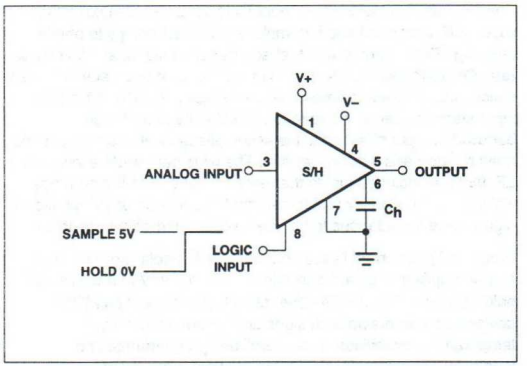
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	LF198FE	0580A
14-Pin Plastic Small Outline (SO) Package	0 to +70°C	LF398D	0175D
8-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	LF398FE	0580A
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	LF398N	0404B
8-Pin Ceramic Dual In-Line Package (CERDIP)	-25°C to +85°C	LF298FE	0580A
8-Pin Plastic Dual In-Line Package (DIP)	-25°C to +85°C	LF298N	0404B

FUNCTIONAL DIAGRAM



TYPICAL APPLICATIONS



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±18	V
	Maximum power dissipation T_A=25°C (still-air)[3]		
	F package	780	mW
	N package	1160	mW
	D package	1040	mW
T_A	Operating ambient temperature range		
	LF198	-55 to +125	°C
	LF298	-25 to +85	°C
	LF398	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
V_{IN}	Input voltage	Equal to supply voltage	
	Logic-to-logic reference differential voltage[2]	+7, -30	V
	Output short-circuit duration	Indefinite	
	Hold capacitor short-circuit duration	10	sec
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. The maximum junction temperature of the LF398 is 150°C. When operating at elevated ambient temperature, the packages must be derated based on the thermal resistance specified.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.
3. Derate above 25°C, at the following rates:
   F package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 8.3mW/°C

DC ELECTRICAL CHARACTERISTICS

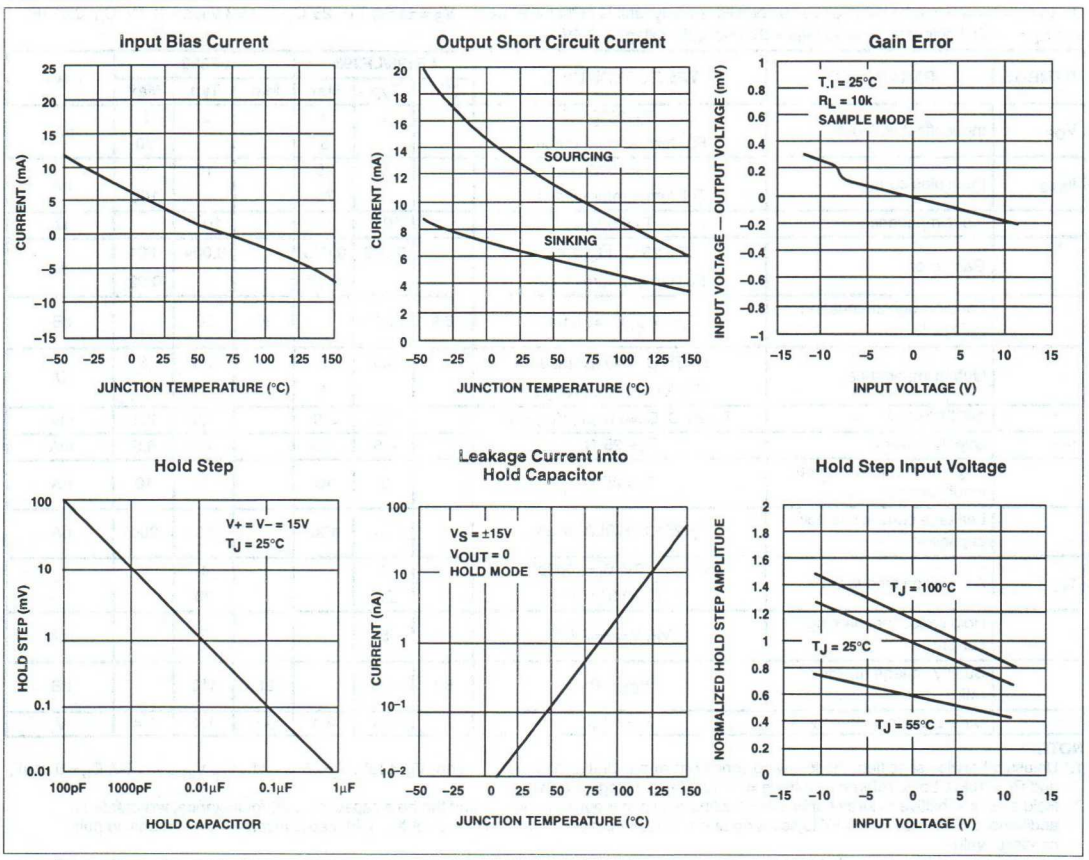
Unless otherwise specified, the following conditions apply: unit is in "sample" mode; $V_S = \pm 15V$; $T_J = 25°C$; -11.5V3 $V_{IN} \leq +11.5V$; $C_H = 0.01\mu F$; and $R_L = 10k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.

SYMBOL	PARAMETER	TEST CONDITIONS	LF198/LF298			LF398			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[4]	$T_J=25°C$ Full temperature range		1	3 5		2	7 10	mV
I_{BIAS}	Input bias current[4]	$T_J=25°C$ Full temperature range		5	25 75		10	50 100	nA
	Input impedance	$T_J=25°C$		10^{10}			10^{10}		Ω
	Gain error	$T_J=25°C$, $R_L=10k$ Full temperature range		0.002	0.005 0.02		0.004	0.01 0.02	%
	Feedthrough attenuation ratio at 1kHz	$T_J=25°C$, $C_h=0.01\mu F$	86	96		80	90		dB
	Output impedance	$T_J=25°C$, "HOLD" mode Full temperature range		0.5	2 4		0.5	4 6	Ω
	"HOLD" step[2]	$T_J=25°C$, $C_h=0.01\mu F$, $V_{OUT}=0$		0.5	2.0		1.0	2.5	mV
I_{CC}	Supply current[4]	$T_J \leq 25°C$		4.5	5.5		4.5	6.5	mA
	Logic and logic reference input current	$T_J = 25°C$		2	10		2	10	μA
	Leakage current into hold capacitor[4]	$T_J=25°C$, "HOLD" mode		30	100		30	200	pA
t_{AC}	Acquisition time to 0.1%	$\Delta V_{OUT}=10V$, $C_h=1000pF$ $C_h=0.01\mu F$		4 20			4 20		μs
	Hold capacitor charging current	$V_{IN}-V_{OUT}=2V$		5			5		mA
	Supply voltage rejection ratio	$V_{OUT}=0$	80	110		80	110		dB
	Differential logic threshold	$T_J=25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

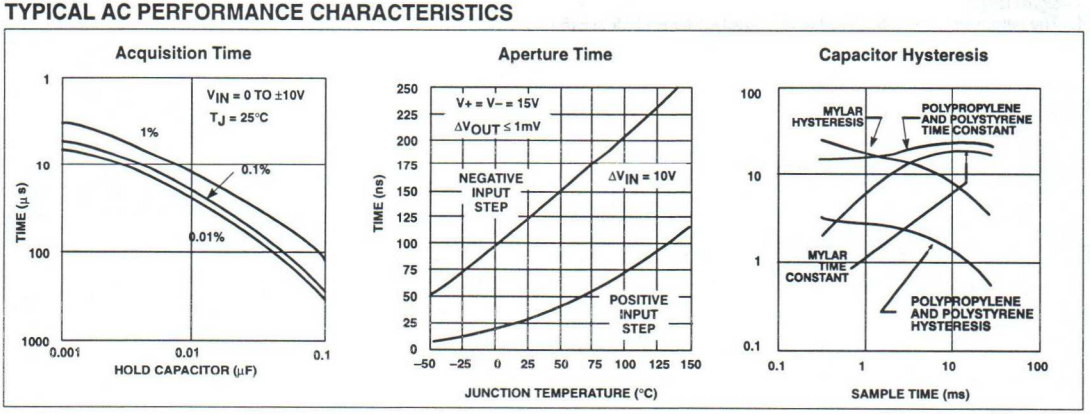
NOTES:

1. Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S=\pm 15V$, $T_J=25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.
2. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
3. Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
4. The parameters are guaranteed over a supply voltage of ±5 to ±18V.

TYPICAL DC PERFORMANCE CHARACTERISTICS

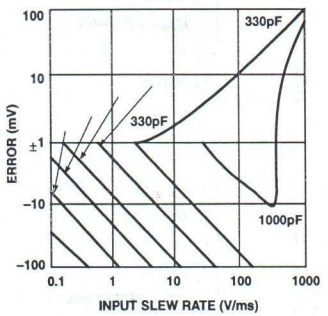


TYPICAL AC PERFORMANCE CHARACTERISTICS

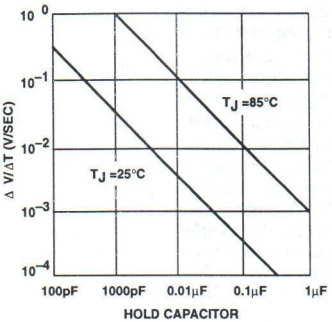


TYPICAL AC PERFORMANCE CHARACTERISTICS (Continued)

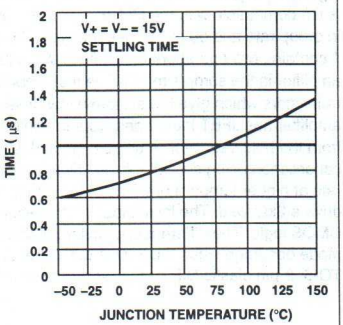
Dynamic Sampling Error



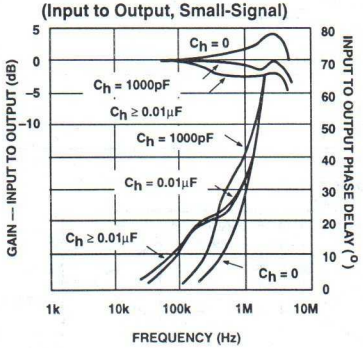
Output Droop Rate



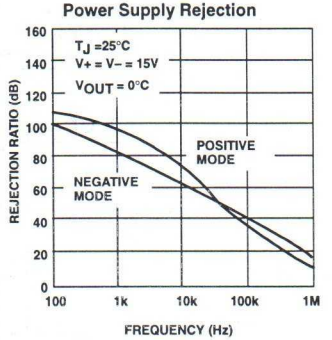
'Hold' Sampling Time



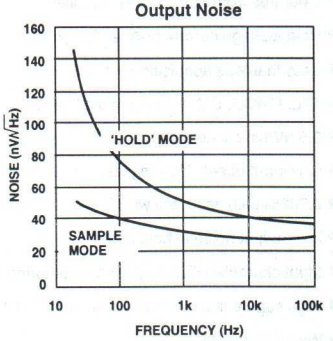
Phase And Gain
(Input to Output, Small-Signal)



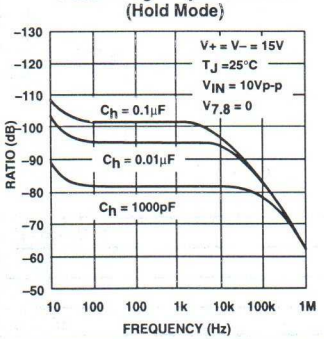
Power Supply Rejection



Output Noise



Feedthrough Rejection Ratio
(Hold Mode)



Sample-and-hold amplifier — NE/SE5537

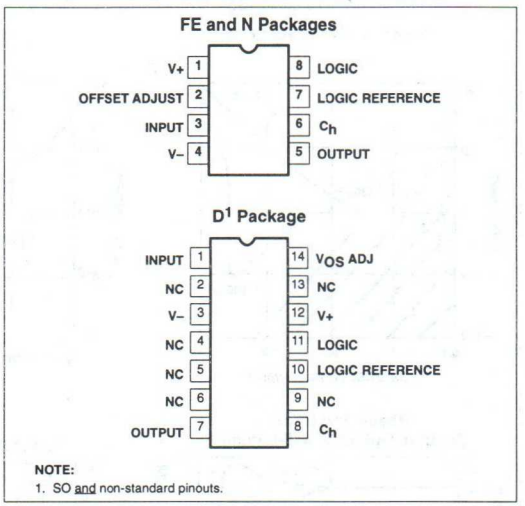
DESCRIPTION

The NE5537 monolithic sample-and-hold amplifier combines the best features of ion-implanted JFETs with bipolar devices to obtain high accuracy, fast acquisition time, and low droop rate. This device is pin-compatible with the LF198, and features superior performance in droop rate and output drive capability. The circuit shown in Figure 1 contains two operational amplifiers which function as a unity gain amplifier in the sample mode. The first amplifier has bipolar input transistors which give the system a low offset voltage. The second amplifier has JFET input transistors to achieve low leakage current from the hold capacitor. A unique circuit design for leakage current cancellation using current mirrors gives the NE5537 a low droop rate at higher temperature. The output stage has the capability to drive a 2kΩ load. The logic input is compatible with TTL, PMOS or CMOS logic. The differential logic threshold is 1.4V with the sample mode occurring when the logic input is high. It is available in 8-lead TO-5, 8-pin plastic DIP packages, and 14-pin SO packages.

FEATURES

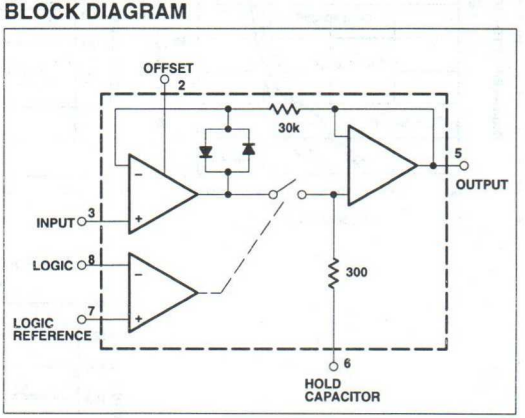
- Operates from ±5V to ±18V supplies
- Hold leakage current 6pA @ T_J = 25°C
- Less than 4μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5mV typical hold step at CH=0.01μF
- Low input offset: 1MV (typical)
- 0.002% gain accuracy with R_L=2kΩ
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

PIN CONFIGURATIONS



NOTE:
1. SO and non-standard pinouts.

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5537N	0404B
14-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE5537D	0175D
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE5537FE	0404B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Voltage supply	±18	V
P_D	Maximum power dissipation T_A=25°C (still-air)[1]		
	N package	1160	mW
	D package	1090	mW
	FE package	780	mW
T_A	Operating ambient temperature range		
	SE5537	-55 to +125	°C
	NE5537	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
V_{IN}	Input voltage	Equal to supply voltage	
	Logic to logic reference differential voltage[2]	+7, -30	V
	Output short circuit duration	Indefinite	
	Hold capacitor short circuit duration	10	s
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 8.3mW/°C
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

DC ELECTRICAL CHARACTERISTICS[1]

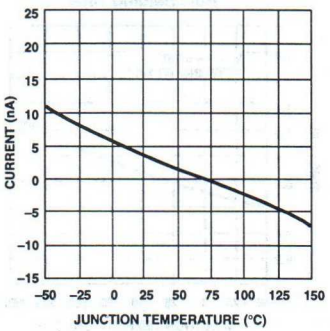
SYMBOL	PARAMETER	TEST CONDITIONS	SE5537			NE5537			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[4]	T_J=25°C		1	3		2	7	mV
		Full temperature range			5			10	mV
I_{BIAS}	Input bias current[4]	T_J=25°C		5	25		10	50	nA
		Full temperature range			75			100	nA
	Input impedance	T_J=25°C		10^{10}			10^{10}		Ω
	Gain error	T_J=25°C		0.002	0.007		0.004	0.01	%
		-10V≤V_{IN}≤10V, R_L=2kΩ -11.5V≤V_{IN}≤11.5V, R_L=10kΩ							
		Full temperature range			0.02			0.02	%
	Feedthrough attenuation ratio at 1kHz	T_J=25°C, C_H=0.01µF	86	96		80	90		dB
	Output impedance	T_J=25°C, "HOLD" mode		0.5	2		0.5	4	Ω
		Full temperature range			4			6	
	"HOLD" Step[2]	T_J=25°C, C_H=0.01µF, V_{OUT}=0		0.5	2.0		1.0	2.5	mV
I_{CC}	Supply current[4]	T_J=25°C		4.5	6.5		4.5	7.5	mA
	Logic and logic reference input current	T_J=25°C		2	10		2	10	µA
	Leakage current into hold capacitor[4]	T_J=25°C "hold" mode[3]		6	50		6	100	pA
	Acquisition time to 0.1%	V_{OUT}=10V, C_H=1000pF		4			4		µs
		C_H=0.01µF		20			20		µs
	Hold capacitor charging current	V_{IN}-V_{OUT}=2V		5			5		mA
SVRR	Supply voltage rejection ratio	V_{OUT}=0V	80	110		80	110		dB
	Differential logic threshold	T_J=25°C	0.8	1.4	2.4	0.8	1.4	2.4	V

NOTES:

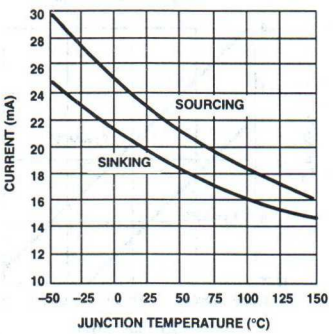
1. Unless otherwise specified, the following conditions apply: Unit is in "sample" mode. V_S=±15V, T_J=25°C, -11.5V≤V_{IN}≤11.5V, C_H=0.01µF, and R_L=2kΩ. Logic reference voltage=0V and logic voltage=2.5V.
2. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01F hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
3. Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
4. These parameters guaranteed over a supply voltage range of ±5 to ±18V.

TYPICAL PERFORMANCE CHARACTERISTICS

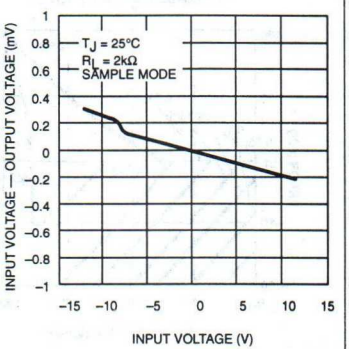
Input Bias Current



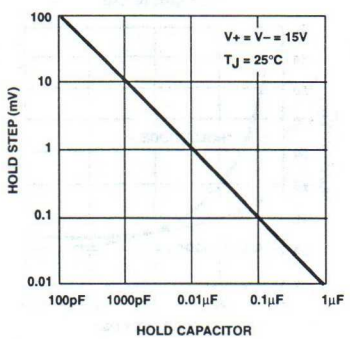
Output Short-Circuit Current



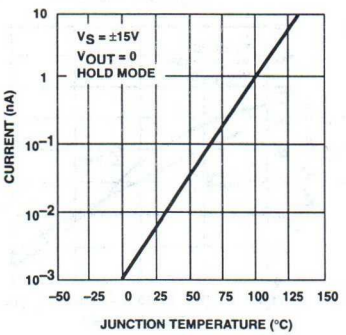
Gain Error



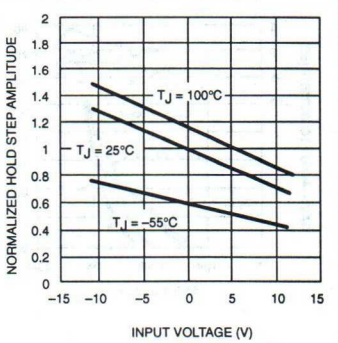
Hold Step



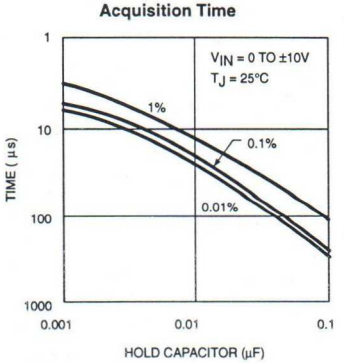
Leakage Current Into Hold Capacitor



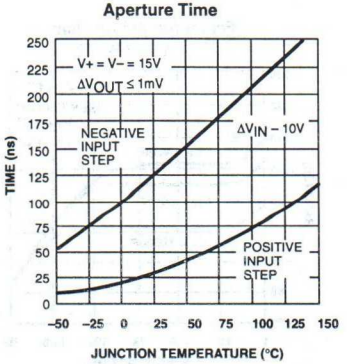
Hold Step vs Input Voltage



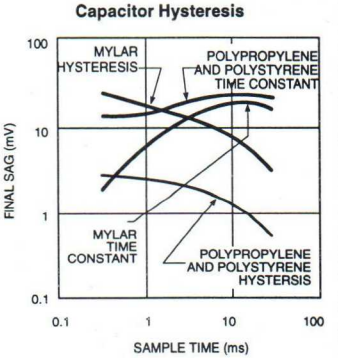
Acquisition Time



Aperture Time

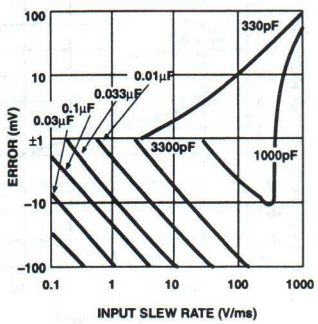


Capacitor Hysteresis

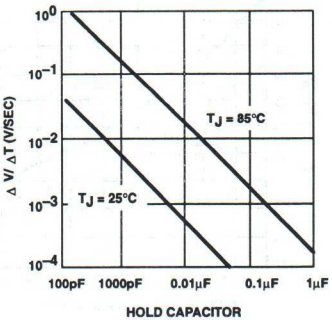


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

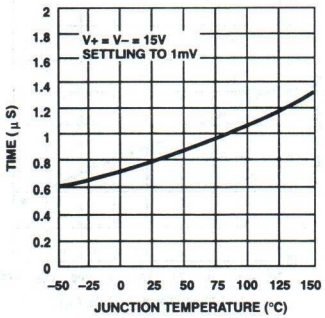
Dynamic Sampling Error



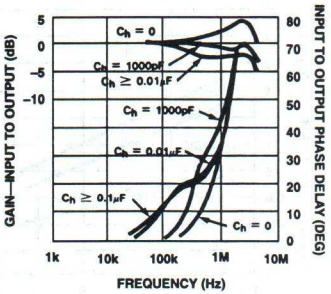
Output Droop Rate



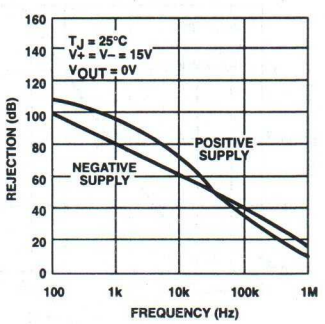
Hold Settling Time



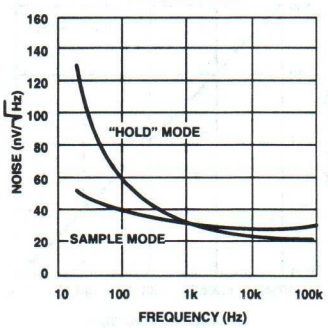
Phase and Gain (Input-to-Output, Small-Signal)



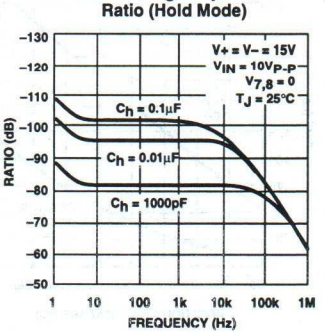
Power Supply Rejection



Output Noise



Feedthrough Rejection Ratio (Hold Mode)



SAMPLE-AND-HOLD

For many years designers have used the sample-and-hold (or track-and-hold) to operate on analog information in a time frame which is expedient.

By sampling a segment of the information and holding it until the proper timing for converting to some form of control signal or readout, the designer maintains certain freedom in performing predetermined manipulative functions. Therefore, the sample-and-hold can be defined as a "selective analog memory cell".

The memory is volatile and will also decay with time.

When using the sample-and-hold method for evaluating signal information, the designer is given the added feature of eliminating outside noise elements. With the analog-to-digital converter products available today, the "DC memory" of the sample-and-hold can be easily converted to digital format and further incorporated into microprocessor-based systems.

Parametric evaluation of the sample-and-hold will be discussed in the following paragraphs.

DEFINITION OF TERMS

Acquisition Time —
The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Delay Time —
The time elapsed from the hold command to the opening of the switch.

Aperture Jitter —
Also called "aperture uncertainty time", it is the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

Aperture Time —
The delay required between "HOLD" command and an input analog transition, so that the transition does not affect the held output.

Bandwidth —
The frequency at which the gain is down 3dB from its DC value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

Dynamic Sampling Error —
The error introduced into the hold output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Effective Aperture Delay —
The time difference between the hold command and the time at which the input signal is at the held voltage.

Figure of Merit —
The ratio of the available charging current during sample mode to the leakage current during hold mode.

Gain Error —
The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold Mode Droop —
The output voltage change per unit of time while in hold. Commonly specified in V/s, μV/μs or other convenient units.

Hold Mode Feedthrough —
The percentage of an input sinusoidal signal that is measured at the output of a sample-hold when it's in hold mode.

Hold Settling Time —
The time required for the output to settle within 1mV of final value after the "HOLD" logic command.

Hold Step —
The voltage step at the output of the sample-and-hold when switching from sample mode to hold mode with a steady (DC) analog input voltage. Logic swing is 5V.

Sample-to-Hold Offset Error —
The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

Slew Rate —
The fastest rate at which the sample-and-hold output can change (specified in V/μs).

Threshold Level —
That level which causes the switch control to change state.

BASIC BLOCK DIAGRAM

The basic circuit concept of the sample-and-hold circuit incorporates the use of two (2) operational amplifiers and a switch control mechanism (which determines sample, hold or track conditions).

The block diagram of the NE5537 is a closed loop, non-inverting unity gain sample-and-hold system. The input buffer amplifier supplies the current necessary to charge the hold capacitor, while the output buffer amplifier closes the loop so that the output voltage is identical to the input voltage (with consideration for input offset voltage, offset current, and temperature variations which are common to all sample-and-hold circuits, be they monolithic, hybrid or modular).

When the sampling switch is open (in the hold mode), the clamping diodes close the loop around the input amplifier to keep it from being overdriven into saturation.

The switch control is driven by external logic levels via a timing sequence remote from the sample-and-hold device (See Figure 1). The switch control has a floating reference (Pin 7), referred to as the logic reference which makes the sample-and-hold device compatible to several types of external logic signals (TTL, PMOS, and CMOS). The switching device operates at a threshold level of 1.4V.

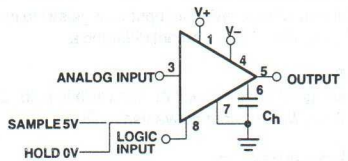


Figure 1. Typical Connection

The switch mechanism is on (sampling an information stream) when the logic level is high (Pin 8 is 1.4V higher than Pin 7) and presents a load of 5μA to the input logic signal. The analog sampled signal is amplified, stored (in the external holding capacitor), and buffered. At the end of the sampling period, the internal switch mechanism turns off (switch opens) and the "stored analog memory" information on the external capacitor (Pin 6) is loaded down by an operational amplifier connected in the unity gain non-inverting configuration. This input impedance of this amplifier is effectively:

$$R = R_{IN}(A_{OL}) / (1 + 1/A)$$

where R = Effective input impedance

R_{IN} = Open-loop input impedance

A_{OL} = Open-loop gain

A = AC loop gain

Therefore, the higher the open-loop gain of the second operational amplifier, the larger the effective loading on the capacitor. The larger the load, the lower the "leakage" current and the better the droop characteristics.

In actuality, the amplifiers are designed with special leakage current cancellation circuits along with FET input devices. The leakage current cancellation circuits give better high temperature operation. (Remember that the FET amplifiers double in required bias current for every 10 degree increase in junction temperature.)

Sampling time for the NE5537 is less than 10μs (measured to 0.1% of input signal). Leakage current is 6pA at a rate output load of 2kΩ.

BASIC APPLICATIONS

Multiplying DAC

As depicted in the block diagram of Figure 2, the sample-and-hold circuit is used to supply a "variable" reference to the digital-to-analog converter. As the input reference varies, the output will change in accordance with Equation 1, shown in Figure 2.

Varying the input signal reference level can aid the system in performing both compression and expansion operations. The multiplying DACs used are the Philips Semiconductors NE/SE5008; however, if the rate of change of the reference variation is kept slow enough, a microprocessor-compatible DAC can be incorporated, such as the NE5018 or the NE5020.

DATA ACQUISITION SYSTEMS

As mentioned earlier, the designer may wish to operate on several different segments of an "analog" signal; however, he is limited by the fact that only one analog-to-digital converter channel is available to him. Figure 3 shows the means by which a multiplexing system may be accomplished.

APPLICATION HINTS

Hold Capacitor

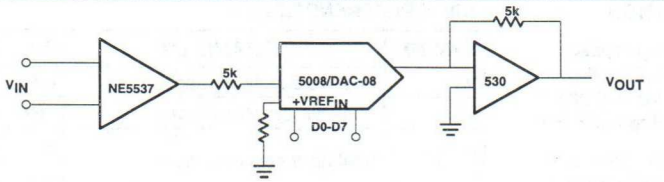
A significant source of error in an accurate sample-and-hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long "soak" time is required before the circuit can be put back in the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with >1% hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. The hysteresis relaxation time constant in polystyrene, for instance, is 10-50ms. If A-to-D conversion can be made within 1ms, hysteresis error will be reduced by a factor of ten.

DC ZEROING

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1kΩ potentiometer which has one end tied to V+ and the other end tied through a resistor to ground. The resistor should be selected to give 0.6mA through the 1kΩ potentiometer.

Sampling Dynamic Signals

Sampling errors due to moving (changing) input signals are of significant concern to designers employing sample-and-hold circuits. There exist finite phase delays through the sample-and-hold circuit causing an input-output phase of differential for moving signals. In addition, the series protection resistor (300Ω to Pin 6 of the NE5537) will add an RC time constant, over and above the slew rate limitation of the input buffer/current drive amplifier. This means that at the moment the "HOLD" command arrives, the hold capacitor voltage may be somewhat different from the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 V_{P-P} at 10kHz. Maximum dV/dt is 0.6V/μs. With no analog phase delay and 100ns logic delay, one could expect up to (0.1μs) (0.6V/μs) =60mV error if the "HOLD" signal arrived near maximum dV/dt of the input. A positive-going input would give a ±60mV error. Now assume a 1MHz (3dB) bandwidth for the overall analog loop. This generates a phase delay of 160ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16μs) (0.6V/μs)=-96mV (analog) for a total of -36mV. To add to the confusion, analog delay is proportional to hold capacitor value, while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.



NOTE:

$V_{OUT} = V_{IN} \times \frac{1}{256} (20\ D_0 + 2^1 D_1 + 2^7 D_7)$ Equation 1

Figure 2. Multiplying DAC Application

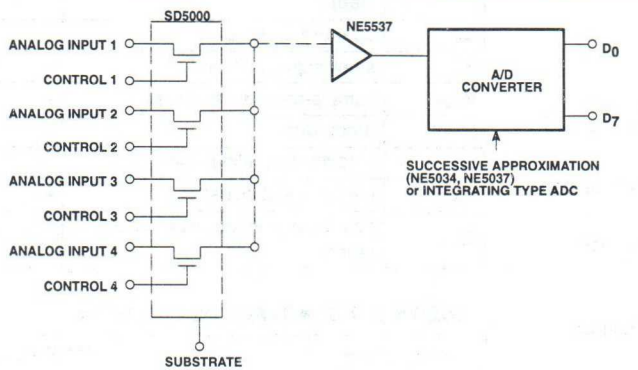


Figure 3. Analog Data Multiplexing

A curve labeled "Aperture Time" has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "HOLD" command. This curve is based on a 1mV error fed into the output.

A second curve, "Hold Settling Time," indicates the time required for the output to settle to 1mV after the "HOLD" command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

Logic signals also couple to the hold capacitor. This hold capacitor should be guarded by a PC card trace connected to the sample-and-hold output. This will also minimize board leakage.

SPECIAL NOTES

1. Not all definitions herein defined are measured parametrically for the NE5537, but are legitimate terms used in sample-and-hold systems.
2. Reference should be made to Design Engineering, Volumes 23 (Nov. 8, 1978), 25 (Dec. 6, 1978) and 26 (Dec. 20, 1978) for articles written by Eugene Zuch of Datel Systems, Inc., for a further discussion of sample-and-hold circuits.
3. Reference also made to National Semiconductor Corporation's Special Functions Data Book (1976).

High-speed single sample-and-hold amplifier — TDA1535B

GENERAL DESCRIPTION

The TDA1535B is a high-speed sample-and-hold amplifier with a total harmonic distortion of 0.001%, and a very high signal-to-noise ratio.

The excellent performance of the circuit makes it suitable for data acquisition systems with resolution up to 16 bits. The control input is TTL compatible.

FEATURES

- High-speed: fast acquisition, hold-mode settling and aperture time
- Small sample-to-hold offset step, low droop rate
- Low noise: low total harmonic distortion and high signal-to-noise ratio
- Control circuit with TTL input.

FUNCTIONAL DESCRIPTION

The operation of the circuit will be explained using the application diagram (Fig.3). The circuit is a single Sample-and-Hold circuit. The several parts of the diagram will be described in the next sections.

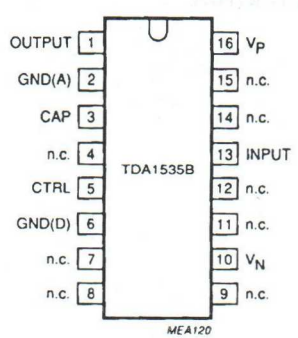


Fig.1 Pinning diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage	4.5	5.0	5.5	V
V_N	negative supply voltage	-5.5	-5.0	-4.5	V
THD	total harmonic distortion	–	-100	–	dB
		–	0.001	–	%
S/N	signal-to-noise ratio	–	110	–	dB
t_{ac}	acquisition time to 0.001% (8 V step)	–	2	–	µs
t_{av}	aperture uncertainty	–	0.1	–	ns
B	small signal bandwidth	–	2	–	MHz
V_{SHO}	sample-to-hold offset step	–	2	–	mV
dV/dt	droop rate	–	40	–	mV/s
t_{se}	hold-mode settling time	–	1	–	µs
P_{tot}	total power dissipation	–	225	–	mW
T_{amb}	operating ambient temperature range	-30	–	+85	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1535B	16	DIL	plastic	SOT38

PINNING

SYMBOL	PIN	DESCRIPTION
OUTPUT	1	output
GND(A)	2	analog ground
CAP	3	S/H capacitor
n.c.	4	not connected
CTRL	5	S/H control
GND(D)	6	digital ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
V_N	10	negative supply voltage
n.c.	11	not connected
n.c.	12	not connected
INPUT	13	input
n.c.	14	not connected
n.c.	15	not connected
V_P	16	positive supply voltage

Supply block

The circuit must be supplied by a dual supply voltage. Nominally the supply voltages are plus and minus 5 V. This supply voltage is needed for a rated output voltage of 8 Vtt, but the circuit will also operate at lower supply voltages. Furthermore separate 'grounds' for analog and digital signals are used. The supply circuit consists of a current source circuit which contains separate sources for the voltage follower, and the hold amplifier to prevent feedthrough in the hold condition. The supply acts as a current source, so the current consumption is almost independent of the supply voltage resulting in a good supply ripple rejection.

Voltage follower amplifier

The voltage follower amplifier is an operational amplifier in voltage follower configuration. It contains two PMOS input stages controlled by the S/H switch, one input stage for the track mode, the other for the hold mode. The input stage that is used in the hold mode has it's + input connected to the analog ground forcing the output to analog ground too. In this way, feedthrough of the input signal is prevented in the hold mode.

Hold switch

The hold switch is a large NMOS transistor with an on-resistance of 50 Ω. In order to reduce the charge transfer of the digital signal into the analog path, two short-circuited NMOS transistors, with the inverse, digital signal on their gate, are added on both sides of the switching transistor.

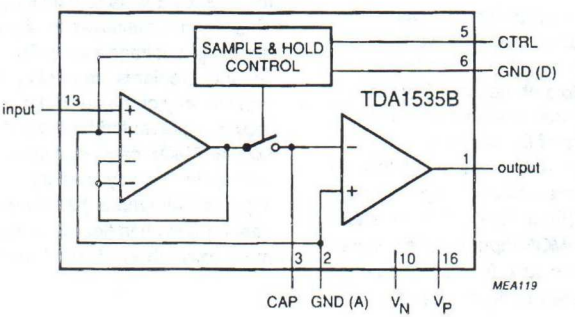


Fig.2 Block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage		–	6	V
V_N	negative supply voltage		–6	–	V
T_{stg}	storage temperature range		–55	+150	°C
T_{amb}	operating ambient temperature range		–30	+85	°C
V_{es}	electrostatic handling	see note 1	–2000	+2000	V

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction-to-ambient	75	K/W

Hold amplifier

The hold amplifier is an operational amplifier similar to the voltage follower amplifier. The PMOS transistors of the input stage are very useful for a hold amplifier because of the very low input-current, resulting in a low droop rate and a low input current noise. The tail current and the W/L of the PMOS input transistors are chosen in such a way that a very good noise performance is achieved. The input stage is followed by a voltage gain stage. This stage is optimized for linearity and output voltage swing. The usual linearity problems, caused by the non-linearity of the current source load, are prevented by the use of a special PMOS cascoded current source. In this way linearity improves with more than 20 dB thus offering distortion figures in the track mode lower than - 100 dB for input frequencies up to 20 kHz and output voltages up to 8 Vtt.

Sample-and-hold control

The sample-and-hold control input is a TTL compatible input. The signal on this input controls the switches mentioned in the above sections in the correct timing order. The supply is taken from the 'V_p' pin via an on-chip separate supply line.

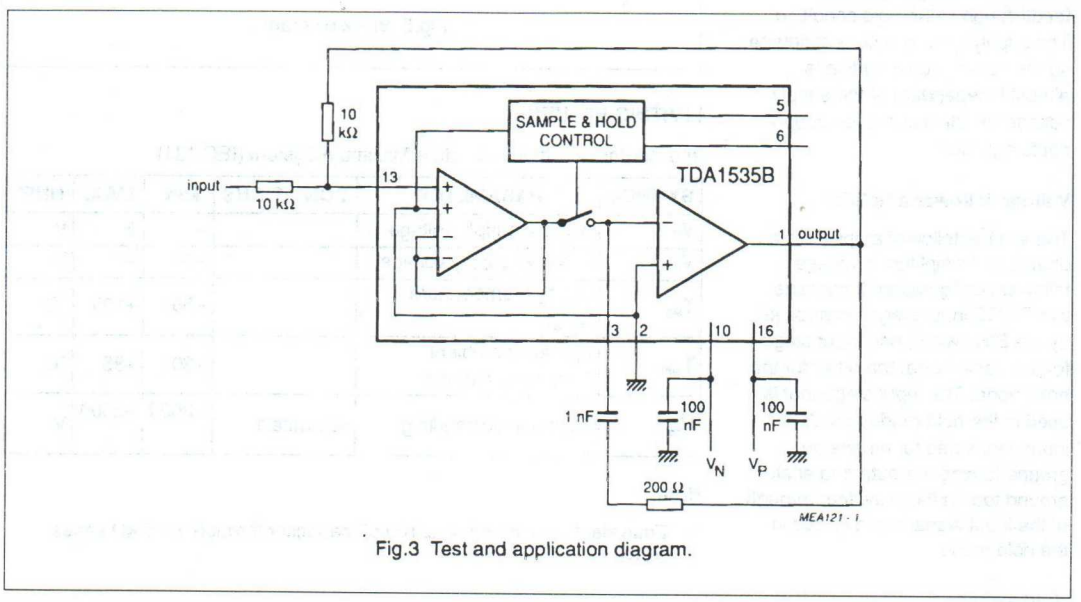


Fig.3 Test and application diagram.

CHARACTERISTICS

V_P = +5 V; T_{amb} = +25 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage		4.5	5.0	5.5	V
V_N	negative supply voltage		−5.5	−5.0	−4.5	V
I_P	positive supply current		–	22	–	mA
I_N	negative supply current		–	−23	–	mA
P_{tot}	total power dissipation		–	225	–	mW
Input/Output						
A_v	gain	note 2	–	−1	–	V/V
V_i	input voltage (RMS value)		–	–	2.82	V
Sample mode						
THD	total harmonic distortion	notes 1,2,3	–	−100	–	dB
SNR	S/N ratio	notes 1,2,3	–	110	–	dB
B	small signal band width		–	2	–	MHz
Sample/hold mode						
t_{ad}	aperture delay time	see Fig.4	–	100	–	ns
t_{av}	aperture uncertainly (RMS)	see Fig.4	0	0.1	0.2	ns
V_{SHO}	sample-to-hold (pedestal)	see Fig.4	–	2	–	mV
dV/dt	offset step droop rate	see Fig.4	–	40	–	mV/s
t_{ac}	acquisition time to 0.001%	see Fig.4	–	2	–	µs
t_{se}	hold-mode settling time	see Fig.4	–	1	–	µs
THDF	total harmonic distortion functional	notes 1,4	–	−100	−96	dB
Supply voltage ripple rejection						
SVRR		note 5	–	80	–	dB
SVRR		note 5	55	80	–	dB
Digital inputs						
V_{IH}	digital input voltage, hold mode (logic 1)		2	–	V_p	V
I_{IH}	digital input current, sample mode	V_{IH} = 2.4 V	–	–	20	µA
V_{IL}	digital input voltage, sample mode (logic 0)		0	–	0.8	V
I_{IL}	digital input current, hold mode	V_{IL} = 0.4 V	−400	–	–	µA

Notes

1. Over audio band (20 Hz to 20 kHz).
2. In sampling mode.
3. At maximum input signal.
4. Distortion of sampled signal at a sample frequency of 50 kHz.
5. The ripple rejection is measured at the output of the hold amplifier; amplitude = 0.5 Vtt. f = 100 Hz to 10 kHz.

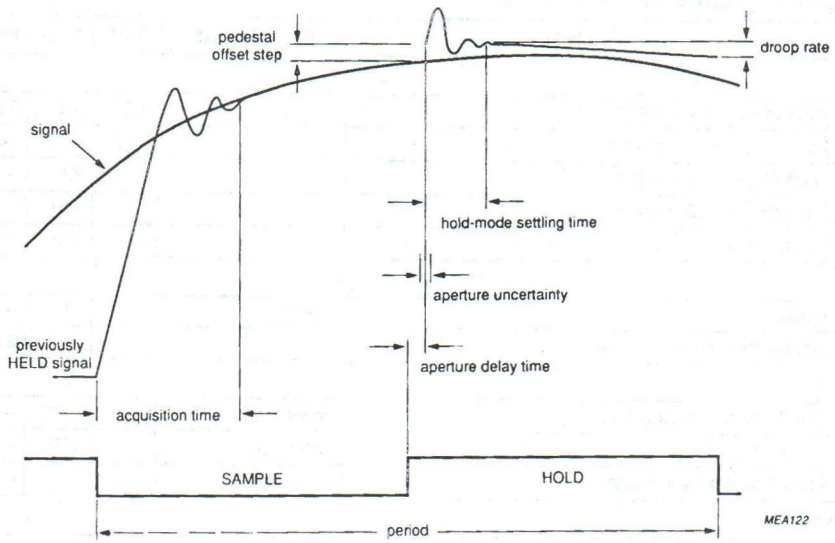


Fig.4 Sample/hold timing characteristics (not to scale).

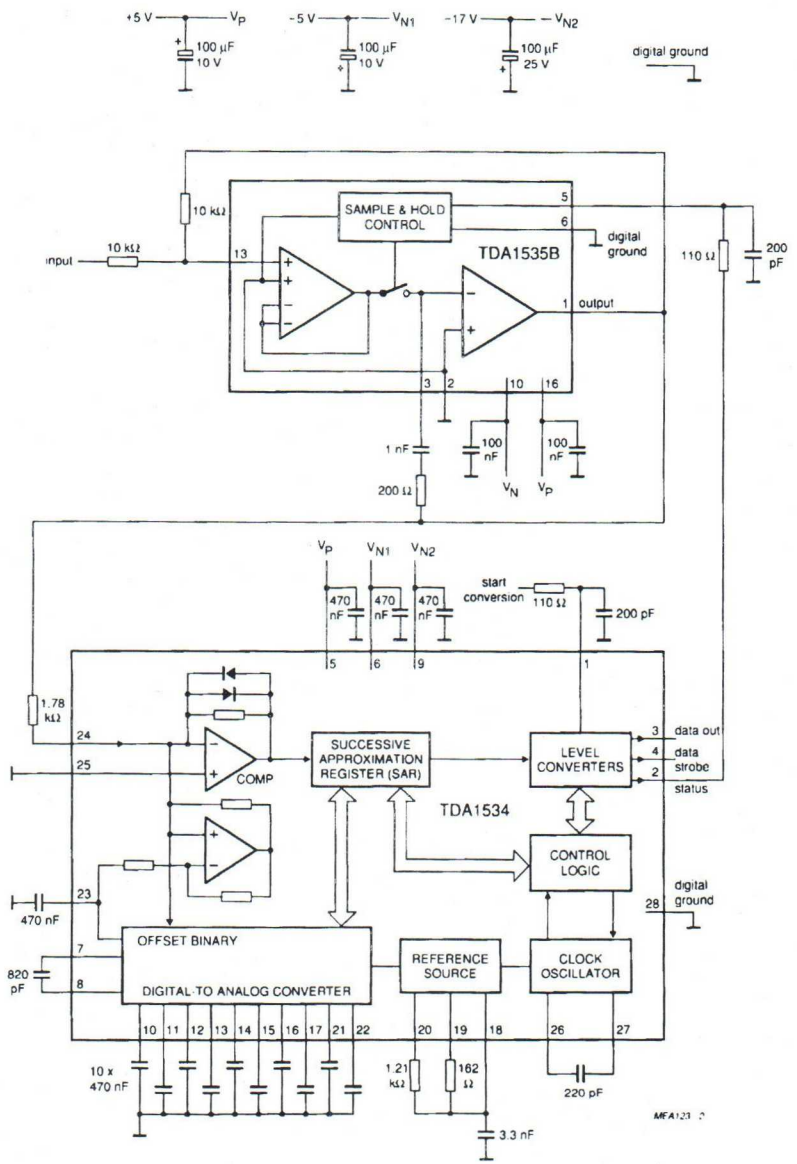


Fig.5 Application diagram of TDA1535B in combination with TDA1534.

Section 13
Position Measurement

INDEX

NE/SA/SE5521 LVDT signal conditioner 901
AN1182 Using the NE5521 signal conditioner in multi-faceted applications 906

LVDT signal conditioner — NE/SA/SE5521

DESCRIPTION

The NE/SA/SE5521 is a signal conditioning circuit for use with Linear Variable Differential Transformers (LVDTs) and Rotary Variable Differential Transformers (RVDTs). The chip includes a low distortion, amplitude-stable sine wave oscillator with programmable frequency to drive the primary of the LVDT/RVDT, a synchronous demodulator to convert the LVDT/RVDT output amplitude and phase to position information, and an output amplifier to provide amplification and filtering of the demodulated signal.

FEATURES

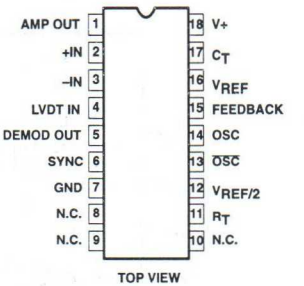
- Low distortion
- Single supply 5V to 20V, or dual supply ±2.5V to ±10V
- Oscillator frequency 1kHz to 20kHz
- Capable of ratiometric operation
- Low power consumption (182mV typ)

APPLICATIONS

- LVDT signal conditioning
- RVDT signal conditioning
- LPDT signal conditioning
- Bridge circuits

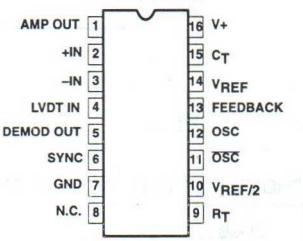
PIN CONFIGURATIONS

F, N Packages



TOP VIEW

D[1] Package



TOP VIEW

NOTE:
1. SOL — released in large SO package only.

ORDERING INFORMATION

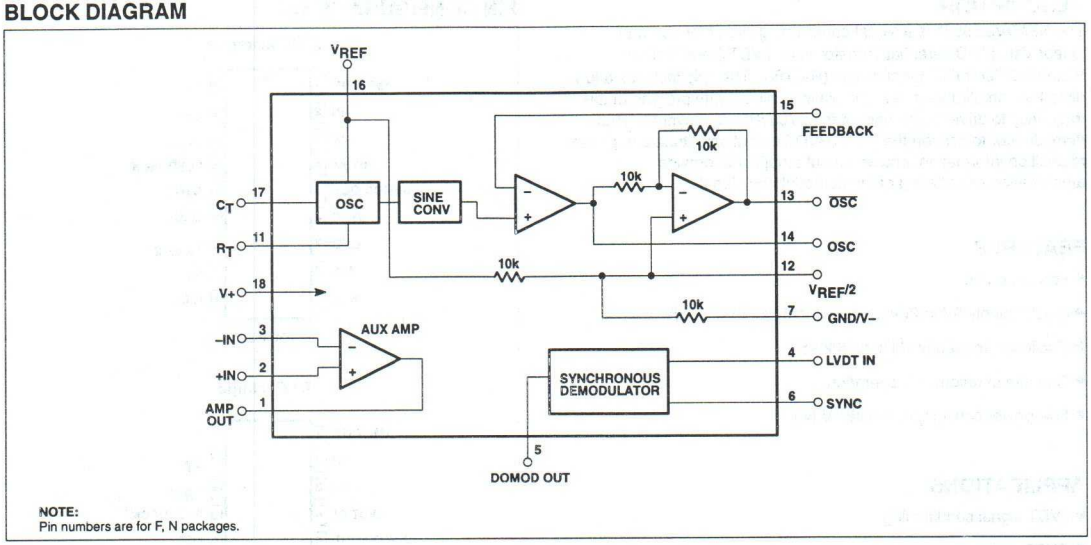
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
18-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5521N	0407A
16-Pin Small Outline Large (SOL) Package	0 to +70°C	NE5521D	0171B
18-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA5521N	0407A
18-Pin Ceramic Dual In-Line Package (CERDIP)	–55 to +125°C	SE5521F	0583A
16-Pin Ceramic Dual In-Line Package (CERDIP)	–40 to +85°C	SA5521D	0582B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+20	V
	Split supply voltage	±10	V
T_A	Operating temperature range NE5521 SA5521 SE5521	 0 to 70 –40 to +85 –55 to +125	 °C °C °C
T_{STG}	Storage temperature range	–65 to +125	°C
P_D	Power dissipation[1]	910	mW

NOTES:
1. For derating, see typical power dissipation versus load curves (Figure 1).

BLOCK DIAGRAM



NOTE:
Pin numbers are for F, N packages.

PIN DEFINITIONS FOR D, F AND N PACKAGES

PIN NO.		SYMBOL	DEFINITION
D	F, N		
1	1	Amp Out	Auxiliary Amplifier Out.
2	2	+IN	Auxiliary Amplifier non-inverting input.
3	3	–IN	Auxiliary Amplifier inverting input.
4	4	LVDT IN	Input to Synchronous Demodulator from the LVDT/RVDT secondary.
5	5	DEMOD OUT	Pulsating DC output from the Synchronous Demodulator output. This voltage should be filtered before use.
6	6	SYNC	Synchronizing input for the Synchronizing Demodulator. This input should be connected to the OSC or $\overline{OSC}$ output. Sync is referenced to $V_{REF}/2$.
7	7	GND	Device return. Should be connected to system ground or to the negative supply.
8	8	NC	No internal connection.
--	9	NC	No internal connection.
--	10	NC	No internal connection.
9	11	R_T	A temperature stable 18kΩ resistor should be connected between this pin and Pin 7.
10	12	$V_{REF}/2$	A high impedance source of one half the potential applied to V_{REF}. The LVDT/RVDT secondary return should be to this point. A bypass capacitor with low impedance at the oscillator frequency should also be connected between this pin and ground.
11	13	$\overline{OSC}$	Oscillator sine wave output that is 180° out of phase with the OSC signal. The LVDT/RVDT primary is usually connected between OSC and $\overline{OSC}$ pins.
12	14	OSC	Oscillator sine wave output. The LVDT/RVDT primaries are usually connected between OSC and $\overline{OSC}$ pins.
13	15	FEEDBACK	Usually connected to the OSC output for unity gain, a resistor between this pin and OSC, and one between this pin and ground can provide for a change in the oscillator output pin amplitudes.
14	16	V_{REF}	Reference voltage input for the oscillator and sine converter. This voltage MUST be stable and must not exceed +V supply voltage.
15	17	C_T	Oscillator frequency-determining capacitor. The capacitor connected between this pin and ground should be a temperature-stable type.
16	18	+V	Positive supply connection.

DC ELECTRICAL CHARACTERISTICS

$V+ = V_{REF} = 10V$, $T_A = 0$ to 70°C for NE5521, $T_A = -55$ to +125°C for SE5521, $T_A = -40$ to 85°C for SA5521, Frequency = 1kHz, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5521			SA/SE5521			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply current			12.9	20		12.9	18	mA
I_{REF}	Reference current			5.3	8		5.3	8	mA
V_{REF}	Reference voltage range		5		V+	5		V+	V
P_D	Power dissipation			182	280		182	260	mW
Oscillator Section									
	Oscillator output	$R_L = 10k\Omega$	$\frac{V_{REF}}{8.8}$				$\frac{V_{REF}}{8.8}$		V_{RMS}
THD	Sine wave distortion	No load		1.5			1.5		%
	Initial amplitude error	$T_A = 25°C$		0.4	±3		0.4	±3	%
	Tempco of amplitude			0.005	0.01		0.005	0.01	%/°C
	Init. accuracy of oscillator freq.	$T_A = 25°C$		±0.9	±5		±0.9	±5	%
	Temperature coeff. of frequency[1]			0.05			0.05		%/°C
	Voltage coeff. of frequency			2.5			3.3		%/V(V_{REF})
	Min OSC ($\overline{OSC}$) Load[2]		300	170		300	170		Ω
Demodulator Section									
ϵ_r	Linearity error	$5V_{P-P}$ input		±0.05	±0.1		±0.05	±0.1	%FS
	Maximum demodulator input			$\frac{V_{REF}}{2}$			$\frac{V_{REF}}{2}$		V_{P-P}
V_{OS}	Demodulator offset voltage			±1.4	±5		±1.4	±5	mV
TCV_{OS}	Demodulator offset voltage drift			5	25		5	25	µV/°C
I_{BIAS}	Demodulator input current		–600	–234		–500	–234		nA
	$V_{R/2}$ accuracy			±0.1	±1		±0.1	±1	%
Auxiliary Output Amplifier									
V_{OS}	Input offset voltage			±0.5	±5		±0.5	±5	mV
I_{BIAS}	Input bias current		–600	–210		–500	–210		nA
I_{OS}	Input offset current			10	50		10	50	nA
A_V	Gain		100	385		100	385		V/mV
SR	Slew rate			1.3			1.3		V/µs
GBW	Unity gain bandwidth product	$A_V = 1$		1.6			1.6		MHz
	Output voltage swing	$R_L = 10k\Omega$	7	8.2		7	8.2		V
	Output short circuit current to ground or to V_{CC}	$T_A = 25°C$		42	100		42	100	mA

NOTES:

1. This is temperature coefficient of frequency for the device only. It is assumed that C_T and R_T are fixed in value and C_T leakage is fixed over the operating temperature range.
2. Minimum load impedance for which distortion is guaranteed to be less than 5%.

DEFINITION OF TERMS

Oscillator Output	RMS value of the AC voltage at the oscillator output pin. This output is referenced to $V_{REF/2}$ and is a function of V_{REF}.
Sine Wave Distortion	The Total Harmonic Distortion (THD) of the oscillator output with no load. This is not a critical specification in LVDT/RVDT systems. This figure could be 15% or more without affecting system performance.
Initial Amplitude Error	A measure of the interchangeability of NE/SA/SE5521 parts, not a characteristic of any one part. It is the degree to which the oscillator output of a number of NE/SA/SE5521 samples will vary from the median of that sample.
Initial Accuracy of Oscillator Frequency	Another measure of the interchangeability of individual NE/SA/SE5521 parts. This is the degree to which the oscillator frequency of a number of NE/SA/SE5521 samples will vary from the median of that sample with a given timing capacitor.
Tempco of Oscillator Amplitude	A measure of how the oscillator amplitude varies with ambient temperature as that temperature deviates from a 25°C ambient.
Tempco of Oscillator Frequency	A measure of how the oscillator frequency varies with ambient temperature as that temperature deviates from a 25°C ambient.
Voltage Coefficient of Oscillator Frequency	The degree to which the oscillator frequency will vary as the reference voltage (V_{REF}) deviates from +10V.
Min OSC ($\overline{OSC}$) Load	Minimum load impedance for which distortion is guaranteed to be less than 5%.
Linearity Error	The degree to which the DC output of the demodulator/amplifier combination matches a change in the AC signal at the demodulator input. It is measured as the worst case nonlinearity from a straight line drawn between positive and negative fullscale end points.
Maximum Demodulator Input	The maximum signal that can be applied to the demodulator input without exceeding the specified linearity error.

APPLICATION INFORMATION

$$\text{OSC frequency} = \frac{V_{REF} - 1.3V}{V_{REF}\,(R_T + 1.5k)\,C_T}$$

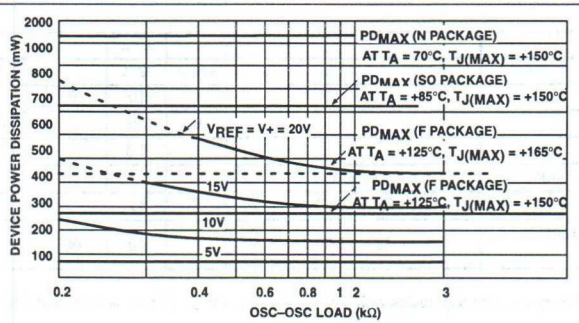


Figure 1. Device Power Dissipation vs OSC – $\overline{OSC}$ Load at +25°C

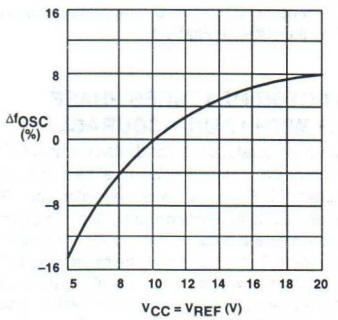


Figure 2. Oscillator Frequency Variation With Voltage (Normalized to $V_{REF} = V_{CC} = 10V$) $T_A = +25°C$

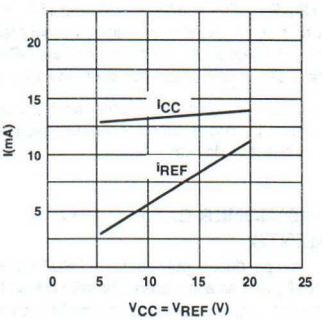


Figure 3. I_{REF} and I_{CC} vs Voltage ($T_A = +25°C$)

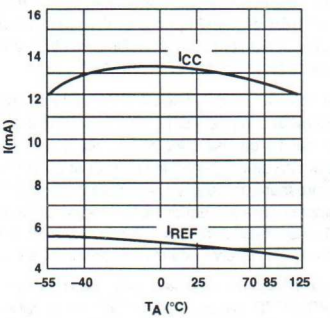


Figure 4. I_{REF} and I_{CC} vs Temperature ($V_{REF} = V_{CC} = 10V$)

Using the NE5521 signal conditioner in multi-faceted applications

AN1182

Author: Zahid Rahim

Position transducers call for a great deal of complex interface circuitry for input and output signal conditioning. The Philips Semiconductors NE/SA/SE5521 packs all the interface circuitry on one chip and provides a complete monolithic solution to all the signal conditioning required for position transducers.

Position transducers are widely used in industrial and commercial applications for measuring very small displacement or rotation. In fact, such transducers can be used for any application where a given parameter can be converted to linear or angular motion. Weight, force, pressure, torque, and acceleration are often converted to linear displacement or linear rotation using position transducers. The displacement or rotation information is next conditioned to provide an accurate measurement of the parameter.

SE5521 can interface with all of the popular position transducers such as the LVDT, RVDT, and LPDT. In addition, by varying the arrangement of external components, you can also configure a phase detector, an AC bridge circuit, and an AC voltmeter. For a brief description of the IC, see the section entitled "A Look at the Signal Conditioning IC."

IC PROVIDES SINGLE-CHIP SOLUTION TO LVDT MEASUREMENTS

Figure 1a shows a typical single supply LVDT displacement measurement circuit. The uncommitted amplifier is configured as a second-order, low-pass Butterworth filter with gain. The gain of the amplifier is $1+R_F/(R/2)$. The 1k offset adjust potentiometer is used to trim out the LVDT/signal conditioner system offset at null.

Exciting an LVDT at zero phase angle frequency results in minimum null voltage and optimum linearity (for a discussion, see "How an LVDT Works"). There are two ways of reducing null voltage—the first method is to adjust the oscillator frequency so that the secondary voltage is in phase with the primary excitation. The demodulator and oscillator voltage can be monitored on an oscilloscope for correct phasing as depicted in Figures 1b and 1c. A second method of phase compensation is to use a variable phase shift network between the oscillator output and the sync input to the device. An optional phase shift network in Figure 1a consists of a 20k phase adjust potentiometer in series with capacitor C_3. The potentiometer is adjusted for correct demodulator phasing as illustrated in Figures 1b and 1c. With R_O=10k, C_O=2nF, and at oscillator frequency, f_{OSC}=2900Hz, the phase shift is $\varphi=-\tan^{-1}(\omega R_O C_O)=-20°$.

The LVDT output is referenced to $V_{R/2}$ by tying one end of the secondary to Pin 12 of the device. A capacitor between Pin 12 and ground provides an AC ground for $V_{R/2}$. Since the output of Pin 12 is a source of high impedance, Pin 12 may need to be buffered in some applications so as to prevent loading effects on the voltage divider. The common mode voltage and the RMS value of the oscillator signals are determined by V_R; consequently, V_R should be a fixed reference voltage. By making V+ greater than V_R, the output swing of the auxiliary amplifier is increased and the filter can accommodate higher closed-loop gain.

The demodulator output has positive polarity when the LVDT output signal is 180° out of phase with the primary excitation (see Figure 1d), and has negative polarity when the LVDT output is in phase with the primary excitation (see Figure 1e). The polarity of the demodulator signal indicates on which side of null the core is while the amplitude indicates the relative displacement of the core from the null position.

Filtered DC output appears at Pin 1 of the device. Measurements with 10-bit accuracy at -55°C to +125°C temperature range are easily achieved by the circuit in Figure 1.

PHASE DETECTOR MEASURES PHASE DIFFERENCE WITH 10-BIT ACCURACY

The synchronous demodulator easily lends itself to phase detection as illustrated in Figure 2a. If signals of identical frequency are applied to sync input (Pin 6) and to the demodulator input (Pin 4), respectively, the demodulator functions as a phase detector with output DC component being proportional to phase difference between the two inputs. The signals must be referenced to 0V for dual supply operation or to $V_{R/2}$ for single supply operation. At ±5V supplies, the demodulator can easily handle 7V peak-to-peak signals. The low-pass network configured with the uncommitted amplifier provides DC output at Pin 1 of the device. The DC output is maximum (+full-scale) when V_1 and V_2 are 180° out of phase (see Figure 1d) and minimum (-full-scale) when the signals are in phase (see Figure 1e). At quadrature (φ = 90°), the DC output is 0V as shown in Figure 2b. By calibrating the -FS, 0, and +FS points, any unknown phase difference may be determined by just measuring the DC output at Pin 1. A linear relationship between the DC output and phase difference is shown by the transfer curve in Figure 2c.

Even though the oscillator signals are not utilized in this particular application, the use of C_T and R_T is still recommended in order to prevent saturation of active devices in the IC.

SIGNAL CONDITIONER EASES LPDT MEASUREMENTS

Figure 3 shows a simple dual supply setup for LPDT measurements. Op amp IC_1 is configured as a low-pass filter with cut-off frequency equal to the oscillator frequency of 2900Hz. The filter attenuates the higher order spectral components of the oscillator signal and produces a low-distortion sine wave at the output. This sine wave excites one primary, while the other primary is excited by a cosine wave produced by amp IC_2. Amp IC_2 is configured as a constant amplitude lag circuit that preserves the amplitude of the sine wave input from IC_1, but phase shifts the signal by 90° at the output. The phase shift, φ, is given by $\varphi = -2\tan^{-1}(2\pi f_{OSC} R_5 C_3)$. Thus, at 90° phase shift, $f_{OSC}=1/(2\pi R_5 C_3)$. R_5 is a 10k potentiometer with its center wiper tied to one end. The potentiometer is tweaked and the wave forms from IC_1 and IC_2 are observed on an ocilloscope for 90° phase difference and 0V at the output of the device (Pin 1). The system is now ready to make phase measurements as discussed earlier.

For dual supply operation, both the positive and negative supplies should be closely regulated since the oscillator common mode voltage varies with the supplies.

AC BRIDGE CALIBRATES RESISTORS AND CAPACITORS WITH 10-BIT ACCURACY

An AC bridge, shown in Figure 4, provides a simple and cost-effective solution to matching resistors and capacitors on production lines. Impedances Z_R and Z_X form a half-bridge, while OSC and $\overline{OSC}$ excite the bridge differentially. The external op amp is a JFET input amplifier (LF356) with very low input bias current on the order of 30pA (typical). C_1 allows AC coupling by blocking the DC common mode voltage from the bridge, while R_1 biases the

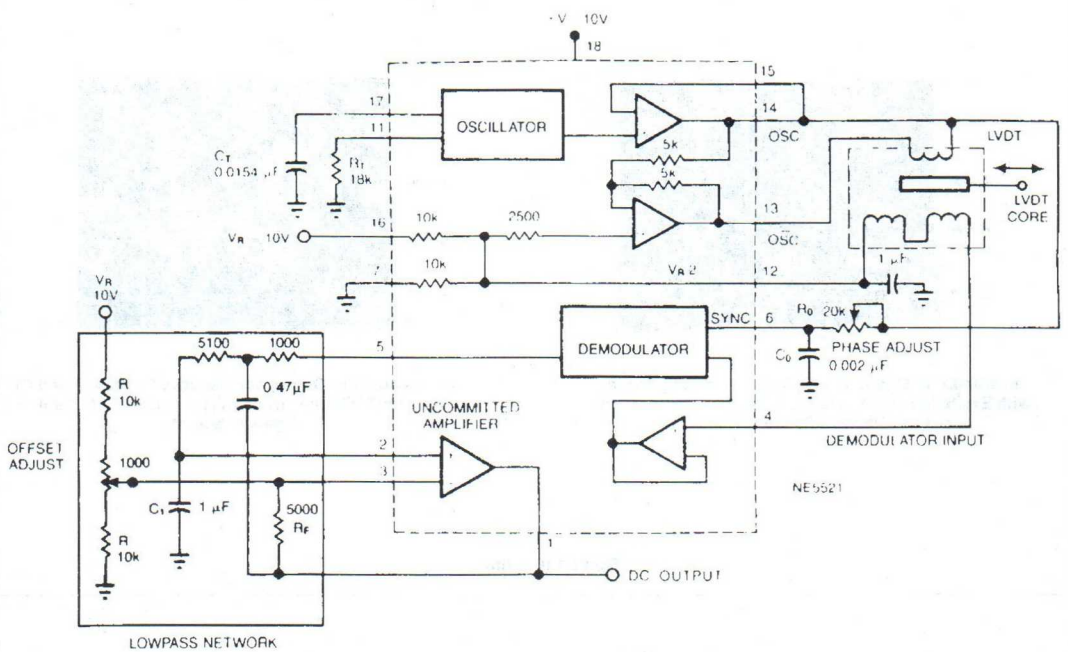
output of LF356 to 0V at DC. Use of FET input op amp insures that DC offset due to bias current through R_1 is negligible. AC output of the demodulator is filtered via the uncommitted amp to provide DC voltage for the meter. The 10k potentiometer, R_5, limits the current into the meter to a safe level. Calibration begins by placing equal impedances at Z_R and Z_X, and the system offset is nulled by the offset adjust circuit so that Pin 1 is at 0V. Next, known values are placed at Z_X and the meter deviations are calibrated. The bridge is now ready to measure an unknown impedance at Z_X with ±0.05% accuracy or better.

RMS-TO-DC CONVERTER YIELDS 10-BIT ACCURACY

An AC voltmeter may be easily constructed as in Figure 5; the simplicity of the circuit and low component count make it particularly attractive. The demodulator output is a full-wave rectified signal from the AC input at Pin 4. DC component of the rectified signal at Pin 5 varies linearly with the RMS input at Pin 4 and thus provides an accurate RMS-to-DC conversion at the output of the filter (Pin 1). C_T is a variable capacitor that is tweaked until the oscillator signal to the sync input of the demodulator is in phase with the AC signal at Pin 4.

In many applications it may not be desirable to adjust C_T each time the AC signal frequency changes. An alternate approach is to use a zero-crossing detector to excite the sync input of the device. The LM311 comparator in Figure 6 produces a square wave (trace A in Figure 6b) in phase with the AC signal (trace B). Optimum rectification thus occurs at the demodulator output (trace C). For precision measurements at high frequencies, a fast, low offset comparator is recommended.

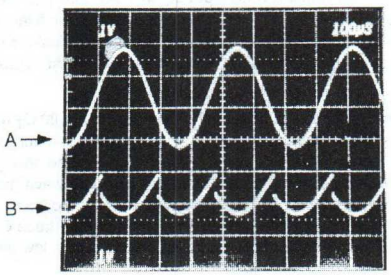
2. C_T is tweaked until the sync signal is in phase with the AC signal.



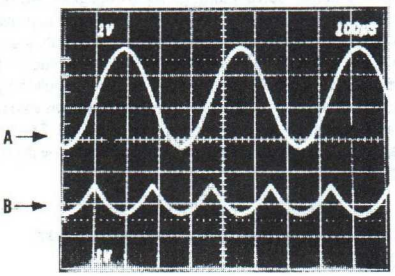
NOTE:
V_R is a fixed reference voltage, OSC frequency, f_{OSC} = 2.9kHz. Phase shift, $\phi = -\tan^{-1}(\omega R_O C_O)$.

a. Typical Single Supply LVDT Measuring Circuit

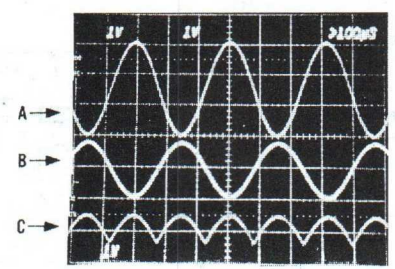
Figure 1.



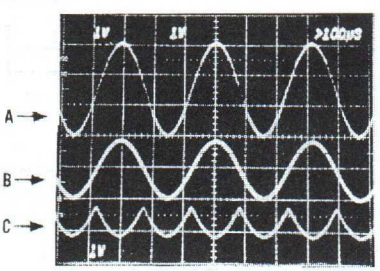
b. Trace A is the Oscillator Signal and Trace B is the Demodulator Output Resulting from LVDT Phase Shift



c. Trace B is the Demodulator Output After Proper Phase Adjustment



b. With LVDT Output (Trace B) at 180° Out of Phase With Excitation Signal (Trace A), the Demodulator Output has Positive Polarity (Trace C)

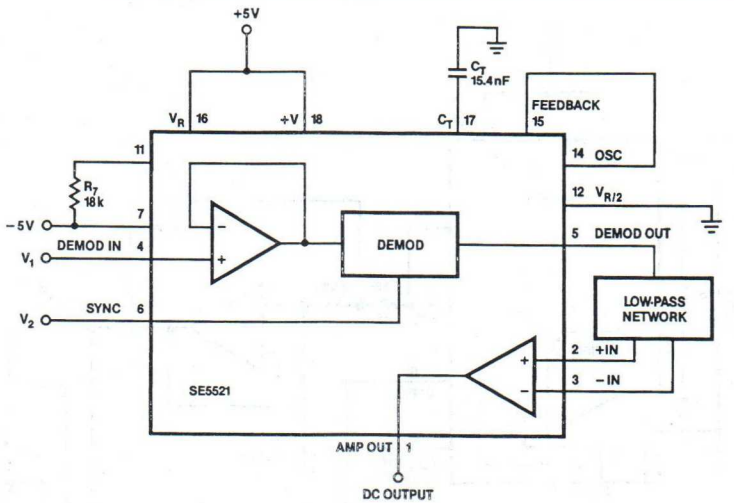


d. Demodulator Output has Negative Polarity (Trace C) When LVDT Output (Trace B) is in Phase With Primary Signal (Trace A)

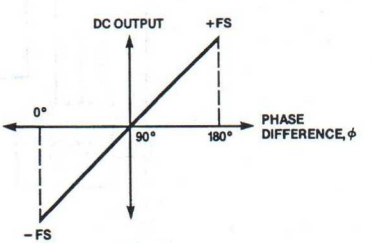
Figure 1 (Continued)

Using the NE5521 signal conditioner in multi-faceted applications

AN1182



a. Phase Detector Measures Difference Between Signals V_1 and V_2 and Provides DC Output at Pin 1



c. When V1 and V2 in (a) are at Quadrature (Traces A and B), the DC Component of Demodulator Output (Trace C) is at 0V

c. The DC Output and Phase Vary Linearly

Figure 2.

Using the NE5521 signal conditioner in multi-faceted applications

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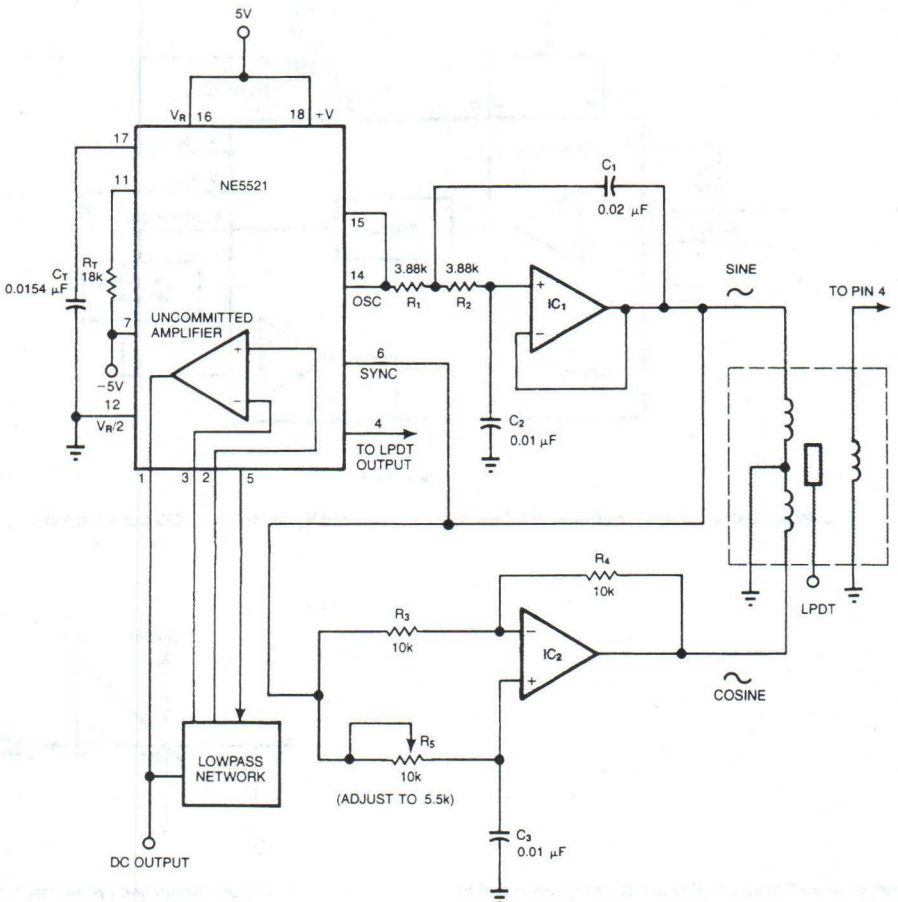


Figure 3.

Using the NE5521 signal conditioner in multi-faceted applications

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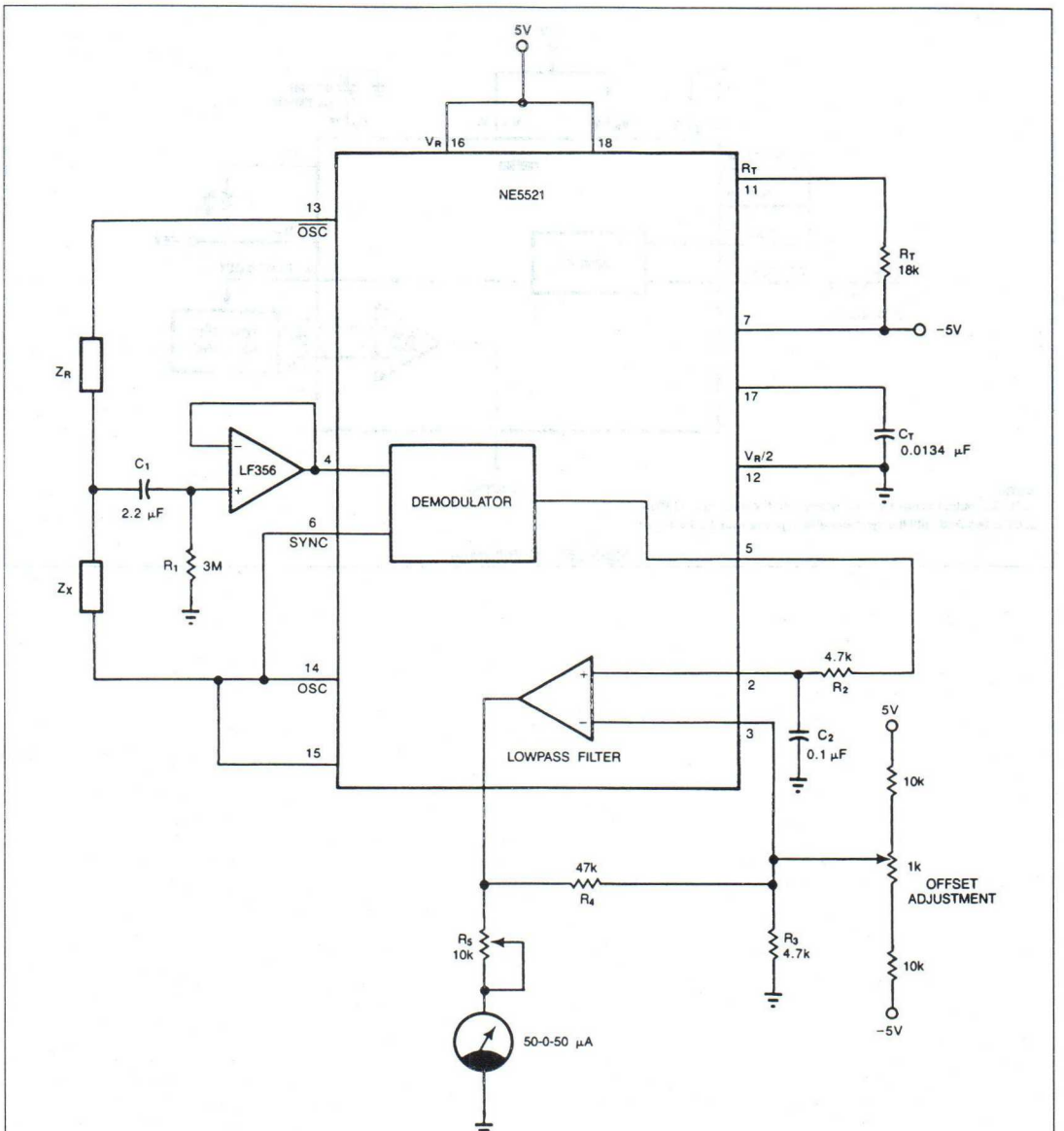
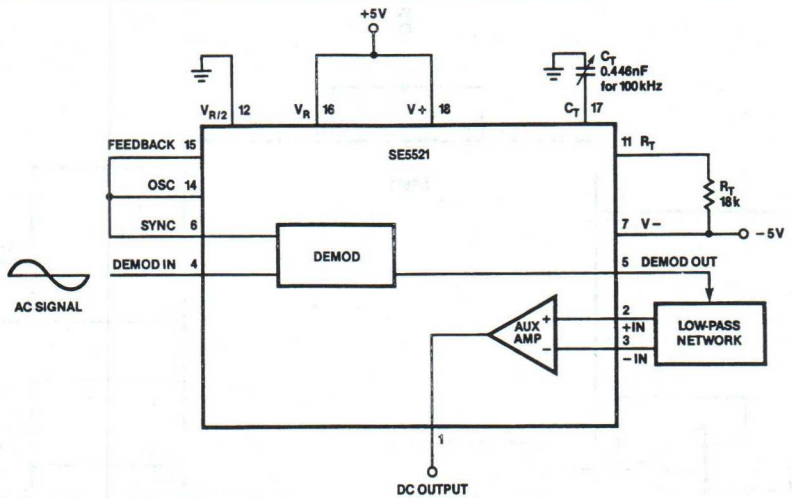


Figure 4. Signal Conditioner Used as an AC Bridge to Calibrate Resistors/Capacitors

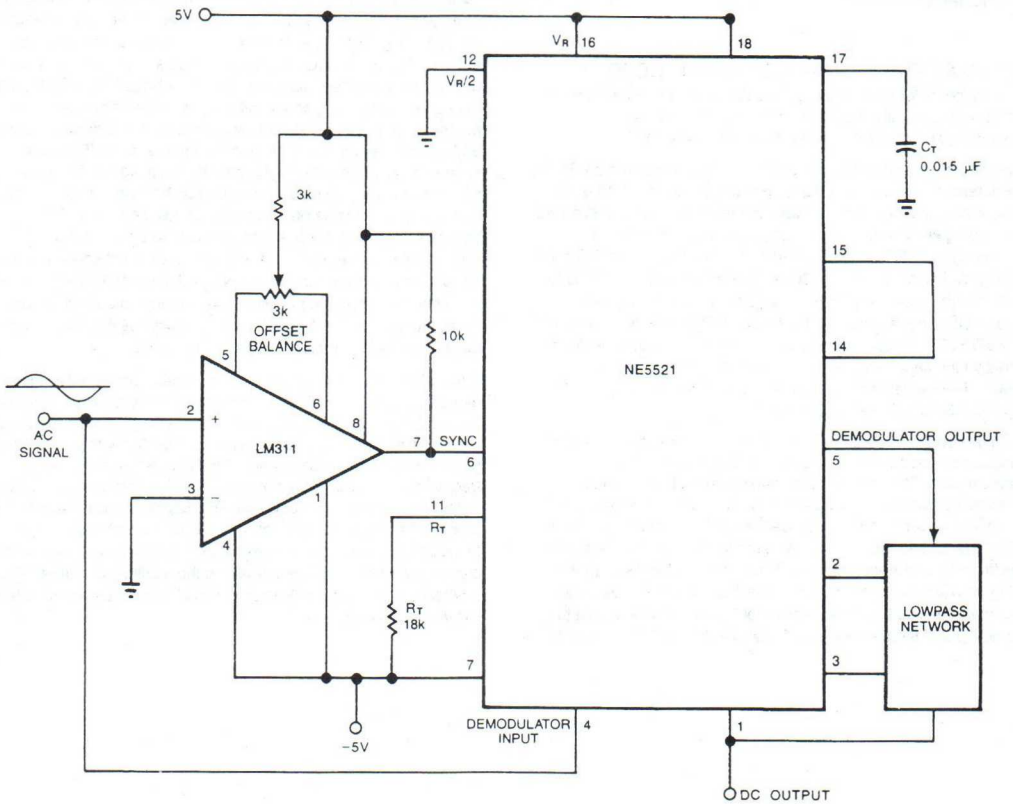
Using the NE5521 signal conditioner in multi-faceted applications

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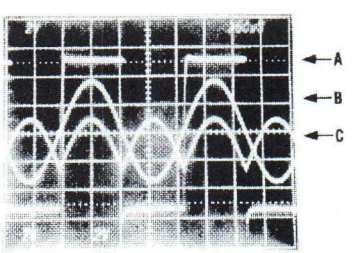


NOTE:
1. The DC output at Pin 1 varies linearly with the RMS input at Pin 4.
2. CT is tweaked until the sync signal is in phase with the AC signal.

Figure 5. AC Voltmeter



a. AC Voltmeter. Comparator CI (LM311, Used as a Zero-Crossing Detector, Produces a Constant Amplitude Square Wave to Excite the Sync Input of the Demodulator. DC Output Appears at Pin 1



b. Trace B is the AC Signal at the Comparator and Demodulator Input. The Output of the Zero-Crossing Detector (Trace A) at Sync Input Causes Synchronous Rectification at the Demodulator Output (Trace C). Auxiliary Amplifier Filter Produces DC Output at Pin 1

Figure 6.

Using the NE5521 signal conditioner in multi-faceted applications

AN1182

APPENDIX I

A LOOK AT THE SIGNAL CONDITIONING IC

The signal conditioner essentially consists of three major blocks: an oscillator with programmable frequency, a synchronous demodulator, and an auxiliary amplifier (see Figure 7).

The oscillator generates a stable amplitude sine wave with an RMS value determined by a fixed reference voltage, V_R, at Pin 16 of the device, and referenced to $V_{R/2}$. Next, the oscillator signal is buffered by two high-gain, low-offset op amps to produce the buffered oscillator signal, OSC, and the inverted signal, $\overline{OSC}$. The OSC and $\overline{OSC}$ signals exhibit less than 50ppm/°Camplitude drift (at -55°C to +125°C temperature range) with total harmonic distortion under 2%. OSC and $\overline{OSC}$ signals are used to differentially excite the primary of the LVDT/RVDT. A fixed 18k resistor, R_T (external to chip), and an external timing capacitor, C_T, determine the frequency of the oscillator. The oscillator frequency is given by the following: $f_{OSC}=(V_R\text{-}1.3V)/[V_R(R_T+1.5k\Omega)\ C_T]$.

The signal conditioner employs a synchronous demodulatorulation technique to extract position and phase information of the transducer core. The synchronous demodulator block not only conditions the transducer output to provide usable information, but also provides a very high impedance load to the transducer output (on the order of several MΩ for maximum linearity and for relative insensitivity to frequency drift (see "How an LVDT Works", Figure 11). Figure 8 shows how the demodulator functions. The oscillator signal, which is also the primary drive for the transducer, is tied to the sync input of the demodulator. Note that the OSC signal and the transducer output (demodulator input) are both referenced to $V_{R/2}$. The sync signal is compared to an internally-generated reference voltage, $V_{R/2}$. During the first half-cycle, as the sync signal goes above $V_{R/2}$, the demodulator functions as an inverter and, thus, the demodulator input appears inverted at the output. However, during the second half-cycle, as the sync signal goes below $V_{R/2}$, the demodulator functions as a follower and, thus, the demodulator input appears at the output with unity gain. Full-wave rectification thus occurs in synchronism with the primary drive signal. The amplitude of the rectified signal tells the position of the core, while the polarity of the output indicates on which side of null the core is. The demodulator offset is measured at less than 2mV with 5μV/°C offset drift, and linearity error is measured at ±0.05% full-scale (at -55°C to +125°C temperature range). A low offset is essential for transducer systems in precision applications since a high offset will not only mask the transducer null, but will also make position measurements inaccurate as the ambient temperature varies.

Since all readout devices (meters, recorders, etc.) are DC input devices, the AC output of the demodulator has to be converted to filtered DC before being applied to the readouts. Consequently, an on-chip amplifier may be used as an active filter with programmable gain for the demodulator output. The filter removes the carrier frequency and other higher-order harmonics from the demodulator output and produces a ripple-free DC output. The amplifier exhibits an open-loop gain of 380V/mV (typical) and 0.5mV input offset (typical). DC offsets from the transducer/signal conditioner system can be nulled by offset adjustment at the auxiliary amplifier. The device operates from 4.5V to 22V with single supply, or ±2.25V to ±11V with dual supplies.

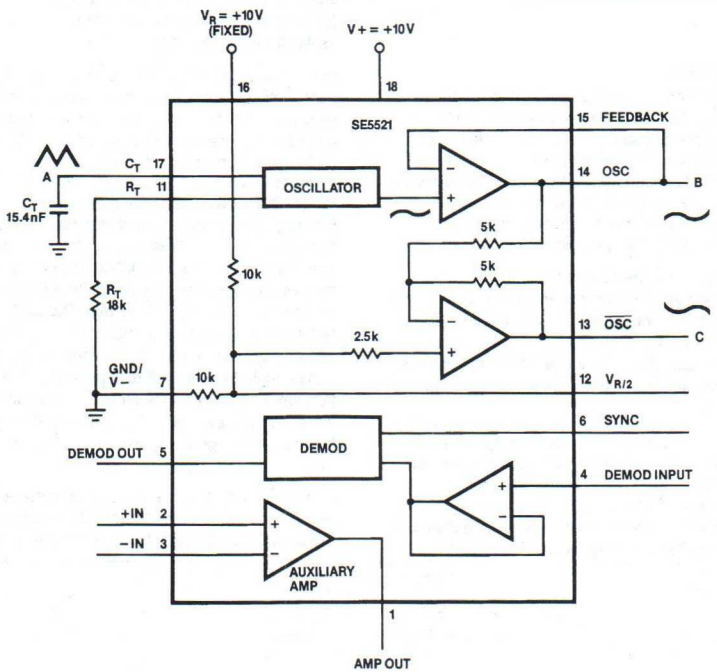


Figure 7. SE5521 Block Diagram

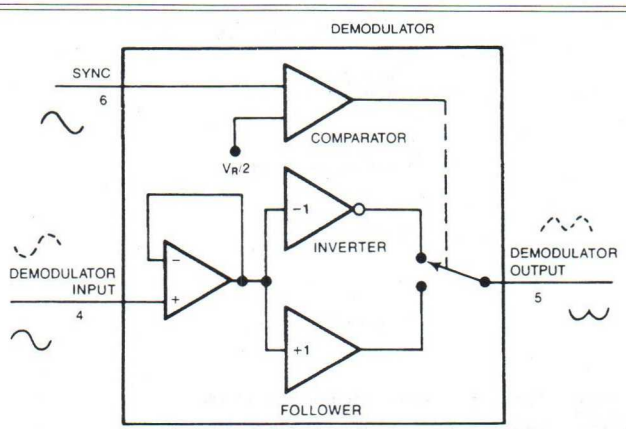


Figure 8. Synchronous Demodulator Full-Wave Rectifies the Demodulator Input Signal in Synchronization With the Sync Signal at Pin 6

Using the NE5521 signal conditioner in multi-faceted applications

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APPENDIX II

HOW AN LVDT WORKS

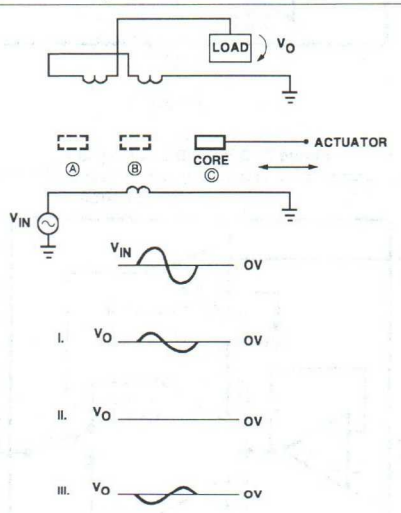
Linear Variable Differential Transformers (LVDTs) are position transducers that have long been used to measure very small displacement and any parameter that can be converted to linear motion. LVDTs are mutual inductance devices consisting of a primary winding and a pair of secondary windings that are wound on an insulated bobbin, and a non-contacting magnetic core capable of free motion inside the transformer. The secondaries are tied together externally in a series-opposing configuration.

With AC excitation at the primary, the core controls the coupling between the primary and the secondaries and produces a differential voltage across the secondaries. The magnitude of the voltage across the secondaries varies linearly with core displacement and contains both the position and phase information (direction of motion) of the core with respect to the center of the secondaries (null position).

With the core at null, the voltage induced at each secondary is equal and of opposite phase; thus cancellation occurs, resulting in a zero AC output. As the core traverses away from the null position, a sinusoidal voltage is developed across the secondaries, the amplitude of which contains the position information. Once the core moves through null, a 180° phase reversal occurs in the output signal with respect to the primary signal. Direction of the core (phase information) with respect to the null position is thus indicated as illustrated in Figure i.

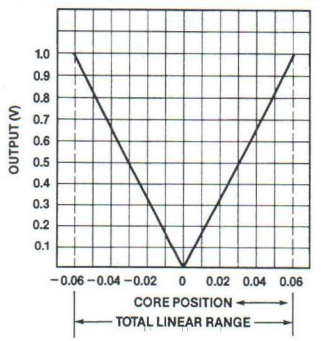
In order to obtain any useful information, some form of signal conditioning is required. Figure 10 shows the DC output of the LVDT as a linear function of the core position after proper signal conditioning. The output voltage of the LVDT is directly proportional to the excitation voltage; therefore, it is essential that the excitation signals have a constant amplitude over the operating temperature range. Output voltage also varies with the excitation frequency. However, the change is not directly proportional to frequency, as shown in Figure 11. Most LVDTs show a small amount of phase shift between the excitation signal at the primary and the output signal at the secondaries. The phase shift introduces a DC offset at null and thus tends to mask the LVDT null. The LVDT null voltage may be reduced by exciting the primary at a frequency where both the primary signal and the output signal are in phase—this is the zero phase angle frequency. Exciting the LVDT at its zero-phase angle frequency optimizes linearity and repeatability of the measurements, while a high impedance load at the LVDT output eliminates the need for frequency regulation, as can be observed from Figures iiia and iiib.

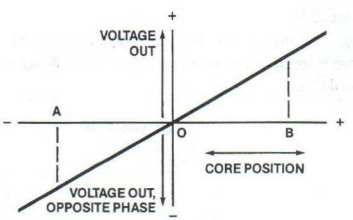
Another popular position transducer is the Rotary Variable Differential Transformer (RVDT). The RVDT operation is analogous to the LVDT, except that the core motion is rotary.



NOTES:
1. With core at a, output is in phase with input. Output amplitude decreases as core moves from A to B.
2. AC output is zero when core is at B (null).
3. Output amplitude increases as core moves from B to C, output is 180° out of phase with respect to input.

Figure 9. The LVDT Output Signal Changes Relative to Core Position





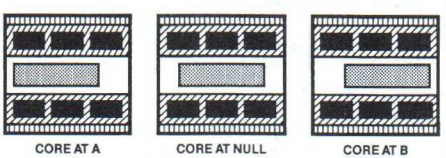
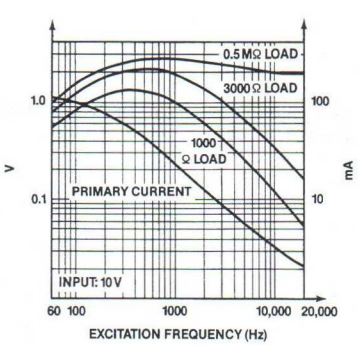
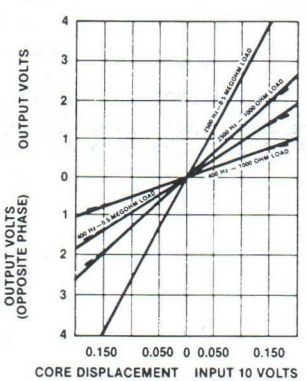


Figure 10. Absolute Magnitude of Output Voltage (Left) and Phase-Referenced Output Voltage (Right) as a Function of LVDT Core Position (Courtesy Schaevitz Engineering)



a, Nominal Full-Scale Output at Various Loads and Primary Current vs Ecitation Frequency for a Typical LVDT



a, Output Characteristics of a Typical LVDT for Various Loads and Excitation Frequencies (Courtesy Schaevitz Engineering)

Figure 11.

APPENDIX III

LPDT CHANGES PHASE INSTEAD OF AMPLITUDE

A recently developed linear position transducer, the LPDT (Linear Phase Differential Transformer), produces a phase output linear with the core motion. The transducer construction is similar to the LVDT, the main exception being that there are six primary coils which are wound on a bobbin at a slant. The excitation to the transducer primaries consists of a sine wave and a cosine wave of equal magnitude. The output at the secondary is an AC signal of constant amplitude, which is the vector sum of the sine and cosine excitation

signals, with a phase angle that varies linearly with core position. Figure 12 shows how the transducer is energized.

REFERENCES

1. Handbook of Measurement and Control, Revised Edition 1976, by Edward Herceg, Schaevitz Engineering Publication, Pennsauken, New Jersey.
2. Philips Semiconductors Linear LSI Data and Applications Manual, 1985 Edition, pg 4-212, 9-41. Philips Semiconductors Corporation, Sunnyvale, CA, 94086.
3. Frank Yeaple, "Linear Position Transducer Changes Phase Instead Of Amplitude", Design News, November 5, 1984, pg 180.

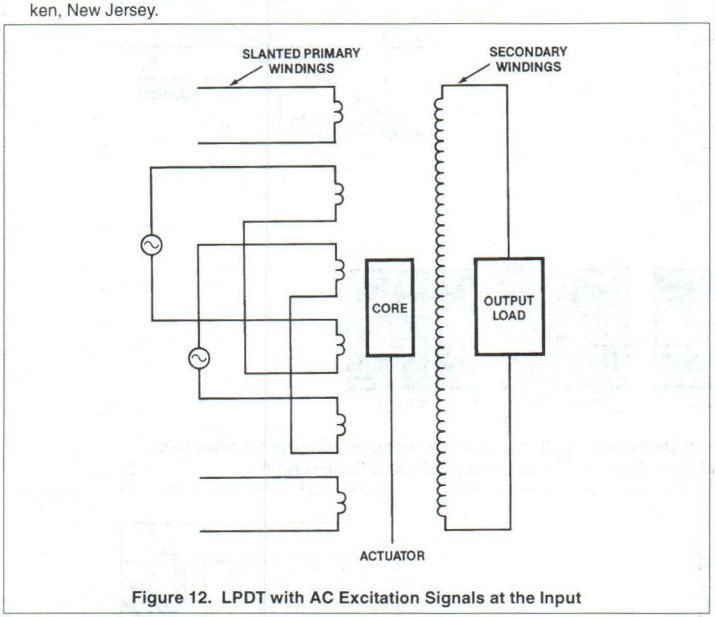


Figure 12. LPDT with AC Excitation Signals at the Input

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Section 14
Battery Management/DC Voltage Detection and Control Circuits

INDEX

SAA1500T	State-of-charge indicator for NiMH and NiCd powered applications	921
TEA1041T	Battery low-level indicator	938
TEA1088T	Switched-mode power supply battery charger control circuit	946
TEA1100;TEA1100T	Battery monitor for NiCd and NiMH chargers	959
TEA1101;TEA1101T	Battery monitor for NiCd and NiMH chargers	972
TEA5500TEA5500T	Coded locking circuit for security systems	986
TEA5501	Coded locking circuit for security systems (one-shot output; 6.5k codes)	995
74LV4799	Timer for NiCd and NiMH chargers	1005

State-of-charge indicator for NiMH and NiCd powered applications

SAA1500T

FEATURES

- 5-segment state-of-charge indication for LED or LCD displays
- Numerous display facilities to indicate the operational modes
- Designed for constant charge and varying discharge currents
- Large dynamic range of discharge currents
- Independent setting for charge and discharge efficiency
- Battery self-discharge compensation
- Automatic switch-over from fast to trickle charge (to prevent overcharging)
- Low standby current for permanent integration into a battery pack.

APPLICATIONS

- Intelligent battery powered, portable, applications with 'remaining energy' indication and fast charge control.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		1.8	–	7.0	V
I_{CC}	supply current	V_{CC} = 2.6 V; V_{CI} = 0 V	–	–	90	µA
f_{OSC}	fixed frequency	charging	–	4.2	–	kHz
V_{CI}	input sense voltage	discharging	20	–	200	mV
T_{amb}	operating ambient temperature		0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA1500T	20	SO20L	plastic	SOT163AH

State-of-charge indicator for NiMH and NiCd powered applications

SAA1500T

INTRODUCTION

More and more portable appliances are being used because they can operate independently from power sources such as mains or car batteries (see Fig.1). In many cases, NiCd (powerful appliances) and NiMH (environment) rechargeable batteries are used. Because of the constant voltage of these batteries, it is not the energy (Wh) but the charge amount (Ah) that has to be known to enable the state-of-charge indication. In systems with known charge and discharge currents, time is an equivalent for the charge amount in the battery ($t = Q/I$). The charge time can be registered easily on a counter.

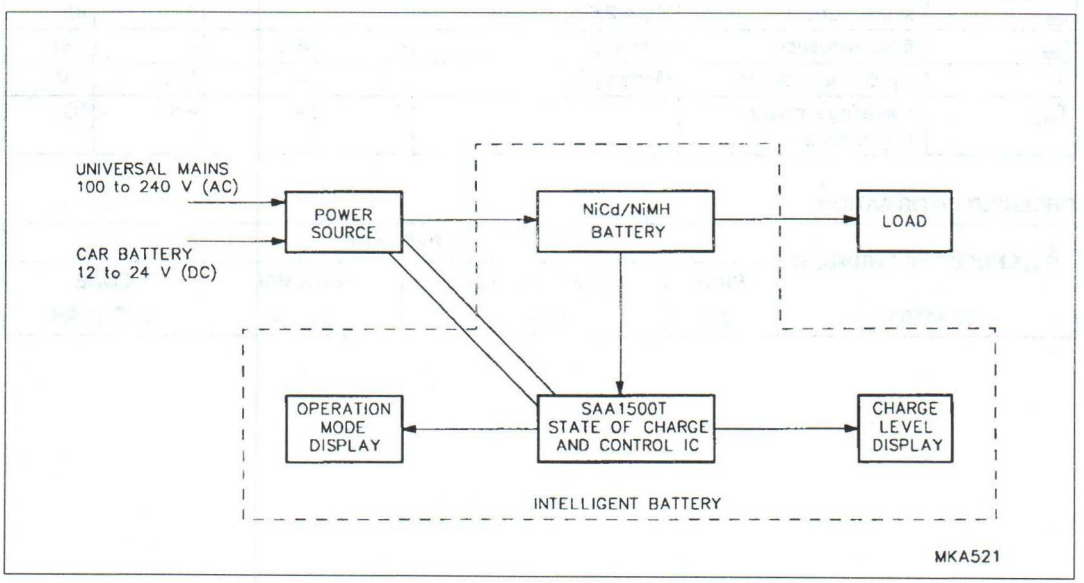
The system can be made universal by adapting the counting frequency to the used battery type, thereby making the counter contents a reflection of the energy state of the battery. The requirements of a battery state-of-charge indicator are in many ways similar to those of a fuel gauge for a car.

The SAA1500T is designed for enhanced systems with varying discharge currents. A variety of loads can discharge the battery without disturbing the charge account. If the equivalent of the charge counter contents is known in the SAA1500T, then the following information can be made available:

- The state-of-charge, indicated by LED or LCD displays
- The battery low state, indicated by LED and acoustic alarms
- The full state. A control signal can automatically switch the charge current from a fast to a trickle level to prevent overcharge.

The state-of-charge indication is an important and useful addition to any rechargeable battery pack for a variety of reasons. An underlying problem is the common tendency to recharge batteries many times, in fact more often than actually necessary. People waste time and effort in this way because they are always afraid of being caught out with flat batteries. The state-of-charge indicator helps to overcome this problem and brings other benefits such as:

- Increased battery cycling and consequently improved battery performance and lifetime
- Enhanced customer satisfaction
- Excellent selling feature.



State-of-charge indicator for NiMH and NiCd powered applications

SAA1500T

GENERAL DESCRIPTION

The SAA1500T is manufactured in a low voltage SACMOS process and has been designed for use as a battery state-of-charge indicator and as a battery charge controller for rechargeable batteries. In principle only four states exist (but because of two charging levels, fast and trickle charge), six states can be considered for the batteries; fast and trickle charge, fast and trickle charge and discharge at the same time, standby and battery discharge (see Fig.2 State diagram).
During charging, activated by power-on, the charge rate increases linearly with the charge time (assuming constant charge current). During discharge, activated by the 'load switch ON', the charge rate decreases linearly with the discharge time and the discharge current level. During charge/discharge, the charge rate is kept constant. In standby, the charge rate is decreased to compensate for the battery self-discharge.
In the SAA1500T, the known charge current and the measured discharge current are transferred in up/down oscillator pulses. By book-keeping the pulses, an image of the battery charge is created in the counter. The contents of the counter are output via 5 LEDs or a 6 segment LCD bar graph display. Two signal outputs are available to drive the LEDs to indicate whether the batteries are being charged or to indicate the nearly empty state.

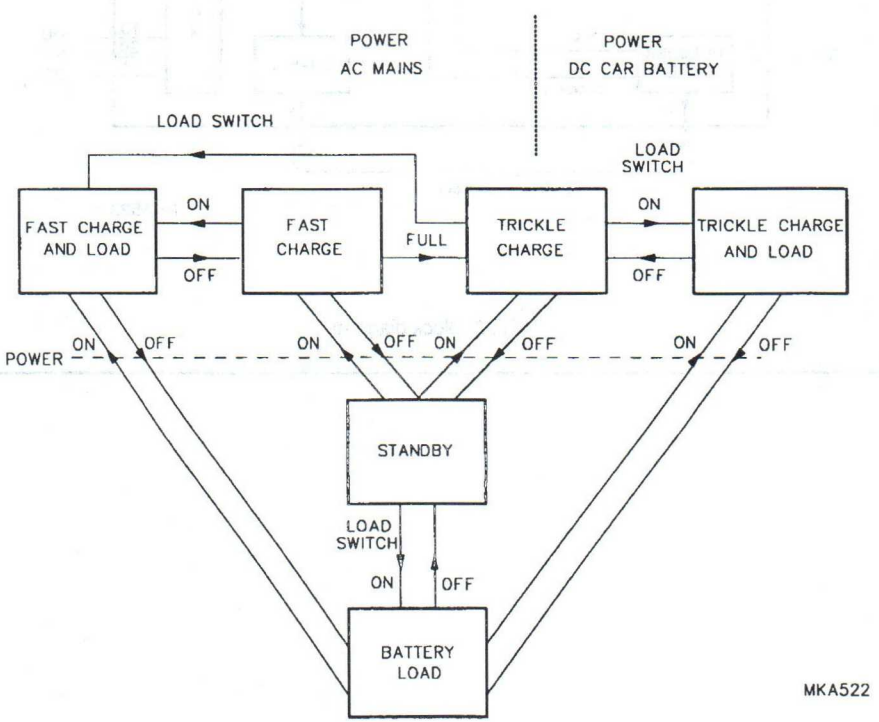


Fig.2 State diagram.

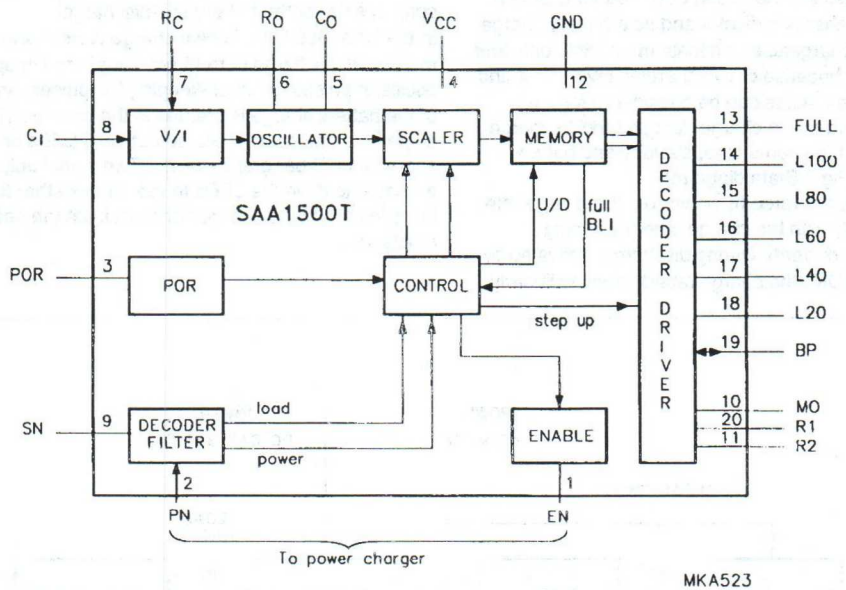


Fig.3 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
EN	1	enable control signal for battery charge unit
PN	2	power NOT mode detection
POR	3	power-on-reset, reset at LOW battery voltage
V_{CC}	4	supply voltage
C_O	5	capacitor for oscillator frequency
R_O	6	resistor for charge or self-discharge oscillator frequency
R_C	7	resistor to convert sense input voltage
C_I	8	discharge current sense input
SN	9	switch NOT, load switch ON detection
MO	10	mains ON state indication
R2	11	battery LOW drive signal for external buzzer
GND	12	ground
FULL	13	battery FULL indication, only LCD
L100	14	100% indication, LCD or LED driven
L80	15	80% indication, LCD or LED driven
L60	16	60% indication, LCD or LED driven
L40	17	40% indication, LCD or LED driven
L20	18	20% indication, LCD or LED driven
BP	19	backplane, (LCD), LCD/LED mode detection input
R1	20	battery LOW indicator, LOW drive

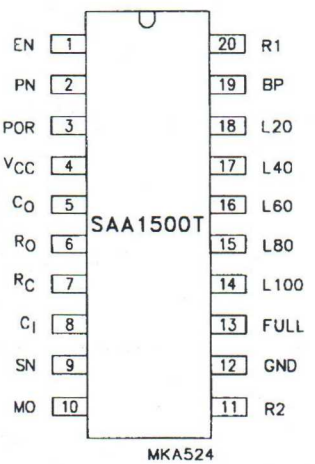


Fig.4 Pin configuration.

FUNCTIONAL DESCRIPTION

Power-on-reset

The POR circuit resets all counters if the supply voltage rises from 0 to V_{CC}. Reset is performed before V_{CC} = 1.8 V.
If the rise time of V_{CC} is fast, an external resistor and capacitor ensure the minimum pulse width of the internal reset pulse. If the rise time of V_{CC} is slow, the POR circuit acts as a level detector. The counters are also reset before V_{CC} = 1.8 V.

Oscillator (see Fig.5)

An RC type oscillator is used in the SAA1500T. The HIGH and LOW switching levels, and thus the voltage swing of the oscillator, are derived from V_{CC}. The timing components are designed so that the oscillator frequency is at V_{CC} and temperature independent.

The rise and fall times of the oscillator period are:

$t_r = R_O \times C_O \times \ln 2$; $t_f = R_O // 10\ k\Omega \times C_O \times \ln 2$;
$t_u \approx 15\ \mu s$ (9.1)

t_u is the undershoot time. The timings given in the specification are referenced to a fixed frequency of 4.2 kHz. Table 1 gives the modes at which the fixed frequency is active.

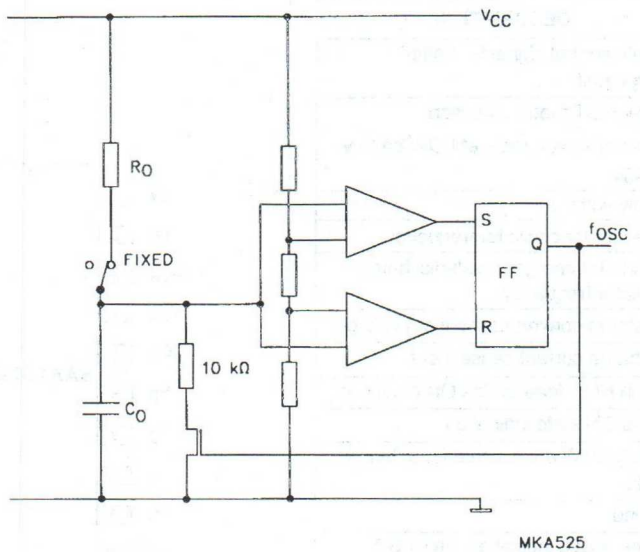


Fig.5 Fixed oscillator frequency.

V/I convertor (variable frequency)

The discharge current is sensed over a low ohmic (less dissipation) resistor R_{sense} (70 mΩ). In the voltage-to-current block (V/I), the sense voltage is converted into a current and this current is used to charge the oscillator capacitor C_O, (see Fig.6).

The period time can be calculated using the following equation:

$t_r = (C_O \times V_{CC} \times R_{conv})/(3 \times I_{load} \times R_{sense})$;
$t_f \approx 10\ k\Omega \times C_O \times \ln 2$; $t_u \approx 15\ \mu s$ (9.2)

The rise time is the dominating factor, and so it is clear that the countdown frequency is proportional to the discharge current .
In the discharge mode the frequency is V_{CC} dependent. However, as the battery voltage is rather insensitive to the battery charge, this influence is low.
The input voltage to the V/I block ranges from 20 mV to 200 mV. Outside of this range it is less accurate (see Fig.7).

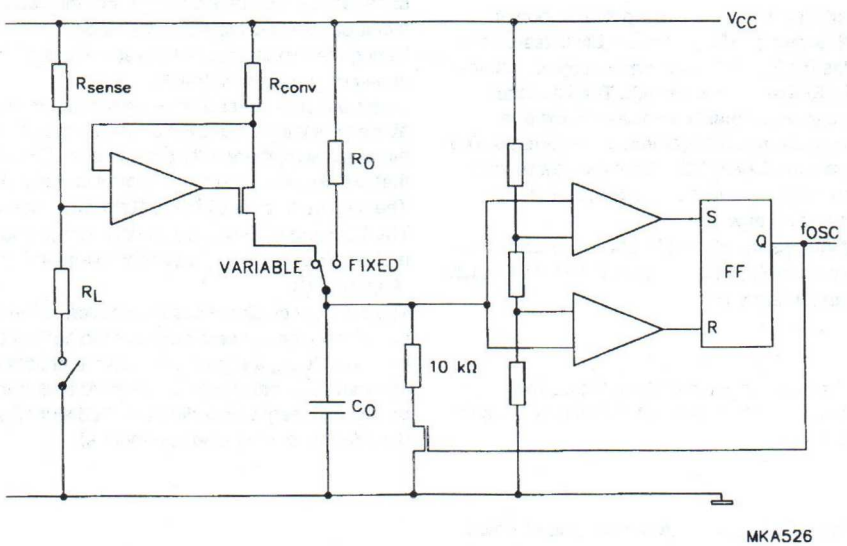


Fig.6 Variable oscillator frequency.

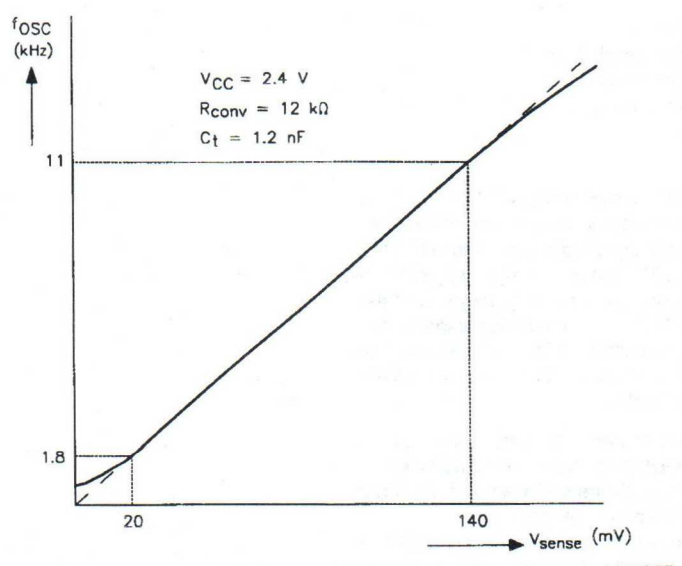


Fig.7 Voltage to frequency conversion.

Decoder filter

In the decoder filter block, the two inputs PN (power NOT) and SN (switch NOT) are tested. SN is tested on two logic states (HIGH and LOW) and PN on four states (HIGH, LOW, >5Ffixed and <3Ffixed). The inputs are digitally filtered to make them insensitive to external interference caused by motor commutation currents. The PN input informs the SAA1500T about the power charge unit state. The most important states are; fast charge, trickle charge and no power.
The SN input informs the SAA1500 about the load state. Two states are possible, load or no load. The load switch is sensed for that information.

Memory

The memory has a fixed volume of ten times. The memory contents (= battery charge) will be output via the decoder/driver block.

Scaler

In the scaler, a scale factor is introduced to scale down the memory counting frequency. In the trickle and standby modes, the battery current is adapted and so the memory counting frequency is changed accordingly. For the following modes, fixed scale factors are programmed:

- fast charge = 7.37×10^5
- trickle charge = 32 x fast charge
- standby = 150 x trickle charge
- discharge mode = 8.85×10^5.

Control

In the control block, in co-operation with the decoder/filter, six user modes and two test modes are provided together with appropriate signals to select the correct scale factors. The pin control signals, the different modes of operation, the oscillator frequency and scale factors are given in Table 1. The direction of the scale factor, up or down, is dependent on the mode, and thus determined in the control block. Four user modes have been explained previously.

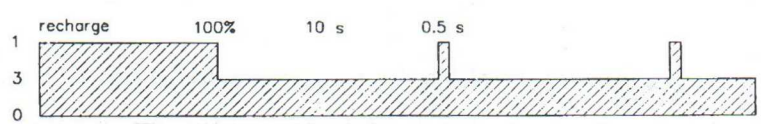
In the 'trickle charge and load mode', the discharge current is nearly always much higher than the trickle charge level, consequently the scale factor is chosen to be the same as in the discharge mode.
In many cases a motor is driven in the 'fast charge and load mode'. The control pin EN switches the system from a current source to a voltage source regulation to keep the motor speed constant. This ensures that only the current demanded by the motor will be delivered and the batteries will remain unaffected. For this reason a scale factor of zero is selected in this mode.
During the two test modes the scale factor is set at 1 to speed up the counter checks.
Step-up means that LEDs are switched on successively at the beginning of an LED display. If the LEDs are already active, there will be no step-up. Only those LEDs that are concerned with the charge status are activated. The step up frequency is $2 \times 10^{-3} \times f_{osc}$ (see appendix B).
The LED and LCD display, during charge and discharge, is illustrated in Fig.12 (Appendix A) and in Fig.13 (Appendix B).
The memory block passes information to the control unit concerning the extreme states of the battery charge. At batteries FULL, a signal is sent to the enable block to terminate the fast charge session. At batteries almost empty, a Battery Low Indication (BLI) signal is sent to the decoder/driver (see also appendix A).

Table 1 Modes of operation.

INPUTS		MODES OF OPERATION	INDEX	OSCILLATOR FREQUENCY	SCALE FACTOR
PN	SN				
L	L	test, very fast down count	TD	fixed	512
<3Ffix	L	trickle charge and load, count down	TCL	variable	885k
>5Ffix	L	fast charge and load, no count	FCL	fixed	0
H	L	battery load, count down	BL	variable	885k
L	H	test, very fast up count	TU	fixed	512
<3Ffix	H	trickle charge, slow up count	TC	fixed	23M6
>5Ffix	H	fast charge, fast up count	FC	fixed	737k
H	H	standby, self discharge, POR active	SB	fixed	7G1
H	H	standby, self discharge, after POR	SB	fixed	3G5

Enable

It is possible to use the enable output (EN) to control the fast charge on the batteries. The EN signal is HIGH when the indicator shows not full. When an LED bar-graph is used and it shows FULL, then the EN signal will pulsate between HIGH and OPEN states. This provides a pulsating trickle charge waveform with a 5% duty factor for a 10 second period to compensate for the LED currents. If an LCD bar-graph is used, then at the full state, the EN output goes into a continuous high impedance state (see Fig.8).



0 = V_{SS}
1 = V_{CC}
3 = 3-state; high impedance
EN signal with LED bar graph applied.
With LCD bar graph, the signal is continuously 3-state after 100%.

MKA528

Fig.8 Waveform of enable signal with full batteries.

Decoder driver

The SAA1500T is intended to display the charge of the batteries in a six segment LCD bar graph or five segment LED display. LED indication is also given for batteries nearly empty, batteries on recharge and batteries full during recharge. Outputs L100, L80, L60, L40, L20 and FULL are designed to drive an LCD bar-graph with output BP connected to the backplane of the LCD. The LCD segment is active if the segment voltage is in antiphase with the BP voltage. If, however, BP is connected to ground (V_{SS}), then outputs L100, L80, L60, L40 and L20 may drive the LEDs directly with their anodes connected to the positive supply (V_{CC}). Outputs MO and R1 can drive LEDs directly. Output MO indicates batteries on recharge (LED constantly ON) and batteries full while recharging (LED flashes). Output R1 indicates that the battery is nearly empty. Output R2 provides a second battery nearly empty signal which can be used to drive a simple electroacoustic transducer with an audio tone via an external transistor. Circuit waveforms are illustrated in Fig.9.

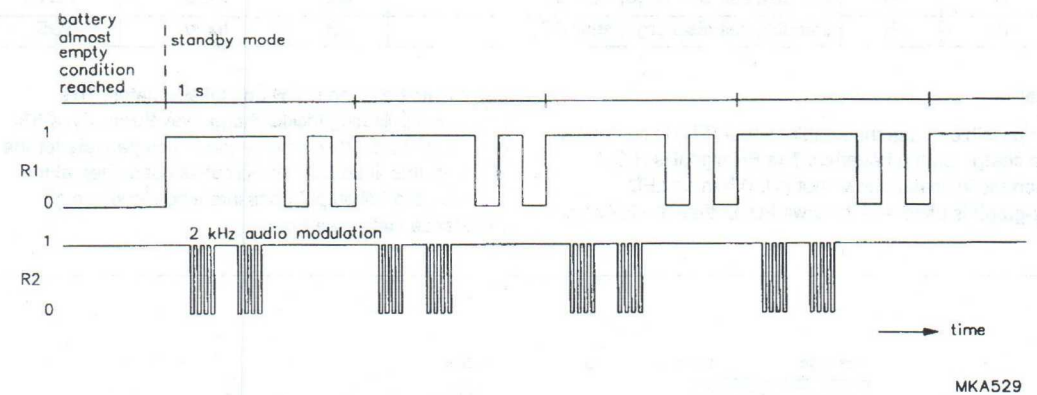


Fig.9 Waveform of R1 and R2 signalling empty batteries.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		−0.5	7.0	V
V_I	input voltage	note 1	−0.5	V_{CC}+0.5	V
V_O	output voltage	note 1	−0.5	V_{CC}+0.5	V
I_{CC}	supply current		−	40	mA
I_{SS}	supply current		−	−120	mA
I_I	input current		−	±10	mA
I_O	output current		−	±20	mA
T_{amb}	operating ambient temperature		0	+70	°C
T_{stg}	storage temperature		−65	+150	°C

Note

1. V_{CC} + 0.5 V must not exceed 7.0 V.

DC CHARACTERISTICS

T_{amb} – 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OH}	HIGH level output voltage (pins 13 and 19)	V_{CC} = 2.4 V; I_O = –650 µA	2.0	–	–	V
V_{OH}	HIGH level output voltage (pins 1 and 11)	V_{CC} = 2.4 V; I_O = –1 mA	2.0	–	–	V
V_{OH}	HIGH level output voltage (pins 10, 14 to 18 and 20)	V_{CC} = 2.4 V; I_O = –300 µA	2.0	–	–	V
V_{OL}	LOW level output voltage (pins 13 and 19)	V_{CC} = 2.4 V; I_O = 650 µA	–	–	0.4	V
V_{OL}	LOW level output voltage (pin 11)	V_{CC} = 2.4 V; I_O = 1 mA	–	–	0.4	V
V_{OL}	LOW level output voltage (pins 10 14 to 18 and 20)	V_{CC} = 3.8 V; I_O = 15 mA	1.8	–	–	V
		V_{CC} = 2.4 V; I_O = 5 mA	–	–	0.55	V
$\|I_{LO}\|$	output leakage current (pins 1 and 19)	V_{CC} = 3.8 V; V_O = V_{CC} or 0 V	–	–	±1	µA
$\|I_{LI}\|$	input leakage current (pin 3)	V_{CC} = 3.8 V; V_3 = 0 V	–	–	1	µA
$\|I_{LI}\|$	input leakage current (pin 2)	V_{CC} = 3.8 V	–	–	1	µA
I_9	input current (pin 9)	V_{CC} = 2.4 V	30	–	80	µA
V_{ihs}	Schmitt trigger HIGH (pins 2, 9 and 19)	V_{CC} = 2 V	1.6	–	–	V
		V_{CC} = 4 V	2.2	–	–	V
V_{ils}	Schmitt trigger LOW (pins 2, 9 and 19)	V_{CC} = 2 V	–	–	0.4	V
		V_{CC} = 4 V	–	–	0.18	V
V_{hys}	hysteresis voltage (pins 2, 9 and 19)	V_{CC} = 2 V	0.4	–	–	V
		V_{CC} = 4 V	0.5	–	–	V
V_{IH}	HIGH level input voltage (pin 3)	V_{CC} = 3.8 V; I_3 = 1 µA	0.8	–	1.5	V
		V_{CC} = 1.8 V; I_3 = 1 µA	–	–	1.55	V
V_{IL}	LOW level input voltage (pin 3)	V_{CC} = 1.8 V; I_3 = 1 µA	–	–	1.55	V
I_5	input current (pin 5)	V_{CC} = 2.4 V; V_5 = 2.4 V	150	–	360	µA
I_{CC}	supply current	V_{CC} = 2.6 V; V_3 = V_8 = 0 V; V_5 = V_7 = 0 V	–	–	90	µA

AC CHARACTERISTICS

T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{osc}	fixed oscillator frequency	V_{CC} = 2.4 V; R_6 = 260 kΩ C_5 = 1.2 nF; $V_8 = V_2 = V_9$ = 0 V	3.81	4.24	4.67	kHz
Δf_{osc}	variable oscillator frequency	V_{CC} = 2.4 V; V_8 = 56 mV; R_7 = 12 kΩ C_5 = 1.2 nF; PN = 1; SN = 0	4.04	4.65	5.02	kHz
		V_{CC} = 2.4 V; V_8 = 35 mV; R_7 = 12 kΩ C_5 = 1.2 nF; PN = 1; SN = 0	2.47	2.94	3.24	kHz
SVRR	supply voltage ripple rejection	V_{CC} = 2.2 to 2.6 V; V_8 = 49 mV	–	–	5	%/0.1V

QUALITY SPECIFICATION

General quality specification for integrated circuits: UZW - BO/FQ - 601.

APPLICATION INFORMATION

The SAA1500T can be used in many applications with different types and sizes of rechargeable batteries. In the Introduction it is stated that the discharge/charge time is the equivalent of the battery charge.
The formula of the elapsed discharge/charge time and thus the collected charge is (see Fig.3):

discharge/charge time = t_{osc} x scale factor x memory

(1) The fixed time period of the oscillator during charging is given in the following equation:

t_{osc} = (Charge Time) / (scale factor x 10)

Where: the Charge Time (CT) is the time taken to fully charge empty batteries.

Therefore: f_{osc} = 7370 / (3600 x CT [h]) [kHz]; (exclusive efficiency corrections) (13.1)

From formula (13.1) it is clear that the fixed oscillator frequency is dependent on the charge time (and so the charge current) and not on the battery size.
If the charge time and the oscillator frequency are fixed, the external components C_O and R_O can be calculated with formula (9.1). Some examples are given in Table 2.

(2) Many timing functions are related to the fixed oscillator frequency. The most important are the trickle charge and the self-discharge times (see also Table 2).

(3) The variable time period of the oscillator during discharge is given in the following equation:

t_{osc} = (discharge time) / (scale factor x 10)

Therefore: f_{osc} = 8850 / (3600 x DT) [kHz] (13.2)

Furthermore, formulas (9.1) and (9.2) are valid and, combining them with formula (13.2), the external components R_{conv}, and R_{sense} can be calculated:

R_{conv}/R_{sense} ' 500 x 10^3 x Q [Ah] / C_O [nF]; (V_{CC} = 2.4 V) (13.3)

As can be seen from formula (13.3), it is the battery size that is of importance and not the discharge time. Some examples are given in Table 3.

Table 2 Charge components.

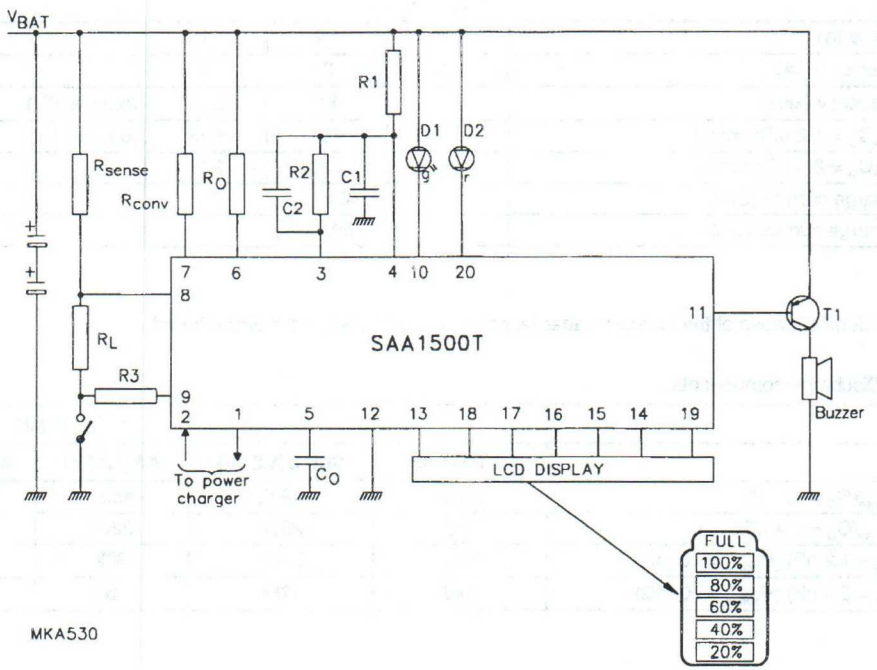
NiXX / xxAh				
charge time (h)	1/3	1/2	1	
charge current (CA)	3	2	1	
fixed frequency (kHz)	6.1	4.1	2.05	formula 13.1
R_O (kΩ) (C_O = 1.2 nF); note 1	180	264	556	formula 9.1
R_O (kΩ) (C_O = 2.4 nF); note 1	90	132	277	
trickle charge current (CA)	1/32 x I_{charge}			
self-discharge current (CA)	1/150 x $I_{trickle}$			

Note

1. C_O > 1.2 nF because of the parasitic capacitance influence on the printed-circuit board.

Table 3 Discharge components.

	NiCd		NiMH	
	AA(600mAh)	Sub C(1.2Ah)	AA(1.1Ah)	AA(1.7Ah)
R_{conv}/R_{sense}(C_O = 1.2 nF)	252k	499k	459k	706k
R_{conv}/R_{sense}(C_O = 2.4 nF)	126k	252k	229k	352k
R_{conv} (C_O = 1.2 nF) (R_{sense} = 70 mΩ)	17k6	34k8	32k	49k3
R_{conv} (C_O = 2.4 nF) (R_{sense} = 70 mΩ)	8k8	17k4	16k	24k6



R1 = 100 Ω; R2 = 1.5 MΩ; R3 = 5.1 kΩ; C1 = 100; C2 = 1.2 nF.

Fig.10 Application diagram for LCD display.

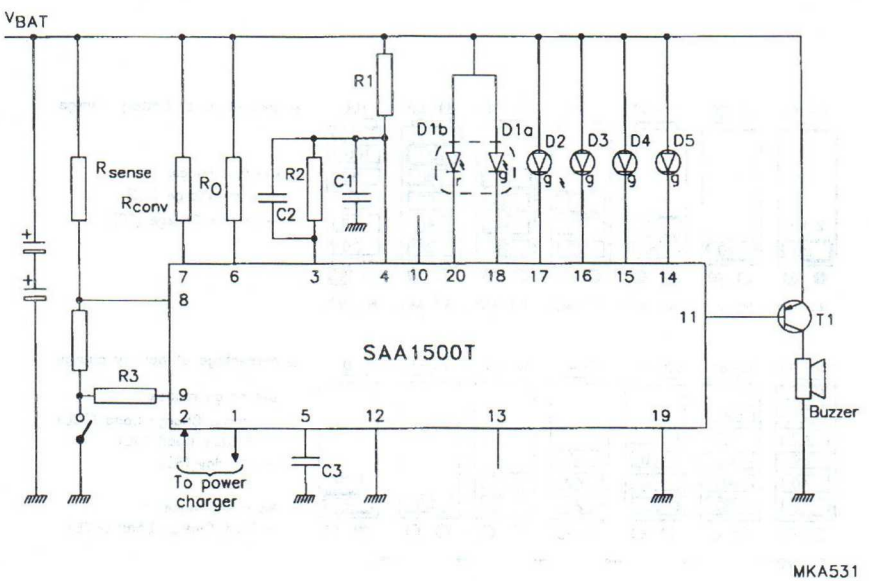


Fig.11 Application diagram for LED display.

APPENDIX A

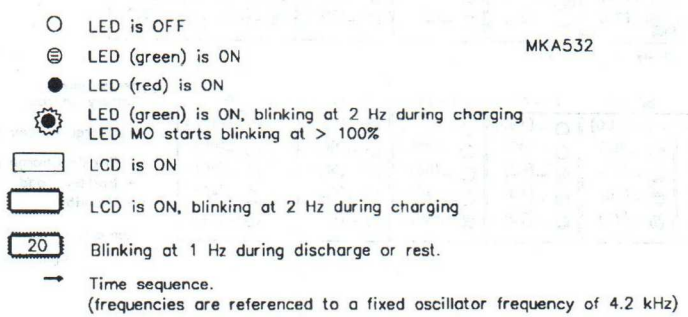


Fig.12 Legend for figure 13.

APPENDIX B

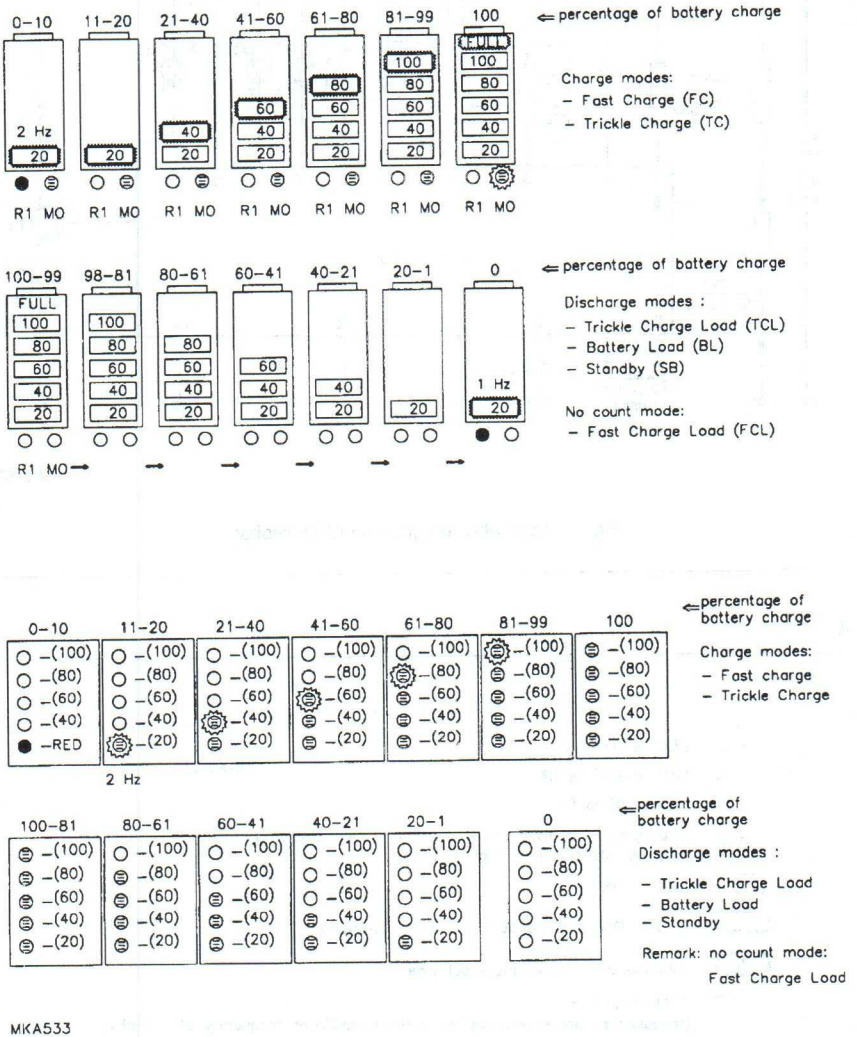


Fig.13 Battery charge displayed by LCD and LED.

Remarks to figure 13

LED mode

The LEDs are activated at every operational mode change. If the LEDs were already active before the mode change, the display will not be changed. If the LEDs were not active before the mode change, a step-up pattern is generated. Step up means that the LEDs are activated successively recording the charge status every 1/8 second. In the Battery Load, Trickle Charge Load and Standby modes, the LEDs are switched off after 8 second. In the Fast Charge, Trickle Charge and Fast Charge Load modes, the LEDs remain on.

Battery Low Indication is active if;

The charging (FC,TC) is stopped (==> standby) before 10% charge is reached.
The discharging (BL, TCL) is started below 10% and stopped (==> SB) above 0%.
The discharging is stopped (==>) at 0%.
For BLI waveforms (see Fig.9) R1 is active before the mode is switched over to standby.

Battery Low Indication is not active if;

Discharging is started above 10% and stopped 10-1%. Instead, the green L20 LED will be active for 8 seconds. If recharging is started during 1-10%. The L20 LED is blinking at 2 Hz, the red LED is not active.

LCD mode

The LCD display, as against the LED mode, is always visible.

Battery Low Indication is active if:

The charging (FC, TC) is stopped (==> standby) before 10% charge is reached.
The discharging (BL, TCL) is stopped (==> SB) at 0% charge.

Battery low-level indicator — TEA1041T

FEATURES

- Optical signal following battery low-level detection
- Additional warning ('recharge needed') at end of system operation
- One or two LED indication
- Trigger level adjustable
- Low stand-by current
- Insensitive to interference
- Few external components

APPLICATIONS

- Battery operated systems

GENERAL DESCRIPTION

Intended for use with battery operated systems, the TEA1041T generates an optical alarm via one or two LEDs when the battery supply voltage falls below a preset threshold level.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_p	supply voltage	1.8	-	4.0	V
I_{sb}	stand-by current	-	-	10	µA
P_{tot}	total power dissipation	-	-	150	mW
I_L	output current LED outputs	-	-	59	mA

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1041T	8	SO8	plastic	SOT96A

FUNCTIONAL DESCRIPTION

Supply (pin 8)

The supply voltage, which may range from 1.8 to 4.0 V, is connected to pin 8.

Voltage sense input (pin 1)

Pin 1 is connected to a trigger circuit consisting of a trigger amplifier and a Schmitt trigger.

An up / down counter in the control and timing logic is enabled when the potential at pin 1 falls below 1.25 V. Unless this voltage increases above 1.25 V the counter will operate for approximately two seconds. When the voltage increases or the count is timed-out, the counter will then begin counting-down. The circuit is thus protected from any disturbance of less than two seconds duration. LED 1 becomes lit on the next occasion that for two seconds the potential on pin 1 is less than 1.25 V.

Following low level detection the circuit is de-activated by operation of S1. For a period of 4 seconds LEDs 1 and 2 will then each be alternately lit for a duration of approximately 500 ms.

LED 1 and LED 2 connections (pin 7, 6)

The cathodes of LEDs 1 and 2 must be connected respectively to pins 7 and 6. The circuit will also function with only LED 1 connected.

Oscillator capacitor connection (pin 4)

Circuit timing is provided by the internal oscillator, the frequency of which is determind by a capacitor connected to pin 4.

Forcing a current (max. 5 mA) into pin 4 permits direct monitoring of the trigger circuit at pins 6 and 7. When V_i is above 1.25 V, pin 7 will be LOW and pin 6 will be HIGH. Alternatively, when V_i is below the 1.25 V threshold level pin 7 will be HIGH while pin 6 will be rendered LOW. This feature facilitates easier circuit adjustment.

Pin 2 Test Pin

An external clock signal may be connected to pin 2 for test purposes. This may be used to shorten the test time (see also test and application information).

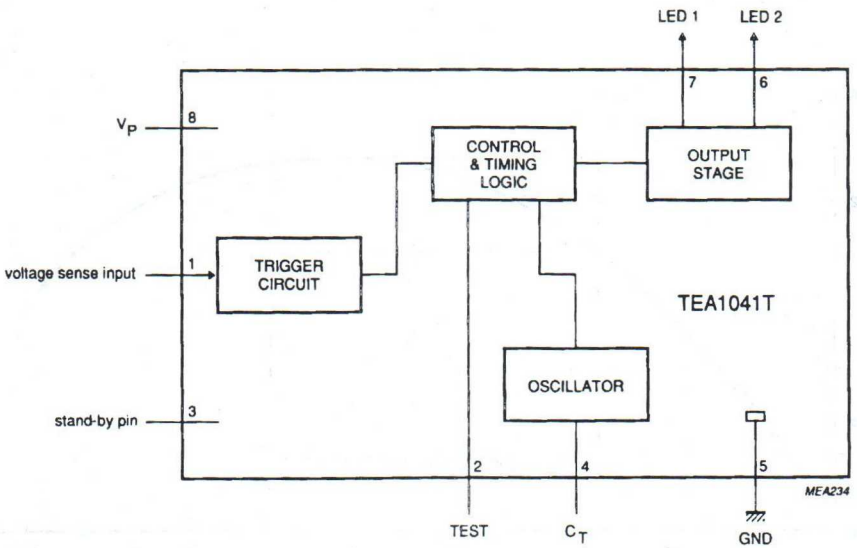


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_I	1	voltage sense input
TEST	2	test pin
V_{sw}	3	stand-by
C_T	4	oscillator capacitor
GND	5	ground
L2	6	LED 2
L1	7	LED 1
V_p	8	supply voltage

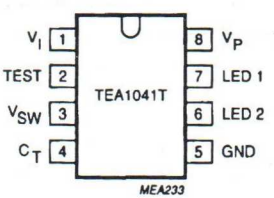


Fig.2 Pin configuration.

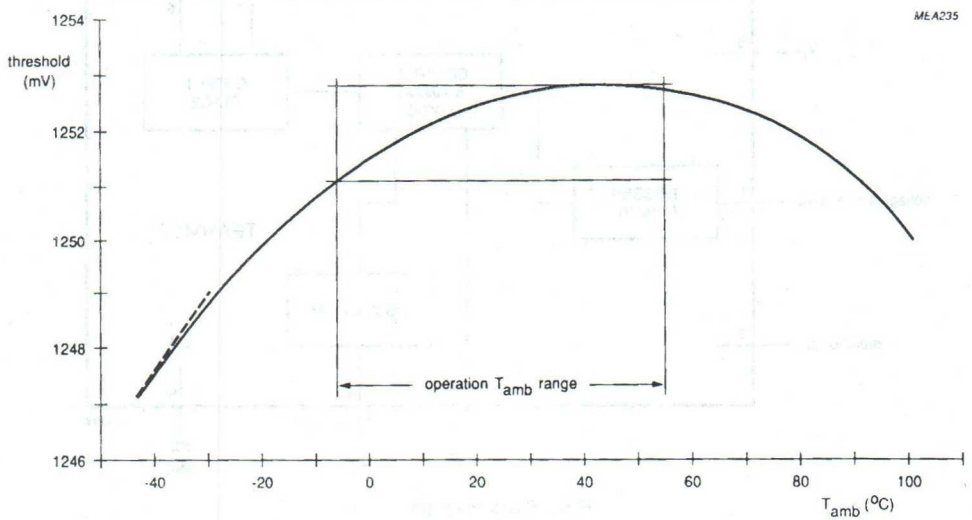


Fig.3 Thermal drift of the input threshold.

LIMITING VALUES

In accordance with the absolute maximum system (IEX 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_j	junction temperature	−25	+125	°C
T_{stg}	storage temperature range	−25	+125	°C
V_{max}	maximum voltage (pins 1, 3 and 8)	−0.5	4	V
V_{max}	maximum voltage (pins 6 and 7)	−0.5	5.5	V
I_4	maximum current into pin 4	-	5	mA
	during 1 µs into V_p	-	90	mA
I_{max}	maximum current into test pin	-	0.5	mA
P_{tot}	total power dissipation	-	150	mW
T_{amb}	operating ambient temperature range	−5	+55	°C

Note

Voltages with respect to 0 V unless otherwise specified

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT.
R_{th}	thermal resistance	mounted on PC board	-	240	-	K/W
R_{th}		mounted on ceramic	-	170	-	K/W
R_{th}		mounted with heatsink on ceramic	-	120	-	K/W

CHARACTERISTICS

Voltages with respect to 0 V; $Tamb_{min} < Tamb < Tamb_{max}$; V_{SW} = 0 V, V_p = 1.8 to 4.0 V; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_p	supply voltage range		1.8	-	4	V
V_{cl}	clamp voltage V_p; V_{SW}; V_I	I = 10 mA	-	7.5	8.5	V
I_{SW}	supply current	V_p = 1.8 - 4 V	0.65	-	2.2	mA
I_p		V_p = 1.8 V; FF is not triggered	2.2	-	4.4	mA
I_p		V_p = 4 V; FF is triggered	4	-	8	mA
I_{sb}	stand-by current	measured 1 s after S1 is opened; V_p = 4 V	-	-	10	µA
Trigger amplifier T						
V_I	threshold	T_j = 25 °C	1.17	1.25	1.33	V
	temperature coefficient		−250	-	+250	10^{-6}/°C
ΔV_I	lifetime drift threshold level		-	1	-	mV/1000h
	hysteresis at input V_I due to Schmitt trigger		3	5	7	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing circuitry						
t_{PLH}	propagation delay during adjustment	from passing threshold at input to 50% of output switching edge at I_O = 1 mA	-	1	10	µs
t_s	settling time of IC during adjustment		-	-	1	ms
f_{osc}	oscillator frequency	C = 10 nF; V_p = 2 to 2.8 V	5.7	8.2	10.7	kHz
I_c	required current I_c to switch adjusting circuitry		2.2	-	2.8	mA
Output circuit						
I_{L1}	output current	$V_{L1} = V_{LB2}$ = 0.5 V; V_p = 1.8 V	14	20	39	mA
I_{L2}		$V_{L1} = C_{L2}$ = 2.5 V V_p = 4 V	-	-	59	mA
ΔI_L	output current difference 100 $(I_{L1} - I_{L2} / (I_{L1} + I_{L2}) / 2)$		−15	-	+15	%
V_{sat}	output saturation voltage	I_{L1}; I_{L2} = 10 mA	-	-	200	mV
	output leakage current	$T_j \leq$ 55°C; V_p = 4 V	-	-	10	µA
Test pin TP						
V_2	high voltage level	used as output	450	-	-	mV
V_2	low voltage level	used as output	-	-	150	mV
$+I_{TP}$	required input current high	used as input	300	-	-	µA
$-I_{TP}$	input current low	used as input	-	-	40	µA
f_{test}	maximum input frequency		10	-	-	kHz

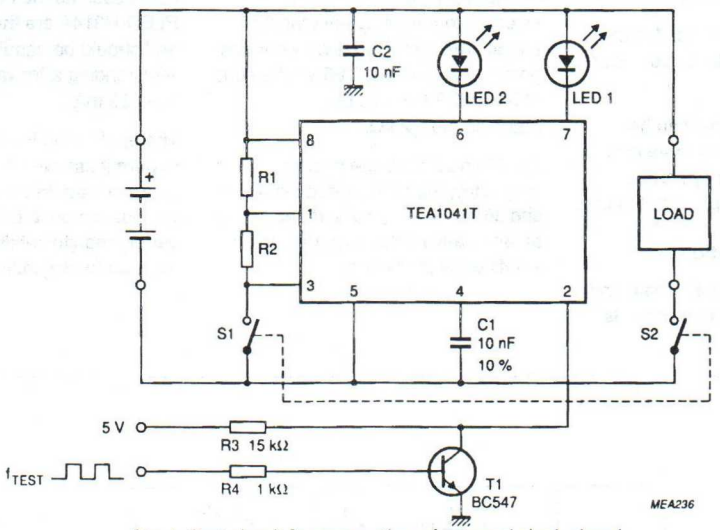


Fig.4 Test circuit for connection of external clock signal.

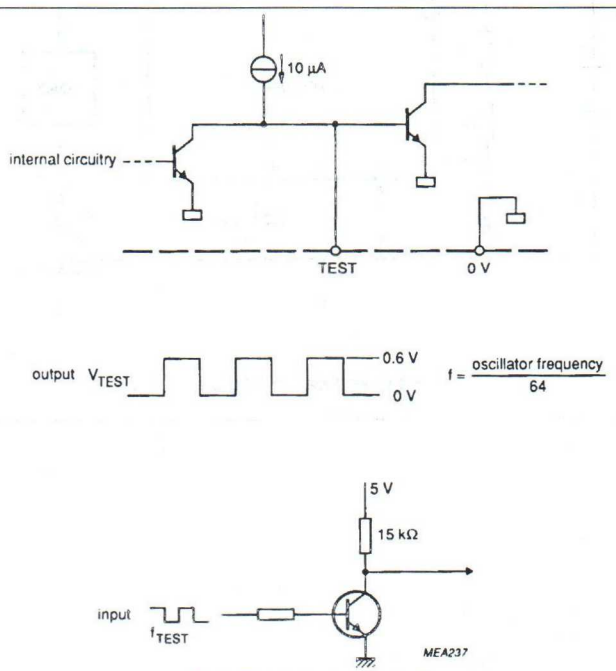


Fig.5 Test information pin 2.

Test information

The circuit depicted in Fig. 4 is that realized on the standard application PCB.

An external clock signal can be connected to pin 2 via a transistor. The oscillator frequency can be monitored when this pin is not in use.

Application information

The application circuit is simple and requires few external components.

A potential divider R1 - R2 is selected to permit achievement of the desired threshold level when the potential on pin 1 is 1.25 V. The sum of R1 and R2 should be approximately 2 kΩ.

To obtain an accurate oscillator frequency, the capacitor at pin 4 should be 10 nF ± 10%. If necessary an alternative value may be chosen to influence the timing.

LEDs such as the Philips PLED-H314A are the most suitable and should be capable of withstanding a forward current of at least 59 mA.

The application PCB was designed to permit use with or without an external load. In the latter instance S1 must be used to activate the battery monitor whilst S2 connects the load to its supply.

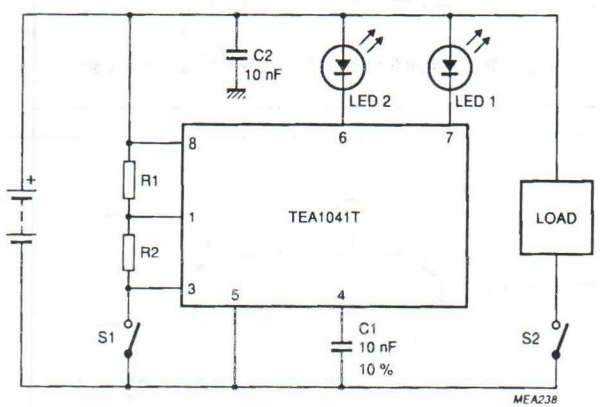
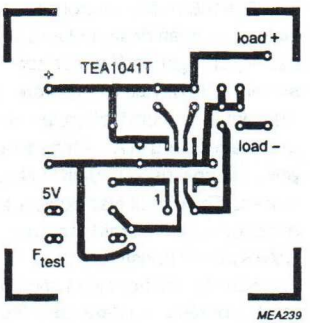


Fig.6 Application diagram.



Printed circuit board copper side, scale 2:1

Fig.7 Application PCB details.

APPLICATION CIRCUIT COMPONENT DETAILS

REFERENCE	TYPE	VALUE	UNIT
R1 + R2	-	±2	kΩ
R3	-	15	kΩ
R4	-	1	kΩ
C1	-	10 ±10%	nF
C2	-	10	nF
LED1, LED2	PLED-H314A	-	-
T1	BC547	-	-

Note

The TEA1041 must be soldered to the copper side of the printed-circuit board.

Switched-mode power supply battery charger control circuit

TEA1088T

FEATURES

- SMPS control circuit
  fixed frequency/duty factor regulation
  emitter drive for power switch
  current mode control
  dynamic primary current limiting
- Charge control circuit
  accurate output current setting
  fast, two stages, charge mode
  two hours fast charge protection limit
  trickle charge mode for full batteries
- Voltage control circuit
  voltage regulation for connected mains and load
- Battery monitor circuit
  accurate fully charged detection (– dV phenomenon)
  LOW-level detection and indication
  protection against faulty batteries, short or open-circuit
  data output for condition of charge processing
  very LOW stand-by current, < 10 μA

GENERAL DESCRIPTION

The TEA1088T is a control circuit which has been designed for use in a battery charger and/or monitor system. The device incorporates all the control and protection functions that are required in a switched-mode power supply used to deliver charge current. The circuit also achieves direct drive to the emitter of the SMPS power transistor.

The battery monitor circuit includes a reliable battery-full detector which controls the switch-over from fast charge to trickle charge mode and, in the discharge mode, a battery-LOW detector with two outputs for an LED or buzzer warning indicator.

Protections are provided against open-circuit, short-circuit or faulty batteries.

The device is primarily designed to control two batteries in series. The number of cells can be extended by using a tap.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1088T	16	SO16	plastic	SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_6	supply voltage	charge	5.5	-	31.0	V
I_6	supply current	charge	-	-	19	mA
I_{10}	supply current	discharge	-	-	12	mA
i_{10}	stand by current		-	-	10	µA
I_1	SMPS transistor bias current		-	–2	-	mA
V_2-V_3	saturation voltage emitter switch	I_2 = 350 mA	0.9	-	1.4	V
V_{10}	battery voltage range	2 cells	1.8	-	4.0	V
V_{11}	threshold battery LOW indication		1.17	-	1.33	V
$I_{13,14}$	LED output currents	$V_{13,14}$ = 0.5 V	21	30	39	mA
V_{10}	voltage range of battery full detection		2.3	-	4.3	V
V_{10}	threshold for full indication		-	–22	-	mV

Switched-mode power supply battery charger control circuit

TEA1088T

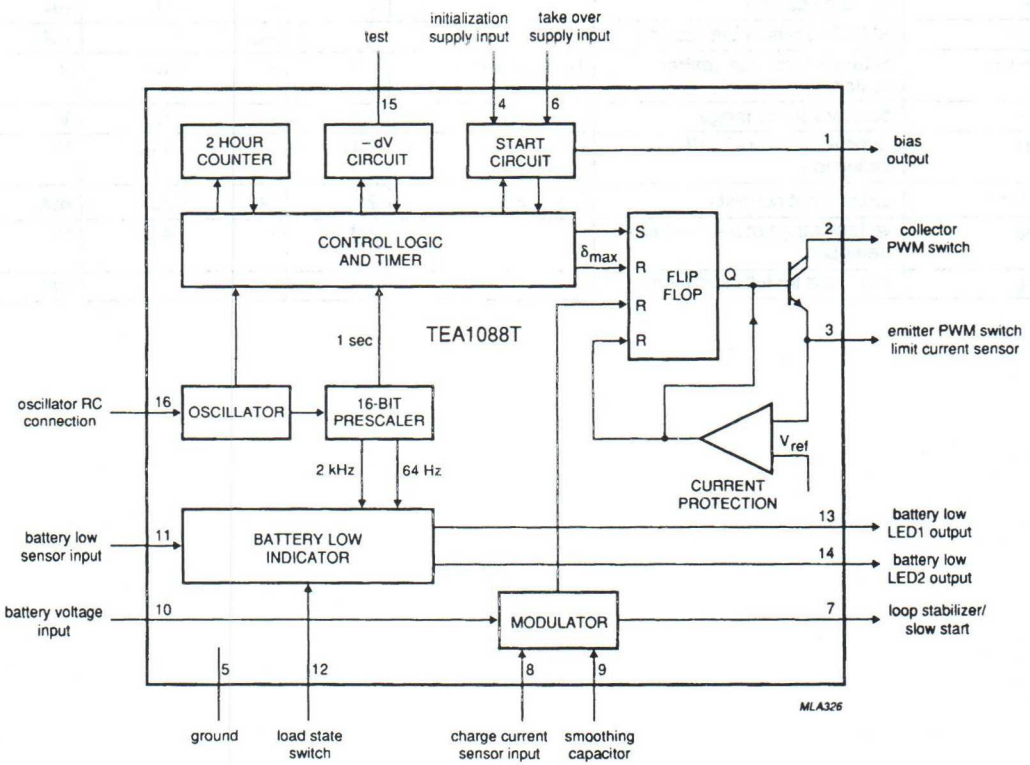


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
O2	1	bias output
O1	2	collector PWM switch
IT	3	emitter PWM switch/limit current sensor
V_{IC}	4	initialization supply input
GND	5	ground
V_{AT}	6	take over supply input
MI	7	loop stabilizer/slow start
I_{IN}	8	charge current sense input
V_{IN}	9	"V_{AC}" smoothing capacitor
V_{AC}	10	battery voltage input
BLI	11	battery LOW sense input
LS	12	load state switch
L1	13	battery LOW LED1 output
L2	14	battery LOW LED2 output
TEST	15	test pin
OSC	16	oscillator RC connection

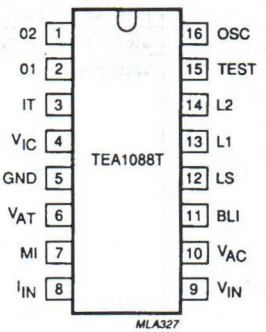


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The pin description of the device refers to external components as illustrated in the test circuit diagram (Fig.9). In this circuit the TEA1088T directly drives the emitter of the SMPS Darlington power transistor to provide fast switching and a wide reverse bias SOAR.
The supply output characteristics are shown in Fig.4 and the operational cycles of the charger system are shown in Fig.5.

The battery monitor circuit includes a reliable battery-full detector which controls switch-over from the fast charge to the trickle charge mode. The battery-full detector employs the phenomenon of an increase in battery voltage during charge due to the conversion of charge current into stored energy and, when the battery is full, a slight decrease in voltage due to a negative temperature coefficient when the charge current is only dissipative.
During charging the battery voltage is carefully sampled every second, the SMPS is then stopped to prevent interference. When a reducing voltage, –dV, is measured in succession the detector circuit sets the trickle charge mode.

In the discharge mode the battery LOW detector monitors the battery voltage and an output is given when the voltage drops below a set value. The output signals on the L1 and L2 pins are given in Figure 6. The device can also be employed purely as a monitor, this is because the monitor circuit is separate from the charge circuit. Figure 8 gives an application example.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134); voltage with respect to O V.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_j	junction temperature		–25	+125	°C
T_{stg}	storage temperature range		–25	+125	°C
V_6	voltages	continuous	–2.0	31	V
		peak during 100 ms; non-repetition	-	45	V
V_{10}		continuous	-	4.0	V
		peak during 2 µs; 50 ms repetition	-	12	V
V_1			–5.0	15	V
V_2		I_2 = 0 mA	–0.5	30	V
V_{11}, V_{12}			–0.5	4.0	V
		V_{10} < 4 V	–0.5	V_{10} +0.3	V
V_8			–0.5	0.5	V
V_{13}, V_{14}			–0.5	10	V
I_2, I_3	currents	continuous	0	350	mA
		peak 1 µs	0	1.0	A
I_8, I_9, I_{11}			-	2.0	mA
I_{13}			-	10	mA
I_{14}	battery LOW LED1 output		-	50	mA
P_{tot}	total power dissipation	Fig.3	-	500	mW

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	90	K/W

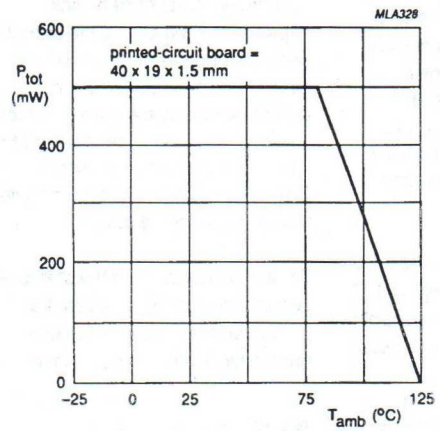


Fig.3 Power derating curve.

Supply (pins 4 and 6)

Pin 6 is the main supply input for the device if it is employed as a battery charger. It can be fed from a DC or AC voltage source; the latter can be provided by a SMPS transformer winding. The positive value of an AC voltage has to be between 7 and 31 V (45 V peak) while the negative value is restricted to −2 V.

Internally, the main supply voltage is series regulated to approximately 6 V which is available at pin 4 for connection of a smoothing capacitor. Initialization is also accomplished via pin 4 by pre-charging the capacitor up to 7.5 V via a resistor from the system power source. At the start of system operation the supply on pin 6 must take over.

When the voltage at pin 4 drops below 3.9 V the circuit switches off and restart occurs via initialization.

Output stage (pins 1, 2 and 3)

The PWM output stage consists of a Darlington power transistor with the collector and emmitter connected to pins 2 and pin 3 respectively. The current capability is 500 mA peak. This transistor drives a Darlington high voltage transistor switch directly at its emitter to ensure a large reverse bias SOAR and fast switching. The base of the Darlington high voltage transistor is biased by a current source (>1 mA) from pin 1 in combination with an external Zener diode and capacitor (pre-charged at initialization) in order to provide a low impedance base path during switching.

Dynamic primary current limit (cycle-by-cycle) (pin 3)

The primary switching current is sensed across an external resistor connected to the emitter of the PWM output switch at pin 3. Internally, the voltage on pin 3 is compared to a reference voltage which in turn is inversely proportional to the voltage difference between V_{AT} (pin 6) and V_{AC} (pin 10). This voltage difference reflects the input voltage of the system. This method compensates for primary current overshoot variations with input voltage which are caused by internal delay in the IC and storage time in the power transistor. The voltage reference level is defined by:

$V_{ref} = 0.44 - 5 \times 10^{-3} \times V_{IN}/N$ [V]

where (N = transformer winding ratio

If the sense voltage rises above V_{ref} then the output is terminated every cycle.

Modulator (pins 7 to 10)

The PWM is connected with two error amplifiers for regulation of the SMPS output current and voltage. Voltage regulation is enabled only when the SMPS is operative and while the batteries are loaded (pin 12 connected to ground). The current feedback input, pin 8, receives the current information from a resistor R_s in the output current loop. The voltage waveform across this resistor is negative-going but is shifted to a positive value by addition of a voltage $I_8 \times R8$ and integration with C8. (I_8 is a reference current from pin 8). This feedback voltage is compared and regulated to the common potential, the output current is defined by:
$I_O = R9/R_s$.
The value of the reference current I_8 depends on the operational state set by the control block which distinguishes:

- First 17 minutes of charge I_8(typ.) = 40 µA (2C)
- Proceeding charge = 20 µA (1C)
- Trickle charge (on/off = 1/9) = 20 µA (0.1C)
- Current limit at voltage regulation = 46 µA

In the voltage regulation mode the battery output voltage is sensed at pin 10. Internally, this voltage is divided by two and made available at pin 9, for smoothing purpose only, and compared with a 1.25 V reference voltage.

Pin 7 is connected directly to the summing point of the PWM input and the output from both error amplifiers. By connecting a capacitor between pin 7 and pin 3, the primary current sense voltage is added to the error signal which results in a current mode control that enhances load response and control loop stability. This capacitor also provides slow start at a start cycle.

When the device is supplied via pin 6 the minimum duty factor is restricted to 3% to ensure a continuous supply from the SMPS. The maximum duty factor is limited to 60%.
Open or short-circuit battery output is detected via pin 10. If the voltage at pin 10 rises above 5 V or, in the charging mode, remains below 2 V during the first 4 charge minutes, the circuit will switch off and the start-up procedure will be resumed.

Load identification (pin 12)

The switch input recognizes a load connected to the output by the state of switch S1. The difference between a closed switch or an open switch with short-circuit or flat batteries is identified if the external resistance value of R11 + R12 is greater than 4.2 kΩ.

Battery LOW sense (pin 11)

In the battery discharge mode the battery voltage is protected at pin 11 via a resistor divider. The input is immune to any spurious interference from the load. When the voltage level drops below 1.25 V the indicator output at pin 13 is set. At load switch OFF (S1 open) the indicator outputs (pin 13 and pin 14) will give alternating bursts for 4 seconds.

Indicator outputs (pins 13 and 14)

The indicator outputs have an open collector with set current sink capability. When active, the output generates pulses at 2 kHz. When pins 13 and 14 are alternating, the output generates two bursts of these pulses at 4 Hz per cycle. More detailed information is given in Figure 6. These signals are suitable for driving LED and buzzer indicators.

Serial data concerning the status of circuit operation from which the battery state-of-charge can be processed is also output from pin 13.

Test pin (pin 15)

This pin must not be connected.

Oscillator (pin 16)

An R-C network sets the frequency of the oscillator. The switching frequency of the SMPS and all the internal timing is derived from this oscillator which should be nominally 33 kHz. The capacitor is charged via pin 16 (flyback) and discharged by the parallel resistor. The required frequency is set with R = 36 kΩ and C = 560 pF.

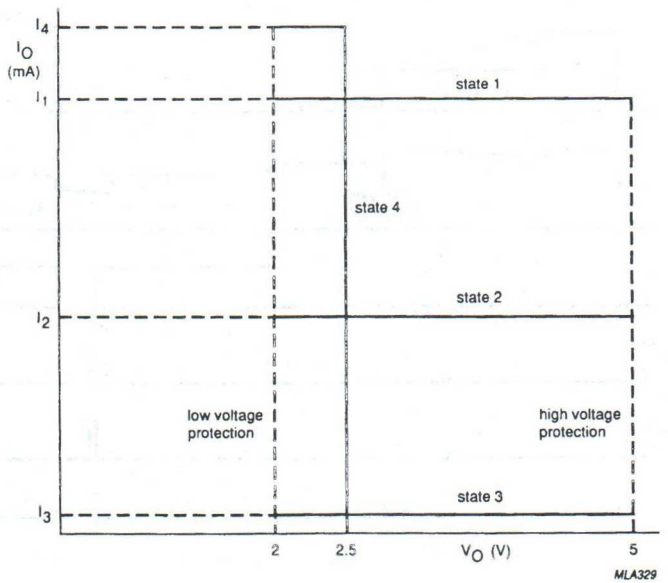
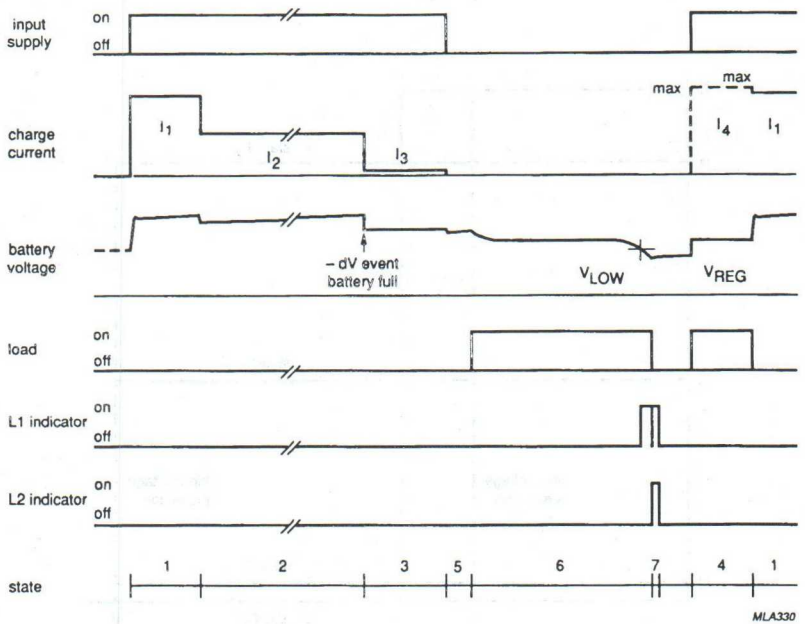


Fig.4 Supply output characteristics.



State 1; Boost charge. $I_1 = 2 \times I_2$
State 2; Fast charge.
$I_2 = (20 \times 10^{-6}) \times R8/R_s$.
State 3; Trickle charge. $I_3 = 0.1 \times I_2$
(i.e. I_2 pulsed with 10% duty factor at 1 Hz rate.
State 4; Voltage regulation.
$V_O = 2.5$ V; $I_{O(max)} = 2.3 \times I_2$.

Fig.5 Operational cycles of the SMPS charger system.

State 1; Boost charge current during 17 minutes after supply turn on. The current I_1 is twice the fast charge current I_2. This state helps completely empty batteries, possibly reversed in polarity, to quickly regain their charge store potential. Within the first 4 charge minutes the battery voltage should rise above 2 V otherwise protection occurs by stop and initialization in repeating succession.

State 2; Fast charge current that proceeds until either battery full is detected (–dV) or a maximum charge time of 2 hrs is reached.

State 3; Trickle charge which keeps the batteries fully charged. This current is sufficiently low not to harm the batteries when maintained for a long period.

State 4; Output voltage regulation when both the charger is on and a load is applied to the batteries. This provides direct output power to the load even when the batteries are empty.

State 5; Stand-by at neither input nor output. Negligible IC current (to keep the internal memories active) is drawn from the batteries.

State 6; Discharge of the batteries. The monitor circuit is activated and senses the battery voltage. Signal output (L1) is given when the sense voltage drops below a set value (V_{LOW}).

State 7; By removing the load after state 6, both indicator outputs give signals in an alternating mode for 4 seconds (see also Fig.6).

CHARACTERISTICS

V_6 = 10 V; V_{10} = 2.5 V; R16 = 36 kΩ; C16 = 560 pF; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_6	take over supply		5.5	-	31.0	V
I_6	supply current		10	15	19	mA
V_4	initialization level		6.5	7.0	7.5	V
V_4	internal supply voltage output		5.4	6.5	6.9	V
I_4	supply current	V_6 = 0 V	6.5	9.5	12.5	mA
I_{10}	input current	stand-by	-	5.0	10.0	µA
		battery discharge	6.0	9.0	12.0	mA
		BLI blinking	7.0	10.5	14	mA
		count 2 hr timer	4.9	7.8	10.8	mA
		charging	0.3	0.5	0.7	mA
Protection circuits						
V_4	LOW supply protection		3.0	3.5	3.9	V
V_{10}	minimum input voltage	charge period > 4 min.	1.8	2.0	2.2	V
V_{10}	maximum input voltage		4.5	5.0	5.5	V
Oscillator (supplied via V_4 or V_{10} = V_P)						
V_{16}	voltage level HIGH		-	4/5 V_P	-	V
V_{16}	voltage level LOW		-	1/5 V_P	-	V
	initial accuracy excluding external components	V_4 = 5.7 V	−10.0	-	+10.0	%
Δf	frequency deviation	V_4 to V_{10} supply	-	1.5	3.0	%
f	frequency	R = 36 kΩ; C = 560 pF	-	33.0	-	kHz
TC_f	temperature coefficient of frequency		-	−150	-	10^{-6}/°C
BLI function						
V_{10}	input voltage range		1.8	-	4.0	V
V_{11}	BLI reference voltage		1.17	-	1.33	V
TC_{ref}	temperature coefficient reference		−250	-	+250	10^{-6}/°C
ϕ	hysteresis reference voltage output		2.0	3.5	6.0	mV
$I_{13,14}$	BLI output current	V_O = 0.5 V	21	30	39	mA
I_{13}/I_{14}	output currents match		0.9	1.0	1.1	mA
$V_{13,14}$	saturation voltage	I_O = 10 mA	-	-	200	mV
$I_{13,14}$	leakage current	V_O = 4 V	-	-	10	µA
V_{13}	breakdown voltage	I_O = 10 mA	15.0	17.0	18.5	V
V_{14}	breakdown voltage	I_O = 50 mA during burst	15.0	17.0	18.5	V
$f_{13,14}$	frequency output signal		-	2	-	kHz
$f_{13,14}$	burst frequency	load switch off	-	1	-	Hz
$f_{13,14}$	alternating frequency	load switch off	-	4	-	Hz
−dV detector						
V_{10}	minimum input level		-	2.3	2.5	V
V_{10}	maximum input level		4.0	4.3	-	V
$-dV_{10}$	detector threshold		15	22	30	mV
t_m	sampling time		-	1	-	ms
t_{rep}	sampling repetition		-	1	-	s

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SMPS outputs						
I_1	bias output		1.0	2.0	4.0	mA
V_2-V_3	saturation voltage	I_2 = 350 mA	0.9	-	1.4	V
V_3	current protection threshold voltage	V_6-V_{10} = 3 V	340	425	510	mV
		V_6-V_{10} = 22 V	262	328	394	mV
t_p(V2)	minimum output pulse	V_6-V_{10} > 25 V	0.3	0.6	1.6	µs
t_d	current trip delay to output	V_3 = 1.2 x $V_{threshold}$	-	0.6	-	µs
Modulator						
V_{10}	reference level	voltage regulation	2.4	2.55	2.7	V
TC	temperature coefficient $V_{reference}$		-	+25	-	10^{-6}/°C
I_8	reference input current	fast charge	−10	−20	−30	µA
		boost charge	−20	−40	−60	µA
		voltage regulation	−26	−46	−69	µA
	ratio reference current	boost/fast charge	1.9	2.0	2.1	
		voltage regulator/ boost charge	1.09	1.15	1.21	
V_8	reference level	current regulation	−10	-	+10	mV
I_7	PWM input source current	voltage level HIGH	−6.5	−10.0	−13.5	µA
	PWM input sink current	voltage level LOW	6.5	10.0	13.5	µA
V_7	maximum PWM input voltage	slow start	-	0.8 x V_4	-	V
d	maximum duty factor		55	60	65	%
Periods						
t_{inh}	inhibit time of −dV circuit	start boost charge	-	4.3	-	min
		start fast charge	-	4.3	-	min
t_{bc}	boost charge duration		-	17	-	min
t_{fc}	maximum fast charge time		-	2.1	-	hr
Computer control interface						
I_{13}	status indication current source at L1		−490	−820	−1150	µA

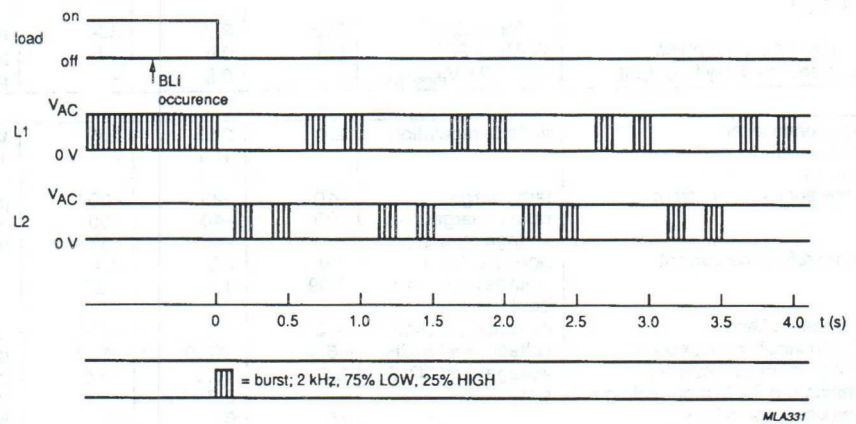


Fig.6 BLI signalling scheme.

Battery monitor for NiCd and NiMH chargers

TEA1100; TEA1100T

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

FEATURES

- Accurate regulation of charge current settings in co-operation with a switched mode power supply
- Accurate detection of fully charged batteries by currentless battery voltage sensing
- Switch over from fast to normal charging when batteries are fully charged
- Adjustable fast charging level (1 C to 5 C)
- Adjustable normal charging level (0.05 C to 0.25 C)
- Temperature guarding by means of an NTC resistor
- Tracking of maximum fast charging time with fast charging current level
- Protections against short-circuited and open batteries
- Large battery voltage range
- Both DC and PWM outputs with polarity switch

APPLICATIONS

- Charge systems for NiCd and NiMH batteries

GENERAL DESCRIPTION

The TEA1100 is manufactured in a BICMOS process intended to be used as a battery monitor circuit in charge systems for NiCd and NiMH batteries.

The circuit has to be situated on the secondary side in mains-isolated systems where it monitors the battery voltage and the charge current. The circuit drives, by means of an opto-coupler or a pulse transformer interface, an SMPS circuit, situated on the primary side of the system, thus controlling the charge current of the batteries. The circuit can drive the external power transistor in switched mode systems, which have a DC power source, via a driver stage.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1100	16	DIL	plastic	SOT38G
TEA1100T	16	SO16L	plastic	SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		5.65	–	11.5	V
I_P	supply current	outputs off	–	–	4.1	mA
V_{VAC}	voltage range of battery-full detection		0.385	–	3.85	V
dV_{VAC}/V_{VAC}	–dV detection level w.r.t. top value	note 1	–	1	–	%
I_{VAC}	input current battery monitor		–	–	1	nA
V_{VAC}	voltage protection battery low battery high		 – –	 0.3 4.25	 – –	 V V
	charging level	$I_{charge} = R1/R_s \times I$; see Fig. 3				
I_{ref}	fast	$I = I_{ref}$	20	–	100	µA
I_n	normal	$I = 1/p \times 0.1 \times I_n$ (p = prescale factor)	10	–	50	µA
f_{osc}	oscillator frequency		10	–	100	kHz

Note to the quick reference data

1. The –dV detection level can be adjusted by use of an external voltage regulator diode to increase the sensitivity.

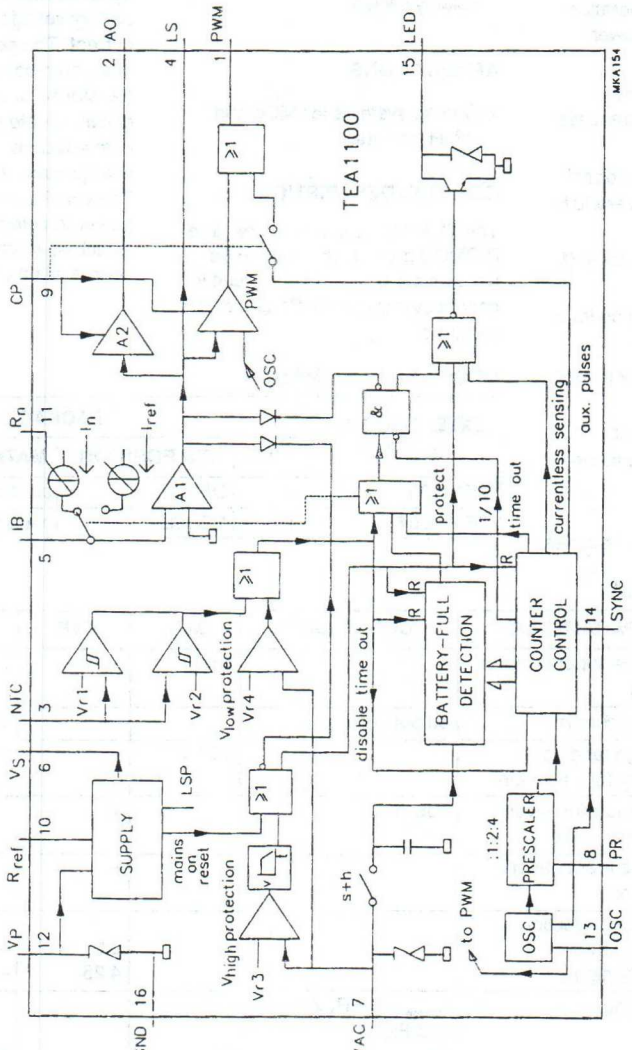


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
PWM	1	pulse width modulator
AO	2	analog output
NTC	3	temperature sensor input
LS	4	loop stability
IB	5	charge current
V_S	6	stabilized supply voltage
VAC	7	battery voltage
PR	8	prescaler
CP	9	change polarity
R_{ref}	10	reference resistor
R_n	11	normal charge reference resistor
V_P	12	positive supply voltage
OSC	13	oscillator input
SYNC	14	synchronization input
LED	15	LED output
GND	16	ground

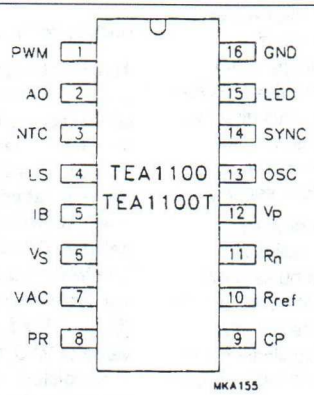


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The operation of the circuit will be explained with the aid of Fig.1 (block diagram) and Fig.3 (application diagram). The circuit is divided into several blocks which are described separately.

Supply block

The circuit needs a supply voltage on pin V_P with a value between 5.65 and 11.5 V. Above 6.4 V typ., the circuit starts up assuming that mains is connected to the system and the charge session begins. This supply can be generated by a separate winding on the transformer, as shown in Fig.3 (application diagram), in either the flyback or the forward stroke. Another possibility is rectification from the mains secondary winding (at the connection D1 and L2). Considerations for choosing the way of supplying the IC are:

- supply voltage range of 5.65 to 11.5 V under all circumstances (also during the 90% pause at normal charging, the standby current then is 1 mA typ.)
- maximum battery voltage (flyback stroke)
- minimum power delivered by the primary SMPS (normal charging)

The supply block delivers the following outputs:

- By using an external resistor R_{ref} at pin 10 (R_{ref}) a reference current is obtained which defines all external related currents (charge reference currents, oscillator).
- Externally available 4.25 V stabilized voltage source (V_S). This source is used internally for a large part of the circuit and can be used to set the NTC biasing and to supply other external circuitry. V_S is cut off in the 90% pause during normal charging.
- Low Supply voltage Protection signal (LSP). When the supply voltage is lower than 5.25 V typ., there is supply voltage enough left to switch off the power regulation and hereafter the IC current is limited to the start level of 35 µA typ.
- Mains on reset pulse resets all digital circuitry after a start or restart due to an interrupted supply (V_P).

Charge current regulation

The charge current has to be sensed by means of a low-ohmic resistor in series with diode D1. The waveform on resistor R_s (see Fig.4 for a flyback converter) has the form of a negative-going ramp and after filtering a negative DC voltage is obtained. Across resistor R1 a positive voltage is created by means of the current sources set by the pins R_{ref} and R_n. The error amplifier A1 references the result to ground and via the regulation loop of the SMPS, the secondary current will be regulated to a value which is defined by:

$I_{ch} \times R_s = R1 \times I_{ref}$ (fast charge) or,
$I_{ch} \times R_s = R1 \times I_n$ (normal charge)

The I_{ref} current is the fast charging reference current, the I_n current is used for regulation after a full battery is detected. The I_{ref} current is the reference current set by R_{ref} while I_n is dependent on the resistor at pin R_n. With no resistor on pin R_n, the I_n current has a default value which is half the I_{ref} current.
By choosing the correct resistor values R_s, R1, R_{ref} and R_n, a wide range of charge currents can be set as well as a wide range of the ratio fast charge current as a function of normal charge current. For determination of the normal charge current the 1:10 duty cycle and the programmable prescale factor (p) should be taken into account (see Logic block); $I_n = 1/p \times 0.1 \times I_n$. The output of amplifier A1 is available at the loop stability pin (LS), so the time constant of the SMPS loop can be set at the secondary side of the system.

NTC block

The voltage at the NTC pin is compared with two reference voltages. When the NTC voltage is between V_{r1} and V_{r2}, the charge current regulation is unaffected. When the NTC voltage is outside this window, the power of the SMPS is reduced to the normal charge level.
The NTC input can be used for temperature protection as shown in Fig.3 (application diagram) by using a suitable NTC resistor. To avoid switching on and off with temperature, a hysteresis is built in for both levels.

Output drivers

The SMPS regulation signal is available at different pins:

- Analog voltage output (push or pull) at AO (pin 2) to drive an opto-coupler in mains separated applications when an external resistor is connected between AO and the opto-coupler. The maximum current through the opto-coupler diode is 2 mA. The voltage gain of amplifier A2 is: $A = (V_{LS} - 1.4) \times 4$ and is typ. 12 dB. The voltage at AO can also be used to drive a PWM input of an SMPS circuit directly. During 'inhibit SMPS' the AO output is fixed to zero charge current for currentless sensing.
- The LS voltage is compared internally with the oscillator voltage to deliver a pulse width modulated output at PWM (pin 1) to drive an output device in a DC/DC converter application via a driver stage. The PWM output is latched to prevent multi-pulsing. Moreover with the latch a kind of current mode control is possible. The maximum duty cycle is internally fixed to 78% (typ.). The 'PWM' output can be used for synchronization and duty cycle control of a primary SMPS via a pulse transformer (the SMPS inhibit and auxiliary pulses are also available at pin PWM).
- The AO and PWM outputs can be changed in polarity by programming the change polarity pin CP. The PWM output in the on-state pushes current (CP = 0) or pulls current (CP = 1). The appearance of the auxiliary pulses at pin PWM can also be programmed with CP.

The 'LED' output pin offers the following output signals:

- 10/90% signal for driving a LED when the duty cycle is too small during the 10% time. This occurs when there is a large difference between fast and normal charge currents. The LED frequency is $f_{LED} = 2^{-12} \times 1/p \times f_{osc}$
- An SMPS inhibit period (duration 10 OSC pulses) for currentless VAC sensing.
- VAC high voltage protection signals.

Battery monitor

At higher battery voltages it is advised to divide the battery voltage with a factor 5 before offering this to pin VAC (Voltage ACcumulator). It is also possible to take a tap on the chain of batteries.
The VAC voltage range has to be between 0.385 V and 3.85 V.
The VAC voltage is sampled at a low cycle frequency ($f_{cycle} = 2^{-16} \times f_{osc}$) and the analog value of VAC is digitized and stored in a register. One cycle later, the digitized value is converted back to the analog value and compared with the actual value of VAC. If the actual value is higher, then the new VAC voltage is stored in the register, otherwise no conversion is done. So the VAC top value is stored and it is possible to detect an increasing VAC indicating 'not yet full batteries' or decreasing VAC indicating that the batteries are probably fully charged.

The circuit waits until the battery voltage has dropped 1% below the top value before indicating 'full batteries'. However, by applying a voltage regulator diode in the battery voltage sense-line (see Fig.7) an increased sensitivity of the –dV detection level can be obtained, e.g. 0.5% or even a lower value.
In Fig.5 the battery voltage as function of the charging time is shown. The negative slope depends on the charge current and is approximately 3 mV/cell/K.

The switching of the SMPS can cause interference on the battery voltage and therefore it has been necessary to stop the SMPS during the inhibit time (see Fig.8). This can be done automatically via the regulation pins AO and PWM or by using the SYNC output of the logic block. The SMPS is stopped for 10 periods at the end of which sampling is done. The VAC voltage will now be sensed currentless. To avoid false decisions concerning a falling VAC voltage, VAC is digitally filtered and analog stored in a sample-and-hold circuit. This approach ensures, even at very high –dV sensitivity (<1%) accurate detection of the battery full condition. Immediately hereafter decisions and VAC digitizing takes place. The benefit of a sample-and-hold circuit is that at high frequencies the noise on the VAC voltage is filtered and the VAC manipulations like decisions and digitizing are done on the same VAC voltage available in the sample-and-hold circuit.

When a –dV is detected, the reference current I_{ref} is switched off, the normal current I_n is switched on during 10% of regulation and the outputs are high-ohmic during 90%. This 1:10 ratio in active regulation, together with the ratio in reference currents (I_n as a function of I_{ref}), ensures that the resulting charge current is low enough to be allowed to flow through the batteries for a long time to overcome the self-discharge of the batteries without causing memory effects. In case the prescale factor p is programmed, the I_n current has to be lowered with the p factor, so $I_n = 1/p \times 0.1 \times I_n$.

Protections

- The circuit goes into standby (not active, low current consumption) when the supply voltage is less than 5.25 V (LSP).
- When the divided battery voltage exceeds the V_{r3} level (nominal 4.25 V) this is recognized as open or removed batteries and the output control signals terminate to stop the SMPS operation. This over-voltage sensing is digitally filtered. In above cases the 'battery full detector' and the 'counter/control' will be reset.
- When the divided battery voltage is less than V_{r4} (0.3 V), the circuit assumes short-circuited batteries, the charge current is reduced to the normal charge level. As soon as the voltage exceeds V_{r4}, the fast charging starts.
- The temperature protections are already mentioned in section NTC. In the case of short-circuited batteries or active temperature protections the 'battery full detector' is reset and the 'counter/control' is stopped.

Oscillator and control logic

The whole timing of the circuit is controlled by the oscillator.
The period time is defined by:
$T_{osc} = 0.93 \times R_{ref} \times C_{osc}$.

The counter block defines a maximum fast charge time called 'Time Out' (TO). As the charge current and the oscillator frequency (and so the TO) are both set by R_{ref}, changing one effects the other. Initially the oscillator capacitor can be chosen such that the fast charge time is half the TO time. This means that in case of a one hour (1C) charger, the TO signal occurs at 2 hours, in case of a quarter of an hour (4C) charger, the TO signal is active after half an hour. After that the circuit switches over to normal charging.

To adapt the SMPS switching frequency in the synchronized mode to the required oscillator frequency of the timing logic, the timer logic is preceded by a programmable divider. By means of the PR pin the divider ratio can be set to 1, 2 or 4 (p factor). Doing so the oscillator frequency can be increased with the factor p without changing TO.

Fast charging current:
$I_{ch} = R1/R_s \times V_{ref}/R_{ref}$
Time out:
$TO = 2^{26} \times 0.93 \times R_{ref} \times C_{osc} \times p$
Normal charging current:
$I_{ch} = R1/R_s \times 1/p \times 0.1 \times V_{ref}/R_n$

The control block determines the following timing sequences:

- VAC sampling; this takes 1 clock pulse every interval cycle.
  The power converter is switched off during VAC sampling. As there are several types of converters, there also are several control signals available at :
  - pin 'SYNC' for synchronization in analog voltage controlled primary SMPS circuits
  - pin 'PWM' for digital controlled primary SMPS and DC/DC converters
  - pin 'LED' in special applications

- Disabling –dV during 2^{-5} x TO (3% of TO) for proper start with flat or inverse polarized batteries. Disabling is active at each fast charge cycle.
- Maximum fast charging time (TO): the maximum timer is stopped during VAC low voltage protection and outside temperature range.
- The normal charge duty cycle is 1/p x 0.1
- Auxiliary pulses to support the supply voltage of the primary SMPS circuit via pin PWM: the pulses can be programmed on and off at an appearance rate of $f_{osc}/8$ with a duty cycle of 14%; programming is achieved by activating CP.

The timing logic and the –dV recognition circuitry are reset after each supply voltage failure and after a battery over-voltage recognition. The –dV circuit is also reset during normal charging.

The SYNC output delivers negative-going synchronization pulses which are suppressed during the sampling of the battery voltage. With these sync pulses the SMPS can be synchronized. The polarity of the sync pulses is chosen so that in case of an open SYNC pin in the synchronization mode, the power is regulated to a minimum. During the VAC sampling the absense of sync pulses causes the SMPS to stop thus minimizing interference (see Fig.8, synchronization waveforms).

During the 90% pause, only the oscillator and the control logic are operative to save current. In the pause V_P is never allowed to become less than V_{LSP}. This would cause a 'mains-on-reset' and so fast charging.

Programming

With pins 'CP' (change polarity) and 'PR' (prescaler) several functions can be programmed.

By defining the current (V_{ref}/R_{CP}) at pin CP, the following functions can be activated :

1	change polarity	CP = 0, normal polarity CP = 1, changed polarity
2	no auxilliary pulses at PWM	aux = 0
3	auxilliary pulses at f/8	aux = 8

CP PIN	FUNCTIONS	
	CP	aux
open pin	0	0
10 µA	0	8
22 µA	1	0
57 µA	1	8

By defining the voltage at pin PR, the following functions can be activated :

PR PIN	FUNCTIONS
V_S	prescaler divide by 1
open pin	prescaler divide by 2
ground	prescaler divide by 4

Formulas

DESCRIPTION	SYMBOL	FORMULA	FUNCTION
timing	T_{osc}	$0.93 \times R_{ref} \times C_{osc}$	repetition
	TO	$2^{-26} \times p \times T_{osc}$	duration
	$T_{disable}$	$2^{-5} \times TO$	duration
	$T_{LED} = T_{trickle}$	$2^{12} \times p \times T_{osc}$	repetition
	$T_{LED} = T_{trickel}$	$3/4 \times 2^9 \times T_{osc}$	duration
	$T_{inhibit}$	$2^{16} \times T_{osc}$	repetition
	$T_{inhibit}$	$10 \times T_{osc}$	duration
charge currents	I_{fast}	$R1/R_s \times V_{ref}/R_{ref}$	
	I_{normal}	$R1/R_s \times 1/p \times 0.1V_{ref}/R_n$	

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

All voltages with respect to ground; positive currents flow into the IC; all pins not mentioned in the voltage list are not allowed to be voltage driven. The voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the power rating is not violated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Voltages					
V_P	positive supply voltage (pin 12)		−0.5	13.2	V
V_{LED}	LED voltage (pin 15)		−0.5	13.2	V
$V_{1,8,4,3}$	voltage at PWM (pin 1), PR (pin 8), LS (pin 4), NTC (pin 3)		−0.5	V_P	V
V_{IB}	voltage at IB (pin 5)		−0.5	−1	V
Currents					
I_{VS}	current at V_S (pin 6)		−3	+0.01	mA
I_{LED}	current at LED (pin 15)		–	25	mA
I_{AO}	current at AO (pin 2)		−5	+5	mA
I_{PWM}	current at PWM (pin 1)		−15	+15	mA
I_{SYNC}	current at SYNC (pin 14)		−2	+2	mA
$I_{11,10,9}$	current at R_n (pin 11), R_{ref} (pin 10), CP (pin 9)		−1	+0.01	mA
$I_{4,5,7}$	current at LS (pin 4), IB (pin 5), VAC (pin 7)		−1	+1	mA
I_P	current at V_P (pin 6)		–	15	mA
Dissipation					
P_{tot}	total power dissipation	T_{amb} = 85 °C SOT38G SOT162A	 – –	 0.6 0.3	 W W
Temperatures					
T_{amb}	operating ambient temperature		−20	+85	°C
T_j	junction temperature		–	+150	°C
T_{stg}	storage temperature		−55	+150	°C

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 10 V; R_{ref} = 33 kΩ; R_n = 68 kΩ; C_{OSC} = 1 nF; CP is open; PR connected to V_S; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (V_P, V_S, R_{ref})						
V_P	supply voltage range		5.65	–	11.5	V
V_{PC}	clamp voltage	I_{PC} = 10 mA	11.5	–	12.8	V
V_{PS}	start voltage		6.1	6.4	6.7	V
V_{PLSP}	low supply protection level		4.85	5.25	5.65	V
V_{PLSPH}	hystereris of V_{PLSP}		0.3	0.95	–	V
I_P	supply current	outputs off	–	–	4.1	mA
I_{PP}	supply pause current	V_P = 6 V	–	–	1.71	mA
I_{PSB}	standby current	V_P = 4 V	–	35	45	µA
V_S	source voltage (stabilized)	I_S = 1 mA	4.03	4.25	4.46	V
V_{ref}	reference voltage	I_{ref} = 20 µA	1.18	1.25	1.31	V
TC_{Vref}	temperature coefficient of V_{ref}	T_{amb} = 0 to 45 °C	–	±100	±200	ppm/K
dV_{ref}/dV_P	power supply rejection ratio (PSRR) of V_{ref}	f = 100 Hz; dV_P = 2 V (peak-to-peak value); V_P = 8 V	−46	–	–	dB
ΔV_{ref}	voltage difference	dI_S = 1 mA	–	–	5	mV
I_{Rref}	current range of R_{ref}		10	–	100	µA
Charge current regulation (IB, R_n, R_{ref})						
V_n	voltage at pin R_n	I_n = 10 µA; I_{ref} = 20 µA	1.17	1.25	1.32	V
I_n	current range at R_n		5	–	50	µA
I_{IB}/I_{ref}	input current ratio normal charging fast charging	R_n not connected V_{IB} = 0 V_{IB} = 0	 0.475 0.95	 0.5 1	 0.525 1.05	
I_{IB}/I_n	input current ratio normal charging	R_n connected	0.90	0.97	1.04	
V_{thIB}	threshold voltage at IB	T_{amb} = 25 °C T_{amb} = 0 to 45 °C	−5 −7	– –	+5 +7	mV mV
NTC input						
V_{NTCSPH}	switching protection voltage on high temperatures		0.75	0.81	0.87	V
V_{NTCHH}	hysteresis of V_{NTCSPH}		60	90	120	mV
V_{NTCSPL}	switching protection voltage on low temperatures		2.78	3.00	3.20	V
V_{NTCHL}	hysteresis of V_{NTCSPL}		65	100	135	mV
I_{NTC}	input current	V_{NTC} = 2 V	−5	–	+5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output drivers (AO, LS, PWM, LED)						
$I_{AOsource}$	source current	V_{AO} = 3 V; CP = 0	–	–	–2	mA
I_{AOsink}	sink current	V_{AO} = 0.5 V; CP = 1	2	–	–	mA
g_m	transconductance A1	V_{IB} = 50 mV	–	300	–	µS
G_{v1}	voltage gain A1 x A2	V_{AO} = 2 V (peak-to-peak value)	–	72	–	dB
G_{v2}	voltage gain A2	V_{AO} = 2 V (peak-to-peak value)	–	12	–	dB
$I_{LSsource}$	maximum source current	V_{LS} = 2.25 V	–25	–21	–16	µA
I_{LSsink}	maximum sink current	V_{LS} = 2.25 V	16	21	25	µA
I_{PWMH}	HIGH level output current	V_{PWM} = 3 V	–18	–14	–10	mA
I_{PWML}	LOW level output current	V_{PWM} = 0.5 V	7	12	17	mA
$I_{PWMleak}$	leakage current	V_{PWM} = 4.25 V	–	0.2	10	µA
δ_{PWM}	maximum duty cycle		70	78	86	%
δ_{PWMaux}	auxiliary pulse duty cycle		12.6	14	15.4	%
V_{LEDsat}	saturation voltage	I_{LED} = 15 mA	–	–	600	mV
$I_{LEDleak}$	leakage current	V_{LED} = 10 V	–	–	5	µA
Battery monitor (VAC)						
I_{VAC}	input current	V_{VAC} = 4.25 V	–	1	–	nA
V_{VAC}	voltage range of –dV detection		0.385	–	3.85	V
dV_{VAC}/V_{VAC}	–dV detection level w.r.t. top level	V_{VAC} = 2 V	0.85	1	1.15	%
ΔV_{VAC}	resolution –dV		0.42	0.6	0.78	mV
T_{-dV}	temperature range of –dV detection		0	–	50	°C
Protections (VAC)						
V_{VACLBP}	low battery voltage protection		–	0.3	0.33	V
V_{VACHBP}	high battery voltage protection	with respect to V_P	–	0	150	mV
Oscillator, logic (OSC, SYNCH)						
V_{OSCH}	oscillator switching level HIGH		–	2.5	–	V
V_{OSCL}	oscillator switching level LOW		–	1.5	–	V
K	period time $T_{osc} = K \times R_{ref} \times C_{osc}$		0.84	0.93	1.02	
f_{OSC}	oscillator frequency range		10	–	100	kHz
V_{SYNCH}	SYNC output level HIGH	I_{SYNCH} = –0.4 mA	3.4	–	–	V
V_{SYNCL}	SYNC output level LOW	I_{SYNCL} = 0.4 mA	–	–	0.85	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Programming (CP)						
I_{CP}	programming currents					
	CP = 0; aux = 0	R_{CP} = 330 kΩ	–	–	4.2	µA
	CP = 0; aux = 8	R_{CP} = 120 kΩ	9.4	10.4	11.4	µA
	CP = 1; aux = 0	R_{CP} = 56 kΩ	20.0	22.3	24.5	µA
	CP = 1; aux = 8	R_{CP} = 22 kΩ	51.1	56.8	62.5	µA

QUALITY SPECIFICATION

General quality specification for integrated circuits: UZW-B0/FQ-0601.

Remark: for the synchronization pin (14), the ESD positive zap voltage is restricted to a maximum of 1000 V.

TEST AND APPLICATION INFORMATION

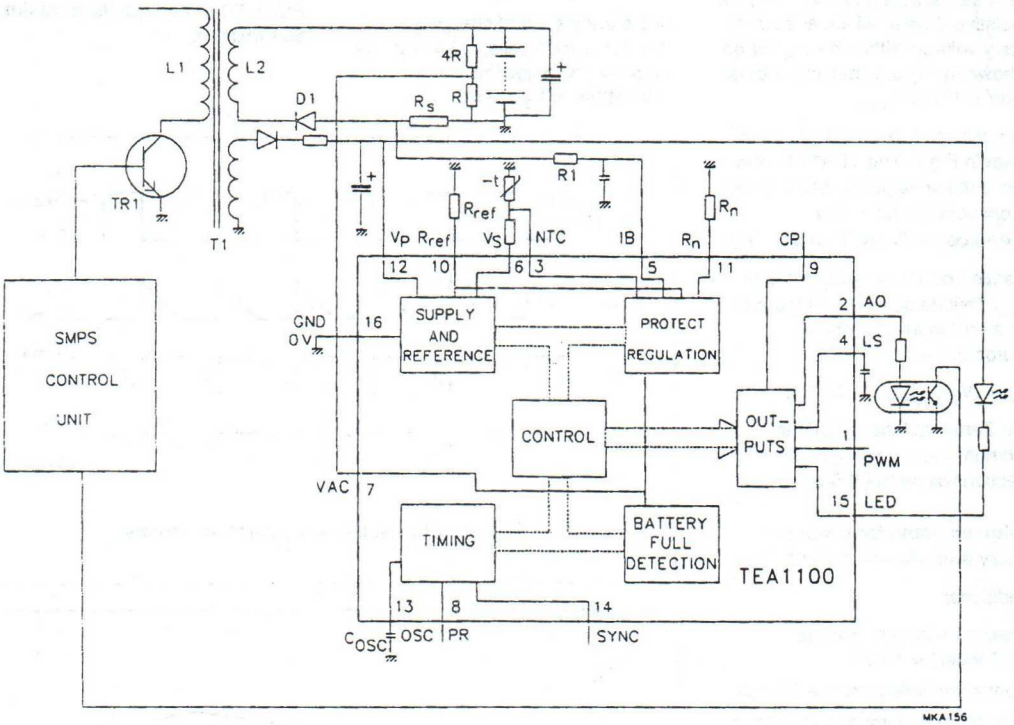


Fig.3 Application diagram.

Notes to Fig.3

1. Signaling the status of the charging session can be done by a LED-diode-resistor combination parallel to L2 (transformer T1). During the fast charging period the LED will burn continuously. During normal charging the LED will switch with the 10/90% rhythm. With mains-off the LED is off, thus not discharging the batteries. If at normal charging the duty cycle is too low during the 10% because of a very large difference between the fast charge and the normal charge levels, the LED can be driven by the LED pin.
2. With R_s = 50 mΩ and a required fast charging current level of 6 A (5C for 1.2 Ah batteries), the average current sense level is 300 mV. Power dissipation in R_s = 1.8 W.
   With a 3 kΩ resistor for R1, the required I_{ref} current is 300 mV/3 kΩ = 100 µA. For a normal charge level of 0.25C (300 mA) the voltage drop over R_s is 15 mV. Taken into account the duty cycle of 10%, the voltage drop over R1 = 150 mV. So the I_{Rn} current has to be: 150 mV/3 kΩ = 50 µA (p = 1).

Method to increase –dV sensitivity

The basic, direct battery sensing via a resistive divider, which adapts the battery voltage within the V_{AC} range, is shown in Fig.6. Detection occurs at –dV = 1% of $V_{B(max)}$.

The position of the Zener diode is shown in Fig.7. The TEA1100 now senses the voltage V_R, which is the battery voltage minus the Zener-diode voltage ($V_R = V_B - V_Z$).

Detection occurs at $-dV_R$ = 1% of V_{Rmax}. This detection corresponds with a –dV in the battery in accordance with:

$dV_{bat} = (V_Z/V_{B(max)}) - 1$ (in %).

If the Zener voltage is half the maximum battery voltage, the dV_B detection will be at –0.5%.

Design example for six-cells' battery and 5% –dV cut-off

Conditions:

- maximum battery voltage (1.7 V/cell) = 10.2 V
- sense network current ≈ 300 µA
- maximum monitor sense voltage V_{AC} = 3.6 V (<3.85 V)

For –dV ≈ 0.5%, a Zener voltage of about half the battery voltage is required; choose V_Z = 5 V. Now V_R at top level is ≈5.2 V and the required divider factor (V_{AC}/V_R) is 0.69. R1 and R2 become 5.6 kΩ and 12 kΩ respectively (see Figs 6 and 7).

During charge the battery voltage rises with a minimum rate of ≈8 mV per minute for 6 cells under 1 C charge. The temperature coefficient of the Zener diode and its ambient temperature change should not cause a premature full detection.

With the following equation the allowance of the Zener-diode temperature change can be derived:

K/minute < {0.5%($V_B - V_Z$) + (8 mV/minute)}/S_Z

At the early state of charging, V_B ≈ 8.4 V for 6 cells; 0.5% is a safe value for 1% detection in the TEA1100 and V_Z = 5 V.

Assuming a S_Z of +0.5 mV/K (typ. 0.2 mV/K for e.g. Zener diode PLVA450A), this results in maximum 50 K/minute.

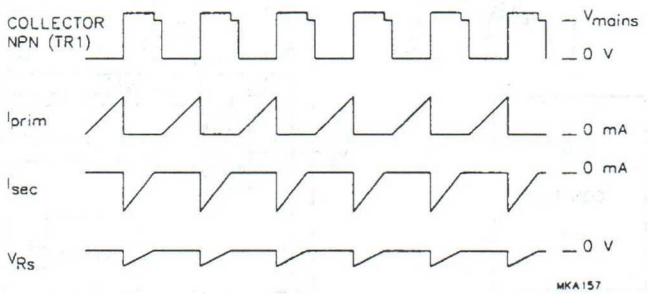


Fig.4 SMPS voltage and current waveforms.

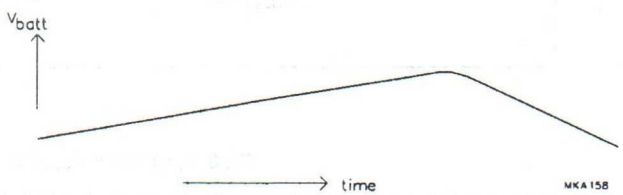


Fig.5 Battery voltage during charging.

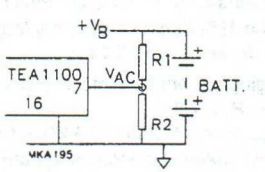


Fig.6 Basic circuit for direct battery sensing.

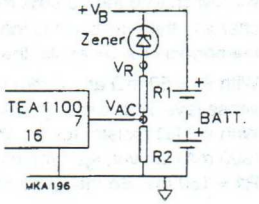


Fig.7 Basic circuit showing the use of a Zener diode.

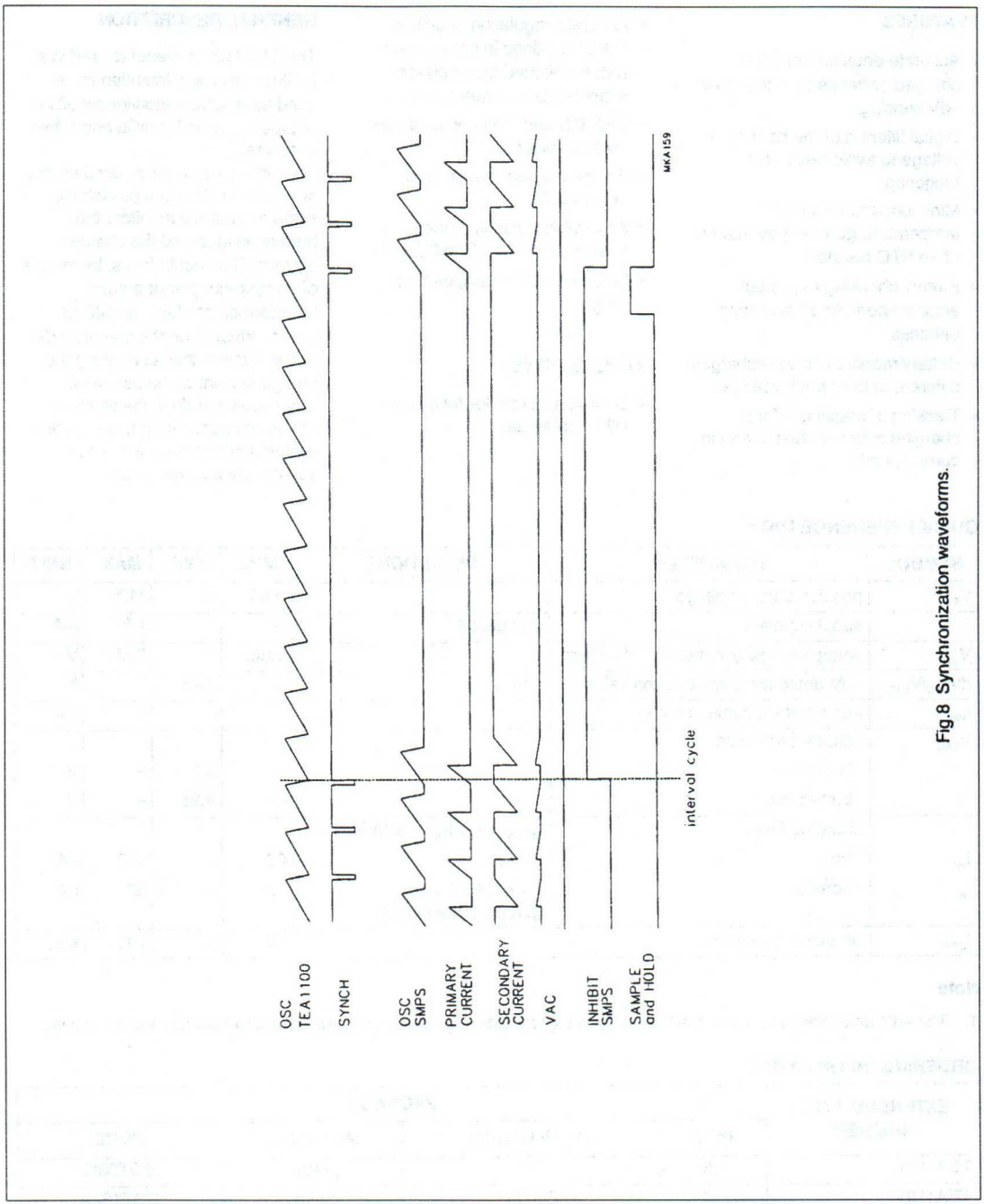


Fig.8 Synchronization waveforms.

Battery monitor for NiCd and NiMH chargers

TEA1101; TEA1101T

FEATURES

- Accurate detection of fully charged batteries by currentless –dV sensing
- Digital filtering of the battery voltage to avoid false –dV triggering
- Minimum and maximum temperature guarding by means of an NTC resistor
- Battery checking to protect against short-circuit and open batteries
- Battery monitor allows recharging different battery-pack voltages
- Tracking of maximum fast charging time with fast charging current level
- Accurate regulation of charge current settings in co-operation with a switched mode power supply or DC current source
- Both DC and PWM outputs with polarity switch
- Adjustable fast charge level (1 C to 5 C)
- Adjustable pulsating trickle charge level (0.05 C to 0.25 C)
- Large operating temperature range.

APPLICATIONS

- Charge systems for NiCd and NiMH batteries.

GENERAL DESCRIPTION

The TEA1101 is manufactured in a BICMOS process intended to be used as a battery monitor circuit in charge systems for NiCd and NiMH batteries.

The circuit has to be situated on the secondary side in mains-isolated systems where it monitors the battery voltage and the charge current. The circuit drives, by means of an opto-coupler or a pulse transformer interface, an SMPS circuit, situated on the primary side of the system, thus controlling the charge current of the batteries.

The circuit can drive the external power transistor in switched mode systems, which have a DC power source, via a driver stage.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		5.65	–	11.5	V
I_P	supply current	outputs off	–	–	4.3	mA
V_{VAC}	voltage range of battery-full detection		0.385	–	3.85	V
dV_{VAC}/V_{VAC}	–dV detection level w.r.t. top value	note 1	–	0.25	–	%
I_{VAC}	input current battery monitor		–	–	1	nA
V_{VAC}	voltage protection					
	battery low		–	0.3	–	V
	battery high		–	4.25	–	V
	charging level	$I_{charge} = R1/R_s \times I$; see Fig.3				
I_{ref}	fast	$I = I_{ref}$	20	–	100	µA
I_n	normal	$I = 1/p \times 0.1 \times I_n$ (p = prescale factor)	10	–	50	µA
f_{osc}	oscillator frequency		10	–	100	kHz

Note

1. The –dV detection level can be adjusted by use of an external voltage regulator diode to increase the sensitivity.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1101	16	DIL	plastic	SOT38G
TEA1101T	16	SO16L	plastic	SOT162A

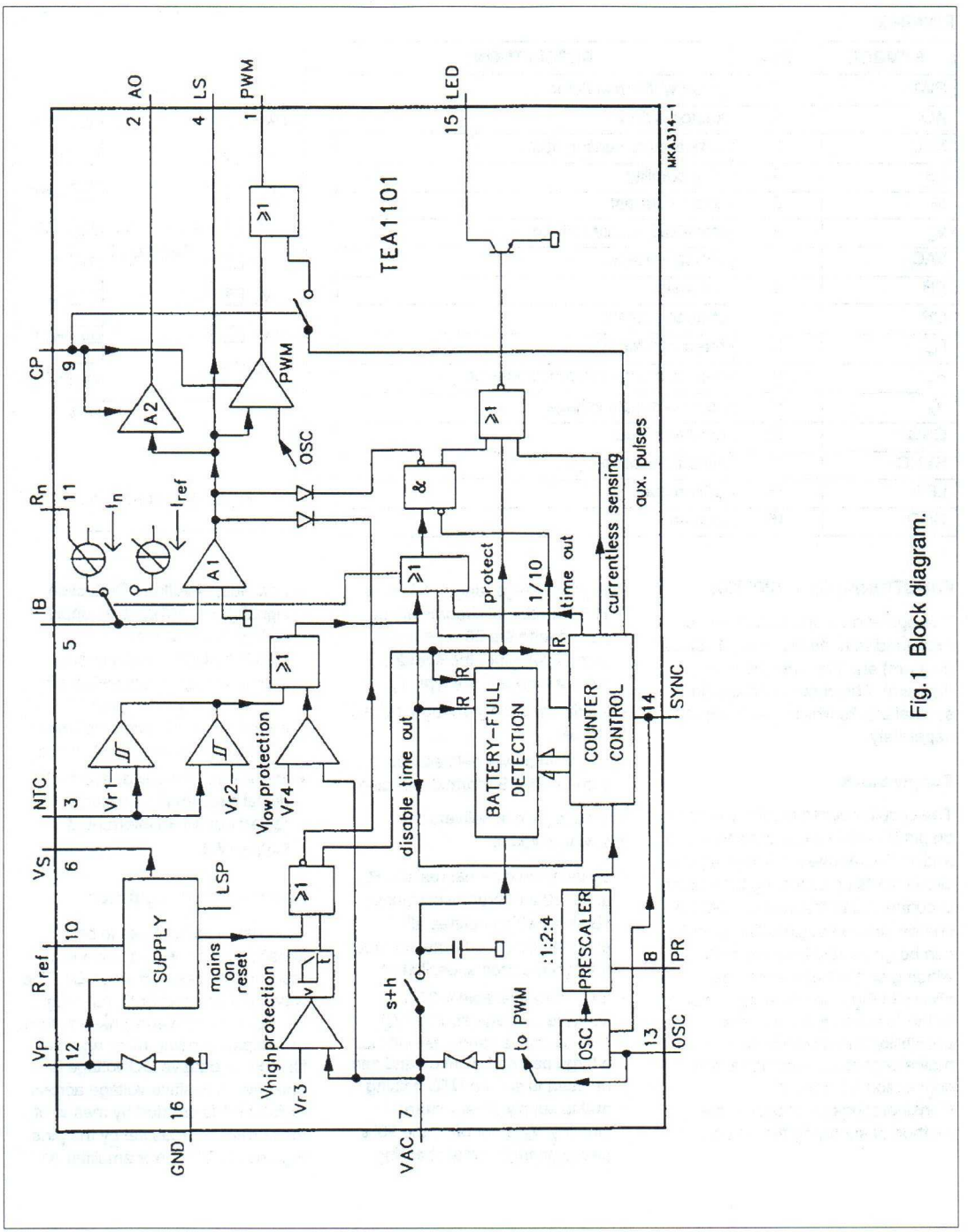


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
PWM	1	pulse width modulator
AO	2	analog output
NTC	3	temperature sensor input
LS	4	loop stability
IB	5	charge current
V_S	6	stabilized supply voltage
VAC	7	battery voltage
PR	8	prescaler
CP	9	change polarity
R_{ref}	10	reference resistor
R_n	11	normal charge reference resistor
V_P	12	positive supply voltage
OSC	13	oscillator input
SYNC	14	synchronization input
LED	15	LED output
GND	16	ground

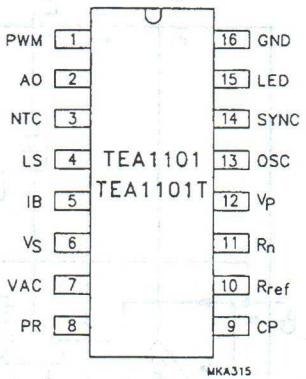


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The operation of the circuit will be explained with the aid of Fig.1 (block diagram) and Fig.3 (application diagram). The circuit is divided into several blocks which are described separately.

Supply block

The circuit requires a supply voltage on pin V_P with a value between 5.65 and 11.5 V. Above 6.4 V typical, the circuit starts up assuming that mains is connected to the system and the charge session begins. This supply can be generated by a separate winding on the transformer, as shown in Fig.3, in either the flyback or the forward stroke. Another possibility is rectification from the mains secondary winding (at the connection D1 and L2). Considerations for choosing the method of supplying the IC are:

- Supply voltage range of 5.65 to 11.5 V under all circumstances (also during the 90% pause at normal charging, the standby current then is 1 mA typical)
- Maximum battery voltage (flyback stroke)
- Minimum power delivered by the primary SMPS (normal charging)

The supply block delivers the following outputs:

- By using an external resistor R_{ref} at pin 10 a reference current is obtained which defines all external related currents (charge reference currents, oscillator)
- Externally available 4.25 V stabilized voltage source (V_S). This source is used internally for a large part of the circuit and can be used to set the NTC biasing and to supply other external circuitry. V_S is cut off in the 90% pause during normal charging
- Low Supply voltage Protection signal (LSP). When the supply voltage is lower than 5.25 V typical, there is enough supply voltage left to switch off the power regulation and hereafter the IC current is limited to the start level of 35 µA typical
- Mains on reset pulse resets all digital circuitry after a start or restart due to an interrupted supply (V_P).

Charge current regulation

The charge current has to be sensed by means of a low-ohmic resistor in series with diode D1. The waveform on resistor R_s (see Fig.5 for a flyback converter) has the form of a negative-going ramp and after filtering a negative DC voltage is obtained. A positive voltage across resistor R1 is created by means of the current sources set by the pins R_{ref} and R_n. The error amplifier A1

references the result to ground and via the regulation loop of the SMPS, the secondary current will be regulated to a value which is defined by:

$I_{ch} \times R_s = R1 \times I_{ref}$ (fast charge) or,
$I_{ch} \times R_s = R1 \times I_n$ (normal charge)

The I_{ref} current is the fast charging reference current, the I_n current is used for regulation after a full battery is detected. The I_{ref} current is the reference current set by R_{ref} while I_n is dependent on the resistor at pin R_n. With no resistor on pin R_n, the I_n current has a default value which is half the I_{ref} current.
By choosing the correct resistor values R_s, R1, R_{ref} and R_n, a wide range of charge currents can be set plus a wide range of the ratio fast charge current as a function of normal charge current. For determination of the normal charge current the 1:10 duty cycle and the programmable prescale factor (p) should be taken into account (see Logic block); $I_n = 1/p \times 0.1 \times I_n$. The output of amplifier A1 is available at the loop stability pin (LS), so the time constant of the SMPS loop can be set at the secondary side of the system.

NTC block

The voltage at the NTC pin is compared with two reference voltages. When the NTC voltage is between V_{r1} and V_{r2}, the charge current regulation is unaffected. When the NTC voltage is outside this window, the power of the SMPS is reduced to the normal charge level.
The NTC input can be used for temperature protection as shown in Fig.3 (application diagram) by using a suitable NTC resistor. To avoid switching on and off with temperature, a hysteresis is built in for both levels.

Output drivers

The SMPS regulation signal is available at different pins:

- Analog voltage output (push or pull) at AO (pin 2) to drive an opto-coupler in mains separated applications when an external resistor is connected between AO and the opto-coupler. The maximum current through the opto-coupler diode is 2 mA. The voltage gain of amplifier A2 is: $A = (V_{LS} - 1.4) \times 4$ and is typically 12 dB. The voltage at AO can also be used to directly drive a PWM input of an SMPS circuit. During 'inhibit SMPS' the AO output is fixed to zero charge current for currentless sensing
- The LS voltage is compared internally with the oscillator voltage to deliver a pulse width modulated output at PWM (pin 1) to drive an output device in a DC/DC converter application via a driver stage. The PWM output is latched to prevent multi-pulsing. Moreover with the latch a kind of current mode control is possible. The maximum duty factor is internally fixed to 78% (typical). The 'PWM' output can be used for synchronization and duty factor control of a primary SMPS via a pulse transformer (the SMPS inhibit and auxiliary pulses are also available at pin PWM)
- The AO and PWM outputs can be changed in polarity by programming the change polarity pin CP. The PWM output in the on-state pushes current (CP = 0) or pulls current (CP = 1). The appearance of the auxiliary pulses at pin PWM can also be programmed with CP.

The 'LED' output pin offers the following output signals:

- 10/90% signal for driving a LED when the duty factor is too small during the 10% time. This occurs when there is a large difference between fast and normal charge currents. The LED frequency is $f_{LED} = 2^{-12} \times 1/p \times f_{osc}$
- An SMPS inhibit period (duration 10 OSC pulses) for currentless VAC sensing
- VAC high voltage protection signals.

Battery monitor

Two batteries can be connected directly to the 'VAC' pin (Voltage ACcumulator). At higher battery voltages it is advised to divide the battery voltage with a factor by an external resistor tap, before offering this to pin VAC. It is also possible to take a tap on the chain of batteries. The VAC voltage range has to be between 0.385 V and 3.85 V.
The VAC voltage is sampled at a low cycle frequency ($f_{cycle} = 2^{-16} \times f_{osc}$) and the analog value of VAC is digitized and stored in a register. One cycle later, the digitized value is converted back to the analog value and compared with the actual value of VAC. If the actual value is higher, then the new VAC voltage is stored in the register, otherwise no conversion is carried out. Thus the VAC top value is stored and it is possible to detect an increasing VAC indicating 'not yet full batteries' or decreasing VAC indicating that the batteries are probably fully charged. The circuit waits until the battery voltage has dropped 0.25% below the top value before indicating 'full batteries'. However, by applying a voltage regulator diode in the battery voltage sense-line (see Fig.8) an increased sensitivity of the –dV detection level can be obtained, e.g. 0.125%.
In Fig.6 the battery voltage as

function of the charging time is shown. The negative slope depends on the charge current and the battery type.

The switching of the SMPS can cause interference on the battery voltage and therefore it has been necessary to stop the SMPS during the inhibit time (see Fig.9). This can be achieved automatically via the regulation pins AO and PWM or by using the SYNC output of the logic block. The SMPS is stopped for 10 periods at the end of which sampling is carried out. The VAC voltage will now be sensed currentless. To avoid false decisions concerning a falling VAC voltage, VAC is digitally filtered and analog stored in a sample-and-hold circuit. This approach ensures, even at very high –dV sensitivity (<0.25%) accurate detection of the battery full condition. Immediately after decisions and VAC digitizing takes place. The benefit of a sample-and-hold circuit is that at high frequencies the noise on the VAC voltage is filtered and the VAC manipulations like decisions and digitizing are carried out on the same VAC voltage available in the sample-and-hold circuit.

When a –dV is detected, the reference current I_{ref} is switched off, the normal current I_n is switched on during 10% of regulation and the outputs are high-ohmic during 90%. This 1:10 ratio in active regulation, together with the ratio in reference currents (I_n as a function of I_{ref}), ensures that the resulting charge current is low enough to be allowed to flow through the batteries for a long time to overcome the self-discharge of the batteries without causing memory effects. If the prescale factor p is programmed, the I_n current has to be lowered with the p factor, so $I_n = 1/p \times 0.1 \times I_n$.

Protections

- The circuit goes into standby (not active, low current consumption) when the supply voltage is less than 5.25 V (LSP).
- When the divided battery voltage exceeds the V_{r3} level (nominal 4.25 V) this is recognized as open or removed batteries and the output control signals terminate to stop the SMPS operation. This over-voltage sensing is digitally filtered. In above events the 'battery full detector' and the 'counter/control' will be reset.
- When the divided battery voltage is less than V_{r4} (0.3 V), the circuit assumes short-circuited batteries, the charge current is reduced to the normal charge level. As soon as the voltage exceeds V_{r4}, the fast charging starts.
- The temperature protections are already mentioned in section NTC. In the event of short-circuited batteries or active temperature protections the 'battery full detector' is reset and the 'counter/control' is stopped.

Oscillator and control logic

The complete timing of the circuit is controlled by the oscillator.
The period time is defined by:
$T_{osc} = 0.93 \times R_{ref} \times C_{osc}$.

The counter block defines a maximum fast charge time called 'Time Out' (TO). As the charge current and the oscillator frequency (and thus the TO) are both set by R_{ref}, changing one affects the other. Initially the oscillator capacitor can be chosen such that the fast charge time is half the TO time. This means that in the event of a one hour (1C) charger, the TO signal occurs at 2 hours, in the event of a quarter of an hour (4C) charger, the TO signal is active after half an hour. After that the circuit switches over to normal charging.

To adapt the SMPS switching frequency in the synchronized mode to the required oscillator frequency of the timing logic, the timer logic is preceded by a programmable divider. The divider ratio can be set to 1, 2 or 4 (p factor) by means of the PR pin. Doing this means that the oscillator frequency can be increased with the factor p without changing TO.

Fast charging current:
$I_{ch} = R1/R_s \times V_{ref}/R_{ref}$
Time out:
$TO = 2^{26} \times 0.93 \times R_{ref} \times C_{OSC} \times p$
Normal charging current:
$I_{ch} = R1/R_s \times 1/p \times 0.1 \times V_{ref}/R_n$

The control block determines the following timing sequences:

- VAC sampling; this takes 1 clock pulse every interval cycle.

  The power converter is switched off during VAC sampling. As there are several types of converters, there also are several control signals available at :

  pin 'SYNC' for synchronization in analog voltage controlled primary SMPS circuits

  pin 'PWM' for digital controlled primary SMPS and DC/DC converters

  pin 'LED' in special applications
- Disabling –dV during $2^{-5} \times TO$ (3% of TO) for correct start with flat or inversely polarized batteries. Disabling is active at each fast charge cycle
- Maximum fast charging time (TO): the maximum timer is stopped during VAC low voltage protection and outside temperature range

- The normal charge duty cycle is 1/p x 0.1
- Auxiliary pulses to support the supply voltage of the primary SMPS circuit via pin PWM: the pulses can be programmed on and off at an appearance rate of $f_{osc}/8$ with a duty cycle of 14%; programming is achieved by activating CP.

The timing logic and the –dV recognition circuitry are reset after each supply voltage failure and after a battery over-voltage recognition. The –dV circuit is also reset during normal charging.

The SYNC output delivers negative-going synchronization pulses which are suppressed during the sampling of the battery voltage. With these sync pulses the SMPS can be synchronized.The polarity of the sync pulses is chosen so that in the event of an open SYNC pin in the synchronization mode, the power is regulated to a minimum. During the VAC sampling the absense of sync pulses causes the SMPS to stop thus minimizing interference (see Fig.9, synchronization waveforms).

During the 90% pause, only the oscillator and the control logic are operative to save current. In the pause V_P is never allowed to become less than V_{LSP}. This would cause a 'mains-on-reset' and thus fast charging.

Programming

With pins 'CP' (change polarity) and 'PR' (prescaler) several functions can be programmed.

By defining the current (V_{ref}/R_{CP}) at pin CP, the following functions can be activated :

1	change polarity	CP = 0, normal polarity CP = 1, changed polarity
2	no auxilliary pulses at PWM	aux = 0
3	auxilliary pulses at f/8	aux = 8

CP PIN	FUNCTIONS	
	CP	aux
Open pin	0	0
10 µA	0	8
22 µA	1	0
57 µA	1	8

By defining the voltage at pin PR, the following functions can be activated :

PR PIN	FUNCTIONS
V_S	prescaler divide by 1
Open pin	prescaler divide by 2
Ground	prescaler divide by 4

Table 1 Formulae.

DESCRIPTION	SYMBOL	FORMULA	FUNCTION
Timing	T_{osc}	$0.93 \times R_{ref} \times C_{osc}$	repetition
	TO	$2^{-26} \times p \times T_{osc}$	duration
	$T_{disable}$	$2^{-5} \times TO$	duration
	$T_{LED} = T_{trickle}$	$2^{12} \times p \times T_{osc}$	repetition
	$T_{LED} = T_{trickel}$	$3/4 \times 2^{9} \times T_{osc}$	duration
	$T_{inhibit}$	$2^{16} \times T_{osc}$	repetition
	$T_{inhibit}$	$10 \times T_{osc}$	duration
Charge currents	I_{fast}	$R1/R_s \times V_{ref}/R_{ref}$	
	I_{normal}	$R1/R_s \times 1/p \times 0.1V_{ref}/R_n$	

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134); note 1.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
Voltages				
V_P	positive supply voltage (pin12)	−0.5	13.2	V
V_{LED}	LED voltage (pin 15)	−0.5	13.2	V
$V_{1,8,4,3}$	voltage at PWM (pin 1), PR (pin 8), LS (pin 4), NTC (pin 3)	−0.5	V_P	V
V_{IB}	voltage at IB (pin 5)	−0.5	+1	V
Currents				
I_{VS}	current at V_S (pin 6)	−3	+0.01	mA
I_{LED}	current at LED (pin 15)	−	25	mA
I_{AO}	current at AO (pin 2)	−5	+5	mA
I_{PWM}	current at PWM (pin 1)	−15	+15	mA
I_{SYNC}	current at SYNC (pin 14)	−2	+2	mA
$I_{11,10,9}$	current at R_n (pin 11), R_{ref} (pin 10), CP (pin 9)	−1	+0.01	mA
$I_{4,5,7}$	current at LS (pin 4), IB (pin 5), VAC (pin 7)	−1	+1	mA
I_P	current at V_P (pin 6)	−	15	mA
Dissipation				
P_{tot}	total power dissipation at T_{amb} = 85 °C			
	SOT38G	−	0.6	W
	SOT162A	−	0.3	W
Temperatures				
T_{amb}	operating ambient temperature	−20	+85	°C
T_j	junction temperature	−	+150	°C
T_{stg}	storage temperature	−55	+150	°C

Note

1. All voltages with respect to ground; positive currents flow into the IC; all pins not mentioned in the voltage list are not allowed to be voltage driven. The voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the power rating is not violated.

CHARACTERISTICS

V_P = 10 V; T_{amb} = 25 °C; R_{ref} = 33 kΩ; R_n = 68 kΩ; C_{OSC} = 1 nF; CP open-circuit; PR connected to V_S; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (V_P, V_S, R_{ref})						
V_P	supply voltage range		5.65	–	11.5	V
V_{PC}	clamping voltage	I_{PC} = 10 mA	11.5	–	12.8	V
V_{PS}	start voltage		6.1	6.4	6.7	V
V_{PLSP}	low supply protection level		4.85	5.25	5.65	V
V_{PLSPH}	hystereris of V_{PLSP}		0.5	0.95	–	V
I_P	supply current	outputs off	–	–	4.3	mA
I_{PP}	supply pause current	V_P = 6 V	–	–	1.71	mA
I_{PSB}	standby current	V_P = 4 V	–	35	45	µA
V_S	source voltage (stabilized)	I_S = 1 mA	4.03	4.25	4.46	V
V_{ref}	reference voltage	I_{ref} = 20 µA	1.18	1.25	1.31	V
TC	temperature coefficient of V_{ref}	T_{amb} = 0 to 45 °C	–	±100	±200	ppm/K
PSRR	power supply rejection ratio of V_{ref}	f = 100 Hz; dV_P = 2 V (p-p); V_P = 8 V	–46	–	–	dB
ΔV_{ref}	voltage difference	dI_S = 1 mA	–	–	5	mV
I_{Rref}	current range of R_{ref}		10	–	100	µA
Charge current regulation (IB, R_n, R_{ref})						
V_n	voltage at pin R_n	I_n = 10 µA; I_{ref} = 20 µA	1.17	1.25	1.32	V
I_n	current range at R_n		5	–	50	µA
I_{IB}/I_{ref}	input current ratio	R_n not connected				
	normal charging	V_{IB} = 0	0.475	0.5	0.525	
	fast charging	V_{IB} = 0	0.95	1	1.05	
I_{IB}/I_n	input current ratio	R_n connected				
	normal charging		0.90	0.97	1.04	
V_{thIB}	threshold voltage at IB					
	T_{amb} = 25 °C		–2	–	+2	mV
	T_{amb} = 0 to 45 °C		–3	–	+3	mV
NTC input						
V_{NTCSPH}	switching protection voltage on high temperatures		0.75	0.81	0.87	V
V_{NTCHH}	hysteresis of V_{NTCSPH}		60	90	120	mV
V_{NTCSPL}	switching protection voltage on low temperatures		2.78	3.00	3.20	V
V_{NTCHL}	hysteresis of V_{NTCSPL}		65	100	135	mV
I_{NTC}	input current	V_{NTC} = 2 V	–5	–	+5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output drivers (AO, LS, PWM, LED)						
$I_{AOsource}$	source current	V_{AO} = 3 V; CP = 0	–	–	–2	mA
I_{AOsink}	sink current	V_{AO} = 0.5 V; CP = 1	2	–	–	mA
g_m	transconductance A1	V_{IB} = 50 mV	–	300	–	µS
G_{v1}	voltage gain A1 x A2	V_{AO} = 2 V (p-p)	–	72	–	dB
G_{v2}	voltage gain A2	V_{AO} = 2 V (p-p)	–	12	–	dB
$I_{LSsource}$	maximum source current	V_{LS} = 2.25 V	–25	–21	–16	µA
I_{LSsink}	maximum sink current	V_{LS} = 2.25 V	16	21	25	µA
I_{PWMH}	HIGH level output current	V_{PWM} = 3 V	–18	–14	–10	mA
I_{PWML}	LOW level output current	V_{PWM} = 0.5 V	7	12	17	mA
$I_{PWMleak}$	leakage current	V_{PWM} = 4.25 V	–	0.2	10	µA
δ_{PWM}	maximum duty cycle		70	78	86	%
δ_{PWMaux}	auxiliary pulse duty cycle		12.6	14	15.4	%
V_{LEDsat}	saturation voltage	I_{LED} = 15 mA	–	–	600	mV
$I_{LEDleak}$	leakage current	V_{LED} = 10 V	–	–	5	µA
Battery monitor (VAC)						
I_{VAC}	input current	V_{VAC} = 4.25 V	–	1	–	nA
V_{VAC}	voltage range of –dV detection		0.385	–	3.85	V
dV_{VAC}/V_{VAC}	–dV detection level w.r.t. top level	V_{VAC} = 2 V	–	0.25	–	%
ΔV_{VAC}	resolution –dV		0.42	0.6	0.78	mV
T_{-dV}	temperature range of –dV detection		0	–	50	°C
Protections (VAC)						
V_{VACLBP}	low battery voltage protection		–	0.3	0.33	V
V_{VACHBP}	high battery voltage protection	with respect to V_P	–	0	150	mV
Oscillator, logic (OSC, SYNCH)						
V_{OSCH}	oscillator switching level HIGH		–	2.5	–	V
V_{OSCL}	oscillator switching level LOW		–	1.5	–	V
K	period time	$T_{OSC} = K \times R_{ref} \times C_{OSC}$	0.84	0.93	1.02	
f_{OSC}	oscillator frequency range		10	–	100	kHz
V_{SYNCH}	SYNC output level HIGH	I_{SYNCH} = –0.4 mA	3.4	–	–	V
V_{SYNCL}	SYNC output level LOW	I_{SYNCL} = 0.4 mA	–	–	0.85	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Programming (CP)						
I_{CP}	programming currents					
	CP = 0; aux = 0	R_{CP} = 330 kΩ	–	–	4.2	μA
	CP = 0; aux = 8	R_{CP} = 120 kΩ	9.4	10.4	11.4	μA
	CP = 1; aux = 0	R_{CP} = 56 kΩ	20.0	22.3	24.5	μA
	CP = 1; aux = 8	R_{CP} = 22 kΩ	51.1	56.8	62.5	μA

QUALITY SPECIFICATION

General quality specification for integrated circuits: UZW-B0/FQ-0601.

Note: For the synchronization pin (14), the ESD positive zap voltage is restricted to a maximum of 1000 V.

TEST AND APPLICATION INFORMATION

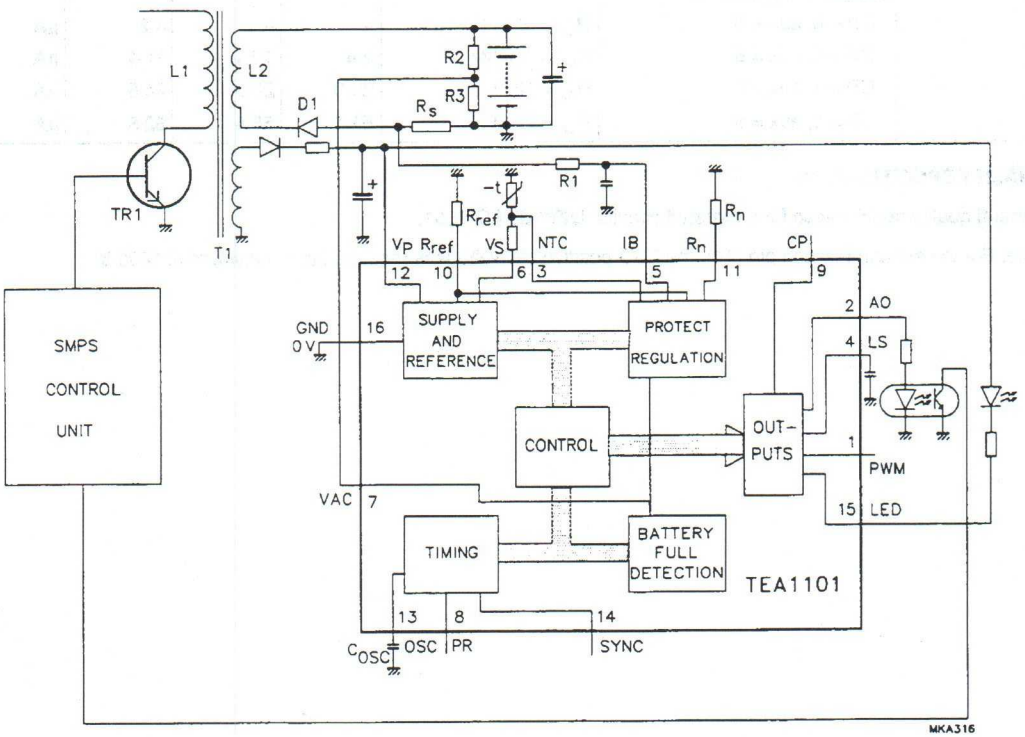


Fig.3 Application diagram.

Notes to Fig.3

1. Signaling the status of the charging session can be achieved by an LED-diode-resistor combination parallel to L2 (transformer T1). During the fast charging period the LED will burn continuously. During normal charging the LED will switch with the 10/90% rhythm. With mains-off the LED is off, thus not discharging the batteries. If at normal charging the duty cycle is too low during the 10% because of a very large difference between the fast charge and the normal charge levels, the LED can be driven by the LED pin.
2. With R_s = 50 MΩ and a required fast charging current level of 6 A (5C for 1.2 Ah batteries), the average current sense level is 300 mV. Power dissipation in R_s = 1.8 W.

   With a 3 kΩ resistor for R1, the required I_{ref} current is 300 mV/3 kΩ = 100 μA. For a normal charge level of 0.25C (300 mA) the voltage drop over R_s is 15 mV. Taking into account the duty cycle of 10%, the voltage drop over R1 = 150 mV. Thus the I_{Rn} current has to be 150 mV/3 kΩ = 50 μA (p = 1).

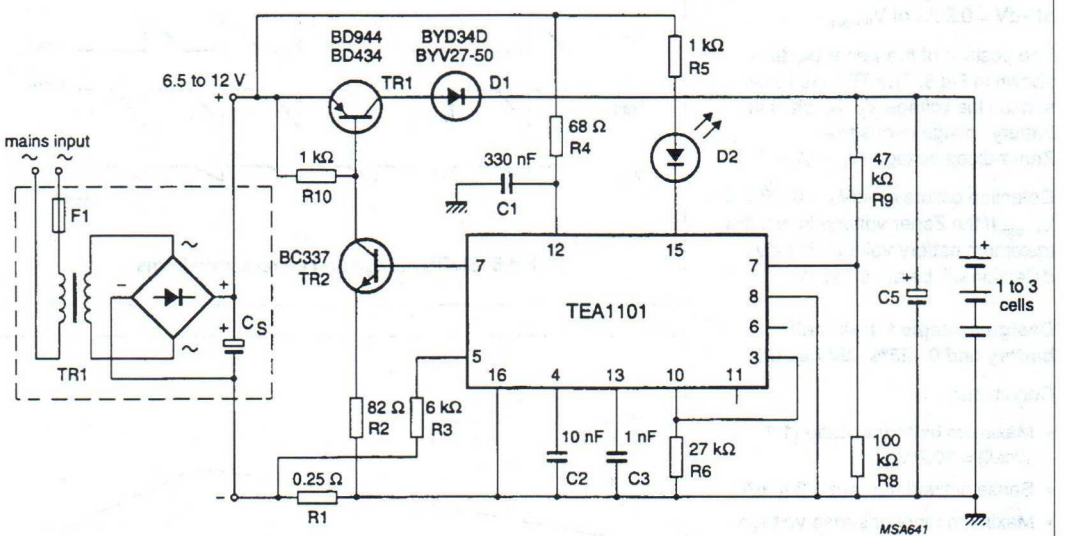


Fig.4 Battery charger with linear regulator.

Method to increase –dV sensitivity

The basic, direct battery sensing via a resistive divider, which adapts the battery voltage within the V_{AC} range, is shown in Fig.7. Detection occurs at –dV = 0.25% of $V_{B(max)}$.

The position of the Zener diode is shown in Fig.8. The TEA1101 now senses the voltage V_R, which is the battery voltage minus the Zener-diode voltage ($V_R = V_B - V_Z$).

Detection occurs at $-dV_R$ = 0.25% of V_{Rmax}. If the Zener voltage is half the maximum battery voltage, the dV_B detection will be at –0.125%.

Design example for six-cell battery and 0.125% –dV cut-off

Conditions:

- Maximum battery voltage (1.7 V/cell) = 10.2 V
- Sense network current ≈ 300 μA
- Maximum monitor sense voltage V_{AC} = 3.6 V (< 3.85 V).

For –dV ≈ 0.125%, a Zener voltage of about half the battery voltage is required; choose V_Z = 5 V. Now V_R at top level is ≈ 5.2 V and the required divider factor (V_{AC}/V_R) is 0.69. R1 and R2 become 5.6 kΩ and 12 kΩ respectively (see Figs 6 and 7).

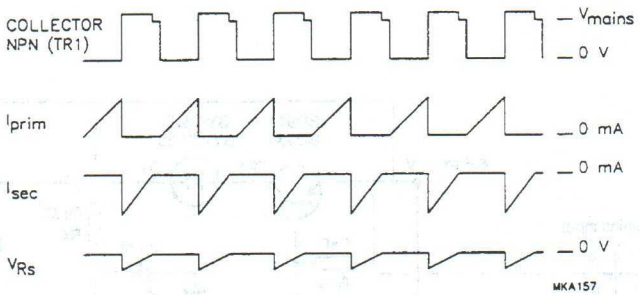


Fig.5 SMPS voltage and current waveforms.

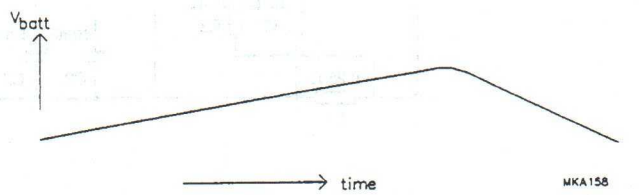


Fig.6 Battery voltage during charging.

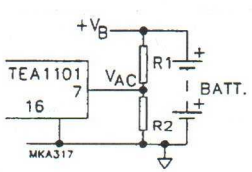


Fig.7 Basic circuit for direct battery sensing.

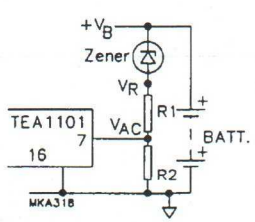


Fig.8 Basic circuit showing the use of a Zener diode.

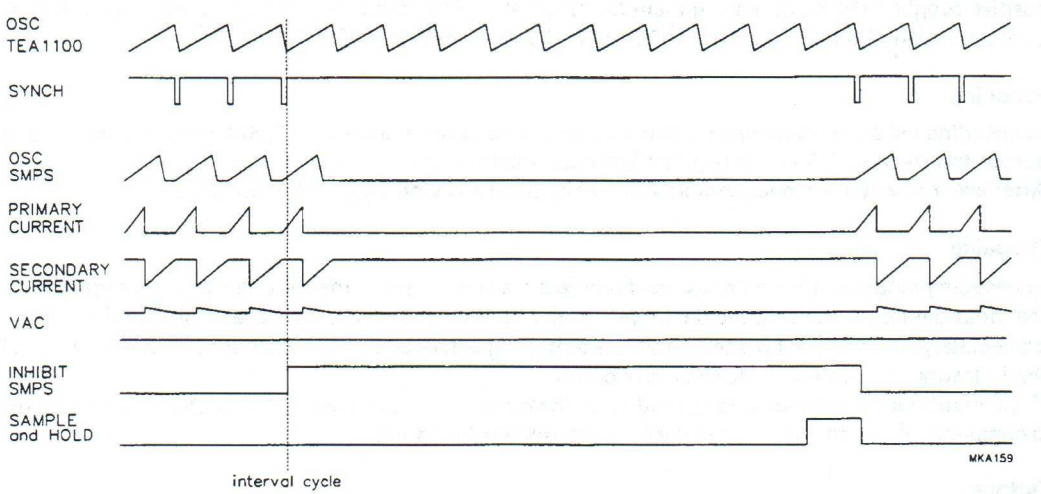


Fig.9 Synchronization waveforms.

Coded locking circuit for security systems

TEA5500
TEA5500T

GENERAL DECRIPTION

The TEA5500 is an encoder/decoder circuit, for security systems. The system has the ability to transmit a complex code between an encoding and decoding unit by infrared radiation. The device can operate as an encoder or decoder depending on the external circuitry connected to the data input. The code is made by the 10 input pins E1 to E10 by connecting them either to ground (LOW) or to the positive supply (HIGH), or leaving them floating (∞). This allows $3^{10}-2$ combinations. Two combinations are prohibited; E1 to E10 = HIGH and E1 to E9 = HIGH, E10 = LOW.

Encoding

In encoding mode the data input is connected to V_P and both outputs (S1, S2) are connected to a pnp output transistor which drives (e.g.) an infrared radiation emitting diode.
After every start the encoder completes three coding runs then stops automatically.

Decoding

In decoding mode an infrared sensitive diode (e.g.) is connected to the data input via an amplifier. If the input data is recognized, the data input of the decoder is temporarily closed (disregarding immediately following data) and one of the outputs is activated for a predetermined time after which the following start will activate the other output.
If the input data is not recognized, neither of the outputs are activated and after the third coding run is completed the data input of the decoder is temporarily closed.

Output

The output is an open-collector configuration (npn), which is active LOW. It can handle a higher supply voltage than V_P (i.e. 16 V max.).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 16)	V_P = 4.5 V	V_P	3.0	4.5	6.5	V
Supply current (pin 16)		I_P	1.8	2.5	3.2	mA
Operating ambient temperature range		T_{amb}	−40	–	+80	°C
Storage temperature range		T_{stg}	−50	–	+150	°C
Total power dissipation		P_{tot}	–	–	500	mW
Maximum voltage at outputs (pins 3,4)		V_O	–	–	16	V

PACKAGE OUTLINES

TEA5500: 16-lead DIL; plastic (SOT38).
TEA5500T: 16-lead mini-pack; plastic (SO16L; SOT162A).

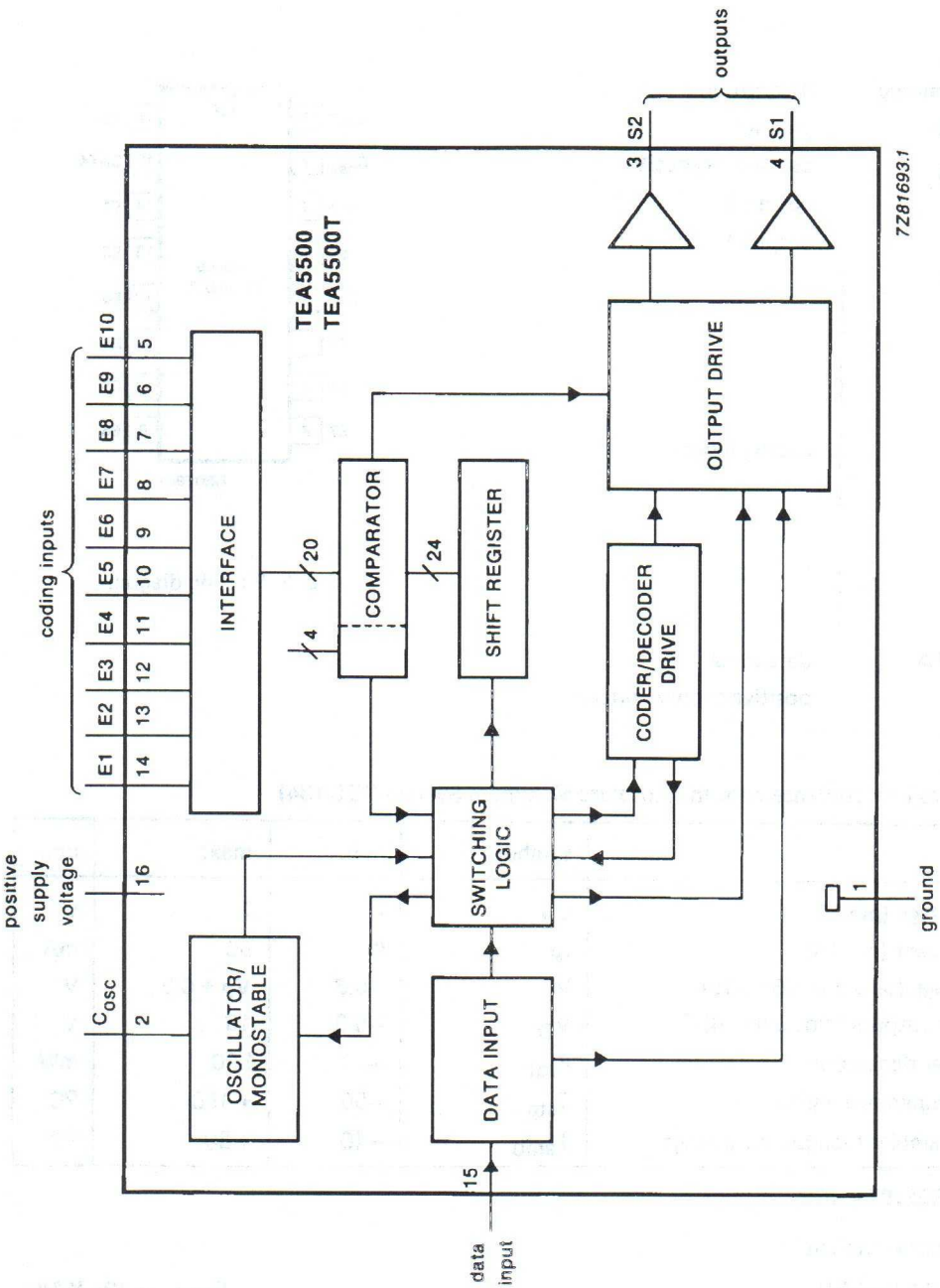


Fig. 1 Block diagram.

PINNING

Pin functions

pin	mnemonic	description
1	GND	ground
2	C_{osc}	oscillator capacitor
3	S2	output 2
4	S1	output 1
5	E10	coding inputs
6	E9	
7	E8	
8	E7	
9	E6	
10	E5	
11	E4	
12	E3	
13	E2	
14	E1	
15	DATA	data input
16	V_P	positive supply voltage

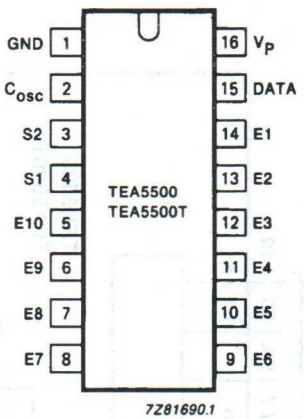


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 16)	V_P	–	7	V
Supply current (pin 16)	I_P	0	50	mA
Input voltage (pins 2 and 5 to 15)	V_I	–0.3	V_P + 0.3	V
Voltage at outputs (pins 3 and 4)	V_O	–0.3	16	V
Total power dissipation	P_{tot}	–	500	mW
Storage temperature range	T_{stg}	–50	+ 150	°C
Operating ambient temperature range	T_{amb}	–40	+ 80	°C

THERMAL RESISTANCE

From junction to ambient

TEA5500: 16-lead DIL — $R_{th\ j\text{-}a}$ = 125 K/W
TEA5500T: 16-lead mini-pack — $R_{th\ j\text{-}a}$ = 160 K/W

CHARACTERISTICS

T_{amb} = 25 °C; voltages with respect to pin 1; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 16)		V_P	3	4.5	6.5	V
Supply current	V_P = 4.5 V	I_P	1.8	2.5	3.2	mA
Zener diode voltage across supply	note 1	V_Z	–	–	8	V
Inputs E1 to E10						
Input voltage HIGH		V_{IH}	V_P −0.3	–	–	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input voltage floating		V_{IFL}	1	–	V_P −1	V
Input current HIGH		I_{IH}	2	7	12	μA
Input current LOW		I_{IL}	−4	−9	−15	μA
Input current floating		I_{IFL}	–	–	2	μA
Data input						
Input voltage						
for encoding mode		V_{de}	V_P −0.6	V_P	V_P +0.3	V
for decoding mode HIGH		V_{ddH}	0.8	–	0.5 V_P	V
for decoding mode LOW		V_{ddL}	–	–	0.5	V
Input current						
in encoding mode	V_{15} = V_P = 4.5 V	I_{de}	8	16	25	μA
in decoding mode HIGH	V_{15} = 2 V; V_P = 4.5 V	I_{ddH}	–	–	2	μA
in decoding mode LOW	V_{15} = 0.3 V; V_P = 4.5 V	I_{ddL}	−8	−16	−25	μA
Minimum pulse width of DATA input signal		r_{dp}	2	–	–	μs
Output (pins 3 and 4)						
Output sink current	output active; V_P = 4.5 V	$I_{O\ (sink)}$	25	–	–	mA
Voltage at output		V_O	–	–	16	V

Note to the supply characteristics

1. Maximum Zener diode current 10 mA.

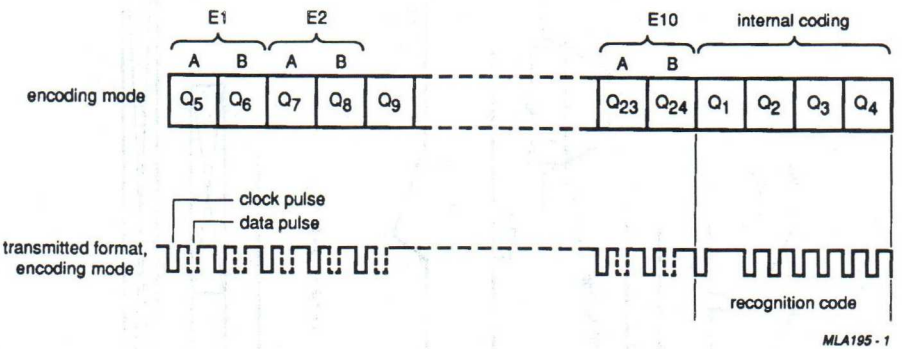
parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator characteristics	V_P = 4.5 V					
Switching voltage thresholds						
high level		V_{th}	3.10	3.32	3.50	V
low level		V_{tl}	0.65	0.71	0.90	V
Input current						
after switching high level		I_{th}	27	36	45	μA
after switching low level		I_{tl}	−6.7	−9	−11.3	μA
Ratio I_{th}/I_{tl}		ΔI_{osc}	3	4	5	
Duration of oscillator pulse						
in coding mode	note 1	τ_c	20	$0.4 \cdot C_{osc}$(pF)	–	μs
in decoding mode		τ_d	$3 \cdot \tau_c$	$0.4 \cdot C_{osc}$(pF)	$5 \cdot \tau_c$	μs
Oscillator capacitor						
in coding mode	notes 1 and 2	C_{osc}	56	–	–	pF
Duration of						
output active status		τ_o	–	$384 \cdot \tau_d$	–	
data input disabled status		τ_x	–	$576 \cdot \tau_d$	–	
Influence of temperature on duration of oscillator pulse		$\frac{\Delta\tau_c/\tau_c}{\Delta T}$	–	0.002	–	K^{-1}
Influence of supply voltage on duration of oscillator pulse		$\frac{\Delta\tau_c/\tau_c}{\Delta V_P}$	–	–	0.16	V^{-1}

Notes to the oscillator characteristics

1. Minimum value encoder – capacitor must provide minimum pulse width of DATA pulse τ_{dp} (= 0.2 τ_c).
2. Ratio encoder/decoder capacitor 1 : 4.

Code

The code consists of 24 bits. Each bit is represented by presence or absence of a data pulse following a clock pulse. The first 10 pairs of bits are determined by the connections of the input pins (E1 to E10). The last 4 bits form the recognition code. For the corresponding code in decoding mode the order of the input pins is reversed and connections "low" (L) and "floating" (∞) are interchanged.



encoding	E1	E2	E3	-----	E8	E9	E10	∞	L	H
decoding	E10	E9	E8	-----	E3	E2	E1	L	∞	H

E	A	B	Q_A	Q_B
L	1	0	0	1
∞	0	1	1	0
H	1	1	0	0

example

encoding	E1 = L	E2 = H	E3 = ∞	E4 = H	-----	E9 = L	E10 = ∞
decoding	E10 = ∞	E9 = H	E8 = L	E7 = H	-----	E2 = ∞	E1 = L

Fig. 3 Coding diagram.

TIMING

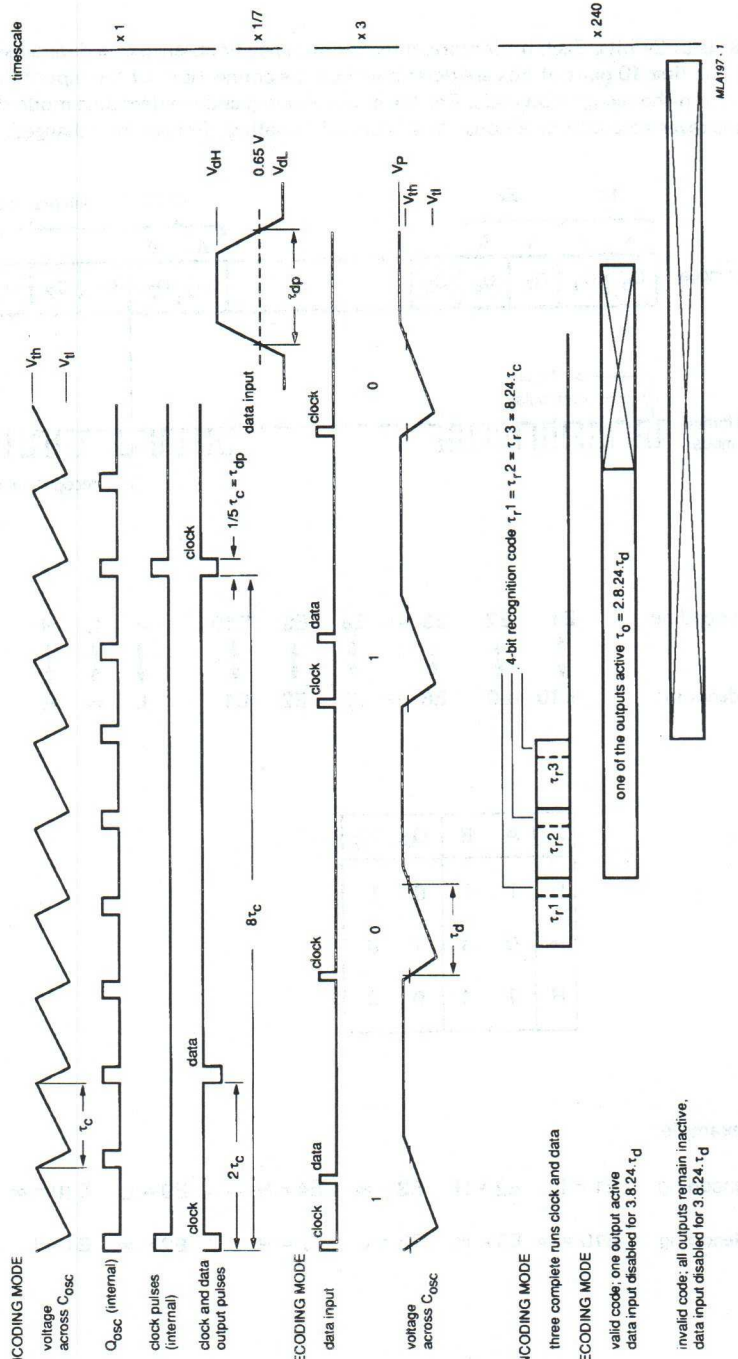
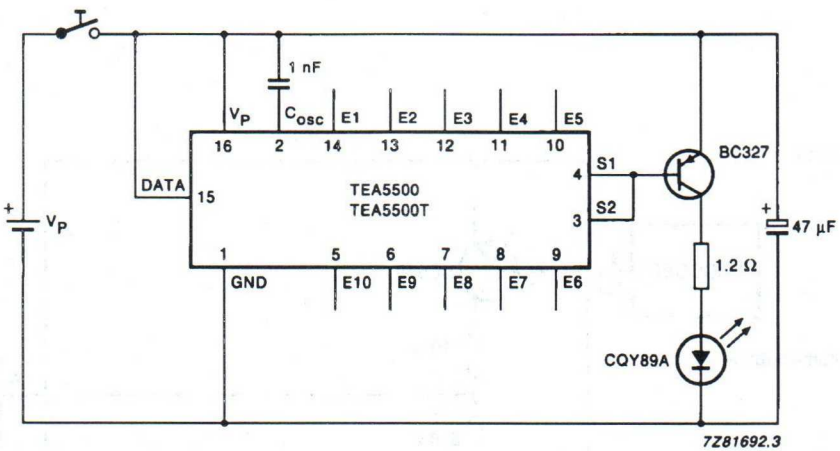


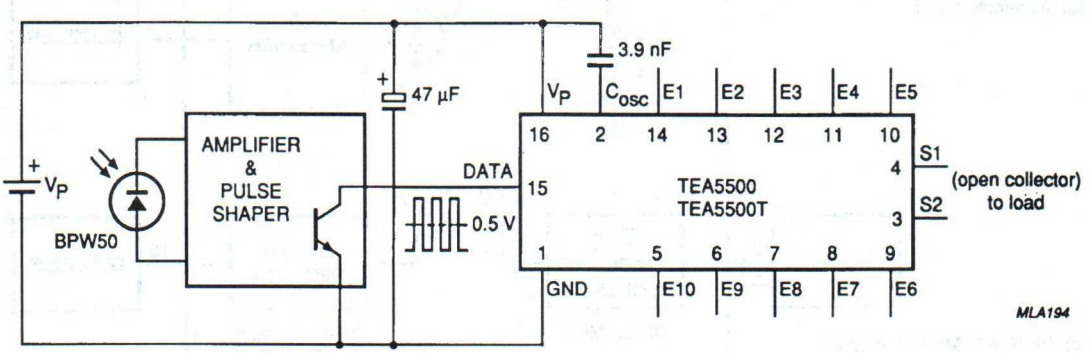
Fig. 4 Timing diagram of TEA5500.

APPLICATION INFORMATION



E1 – E10: code (H, L, ∞).

Fig. 5 Application diagram; coding mode.



E10 – E1: code (H, ∞, L).

Fig. 6 Application diagram; decoding mode.

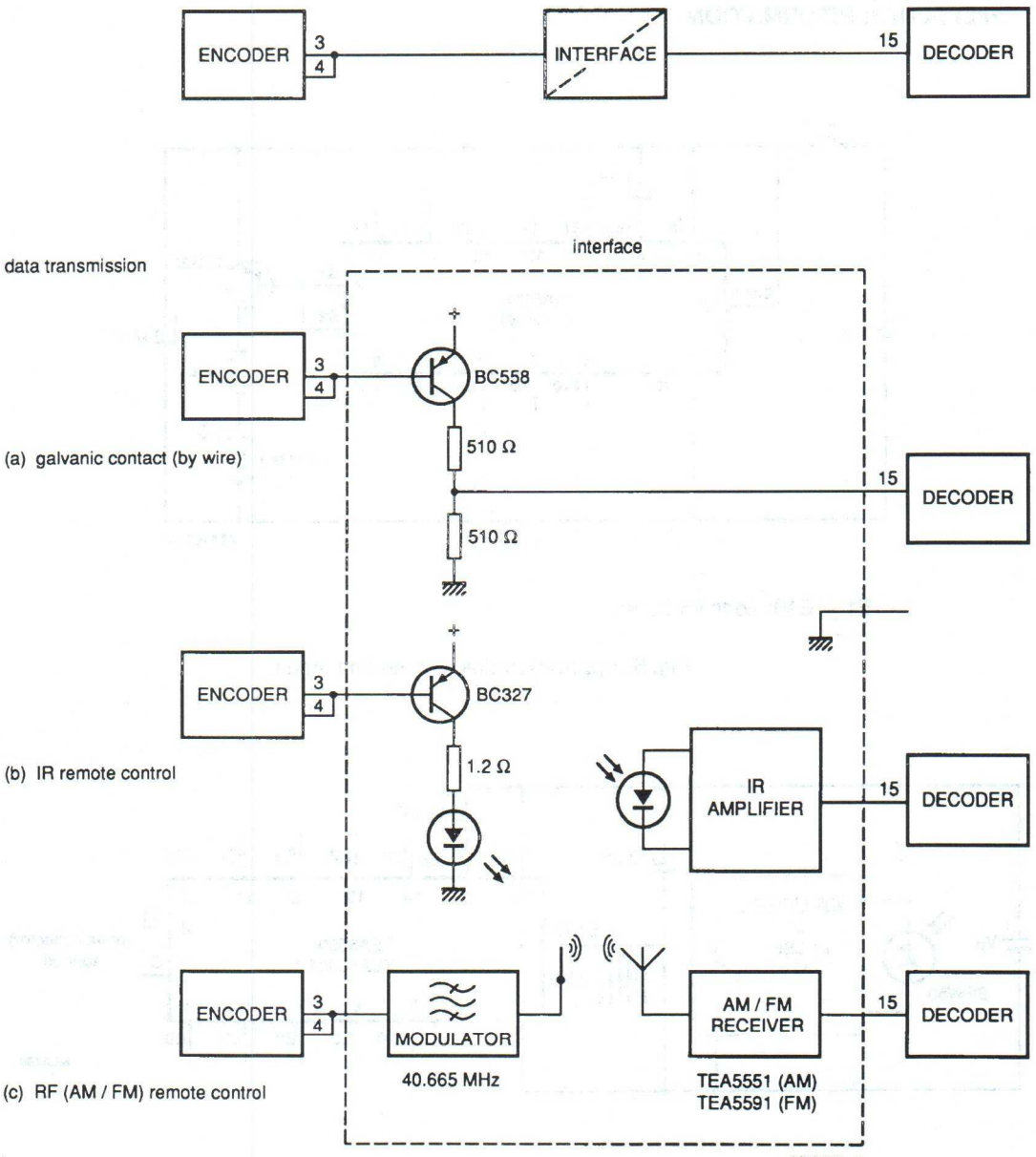


Fig. 7 Application diagram; types of data transmission possible by using different interfaces.

Coded locking circuit for security systems (one-shot output; 6.5k codes)

TEA5501

GENERAL DESCRIPTION

The TEA5501 is an encoder/decoder circuit, for security systems. In the system a complex code is transmitted between an encoding and a decoding unit by e.g. infrared radiation, RF or direct galvanic contact. It can be used as an electronic lock or for (de)activating an alarm. The device can operate as an encoder or decoder. The code (6561 combinations) is hardware programmable.

Features

- Universal encoder/decoder circuit
- 6561 hardware programmable combinations
- Error protection: transmitted code is repeated twice
- Scanning protection: after receiving three invalid codes, data input is disabled for a short time
- Low supply voltage
- High output current

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 14)		V_P	3.0	4.5	6.5	V
Supply current (pin 14)	V_P = 4.5 V	I_P	1.8	2.5	3.2	mA
Operating ambient temperature range		T_{amb}	−40	−	+ 85	°C
Storage temperature range		T_{stg}	−50	−	+ 150	°C
Total power dissipation		P_{tot}	−	−	500	mW
Maximum voltage at output (pin 3)		V_O	−	−	16	V

PACKAGE OUTLINE

14-lead DIL; plastic (SOT27).

Coded locking circuit for security systems (one-shot output; 6.5k codes)

TEA5501

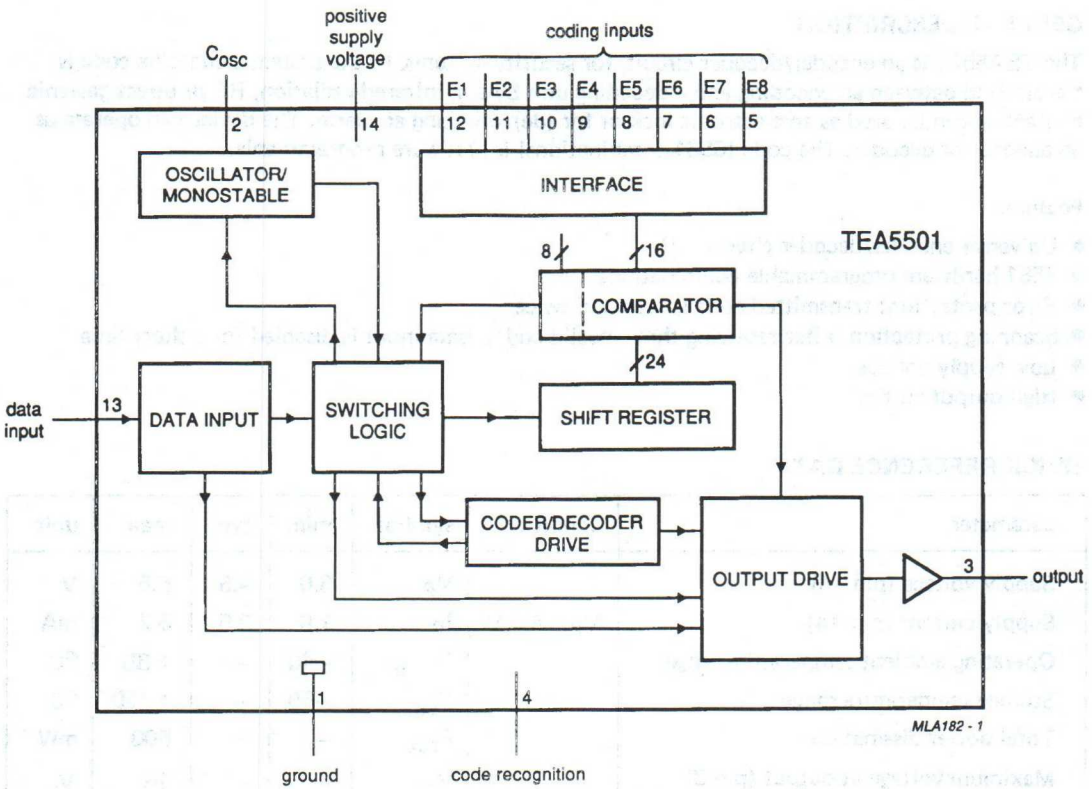


Fig.1 Block diagram.

Coded locking circuit for security systems (one-shot output; 6.5k codes) — TEA5501

PINNING

Pin functions

pin	mnemonic	description
1	GND	ground
2	C_{osc}	oscillator capacitor
3	S	output
4	E_{recogn}	code recognition
5	E8	coding inputs
6	E7	
7	E6	
8	E5	
9	E4	
10	E3	
11	E2	
12	E1	
13	DATA	data input
14	V_P	positive supply voltage

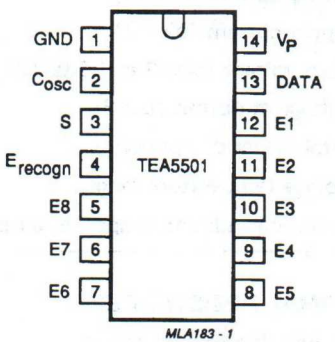


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The TEA5501 is an encoder/decoder circuit, for security systems. The system has the ability to transmit a complex code between an encoding and decoding unit by e.g. infrared radiation, RF or galvanic contact. The device can operate as an encoder or decoder depending on the external circuitry connected to the data input. The code is made by the 8 input pins E1 to E8 by connecting them either to ground (LOW) or to the positive supply (HIGH), or leaving them floating (∞). This allows 3^8 combinations.

Encoding

In encoding mode the data input is connected to V_P. The encoded signal (programmed code plus recognition code) appears at the output S. After every start the encoder completes three coding runs then stops automatically.

Decoding

In decoding mode the data input is open for data from the encoder. If the input data is recognized, the data input of the decoder is temporarily closed (disregarding immediately following data) and the output is activated for a predetermined time.
If the input data is not recognized, the output is not activated and after the third coding run is completed the data input of the decoder is temporarily closed.

Output

The output is an open-collector configuration (npn), which is active LOW. It can handle a higher supply voltage than V_P (i.e. 16 V max.).

Coding input (recognition code)

Pin 4 must either be at ground level or at a maximum level of 0.3 V.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 14)	V_P	–	7	V
Supply current (pin 14)	I_P	0	50	mA
Input voltage (pins 2 and 5 to 12)	V_I	−0.3	V_P + 0.3	V
Voltage at output (pin 3)	V_O	−0.3	16	V
Total power dissipation	P_{tot}	–	500	mW
Storage temperature range	T_{stg}	−50	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 125 K/W

CHARACTERISTICS

T_{amb} = 25 °C; voltages with respect to pin 1; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 14)		V_P	3	4.5	6.5	V
Supply current	V_P = 4.5 V	I_P	1.8	2.5	3.2	mA
Zener diode voltage across supply	note 1	V_Z	–	–	8	V
Inputs E1 to E8						
Input voltage HIGH		V_{IH}	V_P –0.3	–	–	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input voltage floating		V_{IFL}	1	–	V_P –1	V
Input current HIGH		I_{IH}	2	7	12	μA
Input current LOW		I_{IL}	–4	–9	–15	μA
Input current floating		I_{IFL}	–	–	2	μA
Data input						
Input voltage						
for encoding mode		V_{de}	V_P –0.6	V_P	V_P +0.3	V
for decoding mode HIGH		V_{ddH}	0.8	–	0.5 V_P	V
for decoding mode LOW		V_{ddL}	–	–	0.5	V
Input current						
in encoding mode	$V_{13} = V_P$ = 4.5 V	I_{de}	8	16	25	μA
in decoding mode HIGH	V_{13} = 2 V; V_P = 4.5 V	I_{ddH}	–	–	2	μA
in decoding mode LOW	V_{13} = 0.3 V; V_P = 4.5 V	I_{ddL}	–8	–16	–25	μA
Minimum pulse width of DATA input signal		t_{dp}	2	–	–	μs
Output (pin 3)						
Output sink current	output active; V_P = 4.5 V	$I_{O(sink)}$	25	–	–	mA
Voltage at output		V_O	–	–	16	V
Recognition code (pin 4)						
Input voltage		V_I	–	–	0.3	V
Input current		I_I	–4	–9	–15	μA

Note to the supply characteristics

1. Maximum Zener diode current 10 mA.

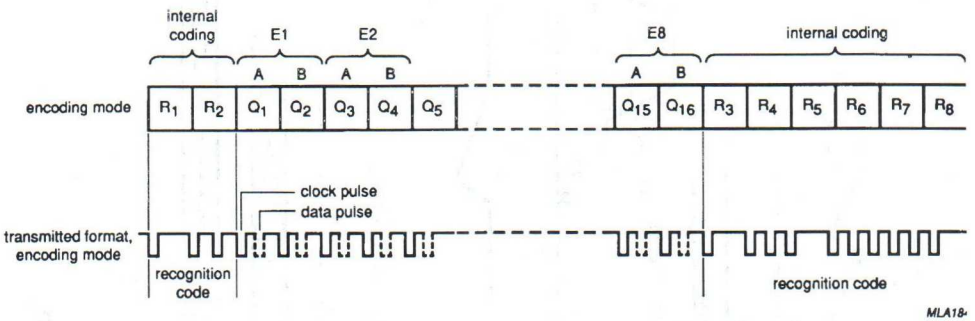
parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator characteristics	V_P = 4.5 V					
Switching voltage thresholds						
high level		V_{th}	3.10	3.32	3.50	V
low level		V_{tl}	0.65	0.71	0.90	V
Input current						
after switching high level		I_{th}	27	36	45	μA
after switching low level		I_{tl}	−6.7	−9	−11.3	μA
Ratio I_{th}/I_{tl}		ΔI_{osc}	3	4	5	
Duration of oscillator pulse						
in coding mode	note 1	τ_c	20	$0.4 \cdot C_{osc}$(pF)	–	μs
in decoding mode		τ_d	$3 \cdot \tau_c$	$0.4 \cdot C_{osc}$(pF)	$5 \cdot \tau_c$	μs
Oscillator capacitor						
in coding mode	notes 1 and 2	C_{osc}	56	–	–	pF
Duration of						
output active status		τ_o	–	$384 \cdot \tau_d$	–	
data input disabled status		τ_x	–	$576 \cdot \tau_d$	–	
Influence of temperature on duration of oscillator pulse		$\frac{\Delta\tau_c/\tau_c}{\Delta T}$	–	0.002	–	K^{-1}
Influence of supply voltage on duration of oscillator pulse		$\frac{\Delta\tau_c/\tau_c}{\Delta V_P}$	–	–	0.16	V^{-1}

Notes to the oscillator characteristics

1. Minimum value encoder – capacitor must provide minimum pulse width of DATA pulse τ_{dp} (= 0.2 τ_c).
2. Ratio encoder/decoder capacitor 1 : 4.

Code

The code consists of 24 bits. Each bit is represented by presence or absence of a data pulse following a clock pulse. The first 2 and last 6 bits form the recognition code. The intermediate 8 pairs of bits are determined by the connections of the input pins (E1 to E8). For the corresponding code in decoding mode the order of the input pins is reversed and connections "LOW" (L) and "floating" (∞) are interchanged.



encoding	E1		E2		E3 ----- E7		E8		∞		L		H		
decoding	E8		E7		E6 ----- E2		E1		L		∞		H		

E	A	B	Q_A	Q_B
L	1	0	0	1
∞	0	1	1	0
H	1	1	0	0

example

encoding E1 = L E2 = H E3 = ∞ E4 = H ----- E7 = L E8 = ∞

decoding E8 = ∞ E7 = H E6 = L E5 = H ----- E2 = ∞ E1 = L

Fig. 3 Coding diagram.

TIMING

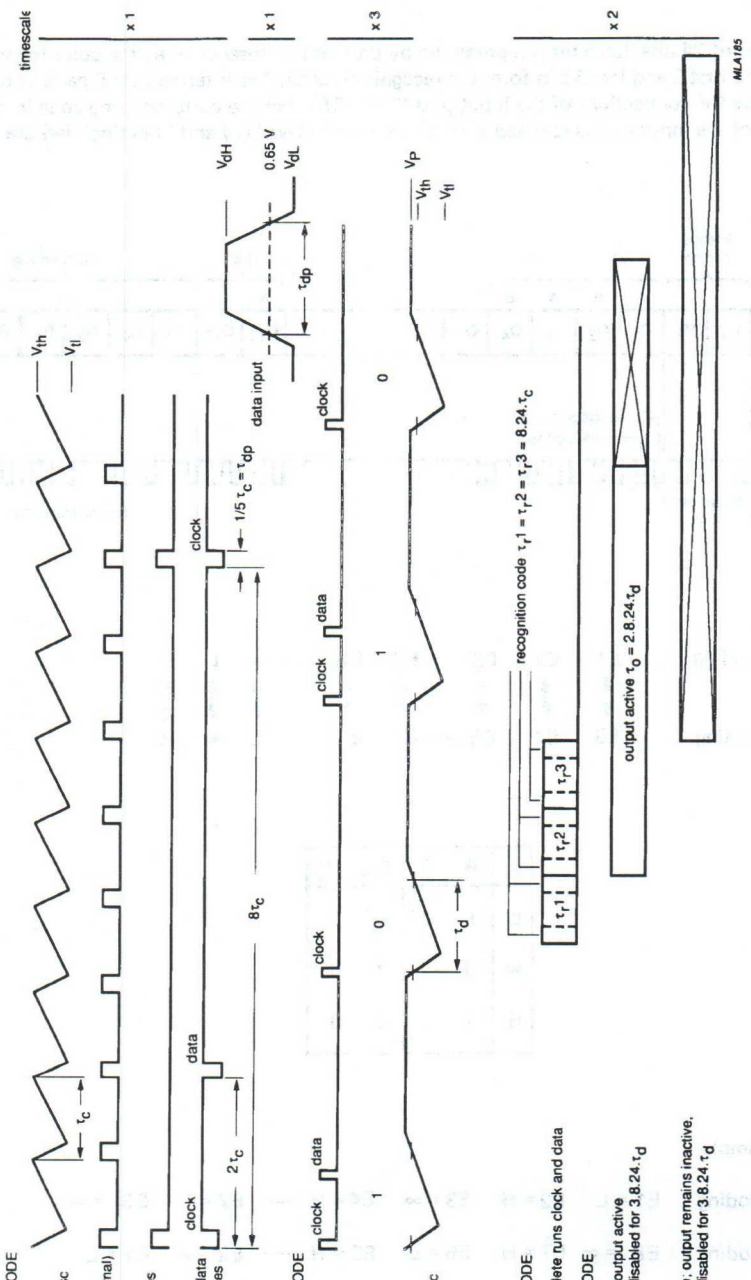
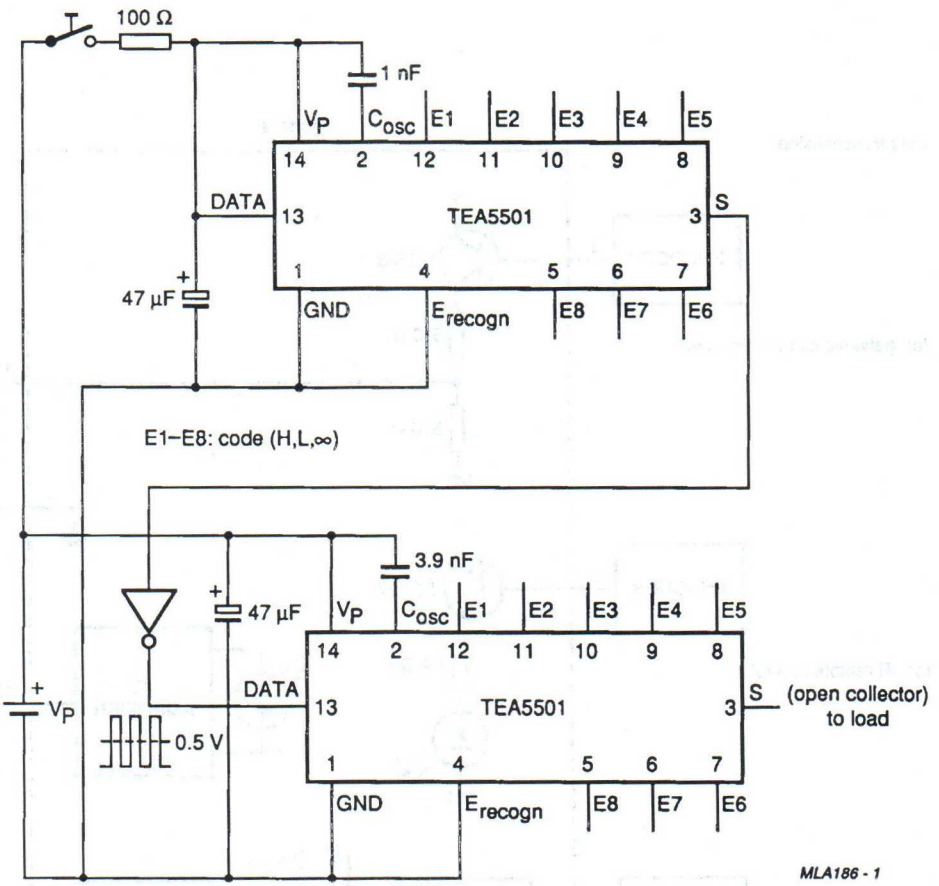


Fig.4 Timing diagram of TEA5501.

APPLICATION INFORMATION



E8 – E1: code (H, ∞, L).

Fig.5 Application diagram; data transmission via direct galvanic contact.

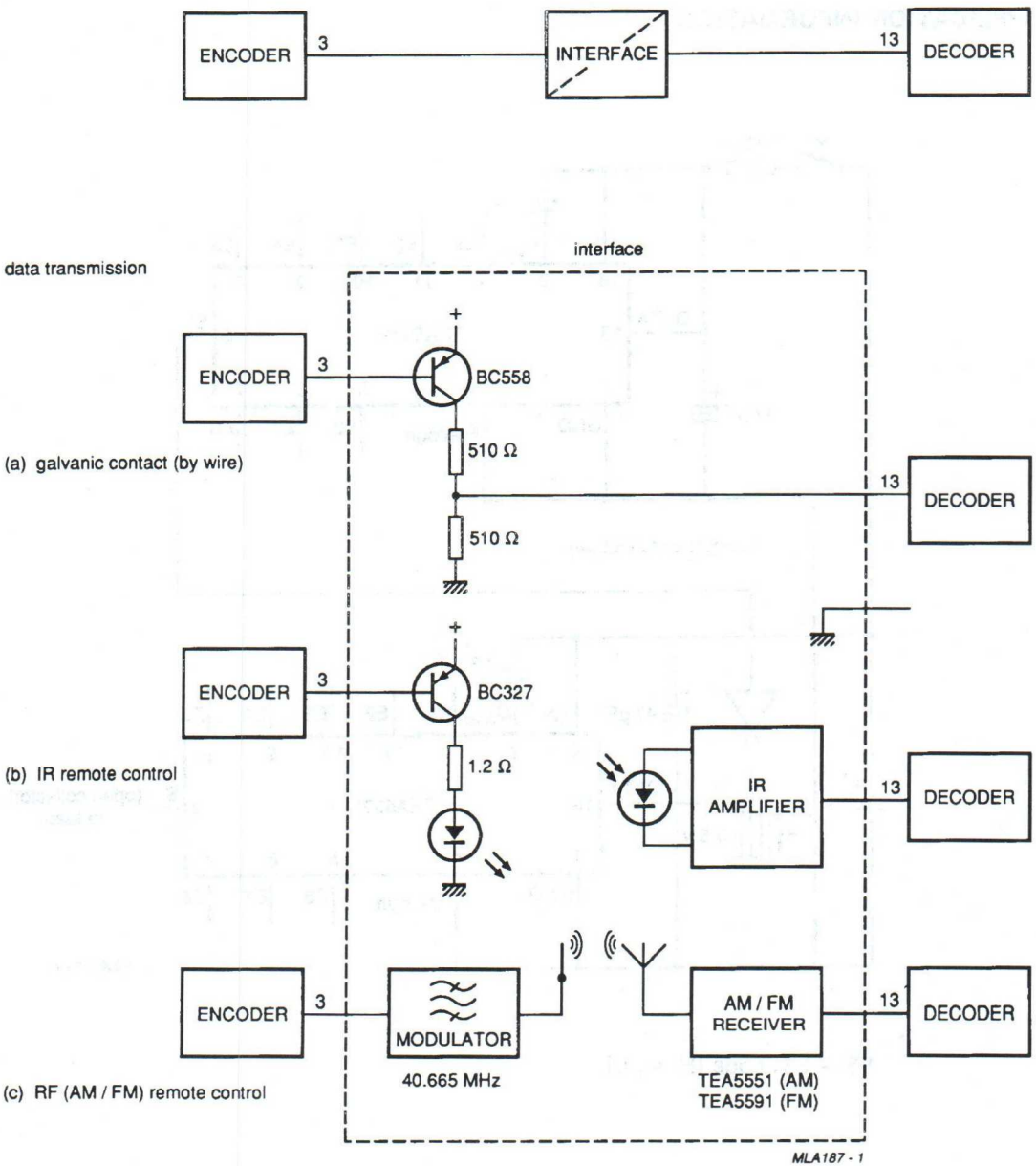


Fig.6 Application diagram; types of data transmission possible by using different interfaces.

Timer for NiCd and NiMH chargers — 74LV4799

FEATURES

- Wide supply voltage range of 0.9 V to 6 V allows 1 to 4-cell applications
- 10 V allowed on special inputs
- Supports virtually all battery chargers, including switched-mode power supplies
- On-chip timer calculates the actual capacity of the battery by measuring the charge time, discharge time and self-discharge time
- Automatic switch-over to trickle charge after completion of the charge time
- Can be adjusted for use with different types of batteries:
  - Charge time: 4 to 16 hours
  - Discharge time: 15 minutes to 4.7 hours
  - Self-discharge time: 50 to 100 days
- Battery status indication included:
  - $\overline{\text{LED}}$ output for charging/full indication
  - $\overline{\text{MOLLI}}$ output for battery-low indication
- LED mode select allows two different methods of indication
- Automatic power-ON reset
- Low power consumption
- Requires only a few peripheral components
- Very accurate on-chip oscillator
- Scan test facilities included
- I_{CC} category: non-standard.

APPLICATIONS

- Time-controlled NiCd and NiMH low-current chargers
- Domestic appliances such as rechargeable battery shavers, electric toothbrushes etc.
- Portable equipment such as notebook PCs, laptop PCs, camera flash units etc.
- Personal communications like cordless telephones, personal mobile radios, pagers etc.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage		0.9	–	6.0	V
I_{CC}	operating supply current	V_{CC} = 3.3 V; self-discharge mode; R_S = 100 kΩ; C_1 = 220 nF	–	36	–	μA
Δf	oscillator frequency tolerance	V_{CC} = 1 to 6 V	–	–	7	%

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4799N	16	DIL16	plastic	SOT38Z
74LV4799D	16	SO16	plastic	SOT109A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{LED}}$	LED driver output pin (active LOW)
2	EN	enable output (active HIGH)
3	$\overline{\text{EN}}$	enable output (active LOW)
4	V_{in}	external supply input
5	PWRS	power sense input
6	$\overline{\text{MOLLI}}$/SCO	more-or-less-low-indication output (active LOW)/scan test output
7	SEL	LED mode select input
8	GND	ground (0 V)
9	$\overline{\text{DIS}}$	discharge input (active LOW)
10	R_C	external resistor pin 3-state oscillator output (charge)
11	R_D	external resistor pin 3-state oscillator output (discharge)
12	R_S	external resistor pin 3-state oscillator output (self-discharge)
13	I_{OSC}	oscillator input
14	SCAN	scan test mode select input (active HIGH)
15	SCI	scan test input
16	V_{CC}	positive supply voltage

Timer for NiCd and NiMH chargers

74LV4799

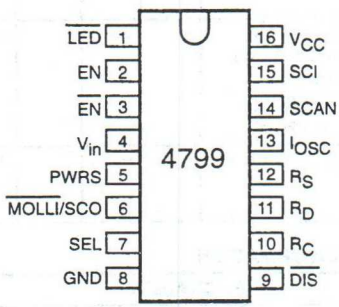


Fig.1 Pin configuration.

GENERAL DESCRIPTION

The 74LV4799 is a low-voltage Si-gate CMOS control IC for battery management. It consists of:

- 17-stage divider
- 10-stage up/down counter
- Control logic
- Integrated precision oscillator (using external timing components)
- Automatic power-ON reset
- Scan test facilities
- Battery charging/full indication output ($\overline{LED}$)
- Battery-low indication output ($\overline{MOLLI}$)
- Open-drain-N outputs for driving the load transistor.

Battery management with the 74LV4799 is based on the principle of time measurement. It measures the charge time, discharge time and self-discharge time by means of a very accurate on-chip oscillator, a divider and an up/down counter.

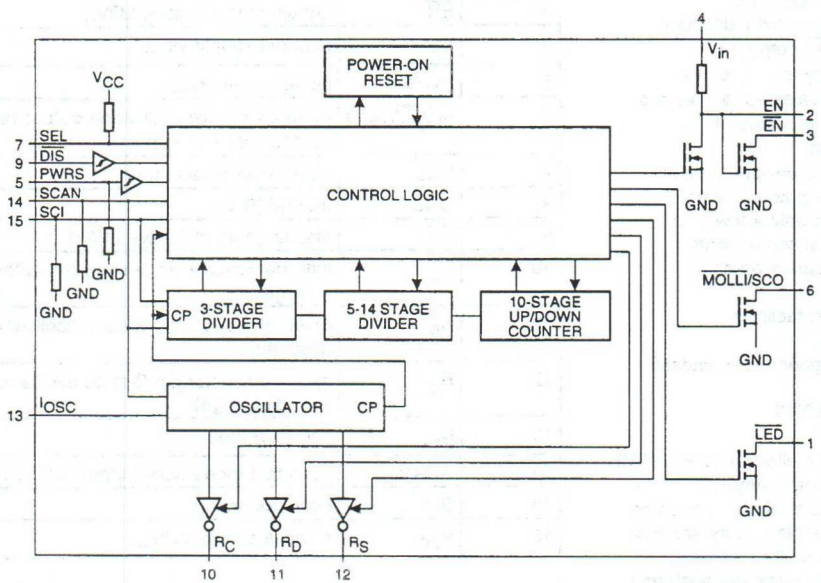


Fig.2 Functional diagram.

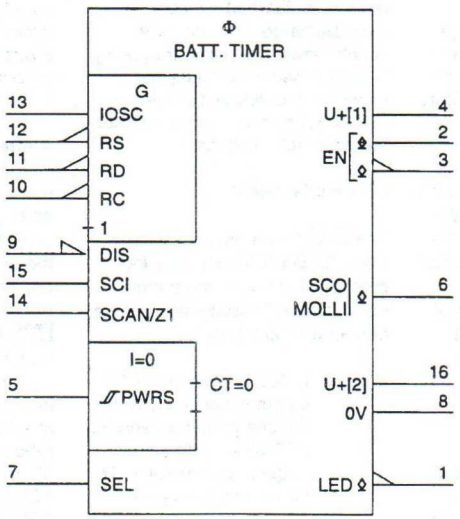


Fig.3 IEC Logic symbol.

Power On Reset.

An automatic Power On Reset initiates the IC when the battery is discharged and power is connected to the circuit. The initial condition is the charge mode in which the counter is reset and counts from zero up to maximum. At start up, the battery therefore always receives a full charge cycle. When a partially charged battery is inserted, it may be over-charged during the first cycle. To guard against this, simply replace the resistor at the R_C pin with an NTC type which is in good thermal contact with the battery. If the temperature of the battery increases, the frequency of the oscillator also increases to quickly reach a counter full indication and switch-over to trickle charge. With a battery that is almost completely discharged, the POR input can also be activated during discharge or self-discharge. The counter will then be reset to zero. This is a correct action while returning to the initial condition.

Power-on sensing.

Because this IC supports virtually all battery chargers, the PWRS input has a broad input frequency spectrum (active HIGH to 100 kHz). A pull-down circuit at the PWRS input allows detection of the open state which corresponds to an inactive charger. A HIGH level on the PWRS input, or an AC signal up to 100 kHz, enables the charge mode.

Start-up with low battery voltage.

Good start-up, even with an un-charged battery, is assured by using the V_{IN} input. The voltage on the V_{IN} input biases the external bipolar transistors at the EN or $\overline{EN}$ output, even if the IC is not yet functioning. After the battery has received sufficient charge, the internal control logic takes over control of the EN and $\overline{EN}$ outputs.

Charge mode.

This mode is selected when PWRS is active (HIGH or pulsed) and the discharge input $\overline{DIS}$ is HIGH. The EN output is HIGH, and the $\overline{EN}$ output is LOW initiating continuous charge of the battery. The counter then counts from the zero state up to the maximum value. The clock frequency is determined by the external capacitor and resistor connected to the R_C output. The counter stops when it reaches its maximum value and the EN and $\overline{EN}$ outputs switch over from the continuous charge to the trickle charge mode.

Trickle charge mode.

At the maximum counter value, it is assumed that the battery is fully charged. The counter stops and remains on this maximum value.

The EN and $\overline{EN}$ outputs switch-over from the continues charge to the trickle charge mode. In the trickle charge mode, the average charge current is reduced to only compensate the self-discharge of the battery by using dedicated duty cycle control. The control is dedicated because it adjusts the duty cycle in inverse proportion to the load current, resulting in a fixed charger current irrespective of the kind of charger (e.g. 4-hour or 16-hour charger). In the trickle charge mode, the oscillator circuitry alternately generates 4 periods of the R_C-C1 time-constant, and 3 periods of the R_S-C1 time-constant. See Fig.4.

Discharge mode.

The discharge input ($\overline{DIS}$) is used to detect the discharge of the battery. If $\overline{DIS}$ is LOW, the counter counts down. The clock frequency is determined by the external capacitor and resistor at the R_D output. If PWRS is inactive (LOW or open), the EN output is LOW, and the $\overline{EN}$ output is in the high impedance OFF-state (no charge of the battery). This is called the discharge mode. If PWRS is active, the circuit is in the charge/discharge mode.

Charge/Discharge mode.

If $\overline{DIS}$ is LOW and PWRS is active (HIGH or pulsed), the circuit is in the charge/discharge mode. The counter counts down. The clock frequency is determined by the external capacitor and resistor tied at the R_D output. The EN output is HIGH, and the $\overline{EN}$ output is LOW initiating continuous charge of the battery. The battery is therefore charged and discharged at the same instant, thereby maintaining a better load condition of the battery.

Self-discharge mode.

If $\overline{DIS}$ is HIGH and PWRS is inactive (LOW or open), the battery is being neither charged nor discharged. The circuit is in the self-discharge mode. This mode represents the battery leakage (self-discharge). The counter counts down. The clock frequency is determined by the external capacitor and resistor at the R_S output. When the counter reaches the zero state, it stops.

LED mode select.

The $\overline{LED}$ output drives a battery status LED which indicates the charge/full status of the battery. For optimum flexibility, two modes of operation are built-in.

Mode 1: If SEL is LOW, the $\overline{LED}$ output is active LOW in the charge mode, and the LED blinks with a frequency of about 1 Hz during trickle charge.

Mode 2: If SEL is HIGH or open, the $\overline{LED}$ output blinks with a frequency of about 0.25 Hz in the charge mode, and is active LOW during trickle charge. In the discharge or self-discharge mode, the $\overline{LED}$ output is open except when PWRS is active (HIGH or pulsed). Then, the battery is charging and discharging simultaneously. Although the discharge mode is dominant, the $\overline{LED}$ output is active when PWRS is also active.

Note: The blink frequency depends on the oscillator frequency. (See application information)

Low indication.

As part of the user interface, the $\overline{MOLLI}$ output shows when the battery needs to be charged. $\overline{MOLLI}$ stands for More Or Less Low Indication (active LOW). The function is as follows: In the discharge mode, ($\overline{DIS}$ is active LOW), the counter counts down and, when it reaches the zero state, it stops. If $\overline{DIS}$ is switched HIGH, the $\overline{MOLLI}$ output gives an output signal of four periods of about one second, with a 50% duty cycle. This can be used to activate a buzzer. The $\overline{MOLLI}$ output signal of four periods will be interrupted as soon as PWRS is activated.

Alarm indication

If an almost completely discharged battery is connected to the charger, it may not be noticed by the user if the load switch is still on. To prevent damaging the battery, an alarm signal on the $\overline{LED}$ output will alert the user to switch off the load. The alarm signal is easily recognised, because the $\overline{LED}$ output will blink at a higher frequency than normal (about 5 Hz instead of 1 Hz). This alarm indication is only active if the SEL input is HIGH or open. If the SEL input is LOW, no alarm indication is present, because in many applications simultaneous charging and discharging is quite acceptable (See charge/discharge mode).

Scan test mode.

If the SCAN input (pin 14) is made active HIGH, the circuit is in the test mode. The tester clock is connected to the I_{OSC} pin (pin 13). In the scan mode, the on-chip oscillator is bypassed to allow rapid testing of the divider/counter. The scan test patterns are available on request. The scan test data is entered serially through the SCI input (pin 15). The scan out data is present on the $\overline{MOLLI}$/SCO output (pin 6), which then acts as a scan output.

Remaining energy indication.

The scan test facility can be used as a remaining energy indication because the value of the counter can be read out at the scan output ($\overline{MOLLI}$/SCO). This is done by briefly interrupting the normal mode of operation, putting the circuit in the scan mode, and reading out the counter value. The

circuit then reverts to the normal mode. This only works correctly with the $\overline{\text{MOLLI}}$/SCO output and SCI input linked (round coupled loop) and with exactly 49 clock pulses applied to the I_{OSC} input.

The serial scan-out data is available on the $\overline{\text{MOLLI}}$/SCO output. The value of the counter can be decoded by reading the correct bits. Details are given in the Chapter "Application information".

Output drivers EN and $\overline{\text{EN}}$.

In one-cell battery (low-voltage) applications, the drive from the ENABLE output ($\overline{\text{EN}}$) is insufficient to provide the base current directly for the external bipolar PNP regulator transistor. The inverse signal has therefore been made available at the ENABLE output (EN) to drive an extra bipolar NPN transistor that can provide the base current for the bipolar PNP regulator transistor as shown in Fig.5.

FUNCTION TABLE 1

OPERATING MODES	INPUTS			OUTPUTS					DIVIDER/COUNTER	
	PWRS	V_{IN}	$\overline{\text{DIS}}$	EN	$\overline{\text{EN}}$	R_C	R_D	R_S	MODE	VALUE
charge	H or ⎍	H	H	H	L	⎍	Z	Z	count up 22 sections	< max
trickle charge	H or ⎍	H	H	⎍	⩛	⎍	Z	⎍	stop	max
charge/discharge	H or ⎍	H	L	H	L	Z	⎍	Z	count down 18 sections	≥ min
discharge	L or open	X	L	L	Z	Z	⎍	Z	count down 18 sections	≥ min
self-discharge	L or open	X	H	L	Z	Z	Z	⎍	count down 27 sections	≥ min

FUNCTION TABLE 2

STATUS INDICATION	INPUTS			OUTPUTS		COUNTER	
	PWRS	$\overline{\text{DIS}}$	SEL[1]	$\overline{\text{LED}}$	$\overline{\text{MOLLI}}$	MODE	VALUE
charge	H or ⎍ H or ⎍	H H	L H or open	L ⩛	Z Z	count up count up	< max < max
charge/discharge	H or ⎍	L	L	L	Z	count down	≥ min
trickle charge	H or ⎍ H or	H H	L H or open	⩛ L	Z Z	stop stop	max max
discharge	L or open	L	X	Z	Z	count down	> min
self-discharge	L or open	H	X	Z	Z	count down	> min
low	L or open	↑	X	Z	⊔	stop	min
low	↑	↑	X	Z	Z[2]	count up	≥ min
alarm	H or	L	H or open	⩛	Z	count down	≥ min

Notes

1. Don't change SEL during operation.
2. The $\overline{\text{MOLLI}}$ function will be interrupted as soon as PWRS is activated.

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state
X = don't care
⎍ = pulsed (H/L)
⩛ = pulsed (Z/L)
⊔ = 4 periods of about one second (Z/L)
↑ = LOW-to-HIGH level transition

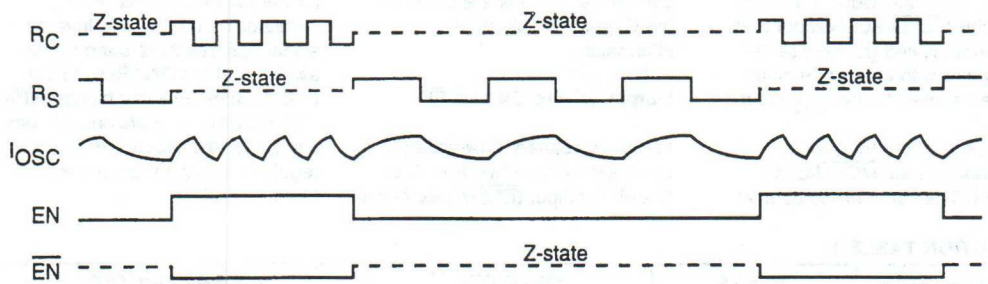


Fig.4 Operation in the trickle charge mode. The duration of the R_C cycle determines the duty cycle of the enable outputs (EN and $\overline{EN}$), allowing a dedicated control. The average trickle charge current will compensate for the self-discharge, independent of the charge current.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	0.9	1.2	6.0	V	
V_I	input voltage pins 4, 5 and 9	0	–	10	V	see note 1
	input voltage pins 7, 13, 14 and 15	0	–	V_{CC}	V	
V_O	output voltage pins 10, 11 and 12	0	–	V_{CC}	V	
	output voltage pins 1, 2, 3 and 6	0	–	10	V	
T_{amb}	operating ambient temperature range in free air	0	–	+70	°C	
t_r, t_f	input rise and fall times pin 5	–	–	10	ms	
	input rise and fall times pins 7, 14 and 15	– – – –	– – – –	4000 1000 500 400	ns ns ns ns	V_{CC} = 1.0 V; V_I = 1.0 V V_{CC} = 2.0 V; V_I = 2.0 V V_{CC} = 3.0 V; V_I = 4.5 V V_{CC} = 6.0 V; V_I = 6.0 V
	input rise and fall times pin 9	–	–	2	µs	

Note

1. Single sided input protection applied on Pins 4, 5 and 9.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7.0	V	
I_{IK}	DC input diode current pins 4, 5 and 9	–	±20	mA	$V_I < -0.5$ or $V_I > 12$ V
	DC input diode current pins 7, 13, 14 and 15	–	±20	mA	$V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V
I_{IK}	NON repetitive peak DC input diode current pin 9	–	10	mA	$V_I > 10$ V and $t < 10$ µs; see note 1
V_I	DC input voltage range pins 4,5 and 9	−0.5	+12	V	
	DC input voltage range pins 7, 13, 14 and 15	−0.5	$V_{CC} + 0.5$	V	
I_{OK}	DC output diode current pins 1, 2, 3 and 6	–	−20	mA	$V_O < -0.5$ V
I_O	DC output sink current pins 1, 2, 3 and 6	–	−25	mA	$V_O > 0$ V
I_{OK}	DC output diode current pins 10, 11 and 12	–	±20	mA	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
I_O	DC output sink or source current pins 10, 11 and 12	–	±25	mA	-0.5 V $< V_O < V_{CC} + 0.5$ V
I_{GND}, I_{CC}	DC GND or V_{CC} current	–	±50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C
	plastic DIL	–	750	mW	above + 70 °C derate linearly with 12 mW/K
	plastic mini-pack (SO)	–	500	mW	above + 70 °C derate linearly with 8 mW/K

Notes

1. In applications where a motor is present, the input voltage may exceed the maximum V_I level of 10 V at the $\overline{DIS}$ input for a very short period when the motor is switched off.
2. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions.
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS		
		+25			0 to +70			V_{CC} (V)	V_I	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.				
V_{IH}	HIGH level input voltage	0.8 3.6 4.8	0.5 2.4 3.2	– – –	0.8 3.6 4.8	– – –	V V V	1.0 4.5 6.0		
V_{IL}	LOW level input voltage	– – –	0.5 2.1 2.8	0.2 0.9 1.2	– – –	0.2 0.9 1.2	V V V	1.0 4.5 6.0		
V_{OH}	HIGH level output voltage; R_C, R_D outputs	0.90 5.73	0.96 5.84	– –	0.89 5.66	– –	V V	1.0 6.0	V_{IH} or V_{IL}	I_O = –190 µA I_O = –6.1 mA
V_{OH}	HIGH level output voltage; R_S output	0.90 5.73	0.96 5.84	– –	0.89 5.66	– –	V V	1.0 6.0	V_{IH} or V_{IL}	I_O = –24 µA I_O = –760 µA
V_{OL}	LOW level output voltage; R_C, R_D outputs	– –	0.04 0.16	0.10 0.26	– –	0.11 0.33	V V	1.0 6.0	V_{IH} or V_{IL}	I_O = 190 µA I_O = 6.1 mA
V_{OL}	LOW level output voltage; R_S output	– –	0.04 0.16	0.10 0.26	– –	0.11 0.33	V V	1.0 6.0	V_{IH} or V_{IL}	I_O = 24 µA I_O = 760 µA
V_{OL}	LOW level output voltage; $\overline{MOLLI}$, $\overline{LED}$ outputs	– –	0.04 0.17	0.10 0.26	– –	0.11 0.33	V V	1.0 6.0	V_{IH} or V_{IL}	I_O = 220 µA I_O = 7.4 mA
V_{OL}	LOW level output voltage; EN output	– –	0.04 0.17	0.10 0.26	– –	0.11 0.33	V V	1.0 6.0	V_{IH} or V_{IL}	I_O = 360 µA; pin 4 open I_O = 13.0 mA; pin 4 open
V_{OL}	LOW level output voltage; EN output	–	0.12	0.35	–	0.40	V V	1.3	V_{IH} or V_{IL}	pin 4 = 10 V; see note 1
V_{OL}	LOW level output voltage; $\overline{EN}$ output	– –	0.04 0.17	0.10 0.26	– –	0.11 0.33	V V	1.0 6.0	V_{IH} or V_{IL}	I_O = 140 µA; pin 4 HIGH I_O = 5.0 mA; pin 4 HIGH
V_{CC}	POR level active inactive	0.25 –	– –	0.65 0.9	– –	– –	V V			

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS		
		+25			0 to +70			V_{CC} (V)	V_I	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.				
I_{CC}	quiescent supply current	–	34	50	–	400	µA	6.0	V_{CC} or GND	pins 5, 14 and 15 at GND; pins 7 and 9 at V_{CC}; see note 2
I_I	input leakage current pins 4 and 9	–	–	500	–	–	nA	1.0	10 V	
I_I	input leakage current pins 14 and 15	–	–	100	–	–	nA	6.0	V_{CC} or GND	
I_I	pull-up current pin 7	–0.5 –0.5	–2.4 –2.4	–10 –10	– –	– –	µA µA	1.0 6.0	GND	
I_I	pull-down current pin 5	0.5 0.5	2.4 2.4	10 10	– –	– –	µA µA	1.0 6.0	V_{CC}	
I_{OZH}	OFF-state current pins 1, 3 and 6	–	–	500	–	–	nA	6.0	V_{IH} or V_{IL}	V_o = 10V
I_{OZH}	OFF-state current pin 2	–	–	100	–	–	nA	6.0		V_o = 6V V_{in} = open
I_{OZH}	OFF-state current pin 3	–	–	100	–	–	nA	6.0	V_{IH} or V_{IL}	V_o = 6V
I_{OZ}	OFF-state current pins 10, 11 and 12	–	–	±100	–	–	nA	6.0	V_{IH} or V_{IL}	V_o = V_{CC} or GND

Notes to the DC characteristics

1. This item guarantees that an external bipolar NPN-transistor can be switched off by the EN output.
2. Oscillator disabled. This can be done by I_{OSC} = HIGH or LOW.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		+25			0 to +70			V_{CC} (V)	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.			
Δf	oscillator frequency spread	−11 −9	−4 −2	+3 +5	– –	– –	% %	1.0 6.0	any resistor or capacitor according to the application information; see note 1
δ_{LED}	duty factor at pin 1	– –	50 50	– –	– –	– –	% %	1.0 6.0	see note 2
δ_{MOLLI}	duty factor at pin 6	– –	50 50	– –	– –	– –	% %	1.0 6.0	see note 3
t_{deb}	debounce suppression at pin 9	– –	67 65	– –	– –	– –	ms ms	1.0 6.0	
$f_{i(max)}$	maximum frequency at power sense input	100 100	– –	– –	– –	– –	kHz kHz	1.0 6.0	
$f_{i(min)}$	minimum frequency at power sense input	– –	– –	50 50	– –	– –	Hz Hz	1.0 6.0	

Notes

1. The oscillator frequency can be calculated by: $f = \frac{0.36}{R \times C1}$
2. During blinking.
3. An output signal of four periods will appear in case of discharged batteries and $\overline{DIS}$ is switched HIGH.

APPLICATION INFORMATION

Oscillator.

The frequency will be determined by the external components R_C, R_D, R_S and C1. The frequencies can be calculated by the following expressions: $f_C = \frac{0.36}{R_C \times C1}$; $f_D = \frac{0.36}{R_D \times C1}$; $f_S = \frac{0.36}{R_S \times C1}$.

R_C and C1 determine the charge time.
R_D and C1 determine the discharge time.
R_S and C1 determine the self-discharge time.

The charge, discharge and self-discharge times can be calculated as follows:

Charge time = $\frac{2^{22}}{f_C}$; Discharge time = $\frac{2^{18}}{f_D}$; Self-discharge time = $\frac{2^{27}}{f_S}$.

In the trickle charge mode the average charge current will be reduced by a factor: $\frac{1}{1 + \frac{3 \times R_S}{4 \times R_C}}$

External components range

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS		
		+25				V_{CC} (V)	V_I	OTHER
		MIN.	TYP.	MAX.				
R_C/R_D	resistor range	5.360	–	100	kΩ	1.0	–	C1 = 0.22 µF
		1.150	–	100	kΩ	2.0	–	
		0.562	–	100	kΩ	4.5	–	
		0.511	–	100	kΩ	6.0	–	
R_S	resistor range	42.20	–	825	kΩ	1.0	–	C1 = 0.22 µF
		9.09	–	825	kΩ	2.0	–	
		4.22	–	825	kΩ	4.5	–	
		3.32	–	825	kΩ	6.0	–	
C1	capacitor range	–	–	no limit	pF	1.0	–	
		–	–	no limit	pF	2.0	–	
		–	–	no limit	pF	4.5	–	
		–	–	no limit	pF	6.0	–	

Charge-discharge times

PARAMETER	TIME RANGE	CONDITIONS
Charge time	4 hours to 16 hours	Components ranges are within the values given in Section "External components range"
Discharge time	15 minutes to 4.7 hours	
Self-discharge time	50 days to 100 days	

LED frequency

The frequency of the $\overline{LED}$ output (pin 1) is determined by the oscillator frequency. Three modes of operation, each with its own frequency, are possible.

Mode	SEL	$\overline{LED}$ frequency
charge	H or open	$\frac{f_C}{256}$
trickle charge	L	$\frac{1}{\frac{8}{f_C} + \frac{6}{f_S}}$
alarm	H	$\frac{f_D}{32}$

$\overline{\text{MOLLI}}$ pulse duration

The $\overline{\text{MOLLI}}$ output gives an output signal of four periods with a 50% duty cycle.
The duration of one period is determined by: $16/f_s$

Timing accuracy.

The timing accuracy depends on the accuracy of the on-chip oscillator and on the external R and C components. The inaccuracy of the on-chip oscillator is specified as maximum ±7%. In most cases the actual inaccuracy will be significantly lower. This depends on the supply voltage as well as the value of the external components.

Influence of Resistor value.

Low resistor values cause some spread because the RC combination is biased by a 3-state push-pull output. The spread of the R_{on} of the push-pull stage will contribute to the frequency spread. When high-value resistors are used, any possible output leakage of the not-selected 3-state outputs will cause a frequency deviation. For these reasons, the resistor values must be within the specified ranges.

Influence of supply voltage

The trip levels of the oscillator are fixed at 20% and 80% of V_{CC}. At higher supply voltages the spread of the trip levels decreases in greater proportion because the offset voltage remains constant, and the propagation delay decreases. Furthermore, the R_{ON} values of the push-pull driving stage decrease at higher voltages.

Spread-causing factors

SYMBOL	PARAMETER	T_{amb} = 25 °C			UNIT	V_{CC} (V)
		MIN.	TYP.	MAX.		
V_{off}	offset voltage	–	7	–	mV	1.0
		–	7	–	mV	6.0
t_P	propagation delay	–	22	–	µs	1.0
		–	5.5	–	µs	6.0
R_{ON}	P-channel resistance R_C, R_D outputs	–	170	–	Ω	1.0
		–	25	–	Ω	6.0
R_{ON}	N-channel resistance R_C, R_D outputs	–	250	–	Ω	1.0
		–	35	–	Ω	6.0
R_{ON}	P-channel resistance R_S output	–	1300	–	Ω	1.0
		–	180	–	Ω	6.0
R_{ON}	N-channel resistance R_S output	–	1300	–	Ω	1.0
		–	180	–	Ω	6.0

Error free operation, even under extreme conditions.

Several measures are taken in the circuit design to ensure error-free operation, even with very low supply voltages. Moreover, the circuit has been made very insensitive to the effects of external fields. The measures taken during the design are:

- Use of synchronous logic
- Bistable POR instead of monostable POR
- Data retention assured below a supply voltage of 0.9 V.
- Debounce circuitry on $\overline{\text{DIS}}$ input (maximum expected debounce time = 10 ms)
- Schmitt trigger on PWRS (power sense) input and on $\overline{\text{DIS}}$ input
- Special oscillator security to prevent any malfunction.

Synchronous logic and bistable POR.

Use of synchronous logic results in much lower sensitivity to spikes on input pins. The POR is adapted to fit well into a synchronous environment. An increasing supply voltage sets the POR. The POR output signal is routed to the control logic and divider/counter. It is synchronized with the on-chip clock. After all flip-flops are reset, a reset acknowledge signal is generated which resets the POR. This method ensures that the POR signal is acknowledged in all cases, even at very low voltages.

Data retention.

The circuit may be used in an application where an electric motor is present. When the motor is switched on, it will disturb the supply voltage for a short period. The POR level is set at such a level that, even with very low supply voltages, the POR will not respond during motor switch on. The flip-flops will retain their data during the supply voltage disturbance because of the inherent data retention of any CMOS gate. However, when the battery is almost completely discharged and the motor switch is activated, the dip on the supply voltage line can be too large. The retention of the POR is therefore made deliberately worse than that of the internal flip-flops. The POR will therefore respond long before the flip-flops will loose their data. This results in a proper start condition for a new charge cycle.

Debounce circuitry on $\overline{DIS}$ input.

A discharge cycle is activated by a switch. To protect the circuit from any bounce of the switch contacts, de-bounce circuitry is provided at the $\overline{DIS}$ input. The circuitry allows a switch de-bounce time of max. 10 ms.

Schmitt trigger on PWRS (power sense) input.

The PWRS input can be corrupted by high transients due to disturbances on the mains supply. To suppress any false triggering, the PWRS input is provided with a Schmitt-trigger. However, for some applications, it is advisable to connect a low-value capacitor (150 pF min.) between the PWRS input and GND.

Special oscillator security to prevent any malfunction.

The excellent performance of the oscillator is achieved by using linear op-amp techniques. The oscillator consists of an internal reference, two comparators and a latch. Care was taken to design a very reliable oscillator even with a supply voltage below 0.9 V. If one of the comparators ceases to operate with a supply voltage below 0.9 V, the latch will not be corrupted. Priority was given to stop the oscillator rather than allow uncontrolled oscillation.

All these measures result in reliable 1-cell to 4-cell battery charge management.

Remaining energy indication:

The scan test facility can be used as a remaining energy indication because the value of the counter can be read-out at the scan output ($\overline{MOLLI}$/SCO). This is achieved by briefly interrupting the normal mode of operation, putting the circuit in the scan mode (pin 14 = HIGH), and reading-out of the counter value. The circuit is then returned to the normal mode (pin 14 = LOW or open).

Read-out procedure: The contents of the counter flip-flops can be read-out in the scan mode. To ensure that there is no disturbance of the circuit function, it is essential to either create a round coupled loop by linking the $\overline{MOLLI}$/SCO output (pin 6) directly to the SCI input (pin 15), or to shift-in the serial data of the scan line at the SCI input after completion of the read out cycle. 49 clock pulses are needed on the I_{OSC} input (pin 13) to shift-out the contents of the whole scan line. The most-significant bit of the counter will appear at the $\overline{MOLLI}$/SCO output after the last clock pulse. The least-significant bit after the penultimate clock pulse, etc. Selecting the last three or four bits will yield sufficiently high accuracy to obtain the counter value which represents the remaining energy of the battery.

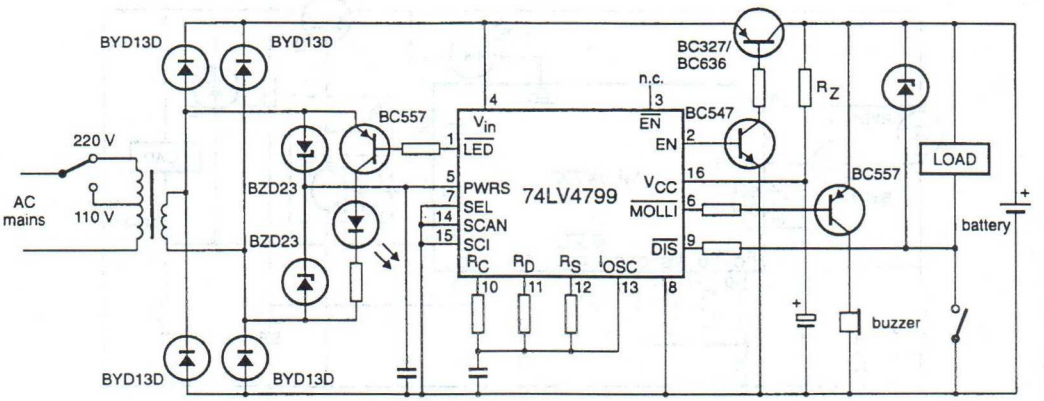


Fig.5 Typical application of the low-voltage 74LV4799.

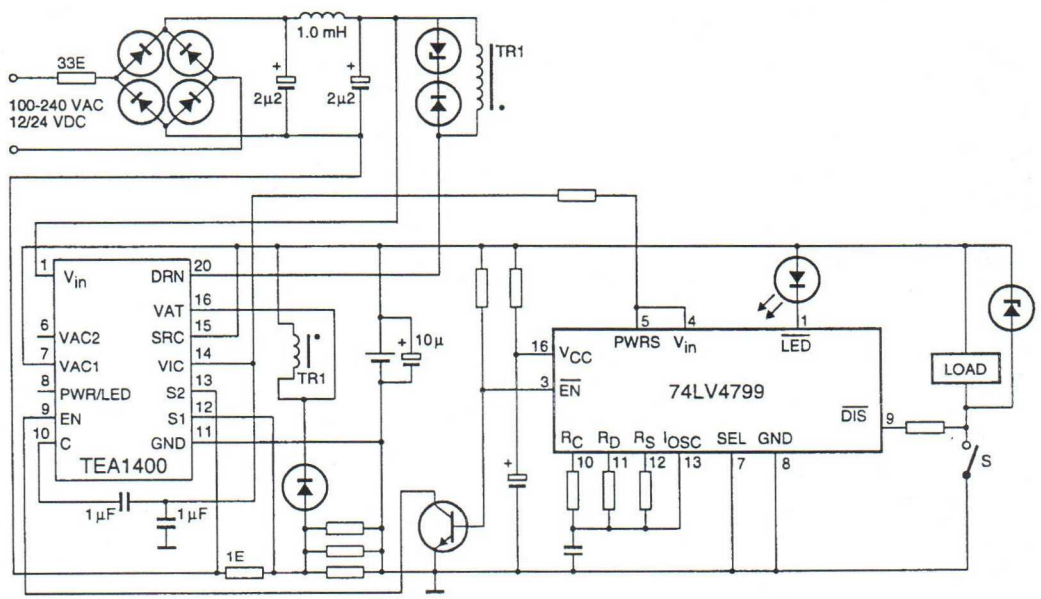


Fig.6 Application diagram of the 74LV4799 in combination with the high-voltage IC TEA1400.

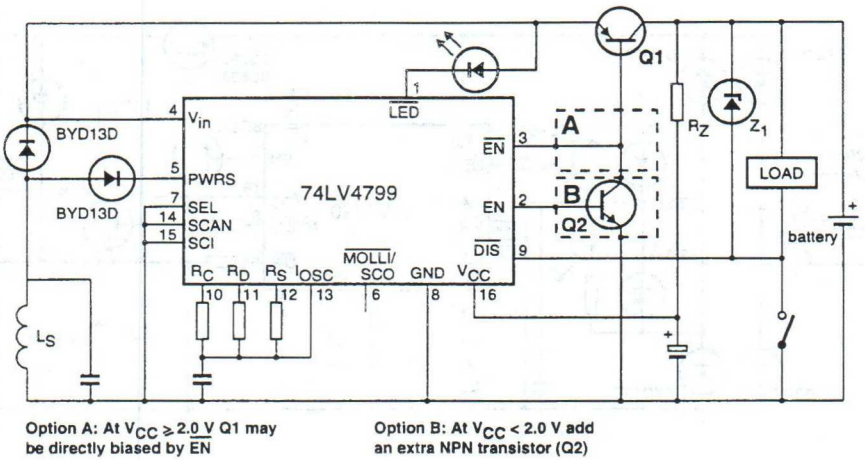


Fig.7 Inductive loader, showing the two options A and B.

Section 15
Switched-Mode Power Supply Circuits/Trigger Circuits

INDEX

AN120	An overview of switched-mode power supplies	1023
NE/SE5560	Switched-mode power supply control circuit	1028
NE/SE5561	Switched-mode power supply control circuit	1044
AN123	NE5561 applications	1049
AN124	External synchronization for the NE5561/5568	1054
NE/SE5562	Switched-mode power supply control circuit	1055
NE5568	Switched-mode power supply controller	1085
SG3524	SMPS control circuit	1087
AN126	Applications using the SG3524	1092
µA723/723C	Precision voltage regulator	1094
UC3842	Current-mode PWM controller	1100
TCA280B	General-purpose triggering circuit	1108
TDA8380	Control circuit for switched-mode power supplies	1120
TEA1039	Control circuit for switched-mode power supply	1137

An overview of switched-mode power supplies

AN120

Conceptually, three basic approaches exist for obtaining regulated DC voltage from an AC power source. These are:

- Shunt regulation
- Series linear regulation
- Series switched-mode regulation

All require AC power line rectification.

The series switched-mode regulators will be referred to as switched-mode power supplies or SMPS during the course of this article

Briefly stated, if all three types of regulation can perform the same function, the following are some of the key parameters to be addressed:

- From an economical point of view, cost of the system is paramount.
- From an operations point of view, weight of the system is critical.
- From a design criteria, system efficiency is the first order of business

The series and shunt regulators operate on the same principle of sensing the DC output voltage, comparing to an internal reference level and varying a resistor (active device) to maintain the output levels within pre-specified limits.

Switched-mode power supplies (SMPS) are basically DC-to-DC converters, operating at frequencies in the 20kHz and higher region. Basically, the SMPS is a power source which utilizes the energy stored during one portion of its operating cycle to supply power during the remaining segment of its operating cycle.

Linear regulators, both shunt and series, suffer when required to supply large currents with resultant high dissipation across the regulating device. Efficiency suffers tremendously. (Efficiencies less than 40% are typical.)

Switched-mode power supplies operate at much higher levels of efficiency (generally in the order of 75% to 80%), thereby reducing significantly the energy wasted in the regulated supply. The SMPS does, however, suffer significantly in the ripple regulation it is able to maintain, as opposed to a much higher degree of regulation available in series (or shunt) linear regulators.

The linear regulators obtain improved regulation by virtue of the series pass elements always conducting, as opposed to SMPS devices having their active devices operative only during a portion of the overall operating period.

Some definitions and comparisons between linear regulators and switched-mode power supplies follow for reference.

REGULATION

Line Regulation — (Sometimes referred to as static regulation) refers to the changes in the output (as a percent of nominal or actual value) as the input AC is varied slowly from its rated minimum value to its rated maximum value (e.g., from $105VAC_{RMS}$ to $125VAC_{RMS}$).

Load Regulation — (Sometimes referred to as dynamic regulation) refers to changes in output (as a percent of nominal or actual value) when the load conditions are suddenly changed (e.g., minimum load to full load.)

NOTES: The combination of static and dynamic regulation are cumulative care should be taken when referring to the regulation characteristics of a power supply

Thermal Regulation — Referred to as changes due to ambient variations or thermal drift.

TRANSIENT RESPONSE

The ability of the regulator to respond to rapid changes in either line variations, load variations, or intermittent transient input conditions. (This parameter is often referred to as "recovery time".)

AC PARAMETERS

Voltage Limiting — The regulator's ability to "shut down" in the event that the internal control elements fail to function properly.

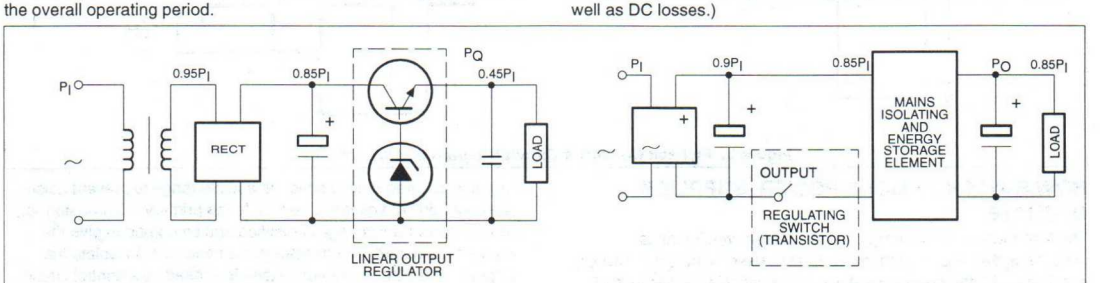
Current Limiting — Often referred to as "fold-back", where the amplifier segment of the regulator folds back the output current of the device when safe operating limits are exceeded.

Thermal Shutdown — The regulator's ability to shut itself down when the maximum die temperature is exceeded.

GENERAL PARAMETERS

Power Dissipation — The maximum power the regulator can tolerate and still maintain operation within the safe operating area of its active devices.

Efficiency — The ratio (in percent) of the usable versus total power being dissipated in a regulated supply. (The losses can be AC as well as DC losses.)



a. Conventional Supply — 45% Efficiency

a. Switched-Mode Supply — 80% Efficiency

Figure 1. Losses in Regulated Power Supplies

An overview of switched-mode power supplies

AN120

EMI/RFI — Generation of ElectroMagnetic/Radio Frequency Interference signals and magnetic field disturbance in SMPS devices. (Transformer and choke design are available which reduce both RFI & EMI to safe acceptance regions.)

The balance of this section will be dedicated to the discussion of the general operation of Switched-Mode Power Supplies (SMPS) with emphasis on the Philips Semiconductors NE5560 Control and Protection Module.

Switched-mode power supplies (SMPS) have gained much popularity in recent years because of the benefits they offer. They are now used on a large scale in desk calculators, computers, instrumentation, etc., and it is confidently expected that the market for this type of supply will grow.

The advantages of SMPS are low weight and small size, high efficiency, wide AC input voltage range, and low cost.

- Low weight and small size are possible because operation occurs at a frequency beyond the audible range; the inductive elements are small.
- High efficiency because, for output regulation, the power transistor is switched rapidly between saturation and cut-off and therefore has little dissipation. This eases heatsink requirements, which contributes to weight and volume reduction. Conventional linear regulator supplies may have efficiencies as low as 50%, or less, but efficiencies of 80% are readily achievable with SMPS (see Figure 1).
- Wide AC input voltage range because the flexibility of varying the switching frequency in addition to the change in transistor duty cycle makes voltage adaptation unnecessary.
- Low overall cost, due to the reduced volume and power dissipation, means that less material is required and smaller semiconductor devices suffice.

Switched-mode power supplies also have slight disadvantages in comparison to linear regulators, namely, somewhat greater circuit complexity, tendency to RFI radiation, slower response to rapid load changes, and less ability to remove output ripple.

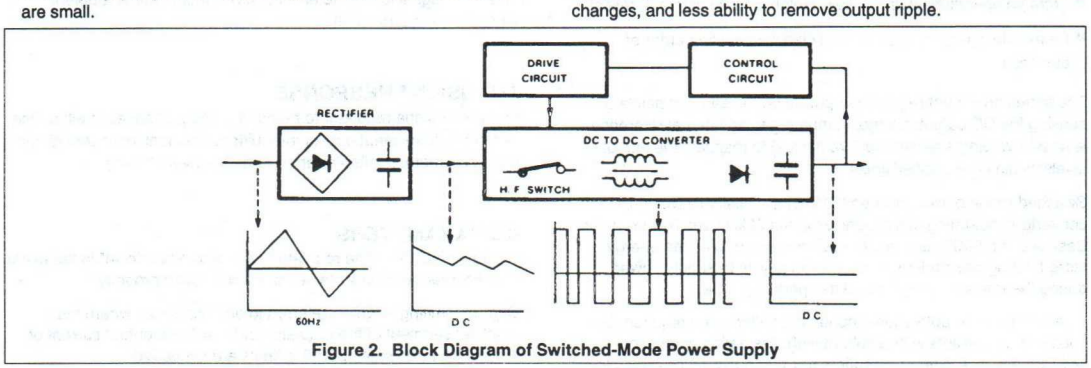


Figure 2. Block Diagram of Switched-Mode Power Supply

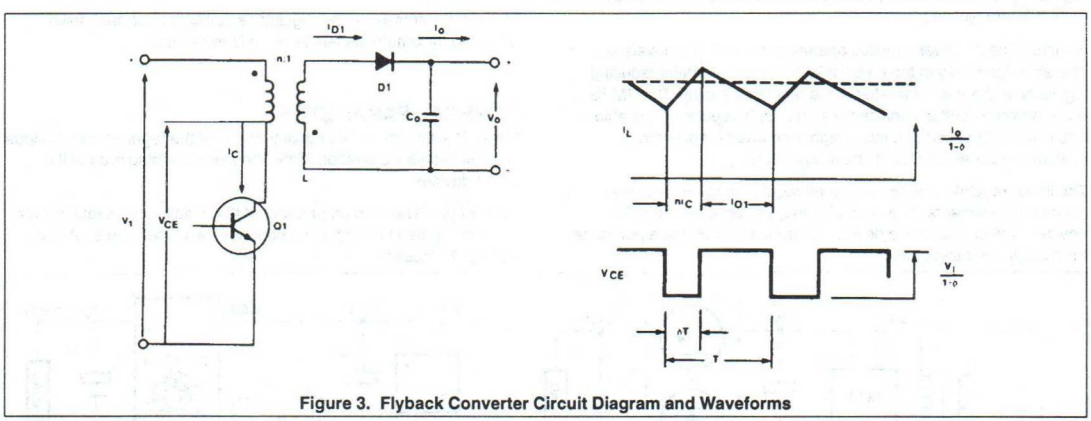


Figure 3. Flyback Converter Circuit Diagram and Waveforms

HOW SWITCHED-MODE POWER SUPPLIES OPERATE

The switched-mode power supply is a modern version of its forerunner, the electromechanical vibrator, used in the past to supply car radios. But the new concept is much more reliable because of the far greater lifetime of the transistor switch. Figure 2 shows the principle of the AC fed SMPS. In this system, the AC voltage is rectified, smoothed, and supplied to the electronic chopper, which operates at a frequency above the audible range to prevent noise. The chopped DC voltage is applied to the primary of a transformer, and the secondary voltage is rectified and smoothed to give the required DC output. The transformer is necessary to isolate the output from the input. Output voltage is sensed by a control circuit, which adjusts the duty cycle of the switching transistor, via the drive circuit, to keep the output voltage constant irrespective of load and

line voltage changes. Without the input rectifier, this system can be operated from a battery or other DC source.

Depending on the requirements of the application, the DC-to-DC converter can be one of the three basic types: flyback converter, forward converter, or push-pull (balanced) converter.

The Flyback Converter

Figure 3 shows the flyback converter circuit, and the waveforms of transistor voltage, V_{CE}, and choke current, I_L, reflected to the primary (choke double-wound for line isolation). Cycle time and transistor duty cycle are denoted T and δ, respectively. While Q1 conducts, energy is accumulated in the choke magnetic field (I_L rising and D_1 reverse-biased), and it is discharged into the output capacitor and the load during the flyback period, that is, while Q1 is off (I_L falling and D_1 forward-biased). During Q1 conduction, C_O continues delivering energy to the load, so providing smoothing action. It will be noted that only one inductive element is needed, in distinction to the converter types discussed below, which require two. As the V_{CE} waveform shows, the peak collector voltage is twice the input voltage, V_I, for δ equal to 0.5.

The Forward Converter

A major advantage of the forward converter, particularly for low output voltage applications, is that the high frequency output ripple is limited by the choke in series with the output. Figure 4 illustrates the circuit. During the transistor-on (or forward) period, energy is simultaneously stored in the choke L_O and passed via D_1 to the load. While Q1 is off, part of the energy accumulated in L_O is transferred to the load through free-wheeling diode D_2. Output capacitor C_O smoothes the ripple due to transistor switching. After transistor turn-off, the magnetic energy built up in the transformer core is returned to the DC input via the demagnetizing winding (closely coupled with the primary) and D_3, so limiting the peak collector voltage to twice the input voltage, V_I.

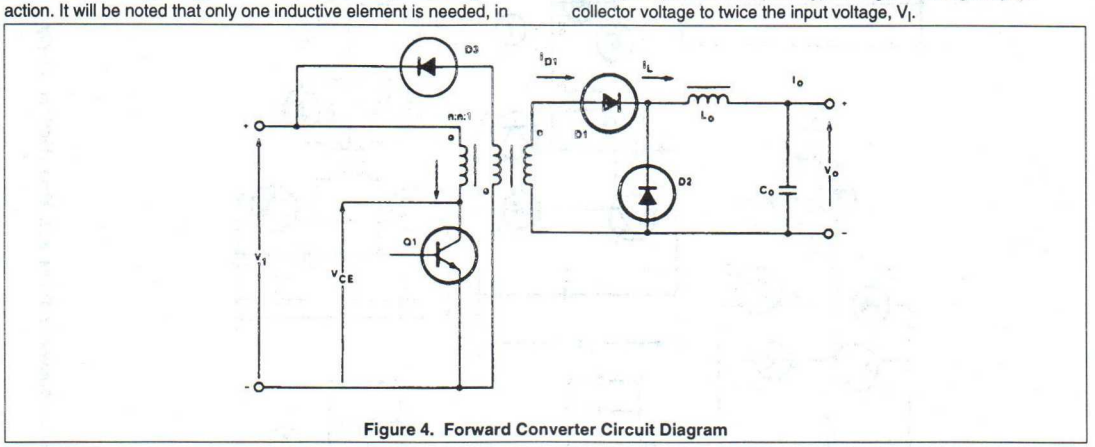


Figure 4. Forward Converter Circuit Diagram

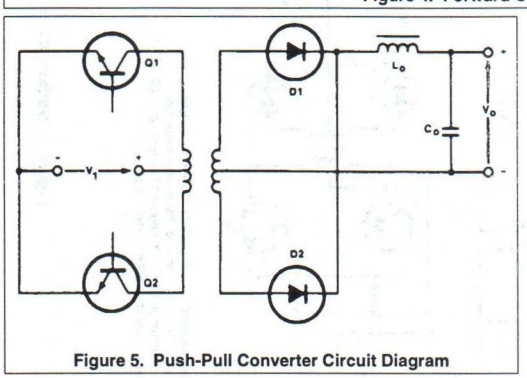


Figure 5. Push-Pull Converter Circuit Diagram

The Push-Pull Converter

This converter type, given in Figure 5, consists of two forward converters operating in push-pull. Diodes D_1 and D_2 rectify the rectangular secondary voltage generated by Q1 and Q2 being turned on during alternate half cycles. Push-pull operation doubles the frequency of the ripple current in output filter L_OC_O and so reduces the output ripple voltage. The peak transistor voltage is $2V_I$.

MAKING THE BEST CONVERTER CHOICE

There exist several versions of the three fundamental circuits described earlier.

These are shown in Figure 6. Circuits IA, IIA and IIIA are the basic types. In the two transistor circuits IB and IIB, transistors Q1 and Q2 conduct simultaneously and diodes D_4 and D_5 limit the peak collector voltage to the level of DC input voltage, V_I. Similarly, in the push-pull circuits IIIB and IIIC, the collector voltage does not exceed V_I; in circuit IIIB, Q1 and Q2 are turned on during alternate half cycles, in circuit IIIC, Q1 and Q4 are turned on in one half cycle and Q2 and Q3 in the next.

Converter choice depends on application and performance requirements. The flyback converter is the simplest and least expensive; it is recommended for multi-output supplies because each output requires only one diode and one capacitor. However, smoothing may be a problem where ripple requirements are severe. The push-pull type has the most complex base drive circuit but it produces the lowest output ripple with given values of L_O and C_O.

Figure 7 is a general guide for the choice of converter type, based on output voltage and power. In the case of the flyback converter, it becomes more and more difficult to keep the percentage output ripple below an acceptable level as the output power increases and the output voltage decreases. For reasons of circuit economy, however, the flyback converter is the best proposition if the output power does not exceed about 10W. For output powers higher than about 1kW, the push-pull converter is preferable.

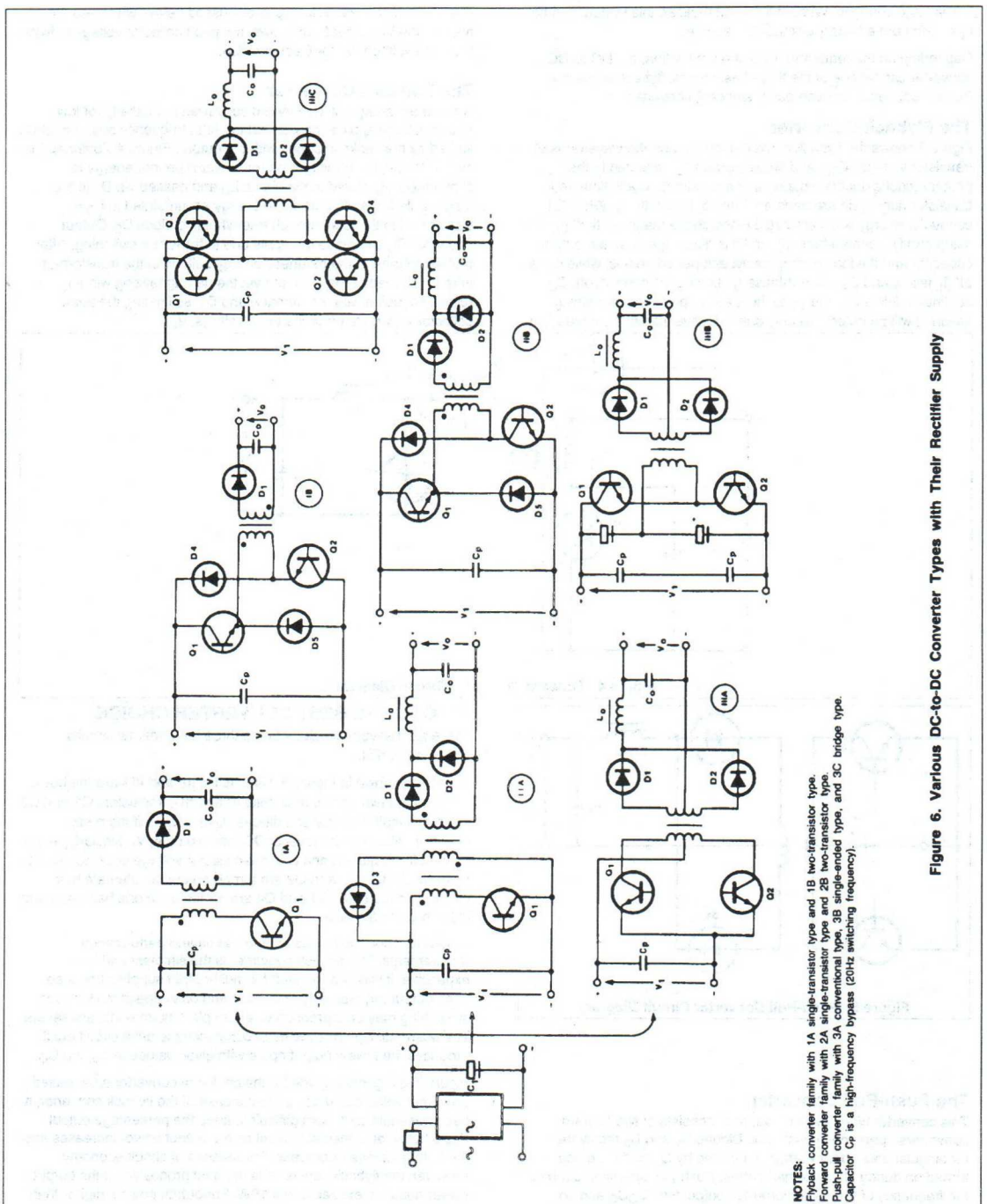


Figure 6. Various DC-to-DC Converter Types with Their Rectifier Supply

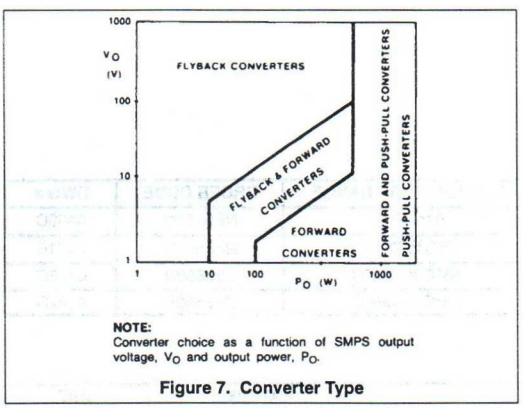
NOTES:
Flyback converter family with 1A single-transistor type and 1B two-transistor type.
Forward converter family with 2A single-transistor type and 2B two-transistor type.
Push-pull converter family with 3A conventional type, 3B single-ended type, and 3C bridge type.
Capacitor C_P is a high-frequency bypass (20Hz switching frequency).

THE CONTROL AND PROTECTION MODULE

In addition to providing adequate output voltage stabilization against line voltage and load changes, the control module must give fast protection against overload, equipment malfunction, and the effects of switch-on immediately following switch-off. In addition the following features are desirable:

- Soft-Start: a gradual increase of the transistor duty cycle after switch-on causing a slow rise of the output voltage, which prevents an excessive in-rush current due to a capacitive load or charging of the output capacitor.
- Synchronization: to prevent interference due to the difference in free-running frequencies (for example, in a system in which a low-power SMPS supplies the base drive circuit of the output switching transistor in a high-power SMPS).
- Remote switch-on and switch-off: essential for sequential switching of supply units in, for instance, a computer supply system.

The control and protection circuitry of a switched-mode power supply (SMPS) is a crucial and complicated part of the whole supply. Integration of this circuitry on a chip will therefore ease the design of an SMPS considerably.



NOTE:
Converter choice as a function of SMPS output voltage, V_O and output power, P_O.

Figure 7. Converter Type

SMPS CONTROL LOOP

Figure 8 shows the principal control loop of a regulated SMPS. The output voltage V_O is sensed and, via a feedback network, fed to the input of an error amplifier where it is compared with a reference voltage.

The output of this amplifier is connected to an input of the pulse-width modulator, PWM.

The other input of this modulator is used for an oscillator signal, which can be a sawtooth or a triangle.

As a result, a rectangular waveform with the frequency of the oscillator is emerging at the output of the PWM.

The width of this pulse is dictated by the output voltage of the error amplifier.

After passing through an output stage, the pulse can be used to drive the power transistor of the SMPS.

When the width of the pulse is varied, the ontime of this transistor will also vary and consequently the amount of energy taken from the input voltage, V_I.

So, by controlling the duty cycle δ of the power transistor, one can stabilize the output of the SMPS against line and load variations. The duty cycle δ is defined as t_{ON}/T for the power transistor. Protections for overvoltage, overcurrent, etc., can be realized with additional inputs on the PWM or the output stage.

INITIAL TURN-ON

It may be helpful to operate an SMPS open loop with reduced error amplifier gain. This provides an easy way to verify correct operation of control loop elements.

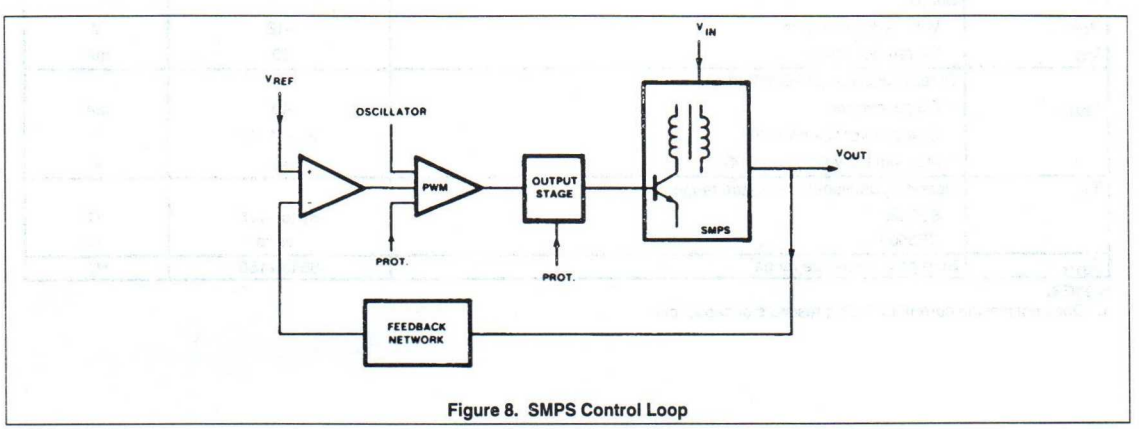


Figure 8. SMPS Control Loop

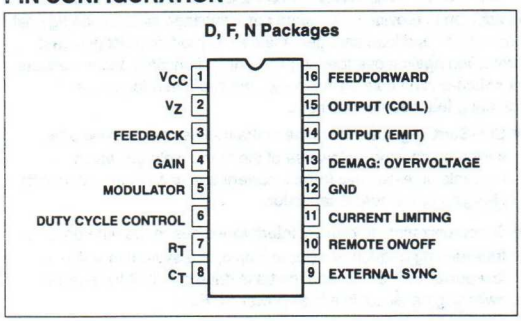
Switched-mode power supply control circuit

NE/SE5560

DESCRIPTION

The NE/SE5560 is a control circuit for use in switched-mode power supplies. This single monolithic chip incorporates all the control and housekeeping (protection) functions required in switched-mode power supplies, including an internal temperature-compensated reference source, internal Zener references, sawtooth generator, pulse-width modulator, output stage and various protection circuits.

PIN CONFIGURATION



FEATURES

- Stabilized power supply
- Temperature-compensated reference source
- Sawtooth generator
- Pulse-width modulator
- Remote on/off switching
- Current limiting
- Low supply voltage protection
- Loop fault protection
- Demagnetization/overvoltage protection
- Maximum duty cycle clamp
- Feed-forward control
- External synchronization

ORDERING INFORMATION

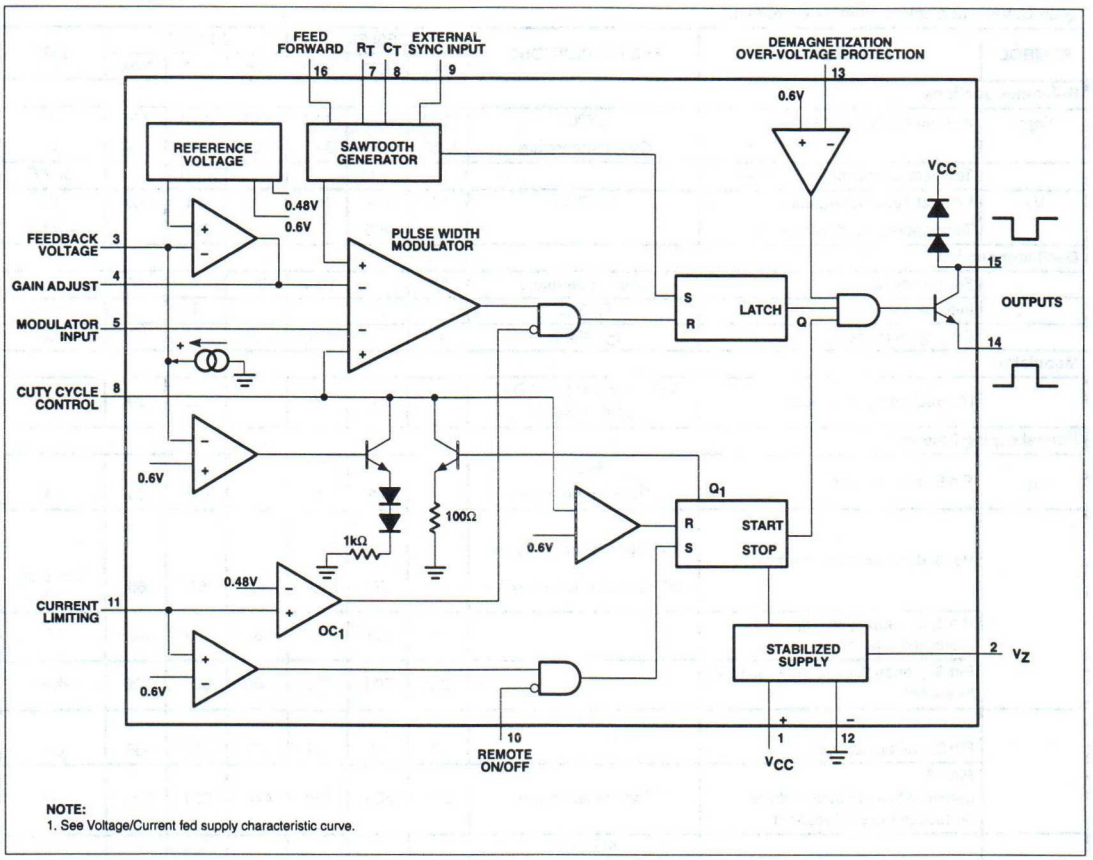
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to 70°C	NE5560N	0406C
16-Pin Plastic Small Outline Large (SOL) Package	0°C to 70°C	NE5560D	0171B
16-Pin Plastic Dual In-Line Package (DIP)	-55°C to 125°C	SE5560N	0406C
16-Pin Cerdip Dual In-Line Package (CERDIP)	-55°C to 125°C	SE5560F	0582B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply[1]		
V_{CC}	Voltage-forced mode	+18	V
I_{CC}	Current-fed mode	30	mA
	Output transistor (at 20-30V max)		
I_{OUT}	Output current	40	mA
	Collector voltage (Pin 15)	V_{CC}+1.4V	V
	Max. emitter voltage (Pin 14)	+5	V
T_A	Operating ambient temperature range		
	SE5560	-55 to +125	°C
	NE5560	0 to 70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Does not include current for timing resistors or capacitors.

BLOCK DIAGRAM



NOTE:
1. See Voltage/Current fed supply characteristic curve.

DC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC}=12V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
			Min	Typ	Max	Min	Typ	Max	
Reference sections									
V_{REF}	Internal reference voltage	25°C	3.69	3.72	3.81	3.57	3.72	3.95	V
		Over temperature	3.65		3.85	3.53		4.00	V
	Temperature coefficient of V_{REF}			-100			-100		ppm/°C
V_Z	Internal Zener reference	I_L=-7mA	7.8	8.4	8.8	7.8	8.4	8.8	V
	Temperature coefficient of V_Z			200			200		ppm/°C
Oscillator section									
	Frequency range	Over temperature	50		100k	50		100k	Hz
	Initial accuracy oscillator	R=5kΩ		5			5		%
	Duty cycle range	f_O=20kHz	0		98	0		98	%
Modulator									
	Modulation input current	Voltage at Pin 5=2V Over temperature		0.2	20		0.2	20	µA
Housekeeping function									
$I_{IN'}$	Pin 6, input current	At 2V							
		Over temperature		0.2	20		0.2	20	µA
	Pin 6, duty cycle limit control	For 50% max duty cycle							
		15kHz to 50kHz/41% of V_Z	40	50	60	40	50	60	% of duty cycle
	Pin 1, low supply voltage protection thresholds		8	9.0	10.5	8	9.0	10.5	V
	Pin 3, feedback loop protection trip threshold		400	600	720	400	600	720	mV
		At 2V							
	Pin 3, pull-up current		-7	-15	-35	-7	-15	-35	µA
	Pin 13, demagnetization/over-voltage protection trip on threshold	Over temperature	470	600	720	470	600	720	mV
I_{IN}	Pin 13, input current	At 0.25V							
		25°C		-0.6	-10		-0.6	-10	µA
		Over temperature			-20			-20	
	Pin 16, feed-forward duty cycle control	Voltage at Pin 16=2V_Z	30	40	50	30	40	50	% original duty cycle
		At 16V, V_{CC}=18V							
	*Pin 16, feed-forward input current	25°C		0.2	5		0.2	5	µA
		Over temperature			10			10	µA
External synchronization									
	Pin 9 Off		0		0.8	0		0.8	V
	On		2		V_Z	2		V_Z	V
	Sink current	Voltage at Pin 9=0V, 25°C		-65	-100		-65	-125	µA
		Over temperature			-125			-125	µA
Remote									
	Pin 10 Off		0		0.8	0		0.8	V
	On		2		V_Z	2		V_Z	V
		At 0V							
	Sink current	25°C		-85	-100		-85	-125	µA
		Over temperature			-125			-125	µA

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
			Min	Typ	Max	Min	Typ	Max	
Current limiting									
I_{IN}	Pin 11 Input current	Voltage at Pin 11=250mV		-2	-20		-2	-20	µA
		25°C							
		Over temperature			-40			-40	µA
	Single pulse inhibit delay	Inhibit delay time for 20% overdrive at 40mA I_{OUT}		0.7	0.8		0.7	0.8	µs
OC2	Trip Levels: Shut down, slow start, low level		0.500	0.600	0.700	0.500	0.600	0.700	V
OC1	Current limit, high level		0.400	0.480	0.560	0.400	0.560	0.500	V
ΔOC	Low Level in terms of high level, OC_2		0.750	0.800	0.850	0.750	0.800	0.850	V
Error amplifier									
V_{OH}	Output voltage swing		6.2		9.5	6.2		9.5	V
V_{OL}	Output voltage swing				0.7			0.7	V
	Open-loop gain		54	60		54	60		dB
R_F	Feedback resistor		10k			10k			Ω
BW	Small-signal bandwidth			3			3		MHz
Output stage									
	V_{CE}(SAT) I_C=40mA				0.5			0.5	V
	Output current (Pin 15)		40			40			mA
	Max. emitter voltage (Pin 14)		5	6		5	6		V
Supply voltage/current[1]									
I_{CC}	Supply current	I_Z=0, voltage-forced,							
		V_{CC}=12V, 25°C			10			10	mA
		Over temp.			15			15	mA
V_{CC}	Supply voltage	I_{CC}=10mA current-fed	20		23	19		24	V
V_{CC}	Supply voltage	I_{CC}=30mA current-fed	20		30	20		30	V

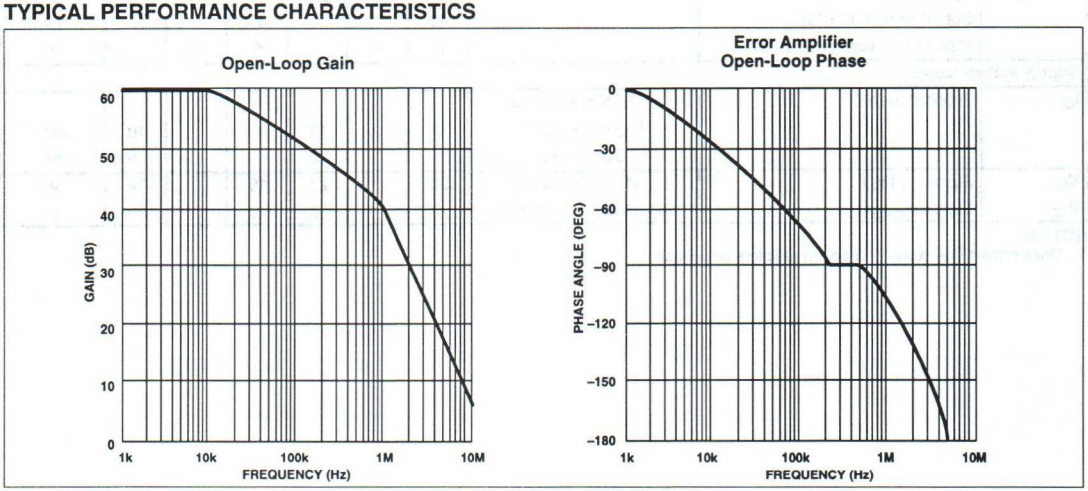
NOTES:
1. Does not include current for timing resistors or capacitors.

MAXIMUM PIN VOLTAGES

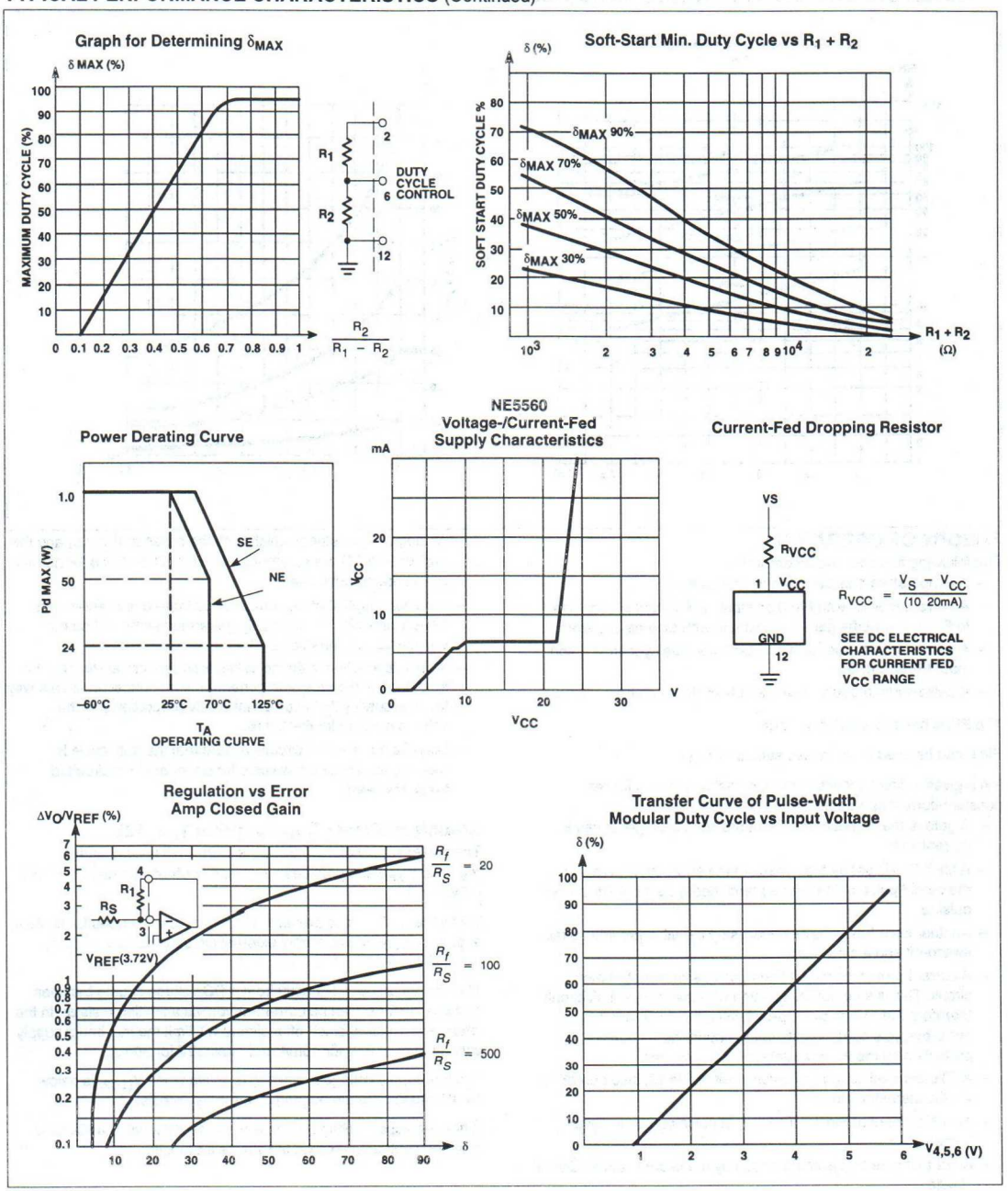
NE5560		
Pin No	**Function**	**Maximum Voltage**
1	V_{CC}	See Note 1
2	V_Z	Do not force (8.4V)
3	Feedback	V_Z
4	Gain	
5	Modulator	V_Z
6	Duty Cycle Control	V_Z
7	R_T	Current force mode
8	C_T	
9	External Sync	V_Z
10	Remote On/Off	V_Z
11	Current Limiting	V_{CC}
12	GND	GND
13	Demagnetization/Overvoltage	V_{CC}
14	Output (Emit)	V_Z
15	Output (Collector)	$V_{CC}+2V_{BE}$
16	Feed-forward	V_{CC}

NOTES:
1. When voltage-forced, maximum is 18V; when current-fed, maximum is 30mA. See voltage-/current-fed supply characteristic curve.

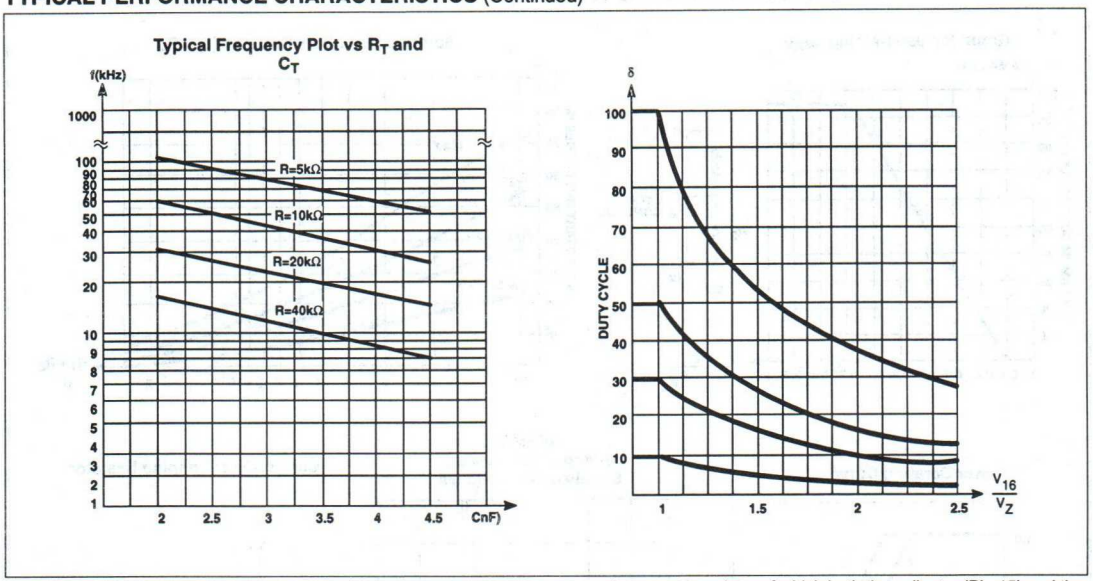
TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



THEORY OF OPERATION

The following functions are incorporated:

- A temperature-compensated reference source.
- An error amplifier with Pin 3 as input. The output is connected to Pin 4 so that the gain is adjustable with external resistors.
- A sawtooth generator with a TTL-compatible synchronization input (Pins 7, 8, 9).
- A pulse-width modulator with a duty cycle range from 0 to 95%.

The PWM has two additional inputs:

Pin 6 can be used for a precise setting of δ_{MAX}

Pin 5 gives a direct access to the modulator, allowing for real constant-current operation:

- A gate at the output of the PWM provides a simple dynamic current limit.
- A latch that is set by the flyback of the sawtooth and reset by the output pulse of the above mentioned gate prohibits double pulsing.
- Another latch functions as a start-stop circuit; it provides a fast switch-off and a slow start.
- A current protection circuit that operates via the start-stop circuit. This is a combined function with the current limit circuit, therefore Pin 11 has two trip-on levels; the lower one for cycle-by-cycle current limiting, the upper one for current protection by means of switch-off and slow-start.
- A TTL-compatible remote on/off input at Pin 10, also operating via the start-stop circuit.
- An inhibit input at Pin 13. The output pulse can be inhibited immediately.
- An output gate that is commanded by the latches and the inhibit circuit.
- An output transistor of which both the collector (Pin 15) and the emitter (Pin 14) are externally available. This allows for normal or inverse output pulses.
- A power supply that can be either voltage- or current-driven (Pins 1 and 12). The internally-generated stabilized output voltage VZ is connected to Pin 2.
- A special function is the so-called feed-forward at Pin 16. The amplitude of the sawtooth generator is modulated in such a way that the duty cycle becomes inversely proportional to the voltage on this pin: $\delta \sim 1/V16$.
- Loop fault protection circuits assure that the duty cycle is reduced to zero or a low value for open- or short-circuited feedback loops.

Stabilized Power Supply (Pins 1, 2, 12)

The power supply of the NE5560 is of the well known series regulation type and provides a stabilized output voltage of typically 8.5V.

This voltage V_Z is also present at Pin 2 and can be used for precise setting of δ_{MAX} and to supply external circuitry. Its max. current capability is 5mA.

The circuit can be fed directly from a DC voltage source between 10.5V and 18V or can be current-driven via a limiting resistor. In the latter case, internal pinch-off resistors will limit the maximum supply voltage: typical 23V for 10mA and max. 30V for 30mA.

The low supply voltage protection is active when $V_{(1-12)}$ is below 10.5V and inhibits the output pulse (no hysteresis).

When the supply voltage surpasses the 10.5V level, the IC starts delivering output pulses via the slow-start function.

The current consumption at 12V is less than 10mA, provided that no current is drawn from V_Z and $R_{(7-12)} \geq 20k\Omega$.

The Sawtooth Generator

Figure 1 shows the principal circuitry of the oscillator. A resistor between Pin 7 and Pin 12 (GND) determines the constant current that charges the timing capacitor $C_{(8-12)}$.

This causes a linear increasing voltage on Pin 8 until the upper level of 5.6V is reached. Comparator H sets the RS flip-flop and Q1 discharges $C_{(8-12)}$ down to 1.1V, where comparator L resets the flip-flop. During this flyback time, Q2 inhibits the output.

Synchronization at a frequency lower than the free-running frequency is accomplished via the TTL gate on Pin 9. By activating this gate (V^9<2V), the setting of the sawtooth is prevented. This is indicated in Figure 2.

Figure 3 shows a typical plot of the oscillator frequency against the timing capacitor. The frequency range of the NE5560 goes from <50Hz up to >100kHz.

Reference Voltage Source

The internal reference voltage source is based on the bandgap voltage of silicon. Good design practice assures a temperature dependency typically ±100ppm/°C. The reference voltage is connected to the positive input of the error amplifier and has a typical value of 3.72V.

Error Amplifier Compensation

For closed-loop gains less than 40dB, it is necessary to add a simple compensation capacitor as shown in Figures 3 and 4.

Error Amplifier with Loop-Fault Protection Circuits

This operational amplifier is of a generally used concept and has an open-loop gain of typically 60dB. As can be seen in Figure 4, the inverting input is connected to Pin 3 for a feedback information proportional to V_O.

The output goes to the PWM circuit, but is also connected to Pin 4, so that the required gain can be set with R_S and $R_{(3-4)}$. This is indicated in Figure 4, showing the relative change of the feedback voltage as a function of the duty cycle. Additionally, Pin 4 can be used for phase shift networks that improve the loop stability.

When the SMPS feedback loop is interrupted, the error amplifier would settle in the middle of its active region because of the feedback via $R_{(3-4)}$. This would result in a large duty cycle. A current source on Pin 3 prevents this by pushing the input voltage high via the voltage drop over $R_{(3-4)}$. As a result, the duty cycle will become zero, provided that $R_{(3-4)}$>100k. When the feedback loop is short-circuited, the duty cycle would jump to the adjusted maximum duty cycle. Therefore, an additional comparator is active for feedback voltages at Pin 3 below 0.6V. Now an internal resistor of typically 1k is shunted to the impedance on the δ_{MAX} setting Pin 6. Depending on this impedance, δ will be reduced to a value δ_0. This will be discussed further.

The Pulse-Width Modulator

The function of the PWM circuit is to translate a feedback voltage into a periodical pulse of which the duty cycle depends on that feedback voltage. As can be seen in Figure 5, the PWM circuit in the NE5560 is a long-tailed pair in which the sawtooth on Pin 8 is compared with the LOWEST voltage on either Pin 4 (error amplifier), Pin 5, or Pin 6 (δ_{MAX} and slow-start). The transfer graph is given in Figure 6. The output of the PWM causes the resetting of the output bi-stable.

Limitation of the Maximum Duty Cycle

With Pins 5 and 6 not connected and with a rather low feedback voltage on Pin 3, the NE5560 will deliver output pulses with a duty cycle of ≈ 95%. In many SMPS applications, however, this high δ will cause problems. Especially in forward converters, where the transformer will saturate when δ exceeds 50%, a limitation of the maximum duty cycle is a must.

A DC voltage applied to Pin 6 (PWM input) will set δ_{MAX} at a value in accordance with Figure 6. For low tolerances of δ_{MAX}, this voltage on Pin 6 should be set with a resistor divider from V_Z (Pin 2). The upper and lower sawtooth levels are also set by means of an internal resistor divider from V_Z, so forming a bridge configuration with the δ_{MAX} setting is low because tolerances in V_Z are compensated and the sawtooth levels are determined by internal resistor matching rather than by absolute resistor tolerance. Figure 7 can be used for determining the tap on the bleeder for a certain δ_{MAX} setting.

As already mentioned, Figure 8 gives a graphical representation of this. The value δo is limited to the lower and the higher side;

- It must be large enough to ensure that at maximum load and minimum input voltage the resulting feedback voltage on Pin 3 exceeds 0.6V.
- It must be small enough to limit the amount of energy in the SMPS when a loop fault occurs. In practice, a value of 10-15% will be a good compromise.

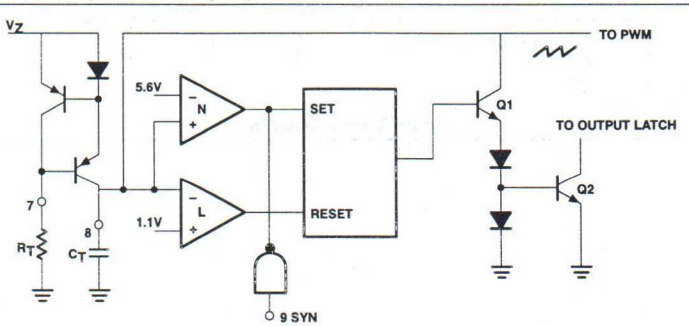


Figure 1. Sawtooth Generator

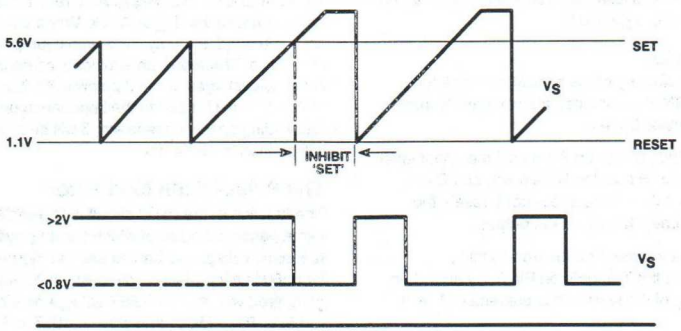


Figure 2. Sawtooth Oscillator Synchronization

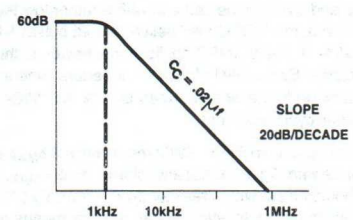


Figure 3. Error Amplifier Compensation Open-Loop Gain

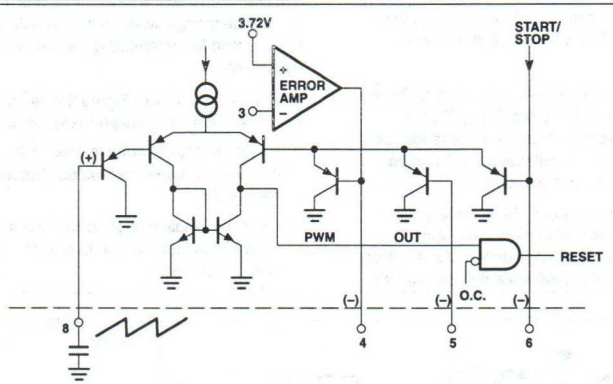
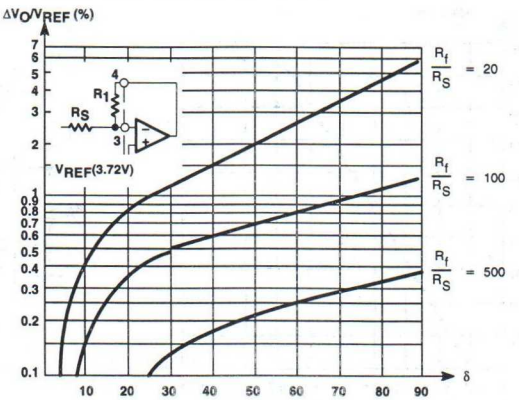
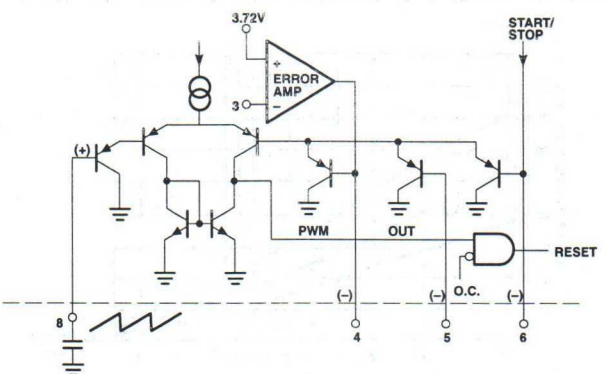


Figure 4. Error Amplifier



a. Duty Cycle — δ — % Regulation



b. Pulse-Width Modulation

Figure 5.

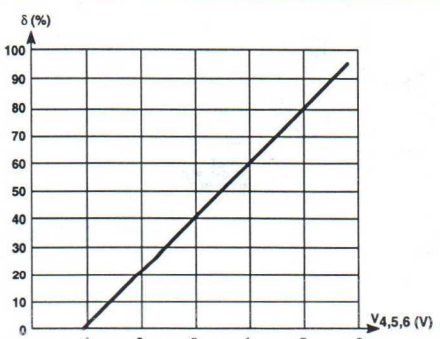


Figure 6. Transfer Curve of Pulse-Width Modulator Duty Cycle vs Input Voltage

Extra PWM Input (Pin 5)

The PWM has an additional inverting input: Pin 5. It allows for attacking the duty cycle via the PWM circuit, independently from the feedback and the δ_{MAX} information. This is necessary when the SMPS must have a real constant-current behavior, possibly with a fold-back characteristic. However, the realization of this feature must be done with additional external components. When not used, Pin 5 should be tied to Pin 6.

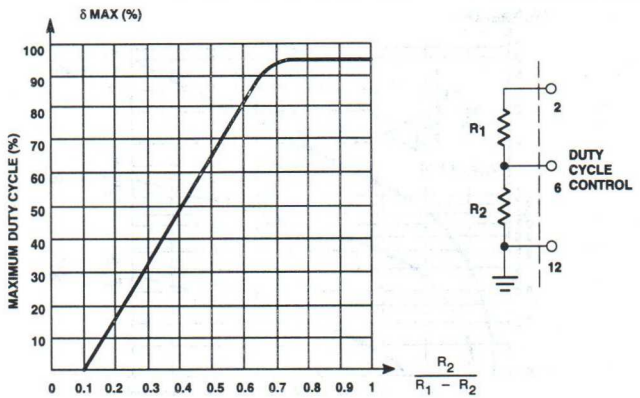


Figure 7. Graph for Determining δ_{MAX}

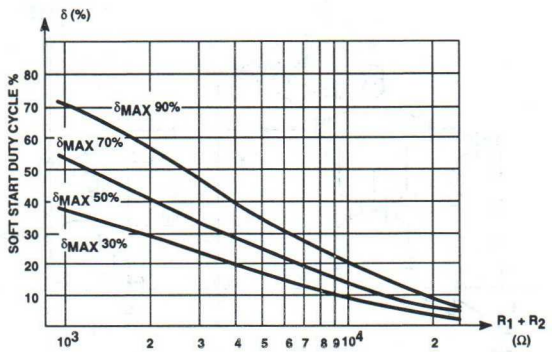


Figure 8. Soft-Start Minimum Duty Cycle vs $R_1 + R_2$

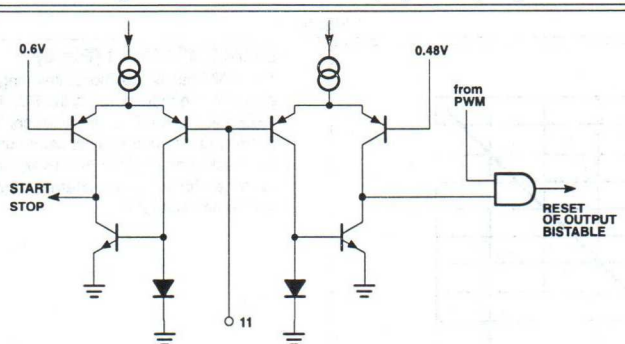


Figure 9. Current Protection Input

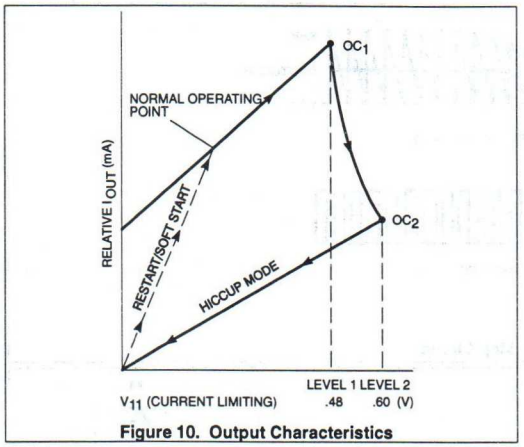


Figure 10. Output Characteristics

Dynamic Current Limit and Current Protection (Pin 11)

In many applications, it is not necessary to have a real constant-current output of the SMPS.

Protection of the power transistor will be the prime goal. This can be realized with the NE5560 in an economical way. A resistor (or a current transformer) in the emitter of the power transistor gives a replica of the collector current. This signal must be connected to Pin 11. As can be seen in Figure 9, this input has two comparators with different reference levels. The output of the comparator with the lower 0.48V reference is connected to the same gate as the output of the PWM.

When activated, it will immediately reset the output flip-flop, so reducing the duty cycle. The effectiveness of this cycle-by-cycle current limit diminishes at low duty cycle values. When δ becomes very small, the storage time of the power transistor becomes dominant. The current will now increase again, until it surpasses the reference of the second comparator. The output of this comparator activates the start-stop circuit and causes an immediate inhibit of the output pulses. After a certain deadtime, the circuit starts again with very narrow output pulses. The effect of this two-level current protection circuit is visualized in Figure 10.

The Start-Stop Circuit

The function of this protection circuit is to stop the output pulses as soon as a fault occurs and to keep the output stopped for several periods. After this dead-time, the output starts with a very small, gradually increasing duty cycle. When the fault is persistent, this will cause a cyclic switch-off/switch-on condition. This "hiccup" mode effectively limits the energy during fault conditions. The realization and the working of the circuit are indicated in Figures 12 and 13. The dead time and the soft-start are determined by an external capacitor that is connected to Pin 6 (δ_{MAX} setting).

An RS flip-flop can be set by three different functions:
1. Remote on/off on Pin 10.
2. Overcurrent protection on Pin 11.
3. Low supply voltage protection (internal).

As soon as one of these functions cause a setting of the flip-flop, the output pulses are blocked via the output gate. In the same time transistor Q1 is forward-biased, resulting in a discharge of the capacitor on Pin 6.

The discharging current is limited by an internal 150Ω resistor in the emitter of Q1. The voltage at Pin 6 decreases to below the lower level of the sawtooth. When V6 has dropped to 0.6V, this will activate a comparator and the flip-flop is reset. The output stage is no longer blocked and Q1 is cut off. Now V_Z will charge the capacitor via R1 to the normal δ_{MAX} voltage. The output starts delivering very narrow pulses as soon as V6 exceeds the lower sawtooth level. The duty cycle of the output pulse now gradually increases to a value determined by the feedback on Pin 3, or by the static δ_{MAX} setting on Pin 6.

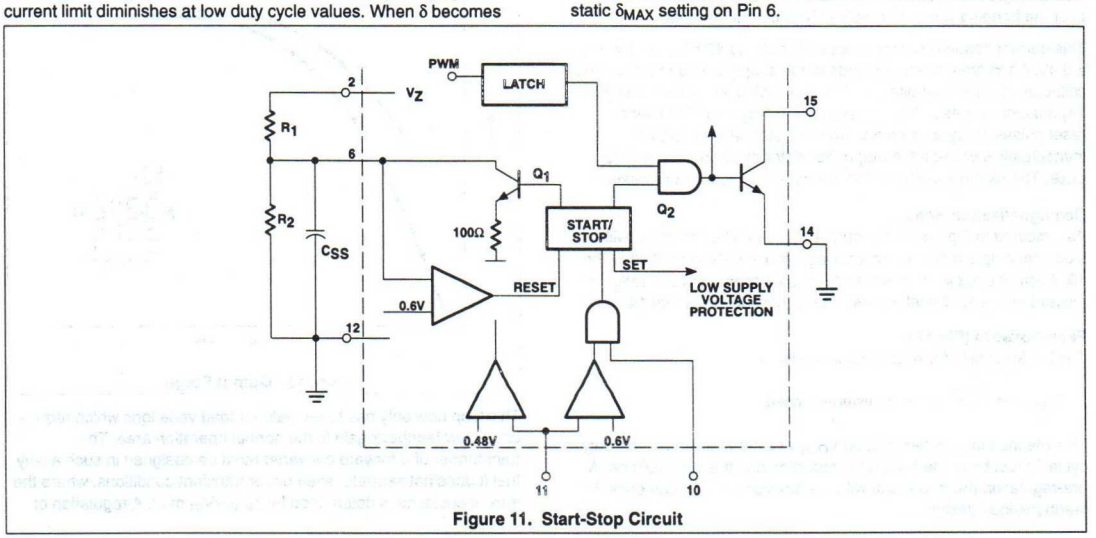


Figure 11. Start-Stop Circuit

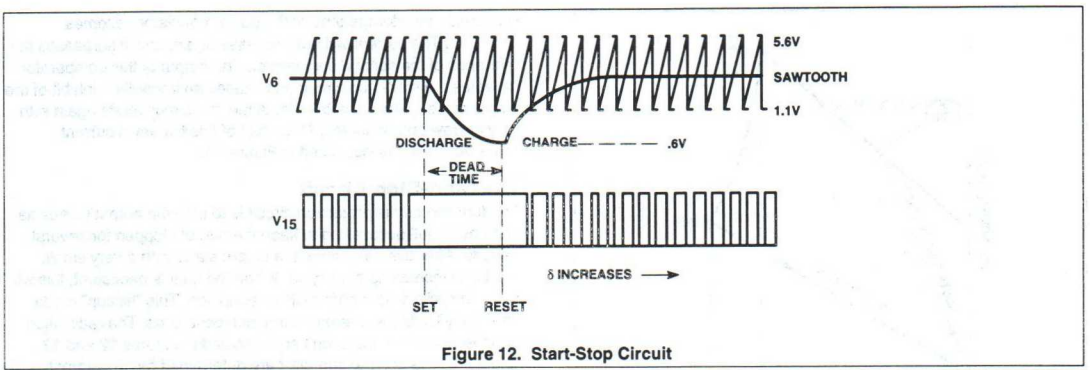


Figure 12. Start-Stop Circuit

Remote On/Off Circuit (Pin 10)

In systems where two or more power supplies are used, it is often necessary to switch these supplies on and off in a sequential way. Furthermore, there are many applications in which a supply must be switched by a logical signal. This can be done via the TTL-compatible remote on/off input on Pin 10. The output pulse is inhibited for levels below 0.8V. The output of the IC is no longer blocked when the remote on/off input is left floating or when a voltage >2V is applied. Start-up occurs via the slow-start circuit.

The Output Stage

The output stage of the NE5560 contains a flip-flop, a push-pull driven output transistor, and a gate, as indicated in Figure 13. The flip-flop is set by the flyback of the sawtooth. Resetting occurs by a signal either from the PWM or the current limit circuit. With this configuration, it is assured that the output is switched only once per period, thus prohibiting double pulsing. The collector and emitter of the output transistor are connected to respectively Pin 15 and Pin 14, allowing for normal or inverted output pulses. An internally-grounded emitter would cause intolerable voltage spikes over the bonding wire, especially at high output currents.

This current capability of the output transistor is 40mA peak for $V_{CE} \equiv 0.4V$. An internal clamping diode to the supply voltage protects the collector against overvoltages. The max. voltage at the emitter (Pin 14) must not exceed +5V. A gate, activated by one of the set or reset pulses, or by a command from the start-stop circuit will immediately switch-off the output transistor by short-circuiting its base. The external inhibitor (Pin 13) operates also via this base.

Demagnetization Sense

As indicated in Figure 13, the output of this NPN comparator will block the output pulse, when a voltage above 0.6V is applied to Pin 13. A specific application for this function is to prevent saturation of forward-converter transformers. This is indicated in Figure 14.

Feed-Forward (Pin 16)

The basic formula for a forward converter is

$$V_{OUT} = \frac{dV_{IN}}{n} \quad (n = \text{transformer ratio})$$

This means that in order to keep V_{OUT} at a constant value, the duty cycle δ must be made inversely proportional to the input voltage. A pre-regulation (feed-forward) with the function $\delta \sim 1/V_{IN}$ can ease the feedback-loop design.

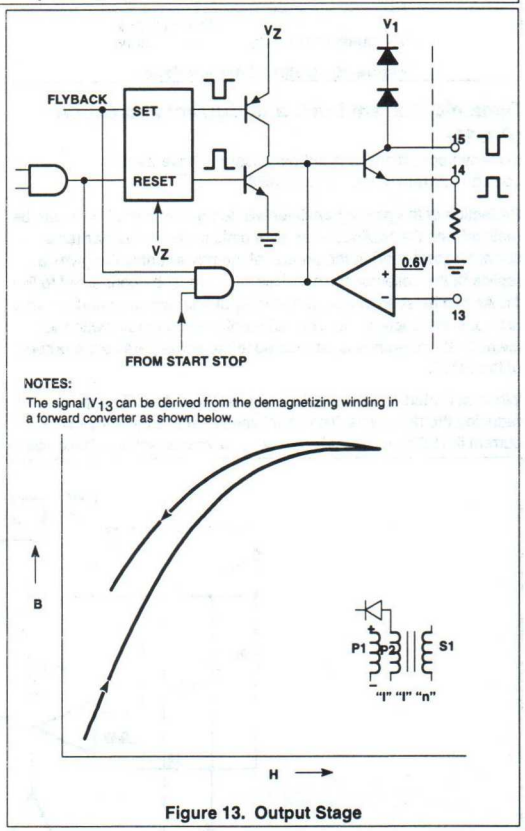


Figure 13. Output Stage

This loop now only has to regulate for load variations which require only a low feedback gain in the normal operation area. The transformer of a forward converter must be designed in such a way that it does not saturate, even under transient conditions, where the max. inductance is determined by $\delta_{MAX} \times V_{IN}$ max. A regulation of

δ_{MAX}~1/V_{IN} will allow for a considerable reduction or simplification of the transformer. The function of δ~1/V_{IN} can be realized by using Pin 16 of the NE5560.

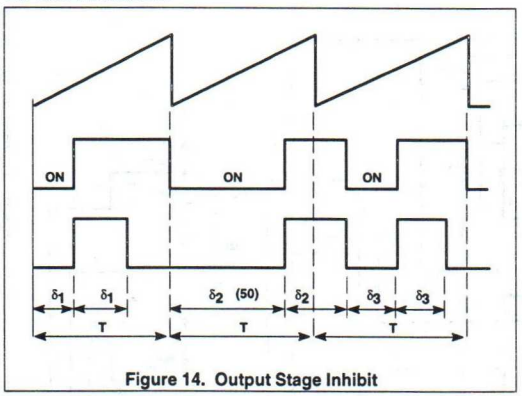


Figure 14. Output Stage Inhibit

Figure 15 shows the electrical realization. When the voltage at Pin 16 exceeds the stabilized voltage V_Z (Pin 2), it will increase the charging current for the timing capacitor on Pin 8.

The operating frequency is not affected, because the upper trip level for sawtooth increases also. Note that the δ_{MAX} voltage on Pin 6 remains constant because it is set via V_Z. Figure 16 visualizes the effect on δ_{MAX} and the normal operating duty cycle δ. For V_{16}=2×V_Z, these duty cycles have halved. The graph for δ=f(V_{16}) is given in Figure 17.

NOTE:
V_{16} must be less than Pin 1 voltage.

APPLICATIONS

NE/SE5560 Push-Pull Regulator

This application describes the use of the Philips Semiconductors NE/SE5560 adapted to function as a push-pull switched mode regulator, as shown in Figures 18 and 19.

Input voltage range is +12V to +18V for a nominal output of +30V and -30V at a maximum load current of 1A with an average efficiency of 81%.

Features include feed-forward input compensation, cycle-to-cycle drive current protection and other voltage sensing, line (to positive output) regulation <1% for an input range of +13V to +18V and load regulation to positive output of <3% for ΔI_L(+) of 0.1 to 1A.

The main pulse-width modulator operates to 48kHz with power switching at 24kHz.

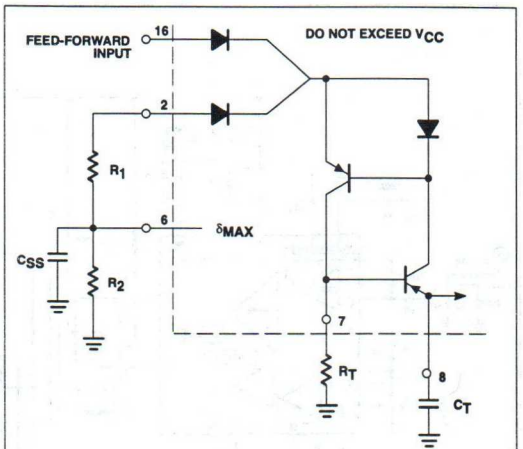


Figure 15. External δ Maximum Control

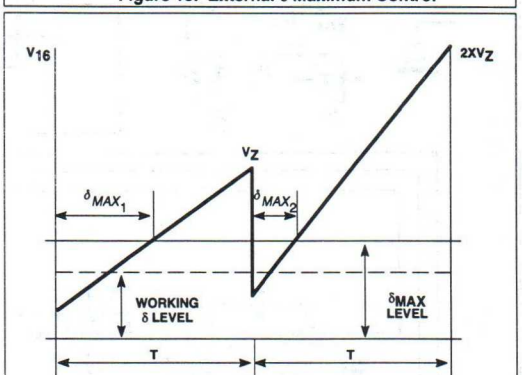


Figure 16. Feed-Forward Circuitry

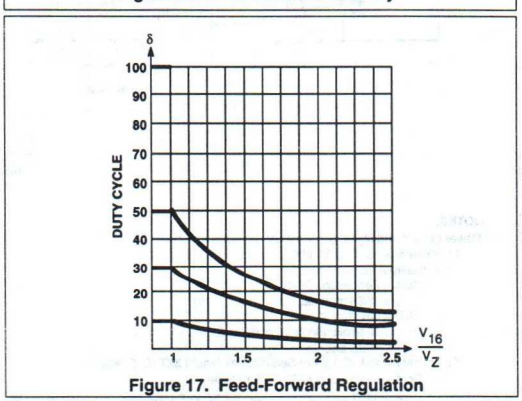
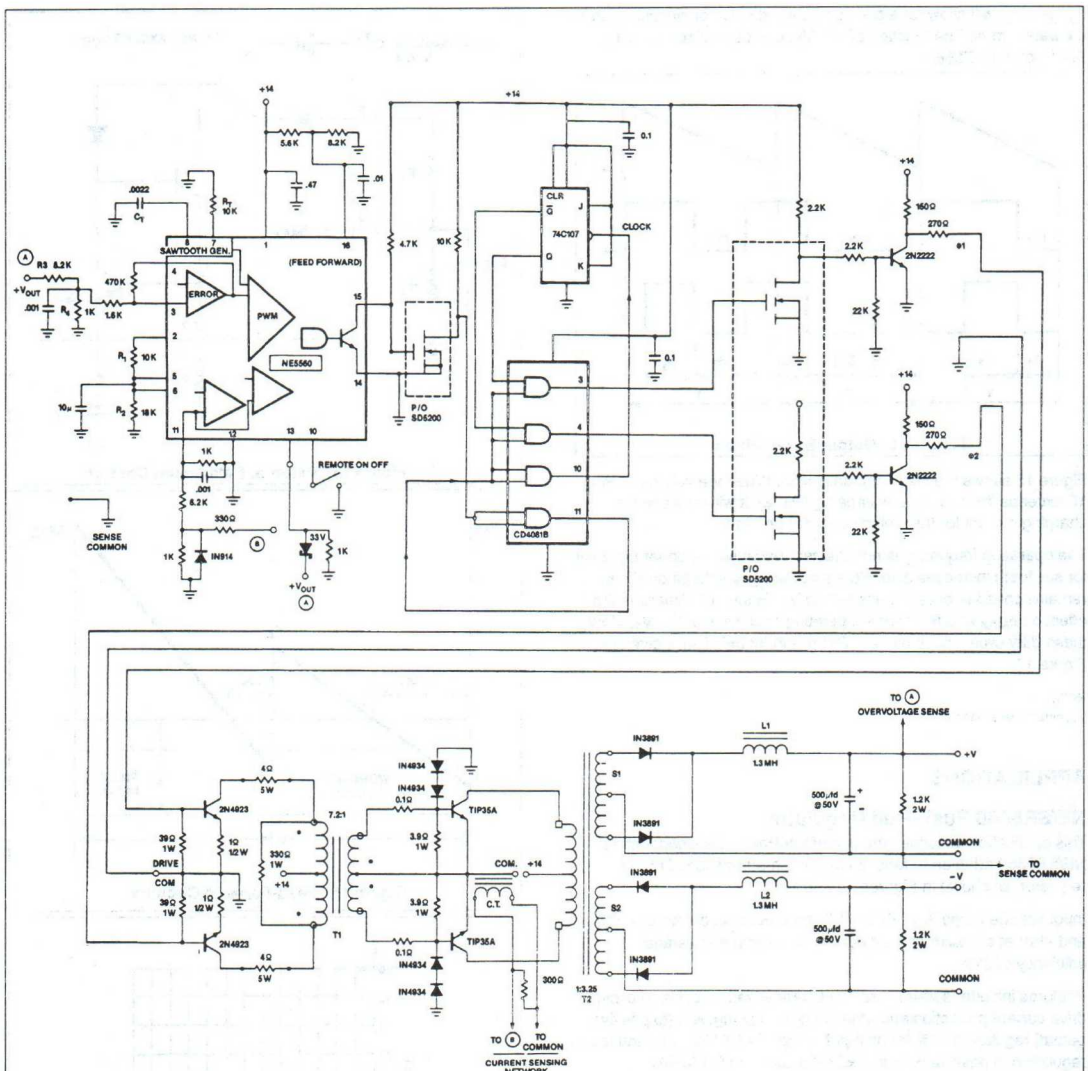


Figure 17. Feed-Forward Regulation



NOTES:

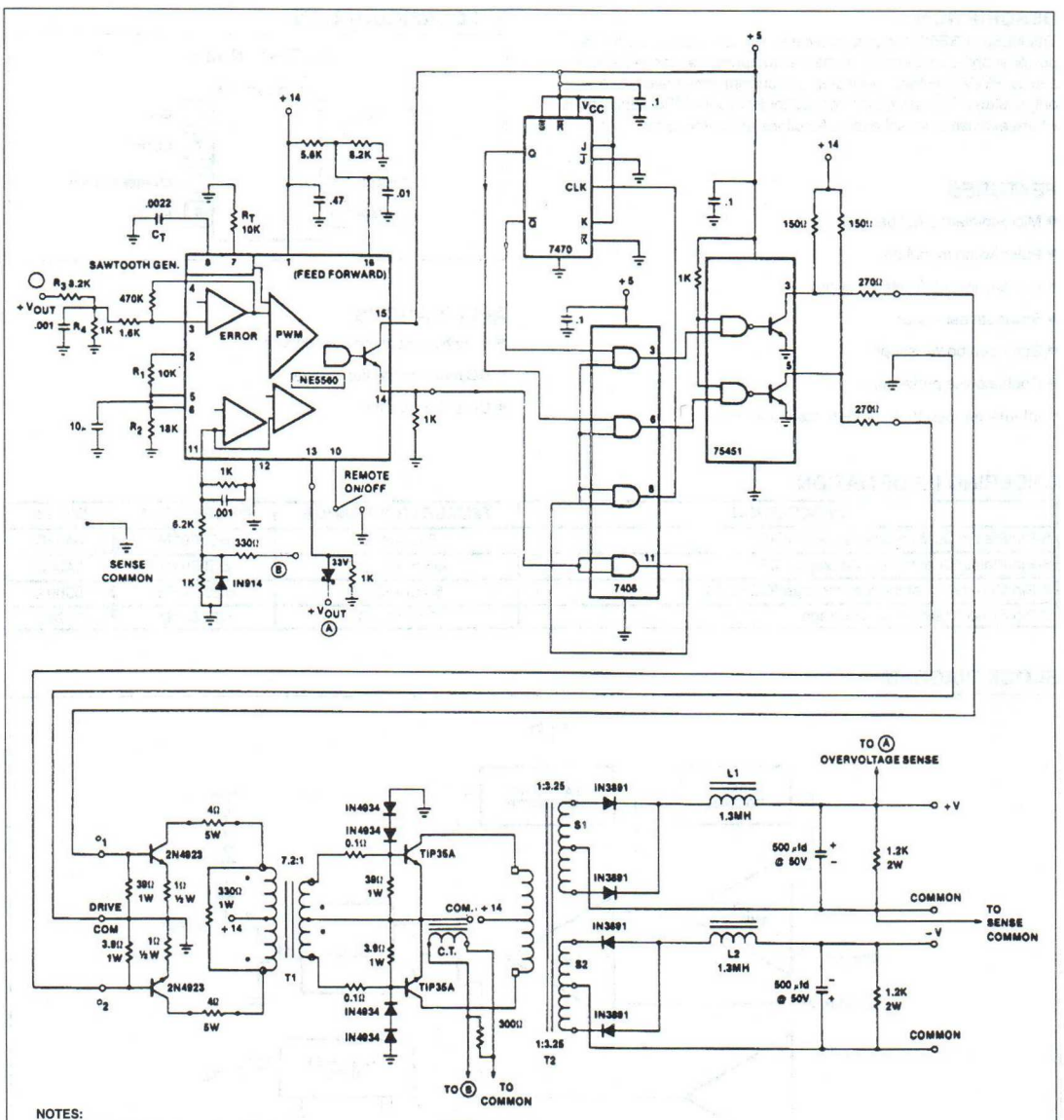
Power ground and signal ground must be kept separated

T1, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622
3C8 material
C.T. = 50T #26 0n
Ferroxcube 2616 core (3C8)
F2D bobbin

T2, Primary = 16T (C.T.) #18 Secondaries (each) 52T (C.T.) #22
Core = Ferroxcube 4229 3C8 material

L_1, L_2 = 120T #20 on single gapped EC35 Ferroxcube core. 3C8 material.

Figure 18. NE/SE5560 Push-Pull Switched-Mode Regulated Supply with CMOS Drive Conversion Logic



NOTES:

Power ground and signal ground must be kept separated

T1, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622
3C8 material
C.T. = 50T #26 0n
Ferroxcube 2616 core (3C8)
F2D bobbin

T2, Primary = 16T (C.T.) #18 Secondaries (each) 52T (C.T.) #22
Core = Ferroxcube 4229 3C8 material

L_1, L_2 = 120T #20 on single gapped EC35 Ferroxcube core. 3C8 material.

Figure 19. NE/SE5560 Push-Pull Switched-Mode Regulated With TTL Drive Conversion Logic

Switched-mode power supply control circuit — NE/SE5561

DESCRIPTION

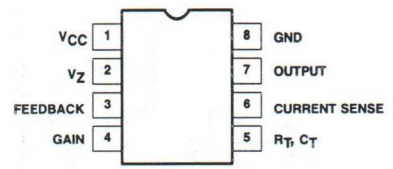
The NE5561/SE5561 is a control circuit for use in switched-mode power supplies. It contains an internal temperature- compensated supply, PWM, sawtooth oscillator, overcurrent sense latch, and output stage. The device is intended for low cost SMPS applications where extensive housekeeping functions are not required.

FEATURES

- Micro-miniature (D) package
- Pulse-width modulator
- Current limiting (cycle-by-cycle)
- Sawtooth generator
- Stabilized power supply
- Double pulse protection
- Internal temperature-compensated reference

PIN CONFIGURATION

D, FE, N Packages



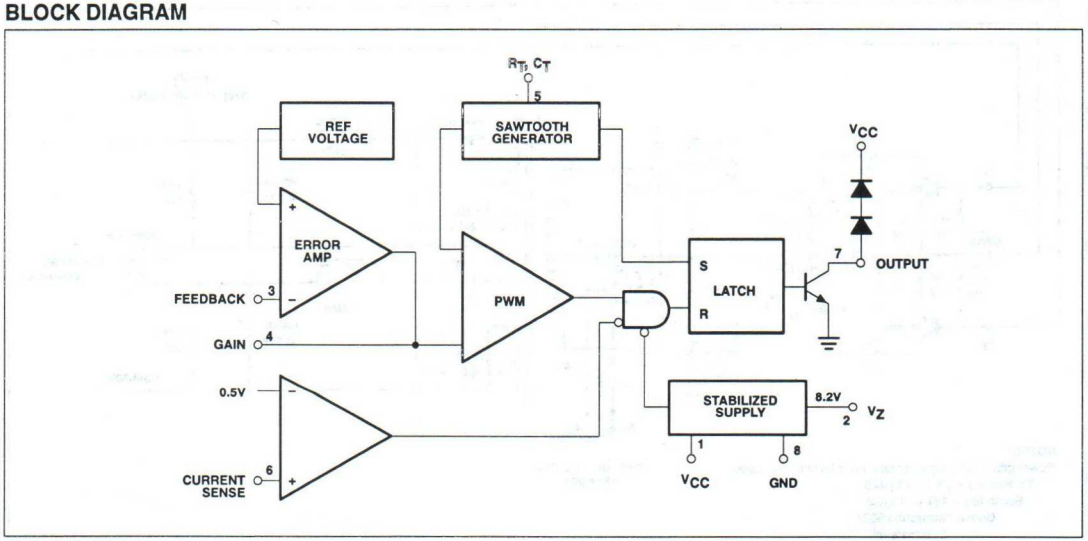
APPLICATIONS

- Switched-mode power supplies
- DC motor controller inverter
- DC/DC converter

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5561N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-55 to +125°C	SE5561N	0404B
8-Pin Ceramic Dual In-Line Package (CERDIP)	-55 to +125°C	SE5561FE	0580A
8-Pin Small Outline (SO) Package	0 to +70°C	NE5561D	0174C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply[1]		
	Voltage-forced mode	+18	V
	Current-fed mode	30	mA
	Output transistor (at 20-30V max)		
I_{OUT}	Output current	40	mA
V_{OUT}	Output voltage	V_{CC}+1.4V	V
	Output duty cycle	98	%
P_D	Maximum total power dissipation	0.75	W
T_A	Operating temperature range		
	SE5561	-55 to +125	°C
	NE5561	0 to 70	°C

NOTES:
1. See Voltage-Current-fed supply characteristic curve.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=12V, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5561			NE5561			UNIT
				Min	Typ	Max	Min	Typ	Max	
Reference section										
V_{REF}	Internal ref voltage	T_A=25°C		3.69	3.75	3.84	3.57	3.75	3.96	V
		Over temperature		3.65		3.88	3.55		3.98	V
V_Z	Internal zener ref	*I_L=7mA		7.8	8.2	8.8	7.8	8.2	8.8	V
	Temp. coefficient of V_{REF}				±100			±100		ppm/°C
	Temp. coefficient of V_Z				±200			±200		ppm/°C
Oscillator section										
	Frequency range	Over temperature		50		100k	50		100k	Hz
	Initial accuracy	R_T and C_T constant			5			5		%
	Duty cycle range	f_O=20kHz		0		98	0		98	%
Current limiting										
I_{IN}	Input current	Pin 6=250mV	T_A=25°C		-2	-10		-2	-10	µA
			Over temp.			-20			-20	µA
	Single pulse inhibit delay	Inhibit delay time for 20% overdrive at	I_{OUT}=20mA		0.88	1.10		0.88	1.10	µs
			I_{OUT}=40mA		0.7	0.8		0.7	0.8	µs
	Current limit trip level			.400	.500	.600	.400	.500	.600	V
Error amplifier										
	Open-loop gain				60			60		dB
	Feedback resistor			10k			10k			Ω
BW	Small-signal bandwidth				3			3		MHz
V_{OH}	Output voltage swing			6.2			6.2			V
V_{OL}	Output voltage swing					0.7			0.7	V
Output stage										
I_{OUT}	Output current	Over temperature		20			20			mA
V_{CE}	Sat	I_C=20mA, Over temp.				0.4			0.4	V

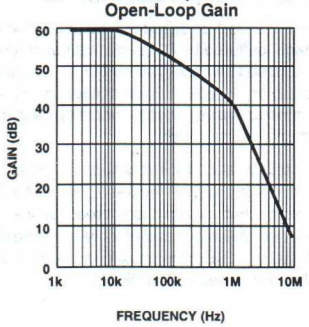
DC ELECTRICAL CHARACTERISTICS

V_{CC}=12V, T_A=25°C, unless otherwise specified.

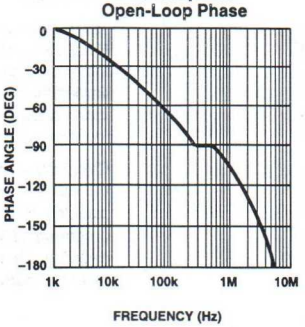
SYMBOL	PARAMETER	TEST CONDITIONS		SE5561			NE5561			UNIT
				Min	Typ	Max	Min	Typ	Max	
Supply voltage/current										
I_{CC}	Supply current	I_Z=0, voltage-forced	T_A=25°C			10.0			10.0	mA
			Over temp.			13.0			13.0	
V_{CC}	Supply voltage	I_{CC}=10mA, current-fed		20.0	21.0	22.0	19.0	21.0	24.0	V
		I_{CC}=30mA current		20.0		30.0	20.0		30.0	
Low supply protection										
	Pin 1 threshold			8	9	10.5	8	9	10.5	V

TYPICAL PERFORMANCE CHARACTERISTICS

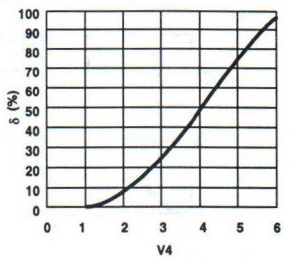
Error Amplifier Open-Loop Gain



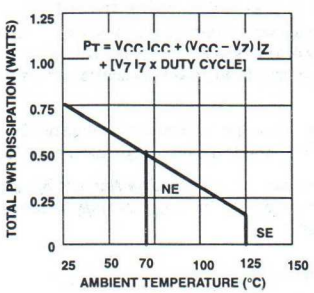
Error Amplifier Open-Loop Phase



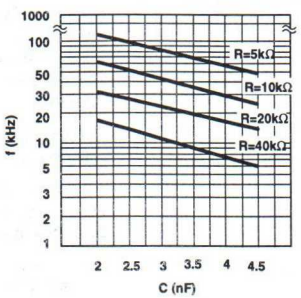
Transfer Curve of Pulse-Width Modulator Duty Cycle vs Input Voltage

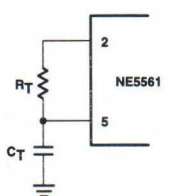


Power Derating Curve

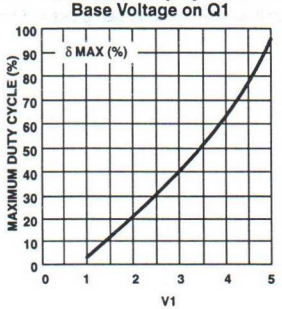


Typical Frequency Plot vs R_T and C_T

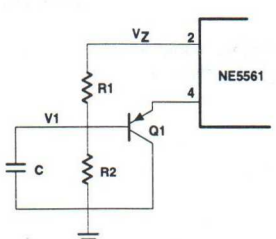




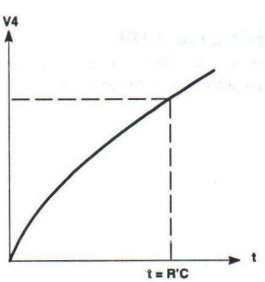
Maximum Duty Cycle vs Base Voltage on Q1



Start-Up Circuit

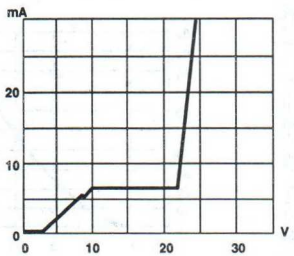


Slow-Start Voltage

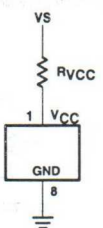


δ max is a function of $f\left[\frac{R2}{R1 + R2} V_Z + V_{BEQ1}\right]$

NE5561 Voltage-Current-Fed Supply Characteristics



Current-Fed Dropping Resistor



$$R_{VCC} = \frac{V_S - V_{CC}}{(10\ 20mA)}$$

NOTE:
See DC Electrical Characteristics for Current Fed V_{CC} Range.

NE5561 START-UP

The start-up, or initial turn-on, of this device requires some degree of external protective duty cycle limiting to prevent the duty cycle from initially going to the extreme maximum (δ>90%). Either overcurrent limit or slow-start circuitry must be employed to limit duty cycle to a safe value during start-up. Both may be used, if desired.

To implement slow-start, the start-up circuit can be used. The divider R1 and R2 sets a voltage, buffered by Q1, such that the output of the error amplifier is clamped to a maximum output voltage, thereby limiting the maximum duty cycle. The addition of capacitor C will cause this voltage to ramp-up slowly when power is applied, causing the duty cycle to ramp-up simultaneously.

Overcurrent limit may be used also. To limit duty cycle in this mode, the switch current is monitored at Pin 6 and the output of the 5561 is disabled on a cycle-by-cycle basis when current reaches the programmed limit. With current limit control of slow-start, the duty cycle is limited to that value, just allowing maximum switch current to flow. (Approximately 0.50V measured at Pin 6.)

APPLICATIONS

5V, 0.5A Buck Regulator Operates from 15V

The converter design shows how simple it is to derive a TTL supply from a system supply of 15V (see Figure 1). The NE5561 drives a 2N4920 PNP transistor directly to provide switching current to the inductor.

Overall line regulation is excellent and covers a range of 12V to 18V with minimal change (<10mV) in the output operating at full load.

As with all NE5561 circuits, the auxiliary slow start and δ_{MAX} circuit is required, as evidenced by Q1. The δ_{MAX} limit may be calculated by using the relationship:

$$\frac{R2}{R1 + R2}(8.2V) = V\delta_{MAX}$$

The maximum duty cycle is then determined from the pulse-width modulator transfer graph, with R1 and R2 being defined from the desired conditions.

NE5561 applications

AN123

INTRODUCTION

5V, 0.5A Buck Regulator Operates From 15V

The converter design shows how simple it is to derive a TTL supply from a system supply of 15V (see Figure 1). The NE5561 drives a 2N4920 PNP transistor directly to provide switching current to the inductor. Overall line regulation is excellent and covers a range of 12V to 18V with minimal change (δ 10mV) in the output operating at full load.

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$$\frac{R2}{R1 + R2}\ (8.2V) = V\delta_{MAX}$$

The maximum duty cycle is then determined from the pulse-width modulator transfer graph, and R1, R2 are defined from the desired conditions. (See Figure 2.)

NE5561 Boost Converter With Output Variable (18V to 30V, 0.2A)

The circuit shown uses the NE5561 SMPS controller in a non-isolated boost converter operating from a 15V line. The addition of three transistors and one diode is necessary to complete the design (see Figure 3).

Operation is as follows. Q1 is a combination slow start and max duty cycle limit transistor. When power is first applied to the circuit, C7 in a discharged state begins to charge toward the divider voltage, V_δ. This $V_\delta + V_{BE}$ controls the voltage on Pin 4, the error amp output, causing the duty cycle to be limited initially to δ_0, then to gradually approach its normal operating range, δ. The base divider is fed from V_Z, which is nominally 8.2V.

Output regulation starts at the error amplifier, with gain set by R2 (adj) and R5 combination. The error amp is stable for closed loop gain in excess of 40dB (x100), for which the regulation will be approximately 1%. C4 is added to the output to insure stability at gain below 40dB. C4 creates a dominant pole at approximately 1kHz, descending at 6dB per octave to unity near 1MHz. Input to the error amplifier is referenced to 3.75V and must reach this reference level for the output of the NE5561 to be active. Output voltage is then the quantity 3.75V times the divider ratio from V_{OUT} to Pin 3 as set by R2.

If the ratio is, for instance, 10:1, the output will be ≡ 37V. If the ratio is 5:1, the output will be ≡ 18.5V, etc.

Output to Q2 base is a square wave of variable duty cycle as determined by load demand. The internal transistor is open-collector and must have a pull-up resistance; in this application the base circuit of Q2. The duty cycle δ is a fraction between 0 and 1. The actual on time is proportional then to δ × T, where T is the period of the free-running frequency of the sawtooth generator internal to the NE5561. Frequency is set by the RC combination, R7× C5 with charging current supplied from V_Z (8.2V). The stabilizing effect of the internal zener supply gives a constant frequency. The sawtooth waveform is related to duty cycle as shown below.

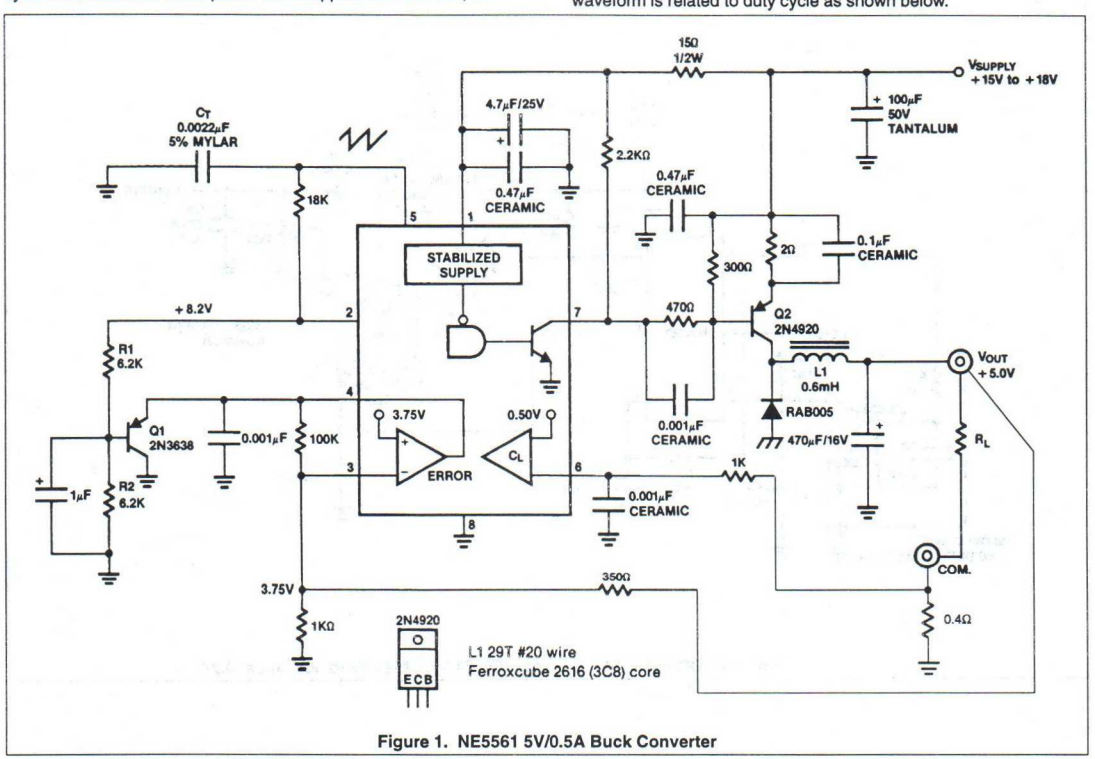


Figure 1. NE5561 5V/0.5A Buck Converter

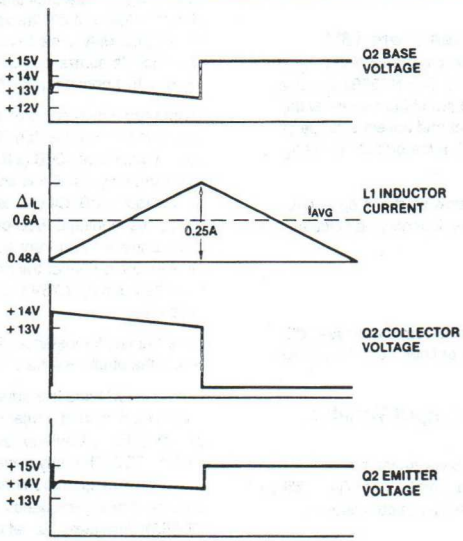


Figure 2. Typical Buck Converter Waveforms

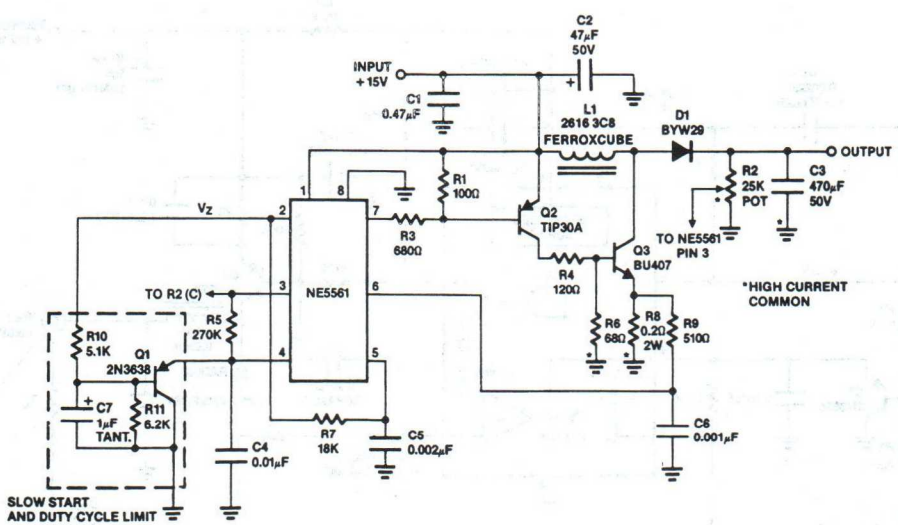
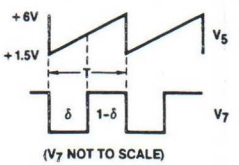


Figure 3. DC-to-DC SMPS Using NE5561 Variable 18V to 30V Out at 0.2A

Q3 is switched on during the saturated portion of the output waveform from Pin 7 of the NE5561, termed δ, and is switched off during the remainder of the cycle (1-δ).

The sawtooth frequency is set at approximately 22kHz in this example. The NE5561 is capable of operation to 100kHz, however.

Pin 6 of the NE5561 operates an overcurrent protective feature which resets the output on Pin 7 if the instantaneous Pin 6 voltage exceeds 0.50V. In this case, R8 determines the peak current of Q3 emitter circuit prior to shutdown. The operation of the overcurrent circuit is on a pulse-to-pulse basis, returning to normal as soon as the Pin 6 voltage falls below 0.50V. As is noted, a small degree of



filtering is needed to eliminate short switching transient, allowing only the primary current wave form to be sensed.

Switching circuit operation proceeds as follows. Q3 turns on, causing magnetization current to begin increasing in L1, the switching indicator. After initial start-up, C3 is charged to the output, thus with Q3 on, Diode D1 is reverse-biased and does not conduct during the duty cycle, δ. C3, the output capacitor, sustains the full load current during this part of the cycle. When Q3 turns off, the magnetic field energy previously stored in L1 is discharged through D1, which is now forward-biased. The output capacitor is incrementally charged, restoring its depleted voltage. The ripple voltage is a function of the size of C3 and its internal resistance. For minimum ripple, a low ESR (Equivalent Series Resistance) capacitor must be used, since previously-mentioned peak load current flows in C3.

Single Transistor 100V, 250mA Buck Converter (Off-Line)

With a single 15V zener diode to limit package dissipation, the NE5561 controller may be operated directly from the rectified AC line. The following example shows the simplicity of such a converter which is capable of a nominal 100V output (see Figure 5). A base drive transformer is used to gain high voltage isolation between the NE5561 and the switching transistor, and to provide adequate base drive. A low power PNP transistor is used in an auxiliary slow-start and duty cycle limiting circuit to prevent over-excitation (Q1).

Operation is as follows. Drive from the NE5561 output is fed to the primary of T1, base drive transformer, with a pulse-width modulated signal causing Q2 (BU407) to switch current to inductor, L1. As the current builds up, energy is stored in L1, coincident with the saturation period (δ) of the NE5561 output stage. During this period, current also flows through L1 to C_O and the load. When Q2 cuts off, the choke field collapses and D1 conducts as the load is sustained by the inductor-stored energy.

V_{OUT} is sampled by the divider R7 and R8, rising until the junction of the divider is forced to 3.75V. Load variations are thus translated to duty cycle variations to maintain constant voltage at the output. The measured efficiency at 0.5A load is in excess of 72%. Line regulation is good from approximately 93V to 120V.

The base current waveform driving Q2 is shown in Figure 4. This indicates that the BU407 base current rises initially to 60mA to obtain fast turn-on, then settles to about 40mA for the remainder of the duty cycle, δ. Reverse-biasing of the emitter-base junction occurs to enhance turn-off.

Snubber networks are necessary, as shown across Q2 and commutation diode D1, to prevent component failure during fast switching. It is critical that these networks be placed physically adjacent to the respective components they protect, and that low inductance capacitors and resistors be used as snubbers (ceramic or dura mica caps and carbon resistors).

The base drive transformer is constructed using a Ferroxcube 2616-3C8 core, with primary of 120 turns of #26 wire, and 20 turns of #26 on secondary. The primary is wound in a simple solenoidal manner, first on the bobbin, followed by a layer of mylar tape to provide voltage isolation. Next, the secondary winding is added. Primary inductance measures 45mH with a leakage inductance of 120μH. It is important to have sufficient primary inductance to prevent excessive droop in base drive current. Also, leakage reactance must be kept reasonably low to minimize ringing.

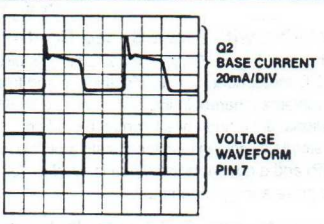


Figure 4. Switching Waveforms

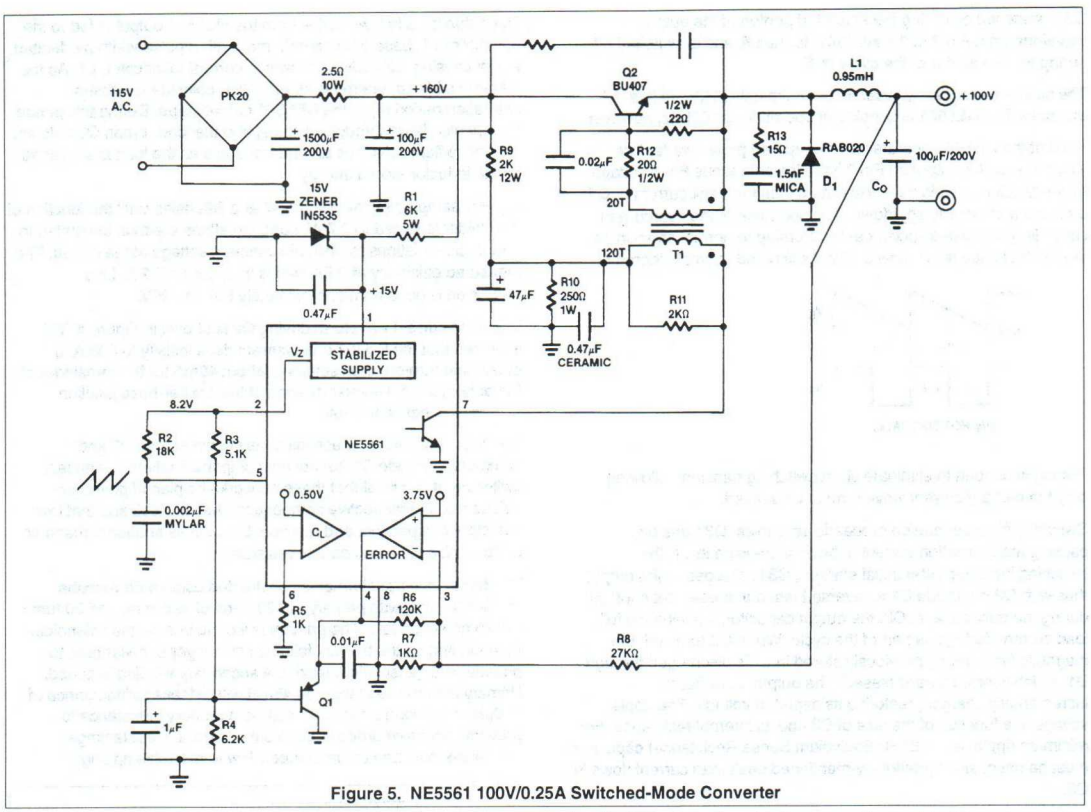


Figure 5. NE5561 100V/0.25A Switched-Mode Converter

DC Motor Drive with Fixed Speed Control

The circuit shown in Figure 7 incorporates a simple switched-mode approach to DC motor control, which is efficient and free of the dissipation problems inherent in linear drives. The NE5561 provides pulse-proportional drive and speed control based on DC tachometer feedback. A simple switching circuit consisting of one transistor (2N4920 PNP) and a commutation diode is used to deliver programmed pulse energy to the motor.

A frequency of approximately 20kHz is used to eliminate audio noise present in some switching drives. The DC tach in this example delivers 2.7V/1000 RPM. Its output is such that negative feedback occurs when this voltage is applied to the error amplifier of the NE5561, Pin 3, through a suitable divider. Note that the voltage to Pin 3 must be 3.75V in order to obtain servo lock. Thus, the divider from the tach output must be appropriate to maintain the proper ratio for speed control to occur.

As shown in the waveform pattern (Figure 6), duty cycle varies directly with load torque demand. No load current is ≅ 0.3A and full load is 0.6A. Current and voltage waveforms at 0.6A are shown in Figure 6. If desired, torque limiting may be set by feeding a derivative of motor return current back to Pin 6 of the NE5561.

Operating range is 12V to 18V input for a tach output nominal variation of less than 20mV, and approximately 4.35V for the divider values shown. The motor is a Globe 100A 565 rated at $12V_{DC}$.

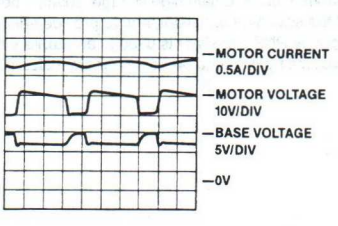


Figure 6. Switching Waveforms

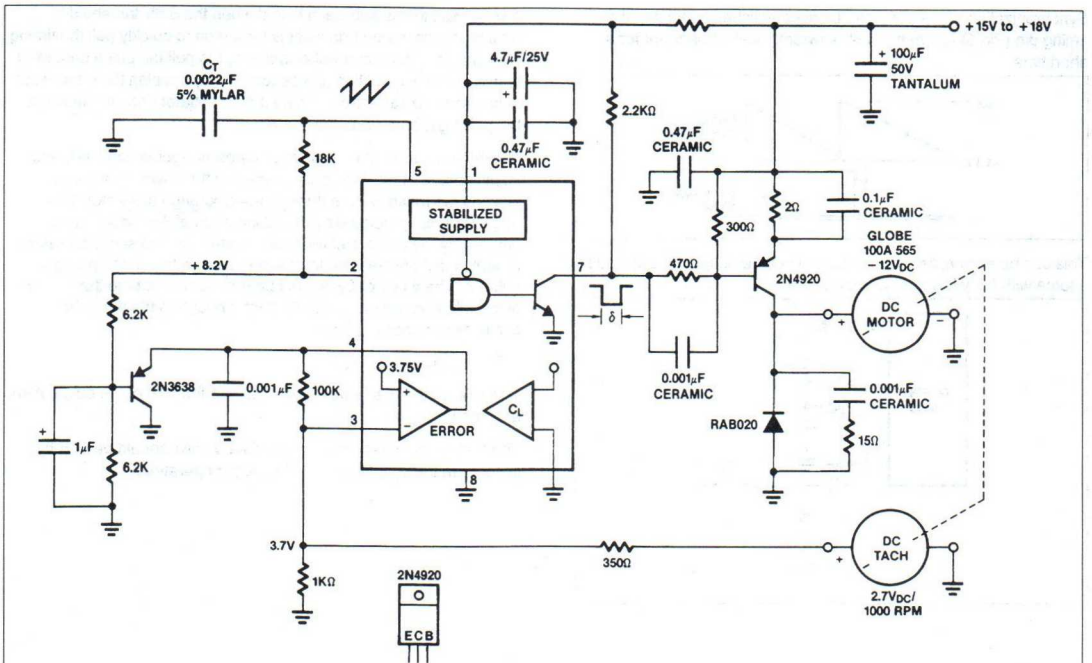
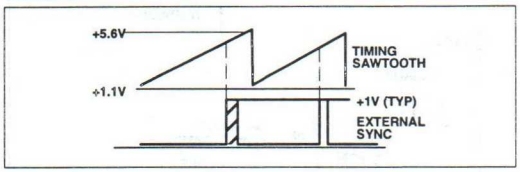


Figure 7. NE5561 Pulse-Width Modulated Motor Drive (Constant Speed)

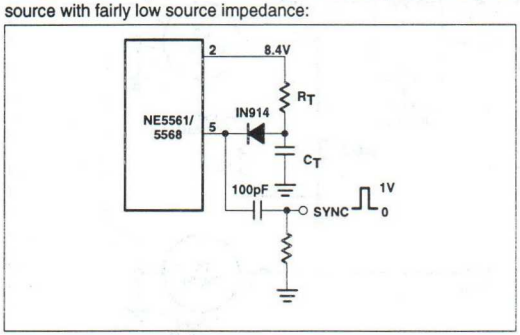
External synchronization for the NE5561/5568

AN124

Synchronization of the 5561 can be accomplished by forcing the timing pin (Pin 5) above the 5.6V sawtooth limit comparator for a short time.



This can be accomplished with a simple diode-coupled narrow pulse source with fairly low source impedance:



A drawback to this approach is that when the 5.6V threshold is reached, a discharge transistor is turned on to quickly pull the timing capacitor to ground and will also attempt to pull the pulse generator to ground. This condition can be avoided by keeping the pulse width very narrow (0.1μs) or by placing a differentiator network between the pulse generator and the diode.

The differentiator will now produce a positive-going spike with the positive edge of the sync pulse, resetting the sawtooth without passing too much current through the discharge transistor. The negative spike produced by the falling edge of the clock will be blocked by the diode and will have no effect on the sawtooth ramp. A narrow sync pulse is no longer necessary while a sharp-edged pulse is. The value of C_D should be sufficient to ensure that a 10V pulse will drive the capacitor, C_T, high enough to trip the 5.6V comparator according to:

$$C_T \Delta V_{CT} = C_D(\Delta V_{CT} - V_D)$$

This relates the magnitude of the spike to the size of the pulse. Also assume $R_D C_D < 1\mu s$.

The free-running frequency of the slaved 5561 should be slightly lower than the sync frequency for proper operation.

Switched-mode power supply control circuit — NE/SE5562

DESCRIPTION

The NE/SE5562 is a single-output control circuit for switched-mode power supplies. This single monolithic IC contains all control and protection features needed for full-featured switched-mode power supplies.

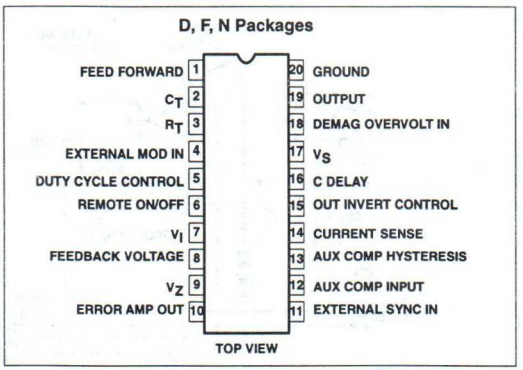
The 100mA source/sink output is designed to drive power FETs directly. The associated output logic is designed to prevent double pulsing or cross-conduction current spiking on the output.

All of the control and protect features work cycle-by-cycle up to the maximum operating frequency of 600kHz.

For ease of interface, all digital inputs are TTL or CMOS compatible.

The NE5562 is supplied in 20-pin glass/ceramic (Cerdip), plastic DIP, and plastic SO packages. The NE grade part is characterized and guaranteed over the commercial ambient temperature range of 0°C to +70°C and junction temperature range of 0°C to +85°C. The SE5562 is supplied in the glass/ceramic (Cerdip) package. The SE grade part is characterized and guaranteed over the ambient temperature range of -55 to +125°C and junction temperature range of -55 to +135°C.

PIN CONFIGURATION



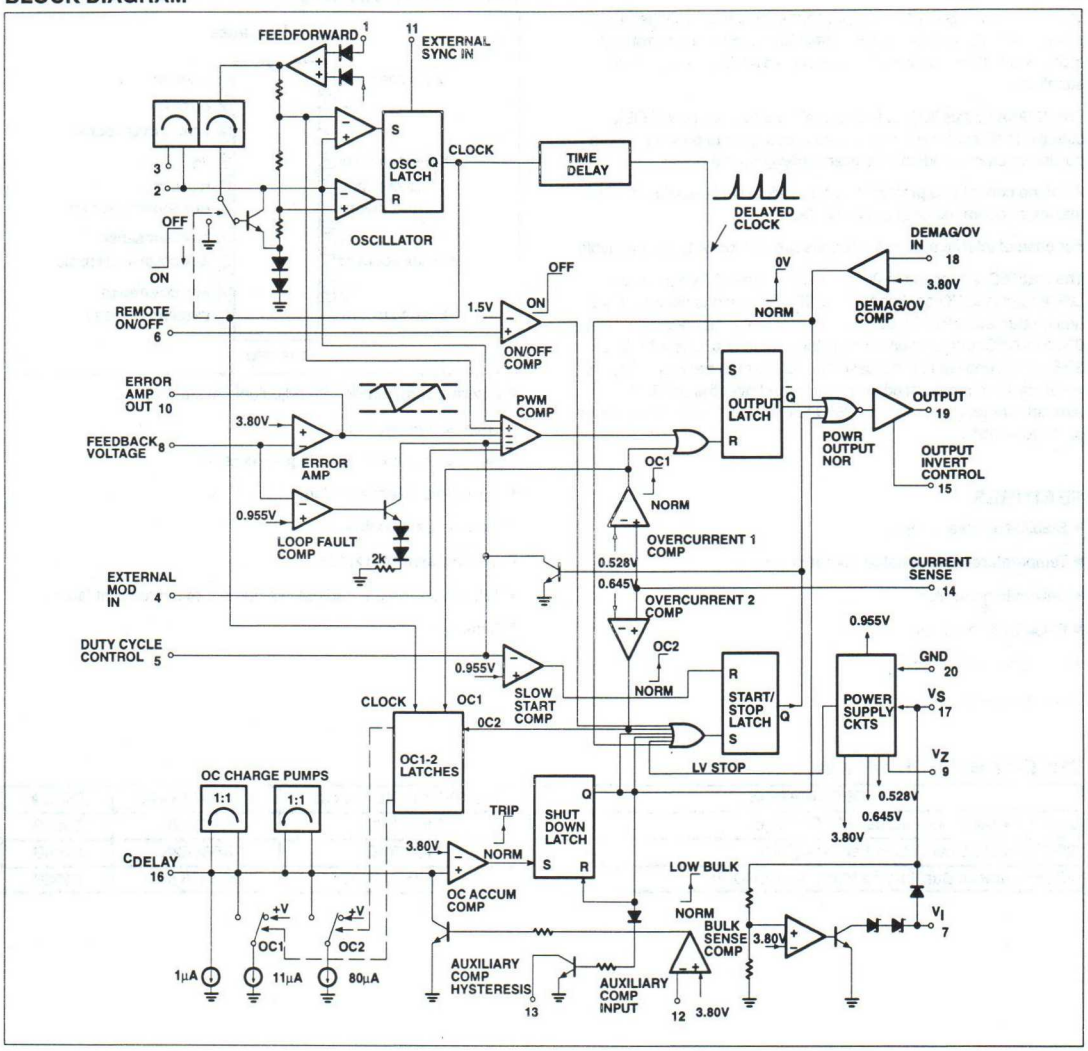
FEATURES

- Stabilized power supply
- Temperature-compensated reference source
- Sawtooth generator
- Pulse width modulator
- Remote on/off switching
- Current limiting (2 levels)
- Auxiliary comparator, with adjustable hysteresis
- Loop fault protection
- Demagnetization/overvoltage protection
- Duty cycle adjust and clamp
- Feed-forward control
- External synchronization
- Total shutdown after adjustable number of overcurrent faults
- Soft-start

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE5562D	1021B
20-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5562N	0408B
20-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE5562F	0408B

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply		
V_S	voltage-fed mode (Pin 17)	16	V
I_{CC}	current-fed mode (Pin 7)	30	mA
	Output transistor output current	100	mA
	Sync (Pin 11)	V_S	V
	Duty cycle control (Pin 5)	V_Z	V
	Remote on/off (Pin 6)	V_S	V
	Output invert control (Pin 15)	V_S	V
	Feedback pin (Pin 8)	V_Z	V
	C_{DELAY} (Pin 16)	V_Z	V
	External mod in (Pin 4)	V_S	V
FF	Feed-forward (Pin 1)	V_S	V
	Demag/overvoltage in (Pin 18)	V_Z	V
	Current sense (Pin 14)	V_S	V
	80Low supply sense and hysteresis (Pins 12, 13)	V_S	V
T_J	Operating junction temperature	135	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec)	300	°C

NOTES:
1. Ground Pin 20 must always be the most negative pin.
2. For power dissipation, see the application section which follows.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
	Supply		
	voltage-fed	10 to 16	V
	current-fed	15	mA
T_A	Ambient temperature range		
	NE grade	0 to +70	°C
	SE grade	-55 to +125	°C
T_J	Junction temperature range		
	NE grade	0 to +85	°C
	SE grade	-55 to +135	°C

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, specifications apply over temperature, unless otherwise specified.

SYMBOL	PARAMETER	TEST PINS	TEST CONDITIONS	SE5562			NE5562			UNIT
				Min	Typ	Max	Min	Typ	Max	
Internal reference										
V_{REF}	Reference voltage	Internal	T_A=25°C	3.76	3.80	3.84	3.76	3.80	3.84	V
V_{REF}	Reference voltage	Internal	Over temp.	3.72	3.8	3.90	3.725	3.8	3.870	V
	Temperature stability	Internal			30			30		ppm/°C
	Long-term stability	Internal			0.5			0.5		µV/1000 hrs

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 12V, specifications apply over temperature, unless otherwise specified.

SYMBOL	PARAMETER	TEST PINS	TEST CONDITIONS	SE5562			NE5562			UNIT
				Min	Typ	Max	Min	Typ	Max	
Reference										
V_Z	Zener voltage	9	I_L=7mA, T_A=25°C	7.35	7.60	7.75	7.35	7.6	7.75	V
V_Z	Zener voltage	9	I_L=7mA, Over temp.	7.25		7.80	7.20		7.78	V
$\Delta V_Z/\Delta T$	Temperature stability	9	I_L<1mA		50			50		ppm/°C
Low supply shutdown										
	Comparator threshold voltage	Internal	T_A=25°C	8.30	8.45	8.75	8.30	8.45	8.75	V
	Comparator threshold voltage	Internal	Over temp.	8.00	8.45	8.90	8.00	8.45	8.90	V
	Hysteresis	Internal		25	50	8.00	25	50	800	mV
Oscillator										
f_{MIN}	Frequency range, minimum	1, 2, 3, 11	R_T=42.7kΩ, C_T=0.47µF		60	80		60	80	Hz
f_{MAX}	Frequency range, maximum	1, 2, 3, 11	R_T=2.87kΩ, C_T=380pF	600			600			kHz
	Initial accuracy	1, 2, 3, 11	f_O=52kHz, R_T=16kΩ and C_T=0.0015µF, T_A=25°C	48.6	54	59.4	48.6	54	59.4	kHz
	Voltage stability	1, 2, 3, 11, 17	10V<V_S<18V		-215			-215		ppm/V
	Temperature stability	1, 2, 3, 11			300	500		300	500	ppm/°C
	Sawtooth peak voltage	2, 3	T_A=25°C[1]	5.00	5.25	5.40	5.00	5.25	5.40	V
		2, 3	Over temp.	4.80	5.25	5.60	4.80	5.25	5.60	V
	Sawtooth valley voltage	2, 3	T_A=25°C	1.25	1.70	2.00	1.25	1.70	2.00	V
		2, 3	Over temp.	1.0	1.7	2.1	1.25	1.7	2.0	V
	Sync. in high level	11		2.0		V_Z	2.0		V_Z	V
	Sync. in low level	11		0.0		0.8	0.0		0.8	V
	Sync. in bias current	11	(Sourced), V_{11}<0.8V		0.50	10.0		0.50	10.0	µA
	Feed-forward ratio, maximum	1			2			2		
	Feed-forward duty cycle reduction	1	V_{FF}=2V_Z, T_A=25°C	11	13.5	19	11	13.5	19	%
		1	Over temp.	6	13.5	22	8		22	%
	Feed-forward reference voltage	9			V_Z	V_S		V_Z	V_S	V
	Feed-forward bias current	1			2.5	50.0		2.5	50.0	µA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 12V, specifications apply over temperature, unless otherwise specified.

SYMBOL	PARAMETER	TEST PINS	TEST CONDITIONS	SE5562			NE5562			UNIT
				Min	Typ	Max	Min	Typ	Max	
Error amp										
I_{BIAS}	Input bias current	8			1.0	5.0		1.0	5.0	µA
A_{VOL}	DC open-loop gain	8, 10	R_L>100kΩ	60	86		60	86		dB
V_{OH}	High output voltage	10	I_{SOURCE}=1mA	5			5			V
V_{OL}	Low output voltage	10	I_{SINK}=1mA			2.0			2.0	V
	PSRR from V_Z and V_S	Internal	f_O<300kHz		-40			-40		dB
BW	Small-signal gain bandwidth product				8			8		MHz
	Feedback resistor range			1		240	1		240	kΩ
I_{SINK}	Output sink current		V8=V10=5V			10			10	mA
I_{SOURCE}	Output source current		V8=3V, V10=1V			5			5	mA
	Sawtooth feedthrough		A_V=100, 0% duty cycle		200			200		mV
PWM comparator and modulator										
	Minimum duty cycle	19	@V_{COMP}<, f=300kHz	0			0			%
	Maximum duty cycle	19	@V_{COMP}>, f=300kHz, V15=0V	95		98	95		98	%
A_{CC}	Duty cycle	10, 19	f=15kHz to 200kHz, V_{IN}=0.472 V_Z	41	49	55	41	49	55	%
t_{PD}	Propagation delay to output	2, 19	V_{15}=0		400			400		ns
I_{BIAS}	Bias current, external modulator input	4	(Sourced)		0.20	20		0.20	20	µA
I_{BIAS}	Bias current, duty cycle control	5	(Sourced)		0.20	20		0.20	20	µA
	Soft-start trip voltage	5		.910	0.955	0.990	0.922	0.955	0.988	V
Remote on/off (shutdown)										
	Output enabled	6		0		0.80	0		0.80	V
	Output disabled	6		2		V_Z	2		V_Z	V
I_{BIAS}	Bias current	6			1	10		1	10	µA
V_{IN}	Maximum input voltage	6		V_Z			V_Z			V
	Delay to output(s)	6, 19			400			400		ns
Current limit comparator(s)										
	Shutdown, OC2	14		.593	0.645	.697	0.593	0.645	0.697	V
	Minimum duty cycle, OC1	14		.486	0.528	.570	0.486	0.528	0.570	V
I_{BIAS}	Bias current	14	(Sourced)		0.5	50		0.5	50	µA
OC_1	C_{DELAY} charge current	16		-18.2	-13	-6.5	-18.2	-13	-7.8	µA
OC2	C_{DELAY} charge current	16		-770	-550	-250	-770	-550	-330	µA
C_{DELAY}	Discharge current	16	V12=V_Z	0.4	1.4	4.0	0.8	1.4	2.0	µA
C_{DELAY}	Shut off trip level	16	T_A=25°C	3.75	3.86	3.97	3.75	3.86	3.97	V

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 12V, specifications apply over temperature, unless otherwise specified.

SYMBOL	PARAMETER	TEST PINS	TEST CONDITIONS	SE5562			NE5562			UNIT
				Min	Typ	Max	Min	Typ	Max	
Auxiliary comparator with shutdown										
I_{BIAS}	Bias current	12	(Sourced)		1	10		1	10	µA
	Threshold voltage	12		3.69	3.80	3.91	3.69	3.80	3.91	V
C_{DELAY}	Discharge current	12	V_{IN}=3V	5	10		5	10		mA
	Hysteresis	12, 13			10			10		mV
Demagnetization overvoltage comparator										
I_{BIAS}	Bias current	18			2	10		2	10	µA
	Threshold voltage	18		3.62	3.80	3.91	3.69	3.80	3.91	V
	Hysteresis	18			10			10		mV
Output stage										
V_{OH}	High output voltage	19	I_{SOURCE}=100mA	V_S-2.5	V_S-1.9		V_S-2.5	V_S-1.9		V
V_{OL}	Low output voltage	19	I_{SINK}=2mA		0.16	0.4		0.16	0.4	V
		19	I_{SINK}=100mA, T_A=25°C		1.4	2.0		1.4	2.0	V
		19	I_{SINK}=100mA, over temp.			2.25			2.25	V
	I_{SINK} max	19		100			100			mA
	I_{SOURCE} max	19		100			100			mA
t_R	Rise time	19	C_L=2000pF		160			160		ns
t_F	Fall time	19	C_L=2000pF		80			80		ns
Supply current/voltage										
I_{CC}	Supply current	17	10V<V_S<16V (Voltage-fed mode), V_I<V_S		9	15		9	15	mA
V_S	Input voltage	7, 17	I_I=15mA, (Current-fed mode) V_S=meter	14.2	15.3	16.7	14.2	15.3	16.7	V
Operating frequency range for all functions but feed-forward working cycle-by-cycle										
f_{MIN}	Minimum frequency	All	R_T=42.7kΩ, C_T=0.47µF		60	80		60	80	Hz
f_{MAX}	Maximum frequency	All	R_T=2.87kΩ, C_T=380pF	600	1000		600	1000		kHz

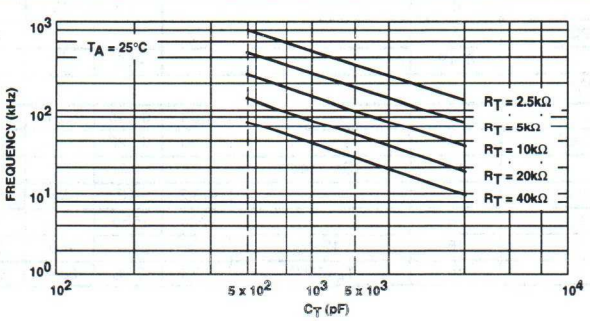


Figure 1. Frequency vs R_T, C_T NE/SE5562

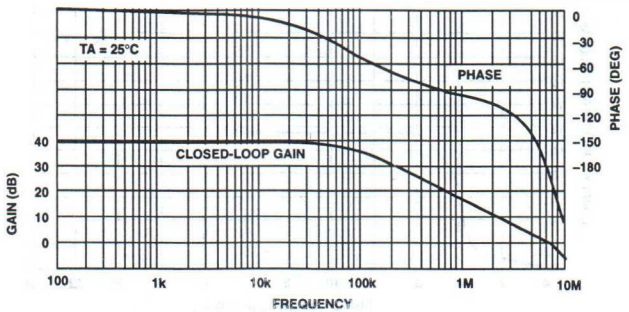


Figure 2. Error Amplifier Closed-Loop Response

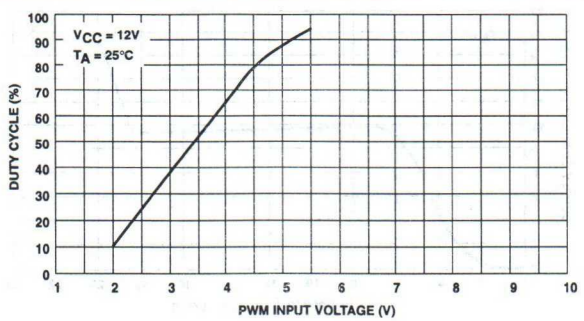


Figure 3. Duty Cycle vs PWM Input Voltage

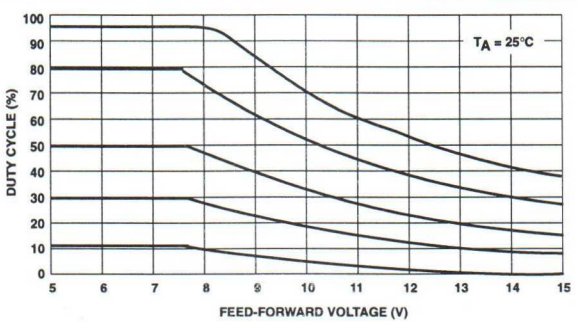


Figure 4. Duty Cycle vs Feed-forward Voltage

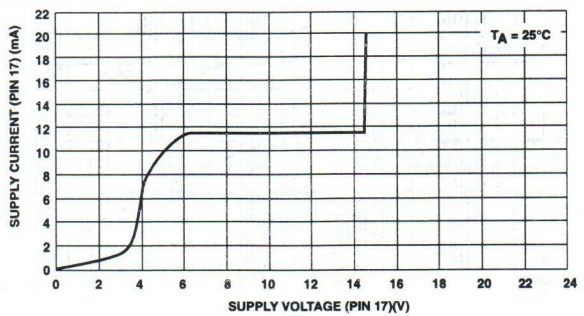


Figure 5. Current-Feed Characteristics

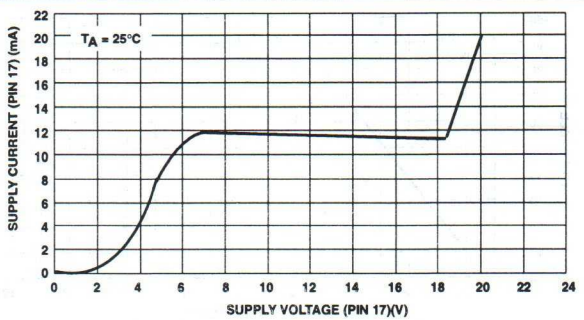


Figure 6. Voltage-Feed Characteristics

THE NE/SE5562 THEORY OF OPERATION

INTRODUCTION

Switched-mode power conversion relies on the principle of pulsed energy storage in an inductive or capacitive element. Capacitive switched converters are typically used with low power systems for which only tens of milliamperes are required. Medium and high power converters tend to use inductive storage elements as shown in Figures 7-9 with which a single switch may be moved around to create step-up (flyback) positive or negative polarity and step-down (forward or buck) conversion from a fixed-voltage source. The relationship between input and output voltage in each case is controlled by the switching on-to-off ratios, which is termed duty cycle. Duty cycle modulation is the common factor in this basic type of power control mechanism. By adding a high-gain operational amplifier, having one input tied to a stable DC reference voltage, configured in a negative feedback loop to maintain a constant output voltage as shown in Figure 10, the switched-mode controller becomes a dynamic voltage regulator. It is this single-switch topology that is most readily adapted to the NE/SE5562 SMPS Control IC.

The ability to switch inductor currents at rates up to 600kHz with state-of-the-art power FETs makes the design of small, efficient switching power converters an attainable reality. Protective features such as programmable slow-start and cycle-by-cycle current limiting allow safe, maintenance-free power supplies to be mass-produced at reduced cost to the manufacturer. Integrated technology makes long-term reliability a predictably achievable goal.

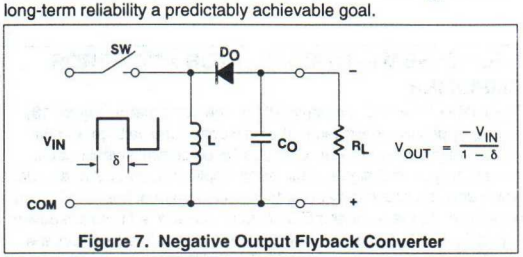


Figure 7. Negative Output Flyback Converter

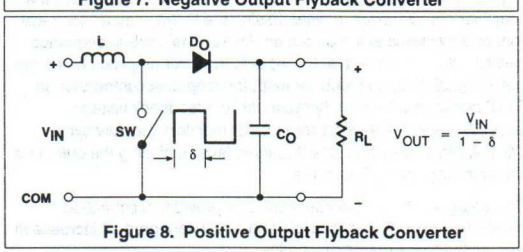


Figure 8. Positive Output Flyback Converter

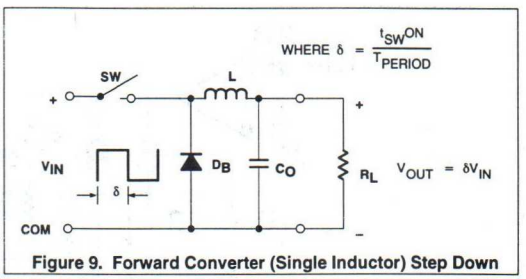


Figure 9. Forward Converter (Single Inductor) Step Down

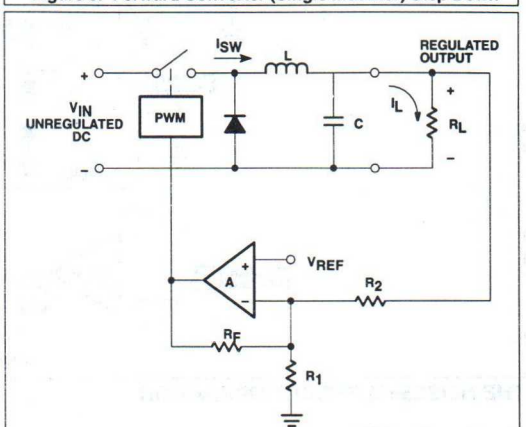


Figure 10. The Forward (Buck) Converter ($V_{OUT} = V_{IN}(\delta)$)

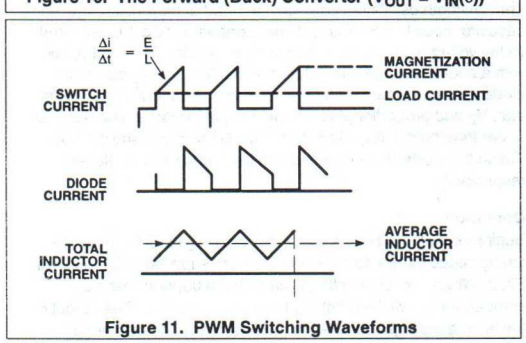


Figure 11. PWM Switching Waveforms

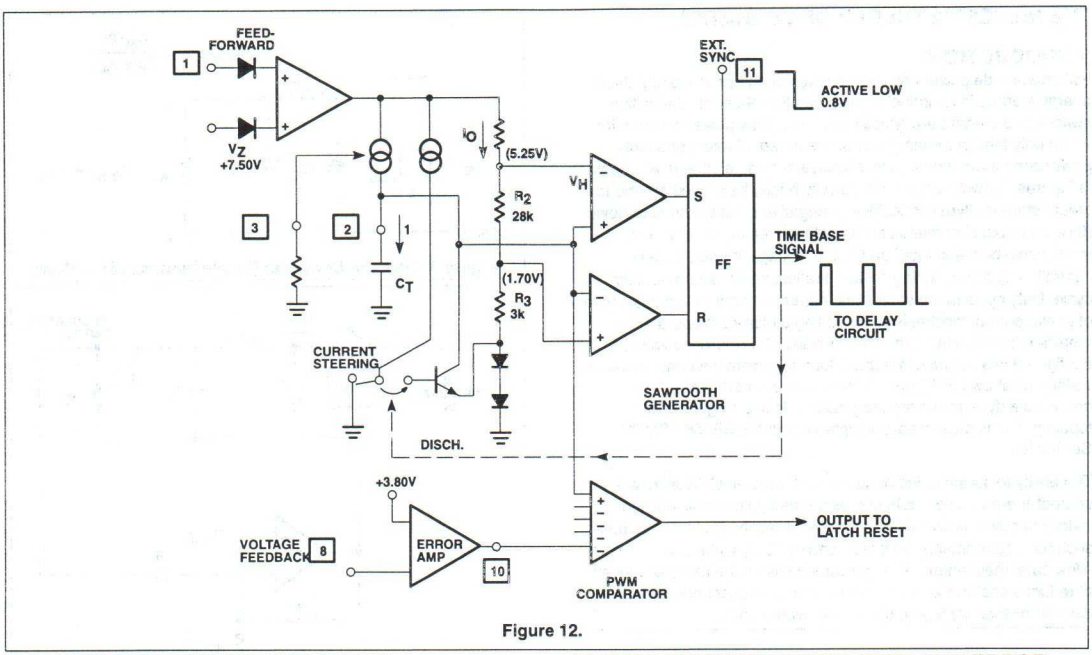


Figure 12.

THE NE/SE5562 THEORY OPERATION

The Sawtooth Oscillator

The sawtooth oscillator consists of a gated charge-discharge capacitor circuit with threshold comparators setting the peak and valley voltages of the ramp. The resistor divider R1-3 is supplied with a source voltage derived from either V_Z (7.50V) minus two diode drops, or, when feed-forward is in control, a voltage greater than V_Z and proportional to the main supply voltage. The nominal upper threshold voltage is 5.25V and the lower threshold 1.70V. These then determine the sawtooth peak and valley voltages, respectively.

Operation

Beginning with the charge cycle, ramp voltage builds up on the timing capacitor due to a constant current supplied to the node at Pin 2. When capacitor voltage reaches the upper threshold, comparator A switches, setting the latching flip-flop. The output of the latch goes high, generating a clock pulse. The discharge transistor is simultaneously turned on, reducing charge on the timing capacitor to the point at which the lower threshold voltage, 1.70V, is reached. The lower comparator is then activated, resetting the latch and terminating the clock pulse. Note that the discharge transistor is referenced to the same return diodes as the threshold resistor divider and the discharge current is made to track with the charge current. This charge and discharge tracking results in a true sawtooth waveform even at extended frequencies. Figure 15 shows a family of curves which explains the relationship between R_T, C_T, and the frequency of the sawtooth generator. The data sheet shows the initial accuracy of the oscillator at 60Hz and 600kHz.

THE PULSE WIDTH MODULATOR AND ERROR AMPLIFIER

The PWM consists of a multi-input voltage comparator (Figure 13) having its positive input tied to the sawtooth ramp voltage and the various negative inputs referenced to ORed control signal nodes. The primary control signal is the error amplifier output voltage node which sets the active duty cycle termination point of the PWM output waveform. As the error amplifier input signal derived from the power supply load voltage varies, for instance in a negative direction, the amplifier output moves upward, raising the PWM comparator toward longer duty cycles at the output on Pin 19. The start-up sequence begins with zero voltage at the input to the error amplifier. Since this could signal an open feedback loop, the loop fault comparator on Pin 8 clamps the PWM duty cycle until the feedback voltage exceeds 0.955V. A second comparator monitors the duty cycle control, Pin 5, with the same threshold level, inhibiting the output via the start-stop latch (Figure 14).

The charging of the slow-start capacitor provides a controlled ramp-up of the output duty cycle and a resultant gradual increase in energy fed to the output magnetics.

The dynamic response of the PWM comparator is shown in the simulated waveform drawing of Figure 15. The error amplifier output voltage is depicted as sloping positive (increasing) with time as referenced to the sawtooth waveform. This causes the duty cycle to increase with time. This is an indication of an increasing load on the power supply as output voltage is decreasing. The Pin 5 (δ_{MAX}) control voltage is also superimposed midway on the sawtooth, indicating the limits of duty cycle increase as the output waveform no longer increases in duty cycle after the δ_{MAX} threshold is crossed. A hypothetical overcurrent pulse (Pin 14) is shown to illustrate cycle termination immediately at the output (Pin 19).

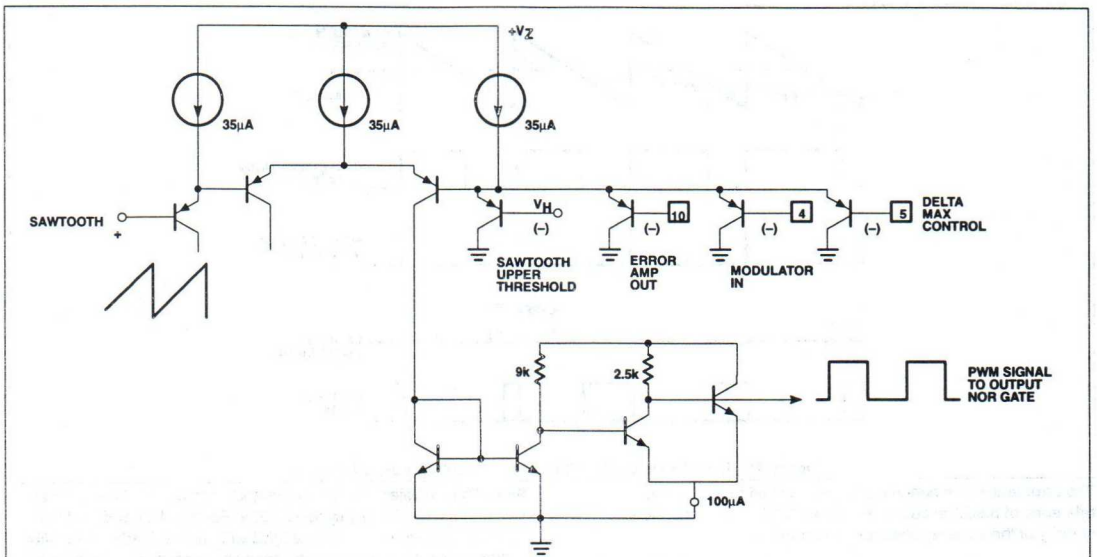


Figure 13. PWM Comparator

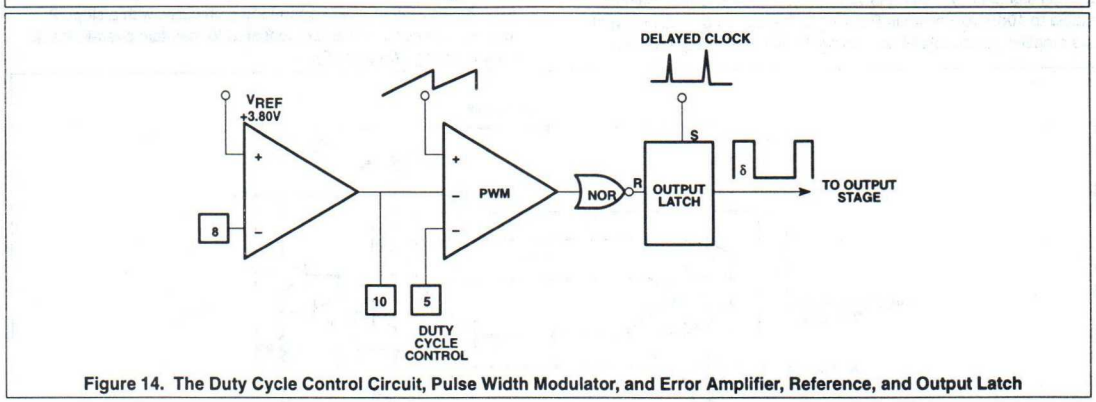


Figure 14. The Duty Cycle Control Circuit, Pulse Width Modulator, and Error Amplifier, Reference, and Output Latch

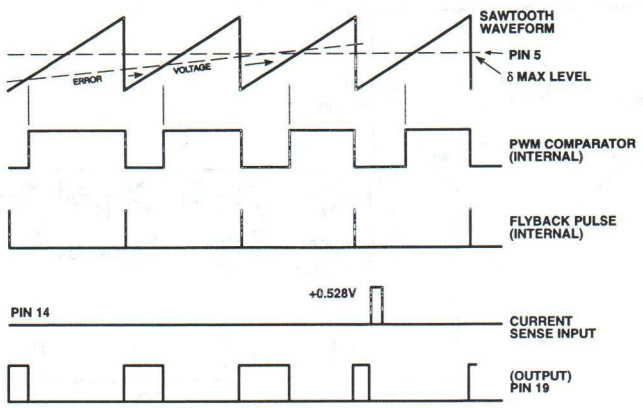


Figure 15. Duty Cycle vs Feedback Error and Overcurrent Sense

The error amplifier's non-inverting input is tied to a bandgap reference of 3.80V, accurate to ±2% at 25°C. The temperature stability of the voltage reference is 30ppm/°C.

The error amplifier is designed for an open-loop gain of 86dB having a small-signal unity gain bandwidth of 3MHz. Closed-loop gain is stable to 10dB, as shown in Figure 17. The DC output excursion of the amplifier is capable of controlling the full PWM range of 0 to 95%. The amplifier can sink 10mA and source 5mA. The nominal DC output for 50% duty cycle is 3.55V. Feedback control resistor value may range from 1kΩ to 240kΩ without overload or instability. However, low closed-loop gains must be compensated by lag lead network techniques for optimum stability. Loop compensation networks may intersect the open-loop gain curve with a slope 2 closure and must then be compensated to maintain overall phase and gain margin (Figure 16).

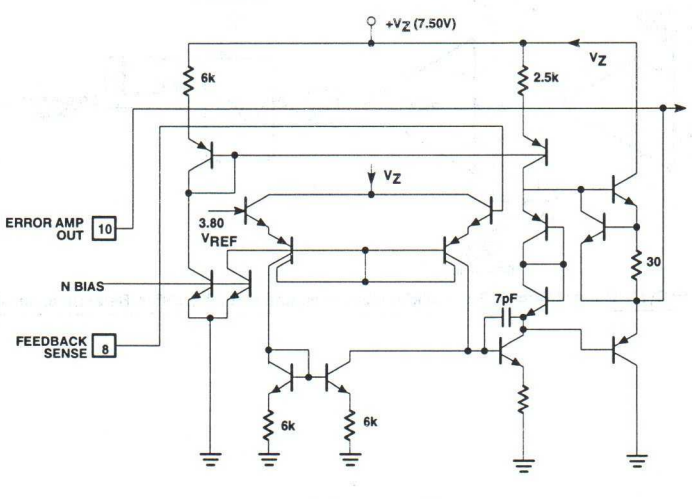


Figure 16. Error Amplifier

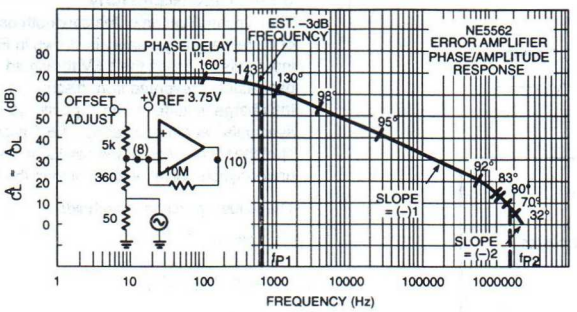


Figure 17. Error Amp Response

FEED-FORWARD COMPENSATION (PIN 1)

To provide a means of automatically improving line-to-load voltage regulation, a technique called feed-forward regulation is made a part of the NE/SE5562 active mechanism. Referring back to the diagram for the sawtooth oscillator, note that Pin 1 is capable of changing the internal supply voltage to the charging circuit for the timing capacitor, C_t.

With a nominal duty cycle of 30%, for instance, increasing Pin 1 voltage by 1V from 10.3 to 11.3 will reduce the output duty cycle by approximately 5%. Thus, a primary voltage change has caused a decrease in volt-seconds (duty cycle X primary volts) of 5/30 or 16% (Figure 4). The result is a small over-compensation in the output energy, but an overall safe margin in transformer flux.

The mechanism which produces inverse duty cycle modulation is shown in Figure 18. Increasing Pin 1 voltage beyond the value of V_Z (7.50V) increases the charge rate on C_T, causing the duty cycle to be terminated earlier for each cycle that input voltage is increased. The threshold voltages at the sawtooth limit comparator reference inputs are changed with Pin 1 also in order to offset any change in oscillator frequency.

The secondary benefit of using feed-forward is the attenuation of any low-frequency AC riding on the DC supply before it reaches the regulated output.

Note that a start delay circuit is added to the Pin 1 divider in order to prevent internal race conditions during initial power-up. Once the turn-on transient has decayed, normal operation of the feed-forward circuit is assured. Figure 19 shows an RC delay placed in a base clamping circuit to provide reliable starting.

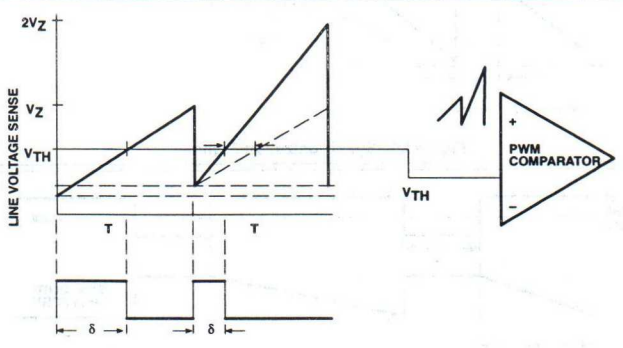


Figure 18. Feed-Forward

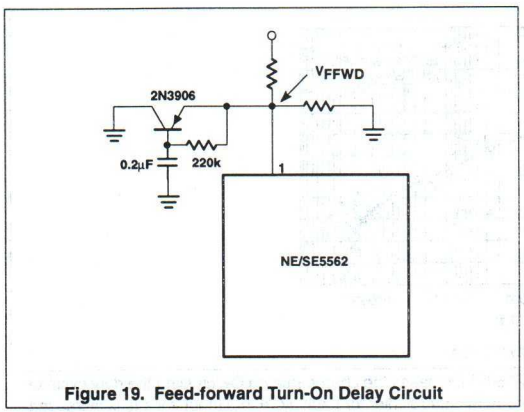


Figure 19. Feed-forward Turn-On Delay Circuit

SYNCHRONIZATION

The synchronization of the sawtooth oscillator to an external pulse of negative-going polarity is shown in Figure 20. When the sync input pulse crosses the 1.5V threshold, negative, the sawtooth oscillator is prevented from discharging the timing capacitor, causing the charge voltage on the capacitor to remain high (5.25V) until the sync pulse again goes above 1.5V, allowing reset. This action stretches the period of the oscillator and results in a lower frequency under-synchronization control than the free-running frequency.

The following relationship holds—

$$f_{free-run} > f_{sync}$$

$$f_{sync} = \frac{1}{t_0 + \tau}$$

A typical recommended starting point in calculating frequency for synchronous operation is to set the free-run frequency approximately 10% higher than the sync frequency. Then set the pulse width, τ, to 10% of t_0, the free-run period, with the desired new frequency determined by the sum as above.

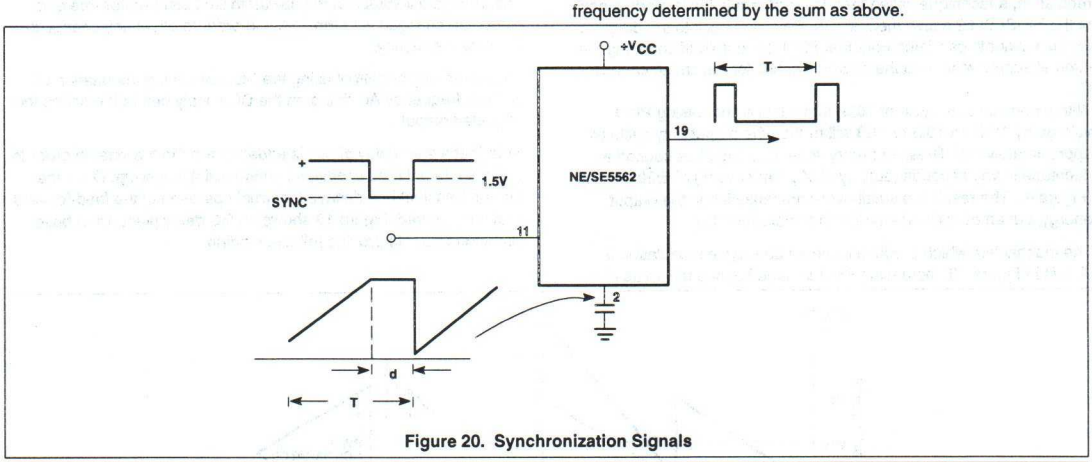


Figure 20. Synchronization Signals

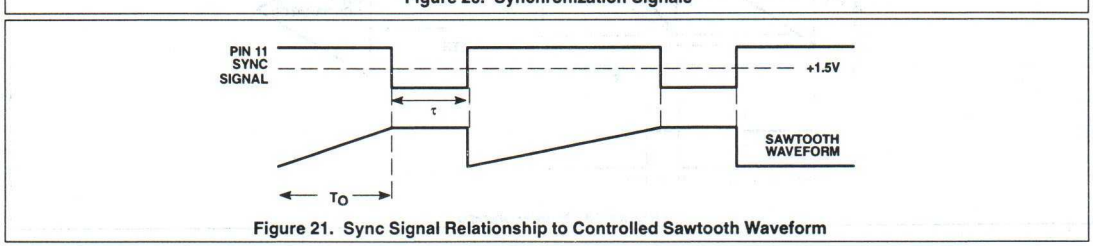


Figure 21. Sync Signal Relationship to Controlled Sawtooth Waveform

DUTY CYCLE LIMIT (PIN 5)

The forward or buck converter, and even the flyback converters, may require an automatic duty cycle limit to prevent transformer saturation or unstable behavior. A special input provides access to the PWM comparator for this purpose. As discussed previously in regard to the error amplifier, increasing load demand may drive the system current beyond safe limits. A simple solution is the placement of a duty cycle limit within the system dynamic response before this can occur. Figure 13 shows the PWM comparator with its multiple input ports. All are inverting in polarity and provide a lowest priority level sensing circuit. The lowest level on Pin 4, 5, or 10 gains control of the duty cycle limit. During normal operation, the δ_{MAX} circuit sends a continuous threshold signal to the PWM comparator, setting a fixed limit on how much the error amplifier is allowed to increase the duty cycle in response to load demand. Figure 22 shows the circuit within the NE/SE5562 which actually controls duty cycle as listed below:

1. Duty cycle ramp-up (slow-start) during power-up. Time constant controlled by external R, C ramp voltage at Pin 5.
2. Slow-start if remote ON/OFF is actuated, if OC2 threshold trips, demagnetization/overvoltage is sensed, or low supply voltage to the internal regulator is sensed (VS≤8.45V).

3. Note that Pin 8 is monitored by the loop fault comparator. When the regulated supply feedback drops below this threshold level (0.955V), the duty cycle is clamped by two diodes in series with a 2kΩ load across Pin 5 to ground. This implies a minimum duty cycle condition as long as the low output level remains.

Referring to the graph in Figure 23, the designer may choose a divider ratio which, when referenced to V_Z, 7.5V, provides an easy duty cycle limit control. For example, a 50% limit results in a ratio of 0.48. Setting R_2 at a nominal value between 10 and 20kΩ and solving for R_1, the proper limit is obtained.

Example:

A duty cycle limit of 50% is required for a forward converter.

$R_2 = 10k\Omega$, find R_1

$$\frac{R_2}{R_1 + R_2} = 0.48$$

$$\therefore R_2 = 0.48 (R_1 + R_2)$$

$$0.48R_1 = R_2 - 0.48R_2$$

$$\therefore R_1 = \frac{R_2(1 - 0.48)}{0.48}$$

$$= \frac{10k\Omega\ (0.52)}{0.48}$$

$$= 10.8k\Omega$$

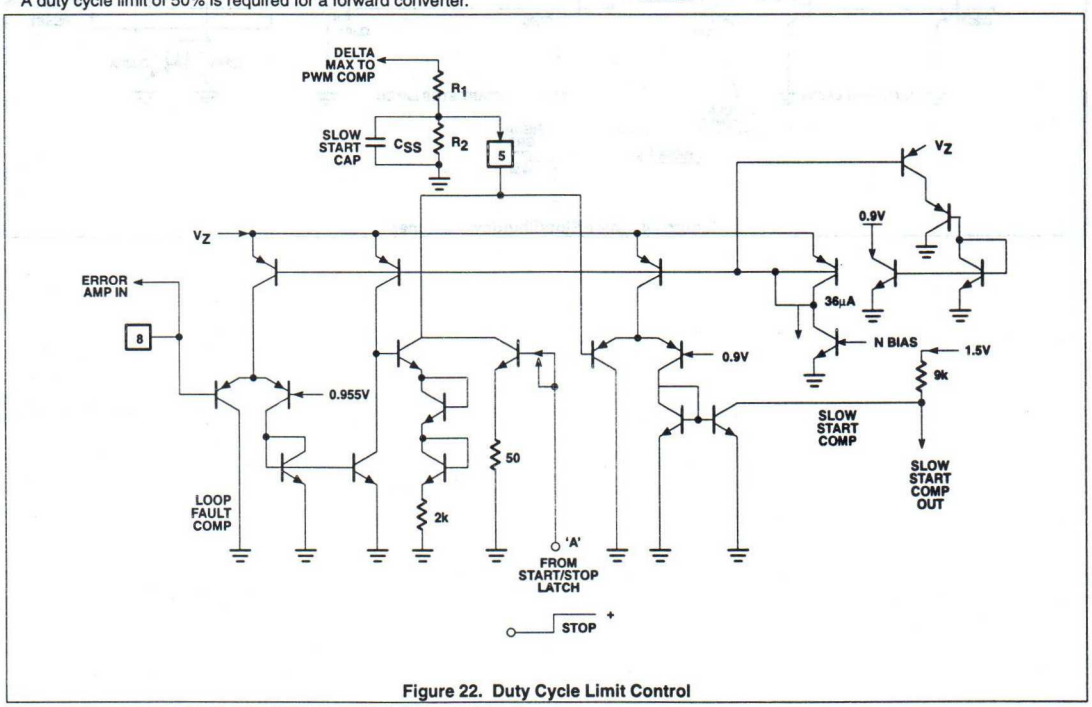


Figure 22. Duty Cycle Limit Control

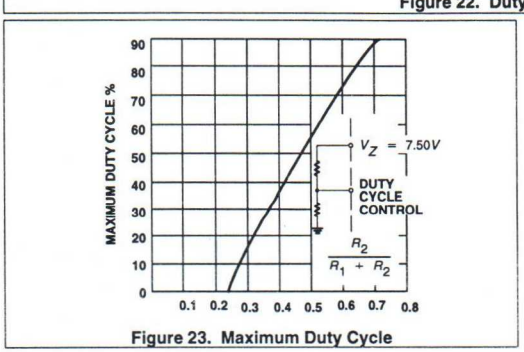


Figure 23. Maximum Duty Cycle

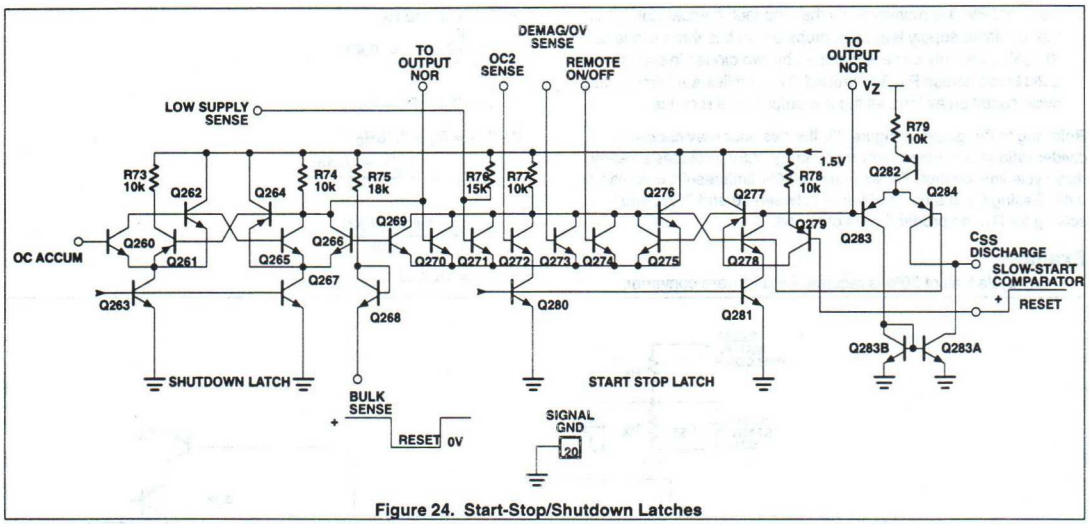


Figure 24. Start-Stop/Shutdown Latches

THE START-STOP CONTROL SEQUENCE

The start-up circuit involves a sequential set of conditions which progresses as follows: power-up after OFF condition or remote ON after OFF. Initially, 0V exist on the supply output, causing zero feedback volts on Pin 8. The slow-start capacitor is discharged, forcing Pin 5 to 0V, having been clamped by the internal discharge transistor. Internal supply regulator input exceeds 8.45V, releasing low voltage shutdown condition with Pin 5 below 0.955V. The slow-start comparator output goes high, resetting the start/stop latch, sending a low output signal to the output stage power NOR gate. The PWM signal is then enabled to feed the output drive circuits, starting energy flow through the magnetics. However, instantaneously the power supply output is still below 0.955V and the loop fault comparator forces the PWM to remain at a minimum duty cycle. The equivalent circuit at this instant in the start-up cycle which exists at Pin 5 is shown in Figure 26.

The actual minimum duty cycle is determined by the parallel source resistance of R_1 and R_2 combined with the shunt loading internal to Pin 5. High values of divider resistance, 20-30kΩ, will supply less shunt current to Pin 5 and create a lower modulator duty cycle, while lower values of R_1 and R_2 (5-10kΩ) will generate a higher modulator voltage and a greater resultant minimum duty cycle.

As the power conversion circuits become active and Pin 8 feedback voltage increases above 0.955V, the duty cycle network is unclamped; duty cycle increases, controlled by the RC time constant $R_1 \| R_2 . C_{SS}$, and as output voltage brings the feedback voltage up to equal the reference voltage, 3.80V, the error amplifier takes control and the supply is in regulation.

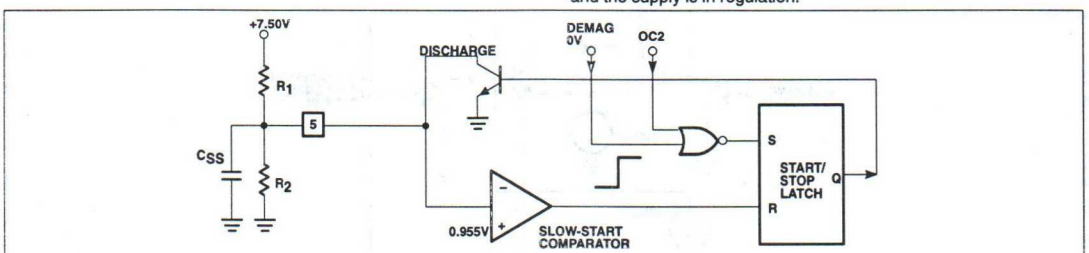


Figure 25. Slow-Start Comparator

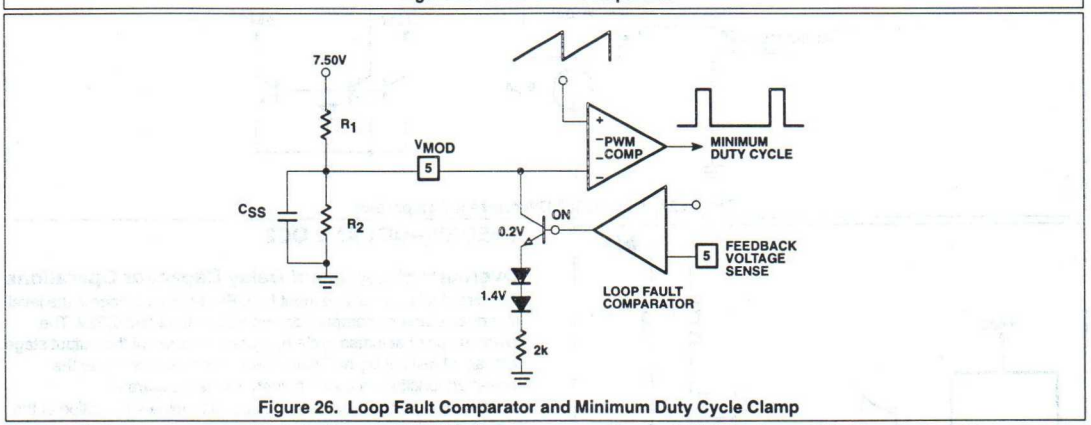


Figure 26. Loop Fault Comparator and Minimum Duty Cycle Clamp

The stop or shutdown sequence is initiated by any of the following conditions:

a. Supply voltage (bulk) sense below 3.80V at Pin 12.

b. Pin 17 below 8.45V or Pin 7 current below level (less than 9mA).

c. Remote ON/OFF voltage at Pin 6 greater than 2V.

d. Sustained OC2 causing C_{DLY} to charge above 3.80V (current sense on Pin 14 continuously above 0.645V peak).

DUAL-LEVEL OVERCURRENT COMPARATORS

The overcurrent sensing circuit (Figure 27) consists of a single PNP input buffer with emitter-follower tied to V_Z, 7.50V, feeding into the base of an NPN split-emitter transistor. This forms the input node to a set of dual-level voltage comparators with references of 0.528 and 0.645V, respectively. Current sources for the comparator are fixed biased NPNs.

The typical transition time delay for an overcurrent fault is 300ns. Bias current at the input averages 500nA.

If the overcurrent sense feature is not used, it is recommended that Pin 14 be tied to ground.

When used for sensing current-derived voltage impulses from the primary driver, a high-speed, low-impedance transient filter network is advised. An example is shown in Figure 28. Keep C_F close to the NE/SE5562.

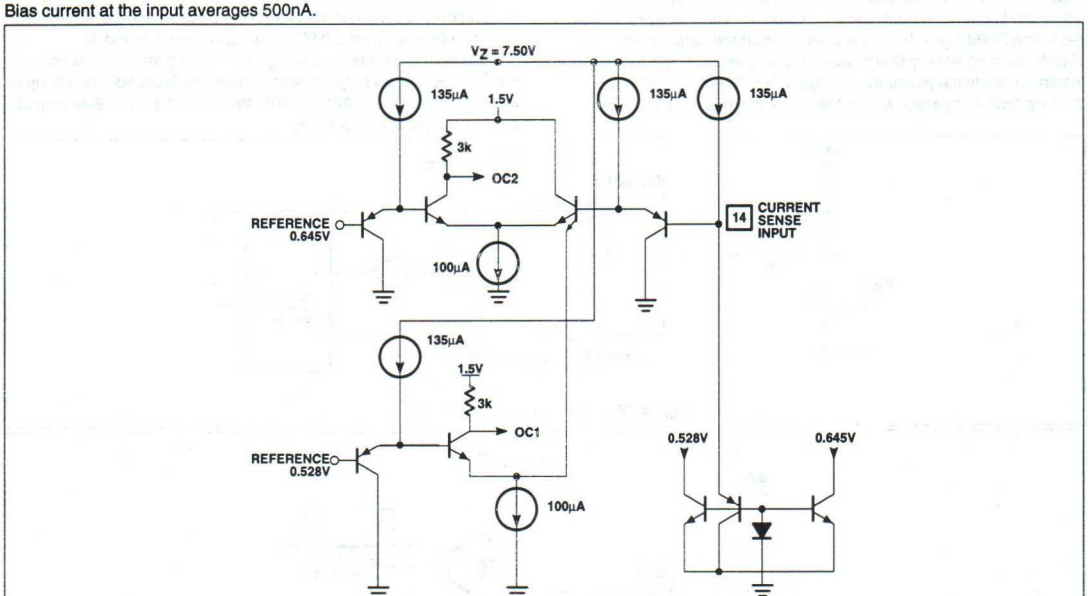


Figure 27. NE/SE5562 Overcurrent Comparator

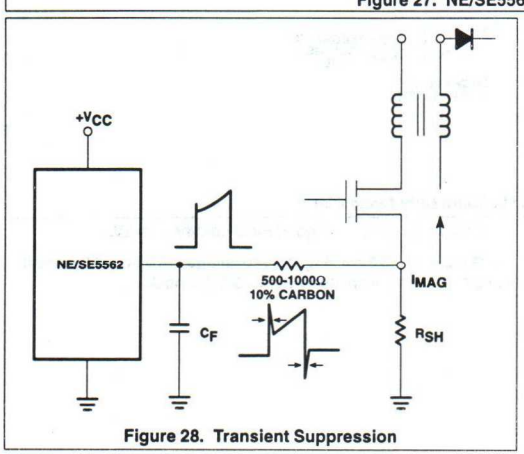


Figure 28. Transient Suppression

THEORY—OC1 AND OC2

Overcurrent Logic and Delay Capacitor Operations

The circuit takes a voltage input from Pin 14 and compares the level to a dual reference comparator with trips at 0.53 and 0.65V. The lower trip point actuates cycle-by-cycle shutdown of the output stage with an intrinsic delay of 400ns. The second level actuates the slow-start function. In addition, there exists a separate housekeeping circuit whose function is to terminate operation of the output stage if its threshold is exceeded. This involves a time delay circuit based on two separate switchable current sources, OC1 and OC2. The time delay capacitor allows the user to program shutdown of the system after a predetermined number of overcurrent cycles have occurred within the period set by the ramp-up of the delay capacitor. Once shutdown has occurred in this manner, external reset is required to restart the system. Referring to the logic block Figure 29, which controls the gating of the two charge pumps into the delay capacitor at Pin 16, the complete signal flow may be traced. Logic signals from the overcurrent 1 and 2 comparators are gated by the clock and delayed clock signals generated by the

sawtooth oscillator. The complete sequence for an overcurrent fault may be understood by referring to Figure 30 for OC2. Here it is shown that an OC2 signal exists indicating that the 0.65V threshold has been exceeded by a signal at Pin 14.

Note that an overcurrent pulse within a particular clock frame turns on the respective OC2 charge ramp during the entire next clock frame. Consecutive overcurrent pulses of either OC1 or OC2 magnitude will activate the selected charge pump for the total duration that such overcurrent occurs. The charging cycle will continue until the delay capacitor reaches the 3.86V trip level.

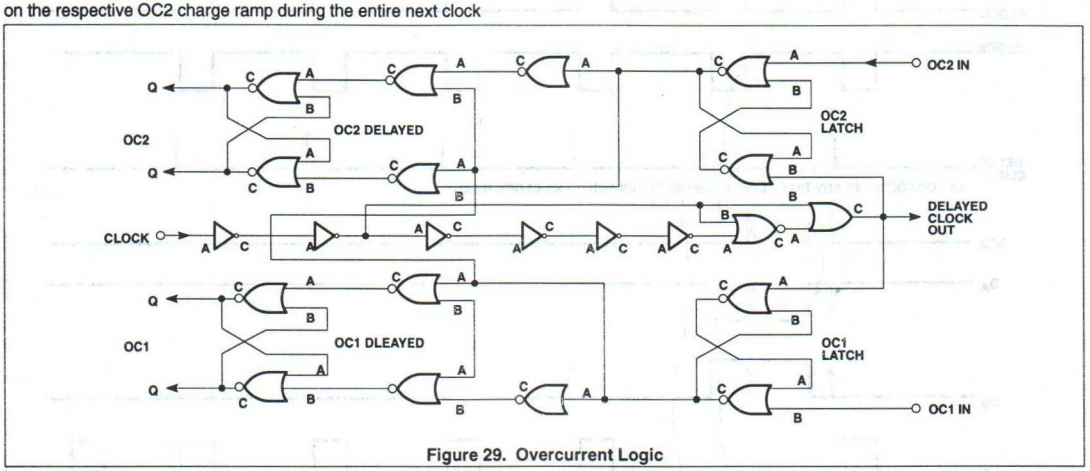


Figure 29. Overcurrent Logic

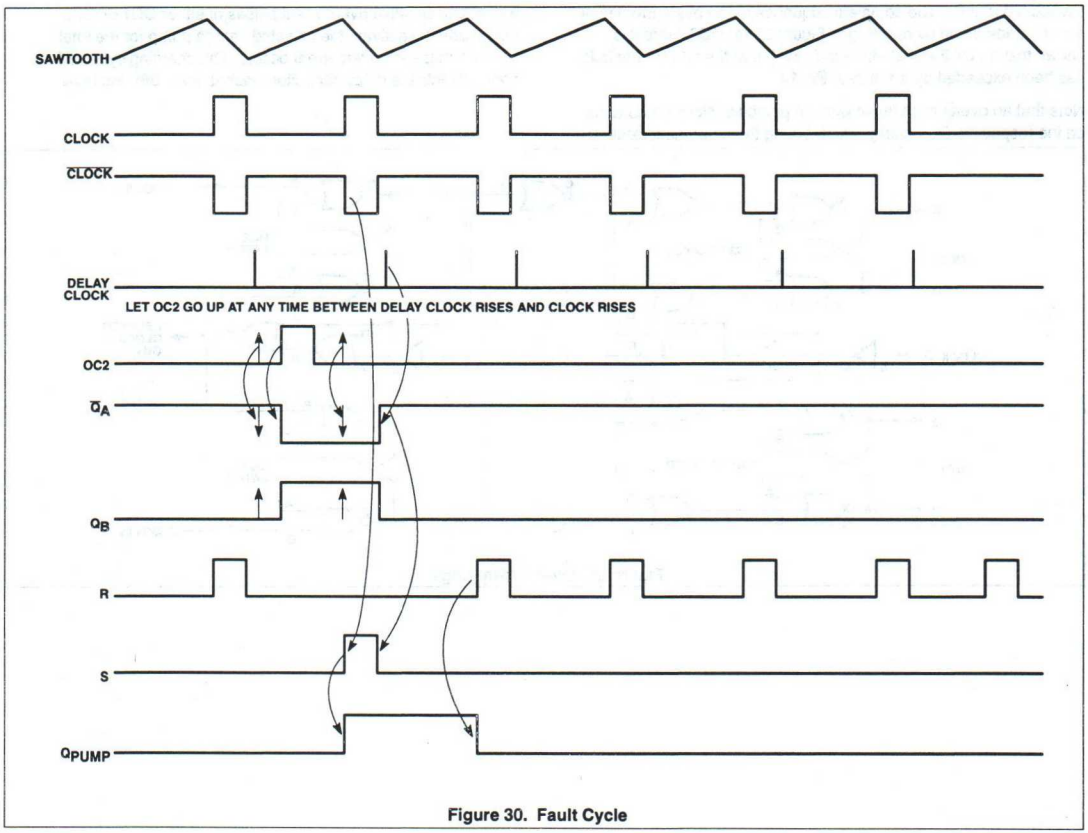


Figure 30. Fault Cycle

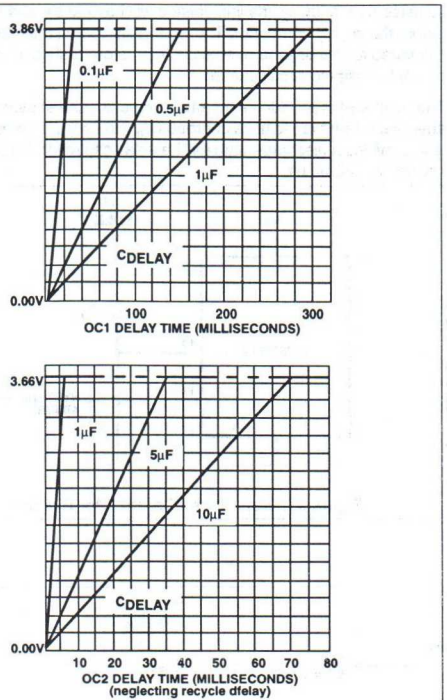


Figure 31. Overcurrent Shutdown Function

CALCULATING THE DELAY CAPACITOR

Actual delay time for a given capacitor value at Pin 16 may be estimated using the graphs in Figure 31 for OC1 and OC2. By first determining the allowable overcurrent time product for a particular power converter, a capacitor delay value may be calculated.

Note that the OC1 charge pump is typically 13µA while OC2 pumps 550µA into the capacitor. If the exact value is to be calculated for a particular delay requirement, use the following procedure:

1. Determine the level of overcurrent—OC1 or OC2.
2. Find the maximum delay time which the supply may safely sustain for this continuous overcurrent condition. Note that OC1 may be activated on every cycle if OC2 is not reached, causing continuous charging of C-Delay. However, OC2 overcurrent detection causes the supply to go into slow-start shutdown (hiccup mode), on the first such pulse. OC2 delays are based on an interrupted charging cycle with total cycle time determined by the external slow-start delay capacitor duty cycle maximum divider—time constant.

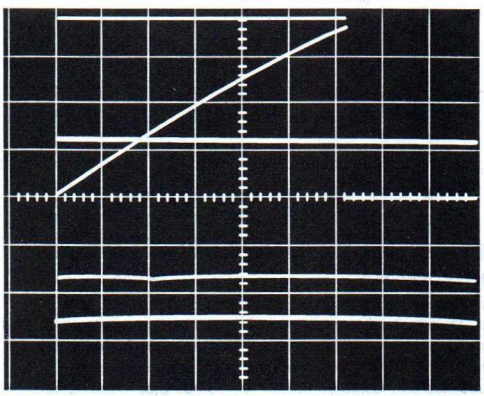


Figure 32. OC1 Ramp and Shutdown Delay

For a continuous OC1 overcurrent:

$$C_{DLY} = \frac{(13X10^{-6})(\text{Delay time} - \text{sec})}{3.86V} \quad (1)$$

For a continuous OC2 overcurrent:

$$C_{DLY} = \frac{(550X10^{-6})(\text{Delay cycles} \times 1/f_{SW})}{3.86V} \quad (2)$$

Some downward adjustment of the OC2 capacitor value may be necessary to compensate for the 1-2µA of discharge current at Pin 16 during the delay cycles.

Example: A maximum of 100 OC2 current fault cycles is allowed.

f_{SW} =400kHz, find C_{DLY}

$$C_{DLY} = \frac{(550X10^{-6})(100 \times 1/4 \times 105)}{3.86V}$$

$$=0.036\mu F$$

Example: OC2/C_{DLY}

Find number of OC1 cycles before shutdown with 0.036µF C_{DLY}.

$$\text{Delay Time} = \frac{(3.6 \times 10^{-8})(3.86V)}{13 \times 10^{-6}A}$$

$$= 10.7ms$$

$$\text{Total cycles shutdown} = \frac{10.7 \times 10^{-3}}{2.5 \times 10^{-6}}$$

$$= 4280$$

Figure 33 shows an actual OC1 charging cycle for continuous fault current sensed at Pin 14 and a DLY = 1µF.

BULK-SENSE AUXILIARY COMPARATOR WITH SHUTDOWN

This circuit is intended to act as an automatic low-line detection mechanism. As shown in Figure 33, a voltage divider is connected from the main unregulated DC supply to Pin 12. The lower divider resistor may be a potentiometer of 5-10kΩ resistance with center-tap connected to Pin 13. The comparator which senses Pin 12 voltage is referenced to 3.80V and Pin 12 divider voltage must be greater than this voltage by a sufficient margin to operate within the prescribed low-line limits. For instance, if a line voltage drop of 25% is considered the shutdown threshold, then V_{12} should be calculated for a nominal operating voltage as shown in Figure 33.

When the line voltage drops more than 25%, the output stage is disabled. With the hysteresis connected as shown and the pot adjusted near midway, the line voltage will have to exceed $V_{NOMINAL}$ before the supply will restart. The hysteresis control may then be calibrated for the desired over-excursion before restart. This prevents unstable circuit chatter.

The reset switch provides a means for resetting the shutdown latch after overcurrent faults have charged C_{DLY} to its trip threshold. This also provides a discharge path for the delay capacitor. Figure 34 shows internal circuit.

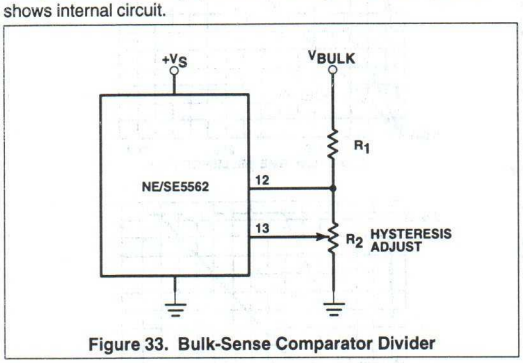


Figure 33. Bulk-Sense Comparator Divider

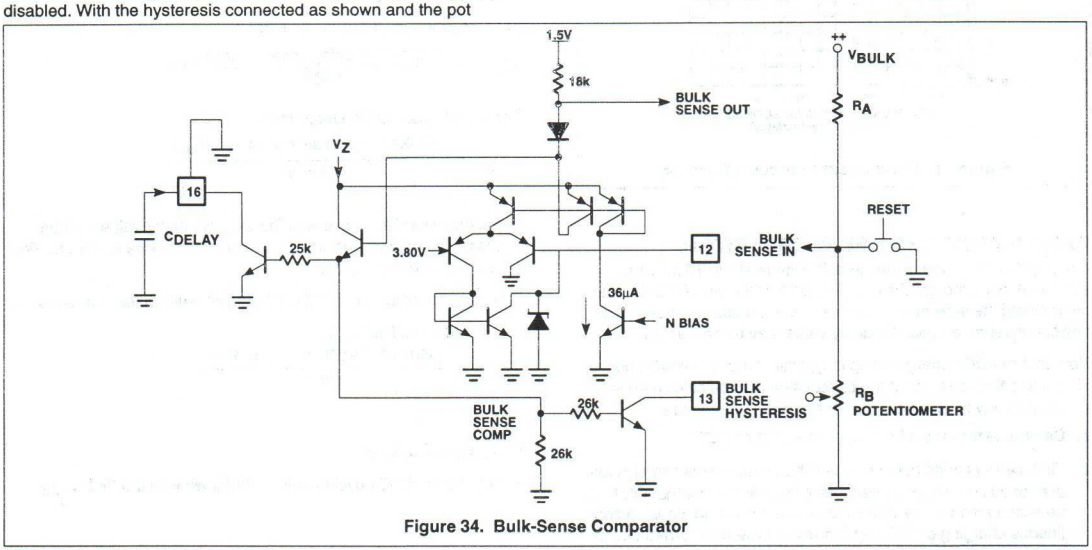


Figure 34. Bulk-Sense Comparator

THE OUTPUT DRIVE STAGE

The output stage contains the power NOR inhibit gate, invert logic function, and source-sink drivers. The driver stage is capable of sourcing and sinking 100mA at frequencies up to 600kHz. The output transistors are Schottky clamped to prevent saturation and the resultant switching delay due to stored charge. A 2.5Ω current sense resistor in the emitter of Q419 serves to drive active clamp Q427 when the output sources more than 200mA. This places a limit on the peak current available during instantaneous charging of a power MOS FET gate. This feature protects the output stage from inadvertent catastrophic overload.

When sinking current, the output is clamped to a maximum of 1.4V. Output swing for positive output is typically V_S-1.9V at 100mA sourcing. Rise time for a 2000pF load at Pin 19 is typically 160ns with a fall time of 80ns.

The power NOR gate provides a fast response inhibit function to shutdown the output in the event of a number of different fault conditions. All inputs are internal to the device and do not appear directly on the external pins as is shown on Figure 35.

The additional flexibility of an invert control allows the polarity at the output during duty cycle to be reversed. This provides a simple

means of designing with P-channel power MOS FETs without adding external inverters. The invert logic is controlled by a simple logic signal at Pin 15. Grounding will cause the output to be a normal positive output and a high level gives inverted output.

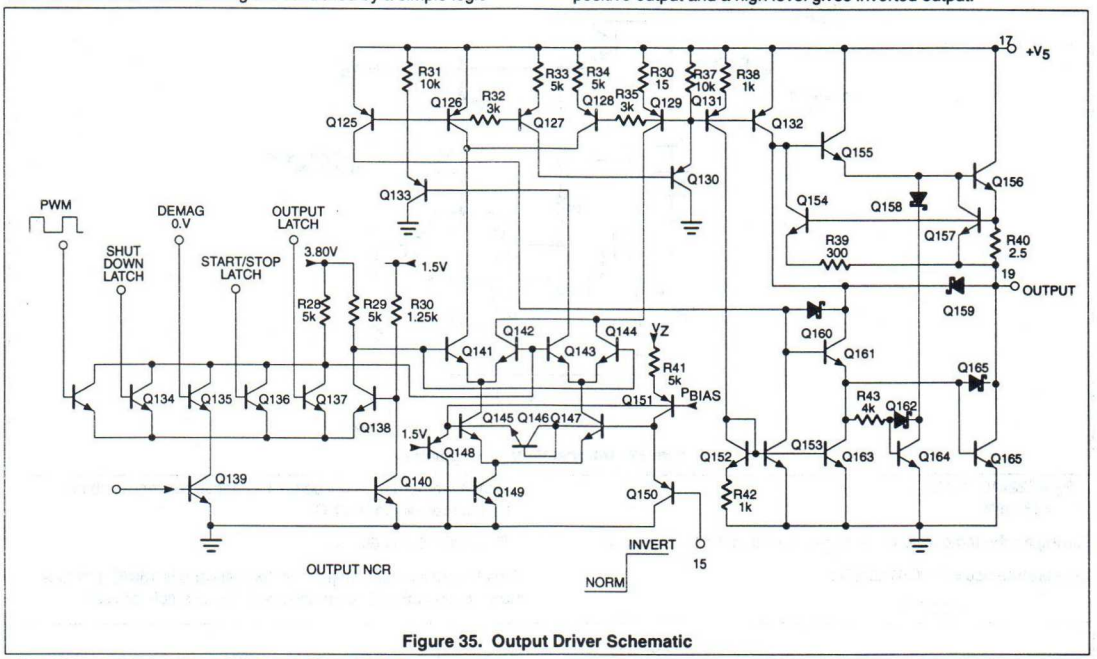


Figure 35. Output Driver Schematic

THE INTERNAL VOLTAGE REGULATOR

The internal regulator is configured to provide for external supply to the NE/SE5562 from either a voltage feed or a current feed.[1]

For the current-fed mode, a series-dropping resistor may be used to power the device from voltages greater than 18V with current supply of 15 to 25mA. Note that supply current stated in the data sheet is for the device only without load on the output or V_Z. Drive currents also are pulse-related and thus reflect frequency components onto the current-feed circuit. These must be filtered out at Pin 7 with adequately large capacitors in order to prevent motor-boating (see Figure 36 and Figure 37).

Input current to Pin 7 flows through Zeners Z_1 and Z_2, and shunt regulator transmitter QR. A differential amplifier with 3.80V reference provides feedback to regulate V_S to 15V.

In the voltage-fed mode using Pin 17, the Zeners prevent current flow through QR for input voltages less than 19V.

Power dissipation of the device must stay within the allowable package limits. These limits are derived from the thermal characteristics of the particular package chosen. The NE5562N plastic package is capable of operating within the temperature range (ambient) of 0 to +70°C. This rating applies to the surface-mount product NE5562D also. Obviously, the power dissipation of the "D" package is lower than the standard DIP. Thermal resistance for the various packages are:

20-Pin plastic—NE5562N/SE5562N: θ_{JA} 61°C/W

20-Pin glass/ceramic—NE5562F/ SE5562F: θ_{JA} 90°C/W

20-Pin SO: -55 to +85°C/W (board-dependent)

NOTE:

1. See Figures 5 and 6 for internal Regulator Response Curves.

Design Example—An NE5562N is operated at 40°C ambient in the voltage-fed mode with V_S=15V; assume I_S=22mA average:

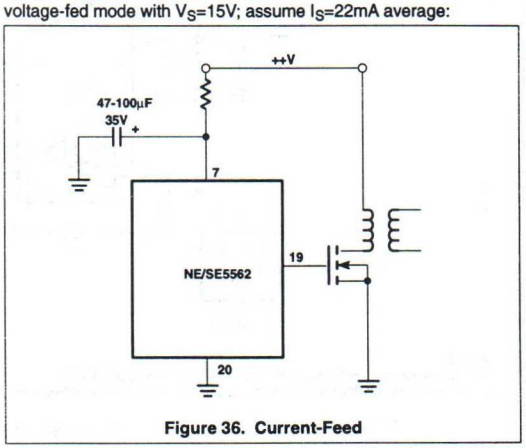


Figure 36. Current-Feed

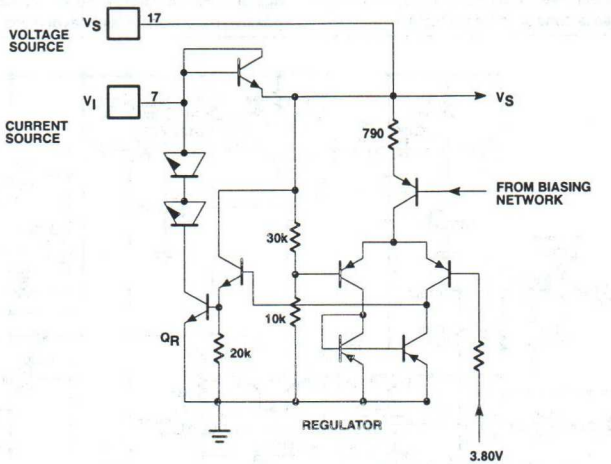


Figure 37. Internal Voltage Regulator

$\therefore P_D = (22 \times 10^{-3})\ (15)$
$= 330mW$

Solving for the temperature rise from ambient to the IC functions:

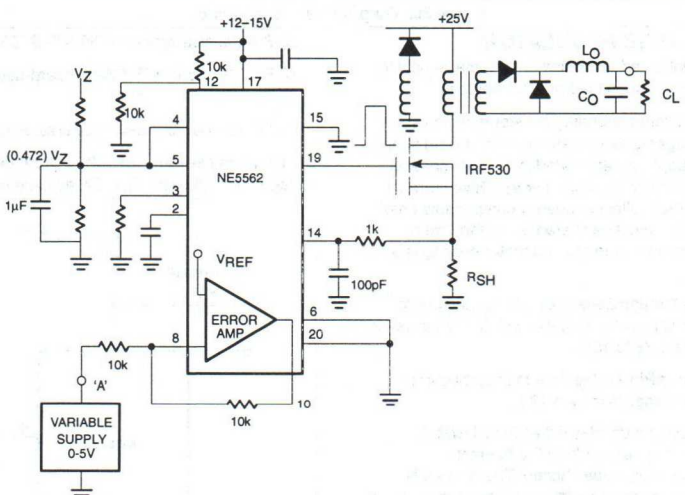
Temperature rise = 61°C/W×0.33W

= 20.1°C

Junction temperatures will be 20.1°C above average ambient temperatures which is 40°C

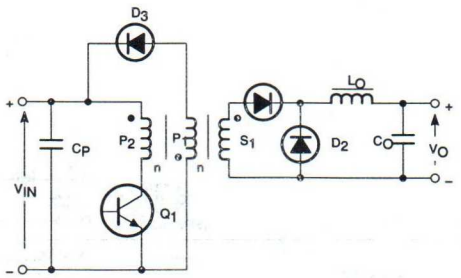
T_J=40°C 20.1°C 60.1°C

The allowable maximum junction temperature is 150°C 125°C is more conservative. The conditions of this example are safe.



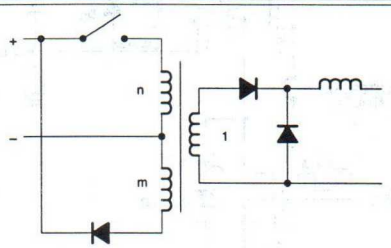
NOTES:
1. Supply will become active as point 'A' reaches the level of V_{REF} 3.80V.
2. Monitor Pin 19 and Pin 2 on dual-trace scope with voltmeter connected to supply output.

Figure 38. Open-Loop Test Setup



NOTE:
The P_1 clamp winding prevents collector voltage from exceeding 2X V_{IN} during off time.

Figure 39. Forward Converter



To Prevent Core Saturation Due to Flux Staircasing

$$\delta_{max} < 1 - \frac{m}{m+n} \text{ if } m = n\ \delta_{max} < .5$$

Demagnetization of Core

$$V_{CEmax} = V_{imax} \times \frac{m+n}{m} \quad (V)$$

Maximum Voltage Across Transistor

Figure 40. Forward Converter Design Formulas

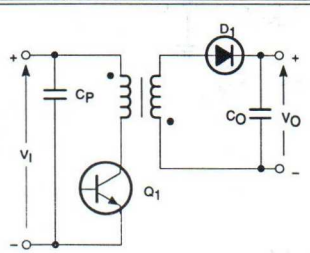


Figure 41. Isolated Secondary

Flyback Converter Design

Flyback Converter

Advantages:

- Simple circuit. Only one inductive component even with line isolation.
- Economic. Low component count, low cost.
- Work over large input voltage variations.
- Can accommodate multiple outputs.

Disadvantages:

- Large output ripple current due to discontinuous energy transfer.
- Large output capacitor; has to supply part of the load current.
- Low leakage inductance required to prevent high voltage spikes at the switching transistors.
- Relatively large core volume for the output power. Core driven in one direction only.

Design Parameters for Flyback Inductor

Input

- Minimum input voltage
- Maximum input voltage

Output

- Output voltage or voltages
- Output current or currents
- Output load

Frequency of Operation

Estimate of Overall Efficiency. (η)

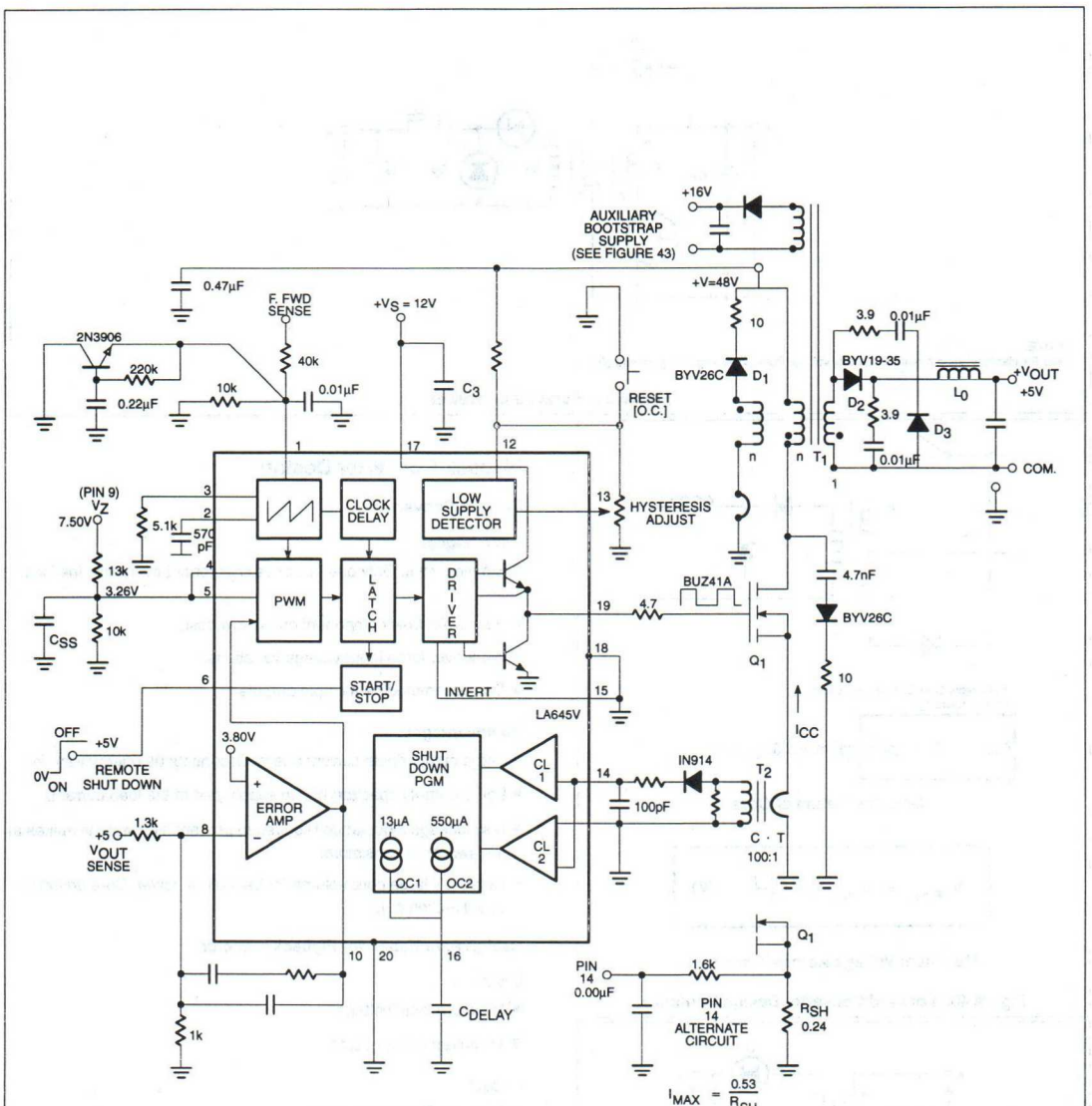


Figure 42. Forward Converter, 100W – 5V

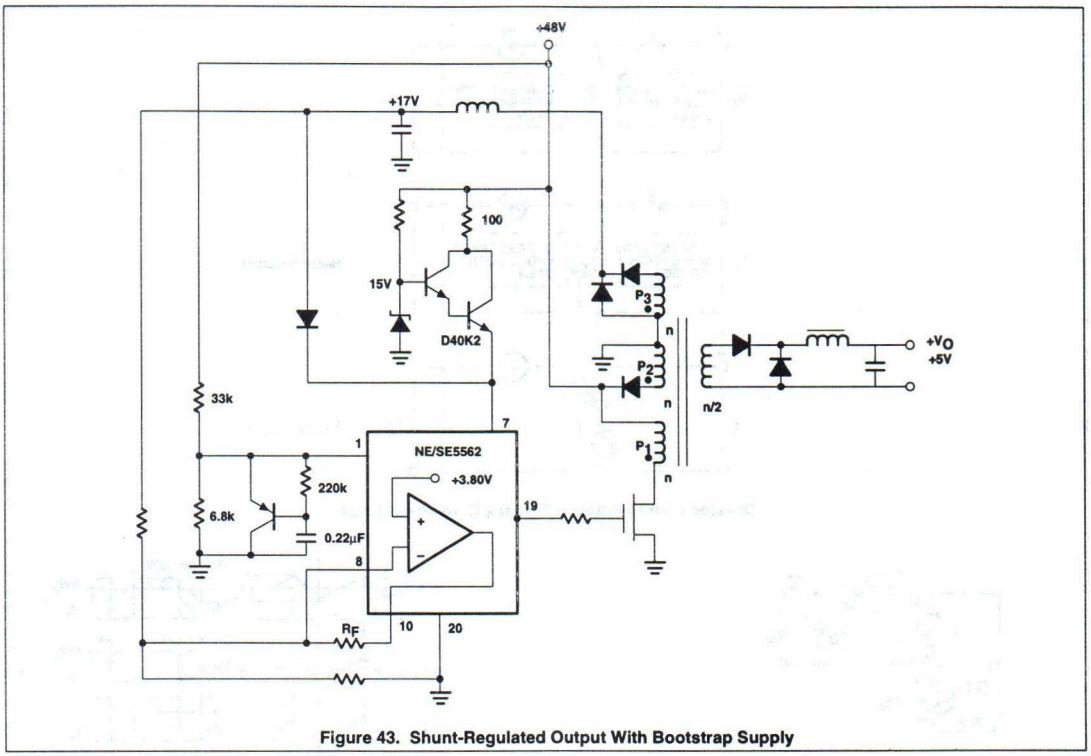
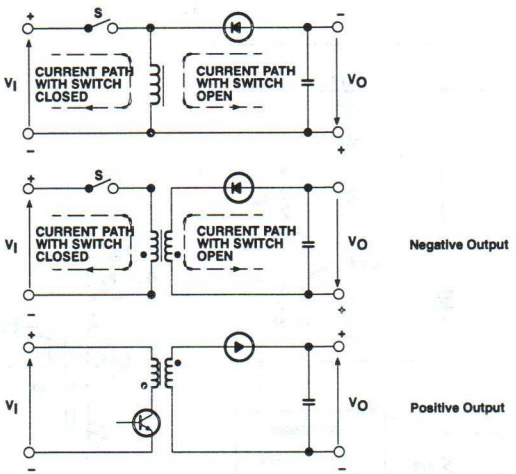
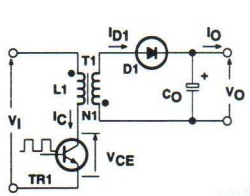
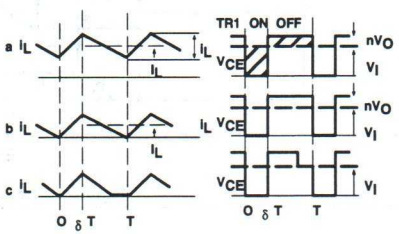


Figure 43. Shunt-Regulated Output With Bootstrap Supply



Development of Practical Flyback Converter Circuit

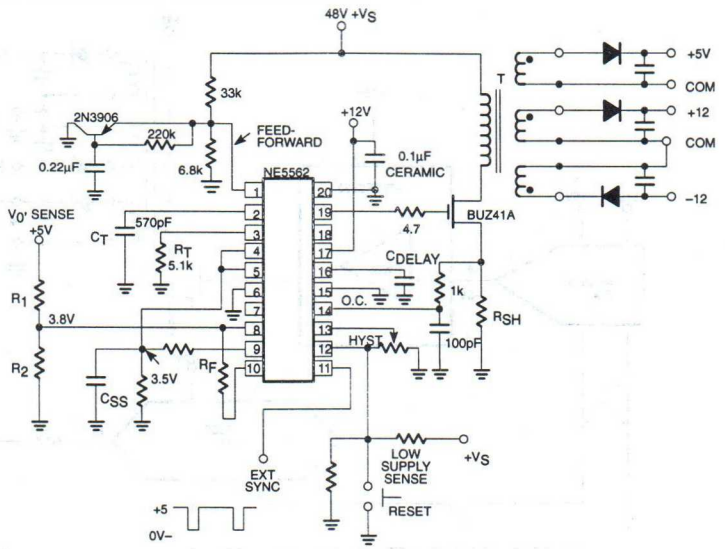




NOTES:
a. Unlimited choke current
b. Interrupted choke current

Flyback Converter and Current and Voltage Waveforms

Figure 44.



NOTE:
400kHz operation with feed-forward line regulation and cycle-by-cycle current timing.

Figure 45. NE5562 Flyback Converter

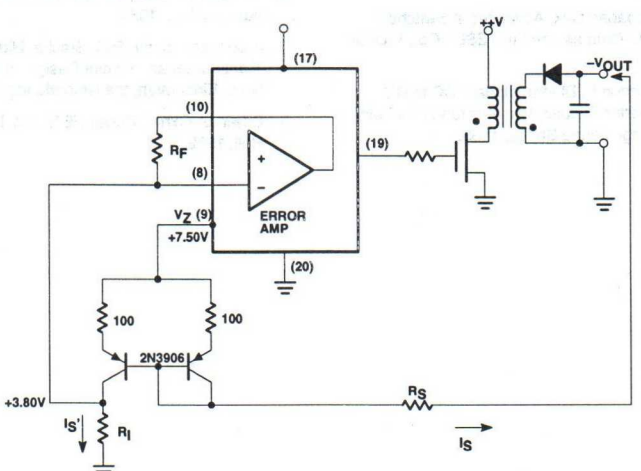


Figure 46. Negative Output Regulator Using Current Mirror

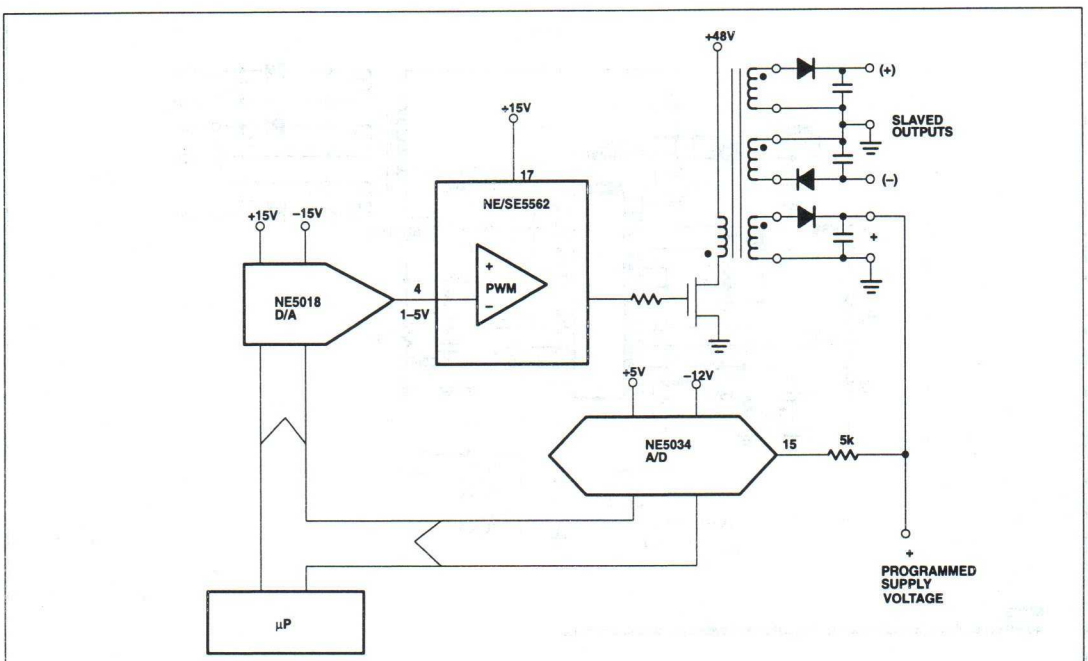


Figure 47. Microprocessor Controlled SMPS

REFERENCES

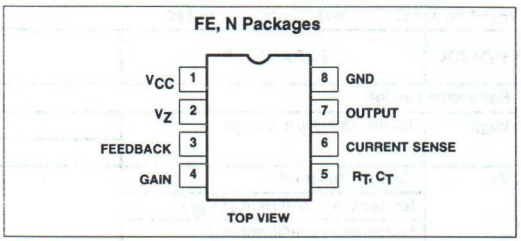
1. R.D. Middlebrook and Slobadan Cuk, Advances in Switched Mode Power Conversion, Volumes I and II, TESLA Co., Pasadena, CA, 1983.
2. Rudolf P. Stevens and Gordon E. Bloom, Modern DC to DC Switchmode Power Convertor Circuits, Van Nostrand Reinhold/ Computer Science and Engineering Series, 1985.
3. H. Dean Venable, Stability Analysis Made Simple, Venable Industries, Inc., 1981.
4. J. Jongsma and L.P.M. Bracke, High Frequency Ferrite Power Transformer and Choke Design, N. V. Philips ELCOMA Publications, Eindhoven, the Netherlands, September 1982.
5. Edwin S. Oxner, Power FETs and Their Applications, Prentice-Hall, 1982.

Switched-mode power supply controller — NE5568

DESCRIPTION

The NE5568 is a control circuit for use in switched mode power supplies. It contains an internal temperature-compensated supply, PWM, sawtooth oscillator, over-current sense latch, and output stage. The device is intended for low cost SMPS applications where extensive housekeeping functions are not required. The NE5568 is a selected version of the NE5561.

PIN CONFIGURATION



FEATURES

- Micro-miniature (D) package
- Pulse width modulator
- Current limiting (cycle by cycle)
- Sawtooth generator
- Stabilized power supply
- Double-pulse protection
- Internal temperature-compensated reference

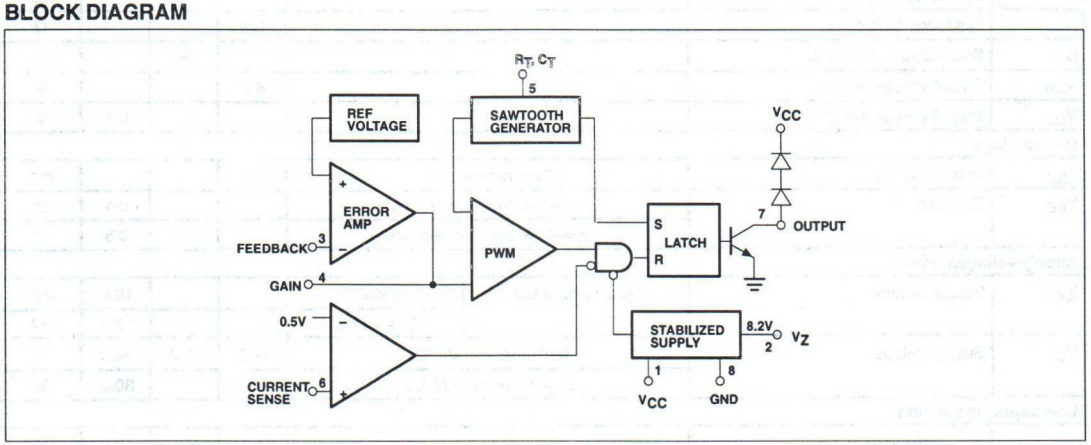
APPLICATIONS

- Switch mode power supplies
- DC motor controller inverter
- DC/DC converter

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5568N	0404B
8-Pin Cerdip Dual In-Line Package (CERDIP)	0 to +70°C	NE5568FE	0580A

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	18	V
I_{OUT}	Output current	40	mA
	Output duty cycle	98	%
P_D	Max total power dissipation	0.75	W
T_A	Operating temperature range	0 to 70	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC}=12V, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		NE5568 Min	NE5568 Typ	NE5568 Max	UNIT
Reference section							
V_{REF}	Internal reference voltage	T_A=25°C		3.69	3.75	3.84	V
		Over temperature		3.66		3.87	V
V_Z	Internal zener ref	I_L=7mA		7.8	8.2	8.8	V
	Temperature coefficient of V_{REF}				± 100		ppm/°C
	Temperature coefficient of V_Z				± 200		ppm/°C
Oscillator section							
f	Frequency range	Over temperature		50		100k	Hz
	Initial accuracy	R_T and C_T Constant			5		%
	Duty cycle range	f_o=20kHz		0		98	%
Current limiting							
I_{IN}	Input current	Pin 6=250mV	T_A=25°C		-2	-10	µA
			Over temp.			-20	µA
	Single pulse inhibit delay	Inhibit delay time for 20% overdrive at	I_{OUT}=20mA		0.88	1.10	µs
			I_{OUT}=40mA		0.7	0.8	µs
	Current limit trip level			0.400	0.500	0.600	V
Error amplifier							
	Open-loop gain				60		dB
	Feedback resistor			10k			Ω
BW	Small-signal bandwidth				3		MHz
V_{OH}	Output voltage swing			6.2			V
V_{OL}	Output voltage swing					0.7	V
Output stage							
I_{OUT}	Output current	Over temperature		20			mA
V_{CE}	Saturation	I_C=20mA, over temperature				0.4	V
		I_C=40mA, over temperature				0.5	V
Supply voltage/current							
I_{CC}	Supply current	I_Z=0, voltage-fed	T_A=25°C			10.0	mA
			Over temp.			13.0	mA
V_{CC}	Supply voltage	I_S=10mA, current-fed		19.0	21.0	24.0	V
		I_{CC}=30mA, current-fed		20.0		30.0	V
Low supply protection							
	Pin 1 threshold			8.0	9.0	10.5	V

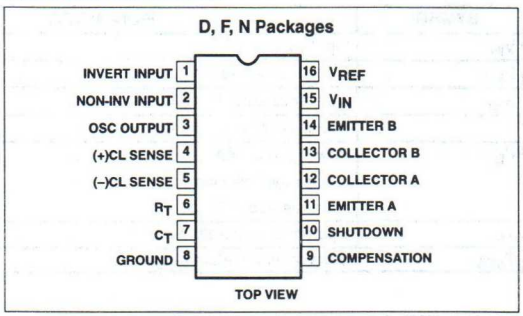
NOTES:
All curves and applications of NE5561 apply exactly

SMPS control circuit — SG3524

DESCRIPTION

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error amplifier, oscillator, pulse-width modulator, pulse steering flip-flop, dual alternating output switches and current-limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer-coupled DC-to-DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG3524 is designed for commercial applications of 0°C to +70°C.

PIN CONFIGURATION



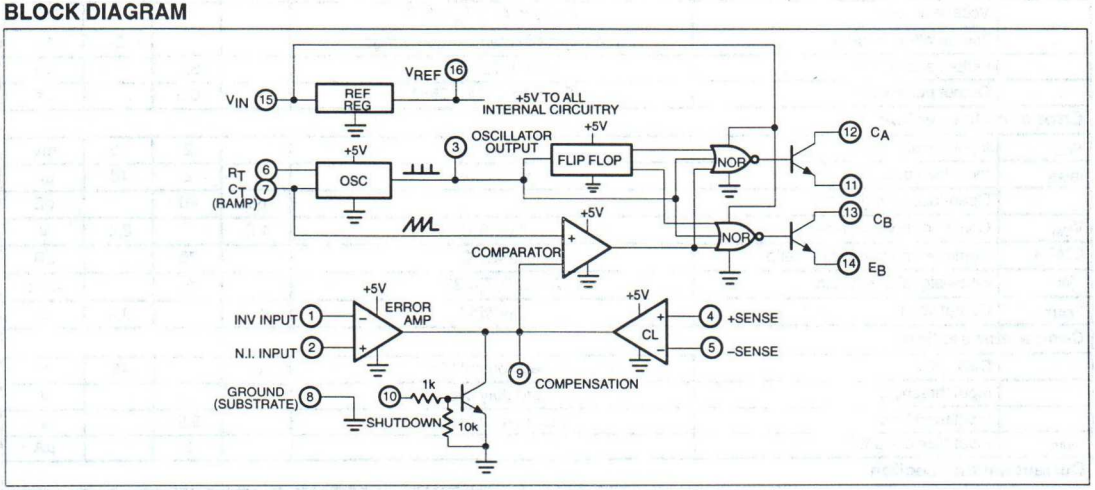
FEATURES

- Complete PWM power control circuitry
- Single ended or push-pull outputs
- Line and load regulation of 0.2%
- 1% maximum temperature variation
- Total supply current is less than 10mA
- Operation beyond 100kHz

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	SG3524N	0406C
16-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	SG3524F	0582B
16-Pin Small Outline (SO) Package	0 to +70°C	SG3524D	0005D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{IN}	Input voltage	40	V
I_{OUT}	Output current (each output)	100	mA
I_{REF}	Reference output current	50	mA
	Oscillator charging current	5	mA
P_D	Power dissipation		
	Package limitation	1000	mW
	Derate above 25°C	8	mW/°C
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

T_A=0°C to +70°C, V_{IN}=20V, and f=20kHz, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Reference section						
V_{OUT}	Output voltage		4.6	5.0	5.4	V
	Line regulation	V_{IN}=8 to 40V		10	30	mV
	Load regulation	I_L=0 to 20mA		20	50	mV
	Ripple rejection	f=120Hz, T_A=25°C		66		dB
I_{SC}	Short circuit current limit	V_{REF}=0, T_A=25°C		100		mA
	Temperature stability	Over operating temperature range		0.3	1	%
	Long-term stability	T_A=25°C		20		mV/kHz
Oscillator section						
f_{MAX}	Maximum frequency	C_T=0.001 µF, R_T=2kΩ		300		kHz
	Initial accuracy	R_T and C_T constant		5		%
	Voltage stability	V_{IN}=8 to 40V, T_A=25°C			1	%
	Temperature stability	Over operating temperature range			2	%
	Output amplitude	Pin 3, T_A=25°C		3.5		V_P
	Output pulse width	C_T=0.01 µF, T_A=25°C		0.5		µs
Error amplifier section						
V_{OS}	Input offset voltage	V_{CM}=2.5V		2	10	mV
I_{BIAS}	Input bias current	V_{CM}=2.5V		2	10	µA
	Open-loop voltage gain		68	80		dB
V_{CM}	Common-mode voltage	T_A=25°C	1.8		3.4	V
CMRR	Common-mode rejection ratio	T_A=25°C		70		dB
BW	Small-signal bandwidth	A_V=0dB, T_A=25°C		3		MHz
V_{OUT}	Output voltage	T_A=25°C	0.5		3.8	V
Comparator section						
	Duty cycle	% each output "ON"	0		45	%
	Input threshold	Zero duty cycle		1		V
	Input threshold	Maximum duty cycle		3.5		V
I_{BIAS}	Input bias current			1		µA
Current limiting section						
	Sense voltage	Pin 9=2V with error amplifier set for maximum out, T_A=25°C	180	200	220	mV
	Sense voltage T.C.			0.2		mV/°C
V_{CM}	Common-mode voltage		-1		+1	V

DC ELECTRICAL CHARACTERISTICS (Continued)

T_A = 0°C to +70°C, V_{IN} = 20V, and f = 20kHz, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Output section (each output)						
	Collector-emitter voltage (breakdown)		40			V
	Collector-leakage current	V_{CE}=40V		0.1	50	µA
	Saturation voltage	I_C=50mA		1	2	V
	Emitter output voltage	V_{IN}=20V	17	18		V
t_R	Rise time	R_C=2kΩ, T_A=25°C		0.2		µs
t_F	Fall time	R_C=2kΩ, T_A=25°C		0.1		µs
Total standby current						
	(excluding oscillator charging current, error and current limit dividers, and with outputs open)	V_{IN}=40V		8	10	mA

THEORY OF OPERATION

Voltage Reference

An internal series regulator provides a nominal 5V output which is used both to generate a reference voltage and is the regulated source for all the internal timing and controlling circuitry. This regulator may be bypassed for operation from a fixed 5V supply by connecting Pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0V.

This reference regulator may be used as a 5V source for other circuitry. It will provide up to 50mA of current itself and can easily be expanded to higher currents with an external PNP as shown in Figure 1.

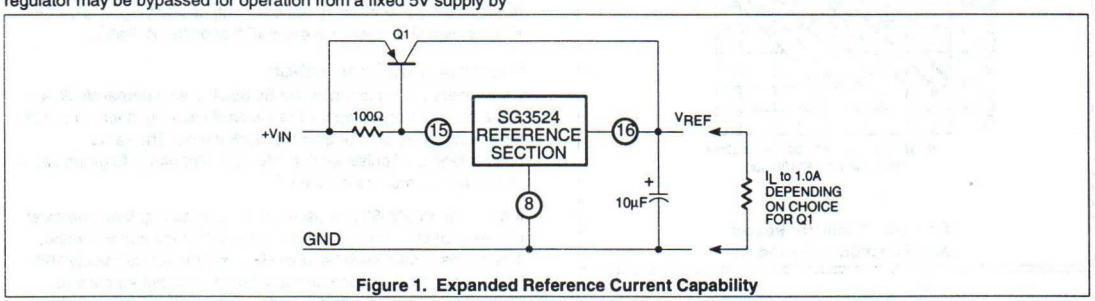
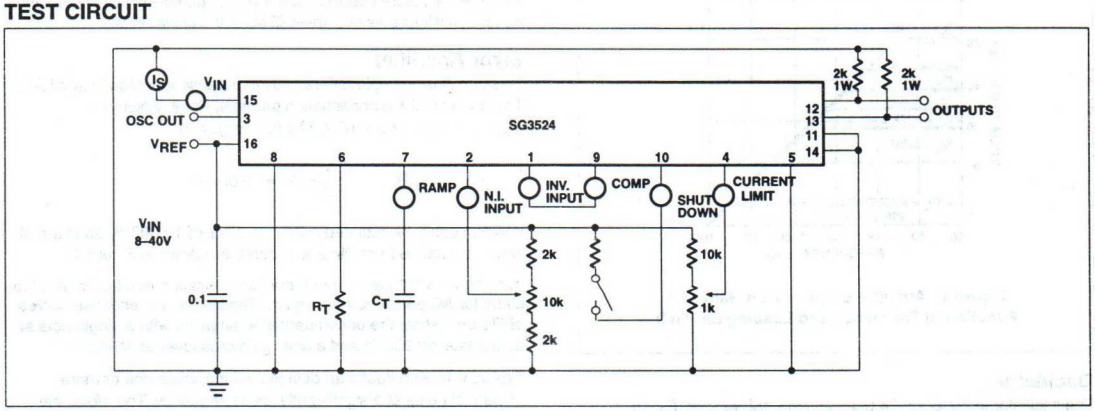


Figure 1. Expanded Reference Current Capability

TEST CIRCUIT



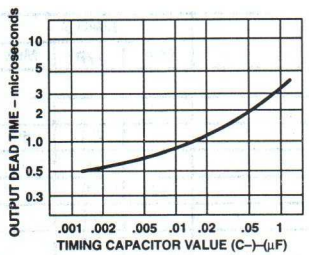


Figure 2. Output Stage Dead Time as a Function of the Timing Capacitor Value

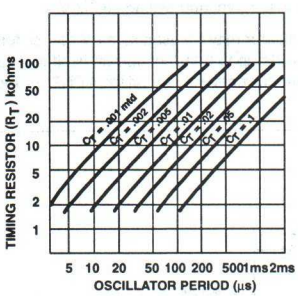


Figure 3. Oscillator Period as a Function of R_T and C_T

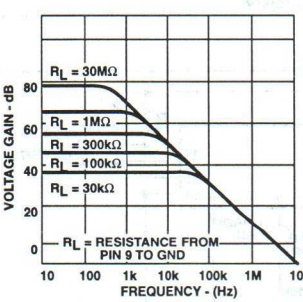


Figure 4. Amplifiers Open-Loop Gain as a Function of Frequency and Loading on Pin 9

Oscillator

The oscillator in the SG3524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series-connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The charging current is equal to 3.6 V ÷ R_T and should be kept within the approximate range of 30μA to 2mA; i.e., 1.8k<R_T<100k.

The range of values for C_T also has limits as the discharge time of C_T determines the pulse-width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 2. A pulse width below approximately 0.5μs may allow false triggering of one output by removing the blanking pulse prior to the flip-flop's reaching a stable state. If small values of C_T must be used, the pulse-width may still be expanded by adding a shunt capacitance (≅100pF) to ground at the oscillator output. [(Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse-width slightly.)] Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between 0.001 and 0.1 μF.

The oscillator period is approximately t=R_TC_T where t is in microseconds when R_T=Ω and C_T=μF. The use of Figure 3 will allow selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each output's duty cycle is 0-45% and the overall frequency is one-half that of the oscillator.

External Synchronization

If it is desired to synchronize the SG3524 to an external clock, a pulse of ≅+3V may be applied to the oscillator output terminal with R_TC_T set slightly greater than the clock period. The same considerations of pulse-width apply. The impedance to ground at this point is approximately 2kΩ.

If two or more SG3524s must be synchronized together, one must be designated as master with its R_TC_T set for the correct period. The slaves should each have an R_TC_T set for approximately 10% longer period than the master with the added requirement that C_T(slave)=one-half C_T (master). Then connecting Pin 3 on all units together will insure that the master output pulse—which occurs first and has a wider pulse width—will reset the slave units.

Error Amplifier

This circuit is a simple differential input transconductance amplifier. The output is the compensation terminal, Pin 9, which is a high-impedance node (R_L≅ 5MΩ). The gain is

$$A_V = g_M R_L = \frac{8\ I_C\ R_L}{2kT} \approx 0.002R_L$$

and can easily be reduced from a nominal of 10,000 by an external shunt resistance from Pin 9 to ground, as shown in Figure 4.

In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 4 show the uncompensated amplifier with a single pole at approximately 200Hz and a unity gain crossover at 5MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly lower frequency. Therefore, the best stabilizing network is a series RC combination between Pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50kΩ plus 0.001μF.

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200μA can pull this point to ground, thus shutting off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal inversions may result. For conventional regulator applications, the 5V reference voltage must be divided down as shown in Figure 5. The error amplifier may also be used in fixed duty cycle applications by using the unity gain configuration shown in the open-loop test circuit.

Current Limiting

The current limiting circuitry of the SG3524 is shown in Figure 6.

By matching the base-emitter voltages of Q1 and Q2, and assuming a negligible voltage drop across R_1:

$$\text{Threshold} = V_{BE}(Q1) + I_1R_2 - V_{BE}(Q2)$$

$$= I_1R_2 \equiv 200\text{mV}$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ±1V common-mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R_1C_1 and Q1 provides a roll-off pole at approximately 300Hz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage required to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, Pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and to shorten an output pulse, should transformer saturation occur. Another application is to ground Pin 5 and use Pin 4 as an additional shutdown terminal: i.e., the output will be off with Pin 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 7. This circuit can reduce the short-circuit current (I_{SC}) to approximately one-third the maximum available output current (I_{MAX}).

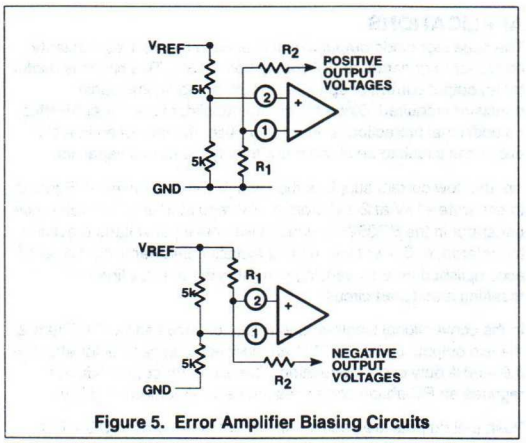


Figure 5. Error Amplifier Biasing Circuits

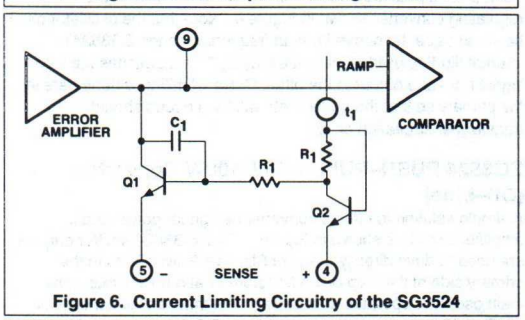


Figure 6. Current Limiting Circuitry of the SG3524

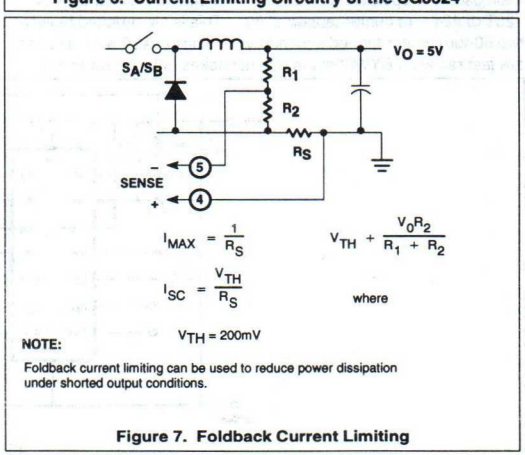


Figure 7. Foldback Current Limiting

Applications using the SG3524

AN126

APPLICATIONS

The capacitor-diode output circuit is used in Figure 1 as a polarity converter to generate a –5V supply from +15V. This circuit is useful for an output current of up to 20mA with no additional boost transistors required. Since the output transistors are current-limited, no additional protection is necessary. Also, the lack of an inductor allows the circuit to be stabilized with only the output capacitor.

Another low current supply is the flyback converter used in Figure 3 to generate +15V at 20mA from a +5V regulated line. The reference generator in the SG3524 is unused with the input voltage providing the reference. Current limiting in a flyback converter Is difficult and is accomplished here by sensing current in the primary line and resetting a soft start circuit.

In the conventional single-ended regulator circuit shown in Figure 2, the two outputs of the SG3524 are connected in parallel for effective 0.0 – 90% duty cycle modulation. The use of an output inductor requires an RC phase compensation network for loop stabllity.

Push-pull outputs are used in this transformer-coupled DC – DC regulating converter shown in Figure 4. Note that the oscillator must be set at twice the desired output frequency, as the SG3524's internal flip-flop divides the frequency by 2 as it switches the PWM signal from one output to the other. Current limiting is done here in the primary so that the pulse width will be reduced should transformer saturation occur.

SG3524 PUSH–PULL + 50V, 100W Converter (Off–Line)

A simple solution to off-line converter design for power audio amplifier circuits is shown in Figure 5. The SG3524 emitter outputs are used to drive directly a pair of BUZ41A Power FETs in the primary side of the step-down transformer at a 50kHz rate. (The main oscillator operates at 100kHz.) The transformer consists of 120T of #24 wire center-tapped at 60T. This is sandwiched befwcen two 50-turn center-tapped secondary windings of #20 wire. Diodes are fast recovery BYW30s; the output chokes, 500µH wound on EC35 (3C8) pair Ferroxcube cores, provide adequate filtering in conjunction with the 1000µF and 0.01µF ceramic capacitors across the output.

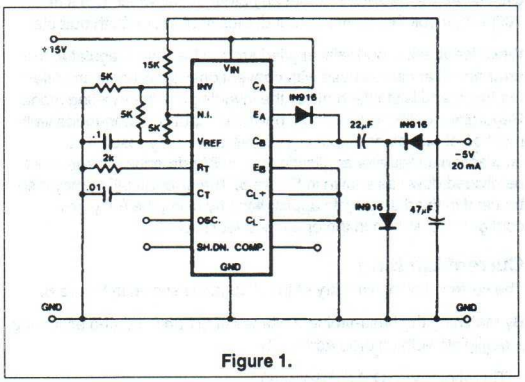


Figure 1.

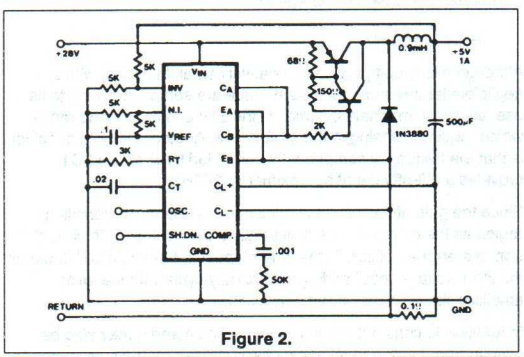


Figure 2.

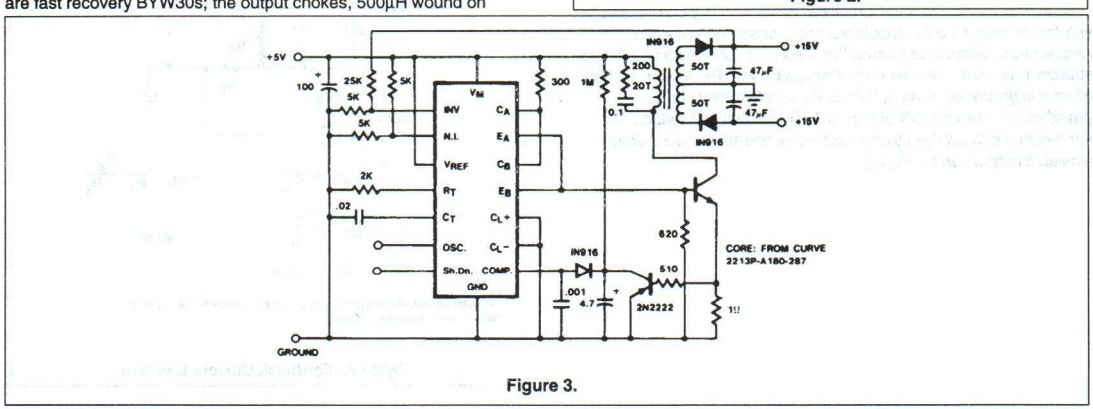


Figure 3.

Applications using the SG3524

AN126

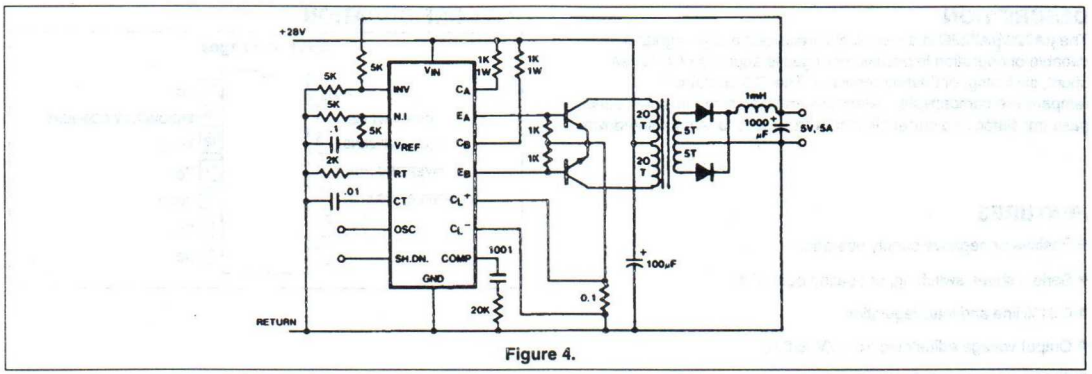


Figure 4.

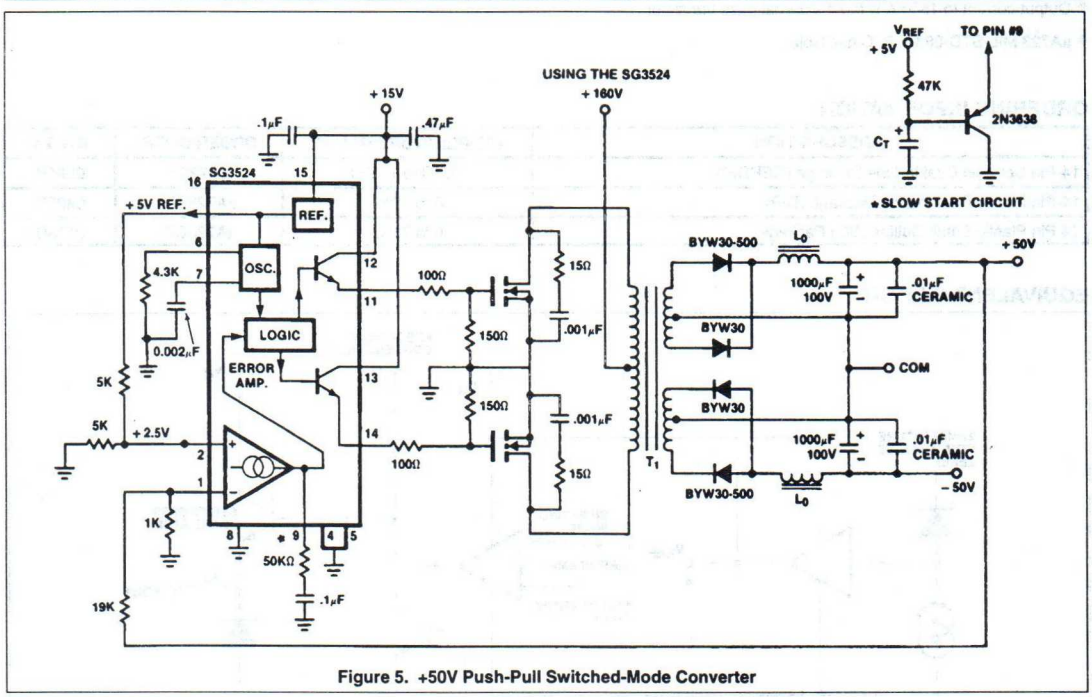


Figure 5. +50V Push-Pull Switched-Mode Converter

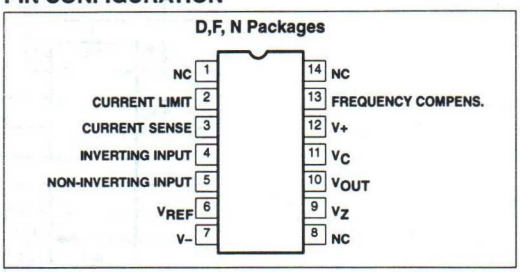
Precision voltage regulator

μA723/723C

DESCRIPTION

The μA723/μA723C is a monolithic precision voltage regulator capable of operation in positive or negative supplies as a series, shunt, switching, or floating regulator. The 723 contains a temperature-compensated reference amplifier, error amplifier, series pass transistor, and current limiter, with access to remote shutdown.

PIN CONFIGURATION



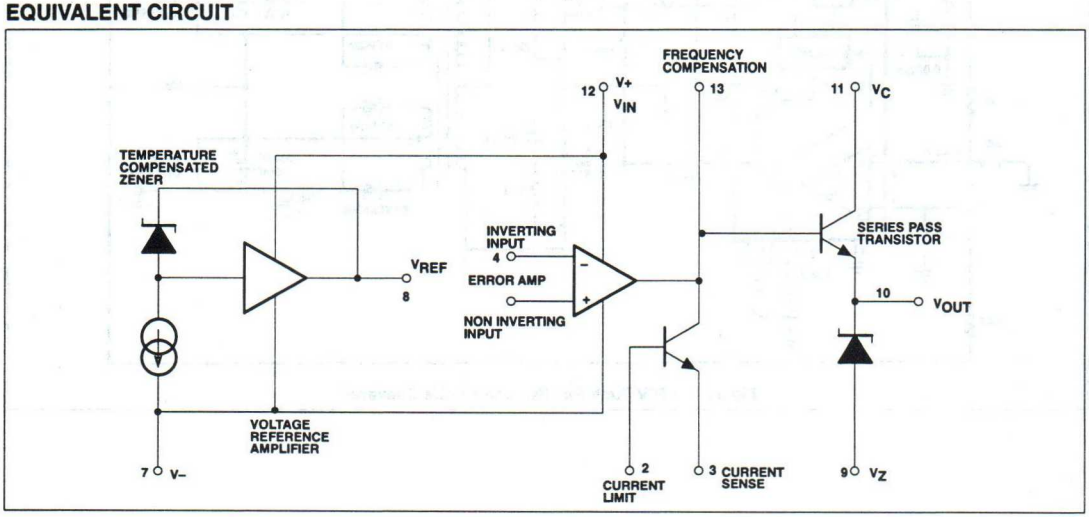
FEATURES

- Positive or negative supply operation
- Series, shunt, switching, or floating operation
- 0.01% line and load regulation
- Output voltage adjustable from 2V to 37V
- Output current to 150mA without external pass transistor
- μA723 MIL-STD-883A, B, C available

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to 125°C	μA723F	0581B
14-Pin Plastic Dual In-Line Package (DIP)	0 to 70°C	μA723CN	0405B
14-Pin Plastic Small Outline (SO) Package	0 to 70°C	μA723CD	0175D

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Pulse voltage from V+ to V- (50ms)	50	V
	Continuous voltage from V+ to V-	40	V
	Input-output voltage differential	40	V
V_{DIFF}	Error amplifier maximum input differential voltage	±5	V
V_{CM}	Error amplifier non-inverting input (Pin 5) to -V (Pin 7)	8	V
I_{OUT}	Maximum output current	150	mA
	Current from V_{REF}	15	mA
	Current from V_Z	25	mA
P_{MAX}	Maximum power dissipation T_A=25°C (still-air)[1]		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
T_A	Operating ambient temperature range		
	µA723	-55 to +125	°C
	µA723C	0 to 70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. The following derating factors should be applied above 25°C
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=25°C, unless otherwise specified.[1]

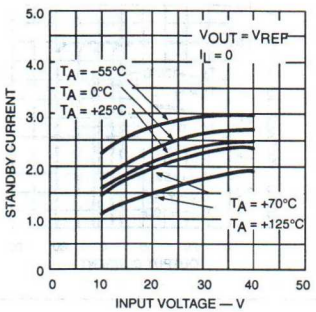
SYMBOL	PARAMETER	TEST CONDITIONS	µA723			µA723C			UNITS
			Min	Typ	Max	Min	Typ	Max	
$V_{R\ LINE}$	Line regulation[2]	V_{IN}=12V to V_{IN}=15V		0.01	0.1		0.01	0.1	%V_{OUT}
		V_{IN}=12V to V_{IN}=40V		0.02	0.2		0.1	0.5	
$V_{R\ LOAD}$	Load regulation[2]	I_L=1mA to I_L=50mA		0.03	0.15		0.03	0.2	%V_{OUT}
ΔVIN/Δ VO	Ripple Rejection	f=50Hz to 10kHz, C_{REF}=0		74			74		dB
		f=50Hz to 10kHz, C_{REF}=5µF		86			86		
I_{OS}	Short-circuit current	R_{SC}=10Ω, V_{OUT}=0		65			65		mA
V_{REF}	Reference voltage	I_{REF}=0.1mA	6.95	7.15	7.35	6.80	7.15	7.50	V
$V_{REF\ (LOAD)}$	Reference voltage change with load	I_{REF}=0.1mA to 5mA			20			20	mV
V_{NOISE}	Output noise voltage	BW=100Hz to 10kHz, C_{REF}=0		20			20		μV_{RMS}
		BW=100Hz to 10kHz, C_{REF}=5µF		2.5			2.5		
S	Long-term stability	Tj=Tjmax. TA=25°C for end point measurment		0.1			0.1		%1000 hrs.
I_{SCD}	Standby current drain	I_L=0, V_{IN}=30V		2.3	3.5		2.3	4.0	mA
V_{IN}	Input voltage range		9.5		40	9.5		40	V
V_{OUT}	Output voltage range		2.0		37	2.0		37	V
V_{DIFF}	Input-output voltage differential		3.0		38	3.0		38	V
The following specifications apply over the operating temperature ranges.									
$V_{R\ LINE}$	Line regulation	V_{IN}=12V to V_{IN}=15V			0.3			0.3	%V_{OUT}
$V_{R\ LOAD}$	Load regulation	I_L=1mA to I_L=50mA			0.6			0.6	%V_{OUT}
TC	Average temperature coefficient of output voltage			0.002	0.015		0.003	0.015	%/°C

NOTES:

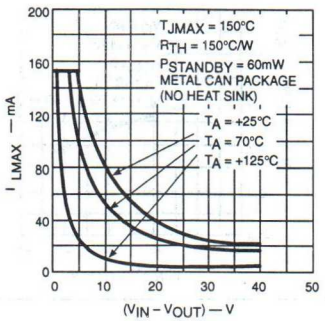
1. V_{IN}=V+=V_C=12V, V-=0V, V_{OUT}=5V, I_L=1mA, R_{SC}=0, C_1=100pF, C_{REF}=0 and divider impedance as seen by error amplifier≤10kΩ.
2. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

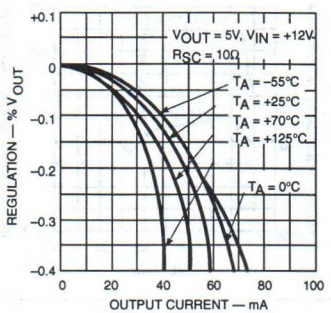
Standby Current Drain as a Function of Input Voltage



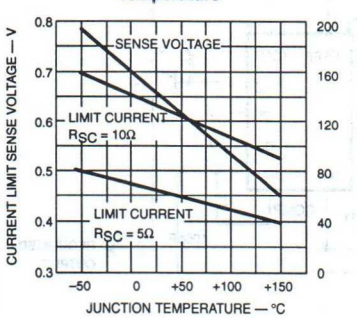
Maximum Load Current as a Function of Input-Output Voltage Differential



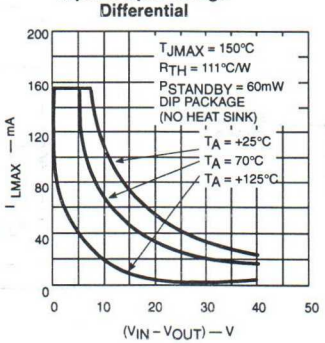
Load Regulation Characteristics with Current Limiting



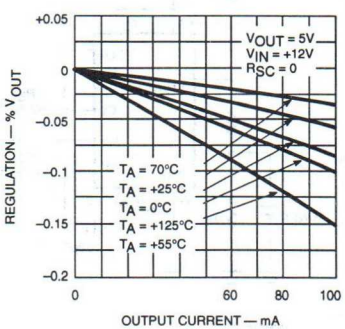
Current Limiting Characteristics as a Function of Junction Temperature



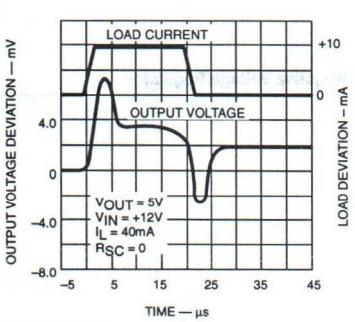
Maximum Load Current as a Function of Input-Output Voltage Differential



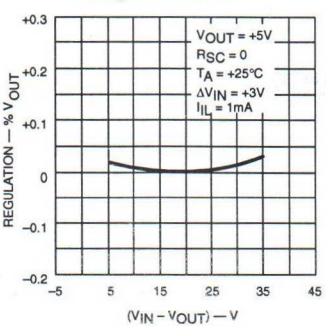
Load Regulation Characteristics Without Current Limiting



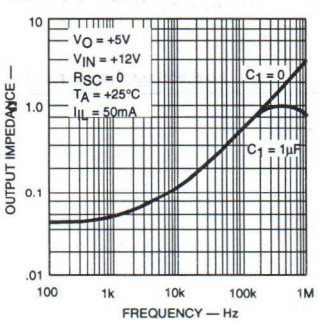
Load Transient Response



Line Regulation as a Function of Input-Output Voltage Differential

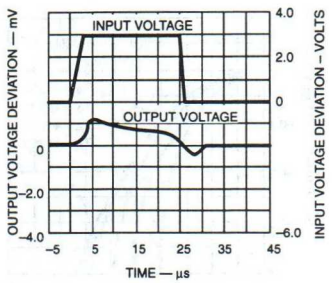


Output Impedance as a Function of Frequency

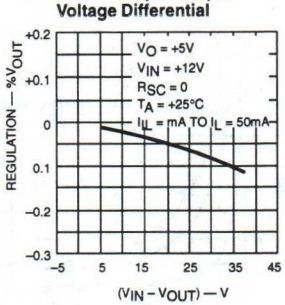


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

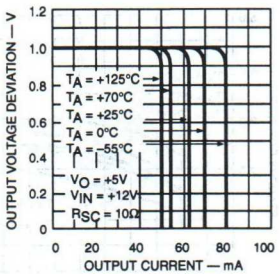
Line Transient Response



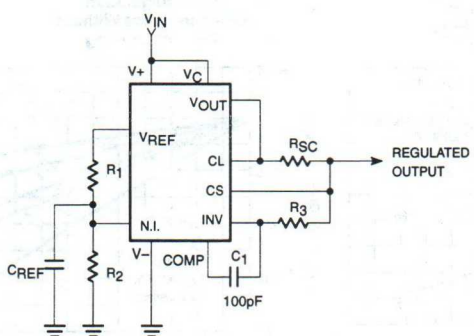
Load Regulation as a Function of Input-Output Voltage Differential



Current Limiting Characteristics



TYPICAL APPLICATIONS

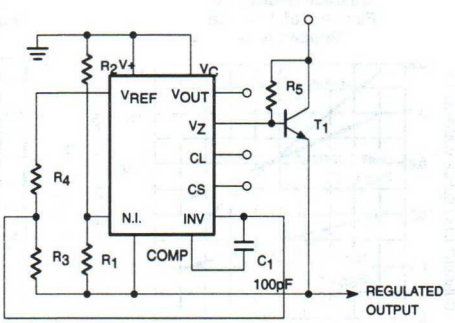


NOTES:

$$V_{OUT} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2}\right]$$

$$R_3 = \frac{R_1 R_2}{R_1 + R_2} \text{ for minimum temperature drift}$$

Low Voltage Regulator (V_{OUT} = 2 to 7V)

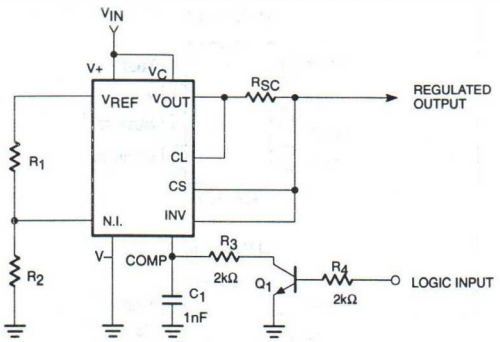


NOTE:

$$V_{OUT} = \left[\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}\right]; \; R_3 = R_4$$

Negative Voltage Regulator

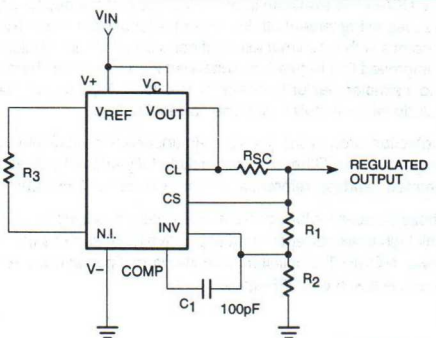
TYPICAL APPLICATIONS (Continued)



NOTE:

$$V_{OUT} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2}\right]$$

Remote Shutdown Regulator With Current Limiting (V_{OUT} = 2 to 7V)



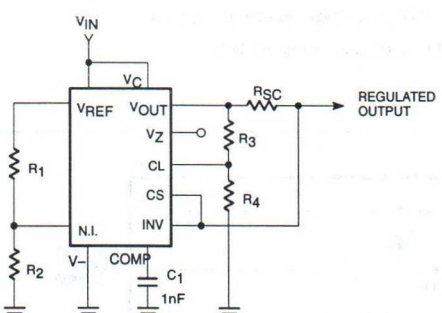
NOTE:

$$V_{OUT} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2}\right]; \quad R_3 = R_4$$

$$R_3 = \frac{R_1 R_2}{R_1 + R_2} \text{ for minimum temperature drift}$$

R3 may be eliminated for minimum component count

High Voltage Regulator (V_{OUT} = 7 to 37V)

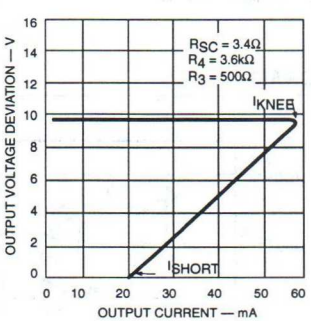


NOTES:

$$I_{KNEE} = \left[\frac{V_{OUT}\, R_3}{R_{SC}\, R_4} + \frac{V_{SENSE}\,(R_3 + R_4)}{R_{SC}\, R_4}\right]$$

$$V_{OUT} = \left[V_{REF} \times \frac{R_1 + R_2}{R_4}\right]$$

$$I_{SHORT\ CKT} = \left[\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4}\right]$$



NOTES:

$$\frac{R_4}{R_3} = \frac{V_{OUT}\, I_{SC}}{V_{SENSE}\,(I_{KNEE} - I_{SHORT\ CKT})} - 1$$

$$R_{SC} = \frac{V_{SENSE}}{I_{SC}}\left[1 + \frac{R_3}{R_4}\right]$$

Foldback Current Limiting Regulator (V_{OUT} = 2 to 7V)

Current-mode PWM controller

UC3842

DESCRIPTION

The UC3842 is available in an 8-Pin mini-DIP the necessary features to implement off-line, fixed-frequency current-mode control schemes with a minimal external parts count. This technique results in improved line regulation, enhanced load response characteristics, and a simpler, easier to design control loop. Topological advantages include inherent pulse-by-pulse current limiting.

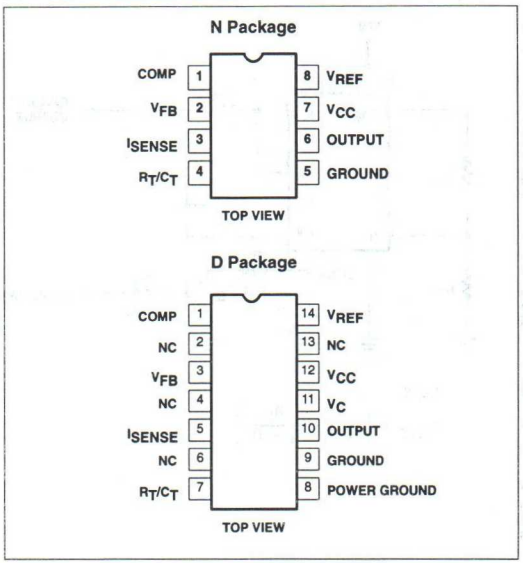
Protection circuitry includes built-in undervoltage lock-out and current limiting. Other features include fully-latched operation, a 1% trimmed bandgap reference, and start-up current less than 1mA.

These devices feature a totem-pole output designed to source and sink high peak current from a capacitive load, such as the gate of a power MOSFET. Consistent with N-channel power devices, the output is low in the OFF-state.

FEATURES

- Low start-up current (≤1mA)
- Automatic feed-forward compensation
- Pulse-by-pulse current limiting
- Enhanced load response characteristics
- Undervoltage lock-out with hysteresis
- Double pulse suppression
- High current totem-pole output
- Internally-trimmed bandgap reference
- 400kHz operation, guaranteed min

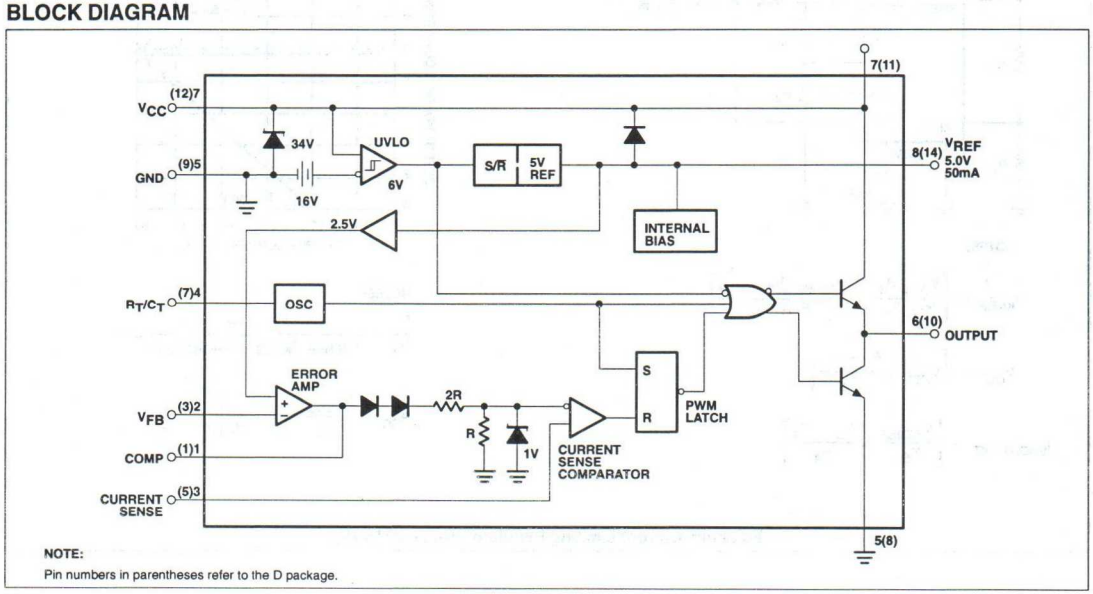
PIN CONFIGURATIONS



APPLICATIONS

- Off-line switched mode power supplies
- DC-to-DC converters UC3842

BLOCK DIAGRAM



NOTE:
Pin numbers in parentheses refer to the D package.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	UC3842N	0404B
14-Pin Plastic Small Outline (SO) Package	0 to +70°C	UC3842D	0405B

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (I_{CC}<30mA)		Self-Limiting
V_{CC}	Supply voltage (low impedance source)	30	V
I_{OUT}	Output current [2, 3]	±1	A
	Output energy (capacitive load)	5	µJ
	Analog inputs (Pin 2, Pin 3)	-0.3 to 6.3	V
	Error amp output sink current	10	mA
P_D	Power dissipation at T_A≤70°C (derate 12.5mW/°C for T_A>70°C)[2]	1	W
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead temperature (soldering, 10sec max)	300	°C

NOTES:
1. All voltages are with respect to Pin 5; all currents are positive into the specified terminal.
2. See section in application note on "Power Dissipation Calculation".
3. This parameter is guaranteed, but not 100% tested in production.

DC AND AC ELECTRICAL CHARACTERISTICS

$0 \le T_J \le 70°C$ for UC3842; V_{CC}=15V; R_T=10kW; C_T=3.3nF, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	UC3842			UNIT
			Min	Typ	Max	
Reference section						
V_{OUT}	Output voltage	T_J=25°C, I_O=1mA	4.90	5.00	5.10	V
	Line regulation	$12 \le V_{IN} \le 25V$		6	20	mV
	Load regulation	$1 \le I_O \le 20mA$		6	25	mV
	Temp. stability[1]			0.2	0.4	mV/°C
	Total output variation[1]	Line, load, temp.	4.82		5.18	V
V_{NOISE}	Output noise voltage[1]	$10Hz \le f \le 10kHz$, T_J=25°C		50		µV
	Long-term stability[1]	T_J=125°C, 1000 Hrs.		5	25	mV
	Output short-circuit	T_J=25	-30	-100	-130	mA
	Output short-circuit	$-55 < T_J \le 0°C$	-30	-100	-180	mA
Oscillator section						
	Initial accuracy	T_J=25°C	47	52	57	kHz
	Voltage stability	$12 \le V_{CC} \le 25V$		0.2	1	%
	Temp. stability[1]	$T_{MIN} \le T_J \le T_{MAX}$		5		%
	Amplitude	$V_{PIN\ 4}$ peak-to-peak		1.7		V
Error amp section						
	Input voltage	V Pin 1=2.5V	2.42	2.50	2.58	V
I_{BIAS}	Input bias current			-0.3	-2	µA
A_{VOL}		$2 \le V_O \le 4V$	65	90		dB
	Unity gain bandwidth[1]	T_J=25°C	0.7	1		MHz
	Unity gain bandwidth	$T_{MIN} < T_J < T_{MAX}$	0.5			MHz
PSRR	Power supply rejection ratio	$12 \le V_{CC} \le 25V$	60	70		dB
I_{SINK}	Output sink current	$V_{PIN\ 2}$=2.7V, $V_{PIN\ 1}$=1.1V	2	6		mA
I_{SOURCE}	Output source current	$V_{PIN\ 2}$=2.3V, $V_{PIN\ 1}$=5V	-0.5	-0.8		mA
	V_{OUT} High	$V_{PIN\ 2}$=2.3V, R_L=15k to ground	5	6		V
	V_{OUT} Low	$V_{PIN\ 2}$=2.7V, R_L=15k to Pin 8		0.7	1.1	V
Current sense section						
	Gain [2, 3]		2.85	3	3.15	V/V
	Maximum input signal[2]	$V_{PIN\ 1}$=5V	0.9	1	1.1	V
PSRR	Power supply rejection ratio[2]	$12 \le V_{CC} \le 25V$		70		dB
I_{BIAS}	Input bias current			-2	-10	µA
	Delay to output[1]			150	300	ns

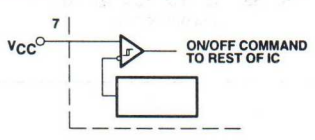
DC AND AC ELECTRICAL CHARACTERISTICS

$0 \le T_J \le 70°C$ for UC3842; V_{CC}=15[4]; R_T=10kΩ; C_T=3.3nF, unless otherwise specified

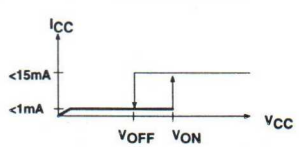
SYMBOL	PARAMETER	TEST CONDITIONS	UC3842			UNIT
			Min	Typ	Max	
Output section						
V_{OL}	Output Low-Level	I_{SINK}=20mA		0.1	0.4	V
		I_{SINK}=200mA		1.5	2.2	
V_{OH}	Output High-Level	I_{SOURCE}=20mA	13	13.5		V
		I_{SOURCE}=200mA	12	13.5		
t_R	Rise time	C_L=1nF		50	150	ns
t_F	Fall time	C_L=1nF		50	150	ns
Undervoltage lockout section						
	Start threshold		14.5	16	17.5	V
	Min. operating voltage after turn on		8.5	10	11.5	V
PWM section						
	Maximum duty cycle		93	97	100	%
	Minimum duty cycle				0	
Total standby current						
	Start-up current			0.5	1	mA
I_{CC}	Operating supply current	$V_{PIN\ 2}$=$V_{PIN\ 3}$=0V		11	17	mA
	V_{CC} zener voltage	I_{CC}=25mA		34		V
Maximum operating frequency section						
	Maximum operating frequency for all functions operating cycle-by-cycle		400			kHz

NOTES:
1. These parameters, although guaranteed, are not 100% tested in production.
2. Parameter measured at trip point of latch with $V_{PIN\ 2}$=0.
3. Gain defined as: $A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}$; $0 \le V_{PIN\ 3} \le 0.8V$

UNDERVOLTAGE LOCKOUT

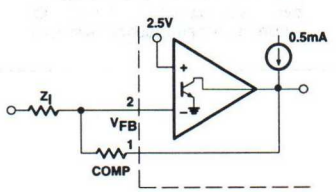


	UC3842
V_{ON}	16V
V_{OFF}	10V



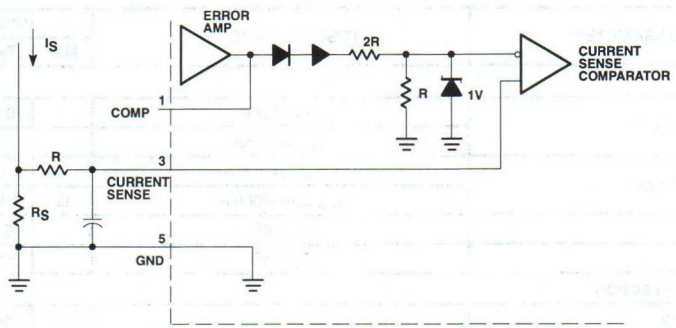
NOTE:
During Undervoltage Lock-Out, the output driver is biased to a high impedance state. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with output leakage current.

ERROR AMP CONFIGURATION



NOTE:
Error AMP can source or sink up to 0.5mA.

CURRENT SENSE CIRCUIT



NOTE:

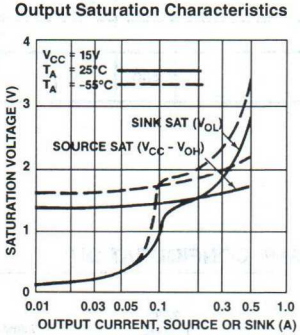
Peak current (I_S) is determined by the formula:

$$I_{S\ MAX} = \frac{1.0V}{R_S}$$

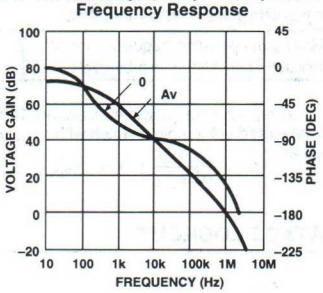
A small RC filter may be required to suppress switch transients.

TYPICAL PERFORMANCE CHARACTERISTICS

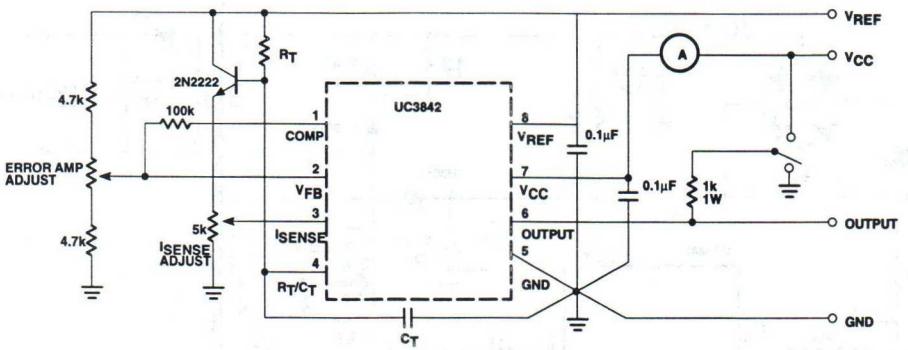
Output Saturation Characteristics



Error Amplifier Open-Loop Frequency Response

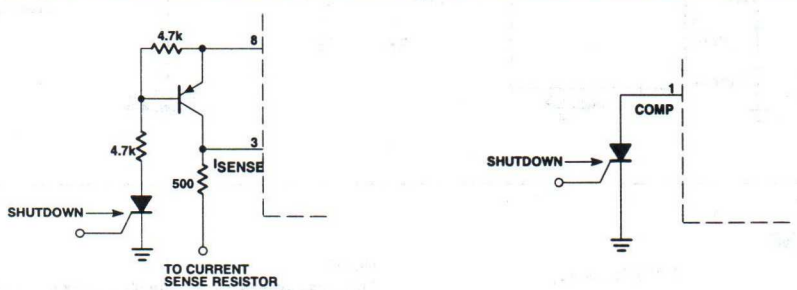


OPEN-LOOP LABORATORY TEST FIXTURE



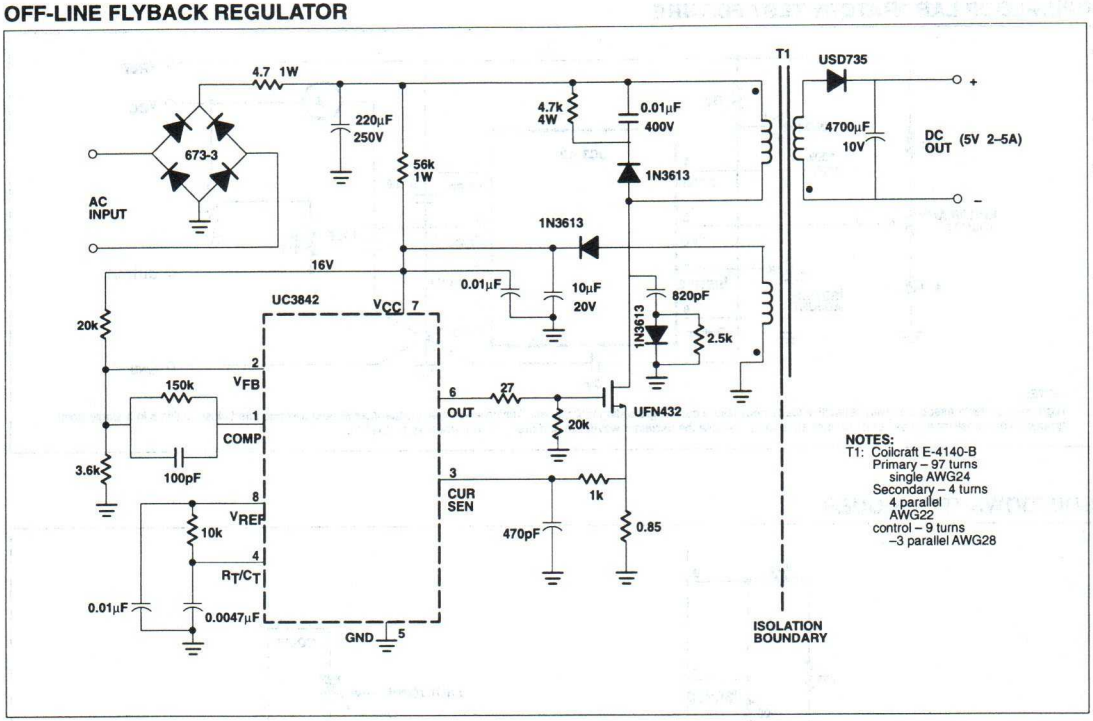
NOTE:
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Pin 3.

SHUTDOWN TECHNIQUES



NOTE:
Shutdown of the UC3842 can be accomplished by two methods; either raise Pin 3 above 1V or pull Pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to Block Diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at Pins 1 and/or 3 is removed. In the examples shown, an externally-latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower UVLO threshold (10V). At this point all internal bias is removed, allowing the SCR to reset.

OFF-LINE FLYBACK REGULATOR

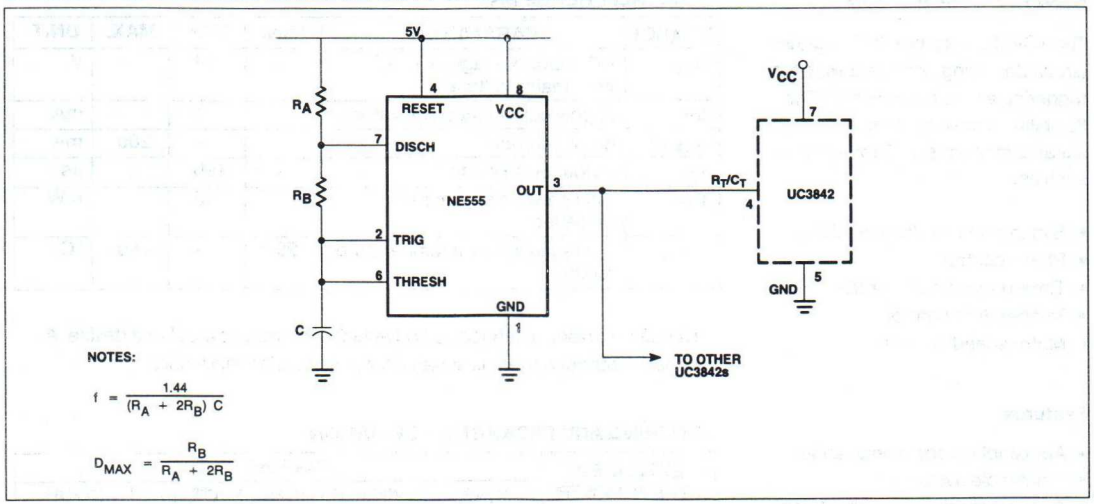


SPECIFICATIONS

Input line voltage:	$90V_{AC}$ to $130V_{AC}$
Input frequency:	50 or 60Hz
Switching frequency:	40kHz±10%
Output power:	25W maximum
Output voltage:	5V±5%
Output current:	2 to 5A
Line regulation:	0.01%/V
Load regulation:	8%/A*
Efficiency @ 25 W,	
$V_{IN}=90V_{AC}$:	70%
$V_{IN}=130V_{AC}$:	65%
Output short-circuit current:	2.5A average

NOTE:
This circuit uses a low-cost feedback scheme in which the DC voltage developed from the primary-side control winding is sensed by the UC3842 error amplifier. Load regulation is therefore dependent on the coupling between secondary and control windings, and on transformer leakage inductance. For applications requiring better load regulation, a UC1901 Isolated Feedback Generator can be used to directly sense the output voltage.

SYNCHRONIZATION AND MAXIMUM DUTY CYCLE CLAMP



NOTES:

$$f = \frac{1.44}{(R_A + 2R_B)\,C}$$

$$D_{MAX} = \frac{R_B}{R_A + 2R_B}$$

General-purpose triggering circuit

TCA280B

GENERAL DESCRIPTION

The TCA280B is a bipolar integrated circuit delivering positive pulses for triggering a triac or a thyristor. The flexibility of the circuit makes it suitable for a variety of applications, such as:

- Synchronous on/off switching
- Phase control
- Time-proportional control
- Temperature control
- Motor speed control

Features

- Adjustable proportional range
- Adjustable hysteresis
- Adjustable firing burst repetition time
- Adjustable pulse width
- Supplied from the mains
- Provides supply for external temperature bridge
- Low supply current, low dissipation

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage (derived from mains voltage)	-	14	-	V
I_{CC}	supply current (average value)	-	1	-	mA
$-I_{QAH}$*	output current	-	-	200	mA
t_W	output pulse width	-	190	-	µs
P_{tot}	total power dissipation, unloaded	-	15	-	mW
T_{amb}	operating ambient temperature range	−20	-	+80	°C

* Negative current is defined as conventional current flow out of a device. A negative output current is suitable for positive triac triggering.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TCA280B	16	DIL	plastic	SOT38

General-purpose triggering circuit TCA280B

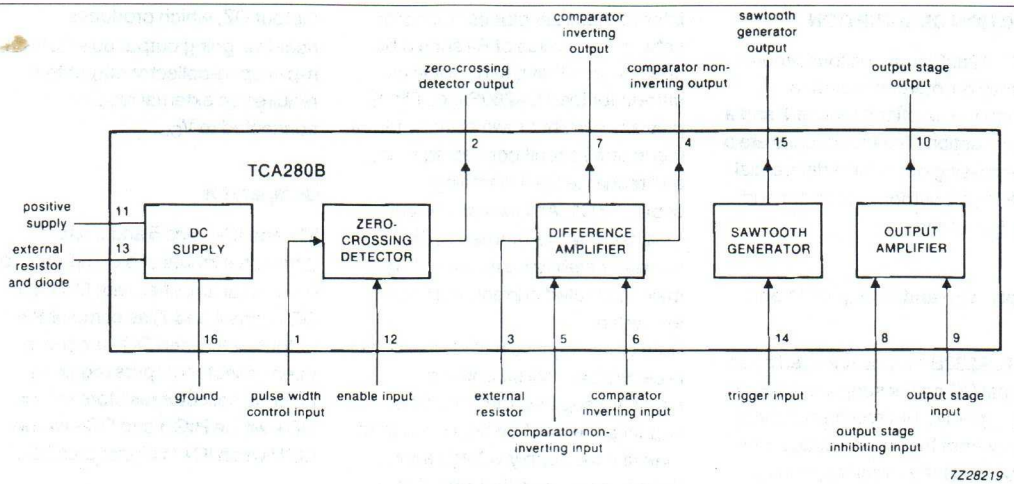


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
PW	1	pulse width control input
QZ	2	zero-crossing detector output
RX1	3	external resistor
QC+	4	comparator non-inverting output
IC+	5	comparator non-inverting input
IC−	6	comparator inverting input
QC−	7	comparator inverting output
INHA	8	output stage inhibiting input
IA	9	output stage input
QA	10	output stage output
V_{CC}	11	positive supply
ENZ	12	enable input, zero crossing detector
RX2	13	external resistor and diode
IS	14	sawtooth generator trigger input
QS	15	sawtooth generator output
V_{EE}	16	ground

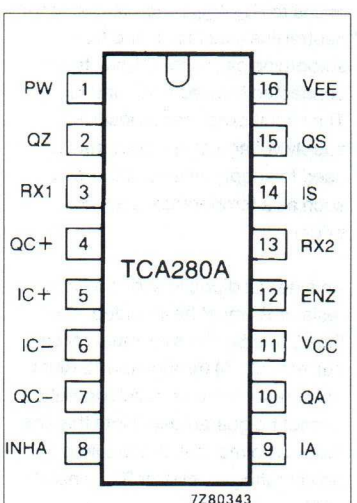


Fig.2 Pin configuration.

General-purpose triggering circuit TCA280B

FUNCTION DESCRIPTION

The TCA280B contains four circuits, that may be interconnected to perform the functions required, and a supply section. The four circuits are a zero-crossing detector, a differential amplifier, a sawtooth generator and an output stage.

Supply: V_{CC} and RX2 (pins 11 and 13)

The TCA280B may be supplied by an external DC power supply connected to V_{CC} (pin 11), but can be supplied directly from the mains voltage. For this purpose the circuit contains a number of stabilizer diodes, and a transistor connected between V_{CC} and V_{EE}, that limit the DC supply voltage. An external resistor R_d and an external diode (mains voltage rated) has to be connected from the mains to R_{X2}; V_{EE} is connected to the neutral line (see Figs 5 and 6). A smoothing capacitor C1 has to be connected between V_{CC} and V_{EE}. The circuit produces a positive supply voltage at V_{CC}, this may be used to supply an external circuit such as a temperature sensing bridge.

An external diode in series with the resistor R_d must be included (see Figs 5 and 6). The maximum reverse current (10 μA) through pin 13 must not be exceeded or circuit operation cannot be guaranteed. Note that the diode also reduces the required power rating of resistor R_d by nearly 50%.

During the positive half of the mains cycle the current through the external voltage dropping resistor R_d charges the external smoothing capacitor C1 to the stabilizing voltage of the internal stabilizer diodes/transistor network. The value of R_d should be chosen such that it can supply the current for the TCA280B (see Fig.4) plus any current drawn by an external (peripheral) circuit connected to V_{CC} and recharge the smoothing capacitor C1. Any excess current is bypassed by the internal diode/ transistor stabilizing network. The maximum rated current must not be exceeded.
During the negative half of the mains cycle the external smoothing capacitor supplies the circuit. Its capacitance must be high enough to maintain the supply voltage above the minimum specified limit. For values of R_d and C1 see Figs 5 and 6.

A suitable VDR connected across the mains provides protection for the TCA280B and the triac against mains-borne transients.

Zero-crossing detector

The TCA280B contains a zero-crossing detector to produce pulses that coincide with the zero crossings of the mains voltage for minimum RF interference and transients on the mains supply.

The pulse width control input PW (pin 1) allows adjustment of the pulse width at output QZ (pin 2), to the value required for the triac, by choosing the value of the external synchronization resistor R_S between PW and the AC mains. The pulse width is inversely proportional to the input current and to the mains frequency.

The zero-crossing detector is inhibited when the ENZ input (pin 12) is HIGH, and enabled when ENZ is LOW, e.g. connected to V_{EE}.

Output QZ, which produces negative-going output pulses, is an n-p-n open-collector output that requires an external resistor connected to V_{CC}.

Comparator

IC+ and IC– (pins 5 and 6) are differential inputs of a comparator or differential amplifier, with QC+ and QC– (pins 4 and 7) as complementary outputs. QC+ and QC– are p-n-p open collector outputs requiring external collector resistors to V_{EE}. QC+ will be HIGH and QC– will be LOW when IC+ is higher than IC–.

The comparator contains a long-tailed pair with a current source in its tail. The tail current is activated by a current into RX1 (pin 3). When an inductive load is driven with phase control the trigger pulse may be terminated at the instant of firing of the thyristor or triac. This may be achieved by connecting RX1 via a resistor to the anode of the thyristor or triac.

Sawtooth generator

The sawtooth generator may be used to produce bursts of trigger pulses, with the net effect that the load is periodically switched on and off.

The heart of the sawtooth generator is a thryristor arrangement. The firing burst repetition time is usually determined by an external resistor and capacitor connected to the sawtooth generator trigger input IS (pin 14). The repetition time is typical 0.7 x RC.

FUNCTIONAL DESCRIPTION

(continued)

The output QS (pin 15) is an n-p-n open-collector output. During the flyback period of the sawtooth pulse the transistor is ON and is capable of sinking current.

Output stage

The output stage is driven by current drawn from input IA (pin 9). This drive may be inhibited by drawing current from inhibiting input INHA (pin 8). Hence the output will be HIGH only if current is drawn from IA and no current is from of INHA i.e. if inhibiting input INHA (pin 8) is HIGH and input IA (pin 9) is LOW. Both inputs may be used as a single input provided the other one is suitably biased.

The output QA (pin 10) is an n-p-n open-emitter output capable of sourcing an output current, i.e. conventional current flow out of the circuit.

A gate resistor R_G should be connected between the output QA and the triac or thyristor gate to limit the output current to the minimum required by the triac or thyristor. This minimizes the total supply current and the power dissipation. Output QA is protected with a diode to V_{EE} (pin 16) against damage by undershoot of the output voltage, e.g. caused by an inductive load.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage (voltage source) supply current (current source)		-	17	V
$I_{RX2(AV)}$	average		-	17	mA
$I_{RX2(RM)}$	repetitive peak		-	80	mA
$I_{RX2(SM)}$	non-repetitive peak	$t < 10\ \mu s$	-	2	A
$I_{RX2(RV)}$	reverse		-	−10	μA
V_I	input voltage, all inputs		-	17	V
V_{ID}	differential input voltage between IC+ and IC−		-	7	V
I_I	input current, all inputs		-	10	mA
	output current				
$I_{QA(AV)}$	average		−30	-	mA
$I_{QA(SM)}$	non-repetitive peak	$t < 300\ \mu s$	−600	-	mA
P_{tot}	total power dissipation	see Fig.3			
T_{stg}	storage temperature range		−55	+125	°C
T_{amb}	operating ambient temperature range		−20	+80	°C

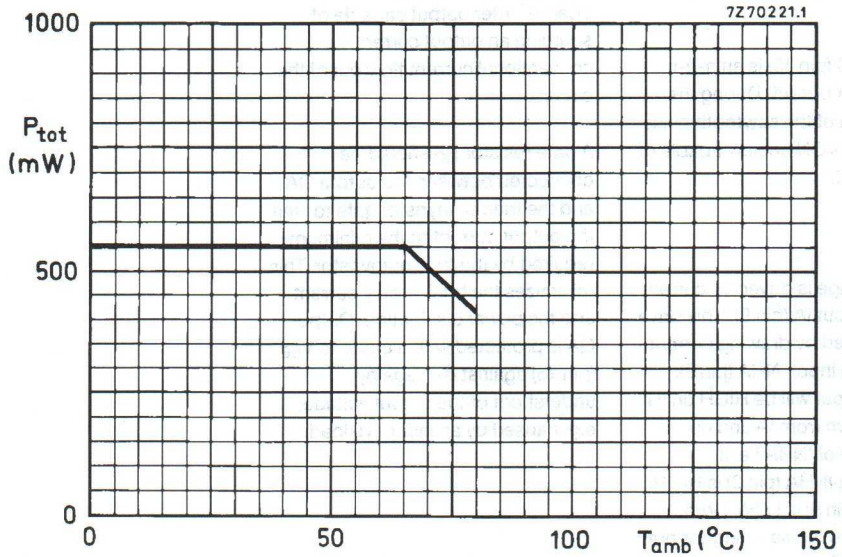


Fig.3 Power derating curve.

CHARACTERISTICS

V_{CC} = 11 to 17 V; V_{EE} = 0 V; I_{RX1} = 10 µA or I_{RX1} = −30 µA;
T_{amb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage, external		11	-	17	V
V_{CC}	supply voltage, internally generated	$I_{RX2(RMS)}$ = 5 mA, unloaded	11.0	14.3	15.0	V
I_{CC}	supply current, unloaded		0.3	-	0.75	mA
$\Delta I_{CC}/\Delta V_{CC}$	variation with supply voltage		-	-	0.03	mA/V
Pulse width control input PW (pin 1)						
	input voltage					
V_{PW}		I_{PW} = 100 µA	-	-	1.9	V
V_{PW}		I_{PW} = −100 µA	−0.25	-	-	V
$I_{PW(RMS)}$	input current(RMS value)	I_{QZ} = 0.5 mA	30	-	50	µA
t_w	pulse width	$I_{PW(RMS)}$ f = 50 Hz (at pin 2)	-	190	-	µs
$\Delta t/\Delta V$	variation with supply voltage		-	27	-	µs/V
Zero crossing detector enable input ENZ (pin 12)						
V_{ENZH}	input voltage HIGH	inhibit	1.2	-	-	V
V_{ENZL}	input voltage LOW	enable	-	-	0	V

CHARACTERISTICS (continued)

Zero crossing detector output QZ (pin 2)						
I_{QZH}	output current HIGH		−1	-	-	μA
I_{QZL}	output current LOW		-	-	−40	mA
Comparator input IC+ and IC− (pins 5 and 6)						
$\pm V_{ID}$	differential input voltage		-	-	7	V
I_{IC+}	input bias current	$V_{IC+} > V_{IC-} + 1$ V	-	5	10	μA
I_{IC-}		$V_{IC-} > V_{IC+} + 1$ V	-	5	10	μA
Comparator outputs QC+ and QC− (pins 4 and 7)						
V_{OH}	output voltage	$I_{OH} = -0.3$ mA	$V_{CC}-1.5$	-	-	V
I_{OH}	output current HIGH		-	-	−0.3	mA
I_{OL}	output current LOW		−90	-	-	nA
Sawtooth generator trigger input IS (pin 14)						
V_{ISH}	input trigger voltage		7.0	-	8.3	V
I_{ISH}	input trigger current		-	-	3	μA
V_{ISL}	thyristor holding voltage		1.8	-	2.8	V
I_{ISL}	thyristor holding current		95	-	210	μA
Sawtooth generator output QS (pin 15)						
I_{QSL}	output current LOW		-	-	−5	mA
I_{QSH}	output current HIGH		−100	-	-	nA
Output stage inhibiting input INHA (pin 8)						
I_{INHA}	input current	$I_{IA} = -100$ μA	−50	-	−20	μA
V_{INHA}	input voltage	$I_{IA} = -100$ μA	-	$V_{CC}-2$	-	V
Output stage input IA (pin 9)						
I_{IA}	input current	$I_{QA} = -200$ mA	-	-	15	μA
V_{IA}	input voltage	$I_{IA} = -50$ μA	$V_{CC}-8.3$	-	$V_{CC}-7$	V
Output stage output (pin 10)						
V_{QAH}	output voltage HIGH	$I_{QAH} = -200$ MA $V_{CC} = 13$ V INHA open-circuit	$V_{CC}-2.8$	-	-	V
I_{QAH}	output current HIGH		−200	-	-	mA
I_{QAL}	output current LOW		-	-	1	μA

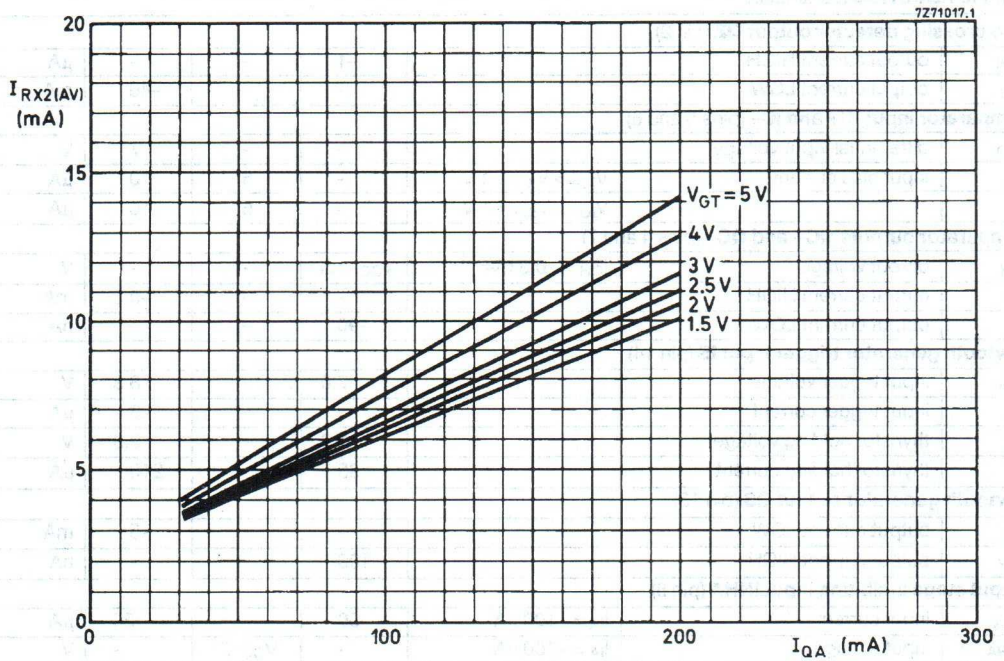
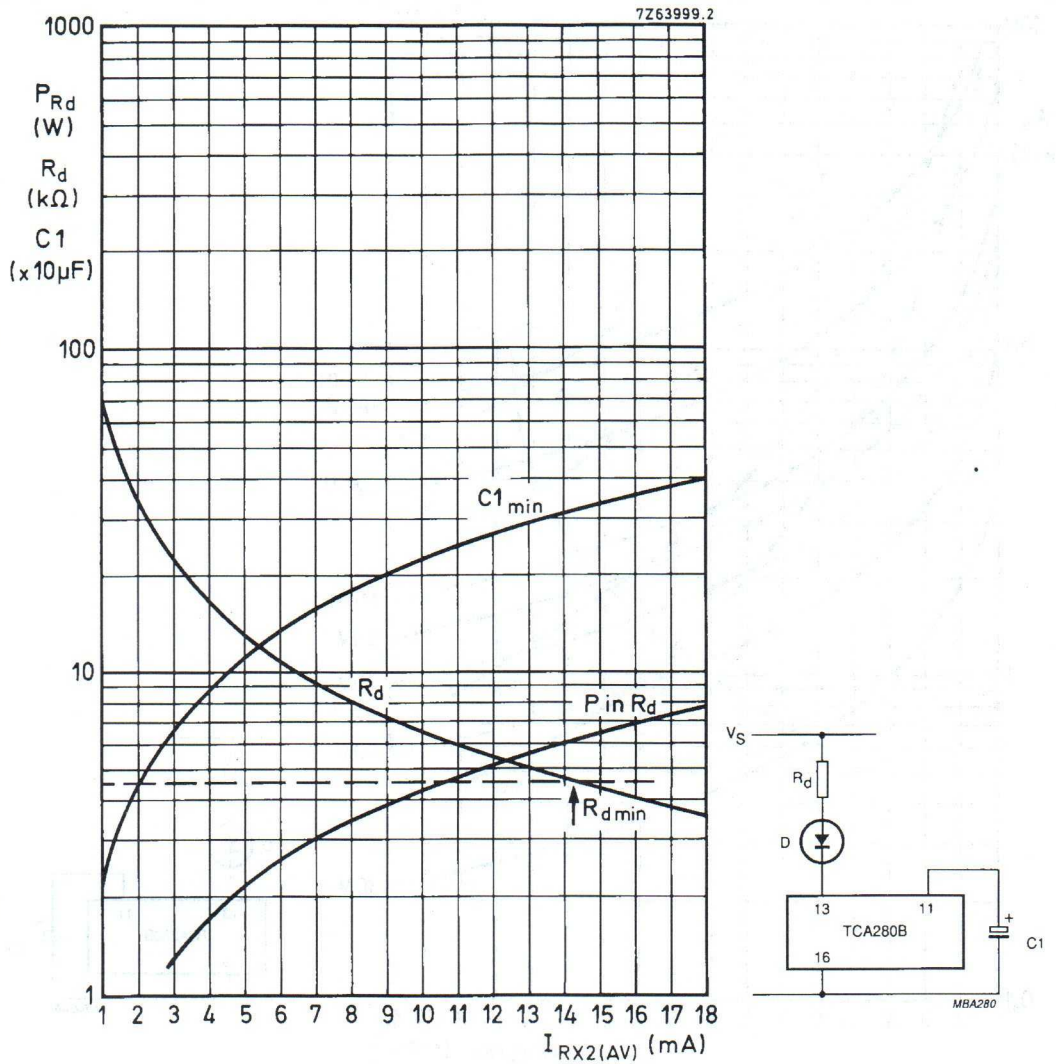
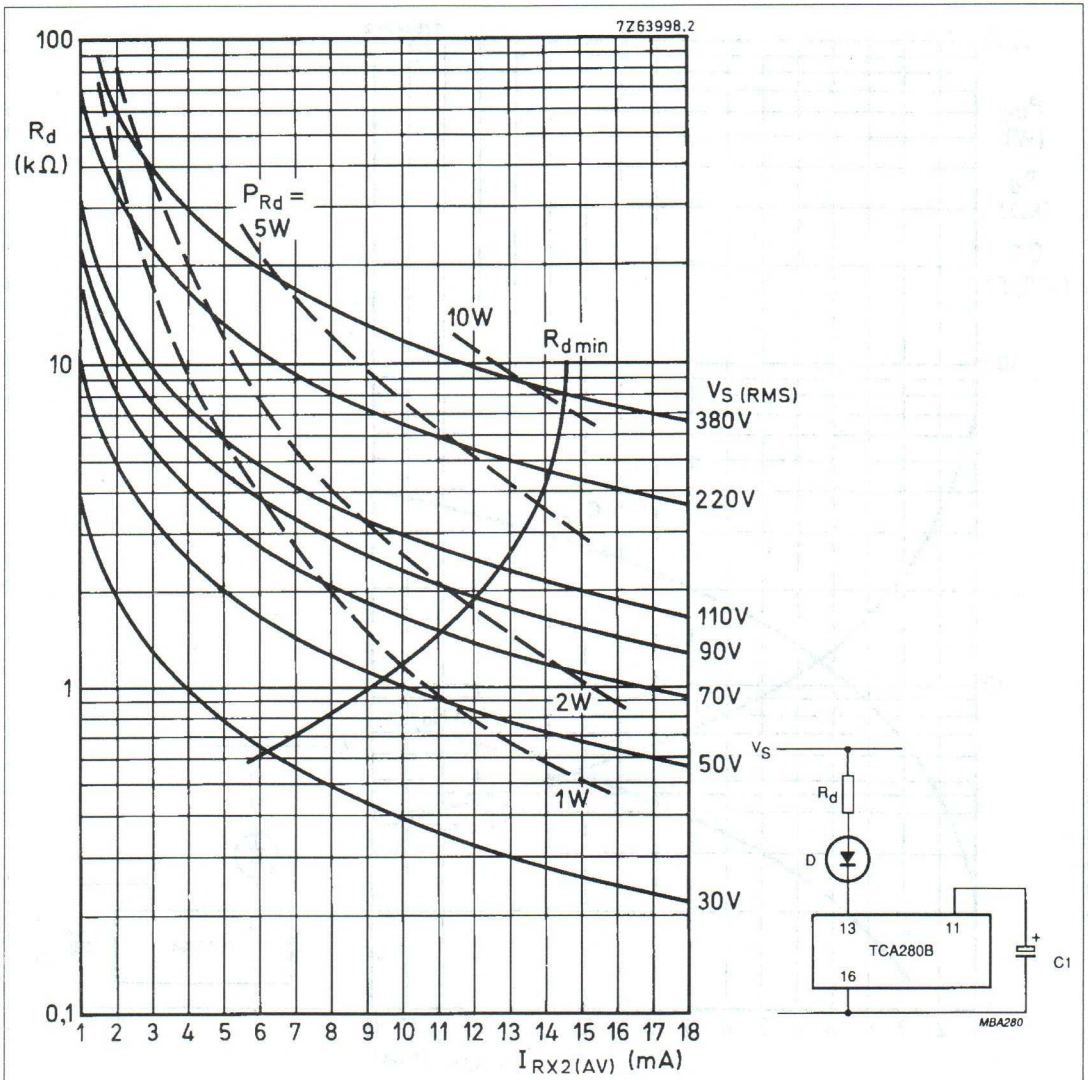


Fig.4 Average supply current $I_{RX2(AV)}$ as a function of output current I_{QA} with triac gate trigger voltage V_{GT} as a parameter; typical performance.



Note: In certain applications the time proportional controller requires a value of smoothing capacitor (C1) three times higher; typical performance.

Fig.5 Voltage dropping resistor R_d, dissipation P_{Rd} in this resistor, and recommended minimum value of smoothing capacitor C1 as a function of average supply current $I_{RX2(AV)}$, for the supply arrangement with series diode D. $I_{RX2(AV)}$ includes the supply of any external (peripheral) circuit supplied from V_{CC}.



Note: $I_{RX2(AV)}$ includes the supply current of any external (peripheral) circuit supplied from V_{CC}.

Fig.6 Voltage dropping resistor R_d and power dissipation P_{Rd} in this resistor as a function of supply current $I_{RX2(AV)}$, for the supply arrangement with series diode. Also shown is the RMS mains supply voltage ($V_{S(RMS)}$) as a function of $I_{RX2(AV)}$; typical performance.

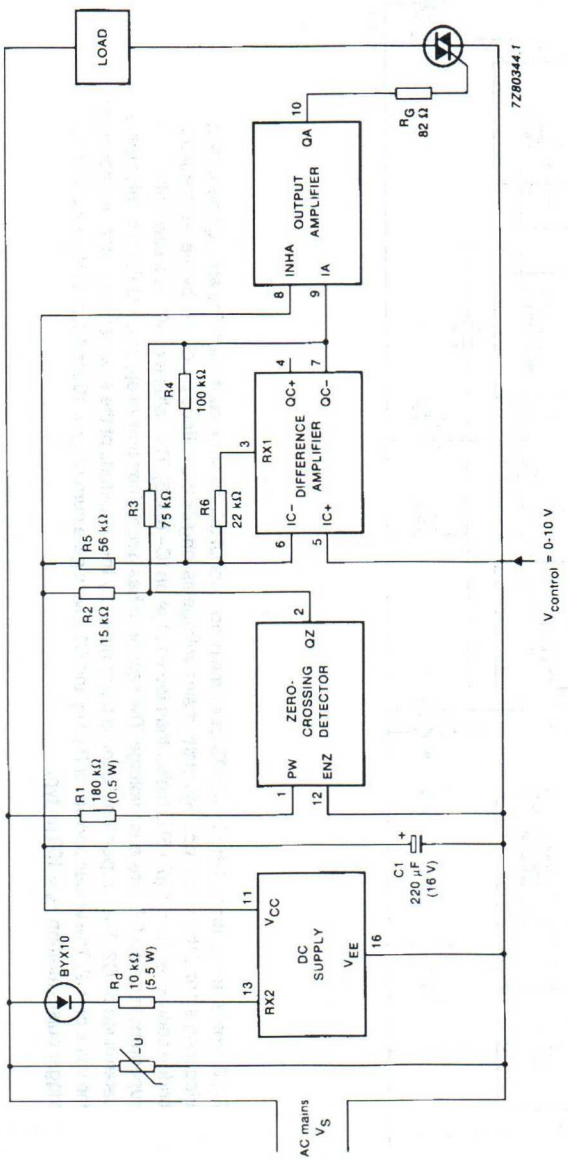


Fig.7 Typical application of the TCA280B as a static switch for resistive loads. The arrangement gives triggering around the zero crossings of the mains voltage. The values shown for R_d, R_G and C1 give a gate current I_{GT} = 100 mA typical at V_{GT} = 2.5 V and a trigger pulse duration t_w = 160 µs typical.

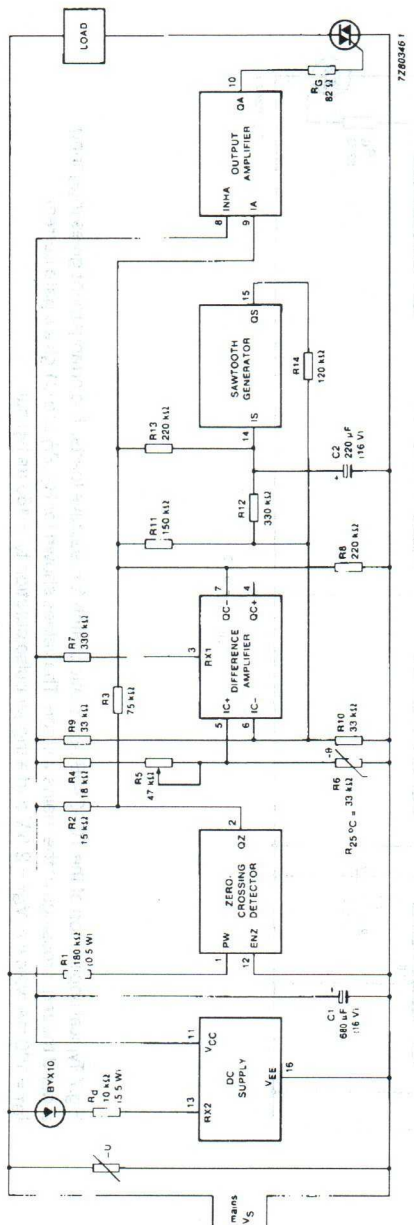


Fig.8 Typical application of the TCA280B as a time proportional temperature controller. The arrangement gives triggering around the zero crossings of the mains voltage as long as the voltage produced by the temperature bridge connected to IC+ (pin 5) is higher than the voltage on IC− (pin 6). The voltage on IC− is a sawtooth superimposed on a DC reference voltage. The sawtooth has a repetition time of approximately 30 s; this time is determined by C2. The proportional band is determined by the amplitude of the sawtooth; this can be chosen by the value of R12. The values shown for R_d, R_G and C1 give a gate current I_{GT} = 100 mA typ. at V_G = 2.5 V and a trigger pulse duration t_W = 160 µs typ.

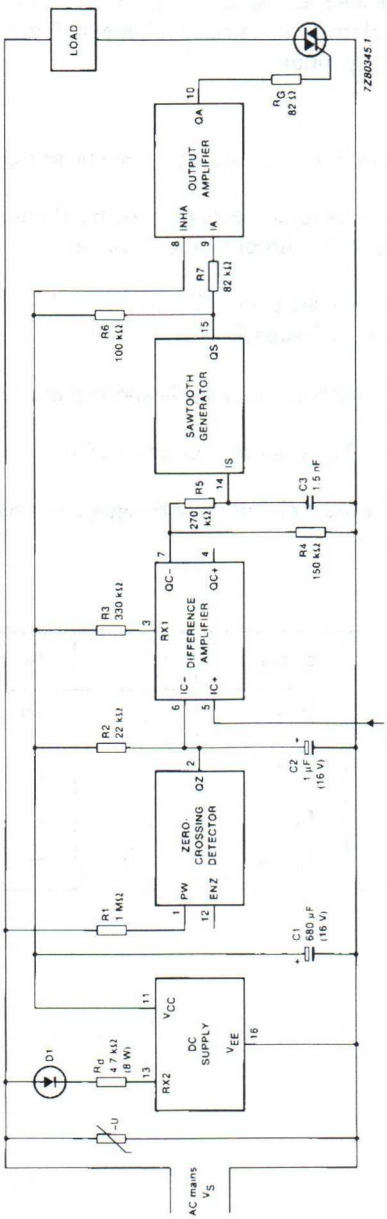


Fig.9 Typical application of the TCA280B as a single-phase control circuit. The circuit produces bursts of trigger pulses at the gate of the triac of thyristor. The pulses coincide with the zero crossings of the mains voltage. The arrangement forms a full-wave AC controller when used with a triac, and a controlled half-wave rectifier when used with a thyristor.

Control circuit for switched-mode power supplies — TDA8380

GENERAL DESCRIPTION

The TDA8380 is an integrated circuit intended for use as a control circuit in low-cost switched mode power supplies for television, monitors and small industrial equipment. The TDA8380 operates using duty factor regulation in the fixed frequency mode.

Features

- A low-current initialization circuit (maximum 150 μA) which can be switched off
- A bandgap reference generator
- Circuitry for slow-start combined with an accurate setting of the maximum duty factor (D_{max})
- Programmable low supply voltage protection with one default value
- High supply protection circuitry
- Error amplifier with a transfer characteristic generator (TCG)
- Protection against open- and short-circuited feedback loop
- An overload voltage foldback
- Primary current protection circuitry for both cycle-by-cycle and trip mode
- Protection against transformer saturation
- A direct drive output stage (sink current 2.5 A, source current 0.75 A)
- Anti-double pulse logic
- Protected against damage as a result of a short-circuited high-voltage transistor
- RC oscillator with synchronization input

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	–	14	–	V
Supply current	I_{CC}	–	–	15	mA
Output pulse repetition frequency range	f_o	10	–	100	kHz
Operating ambient temperature range	T_{amb}	−25	–	+ 70	°C

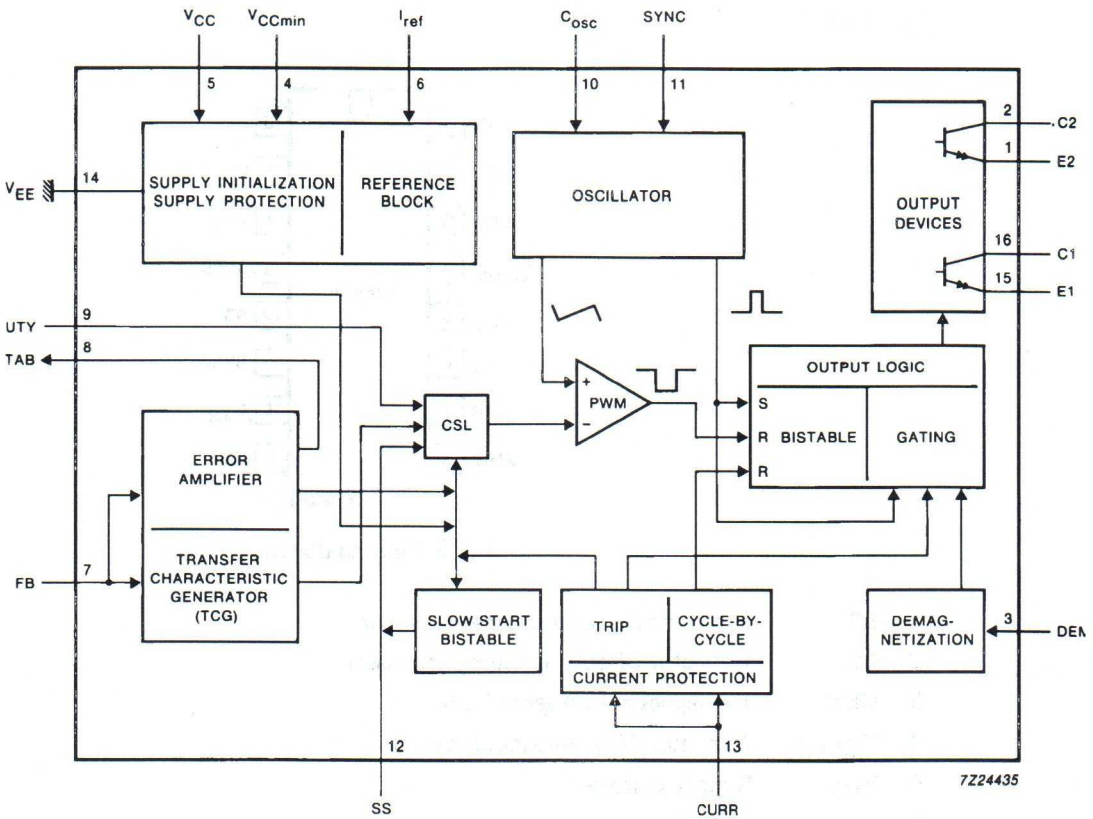


Fig.1 Block diagram.

PINNING

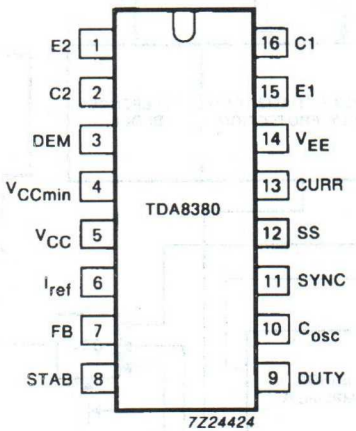


Fig.2 Pinning diagram.

1	E2	Emitter of output source transistor
2	C2	Collector of output source transistor
3	DEM	Demagnetization sense input
4	V_{CCmin}	Minimum V_{CC} threshold setting
5	V_{CC}	Supply voltage
6	I_{ref}	Reference current setting
7	FB	Feedback input
8	STAB	Output error amplifier
9	DUTY	Pulse width modulator input
10	C_{OSC}	Oscillator capacitor
11	SYNC	Synchronization input
12	SS	Maximum duty factor (D_{max}) setting plus slow-start
13	CURR	Input current protection
14	V_{EE}	Ground
15	E1	Emitter of output sink transistor
16	C1	Collector of output sink transistor

FUNCTIONAL DESCRIPTION

The TDA8380 is a control circuit which generates the pulses required to drive the switching transistor in a switched mode power supply (SMPS).

Supply

This device is intended to be used on the primary side of the power supply and can be supplied via a take-over (auxiliary) winding on the transformer.

The device is initialized via a high value resistor connected between the rectified mains voltage and the device's supply pin (pin 5), which causes the capacitor connected to this pin to charge slowly. When the voltage exceeds the initialization level (typically 17 V) the device will start up and the duty cycle will be slowly increased by the slow-start circuit. After a short period the take-over winding will supply the device. The value of the resistor is normally defined by the time taken to charge the capacitor. A one second delay between switching on and operation of the power supply is acceptable in most cases.

The operating voltage range is from 9 to 20 V. The supply pin is protected by a 23 V Zener diode. The supply protection circuit is activated once the Zener diode is conducting. The slow-start procedure begins after initialization, until then the output is off. The current drawn by the device during the initialization period is less than 150 μA.

When the supply voltage falls below the minimum trip level, the device switches off and the start-up procedure is repeated. The minimum voltage supply threshold setting (V_{CCmin}) can be set externally with a resistor connected between the V_{CCmin} pin (pin 4) and ground (pin 14) (see Fig.3).

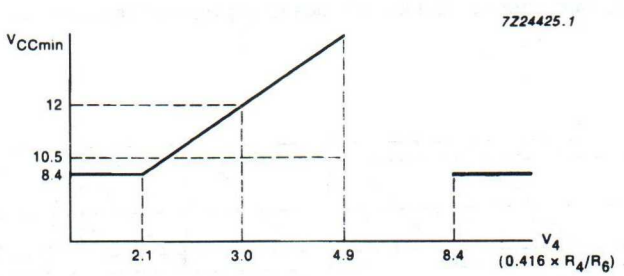


Fig.3 Trip level setting of minimum V_{CC} protection level.

V_{CCmin} can be set between 8.4 V (an internally fixed overriding protection level) and 17 V by means of an external resistor connected to pin 4.

When choosing the initialization and minimum supply voltages the following should be taken into account:

- The difference between the two voltages should be large enough to enable a supply voltage dip during start-up.
- The value of the minimum supply voltage should be high enough to ensure that the high-voltage transistor is correctly driven. A high protection level makes it possible to have a large resistor value in series with the base drive.

For battery line input operation, the V_{CCmin} pin is connected to V_{CC}, the start-up circuit is then inhibited and the device starts operating when V_{CC} exceeds the 8.4 V protection level (this level has a hysteresis of approximately 50 mV). The device draws current continuously under these conditions.

Reference block

A bandgap based reference generates a stabilized voltage of 7 V to supply most of the device's internal circuits, this decreases chip size and increases reliability. The only circuits connected to V_{CC} are:

- The initialization circuit
- The output circuitry
- The series transistor of the stabilized voltage

By means of a resistor (R_6) connected to the I_{ref} input a reference current is defined which determines six other device settings.

Part of the reference current is used to charge the oscillator capacitor (C_{10}), therefore, the charging time is proportional to $R_6 \times C_{10}$. The maximum duty factor (D_{max}) is set by the resistor connected to pin 12 (R_{12}) and is defined by the ratio R_6/R_{12}. The minimum supply voltage (pin 5) set by the resistor (R_4) at input V_{CCmin} is defined by: $4/6 \times V_6 \times R_4/R_6$.

Oscillator

The oscillator capacitor is charged and discharged between the high and low voltage levels as defined by the bandgap reference (high voltage typically 5 V and low voltage typically 1.4 V). The charge current is 1/6 of the reference current, the discharge current having the same value as the reference current. The period is therefore defined by $10 \times R_6 \times C_{10}$.

The oscillator flyback pulse is used to set the bistable in the output logic, however the output remains low until the positive ramp starts (see Fig.4). The oscillator can be synchronized by means of the SYNC pin. When this pin is connected to V_{CC}, the oscillator is free running. When it is between 0.85 and 5.6 V, the oscillator stops at the low voltage level prior to the next positive ramp.

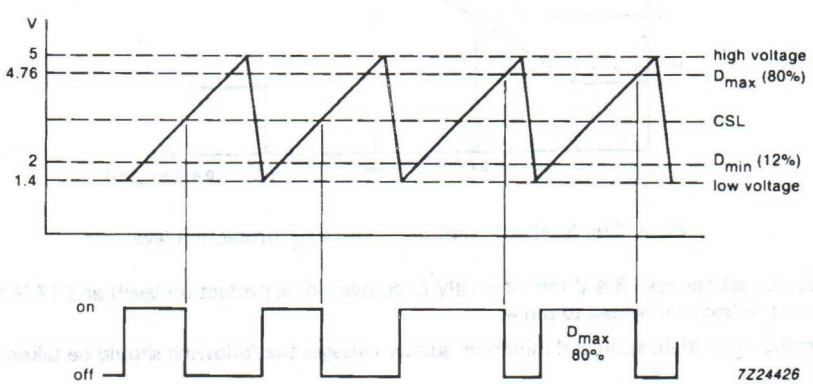


Fig.4 Oscillator levels.

FUNCTIONAL DESCRIPTION (continued)

Synchronization

The synchronization input (pin 11) can be driven by either an optocoupler or a loosely coupled pulse transformer.

Figure 5(a) illustrates synchronization using the 0.85 V threshold and a digital signal connected to the SYNC input (for example, an optocoupler between pin 11 and V_{CC}); the duty factor of the pulse is not very important. The oscillator starts at the first negative going edge of the sync. signal after the low voltage level has been reached. The synchronization frequency must be lower than the free running frequency. Synchronization must never affect the period time as this will corrupt the setting of the maximum duty factor.

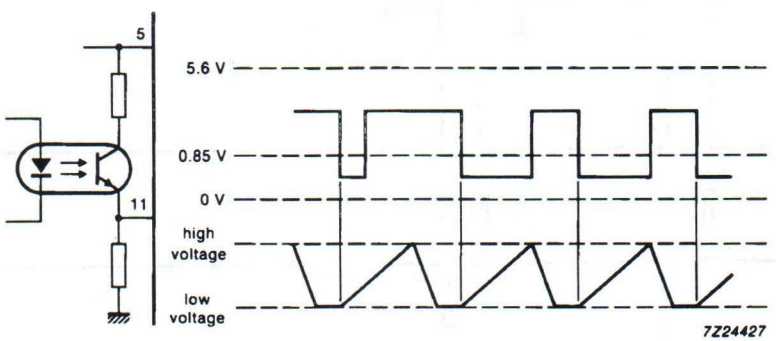


Fig. 5(a) DC coupled synchronization using the 0.85 V level.

In Fig.5(b) the disabling threshold (5.6 V) is used for synchronization. In this case the oscillator starts at the positive going edge of the sync. signal.

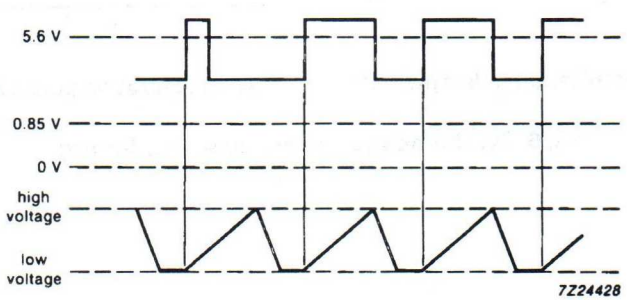
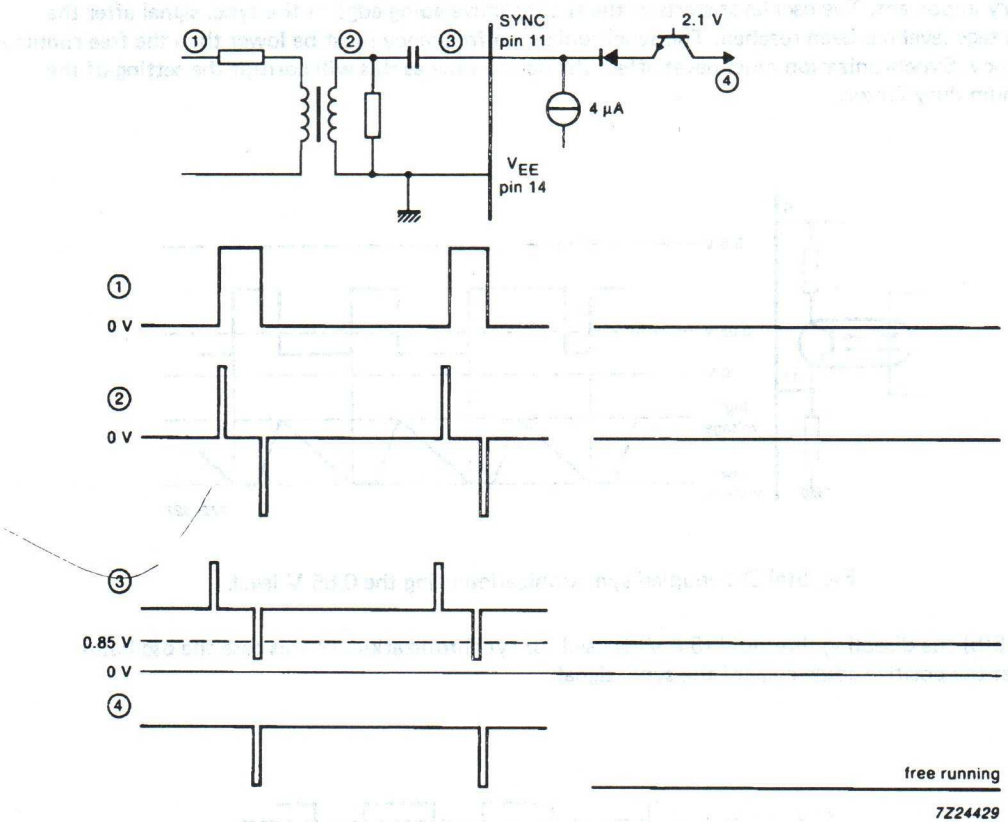


Fig.5(b) DC coupled synchronization using the 5.6 V level.

Figure 6 illustrates synchronization using a pulse transformer. Internal circuitry causes a DC shift which informs the device that synchronization pulses are present (spikes around 0 V at the output of the pulse transformer) or not present (DC 0 V at the output of the pulse transformer). When synchronization is not used the SYNC pin must be connected to V_{CC}, it must not be connected directly to ground or left open.



Synchronization pulses present. Synchronization pulses not present.

Fig.6 Synchronization using a pulse transformer.

FUNCTIONAL DESCRIPTION (continued)

Error amplifier

The error amplifier compares the feedback voltage of the SMPS with a reference voltage (nominally 2.5 V). The amplifier output at pin 8 enables gain setting. The amplifier is stable for a gain greater than 20 dB.

The output of the error amplifier is not internally connected to the Pulse Width Modulator (PWM). One input to the PWM is available at the DUTY input (pin 9) via the Control Slicing Level (CSL) circuit. Normally the STAB and DUTY pins are connected together, but direct driving of pin 9 via an optocoupler from the secondary side is also possible. A type of current mode control can be achieved by mixing the STAB signal with the primary current signal before applying it to the DUTY input.

The feedback (FB) input (pin 7) is used as the input to the Transfer Characteristic Generator (TCG) circuit which ensures well defined duty factors at low FB voltages; a voltage foldback is an inherent characteristic. In Fig.7, the duty factor is shown as a function of the voltages at the FB, DUTY and SS inputs. The input which gives the lowest duty factor overrides the others.

The left hand curve is passed through during a slow-start (via the slow-start input pin 12) when the duty cycle slowly increases linearly with respect to V_{12}. The right-hand curve is passed through at start-up. The FB voltage slowly increases from zero and the duty factor, starting at 12%, increases until the maximum duty factor (D_{max}) is reached. A few hundred millivolts later, the FB voltage reaches the start of the regulation curve which is at approximately 2.5 V. The plateau area between reaching D_{max} and starting the regulation curve is kept as small as possible (typically 200 mV).

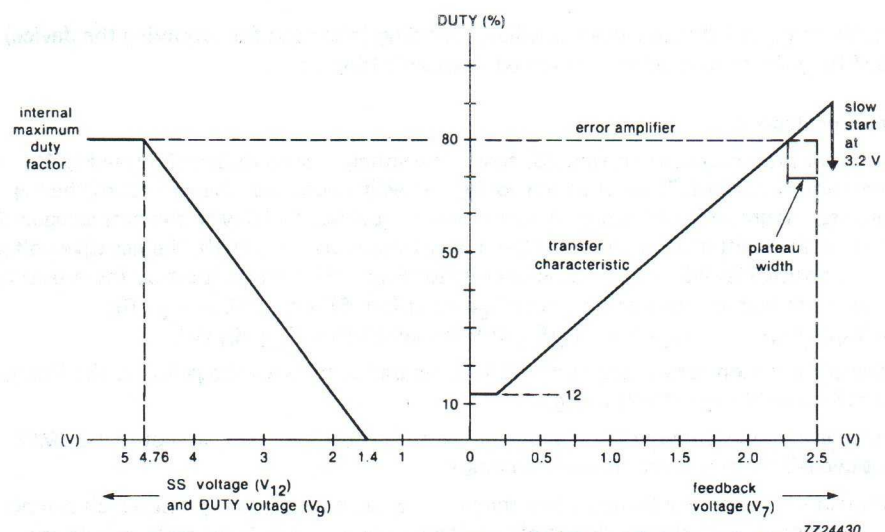


Fig.7 The duty factor as a function of the FB, SS and DUTY voltages.

Due to the characteristics of the TCG, and the fact that an open FB input results in a low voltage at the FB input, open- and short-circuit feedback loops will result in low duty factors. When DC feedback is used across the error amplifier, the current capability of the error amplifier must be considered when determining the feedback resistor value.

When the input to the PWM (pin 9) is driven by an optocoupler, the TCG can be used when a rough primary voltage is applied to the FB input. In this situation an open feedback loop will cause an increase in the FB voltage as the duty factor rises to its maximum. As soon as the FB voltage exceeds the reference by 0.7 V, the slow-start is triggered.

Demagnetization sense circuit

To enable the SMPS to be kept in the non-continuous mode, an input is available which delays switch-on of the high-voltage transistor until the transformer currents have decayed to zero. This is an effective way of avoiding transformer saturation. The waveforms illustrated by Fig.8 show demagnetization with respect to the application diagram of Fig.12.

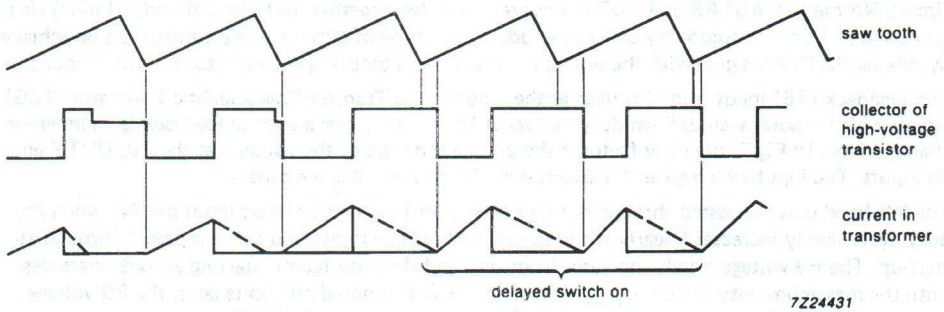


Fig.8 Demagnetization function.

As long as the voltage of the take-over (auxiliary) winding (also used for supplying the device) is above 0.6 V (V_3) the output will be prevented from switching on.

Over-current protection

The over-current protection circuit (pin 13) senses the voltage across resistor R_s (see Fig.12), which reflects the primary current. This generated voltage is negative-going as the emitter of the high-voltage power transistor is grounded (this circuit arrangement provides the IC with the best safeguard against a possible collector-emitter short-circuit in the power transistor). At pin 13, the negative voltage signal is shifted to a positive level by a voltage across resistor R_{13}. This voltage is set by the reference current at pin 13 and is defined by resistor R_6 at the I_{ref} input (pin 6) and = $1/6 \times V_{ref}/R_6$.
Therefore $V_{shift}(V_{R13}) = V_{ref}/6 \times R_{13}/R_6$ or nominal $0.416 \times R_{13}/R_6$ (V).

The positive current monitor voltage at pin 13 is compared with two voltage levels: the first level = 0.2 V and the second level = 0 V (see Fig.9).

The first trip level only switches off the high-voltage transistor for a cycle and puts the SMPS in a continuous cycle-by-cycle current protection mode.

The second trip level is only activated when the primary current rise is very fast which can occur during a short-circuited output. In this mode the high-voltage transistor is quickly switched off and the slow-start procedure is activated.

The difference between the first and second primary current peak levels is set by R_s:

$I_2 - I_1 = 0.2/R_s$.

The absolute peak values are set by R_6 and R_{13}:

$I_2 \times R_s = 0.416 \times R_{13}/R_6$ or

$I_1 \times R_s = (0.416 \times R_{13}/R_6) - 0.2$

FUNCTIONAL DESCRIPTION (continued)

Over-current protection (continued)

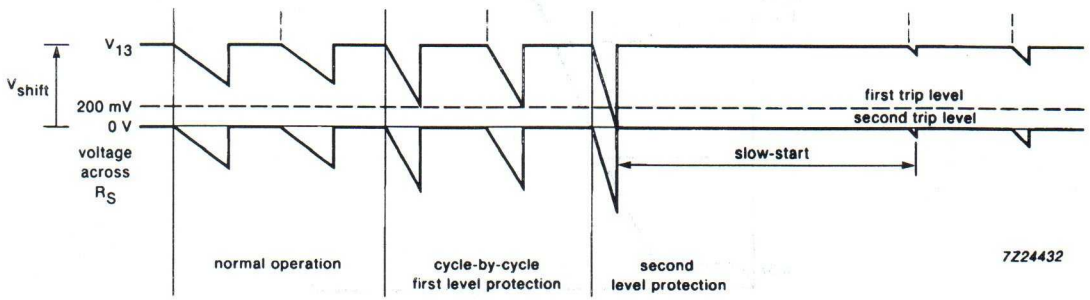


Fig.9 Current protection.

Slow-start circuit

A slow-start occurs:

- At Switch-on of the SMPS
- After a current trip as described in the section **Over-current protection**
- After a low or high V_{CC} trip.

The capacitor at the SS input is discharged and the slow-start bistable is reset when the voltage at the SS input falls below 0.5 V after which the circuit is ready for a slow-start. The dead time (during which the capacitor at the SS input is being charged to the 1.4 V lower level of the sawtooth) before duty cycle regulation starts is minimal. The SS input can also be used for D_{max} setting by connecting a resistor to ground. The voltage across this resistor is then limited to $1/6 \times V_{ref} \times R_{12}/R_6$.

Output stages

The output stage consists of two NPN darlington transistors, their collector and emitter connected to separate pins (see Fig.12). The top transistor is capable of sourcing a maximum of 0.75 A to the high-voltage transistor while the bottom transistor can sink peak currents up to 2.5 A.

For low currents up to 10 mA, the saturation voltage of the sink darlington transistor is similar to that of a single transistor (see Fig.10). During switching of this transistor dV/dt is internally limited to reduce interference.

Care should be taken with the external wiring of the output pins to avoid oscillation or interference due to parasitic inductance and wire resistance.

During start-up a small current flows from V_{CC} to E2 to precharge the series capacitor at the output (see Fig.12).

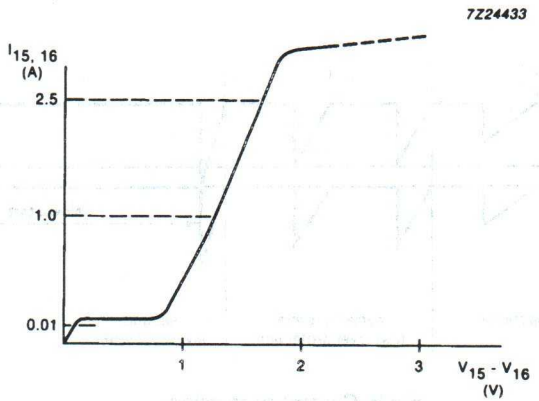


Fig.10 Saturation curve.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Voltage					
pin 5 (V_{CC})		−0.5	–	20	V
pins 1, 2, 4 and 16		−0.5	–	V_{CC}	V
pins 3 and 13		−0.5	–	0.5	V
pins 7 and 9		−0.5	–	6.5	V
pin 11		0.6	–	V_{CC}	V
Currents					
pin 5 (V_{CC})		0	–	20	mA
pin 1		−0.75	–	0	A
pin 2		0	–	0.75	A
pins 3, 4, 6 to 8 and 10 to 12		−10	–	10	mA
pin 13		−200	–	10	mA
pin 15		−2.5	–	0	A
pin 16		0	–	2.5	A
Total power dissipation	P_{tot}		see Fig.11		
Operating ambient temperature range (for dissipation $\leqslant$ 1 W)	T_{amb}	−25	–	+ 70	°C
Storage temperature range	T_{stg}	−55	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a(max)} = 55$ K/W

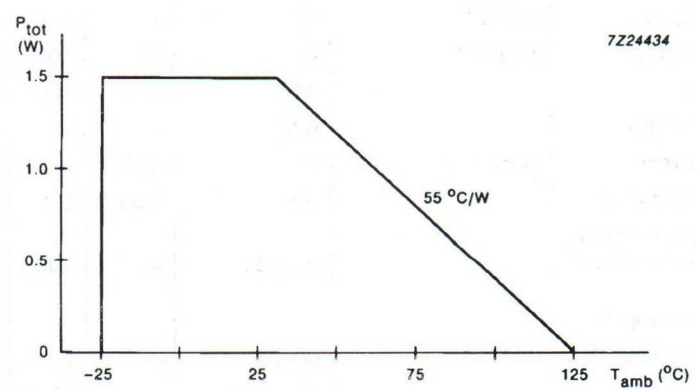


Fig.11 Power derating curve.

CHARACTERISTICS

V_{CC} = 14 V; T_{amb} = 25 °C; reference resistor = 5 kΩ unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{CC}	9	–	20	V
Supply initialization level		V_5	15	17	18	V
High voltage protection		V_5	21	23	25	V
Internal fixed minimum protection level		V_5	7.9	8.4	8.9	V
Hysteresis		dV_{CC}	–	50	–	mV
Supply current operational		I_{CC}	–	–	15	mA
before initialization		I_{CC}	–	100	150	μA
Reference current (pin 4)	note 1	I_4	$I_6/5.7$	$I_6/6$	$I_6/6.4$	mA
Trigger level V_{CCmin} setting		V_5	$3.6V_4$	$3.8V_4$	$4.2V_4$	V
Clamp voltage	at 20 mA		21.5	23.5	25.5	V
Reference (pin 6)						
Reference voltage		V_{ref}	2.4	2.5	2.6	V
Current range		I_{ref}	200	–	800	μA
Reference voltage over I_6 range		dV_{ref}	–20	–	+ 20	mV
Error amplifier						
Error amplifier threshold	V_{CC} = 8.5 to 20 V	V_7	2.4	2.5	2.6	V
Input current		I_7	0	–	5	μA
Sink current output	at 1.2 V	I_8	1	–	–	mA
Source current output	at 5.5 V	I_8	80	100	130	μA
Open loop gain		A0	–	100	–	dB
Unity gain bandwidth		BW	–	5	–	MHz
Input DUTY current	note 1	I_9	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
High FB protection level		V_7	2.95	3.1	3.25	V
Temperature coefficient of error amplifier threshold		dV_7/dT	–	100	–	10^{-6}/K
TCG function (see Fig.7)						
Transfer characteristic		dD/dV_7	–	32	–	%/V
Minimum duty factor		D_{min}	–	12	–	%
Plateau width		V_7	–	200	–	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Slow-start function						
Transfer characteristic		dD/dV_{12}	–	23.8	–	%/V
Input current	note 1	I_{12}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
Sink current during faults	at 0.5 V	I_{12}	8	–	–	mA
Internally fixed maximum duty factor		D_{max}	75	80	85	%
Clamp current	at V_{12} = 0.5 V	I_{12}	–	–2	–	mA
Output stage						
Source transistor						
Voltage drop with respect to V_{CC}	at 0.75 A	$V_{CC}-V_1$	–	2	–	V
Pull-up current	$V_{CC} - V_1$ = 15 V	$-I_1$	25	–	100	μA
Operating current range		$-I_1$	0	–	0.75	A
Sink transistor (see Fig.10)						
Saturation voltage						
at 2.5 A		$V_{16} - V_{15}$	–	2	–	V
at 1 A		$V_{16} - V_{15}$	–	1.5	–	V
at 10 mA		$V_{16} - V_{15}$	–	0.3	–	V
Leakage current	$V_{16} - V_{15}$ = 20 V	I_{16}	–	–	1	μA
Falling edge		dV_{16-15}/dt	–	0.2	–	V/ns
Operating current range						
Peak		I_{16}	0	–	2.5	A
Average		I_{16}	–	–	250	mA
Oscillator						
High level voltage		V_{10}	–	5	–	V
Low level voltage		V_{10}	–	1.4	–	V
Charge current	note 1	I_{10}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
Frequency range		f_o	10	–	100	kHz
Frequency	R_6 = 5 kΩ C_{10} = 680 pF	f_o	27	28.5	30	kHz
Temperature coefficient of the frequency		df/dT	–	100	–	10^{-6}/K

parameter	conditions	symbol	min.	typ.	max.	unit
Synchronization						
Minimum synchronization pulse width		t_{11}	–	–	0.5	μs
Switching threshold		V_{11}	0.7	0.85	0.9	V
Input current		I_{11}	2.5	5.0	7.5	μA
Disabling threshold		V_{11}	4.2	5.6	6.0	V
Input voltage	at −700 μA	V_{11}	390	–	550	mV
Demagnetization input						
Pin voltage	at 0 A	V_3	–	690	–	mV
Input current	at 0 V	I_3	−30	−40	−55	μA
Current range of clamp circuits		I_3	−10	–	+ 10	mA
Clamp level positive	at 10 mA	V_3	–	950	–	mV
Clamp level negative	at −10 mA	V_3	–	−800	–	mV
Current protection						
Input current	note 1	I_{13}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
First threshold		V_{13}	190	200	210	mV
Second threshold		V_{13}	−10	0	10	mV
Delay to switch output via level 1	pulse at pin 13 from 300 mV to 100 mV; I_O = 500 mA	–	–	350	–	ns
Delay to switch output via level 2	pulse at pin 13 from 300 mV to −200 mV; I_O = 500 mA	–	–	300	500	ns
First threshold including R_{13} (12 kΩ)	R_6 = 5 kΩ	–	–	−800	–	mV
Threshold for open pin detection		V_{13}	–	3.5	–	V

Note to the characteristics

1. Over the current range of I_6; 200 to 800 μA.

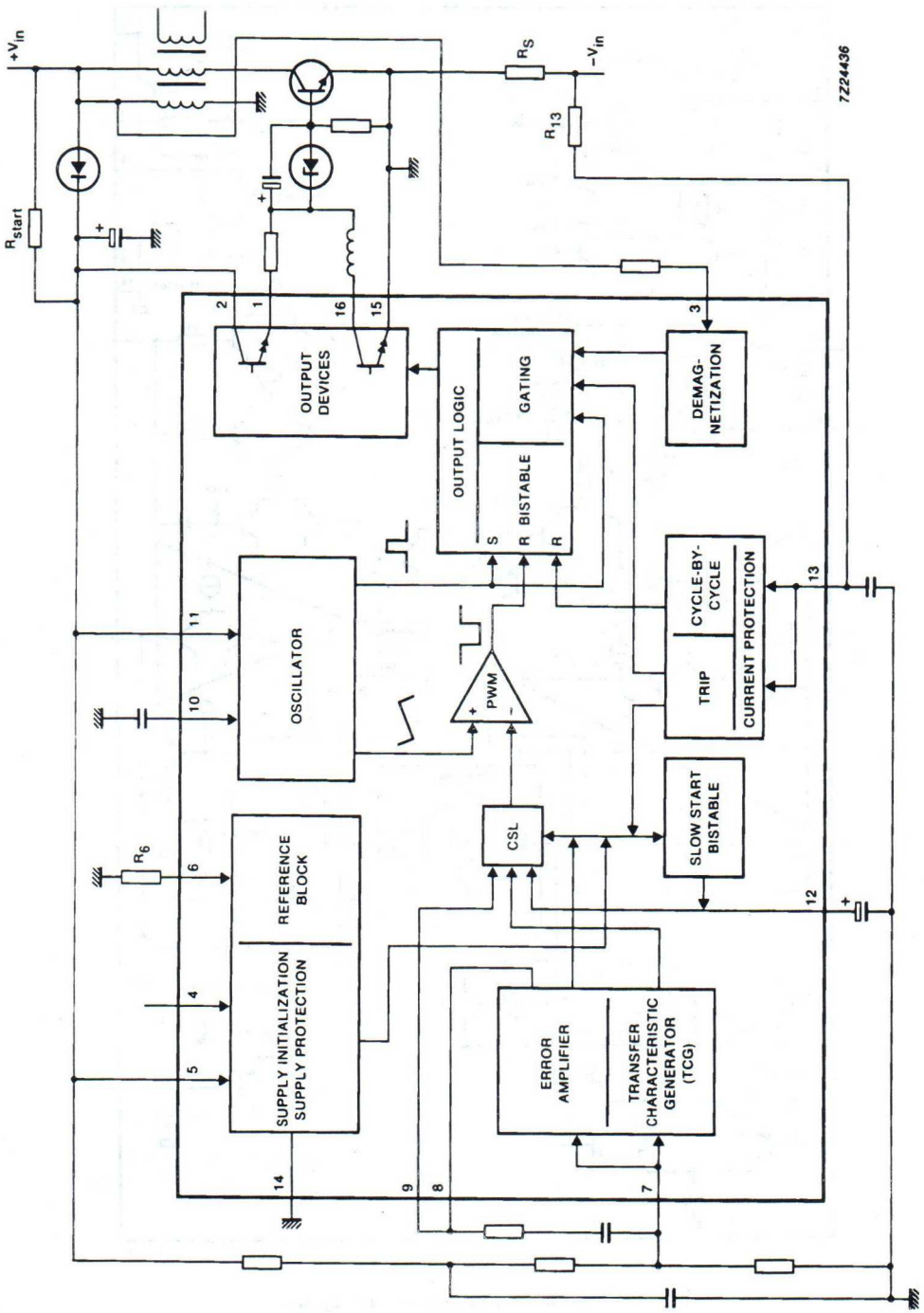


Fig.12 Simplified application diagram.

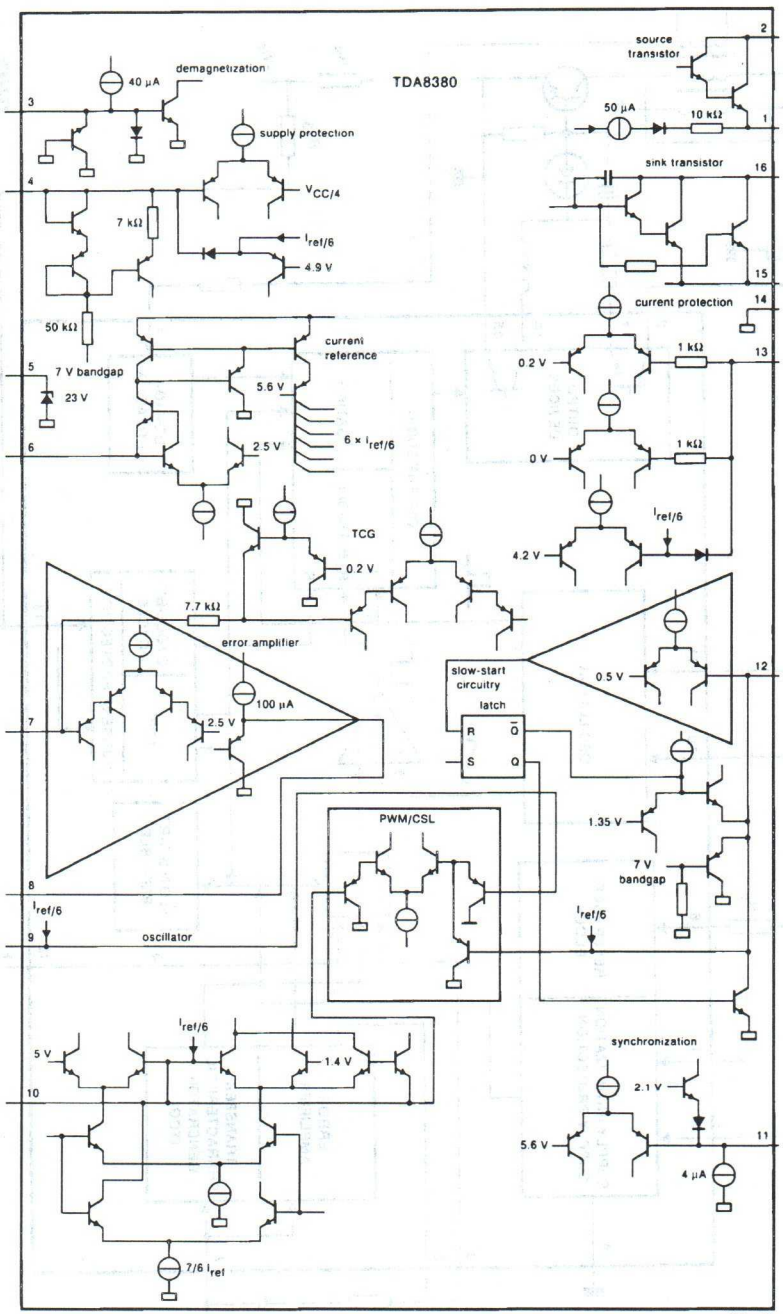


Fig.13 Input and output loading diagram.

Control circuit for switched-mode power supply TEA1039

GENERAL DESCRIPTION

The TEA1039 is a bipolar integrated circuit intended for the control of a switched-mode power supply. Together with an external error amplifier and a voltage regulator (e.g. a regulator diode) it forms a complete control system. The circuit is capable of directly driving the SMPS power transistor in small SMPS systems.

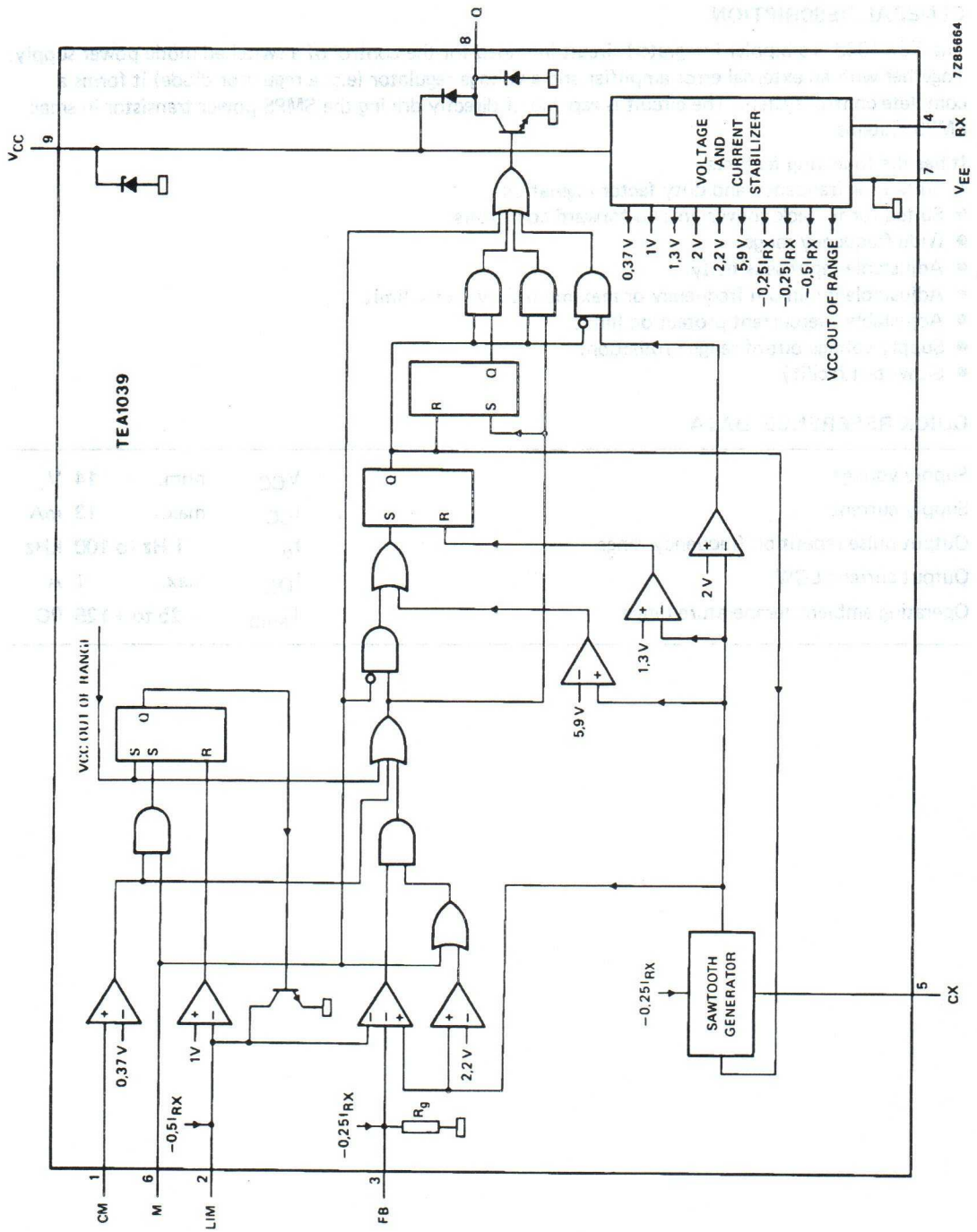
It has the following features:

- Suited for frequency and duty factor regulation.
- Suited for flyback converters and forward converters.
- Wide frequency range.
- Adjustable input sensitivity.
- Adjustable minimum frequency or maximum duty factor limit.
- Adjustable overcurrent protection limit.
- Supply voltage out-of-range protection.
- Slow-start facility.

QUICK REFERENCE DATA

Supply voltage	V_{CC}	nom.	14 V
Supply current	I_{CC}	max.	13 mA
Output pulse repetition frequency range	f_o	1 Hz to	100 kHz
Output current LOW	I_{OL}	max.	1 A
Operating ambient temperature range	T_{amb}	−25 to +	125 °C

Control circuit for switched-mode power supply — TEA1039



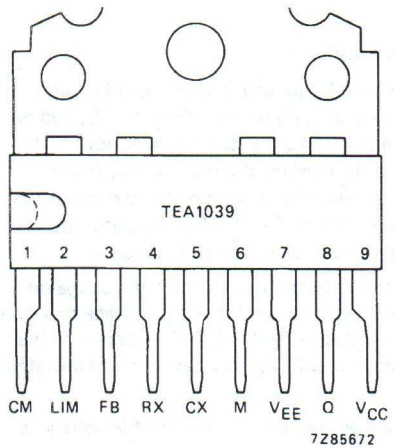


Fig. 2 Pinning diagram.

PINNING

1	CM	overcurrent protection input
2	LIM	limit setting input
3	FB	feedback input
4	RX	external resistor connection
5	CX	external capacitor connection
6	M	mode input
7	V_{EE}	common
8	Q	output
9	V_{CC}	positive supply connection

FUNCTIONAL DESCRIPTION

The TEA1039 produces pulses to drive the transistor in a switched-mode power supply. These pulses may be varied either in frequency (frequency regulation mode) or in width (duty factor regulation mode).

The usual arrangement is such that the transistor in the SMPS is ON when the output of the TEA1039 is HIGH, i.e. when the open-collector output transistor is OFF. The duty factor of the SMPS is the time that the output of the TEA1039 is HIGH divided by the pulse repetition time.

Supply V_{CC} (pin 9)

The circuit is usually supplied from the SMPS that it regulates. It may be supplied either from its primary d.c. voltage or from its output voltage. In the latter case an auxiliary starting supply is necessary.

The circuit has an internal V_{CC} out-of-range protection. In the frequency regulation mode the oscillator is stopped; in the duty factor regulation mode the duty factor is made zero. When the supply voltage returns within its range, the circuit is started with the slow-start procedure.

When the circuit is supplied from the SMPS itself, the out-of-range protection also provides an effective protection against any interruption in the feedback loop.

Mode input M (pin 6)

The circuit works in the frequency regulation mode when the mode input M is connected to ground (V_{EE}, pin 7). In this mode the circuit produces output pulses of a constant width but with a variable pulse repetition time.

The circuit works in the duty factor regulation mode when the mode input M is left open. In this mode the circuit produces output pulses with a variable width but with a constant pulse repetition time.

FUNCTIONAL DESCRIPTION (continued)

Oscillator resistor and capacitor connections RX and CX (pins 4 and 5)

The output pulse repetition frequency is set by an oscillator whose frequency is determined by an external capacitor C5 connected between the CX connection (pin 5) and ground (V_{EE}, pin 7), and an external resistor R_4 connected between the RX connection (pin 4) and ground. The capacitor C5 is charged by an internal current source, whose current level is determined by the resistor R4. In the frequency regulation mode these two external components determine the minimum frequency; in the duty factor regulation mode they determine the working frequency (see Fig. 4). The output pulse repetition frequency varies less than 1% with the supply voltage over the supply voltage range.

In the frequency regulation mode the output is LOW from the start of the cycle until the voltage on the capacitor reaches 2 V. The capacitor is further charged until its voltage reaches the voltage on either the feedback input FB or the limit setting input LIM, provided it has exceeded 2,2 V. As soon as the capacitor voltage reaches 5,9 V the capacitor is discharged rapidly to 1,3 V and a new cycle is initiated (see Figs 5 and 6).

For voltages on the FB and LIM inputs lower than 2,2 V, the capacitor is charged until this voltage is reached; this sets an internal maximum frequency limit.

In the duty factor regulation mode the capacitor is charged from 1,3 V to 5,9 V and discharged again at a constant rate. The output is HIGH until the voltage on the capacitor exceeds the voltage on the feedback input FB; it becomes HIGH again after discharge of the capacitor (see Figs 7 and 8). An internal maximum limit is set to the duty factor of the SMPS by the discharging time of the capacitor.

Feedback input FB (pin 3)

The feedback input compares the input current with an internal current source whose current level is set by the external resistor R4. In the frequency regulation mode, the higher the voltage on the FB input, the longer the external capacitor C5 is charged, and the lower the frequency will be. In the duty factor regulation mode external capacitor C5 is charged and discharged at a constant rate, the voltage on the FB input now determines the moment that the output will become LOW. The higher the voltage on the FB input, the longer the output remains HIGH, and the higher the duty factor of the SMPS.

Limit setting input LIM (pin 2)

In the frequency regulation mode this input sets the minimum frequency, in the duty factor regulation mode it sets the maximum duty factor of the SMPS. The limit is set by an external resistor R2 connected from the LIM input to ground (pin 7) and by an internal current source, whose current level is determined by external resistor R4.

A slow-start procedure is obtained by connecting a capacitor between the LIM input and ground. In the frequency regulation mode the frequency slowly decreases from f_{max} to the working frequency. In the duty factor regulation mode the duty factor slowly increases from zero to the working duty factor.

Overcurrent protection input CM (pin 1)

A voltage on the CM input exceeding 0,37 V causes an immediate termination of the output pulse. In the duty factor regulation mode the circuit starts again with the slow-start procedure.

Output Q (pin 8)

The output is an open-collector n-p-n transistor, only capable of sinking current. It requires an external resistor to drive an n-p-n transistor in the SMPS (see Figs 9 and 10).

The output is protected by two diodes, one to ground and one to the supply.

At high output currents the dissipation in the output transistor may necessitate a heatsink. See the power derating curve (Fig. 3).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range, voltage source	V_{CC}	−0,3 to +20 V
Supply current range, current source	I_{CC}	−30 to +30 mA
Input voltage range, all inputs	V_I	−0,3 to +6 V
Input current range, all inputs	I_I	−5 to +5 mA
Output voltage range	V_{8-7}	−0,3 to +20 V
Output current range		
output transistor ON	I_8	0 to 1 A
output transistor OFF	I_8	−100 to + 50 mA
Storage temperature range	T_{stg}	−55 to +150 °C
Operating ambient temperature range (see Fig. 3)	T_{amb}	−25 to +125 °C
Power dissipation (see Fig. 3)	P_{tot}	max. 2 W

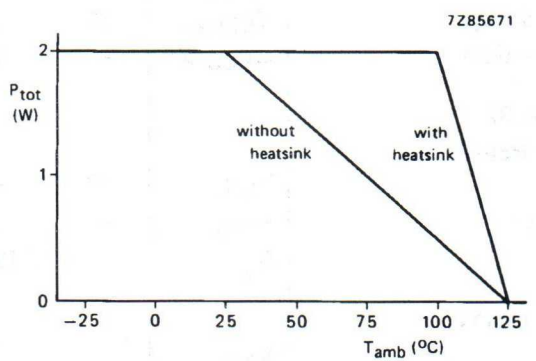


Fig. 3 Power derating curve.

CHARACTERISTICS

V_{CC} = 14 V; T_{amb} = 25 °C unless otherwise specified

	symbol	min.	typ.	max.	unit
Supply V_{CC} (pin 9)					
Supply voltage, operating	V_{CC}	11	14	20	V
Supply current					
at V_{CC} = 11 V	I_{CC}	–	7,5	11	mA
at V_{CC} = 20 V	I_{CC}	–	9	12	mA
variation with temperature	$\frac{\Delta I_{CC}/I_{CC}}{\Delta T}$	–	–0,3	–	%/K
Supply voltage, internally limited at I_{CC} = 30 mA	V_{CC}	23,5	–	28,5	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	18	–	mV/K
Low supply threshold voltage	V_{CCmin}	9	10	11	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	–5	–	mV/K
High supply threshold voltage	V_{CCmax}	21	23	24,6	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	10	–	mV/K
Feedback input FB (pin 3)					
Input voltage for duty factor = 0; M input open	V_{3-7}	0	–	0,3	V
Internal reference current	$-I_{FB}$	–	0,5 I_{RX}	–	mA
Internal resistor R_g	R_g	–	130	–	kΩ
Limit setting input LIM (pin 2)					
Threshold voltage	V_{2-7}	–	1	–	V
Internal reference current	$-I_{LIM}$	–	0,25 I_{RX}	–	mA
Overcurrent protection input CM (pin 1)					
Threshold voltage	V_{1-7}	300	370	420	mV
variation with temperature	$\Delta V_{1-7}/\Delta T$	–	0,2	–	mV/K
Propagation delay, CM input to output	t_{PHL}	–	500	–	ns

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.	unit
Oscillator connections RX and CX (pins 4 and 5)					
Voltage at RX connection at $-I_4$ = 0,15 to 1 mA	V_{4-7}	6,2	7,2	8,1	V
variation with temperature	$\Delta V_{4-7}/\Delta T$	–	2,1	–	mV/K
Lower sawtooth level	V_{LS}	–	1,3	–	V
Threshold voltage for output H to L transition in F mode	V_{FT}	–	2	–	V
Threshold voltage for maximum frequency in F mode	V_{FM}	–	2,2	–	V
Higher sawtooth level	V_{HS}	–	5,9	–	V
Internal capacitor charging current, CX connection	$-I_{CX}$	–	0,25 I_{RX}	–	mA
Oscillator frequency (output pulse repetition frequency)	f_o	1	–	10^5	Hz
Minimum frequency in F mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Maximum frequency in F mode, initial deviation	$\Delta f/f$	−20	–	+20	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	−0,16	–	%/K
Output LOW time in F mode, initial deviation	$\Delta t/t$	−25	–	+25	%
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Pulse repetition frequency in D mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Minimum output LOW time in D mode at C_5 = 3,6 nF	t_{OLmin}	–	1	–	μs
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Output Q (pin 8)					
Output voltage LOW at I_8 = 100 mA	V_{8-7}	–	0,8	1,2	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	1,5	–	mV/K
Output voltage LOW at I_8 = 1 A	V_{8-7}	–	1,7	2,1	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	−1,4	–	mV/K

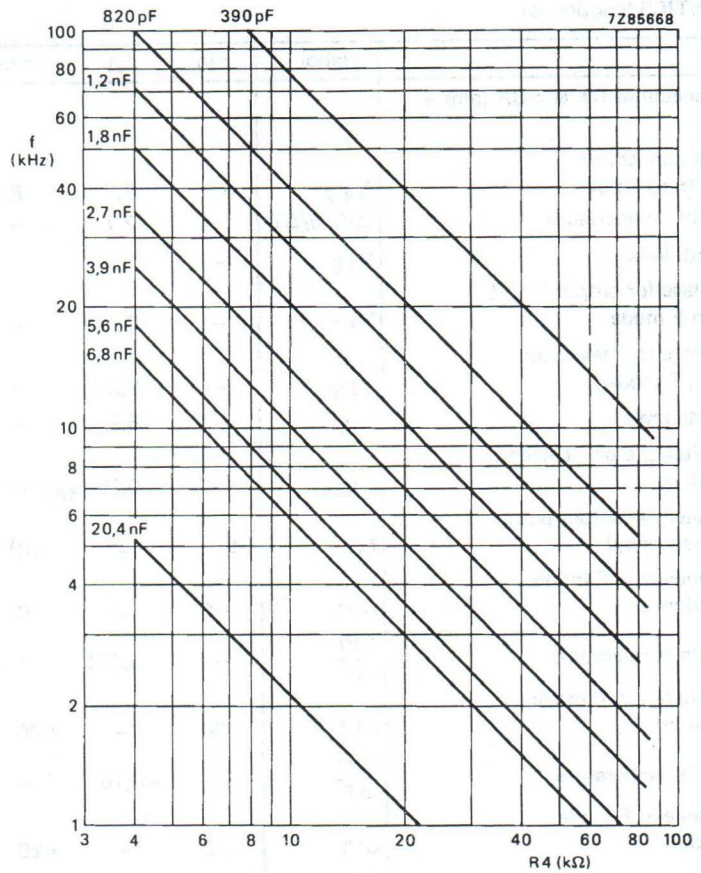


Fig. 4 Minimum pulse repetition frequency in the frequency regulation mode, and working pulse repetition frequency in the duty factor regulation mode, as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

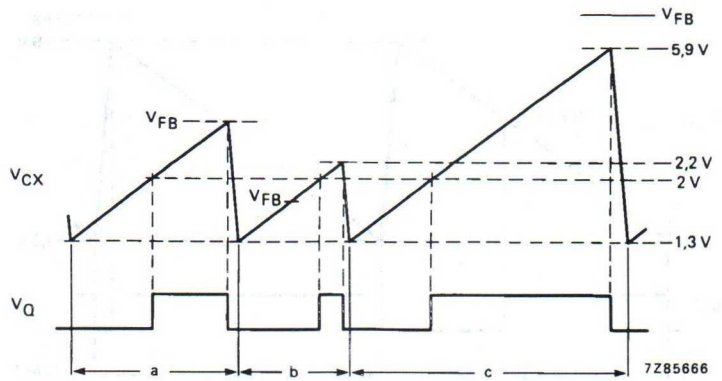


Fig. 5 Timing diagram for the frequency regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for three combinations of input signals. *a:* The voltages on inputs FB or LIM are between 2,2 V and 5,9 V. The circuit is in its normal regulation mode. *b:* The voltage on input FB or input LIM is lower than 2,2 V. The circuit works at its maximum frequency. *c:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit works at its minimum frequency.

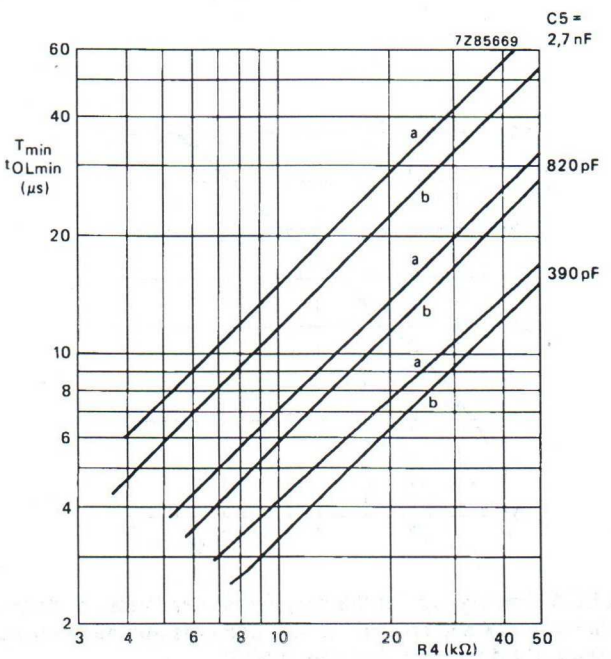


Fig. 6 Minimum output pulse repetition time T_{min} (curves a) and minimum output LOW time t_{OLmin} (curves b) in the frequency regulation mode as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

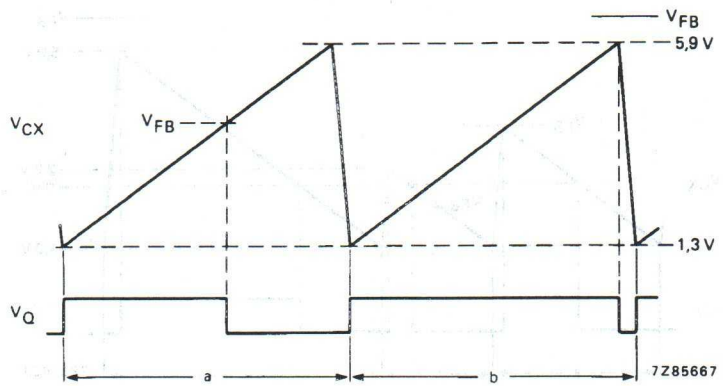


Fig. 7 Timing diagram for the duty factor regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for two combinations of input signals. *a:* The voltages on inputs FB or LIM are below 5,9 V. The circuit is in its normal regulation range. *b:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit produces its minimum output LOW time, giving the maximum duty factor of the SMPS.

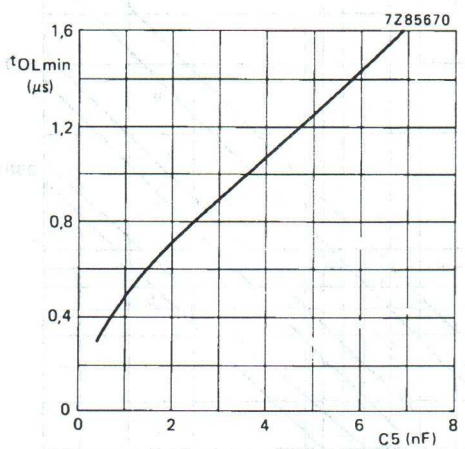


Fig. 8 Minimum output LOW time t_{OLmin} in the duty factor regulation mode as a function of external capacitor C5 connected between CX and ground. In this mode the minimum output LOW time is independent of R4 for values of R4 between 4 kΩ and 80 kΩ.

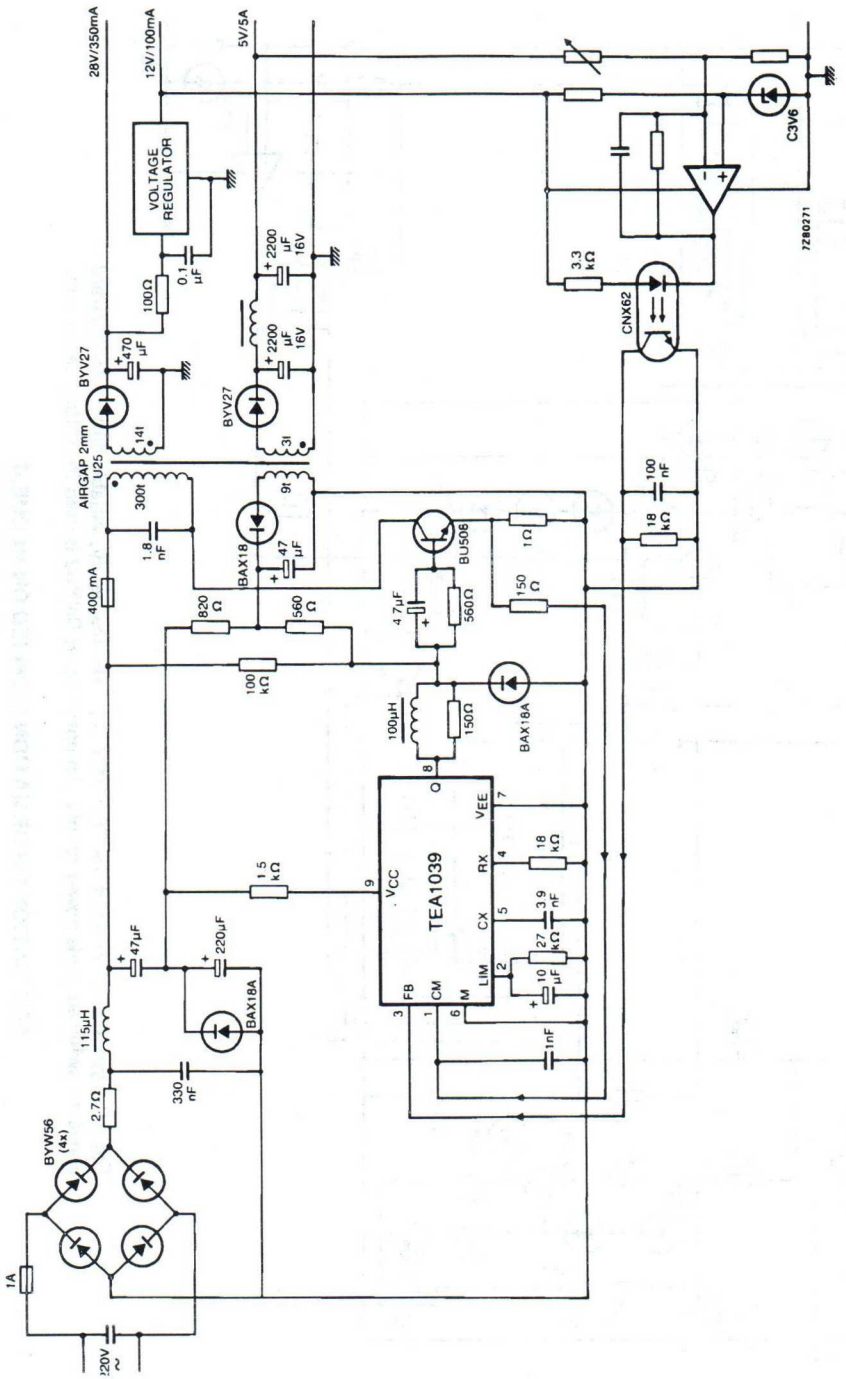


Fig. 9 Typical application of the TEA1039 in a variable-frequency flyback converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

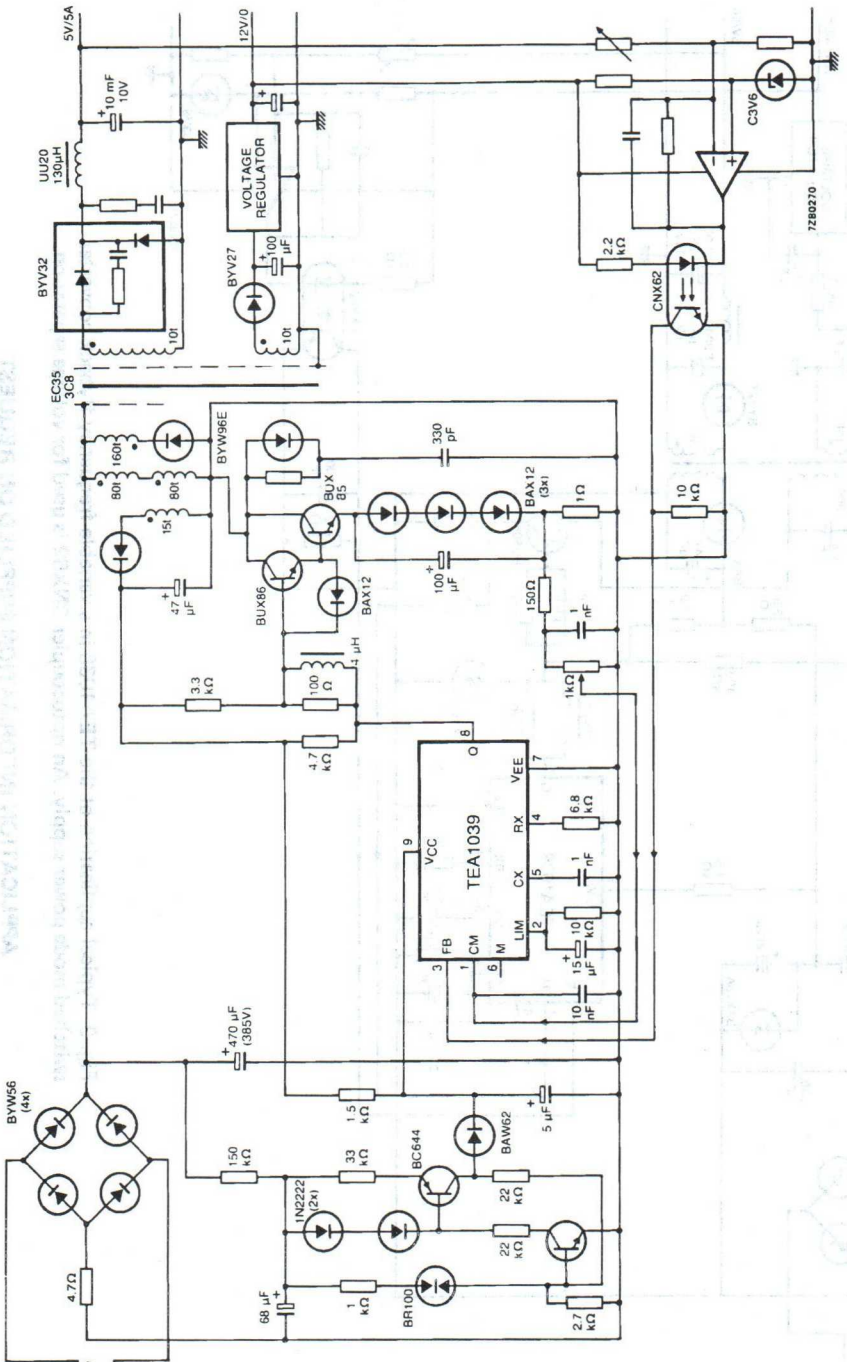


Fig. 10 Typical application of the TEA1039 in a fixed-frequency, variable duty factor forward converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

Section 16
Motor control circuits

INDEX

NE/SA5570	Brushless DC motor controller	1151
AN1281	NE5570: A theory of operation and applications	1156
TDA5140A	Brushless DC motor drive circuit	1169
TDA5141	Brushless DC motor drive circuit	1184
TDA5142T	Brushless DC motor drive circuit	1200
TDA5143T	Brushless DC motor drive circuit	1215
TDA5144	Brushless DC motor drive circuit	1229
TDA5145	Brushless DC motor drive circuit	1243

Brushless DC motor controller

NE/SA5570

DESCRIPTION

The NE/SA/SE5570 is a three-phase brushless DC motor controller with a microprocessor-compatible serial input data port; 8-bit monotonic digital-to-analog converter; PWM comparator; oscillator; three Hall sensor inputs and six source/sink phase pre-drivers.

FEATURES

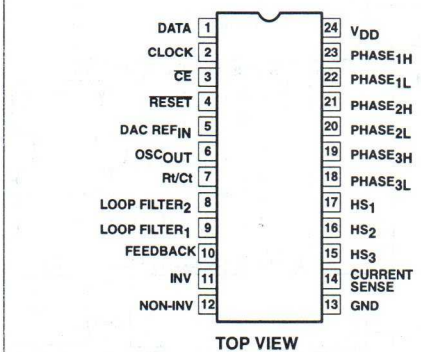
- 8-bit DAC
- Serial-to-parallel converter
- Output pre-drivers
- Entire switch mode conversion
- Adaptable to 60° or 120° commutation
- Overcurrent protection

APPLICATIONS

- Motor controller for three-phase brushless DC motor
- Robotics
- Computer peripherals

PIN CONFIGURATION

D[1], N Packages



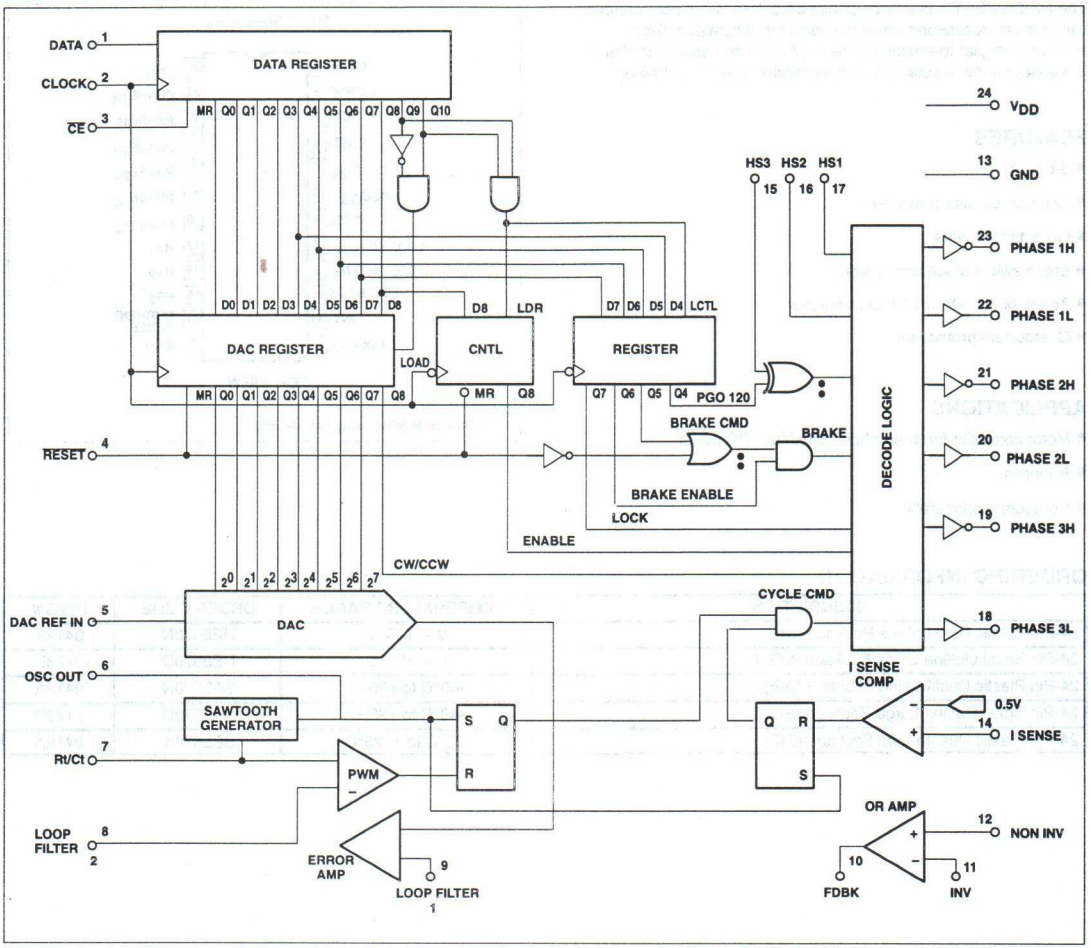
TOP VIEW

NOTE:
1. Available in large SO (SOL) package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5570N	0412A
24-Pin Small Outline Large Package (SOL)	0 to +70°C	NE5570D	0173D
24-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA5570N	0412A
24-Pin Small Outline Large Package (SOL)	-40°C to +85°C	SA5570D	0173D
24-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE5570N	0412A

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING			UNIT
		NE5570	SA5570	SE5570	
	Temperature range				
T_A	Operating ambient	0 to 70	-40 to 85	-55 to 125	°C
T_J	Operating junction	-55 to 150	-55 to 150	-55 to 150	°C
T_{STG}	Storage	-65 to 150	-65 to 150	-65 to 150	°C
V_{DD}	Power supply	16	16	16	V
	Logic inputs, all	-0.3 to 15	-0.3 to 15	-0.3 to 15	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient temperature range		
	NE Grade	0 to 70	°C
	SA Grade	-40 to 85	°C
	SE Grade	-55 to 125	°C
T_J	Junction temperature range		
	NE Grade	0 to 90	°C
	SA Grade	-40 to 105	°C
	SE Grade	-55 to 145	°C
V_{DD}	Supply voltage	9.6 to 14.4	V

DC ELECTRICAL CHARACTERISTICS

Limits apply at V_{DD}=12V ±10%, V_{REF}=5V and over operating temperature range unless otherwise specified. Typical data applies at T_A=25°C

SYMBOL	PARAMETER	TEST CONDITIONS	SA/NE5570			SE5570			UNIT
			Min	Typ	Max	Min	Typ	Max	
Oscillator									
f_O	Frequency initial accuracy	T_A=25°C, R_T=2.49kΩ, C_T=22nF	18.5	20	21	18.5	20	21	kHz
f_C	Frequency drift over temp	R_T=2.49kΩ, C_T=22nF	18		22	18		22	kHz
	Supply voltage sensitivity	T_A=25°C		±2			±2		%/V
	Output pulse width	T_A=25°C, R_T=2.49kΩ, C_T=22nF		500	1000		500	1000	ns
Motor Phase Pre-Drivers									
t_R	Rise time	R_L=2kΩ to Gnd, C_L=2nF [1V to 11V]			500			500	ns
t_F	Fall time	R_L=2kΩ to V_{CC}, C_L=2nF [1V to 11V]			500			500	ns
I_{OUT}	I_{SOURCE}	V_{OH}=8V	80			80			mA
	I_{SINK}	V_{OL}=3.1V	80			80			
V_{OUT}	V_{OH}	I_{SOURCE}=5mA	11	11.8		11	11.8		V
		I_{SOURCE}=80mA (over temp)	8	10		8	10		
	V_{OL}	I_{SINK}=5mA		0.4	1		0.4	1	
		I_{SINK}=80mA (over temp)		2	3.1		2	3.1	
PWM Comparator									
I_{BIAS}	Input bias current				1			1	µA
Current Sense Comparator									
I_{BIAS}	Input bias current				1			1	µA
V_{TH}	Current sense trip level		350	500	600	350	500	600	mV
t_{PD}	Propagation delay to output drivers	C_L=2nF		250			250		ns
Error Amplifier									
I_{BIAS}	Input bias current				1			1	µA
V_{CM}	Input common-mode voltage range		0		5	0		5	V
V_{OL}	Large-signal voltage gain	V_{OUT}=1V to 11V	70	90		70	90		dB
PSRR	Power supply rejection ratio		60			60			dB
V_O	Output voltage swing	V_{IN}=+50mV, I_L=-150µA	11.5	11.7		11.5	11.7		V
		V_{IN}=-50mV, I_L=+150µA		0.2	0.5		0.2	0.5	V

DC ELECTRICAL CHARACTERISTICS

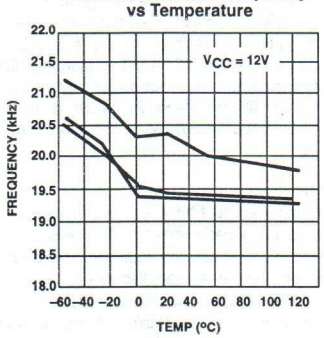
(Continued) Limits apply at V_{DD}=12V +10%, V_{REF}=5V and over operating temperature range unless otherwise specified. Typical data applies at T_A=25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	SA/NE5570			SE5570			UNIT
			Min	Typ	Max	Min	Typ	Max	
Operational Amplifier									
V_{OS}	Offset voltage		-20	3	+20	-20	3	+20	mV
I_{BIAS}	Input bias current				1			1	µA
V_{CM}	Input common-mode voltage range	T_A=25°C Over temp.	-0.3 0		5 5	-0.3 0		5 5	V
V_{OL}	Large signal voltage gain	V_{OUT}=1V to 11V	70	90		70	90		dB
PSRR	Power supply rejection ratio		60	90		60	90		dB
V_O	Output voltage swing	V_{IN}=+50mV, I_L=-150µA V_{IN}=-50mV, I_L=+150µA	11.5	11.7 0.2	 0.5	11.5	11.7 0.2	 0.5	V V
CMRR	Common-mode rejection ratio	R_S=10kΩ	60	80		60	80		dB
GBW	Gain bandwidth	R_F=100kΩ		250			250		kHz
V_{NN}	Input noise voltage	F=1kHz		300			300		nV/√Hz
Digital-to-Analog Converter									
	Resolution				8			8	bits
INL	Integral non-linearity error			±1	±2		±1	±2	LSB
DNL	Differential non-linearity error[1]			±0.5	±1		±0.5	±1	LSB
V_{FS}	Full-scale gain error	Error amp. A_V=1		±0.2	±0.8		±0.2	±0.8	%FS
	Full-scale temperature drift	$V_{REF}T_C$=0ppm/°C		20			20		ppm/°C
V_{ZS}	Zero-scale offset error	Error amp. A_V=1		±1	±2		±1	±2	LSB
Z_{IN}	Input impedance (DAC ref. in)		30	45	60	30	45	60	kΩ
t_S	Settling time to ±0.5 LSB			5			5		µs
t_{PLH}	Propagation delay time (high)	Through DAC		200			200		ns
t_{PHL}	Propagation delay time (low)	Through DAC		200			200		ns
Logic Inputs									
V_{IH}	Input voltage: TTL high		2.0		12	2.0		12	V
V_{IL}	Input voltage: TTL low		0		0.8	0		0.8	V
I_{IH}	Input current: TTL high				±1			±1	µA
I_{IL}	Input current: TTL low				±1			±1	µA
Supply Current									
I_{DD}				1.8	5.0		1.8	5.0	mA

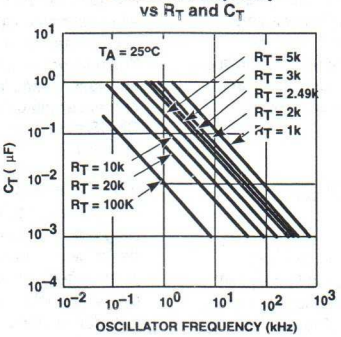
NOTES:
1. Monotonicity guaranteed over operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

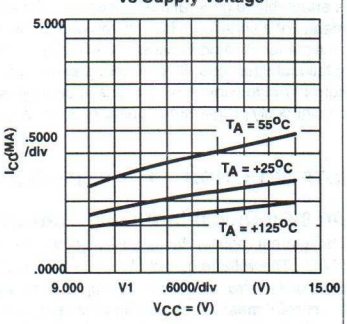
NE5570 Oscillator Frequency vs Temperature



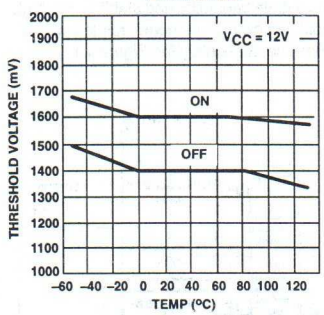
Oscillator Frequency vs R_T and C_T



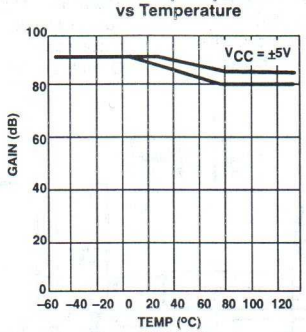
NE5570 Oscillator Frequency vs Supply Voltage



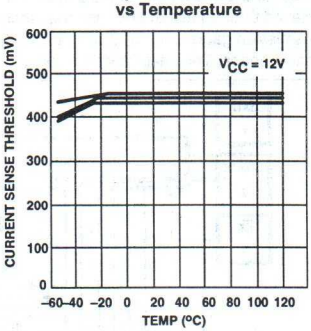
NE5570 Oscillator Output Pulse Width



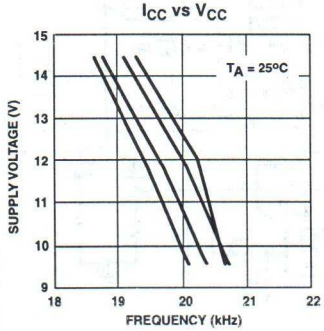
NE5570 Op Amp Gain vs Temperature



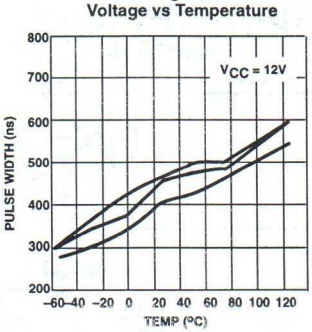
NE5570 Current Sense Comparator Threshold vs Temperature



I_{CC} vs V_{CC}



NE5570 Logic Threshold Voltage vs Temperature



NE5570: A theory of operation and applications AN1281

Authors: Larry Engh, Carl Fenger, Les Hadley, Dan Linebarger

The Philips Semiconductors NE5570 monolithic CMOS controller is described with basic applications showing its adaptation to microprocessor-controlled servo systems. The controller (NE5570) is adaptable to general three-phase brushless motor control by means of a serial data input command format which provides multiple function addressing within the chip. These functions include rotational directions, 60 or 120 degrees commutation select, and current mode control to each phase on a dynamic basis by continuously programmed pulse width modulator.

INTRODUCTION TO CIRCUIT FEATURES

An 8-Bit Digital-to-Analog Converter

The internal register drives an 8-bit digital-to-analog converter (DAC). The voltage output of this converter is applied to the positive input of the error amp. This op amp is normally used for integrating the current measure at the output of op amp one. The error amplifier output drives the pulse width modulator (PWM).

For ease of use, the DAC voltage is continuously present to the error amplifier input. Even during changes of value, the transition is smooth to a new set point of the pulse width modulator. This is achieved through use of precision ratio resistors and CMOS transmission gates. The DAC can be quickly updated through the serial interface. The integrator time constant should be chosen to complement the motor dynamics, i.e., transient response, gain, and phase margin.

The accuracy of the DAC features excellent differential linearity. This is helpful for precision control. Integral linearity is very good; this allows consistent production tolerance for the overall system. The DAC reference input directly drives the resistor string of the DAC. The nominal reference voltage is 5V, and this is the voltage at which accuracy is specified. For consistent system performance, the reference voltage should be well filtered. Because the DAC is a CMOS design, voltages other than precisely 5V can be tolerated, however.

The Operational Amplifier

The op amp used for current sense must have a common-mode range which includes ground and negative down to 0.5V. A special design was required to meet this performance objective. The input is level-shifted with a source-follower pair and applied to a p-channel differential pair. This technique preserves the very high input impedance of a CMOS input down to -0.5V. At this voltage, the input protection network begins to draw current, and inputs should be current limited if negative spikes are present.

Output Stage

The output stage is an inverter design. It features moderate idle current with good capacitive drive capability and stability. For high resistance loads, the output can swing very nearly rail-to-rail. Outputs are tested at 100mA source-sink. (See Figure 1.)

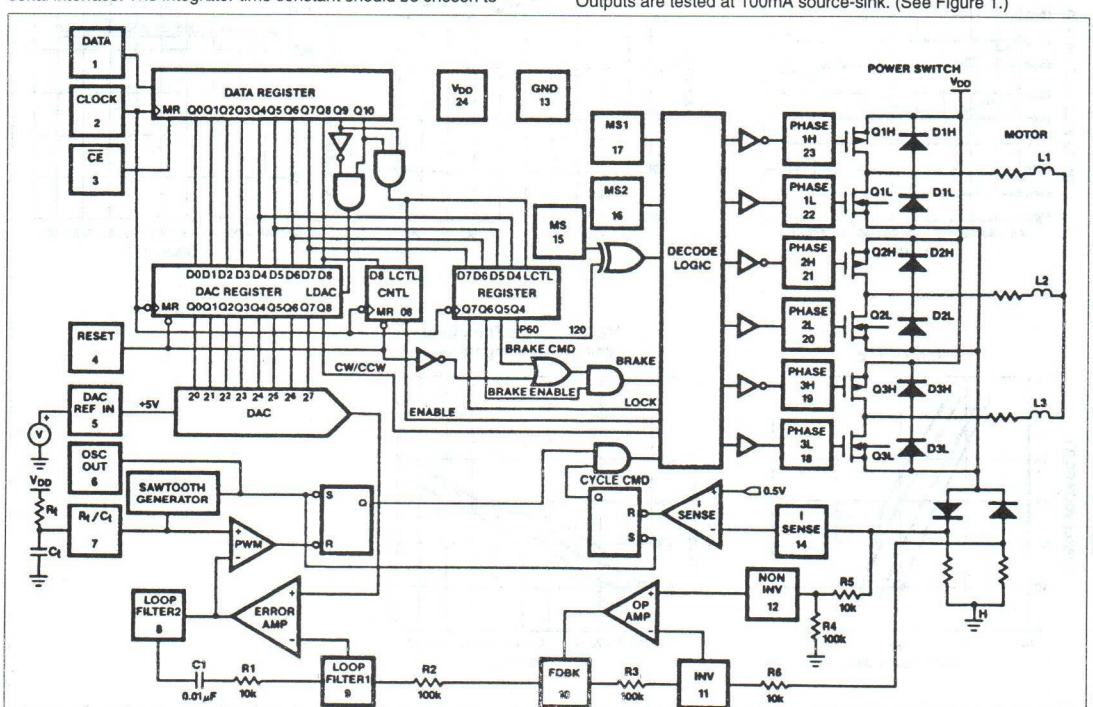
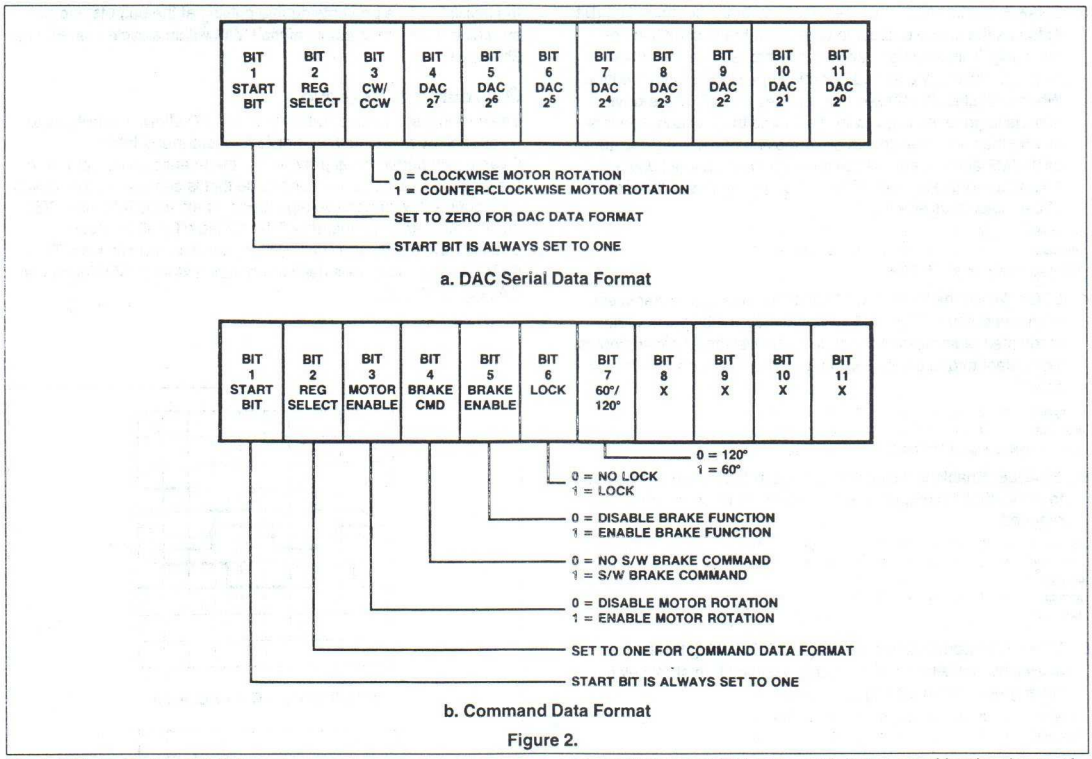


Figure 1. NE5570 Block Diagram



a. DAC Serial Data Format

b. Command Data Format

Figure 2.

Serial Data Entry-DAC Input

Three pins are used to allow the input of a serial word into an 11-bit serial-to-parallel data register. When CE is active, data may be clocked into the DATA pin using a rising edge clock into pin CLOCK. These three pins (DATA, CLOCK, CHIP ENABLE) are compatible with standard TTL input levels. The first two bits of the serial word select either the DAC data register or the Command control register.

In order to select the DAC register, the first two data bits must be 1 followed by a 0. The remaining nine bits are used to set the DAC to the desired level and control the direction of the motor rotation (CW or CCW). All eleven data bits must be shifted in before the DAC can be selected. The DAC register has an internal serial address of 10. (See Figure 2a.)

NOTE:
Output change will occur on the falling edge of the 11th clock bit.

The Control and Command Registers

The control register has an internal binary address of 11 (see Figure 2b). When the
control register has been selected by clocking in an 11-bit serial word with the first two bits equal to 11 in binary, the command register can select any of five different motor control commands. This register can direct the outputs to switch at the oscillator frequency in order to drive the motor, lock the motor in a fixed position, smoothly brake the motor, disable the driving outputs, or switch between 60 degree and 120 degree commutating mode. When the run command is selected, the output phase pre-drivers will generate pulse width-modulated signals that can drive the gates of a six transistor FET bridge which in turn can drive the phases of the motor. The purpose of the decode logic is to take the rotor position information (from Hall effect devices) at HS1, HS2, HS3 (Figure 3a), Pins 17, 16, and 15, together with the active state of ENABLE, CW/CCW, LOCK, BRAKE, and CYCLE to determine which of six outputs to turn on or off. The PWM duty cycle is then varied to regulate the current through the motor to a preset level controlled by the previous state of the DAC register.

Command Data Format

1. The RUN command is the normal mode of operation for driving the motor. The input format for selecting run mode is shown below (Bit 3 High):

clk cycles	1	2	3	4	5	6	7	8	9	10	11
cmd data	1	1	1	0	0	0	0	0	0	0	0

Active on falling edge of 11th clock.

2. BRAKE ENABLE: The brake enable command function allows a versatile way to brake the motor during a fault or power failure condition. For example, assume that previous commands have given the DAC a value above 0. The run command can be issued with the brake enable (Bit 5) register set to 1. The outputs will switch until RESET (Pin 4) is set to a Low state. This will reset the DAC register to 0 and cause the low-phase (sink) outputs P1L, P2L, and P3L to the High state, braking the motor to a halt.

clk cycles	1	2	3	4	5	6	7	8	9	10	11
cmd data	1	1	1	0	1	0	0	0	0	0	0

Active on falling edge of 11th clock.

3. BRAKE COMMAND: When set High, the brake command bit (Bit 4) forces the phase outputs to go into the brake condition immediately. This may be used to gently brake the motor when a fault is detected by a software routine or a loss of motor control. When activated, the brake signal causes the 6 FET pre-driver outputs to go to the High state. This turns the p-channel drivers off and the n-channel drivers on. A moving motor will generate back EMF and current will flow through the n-channel drivers. The motor torque generated by this current opposes the motion of the motor, thus slowing it.

clk cycles	1	2	3	4	5	6	7	8	9	10	11
cmd data	1	1	1	1	1	0	0	0	0	0	0

Active on falling edge of 11th clock.

4. LOCK: When the lock bit (Bit 6) of the command register is set High, the outputs Phase 1H and Phase 3L will be pulse width-modulated regardless of the state of the Hall effect sensor inputs. The detent torque created will force the motor into a fixed position.

clk cycles	1	2	3	4	5	6	7	8	9	10	11
cmd data	1	1	1	1	1	1	0	0	0	0	0

Active on falling edge of 11th clock.

5. ENABLE: Enable is a digital on/off switch (Bit 3) and can be used to insure that the outputs are completely off when no drive is required.

clk cycles	1	2	3	4	5	6	7	8	9	10	11
cmd data enable)	1	1	1	0	0	0	0	0	0	0	0
cmd data disabled)	1	1	0	0	0	0	0	0	0	0	0

6. 60° or 120° Commutation Select (60-120): Setting this bit Low allows the Hall effect sensor inputs to commutate at 120 electrical degrees. When set High,

clk cycles	1	2	3	4	5	6	7	8	9	10	11
cmd data	1	1	1	0	0	0	1	0	0	0	0

the sensor inputs can be reconfigured for driving motors with 60 degree commutation cycles. This is done by connecting Hall sensor 2 to the Pin HS3. Hall sensor 3 is connected to Pin HS2. HS1 is unchanged.

The Sawtooth Oscillator

The oscillator develops a sawtooth waveform on pin R_T/C_T (Pin 7) by charging a capacitor C_T through the resistor R_T. The internal DC trip points of the oscillator are at V_{DD} and V_{DD}. At the end of each timing cycle, a low duty cycle output pulse is generated on "OSC OUT" (Pin 6). This output pulse sets the output of two internal R/S latches High, which makes the "CYCLE COMMAND" (internal) Active-High. This will allow the outputs to go to the last programmed state with respect to the condition of the Hall sensor inputs.

The Pulse Width Modulator (PWM) Comparator

Under current mode control, instantaneous current in the motor is summed at the input of the

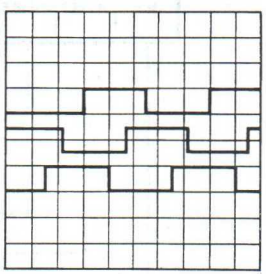
op amp (Pin 12) to obtain the current mode feedback signal. Thus the error loop controlling the PWM duty cycle is normally responsive to motor current (see Figure 4).

The output of the error amplifier (Pin 8) is compared by the PWM to the analog ramp of the oscillator. When the ramp voltage exceeds the voltage at the output of the error amplifier, one R/S latch is reset, the "Cycle Command"

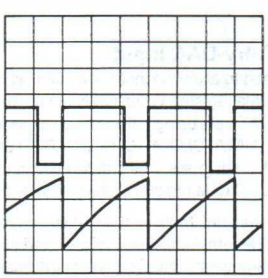
is then Low and the output drivers are turned off. This condition is maintained until the next "OSC OUT" pulse is again generated by the oscillator. This prevents double pulsing at the outputs due to switching noise at the inputs of the PWM within a cycle (see Figures 3b and c).

Overcurrent Protection

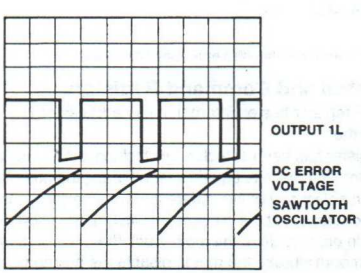
The current sense comparator input (Pin 14) allows the outputs to be shut off by resetting the other R/S (overcurrent) latch. Overcurrent protection is provided by the I-sense comparator with the input connected to a voltage node that is sensitive to the forward motor current. When the voltage at Pin 14 exceeds 0.5V, the R/S latch is reset and the outputs will be turned off until the next oscillator cycle. This provides cycle-by-cycle current limiting. The 0.5V reference voltage is derived from the external 5V reference at $DAC_{REF\ IN}$ (Pin 5).



a. Hall Sensor Commutation



b. PWM Duty Cycle Generation



c. Error Amplifier Output vs Sawtooth and Duty Cycle

Figure 3.

NE5570 APPLICATIONS

Driving the Brushless Motor Commutation

Today's DC brushless motor is the result of an effort to improve overall DC motor reliability by eliminating contact brushes to the armature. A secondary result is that RFI is greatly reduced. Motor manufacturers are now working to improve the rotor magnetics with rare earth materials such as neodymium iron and samarium cobalt. Inherent in the process of removing brush-type mechanical commutation to the rotating magnetics is the introduction of some method of electrically switching field polarity synchronously with rotor position. Hall effect magnetic field sensors and the necessary logic for commutation are now built as an integral part of the motor. TTL-compatible outputs make interfacing to external controllers a simple matter. With just a few logic gates driven by the Hall signals (as shown in Figure 5), an

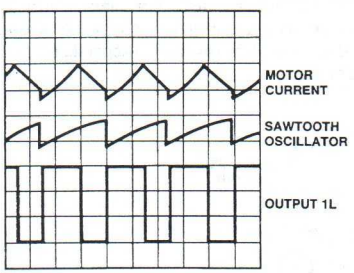


Figure 4. Motor Current vs Ramp and Duty Cycle

electrically-commutated brushless motor may be made to run on a single DC supply.

A Hall element gives a positive output when in close proximity to the north pole of a rotor magnet. The three-phase windings are connected in a star configuration with a 6-switch drive as shown in Figure 6. Programming the switches in the proper sequence will create a rotating vector field, driving the rotor in a clockwise or counter-clockwise direction. Phase signals are programmed as shown in the example.

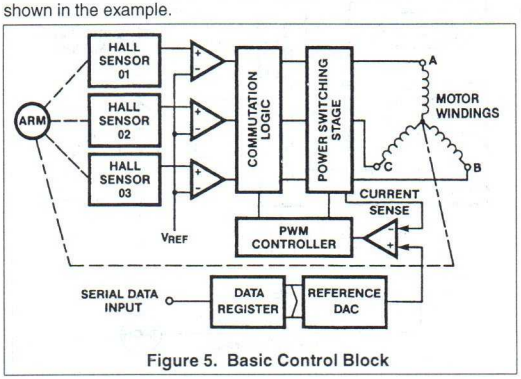


Figure 5. Basic Control Block

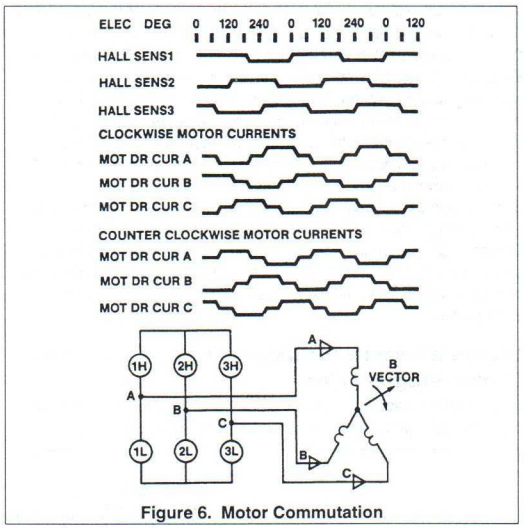


Figure 6. Motor Commutation

PWM Controls Motor Current

With the motor commutation provided from shaft position, field coils are switched in the proper manner to develop self-synchronous rotation. This differs from the AC induction motor which is dependent on line frequency and so operates at fixed speeds that are submultiples of 50, 60, or 400Hz. For example: the brushless motor, which is synchronous with the commutation signals, develops rotational velocity based on its speed-torque characteristics much as does a DC brush motor. Speed then must be approached as a function of torque, average current, acceleration and load inertia in addition to supply voltage. High efficiency results from controlling speed by means of pulse width-modulated drive to the field windings of the motor. Normally PWM frequency is set at a rate orders of magnitude above the commutation rate. Generally, this is determined by the motor inductance and field resistance. Ideal switching rates are above the audio range, that is, 15 to 20kHz and greater.

With a fixed supply voltage, a change in the PWM duty cycle controls the average current in the motor. This develops a control variable capable of determining motor torque under varying load conditions.

Instantaneous control of duty cycle allows acceleration modeling, making an algorithm under microprocessor control a repeatably accurate technique for various ramp-up/ramp-down subroutines.

Constant Torque with the NE5570

Using current sense feedback to force the brushless motor switching currents to null at some average fixed level results in a constant torque output. (See Figure 7.)

With the NE5570, input commands to the current control DAC force the PWM duty cycle to generate a fixed output current to the motor. Once a current control command is received by the NE5570, the DAC latches the data into an 8-bit register and the motor is under local closed-loop control. With this configuration, a remotely located microprocessor or serial command module can generate new torque control commands and the controller will instantaneously respond with the required output current level. The NE5570 also contains internal automatic cycle-by-cycle overcurrent protection to limit the duty cycle in case of an overload such as a stalled rotor condition. This feature is independent of the DAC control signal to the PWM. Current monitoring may be carried out by use of a simple resistive shunt in the driver current return leads, or a current transformer may be implemented for developing step-up voltage gain and lower impedance.

Constant Velocity (Voltage Mode) and Acceleration Control Programming

By providing velocity feedback in addition to a motor drive current loop, an additional degree of control may be added. Velocity feedback may be derived from the commutation signals in cases where low cost is of primary concern or a tach generator may be added if increased inertia is not prohibited. A shaft encoder may also be utilized if a direct microprocessor control loop is required.

Velocity feedback may be addressed in either of two ways: Digital, where the shaft speed and position are under constant monitoring by the microprocessor; Analog loop, in which case direct voltage feedback is summed within the PWM control loop as shown in Figures 8, 9, and 10.

Multiple Motors Under Serial Bus Control

The requirement to control a number of brushless motors of various sizes and at different physical locations represents an interesting challenge. An ideal solution is demonstrated in an example which uses the Inter-IC (I^2C) bus in modified form. The NMOS SCN8400 provides serial bus control using standard two-wire bus architecture, data plus clock; however, the NE5570 requires an additional chip enable signal input line (CE) in order to operate. As shown in Figure 11, this is easily implemented by using a separate I/O port signal line for each motor

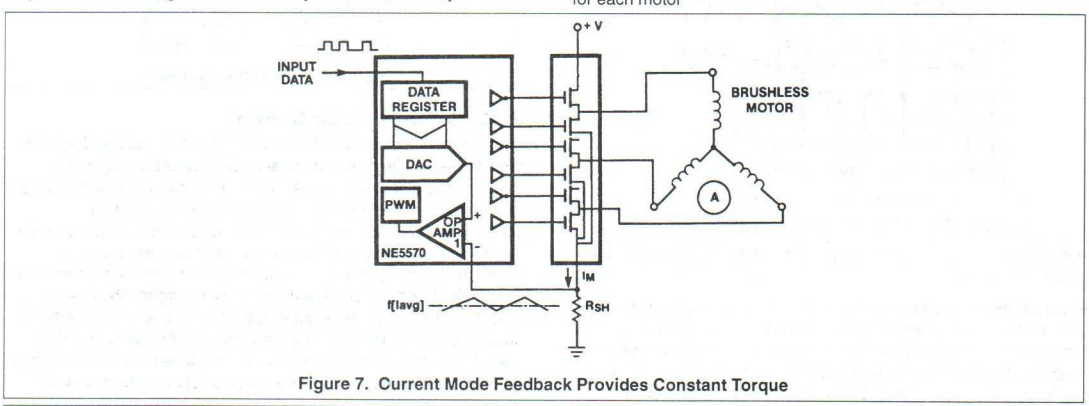


Figure 7. Current Mode Feedback Provides Constant Torque

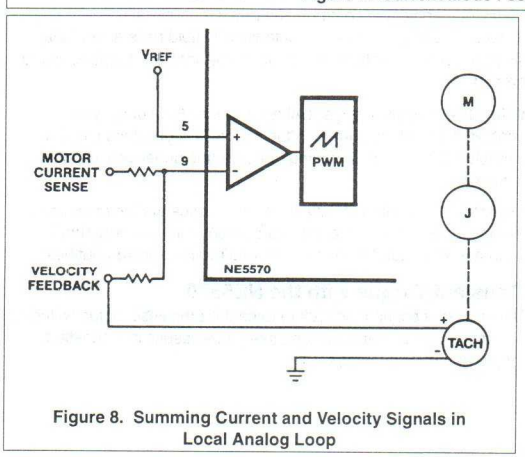


Figure 8. Summing Current and Velocity Signals in Local Analog Loop

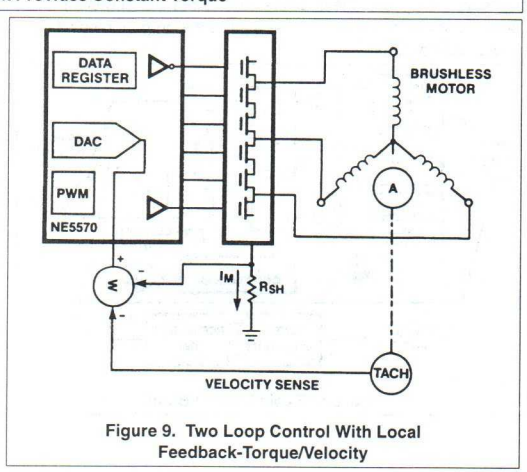


Figure 9. Two Loop Control With Local Feedback-Torque/Velocity

control module. To select a particular motor, the I/O port sends the CE signal which enables the respective NE5570 to receive the proper input data commands. This allows several motors within a radius of approximately 10 to 12 feet to be controlled by a single I^2C processor simultaneously. (See Figure 11.)

ESD Protection

The NE5570 must be protected from external power supply transients which exceed 16V — even for a few nanoseconds (see Figure 12). This is due to the presence of a snap-back clamp circuit connected from the supply pin (Pin 24) to ground. This device forms a negative resistance switch (NPN) which, if not current-limited after turn-on, can short the supply to ground. The resulting current obviously will destroy the device.

Power-Up Sequence

In order to insure that the outputs of the NE5570 are in defined states at power-up, some timing delays must be added externally. It is essential that the V_{REF} supply (Pin 5) come up before the 12V supply. Minimum delay of the 12V supply with respect to V_{REF} is 1µs. Second, reset must be programmed Low (active) for a period lasting until both the V_{DD} supply (Pin 24) and V_{REF} (Pin 5) are active.

By adding a PNP transistor, as shown in Figure 13, with an RC delay circuit connected from V_{REF} (+5V) to the base of the transistor, initial power-up starts with the condition that the base is at 0V and the transistor is in conduction shorting Pin 4 to Ground. As the base-emitter voltage approaches 0V, Q1 turns off, setting the internal logic in the proper states. Pin 4 is now accessible to external reset signals for normal programming.

A SERIAL BUS MICROPROCESSOR

Interface for the NE5570

Figure 14 shows a completed design example of a brushless motor controller which utilizes an SCN8400 microprocessor with a piggyback 2732 PROM as an automatic function generator. Command selection is via a small keypad attached to the PC board. The procedure calls for entry of the DAC commands in three-digit format with a range from 0 to 255. The complete controller is mounted on a single PC board as shown in Figure 15. Lock, Brake, and Disable commands, in addition to Reverse, are entered on separate keys from the DAC commands.

Clock and Data from the microprocessor (SCN8400) are all that comprise a normal I^2C bus using the standard Philips I^2C peripherals; however, the NE5570 requires a

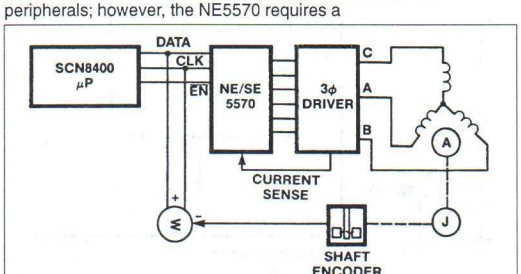


Figure 10. Velocity Feedback With Microprocessor ControllerResponse -- Serial Bus

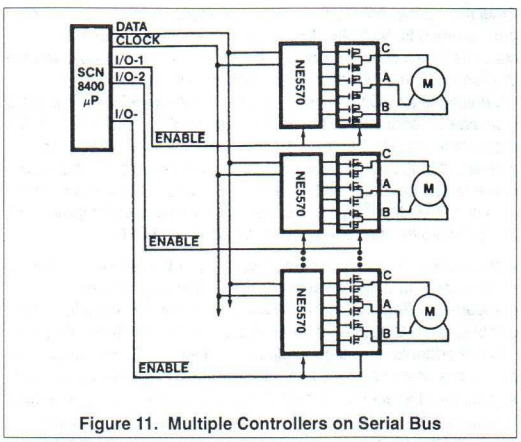


Figure 11. Multiple Controllers on Serial Bus

Chip Enable and this must be provided from a separate I/O port (Pin 27).

A Microprocessor-Controlled Servo with Torque or Velocity Feedback (Figure 14)

Input data loading of the command word is illustrated in Figure 14. After lowering the chip enable input (Pin 3), an 11-bit word is loaded in sequence. Data bits are latched during rising edges of the clock. After 11 clock pulses, the chip enable is deactivated by raising Pin 3 High.

The 11-bit data word is organized into two fields: a rotation field and a speed field. From Figure 15, Bits 1, 2, and 3 determine the direction of rotation; a 101 indicates clockwise, a 100 indicates counter-clockwise. Data Bits 4-11 are decoded as one of 256 possible speeds, from 11 to 255.

Commands are as follow:

Lock — On this command the motor magnets oppose each other and result in the motor coming to an immediate halt in a fixed position with detent torque. *H4BrakelDuring motor operation, issuing the brake command causes the motor to come to an immediate halt, thus ending in a non-torqued or disabled state.

Disable — Issuing the disable command causes the driver FETs to immediately disengage and causes an immediate condition of zero torque. If issued during motor rotation, the motor will immediately cease to be driven and will slow to a stop from its own frictional losses.

Run — The run command tells the NE5570 to activate immediately using the command that is currently resident in the 11-bit shift register. When coming out of a Lock, Brake, or Disabled state, the NE5570 must be given both a speed/rotation command plus an additional run command to start.

The special function commands are defined by the 11-bit words shown in Figure 17.

Interfacing to the NE5570 may be accomplished by almost any microcontroller or computer through the use of 3 I/O port lines.

Emulation of the motor commands may easily be implemented via port commands. Multiple NE5570s may be implemented and controlled via a central processor by address decoding logic and the chip enable lines. As an example, Figure 14 illustrates the interfacing to an SCN8400 microcontroller via the I²C bus. The Data input line is connected to the SDA (serial data) pin on the SCN8400 microcontroller (Pin 2). The Clock input line from the NE5570 is connected to the serial clock pin (Pin 3), and the Chip Enable input is connected to Port 2, Bit 2 (Pin 27 on the 8400). To emulate the commands via the I²C port, a series of instructions are incorporated in a software routine called "motor" listed in Figure 18.

In this routine, the rotation control word is pre-loaded in the 3 MSBs of Register 1, and the remaining 8 bits defining speed are pre-loaded in Register r0. This routine accomplishes the following: disables any I²C device that may also be on the bus by issuing the "disable address" (it is a good idea to disable any CLIPs peripherals on the bus when using the bus for any non-I²C operations); second, toggles the chip enable High-Low-High once (an optional procedure to ensure that the shift register is initialized); third, programs the interface for a no-acknowledge mode (this tells the microcontroller to not generate an extra clock pulse for a peripheral acknowledgement; the NE5570 does not generate an acknowledgement). The routine then activates the NE5570 via port instructions, and transmits a series of 11 bits, the 3 MSBs from register f1, and all 8 bits from register r0 in high-bit to low-bit order. Assuming that these registers are properly loaded with a correct motor command, all motor control possibilities can be transmitted via this routine. To finish, the routine deactivates the chip enable line, "wakes up" the CLIPs peripherals that may be on the bus by issuing a STOP command, restores the normal I²C mode of operation, and returns.

This configuration may be extended to control multiple NE5570s by simply utilizing different port lines connected directly or through a decoder to each chip enable line on the motor controller ICs. The same routine may be used; just activate the appropriate chip enables. For additional serially-loading peripherals, refer to application notes AN163 and AN1681 "TEA1017: Using the C-Bus Devices on the I²C Bus".

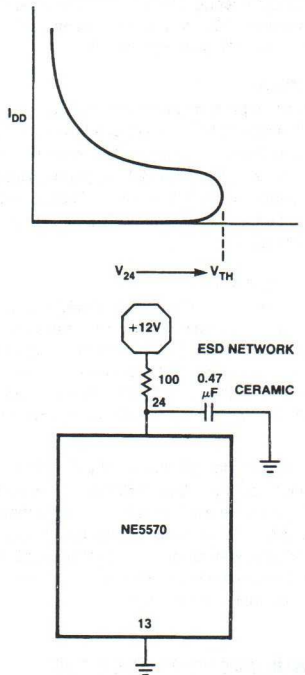


Figure 12. Recommended Protection Circuit for NE5570

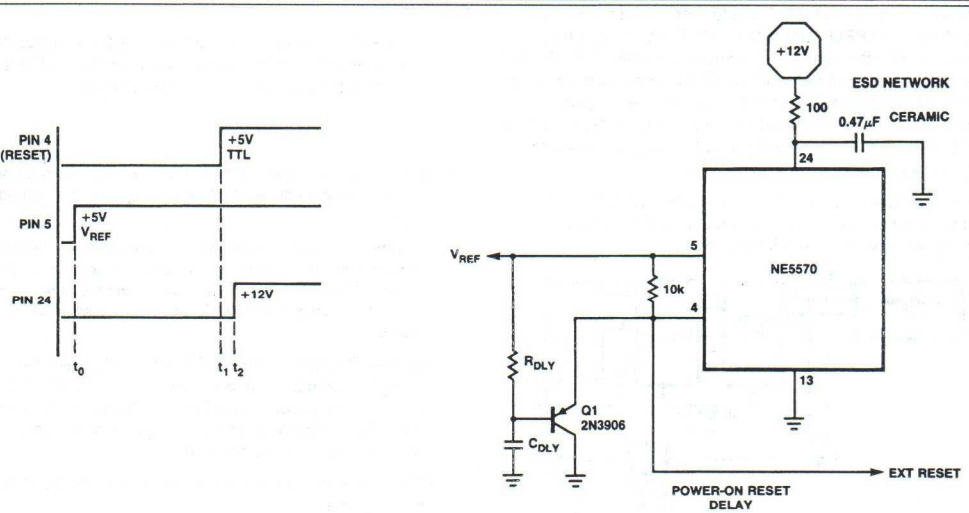


Figure 13. Supply and Reference Start Sequence

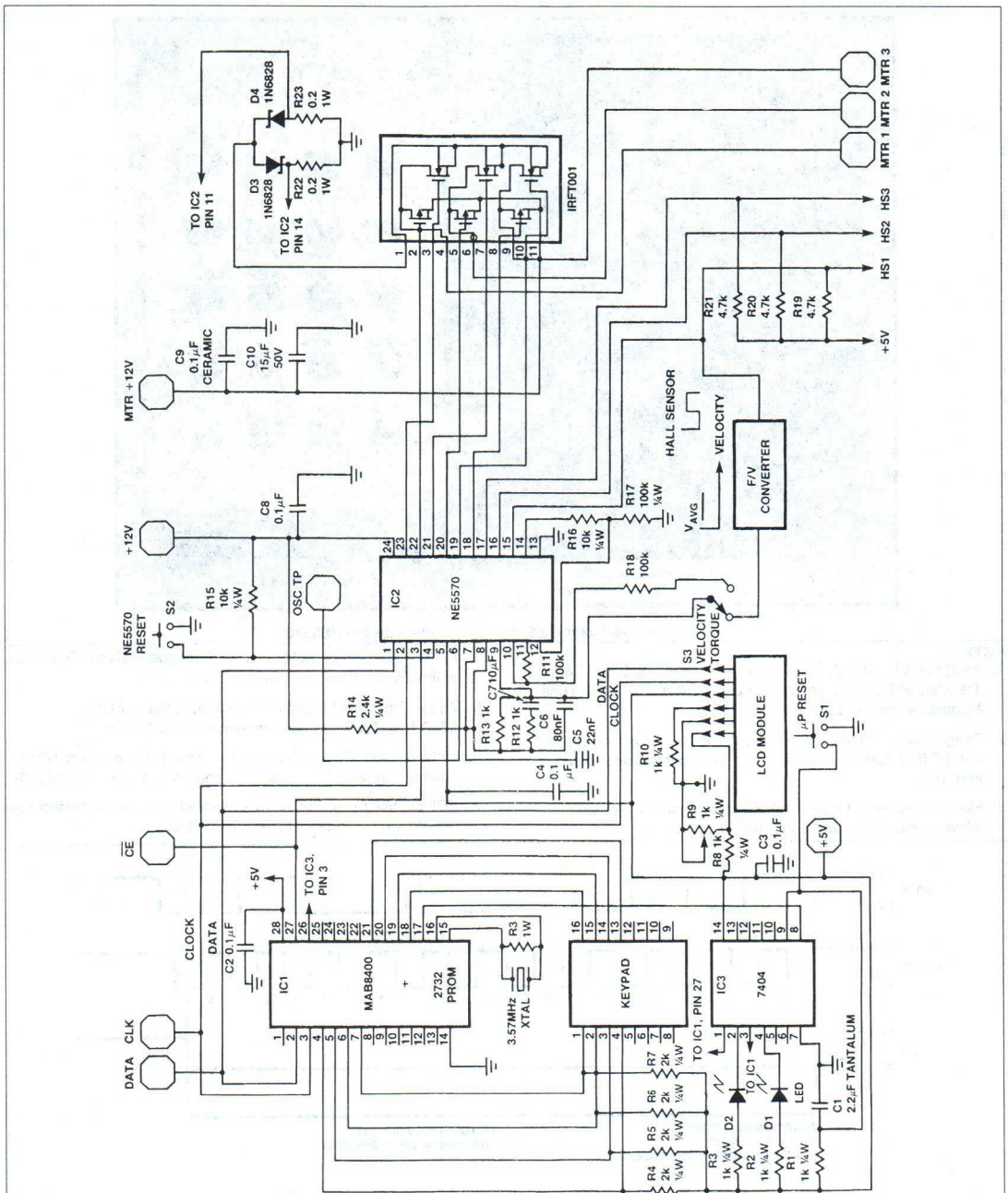


Figure 14. SCN8400 Serial Bus Microprocessor Controller

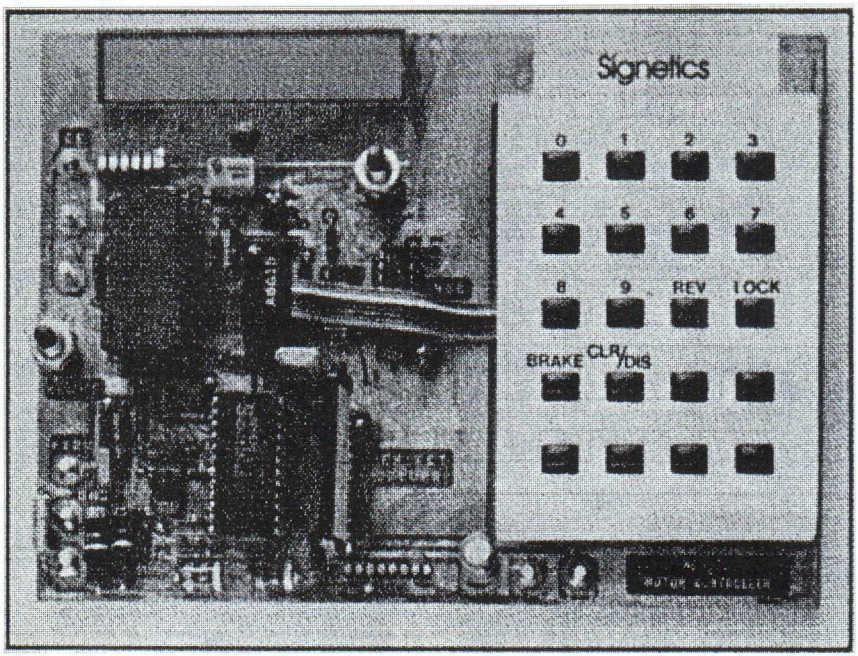


Figure 15. Constant Current Motor Drive With the NE5570

NOTES:

1. Fenger, Carl, "AN163: Small Area Networks Using Serial Data Transfer," Philips Semiconductors Linear Data and Applications Manual, Volume II, Sunnyvale, CA, 1985.
2. Fenger, Carl, "AN1681: TEA1017: Using the C-Bus Devices on the I2C Bus, "Linear Division, Philips Semiconductors Corporation, 1986.
3. Holt, Charles A., Introduction to Electromagnetic Fields and Waves; John Wiley and Sons, 1963.
4. Rutkowski, George B., Handbook of Integrated Circuit Operational Amplifiers; Prentice Hall, Inc., 1975.
5. Airpax Brushless Motors-Model K85901; Pub. Catalog CMO-834, 1983, Airpax Corporation, Cheshire, CN.
6. MotorCon '85, Official Proceedings of the 7th International Conference, Chicago, IL, Intertec Communications, Inc., Oxnard, CA.
7. PCI '82, Volume 4, Conference Proceedings, San Francisco, CA, Intertec Communications, Inc., Oxnard, CA.

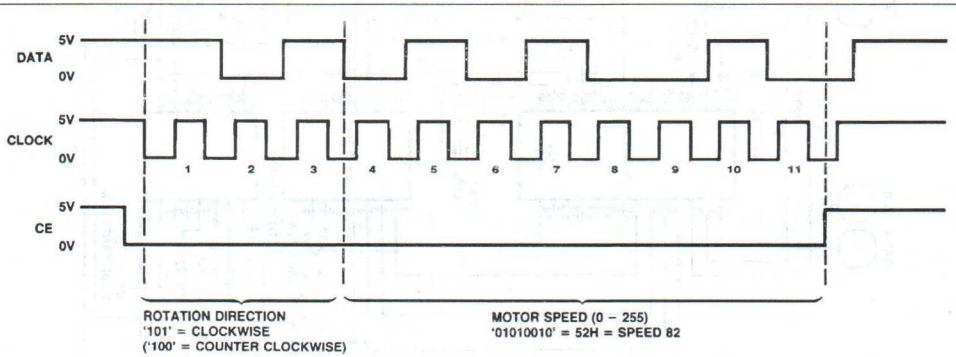


Figure 16. A Typical Command for the NE5570 Motor Controller

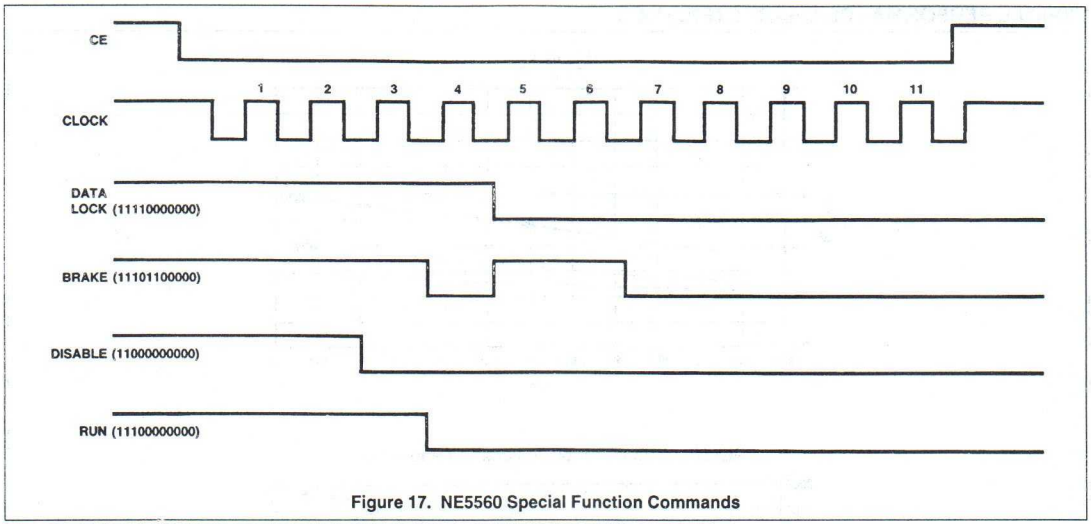


Figure 17. NE5560 Special Function Commands

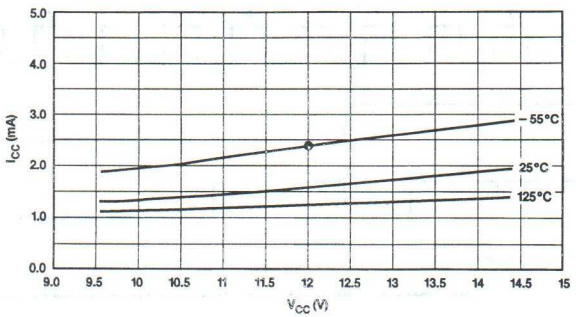
```
Motor           mov s1, #H'18'      ;Reset S10 status.
                mov s0, #H'02'      ;Load iic disable.
                mov s1, #H'0F8'     ; Start condition
                call pinwt          ;
                orL p2, #H'02'      ;
                nop                 ;
                anL p2, #H'0FD'     ;Clear motor controller
                nop                 ;
                orL p2, #H'02'      ;
          *
          *     mov s1, #H'18'      ;Initial bus status register to a know
                                    ;state.
                mov s2, #H'07'      ;Leave acknowledge mode
          *                         ;and program bus clock frequency
                                    (45kHz).

                mov s1, #H'0EB'     ;Prepare for a 3-bit transmission.
                mov a, rl           ;send rotation command.
                mov s0, a           ;Transmit first 3-bits.
                call pinwt          ;Wait for transmission complete.
                mov a, r0           ;Get speed command.
                mov s0, a           ;Transmit.
                call pinwt          ;Wait for transmission complete.
                orL p2, #H'02'      ;Deactivate.
                mov s1, #H'0D8'     ;Stop condition
                mov s1, #H'18'      ;reset sio
                mov s2, #H'41'      ;restore ack mode.
                ret
          *
          *
pinwt           mov a, s1           ;Wait for end of serial transmission
                jb4 pinwt           ;via polling of PIN bi in reg s1.
                ret                 ;
```

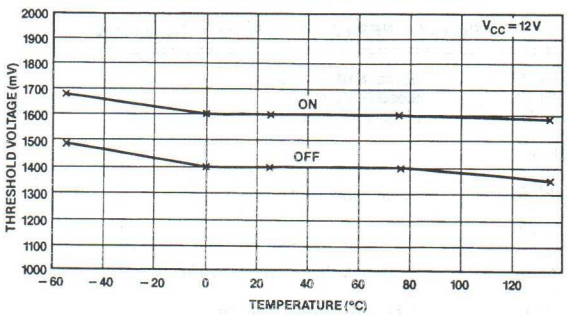
Figure 18. Motor-Controller Routine for Use on the I^2C Bus

TYPICAL PERFORMANCE CHARACTERISTICS

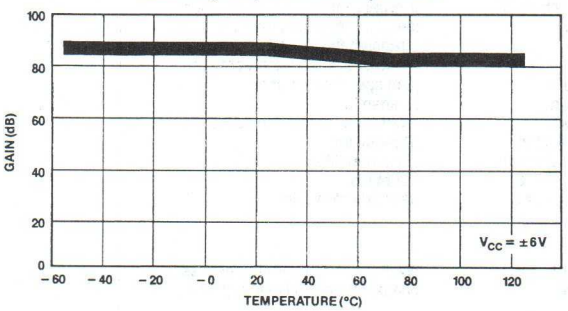
I_{CC} vs V_{CC}



NE5570 Logic Threshold Voltage vs Temperature

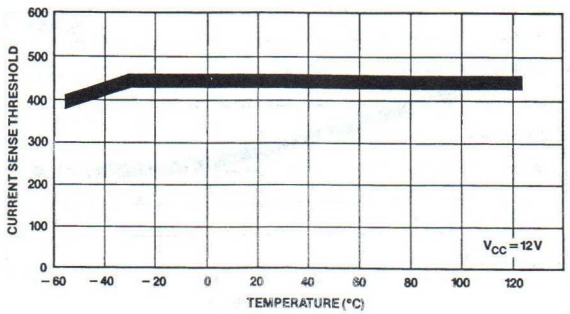


NE5570 Op Amp Gain vs Temperature

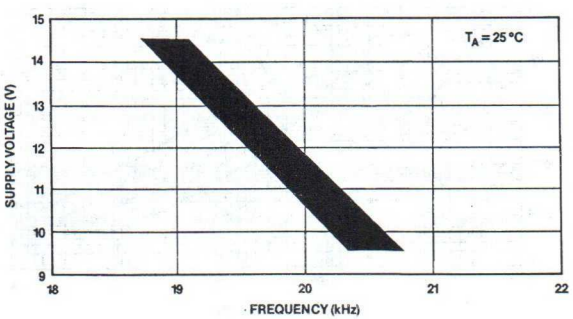


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

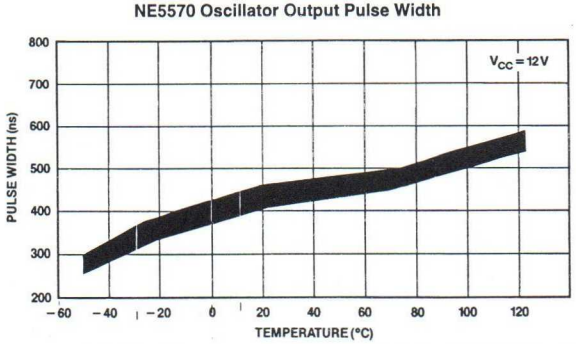
NE5570 Current Sense Comparator Threshold vs Temperature



NE5570 Oscillator Frequency vs Supply Voltage

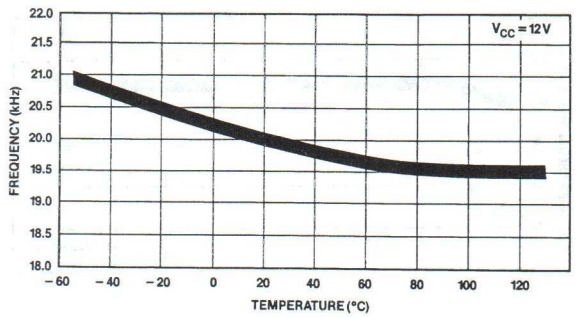


NE5570 Oscillator Output Pulse Width

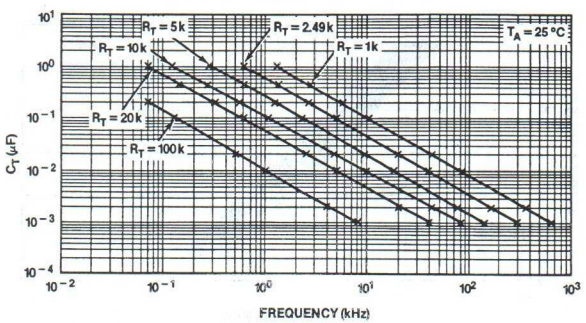


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

NE5570 Oscillator Frequency vs Temperature



Oscillator Frequency vs R_T and C_T



Brushless DC motor drive circuit — TDA5140A

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - 0.8 A output current (typ.)
  - low saturation voltage
  - built-in current limiter
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Position pulse stage for phase-locked-loop control
- Transconductance amplifier for an external control transistor.

APPLICATIONS

- VCR
- Laser beam printer
- Fax machine
- Blower
- Automotive

GENERAL DESCRIPTION

The TDA5140A is a bipolar integrated circuit used to drive 3-phase brushless DC motors in full-wave mode. The device is sensorless (saving of 3 hall-sensors) using the back-EMF sensing technique to sense the rotor position.

QUICK REFERENCE DATA

Measured over full voltage and temperature range.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	note 1	4	–	18	V
V_{VMOT}	input voltage to the output driver stages	note 2	1.7	–	16	V
V_{DO}	drop-out output voltage	I_O = 100 mA	–	0.93	1.05	V
I_{LIM}	current limiting	V_{VMOT} = 10 V; R_O = 3.9 Ω	0.7	0.8	1	A

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN = –AMP IN = 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5140A	18	DIL	plastic	SOT102
TDA5140AT	20	SOL	plastic	SOT163A

BLOCK DIAGRAM

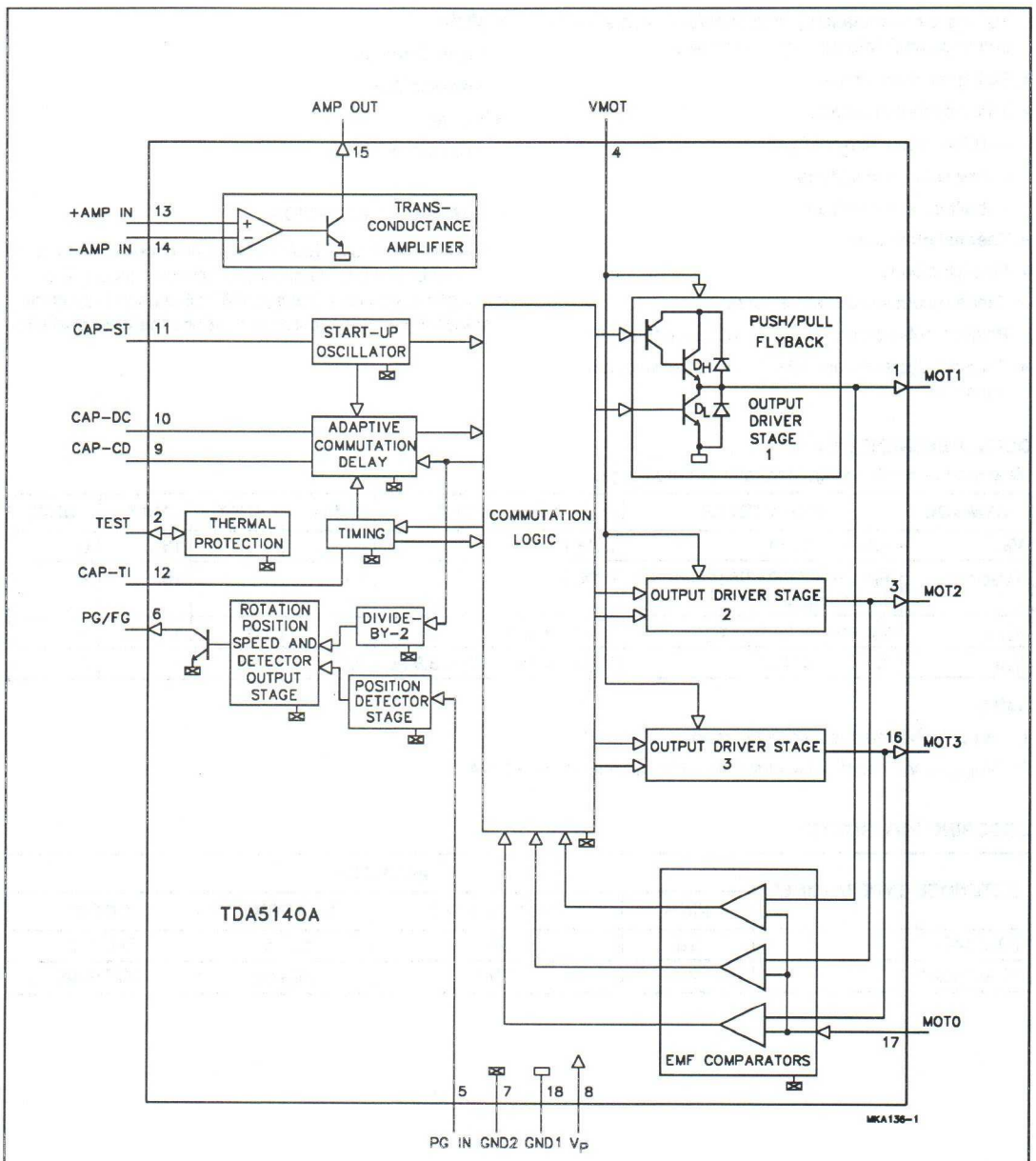


Fig.1 Block diagram (SOT102; DIL18).

PINNING

SYMBOL	PIN DIL18	PIN SO20	DESCRIPTION
MOT1	1	1	driver output 1
TEST	2	2	test input/output
n.c.		3	not connected
MOT2	3	4	driver output 2
VMOT	4	5	input voltage for the output driver stages
PG IN	5	6	position generator: input from the position detector sensor to the position detector stage (optional); only if an external position coil is used
PG/FG	6	7	position generator/frequency generator: output of the rotation speed and position detector stages (open collector digital output, negative-going edge is valid)
GND2	7	8	ground supply return for control circuits
V_P	8	9	positive supply voltage
CAP-CD	9	10	external capacitor connection for adaptive communication delay timing
CAP-DC	10	11	external capacitor connection for adaptive communication delay timing copy
CAP-ST	11	12	external capacitor connection for start-up oscillator
CAP-TI	12	13	external capacitor connection for timing
+AMP IN	13	14	non-inverting input of the transconductance amplifier
–AMP IN	14	15	inverting input of the transconductance amplifier
AMP OUT	15	16	transconductance amplifier output (open collector)
MOT3	16	17	driver output 3
n.c.	–	18	not connected
MOT0	17	19	input from the star point of the motor coils
GND1	18	20	ground (0 V) motor supply return for output stages

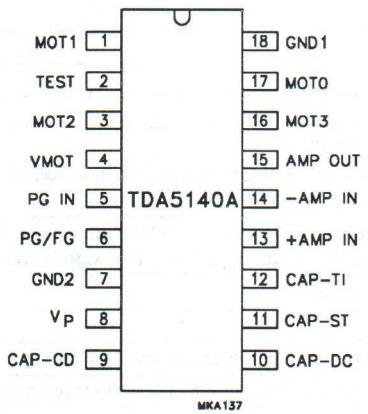


Fig.2 Pin configuration (SOT102; DIL18).

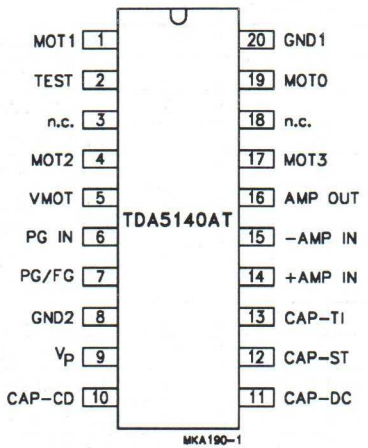


Fig.3 Pin configuration (SOT163A; SO20L).

FUNCTIONAL DESCRIPTION

The TDA5140A offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5140A offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5140A offers the following features:

- Sensorless commutation by using the motor EMF.
- Built-in start-up circuit.
- Optimum commutation, independent of motor type or motor loading.
- Built-in flyback diodes.
- Three phase full-wave drive.
- High output current (0.8 A).
- Outputs protected by current limiting and thermal protection of each output transistor.
- Low current consumption by adaptive base-drive.
- Accurate frequency generator (FG) by using the motor EMF.
- Amplifier for external position generator (PG) signal.
- Suitable for use with a wide tolerance, external PG sensor.
- Built-in multiplexer that combines the internal FG and external PG signals on one pin for easy use with a controlling microprocessor.
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	18	V
V_I	input voltage; all pins except VMOT	$V_I < 18$ V	−0.3	$V_P + 0.5$	V
V_{VMOT}	VMOT input voltage		−0.5	17	V
V_O	output voltage				
	AMP OUT and PG/FG		GND	V_P	V
	MOT1, MOT2 and MOT3		−1	$V_{VMOT} + V_{DHF}$	V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC		–	2.5	V
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
P_{tot}	total power dissipation	see Figs 4 and 5	–	–	W
V_{es}	electrostatic handling	see "Handling"	–	500	V

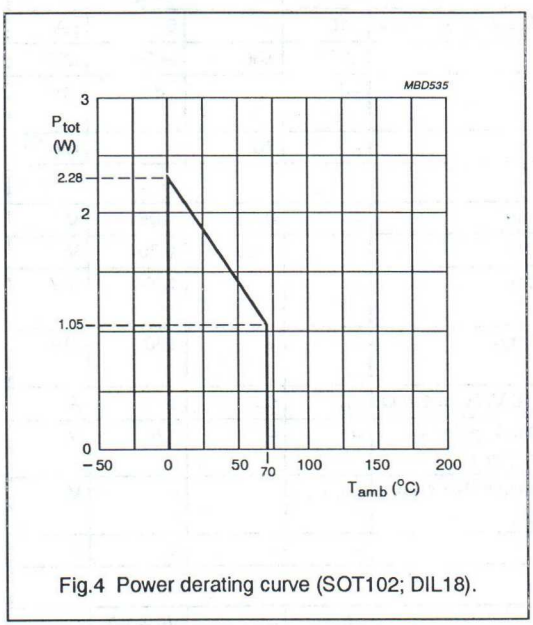


Fig.4 Power derating curve (SOT102; DIL18).

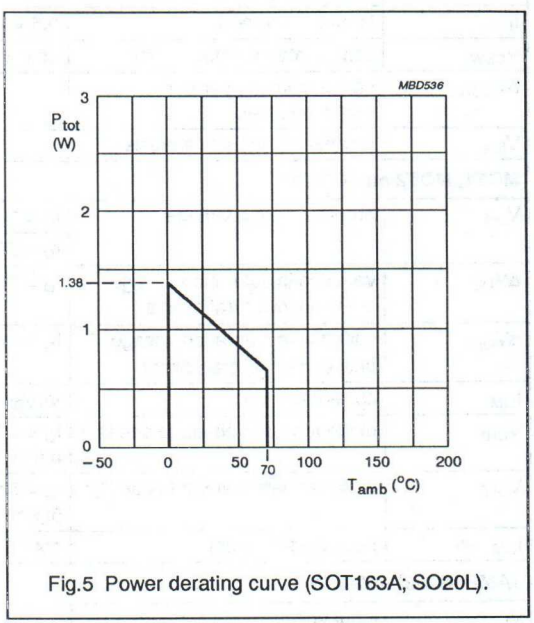


Fig.5 Power derating curve (SOT163A; SO20L).

HANDLING

Every pin withstands the ESD test in accordance with *"MIL-STD-883C class 2"*. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulses − on each pin referenced to ground.

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	4	–	18	V
I_P	supply current	note 2	–	3.7	5	mA
V_{VMOT}	input voltage to the output driver stages	see Fig.1	1.7	–	16	V
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} – 30	–	K
MOT0; centre tap						
V_I	input voltage		–0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} – 1.5 V	–10	–	0	μA
V_{CSW}	comparator switching level	note 3	±20	±30	±40	mV
ΔV_{CSW}	variation in comparator switching levels		–3	0	+3	mV
V_{hys}	comparator input hysteresis		–	75	–	μV
MOT1, MOT2 and MOT3						
V_{DO}	drop-out output voltage	I_O = 100 mA	–	0.93	1.05	V
		I_O = 500 mA	–	1.65	1.80	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = –100 mA	–	–	180	mV
I_{LIM}	current limiting	V_{VMOT} = 10 V; R_O = 6.8 Ω	0.7	0.8	1	A
V_{DHF}	diode forward voltage (diode D_H)	I_O = –500 mA; notes 4 and 5; see Fig.1	–	–	1.5	V
V_{DLF}	diode forward voltage (diode D_L)	I_O = 500 mA; notes 4 and 5; see Fig.1	–1.5	–	–	V
I_{DM}	peak diode current	note 5	–	–	1	A
+AMP IN and –AMP IN						
V_I	input voltage		–0.3	–	V_P – 1.7	V
	differential mode voltage without 'latch-up'		–	–	±V_P	V
I_b	input bias current		–	–	650	nA
C_I	input capacitance		–	4	–	pF
V_{offset}	input offset voltage		–	–	10	mV

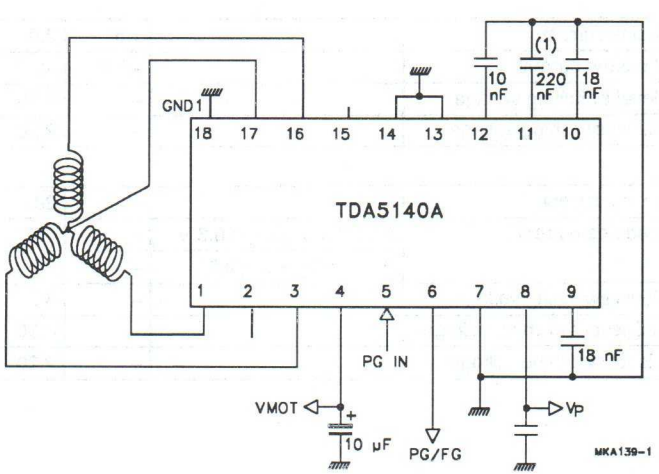
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AMP OUT (open collector)						
I_I	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_O	output voltage		−0.5	–	+18	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	–	60	–	mA/μs
G_{tr}	transfer gain		0.3	–	–	S
PG IN						
V_I	input voltage		−0.3	–	+5	V
I_b	input bias current		–	–	650	nA
R_I	input resistance		5	–	30	kΩ
V_{CWS}	comparator switching level		86	–	107	mV
V_{hys}	comparator input hysteresis		–	±8	–	mV
PG/FG (open collector)						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
$V_{OH(max)}$	maximum HIGH level output voltage		V_P	–	–	V
t_{THL}	HIGH-to-LOW transition time	C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	μs
	ratio of PG/FG frequency and commutation frequency		–	1 : 2	–	
δ	duty factor		–	50	–	%
t_{PL}	pulse width LOW	after a PG IN pulse	5	7	18	μs
CAP-ST						
I_{sink}	output sink current		1.5	2.0	2.5	μA
I_{source}	output source current		−2.5	−2.0	−1.5	μA
V_{SWL}	LOW level switching voltage		–	0.20	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-TI						
I_{sink}	output sink current		–	28	–	μA
I_{source}	output source current	0.05 V < V_{CAP-TI} < 0.3 V	–	−57	–	μA
		0.3 V < V_{CAP-TI} < 2.2 V	–	−5	–	μA
V_{SWL}	LOW level switching voltage		–	50	–	mV
V_{SWM}	MIDDLE level switching voltage		–	0.30	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CAP-CD						
I_{sink}	output sink current		10.6	16.2	22	µA
I_{source}	output source current		−5.3	−8.1	−11	µA
I_{sink}/I_{source}	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage		850	875	900	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V
CAP-DC						
I_{sink}	output sink current		10.1	15.5	20.9	µA
I_{source}	output source current		−20.9	−15.5	−10.1	µA
I_{sink}/I_{source}	ratio of sink to source current		0.9	1.025	1.15	
V_{IL}	LOW level input voltage		850	875	900	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P; I_O = 0 mA.
3. Switching levels with respect to MOT1, MOT2 and MOT3.
4. Drivers are in the high-impedance OFF-state.
5. The outputs are short-circuit protected by limiting the current and the IC temperature.

APPLICATION INFORMATION



(1) Value selected for 3 Hz start-up oscillator frequency.

Fig.6 Application diagram without use of the operational transconductance amplifier (OTA).

Introduction (see Fig.7)

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing (H) and one sinking (L). The third output presents a high impedance (Z) to the motor which enables measurement of the motor back-EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator. In Table 1 the sequence of the six possible states of the outputs has been depicted.

Table 1 Output states.

STATE	MOT1[1]	MOT2[1]	MOT3[1]
1	Z	L	H
2	H	L	Z
3	H	Z	L
4	Z	H	L
5	L	H	Z
6	L	Z	H

Note

1. H = HIGH state;
   L = LOW state;
   Z = high impedance OFF-state.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

The detected zero-crossings are used to provide speed information. The information has been made available on the PG/FG output pin. This is an open collector output and provides an output signal with a frequency that is half the commutation frequency. A VCR scanner also requires a PG phase sensor. This circuit has an interface for a simple pick-up coil. A multiplexer circuit is also provided to combine the FG and PG signals in time.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5140A also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5140A is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patented), possibility of using a pick-up coil without bias current.

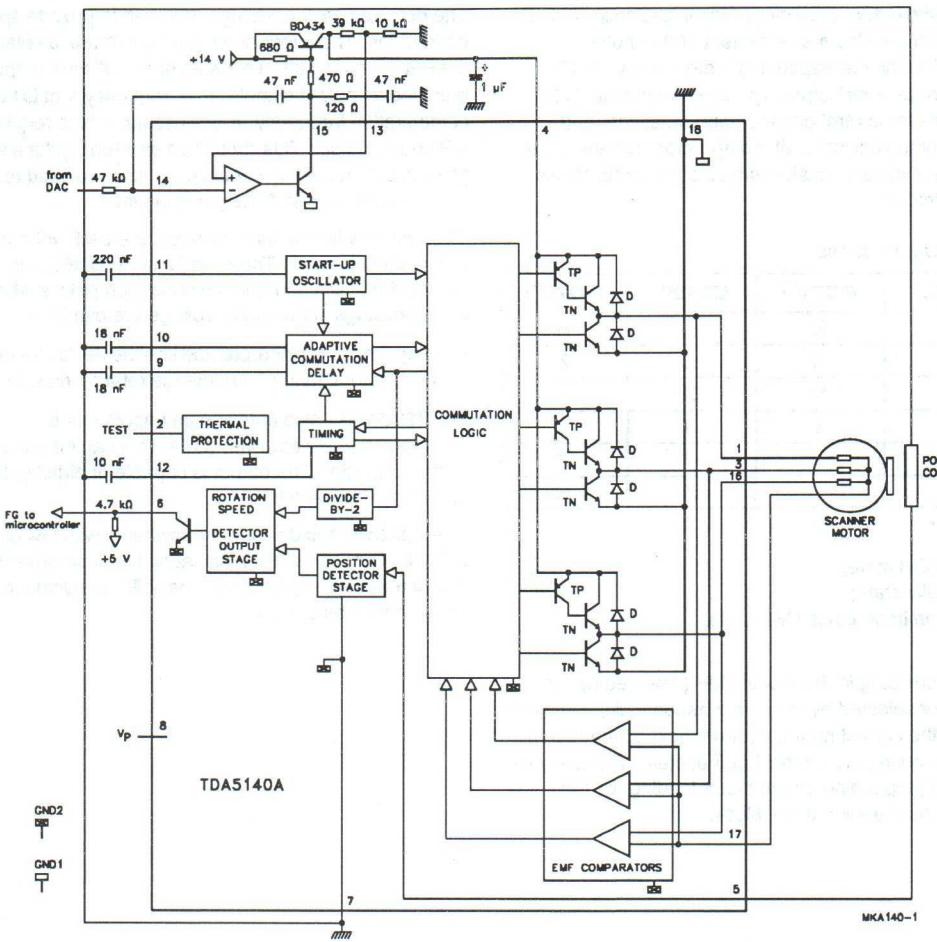


Fig.7 Typical application of the TDA5140A as a scanner driver, with use of OTA.

Adjustments

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator.
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor.
- The timing capacitor; this provides the system with its timing signals.

THE START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:

t_{start} = (2.15 × C) s (with C in μF)

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5140A will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$$f_{osc} = \frac{1}{2\pi\sqrt{\frac{K_t \times I \times p}{J}}}$$

where:

K_t = torque constant (N.m/A)

I = current (A)

p = number of magnetic pole-pairs

J = inertia J ($kg.m^2$)

Example: J = 72 × 10^{-6} $kg.m^2$, K = 25 × 10^{-3} N.m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF, (choose 220 nF).

THE ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 μA and the discharging current 16.2 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{c1}

$$C = \frac{8.1 \times 10^{-6}}{f \times 1.3} = \frac{6231}{f_{c1}} \text{ (C in nF)}$$

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 16.2 μA.

maximum delay = (0.076 × C) ms (with C in nF)

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz, so:

$$\text{CAP-CD} = \frac{6231}{400} = 15.6 \text{ (choose 18 nF)}$$

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 15.5 μA. The same value can be chosen as for CAP-CD. Figure 8 illustrates typical voltage waveforms.

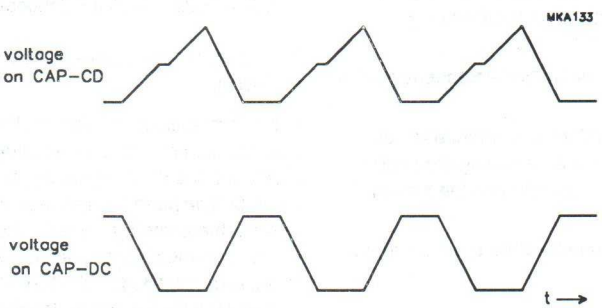


Fig.8 CAP-CD and CAP-DC typical voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).

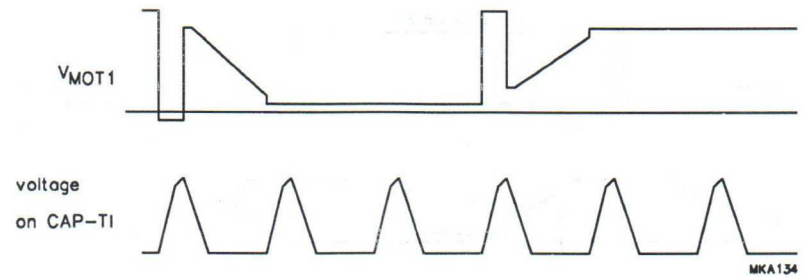
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 μA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 μA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 μA. The watchdog time is the time taken to charge the capacitor, with a current of 5 μA, from 0.3 to 2.2 V.

To ensure that the internal delays are covered CAP-TI must have a minimum value of 2 nF. For the watchdog function a value for CAP-TI of 10 nF is recommended.

To ensure a good start-up and commutation, care must be taken that no oscillations occur at the trailing edge of the flyback pulse. Snubber networks at the outputs should be critically damped.

Typical voltage waveforms are illustrated by Fig.9.



If the chosen value of CAP-TI is too small oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

Fig.9 Typical CAP-TI and V_{MOT1} voltage waveforms in normal running mode.

Other design aspects

There are other design aspects concerning the application of the TDA5140A besides the commutation function. They are:

- Generation of the tacho signal FG
- A built-in interface for a PG sensor
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Reliability.

FG SIGNAL

The FG signal is generated in the TDA5140A by using the zero-crossing of the motor EMF from the three motor windings. Every zero-crossing in a (star connected) motor winding is used to toggle the FG output signal. The FG frequency is therefore half the commutation frequency. All transitions indicate the detection of a zero-crossing (except for PG). The negative-going edges are called FG pulses because they generate an interrupt in a controlling microprocessor.

The accuracy of the FG output signal (jitter) is very good. This accuracy depends on the symmetry of the motor's electromagnetic construction, which also effects the satisfactory functioning of the motor itself.

Example: A 3-phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 × 6 × 6 = 900 Hz, and generates a tacho signal of 450 Hz.

PG SIGNAL

The accuracy of the PG signal in applications such as VCR must be high (phase information). This accuracy is obtained by combining the accurate FG signal with the PG signal by using a wide tolerance external PG sensor. The external PG signal (PG IN) is only used as an indicator to select a particular FG pulse. This pulse differs from the other FG pulses in that it has a short LOW-time of 18 µs after a HIGH-to-LOW transition. All other FG pulses have a 50% duty factor (see Fig.10).

For more information also see *"application note EIE/AN 93014"*.

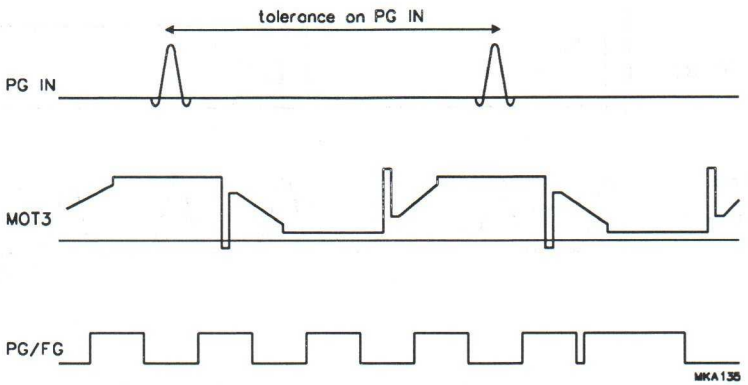


Fig.10 Timing and the FG and PG IN signals.

The special PG pulse is derived from the negative-going zero-crossing from the MOT3 output (pin 16). The external PG signal (PG IN on pin 5) must sense a positive-going voltage (>80 mV) within 1.5 to 7.5 commutation periods before the negative-going zero-crossing in MOT3 (see Fig.10).

The voltage requirements of the PG IN input are such that an inexpensive pick-up coil can be used as a sensor (see Fig.11).

Example: If p = 6, then one revolution contains 6 × 6 = 36 commutations. The tolerance is 6 periods, that is 60 degrees (mechanically) or 6.67 ms at 1500 rpm.

If a PG sensor is not used, the PG IN input must be grounded, this will result in a 50% duty factor FG signal.

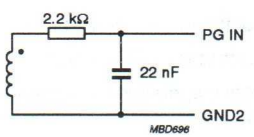


Fig.11 Pick-up coil as PG sensor.

THE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier. The common mode input range includes ground (GND) and rises to V_P – 1.7 V. The high sink current enables the OTA to drive a power transistor directly in an analog control amplifier.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (AMP OUT) to the positive supply, a positive-going voltage is found when the non-inverting input (+AMP IN) is positive with respect to the inverting input (–AMP IN). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

MOTOR CONTROL

DC motors can be controlled in an analog manner using the OTA.

For the control an external transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.7).

RELIABILITY

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+15%). This means that the current to and from the output stages is limited.
- Thermal protection of the six output transistors is achieved by each transistor having a thermal sensor that is active when the transistor is switched on. The transistors are switched off when the local temperature becomes too high.

It is possible, that when braking, the motor voltage (via the flyback diodes and the impedance on VMOT) may cause higher currents than allowed (>0.6 A). These currents must be limited externally.

Brushless DC motor drive circuit

TDA5141

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - output current 1.9 A (typ.)
  - low saturation voltage
  - built-in current limiter
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Position pulse stage for phase-locked-loop control
- Transconductance amplifier for an external control transistor.

APPLICATIONS

- VCR
- Laser beam printer
- Fax machine.

GENERAL DESCRIPTION

The TDA5141 is a bipolar integrated circuit used to drive 3-phase brushless DC motors in full-wave mode. The device is sensorless (saving of 3 hall-sensors) using the back-EMF sensing technique to sense the rotor position. It is ideally suited for applications requiring powerful output stages (minimum current limit of 1.9 A).

QUICK REFERENCE DATA

Measured over full voltage and temperature range.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	note 1	4	–	18	V
V_{VMOT}	input voltage to the output driver stages	note 2	1.7	–	16	V
V_{DO}	drop-out output voltage	I_O = 100 mA	–	0.9	1.05	V
I_{LIM}	current limiting	V_{VMOT} = 10 V; R_O = 1.2 Ω	1.6	1.9	2.3	A

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN = –AMP IN = 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5141	18	DIL	plastic	SOT102
TDA5141T	28	SOL	plastic	SOT136A
TDA5141AT	20	SOL	plastic	SOT163A

BLOCK DIAGRAM

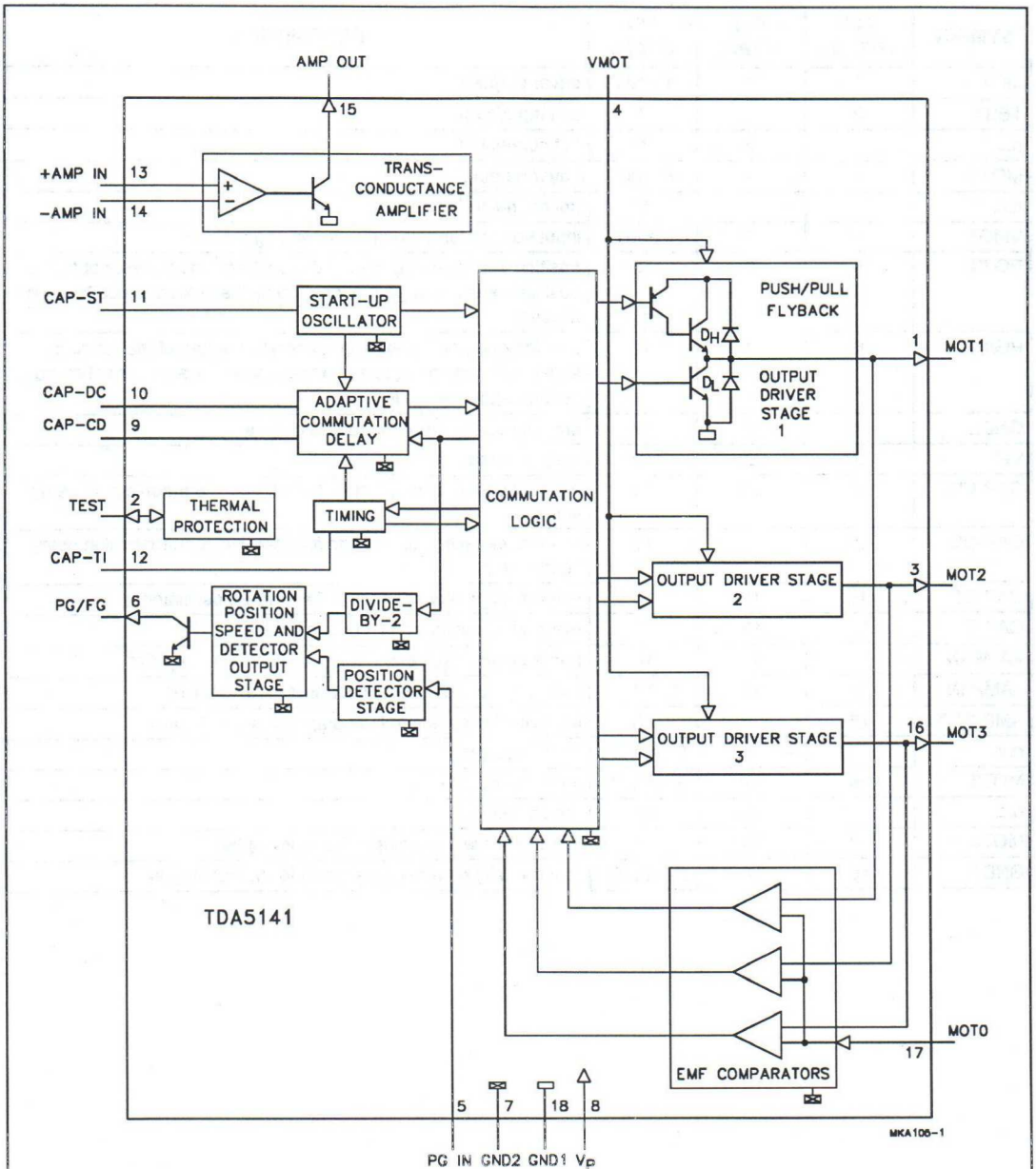


Fig.1 Block diagram (SOT102; DIL18).

PINNING

SYMBOL	PIN DIL18	PIN SO20L	PIN SO28L	DESCRIPTION
MOT1	1	1	1 and 2	driver output 1
TEST	2	2	3	test input/output
n.c.		3	4	not connected
MOT2	3	4	5 and 6	driver output 2
n.c.	–	–	7	not connected
VMOT	4	5	8 and 9	input voltage for the output driver stages
PG IN	5	6	10	position generator: input from the position detector sensor to the position detector stage (optional); only if an external position coil is used
PG/FG	6	7	11	position generator/frequency generator: output of the rotation speed and position detector stages (open collector digital output, negative-going edge is valid)
GND2	7	8	12	ground supply return for control circuits
V_P	8	9	13	supply voltage
CAP-CD	9	10	14	external capacitor connection for adaptive communication delay timing
CAP-DC	10	11	15	external capacitor connection for adaptive communication delay timing copy
CAP-ST	11	12	16	external capacitor connection for start-up oscillator
CAP-TI	12	13	17	external capacitor connection for timing
+AMP IN	13	14	18	non-inverting input of the transconductance amplifier
–AMP IN	14	15	19	inverting input of the transconductance amplifier
AMP OUT	15	16	20	transconductance amplifier output (open collector)
n.c.	–	–	21 and 22	not connected
MOT3	16	17	23 and 24	driver output 3
n.c.	–	18	25	not connected
MOT0	17	19	26	input from the star point of the motor coils
GND1	18	20	27 and 28	ground (0 V) motor supply return for output stages

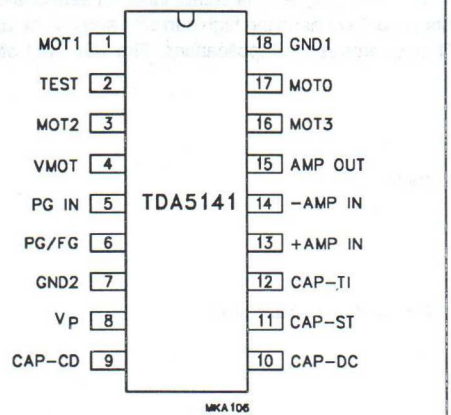


Fig.2 Pin configuration (SOT102; DIL18).

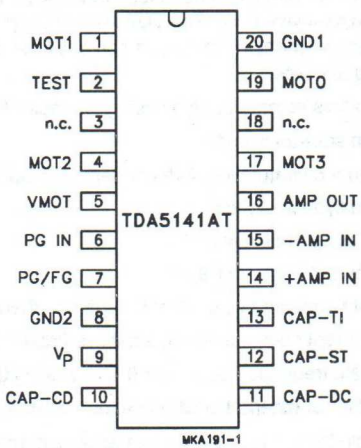


Fig.3 Pin configuration (SOT163A; SO20L).

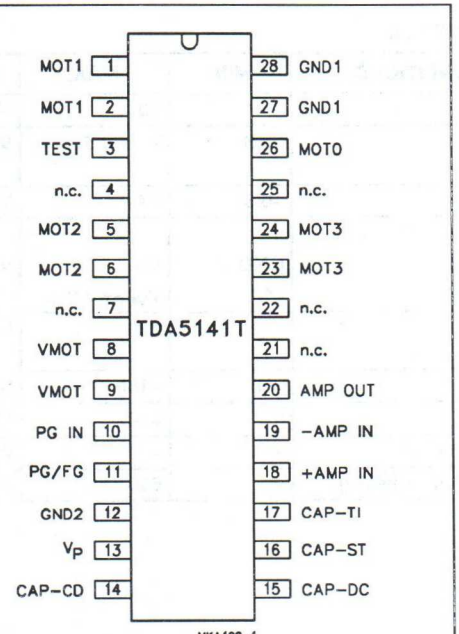


Fig.4 Pin configuration (SOT136A; SO28L).

FUNCTIONAL DESCRIPTION

The TDA5141 offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5141 offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5141 offers the following features:

- Sensorless commutation by using the motor EMF.
- Built-in start-up circuit.
- Optimum commutation, independent of motor type or motor loading.
- Built-in flyback diodes.
- Three phase full-wave drive.
- High output current (1.9 A).
- Outputs protected by current limiting and thermal protection of each output transistor.
- Low current consumption by adaptive base-drive.
- Accurate frequency generator (FG) by using the motor EMF.
- Amplifier for external position generator (PG) signal.
- Suitable for use with a wide tolerance, external PG sensor.
- Built-in multiplexer that combines the internal FG and external PG signals on one pin for easy use with a controlling microprocessor.
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	18	V
V_I	input voltage; all pins except VMOT	$V_I < 18$ V	–0.3	$V_P + 0.5$	V
V_{VMOT}	VMOT input voltage		–0.5	17	V
V_O	output voltage				
	AMP OUT and PG/FG		GND	V_P	V
	MOT1, MOT2 and MOT3		–1	$V_{VMOT} + V_{DHF}$	V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC		–	2.5	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
P_{tot}	total power dissipation	see Figs 5 to 7	–	–	W
V_{es}	electrostatic handling	see Chapter "Handling"	–	500	V

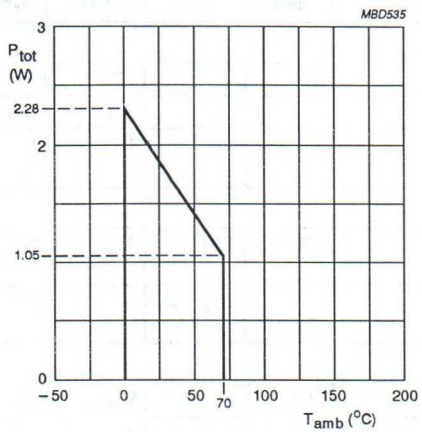


Fig.5 Power derating curve (SOT102; DIL18).

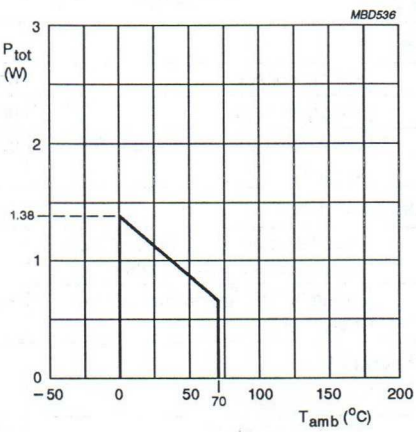


Fig.6 Power derating curve (SOT163A; SO20L).

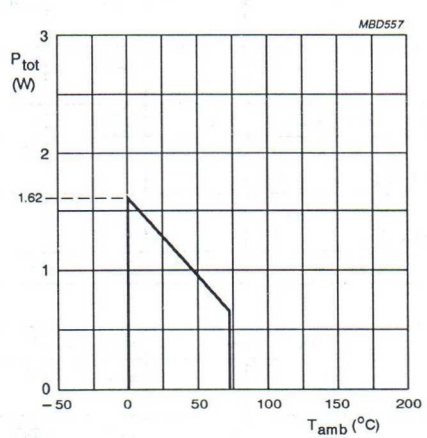


Fig.7 Power derating curve (SOT136A; SO28L).

HANDLING

Every pin withstands the ESD test according to *"MIL-STD-883C class 2"*. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulses − on each pin referenced to ground.

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	4	–	18	V
I_P	supply current	note 2	–	5.2	6.8	mA
V_{VMOT}	input voltage to the output driver stages	see Fig.1	1.7	–	16	V
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} – 30	–	K
MOT0; centre tap						
V_I	input voltage		–0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} – 1.5 V	–10	–	0	µA
V_{CSW}	comparator switching level	note 3	±20	±30	±40	mV
ΔV_{CSW}	variation in comparator switching levels		–3	0	+3	mV
V_{hys}	comparator input hysteresis		–	75	–	µV
MOT1, MOT2 and MOT3						
V_{DO}	drop-out output voltage	I_O = 100 mA	–	0.90	1.05	V
		I_O = 1000 mA	–	1.65	1.85	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = –100 mA	–	–	180	mV
I_{LIM}	current limiting	V_{VMOT} = 10 V; R_O = 1.2 Ω	1.6	1.9	2.3	A
V_{DHF}	diode forward voltage (diode D_H)	I_O = –500 mA; notes 4 and 5; see Fig.1	–	–	1.5	V
V_{DLF}	diode forward voltage (diode D_L)	I_O = 500 mA; notes 4 and 5; see Fig.1	–1.5	–	–	V
I_{DM}	peak diode current	note 5	–	–	2.3	A
+AMP IN and –AMP IN						
V_I	input voltage		–0.3	–	V_P – 1.7	V
	differential mode voltage without 'latch-up'		–	–	±V_P	V
I_b	input bias current		–	–	650	nA
C_I	input capacitance		–	4	–	pF
V_{offset}	input offset voltage		–	–	10	mV

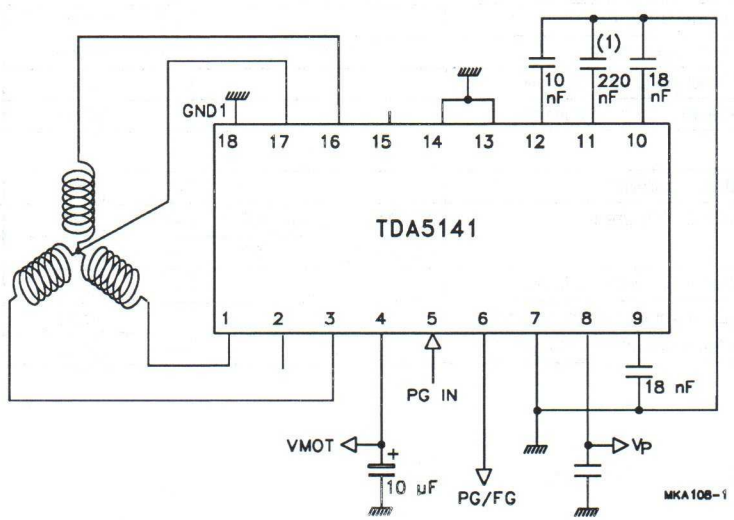
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AMP OUT (open collector)						
I_{sink}	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_O	output voltage		−0.5	–	+18	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	–	60	–	mA/μs
G_{tr}	transfer gain		0.3	–	–	S
PG IN						
V_I	input voltage		−0.3	–	V_P − 1.7	V
I_b	input bias current		–	–	650	nA
R_I	input resistance		5	–	30	kΩ
V_{CWS}	comparator switching level		86	–	107	mV
V_{hys}	comparator input hysteresis		–	±8	–	mV
PG/FG (open collector)						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
$V_{OH(max)}$	maximum HIGH level output voltage		V_P	–	–	V
t_{THL}	HIGH-to-LOW transition time	C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	μs
	ratio of PG/FG frequency and commutation frequency		–	1 : 2	–	
δ	duty factor		–	50	–	%
t_{PL}	pulse width LOW	after a PG IN pulse	5	7	30	μs
CAP-ST						
I_{sink}	output sink current		1.5	2.0	2.5	μA
I_{source}	output source current		−2.5	−2.0	−1.5	μA
V_{SWL}	LOW level switching voltage		–	0.20	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-TI						
I_{sink}	output sink current		–	28	–	μA
I_{source}	output source current	0.05 V < V_{CAP-TI} < 0.3 V	–	−57	–	μA
		0.3 V < V_{CAP-TI} < 2.2 V	–	−5	–	μA
V_{SWL}	LOW level switching voltage		–	50	–	mV
V_{SWM}	MIDDLE level switching voltage		–	0.30	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CAP-CD						
I_{sink}	output sink current		10.6	16.2	22	µA
I_{source}	output source current		−5.3	−8.1	−11	µA
I_{sink}/I_{source}	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage		850	875	900	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V
CAP-DC						
I_{sink}	output sink current		10.1	15.5	20.9	µA
I_{source}	output source current		−20.9	−15.5	−10.1	µA
I_{sink}/I_{source}	ratio of sink to source current		0.9	1.025	1.15	
V_{IL}	LOW level input voltage		850	875	900	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P; I_O = 0 mA.
3. Switching levels with respect to MOT1, MOT2 and MOT3.
4. Drivers are in the high-impedance OFF-state.
5. The outputs are short-circuit protected by limiting the current and the IC temperature.

APPLICATION INFORMATION



(1) Value selected for 3 Hz start-up oscillator frequency.

Fig.8 Application diagram without use of the operational transconductance amplifier (OTA).

Introduction (see Fig.9)

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing (H) and one sinking (L). The third output presents a high impedance (Z) to the motor, which enables measurement of the motor back-EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator. In Table 1 the sequence of the six possible states of the outputs has been depicted.

Table 1 Output states.

STATE	MOT1[1]	MOT2[1]	MOT3[1]
1	Z	L	H
2	H	L	Z
3	H	Z	L
4	Z	H	L
5	L	H	Z
6	L	Z	H

Note

1. H = HIGH state;
   L = LOW state;
   Z = high impedance OFF-state.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

The detected zero-crossings are used to provide speed information. The information has been made available on the PG/FG output pin. This is an open collector output and provides an output signal with a frequency that is half the commutation frequency. A VCR scanner also requires a PG phase sensor. This circuit has an interface for a simple pick-up coil. A multiplexer circuit is also provided to combine the FG and PG signals in time.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5141 also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5141 is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patented), possibility of using a pick-up coil without bias current.

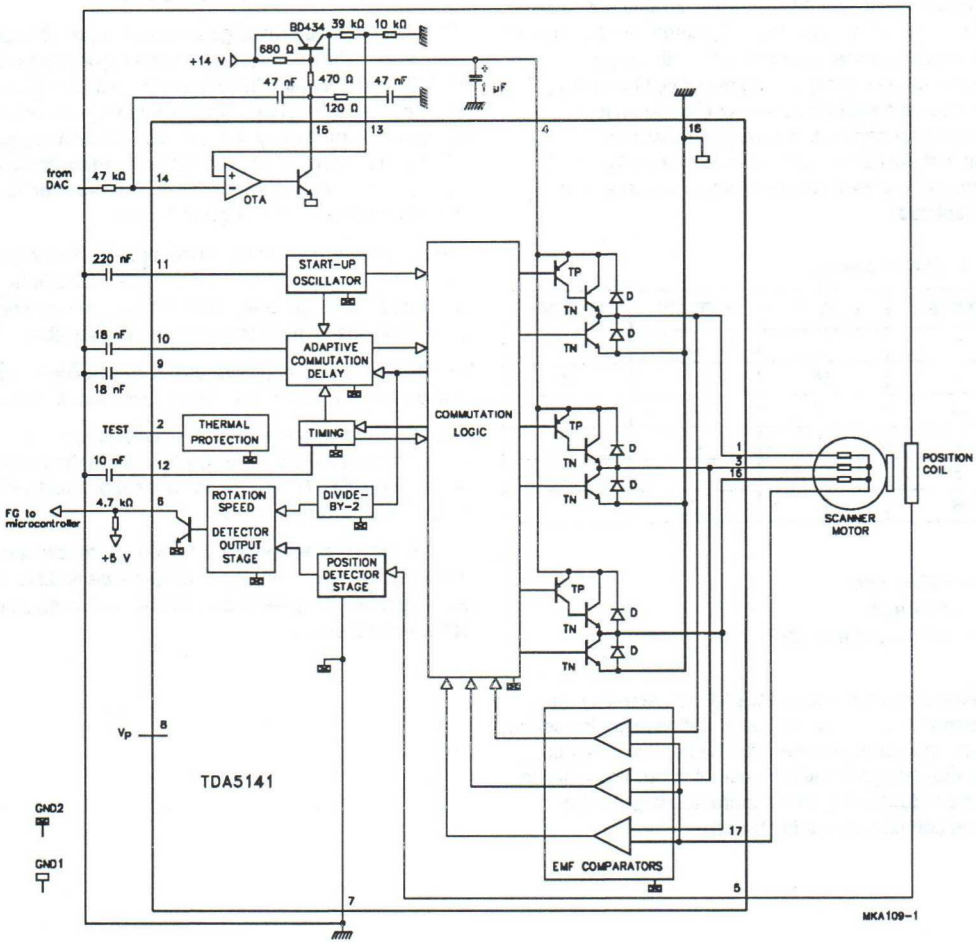


Fig.9 Typical application of the TDA5141 as a scanner driver, with use of OTA.

Adjustments

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator.
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor.
- The timing capacitor; this provides the system with its timing signals.

THE START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:
t_{start} = (2.15 × C) s (with C in μF).

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5141 will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$$f_{osc} = \frac{1}{2\pi\sqrt{\frac{K_t \times I \times p}{J}}}$$

where:

K_t = torque constant (N.m/A)

I = current (A)

p = number of magnetic pole-pairs

J = inertia J (kg.m^2)

Example: J = 72 × 10^{-6} kg.m^2, K = 25 × 10^{-3} N.m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF (choose 220 nF).

THE ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 μA and the discharging current 16.2 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}:

$$C = \frac{8.1 \times 10^{-6}}{f \times 1.3} = \frac{6231}{f_{C1}} \text{ (C in nF)}$$

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 16.2 μA;
maximum delay = (0.076 × C) ms (with C in nF).

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz; so:

$$\text{CAP-CD} = \frac{6231}{400} = 15.6 \text{ (choose 18 nF)}$$

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 15.5 μA. The same value can be chosen as for CAP-CD. Figure 10 illustrates typical voltage waveforms.

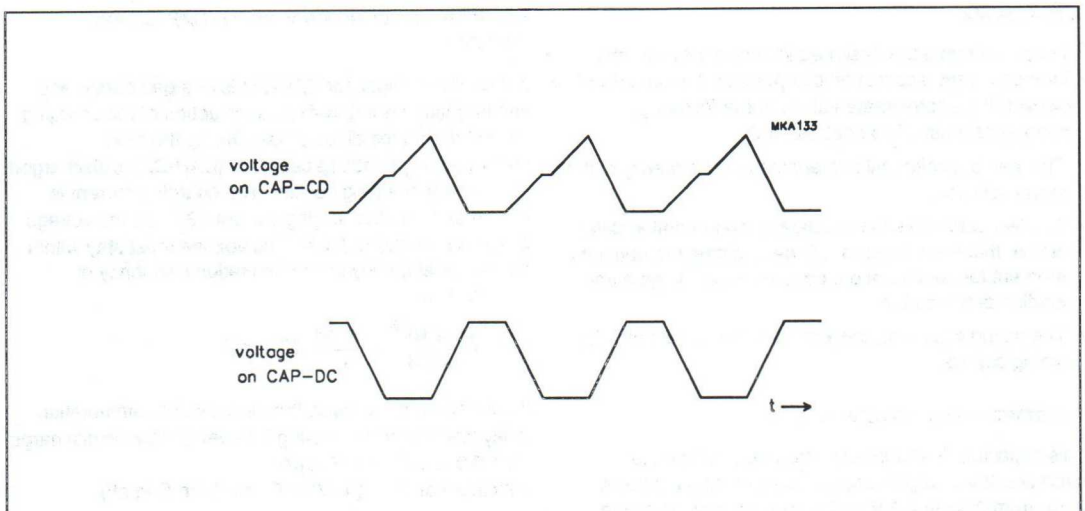


Fig.10 CAP-CD and CAP-DC typical voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).

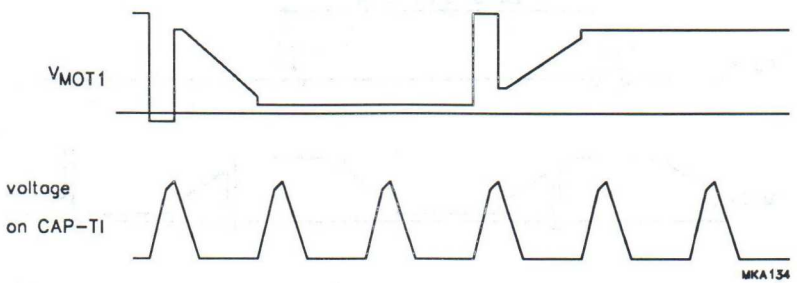
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 μA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 μA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 μA. The watchdog time is the time taken to charge the capacitor, with a current of 5 μA, from 0.3 to 2.2 V.

To ensure that the internal delays are covered CAP-TI must have a minimum value of 2 nF. For the watchdog function a value for CAP-TI of 10 nF is recommended.

To ensure a good start-up and commutation, care must be taken that no oscillations occur at the trailing edge of the flyback pulse. Snubber networks at the outputs should be critically damped.

Typical voltage waveforms are illustrated by Fig.11.



If the chosen value of CAP-TI is too small oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

Fig.11 Typical CAP-TI and V_{MOT1} voltage waveforms in normal running mode.

Other design aspects

There are other design aspects concerning the application of the TDA5141 besides the commutation function. They are:

- Generation of the tacho signal FG
- A built-in interface for a PG sensor
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Reliability.

FG SIGNAL

The FG signal is generated in the TDA5141 by using the zero-crossing of the motor EMF from the three motor windings. Every zero-crossing in a (star connected) motor winding is used to toggle the FG output signal. The FG frequency is therefore half the commutation frequency. All transitions indicate the detection of a zero-crossing (except for PG). The negative-going edges are called FG pulses because they generate an interrupt in a controlling microcontroller.

The accuracy of the FG output signal (jitter) is very good. This accuracy depends on the symmetry of the motor's electromagnetic construction, which also effects the satisfactory functioning of the motor itself.

Example: A 3-phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 × 6 × 6 = 900 Hz, and generates a tacho signal of 450 Hz.

PG SIGNAL

The accuracy of the PG signal in applications such as VCR must be high (phase information). This accuracy is obtained by combining the accurate FG signal with the PG signal by using a wide tolerance external PG sensor. The external PG signal (PG IN) is only used as an indicator to select a particular FG pulse. This pulse differs from the other FG pulses in that it has a short LOW-time of 18 µs after a HIGH-to-LOW transition. All other FG pulses have a 50% duty factor (see Fig.12).

For more information also see application note *"EIE/AN 93014"*.

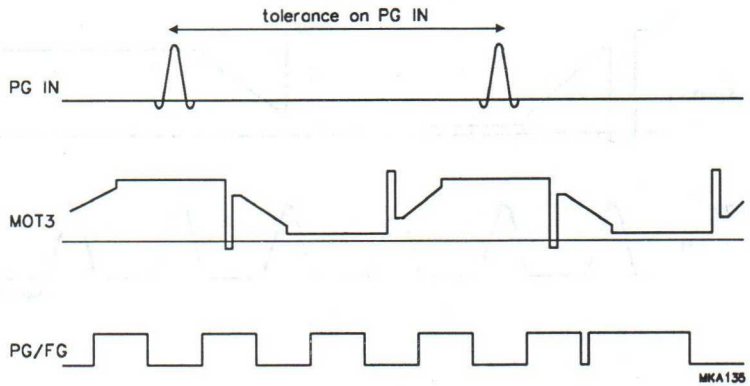


Fig.12 Timing and the FG and PG IN signals.

The special PG pulse is derived from the negative-going zero-crossing from the MOT3 output. The external PG signal (PG IN) must sense a positive-going voltage (>80 mV) within 1.5 to 7.5 commutation periods before the negative-going zero-crossing in MOT3 (see Fig.12).

The voltage requirements of the PG IN input are such that an inexpensive pick-up coil can be used as a sensor (see Fig.13).

Example: If p = 6, then one revolution contains 6 × 6 = 36 commutations. The tolerance is 6 periods, that is 60 degrees (mechanically) or 6.67 ms at 1500 rpm.

If a PG sensor is not used, the PG IN input must be grounded, this will result in a 50% duty factor FG signal.

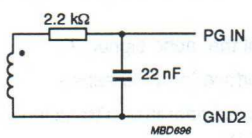


Fig.13 Pick-up coil as PG sensor.

THE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier. The common mode input range includes ground (GND) and rises to V_P – 1.7 V. The high sink current enables the OTA to drive a power transistor directly in an analog control amplifier.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (AMP OUT) to the positive supply, a positive-going voltage is found when the non-inverting input (+AMP IN) is positive with respect to the inverting input (–AMP IN). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

MOTOR CONTROL

DC motors can be controlled in an analog manner using the OTA.

For the control an external transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.9).

RELIABILITY

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+15%). This means that the current to and from the output stages is limited.
- Thermal protection of the six output transistors is achieved by each transistor having a thermal sensor that is active when the transistor is switched on. The transistors are switched off when the local temperature becomes too high.

It is possible, that when braking, the motor voltage (via the flyback diodes and the impedance on VMOT) may cause higher currents than allowed (>0.6 A). These currents must be limited externally.

Brushless DC motor drive circuit TDA5142T

FEATURES

- Full-wave commutation without position sensors
- Built-in start-up circuitry
- Six outputs that can drive three external transistor pairs:
  - output current 0.2 A (typ.)
  - low saturation voltage
  - built-in current limiter
- Thermal protection
- Tacho output without extra sensor
- Transconductance amplifier for an external control transistor
- Motor brake facility.

APPLICATIONS

- High-power applications e.g.:
  - high-end hard disk drives
  - automotive.

GENERAL DESCRIPTION

The TDA5142T is a bipolar integrated circuit used to drive 3-phase brushless DC motors in full-wave mode. The device is sensorless (saving of 3 hall-sensors) using the back-EMF sensing technique to sense the rotor position. It includes a brake function and 6 pre-drivers able to control FETs or bipolar external transistors. It is ideally suited for high-power applications such as high-end hard disk drives, automotive and other applications.

QUICK REFERENCE DATA

Measured over full voltage and temperature range.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	note 1	4	–	18	V
V_{VMOT}	input voltage to the output driver stages		3	–	18	V
V_O	driver output voltage	I_O = 100 mA; lower transistor	–	–	0.35	V
		I_O = 100 mA; upper transistor	1.05	–	–	V
I_{LIM}	current limiting	V_{VMOT} = 14.5 V; R_O = 47 Ω	150	200	250	mA

Note

1. An unstabilized supply can be used.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5142T	24	SOL	plastic	SOT137-1

BLOCK DIAGRAM

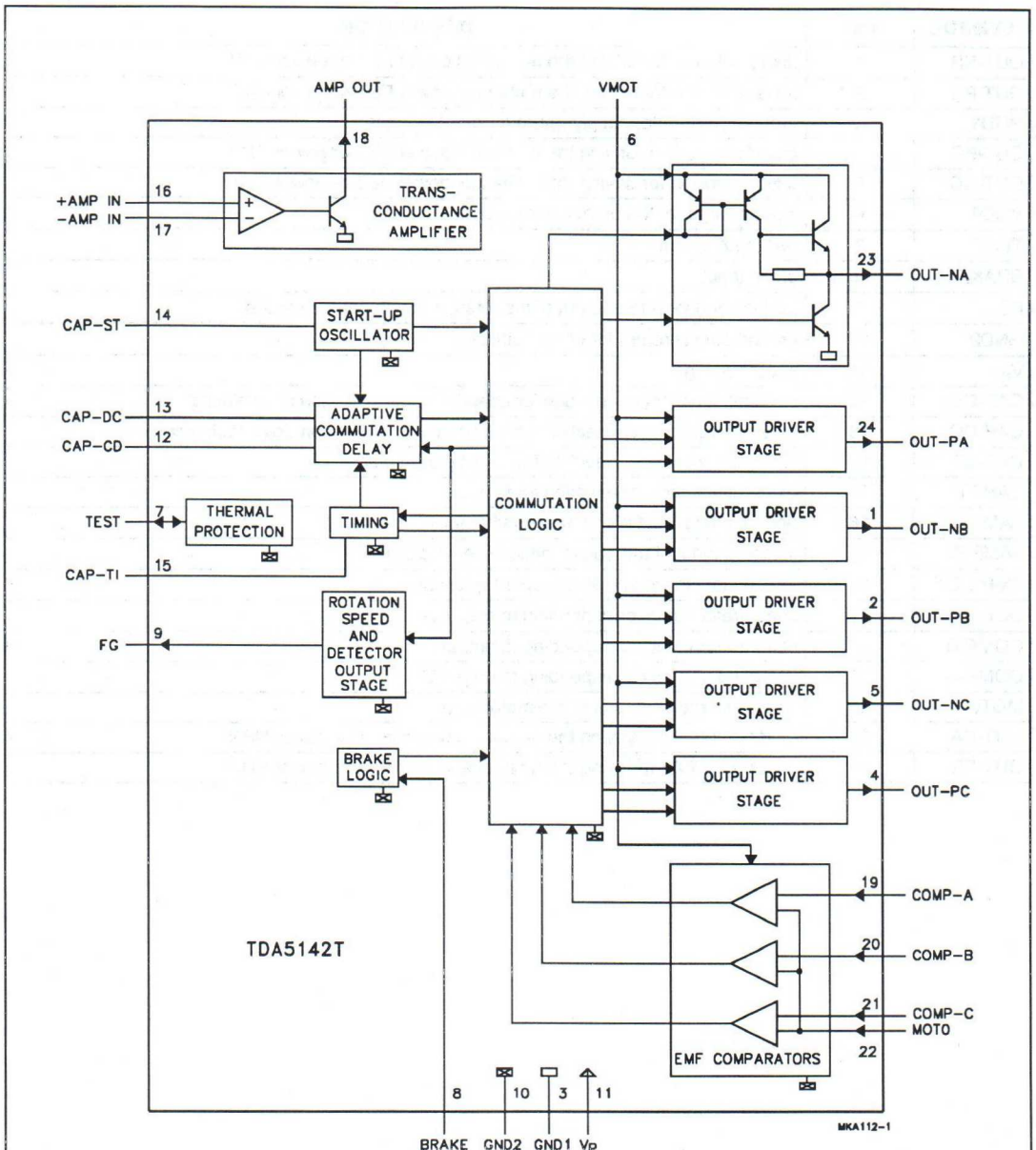


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUT-NB	1	driver output B for driving the n-channel power FET or power NPN
OUT-PB	2	driver output B for driving the n-channel power FET or power PNP
GND1	3	ground (0 V) motor supply return for output stages
OUT-PC	4	driver output C for driving the n-channel power FET or power PNP
OUT-NC	5	driver output C for driving the n-channel power FET or power NPN
VMOT	6	input voltage for the output driver stages
TEST	7	test input/output
BRAKE	8	brake input
FG	9	frequency generator: output of the rotation speed detector stage
GND2	10	ground supply return for control circuits
V_P	11	supply voltage
CAP-CD	12	external capacitor connection for adaptive communication delay timing
CAP-DC	13	external capacitor connection for adaptive communication delay timing copy
CAP-ST	14	external capacitor connection for start-up oscillator
CAP-TI	15	external capacitor connection for timing
+AMP IN	16	non-inverting input of the transconductance amplifier
–AMP IN	17	inverting input of the transconductance amplifier
AMP OUT	18	transconductance amplifier output (open collector)
COMP-A	19	comparator input corresponding to output A
COMP-B	20	comparator input corresponding to output B
COMP-C	21	comparator input corresponding to output C
MOT0	22	input from the star point of the motor coils
OUT-NA	23	driver output A for driving the n-channel power FET or power NPN
OUT-PA	24	driver output A for driving the n-channel power FET or power PNP

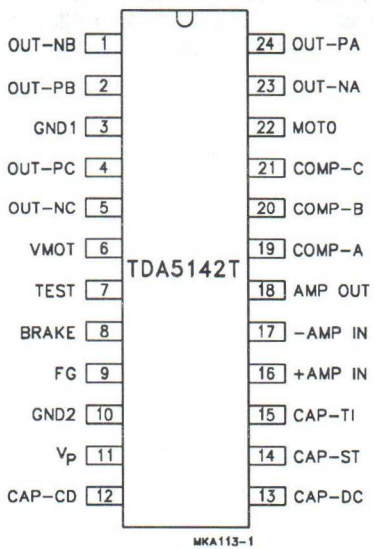


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA5142T offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5142T offers protected outputs capable of driving external power FETs or bipolar power transistors. It can easily be adapted for different motors and applications. The TDA5142T offers the following features:

- Sensorless commutation by using the motor EMF.
- Built-in start-up circuit.
- Optimum commutation, independent of motor type or motor loading.
- Six output drivers.
- Maximum output current 0.25 A.
- Outputs protected by current limiting and thermal protection.
- Low current consumption.
- Accurate frequency generator (FG) by using the motor EMF.
- Brake function.
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier or as a level shifter in a Switched Mode Power Supply (SMPS) drive.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		4	18	V
V_I	input voltage; all pins except VMOT	$V_I < 18$ V	–0.3	$V_P + 0.5$	V
V_{VMOT}	VMOT input voltage		3	18	V
V_O	output voltage				
	FG		GND	V_P	V
	AMP OUT		–	18	V
	OUT-NA, OUT-NB and OUT-NC		–	$V_{VMOT} - 0.9$	V
	OUT-PA, OUT-PB and OUT-PC		0.2	–	V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC		–	2.5	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
P_{tot}	total power dissipation	see Fig.3	–	–	W
V_{es}	electrostatic handling	see Chapter "Handling"	–	500	V

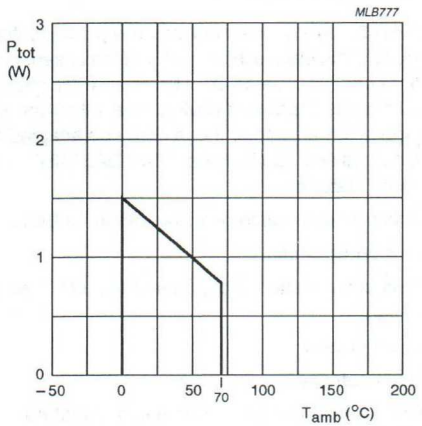


Fig.3 Power derating curve.

HANDLING

Every pin withstands the ESD test according to *"MIL-STD-883C class 2"*. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulses − on each pin referenced to ground.

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	4	–	18	V
I_P	supply current	note 2	–	5.2	6.25	mA
V_{VMOT}	input voltage to the output driver stages	see Fig.1	3	–	18	V
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} − 30	–	K
COMP-A, COMP-B, COMP-C and MOT0						
V_I	input voltage		−0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} − 1.5 V	−10	–	0	μA
V_{CSW}	comparator switching level	note 3	±20	±25	±30	mV
ΔV_{CSW}	variation in comparator switching levels		−3	0	+3	mV
V_{hys}	comparator input hysteresis		–	75	–	μV

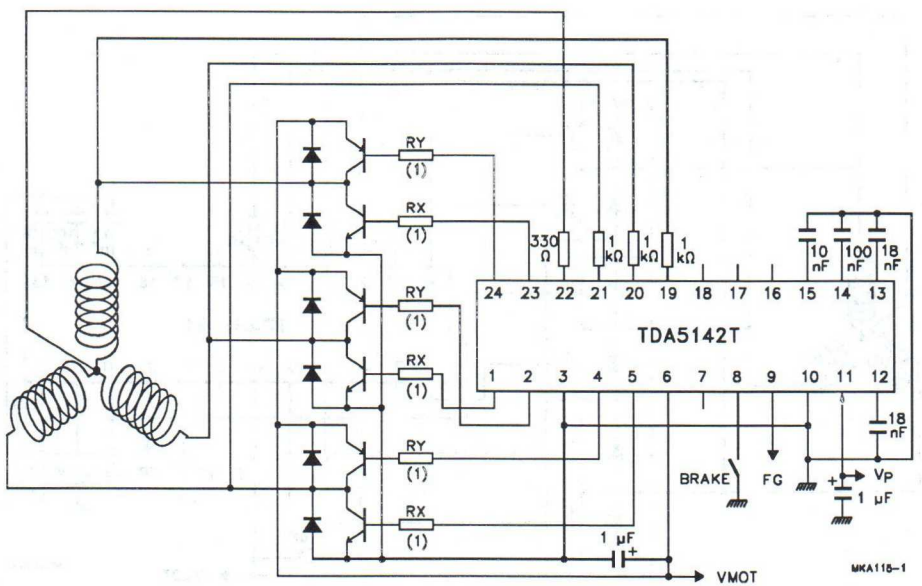
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OUT-NA, OUT-NB, OUT-NC, OUT-PA, OUT-PB and OUT-PC						
V_{O-n}	n-channel driver output voltage	upper transistor; I_O = −100 mA	−1.05	–	–	V
		lower transistor; I_O = 10 mA	–	–	0.35	V
V_{O-p}	p-channel driver output voltage	upper transistor; I_O = −10 mA	−1.05	–	–	V
		lower transistor; I_O = 100 mA	–	–	0.35	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = −100 mA	–	–	180	mV
I_{LIM}	current limiting	V_{VMOT} = 14.5 V; R_O = 47 Ω	150	200	250	mA
+AMP IN and −AMP IN						
V_I	input voltage		−0.3	–	V_P − 1.7	V
	differential mode voltage without 'latch-up'		–	–	$\pm V_P$	V
I_b	input bias current		–	–	650	nA
C_I	input capacitance		–	4	–	pF
V_{offset}	input offset voltage		–	–	10	mV
AMP OUT (open collector)						
I_{sink}	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_O	output voltage		−0.5	–	+18	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	40	–	–	mA/μs
G_{tr}	transfer gain		0.3	–	–	S
BRAKE						
V_{BM}	brake-mode voltage	enable brake mode; 4 V < V_P < 18 V		–	2.3	V
		normal mode; 4 V < V_P < 18 V	2.7	–		V
I_I	input current	brake mode	–	−20	−30	μA
		normal mode	–	0	20	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FG (push-pull)						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = –60 μA		V_P – 0.3	–	V
t_{THL}	HIGH-to-LOW transition time	C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	μs
	ratio of FG frequency and commutation frequency		–	1	–	
CAP-ST						
I_{sink}	output sink current		1.5	2.0	2.5	μA
I_{source}	output source current		–2.5	–2.0	–1.5	μA
V_{SWL}	LOW level switching voltage		–	0.20	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-TI						
I_{sink}	output sink current		–	28	–	μA
I_{source}	output source current	0.2 V < V_{CAP-TI} < 0.3 V	–	–57	–	μA
		0.3 V < V_{CAP-TI} < 2.2 V	–	–5	–	μA
V_{SWL}	LOW level switching voltage		–	50	–	mV
V_{SWM}	MIDDLE level switching voltage		–	0.30	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-CD						
I_{sink}	output sink current		10.6	16.2	22	μA
I_{source}	output source current		–5.3	–8.1	–11	μA
I_{sink}/I_{source}	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage		850	875	900	mV
V_{IH}	HIGH level input voltage		2.3	–	2.5	V
CAP-DC						
I_{sink}	output sink current		10.1	15.5	20.9	μA
I_{source}	output source current		–20.9	–15.5	–10.1	μA
I_{sink}/I_{source}	ratio of sink to source current		0.9	1.025	1.15	
V_{IL}	LOW level input voltage		850	875	900	mV
V_{IH}	HIGH level input voltage		2.3	–	2.5	V

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P; I_O = 0 mA.
3. Switching levels with respect to driver outputs OUT-NA, OUT-NB, OUT-NC, OUT-PA, OUT-PB and OUT-PC.

APPLICATION INFORMATION



(1) RX = RY > 8 (VMOT − 1.5)

Fig.4 Application diagram without use of the operational transconductance amplifier (OTA) with bipolar power transistors.

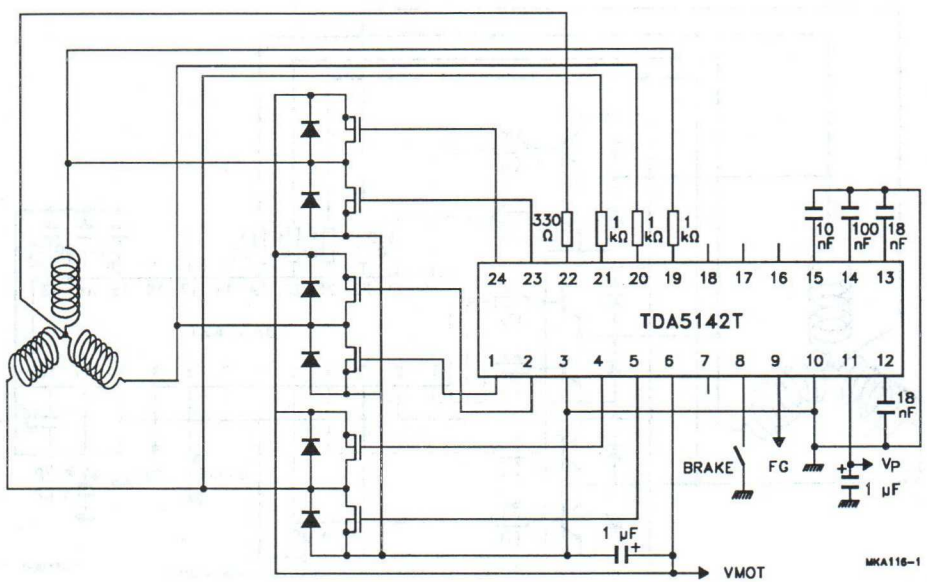


Fig.5 Application diagram without use of the operational transconductance amplifier (OTA) with MOSFETs.

Introduction (see Fig.6)

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing (H) and one sinking (L). The third output presents a high impedance (Z) to the motor, which enables measurement of the motor back-EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator. In Table 1 the sequence of the six possible states of the external connected output transistors has been depicted and the corresponding output levels on the NA, PA, NB, PB, NC and PC outputs of the TDA5142T.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

The output stages are also protected by a current limiting circuit and by thermal protection.

The detected zero-crossings are used to provide speed information. The information has been made available on the FG output pin. This output provides an output signal with a frequency equal to the commutation frequency.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5142T also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5142T is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patented).

Adjustments

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator.
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor.
- The timing capacitor; this provides the system with its timing signals.

THE START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:
$t_{start} = (2.15 \times C)$ s (with C in μF)

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor).

Table 1 Output states.

STATE	MOT1[1]	OUT-NA[1]	OUT-PA[1]	MOT2[1]	OUT-NB[1]	OUT-PB[1]	MOT3[1]	OUT-NC[1]	OUT-PC[1]
1	Z	L	H	L	H	H	H	L	L
2	H	L	L	L	H	H	Z	L	H
3	H	L	L	Z	L	H	L	H	H
4	Z	L	H	H	L	L	L	H	H
5	L	H	H	H	L	L	Z	L	H
6	L	H	H	Z	L	H	H	L	L

Note

1. H = HIGH state; L = LOW state; Z = high-impedance OFF-state.

If the movement of the motor generates enough EMF the TDA5142T will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$$f_{osc} = \frac{1}{2\pi\sqrt{\frac{K_t \times I \times p}{J}}}$$

where:

K_t = torque constant (N.m/A)

I = current (A)

p = number of magnetic pole-pairs

J = inertia J ($kg.m^2$).

Example: $J = 72 \times 10^{-6}$ $kg.m^2$, $K = 25 \times 10^{-3}$ N.m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF (choose 220 nF).

THE ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 μA and the discharging current 16.2 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}:

$$C = \frac{8.1 \times 10^{-6}}{f \times 1.3} = \frac{6231}{f_{C1}} \text{ (C in nF)}$$

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 20 μA;
maximum delay = (0.076 × C) ms (with C in nF)

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz; so:

$$\text{CAP-CD} = \frac{6231}{400} = 15.6 \text{ (choose 18 nF)}$$

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 15.5 μA. The same value can be chosen as for CAP-CD. Figure 7 illustrates typical voltage waveforms.

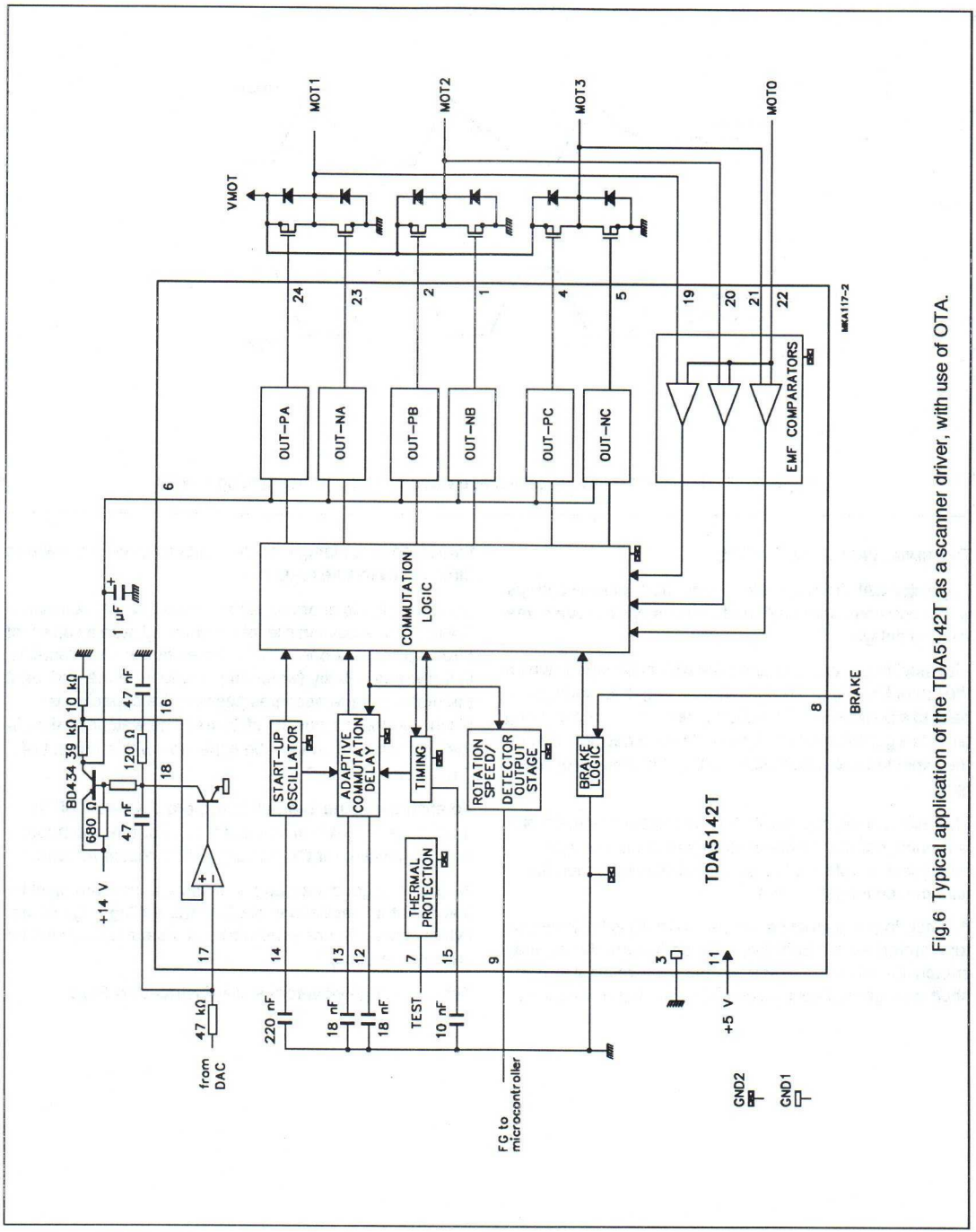


Fig.6 Typical application of the TDA5142T as a scanner driver, with use of OTA.

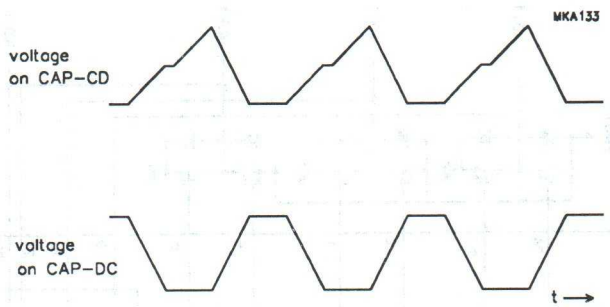


Fig.7 CAP-CD and CAP-DC typical voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).

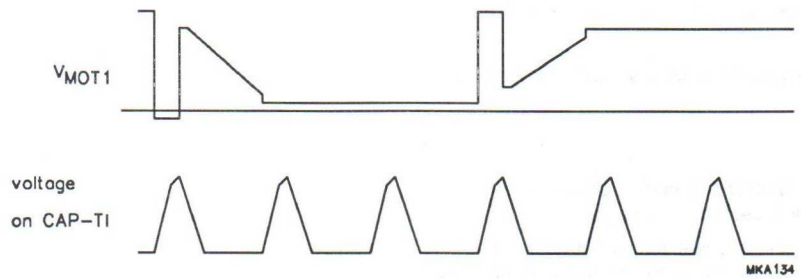
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 μA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 μA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 μA. The watchdog time is the time taken to charge the capacitor, with a current of 5 μA, from 0.3 to 2.2 V.

To ensure that the internal delays are covered CAP-TI must have a minimum value of 2 nF. For the watchdog function a value for CAP-TI of 10 nF is recommended.

To ensure a good start-up and commutation, care must be taken that no oscillations occur at the trailing edge of the flyback pulse. Snubber networks at the outputs should be critically damped.

Typical voltage waveforms are illustrated by Fig.8.



If the chosen value of CAP-TI is too small oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

Fig.8 Typical CAP-TI and V_{MOT1} voltage waveforms in normal running mode.

Other design aspects

There are other design aspects concerning the application of the TDA5142T besides the commutation function. They are:

- Generation of the tacho signal FG
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Brake function
- Reliability.

FG SIGNAL

The FG signal is generated in the TDA5142T by using the zero-crossing of the motor EMF from the three motor windings and the commutation signal.

Output FG switches from HIGH-to-LOW on all zero crossings and from LOW-to-HIGH on all commutations. Output FG can source typically 75 μA and sink more than 3 mA.

Example: a 3-phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 × 6 × 6 = 900 Hz, and generates a tacho signal of 900 Hz.

THE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier. The common mode input range includes ground (GND) and rises to V_P – 1.7 V. The high sink current enables the OTA to drive a power transistor directly in an analog control amplifier.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (AMP OUT) to the positive supply, a positive-going voltage is found when the non-inverting input (+AMP IN) is positive with respect to the inverting input (–AMP IN). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

MOTOR CONTROL

DC motors can be controlled in an analog manner using the OTA.

For the analog control an external transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.6).

BRAKE FUNCTION

- If the voltage on pin 8 is <2.3 V the motor brakes; in this condition the external outputs are driven to a HIGH voltage level.
- If pin 8 is floating or the voltage is >2.7 V the motor runs normally.

RELIABILITY

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+15%). This means that the current to and from the output stages is limited.
- Thermal protection of the six output transistors is achieved in such a way that the transistors are switched off when the local temperature becomes too high.

Brushless DC motor drive circuit — TDA5143T

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - output current 0.85 A (typ.)
  - low saturation voltage
  - built-in current limiter
  - soft-switching outputs for low Electromagnetic Interference (EMI)
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Transconductance amplifier for an external control transistor.

APPLICATIONS

- General purpose spindle driver (e.g. for hard disk)
- Laser beam printer.

GENERAL DESCRIPTION

The TDA5143T is a bipolar integrated circuit used to drive 3-phase brushless DC motors in full-wave mode. The device is sensorless (saving of 3 hall-sensors) using the back-EMF sensing technique to sense the rotor position. A special circuit is built-in to reduce the EMI (soft switching output stages). It is ideally suited as a drive circuit for hard disk drive spindle motor as well as other applications (e.g. laser beam printer).

QUICK REFERENCE DATA

Measured over full voltage and temperature range.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	note 1	4	–	18	V
V_{VMOT}	input voltage to the output driver stages	note 2	1.7	–	16	V
V_{DO}	drop-out output voltage	I_O = 100 mA	–	0.93	1.05	V
I_{LIM}	current limiting	V_{VMOT} = 10 V; R_O = 5.9 Ω	0.7	0.85	1.0	A

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN = –AMP IN = 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5143T	20	SOL	plastic	SOT163-1

BLOCK DIAGRAM

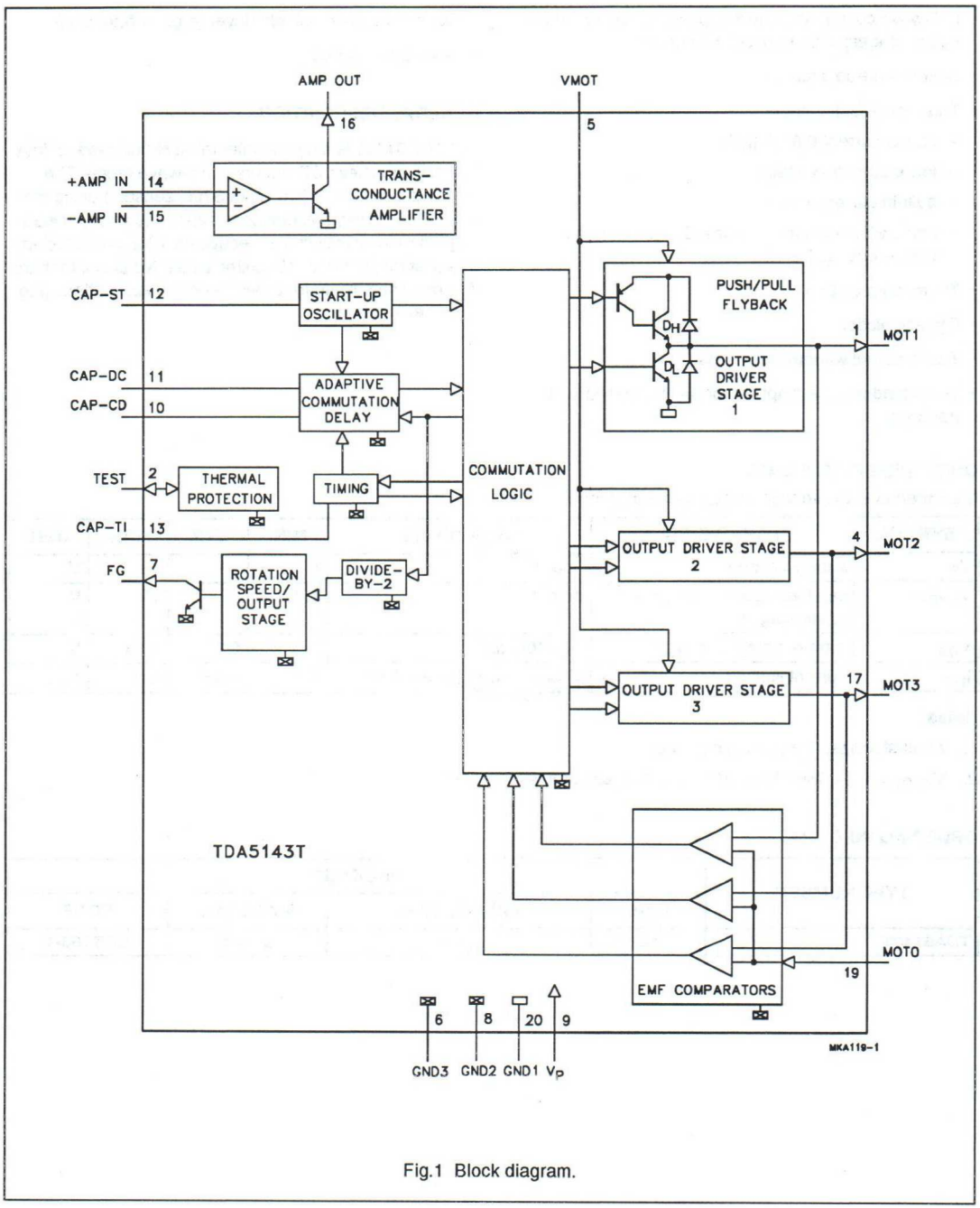


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
MOT1	1	driver output 1
TEST	2	test input/output
n.c.	3	not connected
MOT2	4	driver output 2
VMOT	5	input voltage for the output driver stages
GND3	6	ground supply; must be connected
FG	7	frequency generator: output of the rotation speed (open collector digital output)
GND2	8	ground supply return for control circuits
V_P	9	supply voltage
CAP-CD	10	external capacitor connection for adaptive communication delay timing
CAP-DC	11	external capacitor connection for adaptive communication delay timing copy
CAP-ST	12	external capacitor connection for start-up oscillator
CAP-TI	13	external capacitor connection for timing
+AMP IN	14	non-inverting input of the transconductance amplifier
–AMP IN	15	inverting input of the transconductance amplifier
AMP OUT	16	transconductance amplifier output (open collector)
MOT3	17	driver output 3
n.c.	18	not connected
MOT0	19	input from the star point of the motor coils
GND1	20	ground (0 V) motor supply return for output stages

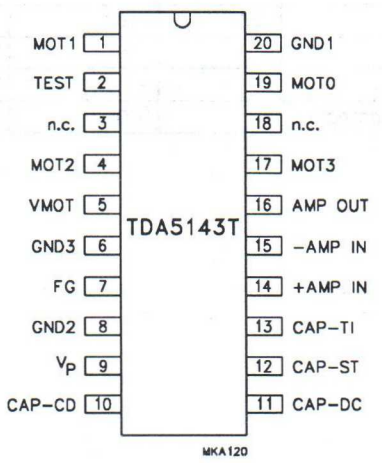


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA5143T offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5143T offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5143T offers the following features:

- Sensorless commutation by using the motor EMF.
- Built-in start-up circuit.
- Optimum commutation, independent of motor type or motor loading.
- Built-in flyback diodes.
- Three phase full-wave drive.
- High output current (0.85 A).
- Outputs protected by current limiting and thermal protection of each output transistor.
- Low current consumption by adaptive base-drive.
- Soft-switching pulse output for low radiation.
- Accurate frequency generator (FG) by using the motor EMF.
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	18	V
V_I	input voltage; all pins except VMOT	$V_I < 18$ V	–0.3	$V_P + 0.5$	V
V_{VMOT}	VMOT input voltage		–0.5	17	V
V_O	output voltage				
	AMP OUT and FG		GND	V_P	V
	MOT0, MOT1, MOT2 and MOT3		–1	$V_{VMOT} + V_{DHF}$	V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC		–	2.5	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
P_{tot}	total power dissipation	see Fig.3	–	–	W
V_{es}	electrostatic handling	see Chapter "Handling"	–	500	V

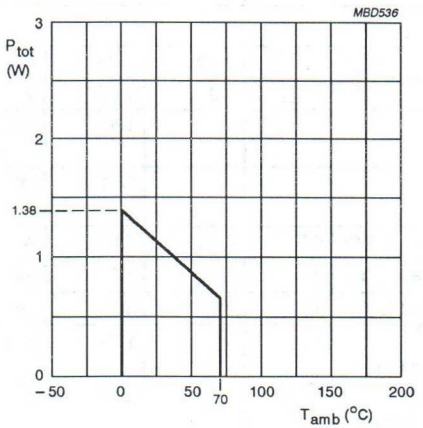


Fig.3 Power derating curve.

HANDLING

Every pin withstands the ESD test according to *"MIL-STD-883C class 2"*. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulses – on each pin referenced to ground.

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	4	–	18	V
I_P	supply current	note 2	–	4.4	5.5	mA
V_{VMOT}	input voltage to the output driver stages	see Fig.1	1.7	–	16	V
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} – 30	–	K
MOT0; centre tap						
V_I	input voltage		–0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} – 1.5 V	–10	–	0	μA
V_{CSW}	comparator switching level	note 3	±20	±30	±40	mV
ΔV_{CSW}	variation in comparator switching levels		–3	0	+3	mV
V_{hys}	comparator input hysteresis		–	75	–	μV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MOT1, MOT2 and MOT3						
V_{DO}	drop-out output voltage	I_O = 100 mA	–	0.93	1.05	V
		I_O = 500 mA	–	1.3	1.65	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = –100 mA	–	–	180	mV
I_{LIM}	current limiting	V_{VMOT} = 10 V; R_O = 5.9 Ω	0.7	0.85	1.0	A
t_r	rise time switching output	V_{VMOT} = 15 V; see Fig.4	7	12	17	µs
t_f	fall time switching output	V_{VMOT} = 15 V; see Fig.4	16	23	30	µs
V_{DHF}	diode forward voltage (diode D_H)	I_O = –500 mA; notes 4 and 5; see Fig.1	–	–	1.5	V
V_{DLF}	diode forward voltage (diode D_L)	I_O = 500 mA; notes 4 and 5; see Fig.1	–1.5	–	–	V
I_{DM}	peak diode current	note 5	–	–	1	A
+AMP IN and –AMP IN						
V_I	input voltage		–0.3	–	V_P – 1.7	V
	differential mode voltage without 'latch-up'		–	–	±V_P	V
I_b	input bias current		–	–	650	nA
C_I	input capacitance		–	4	–	pF
V_{offset}	input offset voltage		–	–	10	mV
AMP OUT (open collector)						
I_{sink}	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_O	output voltage		–0.5	–	+18	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	–	60	–	mA/µs
G_{tr}	transfer gain		0.3	–	–	S
FG (open collector)						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
$V_{OH(max)}$	maximum HIGH level output voltage		V_P	–	–	V
t_{THL}	HIGH-to-LOW transition time	C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	µs
	ratio of FG frequency and commutation frequency		–	1 : 2	–	
δ	duty factor		–	50	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CAP-ST						
I_{sink}	output sink current		1.5	2.0	2.5	µA
I_{source}	output source current		−2.5	−2.0	−1.5	µA
V_{SWL}	LOW level switching voltage		–	0.20	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-TI						
I_{sink}	output sink current		–	28	–	µA
I_{source}	output source current	$0.2\ V < V_{CAP-TI} < 0.3\ V$	–	−57	–	µA
		$0.3\ V < V_{CAP-TI} < 2.2\ V$	–	−5	–	µA
V_{SWL}	LOW level switching voltage		–	50	–	mV
V_{SWM}	MIDDLE level switching voltage		–	0.30	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-CD						
I_{sink}	output sink current		10.6	16.2	22	µA
I_{source}	output source current		−5.3	−8.1	−11	µA
I_{sink}/I_{source}	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage		850	875	900	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V
CAP-DC						
I_{sink}	output sink current		10.1	15.5	20.9	µA
I_{source}	output source current		−20.9	−15.5	−10.1	µA
I_{sink}/I_{source}	ratio of sink to source current		0.9	1.025	1.15	
V_{IL}	LOW level input voltage		850	875	900	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P; $i_O = 0$ mA.
3. Switching levels with respect to MOT1, MOT2 and MOT3.
4. Drivers are in the high-impedance OFF-state.
5. The outputs are short-circuit protected by limiting the current and the IC temperature.

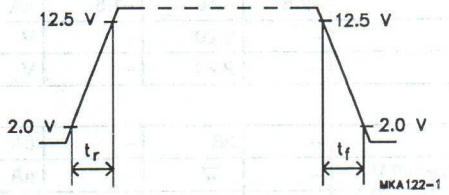
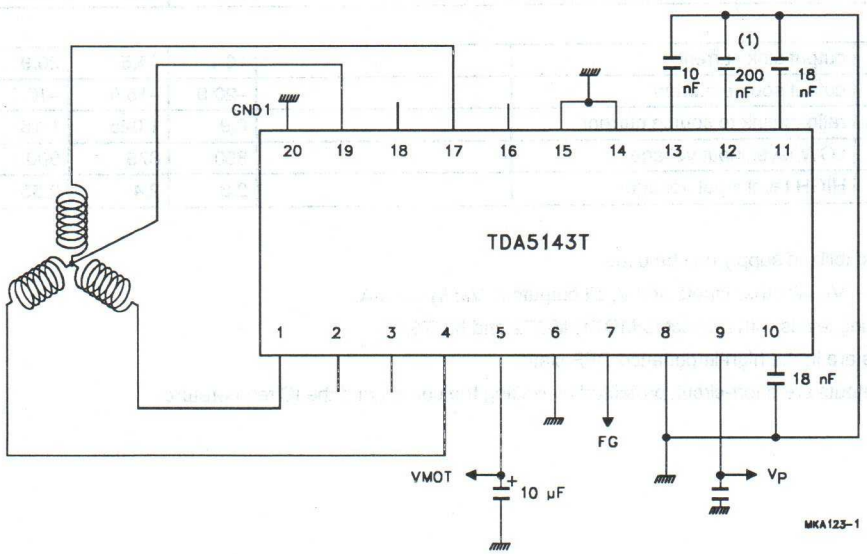


Fig.4 Output transition time measurement.

APPLICATION INFORMATION



(1) Value selected for 3 Hz start-up oscillator frequency.

Fig.5 Application diagram without use of the operational transconductance amplifier (OTA).

Introduction (see Fig.6)

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing (H) and one sinking (L). The third output presents a high impedance (Z) to the motor, which enables measurement of the motor back-EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator. In Table 1 the sequence of the six possible states of the outputs has been depicted.

Table 1 Output states.

STATE	MOT1[1]	MOT2[1]	MOT3[1]
1	Z	L	H
2	H	L	Z
3	H	Z	L
4	Z	H	L
5	L	H	Z
6	L	Z	H

Note

1. H = HIGH state;
   L = LOW state;
   Z = high-impedance OFF-state.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

The detected zero-crossings are used to provide speed information. The information has been made available on the FG output pin. This is an open collector output and provides an output signal with a frequency that is half the commutation frequency.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5143T also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5143T is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patented).

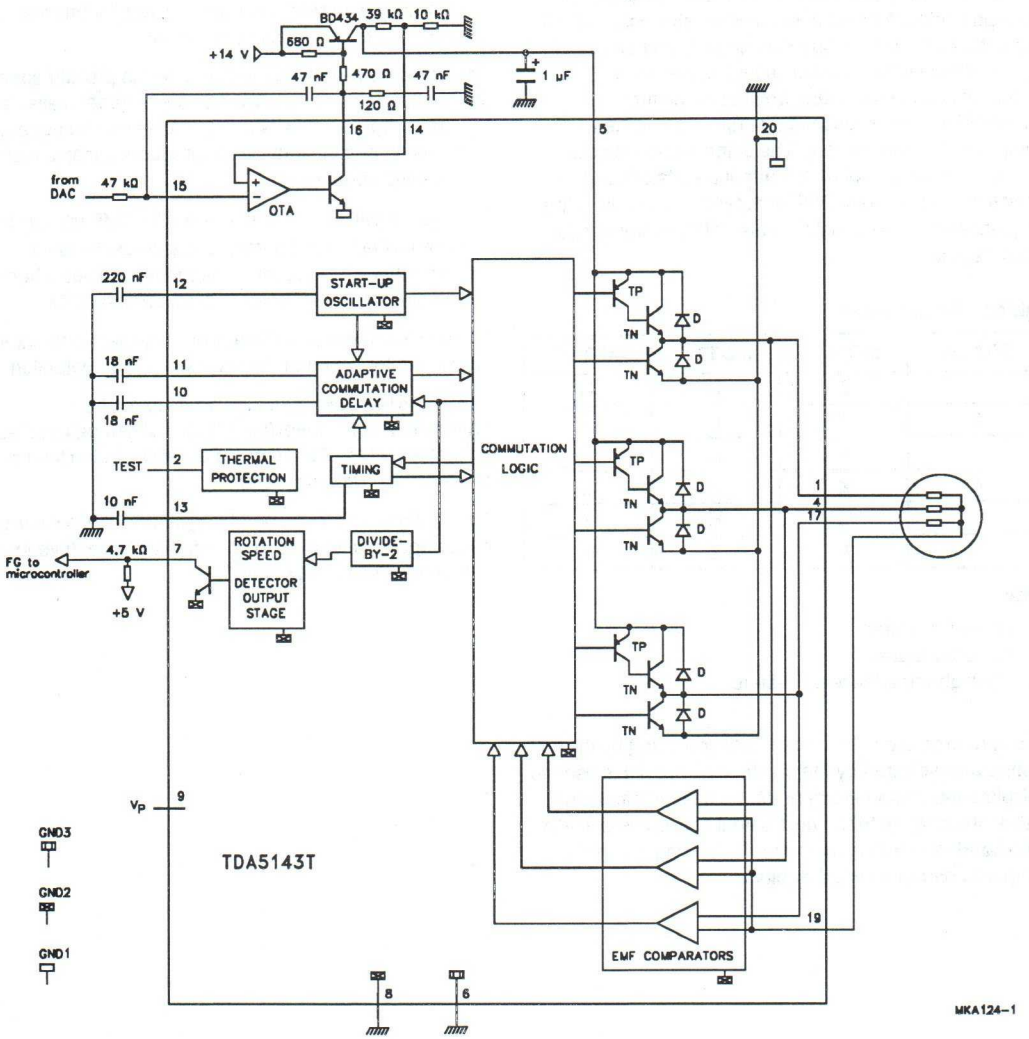


Fig.6 Typical application of the TDA5143T as a scanner driver, with use of OTA.

Adjustments

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator.
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor.
- The timing capacitor; this provides the system with its timing signals.

THE START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:
t_{start} = (2.15 × C) s (with C in μF)

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5143T will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$$f_{osc} = \frac{1}{2\pi\sqrt{\frac{K_t \times I \times p}{J}}}$$

where:

K_t = torque constant (N.m/A)

I = current (A)

p = number of magnetic pole-pairs

J = inertia J (kg.m^2)

Example: J = 72 × 10^{-6} kg.m^2, K = 25 × 10^{-3} N.m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF (choose 220 nF).

THE ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 μA and the discharging current 16.2 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}:

$$C = \frac{8.1 \times 10^{-6}}{f \times 1.3} = \frac{6231}{f_{C1}} \text{ (C in nF)}$$

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 16.2 μA;
maximum delay = (0.076 × C) ms (with C in nF)

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz; so:

$$\text{CAP-CD} = \frac{6231}{400} = 15.6 \text{ (choose 18 nF)}$$

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 15.5 μA. The same value can be chosen as for CAP-CD. Figure 7 illustrates typical voltage waveforms.

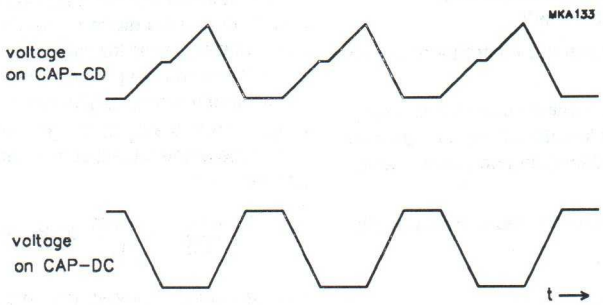


Fig.7 CAP-CD and CAP-DC typical voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).

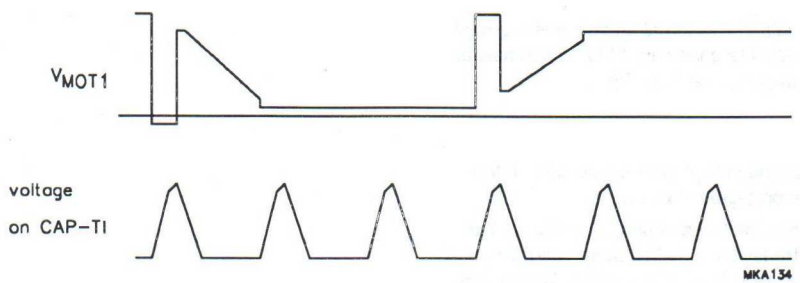
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 μA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 μA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 μA. The watchdog time is the time taken to charge the capacitor, with a current of 5 μA, from 0.3 to 2.2 V.

To ensure that the internal delays are covered CAP-TI must have a minimum value of 2 nF. For the watchdog function a value for CAP-TI of 10 nF is recommended.

To ensure a good start-up and commutation, care must be taken that no oscillations occur at the trailing edge of the flyback pulse. Snubber networks at the outputs should be critically damped.

Typical voltage waveforms are illustrated by Fig.8.



If the chosen value of CAP-TI is too small oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

Fig.8 Typical CAP-TI and V_{MOT1} voltage waveforms in normal running mode.

Other design aspects

There are other design aspects concerning the application of the TDA5143T besides the commutation function. They are:

- Generation of the tacho signal FG
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Reliability.

FG SIGNAL

The FG signal is generated in the TDA5143T by using the zero-crossing of the motor EMF from the three motor windings. Every zero-crossing in a (star connected) motor winding is used to toggle the FG output signal. The FG frequency is therefore half the commutation frequency. All transitions indicate the detection of a zero-crossing.

The accuracy of the FG output signal depends on the symmetry of the motor's electromagnetic construction, which also effects the satisfactory functioning of the motor itself.

Example: a 3-phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 x 6 x 6 = 900 Hz, and generates a tacho signal of 450 Hz.

THE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier. The common mode input range includes ground (GND) and rises to V_P – 1.7 V. The high sink current enables the OTA to drive a power transistor directly in an analog control amplifier.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (AMP OUT) to the positive supply, a positive-going voltage is found when the non-inverting input (+AMP IN) is positive with respect to the inverting input (–AMP IN). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

MOTOR CONTROL

DC motors can be controlled in an analog manner using the OTA.

For the analog control an external transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.6).

RELIABILITY

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+15%). This means that the current to and from the output stages is limited.
- Thermal protection of the six output transistors is achieved by each transistor having a thermal sensor that is active when the transistor is switched on. The transistors are switched off when the local temperature becomes too high.

It is possible, that when braking, the motor voltage (via the flyback diodes and the impedance on VMOT) may cause higher currents than allowed (>0.6 A). These currents must be limited externally.

Brushless DC motor drive circuit — TDA5144

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - output current 2.0 A (typ.)
  - low saturation voltage
  - built-in current limiter
  - soft-switching outputs for low Electromagnetic Interference (EMI)
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Transconductance amplifier for an external control transistor.

APPLICATIONS

- General purpose spindle driver (e.g. for hard disk)
- Laser beam printer.

GENERAL DESCRIPTION

The TDA5144 is a bipolar integrated circuit used to drive 3-phase brushless DC motors in full-wave mode. The device is sensorless (saving of 3 hall-sensors) using the back-EMF sensing technique to sense the rotor position. A special circuit is built-in to reduce the EMI (soft switching output stages). It is ideally suited as a drive circuit for hard disk drive spindle motor requiring powerful output stages (current limit of 2.0 A). It can also be used in e.g. laser beam printer and other applications.

QUICK REFERENCE DATA

Measured over full voltage and temperature range.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	note 1	4	–	18	V
V_{VMOT}	input voltage to the output driver stages	note 2	1.7	–	16	V
V_{DO}	drop-out output voltage	I_O = 100 mA	–	0.90	1.05	V
I_{LIM}	current limiting	V_{VMOT} = 10 V; R_O = 1.2 Ω	1.8	2.0	2.4	A

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN = –AMP IN = 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5144AT	20	SOL	plastic	SOT163-1
TDA5144T	28	SOL	plastic	SOT136-1

BLOCK DIAGRAM

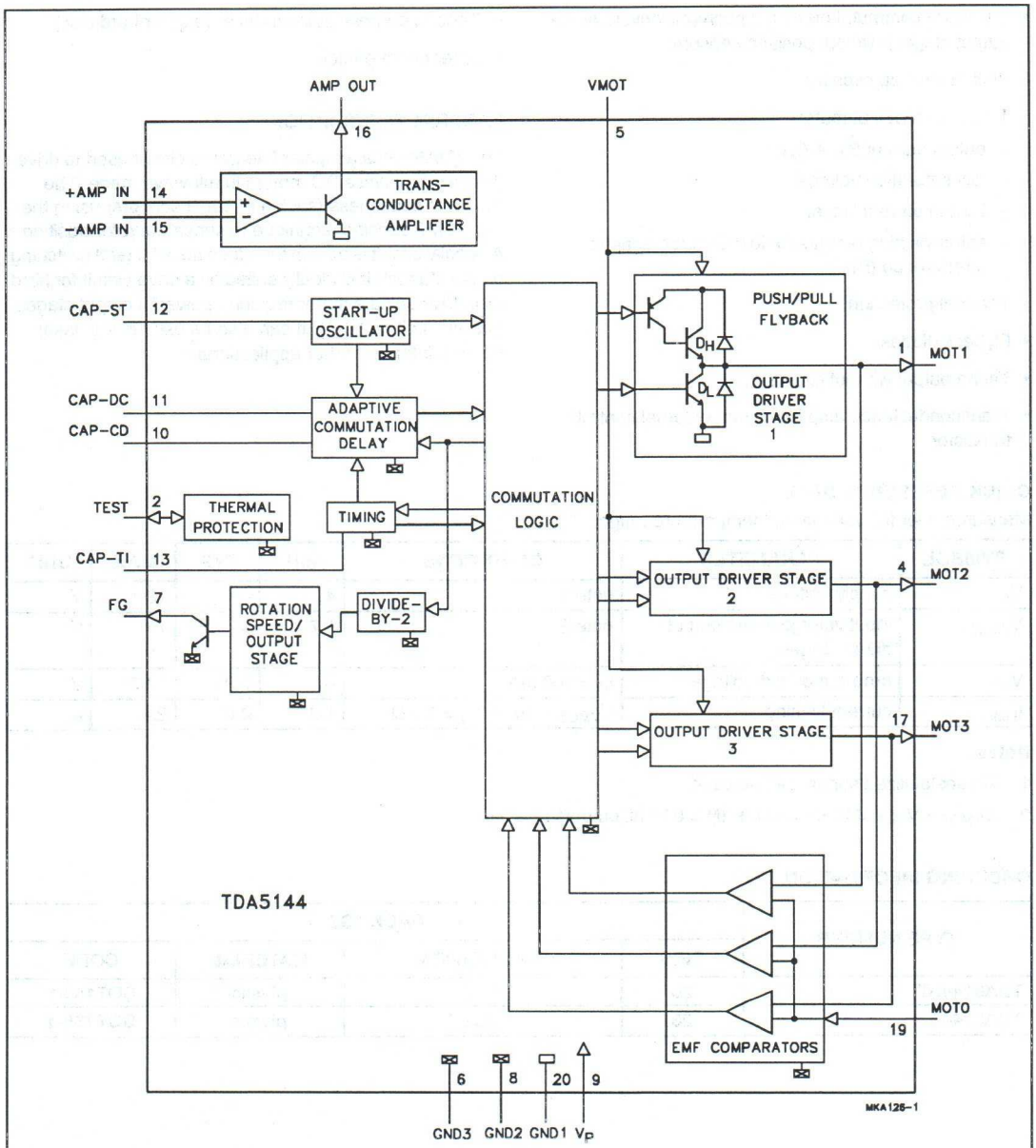


Fig.1 Block diagram (SOT163-1; SO20L).

PINNING

SYMBOL	PIN		DESCRIPTION
	SO20	SO28	
MOT1	1	1 and 2	driver output 1
TEST	2	3	test input/output
n.c.	3	4	not connected
MOT2	4	5 and 6	driver output 2
n.c.	–	7	not connected
VMOT	5	8 and 9	input voltage for the output driver stages
GND3	6	10	ground supply; must be connected
FG	7	11	frequency generator: output of the rotation speed (open collector digital output)
GND2	8	12	ground supply return for control circuits
V_P	9	13	supply voltage
CAP-CD	10	14	external capacitor connection for adaptive communication delay timing
CAP-DC	11	15	external capacitor connection for adaptive communication delay timing copy
CAP-ST	12	16	external capacitor connection for start-up oscillator
CAP-TI	13	17	external capacitor connection for timing
+AMP IN	14	18	non-inverting input of the transconductance amplifier
–AMP IN	15	19	inverting input of the transconductance amplifier
AMP OUT	16	20	transconductance amplifier output (open collector)
n.c.	–	21 and 22	not connected
MOT3	17	23 and 24	driver output 3
n.c.	18	25	not connected
MOT0	19	26	input from the star point of the motor coils
GND1	20	27 and 28	ground (0 V) motor supply return for output stages

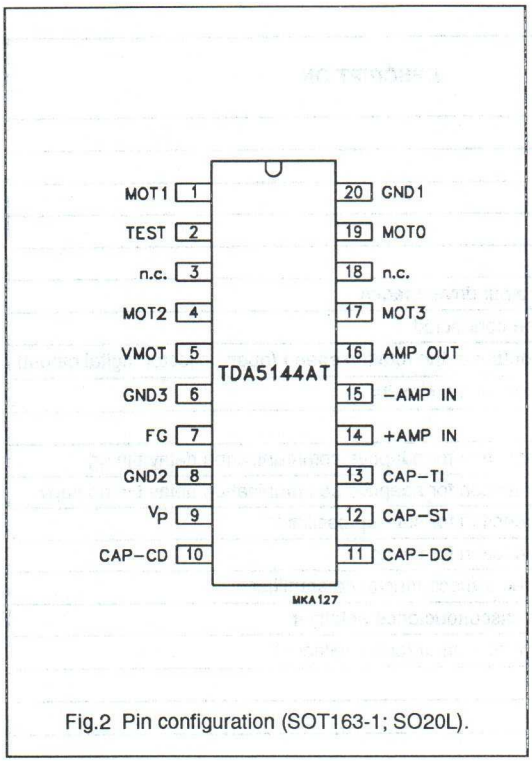


Fig.2 Pin configuration (SOT163-1; SO20L).

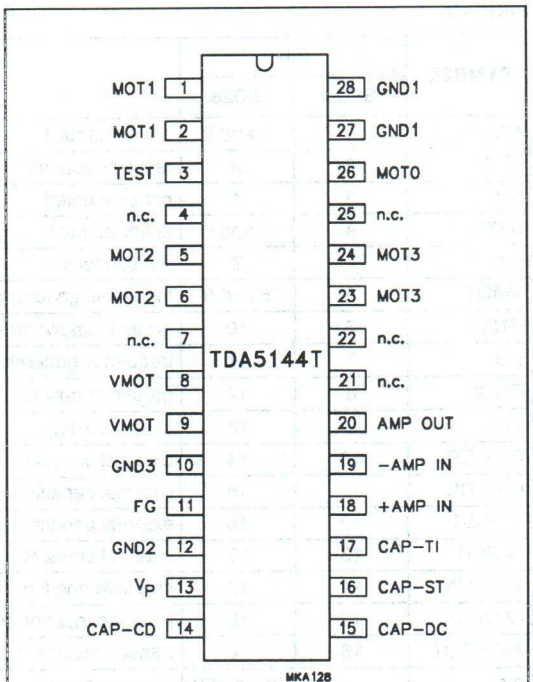


Fig.3 Pin configuration (SOT136-1; SO28L).

FUNCTIONAL DESCRIPTION

The TDA5144 offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5144 offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5144 offers the following features:

- Sensorless commutation by using the motor EMF.
- Built-in start-up circuit.
- Optimum commutation, independent of motor type or motor loading.
- Built-in flyback diodes.
- Three phase full-wave drive.
- High output current (2.0 A).
- Outputs protected by current limiting and thermal protection of each output transistor.
- Low current consumption by adaptive base-drive.
- Soft-switching pulse output for low radiation.
- Accurate frequency generator (FG) by using the motor EMF.
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	18	V
V_I	input voltage; all pins except VMOT	$V_I < 18$ V	−0.3	$V_P + 0.5$	V
V_{VMOT}	VMOT input voltage		−0.5	17	V
V_O	output voltage				
	AMP OUT and FG		GND	V_P	V
	MOT0, MOT1, MOT2 and MOT3		−1	$V_{VMOT} + V_{DHF}$	V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC		–	2.5	V
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
P_{tot}	total power dissipation	see Figs 4 and 5	–	–	W
V_{es}	electrostatic handling	see Chapter "Handling"	–	500	V

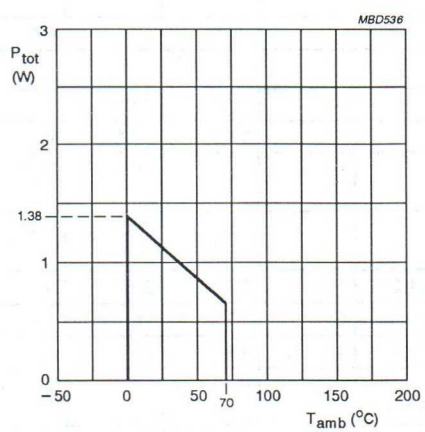


Fig.4 Power derating curve (SOT163-1; SO20L).

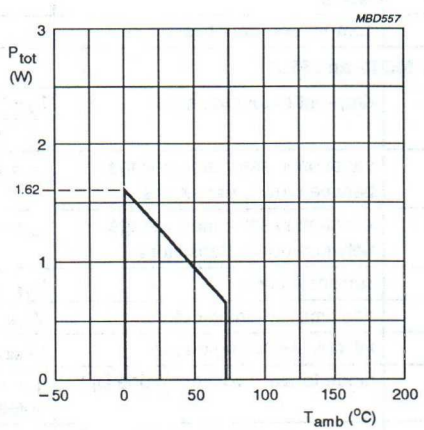


Fig.5 Power derating curve (SOT136-1; SO28L).

HANDLING

Every pin withstands the ESD test according to *"MIL-STD-883C class 2"*. Method 3015 (HBM 1 500 Ω, 100 pF) 3 pulses + and 3 pulses − on each pin referenced to ground.

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	4	–	18	V
I_P	supply current	note 2	–	6.3	7.2	mA
V_{VMOT}	input voltage to the output driver stages	see Fig.1	1.7	–	16	V
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} – 30	–	K
MOT0; centre tap						
V_I	input voltage		–0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} – 1.5 V	–10	–	0	μA
V_{CSW}	comparator switching level	note 3	±20	±25	±30	mV
ΔV_{CSW}	variation in comparator switching levels		–3	0	+3	mV
V_{hys}	comparator input hysteresis		–	75	–	μV
MOT1, MOT2 and MOT3						
V_{DO}	drop-out output voltage	I_O = 100 mA	–	0.9	1.05	V
		I_O = 1000 mA	–	1.6	1.85	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = –100 mA	–	–	180	mV
I_{LIM}	current limiting	V_{VMOT} = 10 V; R_O = 1.2 Ω	1.8	2.0	2.5	A
t_r	rise time switching output	V_{VMOT} = 15 V; see Fig.6	5	10	15	μs
t_f	fall time switching output	V_{VMOT} = 15 V; see Fig.6	10	15	20	μs
V_{DHF}	diode forward voltage (diode D_H)	I_O = –500 mA; notes 4 and 5; see Fig.1	–	–	1.5	V
V_{DLF}	diode forward voltage (diode D_L)	I_O = 500 mA; notes 4 and 5; see Fig.1	–1.5	–	–	V
I_{DM}	peak diode current	note 5	–	–	2.5	A
+AMP IN and –AMP IN						
V_I	input voltage		–0.3	–	V_P – 1.7	V
	differential mode voltage without 'latch-up'		–	–	±V_P	V
I_b	input bias current		–	–	650	nA
C_I	input capacitance		–	4	–	pF
V_{offset}	input offset voltage		–	–	10	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AMP OUT (open collector)						
I_{sink}	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_O	output voltage		−0.5	–	+18	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	–	60	–	mA/μs
G_{tr}	transfer gain		0.3	–	–	S
FG (open collector)						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
$V_{OH(max)}$	maximum HIGH level output voltage		V_P	–	–	V
t_{THL}	HIGH-to-LOW transition time	C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	μs
	ratio of FG frequency and commutation frequency		–	1 : 2	–	
δ	duty factor		–	50	–	%
CAP-ST						
I_{sink}	output sink current		1.5	2.0	2.5	μA
I_{source}	output source current		−2.5	−2.0	−1.5	μA
V_{SWL}	LOW level switching voltage		–	0.20	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-TI						
I_{sink}	output sink current		–	28	–	μA
I_{source}	output source current	0.2 V < V_{CAP-TI} < 0.3 V	–	−57	–	μA
		0.3 V < V_{CAP-TI} < 2.2 V	–	−5	–	μA
V_{SWL}	LOW level switching voltage		–	50	–	mV
V_{SWM}	MIDDLE level switching voltage		–	0.30	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-CD						
I_{sink}	output sink current		10.6	16.2	22	μA
I_{source}	output source current		−5.3	−8.1	−11	μA
I_{sink}/I_{source}	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage		800	875	900	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V
CAP-DC						
I_{sink}	output sink current		10.1	15.5	20.9	μA
I_{source}	output source current		−20.9	−15.5	−10.1	μA
I_{sink}/I_{source}	ratio of sink to source current		0.9	1.025	1.15	
V_{IL}	LOW level input voltage		800	875	900	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V

Notes to the characteristics

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P; $I_O = 0$ mA.
3. Switching levels with respect to MOT1, MOT2 and MOT3.
4. Drivers are in the high-impedance OFF-state.
5. The outputs are short-circuit protected by limiting the current and the IC temperature.

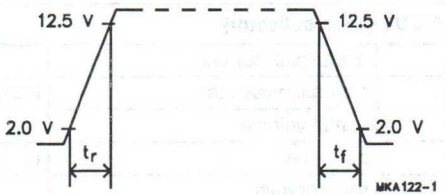
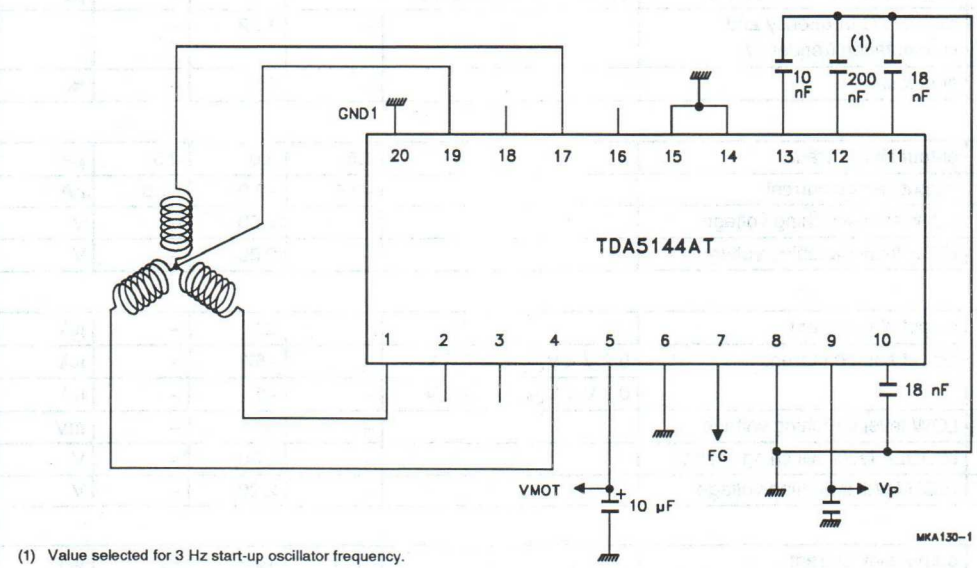


Fig.6 Output transition time measurement.

APPLICATION INFORMATION



(1) Value selected for 3 Hz start-up oscillator frequency.

Fig.7 Application diagram without use of the operational transconductance amplifier (OTA).

Introduction (see Fig.8)

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing (H) and one sinking (L). The third output presents a high impedance (Z) to the motor, which enables measurement of the motor back-EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator. In Table 1 the sequence of the six possible states of the outputs has been depicted.

Table 1 Output states.

STATE	MOT1(1)	MOT2(1)	MOT3(1)
1	Z	L	H
2	H	L	Z
3	H	Z	L
4	Z	H	L
5	L	H	Z
6	L	Z	H

Note

1. H = HIGH state;
   L = LOW state;
   Z = high-impedance OFF-state.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

The detected zero-crossings are used to provide speed information. The information has been made available on the FG output pin. This is an open collector output and provides an output signal with a frequency that is half the commutation frequency.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5144 also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5144 is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patented).

Adjustments

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator.
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor.
- The timing capacitor; this provides the system with its timing signals.

THE START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:
$t_{start} = (2.15 \times C)$ s (with C in μF)

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5144 will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation.

The oscillation of the motor is given by:

$$f_{osc} = \frac{1}{2\pi\sqrt{\frac{K_t \times I \times p}{J}}}$$

where:

K_t = torque constant (N.m/A)

I = current (A)

p = number of magnetic pole-pairs

J = inertia J (kg.m^2)

Example: J = 72 × 10^{-6} kg.m^2, K = 25 × 10^{-3} N.m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF (choose 220 nF).

THE ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 μA and the discharging current 16.2 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}:

$$C = \frac{8.1 \times 10^{-6}}{f \times 1.3} = \frac{6231}{f_{C1}} \text{ (C in nF)}$$

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 16.2 μA;
maximum delay = (0.076 × C) ms (with C in nF).

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz; so:

$$\text{CAP-CD} = \frac{6231}{400} = 15.6 \text{ (choose 18 nF)}$$

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 15.5 μA. The same value can be chosen as for CAP-CD. Figure 9 illustrates typical voltage waveforms.

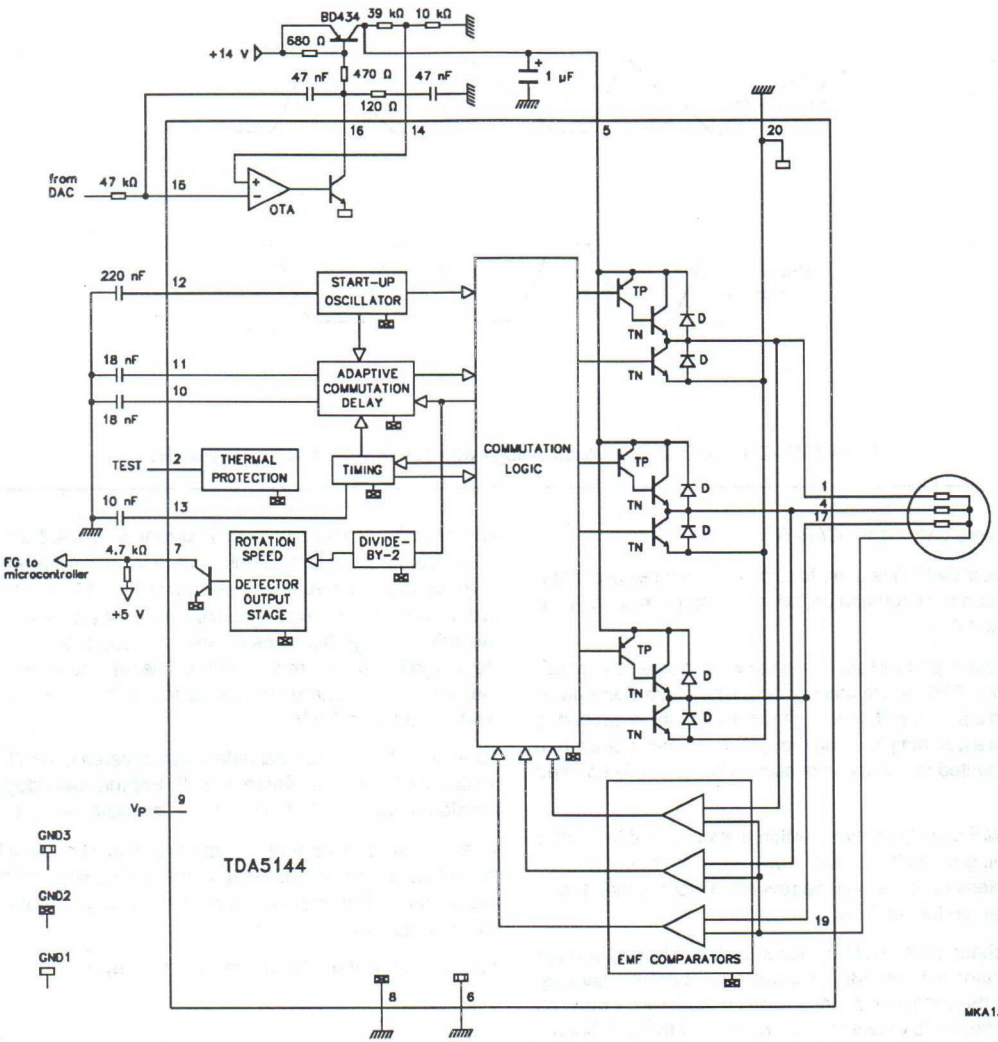


Fig.8 Typical application of the TDA5144 as a scanner driver, with use of OTA.

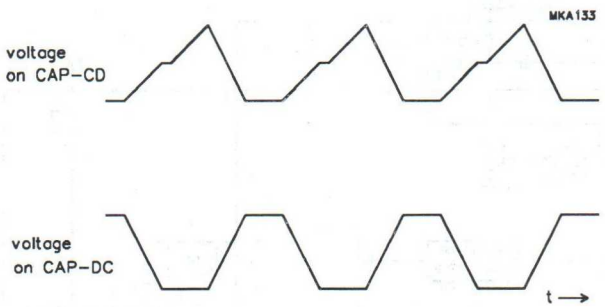


Fig.9 CAP-CD and CAP-DC typical voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).

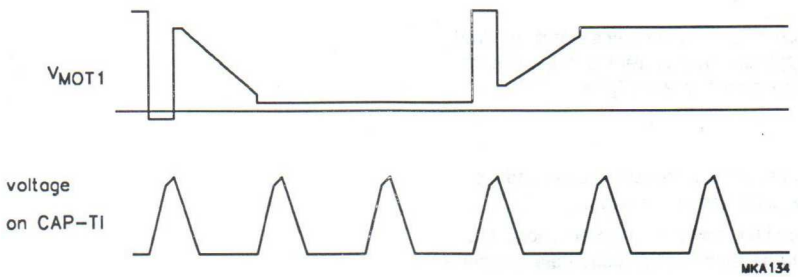
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 μA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 μA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 μA. The watchdog time is the time taken to charge the capacitor, with a current of 5 μA, from 0.3 to 2.2 V.

To ensure that the internal delays are covered CAP-TI must have a minimum value of 2 nF. For the watchdog function a value for CAP-TI of 10 nF is recommended.

To ensure a good start-up and commutation, care must be taken that no oscillations occur at the trailing edge of the flyback pulse. Snubber networks at the outputs should be critically damped.

Typical voltage waveforms are illustrated by Fig.10.



If the chosen value of CAP-TI is too small oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

Fig.10 Typical CAP-TI and V_{MOT1} voltage waveforms in normal running mode.

Other design aspects

There are other design aspects concerning the application of the TDA5144 besides the commutation function. They are:

- Generation of the tacho signal FG
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Reliability.

FG SIGNAL

The FG signal is generated in the TDA5144 by using the zero-crossing of the motor EMF from the three motor windings. Every zero-crossing in a (star connected) motor winding is used to toggle the FG output signal. The FG frequency is therefore half the commutation frequency. All transitions indicate the detection of a zero-crossing.

The accuracy of the FG output signal depends on the symmetry of the motor's electromagnetic construction, which also effects the satisfactory functioning of the motor itself.

Example: a 3-phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 × 6 × 6 = 900 Hz, and generates a tacho signal of 450 Hz.

THE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier. The common mode input range includes ground (GND) and rises to V_P – 1.7 V. The high sink current enables the OTA to drive a power transistor directly in an analog control amplifier.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (AMP OUT) to the positive supply, a positive-going voltage is found when the non-inverting input (+AMP IN) is positive with respect to the inverting input (–AMP IN). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

MOTOR CONTROL

DC motors can be controlled in an analog manner using the OTA.

For the analog control an external transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.8).

RELIABILITY

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current a the conducting 'lower' transistor (+15%). This means that the current to and from the output stages is limite
- Thermal protection of the six output transistors is achieved by each transistor having a thermal sensor that is active when the transistor is switched on. The transistors are switched off when the local temperatur becomes too high.

It is possible, that when braking, the motor voltage (via th flyback diodes and the impedance on VMOT) may cause higher currents than allowed (>0.6 A). These currents must be limited externally.

Brushless DC motor drive circuit — TDA5145

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - output current 2.0 A (typ.)
  - built-in current limiter
  - soft-switching outputs for low Electromagnetic Interference (EMI)
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Motor brake facility
- Direction control input
- Reset function
- Transconductance amplifier for an external control transistor.

APPLICATIONS

- General purpose spindle driver e.g.:
  - Hard disk drive
  - Tape drive
  - Optical disk drive.

GENERAL DESCRIPTION

The TDA5145 is a bipolar integrated circuit used to drive 3-phase brushless DC motors in full-wave mode. The device is sensorless (saving of 3 hall-sensors) using the back-EMF sensing technique to sense the rotor position. It includes bidirectional control, brake function and has a special circuit built-in to reduce the EMI (soft switching output stages).

QUICK REFERENCE DATA

Measured over full voltage and temperature range.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	note 1	4	–	18	V
V_{VMOT}	input voltage to the output driver stages	note 2	1.7	–	16	V
V_{DO}	drop-out output voltage	I_O = 100 mA	–	0.90	1.05	V
I_{LIM}	current limiting	V_{VMOT} = 10 V; R_O = 1.2 Ω	1.8	2.0	2.5	A

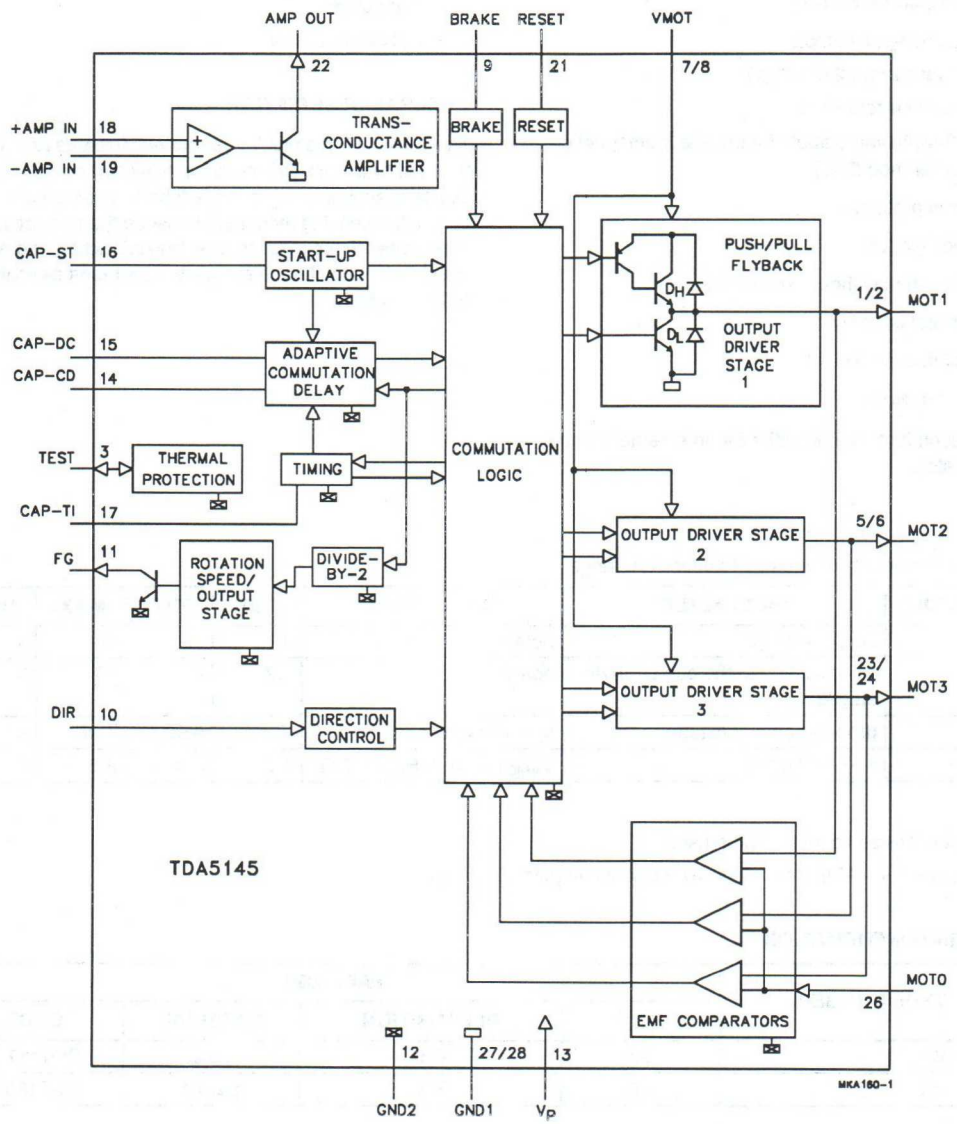
Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN = –AMP IN = 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5145	28	DIL	plastic	SOT117-1
TDA5145T	28	SOL	plastic	SOT136-1

BLOCK DIAGRAM



Pin numbers for both DIL and SOL packages are identical.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN[1]	DESCRIPTION
MOT1	1 and 2	driver output 1
TEST	3	test input/output
n.c.	4	not connected
MOT2	5 and 6	driver output 2
VMOT	7 and 8	input voltage for the output driver stages
BRAKE	9	brake input; this pin may not be left floating, a LOW level voltage must be applied to disable this function
DIR	10	direction control input; this pin may not be left floating
FG	11	frequency generator: output of the rotation speed (open collector digital output)
GND2	12	ground supply return for control circuits
V_P	13	supply voltage
CAP-CD	14	external capacitor connection for adaptive communication delay timing
CAP-DC	15	external capacitor connection for adaptive communication delay timing copy
CAP-ST	16	external capacitor connection for start-up oscillator
CAP-TI	17	external capacitor connection for timing
+AMP IN	18	non-inverting input of the transconductance amplifier
–AMP IN	19	inverting input of the transconductance amplifier
n.c.	20	not connected
RESET	21	reset input; this pin may not be left floating, a LOW level voltage must be applied to disable this function
AMP OUT	22	transconductance amplifier output (open collector)
MOT3	23 and 24	driver output 3
n.c.	25	not connected
MOT0	26	input from the star point of the motor coils
GND1	27 and 28	ground (0 V) motor supply return for output stages

Note

1. Pin numbers for both DIL and SOL packages are identical.

Brushless DC motor drive circuit | TDA5145

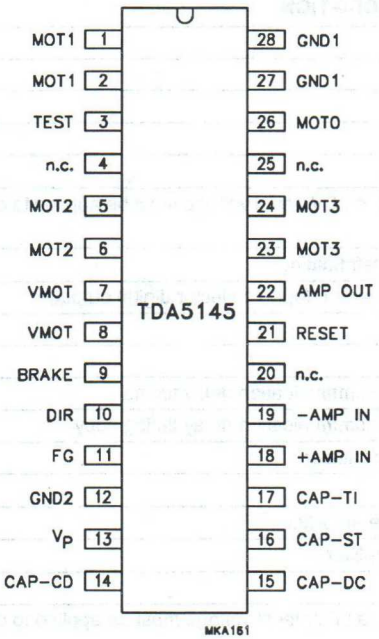


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA5145 offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5145 offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5145 offers the following features:

- Sensorless commutation by using the motor EMF.
- Built-in start-up circuit.
- Optimum commutation, independent of motor type or motor loading.
- Built-in flyback diodes.
- Three phase full-wave drive.
- High output current (2.0 A).
- Outputs protected by current limiting and thermal protection of each output transistor.
- Low current consumption by adaptive base-drive.
- Soft-switching pulse output for low radiation.
- Accurate frequency generator (FG) by using the motor EMF.
- Direction of rotation controlled by one pin.
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier.
- Brake function.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	18	V
V_I	input voltage; all pins except VMOT	$V_I < 18$ V	−0.3	$V_P + 0.5$	V
V_{VMOT}	VMOT input voltage		−0.5	17	V
V_O	output voltage				
	AMP OUT and FG		GND	V_P	V
	MOT0, MOT1, MOT2 and MOT3		−1	$V_{VMOT} + V_{DHF}$	V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC		–	2.5	V
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
P_{tot}	total power dissipation	see Figs 3 and 4	–	–	W
V_{es}	electrostatic handling	see Chapter "Handling"	–	2000	V

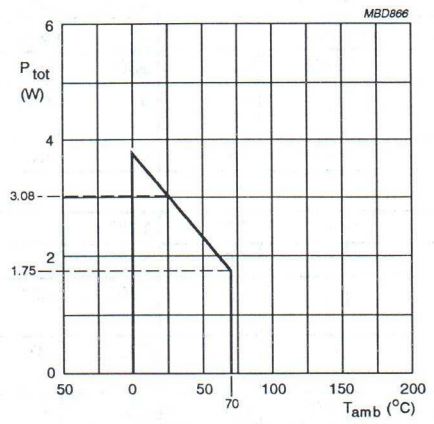


Fig.3 Power derating curve (SOT117-1; DIL28).

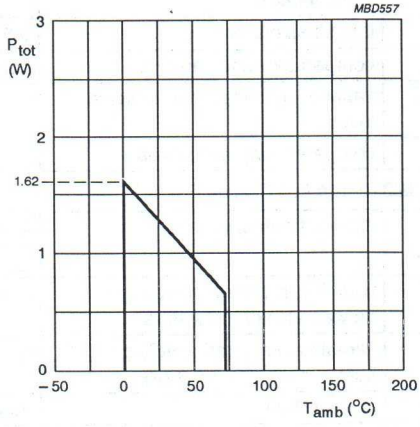


Fig.4 Power derating curve (SOT136-1; SO28L).

HANDLING

Every pin withstands the ESD test according to *"MIL-STD-883C class 2"*. Method 3015 (HBM 1 500 Ω, 100 pF) 3 pulses + and 3 pulses − on each pin referenced to ground.

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	4	–	18	V
I_P	supply current	note 2	–	6.8	7.8	mA
V_{VMOT}	input voltage to the output driver stages	see Fig.1	1.7	–	16	V
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} − 30	–	K

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MOT0; centre tap						
V_I	input voltage		−0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} − 1.5 V	−10	–	–	μA
V_{CSW}	comparator switching level	note 3	±20	±25	±30	mV
ΔV_{CSW}	variation in comparator switching levels		–	–	3	mV
V_{hys}	comparator input hysteresis		–	75	–	μV
MOT1, MOT2 and MOT3; see Fig.5						
V_{DO}	drop-out output voltage	I_O = 100 mA	–	0.9	1.05	V
		I_O = 1000 mA	–	1.6	1.85	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = −100 mA	–	–	180	mV
I_{LIM}	current limiting	V_{VMOT} = 10 V; R_O = 1.2 Ω	1.8	2.0	2.5	A
t_r	rise time switching output	V_{VMOT} = 15 V; see Fig.6	5	10	15	μs
t_f	fall time switching output	V_{VMOT} = 15 V; see Fig.6	10	15	20	μs
V_{DHF}	diode forward voltage (diode D_H)	I_O = −500 mA; notes 4 and 5; see Fig.1	–	–	1.5	V
V_{DLF}	diode forward voltage (diode D_L)	I_O = 500 mA; notes 4 and 5; see Fig.1	−1.5	–	–	V
I_{DM}	peak diode current	note 5	–	–	2.5	A
+AMP IN and −AMP IN						
V_I	input voltage		−0.3	–	V_P − 1.7	V
	differential mode voltage without 'latch-up'		–	–	±V_P	V
I_b	input bias current		–	–	650	nA
C_I	input capacitance		–	4	–	pF
V_{offset}	input offset voltage		–	–	10	mV
AMP OUT (open collector)						
I_{sink}	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_O	output voltage		−0.5	–	+18	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	–	60	–	mA/μs
G_{tr}	transfer gain		0.3	–	–	S
DIR						
V_{IH}	HIGH level input voltage	4 V < V_P < 18 V	2.0	–	–	V
V_{IL}	LOW level input voltage	4 V < V_P < 18 V	–	–	0.8	V
I_{IL}	LOW level input current		–	−20	–	μA
I_{IH}	HIGH level input current		–	20	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RESET						
V_{IH}	HIGH level input voltage	reset mode; 4 V < V_P < 18 V	2.0	–	–	V
V_{IL}	LOW level input voltage	normal mode; 4 V < V_P < 18 V	–	–	0.8	V
I_{IL}	LOW level input current	V_I = 2.0 V	–	–20	–	μA
I_{IH}	HIGH level input current	V_I = 0.8 V	–	20	–	μA
BRAKE						
V_{IH}	HIGH level input voltage	brake mode; 4 V < V_P < 18 V	2.0	–	–	V
V_{IL}	LOW level input voltage	normal mode; 4 V < V_P < 18 V	–	–	0.8	V
I_{IL}	LOW level input current	V_I = 2.0 V	–	–20	–	μA
I_{IH}	HIGH level input current	V_I = 0.8 V	–	20	–	μA
FG (open collector)						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
$V_{OH(max)}$	maximum HIGH level output voltage		V_P	–	–	V
t_{THL}	HIGH-to-LOW transition time	C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	μs
	ratio of FG frequency and commutation frequency		–	1 : 2	–	
δ	duty factor		–	50	–	%
CAP-ST						
I_{sink}	output sink current		1.5	2.0	2.5	μA
I_{source}	output source current		–2.5	–2.0	–1.5	μA
V_{SWL}	LOW level switching voltage		–	0.20	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-TI						
I_{sink}	output sink current		–	28	–	μA
I_{source}	output source current	0.2 V < V_{CAP-TI} < 0.3 V	–	–57	–	μA
		0.3 V < V_{CAP-TI} < 2.2 V	–	–5	–	μA
V_{SWL}	LOW level switching voltage		–	50	–	mV
V_{SWM}	MIDDLE level switching voltage		–	0.30	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-CD						
I_{sink}	output sink current		10.6	16.2	22	μA
I_{source}	output source current		–5.3	–8.1	–11	μA
I_{sink}/I_{source}	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage		850	875	900	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CAP-DC						
I_{sink}	output sink current		10.1	15.5	20.9	µA
I_{source}	output source current		−20.9	−15.5	−10.1	µA
I_{sink}/I_{source}	ratio of sink to source current		0.9	1.025	1.15	
V_{IL}	LOW level input voltage		850	875	900	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P; $I_O = 0$ mA.
3. Switching levels with respect to MOT1, MOT2 and MOT3.
4. Drivers are in the high-impedance OFF-state.
5. The outputs are short-circuit protected by limiting the current and the IC temperature.

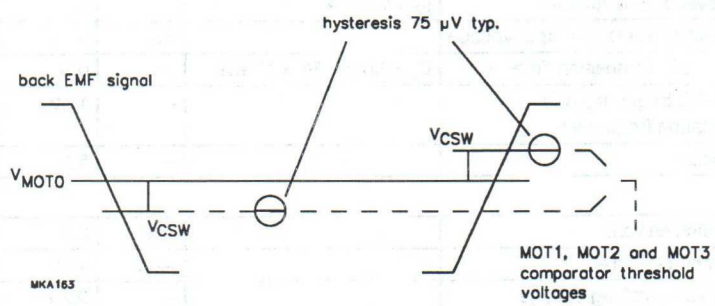


Fig.5 Switching levels with respect to MOT1, MOT2 and MOT3.

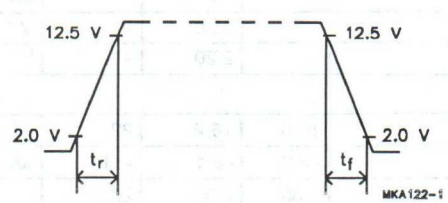
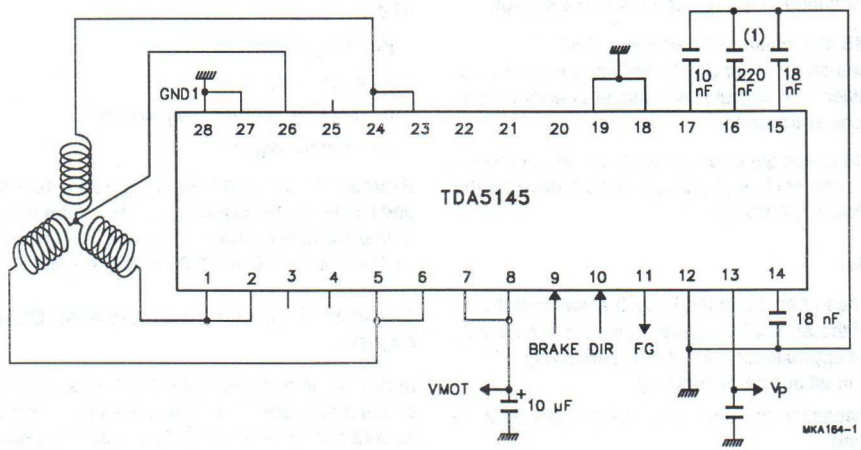


Fig.6 Output transition time measurement.

APPLICATION INFORMATION



(1) Value selected for 3 Hz start-up oscillator frequency.

Fig.7 Application diagram without use of the operational transconductance amplifier (OTA).

Introduction (see Fig.8)

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing (H) and one sinking (L). The third output presents a high impedance (Z) to the motor, which enables measurement of the motor back-EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator. In Table 1 the sequence of the six possible states of the outputs has been depicted.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

Table 1 Output states.

STATE	MOT1(1)	MOT2(1)	MOT3(1)
1	Z	L	H
2	H	L	Z
3	H	Z	L
4	Z	H	L
5	L	H	Z
6	L	Z	H

Note

1. H = HIGH state;
   L = LOW state;
   Z = high-impedance OFF-state.

The detected zero-crossings are used to provide speed information. The information has been made available on the FG output pin. This is an open collector output and provides an output signal with a frequency that is half the commutation frequency.

The system will only function when the EMF voltage from

provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5145 also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5145 is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patented).

Adjustments

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator.
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor.
- The timing capacitor; this provides the system with its timing signals.

THE START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:
t_{start} = (2.15 × C) s (with C in μF)

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5145 will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$$f_{osc} = \frac{1}{2\pi\sqrt{\frac{K_t \times I \times p}{J}}}$$

where:

K_t = torque constant (N.m/A)

I = current (A)

p = number of magnetic pole-pairs

J = inertia J ($kg.m^2$)

Example: J = 72 × 10^{-6} $kg.m^2$, K = 25 × 10^{-3} N.m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF (choose 220 nF).

THE ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 μA and the discharging current 16.2 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}:

$$C = \frac{8.1 \times 10^{-6}}{f \times 1.3} = \frac{6231}{f_{C1}} \text{ (C in nF)}$$

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 16.2 μA;
maximum delay = (0.076 × C) ms (with C in nF)

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz; so:

$$\text{CAP-CD} = \frac{6231}{400} = 15.6 \text{ (choose 18 nF)}$$

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 15.5 μA. The same value can be chosen as for CAP-CD. Figure 9 illustrates typical voltage waveforms.

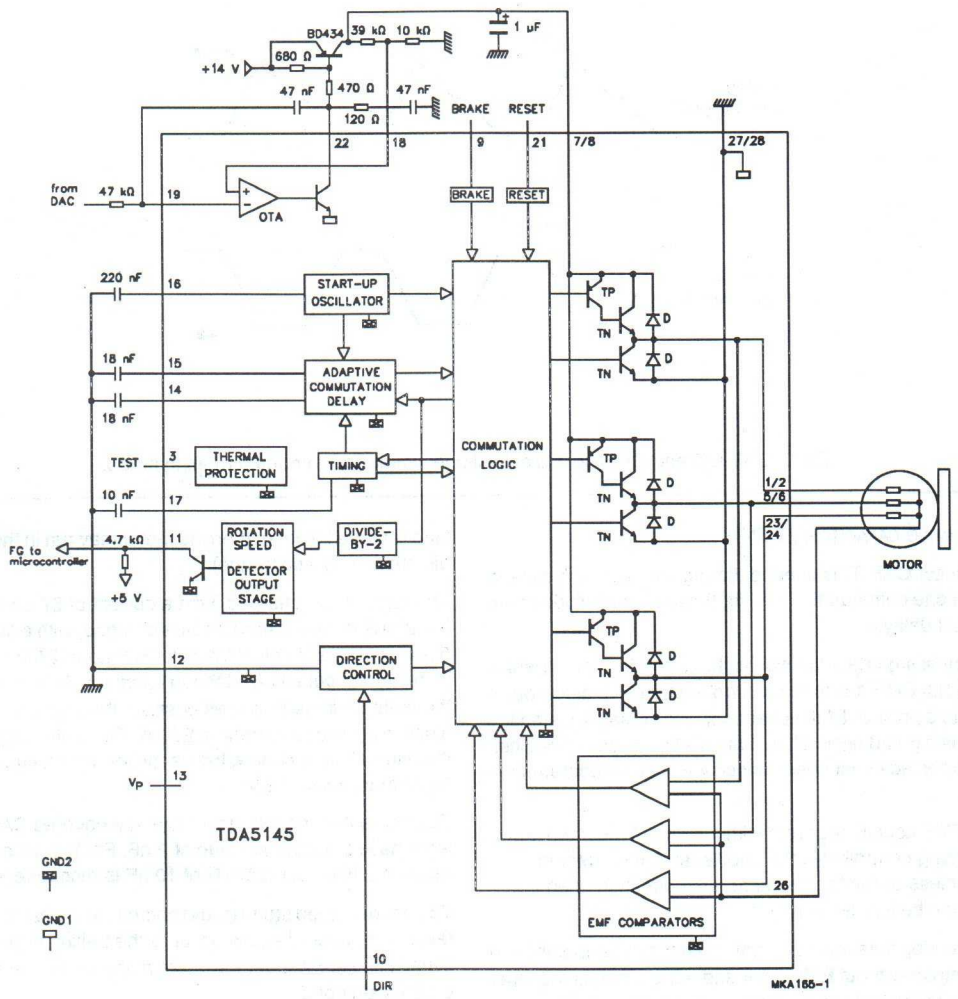


Fig.8 Typical application of the TDA5145 as a scanner driver, with use of OTA.

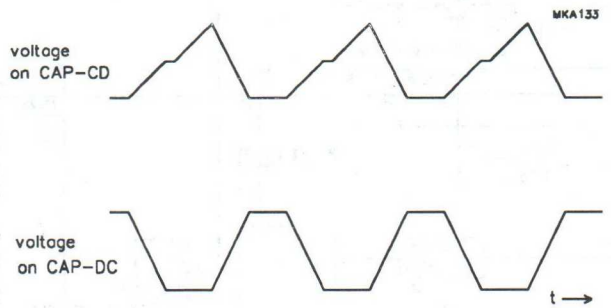


Fig.9 CAP-CD and CAP-DC typical voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).

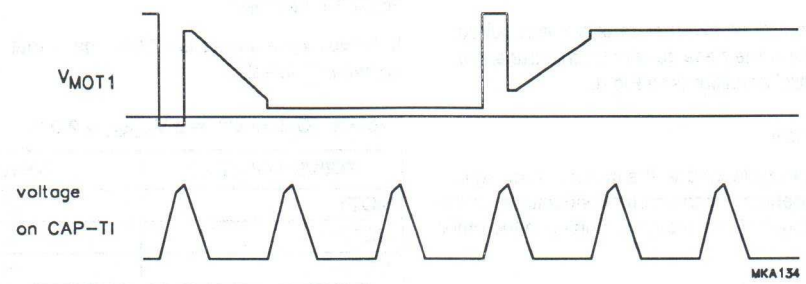
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 μA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 μA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 μA. The watchdog time is the time taken to charge the capacitor, with a current of 5 μA, from 0.3 to 2.2 V.

To ensure that the internal delays are covered CAP-TI must have a minimum value of 2 nF. For the watchdog function a value for CAP-TI of 10 nF is recommended.

To ensure a good start-up and commutation, care must be taken that no oscillations occur at the trailing edge of the flyback pulse. Snubber networks at the outputs should be critically damped.

Typical voltage waveforms are illustrated by Fig.10.



If the chosen value of CAP-TI is too small oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

Fig.10 Typical CAP-TI and V_{MOT1} voltage waveforms in normal running mode.

Other design aspects

There are other design aspects concerning the application of the TDA5145 besides the commutation function. They are:

- Generation of the tacho signal FG
- General purpose operational transconductance amplifier (OTA)
- Motor control
- Direction function
- Brake function
- Reliability.

FG SIGNAL

The FG signal is generated in the TDA5145 by using the zero-crossing of the motor EMF from the three motor windings. Every zero-crossing in a (star connected) motor winding is used to toggle the FG output signal. The FG frequency is therefore half the commutation frequency. All transitions indicate the detection of a zero-crossing.

The accuracy of the FG output signal depends on the symmetry of the motor's electromagnetic construction, which also effects the satisfactory functioning of the motor itself.

Example: a 3-phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 × 6 × 6 = 900 Hz, and generates a tacho signal of 450 Hz.

THE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier. The common mode input range includes ground (GND) and rises to V_P – 1.7 V. The high sink current enables the OTA to drive a power transistor directly in an analog control amplifier.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (AMP OUT) to the positive supply, a positive-going voltage is found when the non-inverting input (+AMP IN) is positive with respect to the inverting input (–AMP IN). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

MOTOR CONTROL

DC motors can be controlled in an analog manner using the OTA.

For the analog control an external transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.8).

DIRECTION FUNCTION

If the voltage at pin 10 is <0.8 V, the motor is running in one direction (depending on the motor connections). If the voltage at pin 10 >2.0 V, the motor is running in the other direction.

BRAKE FUNCTION

If the voltage at pin 9 is >2.0 V, the motor brakes. In that condition, the 3 outputs MOT1, MOT2 and MOT3 are forced at a LOW voltage level and the current limitation is done internally by the sink drivers.

RESET FUNCTION

If the voltage at pin 21 is >2.0 V, the output states are shown in Table 2.

Table 2 Output states if V_{RESET} > 2.0 V.

DRIVER OUTPUT	STATE(1)
MOT1	Z
MOT2	L
MOT3	H

Note

1. Z = high-impedance OFF-state; L = LOW state; H = HIGH state.

Table 3 Switching sequence after a reset pulse.

DIR(1)	RESET(1)	MOT1(1)	MOT2(1)	DIR(1)	FUNCTION
H	H	Z	L	H	reset
H	L	Z	L	H	normal direction mode sequence
H	L	H	L	Z	
H	L	H	Z	L	
H	L	Z	H	L	
H	L	L	H	Z	
H	L	L	Z	H	
L	H	H	L	Z	reset
L	L	H	L	Z	reverse direction mode sequence
L	L	Z	L	H	
L	L	L	Z	H	
L	L	L	H	Z	
L	L	Z	H	L	
L	L	H	Z	L	

Note

1. Z = high-impedance OFF-state; L = LOW state; H = HIGH state.

Table 4 Priority of function.

BRAKE[1]	TEST[1]	RESET[1]	FUNCTION
L	L	L	normal
L	L	H	reset
L	H	L	test
L	H	H	test
H	L	L	brake
H	L	H	brake
H	H	L	brake
H	H	H	brake

Note

1. L = LOW state; H = HIGH state.

RELIABILITY

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+15%). This means that the current to and from the output stages is limited.
- Thermal protection of the six output transistors is achieved by each transistor having a thermal sensor that is active when the transistor is switched on. The transistors are switched off when the local temperature becomes too high.

Section 17
Miscellaneous

INDEX

NE5044	Programmable seven-channel RC encoder	1261
NE/SA630	Single pole double throw (SPDT) switch	1268

Programmable seven-channel RC encoder

NE5044

DESCRIPTION

The NE5044 is a programmable parallel input, serial output pulse width encoder. A multiplexed dual linear ramp technique is used to allow up to 7 inputs to be converted to a serial pulse width modulated signal with excellent linearity and minimal crosstalk. Fixed or variable frame rates can be used, externally controlled, for ease of demodulation. An on-board 5V regulator eliminates power supply sensitivities and provides up to 20mA current capability for driving external loads.

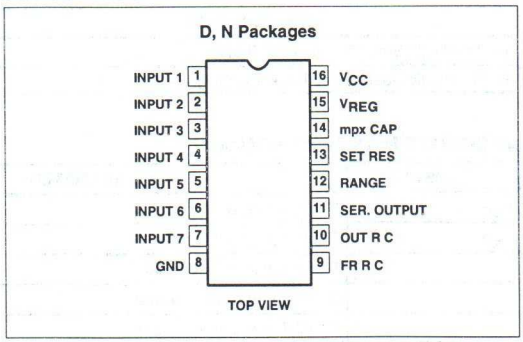
FEATURES

- 3 to 7 channels, externally selectable
- Constant-current dual linear ramp for linearity better than 0.3%
- Internal voltage regulator for low drift
- Wide supply range 4.5-12V
- Fixed or variable frame rate set by external RC
- External control for channel gain or range
- Versatile applications: exponential rates, mixing, dual rate, reversing, etc.
- Compatible with all transmission mediums

APPLICATIONS

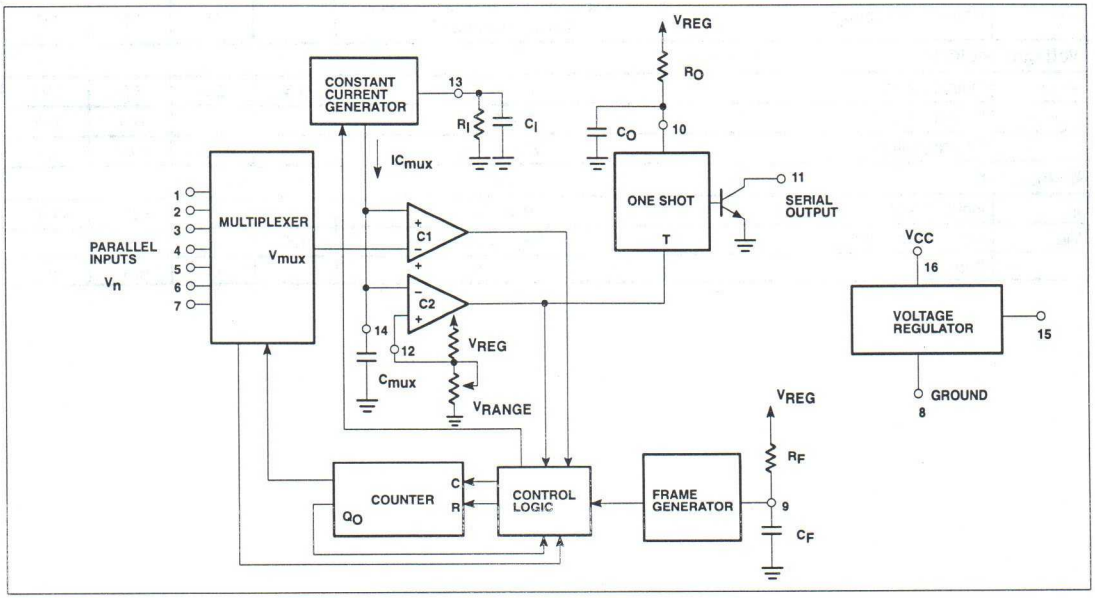
- Radio-controlled aircraft, cars, boats, trains

PIN CONFIGURATION



- Industrial controllers
- Remote-controlled entertainment systems
- Security systems
- Instrumentation recorders/controls
- Remote analog/digital data transmission
- Automotive sensor systems
- Robotics
- Telemetry

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE5044D	0005D
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5044N	0406C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	13	V
I_{OUT}	Regulator output current	-25	mA
	Serial output peak current	30	mA
	Constant-current generator	-1	mA
	Parallel inputs, range input	0-V_{REG}	V
	One-shot input, frame generator input	0-V_{REG}	V
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:
1. T_A=25°C, unless otherwise stated.

DC ELECTRICAL CHARACTERISTICS

Test Conditions T_A = 25°C V_{CC}=10V using Test Circuit, unless otherwise stated.

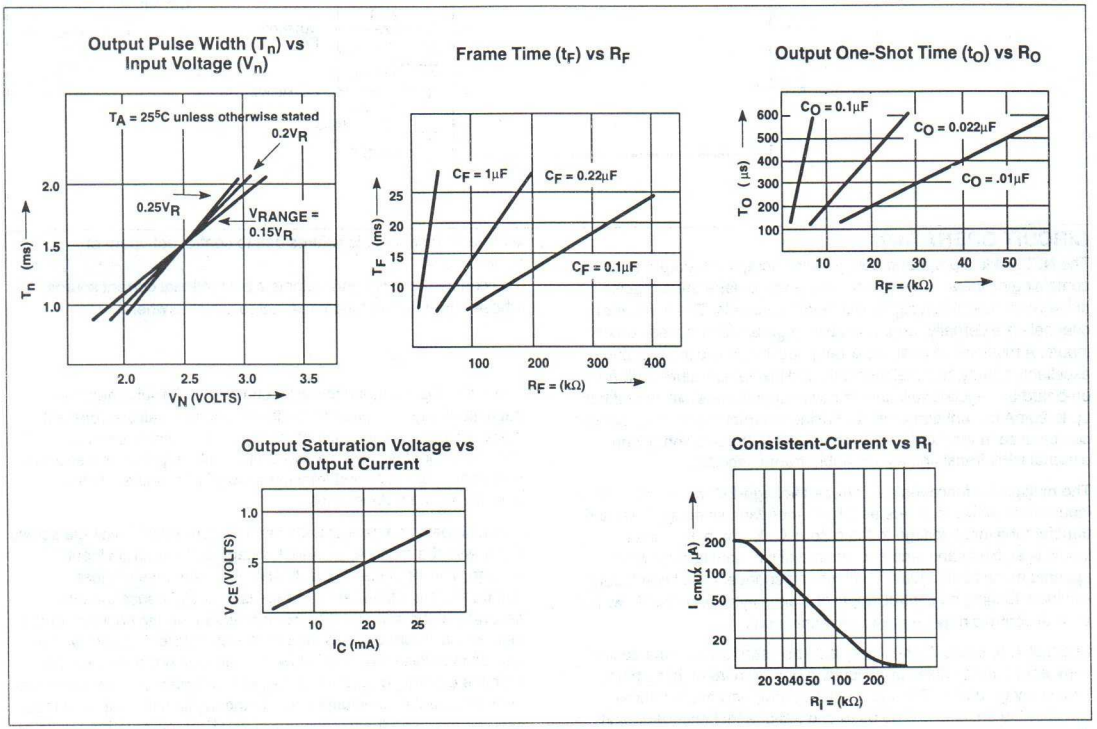
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Power supply requirements						
V_{CC}	Power supply voltage range		4.5		12	V
I_{CC}	Power supply current	Excluding control pots and serial output currents		11	15	mA
Voltage regulator						
V_{REG}	Output voltage		4.5	5.0	5.5	V
I_{OUT}	Output current	$V_R \geq 4.5V$			-20	mA
	Line regulation	$7 \leq V_{CC} \leq 12$		0.005	0.02	V/V
Multiplexer						
I_{IN}	Input current	V_n=2.5V		±30	±200	nA
V_{IN}	Input voltage range	$V_n - V_{Range} \geq 0.75V$	1.5		5	V
	Crosstalk			±1	±5	µs

AC ELECTRICAL CHARACTERISTICS

Test conditions T_A=25°C, V_{CC}=10V using Test Circuit, unless otherwise stated.

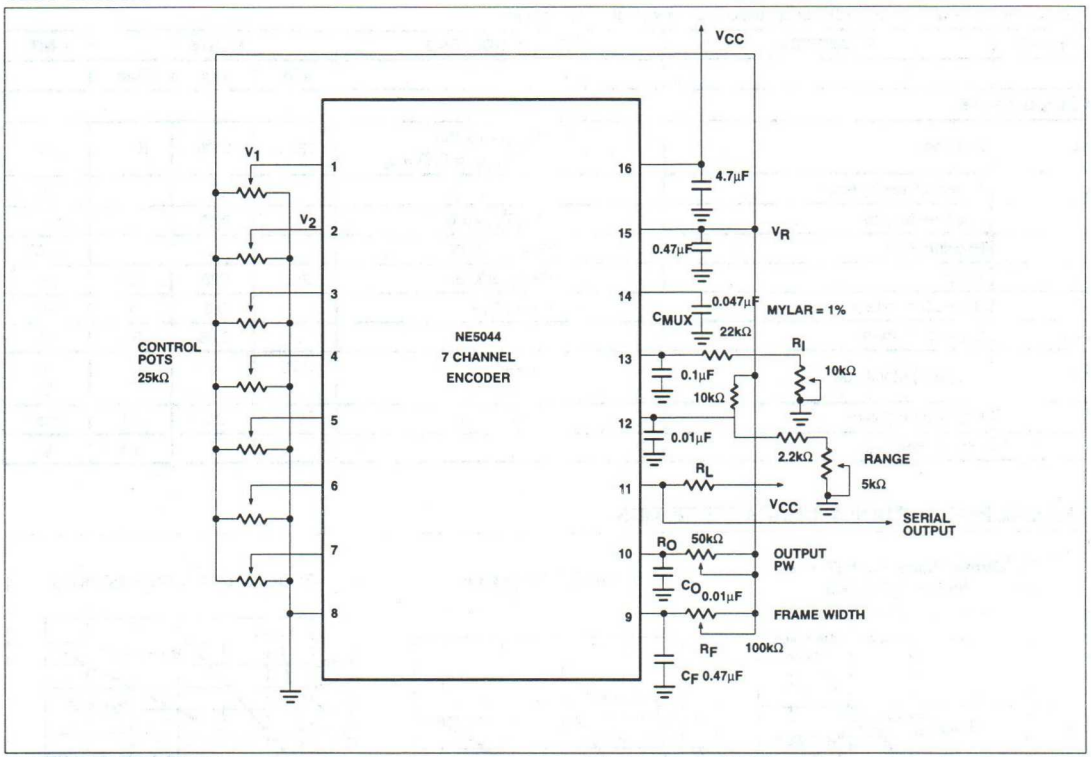
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Output pulse						
t_n	Position	$R_I \bullet C_{MUX}$=1.25ms V_n=0.5V_{REG}; V_{RANGE}=0.2V_{REG}	1350	1500	1650	µs
	Position linearity error			5		µs
	Position tempco	0°C ≤ T_A ≤70°C		0.15		µs/°C
	Position PSR	6V≤V_{CC} ≤12V		0.5	1	µs/V
t_O	Width	R_OC_O=300µs	240	285	330	µs
	Saturation voltage	I_O=25mA		0.6	1	V
I_{11}	Leakage current			0.05	50	µA
R_I	Range input voltage	R_I=50kΩ R_I=25kΩ	0.75 1.00			V V
	Frame time (fixed)	R_FC_F=30ms	17	20	23	ms
	Inhibit threshold				0.4	V

TYPICAL PERFORMANCE CHARACTERISTICS



Programmable seven-channel RC encoder | NE5044

TEST CIRCUIT



CIRCUIT OPERATION

The NE5044 is a programmable parallel input, serial output encoder containing all the active circuitry necessary to generate a precise pulse width modulated signal with 3 to 7 channels. The number of channels is externally programmable by grounding unused control inputs. A multiplexed dual linear ramp technique is used to provide excellent linearity, minimal crosstalk and low temperature drift. An on-board 5V regulator eliminates power supply sensitivities and has up to 20mA current capability for driving external loads. The encoder can be used in the fixed-frame mode or, with the addition of one external NPN transistor, as a variable-frame encoder.

The multiplexer functions as a strobed voltage-follower so that each input, when active, appears as a high-impedance input (>1MΩ) and transfers the input voltage to the output. Only one of the seven inputs is active at any time and when a given input is inactive, it appears as an open circuit. The high-impedance multiplexer inputs eliminate loading on control inputs and simplify mixing circuits where several controls may be mixed onto one input.

Channel 4, 5, 6 and 7 inputs may also be used to select the desired number of output pulses by grounding one or more of these pins. That is, by grounding Pin 4 (Channel 4 input) only the first three inputs of the encoder will be used and a 3-channel encoder results. Grounding Pin 5 results in a 4-channel encoder, and so on. Thus, any number of channels between 3 and 7 may be selected. Internal voltage clamping prevents encoder malfunction if any input is shorted to supply, ground or open-circuited. The remaining channels will continue to be encoded except as noted above. This feature eliminates catastrophic failures due to control pot open- or short-circuits.

The constant-current generator is a bidirectional current source whose current is set by an external resistor R_I, where:

$$I_C = \pm \frac{V_R}{2R_I}$$

The current generator alternately charges and discharges the capacitor C_{MUX}. An internal feedback loop maintains a constant current and very high output impedance. This yields a typical linearity error of voltage input to pulse width output for the encoder of less than 0.1%. An external capacitor, C_I, is required to insure stability of the feedback loop.

Two high gain comparators, C1 and C2, compare the voltage across C_{MUX} with the multiplexer output voltage and the range input voltage. The input bias currents and offset voltages of these comparators are sufficiently low so as to not influence the overall accuracy of the encoder. The comparators feed the counter control logic which in turn controls the counter and current generator. The operation of this loop is as follows: When I_C is positive (sourced from the current generator into C_{MUX}) the capacitor linearly charges up until it reaches a voltage equal to the multiplexer output voltage; assume this to be the voltage at Pin 1, V1. At this time the output of C1 goes high, which reverses the direction of I_C (sinking into current generator from C_{MUX}). C_{MUX} now linearly discharges until it reaches the voltage set on Pin 12, V_{RANGE}. At this time the output of C2 goes high, which again reverses the polarity of I_C, clocks the

counter, and triggers the output one-shot. C_{MUX} again charges up but now C1 goes high when C_{MUX} reaches V2, the voltage on Pin 2. The resulting voltage waveform on C_{MUX} is a triangle wave whose positive peaks correspond to the voltages on Pins 1 through 7 for the first through seventh peaks and whose negative peaks are constant and equal to V_{RANGE}. This waveform is shown in the first portion of Figure 1.

Independent control of I_C and V_{RANGE} allows the encoder to be tailored to virtually any combination of input voltage changes and output pulse width changes. The functional relationships between these variables will be defined in the next section.

The frame generator controls the encoder frame time. It can operate as an astable or monostable multivibrator whose period is $0.66 \times R_F C_F$. The encoder will generate a synchronizing pulse at the end of each frame. When C_{MUX} reaches the seventh positive peak it reverses and discharges to V_{RANGE}. The counter is clocked to the state where Q_O is high when $VC_{MUX}=V_{RANGE}$. C_{MUX} again charges up, but now the output of C1 is ignored, due to Q_O being high, and charges up to V_{CLAMP} and remains there. The encoder will remain in this state until a pulse from the frame generator is received. If R_F and C_F are connected as shown in the Block Diagram, then the frame generator operates in the astable mode, producing a narrow pulse output. This pulse allows C_{MUX} to start discharging again. When C_{MUX} reaches V_{RANGE}, the counter is clocked to the state where Q_1 is high (channel 1) and the entire process starts over. The frame period in this mode is $0.66 \times R_F C_F$ and is referred to as the fixed-frame mode. The variable-frame mode will be discussed in the application section.

The output one-shot generates a positive pulse whose width is equal to $R_O C_O$. The output is an open-collector, NPN transistor capable of sinking 25mA. This configuration allows the encoder to drive a wide variety of RF stages as well as providing current pulses in 2-wire communications applications.

ENCODER DESIGN EQUATIONS

The triangular waveform on C_{MUX} has a fixed slope (constant current) and variable positive peak voltages. The time between the negative peaks of C_{MUX}, which is equal to the output period for that channel, is given by:

$$t_n = \frac{2\,(V_n - V_{RANGE})\,C_{MUX}}{I_C}$$

I_C is given by:

$$I_C = \frac{V_R}{2R_I}$$

where V_R=Reference Voltage.

Additionally, V_n, the voltage on Pin n, which is the control voltage for Channel n, is typically the wiper voltage on a pot connected between V_R and ground. Thus $V_n = X_n V_R$.

V_{RANGE} is also derived from V_R so that $V_{RANGE}=Y\,V_R$. The resulting channel time period is:

$$t_n = \frac{2\,(X_n - Y)\,V_R \cdot C_{MUX}}{(V_R / 2R_I)}$$

$$\boxed{t_n = 4R_I\,C_{MUX}\,(X_n - Y)}$$

Thus, each channel pulse width, t_n, is independent of supply voltage and depends only on external passive components.

The conversion rate, CR, for each channel is the change in output period, Δt_n, divided by the change in input voltage for that channel, ΔV_n.

$$CR = \frac{\Delta\,t_n}{\Delta\,V_n} = \frac{\Delta\,t_n}{\Delta\,X_n} = 4\,R_I\,C_{MUX}$$

In most applications, the input variable X_n will have some neutral or center value about which it will vary, thus $X_n = X_O + X_n$,

and

$$\boxed{CR = \frac{\Delta\,t_n}{\Delta\,X_n} = 4R_I\,C_{MUX}}$$

Where X_O is the neutral value for X and is assumed to be the same for all n. Now

$$t_n = 4R_I C_{MUX}\,(X_O - Y + X_n)$$

If we let $t_{NEUTRAL}=4R_I C_{MUX}\,(X_O - Y)$ be the neutral value for t_n, then

$$\boxed{t_n = t_{NEUTRAL} + 4R_I\,C_{MUX}\,(X_n)}$$

Consider the following example to see how these design equations are used.

Assume:

$t_{NEUTRAL}$=1.5ms

X_O=0.5—Control pot in center at

$t_n = t_{NEUTRAL}$

$\Delta x_n = \pm 0.1$—Control pot resistance varies ±10% (of total resistance) around neutral. This should include mechanical trim if used.

$\Delta t_n = \pm 0.5$ms

For this example, the conversion rate is

$$CR = \frac{\Delta\,t_n}{\Delta\,X_n} = \frac{0.5\text{ms}}{0.1} = 5\text{ms}$$

so

$4R_I C_{MUX}$=5ms.

If we let C_{MUX}=0.047µF then

$$R_I = \frac{5\text{ms}}{4\ X\ 0.047\mu\text{F}} = 26.5\text{k}\Omega = 27\text{k}\Omega$$

and

$t_{NEUTRAL} = 1.5\text{ms} = 4R_I C_{MUX}(X_O - Y)$

$$Y = 0.5 - \frac{1.5\text{ms}}{5\text{ms}} = 0.2$$

The output pulse width is given by

$t_O = R_O C_O$

so if t_O=330µs and C_O=0.01µF then

$$R_O = \frac{330\mu s}{0.01\mu F} = 33k\Omega$$

The frame time constant, t_F, is given by

$t_F = 0.66\ R_F C_F$

If t_F=20ms and C_F=0.47µF

$$R_F = \frac{20ms}{0.66X0.47\mu F} = 62k$$

Figure 2 shows the external connections for this example.

It should be noted that the temperature stability of all the encoded times depend on the temperature coefficients of the respective external R_C time constants. No internal temperature compensation is used on the chip. The typical temperature sensitivity of t_n using wirewound resistors and polycarbonate capacitors is less than 100ppm/°C in the -20°C to +70°C temperature range. For the above example, this corresponds to a change in t_n of ±7.5µs for a change in temperature of ±50°C.

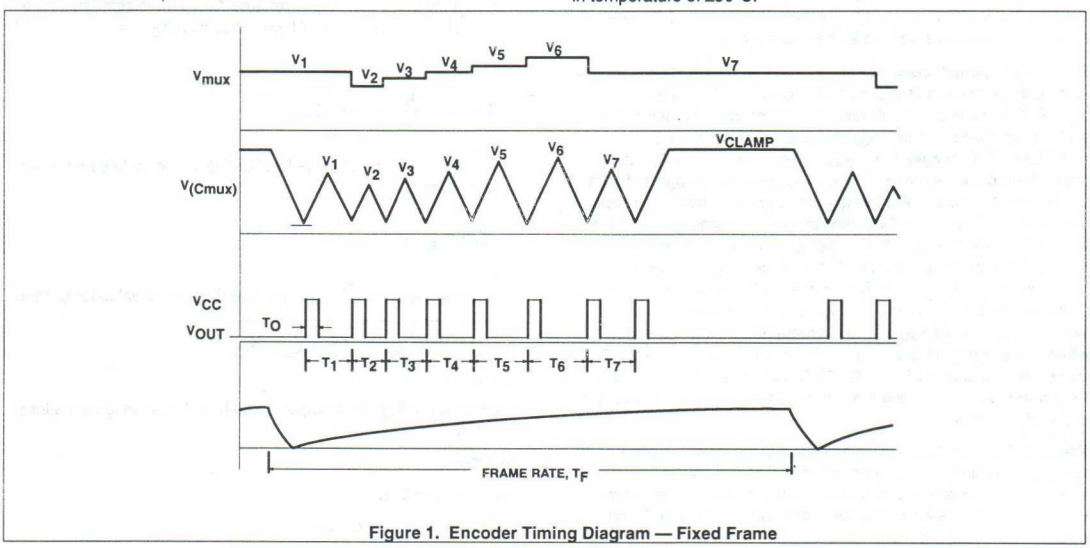


Figure 1. Encoder Timing Diagram — Fixed Frame

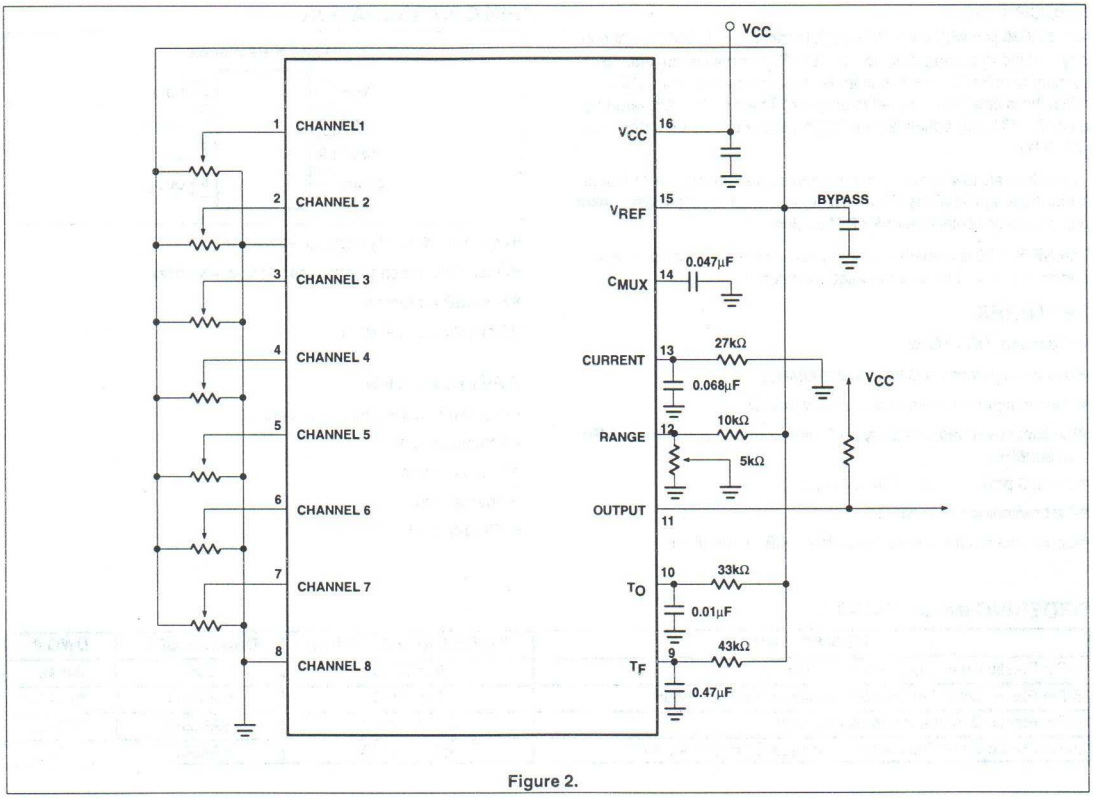

VCC
1
CHANNEL1
2
CHANNEL 2
3
CHANNEL 3
4
CHANNEL 4
5
CHANNEL 5
6
CHANNEL 6
7
CHANNEL 7
8
CHANNEL 8
VCC
16
VREF
15
BYPASS
0.047µF
CMUX
14
27kΩ
CURRENT
13
0.068µF
VCC
10kΩ
RANGE
12
5kΩ
OUTPUT
11
33kΩ
TO
10
0.01µF
43kΩ
TF
9
0.47µF

Figure 2.

Single pole double throw (SPDT) switch — NE/SA630

DESCRIPTION

The NE630 is a wideband RF switch fabricated in BiCMOS technology and incorporating on-chip CMOS/TTL compatible drivers. Its primary function is to switch signals in the frequency range DC - 1GHz from one 50Ω channel to another. The switch is activated by a CMOS/TTL compatible signal applied to the enable channel 1 pin (ENCH1).

The extremely low current consumption makes the NE/SA630 ideal for portable applications. The excellent isolation and low loss makes this a suitable replacement for PIN diodes.

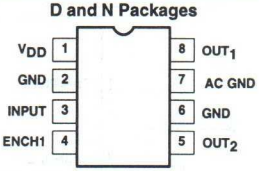
The NE/SA630 is available in an 8-pin dual in-line plastic package and an 8-pin SO (surface mounted miniature) package.

FEATURES

- Wideband (DC - 1GHz)
- Low through loss (1dB typical at 200MHz)
- Unused input is terminated internally in 50Ω
- Excellent overload capability (1dB gain compression point +18dBm at 300MHz)
- Low DC power (170μA from 5V supply)
- Fast switching (20ns typical)
- Good isolation (off channel isolation 60dB at 100MHz)

PIN CONFIGURATION

D and N Packages



- Low distortion (IP_3 intercept +33dBm)
- Good 50Ω match (return loss 18dB at 400MHz)
- Full ESD protection
- Bidirectional operation

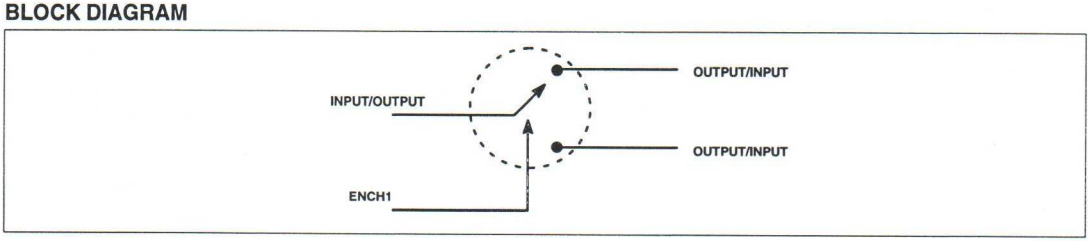
APPLICATIONS

- Digital transceiver front-end switch
- Antenna switch
- Filter selection
- Video switch
- FSK transmitter

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to 70°C	NE630N	0404B
8-Pin Plastic Small Outline (SO) package (Surface-mount)	0 to 70°C	NE630D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA630N	0404B
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA630D	0174C

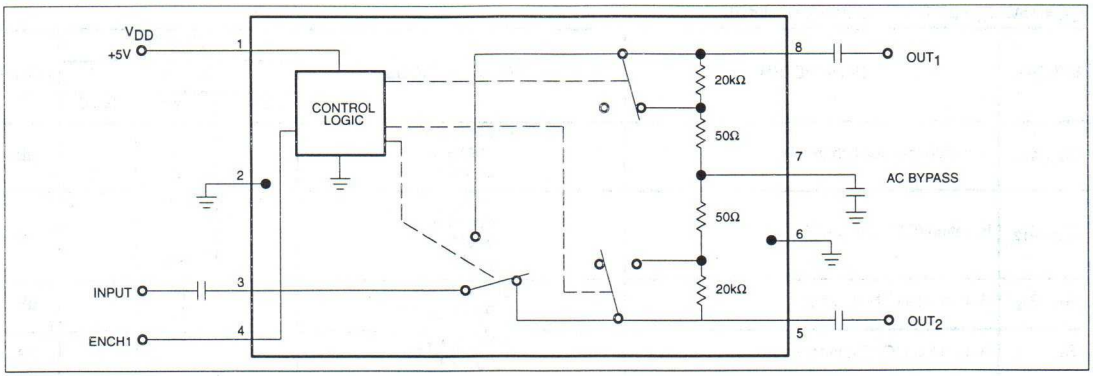
BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	3.0 to 5.5V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	-0.5 to +5.5	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 8-Pin Plastic DIP 8-Pin Plastic SO	 1160 780	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   8-Pin DIP: θ_{JA} = 108°C/W
   8-Pin SO: θ_{JA} = 158°C/W

DC ELECTRICAL CHARACTERISTICS

V_{DD} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA630			
			MIN	TYP	MAX	
I_{DD}	Supply current		40	170	300	µA
V_T	TTL/CMOS logic threshold voltage[1]		1.1	1.25	1.4	V
V_{IH}	Logic 1 level	Enable channel 1	2.0		V_{DD}	V
V_{IL}	Logic 0 level	Enable channel 2	-0.3		0.8	V
I_{IL}	ENCH1 input current	ENCH1 = 0.4V	-1	0	1	µA
I_{IH}	ENCH1 input current	ENCH1 = 2.4V	-1	0	1	µA

NOTE:
1. The ENCH1 input must be connected to a valid Logic Level for proper operation of the NE/SA630.

AC ELECTRICAL CHARACTERISTICS[1] - D PACKAGE

V_{DD} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA630			
			MIN	TYP	MAX	
S_{21}, S_{12}	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2	 2.8	dB
S_{21}, S_{12}	Isolation (OFF channel)[2]	10MHz 100MHz 500MHz 900MHz	70 24	80 60 50 30		dB
S_{11}, S_{22}	Return loss (ON channel)	DC - 400MHz 900MHz		20 12		dB
S_{11}, S_{22}	Return loss (OFF channel)	DC - 400MHz 900MHz		17 13		dB
t_D	Switching speed (on-off delay)	50% TTL to 90/10% RF		20		ns
t_r, t_f	Switching speeds (on-off rise/fall time)	90%/10% to 10%/90% RF		5		ns
	Switching transients			165		mV_{P-P}
P_{-1dB}	1dB gain compression	DC - 1GHz		+18		dBm
IP_3	Third-order intermodulation intercept	100MHz		+33		dBm
IP_2	Second-order intermodulation intercept	100MHz		+52		dBm
NF	Noise figure (Z_O = 50Ω)	100MHz 900MHz		1.0 2.0		dB

NOTE:
1. All measurements include the effects of the D package NE/SA630 Evaluation Board (see Figure 1B). Measurement system impedance is 50Ω.
2. The placement of the AC bypass capacitor is critical to achieve these specifications. See the applications section for more details.

AC ELECTRICAL CHARACTERISTICS[1] - N PACKAGE

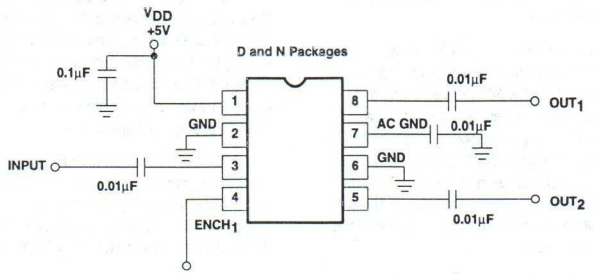
V_{DD} = +5V, T_A = 25°C; all other characteristics similar to the D-Package, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA630			
			MIN	TYP	MAX	
S_{21}, S_{12}	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2.5		dB
S_{21}, S_{12}	Isolation (OFF channel)	10MHz 100MHz 500MHz 900MHz	58	68 50 37 15		dB
NF	Noise figure (Z_O = 50Ω)	100MHz 900MHz		1.0 2.5		dB

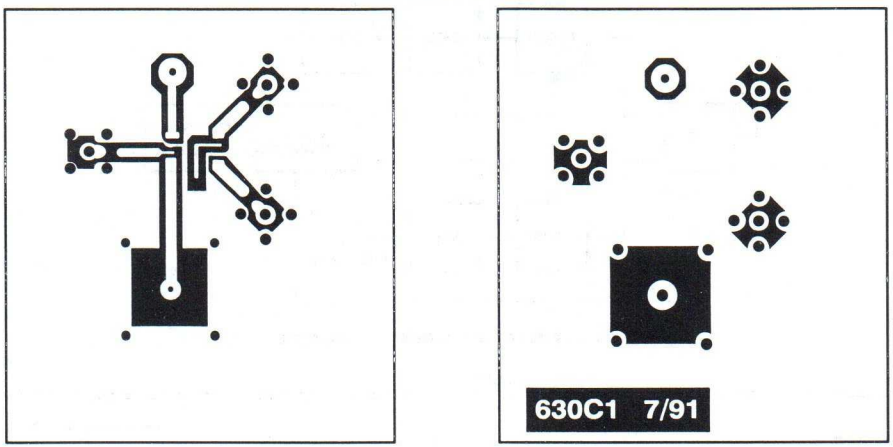
NOTE:
1. All measurements include the effects of the N package NE/SA630 Evaluation Board (see Figure 1C). Measurement system impedance is 50Ω.

APPLICATIONS

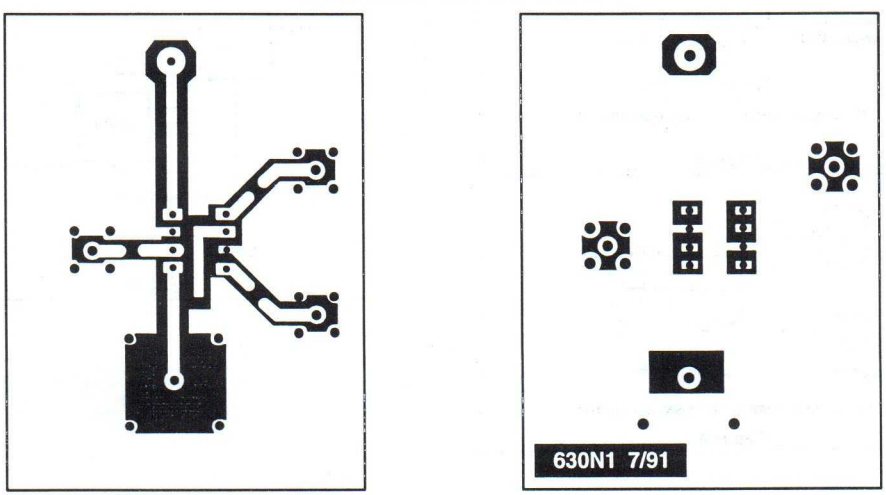
The typical applications schematic and printed circuit board layout of the NE/SA630 evaluation board is shown in Figure 1. The layout of the board is simple, but a few cautions need to be observed. The input and output traces should be 50Ω. The placement of the AC bypass capacitor is *extremely critical* if a symmetric isolation between the two channels is desired. The trace from Pin 7 should be drawn back towards the package and then be routed downwards. The capacitor should be placed straight down as close to the device as practical. For better isolation between the two channels at higher frequencies, it is also advisable to run the two output/input traces at an angle. This also minimizes any inductive coupling between the two traces. The power supply bypass capacitor should be placed close to the device. Figure 7 shows the frequency response of the NE/SA630. The loss matching between the two channels is excellent to 1.2GHz as shown in Figure 10.



a. NE/SA Evaluation Board Schematic



b. NE/SA630 D-Package Board Layout



c. NE/SA630 N-Package Board Layout

Figure 1.

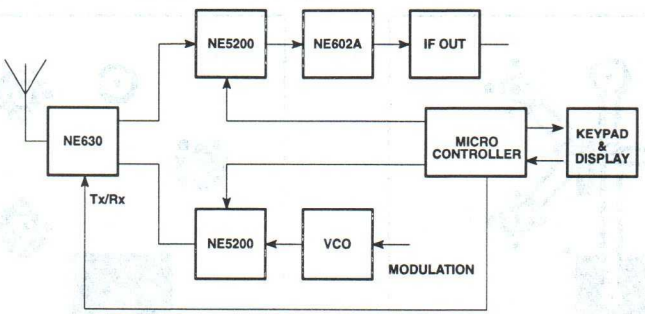
Single pole double throw (SPDT) switch NE/SA630

The isolation and matching of the two channels over frequency is shown in Figures 12 and 14, respectively.

The NE630 is a very versatile part and can be used in many applications. Figure 2 shows a block diagram of a typical Digital RF transceiver front-end. In this application the NE630 replaces the duplexer which is typically very bulky and lossy. Due to the low power consumption of the device, it is ideally suited for handheld applications such as in CT2 cordless telephones. The NE630 can also be used to generate Amplitude Shift Keying (ASK) or On-Off Keying (OOK) and Frequency Shift Keying (FSK) signals for digital RF communications systems. Block diagrams for these applications are shown in Figures 3 and 4, respectively.

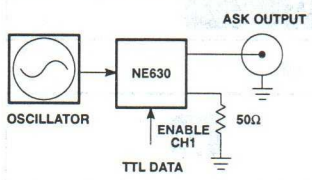
For applications that require a higher isolation at 1GHz than obtained from a single NE630, several NE630s can be cascaded as shown in Figure 5. The cascaded configuration will have a higher loss but greater than 35dB of isolation at 1GHz and greater than 65dB @ 500MHz can be obtained from this configuration. By modifying the enable control, an RF multiplexer/ de-multiplexer or antenna selector can be constructed. The simplicity of NE630 coupled with its ease of use and high performance lends itself to many innovative applications.

The NE/SA630 switch terminates the OFF channel in 50Ω. The 50Ω resistor is internal and is in series with the external AC bypass capacitor. Matching to impedances other than 50Ω can be achieved by adding a resistor in series with the AC bypass capacitor (e.g., 25Ω additional to match to a 75Ω environment).



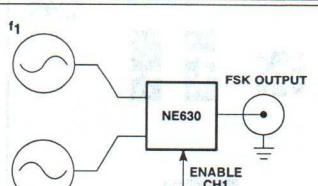
A TYPICAL TDMA/DIGITAL RF TRANSCEIVER SYSTEM FRONT-END

Figure 2.



AMPLITUDE SHIFT KEYING (ASK) GENERATOR

Figure 3.



FREQUENCY SHIFT KEYING (FSK) GENERATOR

Figure 4.

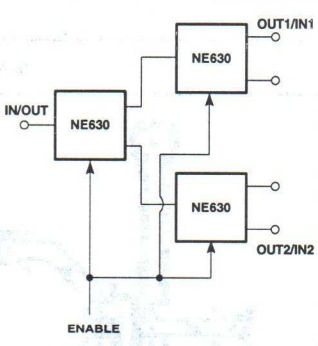


Figure 5.

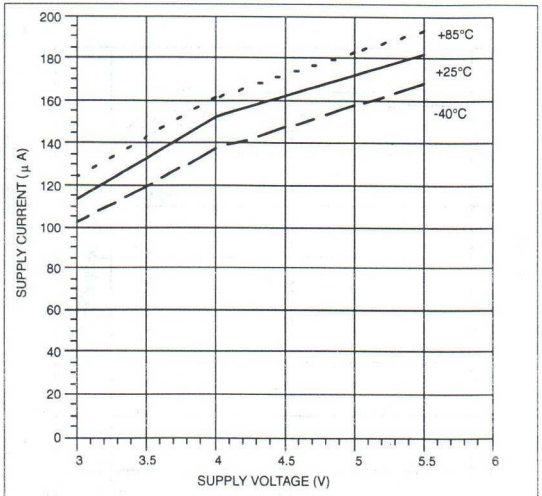


Figure 6. Supply Current vs. V_{DD} and Temperature

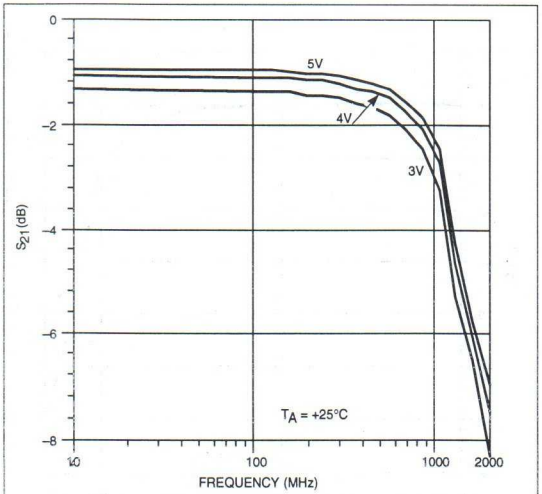


Figure 7. Loss vs. Frequency and V_{DD} for D-Package

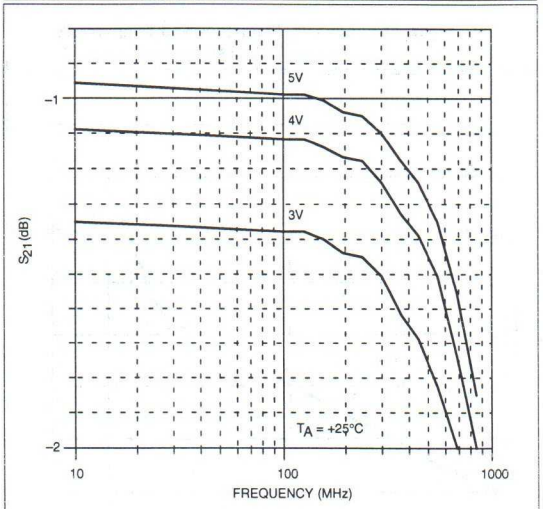


Figure 8. Loss vs. Frequency and V_{DD} for D-Package -Expanded Detail-

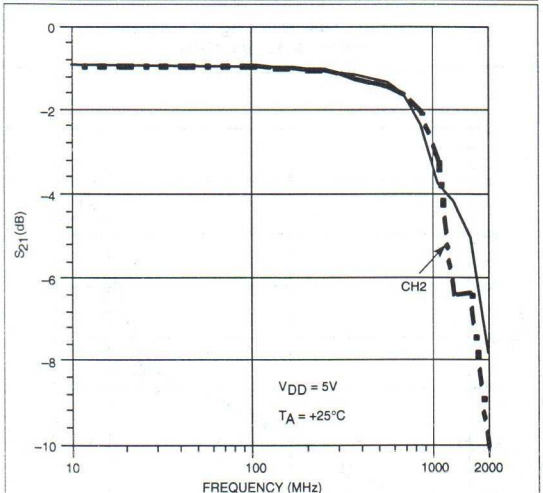


Figure 9. Loss Matching vs. Frequency for N-Package (DIP)

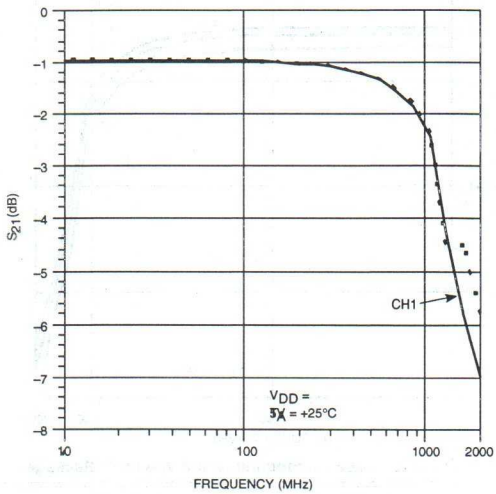


Figure 10. Loss Matching vs. Frequency; CH1 vs. CH2 for D-Pakage

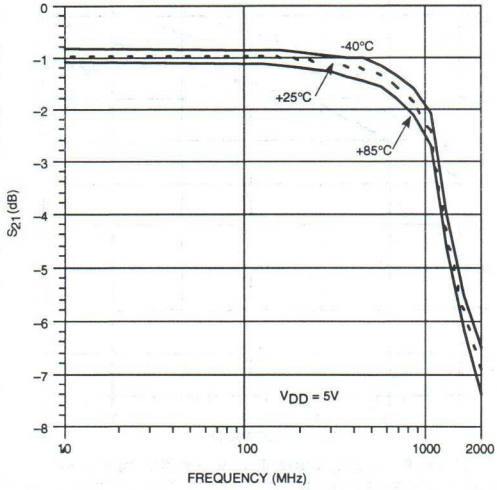


Figure 11. Loss vs. Frequency and Temperature for D-Package

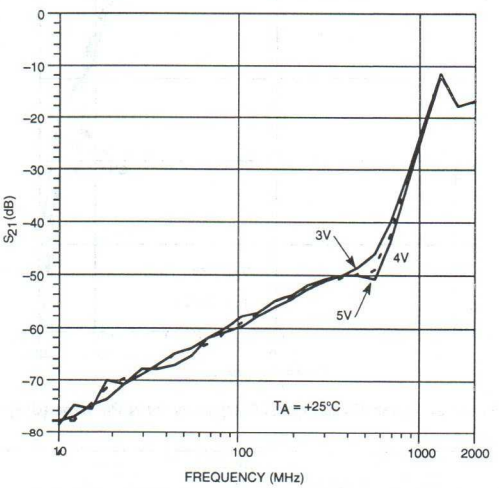


Figure 12. Isolation vs. Frequency and V_{DD} for D-Package

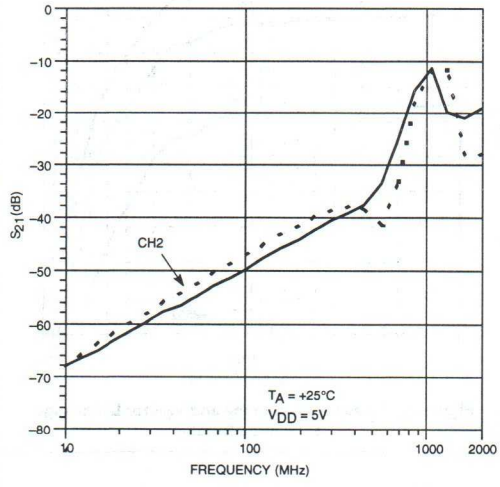


Figure 13. Isolation Matching vs. Frequency for N-Package (DIP)

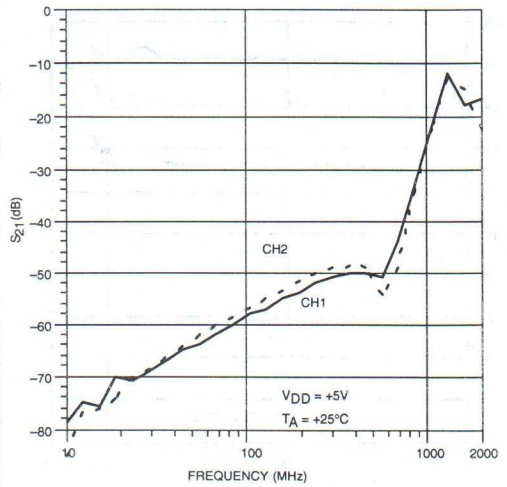


Figure 14. Isolation Matching vs. Frequency; CH1 vs. CH2 for D-Package

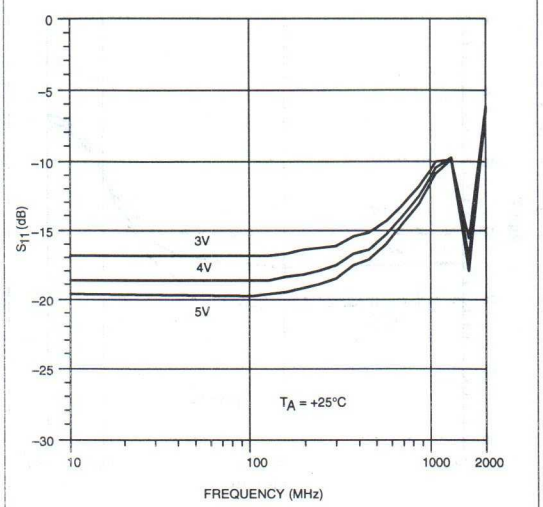


Figure 15. Input Match On-Channel vs. Frequency and V_{DD}

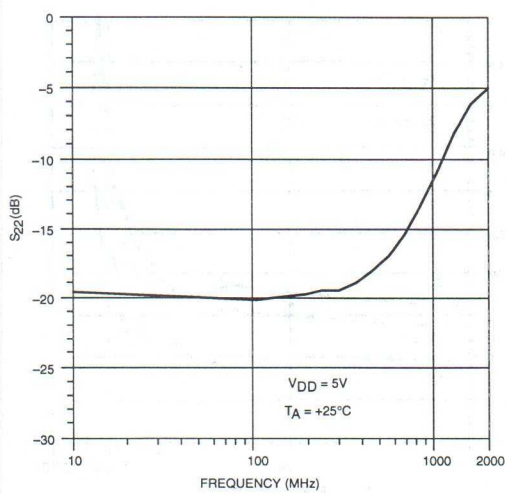


Figure 16. Output Match On-Channel vs. Frequency

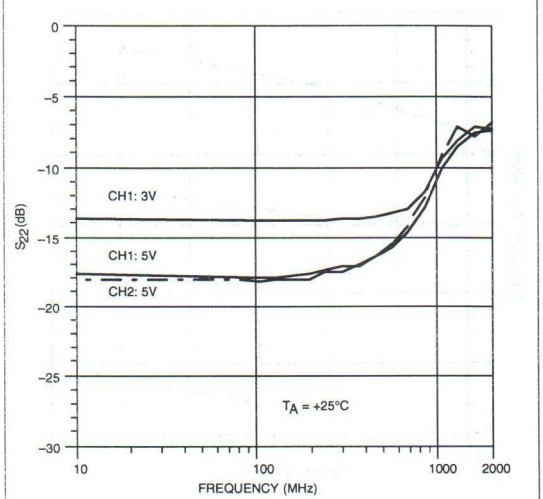


Figure 17. OFF-Channel Match vs. Frequency and V_{DD}

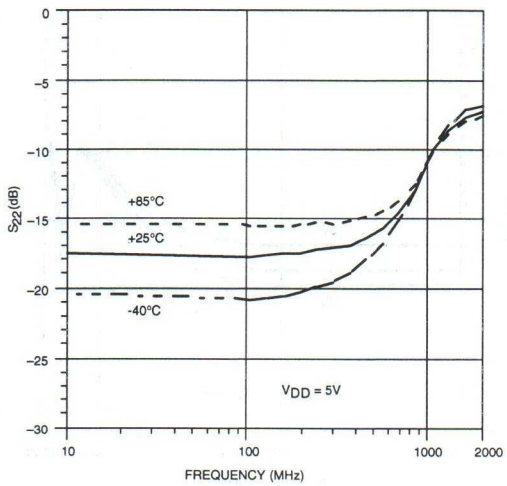


Figure 18. OFF Channel Match vs. Frequency and Temperature

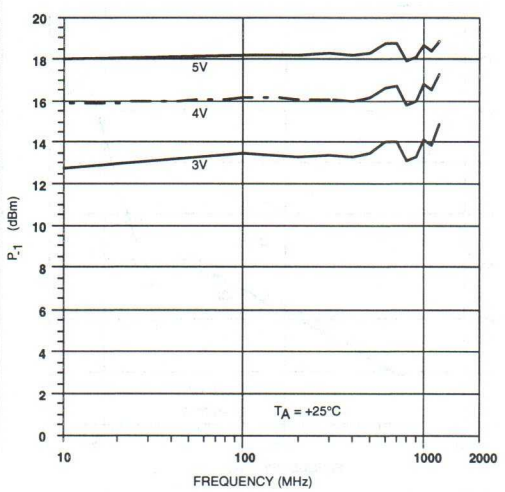


Figure 19. P_{-1} dB vs. Frequency and V_{DD}

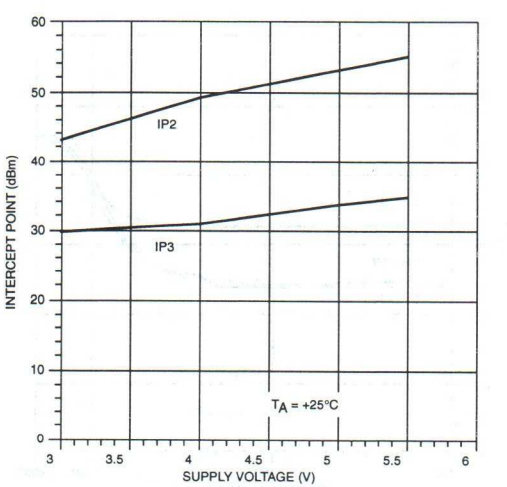


Figure 20. Intercept Points vs.V_{DD}

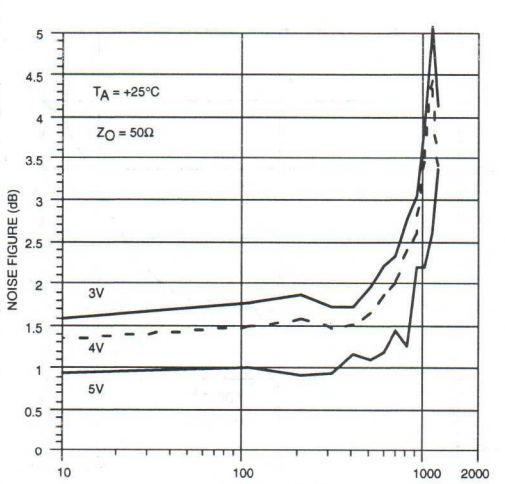


Figure 21. Noise Figure vs. Frequency and V_{DD} for D-Package

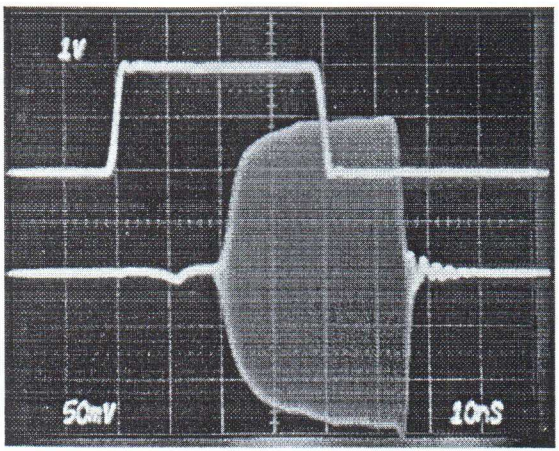


Figure 22. Switching Speed; f_{IN} = 100MHz at -6dBm, V_{DD} = 5V

Section 18
Package outlines

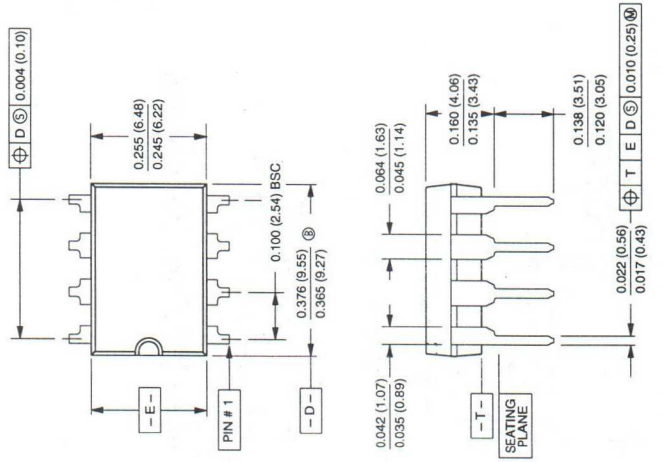
General Purpose/Linear ICs

INDEX

0404B	8-Pin (300 mils wide) Plastic Dual In-Line (N) Package	1281
0174C	8-Pin (157 mils wide) Plastic SO (Small Outline) Dual In-Line (D) Package	1282
0580A	8-Pin (300 mils wide) Ceramic Dual In-line (F) Package	1283
0405B	14-Pln (300 mils wide) Plastic Dual In-Line (N) Package	1284
0175D	14-Pin (157 mils wide) Plastic SO (Small Outline) Dual In-Line (D) Package	1285
0581B	14-Pin (300 mils wide) Ceramic Dual In-line (F) Package	1286
SOT38Z/0406C	16-Pin (300 mils wide) Plastic Dual In-Line (N) Package	1287
0171B	16-Pin (300 mils wide) Plastic SOL (Small Outline Large) Dual In-Line (D) Package	1288
0005D	16-Pin (157 mils wide) Plastic SO (Small Outline) Dual In-Line (D) Package	1289
0582B	16-Pin (300 mils wide) Ceramic Dual In-line (F) Package	1290
0407A	18-Pin (300 mils wide) Plastic Dual In-Line (N) Package	1291
0583A	18-Pin (300 mils wide) Ceramic Dual In-line (F) Package	1292
0408B	20-Pin (300 mils wide) Plastic Dual In-Line (N) Package	1293
0172D	20-Pin (300 mils wide) Plastic SOL (Small Outline Large) Dual In-Line (D) Package	1294
0584B	20-Pin (300 mils wide) Ceramic Dual In-line (F) Package (with Window (FA) Package)	1295
0409B	22-Pin (400 mils wide) Plastic Dual In-Line (N) Package	1296
0585B	22-Pin (400 mils wide) Ceramic Dual In-line (F) Package	1297
SOT101/0410D	24-Pin (300 mils wide) Plastic Dual In-Line (N) Package	1298
0411B	24-Pin (400 mils wide) Plastic Dual In-Line (N) Package	1299
0412A	24-Pin (600 mils wide) Plastic Dual In-Line (N) Package	1300
0173D	24-Pin (300 mils wide) Plastic SOL (Small Outline Large) Dual In-Line (D) Package	1301
0586B	24-Pin (300 mils wide) Ceramic Dual In-line (F) Package (with Window (FA) Package)	1302
0587D	24-Pin (400 mils wide) Ceramic Dual In-line (F) Package	1303
0588B	24-Pin (600 mils wide) Ceramic Dual In-line (F) Package (with Window (FA) Package)	1304
0864D	28-Pin (300 mils wide) Plastic Dual In-Line (N) Package	1305
0413B	28-pin (600 mils wide) Plastic Dual In-Line (N) Package	1306
SOT261/0401F	28-Pin (300 mils wide) Plastic Leaded Chip Carrier (A) Package	1307
SOT97-1	Plastic dual in-line package; 8 leads	1308
SOT96-1	Plastic small outline package; 8 leads	1309
SOT110B	9-Pin Plastic Single In-Line (U) Package	1310
SOT162-1	Plastic small outline package; 16 leads; large body	1311
SOT38-1	Plastic dual in-line package; 16 leads (300 mil)	1312
SOT74	16-Lead dual in-line; ceramic (cerdip)	1313
SOT102	18-Pin Plastic Dual In-Line (N/P) Package with Internal Heatspreader	1314
SOT146-1	Plastic dual in-line package; 20 leads (300 mil)	1315
SOT163-1	Plastic small outline package; 20 leads; large body (SO20L)	1316
SOT101	24-Pin Plastic Dual In-Line (N/P) Package with Internal Heatspreader	1317
SOT137-1	Plastic small outline package; 24 leads; large body	1318
SOT117-1	Plastic dual in-line package; 28 leads (600 mil) with internal heat spreader	1319
SOT136–1	Plastic small outline package; 28 leads; large body	1320
SOT232-1	Plastic shrink dual in-line package; 32 leads (400 mil)	1321

Package outlines

0404B 8-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



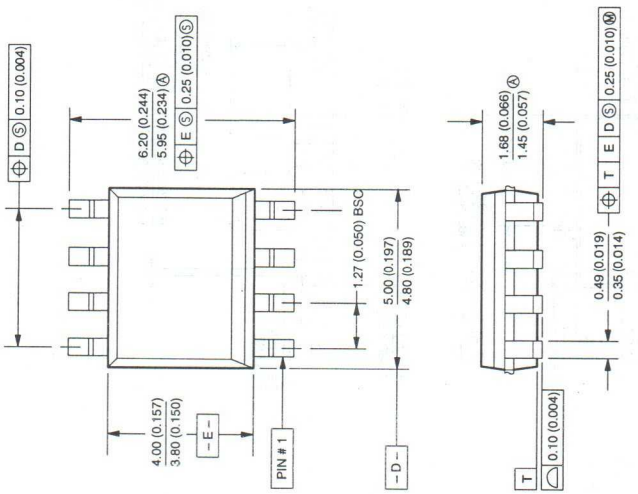
NOTES

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AB for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 8 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #8 when viewed from the top.

853–0404B 07236

Package outlines

0174C 8-PIN (157 mils wide) PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D) PACKAGE



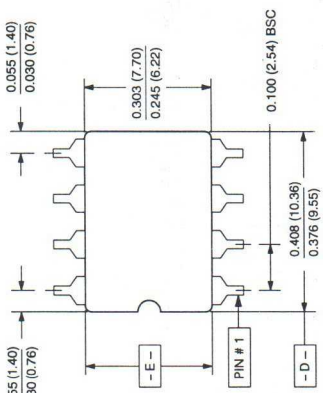
NOTES

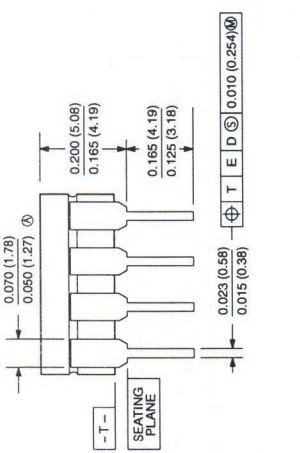
1. Package dimensions conform to JEDEC Specification MS-012-AA for standard Small Outline (SO) package, 8 leads, 3.75mm (0.150") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "D" and "E" are reference datums on the molded body and do not include mold flash/protrusions. Mold flash/protrusions at "D" shall not exceed 0.15mm (0.006") per side. Inter-lead flash/protrusions at "E" shall not exceed 0.25mm (0.010") per side.
5. The lead width above the seating plane shall not exceed a maximum value of 0.61mm (0.024").
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #8 when viewed from top.
7. Signetics ordering code for a product packages in a plastic Small Outline (SO) package is the suffix D after the product number.

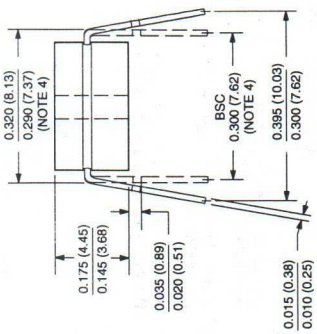
853–0174C 04697

Package outlines

0580A 8-PIN (300 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE







NOTES:

1. Controlling dimension: Inches. Millimeters are shown in parentheses.
2. Dimension and tolerancing per ANSI Y14. 5M-1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #8 when viewed from the top.

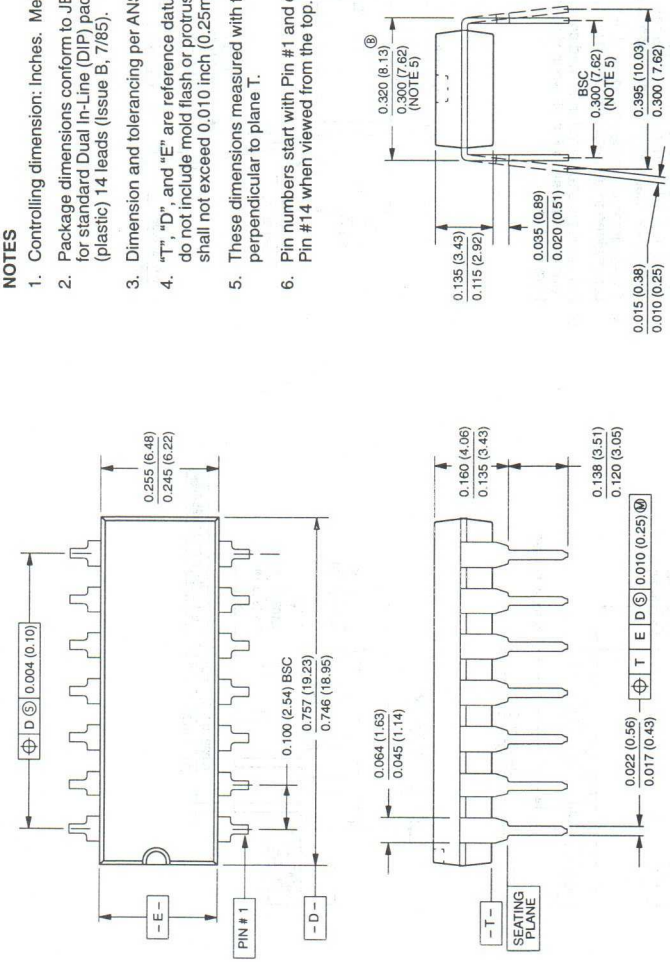
853–0580A 006688

Package outlines

0405B 14-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE

NOTES

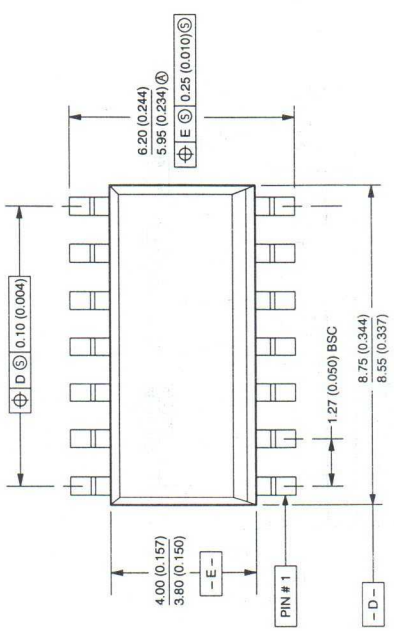
1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AC for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 14 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #14 when viewed from the top.

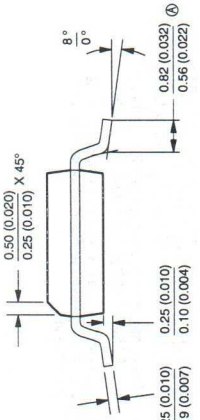


853–0405B 02880

Package outlines

0175D 14-PIN (157 mils wide) PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D) PACKAGE





NOTES

1. Package dimensions conform to JEDEC Specification MS-012-AB for standard Small Outline (SO) package, 14 leads, 3.75mm (0.150") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "D" and "E" are reference datums on the molded body and do not include mold flash/protrusions. Mold flash/protrusions at "D" shall not exceed 0.15mm (0.006") per side. Inter-lead flash/protrusions at "E" shall not exceed 0.25mm (0.010") per side.
5. The lead width above the seating plane shall not exceed a maximum value of 0.61mm (0.024").
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #14 when viewed from the top.
7. Signetics ordering code for a product packages in a plastic Small Outline (SO) package is the suffix D after the product number.

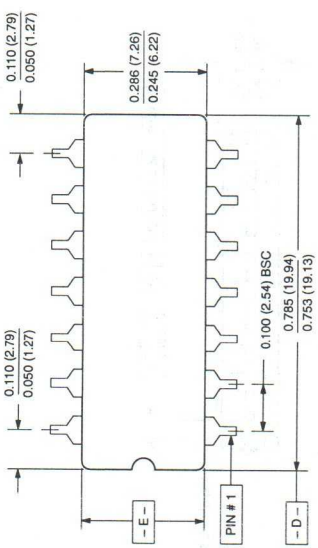
853–0175D 04697

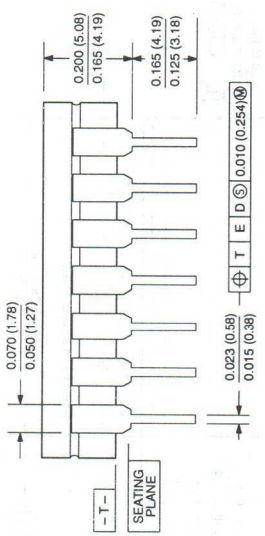
Package outlines

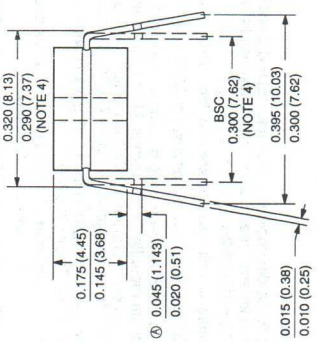
0581B 14-PIN (300 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE

NOTES:

1. Controlling dimension: Inches. Millimeters are shown in parentheses.
2. Dimension and tolerancing per ANSI Y14. 5M-1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #14 when viewed from the top.



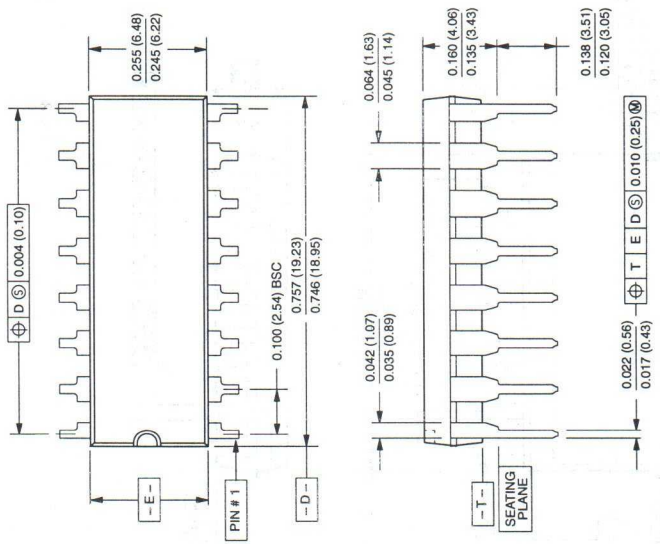




853-0581B 06688

Package outlines

SOT38Z/0406C 16-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



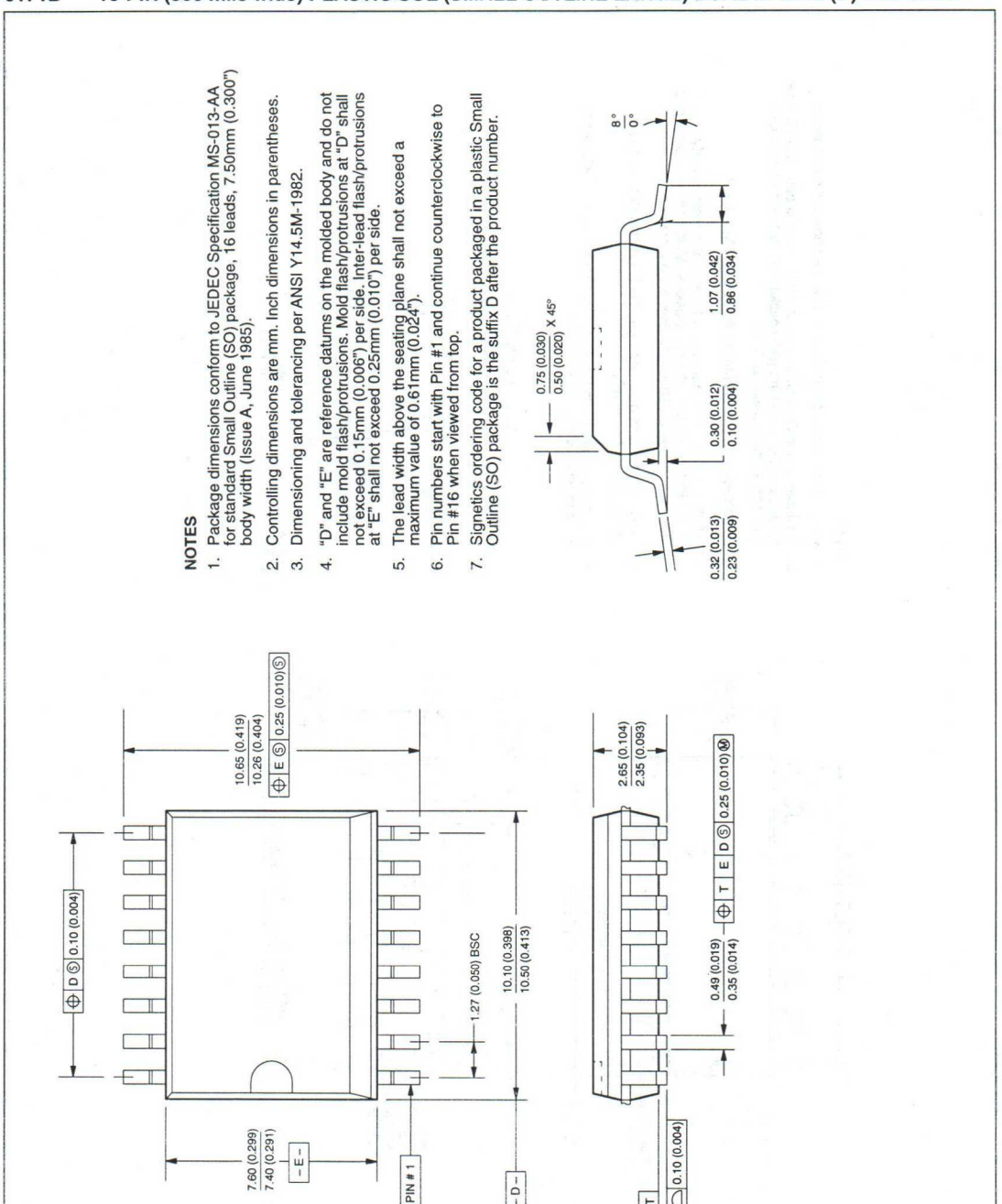
NOTES

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AA for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 16 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #16 when viewed from the top.

853–0406C 02880

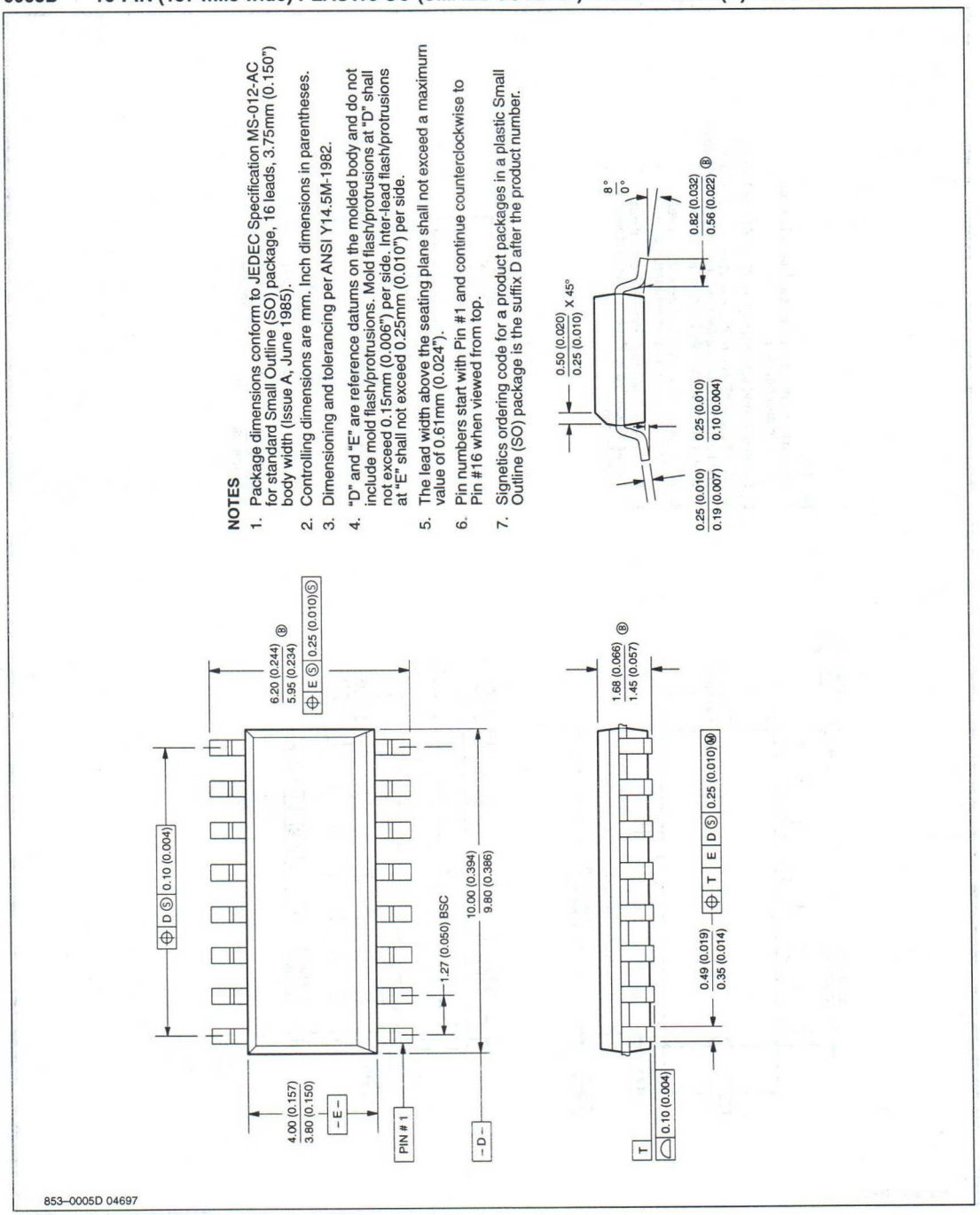
Package outlines

0171B 16-PIN (300 mils wide) PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE



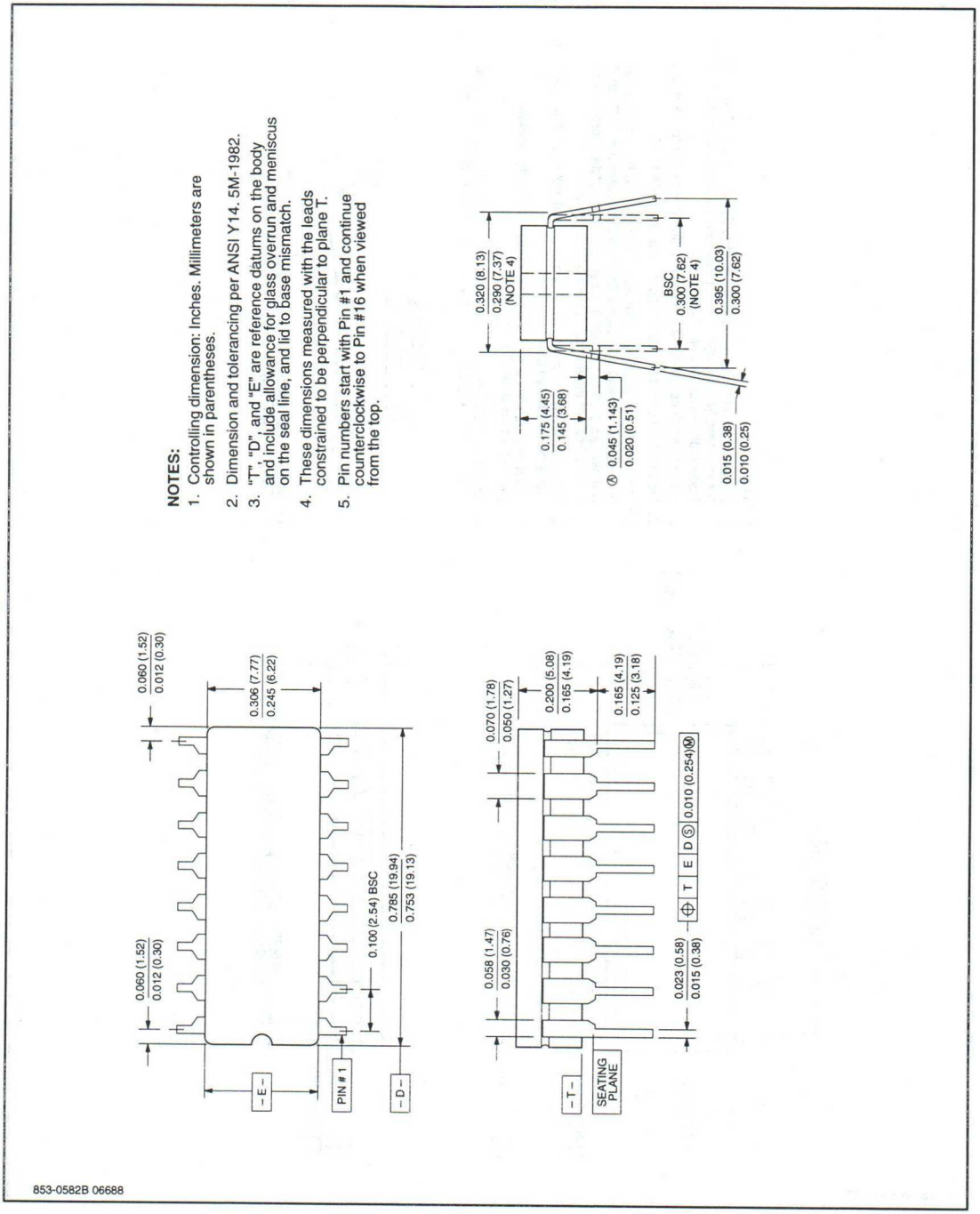
Package outlines

0005D 16-PIN (157 mils wide) PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D) PACKAGE



Package outlines

0582B 16-PIN (300 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE

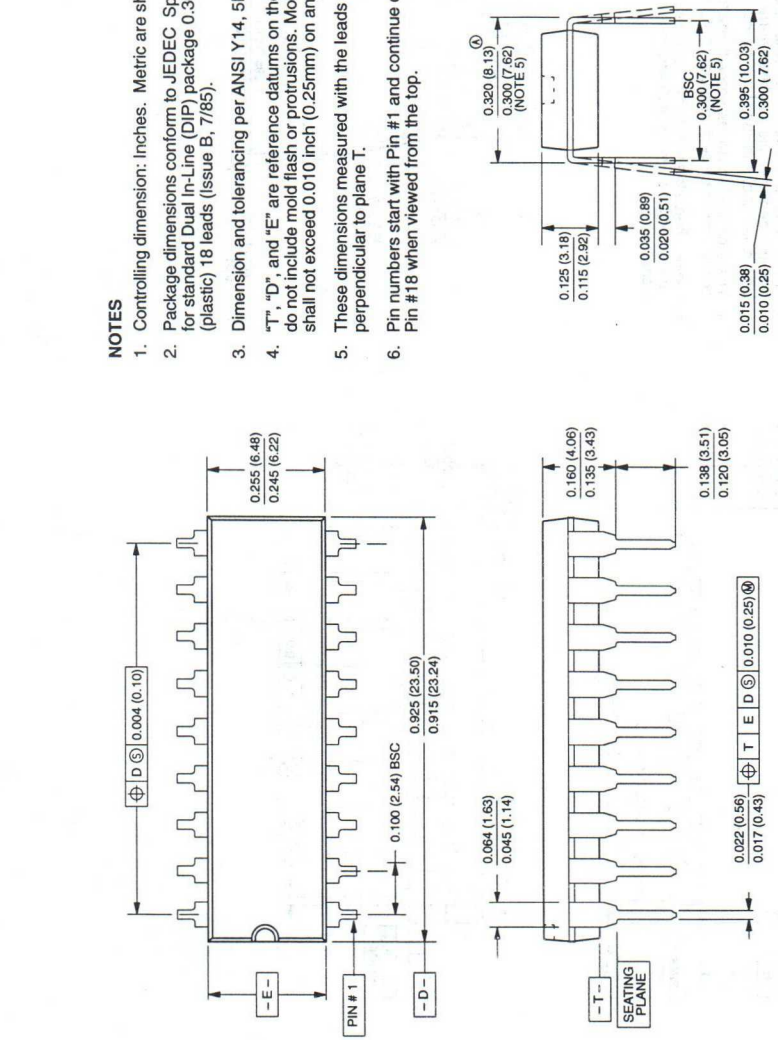


Package outlines

0407A 18-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE

NOTES

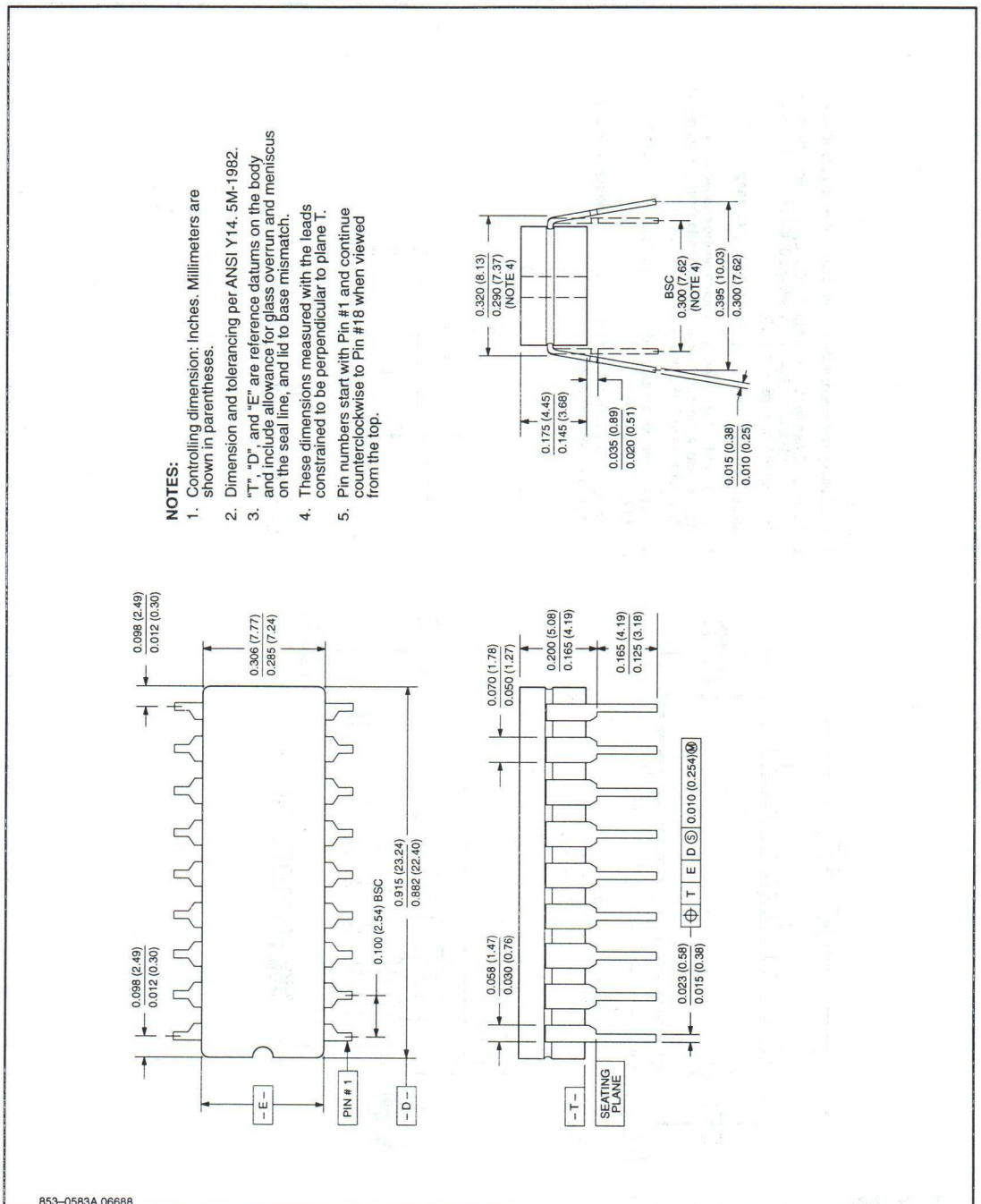
1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AD for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 18 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #18 when viewed from the top.



853–0407A 02880

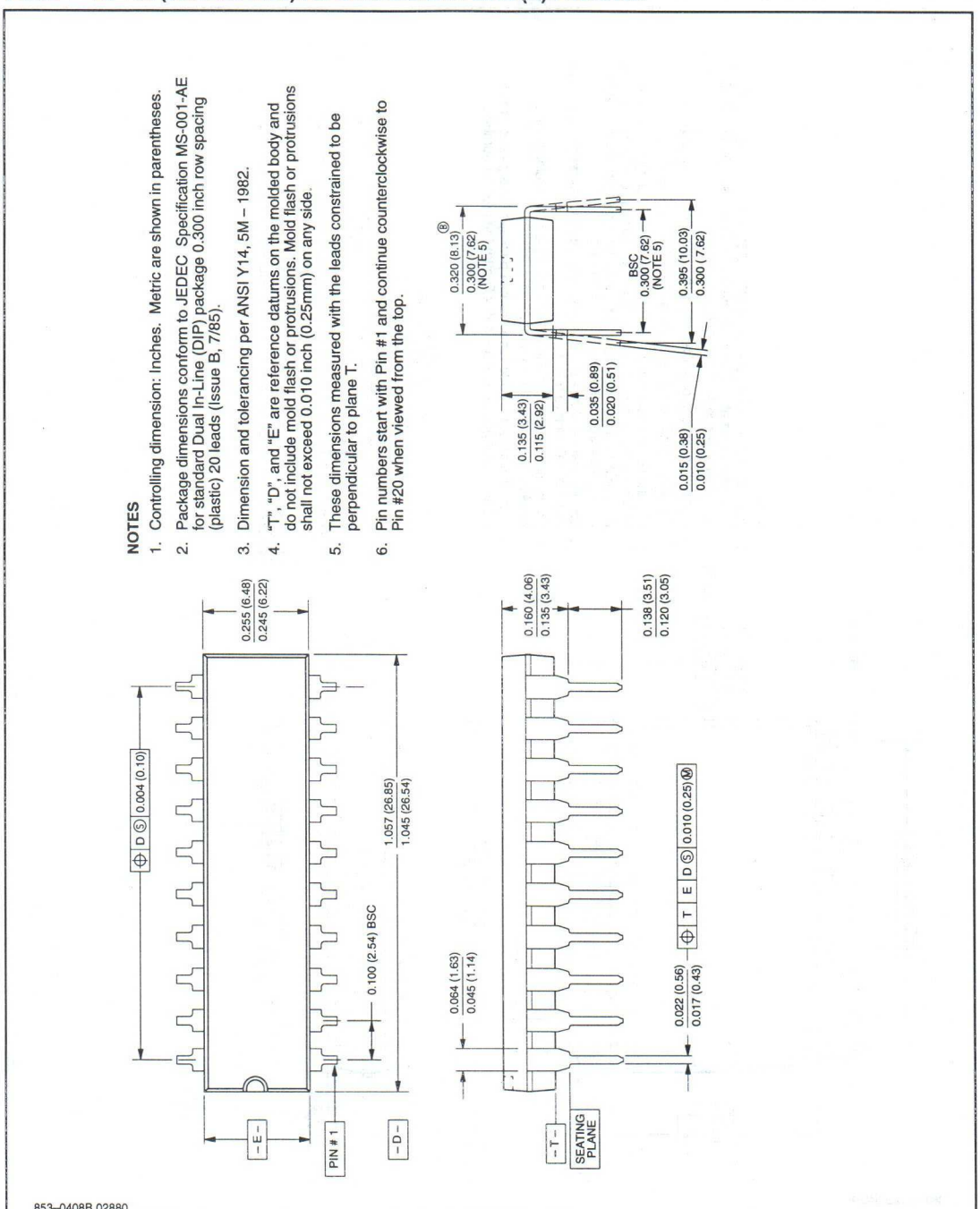
Package outlines

0583A 18-PIN (300 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE



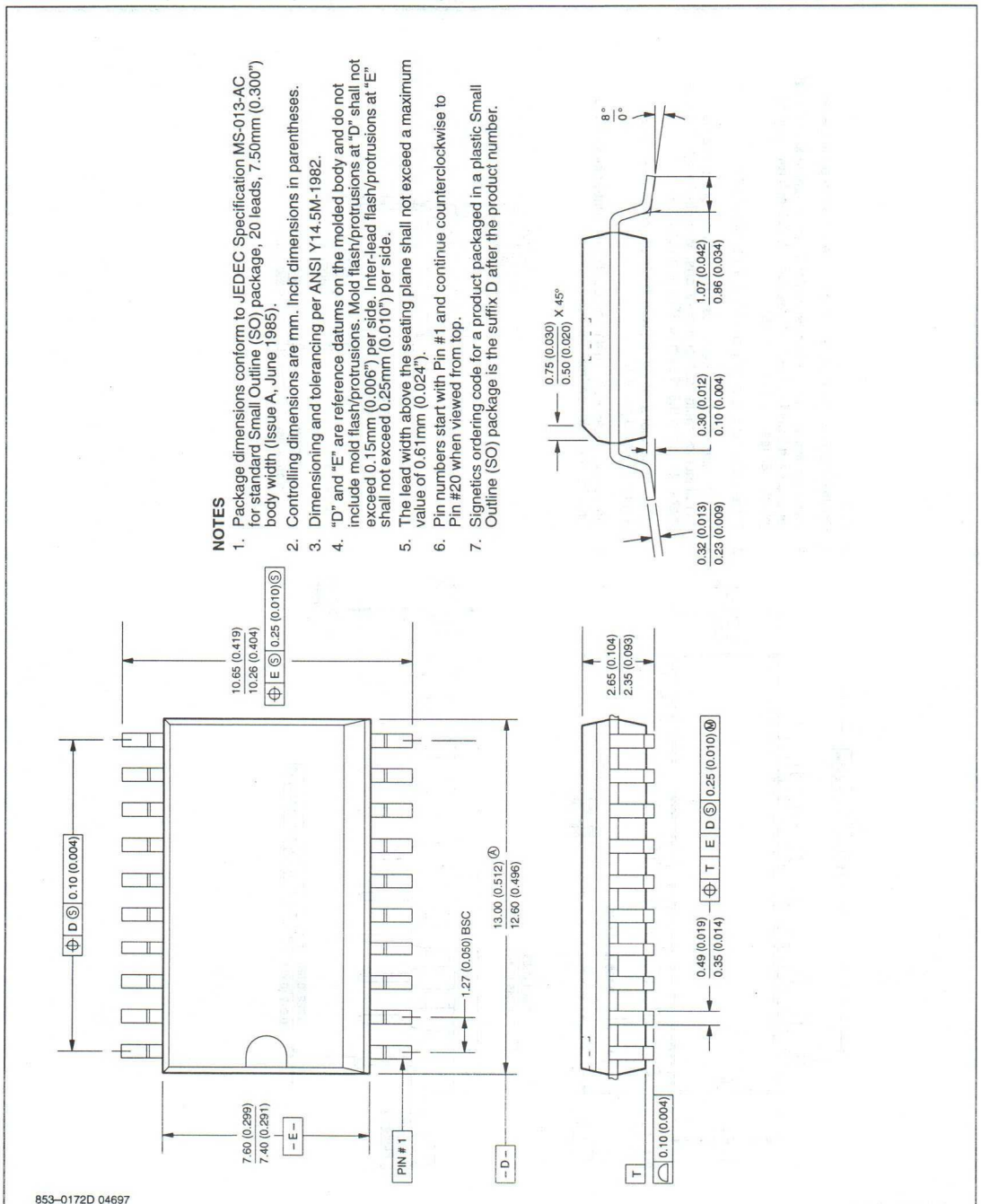
Package outlines

0408B 20-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



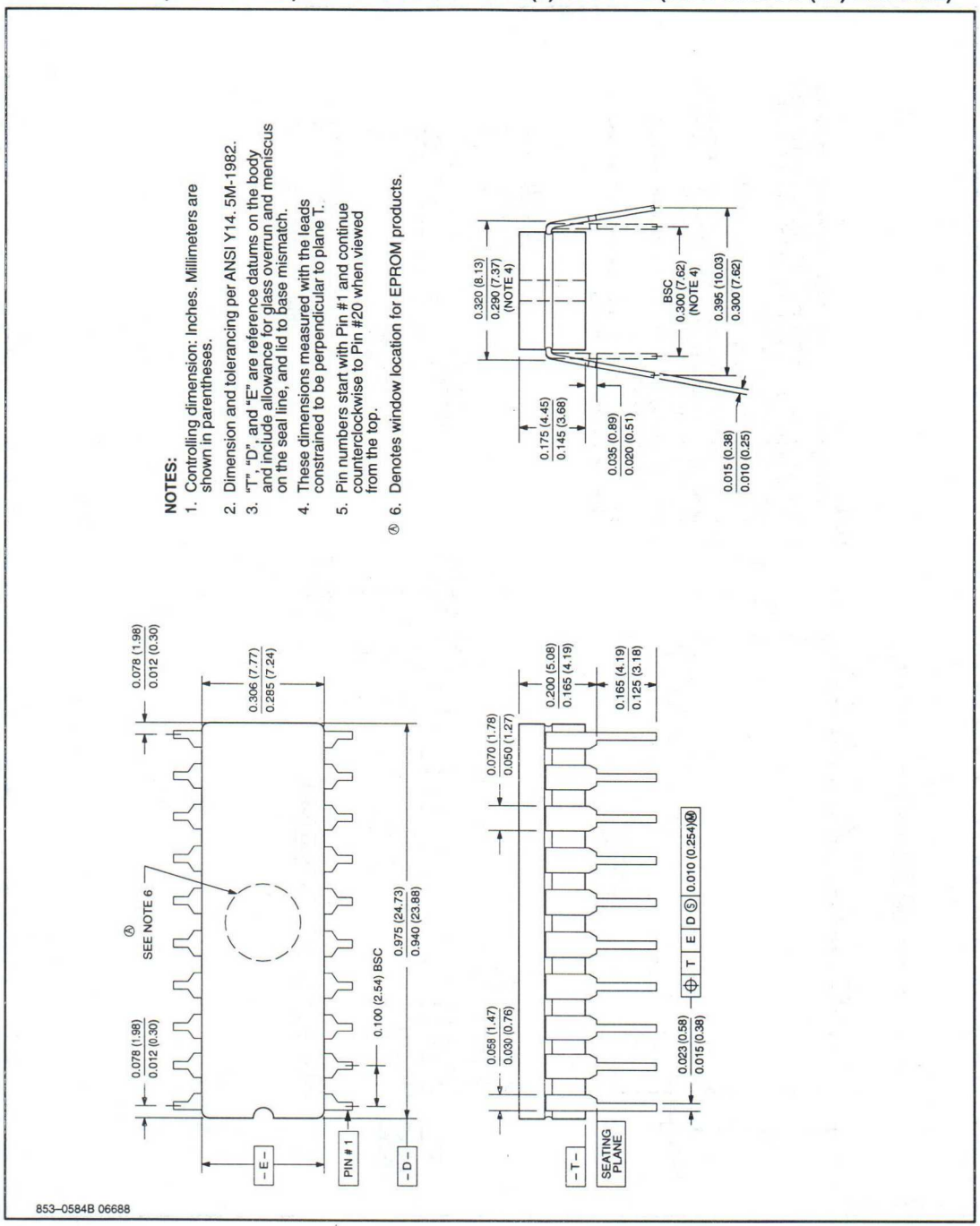
Package outlines

0172D 20-PIN (300 mils wide) PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE



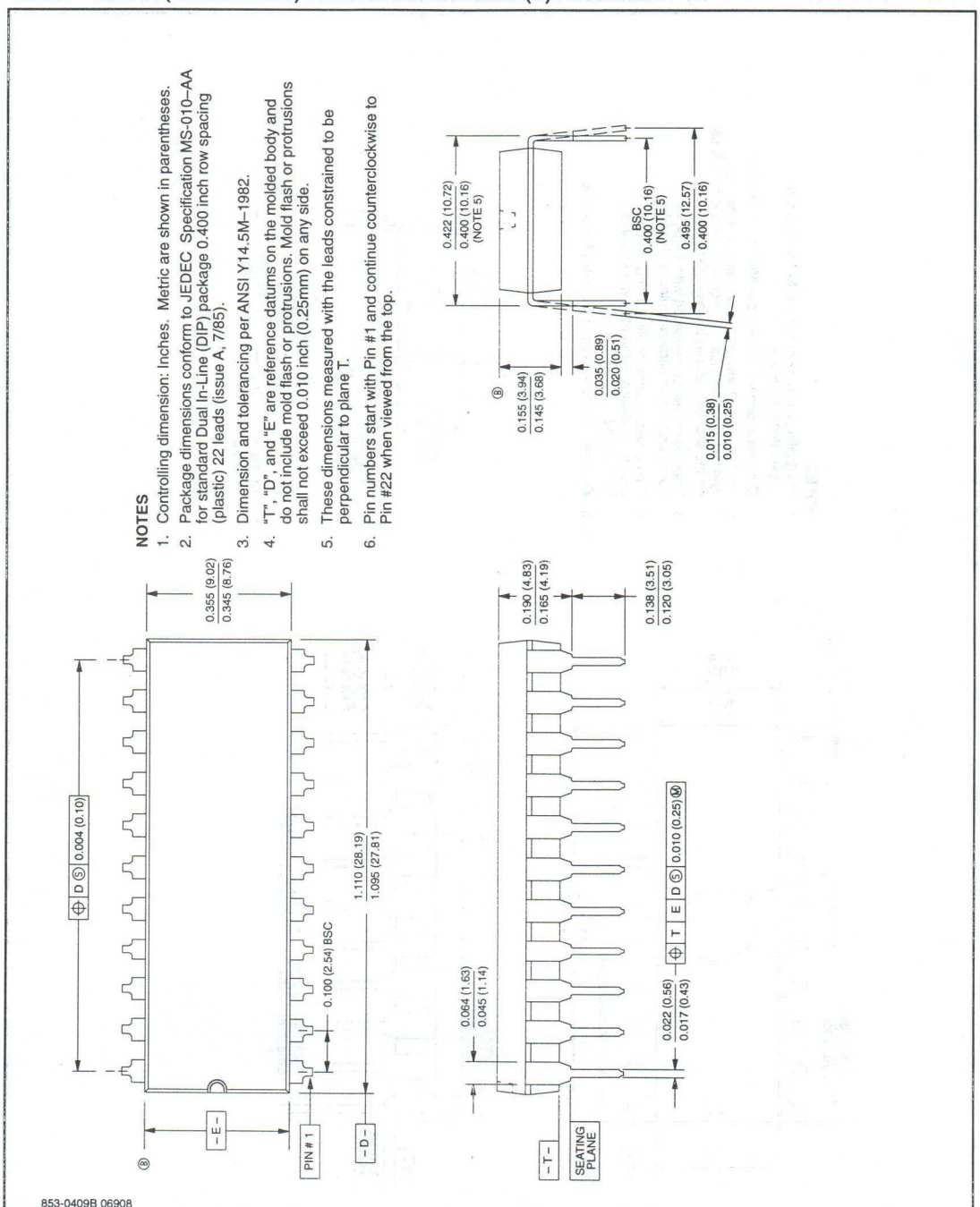
Package outlines

0584B 20-PIN (300 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE (WITH WINDOW (FA) PACKAGE)



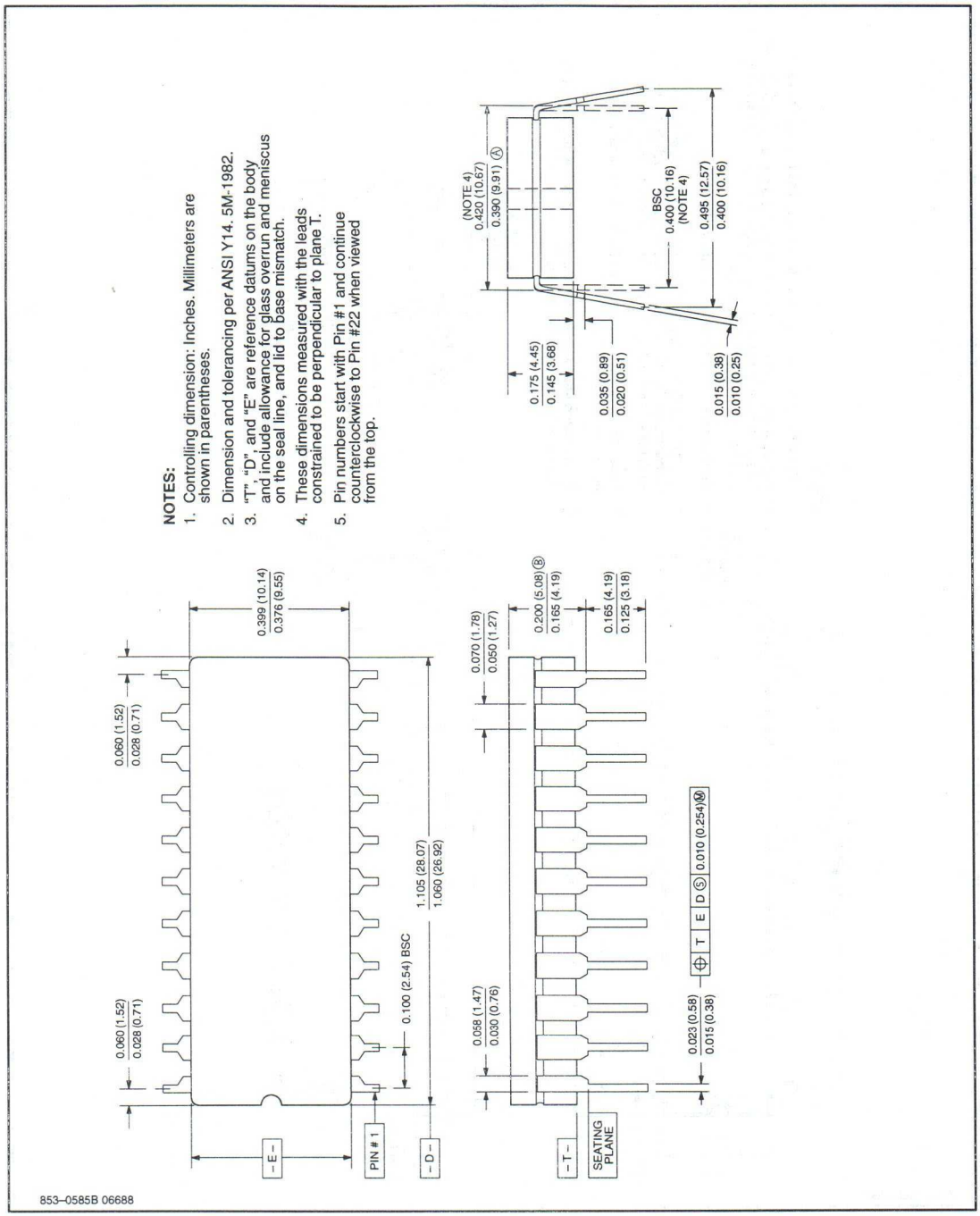
Package outlines

0409B 22-PIN (400 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



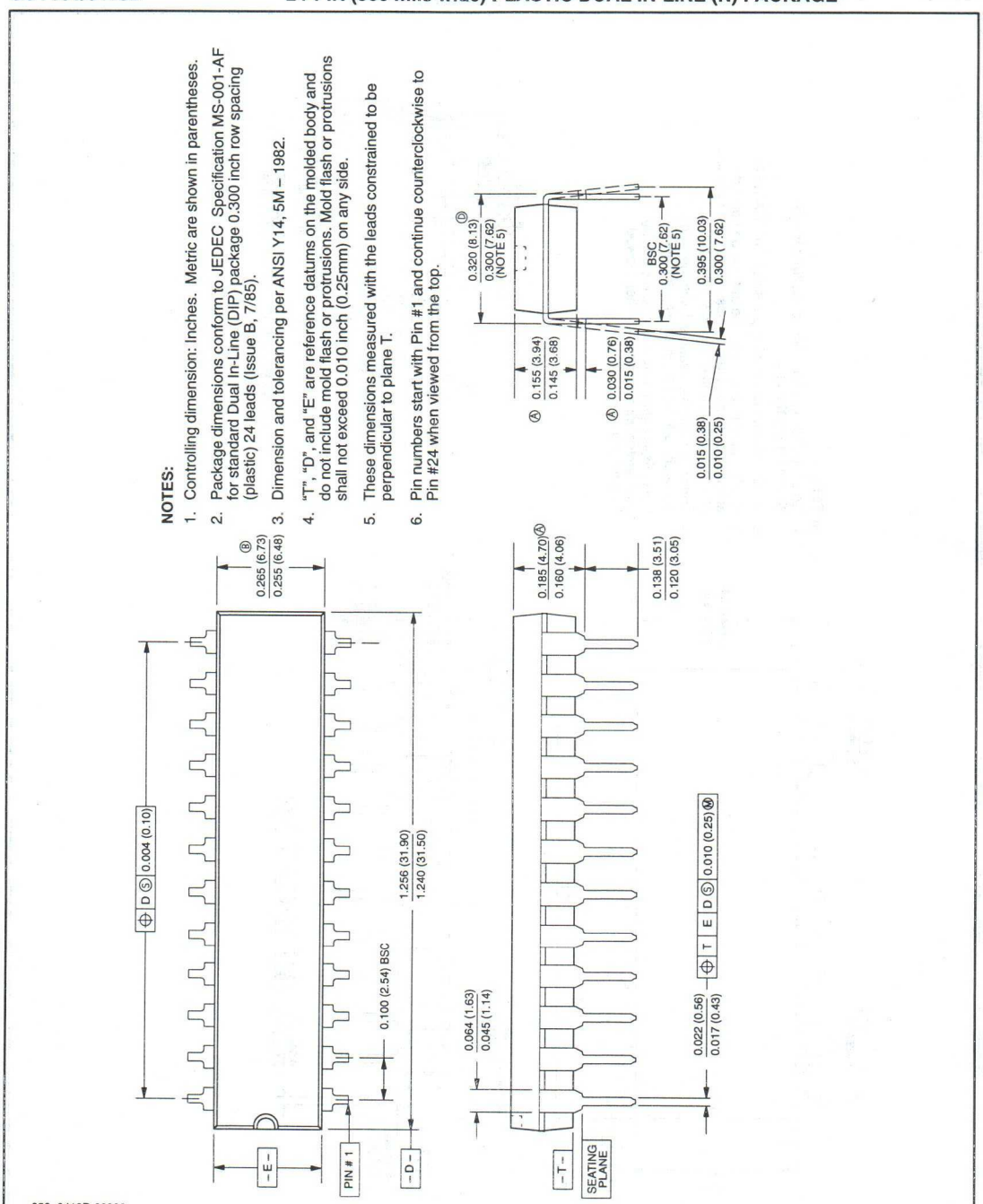
Package outlines

0585B 22-PIN (400 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE



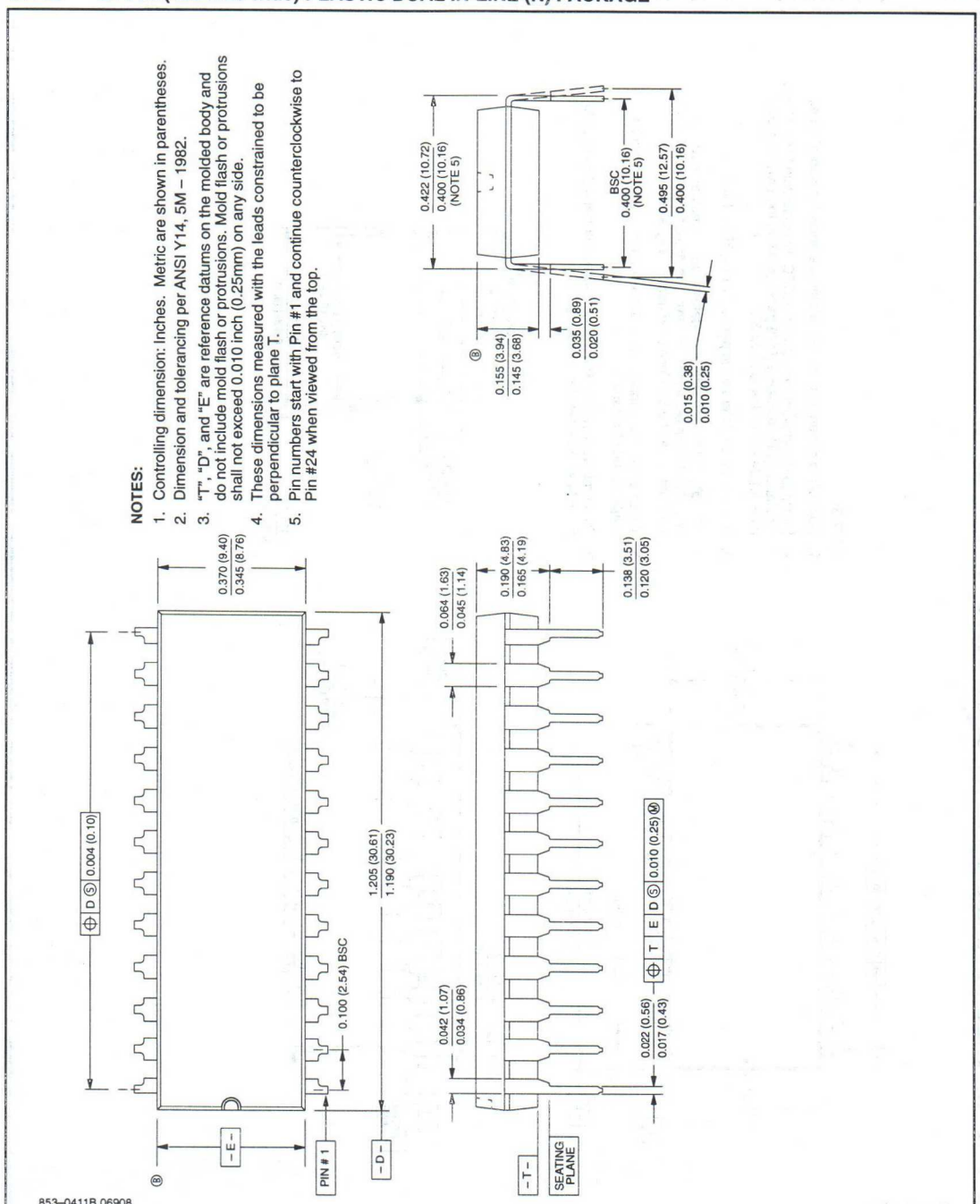
Package outlines

SOT101/0410D 24-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



Package outlines

0411B 24-PIN (400 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE

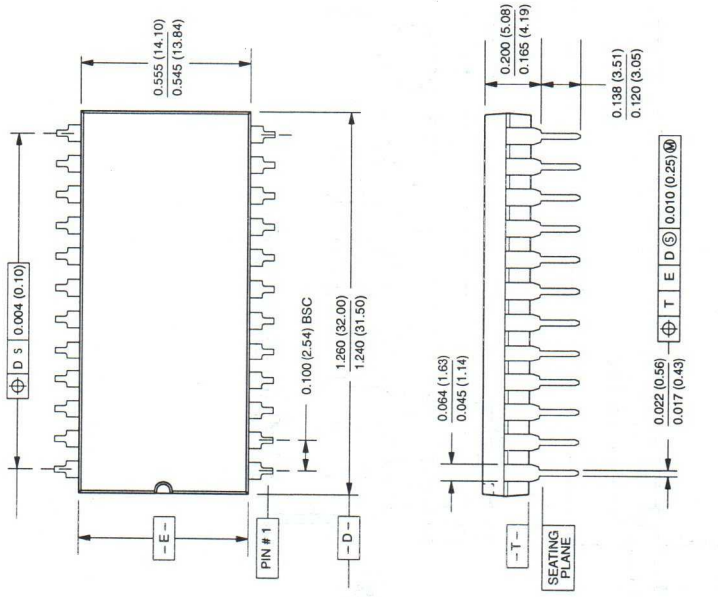


Package outlines

0412A 24-PIN (600 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE

NOTES:

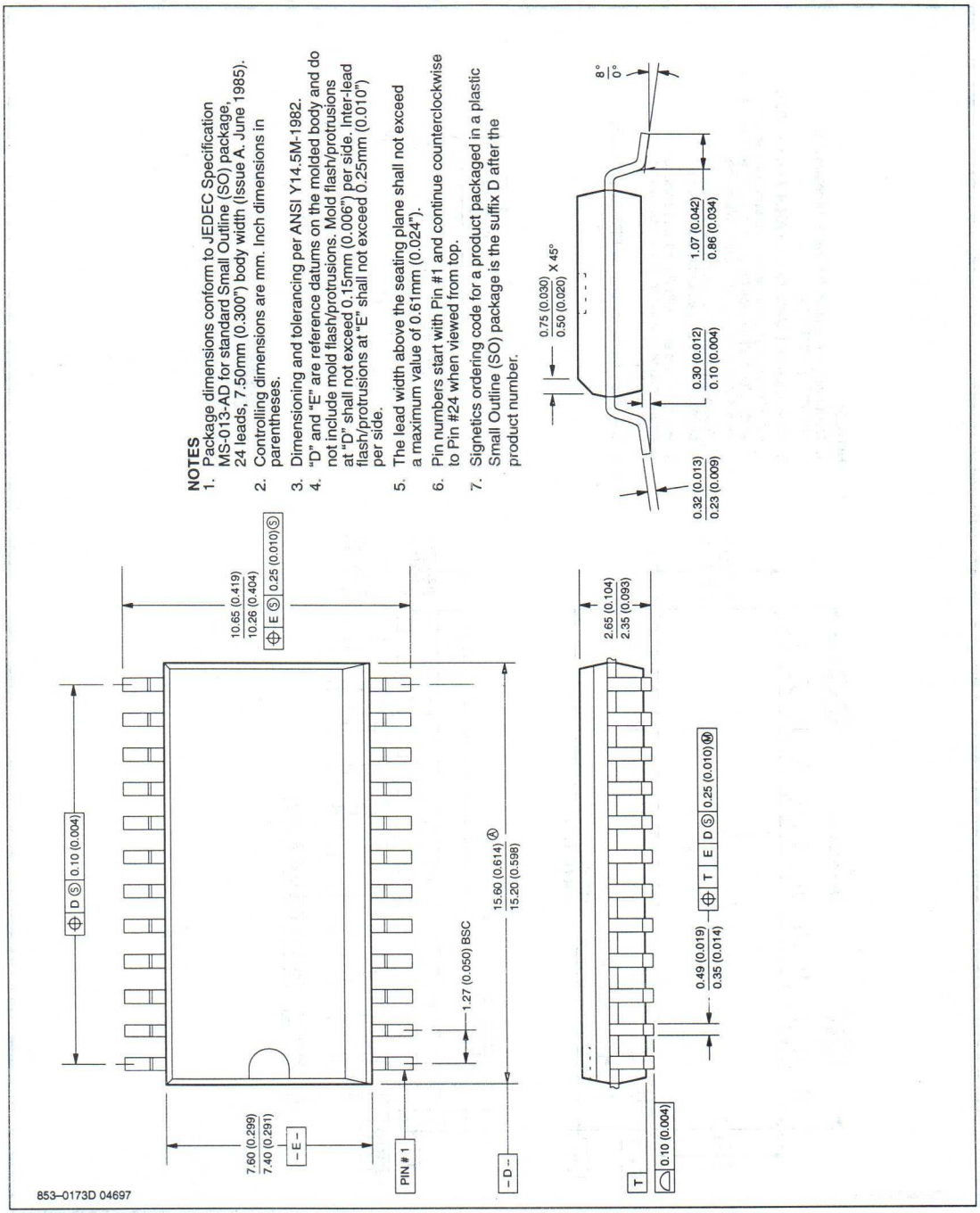
1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-011-AA for standard Dual In-Line (DIP) package 0.600 inch row spacing (plastic) 24 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #24 when viewed from the top.



853–0412A 02880

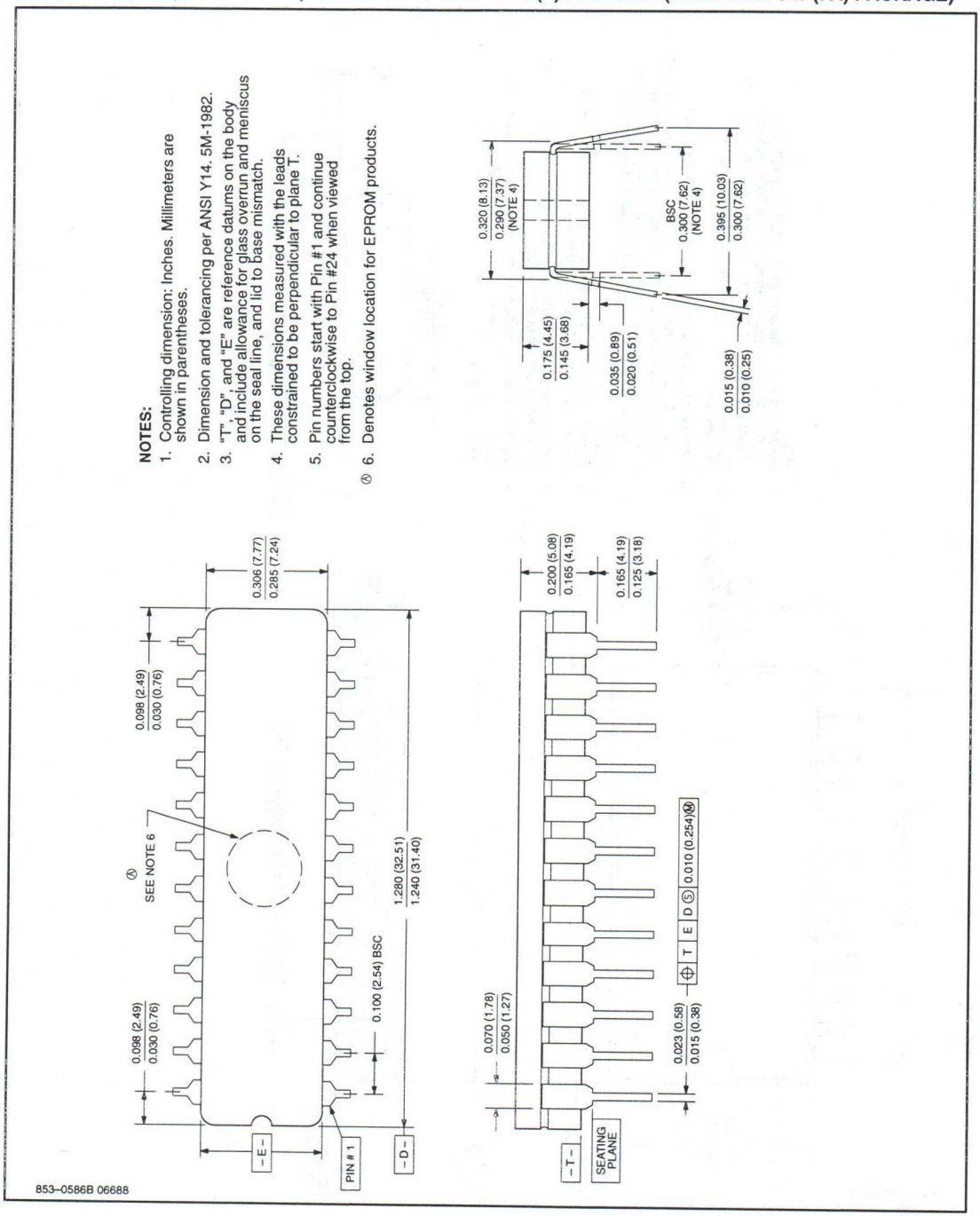
Package outlines

0173D 24-PIN (300 mils wide) PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE



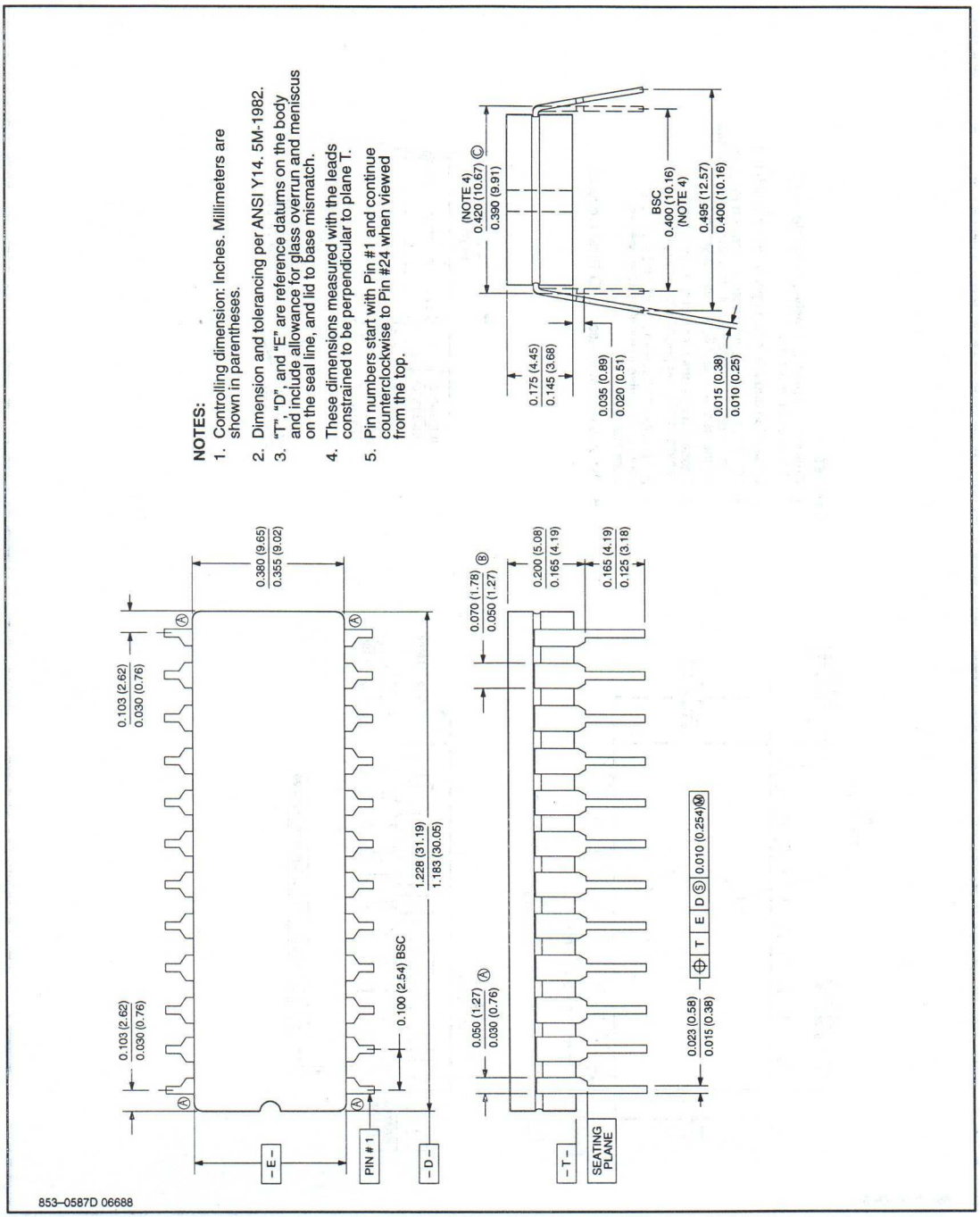
Package outlines

0586B 24-PIN (300 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE (WITH WINDOW (FA) PACKAGE)



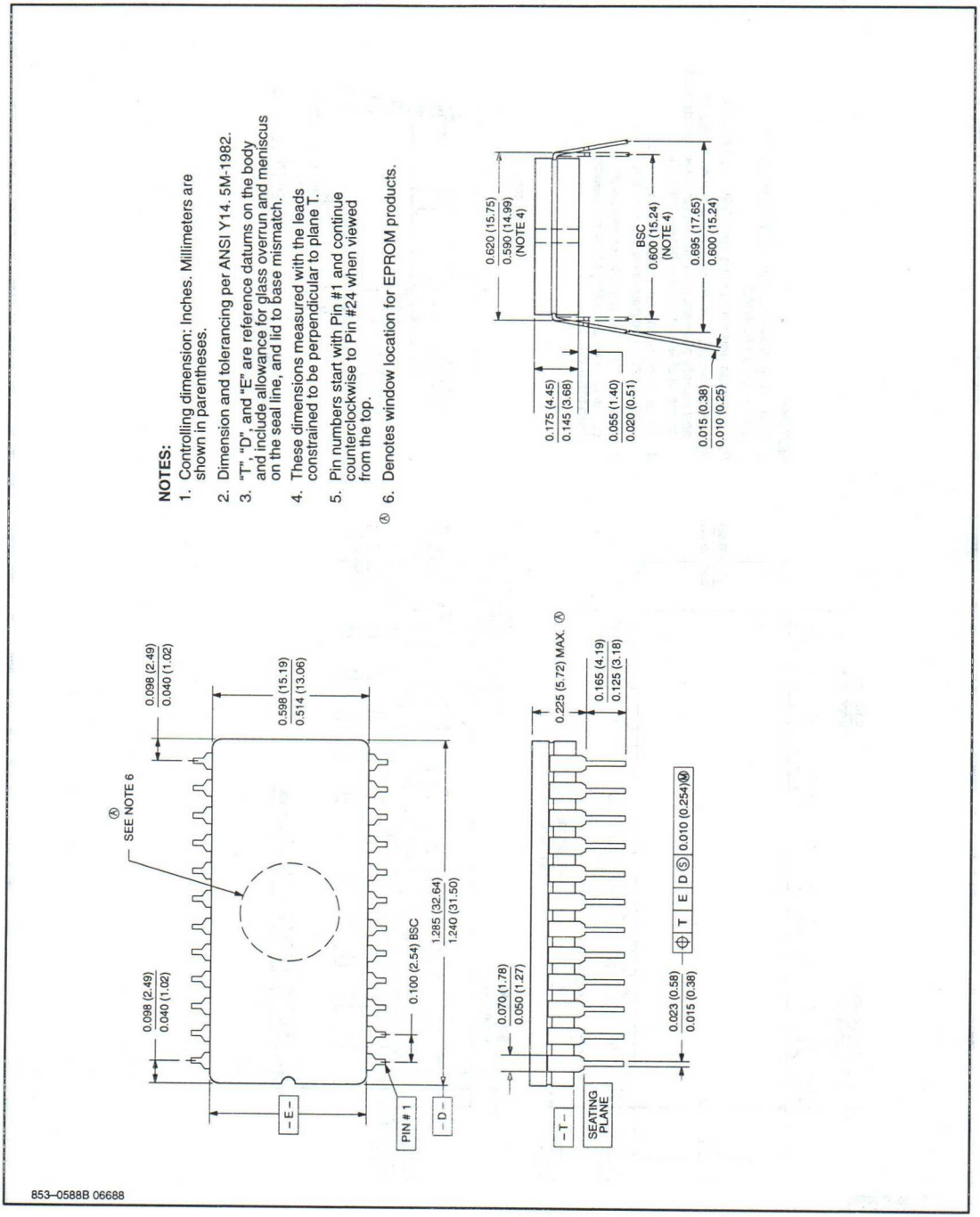
Package outlines

0587D 24-PIN (400 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE



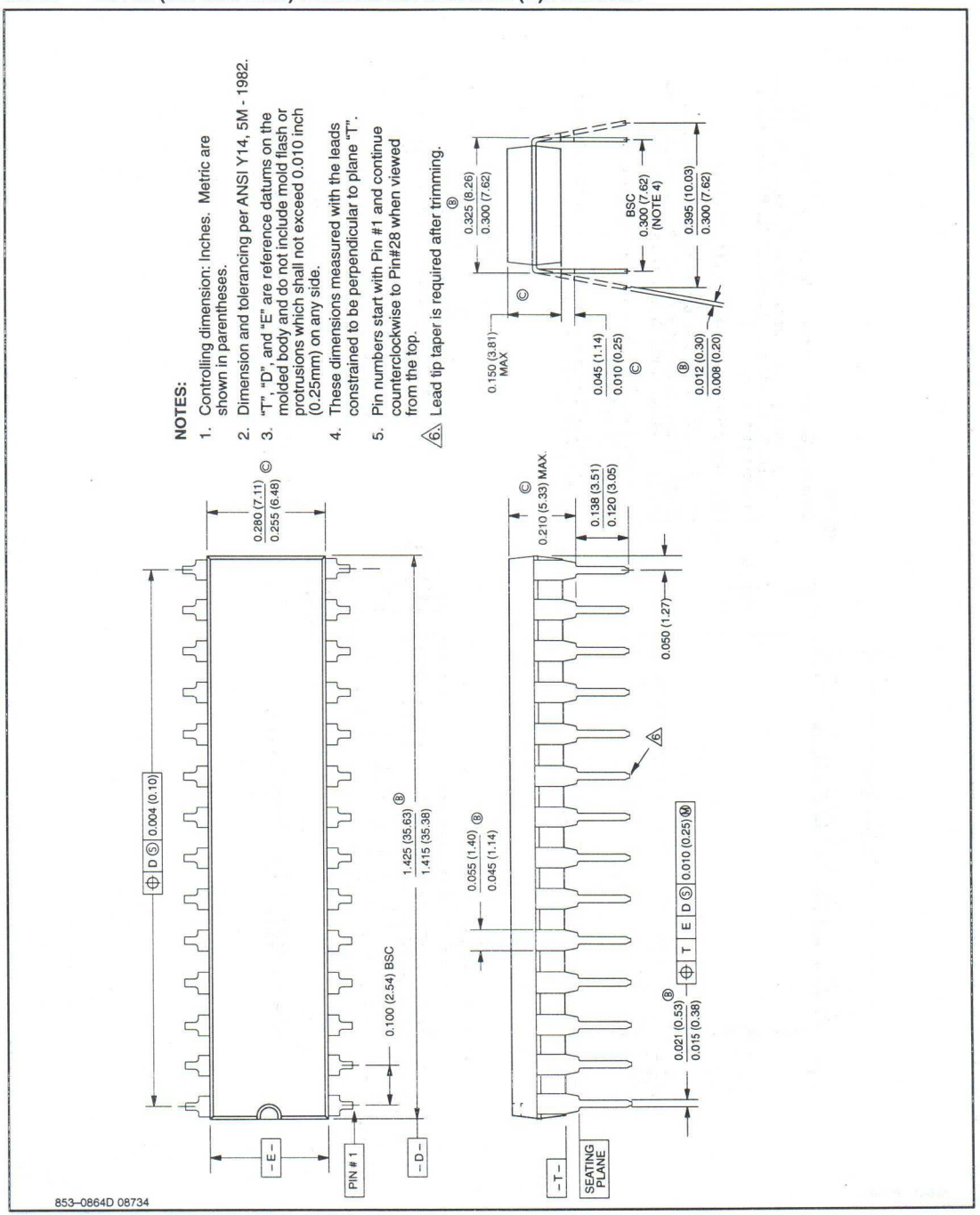
Package outlines

0588B 24-PIN (600 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE (WITH WINDOW (FA) PACKAGE)



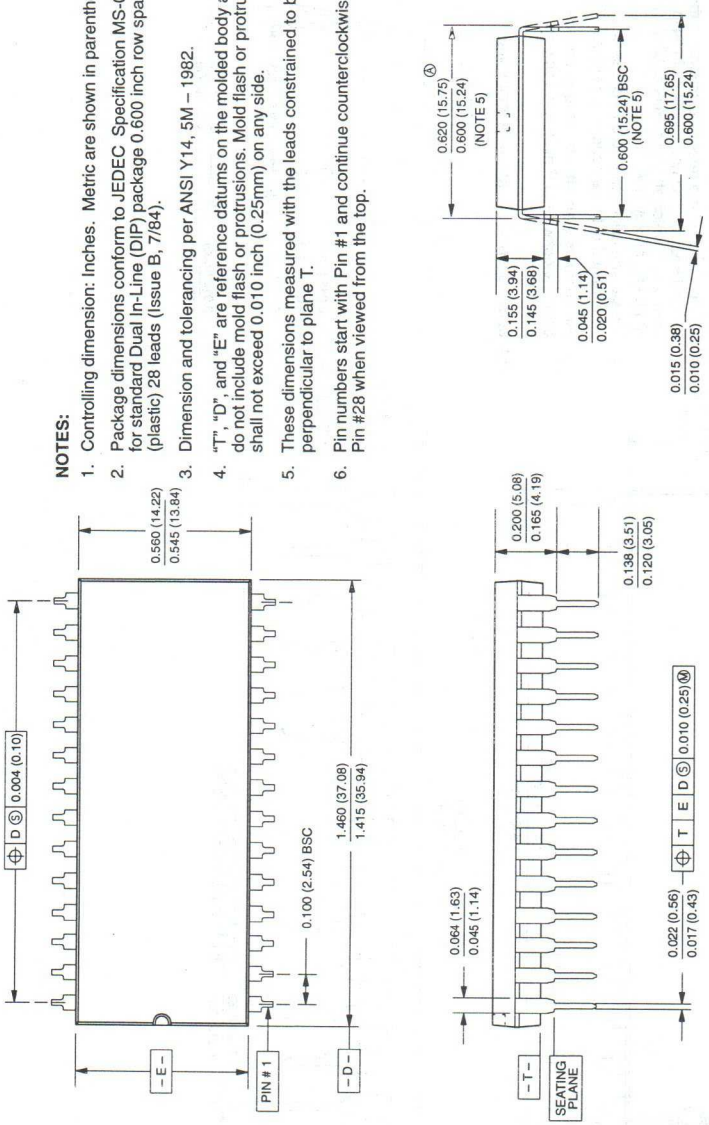
Package outlines

0864D 28-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



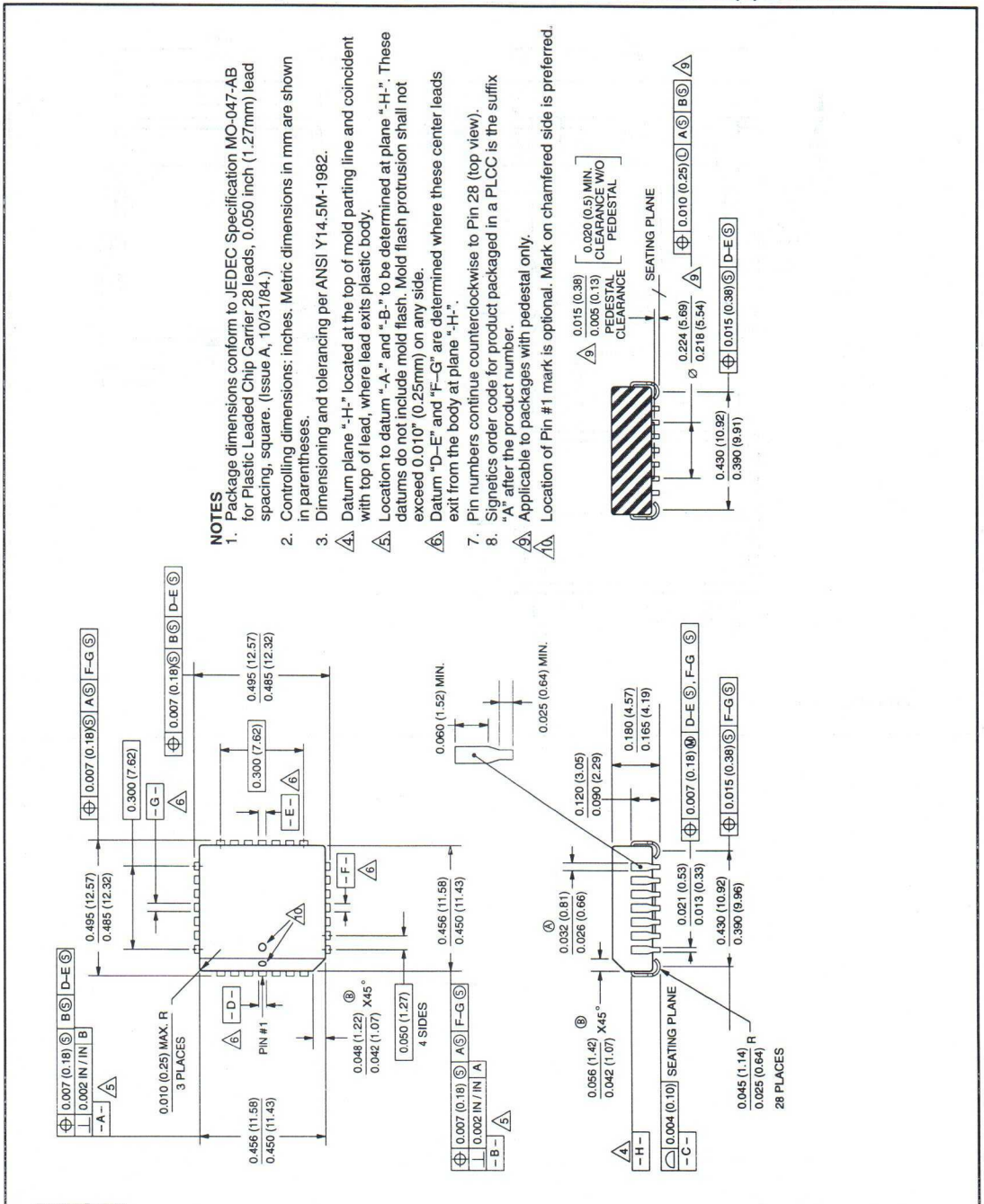
Package outlines

0413B 28-PIN (600 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



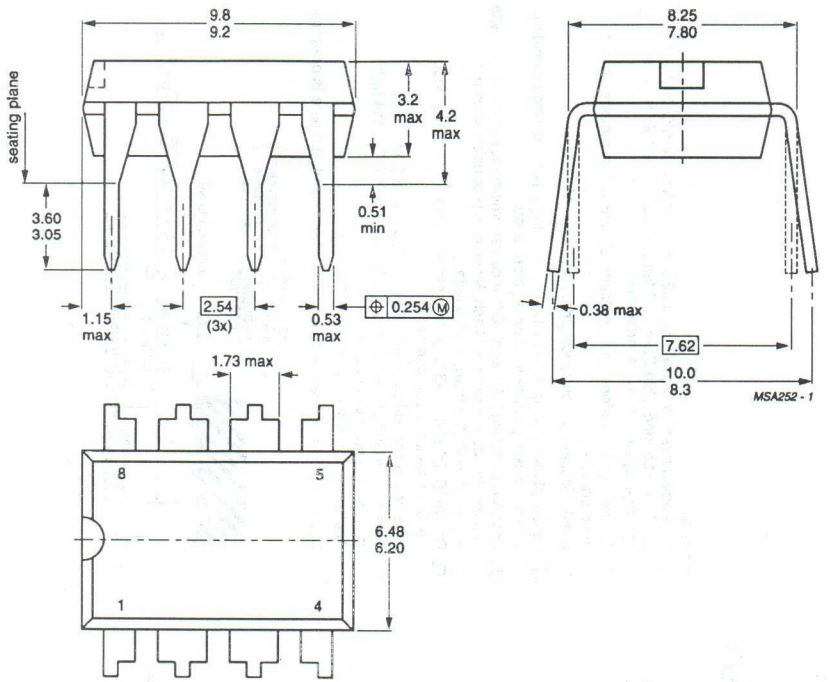
Package outlines

SOT261/0401F 28-PIN (300 mils wide) PLASTIC LEADED CHIP CARRIER (A) PACKAGE



Package outlines

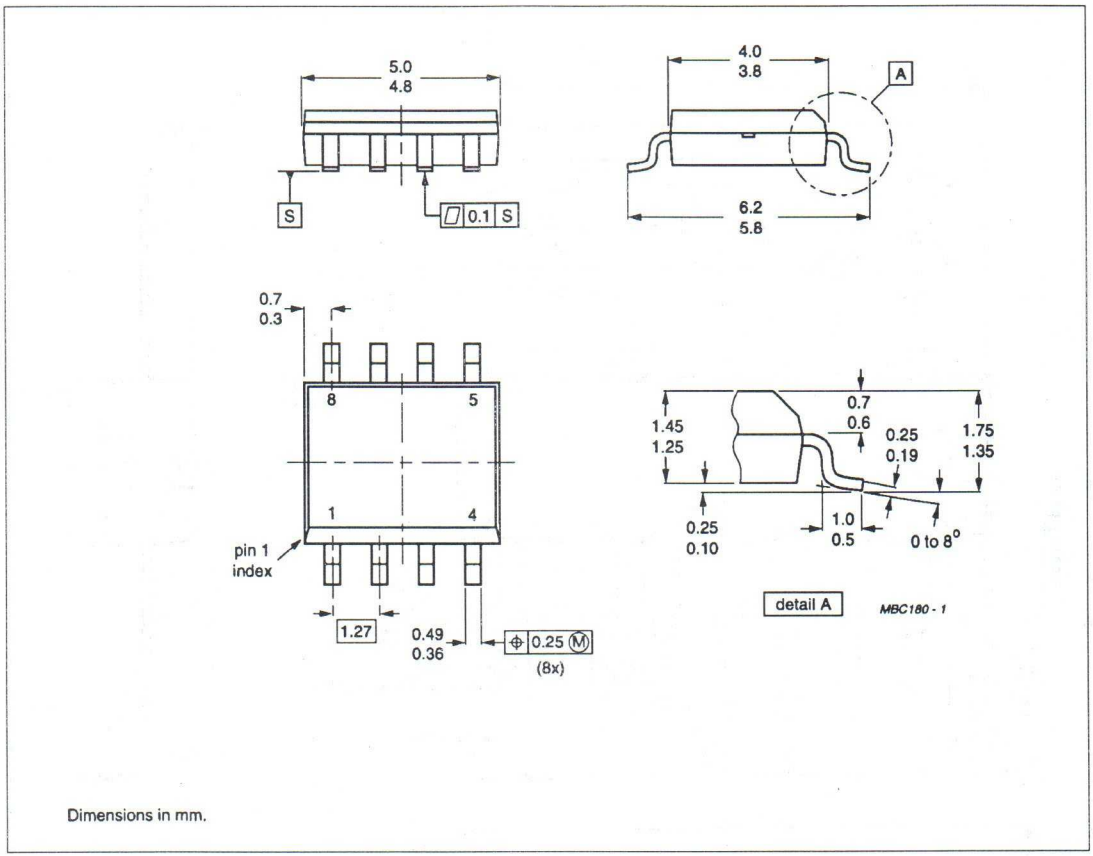
SOT97-1 PLASTIC DUAL IN-LINE PACKAGE; 8 LEADS



Dimensions in mm.

Package outlines

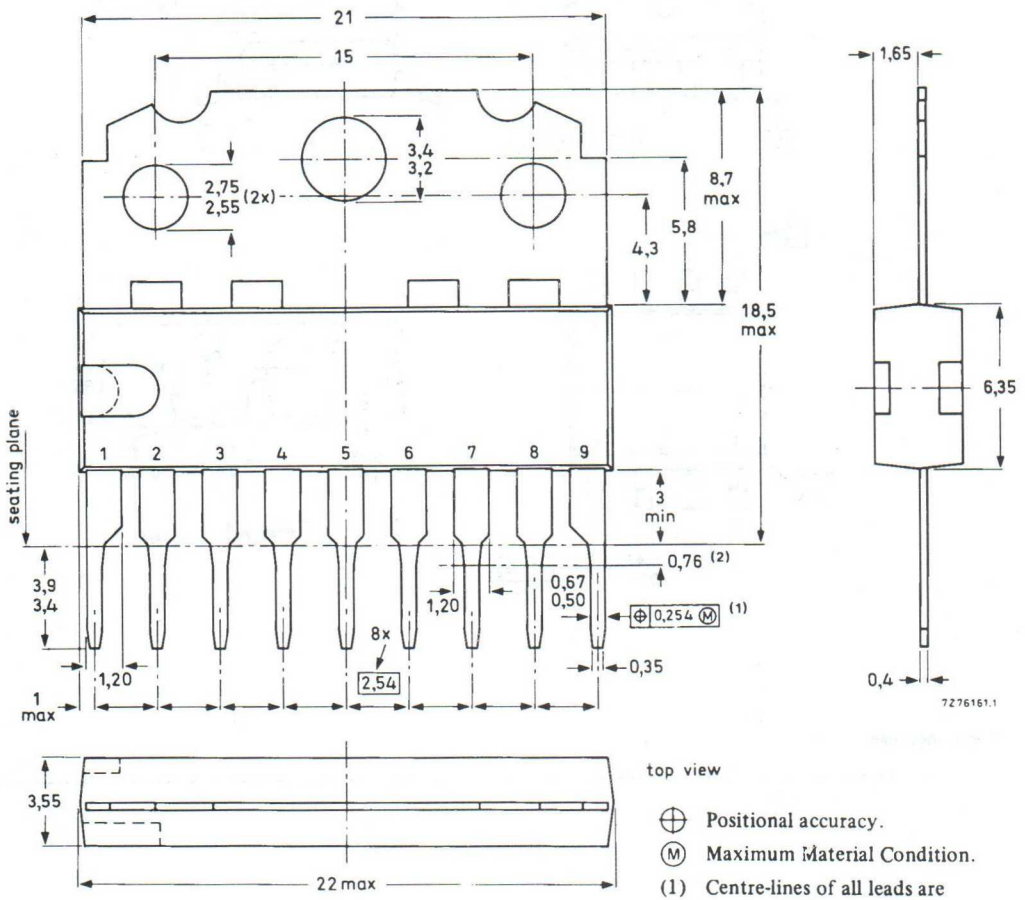
SOT96-1 PLASTIC SMALL OUTLINE PACKAGE; 8 LEADS



Dimensions in mm.

Package outlines

SOT110B 9-PIN PLASTIC SINGLE IN-LINE (U) PACKAGE



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

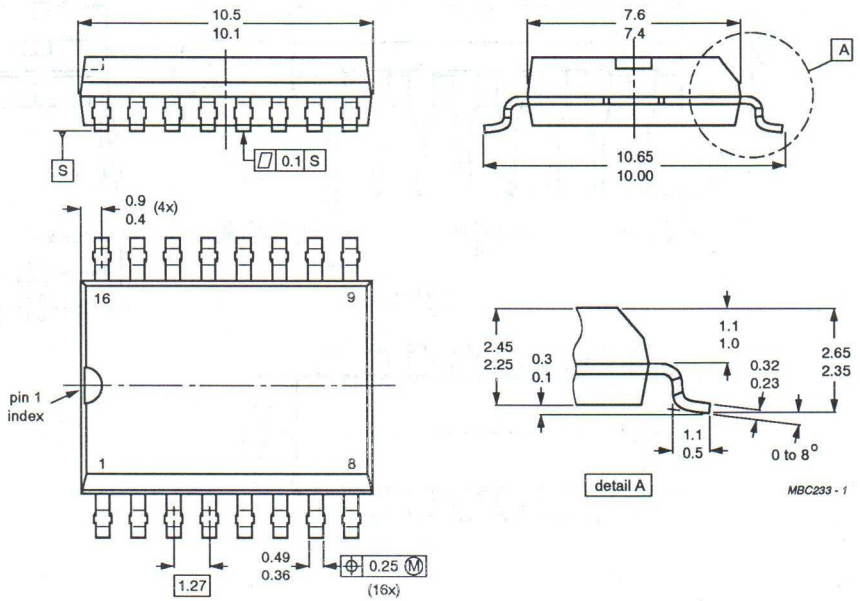
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

7Z76161.1

Package outlines

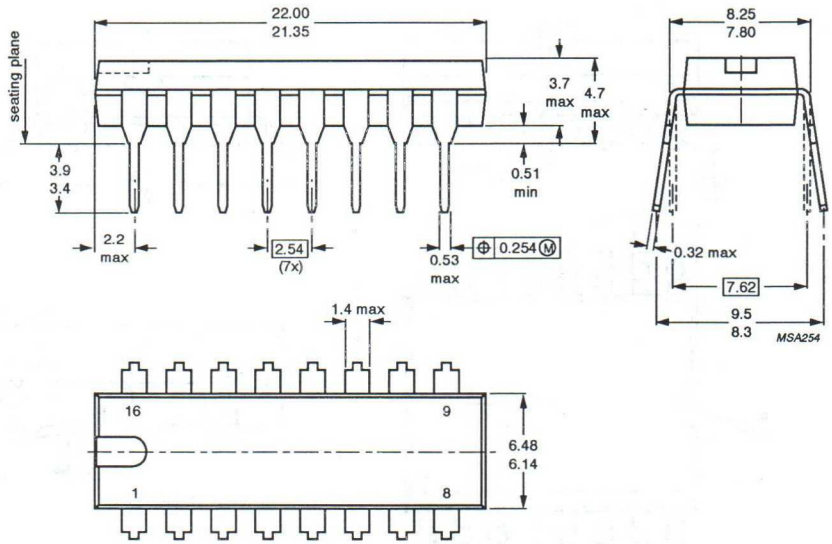
SOT162-1 PLASTIC SMALL OUTLINE PACKAGE; 16 LEADS; LARGE BODY



Dimensions in mm.

Package outlines

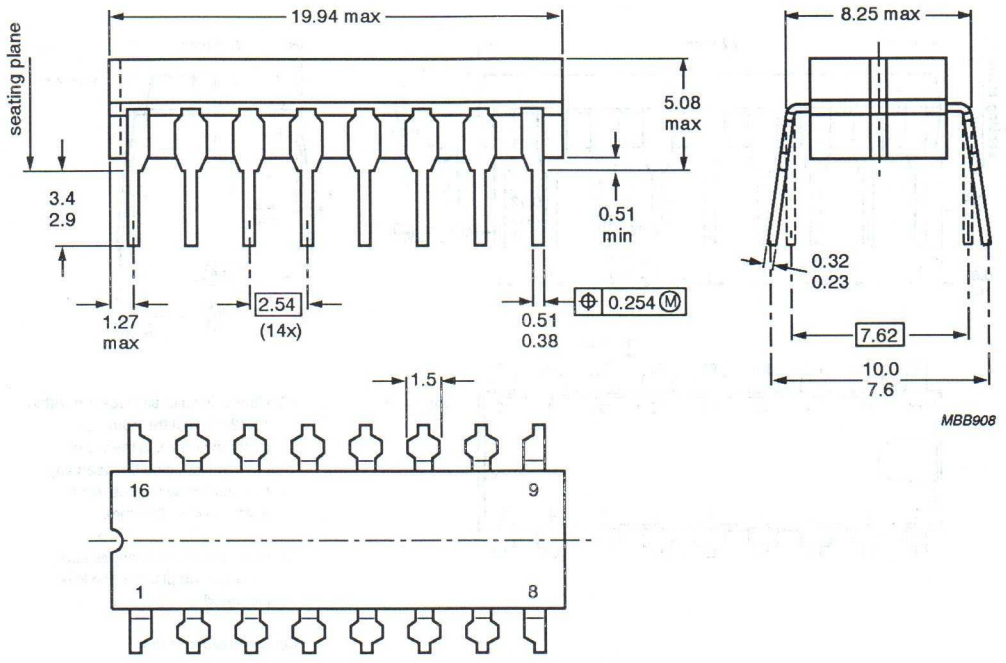
SOT38-1 PLASTIC DUAL IN-LINE PACKAGE; 16 LEADS (300 MIL)



Dimensions in mm.

Package outlines

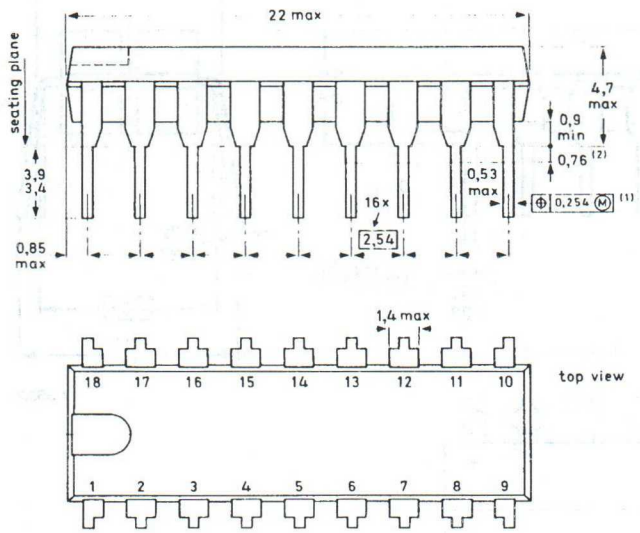
SOT74 16-LEAD DUAL IN-LINE; CERAMIC (CERDIP)

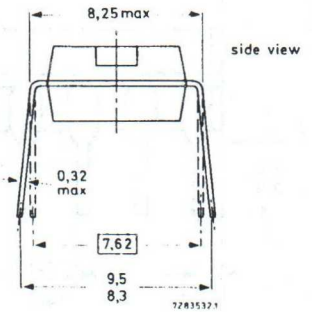


Dimensions in mm.

Package outlines

SOT102 18-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE WITH INTERNAL HEATSPREADER





(1) Centre-lines of all leads are within +0.127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

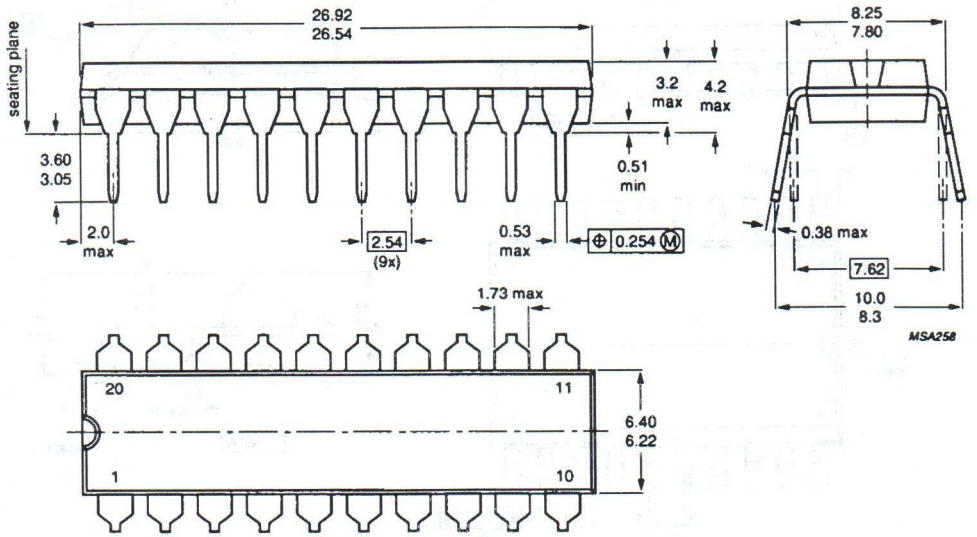
(3) Dimensions in mm.

SOT 102

7Z83532.1

Package outlines

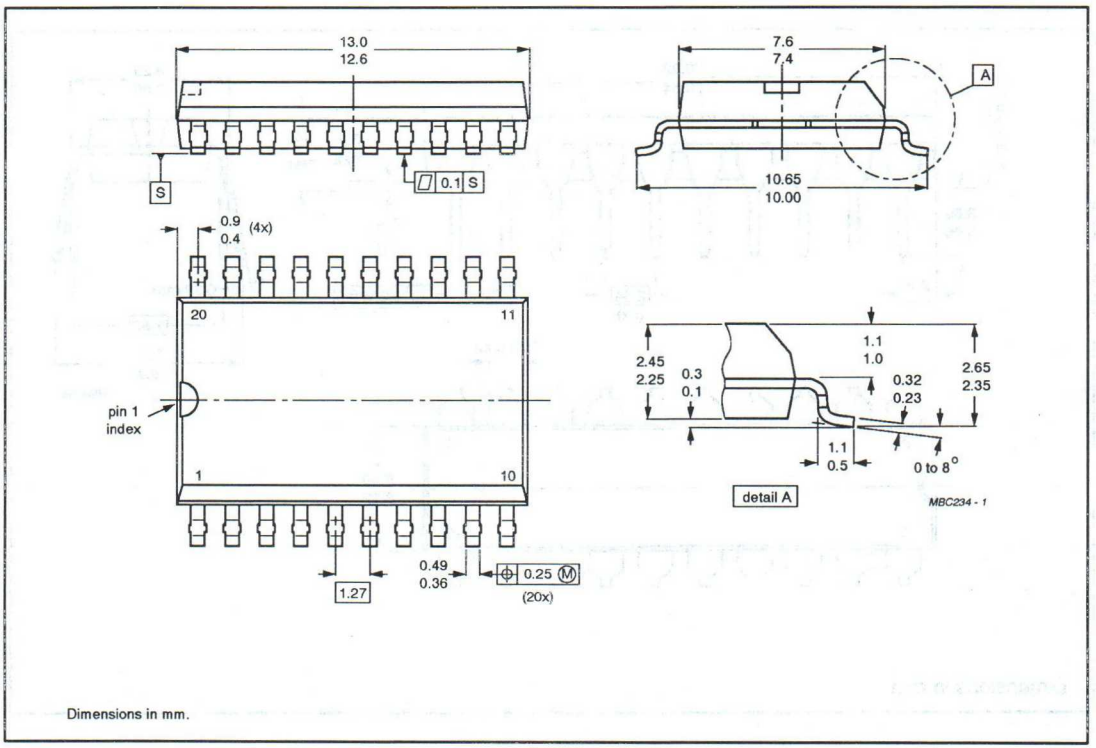
SOT146-1 PLASTIC DUAL IN-LINE PACKAGE; 20 LEADS (300 mil)



Dimensions in mm

Package outlines

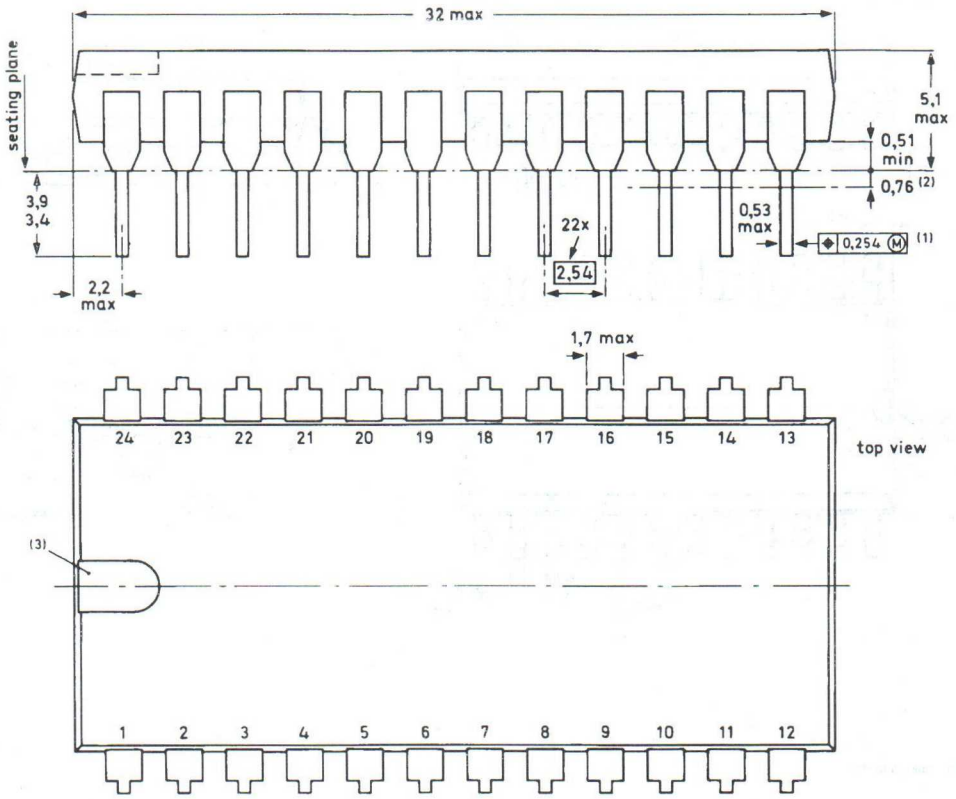
SOT163-1 PLASTIC SMALL OUTLINE PACKAGE; 20 LEADS; LARGE BODY (SO20L)

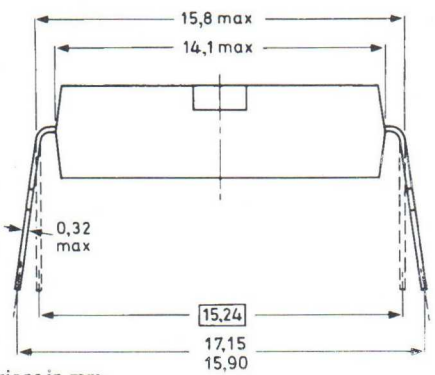


Dimensions in mm.

Package outlines

SOT101 24-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE WITH INTERNAL HEATSPREADER





side view

Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

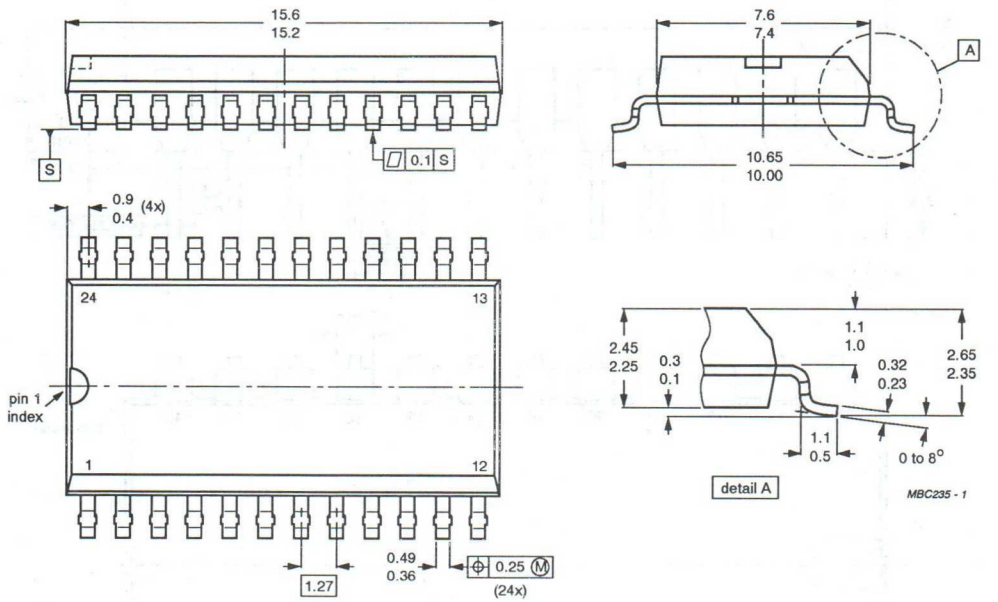
(3) Index may be horizontal as shown, or vertical.

SOT101A, B, F, G, L

7Z73670.5

Package outlines

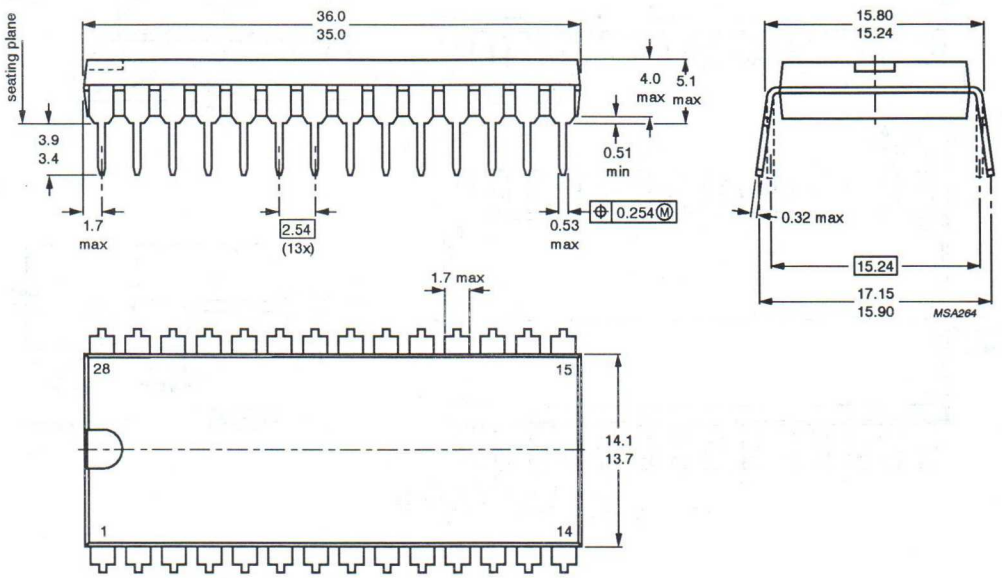
SOT137-1 PLASTIC SMALL OUTLINE PACKAGE; 24 LEADS; LARGE BODY



Dimensions in mm.

Package outlines

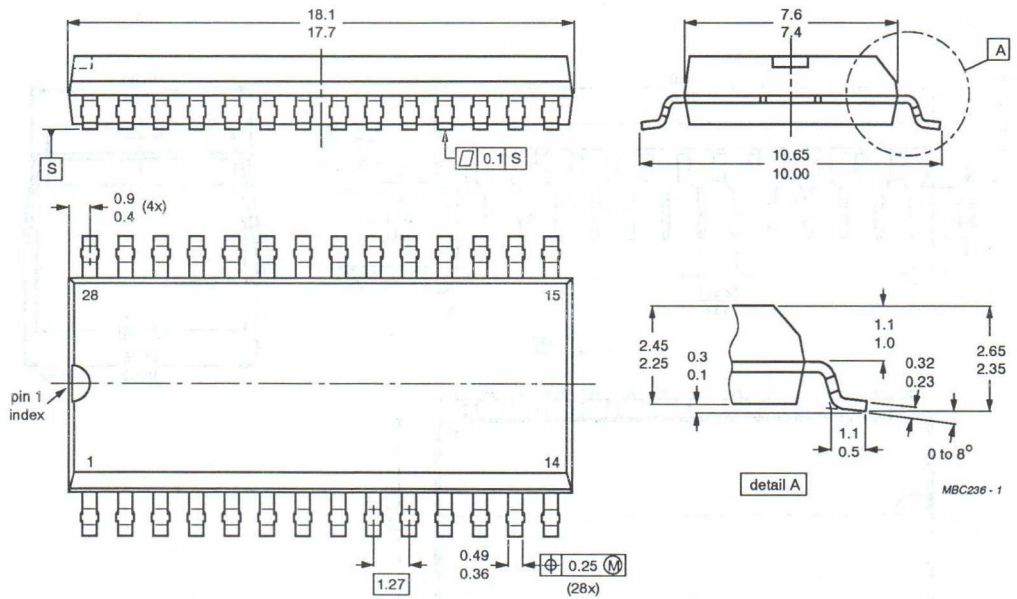
SOT117-1 PLASTIC DUAL IN-LINE PACKAGE; 28 LEADS (600 mil) WITH INTERNAL HEAT SPREADER



Dimensions in mm.

Package outlines

SOT136–1 PLASTIC SMALL OUTLINE PACKAGE; 28 LEADS; LARGE BODY

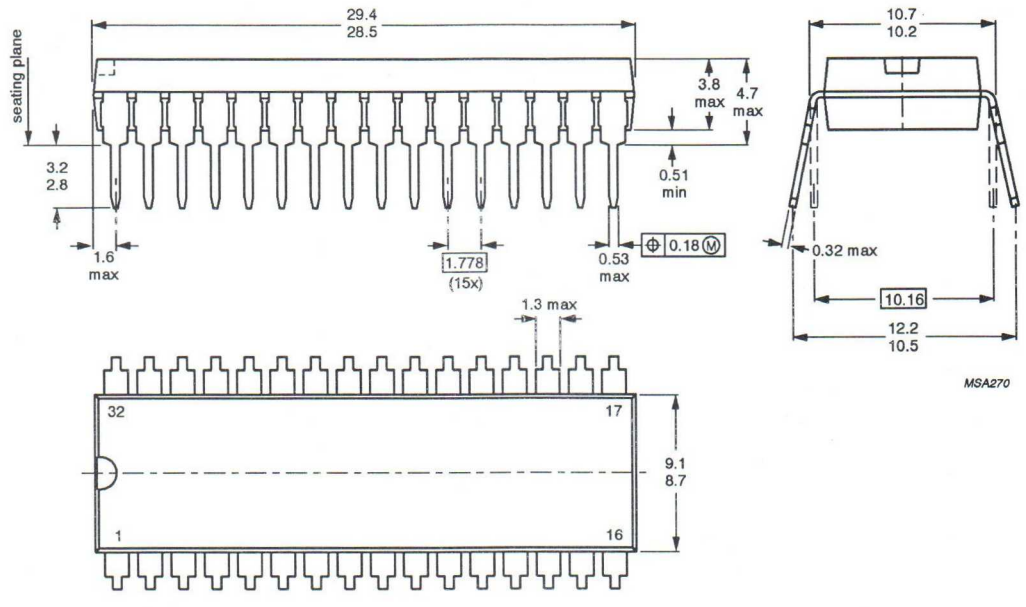


Dimensions in mm.

SOT136–1

Package outlines

SOT232-1 PLASTIC SHRINK DUAL IN-LINE PACKAGE; 32 LEADS (400 MIL)



Dimensions in mm.

Section 19
Sales offices

General Purpose/Linear ICs

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08/09/94

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Data handbook system

Appendix A

DATA HANDBOOK SYSTEM

Philips Semiconductors data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogs are available for selected product ranges (some catalogs are also on floppy discs).

Our data handbook titles are listed here.

Integrated Circuits

Book	*Title*
IC01	Semiconductors for Radio and Audio Systems
IC02	Semiconductors for Television and Video Systems
IC03	Semiconductors for Telecom Systems
IC04	CMOS HE4000B Logic Family
IC05	Advanced Low-power Schottky (ALS) Logic Series
IC06	High-speed CMOS Logic Family
IC08	100K ECL Logic Families
IC10	Memories
IC11	General-purpose/Linear ICs
IC12	Display Drivers and Microcontroller Peripherals (planned)
IC13	Programmable Logic Devices (PLD)
IC14	8048-based 8-bit Microcontrollers
IC15	FAST TTL Logic Series
IC16	ICs for Clocks and Watches
IC18	Semiconductors for In-car Electronics and General Industrial Applications (planned)
IC17	RF/Wireless Communications
IC19	Semiconductors for Datacom: LANs, UARTs, Multi-protocol Controllers and Fibre Optics
IC20	80C51-based 8-bit Microcontrollers
IC21	68000-based 16-bit Microcontrollers (planned)
IC22	ICs for Multi-media Systems (planned)
IC23	QUBiC Advanced BiCMOS Bus Interface Logic ABT, MULTIBYTE™
IC24	Low Voltage CMOS & BiCMOS Logic

Discrete Semiconductors

Book	*Title*
SC01	Diodes
SC02	Power Diodes
SC03	Thyristors and Triacs
SC04	Small-signal Transistors
SC05	Low-frequency Power Transistors and Hybrid IC Power Modules
SC06	High-voltage and Switching NPN Power Transistors
SC07	Small-signal Field-effect Transistors
SC08a	RF Power Bipolar Transistors
SC08b	RF Power MOS Transistors
SC09	RF Power Modules
SC10	Surface Mounted Semiconductors
SC13	Power MOS Transistors including TOPFETs and IGBTs
SC14	RF Wideband Transistors, Video Transistors and Modules
SC15	Microwave Transistors
SC16	Wideband Hybrid IC Modules
SC17	Semiconductor Sensors

Professional Components

PC01	High-power Klystrons and Accessories
PC06	Circulators and Isolators

MORE INFORMATION FROM PHILIPS SEMICONDUCTORS?

For more information about Philips Semiconductors data handbooks, catalogs and subscriptions contact your nearest Philips Semiconductors national organization, select from the **address list on the back cover of this handbook**. Product specialists are at your service and inquiries are answered promptly.

Data handbook system

Appendix A

OVERVIEW OF PHILIPS COMPONENTS DATA HANDBOOKS

Our sister product division, Philips Components, also has a comprehensive data handbook system to support their products. Their data handbook titles are listed here.

Display Components

Book	*Title*
DC01	Colour Display Components Colour TV Picture Tubes and Assemblies Colour Monitor Tube Assemblies
DC02	Monochrome Monitor Tubes and Deflection Units
DC03	Television Tuners, Coaxial Aerial Input Assemblies
DC05	Flyback Transformers, Mains Transformers and General-purpose FXC Assemblies

Magnetic Products

MA01	Soft Ferrites
MA03	Piezoelectric Ceramics Specialty Ferrites
MA04	Dry-reed Switches

Passive Components

PA01	Electrolytic Capacitors
PA02	Varistors, Thermistors and Sensors
PA03	Potentiometers and Switches
PA04	Variable Capacitors
PA05	Film Capacitors
PA06	Ceramic Capacitors
PA07	Quartz Crystals for Special and Industrial Applications
PA08	Fixed Resistors
PA10	Quartz Crystals for Automotive and Standard Applications
PA11	Quartz Oscillators

Professional Components

PC04	Photo Multipliers
PC05	Plumbicon Camera Tubes and Accessories
PC07	Vidicon and Newvicon Camera Tubes and Deflection Units
PC08	Image Intensifiers
PC12	Electron Multipliers

MORE INFORMATION FROM PHILIPS COMPONENTS?

For more information contact your nearest Philips Components national organizaiton shown in the following list.

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Printed in the USA

4190I/51.5M/CR1/pp1228 Date of release: 09-94

Document order number: 9398-652-67011
Document order number USA: 98-2000-100-01



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